

# **Design of Self Biased Rail-to-Rail input Operational Amplifier**

*A Thesis Submitted in partial fulfillment of the  
requirements for the award of degree of*

**Master of Technology  
in  
VLSI Design & CAD**

**Submitted by  
SUDHIR KUMAR SHARMA  
Roll. No: 60761021**

**Under guidance of  
MR. MOHD. ILIYAS  
Project Faculty SMDP II-VLSI, ECED  
Thapar University, Patiala**



**Department of Electronics and Communication Engineering**

**THAPAR UNIVERSITY**

**(Formerly Thapar Institute of Engineering & Technology)**

**PATIALA-147004, INDIA**

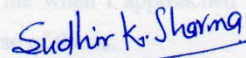
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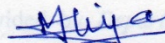
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(**Sudhir Kumar Sharma**)

This is to certify that the above statement made by the candidate is correct and true to best of my knowledge.



**Mr. MOHD. ILIYAS**

**Project faculty**

**SMDP-II VLSI, ECED**

**Thapar University**

**Patiala**



**Dr. A. K. CHATTERJEE**

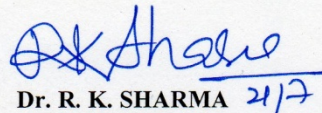
**Professor and Head**

**Electronics & Communication Engineering Department**

**Thapar University,**

**Patiala - 147004**

Counter signed by



**Dr. R. K. SHARMA 21/7**

**Dean of Academic Affairs,**

**Thapar University,**

**Patiala – 147004**

## ACKNOWLEDGEMENT

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With a deep sense of gratitude, I wish to express my sincere thanks to my supervisors, **Mr. Mohd. Ilyas, Project faculty SMDP-II VLSI**, for their immense help in planning and executing the work in time. The confidence and dynamism, with which **Mr. Mohd. Ilyas**, guided the work requires no elaboration. His company and assurance at the time of crisis would be remembered lifelong. His valuable suggestions as final words during the course of work are greatly acknowledged. What I know today about the process of research, I learned from **Mr. Mohd. Ilyas**.

My sincere thanks are due to **Prof. A. K. CHATTERJEE**, professor and head of the department, for providing me constant encouragement. I specially thank **Ms. Alpana Agarwal, Asst. Professor, ECED** for the help extended to me when I approached her and the valuable discussion that I had with her during the course of thesis.

Special thanks are due to **Mrs. Manu Bansal** and **Mr. B. K. Hemant** for extending timely help in carrying out my important works. The cooperation I received from other faculty members of this department is gratefully acknowledged. I will be failing in my duty if I do not mention the laboratory staff and administrative staff of this department for their timely help.

I acknowledge the Hardware & Software support provided by *Department of Information Technology (Govt. of India)* through project “**Special Manpower Development Program for VLSI Design & Related Software (Phase - II)**”.

I also want to thank my friends and parents, who taught me the value of hard work by their own example. I would like to share this moment of happiness with my father, mother, brother and sister. They rendered me enormous support during the whole tenure of my thesis work.

Finally, I would like to thank all whose direct and indirect support helped me completing my thesis in time.

Date:

**SUDHIR KUMAR SHARMA**  
**(60761021)**

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## LIST OF SYMBOLS

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Symbol	Quantity	Units
$\mu$	Charge carrier mobility	$\text{cm}^2/\text{Vs}$
$A_o$	DC open-loop gain	dB
$A_v$	Closed loop voltage gain	dB
B	Bandwidth	Hz
$C_{gs}$	Gate-source capacitance	f
CMRR	Common-mode rejection ratio	dB
$C_L$	Load capacitor	f
$C_{OX}$	Normalized oxide capacitance	$\text{f/m}^2$
F	Frequency	Hz
GBW	Unity gain bandwidth	Hz
$g_m$	Trans-conductance	$\Omega^{-1}$
$g_{m,n}$	Trans-conductance of n-transistor	$\Omega^{-1}$
$g_{m,p}$	Trans-conductance of p-transistor	$\Omega^{-1}$
$g_{m,T}$	Total trans-conductance	$\Omega^{-1}$
ICMR	Input common mode range	dB
$I_d$	Drains current	A
K	Boltzmann's constant	J/K
$K_p$	p-mos Process trans-conductance parameter	$\text{A/V}^2$
$K_n$	n-mos Process trans-conductance parameter	$\text{A/V}^2$
L	Channel length	m or $\mu\text{m}$
W	Channel width	m or $\mu\text{m}$
PSRR	Power Supply Rejection Ratio	dB
SNR	Signal-to-Noise Ratio	dB
SR	Slew rate	$\text{V}/\mu\text{s}$
$V_{CM}$	Common-mode input voltage	V
$V_{DD}$	Positive supply	V
$V_{DG}$	Drain to gate voltage	V
$V_{DS}$	Drain-source voltage	V
$V_{d,sat}$	Saturation voltage	V
$V_{GS}$	Gate-source voltage	V

Vsb	Source-bulk voltage	V
$V_{th}$	Thermal voltage	V
$V_{tn}$	Threshold voltage	V
$V_{tn0}$	Threshold voltage at $V_{sb}=0V$	V
Z	Impedance	$\Omega$
GND	Ground	
S-S	Slow-Slow	
S-F	Slow-Fast	
F-S	Fast-Slow	
F-F	Fast-Fast	
TSMC	Taiwan Semiconductor Manufacturing Corporation	
IC	Integrated Circuit	
ADK	ASIC Design Kit	
DRC	Design Rule Check	
LVS	Layout vs Schematic	
PEX	Post Extraction	
GDS	Graphic Data System	
LEF	Library Exchange Format	

## ABSTRACT

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Operational amplifiers use a large number of external bias voltages. These results in numerous drawbacks, namely, an area and power overhead, susceptibility of the bias lines to noise and cross-talk and high sensitivity of the bias point to process variations. Self-biased operational amplifiers are free from the above mentioned drawbacks and exhibit the same performance as existing folded casode operational amplifiers, except for a small reduction in slew rate.

This thesis work is for the development of new trend of operational amplifier. The technology is shrinking down, portability of electronic systems is gaining more important. With the technology shrinking threshold voltage is not shrinking with the same proportion. So it is useful for operational amplifier to work at any common mode level so a rail-to-rail input stage is a better choice for an operational amplifier. A rail-to-rail input common mode range is an important requirement in operational amplifiers for some applications. Conventional techniques to achieve a constant- $g_m$  rail-to-rail complementary N-P differential input stage require complex additional circuitry. In addition, the frequency response and common-mode rejection ratio (CMRR) are degraded. The technique used here in this thesis work is generating a voltage source between source terminals of both N and P differential pair, which keeps effective gate source voltage hence  $g_m$  constant over the whole rail-to-rail common mode level.

Finally, a self biased rail-to-rail input operational amplifier is designed using *TSMC 0.35  $\mu m$*  CMOS technology with a supply voltage of 3.3V. As the input common mode varies, variation in DC gain is up to 3.65dB. The power dissipation of the operational amplifier is 268.5  $\mu W$  with unity gain bandwidth 9.17MHz and phase margin of 54.94°. Further process corner simulations have been done for process variation of 15% in threshold voltage  $V_{TH}$ , oxide thickness  $t_{ox}$  and mobility  $\mu_0$ . Variation in gain in this process variation is 84.5588 dB to 86.2154 dB which is very less. And power dissipation variation from 44.549  $\mu W$  to around 1 mW.

# CHAPTER 1

## INTRODUCTION

---

With increased demand for the electronic systems, many researches have focused on the development of electronics science. This increases the complexity of the circuit. So requirement of a small simple structured basic building block exists.

This chapter discusses the background and motivation behind the self biased rail-to-rail input stage operational amplifier and ideal requirement for the input stage rail-to-rail. This chapter also discusses various applications of rail-to-rail self biased operational amplifier.

### 1.1 BACKGROUND

Since the 1960's, operational amplifiers, also referred to as op-amp, have been common tools in the world of electronics. It is a fundamental building block for many circuit designs that utilize its high gain, high input impedance, and low output impedance. Constructed from several transistors, operational amplifiers cost much less, and most integrated circuits contain several operational amplifiers on a chip. Operational amplifiers are used in many ways, including as amplifiers, filters, control, feedback, and regulation, like monitoring circuitry, cellular phones, portable devices, medical instrumentation, and solar-powered systems. However, some of these applications require an operational amplifier with rail-to-rail input stage which occupies large area. Now imagine a person carrying a huge and bulky laptop or cell phone.

With the quick improvements of computer aided design (CAD) tools, advancements of semiconductor modeling, steady miniaturization of transistor scaling, and the progress of fabrication processes, the integrated circuit market is growing rapidly. Nowadays, complementary metal-oxide semiconductor (CMOS) technology has become dominant over bipolar technology for analog circuit design in a mixed-signal system due to the industry trend of applying standard process technologies to implement both analog circuits and digital circuits on the same chip.

The operational amplifier can be used in two basic configurations: inverting and non-inverting. These configurations place different requirements on the common-mode input range. The required range varies from almost zero to a full rail to rail. A need for self bias rail-to-rail operational amplifiers, or operational amplifiers, exists for certain applications. As the technology reduces negative supply use, this reduction requires research in the

area of operational amplifier biasing. Most of the operational amplifier circuits uses many biasing voltages this results in numerous drawbacks, namely, an area and power overhead, susceptibility of the bias lines to noise and cross-talk and high sensitivity of the bias point to process variations. The proposed method of this thesis uses self biasing. Means the circuit uses the internal node voltages as the biasing voltage. This eliminates the external bias voltages and related biasing circuits. The required minimum supply voltage is only +3.3 V for 0.35 $\mu$ m CMOS technology. With this new self-biasing rail-to-rail scheme the area and power overhead, susceptibility of the bias lines to noise and cross-talk, and design time are reduced.

The key problems lie at the input stage, and the classic two stage architecture demands a rail-to-rail transconductor function with both constant  $g_m$  and limiting current, so that unity-gain bandwidth and slew rate are maintained over the full common-mode input range. Rail-to-rail input means that input signal can be anywhere between the supply voltages with all the transistors in the saturation region (and often at 100 mV or more beyond). A summing circuit has also been designed and is used to collect the input from the  $g_m$  controlled input amplifier and give a single voltage output. A high gain output stage is required produce a high gain from the circuit.

The differential amplifier is used as the input stage for operational amplifiers. The problem is that it behaves as a differential amplifier only over a limited range of common-mode input. Therefore, to make the operational amplifier versatile, its input stage should work for rail-to-rail common-mode input range. The most common method to achieve this range is to use a complementary differential amplifier at the input stage.

## **1.2 MOTIVATION**

### **1.2.1 NEED OF SELF BIASED OPERATIONAL AMPLIFIER**

In an analog circuit different active devices should be properly biased to get high performance. For instance, most of the transistors in a CMOS operational amplifier should be biased in the saturation region of operation. Usually a separate bias circuit is used to bias the transistors in an operational amplifier. The main disadvantage of using a separate bias circuit is that it requires long wires for broadcasting the bias voltages from the bias circuit to the main operational amplifier circuit. These wires not only consume a considerable amount of area but, what is worse, are also susceptible to noise and cross talk [1].

The folded cascade amplifier is a good choice as a wide-band, fast settling operational amplifier in today's deep sub-micron CMOS technology. But the folded cascade amplifier uses a large number of external bias voltages, and this result in numerous drawbacks, namely, an area and power overhead, susceptibility of the bias lines to noise and cross-talk, and high sensitivity of the bias point to process variations. In an FC amplifier each active devices should be properly biased to get high performance. For instance, most of the transistors should be biased in the saturation region of operation. But in this case determining the proper bias voltages becomes very time-consuming task. To overcome this problem self bias operational amplifier are introduced here in this thesis work.

### **1.2.2 NEED OF RAIL-TO-RAIL INPUT RANGE**

The advances in VLSI technology are forcing the supply voltages down at a rapid rate due to the constraints of transistor breakdown limits, but the threshold voltages are not scaling down in proportion. Due to this the rising concern in the analog designing world is decreasing signal headroom. Consequently, analog blocks with Rail to Rail inputs are becoming more important for mixed-signal audio and video systems designed in submicron CMOS.

A wide input common mode voltage range may be required when the amplifier is used in the voltage follower configuration or in front end circuits, where the useful input signal is superposed on comparatively high and variable common mode voltages, as occurs in some critical sensor applications.

In rail-to-rail differential input operational amplifier circuits, the common mode input voltage extends to rail-to-rail; however, the differential input voltage is very small.

### **1.2.3 TEMPERATURE VARIATION ISSUE**

One of the goals, which have characterized in this analog integrated circuit design, is the development of technologies and architectures able to operate with wide temperature range. The amplifier should work over the wide temperature range of space or Mars mission, with a temperature range wider than military standard of  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

The goal is to develop an operational amplifier that minimizes variation in key performance parameters over wide temperature range such as the Mars environment. In analog design, current biasing strategy has major impact on overall circuit performance

variation over temperature. Two popular bias techniques are constant  $g_m$  (transconductance), which is optimum for minimizing variations in small-signal performance (e.g. bandwidth), and constant  $I$  (current), which is optimum for minimizing variations in large-signal performance (e.g. slew rate) [2].

#### **1.2.4 LOW-VOLTAGE OPERATION ISSUES**

Other goal which is characterized in this analog integrated circuit design, is to able to operate with low supply voltages. Only the positive power supply is use here for circuit design. Small feature sizes and high packing densities are offered by today's VLSI technology because small dimensions result in large electrical fields and cause reliability problems. The main reasons for this interest has been the increasing need for reduced power consumption in portable electronics and in battery-operated systems and also these are most efficient when the circuitry is restricted to a single supply voltage [3].

#### **1.2.5 LOW VOLTAGE OPERATIONAL AMPLIFIERS**

The most power-hungry blocks in analog circuits are operational amplifiers. When supply is scaled down power is increased. Low noise, low offsets, high DC gain and common mode rejection ratio (CMRR) are the main requirements for Low Voltage Operational amplifiers. Operational amplifiers for low supply voltages should be able to utilize the largest possible part of the supply-voltage range for input and output signal operations in order to get the best signal-to-noise ratio [4].

#### **1.3 RAIL TO RAIL INPUT STAGE OPERATIONAL AMPLIFIER**

Requirement of rail-to-rail input stage is to maintain constant  $g_m$ , and for constant slew rate, which are again requirement for performances in wide temperature range. Constant  $g_m$  is needed to maintain the gain-bandwidth product and, hence, the small-signal behavior constant over the entire input common mode range [5, 6].

A constant slew rate is needed to maintain the large-signal response constant over the entire  $V_{Icm}$  range. Slew rate helps us to identify what is the maximum input frequency applicable to the amplifier such that the output is not distorted. To ensure a constant slew rate, the total limiting current of the input stage must be kept constant. This limiting current coincides with the sum of the biasing currents of the differential pairs in the input stage [4].

In operational amplifier design, one of the most important circuit parameters is the trans-conductance,  $g_m$ , of the input stage. In a simple rail-to-rail input stage, an N-channel differential pair and a P-channel differential pair are used in parallel. Trans-conductance of the N-channel and P-channel differential pairs, are  $g_{m-n}$  and  $g_{m-p}$ , respectively. The total input stage trans-conductance,  $g_{mT}$  of the input stage is given by the sum of the trans-conductance of the N-channel and P-channel differential pairs,  $g_{m-n}$  and  $g_{m-p}$ , respectively.

$$g_{mT} = g_{m-n} + g_{m-p} \quad (1.1)$$

There are basically three operation regions, when the common mode voltage,  $V_{CM}$ , is near the *GND* supply, only the P-channel pair operates. For  $V_{cm}$ , near the positive power supply,  $V_{DD}$ , only the N-channel pair operates. For  $V_{cm}$  around mid-rail, both differential pairs operate. That is, at least one of the two differential pairs will be operating for any  $V_{CM}$  between the rails [5, 7].

When  $V_{cm}$  is at middle of both the rail, both transistor pairs are on then there is the problem of constant  $g_{mT}$ , the variation in  $g_{mT}$  as a function of  $V_{cm}$ , can be as much as 100%. This change is not desirable because it complicates the frequency compensation of operational amplifiers and also results in harmonic distortions. When the common mode voltage moves, from one range into another, the trans-conductance of the input stage changes by a factor of two. This problem can be eliminated by using a circuit which is known as constant gm circuit. This circuit should improve improves following:

1. A differential gain and bandwidth which is independent of the input common mode voltage, results in stable phase margin and hence improves the settling time.
2. Increased CMRR.

As gm and slew rate improves circuit is also suitable for wide temperature range. Different circuit techniques for maintaining the trans-conductance ( $g_m$ ) of rail-to-rail operational amplifiers constant over the whole input common mode range have been proposed [3, 8]. Many of these techniques are based on dynamic feedback loops that limit the speed performance of the amplifier. One of the simplest techniques to improve the operational amplifier performance in this respect is keeping the sum of the gate-source voltages of the input transistors, and therefore the  $g_m$  of the input stage, constant. This overlaps the transition regions in a rail-to-rail input stage. The idea of constant gate source voltage has been recently introduced.

## 1.4 APPLICATIONS

1. **Space work:** As due to self biasing no external biasing circuit requires so it consumes less area, less power. It also shows a good performance over a wide range of temperature so circuit is suitable for space work [2].
2. **ADC drive:** To get the maximum code-output range from a conventional ADC, you need to drive its input between ground and its supply rail. This dynamic-range consideration has led to today's generation of operational amplifiers featuring rail-to-rail-output level capabilities.
3. **Comparators:** An operational amplifier has a well balanced difference input and a very high gain. The main difference between a comparator and an operational amplifier is that the operational amplifier is designed to operate in a linear region through a feedback control, while the comparator is designed to produce well-defined limit output voltages that respond quickly to changes in  $V_S$ . The parallels in the characteristics allow the operational amplifiers to serve as comparators in some functions. A standard operational amplifier operating without negative feedback can be used as a comparator.

## 1.5 ORGANIZATION OF THESIS WORK

**Chapter one** is introduction to the concept of designing self biased rail-to-rail input constant  $g_m$  operational amplifiers, keeping the sum of the gate-source voltages of the input transistors, and therefore the  $g_m$  of the input stage, constant.

**Chapter Two** is literature survey starts with explaining the basic of operational amplifier, reasons for the need of a rail-to-rail operation. Different architectures available for constant  $g_m$ , rail-to-rail architectures and their comparisons.

**Chapter Three** presents the analysis of complementary input stage and introduces the idea of gate-source voltages constant, overlapping the transition region of tail current for the N and P-pairs to achieve overall constant  $g_m$ .

**Chapter Four** presents the simulation results of the final circuit with different variation including common mode range, temperature and load. It also shows that weather the designed circuit is performing with desired specification or not. After then layout its LVS and PEX results.

**Chapter Five** presents, post layout simulation, process corner simulation and pad frame formation. In this chapter show matching of layout with schematic which is designed and also shows the performance of layout is comparable with schematic.

**Chapter six** is finally concluding chapter, analyze the circuit for further improvements, which are possible.

## CHAPTER 2 LITERATURE SURVEY

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Before going to design proposed circuit it is necessary to know about the basic terminologies of the op-amp. Here in this chapter number of common input stages for the rail-to-rail op-amp are examined and explains how the input stage design is shaped by the constraints from specifications. The related constraints are common-mode range, DC open loop gain and, input offset voltage, are the discussed in this context. The input common-mode range requirement sketches the preliminary topology of the input stage.

### 2.1 THE IDEAL OP-AMP CHARACTERISTIC [10]

1. Infinite open-loop voltage gain
2. Infinite input impedance
3. Zero output impedance
4. Zero noise contribution
5. Zero DC output offset
6. Infinite bandwidth
7. Differential inputs that stick together

#### 1. INFINITE OPEN-LOOP GAIN

- Open-Loop Gain  $A_{vol}$  is the gain of the op-amp without positive or negative feedback.
- In the ideal op-amp  $A_{vol}$  is infinite.

#### 2. INFINITE INPUT IMPEDANCE

- Input impedance is the ratio of input voltage to input current

$$Z_{in} = \frac{V_{in}}{I_{in}} \quad (2.1)$$

- When  $Z_{in}$  is infinite, the input current  $I_{in}=0$ .

#### 3. OUTPUT IMPEDANCE

- The ideal op-amp acts as a perfect internal voltage source with no internal resistance.
- This internal resistance is in series with the load, reducing the output voltage available to the load.

#### **4. NOISE CONTRIBUTION**

- In the ideal op-amp, zero noise voltage is produced internally.
- Practical op-amp is affected by several noise sources.

#### **5. OUTPUT OFFSET**

- The output offset is the output voltage of an amplifier when both inputs are grounded.
- The ideal op-amp has zero output offset, but real op-amps have some amount of output offset voltage.

#### **6. BANDWIDTH**

- The ideal op-amp will amplify all signals from DC to the all AC frequencies.
- In real op-amps, the bandwidth is rather limited.

#### **7. DIFFERENTIAL INPUTS STICK TOGETHER**

- In the ideal op-amp, a voltage applied to one input also appears at the other input.

### **2.2 SOME CONSTRAINTS FOR OP-AMP**

#### **2.2.1 INPUT COMMON-MODE RANGE**

This is simply the range of voltage that can send to the input terminals while ensuring that the op-amp behaves as expected it to do. If exceed the input voltage range, the amplifier could do some unexpected things.

#### **2.2.2 DC OPEN-LOOP GAIN**

Due to good settling accuracy open loop DC gain of op-amp limited. DC open-loop gain is one of the design goals because the op-amp has to support many applications that require large gains at low frequencies with good settling accuracy and moderate speed. Typically, the DC gain requirement is from 60 *dB* up to 100 *dB* for most of the circuits [11]. For rail to rail input op-amp the DC gain should nearly constant over the full range of CM level. The DC gain, however, has to be constant over the op-amp output voltage range in order to avoid harmonic distortion.

### 2.2.3 SETTLING TIME

The settling time of an amplifier or other output device is the time elapsed from the application of an ideal instantaneous step input to the time at which the amplifier output has entered and remained within a specified error band, usually symmetrical about the final value. Settling time includes a very brief propagation delay, plus the time required for the output to settle near to the final value, within the specified error.

The settling time consists of 30% of slewing time and 70% of linear settling time. The settling time constant  $\tau$  is given by [3].

$$\tau = \frac{C_L}{g_m} \quad (2.2)$$

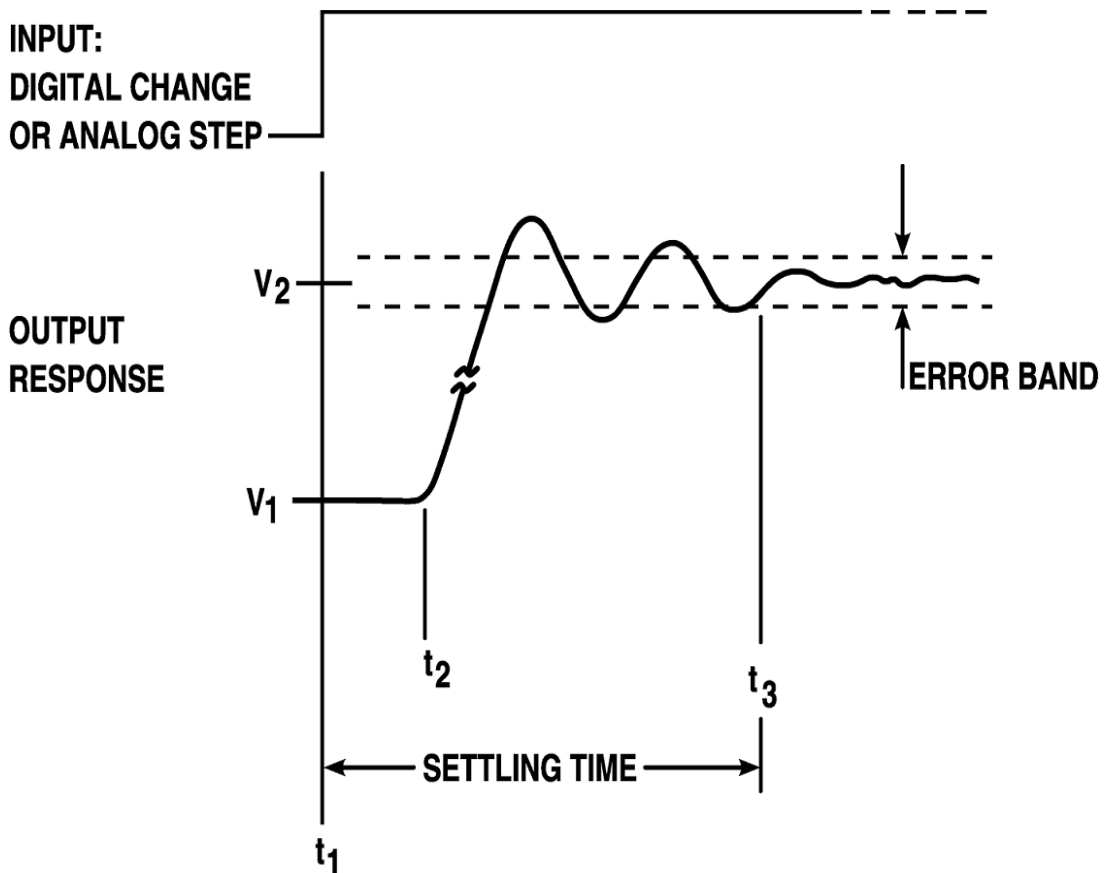


Fig 2.1 Settling time

### 2.2.4 SLEW RATE

The slew rate represents the maximum rate of change of output at any point in a circuit for all possible input signals. Limitations in slew rate capability can give rise to non linear effects in electronic amplifiers. For a sinusoidal waveform not to be subject to

slew rate limitation, the slew rate capability at all points in an amplifier must satisfy the following condition [10].

$$SR \geq 2\pi f \times V_{PK} \quad (2.3)$$

According to definition slew rate is define as:

$$SR = \max\left(\frac{dv_{out}(t)}{dt}\right) \quad (2.4)$$

If the bias current is  $I_{bias}$  and load capacitance is  $C_L$  then slew rate can also given as:

$$SR = \frac{I_{bias}}{C_L} \quad (2.5)$$

### 2.2.5 UNITY GAIN BANDWIDTH

Unity gain bandwidth (UGB) and gain bandwidth product (GBW) are similar and specifies as the frequency at which open loop DC gain of op-amp is unity [10]. Eventually, if keeping up in frequency as measuring the open-loop voltage gain of the op-amp, a frequency where the gain of the system is one. That is to say that the input is the same level as the output. Take the gain at that frequency and multiply it by the frequency (or bandwidth) the Gain Bandwidth Product will found.

$$UGB = A_D \times f_{3-dB} \quad (2.6)$$

### 2.2.6 DYNAMIC RANGE

Dynamic range is defined as:

$$DR = 10 \log\left(\frac{P_{peaksignal}}{P_{noise}}\right) \quad (2.7)$$

The peak signal power is the power of the maximum differential sinusoidal signal that does not overload the amplifier. The noise power is the total noise at the amplifier output integrated from  $1Hz$  to infinity.

### 2.3 BIASING CIRCUIT

Bias, in an electronic circuit, describes the steady state operating characteristics with no signal being applied. Bias is, strictly a DC value which is required the particular transistor in required region of operation. Most of the transistors in a CMOS op-amp should be biased in the saturation region of operation. Usually a separate bias circuit is

used to bias the transistors in an op-amp. There are many different biasing circuits. These circuits required a lot of accuracy and consume area of chip [1].

To overcome this self biasing of transistors is introduced. In this self biasing external biasing is removed and a biasing from any of the internal node, where voltage is near to the required one, is applied at the required biasing point. This self-biasing of the amplifier creates a negative-feedback loop that stabilizes the bias voltages. Any variations in processing parameters or operating conditions that shift the bias voltages away from their nominal values result in a shift in  $V_{bias}$  that corrects the bias voltages through negative feedback [9].

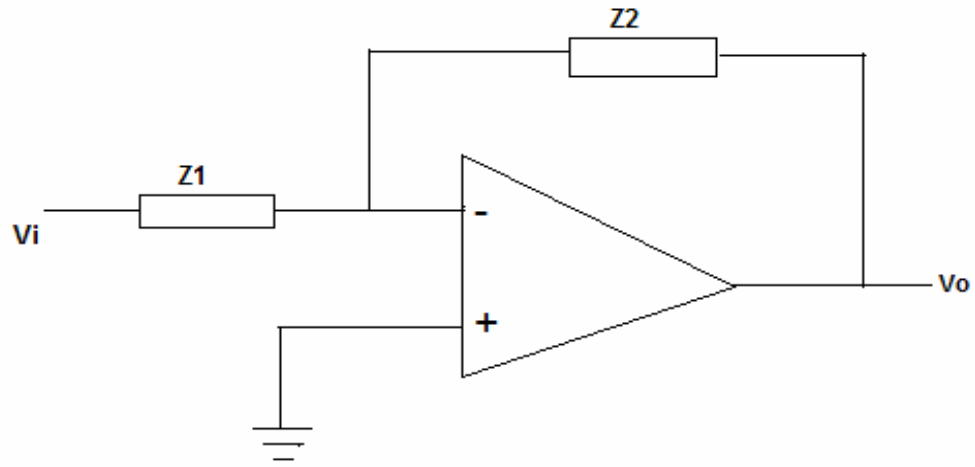
## 2.4 RAIL TO RAIL OPERATION

The op-amp is a circuit building block that can be used in many applications. Op-amps are used in conjunction with feedback networks to achieve several useful functions. There are only two main configurations: the inverting and non-inverting configurations.

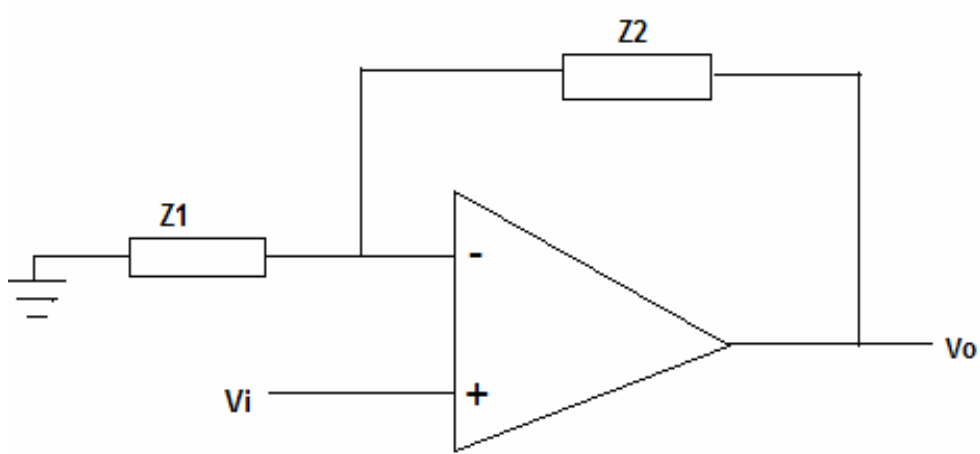
In the inverting configuration, the op-amp will keep the two input nodes at the same voltage. Since the positive terminal is connected to ground, the non-inverting terminal will have the same voltage. Regardless of the changes of the input voltage  $V_i$ , both op-amp terminals will be approximately the same and equal ground potential. Therefore, the op-amp needs almost zero common mode input range.

In the non-inverting configuration, the op-amp will keep the two input nodes at the same voltage. Since the positive terminal is connected to the input voltage, it will have large variations. The inverting terminal must follow these variations.

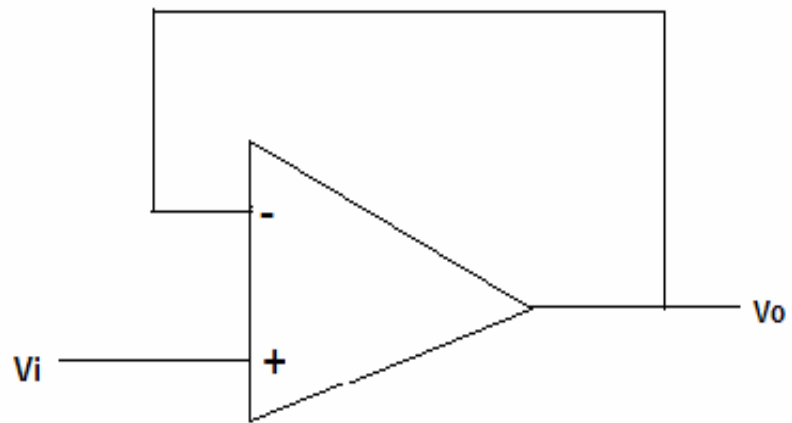
A special case of the non-inverting configuration is the voltage follower shown in Fig 2.2(c). This configuration will have the most constraint requirement for the common mode input range. Similar to the non-inverting configuration, the allowable variation (input swing) is determined by the output voltage and feedback network. But, since the feedback is unity, it is only determined by the output voltage swing. If the op-amp output stage is capable of rail to rail operation, then the common mode input range should be rail to rail [12]. So clear that to design a versatile op-amp that is useful for any configuration; its input stage should have a rail to rail input common mode range capability.



(a)



(b)



(c)

**Fig 2.2 Op-amp in (a) inverting configuration (b) non-inverting configuration (c) voltage follower**

## 2.5 CONSTANT- $g_m$ , RAIL-TO-RAIL INPUT STAGE

### 2.5.1 INPUT STAGE FOR OP-AMP

Op-amp having input terminal that can swing from one power supply rail to the other rail obviously makes any circuit more attractive. In these op-amps, an N-channel differential pair and a P-channel differential pair are used in parallel [13].

#### 2.5.1(A) NMOS INPUT STAGE

Diagram, used to analyze the high common mode input range of the NMOS differential input stage is shown in Fig 2.3. This is sufficient for the purpose of illustration. The range extends from the positive supply to  $(V_{gs,n} + V_{Dsat})$  above the negative supply. This minimum voltage is needed to keep the NMOS differential pair and the tail current source in saturation [12].

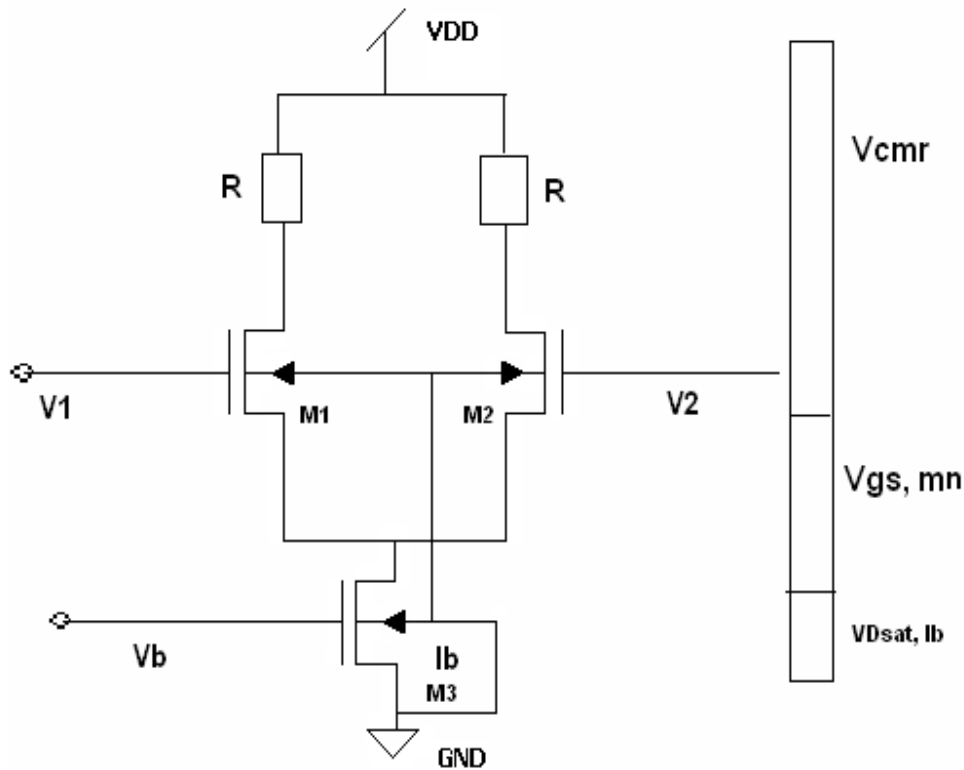


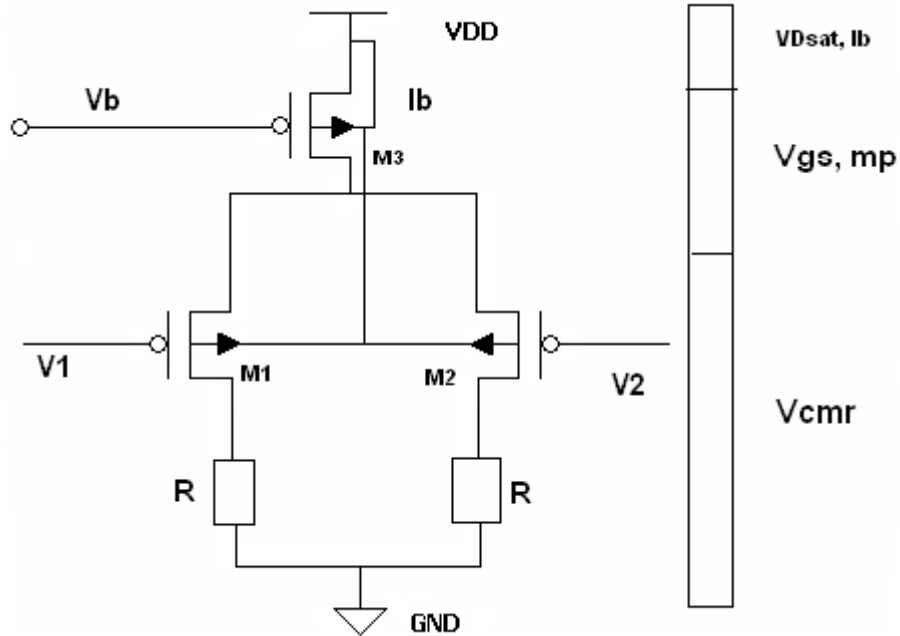
Fig 2.3 NMOS differential pair common mode input range

#### 2.5.1(B) PMOS INPUT STAGE

Another input stage is P-MOS input pair. Diagram, used to analyze the low common mode input range of the NMOS differential input stage is shown in Fig 2.4. The

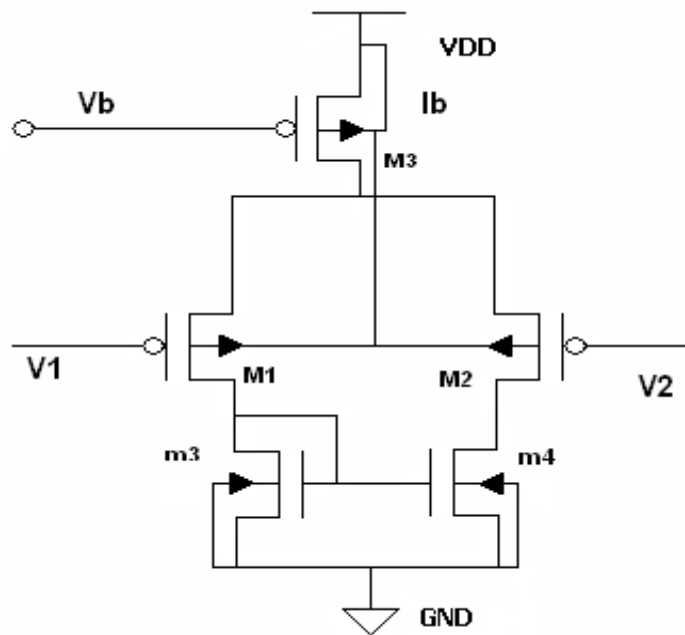
minimum voltage is needed to keep the PMOS differential pair and the tail current source in saturation is given by (2.8).

$$V_{in,CM} = V_{DD} - V_{gs,1} - V_{gs,3} \quad (2.8)$$



**Fig 2.4 PMOS differential pair common mode input range**

In case of practical circuits instead of using a load a current mirror is used as a load.

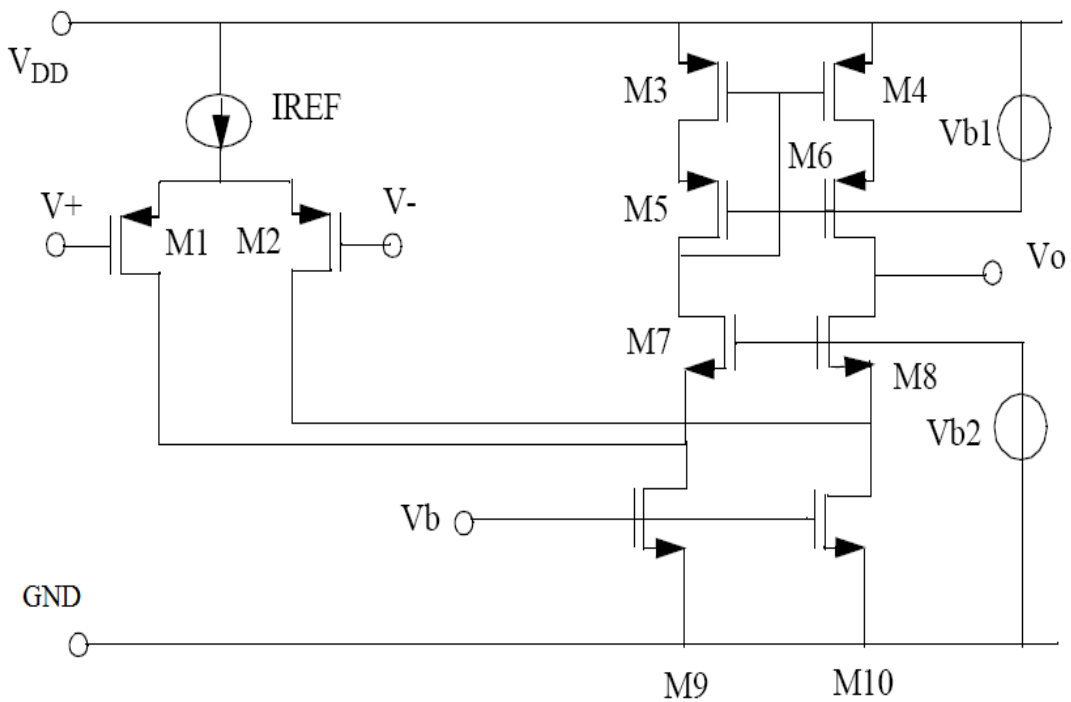


**Fig 2.5 Single differential input pair with a current mirror as a load**

This input stage consists of a P-channel differential pair M1-M2 and a current mirror M3-M4, providing a differential to single ended conversion. This current mirror load drastically reduces the common-mode input range, because the drain voltage of M3 can only reach the negative supply rail within one gate-source voltage. Suppose the common mode input voltage decreases. As a result of this, the current mirror will finally push M1 out of saturation. This yields a common mode input voltage range which is limited to:

$$V_{gs,n} + V_{T,p} < V_{common} < V_{DD} - V_{sg,p} - V_{d,sat} \quad (2.9)$$

The folded cascode input stage, as shown in Fig 2.6, overcomes this problem.



**Fig 2.6 Folded Cascode Input Stage**

The operation of the folded cascode stage can be described briefly as follows; the input stage consists of a P-channel differential pair M1-M2; the folded cascodes M7-M8 provide a level shift function; current mirror M3-M6, providing differential to single ended conversion; M9-M10 function as bias current sources (in order to maximize the output current of the input stage these current sources are biased at the same values as the tail current  $I_{REF}$ ).

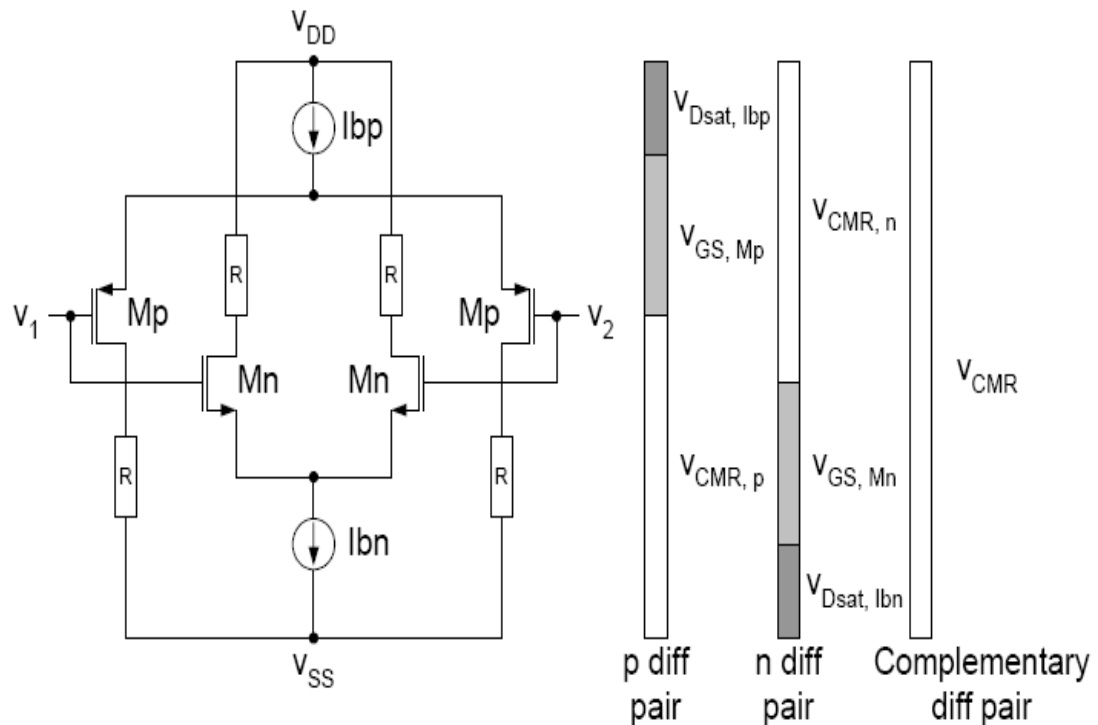
An important parameter of the folded cascode input stage is the input referred offset voltage. The most significant mismatches that give rise to offset are those of

threshold voltages,  $V_T$ , and those of trans-conductance factor. The offset of the folded cascode input stage can be minimized by making:

- The area of the transistors as large as possible.
- The effective gate source voltage of the input transistors as small as possible.
- The  $W/L$  ratio of the current mirror and the current sources as small as possible.

## 2.5.2 RAIL-TO-RAIL INPUT STAGE

The input stage of an amplifier intended for use in a voltage follower configuration has to have a common mode input range which extends from rail to rail. In order to achieve this, an N-channel and a P-channel input pair can be placed in parallel, as shown in Fig 2.7 [12].



**Fig 2.7 Complementary differential pair common mode input range**

This technique enables the input stage to operate rail-to-rail. There are basically three operation regions [7]:

**Region I:** When  $V_{CM}$  is close to the ground rail, only P-channel pair operates. The N-channel pair is off because its  $V_{GS}$  is less than  $V_T$ . The total trans-conductance of the differential pair is given by (2.8)

$$g_{mT} = g_{mp} \quad (2.8)$$

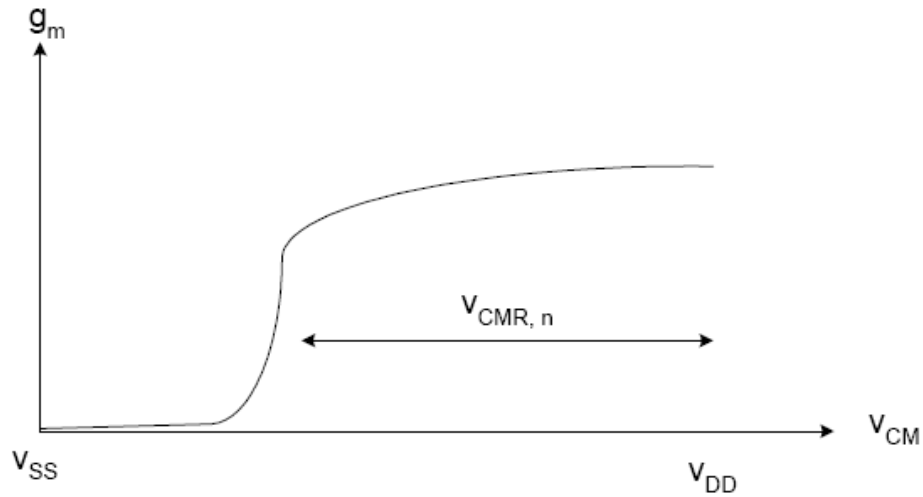
**Region II:** When  $V_{CM}$  is in the middle range, both of the P-and N-pairs operate. The total trans-conductance is given by

$$g_{mT} = g_{mn} + g_{mp} \quad (2.9)$$

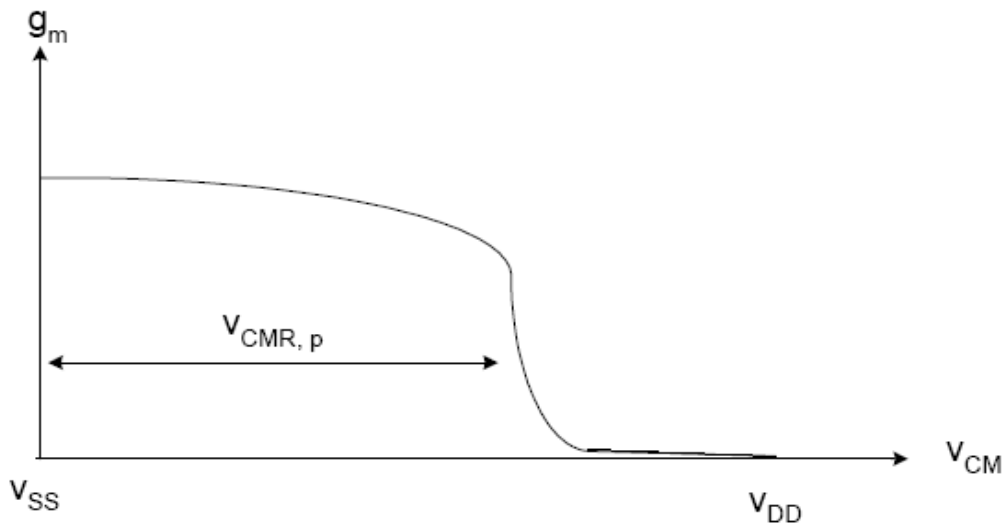
**Region III:** When  $V_{CM}$  is close to the positive rail, only N-channel pair operates. The total trans-conductance is given by

$$g_{mT} = g_{mn} \quad (2.10)$$

To understand the effect, we will investigate how the trans-conductance of each pair and of the complementary pair changes with common mode input signal. First the trans-conductance versus input common mode of the NMOS pair is shown in Fig 2.8

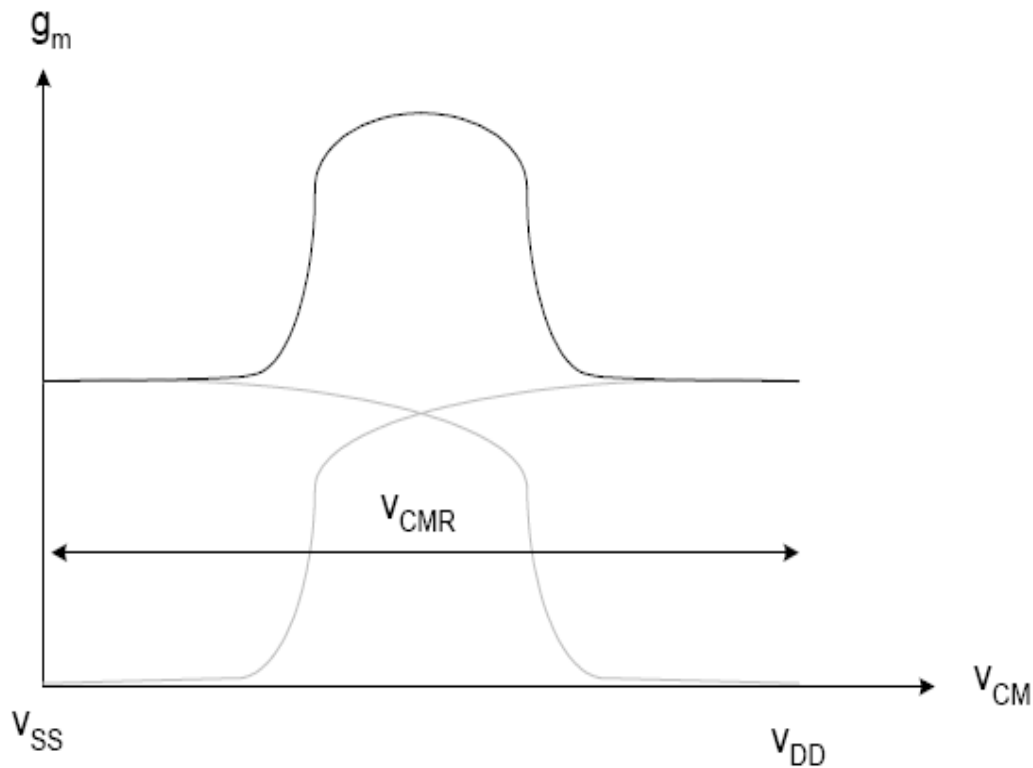


**Fig 2.8 NMOS differential pair trans-conductance versus input common mode**



**Fig 2.9 PMOS differential pair trans-conductance versus input common mode**

In the same manner, the trans-conductance versus input common mode of the PMOS pair is shown in Fig 2.9. Trans-conductance of each pair is almost constant over its common mode range and drops to zero outside this range. Combining these two graphs gives the trans-conductance versus input common mode of the complementary pair as shown in Fig 2.10. It is assumed here that both pairs in the complementary structure had been sized appropriately to obtain equal trans-conductance in their region of operation.



**Fig 2.10 Complementary differential pair trans-conductance versus input common mode**

The trans-conductance of the complementary differential pair ( $g_{m,T}$ ) is almost constant for high or low common mode input when only one of the pairs is active. In the middle region, both pairs are on and the effective trans-conductance is twice that of the other regions. This in turn causes an undesired additional distortion. The large variations in the trans-conductance will result in a suboptimal op-amp design with the complementary differential pair used as the input stage. In op-amps, the distortion will be significantly reduced when the feedback network is added to the amplifier. Therefore, this effect is not usually an issue. By applying self biasing a small feedback is provided which neglect this variation in trans-conductance up to a limit. More methods for reducing the trans-conductance variation are given in 2.5.3.

### 2.5.3 CONSTANT TRANS-CONDUCTANCE CIRCUIT

This is perhaps the most crucial stage of the design as this stage determines the correct functionality of the design in the Rail to Rail configuration. The key issue here is that this stage should ideally have both a constant  $g_m$  and a limiting current so that the unity gain bandwidth and the slew rate are both maintained over the full common mode input range. But this technique suffers from two drawbacks. First, at the extreme input ranges, only one input pairs is active and so the effective trans-conductance is halved. Second, the large signal output current is also halved. Stabilization of the total  $g_m$  over the common mode range can be by different ways. Assuming all transistors are in the saturation region and using the square law models, the complementary differential pair trans-conductance is given by:

$$g_{mT} = g_{mn} + g_{mp} \quad (2.11)$$

$$g_{mT} = \sqrt{\mu_n C_{ox} \left(\frac{w}{l}\right)_n I_n} + \sqrt{\mu_p C_{ox} \left(\frac{w}{l}\right)_p I_p} \quad (2.12)$$

Or from a voltage point of view

$$g_{mT} = \mu_n C_{ox} \left(\frac{w}{l}\right)_n V_{eff,n} + \mu_p C_{ox} \left(\frac{w}{l}\right)_p V_{eff,p} \quad (2.13)$$

By examining the above formula's it can be suggested how to keep  $g_{mT}$  constant. It can be controlled by changing the tail currents of the input transistors.  $g_{mT}$  can be controlled by either changing the tail currents, the gate source voltages or the  $W/L$  ratios.

An ideal constant- $g_m$  technique must be robust and universal. By the term robust, we mean that the accuracy of the circuit in maintaining the total amplifier trans-conductance constant does not rely on any precise matching between the N-channel and the P-channel transistors of the complementary input pairs (*i.e.*, on scaling their geometries to compensate for the mobility difference between electrons and holes). By the term universal, we mean that the accuracy is independent of the type and the operation region of the input transistors. This implies that the technique is valid for any  $g_m/ID$  characteristic of the amplifier input devices and is, therefore, compatible with modern submicron CMOS devices, in which the voltage-to-current square law in saturation region is not completely satisfied.

### 2.5.3(A) TAIL CURRENT CONTROL, CONSTANT $g_m$ METHOD

In the equation 2.12 if we take taking the square root term constant.

$$\sqrt{\mu_n C_{ox} \left(\frac{w}{l}\right)_n} = \sqrt{\mu_p C_{ox} \left(\frac{w}{l}\right)_p} = K \quad (2.14)$$

Equation 2.12 can also be written as

$$g_{mT} = K(\sqrt{I_n} + \sqrt{I_p}) \quad (2.15)$$

Then by keeping  $(\sqrt{I_n} + \sqrt{I_p})$  as constant  $g_{mT}$  can be controlled [5]. The disadvantage of this design is its relative complexity. Also, it is not very accurate since it uses the square law models of the MOS transistors and for today's deep submicron technology; there is a significant deviation from the ideal relation.

Another method that uses tail current to maintain constant  $g_{mT}$  can be understood by putting another condition  $(\sqrt{I_n} = \sqrt{I_p} = \sqrt{I})$ , therefore (2.15) becomes:

$$g_{mT} = 2K\sqrt{I} \quad (2.16)$$

However,  $g_{mT}$  is only half the value given in (2.16) when only one differential pair is operating because  $I$  is half. Therefore, in the regions where one pair is working, an increase in the tail current by a factor of 4 will keep  $g_{mT}$  constant. This can be implemented by diverting the tail current of the non working pair to the working pair after multiplying by a factor of 3. The multiplication by 3 can be accomplished by using a three-time current mirror. The disadvantage of this technique is the limited accuracy due to ideal square law dependence (2.16). Also, the transition between the three regions is not well controlled and will cause variations in  $g_{mT}$  [14].

### 2.5.3(B) ASPECT RATIO CONTROL, CONSTANT $g_m$ METHOD

From the equations (2.12) and (2.13) there possibility of controlling  $g_{mT}$  by controlling the aspect ratio of one or both differential pairs. One method for implementing this is by using a second NMOS and a second PMOS differential pairs in standby that are connected in parallel to the complementary differential pair. In the middle region of operation, both pairs in the complementary differential pair are operating and the other two pairs are off.

Let's start with the input common mode voltage in the middle region and going down towards  $GND$ . When the voltage becomes low enough for the PMOS pair to turn off, the other NMOS differential pair will be activated. Effectively, doubling the aspect ratio for low common mode input, therefore,  $g_{mT}$  is constant. The same happens if the voltage increases towards  $V_{DD}$ , the second PMOS differential pair will be activated and the effective aspect ratio is doubled to keep  $g_{mT}$  constant. The disadvantage of this technique is that in the transition between the three regions results in a non-smooth current transition. This causes relatively large variations in  $g_{mT}$  which results in a suboptimal performance.

The aspect ratio control method was used in [15] and 20%  $g_{mT}$  variations was achieved.

### 2.5.3(C) VOLTAGE CONTROL, CONSTANT $g_m$ METHOD

Form equations (2.13), (2.14) we can simplify a new expression which come as:

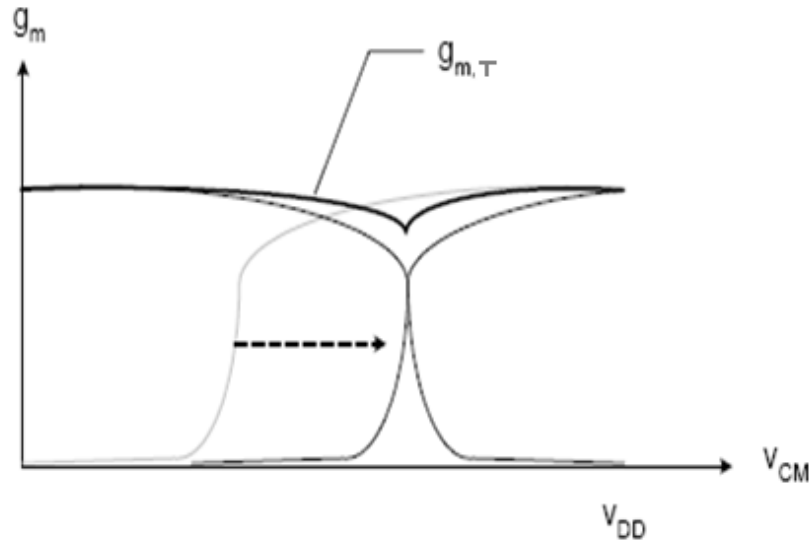
$$g_{mT} = K^2 (V_{gs,n} + V_{sg,p} - V_{th,n} - |V_{th,p}|) \quad (2.17)$$

So to keep  $g_{mT}$  constant, we have to keep  $(V_{gs,n} + V_{sg,p})$  constant. This can be done by connecting a voltage source between the common source of the N-MOS and the common source of the P-MOS differential pairs. This will keep both pairs working for all common mode input voltage. MOS transistors are used for this configuration and sizing them appropriately. The disadvantage of this technique is that the behavior of the transistors is a function of the voltage at input. Therefore,  $g_{mT}$  still has some variations over the common mode input range.

The constant  $(V_{gs,n} + V_{sg,p})$  method was used in [16], 7.5% and 15%  $g_{mT}$  variations was achieved. To overcome its disadvantage input signal is applied at this circuit.

### 2.5.3(D) CONSTANT $g_m$ BY LEVEL SHIFTING

Another method uses DC level shifting. The principle of operation is to shift the trans-conductance characteristics curve of the PMOS differential pair to the left or the trans-conductance characteristics curve of the NMOS differential pair to the right such that the sum of  $g_{mn}$  and  $g_{mp}$  is constant. This can be accomplished simply by applying a DC level shift to the PMOS pair (or NMOS pair) to make its turn on voltage lower (or higher). The principle is illustrated in Fig 2.11 for PMOS shift.



**Fig2.11 DC level shifting**

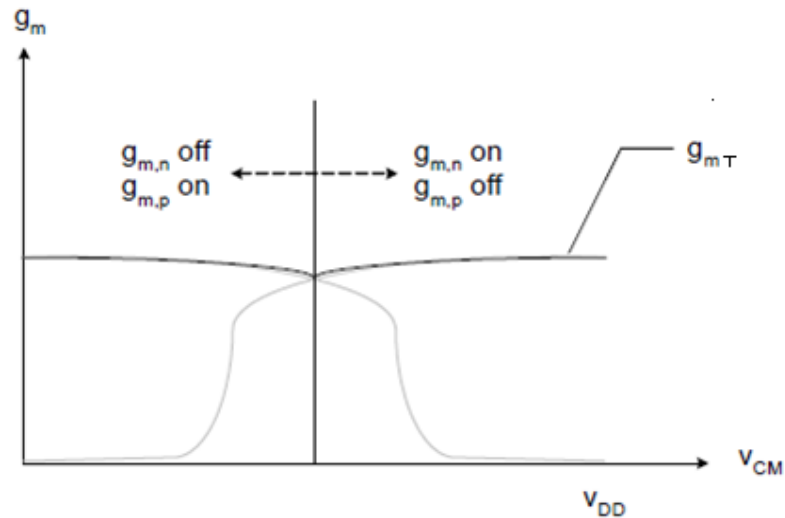
The idea of level shifting to achieve constant  $g_m$  was reported [3]. The transition region (i.e. the  $V_{i,CM}$  range where its tail current source operates in the triode) of the P-channel input differential pair is shifted up by DC level shifters to overlap with that of the N pair. Two P source followers are used as DC level shifters in [3]. It has very good constant behavior ( $\pm 4\%$  deviation) but also a major limitation: there is a need to manually tune the bias currents of the input DC level shifters

This technique accomplishes all of the necessary features of an ideal rail-to-rail input stage except that the measured  $g_m$  deviation exceeds  $\pm 4\%$ . Very small  $g_m$  and SR variations (within  $\pm 5\%$ ) can be achieved using this technique if the DC shift level is tuned carefully. It is worth noting that circuits designed using level shifting techniques are sensitive to  $V_T$  and power supply voltage variations and mismatch between N and P input pairs.

The disadvantage of this method is its need for tuning. Because the characteristics will vary with process, voltage, and temperature, the optimal DC level will change. If the shift level is not tuned, large or small  $g_{mT}$  will appear around the transition region, therefore, instability might occur. Here in the circuit is tuned by applying the input in tuned constant  $g_m$  circuit. This method was used in [3] and achieves 13%  $g_{mT}$  variations before tuning and 5%  $g_{mT}$  variations after tuning.

### 2.5.3(E) CONSTANT $g_m$ BY MAXIMUM/MINIMUM CURRENT SELECTION

In this method utilizes a maximum selection circuit. The principle of operation is to allow only one pair to operate in the middle region. This can be done by keeping the differential pair that has the larger tail current operating and turn the other differential pair off. The scheme assumes that the differential pair with larger tail current is operating properly while the other pair is going into (or just coming out of) triode region. The principle is illustrated in Fig 2.12 for NMOS shift.



**Fig 2.12 Selecting maximum  $g_m$**

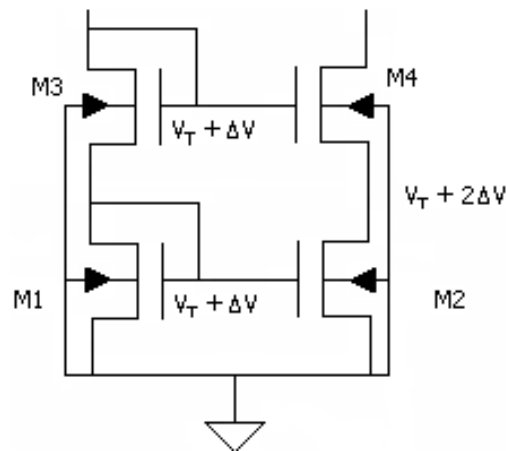
The maximum/minimum current selection technique provides better constant- $g_m$  behavior (5% in [17] and 6% in [15]) than technique used for constant  $g_m$  using variable tail current. As only the largest signal current is chosen, the SR is kept constant. In addition, this technique can work for all operation regions of input MOS transistors. However, the transient settling behavior of this technique is imperfect because the current selection circuit may present open loop high impedance nodes [18], preventing high-speed operation.

The disadvantage of this design is its relative complexity. This method was used in [17] and [19] which achieve 5%  $g_{mT}$  variations.

## 2.6 OUTPUT STAGE

The main purpose of the output stage of an op-amp is to deliver a certain amount of signal power into a load with acceptably low levels of signal distortion. In a low voltage, low-power environment, this has to be achieved by efficiently using the supply voltage as well as the supply current [20]. The output stage of the circuit works as summing circuit, biasing circuit, and load for cascade input. So this is also one the most important stage of the circuit.

Fig 2.13 shows an N-MOS cascode current mirror which works half the output stage [21]. Rest half stage is formed by P-MOS in the same manner.



**Fig 2.13 Cascode current mirror**

The voltage drop across M1 and M3 can be described as

$$V_{gs1} + V_{gs3} = 2(V_T + \Delta V) \quad (2.18)$$

Where

$$\Delta V = \sqrt{\frac{2I_{D1}}{\beta}} \quad (2.19)$$

The maximum output voltage of cascade current mirror is typically 1.5V. So the output voltage swings are limited to 1.5 V around.

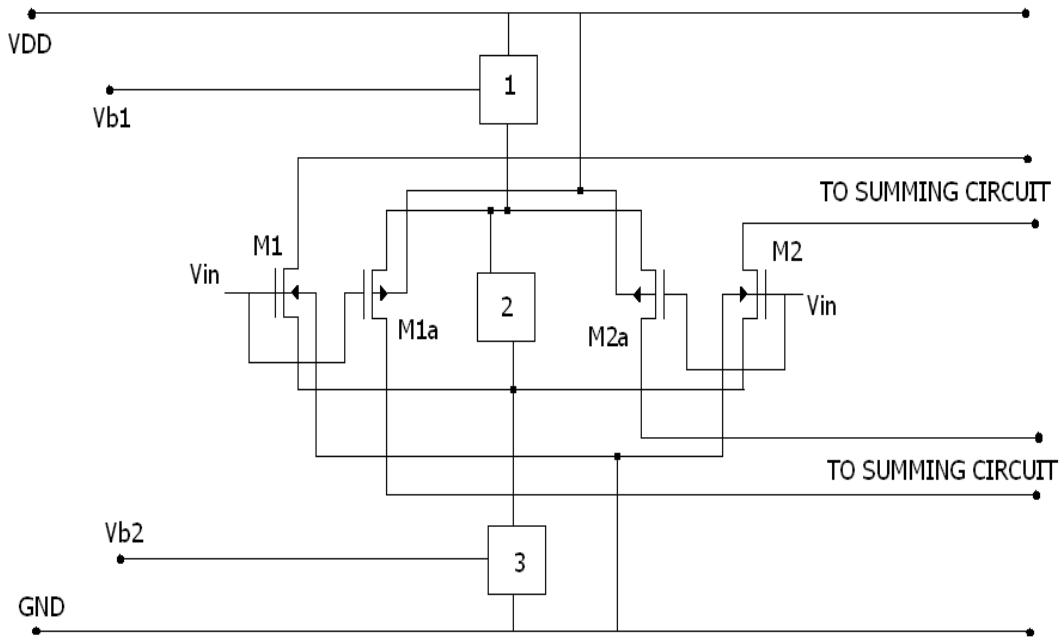
**CHAPTER 3**  
**DESIGN OF SELF BIAS RAIL-TO-RAIL INPUT OPERATIONAL AMPLIFIER**

---

In chapter 2, section 2.5.3, different constant  $g_m$  topologies are discussed these topologies giving an idea to move towards objective of this dissertation. From that discussion we chose the topology of Voltage control, constant  $g_m$  method.

**3.1 INTRODUCTION**

As different constant  $g_m$  topologies are discussed in last chapter an immediate and simple technique for reducing the variations in the small-signal response of rail-to-rail input stages consists in connecting a voltage source between the common source of the N-MOS and the common source of the P-MOS differential pairs. Indeed, with this approach, provided that the two differential pairs are perfectly matched, variations in the total amplifier trans-conductance can only arise in the common transition region of the two pairs, and are much lower with respect to the traditional composite rail-to-rail input stages. The constant  $g_m$  can be achieved by keeping the gate source voltage.



**Fig 3.1 Rail-to-rail CMOS amplifier input stage**

In order to obtain a constant  $g_m$ , the voltage of block 2 of Fig 3.1 should be

$$V_{ref} = -V_{Tp} + V_{Tn} + 2K_{gs.ref} \quad (3.1)$$

Where  $V_{TN}$  and  $V_{TP}$ , are the threshold voltages for P-channel and an N-channel transistor, respectively.  $V_{gs,ref}$  is the effective gate-source voltage of an input transistor biased at  $4I_{ref}$ , i.e., a gate-source voltage,  $V_{gs}$  minus a threshold voltage,  $V_T$  [16]. The subscripts P and N refer to a P-channel and an N-channel transistor, respectively. The factor  $K$  is the trans-conductance parameter of the input transistors which is given by

$$K = \frac{1}{2} \mu_n C_{ox} \left( \frac{w}{l} \right)_n = \frac{1}{2} \mu_p C_{ox} \left( \frac{w}{l} \right)_p = \frac{1}{2} \mu C_{ox} \left( \frac{w}{l} \right) \quad (3.2)$$

Where  $\mu$  is the mobility of the charge carriers, and  $C_{ox}$  is the normalized oxide capacitance.

### 3.2 IMPLEMENTATION OF AN OP-AMP WITH COMPLEMENTARY INPUT STAGE

The op-amp consists following stages:

- 1) Complementary input stage,
- 2) Output stage, summing or biasing stage.

#### 3.2.1 COMPLEMENTARY INPUT STAGE

The schematic of a complementary input stage is shown in Fig 3.2, where M1, M2, and M1a, M2a constitute the N and P-type differential input pairs, respectively.

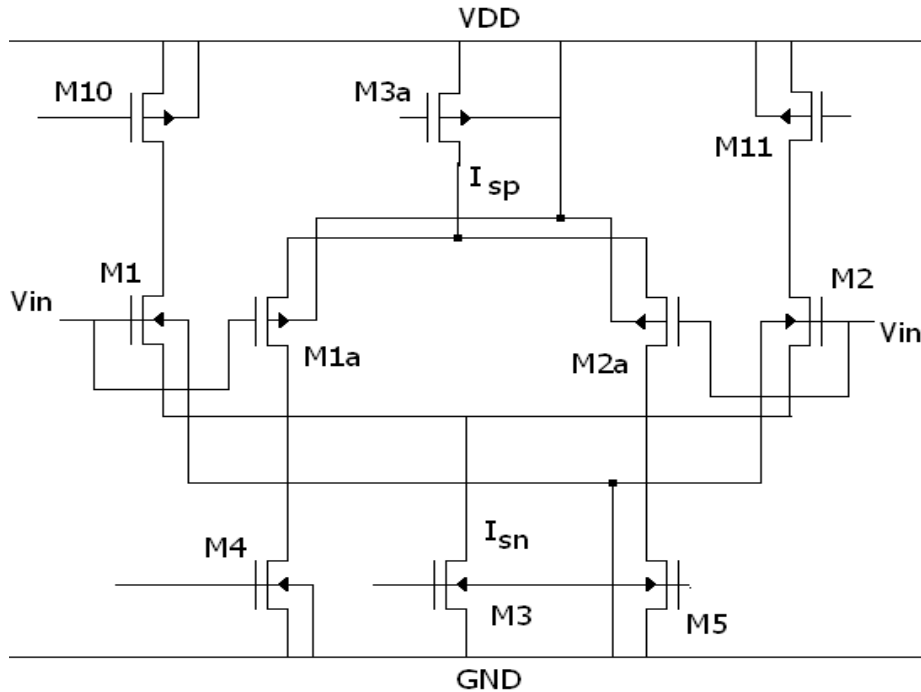
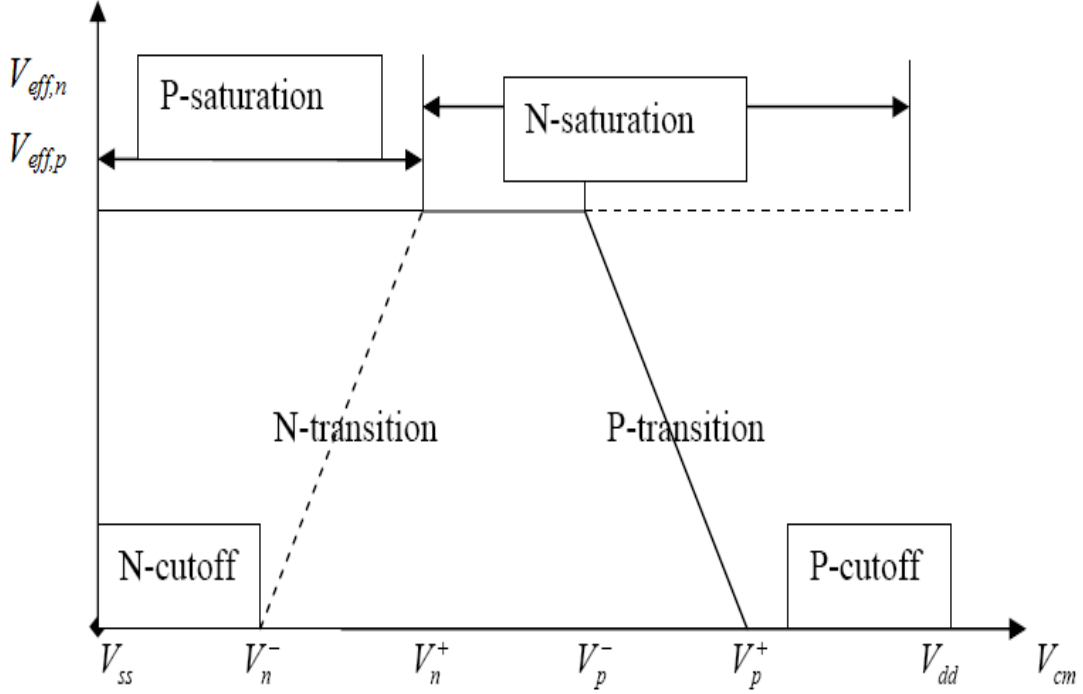


Fig 3.2 Schematic of a complementary input stage

The  $g_m$  of this input stage is constant if the following equation is satisfied [14]

$$g_{mT} = \beta_n V_{eff,n} + \beta_p V_{eff,p} \quad (3.3)$$

Here  $\beta_n = \mu_n C_{ox} \left( \frac{w}{l} \right)_n$  and  $\beta_p = \mu_p C_{ox} \left( \frac{w}{l} \right)_p$ , and  $V_{eff,n}$  and  $V_{eff,p}$  are effective gate source voltage for the N and P-pair transistors, respectively. By choosing  $\beta_n = \beta_p$ ,  $g_m$  is constant if  $V_{GS}$  of input stage is constant as shown in Fig 3.3.



**Fig 3.3 Illustration of on/off region across Common-mode input  $V_{cm}$**

### COMPLEMENTARY INPUT STAGE WITH $g_m$ CONSTANT CIRCUIT

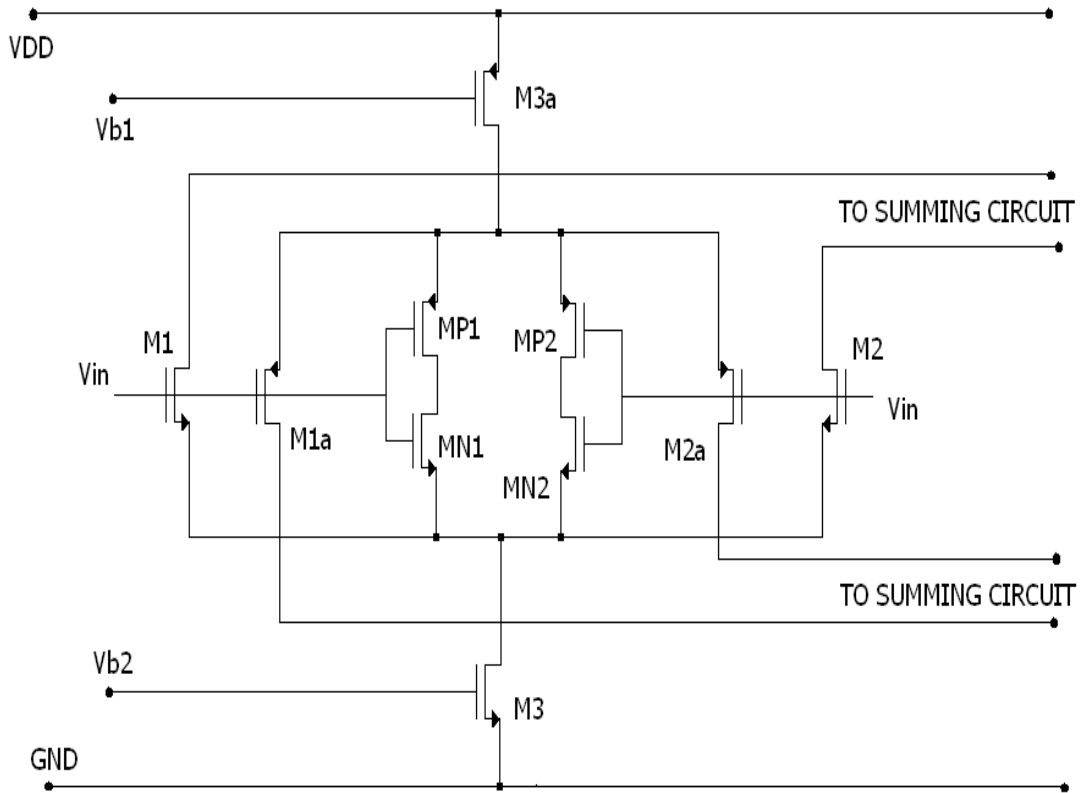
The mobility of an N-type transistor is approximately three times larger than the mobility of a P-type transistor. This difference can be largely compensated by choosing the  $W$  over  $L$  ratio of the P-channel input transistors a factor  $\frac{\mu_n}{\mu_p}$  larger than the  $W$  over  $L$

ratio of the N-channel input transistors. Of course, the factor  $\frac{\mu_n}{\mu_p}$  depends on process

variations. In the used process, this ratio deviates 15% from its nominal value, which entails a variation of the  $g_m$  of approximately 15% over the whole CM input voltage range.

Working of min-max  $g_m$  control circuit can be divided in three parts.

The 1<sup>st</sup> part, while the input common mode level is near to ground rail at this stage P-transistor pair of circuit on while N-transistors pair off. So no current flow and a constant source voltage difference maintained over this range.

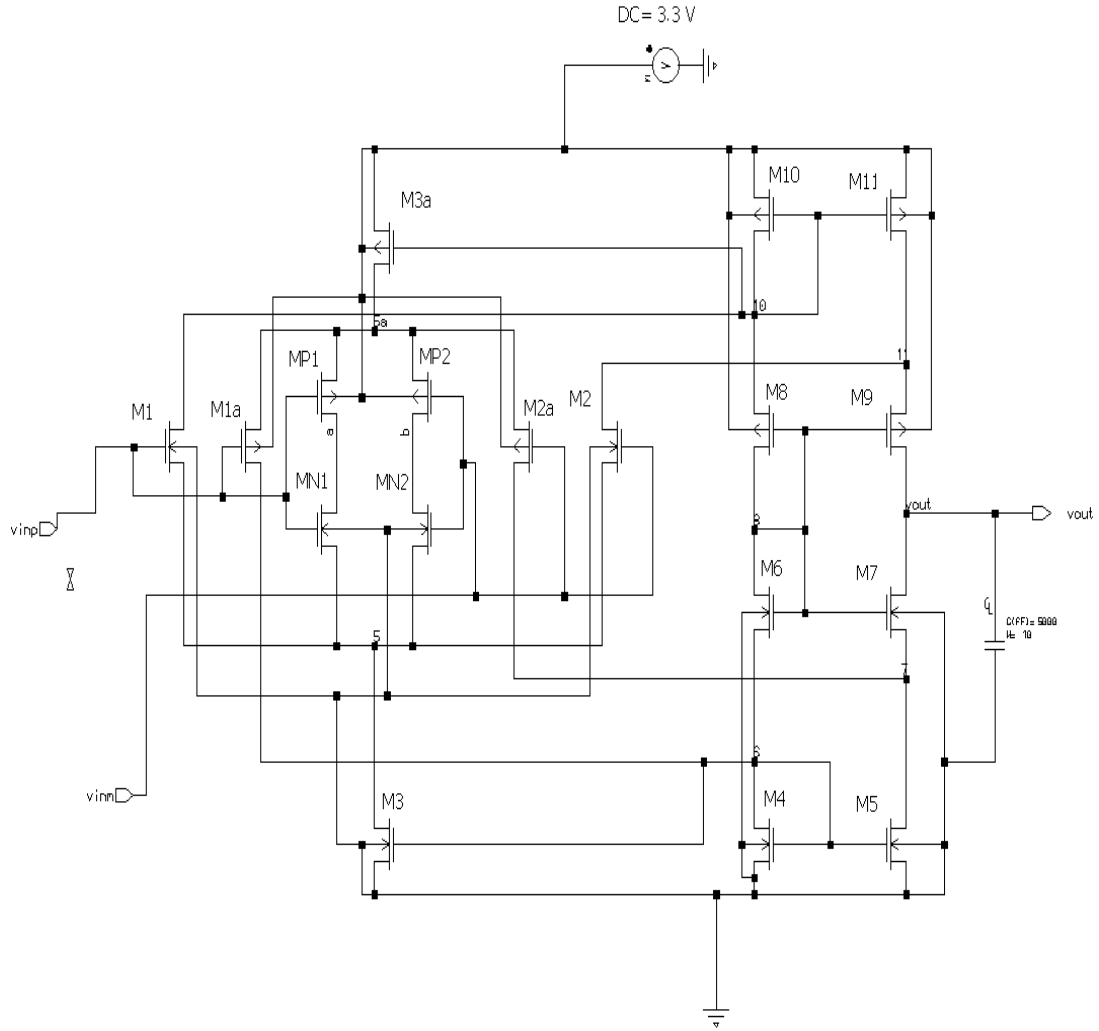


**Fig 3.4 Input stage with min-max  $g_m$  control circuit**

Now while the common mode level is near to  $V_{DD}$  rail at this condition only N-transistor pair will work and again this difference will remain same. In the middle range of CM level both N and P-transistor pair will work which maintain the difference between sources of N and P differential pair. Aspect ratio of these constant  $g_m$  pair circuit is around three times that of input stage transistors.

Here by this circuit  $g_m$  is almost constant except the two transition regions which vary the  $g_m$  7.5% to 15%. During these transition regions the current through each transistor of  $g_m$  control circuit become 3 times larger than  $I_{ref}$ . This circuit is more stable than other configuration.





**Fig 3.6 Complete circuit diagram of self biased rail-to-rail input op-amp**

### 3.3 DESIGNING

#### Technology parameters

$$K_p = 50.13 \mu A/V^2 \quad K_n = 132.5 \mu A/V^2$$

$$V_{tn} = 0.591 V \quad |V_{tp}| = 0.747 V$$

#### Designing the circuit

Initially taking  $SR = 25 V/\mu s$  and  $PD = 2 Mw$ .

To get uniform performance over the common mode range and to get symmetric step response for rising and falling inputs, the following equalities are taken:

$$M_1 = M_2, M_{1a} = M_{2a}, M_4 = M_5, M_6 = M_7, M_8 = M_9, M_{10} = M_{11}, MN_1 = MN_2,$$

$$MP_1 = MP_2 \quad (3.4)$$

$$\beta_1 = \beta_{1a}, \beta_8 = \beta_6, \beta_4 = \beta_{10} \quad (3.5)$$

$$L_{1a} = L_1, L_8 = L_6, L_{10} = L_4 \quad (3.6)$$

$$I_{3a} = I_3 \quad (3.7)$$

Relations used for calculation

$$I_L = SR \times C_L \quad (3.8)$$

$$PD = I_T \times V_{DD} \quad (3.9)$$

$$PM = 180 - \tan^{-1} \frac{GBW}{P1} - \tan^{-1} \frac{GBW}{P2} \dots \quad (3.10)$$

Here  $I_L$ ,  $C_L$ ,  $SR$ ,  $PD$ ,  $I_T$  are load current, load capacitor, slew rate, power dissipation and total current from source respectively.

Relations of current in circuit without  $g_m$  constant circuit:

$$I_{D4} = \frac{I_{D3}}{2} + I_6 (= I_L) \quad (3.11)$$

$$I_T = 2I_{D4} + I_{D3} \quad (3.12)$$

By using the relation of matched transistors and current equation all the aspect ratio can be calculated. Calculating W/L of all transistors, then the W/L of constant  $g_m$  circuits will around 3 times of input stage for p and near to same for n which is iterated later. Finally the values comes are given it table 3.1. The design is simulated then and results are calculated which are shown in the next chapter.

**Table 3.1 Self biased Rail-to-Rail input Operational Amplifier Device Sizes**

Device	Width/Length ( $\mu m$ )	Function
M1, M2	25.2/1.4	Input N-pair Diff. Stage
M1a, M2a	67.2/1.4	Input P-pair Diff. Stage
M4, M5	5.6/1.4	Output Stage
MP1,MP2	211.4/1.4	Constant $g_m$ circuit
M6, M7	4.2/1.4	Output Stage
M8, M9	109.2/2.8	Output Stage
MN1, MN2	50.4/2.8	Constant $g_m$ circuit
M10, M11	71.4/1.4	Output Stage
M3	37.8/1.4	Current Sink
M3a	155.4/1.4	current source

## CHAPTER 4

### SIMULATION RESULTS AND LAYOUT

---

In this chapter the schematic of the circuit has been tested for various parameters. All values have been measured at load capacitance of  $5pF$ . Prepared circuit of amplifier is simulated at mentor graphics ASIC design kit design architect IC tool at TSMC  $0.35\mu m$  CMOS technology. The amplifier is to be powered from a  $3.3V$  power supply and with a tail current reference of  $225\mu A$ . The current sources/sinks required for biasing used from output stage.

Based on the constant- $g_m$  input stage using overlapping of transition region, a rail-to-rail input CMOS Op-amp has been designed. The simulations include AC response, Transient analysis, Common Mode Rejection Ratio, Power Supply Rejection Ratio, Input Common Mode Range. The responses have been checked for temperature variation, Load capacitance variation. Some have also been checked for input dc voltage variation.

#### 4.1 TEST RESULTS

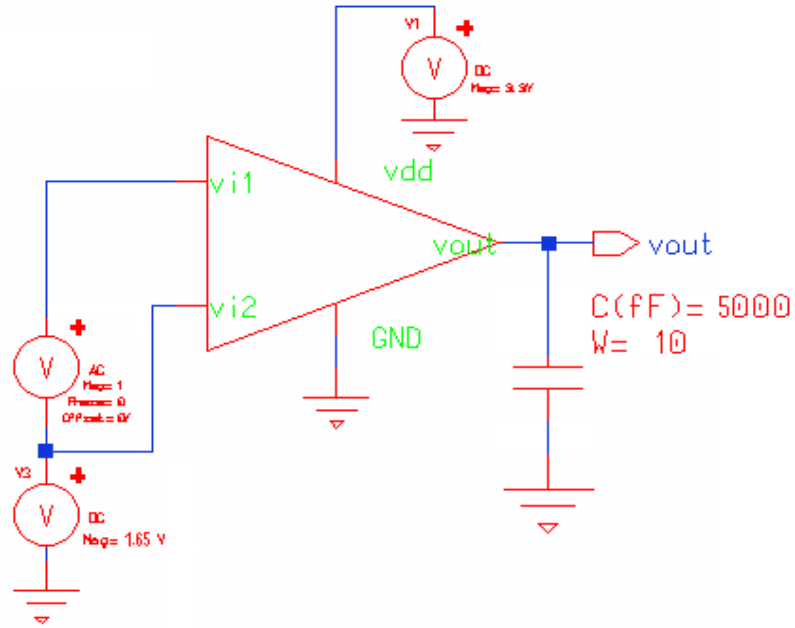
This design provided an overall gain of  $85.513dB$  with a common mode rejection of over  $133.242 dB$ . Output Voltage Swing is  $1.64 V$ , with ICMR greater than  $3.2 V$ . Unity gain bandwidth obtained is  $9.17MHz$ . Slew rates obtained are  $7.27 V/\mu s$  and  $3.62 V/\mu s$ . The phase margin came out to be nearly  $55^\circ$  making design relatively stable.

##### 4.1.1 AC RESPONSE

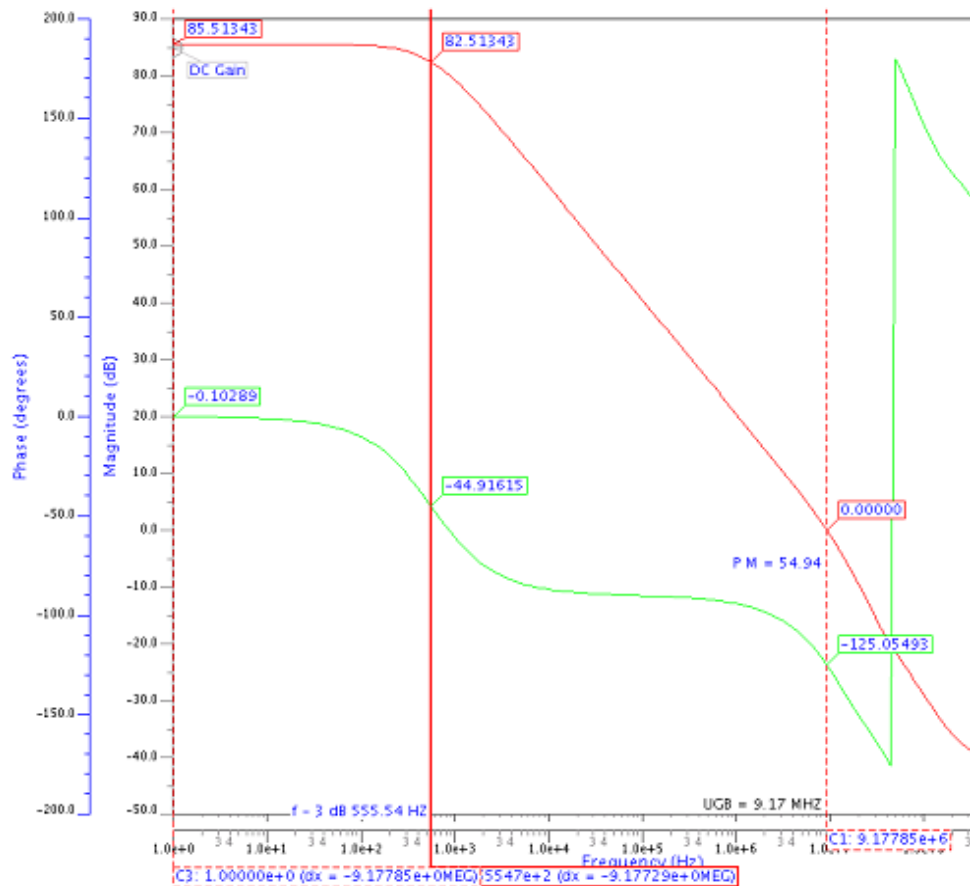
This response is used for observing open loop gain, Unity Gain Bandwidth (UGB),  $3-dB$  bandwidth and the Phase Margin of the circuit. In the test setup a differential AC signal of  $1V$  is applied to the inputs along with this the dc bias potential is also applied.

In Fig 4.1, one method of measuring the AC performance is presented. In this configuration, the amplifier is in open loop configuration, and the small AC signal is applied at the input.

In Fig 4.2, a Gain and phase plot for  $3.3V$   $27^\circ$  is shown. As can be seen, the open loop gain is  $85.513dB$ ,  $3-dB$  frequency is  $555 Hz$  and a phase margin is nearly  $55^\circ$ .



**Fig 4.1 Configuration for simulating the open loop frequency response of operational amplifier**



**Fig 4.2 Frequency response of operational amplifier**

### 4.1.2 TRANSIENT RESULTS

For observing the transient response of the op-amp the test setup of Fig 4.3 must be used. In this setup sinusoidal signals are applied between the two inputs and the effective value of input signal is the difference of the voltage at the two terminals. DC potential is also applied along with the sinusoidal signal in order to provide the bias voltage to the input transistors.

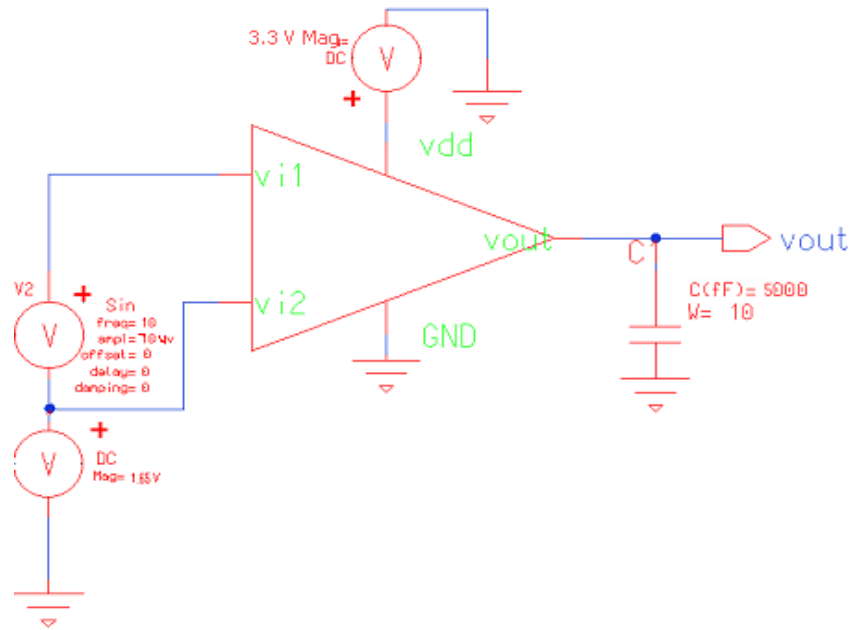


Fig 4.3 Schematic for the simulation of the transient Response

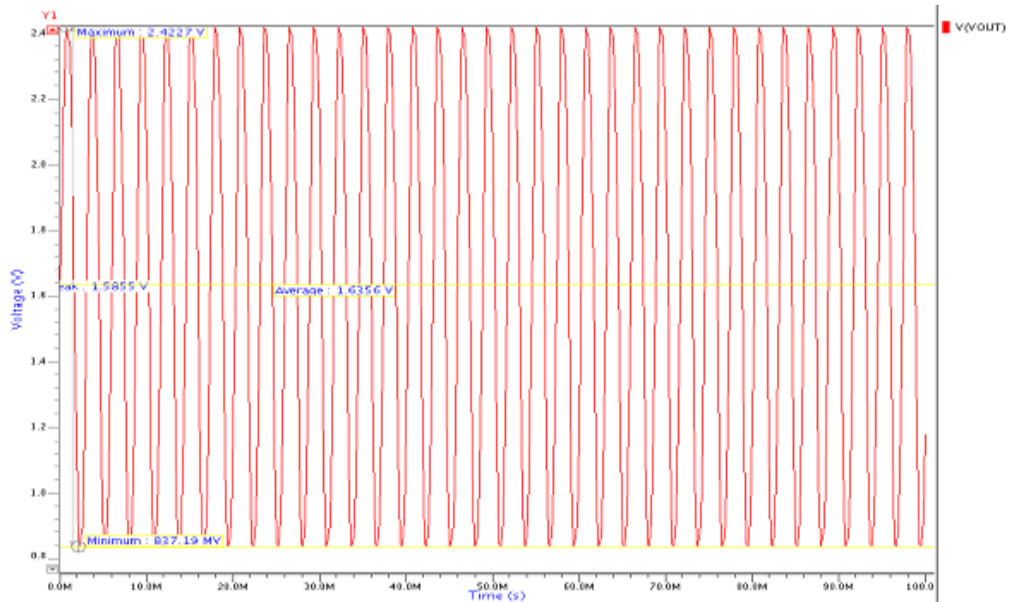
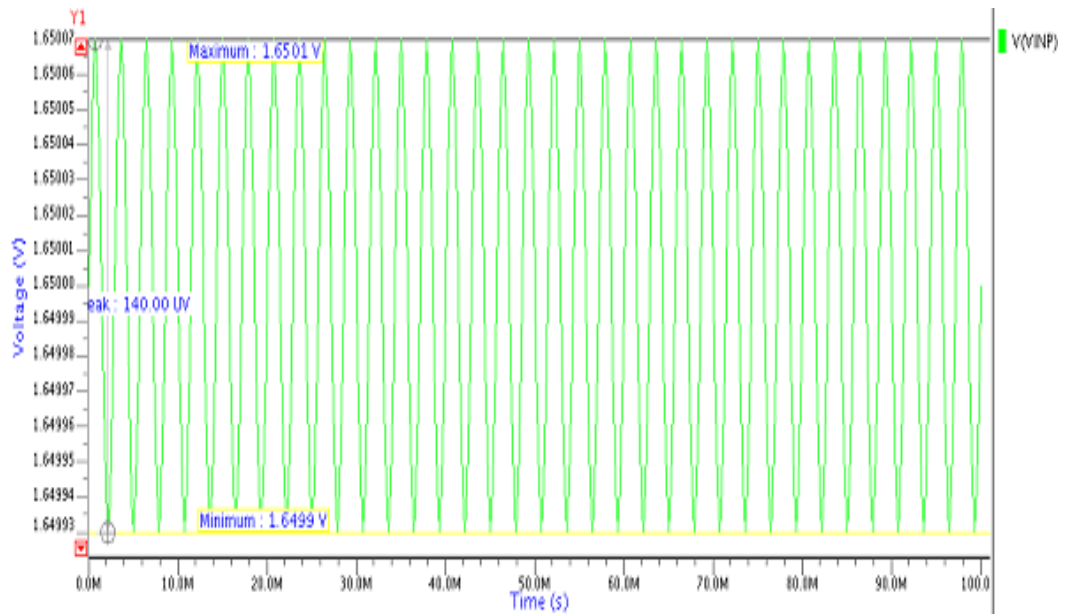
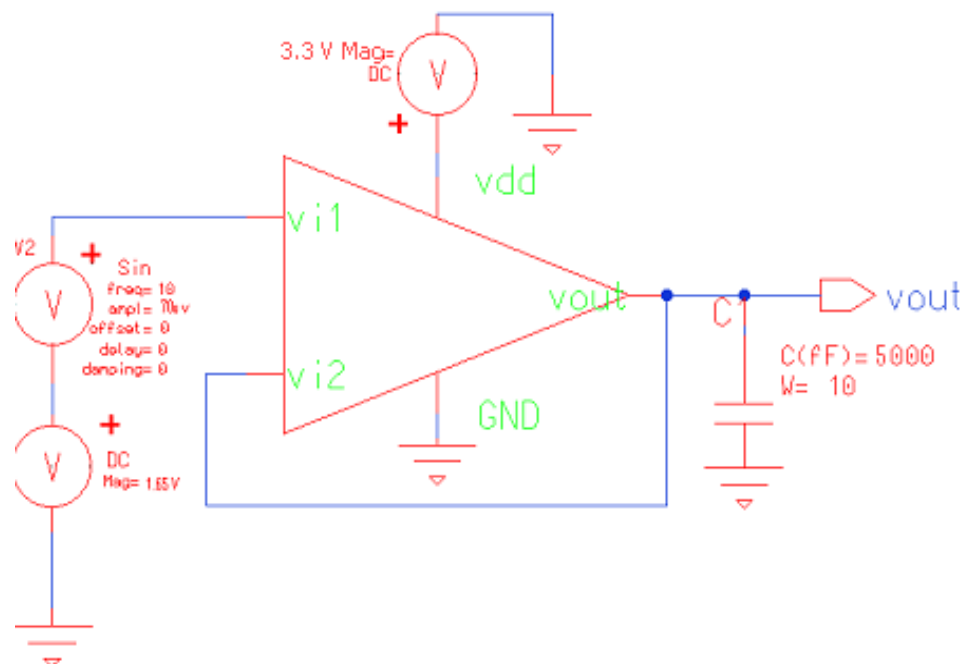


Fig 4.4 Output signal for transient analysis



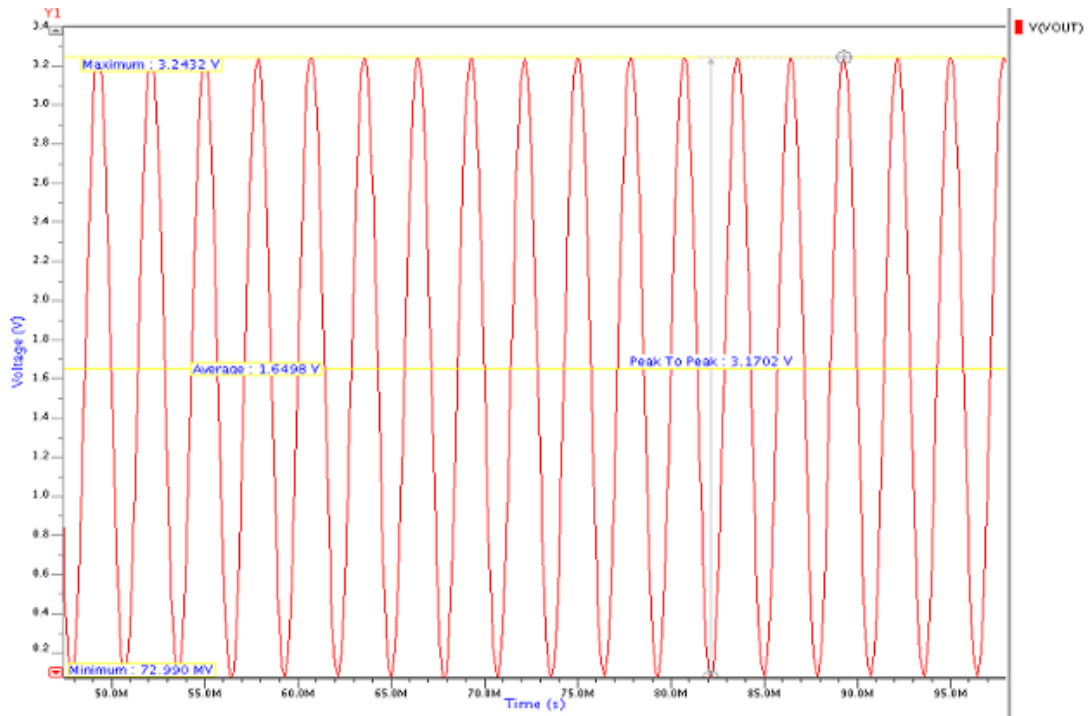
**Fig 4.5 Input signals for transient analysis**

A transient simulation of the amplifier in unity gain configuration with the swing at the input rail-to-rail is the most insightful simulation presented in Fig 4.7, because it exercises the amplifier over the entire common mode range and shows the amplifier is not slewing and is exhibiting reasonable linear behavior.



**Fig 4.6 Schematic for the simulation of the transient Response with unity feed**

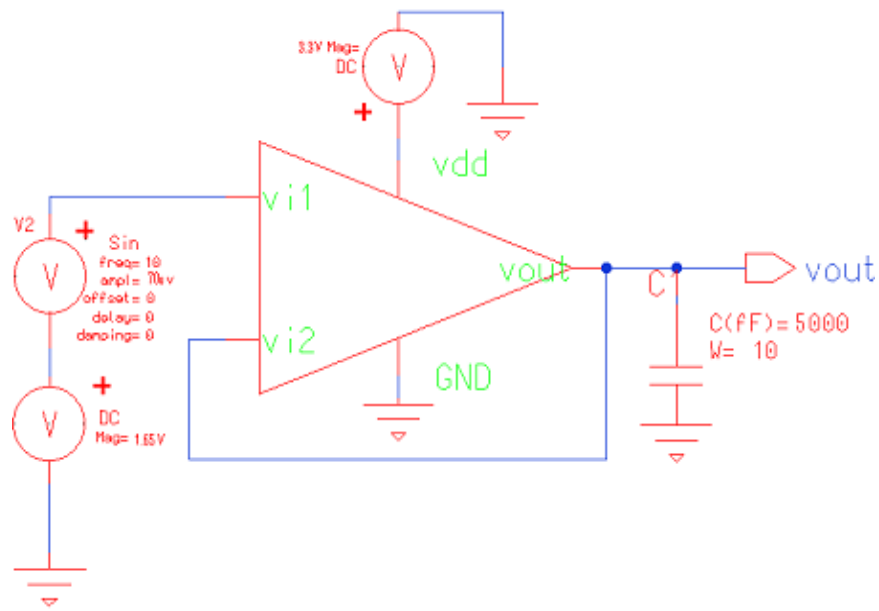
back



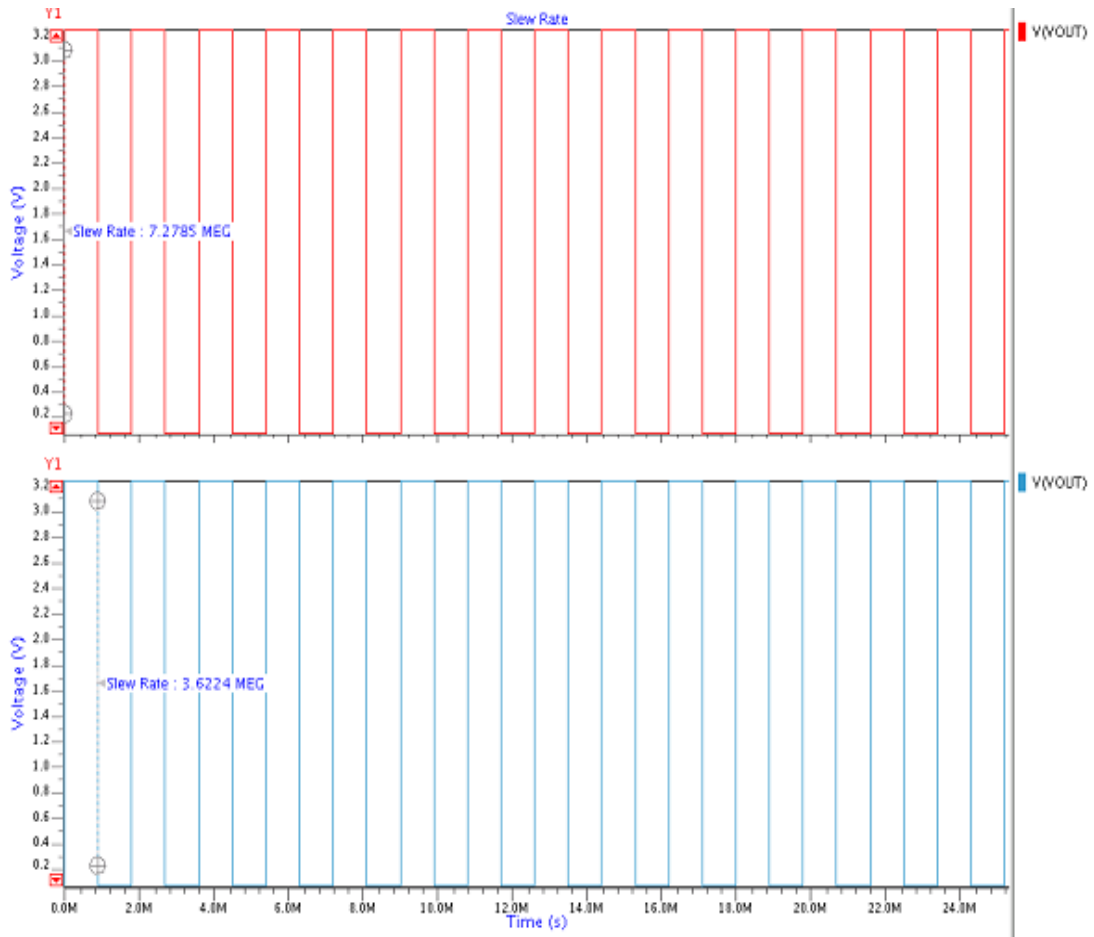
**Fig 4.7 Output for transient analysis with unity feedback**

#### 4.1.3 STEP RESPONSE – SLEW RATE MEASUREMENT

In Fig 4.8, a step from ground to  $V_{DD}$  is applied at the input with unity feedback configuration. The amplifier's slew rate is  $7.2785V/\mu s$  for the rising edge and  $3.622V/\mu s$  for the falling edge.



**Fig 4.8 Schematic for the simulation and measurement of the slew rate**



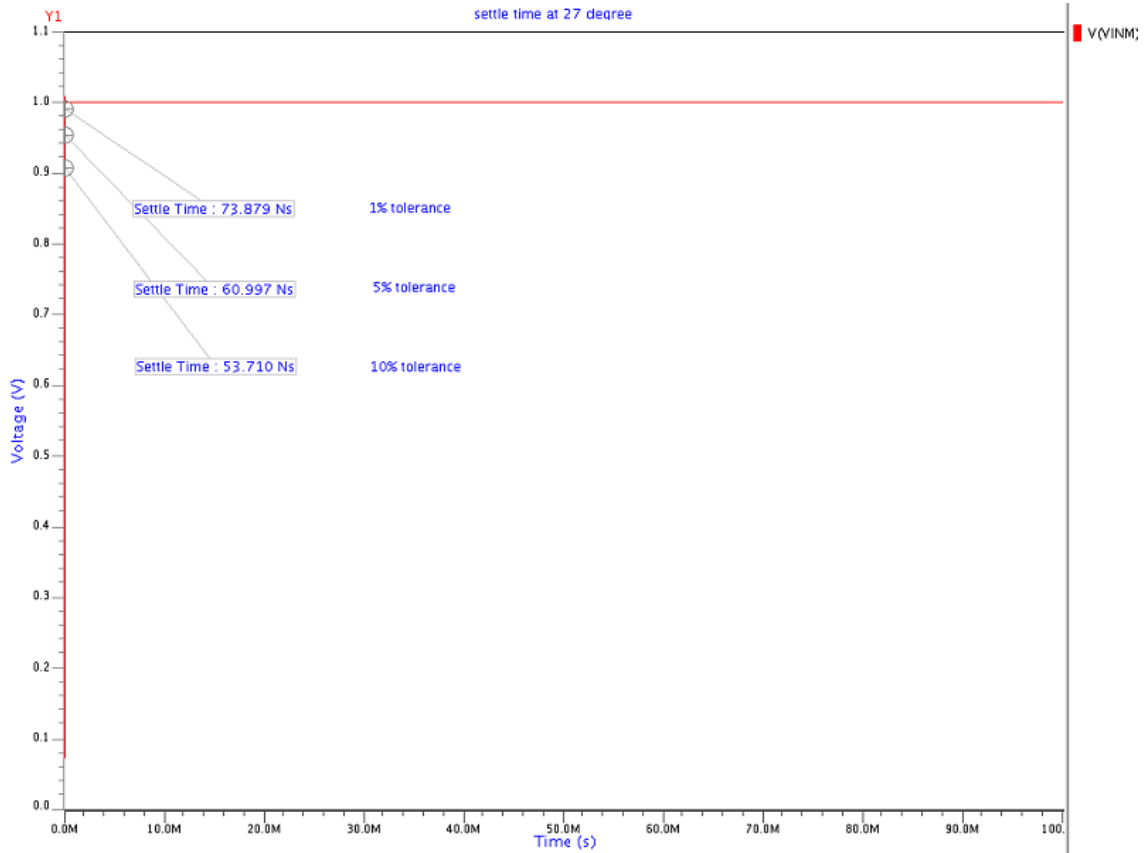
**Fig 4.9 Slew rate for the rising and falling edge with operational amplifier in unity gain configuration**

#### 4.1.4 SETTling TIME

Settling time is the length of time for the output voltage of an op-amp to approach, and remains within, a certain tolerance of its final value. This is usually specified for a fast full-scale input step. In Fig 4.10 shows the settling time of the input pulse of 1V magnitude in unity gain configuration for different tolerance values.

**Table 4.1 Variation of Settling Time of with different Tolerance values**

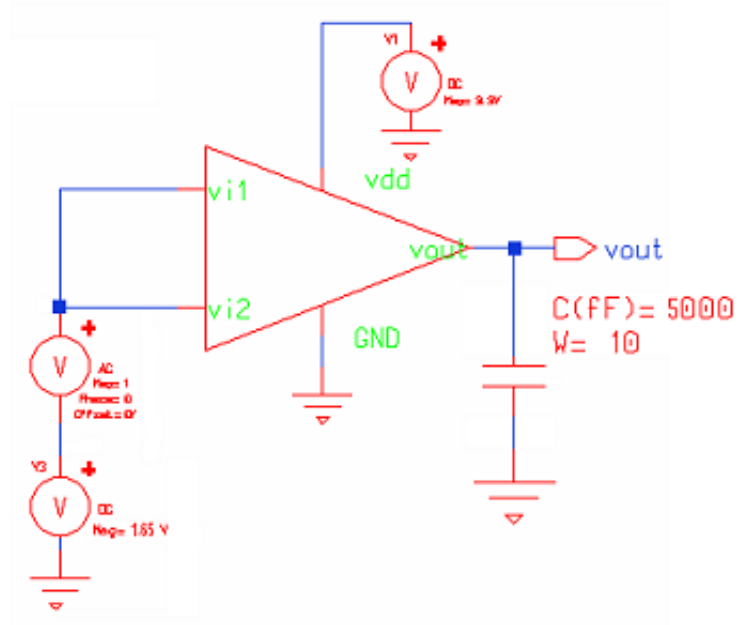
Tolerance (%)	Settling Time (Ns)
1	73.897
5	60.997
10	53.710



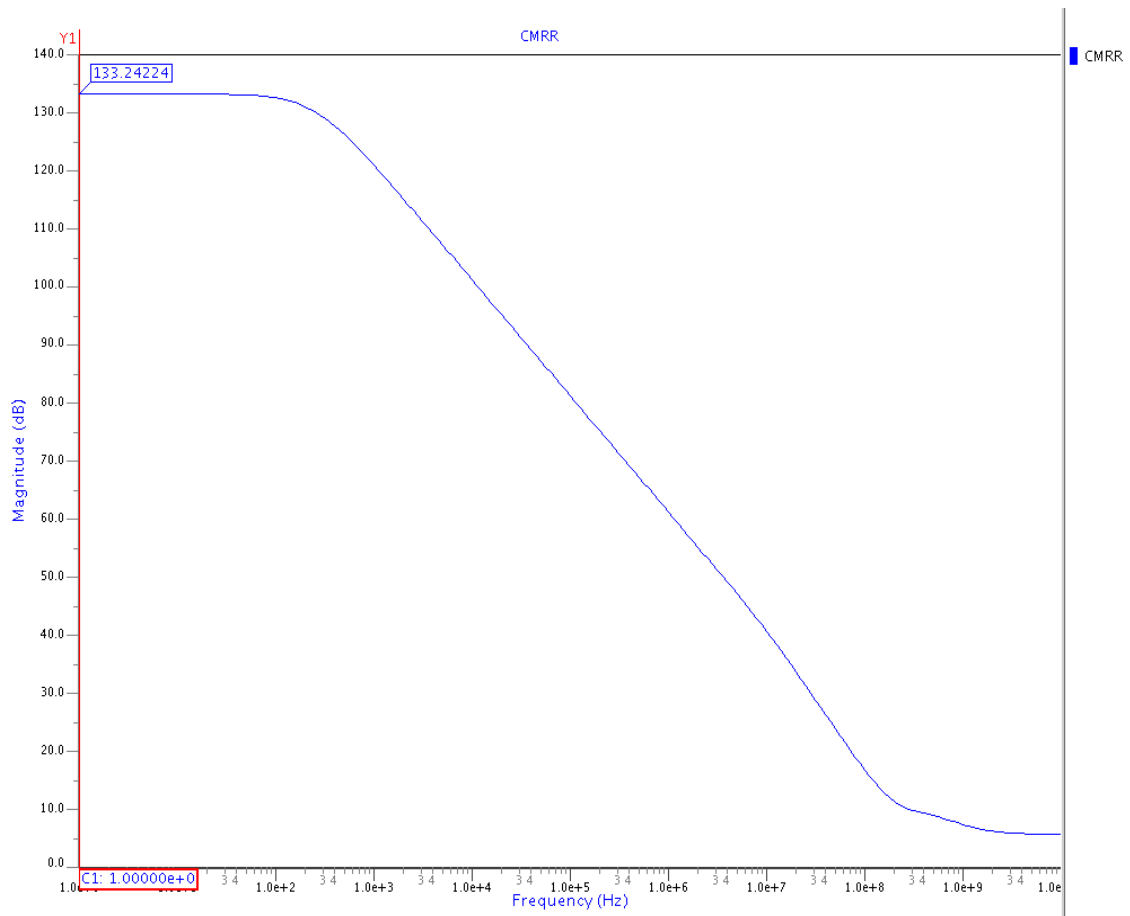
**Fig 4.10 Settling time for the different tolerance values with unity gain configuration**

#### 4.1.5 COMMON MODE REJECTION RATIO

In order to simulate common mode rejection, differential gain as well as the common mode gain of the op-amp is required and the CMRR is obtained by  $A_{DG} (dB) - A_{CG} (dB)$ . A 1V AC source is placed on the positive input as shown in Fig 4.11. When the simulator sweeps the frequency, there will be a 1V AC source on both the positive and negative inputs and hence the AC signal at the output will be the common mode gain [26]. The previously calculated gain (DC gain) can be divided by this gain to give the CMRR. The common mode rejection ratio was found the value  $133.24224dB$ .



**Fig 4.11 Schematic for the simulation of CMRR**



**Fig 4.12 Simulation Result of Common Mode Rejection Ratio**

#### 4.1.6 POWER SUPPLY REJECTION RATIO

PSRR or power supply Rejection Ratio shows the capability of the circuit to reject supply noise. There are two PSRR one for positive supply voltage and other of negative supply voltage. There are two types of PSRR:-

- a) Positive PSRR
- b) Negative PSRR

##### POSITIVE PSRR

The test setup shown below is for positive PSRR in this method we apply only common mode dc potential to the input transistors and a 1V AC signal is inserted between  $V_{DD}$  supply and  $V_{DD}$  port of the circuit.

In order to simulate power supply rejection, differential gain as well as the PSRR+ gain of the op-amp is required and the CMRR is obtained by  $A_{DG} (dB) - A_{PSRR+} (dB)$ . The value of positive PSRR is 90.18313 dB at lower frequency and become zero above 100MHz.

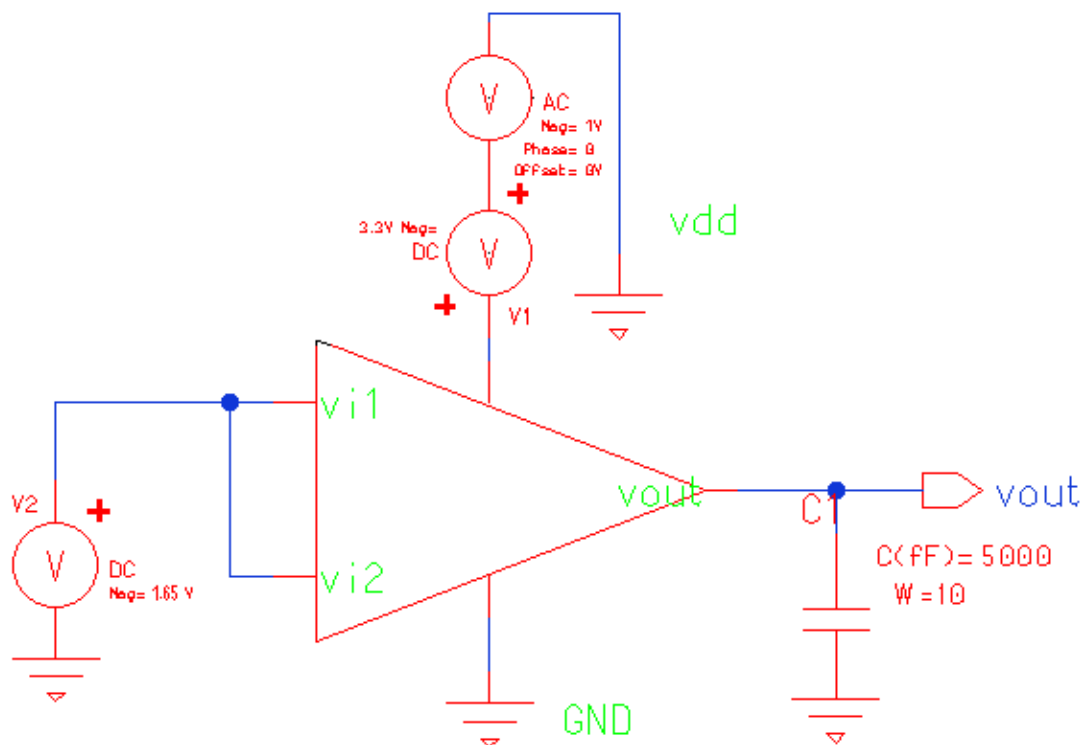
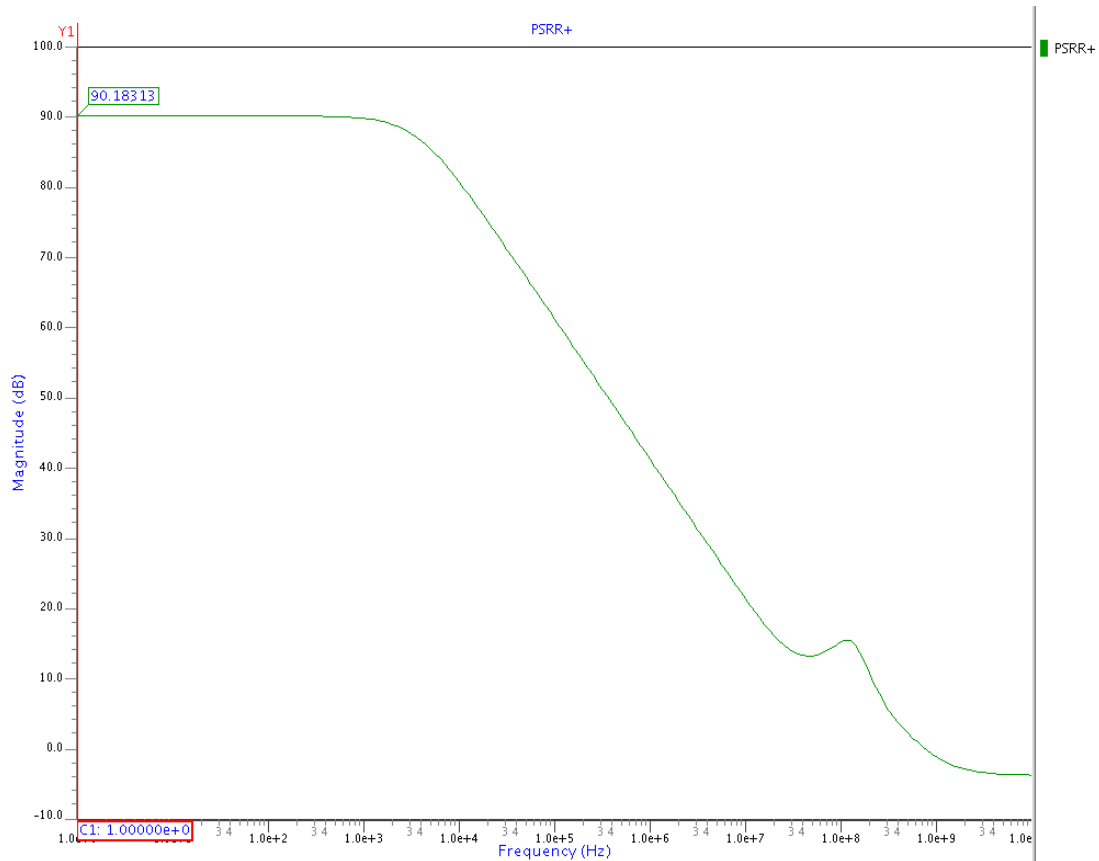


Fig 4.13 Schematic for the simulation of Positive PSRR

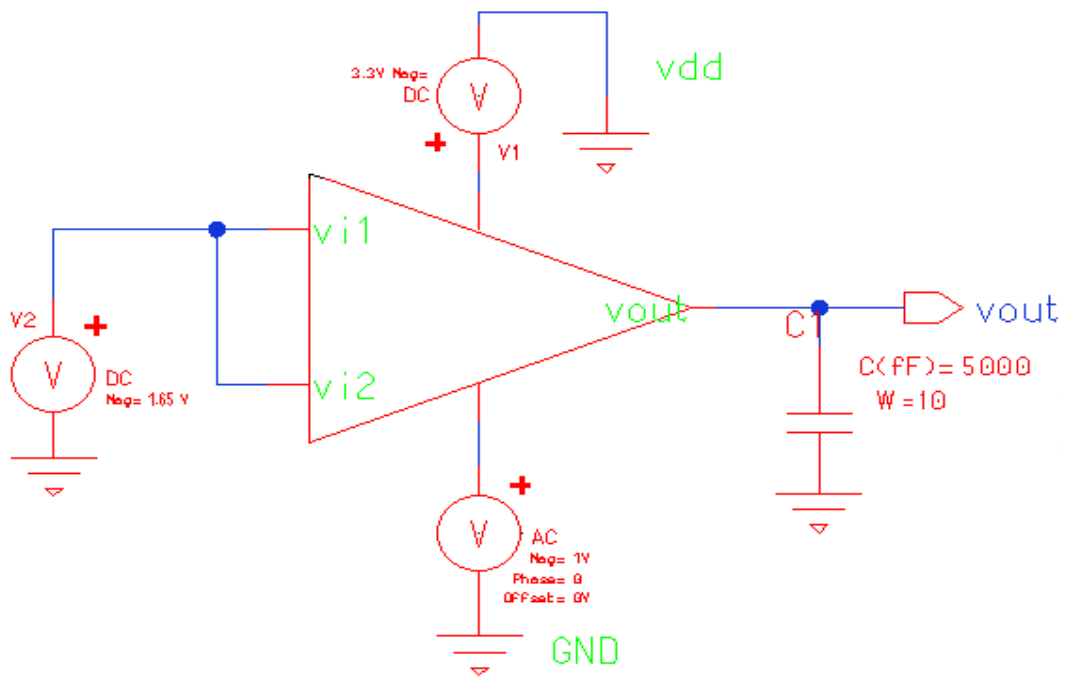


**Fig 4.14 Simulation Result of Positive Power Supply Rejection Ratio**

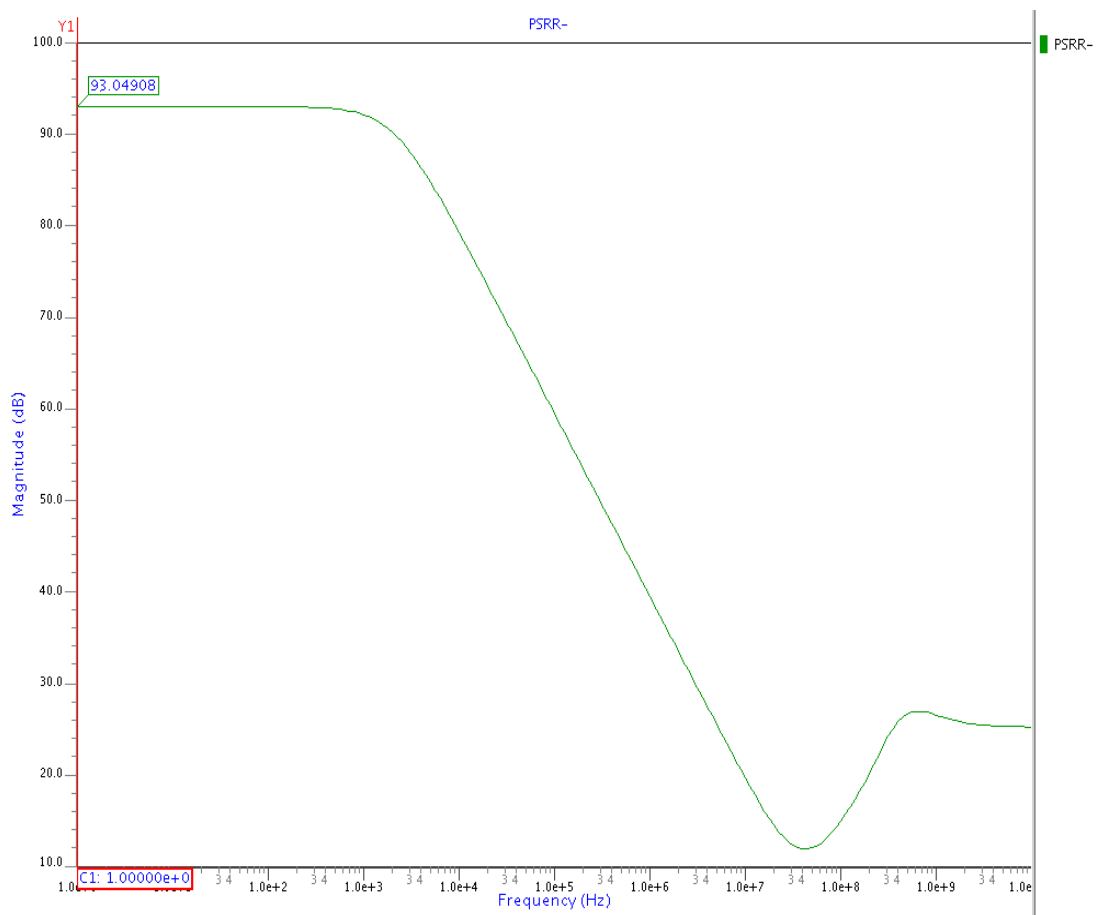
### NEGATIVE PSRR

The test setup shown below is for negative PSRR in this method we apply only common mode dc potential to the input transistors and a 1V AC signal is inserted between ground and the op-amp now the differential gain which we get at the output of the op-amp is noted. This does not give the PSRR plot instead this gain should be subtracted from differential gain  $A_D$  (dB) then the plot we get is the PSRR plot.

The value of positive PSRR is 93.04908 dB at lower frequency and above 10MHz it come nearly 10dB.



**Fig 4.15 Simulation Result of Negative Power Supply Rejection Ratio**

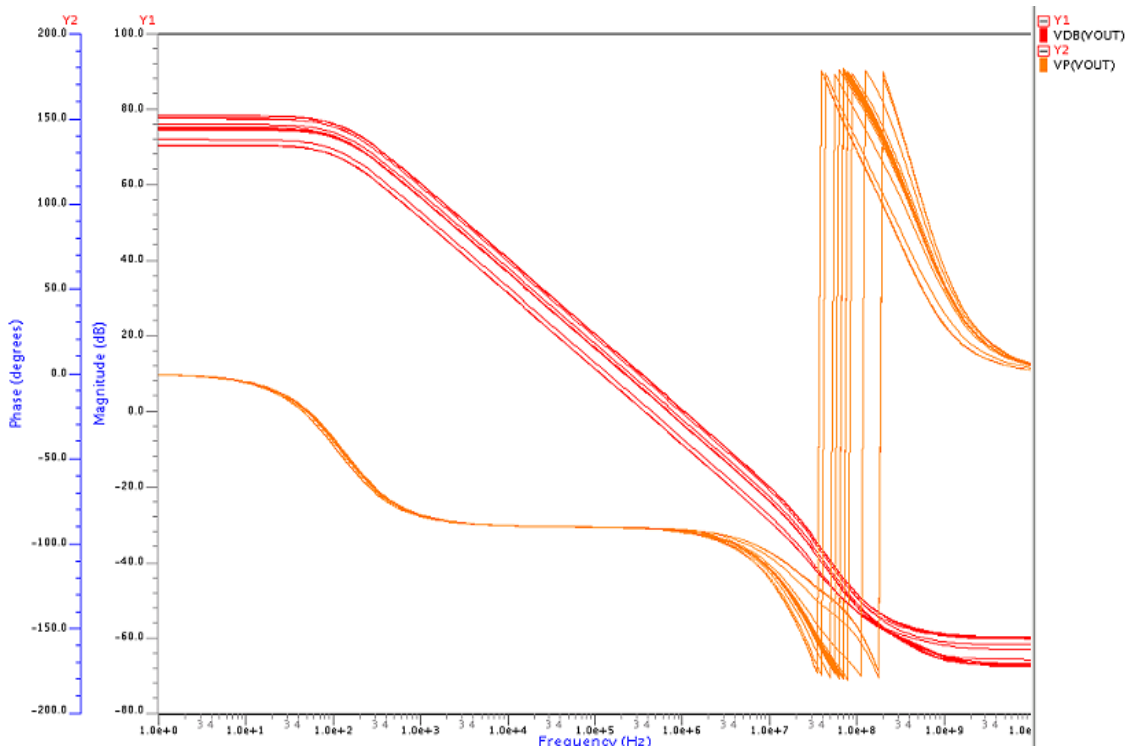


**Fig 4.16 Simulation Result of Negative Power Supply Rejection Ratio**

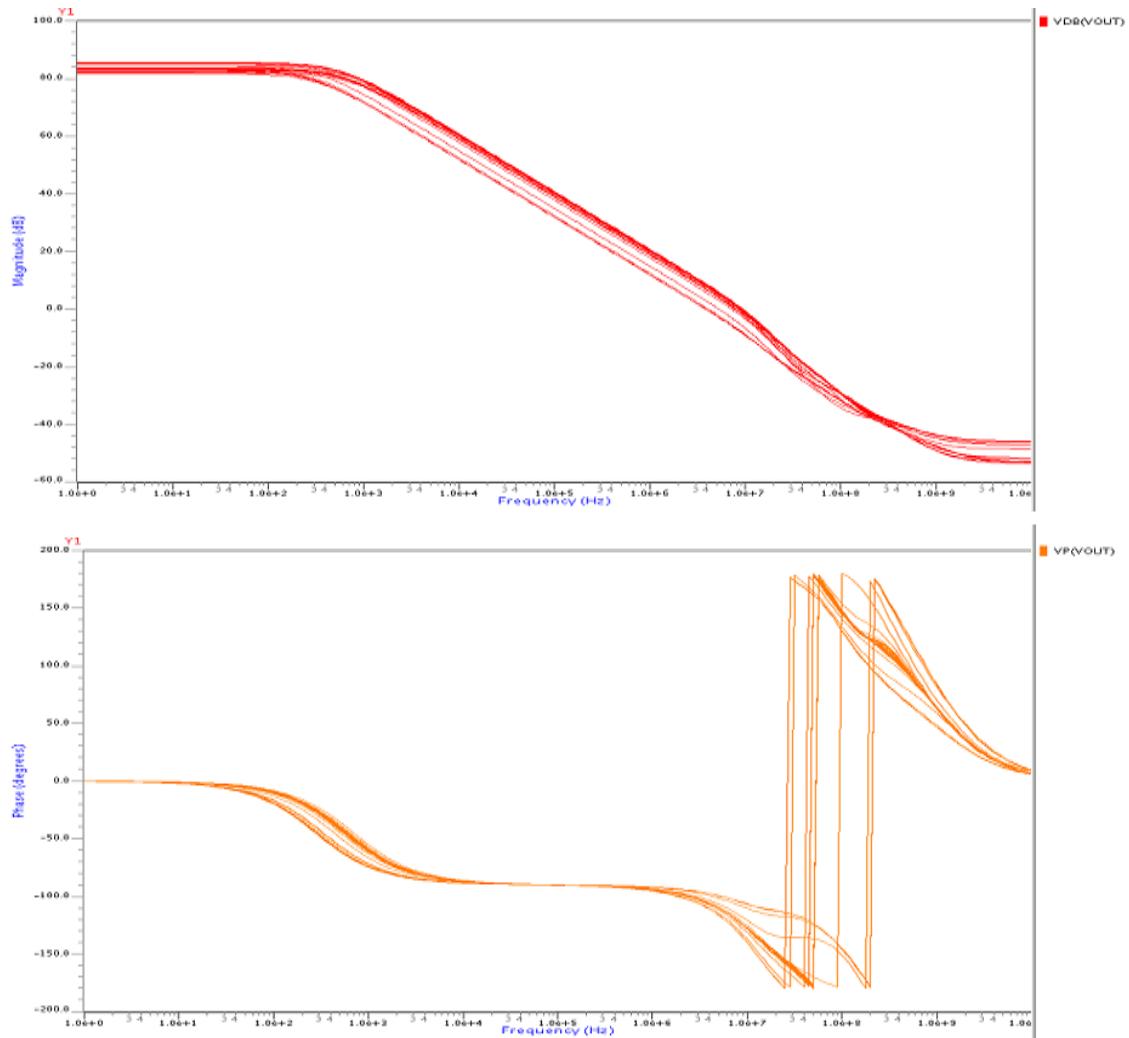
#### 4.1.7 EFFECT OF COMMON MODE VARIATION ON THE DC GAIN

While varying common mode input voltage,  $g_m$  of circuit changes so the DC gain also varies. Fig 4.17(a) shows the frequency response of the op-amp with conventional complementary input stage without using any constant  $g_m$  technique shown. The amplitude and the phase are heavily dependent upon the applied common-mode input voltage  $V_{cm}$ , which is varied from rail (0 V) to rail (3.3 V) by the step of 0.1 V. This op-amp is unstable and cannot be compensated due to varying  $g_m$ , as stated in the earlier chapters. In contrast, Fig. 4.17 (b) shows the frequency responses of the op-amp with constant  $g_m$  circuit stage for the common-mode input voltage varying from rail to rail by a step of 0.1 V. The amplitudes and the phases of the proposed op-amp are almost independent of the applied. Comparing Fig. 4.17(a) and (b), we can see the substantial improvement in the frequency responses of the op-amp with overlapped transition region over that of the conventional complementary op-amp.

Without  $g_m$  constant circuit the gain of the op-amp varies from 70 dB to near about 79 dB. While with constant  $g_m$  circuit gain variation is between 82 dB to around 85.5 dB. The variation is very less also the gain of the op-amp improves with this  $g_m$  constant circuit.



**Fig 4.17 (a) Frequency response of operational amplifier for the input stage without constant  $g_m$  circuit**

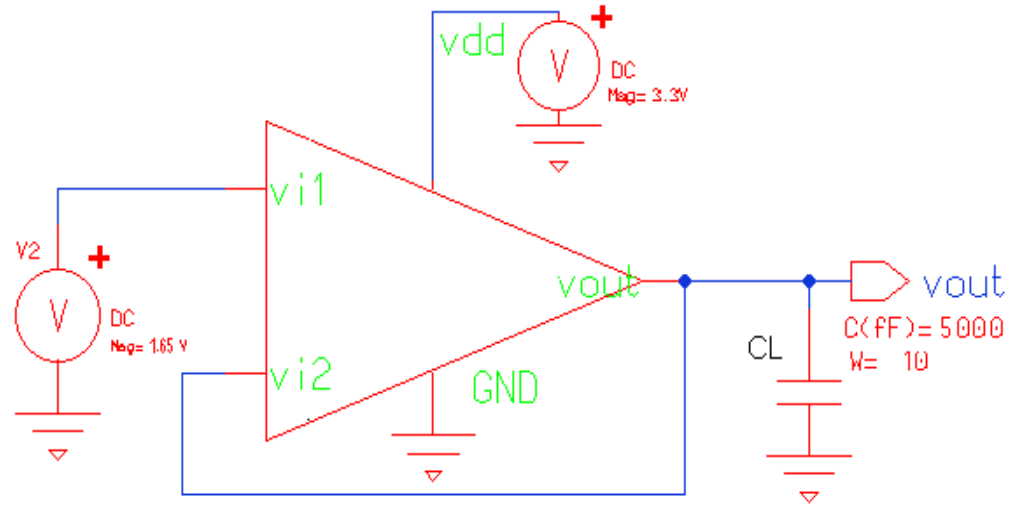


**Fig 4.17 (b) Frequency responses for the input stage with constant  $g_m$  circuit**

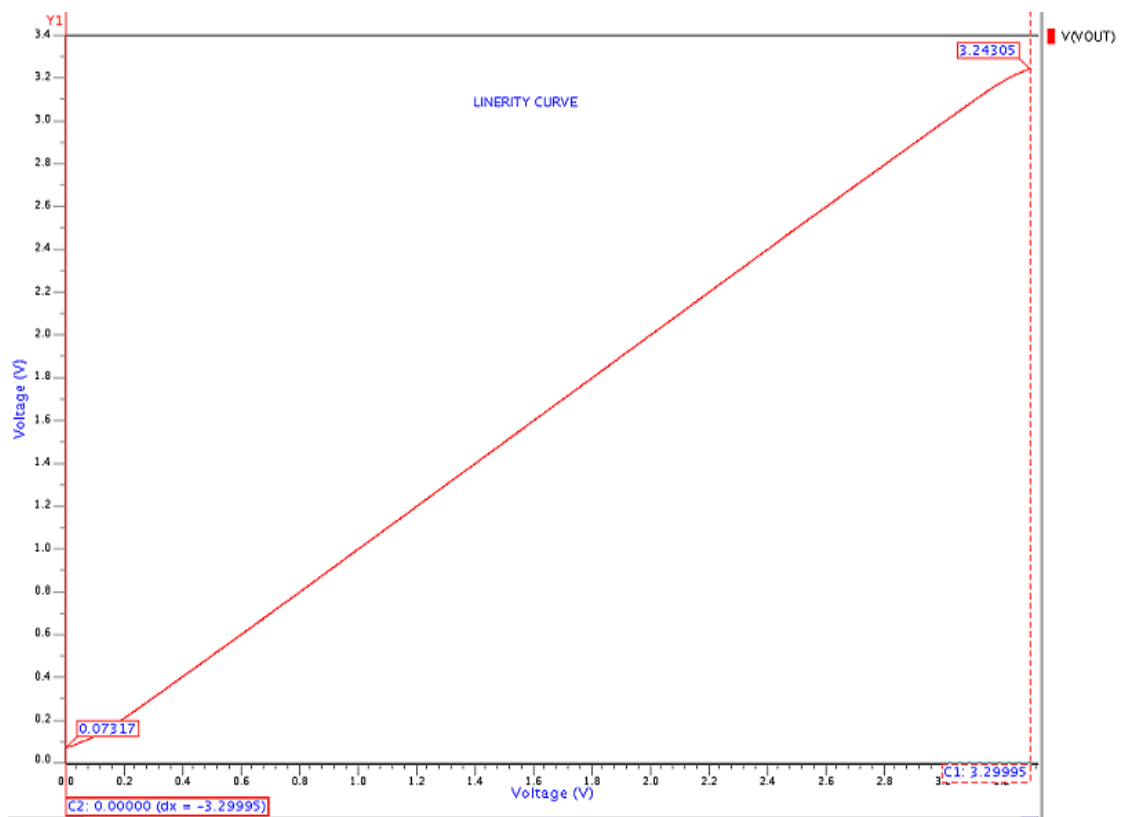
#### **4.1.8 INPUT COMMON-MODE RANGE CHARACTERISTICS USING UNITY GAIN CONFIGURATION**

DC analysis of the circuit provides the ICMR. This test is performed to test the offset voltage and the input common mode range of the op-amp that is the range of op-amp for which there is a linear relationship between input and the output.

Fig 4.18 shows the setup of simulating ICMR op-amp is in unity gain configuration and at non-inverting terminal dc voltage sweep from 0 to 3.3V is applied. As shown in Fig 4.19 at 0 V input voltage, output value is 0.07317V and at 3.3V input voltages, output value is 3.24305V.



**Fig 4.18 Schematic for the simulation of Input Common-Mode Range**



**Fig 4.19 Simulation Result of Input Common-Mode Range**

#### **4.1.9 VARIATION OF FREQUENCY RESPONSE WITH LOAD CAPACITANCE**

Fig 4.20-4.22 shows the effect of variation of load capacitance (1pF, 5pF, 10pF) on the frequency response of the op-amp.

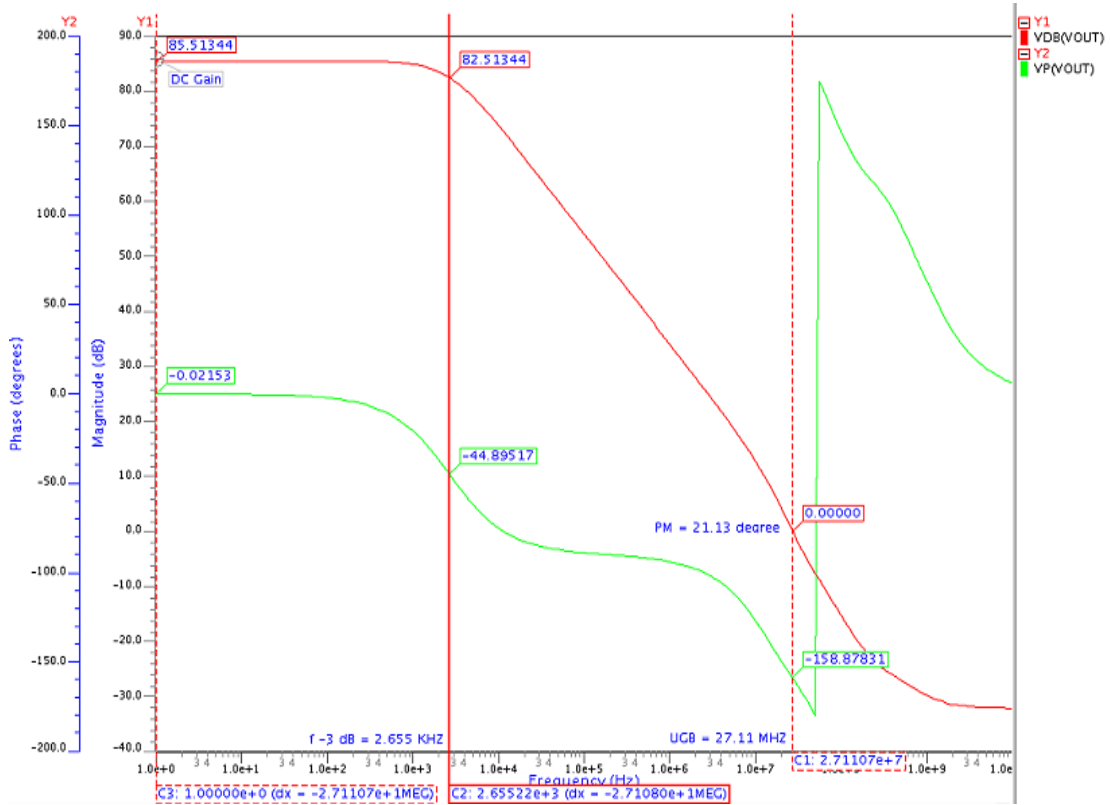


Fig 4.20 Frequency Response at load capacitance 1pF

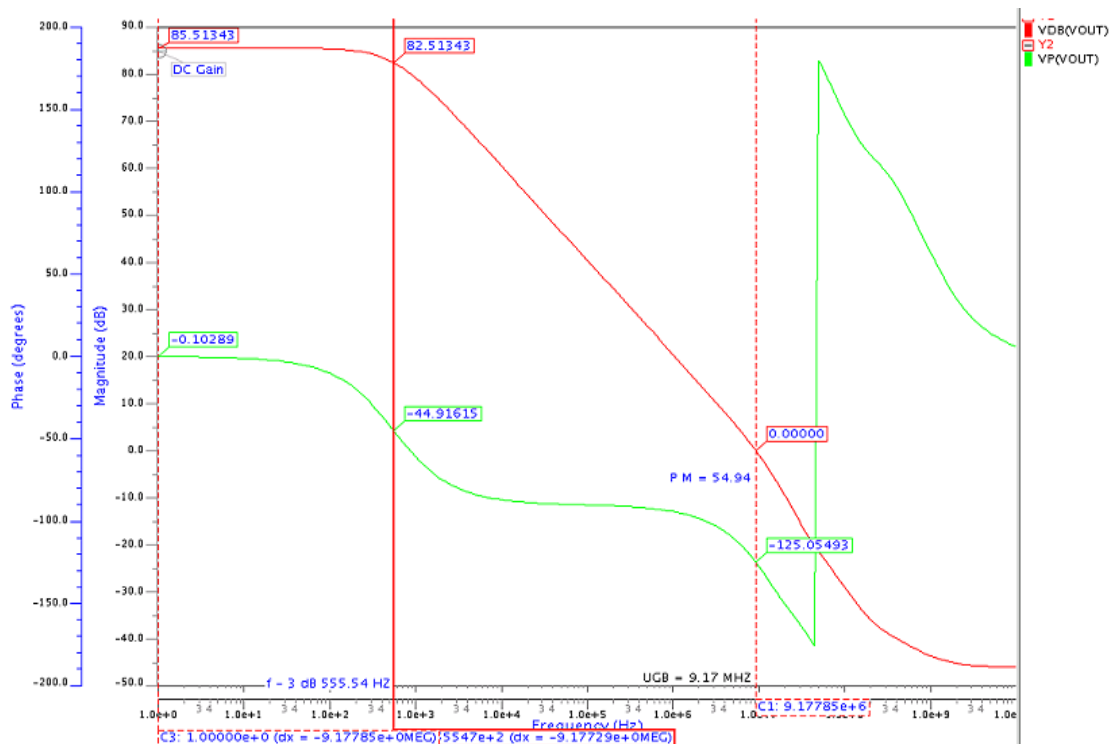
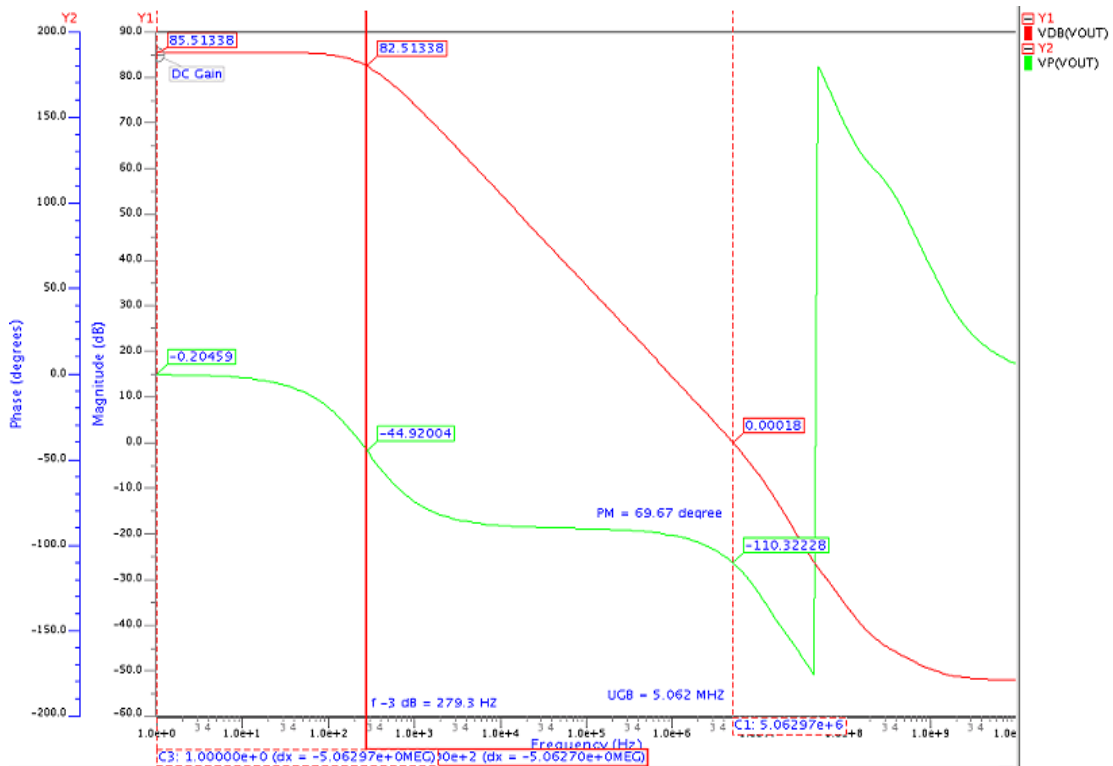


Fig 4.21 Frequency Response at load capacitance 5pF



**Fig 4.22 Frequency Response at load capacitance 10pF**

**Table 4.2 Variation of Unity Gain Bandwidth and phase margin with change in the Load Capacitance ( $C_L$ )**

Load capacitance ( $C_L$ ) (pF)	Unity gain Bandwidth (MHz)	Phase Margin (deg)	f-3dB(Hz)
1	27.11	21.13	2655
5	9.17	54.94	555.54
10	5.062	69.67	279.3

Fig. 4.20 shows the AC response of the circuit at a load capacitance of  $1\text{pF}$  the open loop DC gain of the circuit is  $21.13\text{dB}$ . It is providing  $3\text{-dB}$  frequency of  $2655\text{Hz}$  and UGB of  $27.11\text{MHz}$ . The phase margin is  $21.13^\circ$ .

In the Figs 4.21 and 4.22, the AC responses with load capacitance values  $5\text{pF}$  and  $10\text{pF}$  are shown. With increase in load capacitance the phase margin improves but the UGB decreases. The open loop dc gain is not affected by  $C_L$  variation and remains almost constant at  $85.513\text{dB}$ . The UGB frequency at  $5\text{pF}$  and  $10\text{pF}$  is  $9.17\text{MHz}$  and  $5.062\text{MHz}$  respectively. The phase margins at  $5\text{pF}$  and  $10\text{pF}$  are  $54.942^\circ$  and  $69.67^\circ$  respectively.

## 4.2 EFFECT OF VARIATION OF TEMPERATURE

Taking the temperature variation from  $-130^{\circ}\text{C}$  to  $130^{\circ}\text{C}$ , simulate the proposed circuit for all the response.

### 4.2.1 AC RESPONSE

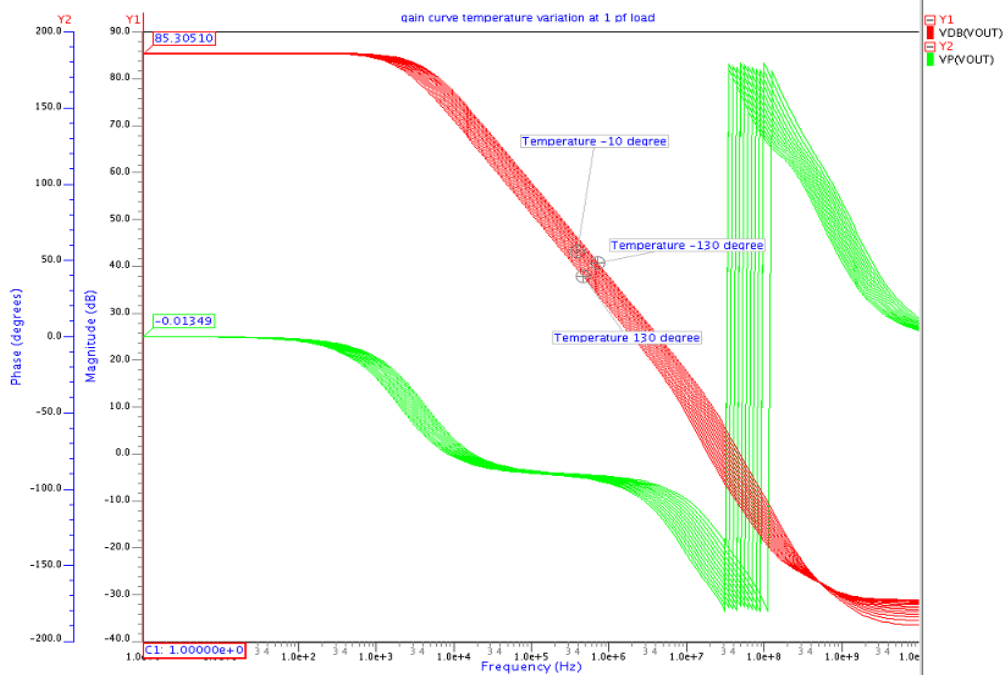


Fig 4.23 Frequency Response at load capacitance 1pF

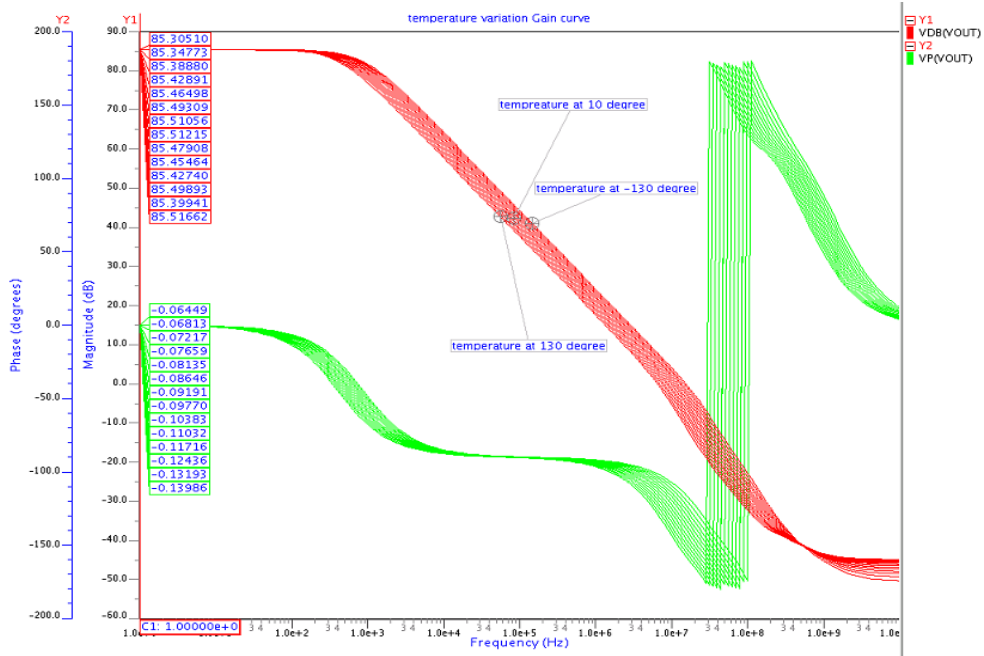
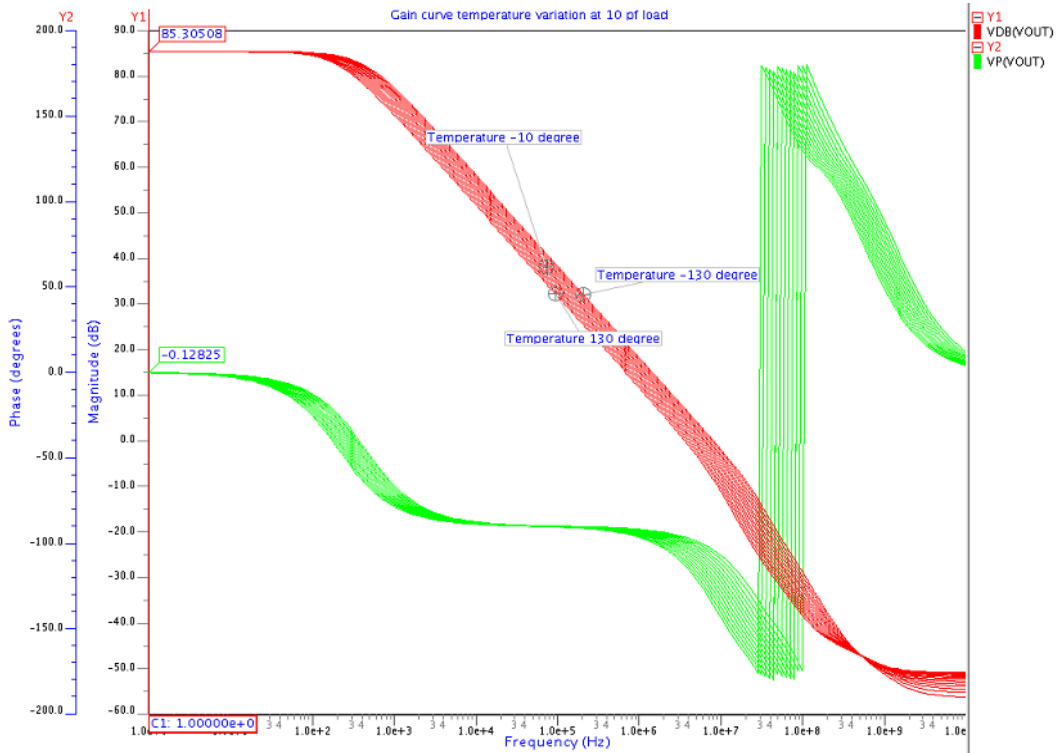


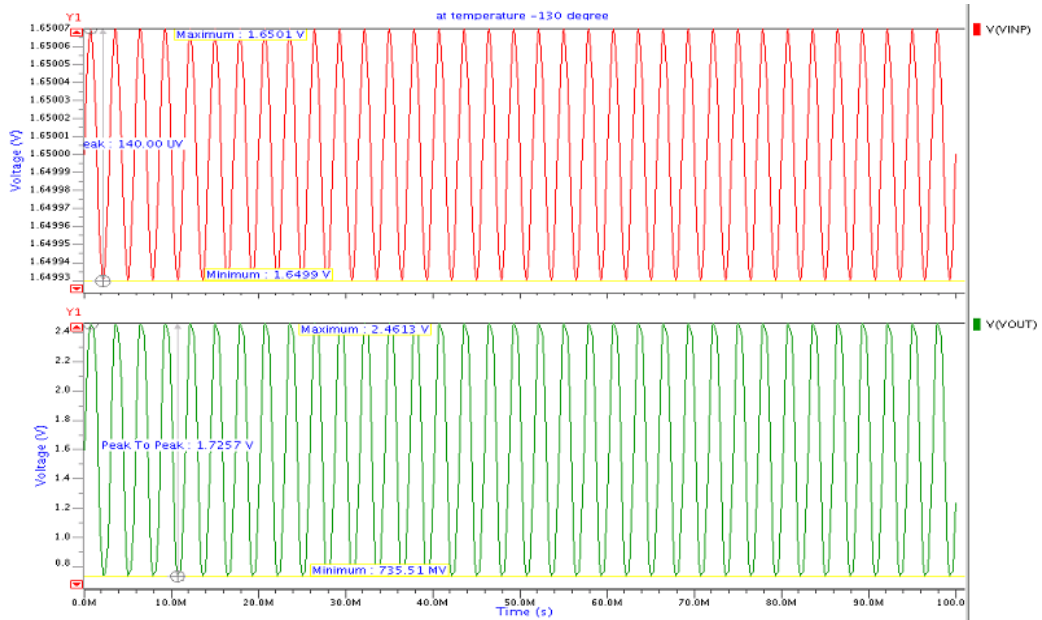
Fig 4.24 Frequency Response at load capacitance 5pF



**Fig 4.25 Frequency Response at load capacitance 10pF**

Variation in gain is negligible at such a wide temperature range. So it's good to work with such a wide temperature range with this op-amp.

#### 4.2.2 TRANSIENT RESULTS



**Fig 4.26 Output signals for transient analysis at -130°C**

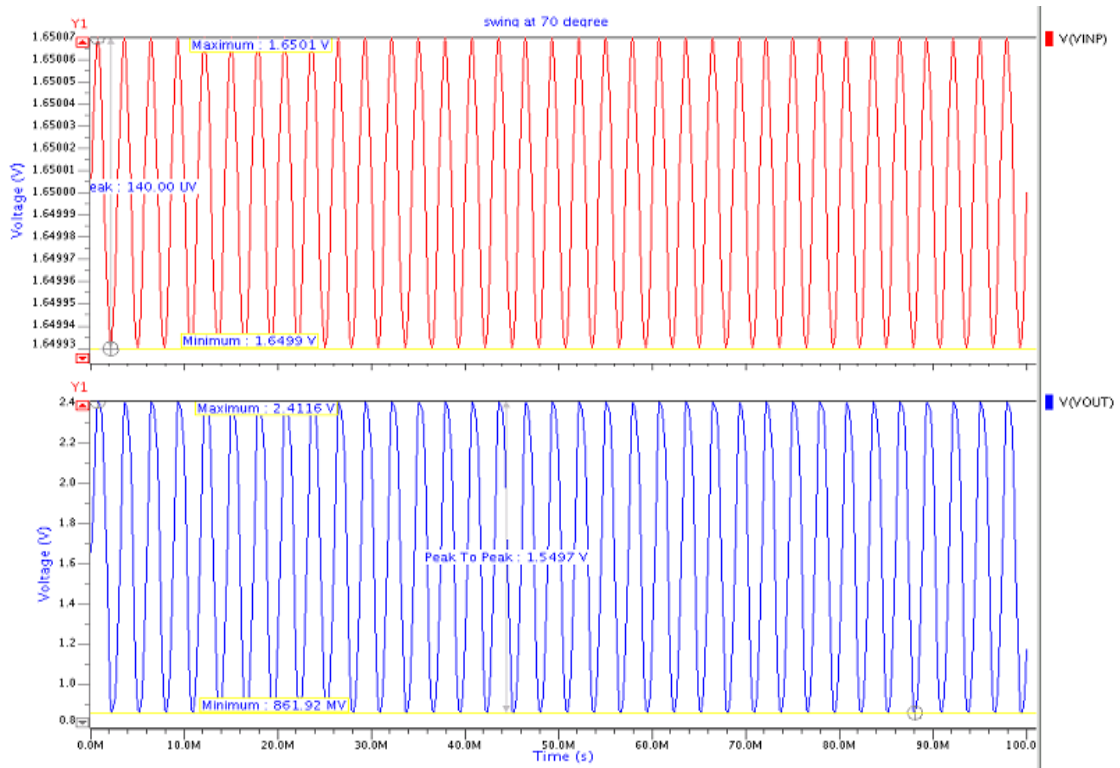


Fig 4.27 Output signals for transient analysis at 70°C

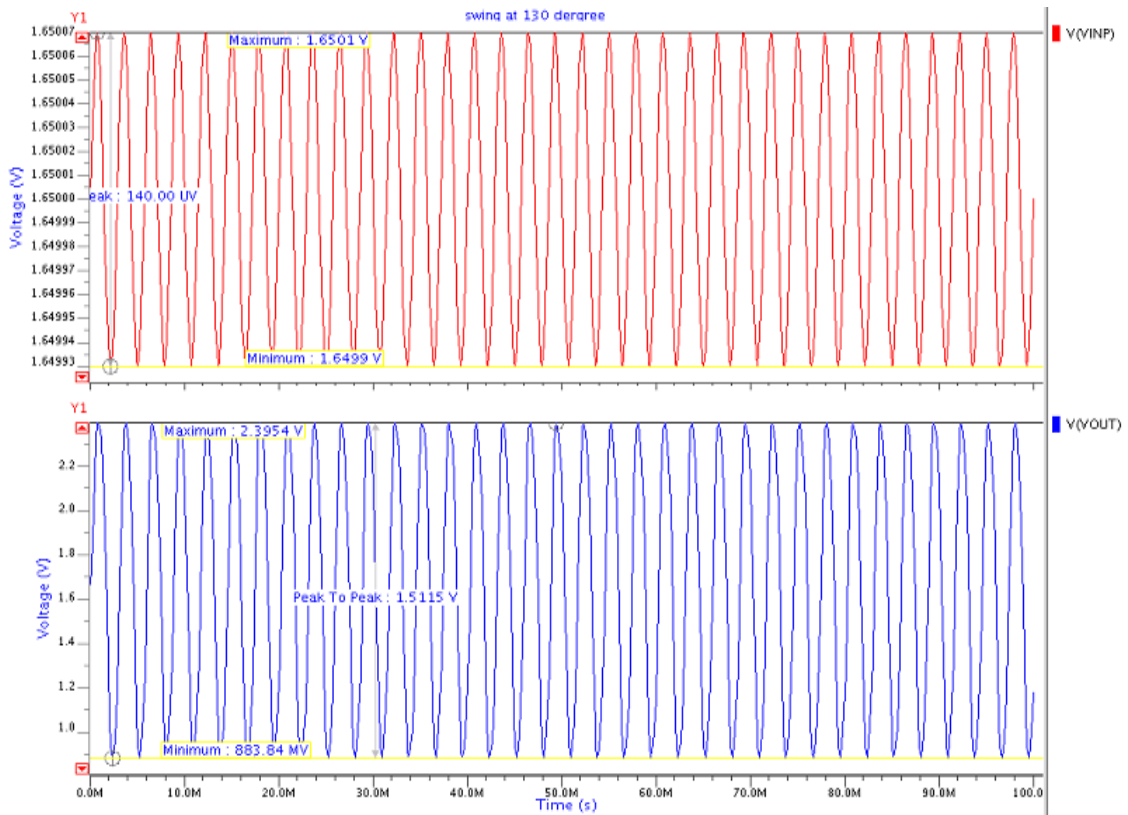


Fig 4.28 Output signals for transient analysis at 130°C

**Table 4.3 Output swing variation with temperature variation**

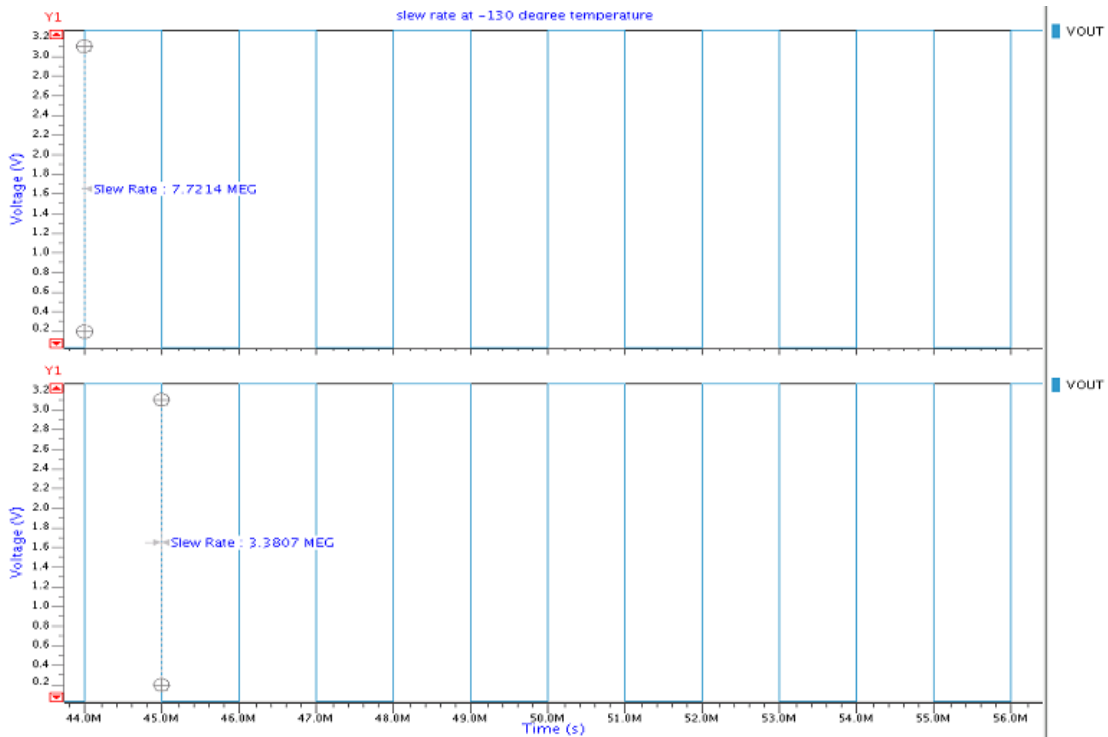
Temperature (°C)	Output swing (V)
-130	1.7257
70	1.5497
130	1.5115

At room temperature swing is 1.5855V. Table 4.3 shows a slight variation in swing with temperature.

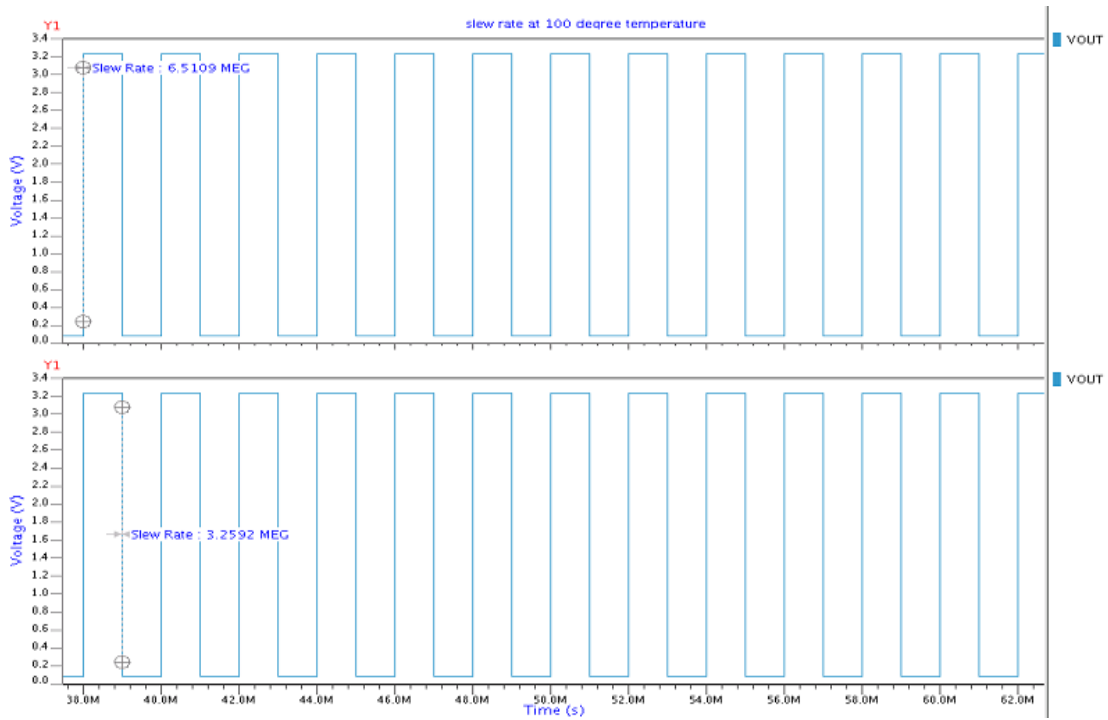
**4.2.3 STEP RESPONSE – SLEW RATE MEASUREMENT**

**Table 4.4 slew rate variation with temperature variation**

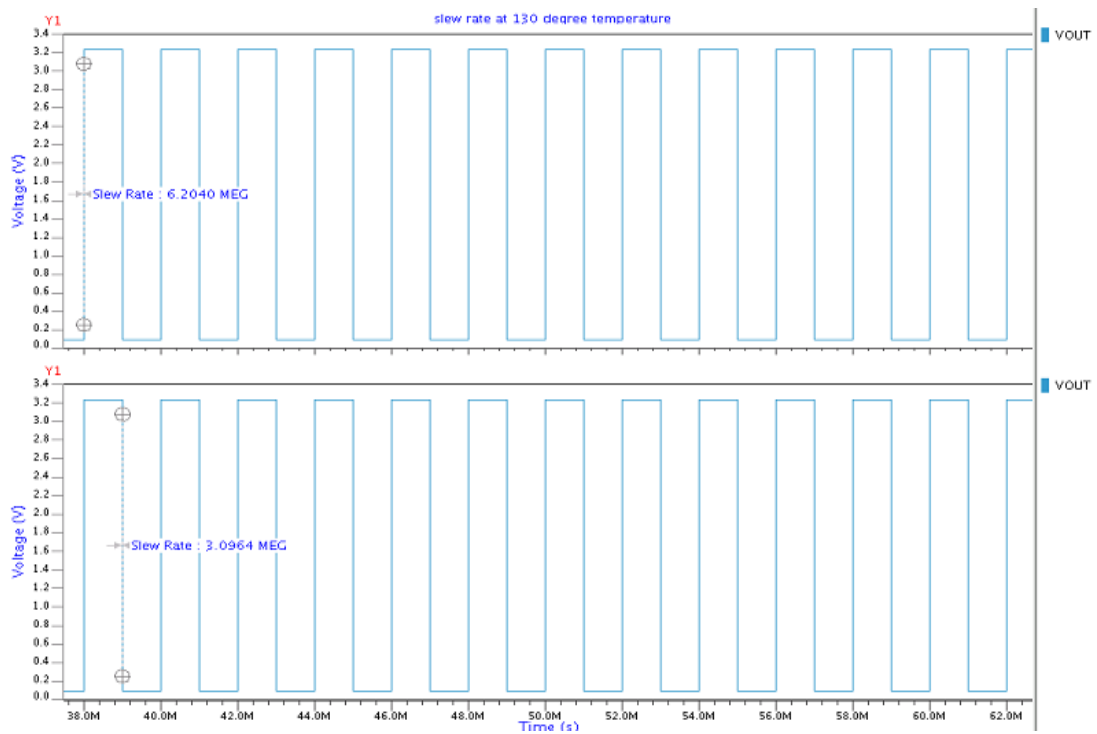
Temperature (°C)	Slew rate(V/μs)
-130	7.7214, 3.3807
100	6.5109, 3.2591
130	6.2040, 3.0964



**Fig 4.29 Slew rate for the rising and falling edge with operational amplifier in unity gain configuration at -130°C temperature**

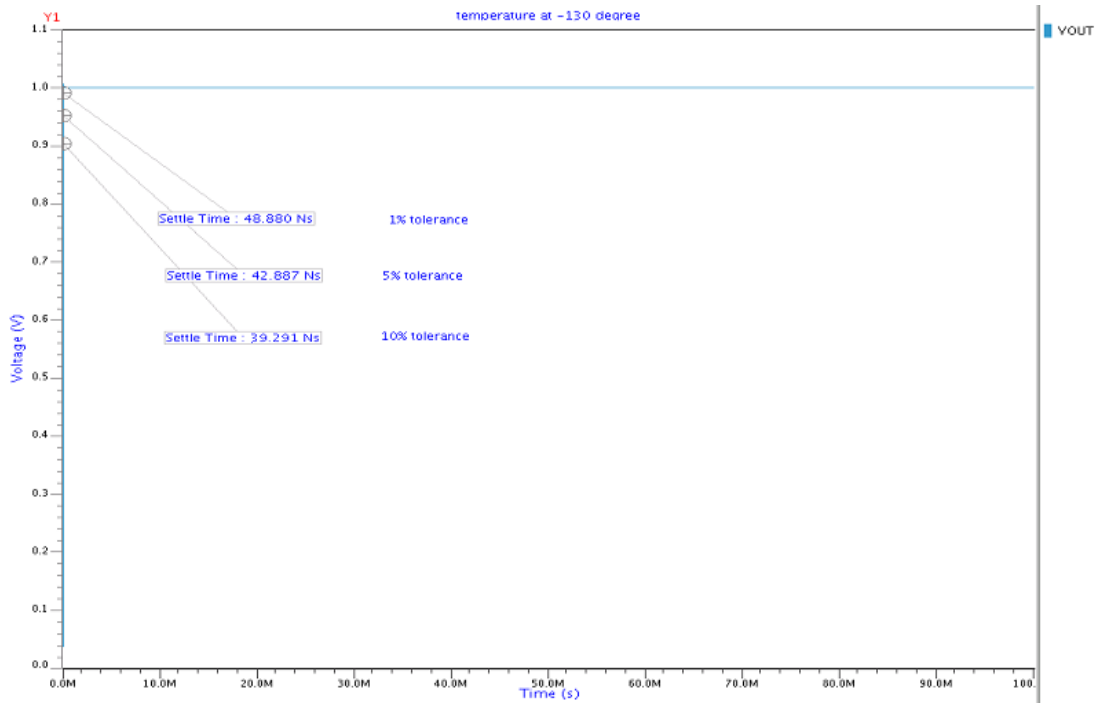


**Fig 4.30 Slew rate for the rising and falling edge with operational amplifier in unity gain configuration at 100°C temperature**

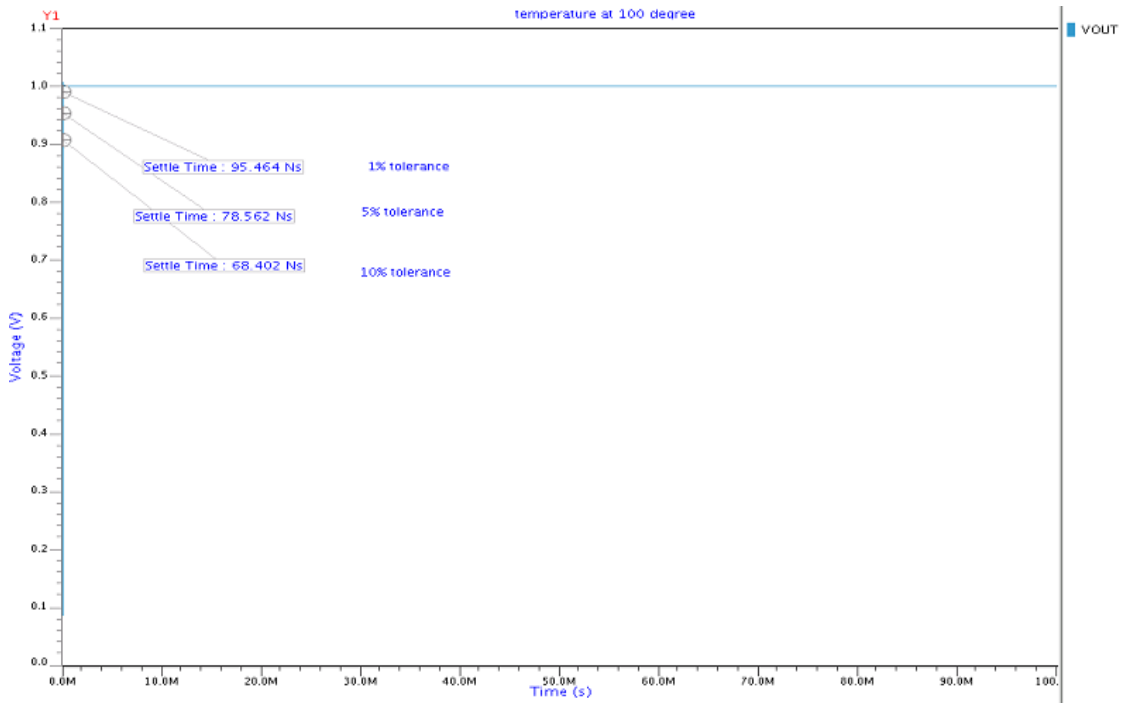


**Fig 4.31 Slew rate for the rising and falling edge with operational amplifier in unity gain configuration at 130°C temperature**

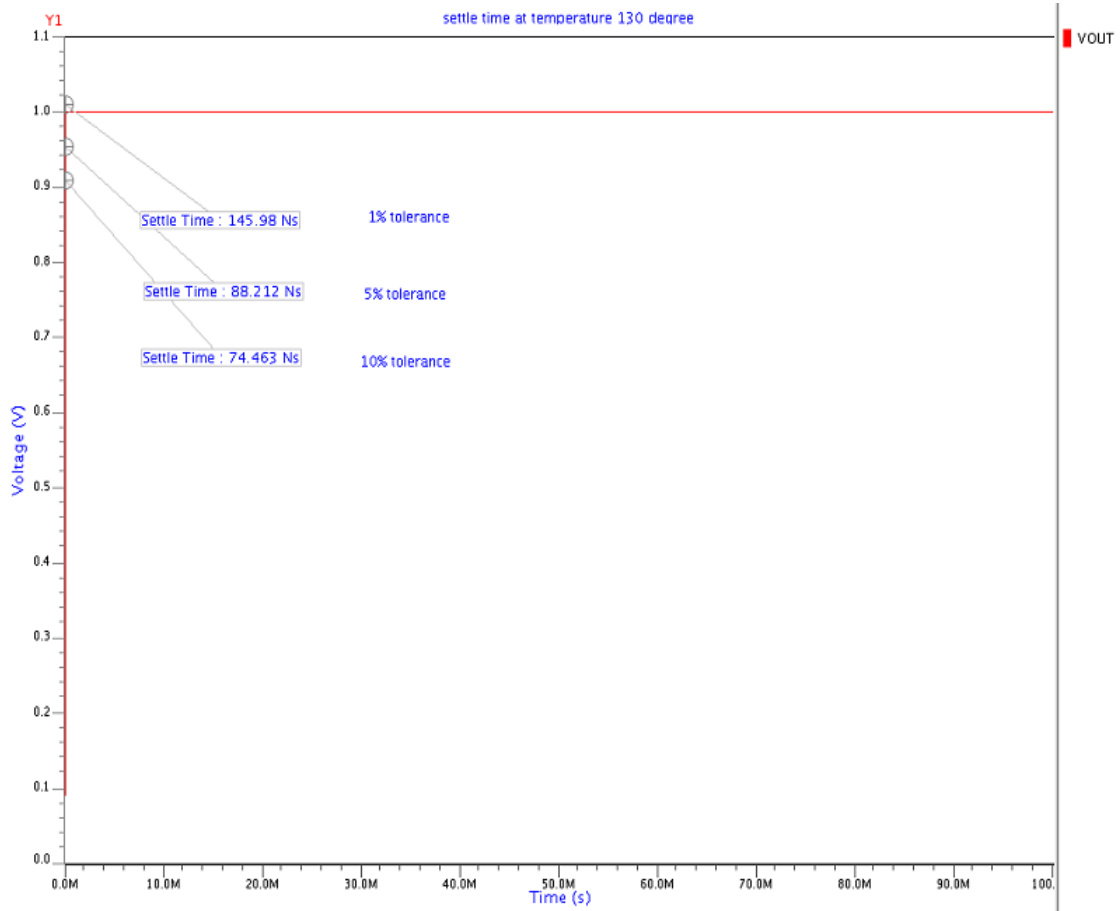
## 4.2.4 SETTLING TIME



**Fig 4.32 Settling time for the different tolerance values with unity gain configuration at -130°C temperature**



**Fig 4.33 Settling time for the different tolerance values with unity gain configuration at 100°C temperature**



**Fig 4.34 Settling time for the different tolerance values with unity gain configuration at 130°C temperature**

**Table 4.5 Settle time variation with temperature variation**

TEMPERATURE (°C)	Settling time(ns)		
	1% tolerance	5% tolerance	10% tolerance
-130	48.880	42.887	39.291
100	95.464	78.562	68.402
130	145.98	88.212	74.463

Settle time varies marginally with temperature. This variation shows that op-amp will go slow at the temperature increases.

## 4.2.5 COMMON MODE REJECTION RATIO

A very small variation in CMRR shown by the circuit. Performances will almost the same in wide temperature range.

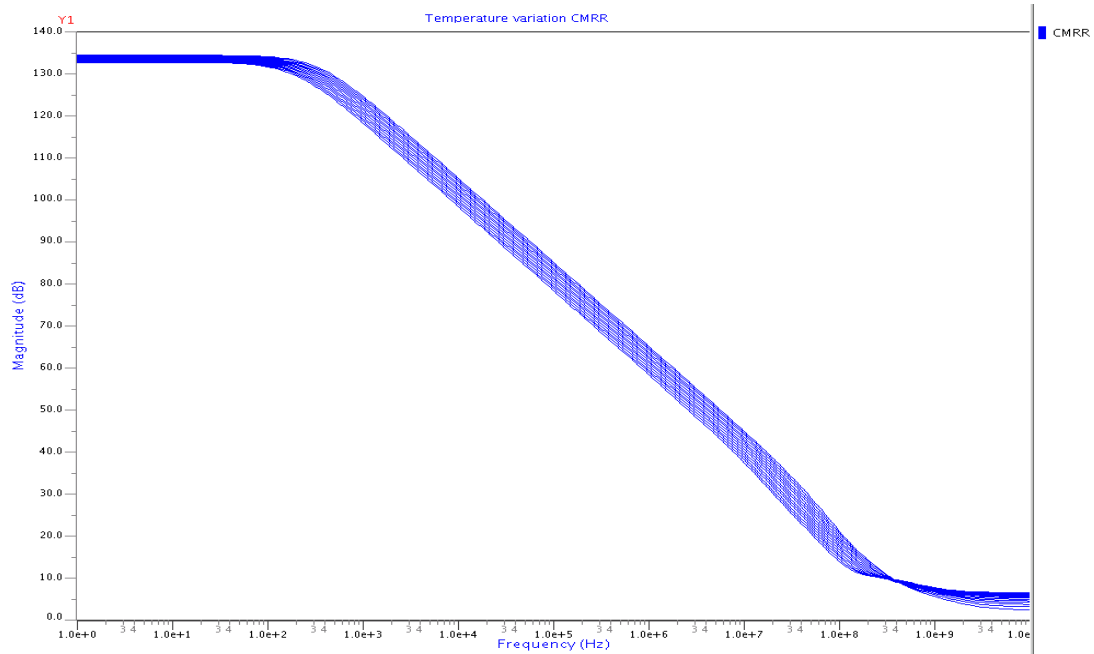


Fig 4.35 CMRR with temperature variation for wide range

## 4.2.6 POWER SUPPLY REJECTION RATIO

### POSITIVE PSRR

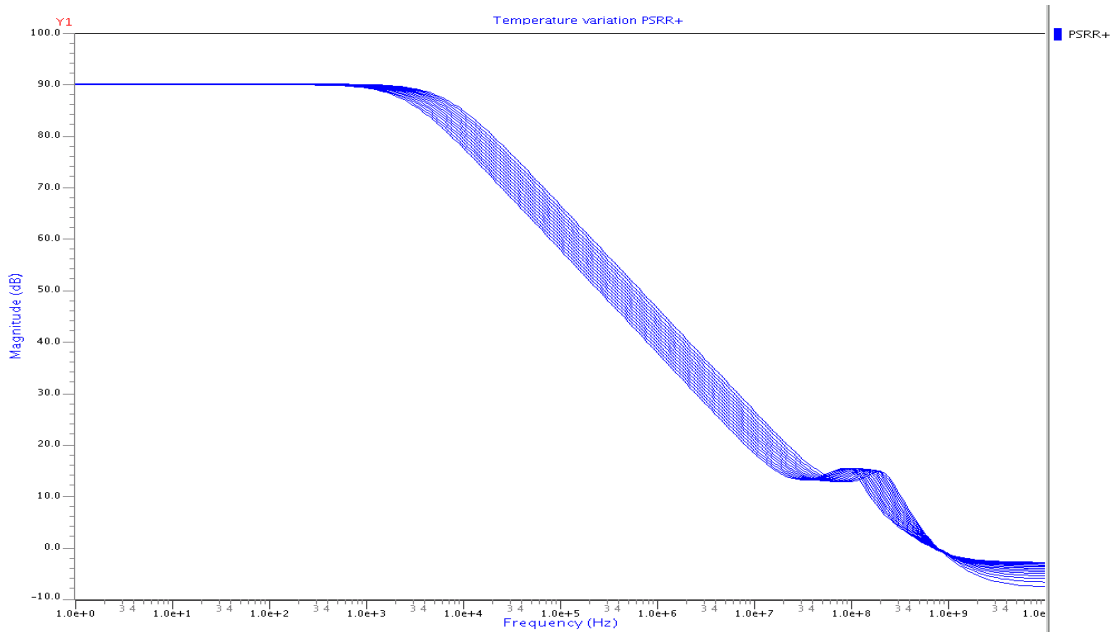


Fig 4.36 Positive PSRR with temperature variation for wide range

## NEGATIVE PSRR

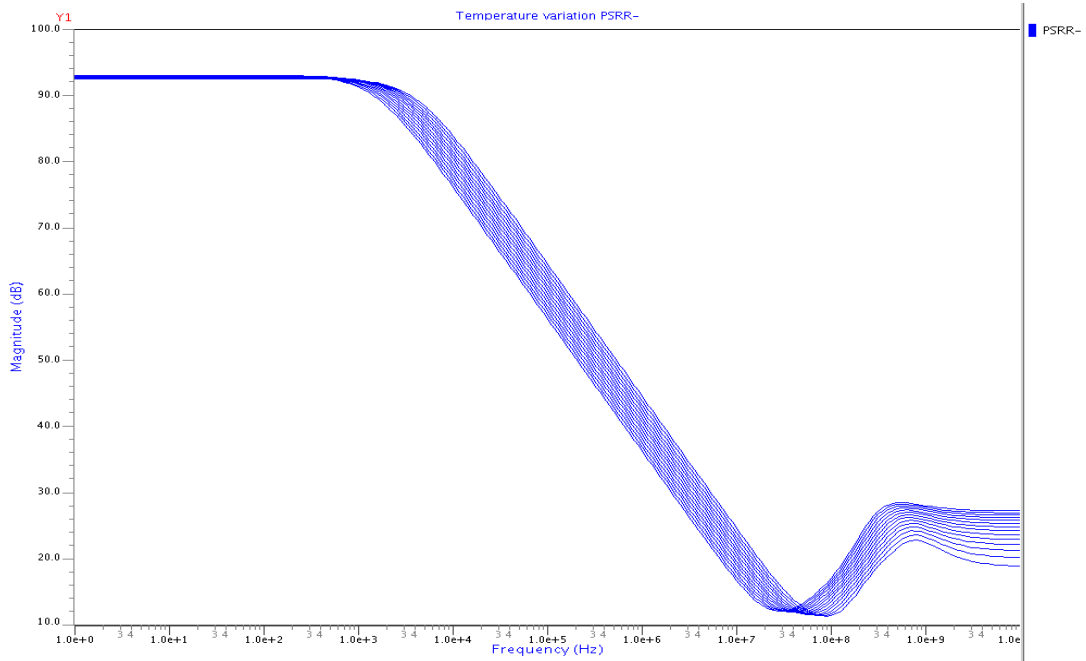


Fig 4.37 Negative PSRR with temperature variation for wide range

## 4.2.7 INPUT COMMON-MODE RANGE CHARACTERISTICS USING UNITY GAIN CONFIGURATION FOR TEMPERATURE VARIATION

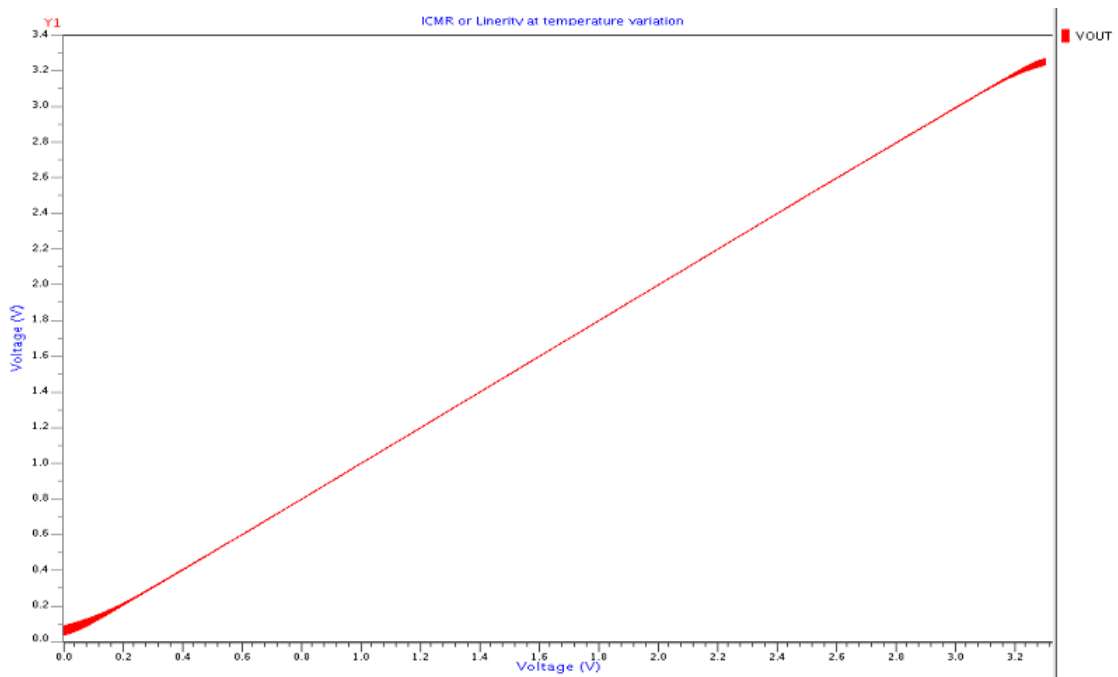


Fig 4.38 Simulation Result of Input Common-Mode Range for temperature variation

```

INFORMATION ABOUT COMPILATION...

Memory space allocated (bytes): 4659938
22 elements
13 nodes
3 input signals

ElDo VERSION : ELDO v6.9_1.1 Production(64 bits) Wed Jun 13 08:32:47 GMT 2007

*** DATE: 9-Jun-2009 09:22:13
*** TITLE: * Component: /home/sudhir/new Viewpoint: tsmc035a
TEMPERATURE : 27.000000 degrees C

Performing DC analysis...
--> Partitioning circuit...
***> DC CPU TIME 0s 000ms <***

DC:15 iterations FOR DC analysis
10          2.4999
11          2.4999
5           772,8873M
5A          2.5135
6           747,5960M
7           747,5960M
8           1.6496
A           887,7812M
B           887,7812M
N$3057     3.3000
VINM       1.6500
VINP       1.6500
VOUT       1.6496

TOTAL POWER DISSIPATION: 268.5437U WATTS

Connecting to JWDB server, please wait...
connected to wdb server : -jwdbhost localhost.localdomain -jwdbport 32828

***>AC analysis starts
***>AC analysis completed
***>CPU TIME 0s 020ms <***

***>Current simulation completed

SIMULATION INFORMATION
memory size allocated in bytes 5736473
nb of components: 58
nb of nodes: 49
nb of MOS or BIP calls: 982
Number of steps computed: 0

***>CPU TIME 0s 020ms <***

***>GLOBAL CPU TIME 0s 040ms <***

***>GLOBAL ELAPSED TIME 1s <***

Press the return key to continue.
□

```

**Fig 4.39 AC analysis Simulation ELDO**

**Table 4.6 Simulation Results of self biases Rail-to-Rail input Operational amplifier**

Specification parameters	Target specifications	Simulation Results
Input Trans-conductance		7.5%
Unity Gain Bandwidth (UGB)	10 MHz	9.17MHz
Low frequency gain	>50 dB	85.51dB
Power Consumption	<2 mW	268μW
Slew Rate	> 25 V/μs	7.27V/μs, 3.6227V/μs
Output offset voltage	-	42.87μV
Phase Margin	-	54.94°
PSRR+	-	90.18313dB
PSRR-	-	93.04908dB
CMRR	-	133.24dB
Settling Time (10%)	-	53.710Ns

### 4.3 LAYOUT

#### 4.3.1 ANALOG LAYOUT

When low-level or high-precision circuitry is being designed, a lot of care is usually given to the details of the circuit schematic and how the signal runs are routed. In doing layouts for digital circuits, the speed and the area are the two most important issues. In contrast, in doing layout for analog circuits, everything should be considered simultaneously.

In addition to the speed and the area, other equally critical considerations should be taken into account. In analog layout more care has to be taken as the circuit performance changes drastically due to noise, mismatches, crosstalk and shielding required to protect critical nodes from being disturbed. Without proper layout, the mismatches and the coupled noise would be quite large and would significantly degrade the performance of the amplifiers.

## 4.3.2 ANALOG LAYOUT ISSUES

### 1. MATCHING OF DEVICES

Device mismatch is too often treated as part of the black art of analog design. Random device mismatch plays an important role in the design of accurate analog circuits. The device mismatch is due to number factors like local process variation, global lithographic variations, local lithographic variations and process gradients. These factors affect all transistors, resistor, capacitors, and therefore similar techniques can be used to match all elements. During fabrication phase mismatch in physical parameters like doping concentration ( $N_a$ ), mobility ( $\mu$ ), oxide thickness ( $t_{ox}$ ) and layout dimensions ( $W, L$ ) gives origin to mismatch in electrical parameter like  $V_T$  and  $\beta$  and thus mismatch in  $I_D$ .

Matching of individual devices is of paramount concern in analog circuit design. Infact almost all of the 'analog layout techniques' are actually methods for improving matching between different devices on a chip. Matching is important because most analog circuit designs use a ratio based design technique. Some common techniques that help improve device matching are MULTI-GATE FINGER LAYOUT and COMMON-CENTROID LAYOUT.

Use of transistor fingering for large and critical transistors is always beneficial. In fingering the transistor is “fingered” into multiple transistors that are connected in parallel. The folded transistors reduce the source/ Drain junction area and the gate resistance. The gate resistance can be reduced by decomposing the transistor into more parallel fingers.

### 2. NOISE

Dynamic range is limited by noise and so it is an important parameter to be considered in all analog circuits. In general there are two types of noise, random noise and environmental noise. Random noise is consisting of a large number of transient disturbances with a statistically random time distribution. Thermal noise is an example of random noise. Random noise is dealt with at the circuit design level. However there are some layout techniques which can help to reduce random noise. The gate resistance of the poly-silicon and the neutral body region, which are both random noise sources, is reduced by multi-gate finger layout.

Other noise considers is environmental noise. Environmental noise is also dealt with at the circuit level. One common design technique used to minimize the effects of

environmental noise is to employ a 'fully-differential' circuit design, since environmental noise generally appears as a common-mode signal. However Substrate plugs is also very useful for reducing 'substrate noise', which is a particularly troublesome form of environmental noise encountered in highly integrated mixed-signal systems and Systems-On-Chip (SOC).

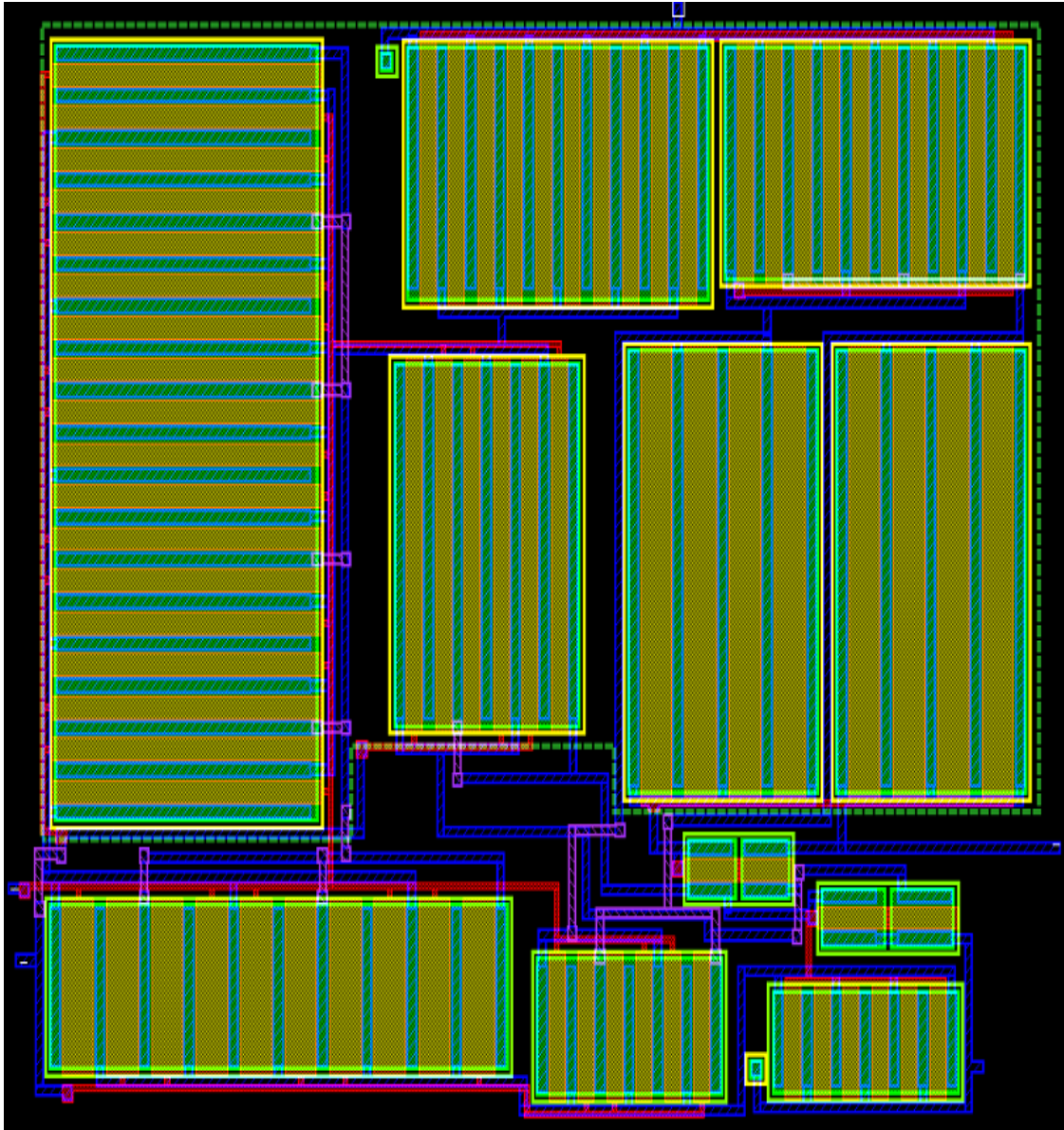
#### 4.3.3 LAYOUT OF OPERATIONAL AMPLIFIER

Due to huge aspect ratio some transistors are divided into multiple fingers. Fig 4.40 shows all the transistors with fingerings. Aspect ratio of M10 and M11 is 71.4/1.4. Since  $71.4 = 5 \times 14.28$  thus a single transistor is divided in to 5 fingers with width of  $14.28\mu m$ . Aspect ratio of M8 and M9 is 109.2/2.8. Since  $109.2 = 4 \times 27.3$  thus a single transistor is divided in to 4 fingers with width of  $27.3\mu m$ . Aspect ratio of M3a 155.4/1.4. Since  $155.4 = 10 \times 15.54$  thus a single transistor is divided in to 10 fingers with width of  $15.54\mu m$ . Aspect ratio of M1a and M2a is 67.2/1.4. Since  $67.2 = 3 \times 22.4$  thus a single transistor is divided in to 3 fingers with width of  $22.4\mu m$ . Aspect ratio of MP1 and MP2 is 211.4/1.4. Since  $211.4 = 9 \times 23.48$  thus a single transistor is divided in to 9 fingers with width of  $23.48\mu m$ . Aspect ratio of M1 and M2 is 25.2/1.4. Since  $25.2 = 3 \times 8.4$  thus a single transistor is divided in to 3 fingers with width of  $8.4\mu m$ . Aspect ratio of MN1 and MN2 is 50.4/1.4. Since  $50.4 = 5 \times 10.08$  thus a single transistor is divided in to 5 fingers with width of  $10.08\mu m$ . Aspect ratio of M3 is 37.8/1.4. Since  $37.8 = 6 \times 6.3$  thus a single transistor is divided in to 6 fingers with width of  $6.3\mu m$ .

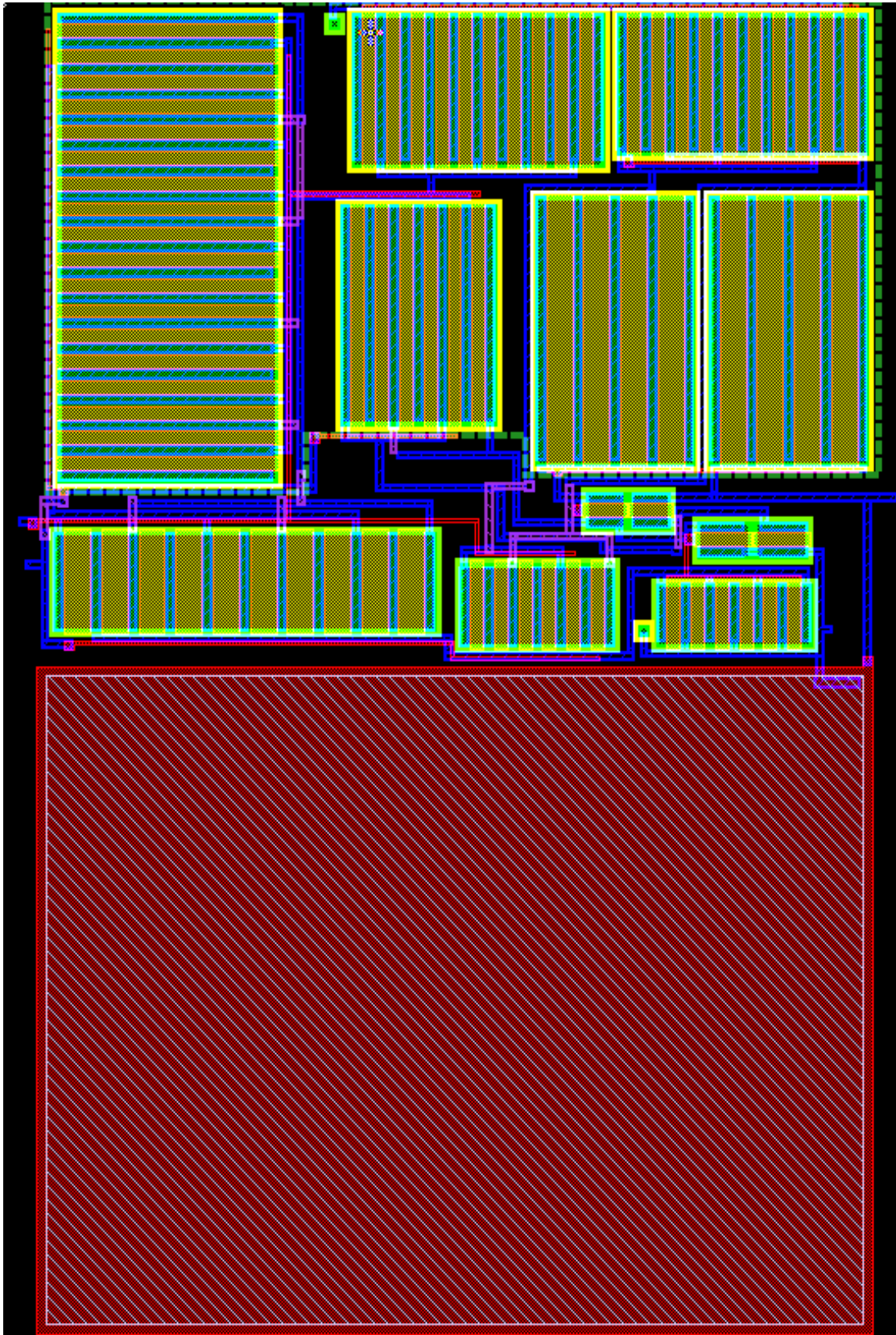
**Table 4.7 Transistor in their fingers aspect ratio**

Transistor	Aspect ratio (in schematic)	Number of finger	Aspect ratio (of each finger)
M1, M2	25.2/1.4	3	8.4/1.4
M1a, M2a	67.2/1.4	3	22.4/1.4
M4, M5	5.6/1.4	1	5.6/1.4
MP1,MP2	211.4/1.4	9	23.48/1.4
M6, M7	4.2/1.4	1	4.2/1.4
M8, M9	109.2/2.8	4	27.3/1.4
MN1, MN2	50.4/2.8	5	10.08/1.4

M10, M11	71.4/1.4	5	14.28/1.4
M3	37.8/1.4	6	6.3/1.4
M3a	155.4/1.4	10	15.54/1.4



**Fig 4.40 layout of all transistors divided in to fingers**



**Fig 4.41 layout of complete operational amplifier with capacitive load**

After completing layout LVS have to match with schematic the report of LVS checking is as follows:

**Table 4.8 LVS report**

```
#####
##                                ##
##          C A L I B R E      S Y S T E M      ##
##                                ##
##          L V S      R E P O R T      ##
##                                ##
#####
```

```
REPORT FILE NAME:      new.lvs.report
LAYOUT NAME:          new.calibre.gds
SOURCE NAME:          /home/sudhir/new/new.src.net ('new')
RULE FILE:            /home/sudhir/_tsmc035.rules_
LVS MODE:             Mask
RULE FILE NAME:       /home/sudhir/_tsmc035.rules_
CREATION TIME:        Mon May 25 10:58:06 2009
CURRENT DIRECTORY:    /home/sudhir
USER NAME:            sudhir
CALIBRE VERSION:      v2006.2_30.26      Fri Jul 7 22:37:10 PDT
2006
```

```
*****
*****
OVERALL COMPARISON RESULTS
*****
*****
```

```

#          #####
#          #          #          *          *
# #        # CORRECT #          |
# #        #          #          \_____/
#          #####
```

-----

INITIAL NUMBERS OF OBJECTS

-----

	Layout	Source	Component	Type
	-----	-----	-----	-----
Ports:	5	5		
Nets:	90	14	*	
Instances:	26	9	*	MN (4 pins)

	52	9	*	MP (4 pins)
	1	1		C (2 pins)
Total Inst:	79	19		

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	5	5	
Nets:	14	14	
Instances:	9	9	MN (4 pins)
	9	9	MP (4 pins)
	1	1	C (2 pins)
Total Inst:	19	19	

\* = Number of objects in layout different from number in source.

This checks all the connections in schematic with layout. After successful competing the LVS, PEX has to check which checks all the components values in schematic with layout and give information about parasitic if they come in to picture.

**Table 4.9 PEX report**

```

* File: new.pex.netlist
* Created: Mon May 25 11:37:05 2009
* Program "Calibre xRC"
* Version "v2006.2_30.26"
*
.include "new.pex.netlist.pex"
.subckt new VINP GND VINM VDD VOUT
*
* VOUT      VOUT
* VDD VDD
* GND GND
* VINP      VINP
* VINM      VINM
MN8__1 N_a_MN8__1_d N_VINP_MN8__1_g N_5_MN8__1_s N_GND_MN8__1_b n
L=2.8e-06
+ W=1.01e-05 AD=1.111e-11 AS=1.212e-11
MN9__1 N_b_MN9__1_d N_VINM_MN9__1_g N_5_MN9__1_s N_GND_MN8__1_b n
L=2.8e-06
+ W=1.01e-05 AD=1.212e-11 AS=1.212e-11
MN9__2 N_b_MN9__2_d N_VINM_MN9__2_g N_5_MN9__2_s N_GND_MN8__1_b n
L=2.8e-06
+ W=1.01e-05 AD=1.212e-11 AS=1.212e-11
MN8__2 N_a_MN8__2_d N_VINP_MN8__2_g N_5_MN8__2_s N_GND_MN8__1_b n
L=2.8e-06
+ W=1.01e-05 AD=1.212e-11 AS=1.212e-11

```

MN8\_\_3 N\_a\_MN8\_\_3\_d N\_VINP\_MN8\_\_3\_g N\_5\_MN8\_\_3\_s N\_GND\_MN8\_\_1\_b n  
 L=2.8e-06  
 + W=1.01e-05 AD=1.212e-11 AS=1.212e-11  
 MN9\_\_3 N\_b\_MN9\_\_3\_d N\_VINM\_MN9\_\_3\_g N\_5\_MN9\_\_3\_s N\_GND\_MN8\_\_1\_b n  
 L=2.8e-06  
 + W=1.01e-05 AD=1.212e-11 AS=1.212e-11  
 MN9\_\_4 N\_b\_MN9\_\_4\_d N\_VINM\_MN9\_\_4\_g N\_5\_MN9\_\_4\_s N\_GND\_MN8\_\_1\_b n  
 L=2.8e-06  
 + W=1.01e-05 AD=1.212e-11 AS=1.212e-11  
 MN8\_\_4 N\_a\_MN8\_\_4\_d N\_VINP\_MN8\_\_4\_g N\_5\_MN8\_\_4\_s N\_GND\_MN8\_\_1\_b n  
 L=2.8e-06  
 + W=1.01e-05 AD=1.212e-11 AS=1.212e-11  
 MN8\_\_5 N\_a\_MN8\_\_5\_d N\_VINP\_MN8\_\_5\_g N\_5\_MN8\_\_5\_s N\_GND\_MN8\_\_1\_b n  
 L=2.8e-06  
 + W=1.01e-05 AD=1.212e-11 AS=1.212e-11  
 MN9\_\_5 N\_b\_MN9\_\_5\_d N\_VINM\_MN9\_\_5\_g N\_5\_MN9\_\_5\_s N\_GND\_MN8\_\_1\_b n  
 L=2.8e-06  
 + W=1.01e-05 AD=1.111e-11 AS=1.212e-11  
 MN3\_\_1 N\_10\_MN3\_\_1\_d N\_VINP\_MN3\_\_1\_g N\_5\_MN3\_\_1\_s N\_GND\_MN8\_\_1\_b n  
 L=1.4e-06  
 + W=8.4e-06 AD=9.24e-12 AS=1.008e-11  
 MN4\_\_1 N\_11\_MN4\_\_1\_d N\_VINM\_MN4\_\_1\_g N\_5\_MN4\_\_1\_s N\_GND\_MN8\_\_1\_b n  
 L=1.4e-06  
 + W=8.4e-06 AD=1.008e-11 AS=1.008e-11  
 MN4\_\_2 N\_11\_MN4\_\_2\_d N\_VINM\_MN4\_\_2\_g N\_5\_MN4\_\_2\_s N\_GND\_MN8\_\_1\_b n  
 L=1.4e-06  
 + W=8.4e-06 AD=1.008e-11 AS=1.008e-11  
 MN3\_\_2 N\_10\_MN3\_\_2\_d N\_VINP\_MN3\_\_2\_g N\_5\_MN3\_\_2\_s N\_GND\_MN8\_\_1\_b n  
 L=1.4e-06  
 + W=8.4e-06 AD=1.008e-11 AS=1.008e-11  
 MN3\_\_3 N\_10\_MN3\_\_3\_d N\_VINP\_MN3\_\_3\_g N\_5\_MN3\_\_3\_s N\_GND\_MN8\_\_1\_b n  
 L=1.4e-06  
 + W=8.4e-06 AD=1.008e-11 AS=1.008e-11  
 MN2 N\_8\_MN2\_d N\_8\_MN2\_g N\_6\_MN2\_s N\_GND\_MN8\_\_1\_b n L=1.4e-06 W=4.2e-06  
 + AD=4.62e-12 AS=4.62e-12  
 MN4\_\_3 N\_11\_MN4\_\_3\_d N\_VINM\_MN4\_\_3\_g N\_5\_MN4\_\_3\_s N\_GND\_MN8\_\_1\_b n  
 L=1.4e-06  
 + W=8.4e-06 AD=9.24e-12 AS=1.008e-11  
 MN1 N\_VOUT\_MN1\_d N\_8\_MN1\_g N\_7\_MN1\_s N\_GND\_MN8\_\_1\_b n L=1.4e-06  
 W=4.2e-06  
 + AD=4.62e-12 AS=4.62e-12  
 MN5\_\_1 N\_5\_MN5\_\_1\_d N\_6\_MN5\_\_1\_g N\_GND\_MN5\_\_1\_s N\_GND\_MN8\_\_1\_b n  
 L=1.4e-06  
 + W=6.3e-06 AD=6.93e-12 AS=7.56e-12  
 MN5\_\_2 N\_5\_MN5\_\_2\_d N\_6\_MN5\_\_2\_g N\_GND\_MN5\_\_2\_s N\_GND\_MN8\_\_1\_b n  
 L=1.4e-06  
 + W=6.3e-06 AD=7.56e-12 AS=7.56e-12  
 MN7 N\_6\_MN7\_d N\_6\_MN7\_g N\_GND\_MN7\_s N\_GND\_MN8\_\_1\_b n L=1.4e-06  
 W=5.6e-06  
 + AD=6.16e-12 AS=6.16e-12  
 MN5\_\_3 N\_5\_MN5\_\_3\_d N\_6\_MN5\_\_3\_g N\_GND\_MN5\_\_3\_s N\_GND\_MN8\_\_1\_b n  
 L=1.4e-06  
 + W=6.3e-06 AD=7.56e-12 AS=7.56e-12  
 MN5\_\_4 N\_5\_MN5\_\_4\_d N\_6\_MN5\_\_4\_g N\_GND\_MN5\_\_4\_s N\_GND\_MN8\_\_1\_b n  
 L=1.4e-06  
 + W=6.3e-06 AD=7.56e-12 AS=7.56e-12

MN6 N\_7\_MN6\_d N\_6\_MN6\_g N\_GND\_MN6\_s N\_GND\_MN8\_\_1\_b n L=1.4e-06  
 W=5.6e-06  
 + AD=6.16e-12 AS=6.16e-12  
 MN5\_\_5 N\_5\_MN5\_\_5\_d N\_6\_MN5\_\_5\_g N\_GND\_MN5\_\_5\_s N\_GND\_MN8\_\_1\_b n  
 L=1.4e-06  
 + W=6.3e-06 AD=7.56e-12 AS=7.56e-12  
 MN5\_\_6 N\_5\_MN5\_\_6\_d N\_6\_MN5\_\_6\_g N\_GND\_MN5\_\_6\_s N\_GND\_MN8\_\_1\_b n  
 L=1.4e-06  
 + W=6.3e-06 AD=6.93e-12 AS=7.56e-12  
 MP8\_\_1 N\_a\_MP8\_\_1\_d N\_VINP\_MP8\_\_1\_g N\_5a\_MP8\_\_1\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.35e-05 AD=2.585e-11 AS=2.82e-11  
 MP9\_\_1 N\_b\_MP9\_\_1\_d N\_VINM\_MP9\_\_1\_g N\_5a\_MP9\_\_1\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.35e-05 AD=2.82e-11 AS=2.82e-11  
 MP9\_\_2 N\_b\_MP9\_\_2\_d N\_VINM\_MP9\_\_2\_g N\_5a\_MP9\_\_2\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.35e-05 AD=2.82e-11 AS=2.82e-11  
 MP8\_\_2 N\_a\_MP8\_\_2\_d N\_VINP\_MP8\_\_2\_g N\_5a\_MP8\_\_2\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.35e-05 AD=2.82e-11 AS=2.82e-11  
 MP8\_\_3 N\_a\_MP8\_\_3\_d N\_VINP\_MP8\_\_3\_g N\_5a\_MP8\_\_3\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.35e-05 AD=2.82e-11 AS=2.82e-11  
 MP9\_\_3 N\_b\_MP9\_\_3\_d N\_VINM\_MP9\_\_3\_g N\_5a\_MP9\_\_3\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.35e-05 AD=2.82e-11 AS=2.82e-11  
 MP9\_\_4 N\_b\_MP9\_\_4\_d N\_VINM\_MP9\_\_4\_g N\_5a\_MP9\_\_4\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.35e-05 AD=2.82e-11 AS=2.82e-11  
 MP8\_\_4 N\_a\_MP8\_\_4\_d N\_VINP\_MP8\_\_4\_g N\_5a\_MP8\_\_4\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.35e-05 AD=2.82e-11 AS=2.82e-11  
 MP8\_\_5 N\_a\_MP8\_\_5\_d N\_VINP\_MP8\_\_5\_g N\_5a\_MP8\_\_5\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.35e-05 AD=2.82e-11 AS=2.82e-11  
 MP9\_\_5 N\_b\_MP9\_\_5\_d N\_VINM\_MP9\_\_5\_g N\_5a\_MP9\_\_5\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.35e-05 AD=2.82e-11 AS=2.82e-11  
 MP9\_\_6 N\_b\_MP9\_\_6\_d N\_VINM\_MP9\_\_6\_g N\_5a\_MP9\_\_6\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.35e-05 AD=2.82e-11 AS=2.82e-11  
 MP8\_\_6 N\_a\_MP8\_\_6\_d N\_VINP\_MP8\_\_6\_g N\_5a\_MP8\_\_6\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.35e-05 AD=2.82e-11 AS=2.82e-11  
 MP8\_\_7 N\_a\_MP8\_\_7\_d N\_VINP\_MP8\_\_7\_g N\_5a\_MP8\_\_7\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.35e-05 AD=2.82e-11 AS=2.82e-11  
 MP9\_\_7 N\_b\_MP9\_\_7\_d N\_VINM\_MP9\_\_7\_g N\_5a\_MP9\_\_7\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.35e-05 AD=2.82e-11 AS=2.82e-11  
 MP9\_\_8 N\_b\_MP9\_\_8\_d N\_VINM\_MP9\_\_8\_g N\_5a\_MP9\_\_8\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.35e-05 AD=2.82e-11 AS=2.82e-11  
 MP8\_\_8 N\_a\_MP8\_\_8\_d N\_VINP\_MP8\_\_8\_g N\_5a\_MP8\_\_8\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.35e-05 AD=2.82e-11 AS=2.82e-11

MP8\_\_9 N\_a\_MP8\_\_9\_d N\_VINP\_MP8\_\_9\_g N\_5a\_MP8\_\_9\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.35e-05 AD=2.82e-11 AS=2.82e-11  
 MP9\_\_9 N\_b\_MP9\_\_9\_d N\_VINM\_MP9\_\_9\_g N\_5a\_MP9\_\_9\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.35e-05 AD=2.585e-11 AS=2.82e-11  
 MP7\_\_1 N\_7\_MP7\_\_1\_d N\_VINM\_MP7\_\_1\_g N\_5a\_MP7\_\_1\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.24e-05 AD=2.464e-11 AS=2.688e-11  
 MP3\_\_1 N\_5a\_MP3\_\_1\_d N\_10\_MP3\_\_1\_g N\_VDD\_MP3\_\_1\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=1.56e-05 AD=1.872e-11 AS=1.716e-11  
 MP6\_\_1 N\_6\_MP6\_\_1\_d N\_VINP\_MP6\_\_1\_g N\_5a\_MP6\_\_1\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.24e-05 AD=2.688e-11 AS=2.688e-11  
 MP3\_\_2 N\_5a\_MP3\_\_2\_d N\_10\_MP3\_\_2\_g N\_VDD\_MP3\_\_2\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=1.56e-05 AD=1.872e-11 AS=1.872e-11  
 MP6\_\_2 N\_6\_MP6\_\_2\_d N\_VINP\_MP6\_\_2\_g N\_5a\_MP6\_\_2\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.24e-05 AD=2.688e-11 AS=2.688e-11  
 MP3\_\_3 N\_5a\_MP3\_\_3\_d N\_10\_MP3\_\_3\_g N\_VDD\_MP3\_\_3\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=1.56e-05 AD=1.872e-11 AS=1.872e-11  
 MP7\_\_2 N\_7\_MP7\_\_2\_d N\_VINM\_MP7\_\_2\_g N\_5a\_MP7\_\_2\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.24e-05 AD=2.688e-11 AS=2.688e-11  
 MP3\_\_4 N\_5a\_MP3\_\_4\_d N\_10\_MP3\_\_4\_g N\_VDD\_MP3\_\_4\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=1.56e-05 AD=1.872e-11 AS=1.872e-11  
 MP7\_\_3 N\_7\_MP7\_\_3\_d N\_VINM\_MP7\_\_3\_g N\_5a\_MP7\_\_3\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.24e-05 AD=2.688e-11 AS=2.688e-11  
 MP3\_\_5 N\_5a\_MP3\_\_5\_d N\_10\_MP3\_\_5\_g N\_VDD\_MP3\_\_5\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=1.56e-05 AD=1.872e-11 AS=1.872e-11  
 MP6\_\_3 N\_6\_MP6\_\_3\_d N\_VINP\_MP6\_\_3\_g N\_5a\_MP6\_\_3\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=2.24e-05 AD=2.464e-11 AS=2.688e-11  
 MP3\_\_6 N\_5a\_MP3\_\_6\_d N\_10\_MP3\_\_6\_g N\_VDD\_MP3\_\_6\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=1.56e-05 AD=1.872e-11 AS=1.872e-11  
 MP3\_\_7 N\_5a\_MP3\_\_7\_d N\_10\_MP3\_\_7\_g N\_VDD\_MP3\_\_7\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=1.56e-05 AD=1.872e-11 AS=1.872e-11  
 MP3\_\_8 N\_5a\_MP3\_\_8\_d N\_10\_MP3\_\_8\_g N\_VDD\_MP3\_\_8\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=1.56e-05 AD=1.872e-11 AS=1.872e-11  
 MP5\_\_1 N\_8\_MP5\_\_1\_d N\_8\_MP5\_\_1\_g N\_10\_MP5\_\_1\_s N\_VDD\_MP8\_\_1\_b p  
 L=2.8e-06  
 + W=2.73e-05 AD=3.003e-11 AS=3.276e-11  
 MP3\_\_9 N\_5a\_MP3\_\_9\_d N\_10\_MP3\_\_9\_g N\_VDD\_MP3\_\_9\_s N\_VDD\_MP8\_\_1\_b p  
 L=1.4e-06  
 + W=1.56e-05 AD=1.872e-11 AS=1.872e-11  
 MP3\_\_10 N\_5a\_MP3\_\_10\_d N\_10\_MP3\_\_10\_g N\_VDD\_MP3\_\_10\_s N\_VDD\_MP8\_\_1\_b  
 p  
 + L=1.4e-06 W=1.56e-05 AD=1.872e-11 AS=1.716e-11

```

MP5__2 N_8_MP5__2_d N_8_MP5__2_g N_10_MP5__2_s N_VDD_MP8__1_b p
L=2.8e-06
+ W=2.73e-05 AD=3.276e-11 AS=3.276e-11
MP5__3 N_8_MP5__3_d N_8_MP5__3_g N_10_MP5__3_s N_VDD_MP8__1_b p
L=2.8e-06
+ W=2.73e-05 AD=3.276e-11 AS=3.276e-11
MP2__1 N_10_MP2__1_d N_10_MP2__1_g N_VDD_MP2__1_s N_VDD_MP8__1_b p
L=1.4e-06
+ W=1.43e-05 AD=1.573e-11 AS=1.716e-11
MP1__1 N_11_MP1__1_d N_10_MP1__1_g N_VDD_MP1__1_s N_VDD_MP8__1_b p
L=1.4e-06
+ W=1.43e-05 AD=1.716e-11 AS=1.716e-11
MP5__4 N_8_MP5__4_d N_8_MP5__4_g N_10_MP5__4_s N_VDD_MP8__1_b p
L=2.8e-06
+ W=2.73e-05 AD=3.003e-11 AS=3.276e-11
MP1__2 N_11_MP1__2_d N_10_MP1__2_g N_VDD_MP1__2_s N_VDD_MP8__1_b p
L=1.4e-06
+ W=1.43e-05 AD=1.716e-11 AS=1.716e-11
MP2__2 N_10_MP2__2_d N_10_MP2__2_g N_VDD_MP2__2_s N_VDD_MP8__1_b p
L=1.4e-06
+ W=1.43e-05 AD=1.716e-11 AS=1.716e-11
MP4__1 N_VOUT_MP4__1_d N_8_MP4__1_g N_11_MP4__1_s N_VDD_MP8__1_b p
L=2.8e-06
+ W=2.73e-05 AD=3.003e-11 AS=3.276e-11
MP2__3 N_10_MP2__3_d N_10_MP2__3_g N_VDD_MP2__3_s N_VDD_MP8__1_b p
L=1.4e-06
+ W=1.43e-05 AD=1.716e-11 AS=1.716e-11
MP1__3 N_11_MP1__3_d N_10_MP1__3_g N_VDD_MP1__3_s N_VDD_MP8__1_b p
L=1.4e-06
+ W=1.43e-05 AD=1.716e-11 AS=1.716e-11
MP4__2 N_VOUT_MP4__2_d N_8_MP4__2_g N_11_MP4__2_s N_VDD_MP8__1_b p
L=2.8e-06
+ W=2.73e-05 AD=3.276e-11 AS=3.276e-11
MP1__4 N_11_MP1__4_d N_10_MP1__4_g N_VDD_MP1__4_s N_VDD_MP8__1_b p
L=1.4e-06
+ W=1.43e-05 AD=1.716e-11 AS=1.716e-11
MP4__3 N_VOUT_MP4__3_d N_8_MP4__3_g N_11_MP4__3_s N_VDD_MP8__1_b p
L=2.8e-06
+ W=2.73e-05 AD=3.276e-11 AS=3.276e-11
MP2__4 N_10_MP2__4_d N_10_MP2__4_g N_VDD_MP2__4_s N_VDD_MP8__1_b p
L=1.4e-06
+ W=1.43e-05 AD=1.716e-11 AS=1.716e-11
MP2__5 N_10_MP2__5_d N_10_MP2__5_g N_VDD_MP2__5_s N_VDD_MP8__1_b p
L=1.4e-06
+ W=1.43e-05 AD=1.716e-11 AS=1.716e-11
MP4__4 N_VOUT_MP4__4_d N_8_MP4__4_g N_11_MP4__4_s N_VDD_MP8__1_b p
L=2.8e-06
+ W=2.73e-05 AD=3.003e-11 AS=3.276e-11
MP1__5 N_11_MP1__5_d N_10_MP1__5_g N_VDD_MP1__5_s N_VDD_MP8__1_b p
L=1.4e-06
+ W=1.43e-05 AD=1.573e-11 AS=1.716e-11
C1 N_VOUT_C1_pos N_GND_C1_neg 5.03332p
*
.include "new.pex.netlist.NEW.pxi"
*
.ends
*
*

```

## CHAPTER 5

### POST LAYOUT, PROCESS CORNER SIMULATION AND PADFRAM DESIGN

#### 5.1 POST LAYOUT SIMULATION

After completing the PEX. Post layout simulations have been done on extracted netlist. The simulation results of post layout simulation are given below.

##### 5.1.1 AC RESPONSE

Post layout gain curve is shown in Fig 5.1. The results show that there is a negligible variation in the performance of op-amp.

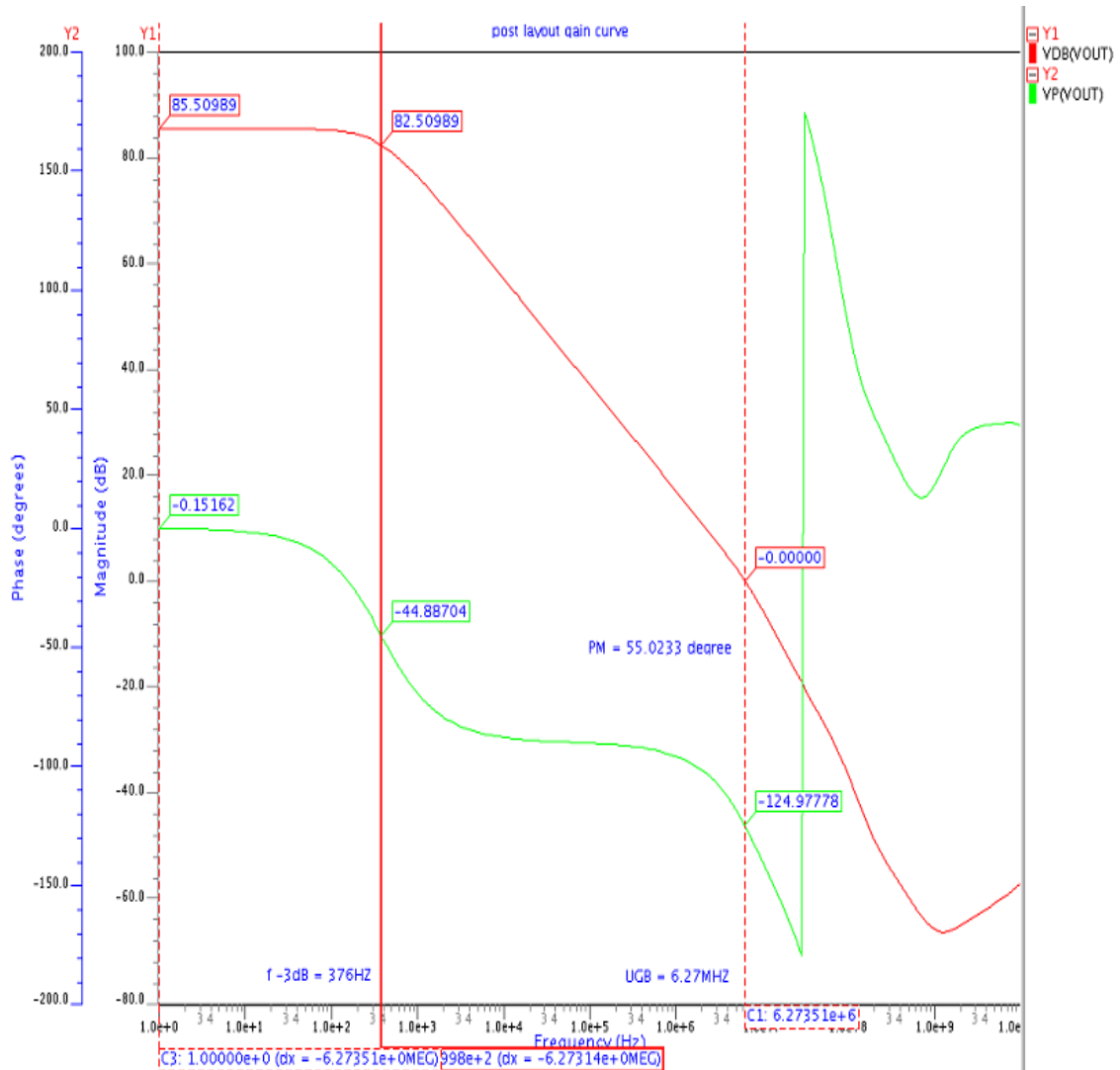


Fig 5.1 Post layout simulation AC analysis DC gain

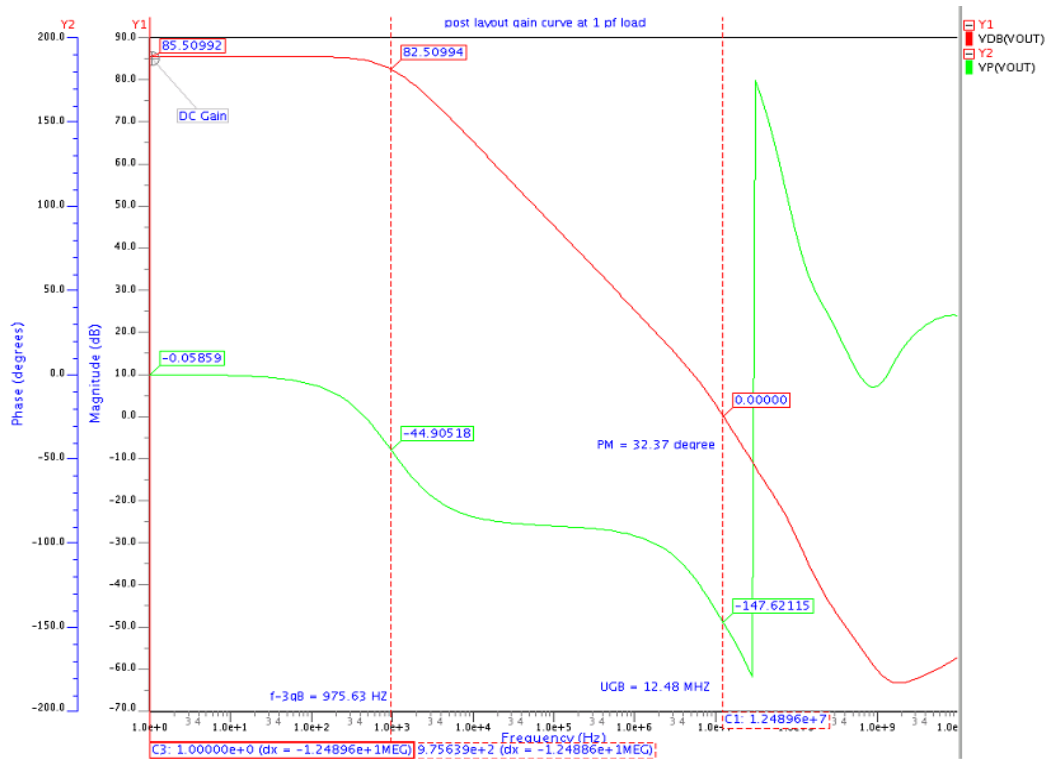


Fig 5.2 Post layout simulation AC analysis DC gain at 1pf load

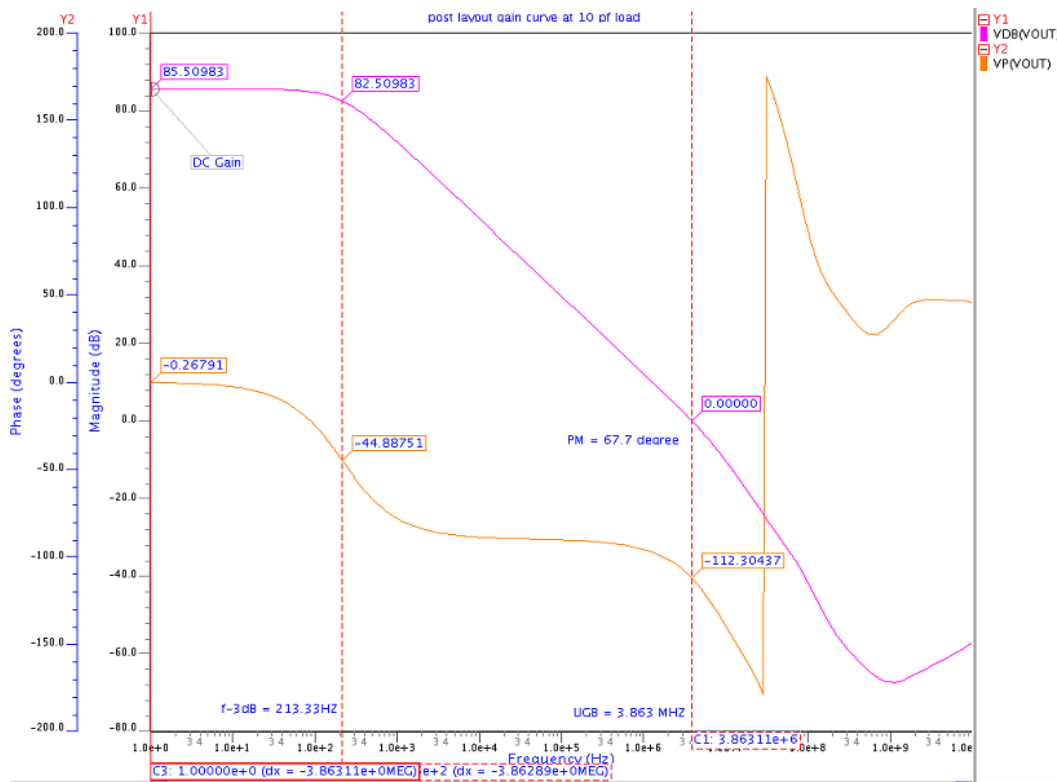


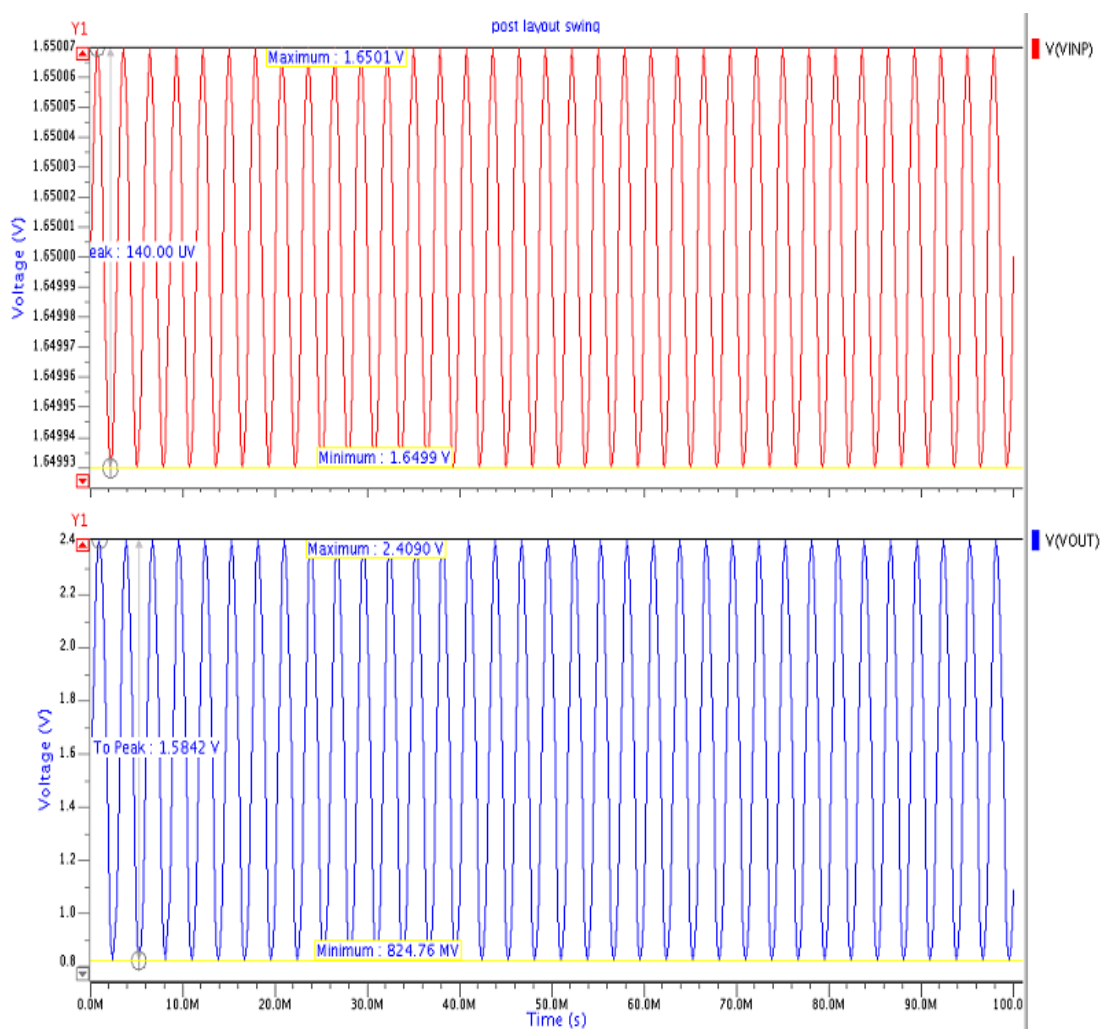
Fig 5.3 Post layout simulation AC analysis DC gain at 10pf load

**Table 5.1 Post layout ac analysis with load variation**

parameter	1pf	5pf	10pf
UGB(MHz)	12.48 MHz	7.27MHz	3.863
f-3dB(Hz)	975.63	376 Hz	213.33
Phase(degree)	32.37	55.0233	67.7
Gain(dB)	85.50992	85.50989	85.50983

### 5.1.2 TRANSIENT RESULTS

In layout peak-to-peak output swing is 1.5842V and maximum and minimum values are 2.409V, 824.76mV.



**Fig 5.4 Post layout simulation output swing**

### 5.1.3 STEP RESPONSE – SLEW RATE MEASUREMENT

With a unity gain feed back in layout step response is measured. Slew rate found is shown in Fig.5.5.

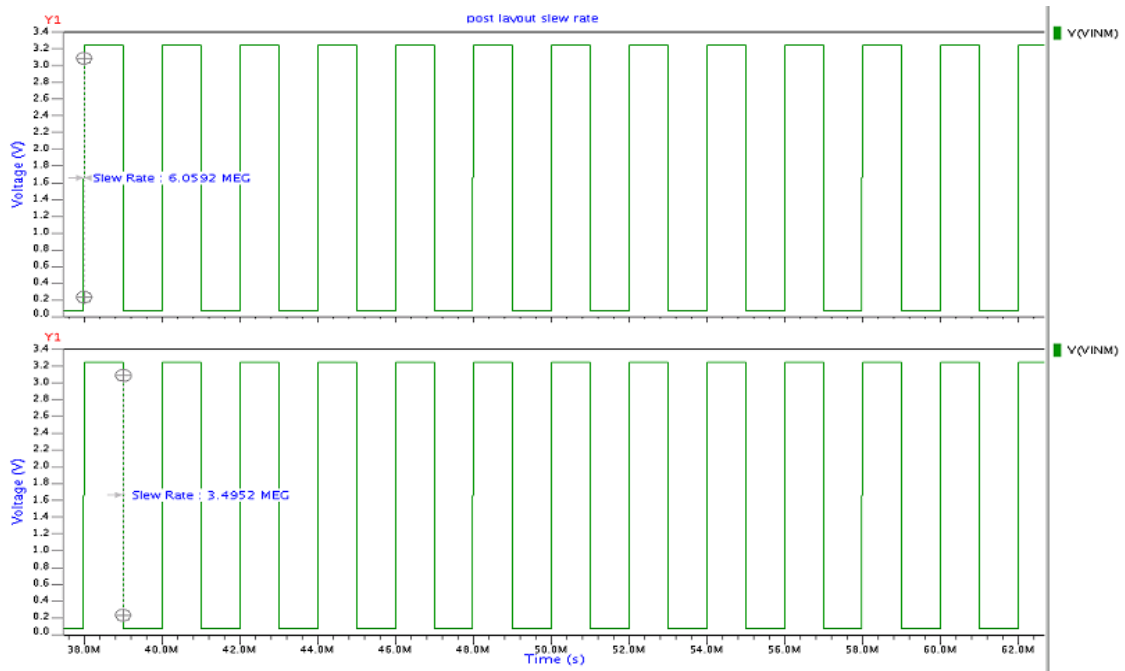


Fig 5.5 Post layout simulation slew rate

### 5.1.4 SETTling TIME

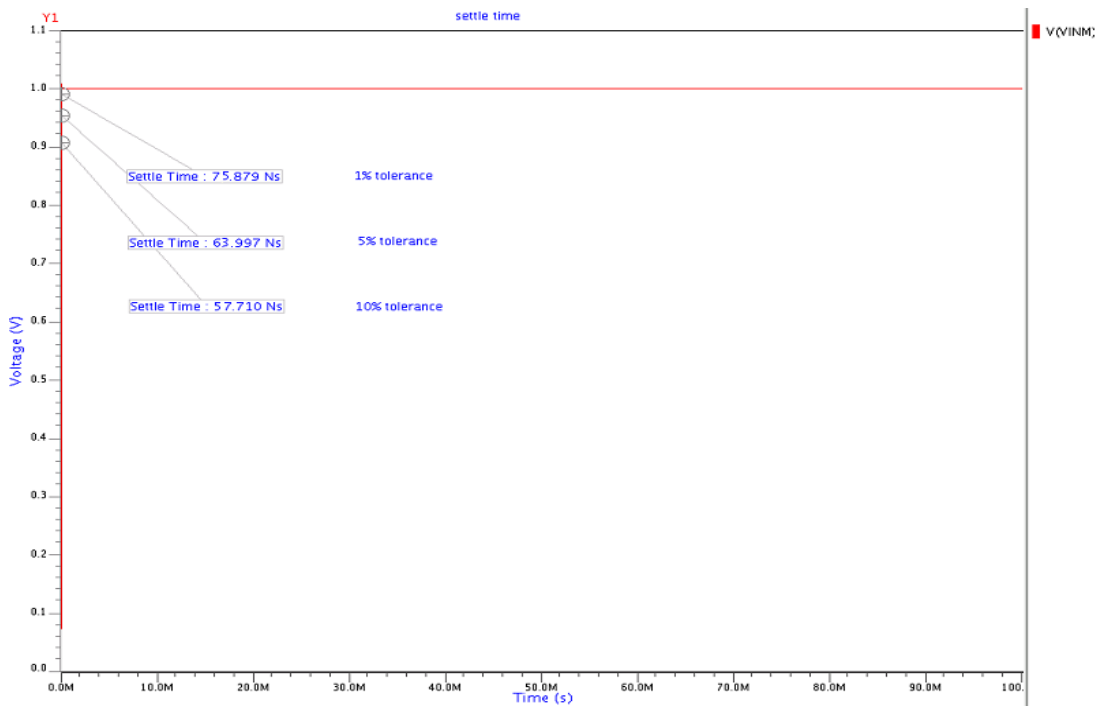
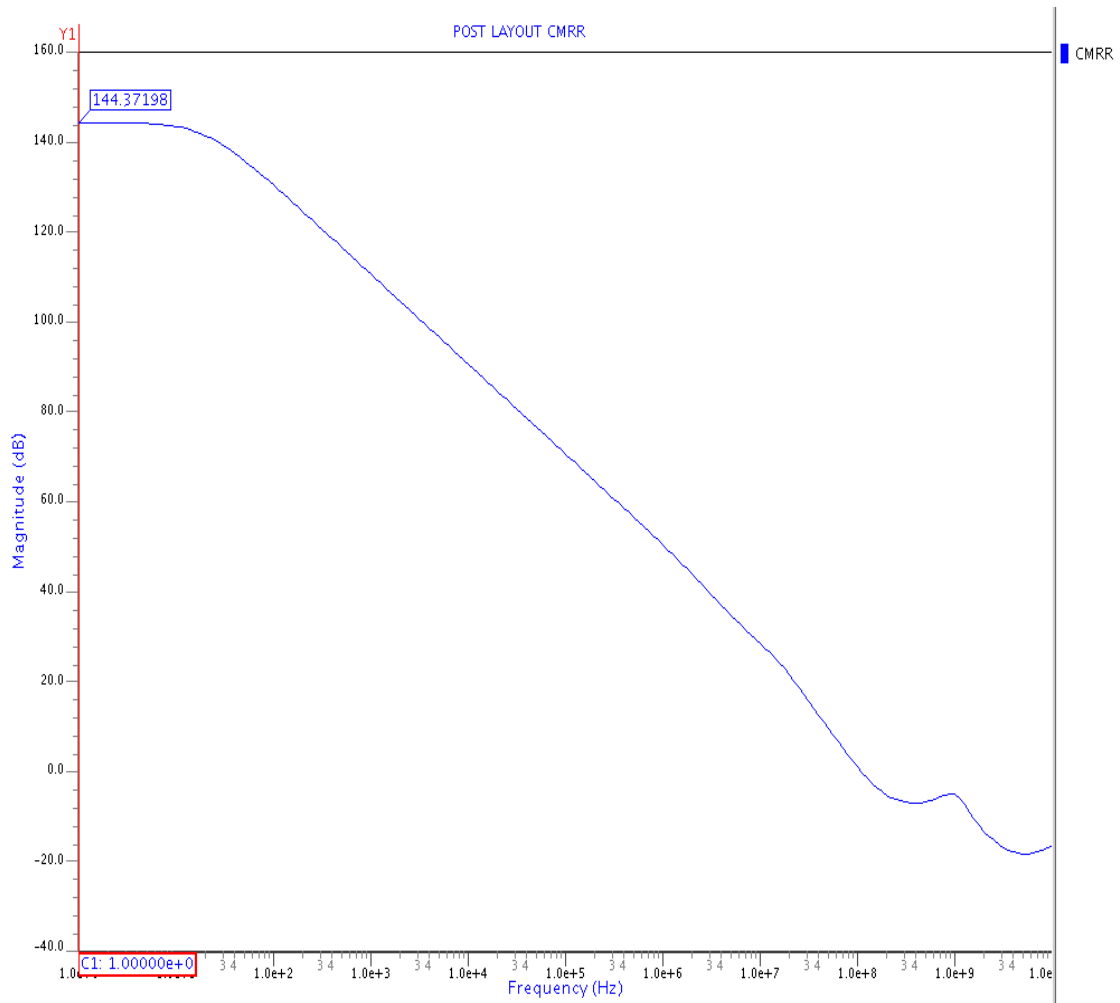


Fig 5.6 Post layout simulation settling time for the different tolerance values

Settling time with layout, simulation comes with some slightly high value then schematic simulation. This is due to parasitic addition in circuit.

### 5.1.5 COMMON MODE REJECTION RATIO

CMRR comes out as  $144.375\text{dB}$  which is higher than schematic simulation. Means CMRR of the circuit improves in layout.

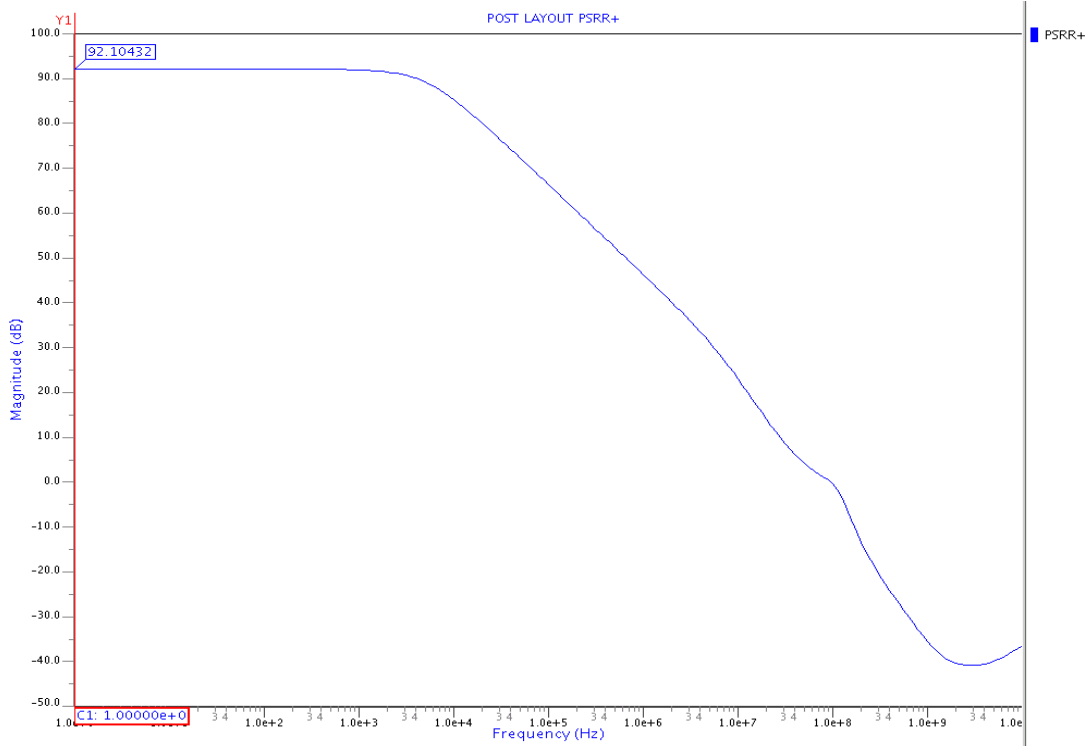


**Fig 5.7 Post layout simulation Common Mode Rejection Ratio**

### 5.1.6 POWER SUPPLY REJECTION RATIO

#### 5.1.6(A) POSITIVE PSRR

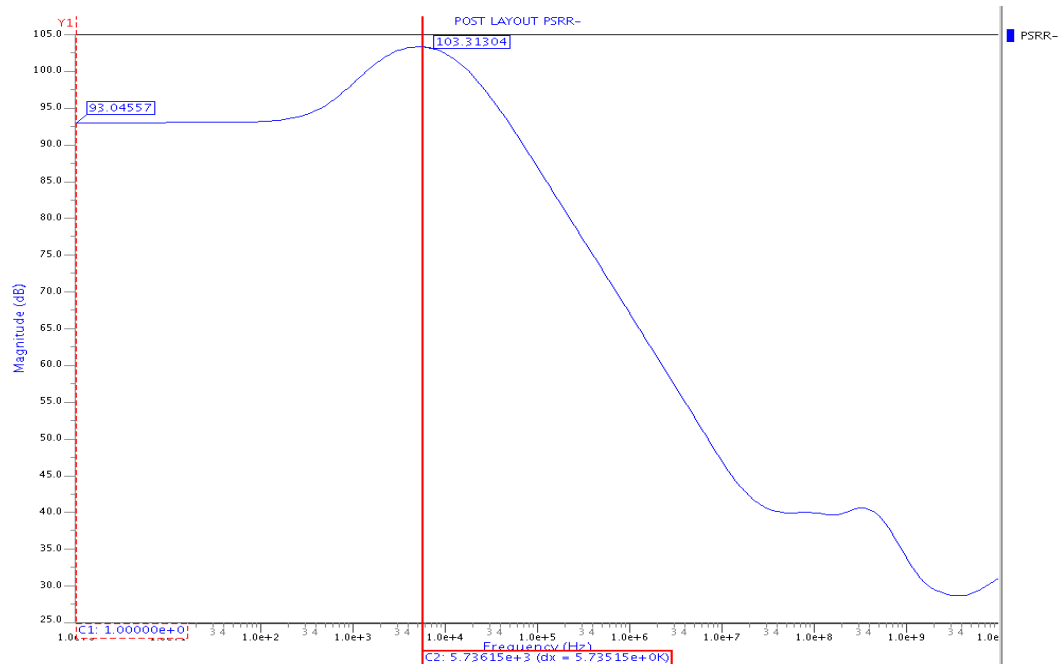
By applying 1V AC source between  $V_{DD}$  and op-amp circuit. PSRR+ is measured and found as shown in Fig 5.8.



**Fig 5.8 Post layout simulation Positive PSRR**

### 5.1.6(B) NEGATIVE PSRR

Test result for negative PSRR is measured by applying 1V AC source between ground and op-amp circuit. Result is in Fig 5.9.



**Fig 5.9 Post layout simulation Negative PSRR**

### 5.1.7 EFFECT OF COMMON MODE VARIATION ON THE DC GAIN

Effect of common mode input voltage variation is given in Fig 5.10.its in a tolerable range.

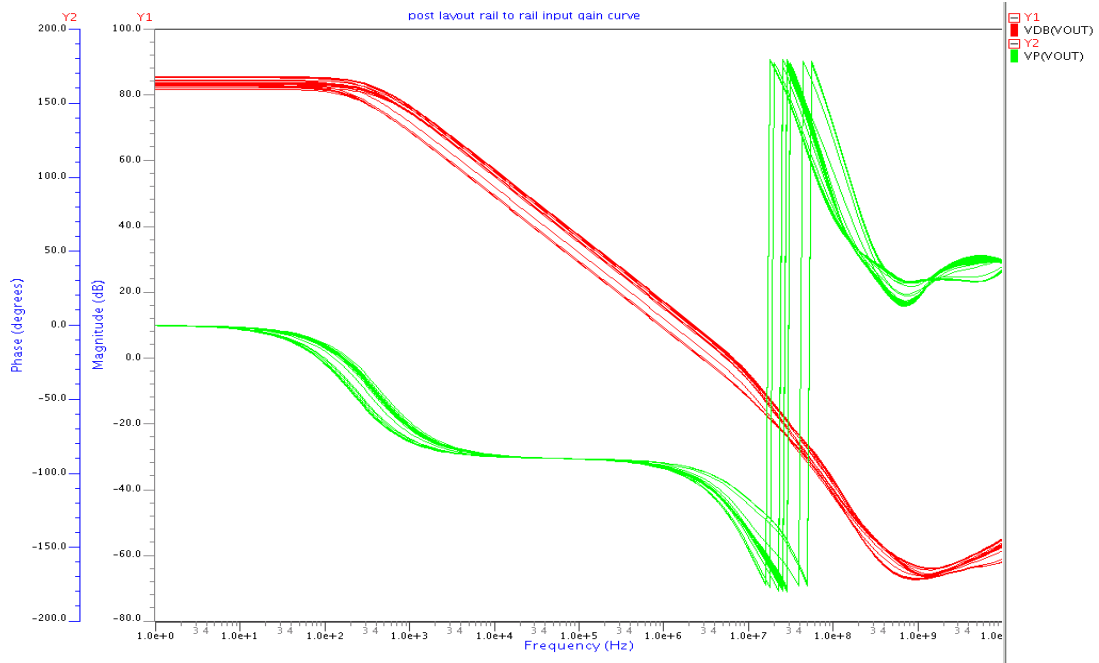


Fig 5.10 Post layout simulation common mode variation

### 5.1.8 INPUT COMMON-MODE RANGE CHARACTERISTICS

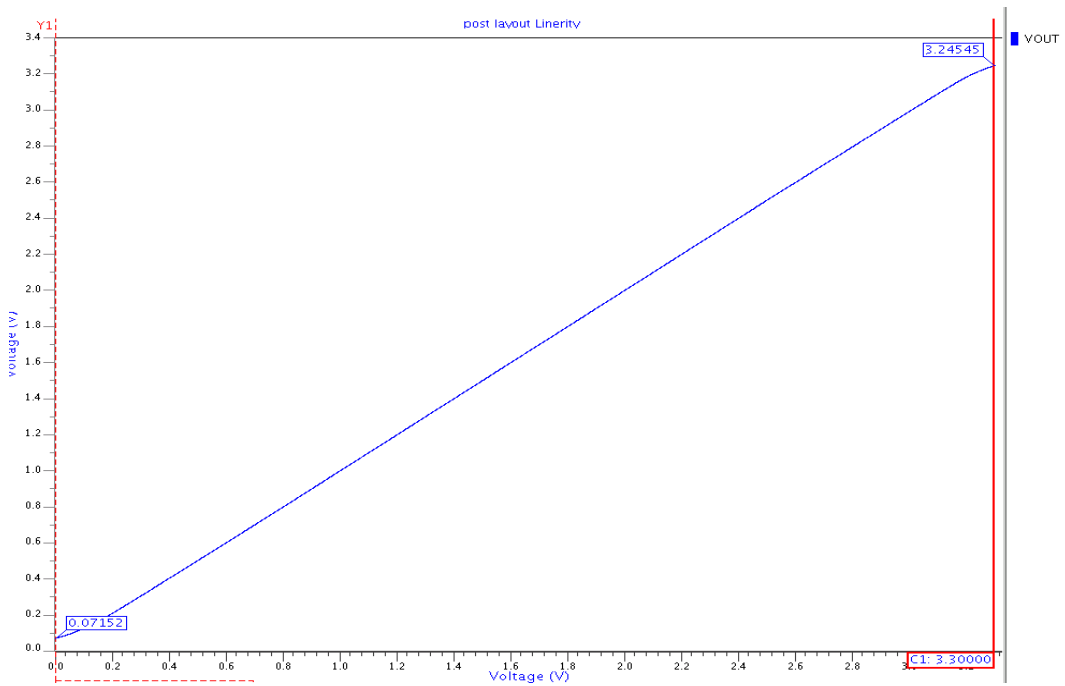


Fig 5.11 Post layout simulation ICMR

### 5.1.9 EFFECT OF VARIATION OF TEMPERATURE ON AC RESPONSE

Gain variation with temperature is negligible. So circuit is suitable for wide temperature range. The gain variation with temperature is shown in Fig 5.12.

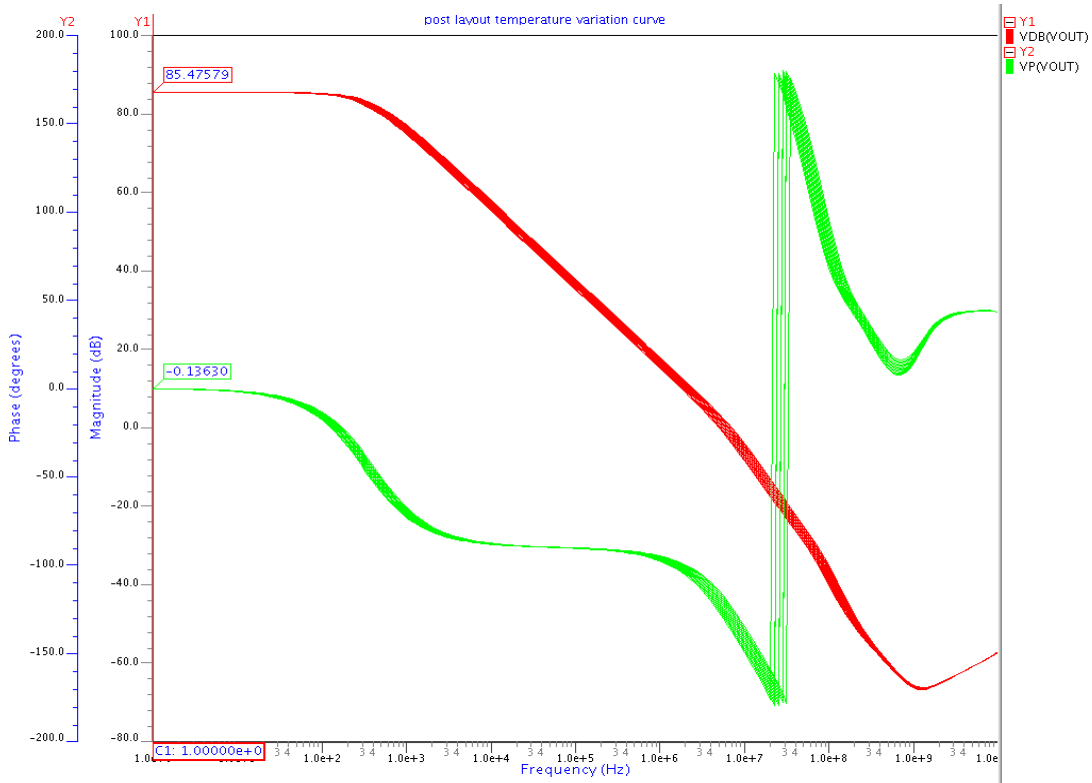


Fig 5.12 Post layout simulation Gain at temperature variation

Table 5.2 schematic and post layout result comparison

Specification parameters	Schematic Results	Post layout Results
Unity Gain Bandwidth (UGB)	9.17MHz	6.27MHz
Low frequency gain	85.51dB	85.50989 dB
Slew Rate	7.27V/ $\mu$ s, 3.622V/ $\mu$ s	6.059V/ $\mu$ s, 3.495V/ $\mu$ s
Phase Margin	54.94°	55.0223°
PSRR+	90.18313dB	92.10423dB
PSRR-	93.04908dB	93.04557 dB
CMRR	133.24dB	144.37198 dB
Settling Time (10%)	53.710Ns	57.71 Ns

## 5.2 PROCESS CORNER SIMULATION

Process corner simulation deals with variation in parameter during fabrication. Simulation has been done on extracted netlist from layout. The netlist extracted also includes two more netlist, one is distributed RC network netlist, which contains distributed RC network formed by considering resistances and parasitic capacitances of different devices and routing in layout. Another netlist included is the netlist of coupling capacitors in adjacent layers. Due to these parasitic care has to be taken for process corners.

Here in this simulation, process parameter like oxide thickness, mobility and electrical parameter threshold voltage are considered with variations of 15% in each.

For n-MOS to be fast,  $V_{th} = 0.466V$   $u_0 = 484.5941$   $t_{ox} = 6.63E-9$

For n-MOS to be slow,  $V_{th} = 0.63144V$   $u_0 = 358.178$   $t_{ox} = 8.97E-9$

For p-MOS to be fast,  $V_{th} = 0.57864V$   $u_0 = 178.847$   $t_{ox} = 6.63E-9$

For p-MOS to be slow,  $V_{th} = 0.782874V$   $u_0 = 132.191$   $t_{ox} = 8.97E-9$

### 5.2.1 AC RESPONSE

Fig 5.13 to 5.16 shows process corner, ac analysis of op-amp circuit.

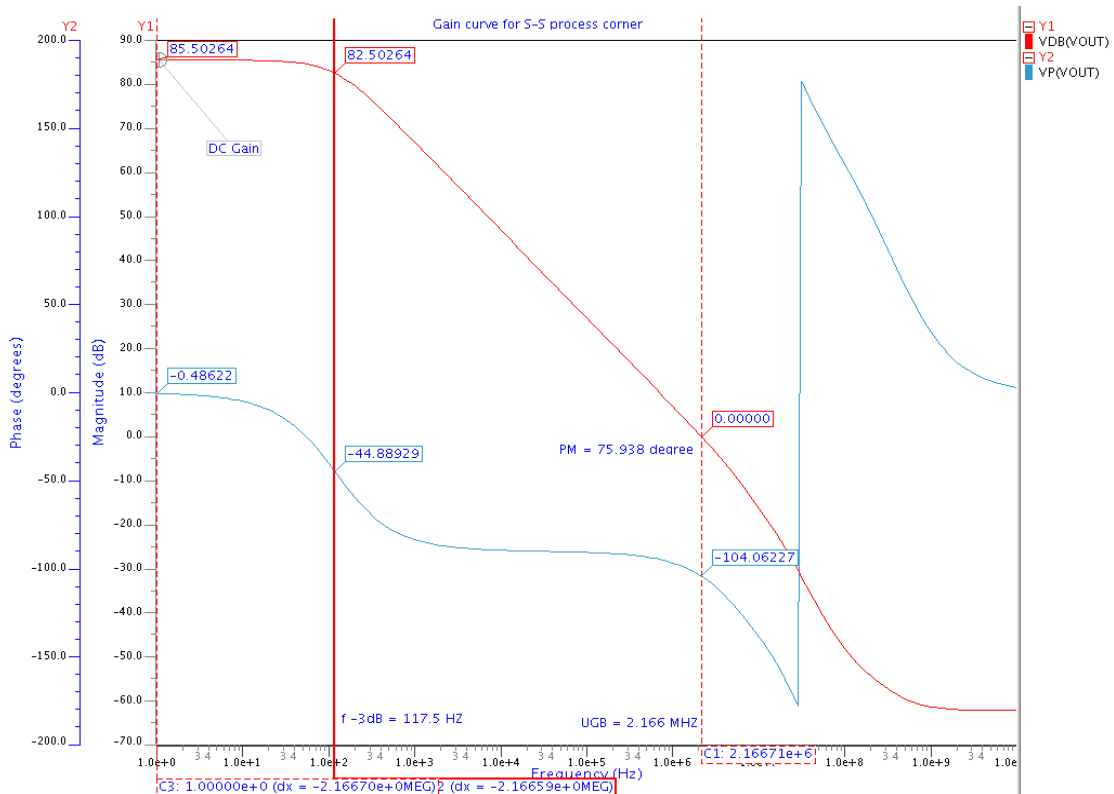


Fig 5.13 Process corner S-S simulation for AC analysis

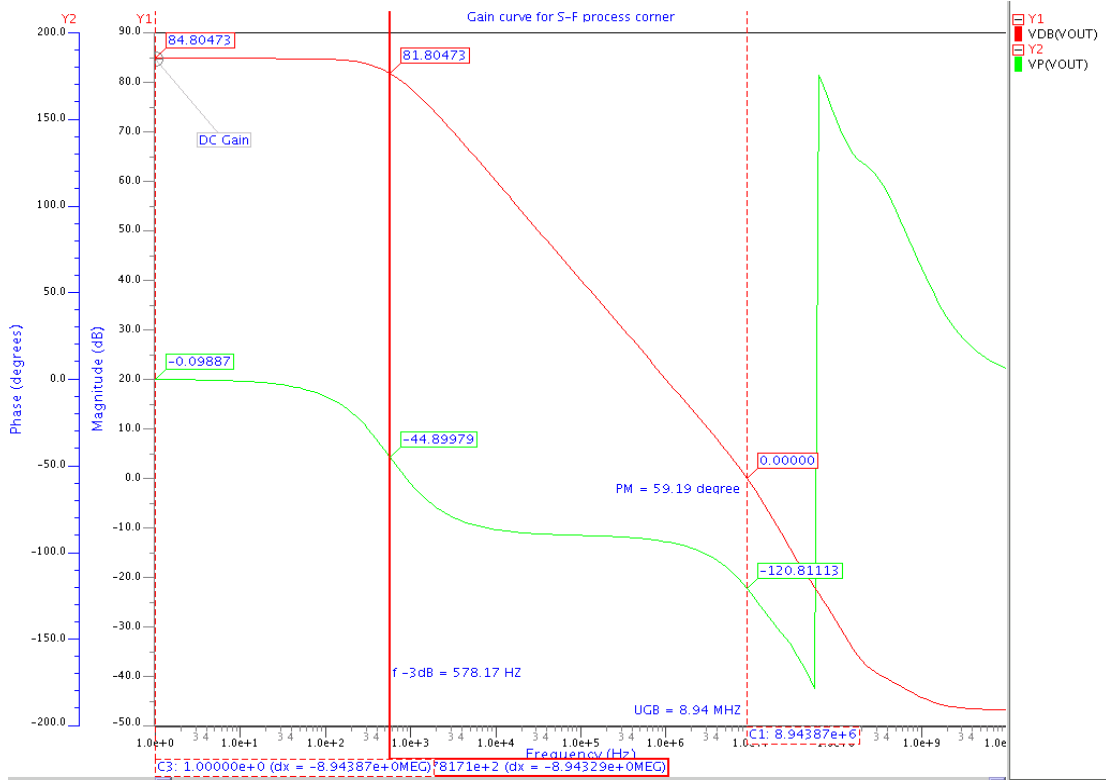


Fig 5.14 Process corner S-F simulation for AC analysis

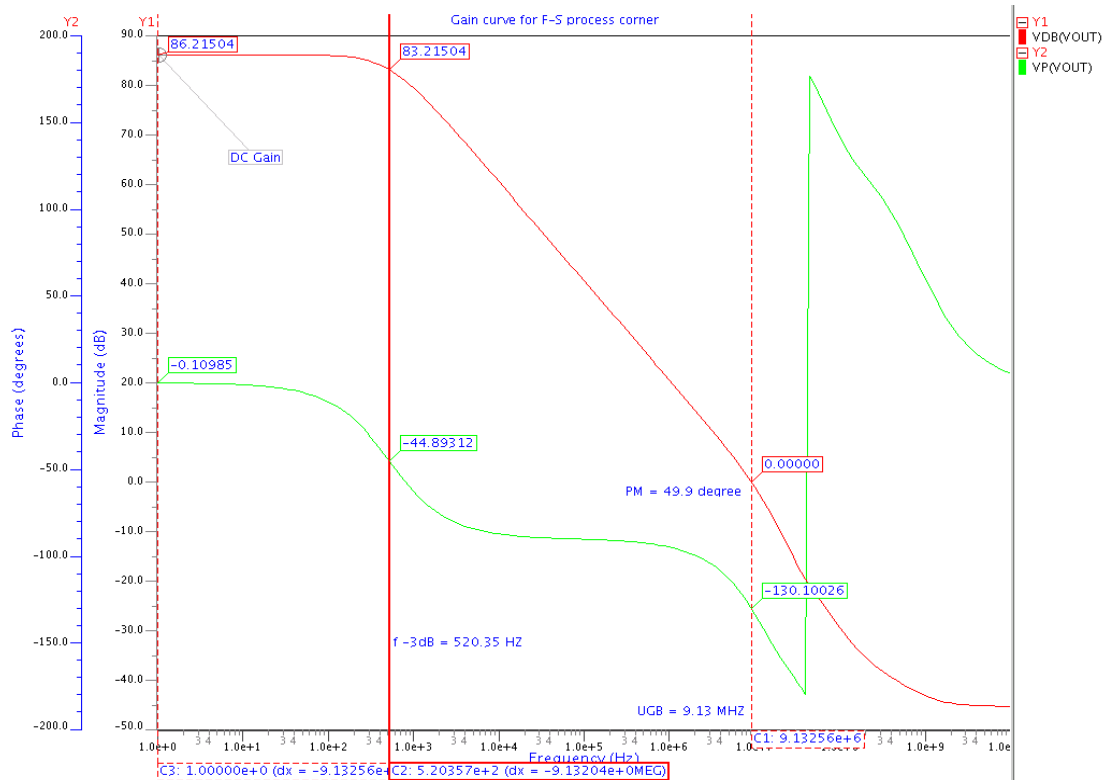


Fig 5.15 Process corner F-S simulation for AC analysis

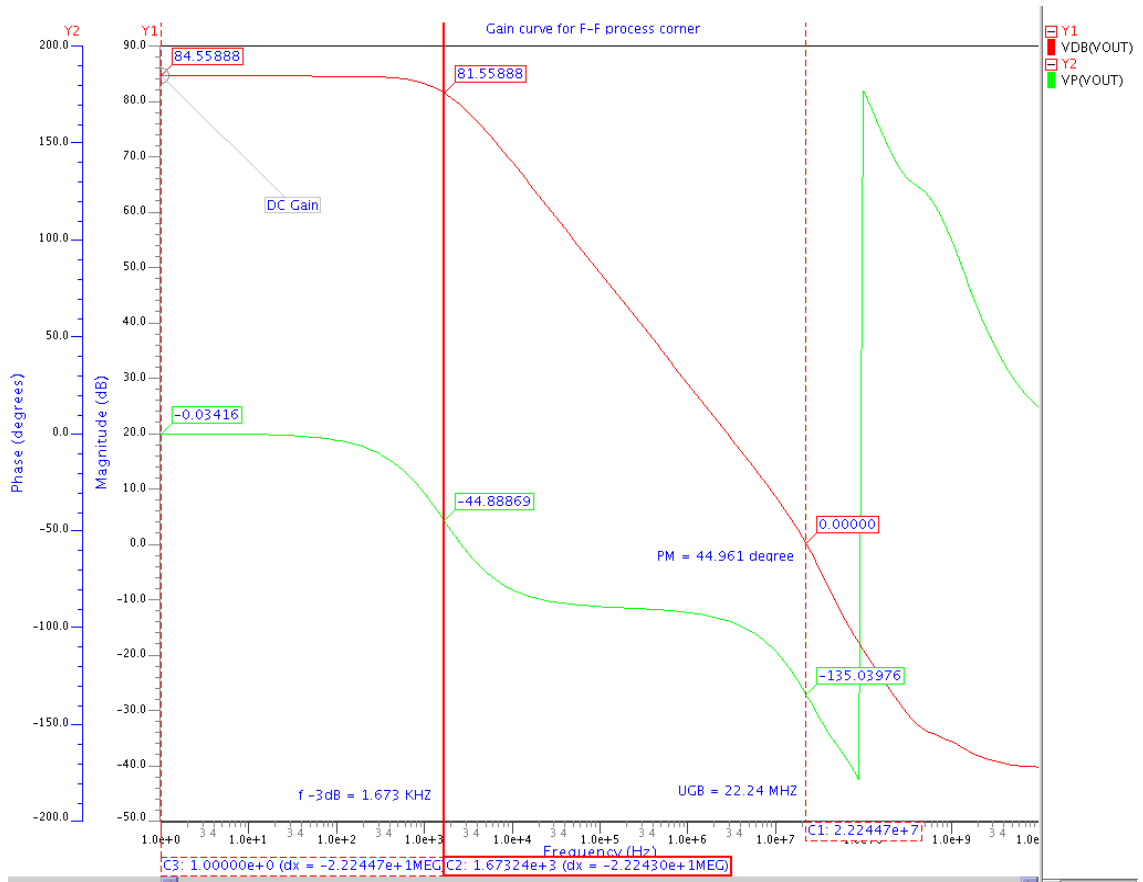


Fig 5.16 Process corner F-F simulation for AC analysis

## 5.2.2 TRANSIENT RESULTS

Fig 5.17 to 5.20 shows process corner, transient analysis of op-amp circuit.

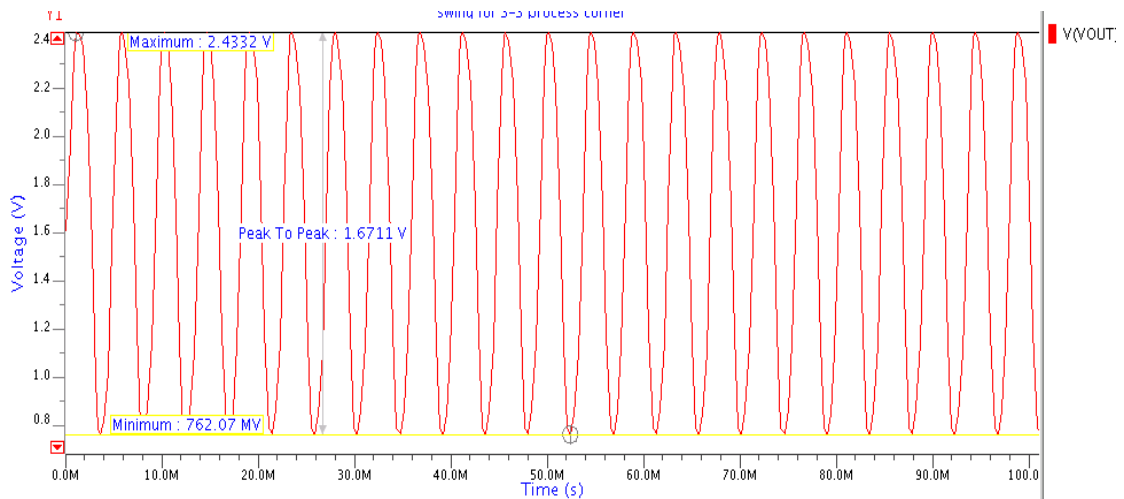
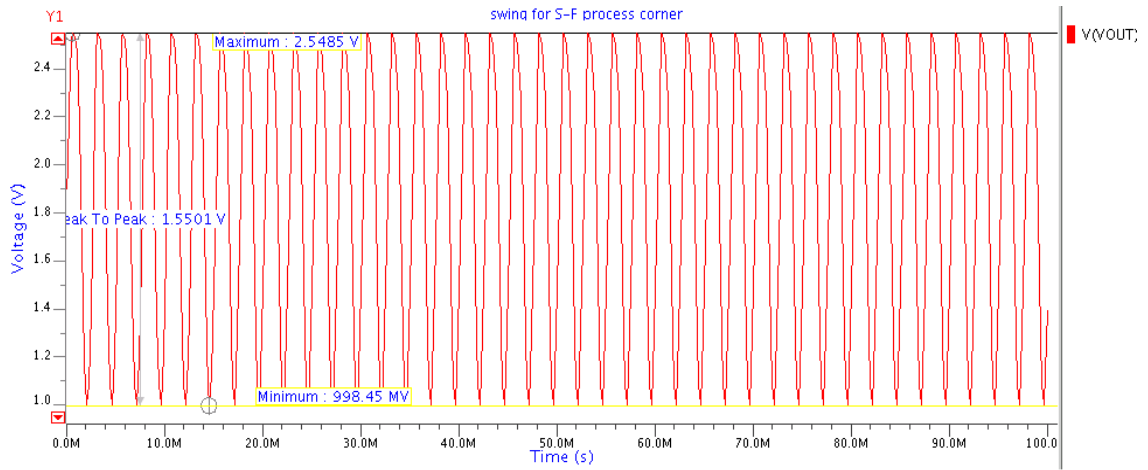
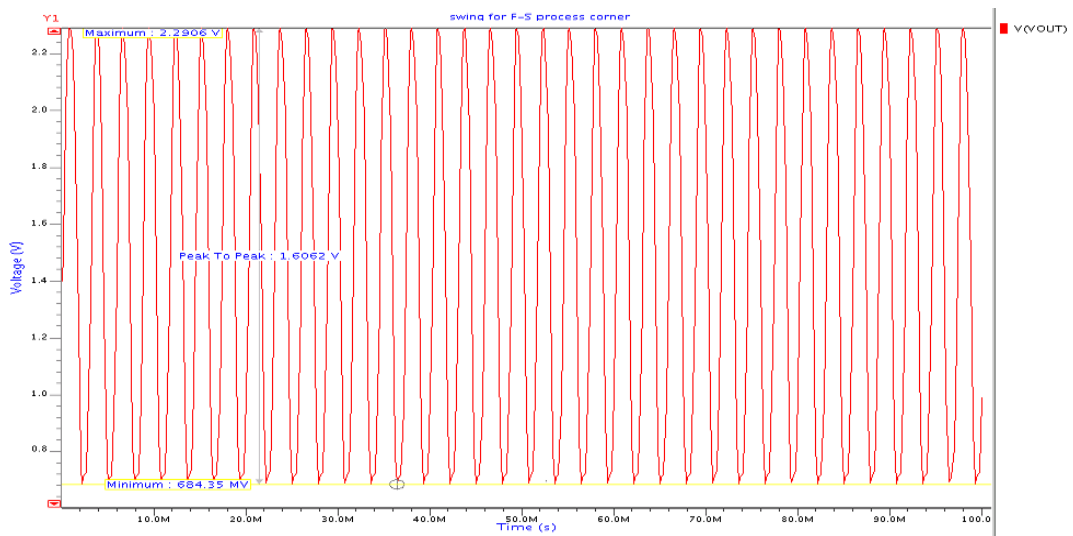


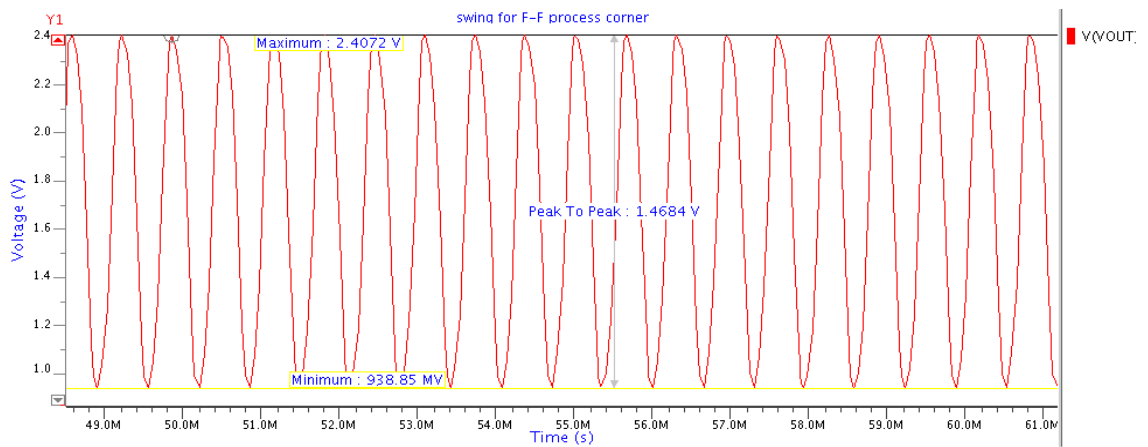
Fig 5.17 Process corner S-S simulation for transient analysis



**Fig 5.18 Process corner S-F simulation for transient analysis**



**Fig 5.19 Process corner F-S simulation for transient analysis**



**Fig 5.20 Process corner F-F simulation for transient analysis**

### 5.2.3 STEP RESPONSE – SLEW RATE MEASUREMENT

Fig 5.21 to 5.24 shows process corner, slew rate of op-amp circuit.

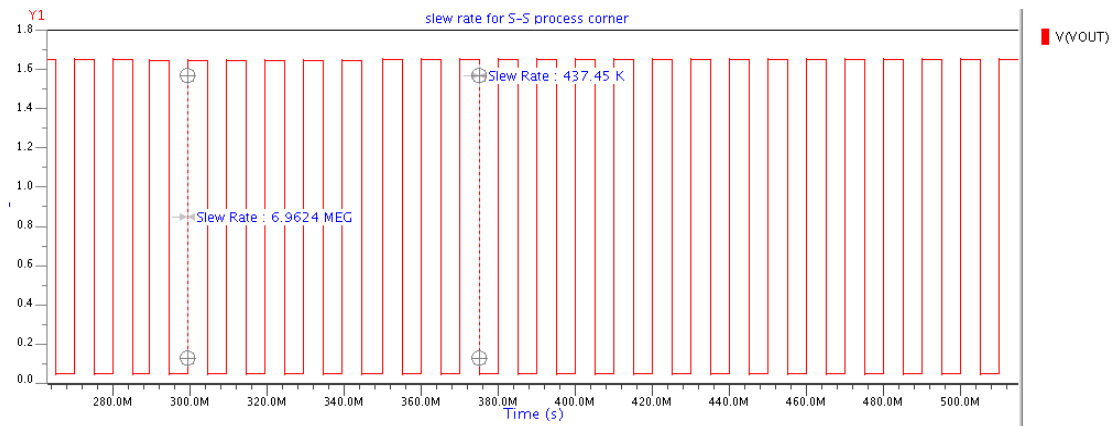


Fig 5.21 Process corner S-S simulation for Slew rate analysis

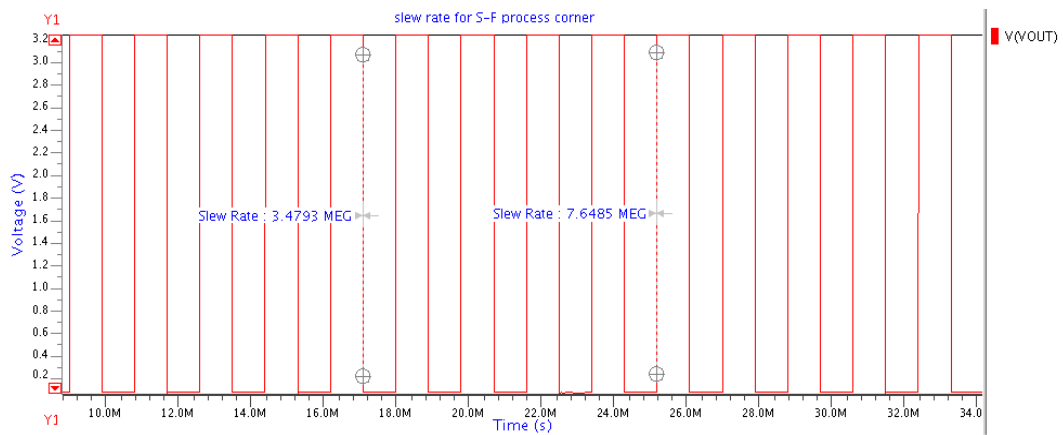


Fig 5.22 Process corner S-F simulation for Slew rate analysis

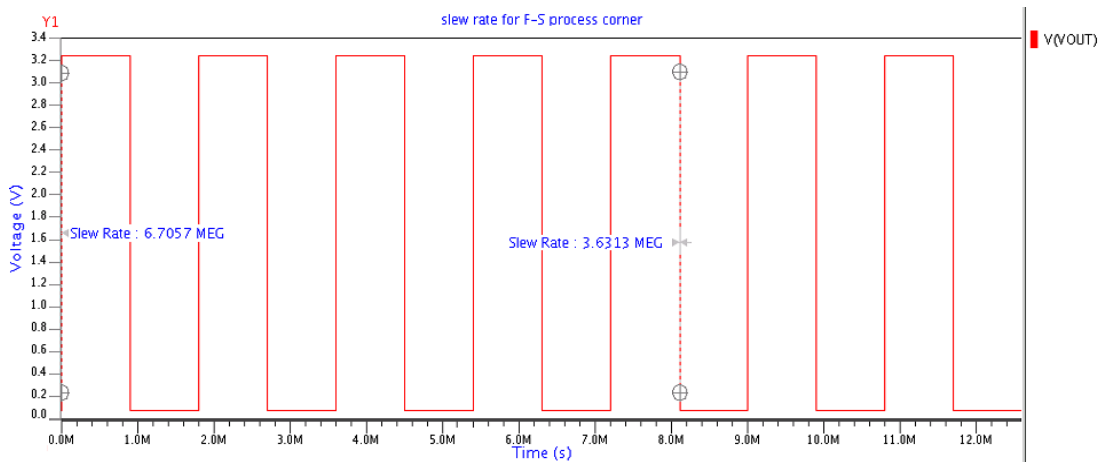
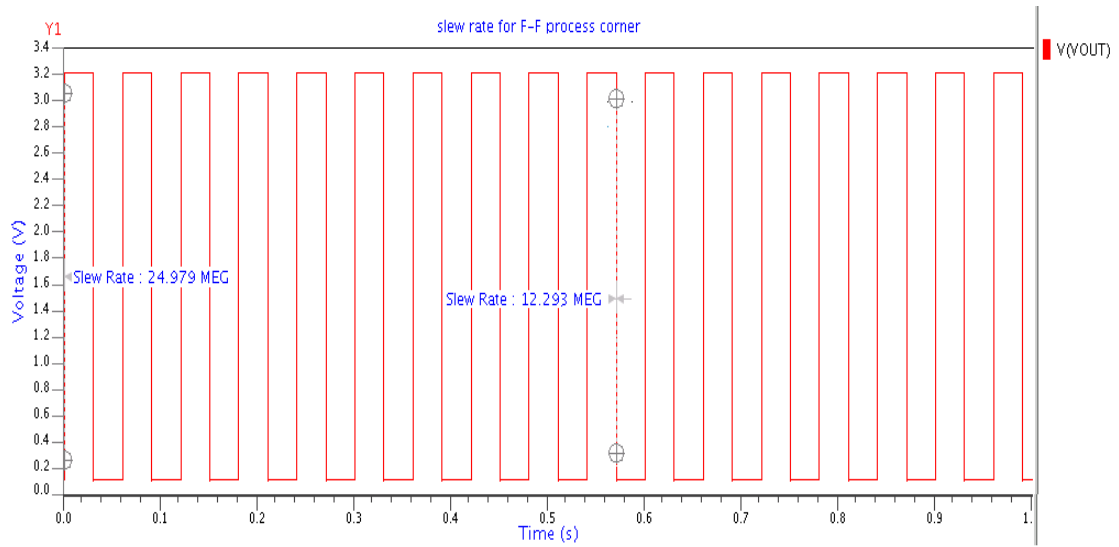


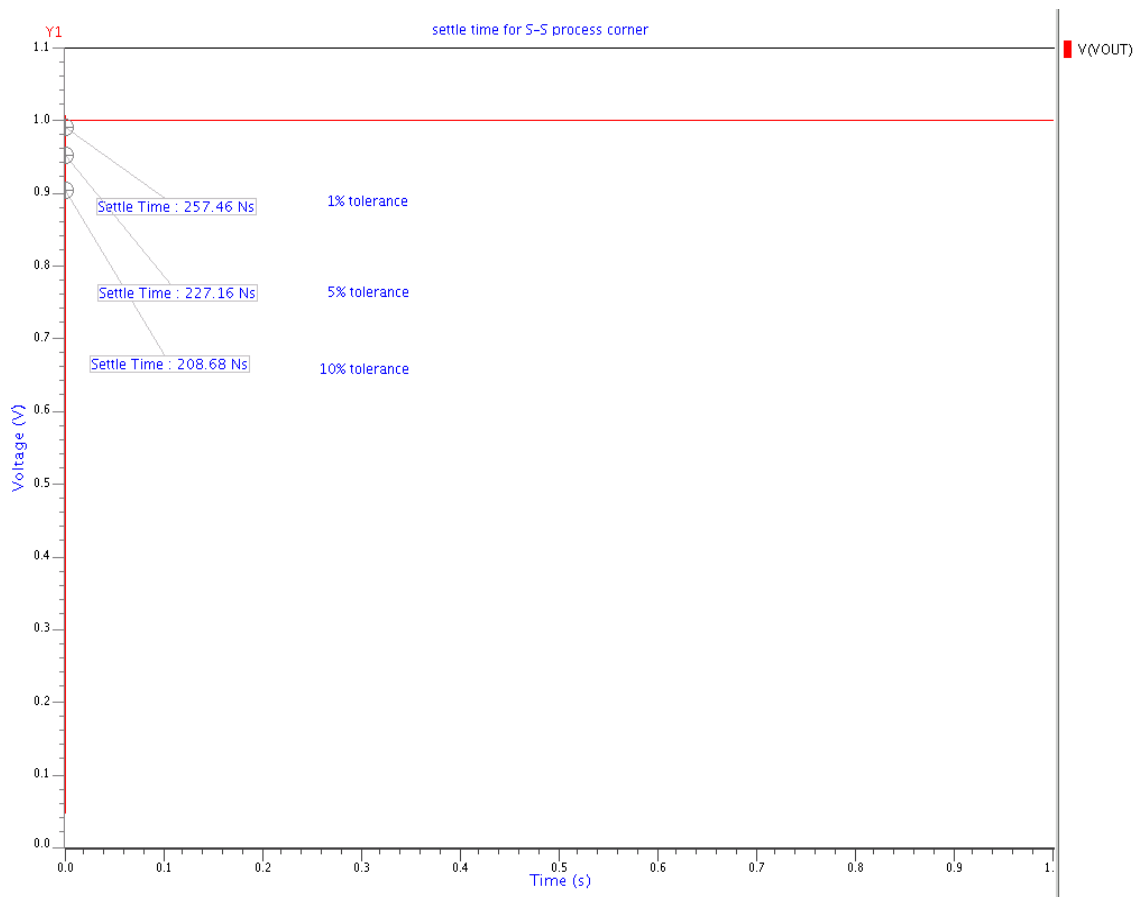
Fig 5.23 Process corner F-S simulation for Slew rate analysis



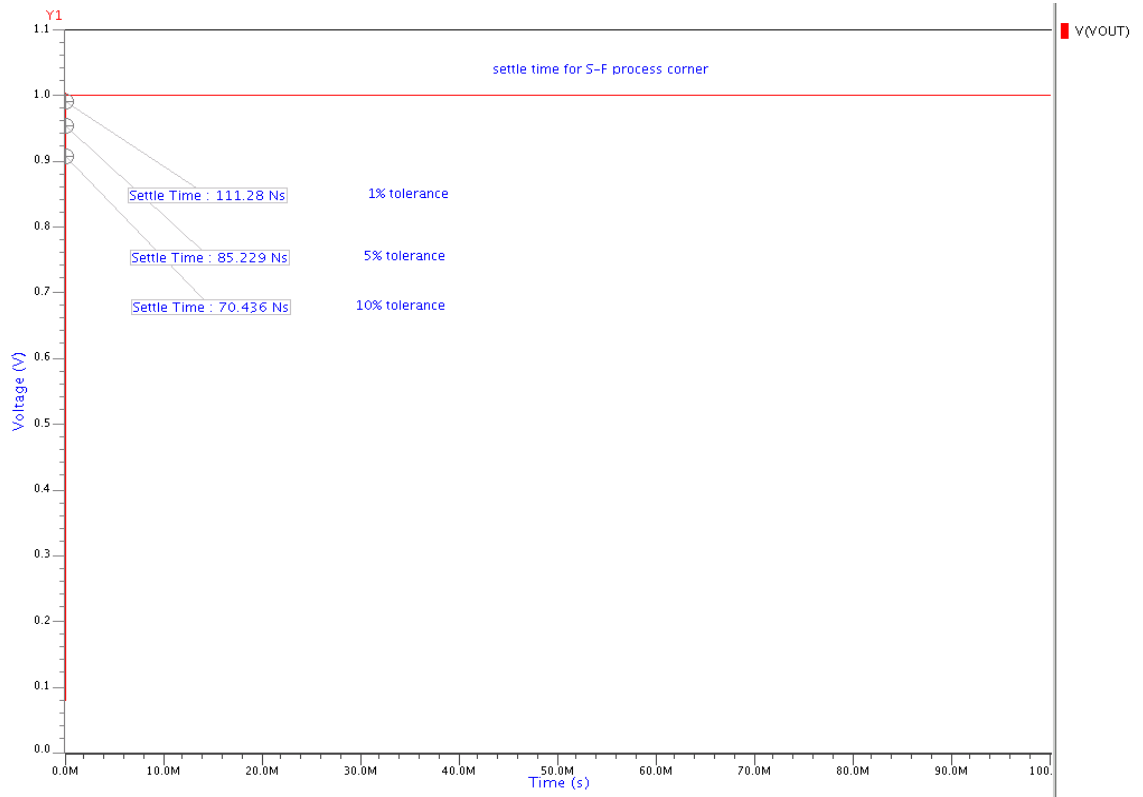
**Fig 5.24 Process corner F-F simulation for Slew rate analysis**

### 5.2.4 SETTling TIME

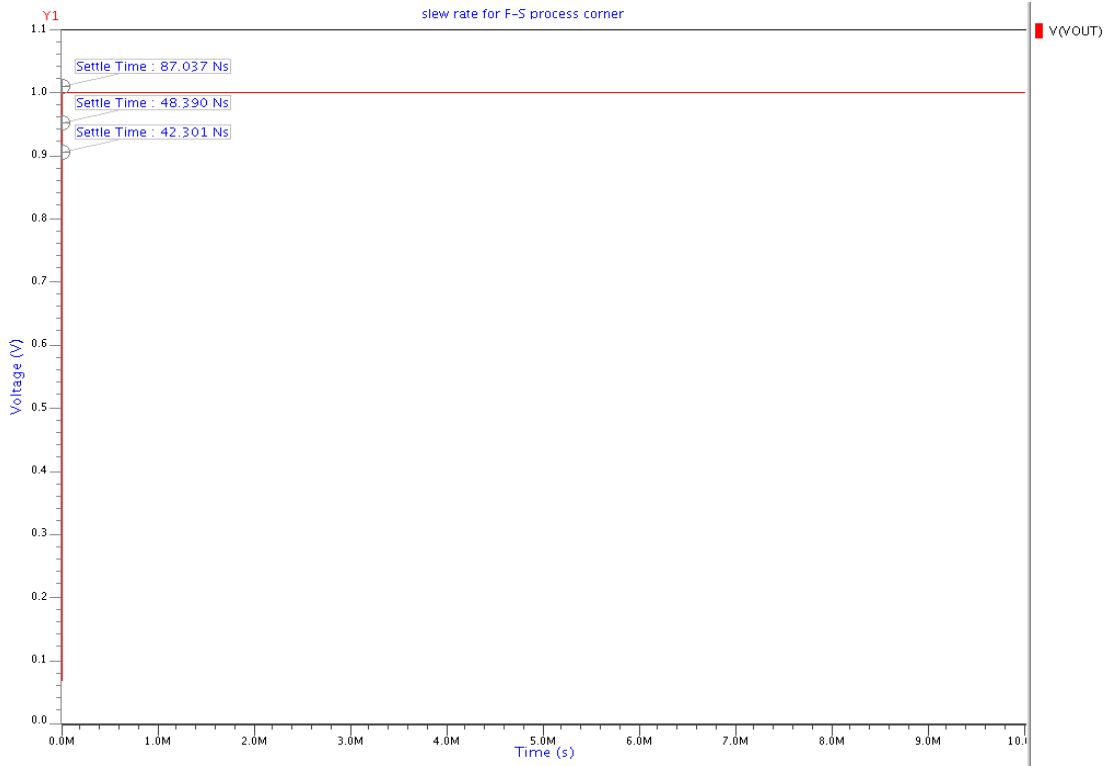
Fig 5.25 to 5.28 shows process corner, settle time analysis of op-amp circuit.



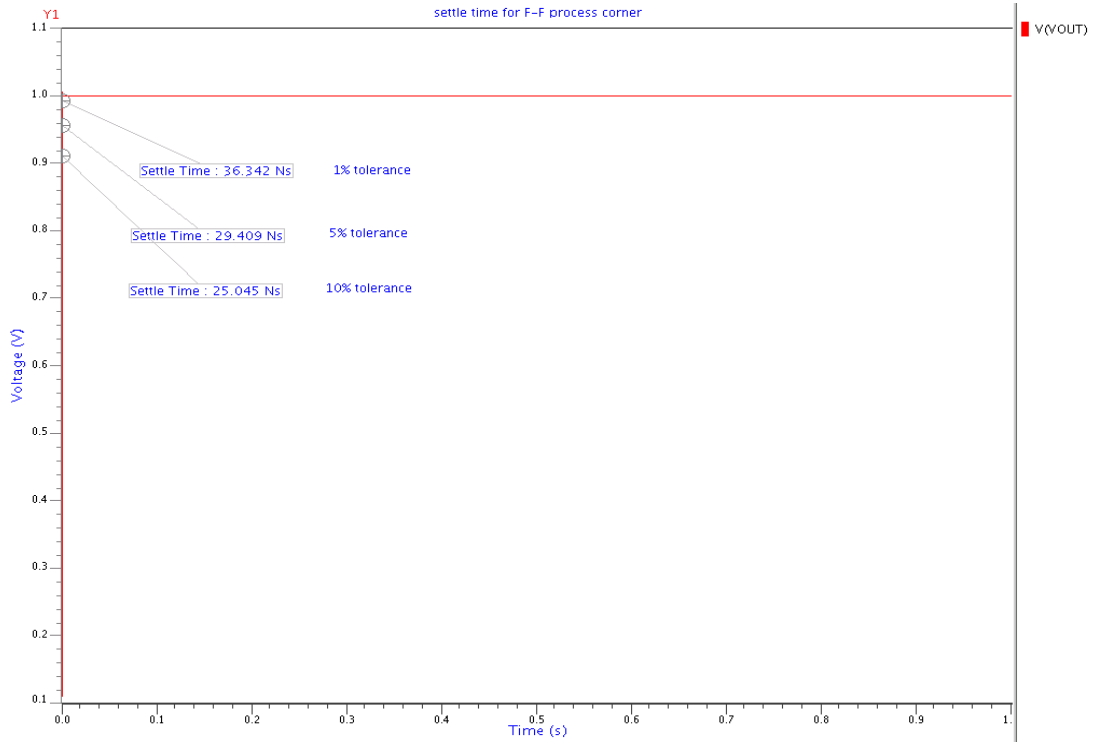
**Fig 5.25 Process corner S-S simulation for settle time analysis**



**Fig 5.26 Process corner S-F simulation for settle time analysis**



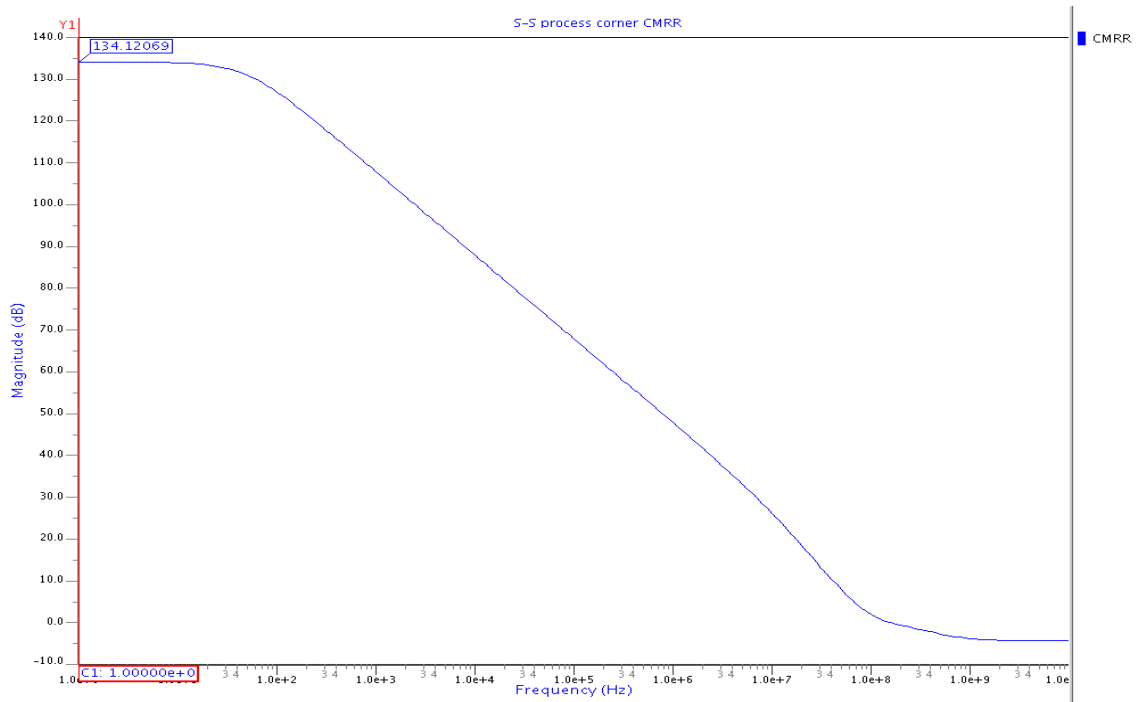
**Fig 5.27 Process corner F-S simulation for settle time analysis**



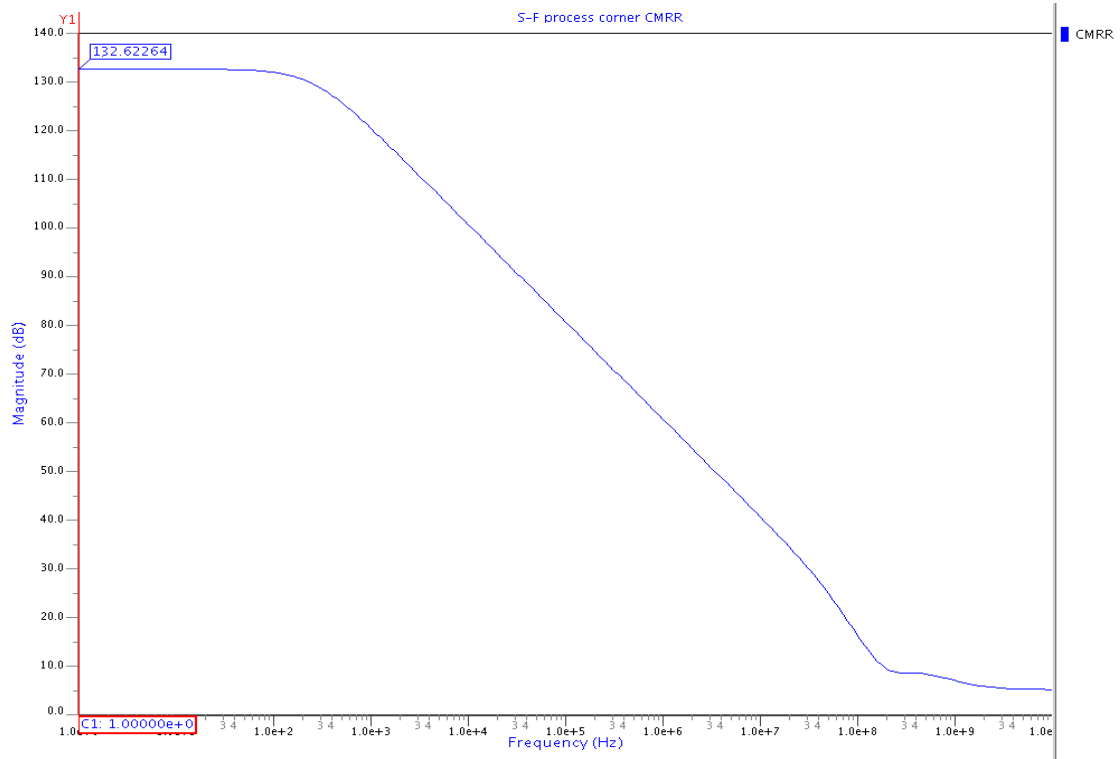
**Fig 5.28 Process corner F-F simulation for settle time analysis**

### 5.2.5 COMMON MODE REJECTION RATIO

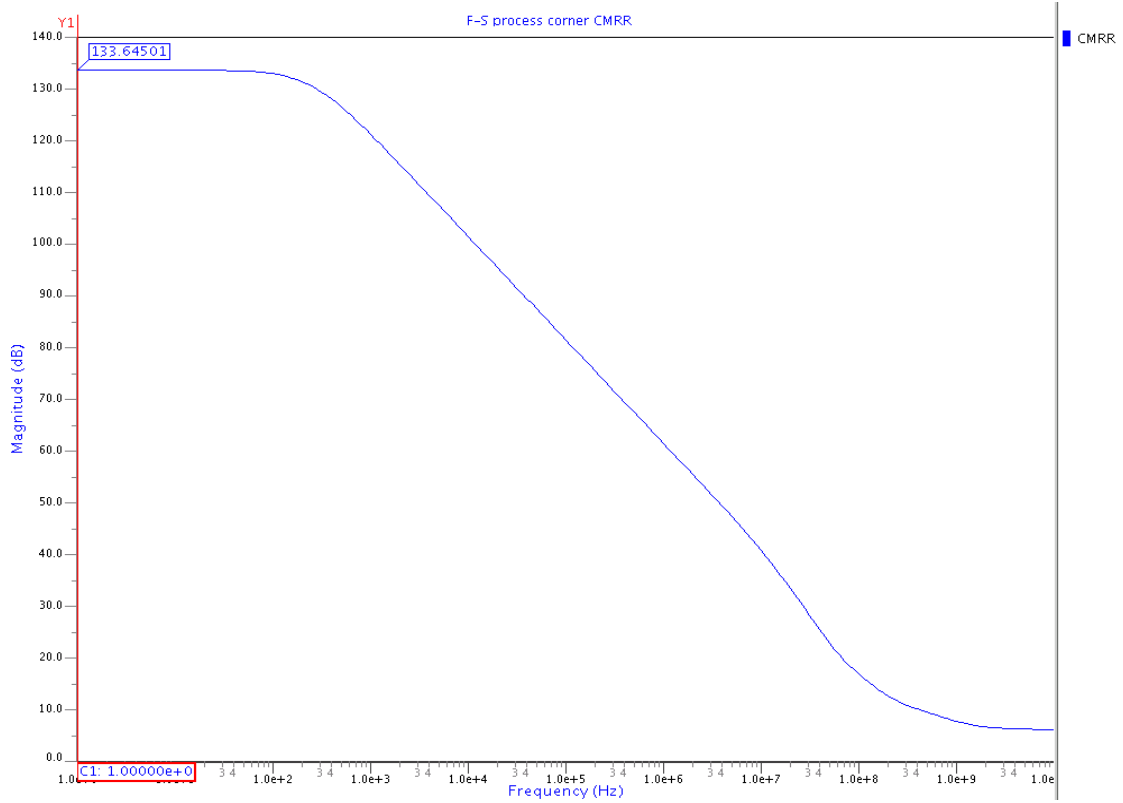
Fig 5.29 to 5.32 shows process corner, CMRR of op-amp circuit.



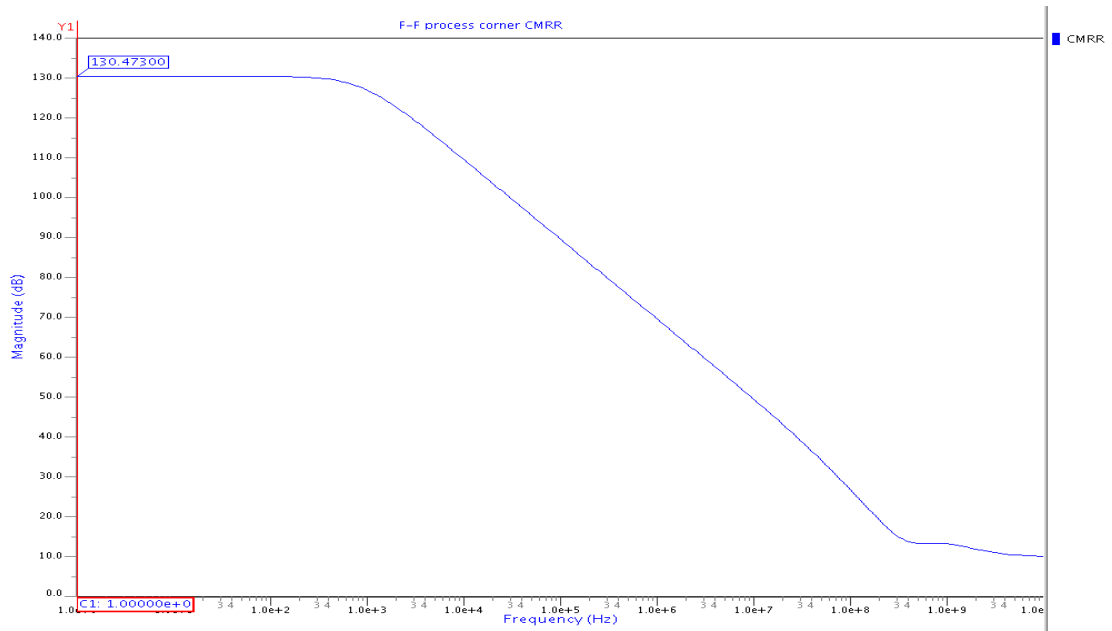
**Fig 5.29 Process corner S-S simulation for CMRR analysis**



**Fig 5.30 Process corner S-F simulation for CMRR analysis**



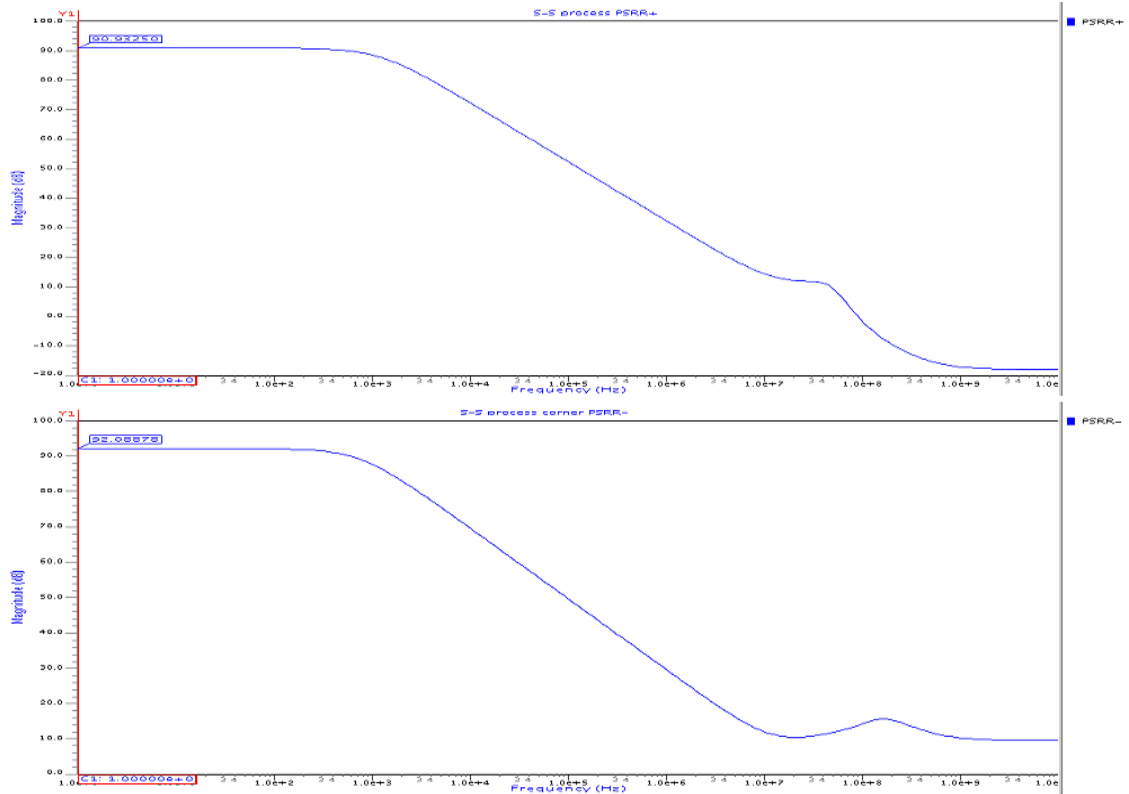
**Fig 5.31 Process corner F-S simulation for CMRR analysis**



**Fig 5.32 Process corner F-F simulation for CMRR analysis**

### 5.2.6 POWER SUPPLY REJECTION RATIO

Fig 5.33 to 5.36 shows process corner, PSRR of op-amp circuit.



**Fig 5.33 Process corner S-S simulation for PSRR analysis**

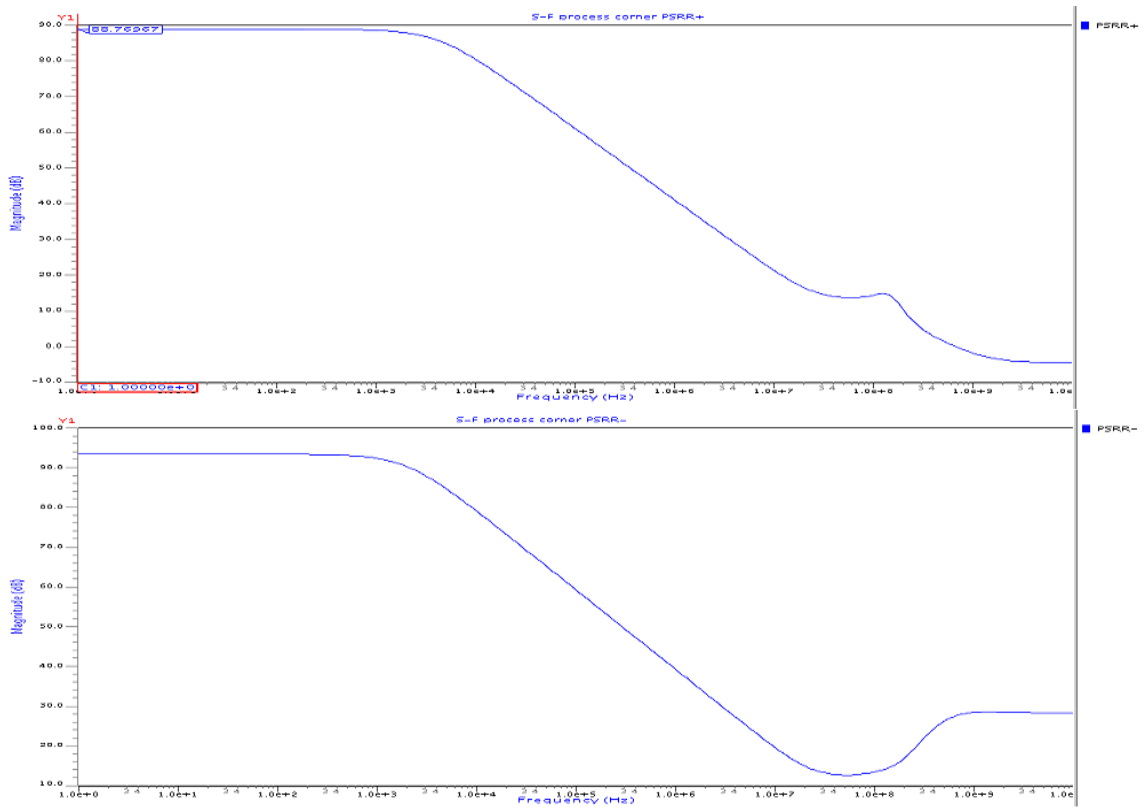


Fig 5.34 Process corner S-F simulation for PSRR analysis

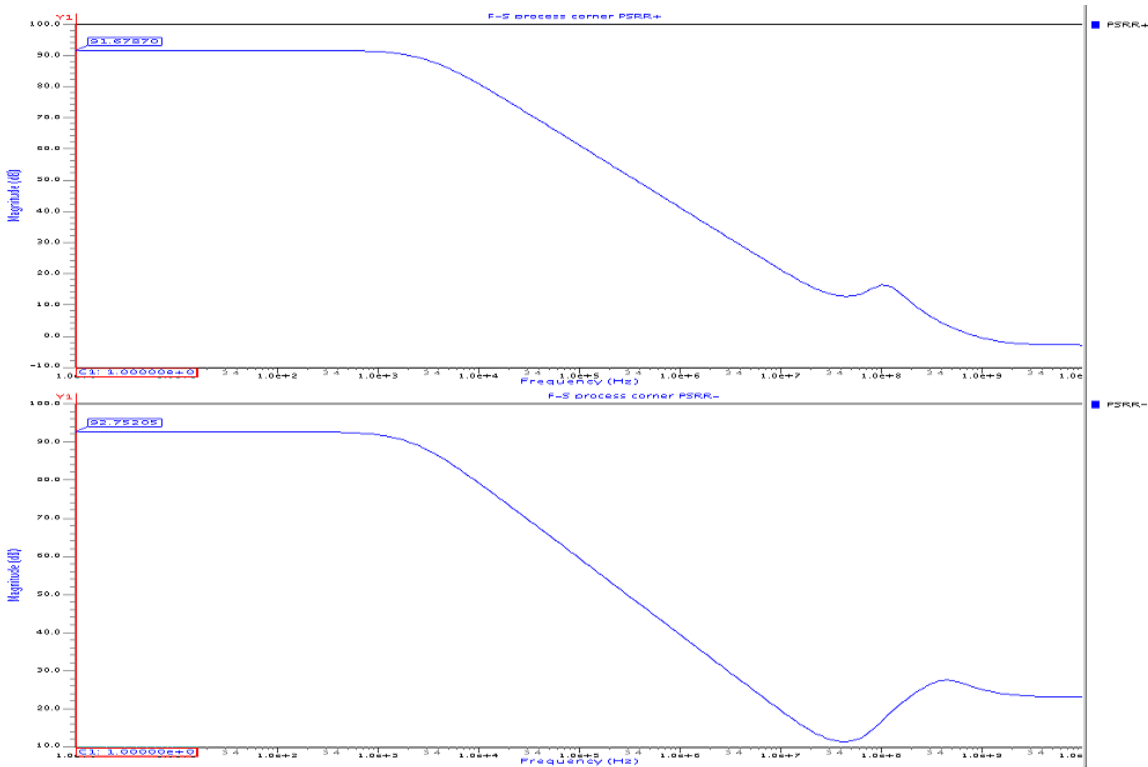
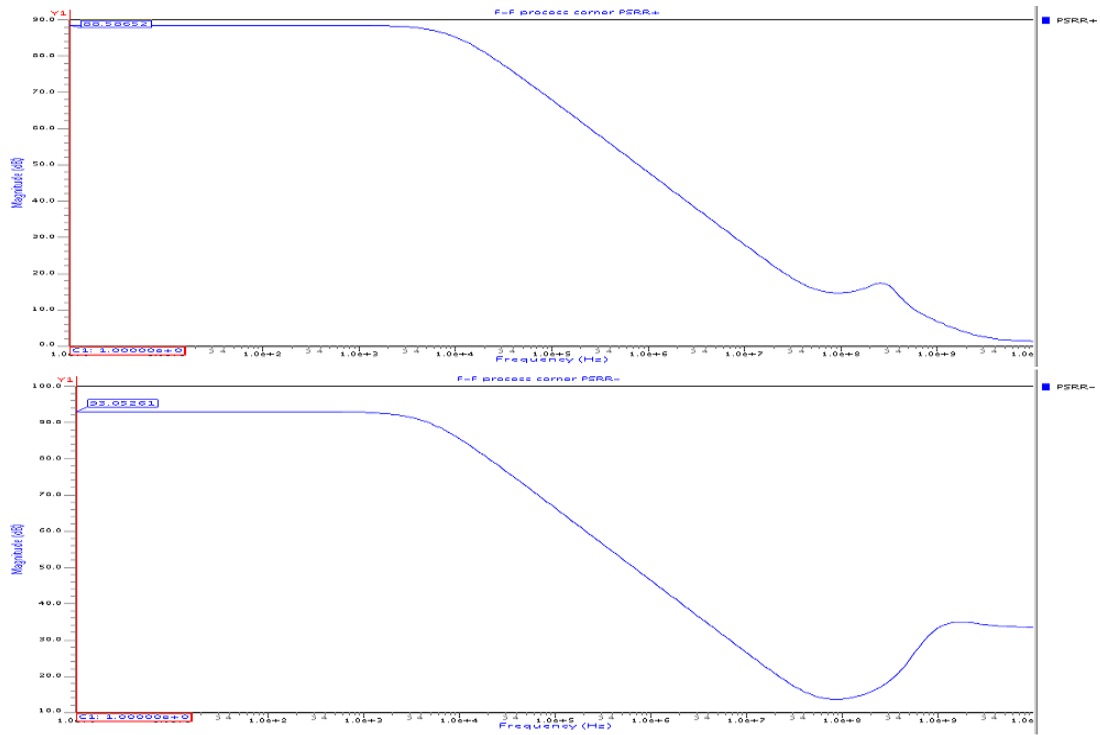


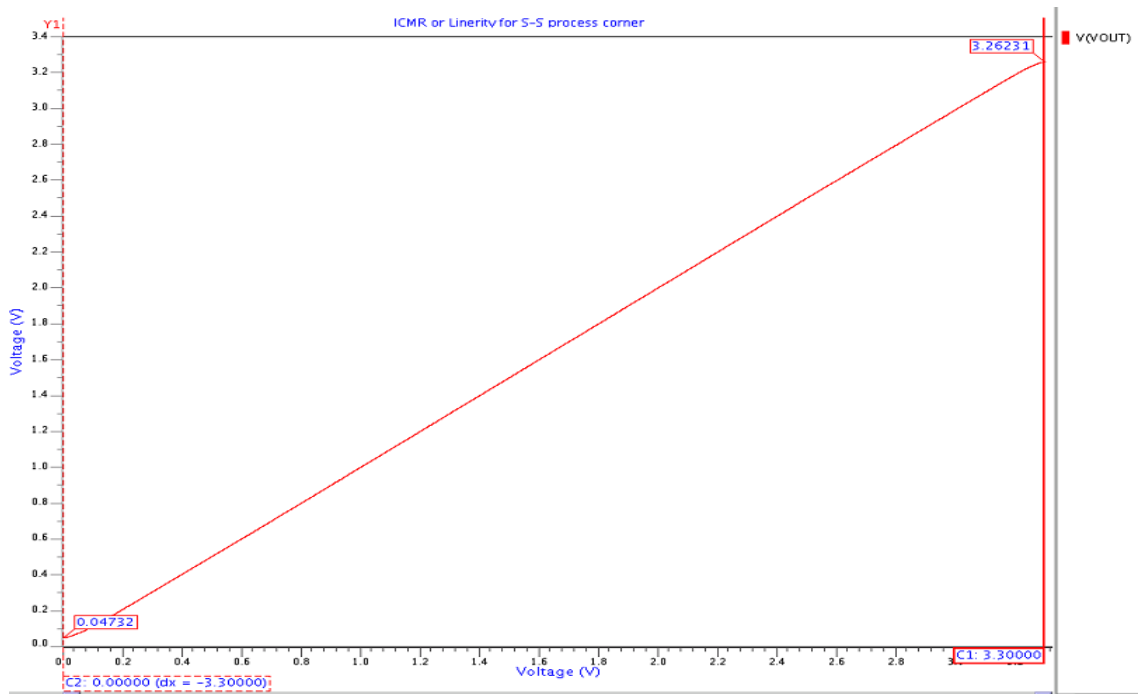
Fig 5.35 Process corner F-S simulation for PSRR analysis



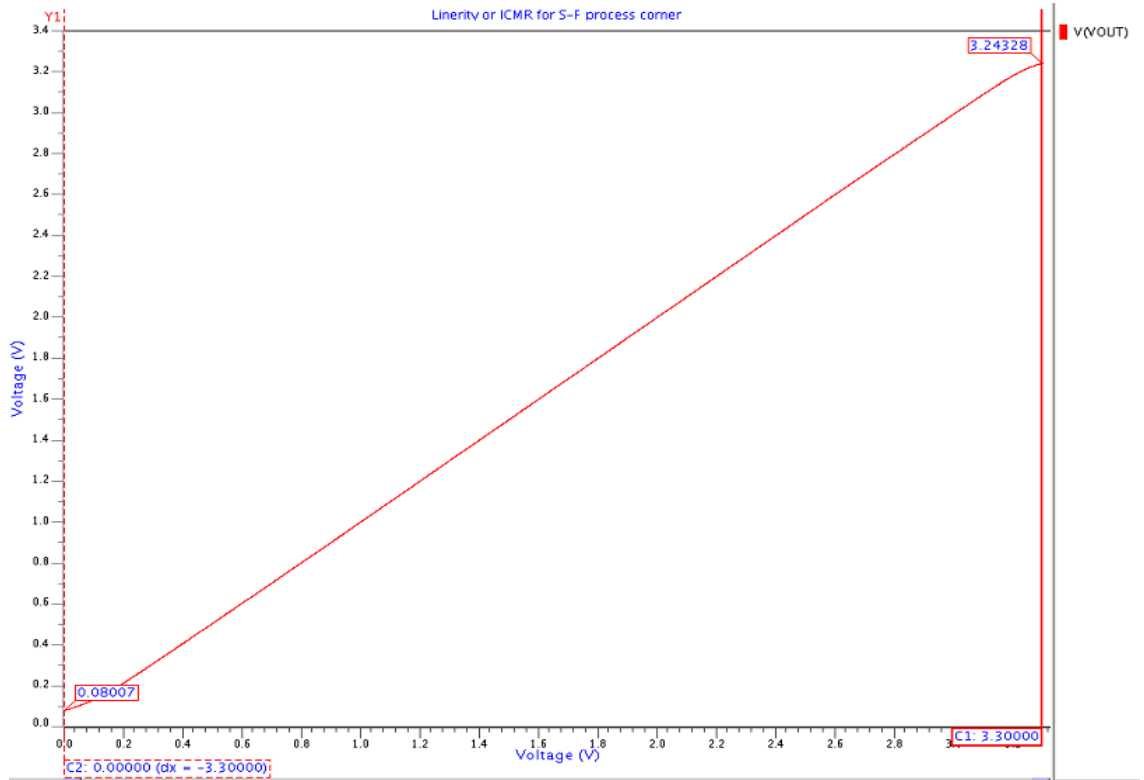
**Fig 5.36 Process corner F-F simulation for PSRR analysis**

### 5.2.7 INPUT COMMON-MODE RANGE

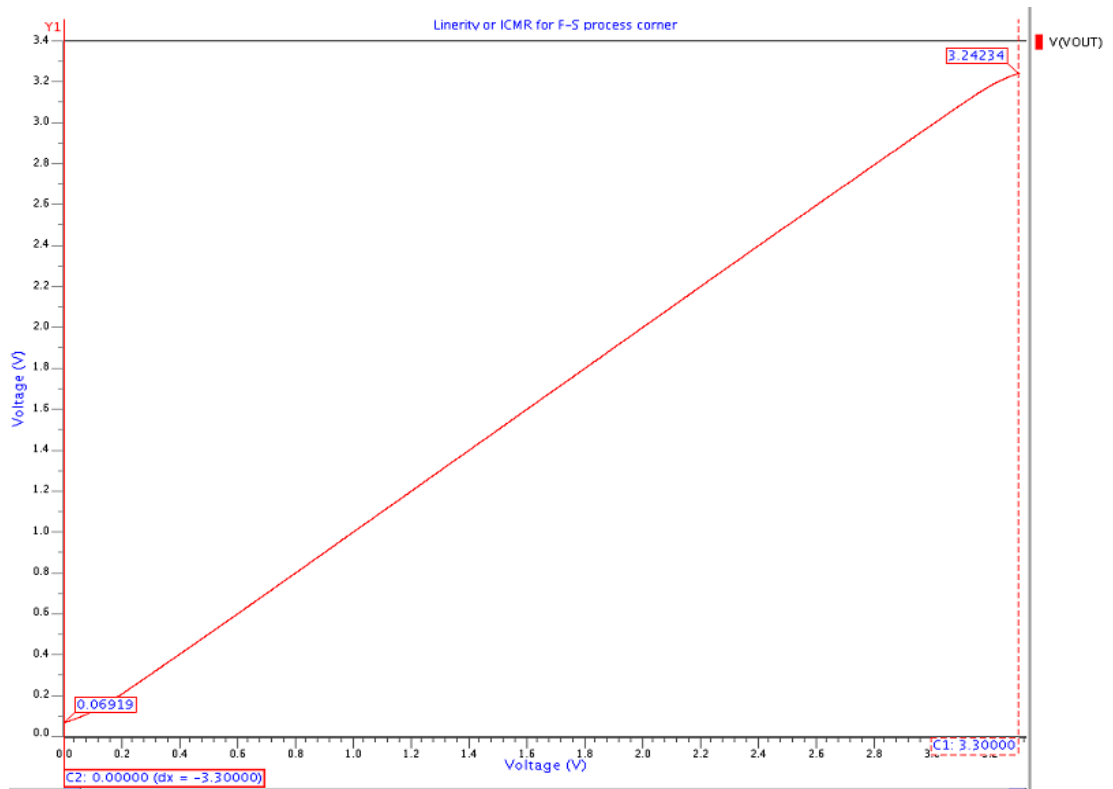
Fig 5.37 to 5.40 shows process corner, ICMR of op-amp circuit.



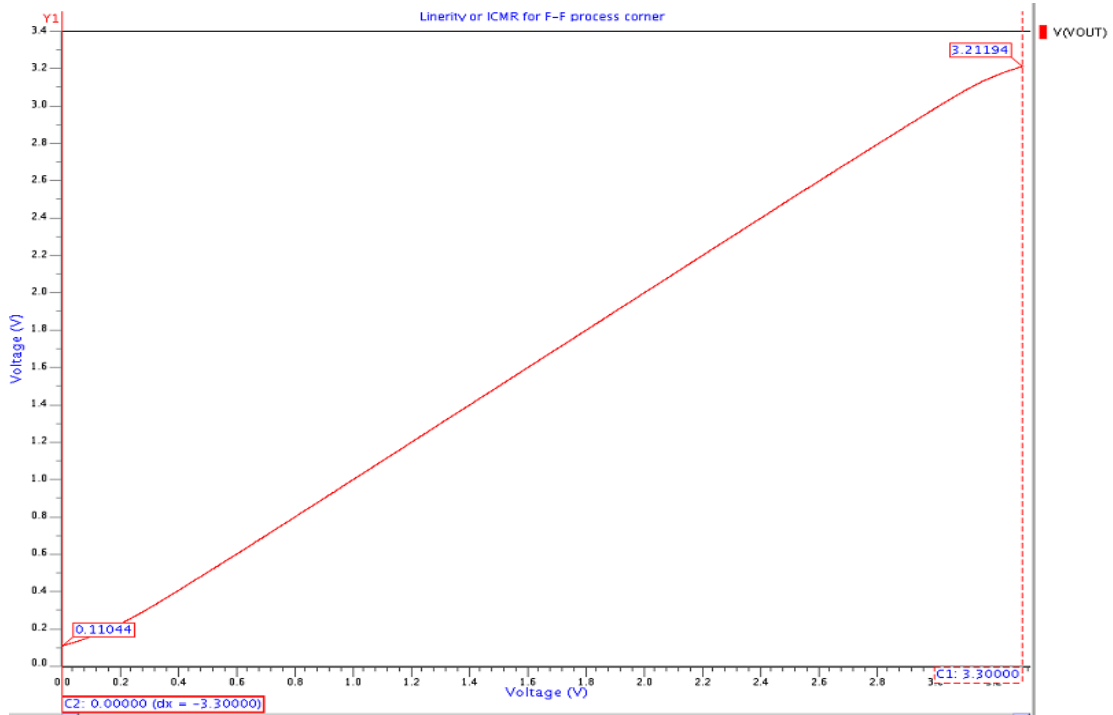
**Fig 5.37 Process corner S-S simulation for ICMR analysis**



**Fig 5.38 Process corner S-F simulation for ICMR analysis**



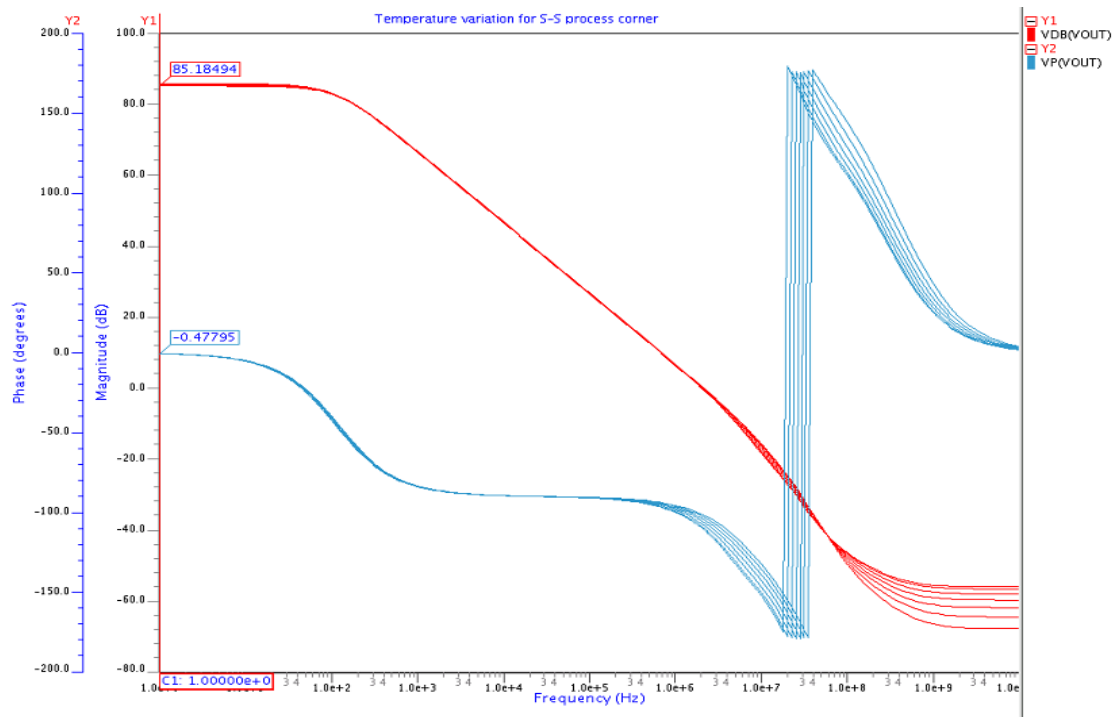
**Fig 5.39 Process corner F-S simulation for ICMR analysis**



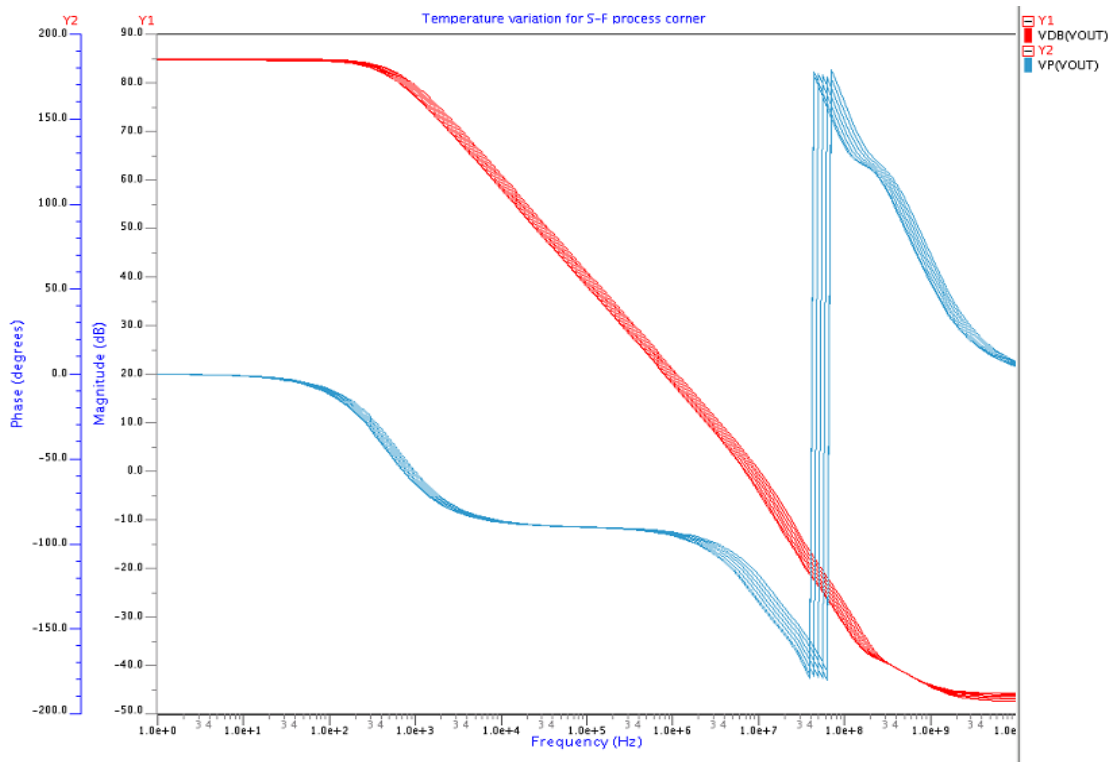
**Fig 5.40 Process corner F-F simulation for ICMR analysis**

## 5.2.8 EFFECT OF VARIATION OF TEMPERATURE ON AC RESPONSE

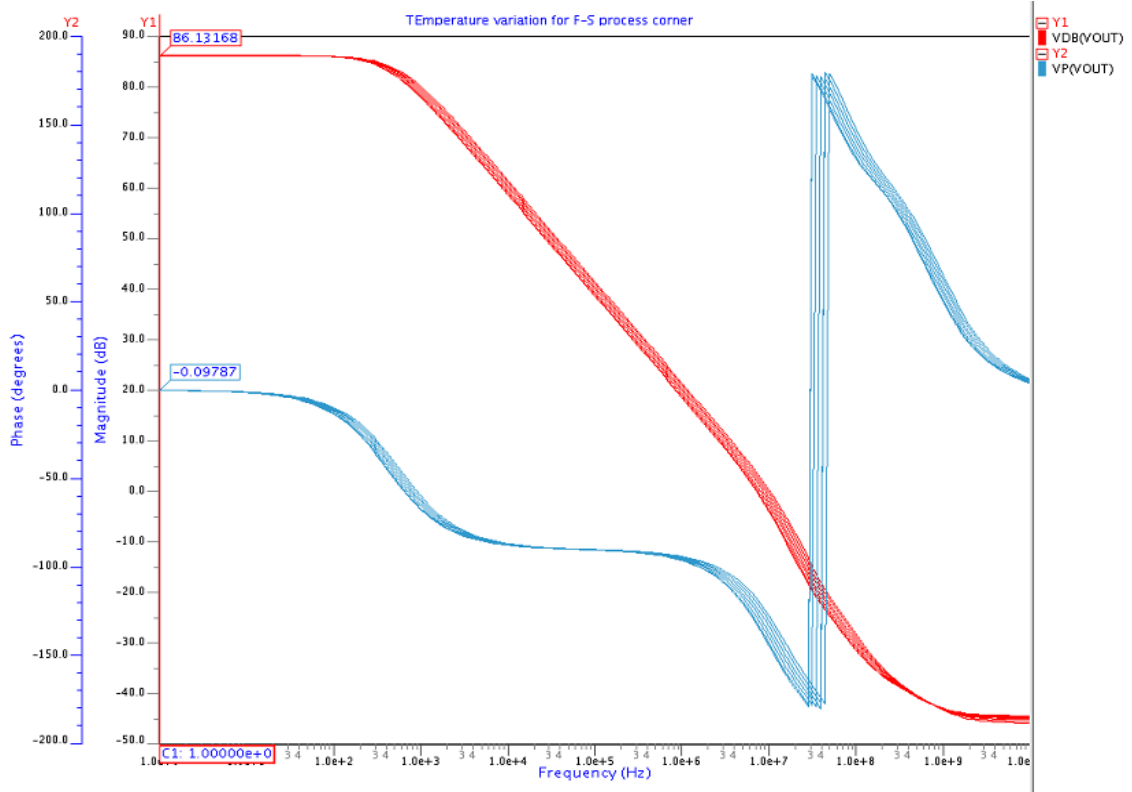
Fig 5.41 to 5.44 shows process corner, ICMR of op-amp circuit.



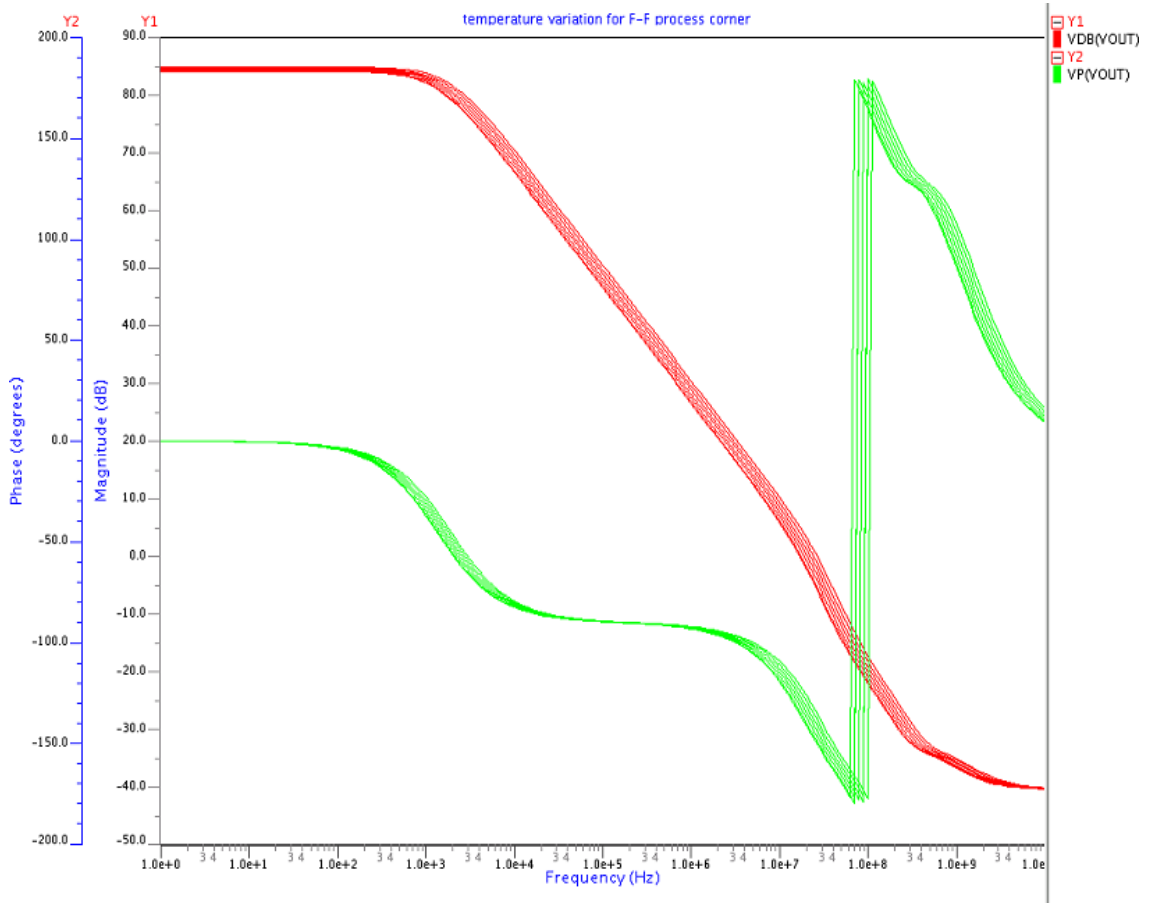
**Fig 5.41 Process corner S-S simulation for temperature variation**



**Fig 5.42 Process corner S-F simulation for temperature variation**



**Fig 5.43 Process corner F-S simulation for temperature variation**



**Fig 5.44 Process corner F-F simulation for temperature variation**

### 5.2.9 COMPARISON OF FOUR PROCESS CORNERS

**Table 5.3 Complete process corner simulation with typical values**

Specifications	Typical Value	Process corner S-S	Process corner F-S	Process corner F-F	Process corner S-F
PD ( $\mu W$ )	268.5437	44.5491	252.7024	1.002E3	275.1931
DC Gain (dB)	85.51	85.50264	86.2154	84.55888	84.80473
UGB (MHz)	9.17	2.166	9.13	22.24	8.94
3dB frequency (Hz)	555.54	117.5	512.35	1673	578.17
Phase Margin	54.94°	75.983°	49.9°	44.961°	59.19°

Slew rate (V/ $\mu$ s)	7.27, 3.6227	6.9624, 437.45E-3	6.7057, 3.6313	24.979, 12.293	7.6485, 3.47930
CMRR (dB)	133.24	134.12069	133.645	130.473	132.62264
Positive PSRR (dB)	90.18313	90.93250	91.6787	88.58652	88.76967
Negative PSRR (dB)	93.04908	92.08878	92.75205	93.05261	93.7850
Settle time (10% Ns)	53.710	208.68	42.301	25.045	70.436

Above table shows comparison of process corners with schematic results.

### 5.3 PAD FRAME DESIGN

After checking the layout that it is working properly and showing result as it is required the next step is to apply the pad frame. Pads are also circuits which used to connect the circuit with the external world. The operational amplifier layout has to be fabricated through any fabrication foundry. Here process used for MOSIS fabrication foundry is, TSMC 0.35 micron SCN4M\_SUBM process. This technology supports the use Scalable CMOS N-well, 4 metals, 1 poly, Silicide block and thick oxide. The parameter  $\lambda$  is 0.20 micron in this technology and the power supply to be used is 3.3V. The pad library for this technology includes Power Pad, Ground Pad, Bi-Directional Pad, Input Pad, Output Pad, and Analog Input/Output Pad.

If the design is too big then two power pins and two ground pins should be placed on each side of the pad frame. The pad frame for this process is shown in Fig 5.45.

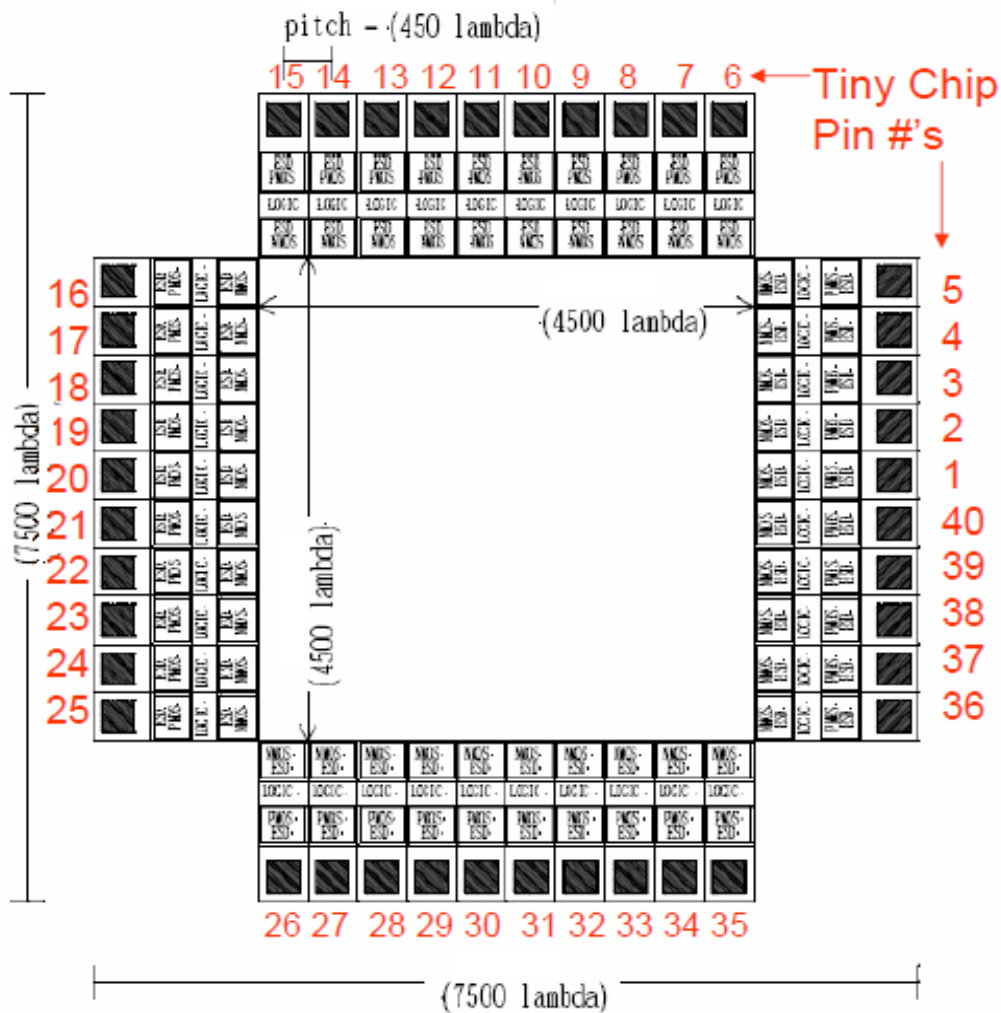


Fig 5.45 Pad frame for MOSIS SCN4M\_SUBM process

To apply pin frame there are several steps which are as follows:

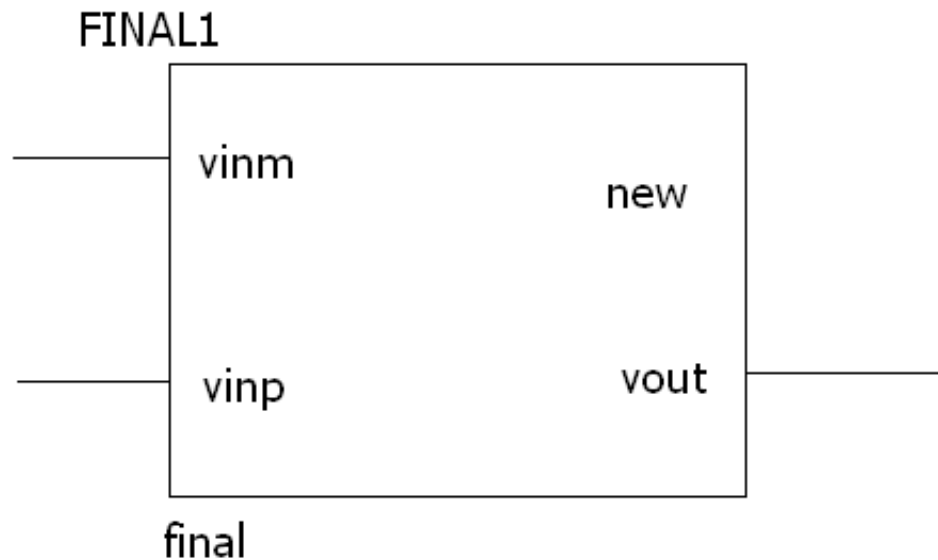
### 5.3.1 SYMBOL GENERATION

A symbol of schematic has to be generated. This symbol is generated in design architect IC by selecting: *Miscellaneous > Generate Symbol*. Add “phy\_comp” property to the symbol by selecting

- Select the body of the symbol
- From the popup menu: *Properties > Add Properties*
- Enter property name: phy\_comp
- Enter property value: (layout cell name for the block created in IC station tool)

After that check and save this symbol.

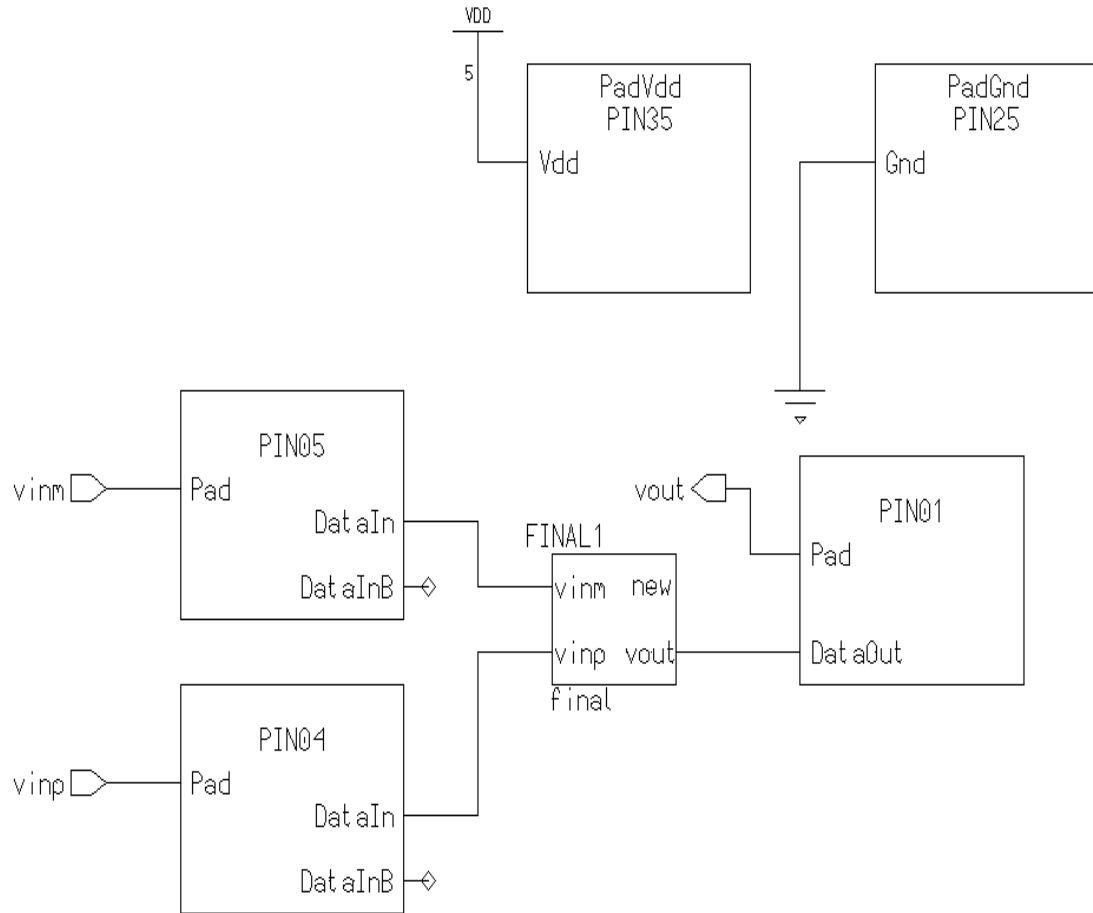
While generating the symbol cares have to be taken for selecting “activate symbol?” and “replace existing?” if already created a symbol. This symbol can be simulated to check whether it gives results same as that of schematic.



**Fig 5.46 Generated symbol for circuit schematic**

After generating symbol next we create a schematic for chip. From Menu pallet: *Add > Instance Select* and place generated symbol. Then add pads from *ADK Library > Std. Cells > Pads > tsmc03 > tsmc035*: In, Out, BiDir, VDD, GND. Wire pads to logic blocks and connectors. After then assign pin numbers by changing the instance name of pad. Finally check and save the design.  $V_{DD}$  and *GND* pads are not connected to schematic symbol.

For further to use this schematic, create view point of this schematic using command *adk\_dve*. Finally the schematic of symbol with pad symbols is shown in the Fig 5.47. Here input and output ports also have to apply.



**Fig 5.47 Schematic for chip**

### 5.3.2 CHIP LAYOUT

To make the chip layout with pad frame open a new cell, whose logic source is “layout view point of chip schematic” then open schematic ADK Edit menu: *Logic Source > Open*. In the schematic, select core cell but not pads then place the cell: *Place > Inst pads*. Generate the pad frame from top menu bar: *ADK > Generate Pad frame > tsmc035*. Put core logic cells as desired to make routing easier, but do not edit or move pad cells.

For connection Auto route all. Select auto route all on *P&R* menu Click “*options*” on prompt bar, and unselect “*Expand Channels*”. After saving the design to check the design,

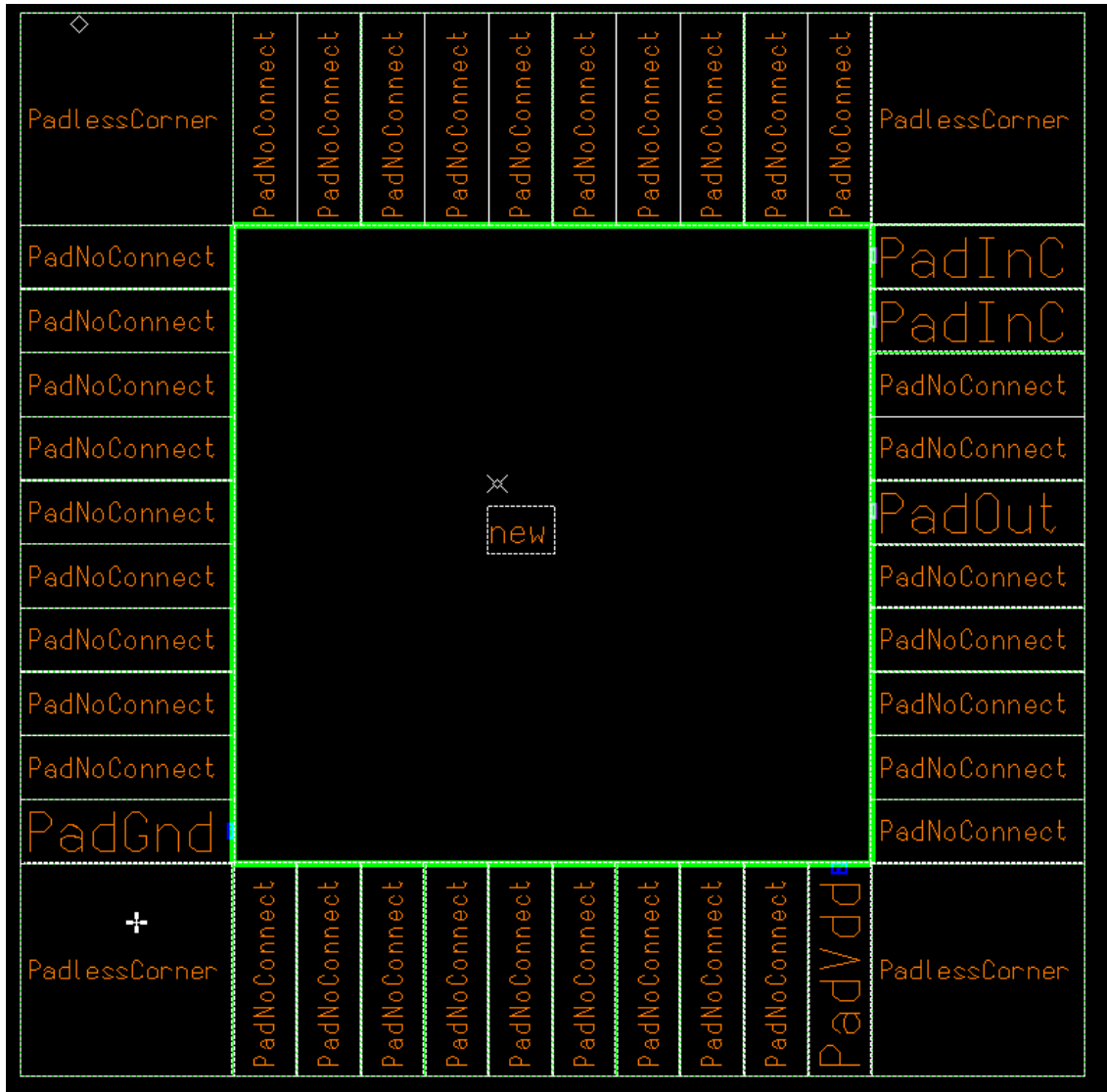
from main palette, select: *IC rule* > *Click Check* In prompt box, enter the names of the pad cells in the “*Exclude Cell*” boxes. Check the design after excluding PadOut, PadInC, PadGnd, PadVdd, PadNoConnect, PadlessCorner.

Dialog box for DRC exclude cell comes out to as shown in Fig 4.48.

**Fig 5.48 Dialog box for DRC exclude cell**

If some DRC errors come, then remove that error. Finally, the pad frame with schematic symbol connected and shown as shown in Fig 5.49. If cell library for foundry is available

then the full circuit can be checked and final layout for fabrication is ready. Pins are assign to pad frame are those which given in symbol schematic in Fig 5.47.



**Fig 5.49 Pad frame with schematic symbol**

After completing this, a GDS and LEF have to create for foundries for fabrication purpose. GDS is for dimensions purpose and LEF for electric connection.

## CHAPTER 6

### CONCLUSION AND FUTURE SCOPE

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#### 6.1 CONCLUSION

In this thesis work, a Self Biased Rail-To-Rail Input Op-Amp is designed and simulated. Here in the circuit a complementary N-P pair with the summing stage is used. This summing stage also works as load as well as biasing circuit.

An economical but efficient technique to achieve a constant rail-to-rail complementary N-P differential input stage used for achieving rail-to-rail input stage. The circuit achieves nearly constant- $g_m$  (7.5 to 15% variation) behavior over the full input common-mode voltage range. The operation of the input stage under different supply voltages and temperature are simulated and analyzed. Simulation also shows that the frequency response of an op-amp using this constant  $g_m$  input stage is nearly independent of the input common-mode voltage variation. As the input common mode varies, variation in DC gain is up to 3.65dB. The power dissipation of the operational amplifier is 268.5  $\mu W$  with unity gain bandwidth 9.17MHz and phase margin of 54.94°. Further process corner simulations have been done for process variation of 15% in threshold voltage  $V_{TH}$ , oxide thickness  $t_{ox}$  and mobility  $\mu_0$ . Variation in gain in this process variation is 84.5588 dB to 86.2154 dB which is very less. And power dissipation variation from 44.549  $\mu W$  to around 1 mW. The minimum CMRR is more than 132dB. Simulation result for temperature variation shows that there is a small variation in performance characteristics so the circuit can be use for wide temperature range. Finally pad frame is generated for this circuit for fabrication purpose.

#### 6.2 FUTURE SCOPE

The circuit proposed here in this thesis work is not Rail-To-Rail for the output. Full output swing at the output of op amp can be obtained. There is a need of improvement in high frequencies so that the high speed performance gets improved.

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