THERMALLY AWARE MODELING AND ANALYSIS OF MIXED CNT FOR FUTURE NANOSCALE TECHNOLOGY NODES

A THESIS

submitted in partial fulfillment of the

requirements for the award of the degree

of

DOCTOR OF PHILOSOPHY

Submitted by

Gurleen Dhillon

Reg No.901706025

Under The Supervision of

Dr. Karmjit Singh Sandha

(Associate Professor, TIET)

Department of Electronics and Communication Engineering

Thapar Institute of Engineering and Technology

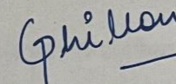
Patiala (147004)

August 2023

CANDIDATE'S DECLARATION

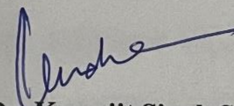
I hereby certify that the work which is being presented in the thesis entitled "**Thermally Aware Modeling And Analysis Of Mixed CNT For Future Nanoscale Technology Nodes**" in partial fulfillment of the requirement for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electronics and Communication Engineering of the Thapar University, Patiala is an authentic record of my work carried out during a period from July 2017 to August 2023 under the supervision of Dr. Karmjit Singh Sandha, Associate Professor, Thapar Institute of Engineering and Technology, Patiala.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.



Gurleen Dhillon
(Reg.no.901706025)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.



Dr. Karmjit Singh Sandha

Associate Professor
Electronics & Comm. Engineering Dept
TIET, Patiala.

ABSTRACT

With the upgrades in technology, the number of functionalities is escalating on advanced integrated chips. In this trend, the number of global interconnects that helps to join these circuit chips is also increasing. Global interconnects are long interconnects that run globally across the chip and help to associate global signals like a clock, power, and round to all modules. In this way, the parasite associated with longer interconnects increases, and ultimately the performance of interconnects is degraded at scaled nodes. So, an indispensable need of the hour demands a suitable material that can be employed for interconnect applications in the coming times. Carbon nanotubes have been advised as the best alternative to copper interconnects, which suffered from electromigration, grain boundary scattering, and surface roughness after 45nm technology node. Because carbon nanotubes possess notably good electrical, mechanical, and thermal properties, they can easily oust copper for interconnect applications. Formed with the layer of carbon in the form of graphite and rolled up in a cylindrical shape, carbon nanotubes are classified into single-walled carbon nanotubes (single layer of graphite), multi-walled carbon nanotubes (multiple layers of graphite rolled concentrically) and double-walled carbon nanotube (two layers of graphite rolled concentrically). Since a single carbon nanotube offers a high value of resistance, the bundle of interconnect is made by placing nanotubes parallelly in the bundle.

Interconnects can be well presented by transmission lines with distributed impedance parameters and are driven by CMOS transistors (using the alpha-power law model). A quick and concise comparative analysis has been done between copper and carbon nanotubes to determine impedance parameters, propagation delay, power dissipation, and power-delay product. It has been analyzed that carbon nanotubes offer better performance than copper at global lengths. The present work focuses on a new mixed class of carbon nanotubes which are formed by changing different

positions of multi-walled and double-walled carbon nanotubes. The equivalent circuit parameters of mixed carbon nanotubes are extracted with the help of single conductor models of multi-walled and double-walled carbon nanotubes. Their impedance parameters are determined to obtain the output waveform analytically and to study the effect of delay, power, and power-delay product.

The simulated results of various mixed carbon nanotubes comprising multi-walled and double-walled carbon nanotubes are then compared with existing carbon nanotubes and copper. The results in the present work present that concerning delay at the final output, the power dissipated and power-delay product, multi and double-walled carbon nanotube bundled structure in which double-walled carbon nanotubes are located in the center and multi-walled carbon nanotubes are placed along the periphery of the bundle yield the best performance among all other interconnect materials. The presence of double-walled carbon nanotubes in the center helps in good conductivity and multi-walled carbon nanotubes along the periphery help in the decreasing coupling, thus these two properties of the bundle come up together to perform better than other counterparts. A brief analysis of crosstalk's effect (both dynamic and functional crosstalk) is also performed for mixed carbon nanotube bundled structures at 32nm, 22nm, and 16nm technology nodes. The stability also helps in determining the performance of the circuit. The stability of multi-walled and double-walled carbon nanotube bundled structures is also determined with the help of rise time, peak overshoot, and Nyquist plots.

The effect of temperature is also added up to analyze the performance of interconnect materials. The temperature is varied from 200 Kelvin to 500 Kelvin. Different types of electron-phonons scattering phenomena (acoustic scattering till 300K and optical scattering at 300K and beyond) are encountered with the increase in temperature which tends to lower the effective mean free path of the conducting electrons. Results also demonstrate that with the inclusion of the effect of temperature, the delay of global interconnects increases and degrades their performance. The

result of the proposed models is also compared with the mixed CNT models existing in the literature. Analytical formulations are done to obtain delay readings and are compared with simulated delay readings.

Based on the results presented, it is found that the mixed carbon nanotube bundle structure (with multi-walled carbon nanotubes in the center and double-walled carbon nanotubes along the periphery of the bundle) outperforms all carbon nanotube bundles (MWCNTs, SWCNTs, DWCNTs) and copper at scaled technology nodes in terms of delay, power and power-delay product. The results emphasize that the study of mixed carbon nanotube bundled structures for interconnects shall be important and useful good-performance integrated chips at advanced nano-regime nodes.

ACKNOWLEDGEMENT

The author expresses her sincere regard and gratitude to her worthy supervisor Dr. Karmjit Singh Sandha, Associate Professor, Department of Electronics and Computer Engineering (E&CE), Thapar Institute of Engineering and Technology, Patiala, for his inspiration, expert guidance, moral boosting, continuous encouragement, and appreciation, which were the vital factors in the successful completion of the present work. I sincerely appreciate their pronounced individualities, and humanistic and warm personal approach, which has given me the strength and will to carry out this research work on a steady and smooth course. I humbly acknowledge a lifetime's deep gratitude to my guide Dr. Karmjit Singh Sandha.

I wish to express my sincere appreciation to my professor and Head ECED, Dr. Alpana Agarwal, for her timely, informative feedback and support during this effort. It has been a great pleasure to learn from her during the process of expanding and refining my research.

My sincere thanks are to Dr. Mayank Kumar Rai, Dr. Mohit Kumar, Dr. Sanjay Kumar, ECED; Dr. Smarajit Ghosh, EIED, Thapar Institute of Engineering and Technology, Patiala for being members of my research committee and sparing their valuable time for critically examining the work and valuable suggestions.

I am also thankful to the entire faculty and staff of the Electronics & Communication Engineering Department for the help and moral support which went along the way for the successful completion of this work.

The author is grateful to all, who generously gave their time and evinced personal care and concern in all stages of this work. I render my gratitude to the Almighty who bestowed self-confidence, ability, and strength in me to complete this work for not letting me down at the time of crisis and showing me the silver lining in the dark clouds.

I wholeheartedly thank my respected and loved parents for their good wishes and prayers.

My parents have always wanted the best for me and I admire their determination and sacrifice. I owe my deepest gratitude to my elder brother Paramveer Singh, for constantly encouraging me throughout this work. I also thank my husband Jai for being my backbone in thick and thin times and providing me with moral support. I do not find enough words with which I can express my indebtedness to my dear friends Neeru, Kriti, Amoldeep, Gurprince, Manju, Ramneek, Aditi, Arun, Manjeet, and Arshdeep for their support and inspiration which went a long way in the successful competition of the present study.

I acknowledge with utmost warmth the everlasting love of my dearest son Abeer for his love and patience when I was away from him since he was born amidst my journey.

Date:23rd August 2023

Place: Patiala

CONTENTS

	Page
Abstract	*iii-v*
Acknowledgment	*vi-vii*
List of Figures	*xi-xvi*
List of Tables	*xvii-xviii*
List of Symbols	*xix-xx*
List of Abbreviation	*xxi*
1 Introduction	**1-11**
1.1 Classification of Interconnects based on Length and Cross-section	**2**
1.2 Interconnect Models	**3**
1.2.1 Lumped Model Designing	**3**
1.2.2 Distributed Model Designing	**3**
1.3 Need of Repeaters for Long Interconnects	**4**
1.4 Classification of Interconnects based on the type of materials	**4**
1.5 Carbon nanotubes (CNT) as VLSI Interconnect	**6**
1.6 Aim of Thesis	**9**
1.7 Organization of Thesis	**10**
2 Literature Survey	**12-35**
2.1 Interconnect Models	**12**
2.2 Copper and CNT as Interconnects	**15**
2.2.1 Problems Faced by Copper Interconnect	**15**
2.2.2 Carbon nanotube as Interconnect	**16**
2.3 Effect of Temperature on Interconnects	**24**
2.4 Mixed CNT bundle as Interconnect	**27**
2.5 Crosstalk and Stability of CNT interconnects	**29**
2.6 Identified gaps in the literature	**33**
2.7 Objectives of the study	**34**
2.8 Research Methodology	**34**

3 Circuit Analysis of Mixed CNTS **36-64**

3.1 Electrical equivalent circuit modeling of interconnects **36**

3.1.1 Copper as an Interconnect material **36**

3.1.2 Single-walled CNT as an Interconnect material **39**

3.1.3 Multi-walled CNT as an Interconnect material **42**

3.1.4 Double-walled CNT as an Interconnect material **46**

3.2 Performance comparison between copper, SWCNT, MWCNT, and DWCNT **48**

3.2.1 Delay-based simulation results **49**

3.2.2 PDP-based simulation results **50**

3.3 Mixed bundle CNT as an Interconnect material **50**

3.3.1 Development of MDCB structures **51**

3.3.2 Determination of RLC values of MDCB structures **55**

3.4 Delay and PDP-based comparison between MDCB interconnects **58**

3.5 Performance comparison between copper, SWCNT, MWCNT, DWCNT, and MDCB structures **60**

3.5.1 Delay based evaluation **60**

3.5.2 PDP based results **62**

3.6 Chapter Summary and Contribution **64**

4 Temperature Dependent Modelling of Mixed CNTS **65-81**

4.1 Temperature-dependent MFP of CNTs **65**

4.2 Temperature-based delay and PDP results **67**

4.2.1 Performance of copper, SWCNT, DWCNT, and MWCNT at 500µm and 1000µm length **67**

4.2.2 Performance of various MDCB structures at 500µm and 1000µm length **71**

4.3 Comparison of temperature-sensitive delay and PDP of copper, SWCNT, DWCNT, MWCNT, and MDCB structures **75**

4.4 Chapter Summary and Contribution **81**

5 Impact of Crosstalk & Stability in Mixed Bundle CNTS **82-105**

5.1 Crosstalk in mixed bundle CNTs **83**

5.1.1 Dynamic Crosstalk **83**

5.1.2 Functional Crosstalk **93**

5.2 Role of Temperature **95**

5.3 Stability analysis **97**

5.3.1 Transient response of mixed CNTs **97**

5.3.2 Maximum overshoot and rise-time **100**

5.3.3 Nyquist Plots **102**

5.4 Chapter Summary and Contribution **104**

6 Comparative Analysis and Analytical Modeling of MDCB Structures **106-115**

6.1 Comparison of proposed MDCB structures with literature **106**

6.2 Analytical delay modeling of mixed CNT bundle interconnects **111**

6.3 Chapter Summary and Contribution **115**

7 Conclusion and Future Scope **116-118**

7.1 Conclusion **116**

7.2 Future Work **117**

List of Publications **119**

References **120-133**

LIST OF FIGURES

Sr.	Title	Page
Figure 1.1	Schematic of Interconnects employed in a circuit	1
Figure 1.2	Representation of Interconnect layers	2
Figure 1.3	L, T and π Lumped Model Designs	3
Figure 1.4	Distributed Model Design	4
Figure 1.5	Interconnect distributed among n-sections through repeaters technique	4
Figure 1.6	Single-wall carbon nanotube structure	7
Figure 1.7	Multi-wall carbon nanotube structure	7
Figure 1.8	Double-wall carbon nanotube structure	7
Figure 1.9	Chirality based on the nanotube axis	8
Figure 1.10	Configurations of CNT based on chirality (a) Zigzag configuration (b) Armchair configuration	8
Figure 2.1	Propagation delay-based comparison of different interconnection techniques concerning values of interconnect parasitic	13
Figure 2.2	Normalized delay (ΓCNT/ ΓCu) at (a) intermediate length (b) global length of interconnect	19
Figure 2.3	Variation in normalized delay and power with the diameter at 32 nm and 22 nm technology node	20
Figure 2.4	Resistivity comparison of copper, SWCNT, and MWCNT over length varied from 1µm to 1000µm at 32 nm, 22 nm, and 14 nm technology node	21
Fure 2.5	Comparison of delay time versus years between copper, SWCNT, and DWCNT interconnect	23
Figure 2.6	Temperature-dependent resistance of SWCNT at varying interconnect lengths	25
Figure 2.7	Temperature-dependent mean free paths of SWCNT at different bias conditions	25

Figure 2.8	Delay comparison of SWCNT, MWCNT, and Mixed bundle interconnect	28
Figure 2.9	Gain versus frequency plot of MLGNR and MWCNT interconnects at varying lengths	32
Figure 3.1	Electrical model of an interconnect material	36
Figure 3.2	Cross-section of copper wires	37
Figure 3.3	Impedance values of copper at different nanotechnology nodes for length varied from 100µm-1000µm (a) Resistance (b) Inductance (c) Capacitance	38
Figure 3.4	Structure of single-walled CNT placed above the ground plane	39
Figure 3.5	Electrical model of SWCNT	39
Figure 3.6	Bundled SWCNT placed over a ground plane	40
Figure 3.7	Impedance values of SWCNT at different technology nodes for length varied from 100µm-1000µm (a) Resistance (b) Inductance (c) Capacitance	42
Figure 3.8	The physical structure of MWCNT placed over the ground plane	43
Figure 3.9	Electrical equivalent model of MWCNT	44
Figure 3.10	Impedance values of MWCNT at various technology nodes for length varied from 100µm-1000µm (a) Resistance (b) Inductance (c) Capacitance	45
Figure 3.11	The physical structure of DWCNT	46
Figure 3.12	Electrical equivalent model of DWCNT interconnect	46
Figure 3.13	Impedance values of DWCNT at various technology nodes for length varied from 100µm-1000µm (a) Resistance (b) Inductance (c) Capacitance	48
Figure 3.14	Distributed element approach setup used for determining signal delay using T-spice	49
Figure 3.15	Analysis of delay between copper, SWCNT, MWCNT, and DWCNT at different technology nodes	49
Figure 3.16	Analysis of PDP among copper, SWCNT, MWCNT, and DWCNT at various technology nodes	50
Figure 3.17	Different types of MDCB structures	51
Figure 3.18	A hierarchical model of MDCB Interconnect	52
Figure 3.19	MTL model of MDCB interconnects	53
Figure 3.20	Simplified electrical structure of MDCB interconnects (stage-1)	54

Figure 3.21 ESC model of MDCB interconnects (final stage) 54
Figure 3.22 Distributed element model used for simulation of MDCB interconnects 55
Figure 3.23 Resistance values of MDCB structures for variable global interconnect lengths at different nanotechnology nodes 56
Figure 3.24 Inductance values of MDCB structures for variable global interconnect lengths at different nanotechnology nodes 57
Figure 3.25 Capacitance values of MDCB structures for variable global interconnect lengths at different nanotechnology nodes 57
Figure 3.26 Comparison of delay between different MDCB structures at variable lengths for different nanotechnology nodes 58
Figure 3.27 Comparison of PDP between different MDCB structures at variable lengths for different nanotechnology nodes 58
Figure 3.28 Comparison of delay between different MDCB structures at different nanotechnology nodes for (a) 500µm (b) 1000µm 59
Figure 3.29 Comparison of PDP between different MDCB structures at 32nm, 22nm, and 16nm technology nodes for (a) 500µm (b) 1000µm 59
Figure 3.30 Delay comparisons between copper, SWCNT, MWCNT, DWCNT, and different MDCB structures at different global lengths for different nanotechnology nodes 61
Figure 3.31 PDP comparison between copper, SWCNT, MWCNT, DWCNT, and different MDCB structures at different global lengths for different nanotechnology nodes 63
Figure 4.1 Temperature-dependent acoustic, optical absorption, emission, and effective MFP of electrons at 22nm technology node for (a) d=1nm (b) d=8nm 66
Figure 4.2 Temperature-sensitive delay of copper, SWCNT, DWCNT, and MWCNT for 500µm and 1000µm interconnect length at 32nm technology node 68
Figure 4.3 Temperature-sensitive delay of copper, SWCNT, DWCNT, and MWCNT for 500µm and 1000µm interconnect length at 22nm technology node 68
Figure 4.4 Temperature-sensitive delay of copper, SWCNT, DWCNT, and MWCNT for 500µm and 1000µm interconnect length at 16 nm technology node 68

Figure 4.5	Temperature-sensitive PDP of copper, SWCNT, DWCNT, and MWCNT for 500µm and 1000µm interconnect length at 32nm technology node	70
Figure 4.6	Temperature-sensitive PDP of copper, SWCNT, DWCNT, and MWCNT for 500µm and 1000µm interconnect length at 22nm technology node	70
Figure 4.7	Temperature-sensitive PDP of copper, SWCNT, DWCNT, and MWCNT for 500µm and 1000µm interconnect length at 16nm technology node	70
Figure 4.8	Temperature-sensitive delay of MDCB structures for 500µm and 1000µm interconnect length at 32nm technology node	72
Figure 4.9	Temperature-sensitive delay of MDCB structures for 500µm and 1000µm interconnect length at 22nm technology node	72
Figure 4.10	Temperature-sensitive delay of MDCB structures for 500µm and 1000µm interconnect length at 16nm technology node	72
Figure 4.11	Temperature-sensitive PDP of MDCB structures for 500µm and 1000µm interconnect length at 32nm technology node	74
Figure 4.12	Temperature-sensitive PDP of MDCB structures for 500µm and 1000µm interconnect length at 22nm technology node	74
Figure 4.13	Temperature-sensitive PDP of MDCB structures for 500µm and 1000µm interconnect length at 16nm technology node	74
Figure 4.14	Comparison of temperature-sensitive delay of copper, SWCNT, DWCNT, MWCNT, and MDCB structures for1500µm interconnect length at (a) 32nm (b)22nm (c) 16nm tech.	76
Figure 4.15	Comparison of temperature-sensitive delay of copper, SWCNT, DWCNT, MWCNT, and MDCB structures for 2000 µm interconnect length at (a) 32nm (b)22nm (c) 16nm tech.	77
Figure 4.16	Comparison of temperature-sensitive PDP of copper, SWCNT, DWCNT, MWCNT and MDCB structures for1500µm interconnect length at (a) 32nm (b) 22nm (c) 16nm tech.	79
Figure 4.17	Comparison of temperature-sensitive PDP of copper, SWCNT, DWCNT, MWCNT, and MDCB structures for 2000µm interconnect length at(a) 32nm (b) 22nm (c) 16nm tech.	80
Figure 5.1	Equivalent circuit of crosstalk affected coupled global mixed CNT interconnects	82

Figure 5.2	a) Block diagram representation of even/in-phase mode of dynamic crosstalk i) Aggressor: 0 to 1 and Victim: 0 to 1. Comparison of temperature sensitive delay of mixed CNT structures with and without crosstalk effect b) at 32nm c) at 22nm and d) at 16nm technology node	85
Figure 5.3	a) Block diagram representation of even/in-phase mode of dynamic crosstalk i) Aggressor: 1 to 0 and Victim: 1 to 0. Comparison of temperature sensitive delay of mixed CNT structures with and without crosstalk effect b) at 32nm c) at 22nm and d) at 16nm technology node	86
Figure 5.4	a) Block diagram representation of odd/out-phase mode of dynamic crosstalk i) Aggressor: 0 to 1 and Victim: 1 to 0. Comparison of temperature sensitive delay of mixed CNT structures with and without crosstalk effect b) at 32nm c) at 22nm and d) at 16nm technology node	87
Figure 5.5	a) Block diagram representation of odd/out-phase mode of dynamic crosstalk ii) Aggressor: 1 to 0 and Victim: 0 to 1. Comparison of temperature sensitive delay of mixed CNT structures with and without crosstalk effect b) at 32nm c) at 22nm and d) at 16nm technology node	89
Figure 5.6	Dynamic crosstalk induced delay comparison of four MDCB structures without crosstalk, with even mode and with odd mode of switching a) at 32nm b) at 22nm, and c) at 16nm technology	91
Figure 5.7	Four cases of functional crosstalk of MDCB coupled interconnects	93
Figure 5.8	Dynamic crosstalk influenced the transient response of MDCB 1 structure for 1000µm length a) at 32nm tech. b) at 22nm tech. c) 16nm tech. the node at 200K-500K	96
Figure 5.9	Transient response for four MDCB structures operating at temperatures ranging from 200K-500K for 32nm technology node	98
Figure 5.10	Transient response for four MDCB structures operating at temperatures ranging from 200K-500K for 22nm technology node	98
Figure 5.11	Transient response for four MDCB structures operating at temperatures ranging from 200K-500K for 16nm technology node	99
Figure 5.12	Nyquist plot of four MDCB structures for 1000µm interconnect length at 32nm technology node	102

Figure 5.13	Nyquist plot of four MDCB structures for 1000µm interconnect length at 22nm technology node	103
Figure 5.14	Nyquist plot of four MDCB structures for 1000µm interconnect length at 16nm technology node	104
Figure 6.1	Various types of Mixed CNT Bundled structures (multi and double-wall CNT bundles (MDCB) and multi and single-wall CNT bundles (MSCB))	106
Figure 6.2	Propagation delay for various mixed CNT bundle structures at 22nm technology node for 1000µm interconnect length	107
Figure 6.3	Temperature sensitive delay for various mixed CNT bundle structures (MDCBs and MSCBs) at (a) 32nm (b) 22nm and (c) 16nm technology node	108
Figure 6.4	Temperature sensitive power for various mixed CNT bundle structures (MDCBs and MSCBs) at (a) 32nm (b) 22nm and (c) 16nm technology node	109
Figure 6.5	Temperature- sensitive PDP for various mixed CNT bundle structures (MDCBs and MSCBs) at (a) 32nm (b) 22nm and (c) 16nm technology node	110
Figure 6.6	Simulated and analytical delay comparison of four mixed CNTs (MDCB 1, MDCB 2, MDCB 3, and MDCB 4) for 1000µm interconnect length at 22nm technology node	112
Figure 6.7	Delay comparisons of four mixed CNTs (MDCB 1, MDCB 2, MDCB 3and MDCB 4) for 1000µm interconnect length at 22nm technology node	112
Figure 6.8	Simulated and analytical delay comparison of four mixed CNTs (MDCB 1, MDCB 2, MDCB 3, and MDCB 4) for 1000µm interconnect length at 16nm technology node	113
Figure 6.9	Delay comparisons of four mixed CNTs (MDCB 1, MDCB 2, MDCB 3, and MDCB 4) for 1000µm interconnect length at 16nm technology node	114

LIST OF TABLES

Sr.	Title	Page
Table 1.1	Comparison of various materials based on different properties	5
Table 1.2	Comparison of different properties of Aluminum and Copper	6
Table 2.1	Comparison of different properties of CNT and Copper	17
Table 3.1	RLC values of copper at variable lengths for various technology nodes	37
Table 3.2	RLC values of SWCNT at variable lengths for various nanotechnology nodes	41
Table 3.3	RLC values of MWCNT at variable lengths for variou nanotechnology nodes	45
Table 3.4	RLC values of DWCNT at different lengths for various nanotechnology nodes	47
Table 3.5	RLC values of Mixed CNT bundle structures at variable lengths (500µm, 1000µm, 1500µm, and 2000µm) for different nanotechnology nodes	55
Table 3.6	Delay-based comparison of copper, SWCNT, MWCNT, DWCNT, and MDCB structures at various lengths for different nanotechnology nodes	60
Table 3.7	PDP-based comparison of copper, SWCNT, MWCNT, DWCNT, and MDCB structures at various lengths for different nanotechnology nodes	62
Table 4.1	Temperature sensitive delay (ns) of copper, SWCNT, DWCNT, and MWCNT for 500µm and 1000µm interconnect lengths at various nanotechnology nodes	67
Table 4.2	Temperature sensitive PDP (µW.ns) of copper, SWCNT, DWCNT, and MWCNT for 500µm and 1000µm interconnect lengths at various nanotechnology nodes	69
Table 4.3	Temperature sensitive delay of MDCB structures for 500µm and 1000µm interconnect lengths at various nanotechnology nodes	71

Table 4.4	Temperature-sensitive PDP of MDCB structures for 500μm and 1000μm interconnect lengths at various nanotechnology nodes	73
Table 4.5	Comparison of temperature sensitive delay of copper, SWCNT, DWCNT, MWCNT, and MDCB structures for 1500μm and 2000μm interconnect lengths	75
Table 4.6	Comparison of temperature-sensitive PDP of copper, SWCNT, DWCNT, MWCNT, and MDCB structures for 1500μm and 2000μm interconnect lengths	78
Table 5.1	Propagation delay (ns) values for without and with (out-phase and in-phase mode) crosstalk influenced mixed (multi and double-wall) CNT structures at 1000μm interconnect length over the temperature range 200-500K at 32nm, 22nm, and 16nm technology	90
Table 5.2	Increase in delay (%) of MDCB structures during out-phase and in-phase mode of dynamic crosstalk switching	92
Table 5.3	Glitch values of mixed CNT coupled interconnects	93
Table 5.4	Functional crosstalk noise values (percentage difference) of MDCB-1 structure with other structures.	94
Table 5.5	Maximum percentage overshoot and switching delay for MDCB structures at 32nm, 22nm, and 16nm technology nodes	101
Table 6.1	Values of propagation delay for Mixed CNT Structures	106
Table 6.2	Simulated and analytical delays for various MDCB structures at 22 nm technology node	111
Table 6.3	Simulated and analytical delays for various MDCB structures at 16 nm technology node	113

LIST OF SYMBOLS

Symbol	Description
Ω	Ohm
λ	Mean Free Path
ε	Damping Factor
δ	Spacing between CNTs (Vander-wal distance=0.34nm)
A	Ampere
cm	Centi-meter
Cu	Copper
C	Capacitance
e	Electron charge
F	Farad
h	Planck's Constant
H	Height of Bundle
J	Joule
k	Kilo
K	Kelvin
l	Length of interconnect
L	Inductance
$\%M_p$	Peak Overshoot Voltage Percentage
m	Meter
nm	Nano-meter
ns	Nano-second

nH	Nano- Henry
R	Resistance
s	Second
tech.	Technology
t_r	Rise time
T	Temperature in Kelvin
μm	Micro-meter
v_f	Fermi-velocity
$V_{i/p}$	Input voltage
$V_{o/p}$	Output voltage
W	Watt

LIST OF ABBREVIATIONS

Abbreviation	Description
CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nanotube
CVD	Chemical Vapor Deposition
DWCNT	Double-Wall CNT
ESC	Equivalent Single Conductor
GHz	Giga-Hertz
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
MDCB	Multi-wall and Double-wall CNT Bundle
MESC	Multi Equivalent Single Conductor
MFP	Mean Free Path
MLGNR	Multi-Layer Graphene Nano-Ribbon
MSCB	Multi-wall and Single-wall CNT Bundle
MTL	Multi Transmission Line
MWCNT	Multi-Wall CNT
PDP	Power Delay Product
PTM	Predictive Technology Model
SPICE	Simulation Program for Integrated Circuit Emphasis
SWCNT	Single-Wall CNT
VLSI	Very Large-Scale Integration

1. INTRODUCTION

The electronics industry has exhibited a wonderful rise in recent years. After the introduction of VLSI circuits in the 1970s, plentiful functionalities can be performed with single IC chips [1,2]. The high computational speed and proficient processing power are the driving strength for technology upgrades. And with moving years, the electronic market, and advanced technology demand high-performance and high-density VLSI chips. The number of complex operations is multiplying in small packages, so there has been a very steady rise in the level of integration as well [3-5]. Scaling (shrinkage of dimensions) in VLSI circuits is done to reduce the dimensions of the device systematically, keeping the geometric ratios preserved at the same time. It is crucial for improving performance, reducing power consumption, enhancing density, maintaining signal integrity, reducing costs, and enabling technological advancements in the semiconductor industry. A VLSI integrated circuit is made by assembling thousands of transistors or devices or modules onto a single chip. A thin conducting material, which helps in giving an electrical connection among various nodes of an electrical circuit as shown in Figure 1.1, is called interconnect.

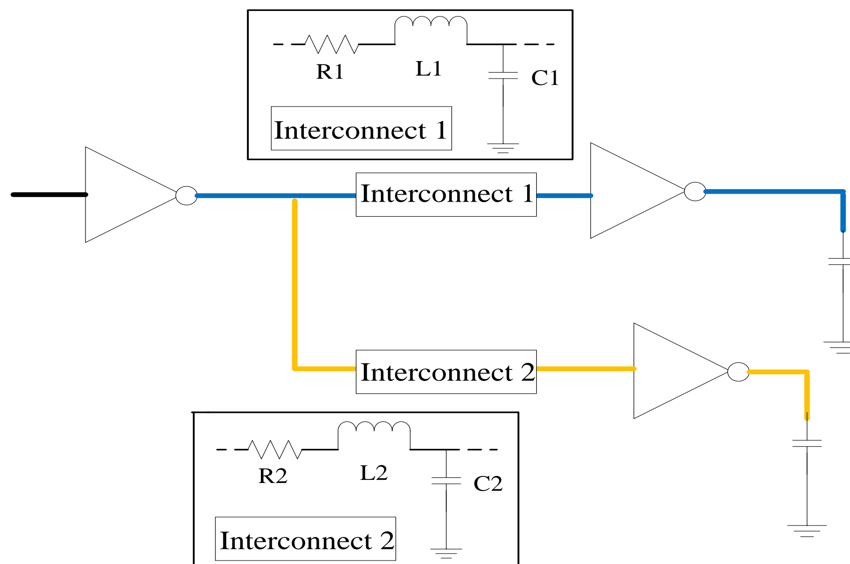


Figure 1.1 Schematic of Interconnects employed in a circuit.

In this manner dimensions of both the devices and interconnects need to be scaled down. At the local lengths, the conduction of the circuit is mainly dependent upon the devices. However, longer lines' performance overrules the circuit's net performance due to large values of impedance parameters at the global level [6-8]. So, interconnect issues need to be addressed at scaled technology nodes. The exquisiteness of integrated circuits lies in the total performance concerning parameters like total area, net cost, high speed, and less power of interconnected

modules [9-10]. If the technology somehow slips to have a good interconnect, then the overall performance of the IC will be corrupted due to high parasitic (resistance, inductance, and capacitance) leading to more delay than transistors or logic gates. To determine the performance of the circuit, interconnects can be represented by equivalent RLC models as demonstrated above in Figure 1.1.

1.1 Classification of Interconnects based on Length and Cross-section

Interconnects are broadly categorized into three groups depending upon the length and cross-section area local, intermediate/semi-global, and global interconnects as shown in Figure 1.2.

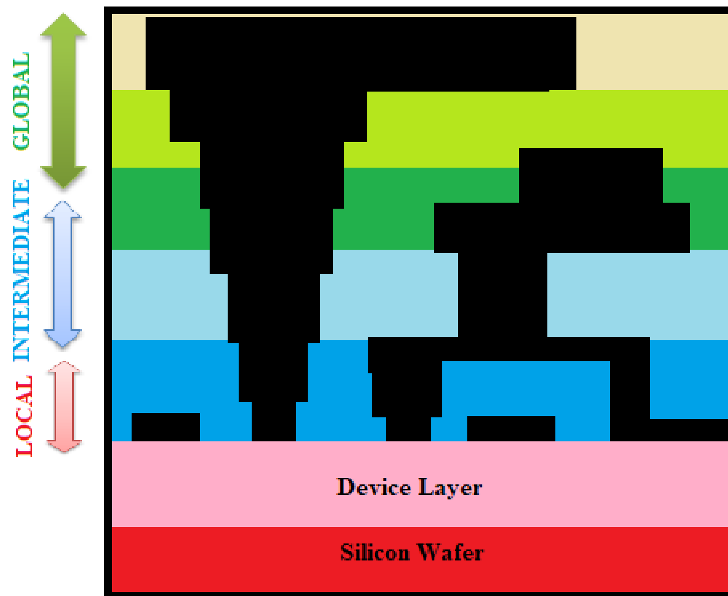


Figure 1.2 Representation of Interconnect layers [2]

- Local interconnects can regularly obtain a length of a few nanometres to connect nearby nodes on the chip. They are used for linking gates and transistors within a module. For these short-length and high-resistance wires, the maximum delay is given by the device themselves and they should be able to operate in an elevated temperature range.
- Intermediate interconnects are bigger than localized interconnects and are also termed semi-global interconnects. Intermediate wiring can help in giving timers and other signals within or nearby functional blocks with lengths of a few hundred micrometers. They help to deal with both short and long-length interconnections.
- The longest in length on the chip, i.e., Global interconnects help in providing bus, power, and clock signals to all modules and devices [11-14]. Global interconnects can extend from ~500μm to 1 mm and even more in length. The power dissipation and propagation delay play a pivotal role in deciding the performance of global interconnects.

1.2 Interconnect Models

In integrated circuits, interconnect wires can be modeled with the help of transmission lines. The performance of interconnects is determined from their equivalent electrical models by studying their parasitic in detail. Interconnect modeling can be done in diverse ways depending on how impedance parameters are arranged [12-16]. Analyse their performance, and the lumped and distributed models of interconnect lines are elucidated in the upcoming sub-sections.

1.2.1 Lumped Model Designing

The electrical parameters i.e., resistance (R), inductance (L), and capacitance (C) of interconnect lines are concentrated into ideal electrical components for lumped designed models [14,15]. Various lumped model designs are exhibited in Figure 1.3 relying upon the arrangement and the way parameters are placed forming the shape they are connected, like L-model lumped design, T-model lumped design, and π-model lumped design.

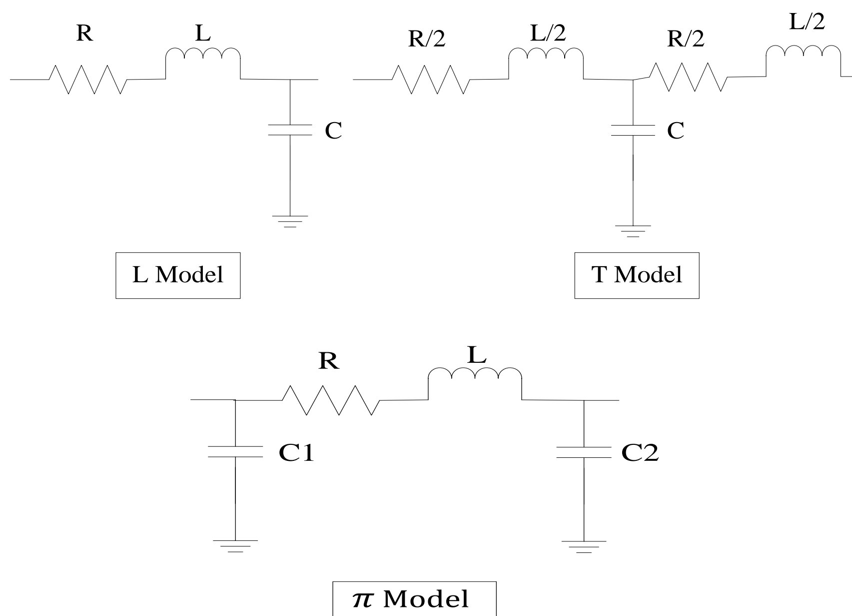


Figure 1.3 L, T and π Lumped Model Designs [13]

1.2.2 Distributed Model Designing

The distributed model is designed with the help of repeaters to increase the driving capacity of the circuit by overcoming large impedance values at long/global lengths and thereby decreasing the overall delay of the circuit for long wires [14]. The distributed models are like multi-stage lumped circuits. The same lumped sub-sections are repeated across the total global length of the interconnect line thereby distributing the total effect of parasitic into smaller regions forming a multi-stage distributed network as presented in Figure 1.4.

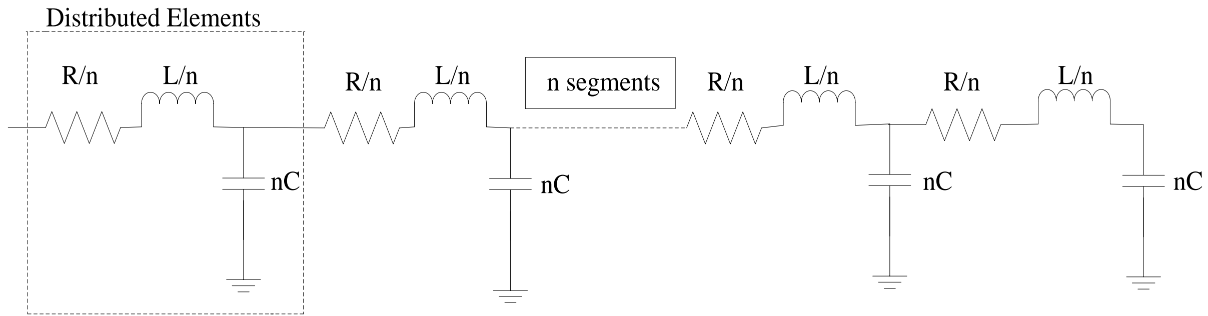


Figure 1.4 Distributed Model Design [14]

1.3 Need of Repeaters for Long Interconnects

The impedance parameters of interconnect wires possess a direct relationship with the length of interconnects. The impedance value of interconnect increases with the lengthiness of the line; therefore, the delay of the circuit shows an acceleration with the length. With scaling at leading-edge technology nodes, the large impedance values of semi-global and global interconnect affect the net performance of the ICs [17,18]. Their high impedance values are well compensated by introducing repeaters to decrease the net delay of the circuit.

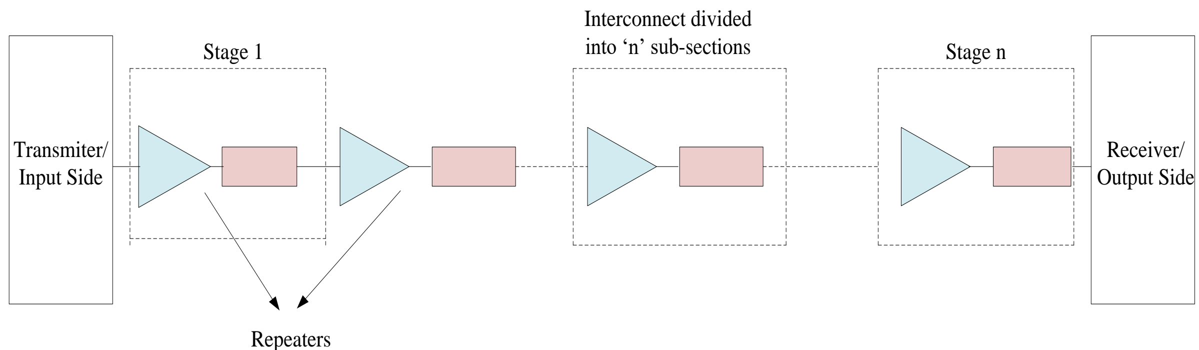


Figure 1.5 Interconnect distributed among n-sections through repeaters technique [12]

Repeaters help in dividing the long interconnect length into certain segments and each sub-section is driven by a buffer (CMOS inverter) as advertised in Figure 1.5. So, the large impedance value is divided among sub-sections and helps in achieving desirable performance concerning factors like delay and PDP [18-20]. The performance concerning propagation delay, and power dissipation, and PDP is attained by using the optimum number and optimum-sized repeaters [21-24] using the distributed model approach.

1.4 Classification of Interconnects based on the Type of Materials.

Several types of interconnect materials like copper, silver, gold, aluminium, and tungsten have also been introduced and comparisons of their properties like resistivity, thermal conductance,

melting point temperature, corrosion, and adhesion to SiO_2 have been listed in Table 1.1. Silver exhibits the least resistivity and best thermal conductivity, and Tungsten shows the highest melting point (3387 Kelvin) of all other materials listed in Table 1.1. The melting point of aluminium is the lowest, but it provides better adhesion with ploy-silicon than copper, silver, gold, and tungsten.

Table 1.1 Comparison of various materials based on different properties.

Properties	**Resistivity (μΩ.cm)**	**Thermal Conductivity (10^3.W/mK)**	**Melting Point (K)**	**Corrosion in air**	**Adhesion to SiO_2**
Copper (Cu)	1.67	0.398	1085	Poor	Not good
Silver (Ag)	1.59	0.425	962	Poor	Not good
Gold (Au)	2.35	0.315	1064	Excellent	Not good
Aluminum (Al)	2.66	0.238	660	Good	Good
Tungsten (W)	5.65	0.174	3387	Good	Not good

Metals like aluminium and copper have been extensively used as interconnect materials for VLSI circuits [25, 26]. Their strengths and weakness are summarised in Table 1.2. Aluminium yields good conductivity, better adherence to the dielectric, and forms good ohmic contacts. When compared between the two, the copper shows a better result as interconnect material in terms of conductivity and delay than aluminium.

Table 1.2 Comparison of different properties of Aluminum and Copper

Interconnect Material	**Advantages**	**Disadvantages**
Aluminum	• Good conductivity • Good adherence to the dielectric material • Forms good ohmic contacts	• Electromigration • Pure aluminum (2.66 μΩ.cm) has more resistivity than copper (1.67 μΩ.cm). So, it is used as an alloy comprising aluminum with copper and silicon to minimize its resistivity. • Offers short MFP of the order of a few nanometers at nano-scaled technology nodes
Copper	• Higher conductivity and delay than aluminum. • High Melting point than Aluminum • More bearable to electromigration than Aluminum; copper can bear (x5) more current density at deep submicron technologies	• Electromigration at high current densities beyond 45nm technology • Surface roughness and grain boundary scattering • High resistivity leads to further high increases in the delay of the circuit and leads to more power dissipation of the circuit

The melting point of silver (962 K) is far more than aluminium (660 K). Though with technological advancement, electromigration problems are faced in both materials. As technology advances and is scaled beyond the 45 nm technology node, the conducting electrons of copper suffer collisions and have shorter mean free paths. As a result of reduced MFP, the resistance of copper increases and conductance decreases and as a result, CNTs are introduced. [27-29]. Also, in a polycrystalline material, the grains which are developed at the interface layer between two crystallites increase scattering and reduce the MFP of electrons. This effect increases with scaling and is termed grain boundary scattering. Due to increased reflections and collisions of electrons, they undergo surface scattering and introduce surface roughness into the material. Deviated and scattered electrons emit and absorb different phonons [30,31]. The thermal resistivity and surface-related impurity defects of material also increase [32].

The transport of momentum takes place among the conducting electrons and diffused metal atoms leading to the gradual displacement of ions. As a result, the mobility of electrons further decreases, and the transport of material takes place leading to electromigration. Such fatal issues in copper beyond the 45 nm technology node, led to its failure as an interconnect material in ICs [28,29]. Due to the increase in the resistance of copper, the delay of the circuit increases and degrades the overall performance of high-speed VLSI circuits. An alarming situation is seen and the need for an interconnect material is observed at deep submicron technology nodes which can perform well under area, speed, and power. So, carbon nanotube interconnects materials emerged as an indispensable need of the VLSI market.

1.5 Carbon nanotubes (CNT) as VLSI Interconnect

Carbon atoms in CNTs placed in sp^2 configuration form the strongest and stiffest structure. These CNTs have provided the best alternative to conventional interconnect materials because of their properties like large current carrying ability ($10^{14}A/m^2$), high thermal conductance (5800 W/mK), and high mechanical strength [33-44]. The most popular techniques to form CNTs are arc discharge (with high current), laser ablation (with a high-intensity laser), and chemical vapor deposition (CVD) (utilizing heat). Commonly, the CVD method at elevated temperatures (850 °C to 1000 °C) in the presence of carbon source gas like methane and iron oxide acting as the catalyst is used to develop high-quality CNTs.

CNT tube is a material made up of an atomic layer of carbon (graphite) and rolled up in the form of a long and hollow cylindrical tube having a diameter in the nanometer range. The

number of graphene sheets rolled up, leads to broadly two types of CNTs [45-48] as shown in Figures 1.6 and 1.7.

- Single-wall CNT (SWCNT) – formed with only one wall of graphene material (diameter ranges from 1-2 nm) [49-57].

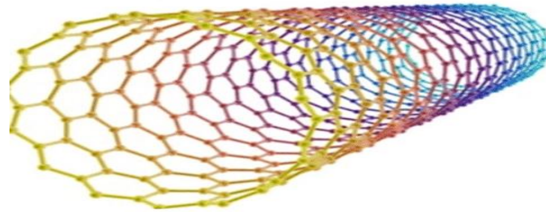


Figure 1.6 Single-wall carbon nanotube structure [56]

- Multiwall CNT (MWCNT) - with many concentric SWCNT-like graphene tubes (diameter ranges from 2-25nm) [58-60].

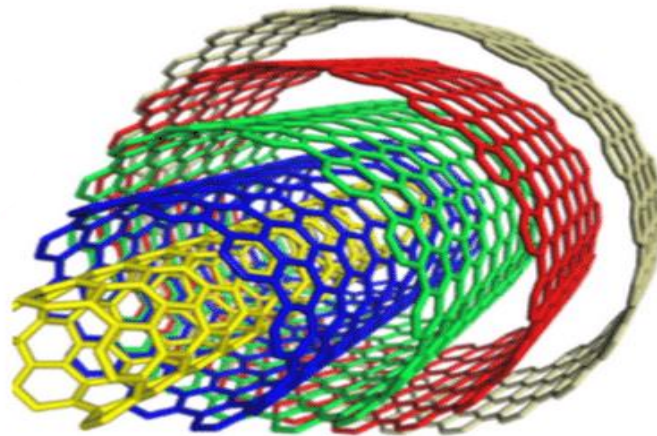


Figure 1.7 Multi-wall carbon nanotube structure [59]

- Double-wall CNT (DWCNT) is formed by rolling two graphene sheets with a common center in the shape of a hollow cylinder as shown in Figure 1.8.

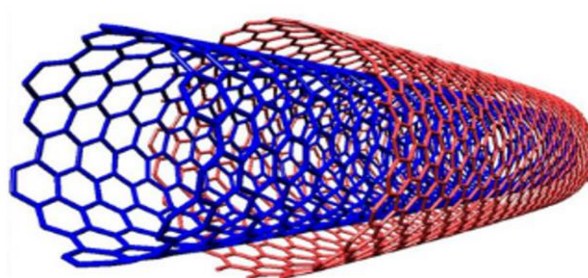


Figure 1.8 Double-wall carbon nanotube structure [76]

According to the values of the chiral index (n, m) represented in Figure 1.9, CNTs can be either armchair or zigzag type as shown in Figure 1.10 [61-66]. For interconnect applications in integrated circuits, metallic CNTs are the suitable choice [67-70].

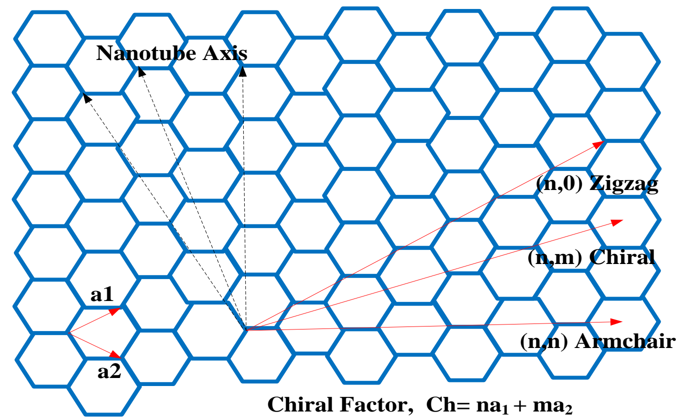


Figure 1.9 Chirality based on the direction of the nanotube axis [55]

- If n or m =0, then zigzag structure is formed.
- For the same value of chiral indices, i.e., n=m, the armchair structure is formed.

Chirality decides the conductivity of CNTs, whether they will have metallic (conducting) or semiconductor nature [71,72]. With 'i' as an integer, for n-m=3i, armchair structures will always be metallic and zigzag structures can be of metallic or semiconducting nature as represented in Figure 1.10.

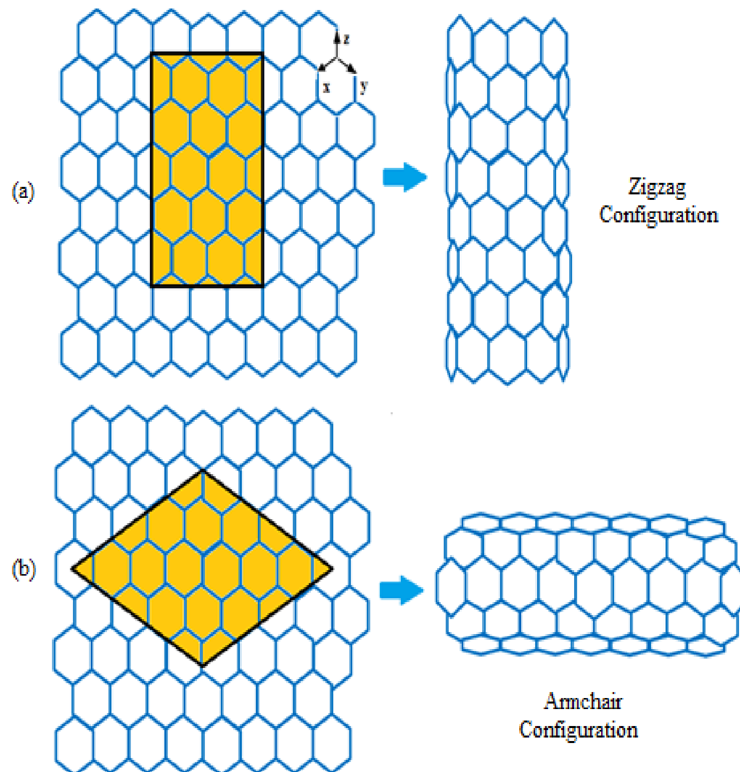


Figure 1.10 Configurations of CNT depending on chirality.
(a) Zigzag configuration (b) Armchair configuration

In SWCNT interconnect bundle, some CNTs are metallic while some are also semiconducting in nature (do not support current conduction) based on the chirality. Multi-walled CNTs are

metallic in electrical behavior [59,60]. Due to their larger diameter and easiness of fabrication, MWCNT bundles also provide satisfactory results as interconnect materials. SWCNT having a single shell of nanotube has the simplest structure with an electron mean free path of around 1 micron and thus, has good conductivity. However, due to the large resistance of isolated CNTs, they are packed in the bundle. CNTs are implanted in a parallel way to develop a bundle.

1.6 Aim of Thesis

Mixed structures are modeled by picking the best properties of constituent CNTs. Though a lot of study and research has been done on mixed bundled interconnects having SWCNTs and MWCNTs or structures with different diameters of MWCNTs [73-79]. With a long mean free path and good conductance, metallic SWCNTs are yet difficult to fabricate due to a lack of control of chirality. Double-wall CNT can easily outperform SWCNT by showing lesser values of parasitic resistances and capacitances. DWCNTs are comparatively easier to fabricate than SWCNTs, metallic in nature with two concentric shells and reduced resistivity can provide equally good conductivity as that of SWCNT; so more improvement can be attained by replacing SWCNTs with DWCNTs. With the upgradation in technology nodes, it is very important to keep in mind the concept of fringing capacitances, temperature, low power designs, and crosstalk [80-83]. Several related studies in the literature have also been done to determine the performance of MEMs (microelectromechanical systems) and NEMs (nanoelectromechanical systems) [84,85]. The performance of multi-wall and double-wall CNTs bundle structure is presented and explored in detail. It has been observed that these mixed models of carbon nanotubes can become a promising candidate for future interconnect applications for future beyond 32nm technology nodes than the isolated counterparts taking all related parameters into account.

These effects have also been considered for global interconnect lengths at nano-regime nodes in this thesis report. The propagation delay and PDP readings estimated from SPICE simulations of mixed CNT bundles are then correlated with the values of conventional materials like copper, SWCNTs, MWCNTs, and DWCNTs mentioned in the literature. The analytical expressions to evaluate the performance of MDCB interconnects are also presented. Later, it is evident from the results presented in this report that MDCB (multi and double-wall carbon nanotube bundle) interconnects undoubtedly show outstanding performance than isolated bundled carbon nanotube counterparts concerning delay and power-delay products. For desirable functioning and to keep output under controllable limits, the stability of circuits is determined. The stability of four MDCB structures is also determined in this report, and it

has been noticed that all structures show good stability response, thus making them appropriate candidates for interconnects.

1.7 Organization of Thesis

A detailed study of the topic is organized in the chapters listed below.

Chapter 1**'Introduction'** gives a glimpse of topics related to interconnect. It presents the need to study carbon nanotubes as interconnect material for VLSI circuits in detail and comprises basic interconnect models, categorization of interconnects depending on the length (local, intermediate, and global), need for repeaters, lumped and distributed modeling, classification of interconnects on the type of material (with their advantages and disadvantages) and issues in copper interconnect and types of CNTs (SWCNTs, MWCNTs, and DWCNTs).

Chapter 2 **'Literature Survey'** provides a quick review of topics like Interconnect models, problems to be addressed in interconnect models, copper interconnects and their problems, carbon nanotubes- single wall, multi-wall, double-wall and various mixed bundled CNTs (formed with different diameter MWCNTs or with SWCNTs and MWCNTs) and their performance analysis, the importance of temperature and crosstalk in the conduction of integrated circuits and stability analysis of interconnects. The problems in copper beyond 45 nm technology are studied in detail. The need for CNTs is highlighted. The excellent properties of carbon nanotubes are mentioned and articles demonstrating the performance of SWCNTs and MWCNTs better than copper are listed. The thermally aware models and various electron-phonon scatterings at high temperature and their impact on the conduction path of electrons are also indexed. The influence of crosstalk on long-coupled CNTs is also studied. Due to some gaps found in the literature, the objectives of the thesis are proposed.

Chapter 3 **'Circuit Analysis of Mixed CNTs'** presents a brief study on interconnect materials like copper, single-walled, multi-walled, and double-walled carbon nanotube bundles with their physical structures, electrical equivalent diagrams, and impedance equations at global interconnect length. Expressions for different kinds of resistance, inductance, and capacitance of CNTs are mentioned. Different mixed CNT bundles are proposed and developed by changing the position of MWCNTs of DWCNTs. The RLC parameters of different mixed bundled structures are determined. Performance and comparison of all these CNTs based on delay and PDP at 32 nm, 22 nm, and 16 nm technology nodes at different global lengths with copper are also demonstrated. It is shown that mixed CNTs can potentially oust copper and their counterparts like MWCNTs and DWCNTs as interconnect materials.

Chapter 4 **'Temperature Dependent Modeling of Mixed CNTs'** highlights thermally aware

proposed modeling of multi-wall and double-wall CNT bundles structures and analyzes the temperature-dependent performance of various MDCB interconnects at various global lengths. Different types of electron and phonon scatterings affecting the conduction path of electrons of SWCNTs, MWCNTs, and DWCNTs at a wide thermal range from 200 K to 500 K are determined. Temperature-dependent delay and PDP comparisons are made for all interconnect materials, and it can be concluded that the MDCB structure with MWCNTs at the outer edges and DWCNTs in the center of bundle performs the best than all other interconnect materials at nano-regime nodes (32nm, 22nm, and 16nm technology).

Chapter 5 **'Impact of Crosstalk and Stability in Mixed Bundle CNTs'** states that long interconnects in integrated circuits face capacitive and inductive couplings. Their performance is affected due to the presence of a closely laid interconnect line on the chip. Functional and dynamic crosstalk are determined to affect the performance of the circuit. The effect of crosstalk (increase in delay or change in functionality) on various MDCB structures is also studied in detail and it is observed that this effect can't be neglected while determining the performance of global interconnects at scaled nodes. The stability analysis with the help of expressions of rise time, peak overshoot voltage ($\%M_p$), transient response waveform, and Nyquist plots is performed on mixed CNT interconnects. It has been observed that MDCB structures gave good stability responses at all nanotechnology nodes.

Chapter 6 **'Comparative Analysis with Literature and Analytical Modeling of MDCB Structures'** presents mathematical modeling of mixed bundled CNT interconnects. The comparison is drawn between the other type of mixed CNT bundles formed with MWCNTs and SWCNTs with proposed MDCB structures formed with MWCNTs and DWCNTs. Analytical delay values are also obtained for MDCB structures. The expressions for the T_{90} delay are given and compared with the simulated data. The readings of simulation and analytical modeling lie in proximity with each other.

Chapter 7 **'Conclusion'** states that MDCB structures can outperform not just copper, but all other CNT materials and it is found that they can be used as interconnect material for future interconnect applications. The outcome of the thesis is presented with the future capacity of CNT interconnects.

2. LITERATURE SURVEY

This chapter provides a brief review based on literature to understand the topic of the thesis. It gives background information required to know and highlights the importance of related topics like various interconnect models, issues in copper interconnect, CNT interconnects, the need for mixed CNT bundles, the impact of temperature, crosstalk, and the stability of interconnects.

2.1 Interconnect Models

The study of delay models of various types of interconnects, scaling, need, and optimization of repeaters, power dissipation issues, and related parameters are as follows:

Saraswat and Mohammadi [12] presented the importance and effect of scaling dimensions with the compression in feature size and expansion in chip size. Further, its effect on the time delay of the circuit is also studied in detail with the help of analytical expressions. With the betterment in technology nodes and scaling, the delay of interconnects also becomes important and further this delay may dominate the net performance of the circuit. So, the delay of interconnects must be analyzed at nanotechnology nodes. Interconnect material should have low resistivity, be mechanically strong, have good conductance, and can withstand high temperatures and electromigration during operation.

Bakoglu and Meindl [14] stated that as device dimensions were reduced, the propagation delay of interconnects line played a very essential part in judging the electrical conduction of integrated circuits. With the decrease in cross-sections of interconnects, RC time delays increase significantly. For an ideal scaling factor 1/S, the output response time of short/local interconnects remains the same, but the problem arises for global interconnects as their delay shows an increase by $S^2S_c^2$, where S_c is the scaling parameter for chip size. The delays of aluminum, polysilicon lines, and $WSiO_2$ are compared. As a result, repeaters were introduced in long conductor lines by dividing long global interconnect lines into smaller equal sub-sections and helped in reducing the propagation delay over the line. Other different methods for improving delay like multilayer connections, properly selected and uniform-sized repeaters, and cascaded drivers are also analyzed which helps in optimizing the driving capability as shown in Figure 2.1. A multilayer connection helps in occupying less area and improves signal delay by using low-resistivity aluminum wires. The cascaded driver technique helps in improving the driving ability of capacitive load. Optimal-sized and optimal numbered repeaters

transform interconnect lines into distributed parameters efficiently and show a drastic decrease in propagation delay.

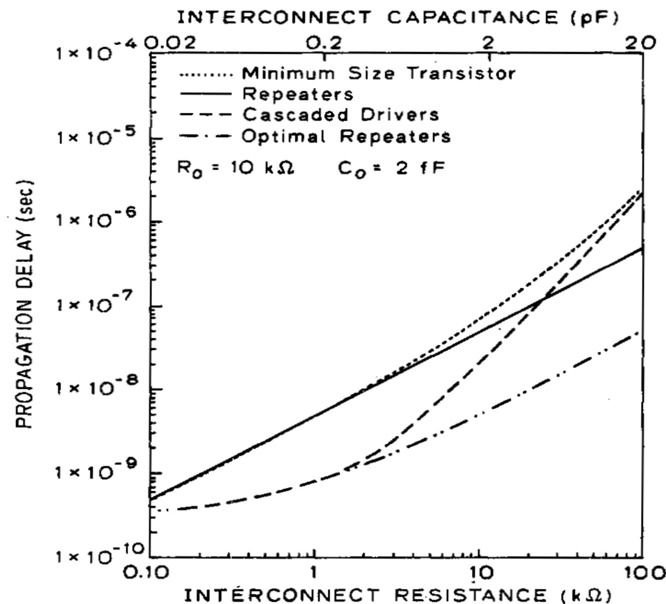


Figure 2.1 Propagation delay-based comparison of different interconnection techniques concerning values. of interconnect parasitic [14]

Sakurai [16] determined a formula for voltage slope and the transit time from waveforms of resistive-capacitive lines with boundary conditions. The future direction of delay of interconnects is also postulated. It has been stated that RC delay plays an imperative role in judging the execution of high-speed VLSI circuits. To minimize delays optimum linewidth is calculated. Also, the mathematical expressions for delay are given. The analytical graphs are accurate and are in close relation with the simulated results. It has been observed that the effect of capacitive coupling is indispensable, and it reduces errors in calculating signal delay.

Adler and Friedman [17] presented the α-power law model of CMOS inverter driving large RC load over global interconnect length. The distributed parameters are driven by the CMOS gate and all four regions of operation of CMOS need to be considered. The voltage waveform is studied in detail for all the regions of operations to determine the delay of the circuit accurately. Various analytical expressions are also presented to validate results. The optimum repeater technique outperforms all other techniques. There is a significant decrease in delay using uniform optimum-sized repeaters. The simulated SPICE values match very closely to the proposed analytical results and analytical readings show a maximum deviation of 15% with SPICE simulated results for different RC loads at global interconnect.

Chandel *et al.* [18] analyzed that with technology advancements, interconnect of global lengths had more propagation delay. It was not a good solution to drive with the help of a single buffer; instead, several buffers were introduced at regular intervals. The other issue was power dissipation due to long interconnects and large loads. For high-speed integrated circuits, both power and delay should be kept to a minimum. Repeaters can be made using minimum-sized, tapered, optimum-sized, or cascaded ways. Depending upon the application and compromising between delay and power and considering all the factors; optimum sized voltage scaled repeaters were inserted for high pace and low power interconnect applications.

Ismail and Friedman [21] stated that inductance also plays an important role in determining circuit delay at scaled technologies and higher frequencies. The delay is calculated for CMOS-driven *RC* and *RLC* circuits. With the increase in the value of inductance, the *LC* time constant dictates the *RC* time constant, and the delay of the line alters its behavior from quadratic behavior to linear. It has also been concluded that if the effect of inductance is ignored, it introduces 35% more delay in RC circuits. So, while estimating delay in repeater circuits, the inductance parameter cannot be neglected, and this percentage error also increases with the scaling of technology.

Banerjee and Mehrotra [22] stated that power dissipation was becoming an issue in scaled circuits. The leakage power because of sub-threshold and gate leakage was also increasing exponentially with the scaling of devices. The short-circuit power steps up further as the rise time of signal delays increases. Also, the dynamic power dissipation due to the increased number of devices, repeaters, and wires and their global interconnect lengths would increase. The chip temperature would also rise thereby degrading the reliability of the circuit. So, a power delay trade-off was faced. It is shown that with the optimum number of equally sized repeaters, there was a 25% reduction in delay as well as an 80% reduction in power.

Khursheed *et al.* [23] stated that the performance of on-chip copper interconnects wires is degraded due to the shrinkage of device dimensions beyond certain nodes. To provide high-speed circuitry, buffers are inserted in the circuit. The number of buffers needs to be optimum keeping the importance of the power parameter in mind. To settle the trade-off between power and speed, various techniques like variable diameter and multi-threshold voltage can be used. The performance comparison between copper and CNTs is determined at various lengths using proposed and existing buffer methods. As compared to existing buffer techniques, buffer

techniques using variable diameters saved dynamic power (89.96%), and leakage power (89%) and offered less delay (77.5%). Also as compared to the conventional buffer method, the buffering technique using multi-threshold methods saved dynamic power (99.94%), and leakage power (97.53%) but offers more delay. All simulations are shown using the SPICE tool at 32nm technology.

Liu *et al.* [24] presented the concept of adding an optimum number and optimally sized repeaters to reduce the propagation delay of MWCNTs which is much lesser than the copper counterpart. It was required to add repeaters at intermediate and global interconnect levels for proper message propagation from the input node to the output node with the least delay. The effect of inductance and contact resistance are also included. For a specified delay MWCNTs require a lower number of repeaters than copper, thereby it cuts down the area and power dissipation at the same time.

2.2 Copper and CNT as Interconnects

Research articles related to copper and carbon nanotubes as interconnect material for scaled technology nodes have been listed below which concludes that CNTs perform better than copper.

2.2.1 Problems Faced by Copper Interconnect.

Copper interconnect faces several issues like breakthroughs in resistivity, electromigration, surface scattering, and grain boundary scattering beyond 45 nm technology nodes at global levels of interconnect.

Li *et al.* [35] stated that copper interconnects are fabricated by the damascene technique for interconnect applications in integrated circuits. Due to better conductivity, copper has replaced its predecessor aluminium successfully by giving improvised results based on power and delay of the circuit. But copper too faces some serious reliability issues like impurity defects, surface scattering, grain boundary scattering, increased resistivity, and electromigration beyond the 45nm technology node. It contributes to devise failure in terms of breakdown, delay, thermal and packaging ability. These fatal issues demand special attention to improve the working of interconnect in the operating environment.

Steinhogl *et al.* [39] studied and analysed the resistivity of copper for 100 nm technology and beyond. The impact of variation in width, height, and aspect ratios are determined. Surface

scattering and grain boundary scatterings in copper are observed beyond 100 nm nodes as the technology is scaled down. Due to the mentioned scattering processes, it leads to an upsurge in the resistivity of material and electromigration. The temperature-sensitive resistance of copper is employed in circuits to determine their performance beyond 100 nm technology. The performance of copper wires degrades concerning the delay of the circuit.

Maffucci and Miano [42] addressed the issues of interconnects with the scaling of devices. The electrical performance of metallic carbon nanotubes is simulated and compared with copper with the help of a transmission line model. Due to problems faced by copper, the value of attained current density, and good thermal and mechanical strength by CNTs help them take their place in the VLSI market. The resistance of a single CNT is too huge, so a stack of CNTs is packed in a bundle to scale down the net value of resistance. The physical model and mathematical equations are present for CNTs to understand their structure and behavior. At the local level, the performance of CNTs is equal to that of copper and it can only give better results if all CNTs are densely packed and metallic. However, at the intermediate and global level, due to longer MFP in CNTs than copper, CNTs achieve superior results than copper in terms of impedances and delays.

Xu *et al.* [43] observed that with increased scaling and complex circuitry, the circuits also need to maintain high speed and low power dissipation requirements. It is seen that with technological upgradations, copper interconnects reach their maximum current carrying limit, beyond these limits at very deep sub-micron technologies, the resistivity and reliability of the circuit are suffered. So, carbon nanotubes with good electrical, and thermal conductivities and process compatibilities are proposed to provide an excellent substitute for copper.

2.2.2 Carbon Nanotube as Interconnect

The excellent conductivity, high current density, and thermal and mechanical strength of CNTs have been extensively explored and suggested as future interconnects material. Work related to SWCNTs, MWCNTs, and DWCNTs is listed below.

Burke [46] presented carbon nanotubes as nano-transmission lines with distributed parameters like resistances, (kinetic and magnetic) inductance, (and quantum and electrostatic) capacitances to determine their performance at gigahertz frequencies using Luttinger Liquid theory. The electrical circuit models of SWCNTs and MWCNTs are explained in detail. The

experimental formulations are in close relation with mathematical expressions. The dynamic circuit properties of SWCNTs are discussed in detail. For MWCNT interconnects all shells contribute to the conduction. CNTs due to extraordinary conducting properties, and good thermal and mechanical ability have the potential to replace all existing interconnect materials.

Srivastava *et al.* [49] presented the application of SWCNTs and MWCNTs with low resistance contacts for next-generation technology nodes at 22 nm nodes using one-dimensional fluid theory. The structures, their electrical equivalents, and impedance equations are explained. Mathematical modeling and simulations are performed for determining delay and power at local and global levels of interconnects. The performance of CNTs is improved by decreasing the resistance and increasing the number of tubes in a bundle. The resistance of copper increases more sharply than CNTs with the increment in the length of interconnect. With superior transmission proficiency, reduced losses, high bandwidth, fewer delays and lower power dissipation, metallic carbon nanotubes with more conducting channels per shell can replace copper as VLSI interconnects.

Banerjee *et al.* [52] suggested that after the discovery of nanotubes with excellent conducting, electrical, mechanical, and thermal properties as mentioned in Table 2.1 by Ijima in 1991, they had been suggested for their use as interconnects in electronic circuits. CNTs are formed with a sheet of graphite arched up in the form of a hollow cylinder. Since copper interconnect was badly affected by issues like electromigration and grain boundary effects and other reliability issues, their resistivity increased at high temperatures and scaled technology nodes and in that case, metallic carbon nanotubes provided a suitable alternative to copper. Dense CNT bundles with low contact resistance attain improvised results at long lengths of interconnect lines.

Table 2.1 Comparison of different properties of CNT and Copper

Properties	CNT	Copper
Mean free path (nm) at room temperature	>1000	40
Maximum current density (A/cm^2)	>1x10^{10}	~1x10^6
Thermal conductivity (W/mk)	5800	385

- **Single-wall carbon nanotube as Interconnect**

Articles presenting the interconnect performance of SWCNT based interconnect are indexed below.

McEuen *et al.* [54] stated that both metallic and semi-conducting graphitic nanotubes are excellent members for VLSI applications. By good conductance and high current densities metallic CNTs or zero band gap semiconductors have beaten the best existing metals. On the other hand, semi-conducting CNTs possess good mobility and transconductance values. Both types of CNTs can withstand high mechanical and thermal conditions. For interconnect applications, metallic CNTs having longer MFP are an appropriate choice. During the manufacturing of CNTs, the diameter needs to be controlled properly as this helps in determining the chirality and nature of CNTs.

CNTs are manufactured using CVD (chemical vapor deposition) technique at an extremely elevated temperature of around 900^0C in the presence of catalysts. To eliminate elevated temperatures, the other technique employs the deposition of tubes on the substrate. But in this method, chirality cannot be controlled. Though there is no accurate method yet developed, to control the chirality of SWCNTs, research is going on other techniques as well like wet processing, deposition using electric fields, etc. SWCNTs are good alternatives to copper at intermediate and global levels. Studies are going on to discover a method that would control the metallic nature and position and diameter of nanotubes during manufacturing.

Naeemi and Meindl *et al.* [55] presented the performance of interconnect using physical circuit models. Different expressions to determine conducting channels, resistances, inductances, and capacitances of CNTs and copper is given at local and global levels. The RLC of both copper and CNTs rises with the increase in a stretch of interconnects. The other process parameters like the number of metallic CNTs in a bundle, diameter, temperature, distance between nanotubes, contact resistance, and technology parameters play relevant factors in deciding the net electrical conduct of interconnect.

For short lengths, CNTs have a large value of resistances because of quantum and contact resistances. So, copper can be successfully used as interconnect material at the local level. However, as the length increases, and with technology scaling, copper faces severe problems like grain boundary, surface scattering, and electromigration. So, SWCNTs can replace copper if densely packed and chirality is controlled or large-diameter MWCNTs can easily replace copper at the global level.

Srivastava *et al.* [56] demonstrated the performance of single-walled CNT interconnects in nanocircuits. The physical and electrical model of SWCNT and its associated parasitic (resistance, inductance, and capacitance) are studied thoroughly. The performance of SWCNT

is then compared with copper interconnect. Due to surface scattering and electromigration concerns of copper beyond 40 nm technology nodes, SWCNTs give better results than copper.

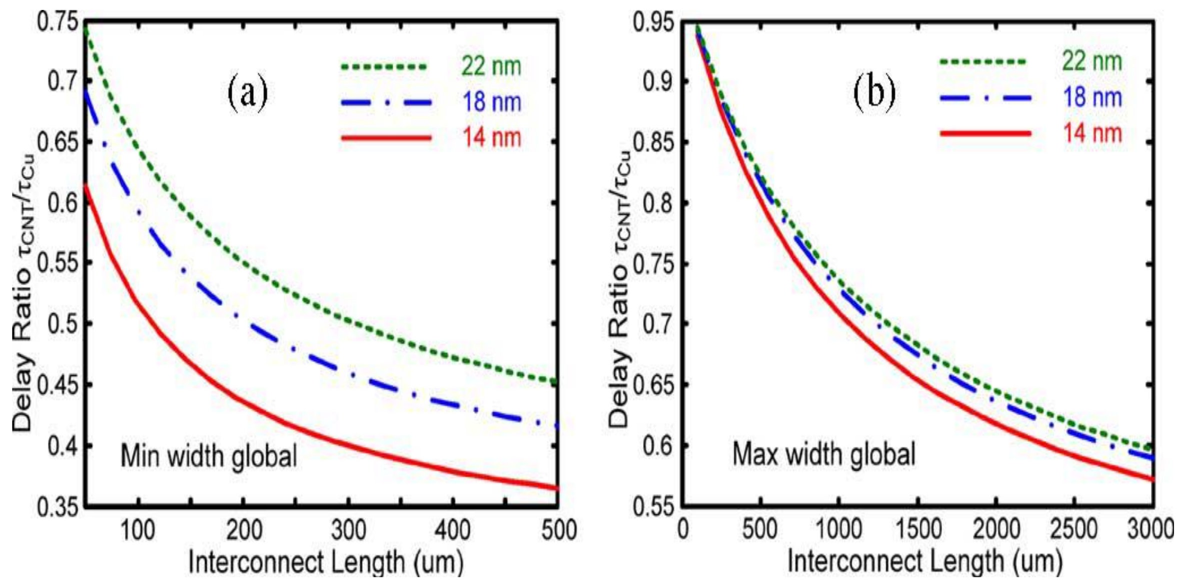


Figure 2.2 Normalized delay (Γ_{CNT}/Γ_{Cu}) at (a) intermediate length (b) global length of interconnect [56]

The results clearly show that there is a 30%-40% decrease in delay while using SWCNTs than copper at the global level as shown in Figure 2.2. Also, considerate power savings is achieved by employing dense SWCNTs at 22nm (4 times) and at 14nm (8 times) technology node. SWCNTs provide an excellent substitute as interconnect in high-paced VLSI circuits to copper at nanotechnology nodes.

Rai and Sarkar [57] presented the impact of the diameter of a single-walled nanotube on the delay and power of the circuit. The diameter of a carbon nanotube is a crucial parameter that plays an extremely critical role in deciding the values of its related electrical parameters like the resistance of nanotubes, inductance, and capacitance of nanotubes.

Also, with the preferment of technology, the resistance of both copper and SWCNT increases, and this increase is more for copper than SWCNT due to grain boundary and surface scatterings. It has been observed that the resistance and inductance of nanotube increases with the increment in diameter of the nanotube which may increase the delay of the circuit. However, the capacitance of the nanotube shows an inverse relationship with the diameter as shown in Figure. For low-power applications, large-diameter SWCNTs can be used. So, to overcome this trade-off between delay and power as demonstrated in Figure 2.3, an optimum diameter of SWCNT must be chosen.

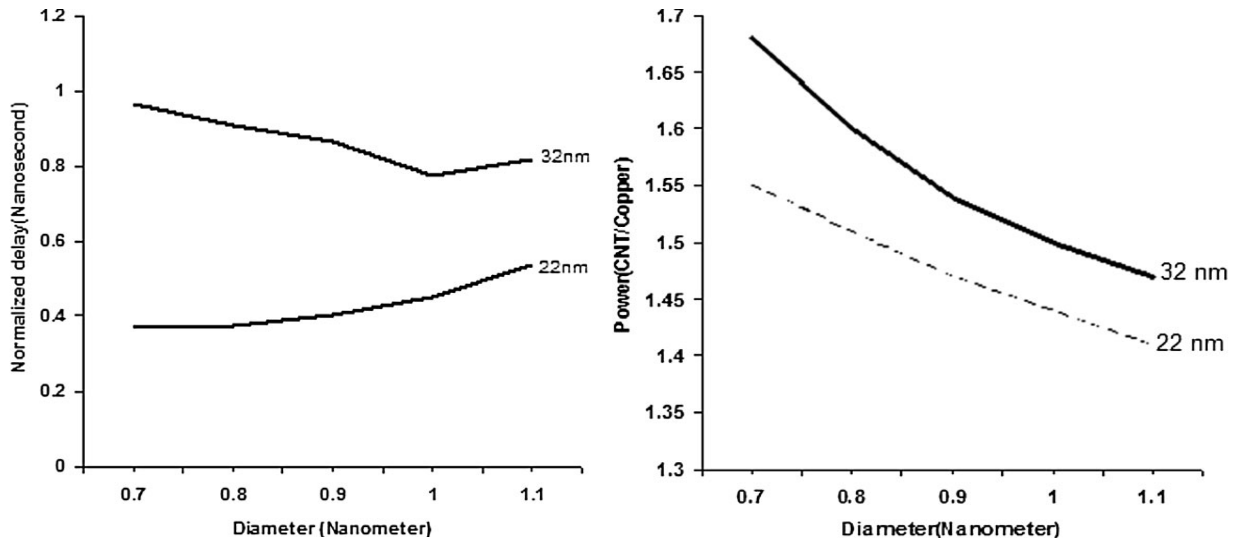


Figure 2.3 Variation in normalized delay and power dissipation with variation in diameter at 32 nm and 22 nm technology node [57]

Liu *et al.* [58] analyzed equivalent electrical circuits of SWCNTs. It has been seen that those thermal issues play an extensive role in deciding the electrical conduction of ICs. Various parameters like crosstalk event, length of interconnect, the diameter of the nanotube, metallic ratio, technology node, and temperature help in deciding the performance of the circuit. The crosstalk peak voltage and peak width of SWCNT reduce by ~23% and ~8% respectively to that of copper line. For larger diameters, the metallic proportion in SWCNT increases. The impact of crosstalk shows an increase with the increment in interconnect length. Also, the pulse width of the crosstalk is more vulnerable to the temperature for a longer length. On the contrary, the pulse voltage of crosstalk is more prone to temperature effects for shorter interconnect lengths.

- **Multi-wall carbon nanotube as Interconnect**

Due to ease in fabrication and high current carrying capability, multi-shell CNTs have gained lots of attention. Below listed work below presents the study of MWCNT interconnects.

Li *et al.* [59] presented the detailed performance of multi-walled CNT and its comparison is made with copper and SWCNT. With larger diameters and different conducting shells, MWCNTs have a complex structure that requires deep knowledge of each shell parameter and couplings between these shells. The equivalent model of MWCNT and its parametric equations are well presented. MWCNTs have larger diameters and longer MFPs.

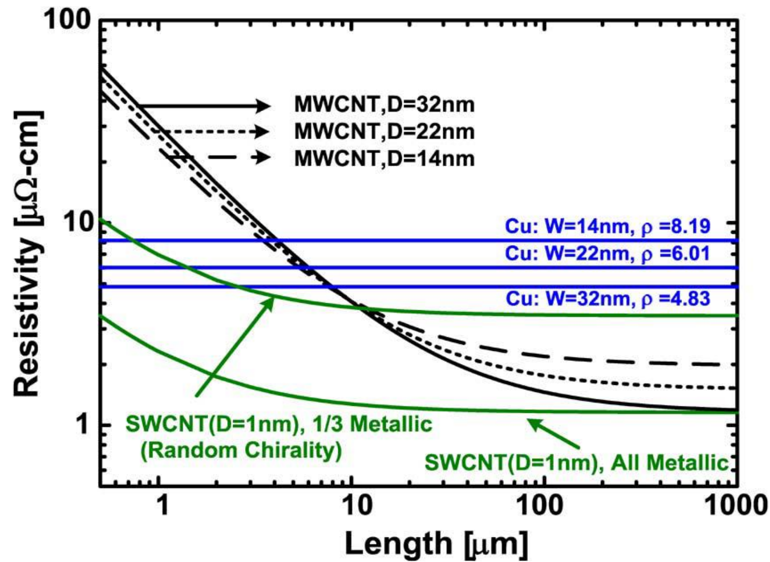


Figure 2.4 Resistivity comparison of copper, SWCNT, and MWCNT over length varied from 1µm to 1000µm at 32 nm tech, 22 nm tech, and 14 nm tech. node [59]

At the local level, MWCNTs show a larger value of delay than copper by 1%-6% because of the presence of quantum and contact resistances in it. For semi-global and global levels, large-diameter MWCNTs show lesser delay and power dissipation than copper counterparts and these results get better with technology advancements. At 1000µm the delay of MWCNT is just 15% that of copper interconnect. For interconnect applications SWCNTs must take care of the chirality index (metallic nature) and should be densely populated in the bundle. MWCNTs are easy to fabricate and are metallic in nature. For global lengths, the electrostatic capacitance value of MWCNT is lesser than SWCNT. At global lengths, MWCNTs have less value of delay than SWCNTs too as can be viewed in Figure 2.4. Large-diameter MWCNT shows promising results as interconnect material for local, intermediate, and global levels at nanometre technology nodes.

D'Amore *et al.* [62] proposed two models to check the electrical performance of CNTs at 22 nm and 14 nm technology nodes. CNTs have captured the interest of the VLSI market due to their high current density and thermal conductivity, and good mechanical, and thermal strength. MTL (multi-conductor transmission line) and MESC (multi-equivalent single conductor) are also presented. The transient response is determined for both interconnects and is in good agreement with simulated results. The MESC model is extremely easy, and simple and saves time in determining a 50%-time delay. Also, the MESC model gives less % error than the MTL model for calculating the delay-based performance of CNT interconnects. Due to the large value of capacitance in SWCNTs, MWCNTs give better results than SWCNTs at global lengths.

Gholipur and Masoumi [65] proposed multi-walled carbon nanotubes for VLSI interconnect material. Physical and circuit modeling along with simulation and analytical expressions are mentioned to decide and compare the performance of MWCNTs and copper. The simulated results are in good accordance with analytical results. MWCNTs possess high current densities and good mechanical, and thermal strength. Copper suffers from grain boundary scattering and electromigration issues beyond the 40 nm technology node. Along the length of interconnect, and with the scaling of dimensions at advanced technology nodes, MWCNTs exhibit a lower value of delay than copper. Analytical expressions also reveal that MWCNTs require a lesser number of buffers than copper.

Singh and Raj [66] analysed the temperature-dependent electrical performance of multi-walled carbon nanotubes, single-walled carbon nanotubes, and copper. Temperature-sensitive electrical models and parasitic equations of MWCNTs are presented. The detailed comparative analysis based on power, signal delay, and PDP is done between MWCNTs, SWCNTs, and copper at 32, 22, and 16nm technology nodes for the wide temperature range varying from 200-450K. The delay of copper rises drastically due to issues like surface scattering and increased resistivity at scaled technology nodes. Large-diameter MWCNTs have lesser values of capacitance than SWCNTs. It is concluded from the results that MWCNTs show the least value of delay, power, and PDP than copper and SWCNT at all technology nodes for a 1mm global interconnect length and prove them the most suitable material for interconnect applications.

- **Double-wall carbon nanotube as Interconnect**

With two concentric graphene sheets coiled in the shape of a cylinder, these double-wall carbon nanotubes offer reduced resistance and thus better conductance than SWCNTs. Research papers analyzing the performance of DWCNTs are mentioned below.

Pu *et al.* [76] proposed some modifications in equivalent electrical models of SWCNTs and DWCNTs. The effect of capacitive couplings between the adjacent nanotubes was considered. The performance of DWCNTs is then compared with copper and SWCNTs (with metallic ratios s 33% and 100%) at the global level and the simulated delay results can be viewed in Figure 2.5. Undoubtedly, both CNTs exhibit improved results than copper concerning the signal delay.

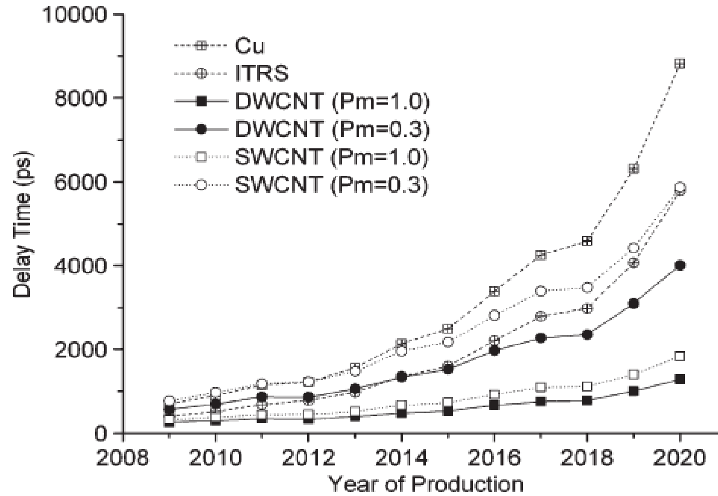


Figure 2.5 Comparison of delay time versus years between copper, SWCNT, and DWCNT interconnect [76]

Also, it is seen that DWCNTs offer lesser delay and capacitive coupling than SWCNTs. Due to such improved results, it has been confirmed that DWCNT bundles can replace SWCNTs and has a bright future in the field of VLSI interconnects.

Kordrostami *et al.* [77] proposed DWCNTs as an interconnect material for integrated circuits. The physical structure has two concentric shells of graphene, and the impedance equations are well presented. Good ohmic contacts are provided at both the ends of nanotube. The time domain response and dynamic behavior of DWCNTs are studied. Experimental results are validated with the simulated data. With two conducting shells and reduced resistance, DWCNTs show a lesser value of resistance and delay than SWCNTs. With faster operations and high current value, DWCNTs became an ideal interconnect material for large-scale integrated chips.

Yin *et al.* [78] investigated the performance of metallic carbon nanotubes. The circuit model and impedance equations of DWCNT are expressed in detail. The equivalent models and performance of SWCNTs and DWCNTs are determined concerning crosstalk-induced signal propagation delay and then it is also compared with copper. CNTs have a long conduction path (around 40 nm) and lower resistivity than copper. The delay of CNT is bigger than copper at the local level but at the semi-global and global levels, the delay of CNT is much smaller than copper. The effect of self-heating and crosstalk including inductive and capacitive coupling are also included. For longer lengths of interconnect, DWCNTs show the least value of delay than copper and even SWCNTs. This special case of CNTs i.e., DWCNTs formed with two shells becomes a potential interconnect material for semiconductor circuits.

Loumi *et al.* [79] analyzed the performance of various carbon nanotube bundles like SWCNTs and DWCNTs. The number of nanotubes available in the interconnect bundle plays a significant role in deciding the amplitude and speed performance of the circuit. It has been observed that as the count of nanotubes in the bunch increases, it increases the electrical conductivity of the bundle and by decreasing the resistance, the signal delay of the circuit improves. On the contrary, increasing the count of nanotubes in the bundle enhances coupling with adjacent nanotubes. With the scaling, results show that for all the cases beyond the 45 nm technology node, CNTs give improvised results than copper and can be successfully implanted as interconnects in miniaturized circuits.

2.3 Effect of Temperature on Interconnects

Temperature variations play a very critical role in determining the electrical conduction of interconnects based on signal delay and power dissipation by affecting the MFP of electrons. Several electron and phonon scattering mechanisms are observed at high temperatures and can also introduce surface roughness and grain boundary defects in copper and graphitic-based CNT interconnects [86-97]. Below listed research papers have analyzed the performance of interconnects based on thermally aware models.

Park *et al.* [86] addressed different electron-phonon scattering phenomena for CNTs. The effective mean free paths are determined for low and high-temperature ranges. The results in the article show that the scattering length at very high voltage is reduced to 100x than the scattering length at low voltage. Acoustic phonon scattering plays a major role at low voltage while optical phonon scattering decides the value of MFP of electrons at high voltages. Different case studies for varying temperatures are observed for experiments and are validated with the proposed model.

Pop *et al.* [87] considered the impact of temperature and different electron-phonon scattering mechanisms in detail for metallic SWCNTs over a wide temperature range from 100-450K and different biasing conditions. The electro-thermal model represented plays an indispensable role in high current-carrying nanotubes as interconnects. The model has also been validated experimentally. It has been observed that as temperature increases, the resistance also shows an increment because of the decrease in effective MFP of conducting electrons of SWCNTs as shown in Figure 2.6.

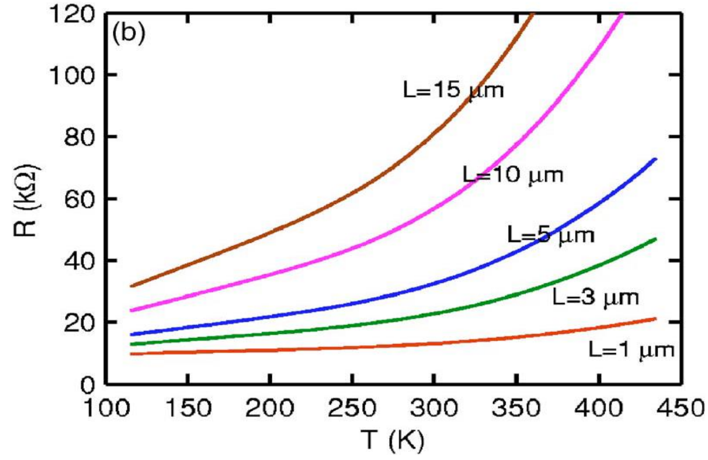


Figure 2.6 Temperature-dependent resistance of SWCNT at varying interconnect lengths [87]

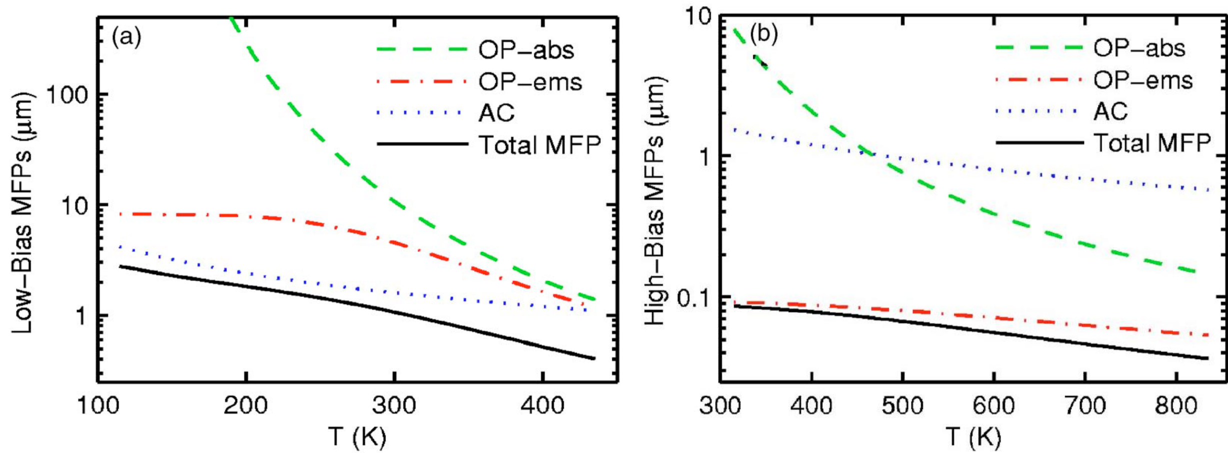


Figure 2.7 Temperature-dependent mean free paths of SWCNT at different bias conditions [87]

For low and high-bias regions, different types of temperature-dependent scattering like acoustic, optical absorption, and optical emission play vital roles in deciding effective value of the mean free path of electrons as shown in Figure 2.7. The results depict that effect of temperature must be included for judging performance of interconnects for future applications.

Naeemi *et al.* [90] analysed temperature-dependent scattering mechanisms for both SWCNTs and MWCNTs. It has been observed that the thermal coefficient of resistance is positive for SWCNTs and is in direct relationship with length too. For larger diameter (~6 nm) MWCNTs, as the conducting channels increase with the increase in temperature, it decreases the impact of the increase of the electron-phonon scattering phenomenon. In small-diameter MWCNTs because of the dictation of quantum resistance, resistance decreases with the temperature rise. However, for long lengths, resistance again upsurges with the temperature due to shortened MFP of electrons. CNTs can be used as VLSI interconnects material for technology nodes beyond 22nm.

Hosseini *et al.* [92] proposed a thermally aware model to decide the performance of graphitic-based interconnects like SWCNTs and MWCNTs. Temperature and different scatterings-dependent impedance expressions for a single shell of the nanotube are also presented and explained in detail and are compared with experimental data. Temperature variations play a very important role in deciding the performance of interconnects. It takes both the effect of self-heating and heat conduction phenomenon into consideration to determine the effective mean free path of the conducting particles of nanotubes. The results obtained give 5x reductions in delay for metallic SWCNTs (for 27-127^{0}C temperature range) at the local level and prove them as a good alternative to classic copper interconnects beyond the 22nm node. By considering the thermally aware model in determining the signal delay, SWCNT proves itself an appropriate nominee for interconnect applications.

Chiariello *et al.* [94] presented the role of size and temperature in determining the performance of interconnects at nano-scaled technology nodes. Temperature-dependent simulation-based results are compared for copper and single-wall graphitic nano interconnects. The electrical resistance including the impact of temperature and cross-sectional area of copper and SWCNT is determined and compared. For both copper and CNT, the resistance increases with the increment in temperature, therefore introducing unwanted delay and degrading the circuit performance. Beyond the 22nm node, SWCNTs have less value of delay and can easily replace copper as interconnects.

Wen Chao Chen *et al.* [96] reflected the impact of self-heating, thermal voltage, power handling capability, temperature-dependent delay, and transient performance of metallic CNT arrays. The role of temperature is observed at low and high voltages, and it is concluded that for local interconnects at high voltages, the effect of self-heating needs to be taken care of while examining crosstalk-induced noise and signal delay. Moreover, the power handling ability and the breakdown also need to be handled. Beyond 300K, the heat generated due to scattering is primarily decided by forces like acoustic electron scattering, optical phonon emission scattering, and optical absorption scattering.

Gautreau *et al.* [97] stated that the scattering increases with the increase in temperature. The possibility of emission rates is more than absorption scattering rates at higher temperatures. It results in the transfer of energy to the lattice, thereby also increasing joule-heating with temperature. The hot phonons contribute to joule-heating only at 300K as a function of the

electric field. At higher temperature ranges, different non-equilibrium phonons decide the conduction of electrons. The acoustic, optical emission scattering, and optical phonon absorption scatterings are observed. Also, the non-linear behavior of the scattering of phonons is observed at higher temperatures. So, it is advisable to employ cooling mechanisms for devices needed to operate at high temperatures.

2.4 Mixed CNT Bundle as Interconnect

Various types of mixed carbon nanotube bundle interconnects are proposed in the literature. These mixed CNTs have shown better performance concerning delay, power, PDP, crosstalk, etc. than their counterparts. Mixed CNT bundles can become promising candidates for the VLSI industry at future nodes.

Majumder *et al.* [98] studied the application of mixed CNTs as interconnect for large-density and high-speed circuits. Varieties of mixed CNT bundle structures are developed by altering the locations of SWCNTs and MWCNTs. The count of CNTs in a bundle is examined which helps to determine the net associated resistance, inductance, and capacitance of the bundle. The distributed parameter technique is employed with repeaters at a global length to evaluate delay and crosstalk (in-phase and out-phase) in the circuit. Analytical results are also shown in good conformation with simulated results at lengths varying from 100µm to 1000µm. The structure with MWCNTs at the edges provides the least coupling with neighboring nanotubes. The structure with MWCNTs along the sides and SWCNTs in the center gives less delay with and without crosstalk than other mixed bundle structures. Some structures of mixed CNT bundles also tend to give better responses than SWCNT and MWCNT counterparts.

Subash and Chowdhury [99] stated that due to the increase in the resistivity of copper, metallic CNTs have proved to be an excellent alternative as interconnect at nanotechnology nodes. When a mixed bundle is formed, the combination of SWCNTs and MWCNTs yields the best results by adding the best properties of the two. The length of graphitic nanotubes and the metallic proportion of nanotubes highly influence the performance of CNTs. The circuit and electrical parameters of the single, bundle, and mixed CNTs are explained with the help of equations. The analytical results mentioned are in good relationship with the simulated data. MWCNTs which are less conductive than SWCNTs can be used at the four sides of the bundle to reduce the effect of capacitance coupling and SWCNTs are the main source of conduction

in the bundle. The results show that mixed CNT bundles can become the future candidate for VLSI interconnects.

Sathyakam and Mallick [100] stated that carbon nanotubes due to their high current densities at elevated temperatures have become an obvious choice over copper as interconnect material for integrated circuits. The modeling of electrical equivalent circuits of SWCNTs and MWCNTs and copper is explained. Transient analysis simulation is performed for lengths varying from 1 μm to 1000 μm. A mixed CNT bundle is developed with large-diameter MWCNTs and SWCNTs. Due to the increased densities of nanotubes and metallic ratios, the conductance and immunity to crosstalk of mixed bundles are increased significantly. It is concluded that if the fabrication of mixed CNT bundles is done precisely, they can perform better than existing materials.

Majumder *et al.* [101] presented mixed CNT bundles to determine their performance in high-density circuits. The mixed CNT bundles comprise randomly distributed SWCNTs and MWCNTs with different diameters. The distributed transmission line modeling with a CMOS inverter as the driver is employed to find the delay of mixed, SWCNT, and MWCNT bundles.

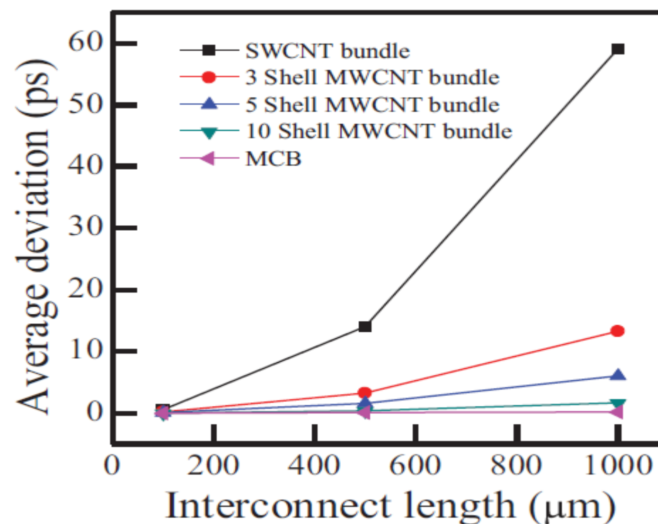


Figure 2.8 Delay comparison of SWCNT, MWCNT, and Mixed bundle interconnect [101]

Various parameters like metallic ratio, contact resistance, bundle area, and temperature and their effect on the performance of CNTs are also examined. Due to uncontrollability during fabrication, the change in metallic ratio impacts the count of channels in nanotubes. By varying the contact resistance from 0 to 100 of kilo Ω, the densely packed structure of mixed CNT bundle performs better than single and multi-walled CNTs. With larger height, width, and bundle area, the resistance and inductance of the bundle decrease by increasing the count of

CNTs in a bundle. The MFP of CNTs reduces with the increase in temperature. The temperature-dependent results show that mixed CNT bundle interconnects have lesser delay than SWCNT and MWCNT counterparts as shown in Figure 2.8.

Kumbhare *et al.* [102] presented crosstalk dependent performance of densely packed mixed carbon nanotube bundle interconnects. Two classes of structures are presented, one having spatially arranged CNTs and the other structure having randomly distributed CNTs. The distributed parameters are determined, and the transient analysis is performed using SPICE simulations. Randomly distributed mixed bundles are easier to fabricate than spatially arranged ones. A mixed CNT bundle with randomly distributed CNT shows better results than arranged mixed CNT bundle in terms of coupling effects. Results show that mixed CNT bundles with randomly distributed CNTs exhibit significantly less delay and power dissipation than spatially arranged mixed CNT bundles at global levels and can be used for high-speed chips.

Sandha and Thakur [103] proposed a mixed CNT bundle structure in which SWCNTs are inserted in an MWCNT interconnect. By inserting SWCNTs in the dead space around MWCNTs in a bunch, it increases the density of graphitic nanotubes and the net resistance and inductance of the bundle decrease. MTL model with CMOS technology is used to examine the electrical conductance of mixed CNT bundle interconnect concerning delay and PDP (power-delay product) at global length. The response of the circuit is determined based on delay for mixed and MWCNT bundle interconnects at 32 nm, 22 nm, and 16 nm technology nodes. By introducing SWCNTs and increasing the conductivity of the bundle, it is observed that this mixed carbon nanotube bundle interconnect attains less value of delay, power, and PDP than MWCNT for lengths varied from 100 µm to 2500 µm and can be employed in future ICs.

2.5 Crosstalk and Stability of CNT Interconnects

- **Crosstalk Analysis of Interconnects**

Global interconnects face capacitive and inductive couplings with adjacent lines which affect their performance on integrated ICs. The below-mentioned research papers include the impact and significance of crosstalk in the performance of interconnection wires [104-115].

Sathyakam *et al.* [104] Proposed a new triangular-shaped geometry for CNT bundles. The paper presents the ESC model of CNTs to determine crosstalk and delay. The spice simulated results show that triangle bundles suffer 29% less capacitive coupling as compared to

conventional square-packed CNT bundles. This capacitive coupling affects the crosstalk of adjacent interconnect lines, and it also increases as the count of lines on the chip increases. The author has proposed that these triangular-packed CNT bundles can replace conventional squarely packed bundles by offering 30% less crosstalk delay. So, triangular-packed CNT bundles can also be used as VLSI interconnect material.

Kaushik *et al.* [105] presented the role of driver width and line resistance on crosstalk coupled interconnects. To increase the driving capability, generally, driver width is increased, and resistance is decreased, but this lowers the performance of the circuit by increasing the crosstalk. The crosstalk noise reduces as the resistance increases since high resistance suppresses the unwanted signals and vice-versa. Also, as the width of the driver transistor increases, the crosstalk effect is enhanced. Nanotubes are highly affected by inductive and capacitive couplings of the adjacent tubes which in turn degrade their performance. So, crosstalk plays a very indispensable role in evaluating the performance of global interconnects.

Rossi *et al.* [106] presented CNTs for interconnect applications at very deep sub-micron technologies. Due to excellent conducting properties, CNTs have replaced all existing interconnect materials. The effect of capacitive and inductive couplings in parallel lying SWCNTs and MWCNTs in a bunch is examined in detail with the support of diagrams. Different cases of dynamic and functional crosstalk switching are explored in detail. Among MWCNT and SWCNT double line architectures, MWCNT performs worse than SWCNT due to the working of complicated shell structures, lesser noise margins, more delay, and more power consumption. Double-wall nanotube bus architectures have also been proposed. Results reveal reductions in crosstalk-induced delay (59%) and crosstalk noise (81%) using three-line DWCNT bus architecture than MWCNT and SWCNT bus structures.

Pu *et al.* [108] showed the role of crosstalk in SWCNT and DWCNT bundle interconnects. Equivalent electrical models incorporating the impact of inductive and capacitive couplings are used to determine and compare the time-based performance of SWCNT, DWCNT, and copper. Both SWCNT and DWCN show better results than copper in terms of crosstalk-induced glitches. It is seen that the value of crosstalk-induced time delay for DWCNT is lesser than SWCNTs at different lengths and technology nodes. DWCNT provides a good replacement to single-wall graphitic nanotubes as interconnects in high-speed integrated circuits at semi-global and global lengths.

Kaushik *et al.* [110] stated that though repeaters are used to decrease delays for long interconnect lines, they can also be efficiently used to decrease the crosstalk effect for coupled lines and proposed a new PDCP (Power Delay Crosstalk Product) parameter as a figure of merit parameter to determine the performance of the circuit.

PDCP=Power Diss. * Avg. 90% Prop. Delay *Normalized Crosstalk (2.1)

This PDCP parameter proves itself as the best parameter as compared to minimum delay and minimum PDP to determine the count of repeaters for long interconnect.

Das and Rahaman [112] presented the effect of crosstalk on device-related parameters i.e., gate oxide reliability. The equivalent models and impedance expressions of SWCNT and MWCNT are presented. To study the impact of crosstalk, it is assumed that nanotubes are lying adjacent to each other and affect each other's performance. Various cases of crosstalk like overshoot and undershoot have been reported for different lengths and technologies. Its net impact on the failure in terms of time is also determined. The crosstalk-based simulated results of CNTs are compared with copper. The results in the journal show that the crosstalk-induced delay of CNT based interconnect is less than copper. CNTs become an obvious choice as VLSI interconnects for future generations. It has also been reported that the crosstalk of copper shows an increase with length, while it remains constant in the case of CNTs. Sparsely populated SWCNTs with a minimum value of resistance don't have much influence on gate-oxide reliability because it is less affected by crosstalk-induced issues than copper and MWCNTs.

Majumder *et al.* [113] presented a crosstalk-affected performance in terms of the propagation delay of multi-wall and single-wall CNT bundles at the global length of interconnect. Interconnects are modeled using equivalent electrical parameters to determine delay. It is very important to address crosstalk issues in MWCNTs and SWCNTs because it depends on several factors like inductive and capacitive couplings, and the value of voltage transitions in adjacent lines. Dynamic crosstalk is noticed when nearby line switches simultaneously (in-phase or out-phase) thus inducing dynamic crosstalk-induced delay. Comparison between SWCNTs and MWCNTs is performed for area and delay. For the same value of delay, it has been observed that MWCNTs require an appreciating lesser (97.8% less) area than SWCNTs. Also, with an area constant for both interconnects, it has been concluded that MWCNTs show less crosstalk-induced delay (52.4% less) than SWCNT bundles. Multi-wall carbon nanotubes can be used as crosstalk immune and compact interconnect material for integrated applications.

Rai *et al.* [114] demonstrated crosstalk reliable electrical performance of various mixed CNTs structures at 22 nm technology nodes. The equivalent models of mixed CNT bundles comprising SWCNTs and MWCNTs are proposed along their parasitic. Various mixed CNTs are developed by altering the position of multi and single-wall nanotubes. The temperature (varying from 300 K to 500 K) based simulations are done to determine crosstalk-dependent delay. The effect of inter-shell coupling is also included, and it is observed that the structure with non-conducting tubes in the center and conducting tubes along the edges offer larger resistance, therefore giving low crosstalk-induced noise voltage. On the other hand, a mixed bundle structure with conducting tubes in the center and non-conducting along the edges gives minimum signal delay time. Depending upon the priority of usage, mixed carbon nanotube bundle structures provide excellent material for interconnects.

- **Stability Analysis of Interconnects**

The frequency, bandwidth, time-response, stability, etc. of interconnects are determined to evaluate their reliability. The following research papers focus on stability-related issues of CNTs.

Majumder *et al.* [115] compared the electrical behavior of MWCNT and MLGNR (multi-layer graphene nanoribbon) in terms of frequency response and bandwidth as shown in Figure 2.9. Interconnects are modeled using a driver-interconnect-load system to determine performance at local and global levels of interconnect. Both interconnects are easy to fabricate and offer high current densities and long MFP of up to 5µm. The electrical parameters like resistance, inductance and capacitance of both interconnects are determined by calculating the count of conducting channels present in each shell.

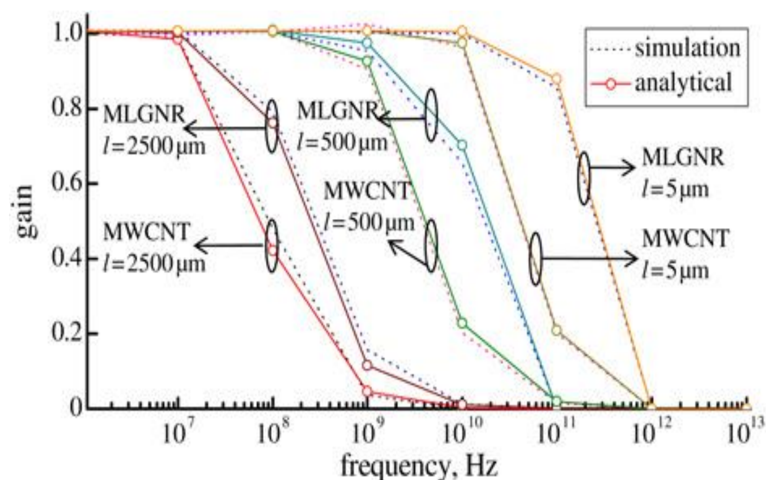


Figure 2.9 Gain versus frequency plot of MLGNR and MWCNT interconnects at varying lengths [115]

The frequency responses form an RC low pass filter. The cut-off frequency is obtained from the absolute frequency responses and then the comparison of bandwidths between the two interconnects is obtained. The frequency response results are compared with HSPICE results. The results are in good relationship with each other. Frequency versus gain plots clearly shows that the bandwidth of MWCNT is 10x smaller than MLGNR at the local level and 4x smaller than MLGNR at the global level.

Kumar *et al.* [116] modeled interconnects using distributed transmission lines and determined the electrical performance of MWCNTs and MLGNR based on signal delay and relative stability for different interconnect lengths. Analytical values of delay of MWCNT and MLGNR are by less than 10% with spice simulated results. It is noticed that for similar delay MWCNTs require 54.5% lesser area than MLGNRs for global levels of interconnect. The relative stability is determined with the response of the transfer function by observing the values of peak overshoots and switching delay, and by drawing Nyquist plots. It is observed that both MWCNT and MLGNR show good stability characteristics. For local interconnect, MLGNR is less stable than MWCNTs; however, at the intermediate and global levels, the stability of multi-layer GNR is more than MWCNTs.

2.6 Identified gaps in the literature.

It is suggested that the resistance of copper rises and the mean free path of electrons decreases beyond the 45 nm technology node. Because of electromigration, surface roughness, and grain boundary scatterings, CNTs have the potential to replace them [117-122]. The performance of SWCNTs is restricted due to fabrication and chirality issues. Multi and double-wall carbon nanotubes have shown reliable results based on delay and power dissipation.

It has also been reported that temperature and crosstalk-dependent mixed carbon nanotube bundles (formed with MWCNTs and SWCNTs and different diameter MWCNTs) have shown outstanding performance as interconnects. These mixed structures also have the potential to replace traditional nanotube materials at global levels. The work presented in this report focuses on temperature-dependent modeling of mixed carbon nanotube bundles formed from MWCNTs and DWCNTs, which have proven themselves better than individual SWCNT, MWCNT, and DWCNT bundles. They can capture the VLSI market at deep submicron technology nodes.

Some of the related domains of CNT that need attention and exploration in detail for the future are mentioned below:

- Studies have compared the performance of copper, SWCNT bundles, MWCNT bundles, and mixed CNTs (bundles formed with different diameter MWCNTs or with SWCNTs and MWCNTs). Yet no work is done on the mixed structure having DWCNTs and MWCNTs. A comparison can be made between the delay and the Power-delay product.
- The effect of temperature can be analyzed for various MDCB structures at different nano-technology nodes.
- The impact of dynamic and functional crosstalk can also be studied on mixed bundle structures having MWCNTs and DWCNTs.
- Stability analysis for MDCB interconnects is also not reported.
- The fabrication of graphitic-based CNT interconnects remains a big challenge. Some new techniques need to be proposed and issues related to it need to be taken off.

2.7 Objectives of the Study

Based on the work done and understanding established from the literature, the listed objectives are proposed:

1. To develop the thermally aware impedance equivalent circuit model for Mixed-CNT bundle as VLSI interconnects.
2. To analyze the impact of temperature variation on the parasitic of different structures of Mixed-CNT bundle for nano-scaled technology nodes.
3. To evaluate the temperature-dependent performance of the Mixed CNT model of proposed structures in terms of delay and PDP at different nano-scaled technology nodes.
4. To compare the results obtained from the above analysis with SWCNT and the copper interconnect.

2.8 Research Methodology

To reach the objectives defined, the following research methodology is opted.

- Problems associated with copper interconnect at scaled technology nodes are recognized.
- Carbon nanotubes and their types- SWCNTs, MWCNTs, and DWCNTs are studied in detail. Their physical structures, electrical equivalents, and parasitic equations are analyzed thoroughly.

- Different structures of mixed CNT bundle (MDCB) interconnect constituting DWCNTs and MWCNTs are developed. The related impedance (R, L, and C) parameters are calculated using mathematical equations.
- The thermally aware models of proposed mixed CNT (MDCB) structures are configured and the effective MFP of conducting electrons is evaluated by considering the influence of various scattering phenomena at high temperatures.
- The schematic diagrams for the thermally dependent models at different nanotechnology nodes and global lengths are formed and simulations are performed with the help of the Tanner tool.
- Delay and PDP-based comparisons are done for all interconnect materials. It has been reported that MDCB structures outperform all existing materials for interconnect applications.
- Global lines face inductive and capacitive coupling effects. So, being an indispensable factor, crosstalk analysis (functional and dynamic) is also done for mixed bundle CNT interconnects.
- Stability analysis in terms of rise time, maximum overshoot, and Nyquist plots of MDCB structures are also performed.
- The mathematical expression of delay (T_{90}) is presented, and the analytical results are also determined. The results lie close to one another and thus validate each other.
- Thus, the obtained results in the report in terms of delay and PDP helps to compare and conclude the performance of mixed CNT with copper and bundled SWCNTs, bundled MWCNTs, and bundled DWCNTs at various technologies. MDCB structures have great potential as VLSI interconnect material for upcoming generations.

3. CIRCUIT ANALYSIS OF MIXED CNTS

The chapter provides insight into the structural and electrical modeling of interconnect materials used for integrated circuit applications at nano-scale nodes. A brief study on copper, single-wall CNT, multi-wall CNT and double-wall CNT, and mixed bundle CNTs is performed to evaluate their performance as global interconnects in terms of delay and PDP [123-135].

3.1 Electrical equivalent circuit modeling of interconnects

The section focuses on physical diagrams, electrical equivalents, and impedance equations of interconnects. Mathematical calculations are performed to determine their values at different lengths and technologies.

3.1.1 Copper as an Interconnect Material

Previously copper has been extensively employed as interconnection material in ICs due to its large melting point temperature and good conductivity. To estimate their delay-based performance the electrical circuit of an interconnecting material is displayed in Figure 3.1. Interconnects are modeled with equivalent parasitic, and their values are determined from respective impedance equations [29,30]. Input pulse is given to the circuitry and transient analysis is performed with CMOS transistor as a driver and is loaded by the capacitor.

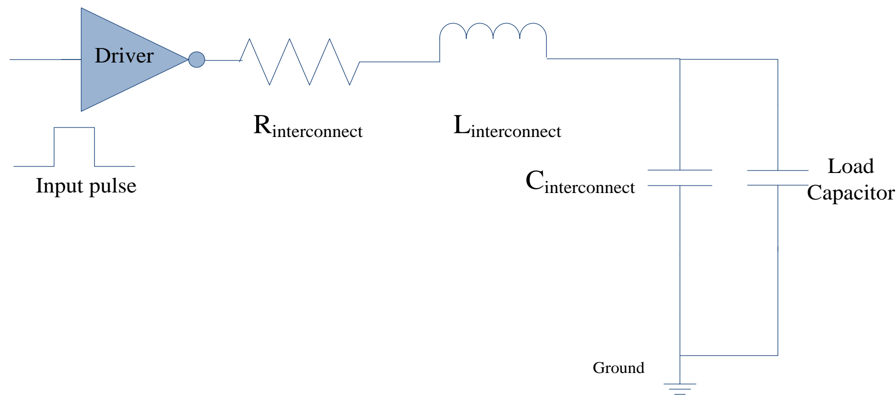


Figure 3.1 Electrical model of an interconnection material

The copper resistance (R_{Copper}) with 'ρ_0' as the technology-reliable resistivity, 'l' as length, 'w' as width, and 't' as the thickness of interconnect (technology parameters, as defined by ITRS) [121,122] is determined from equation (3.1) [35,94].

$$R_{Copper} = \rho_0 (\frac{l}{wt}) \tag{3.1}$$

The schematic diagram of copper wires placed at height 'h_t' from the ground plane and separated by distance 's' from each other is shown in Figure 3.2.

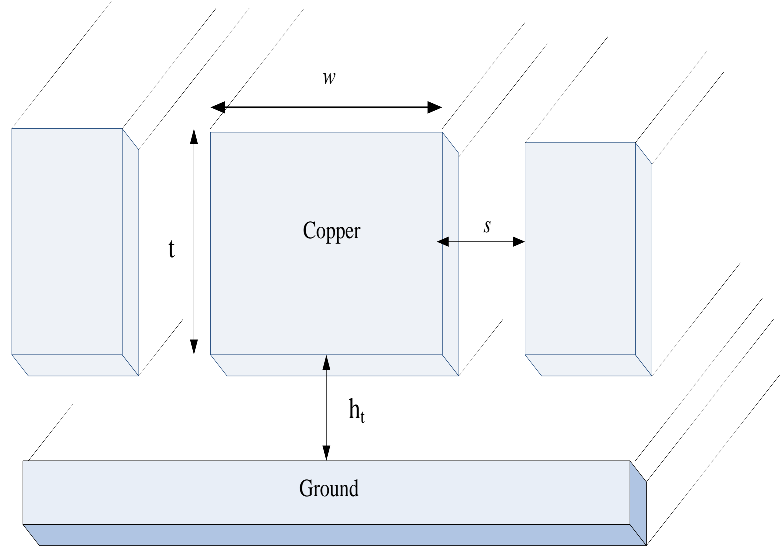


Figure 3.2 Cross-section of copper wires

Copper capacitance (C_{ground}) due to the area covered above the ground plane and fringing flux associated with nearby copper wires is given by equation (3.2).

$$C_{ground} = \varepsilon[\frac{w}{h_t} + 2.22(\frac{s}{s+0.70h_t})^{3.19} + 1.17(\frac{s}{s+1.51h_t})^{0.76}(\frac{t}{t+4.53h_t})^{0.12}] \quad (3.2)$$

The inductance (L_{Copper}) is determined by equation (3.3) [42].

$$L_{Copper} = \frac{\mu_0}{2\pi}[ln(\frac{2l}{w+t}) + \frac{1}{2} + 0.22(\frac{w+t}{l})] \quad (3.3)$$

The values of impedance parameters are determined from equations (3.1), (3.2), and (3.3) by varying lengths of interconnect from 100 µm to 1000µm and are indexed below in Table (3.1).

Table 3.1 RLC values of copper at different lengths for various nanotechnology nodes

	Resistance (kΩ)			Inductance (nH)			Capacitance (pF)		
Length (µm)	32nm	22nm	16nm	32nm	22nm	16nm	32nm	22nm	16nm
100	0.76	1.79	5.85	0.15	0.16	0.17	0.02	0.02	0.02
200	1.53	3.57	11.71	0.33	0.35	0.36	0.05	0.05	0.04
300	2.29	5.36	17.56	0.52	0.55	0.57	0.07	0.07	0.06
400	3.05	7.14	23.42	0.72	0.75	0.79	0.10	0.09	0.08
500	3.81	8.93	29.27	0.92	0.96	1.00	0.12	0.11	0.10
600	4.58	10.71	35.12	1.13	1.17	1.23	0.15	0.14	0.12
700	5.34	12.50	40.98	1.34	1.39	1.45	0.17	0.16	0.14
800	6.10	14.29	46.83	1.55	1.61	1.68	0.19	0.18	0.16
900	6.86	16.07	52.69	1.77	1.83	1.91	0.22	0.20	0.18
1000	7.63	17.86	58.54	1.99	2.06	2.15	0.24	0.23	0.20

Impedance values listed above are also plotted against different lengths and technologies as displayed in Figure 3.3 (a)-(c). Figure 3.3 (a) reflects the resistance values of copper for different

technology nodes. Figure 3.3 (b) shows inductance at three technologies for a wide range of lengths and similarly, Figure 3.3 (c) compares the value of capacitance of copper for different technologies. It can be seen from the line graphs that the impedance values of a copper surge in the length of interconnect.

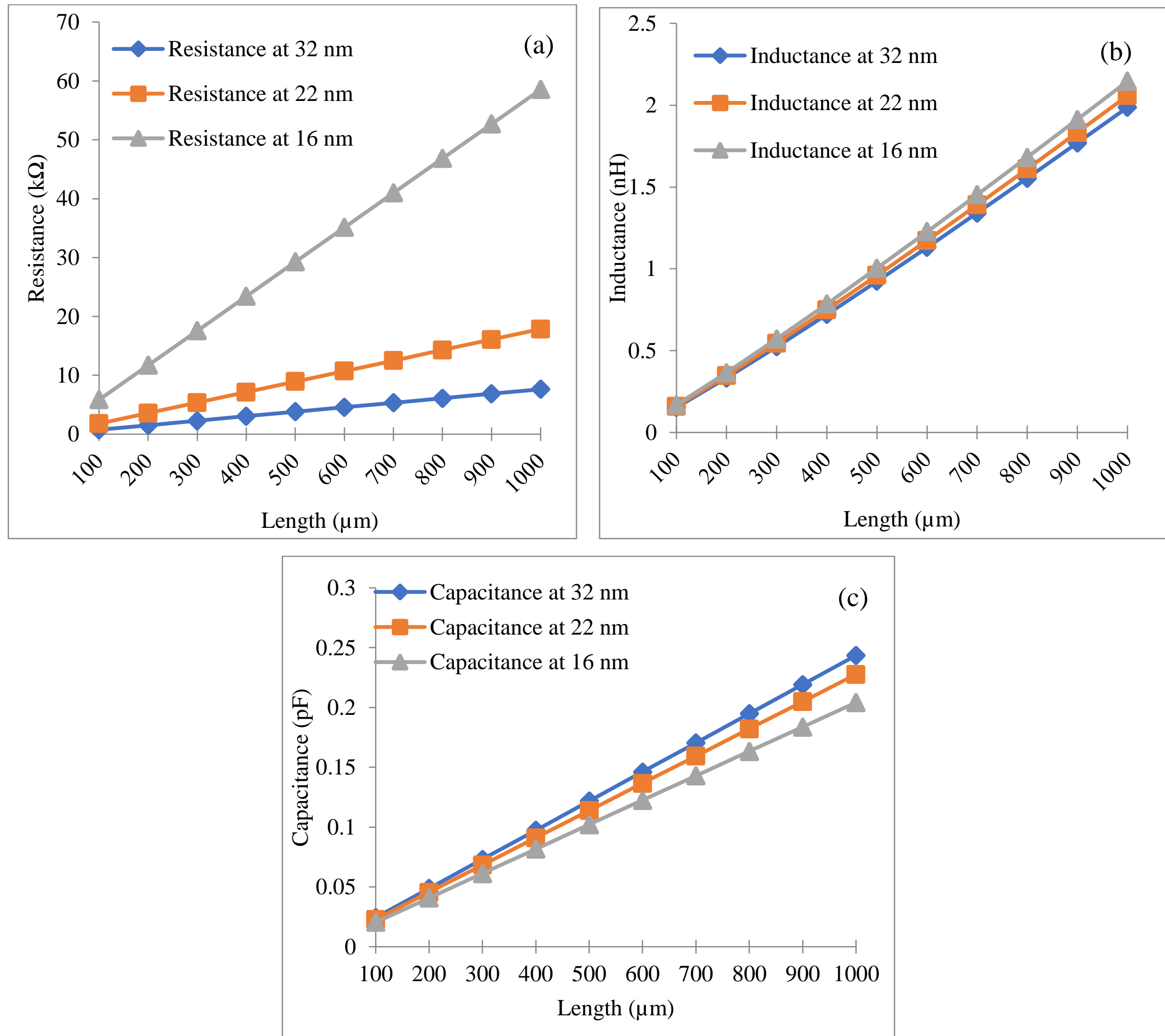


Figure 3.3 Impedance values of copper at different nanotechnology nodes for length varied from 100μm-1000μm (a) Resistance (b) Inductance (c) Capacitance

Copper shows a sudden increase in resistance as shown in Figure 3.3 (a) due to fatal concerns like the migration of electrons, surface roughness, and grain-boundary scattering at the global length of interconnect as we scale down the technology from 32nm to 22nm to 14nm node [29,30]. The trend is true for inductance parameters also but with advancement in technology nodes and reduced dimensions, the capacitance decreases due to decreased capacitive coupling with the ground plane and neighboring interconnect wires. Thus, increased collisions and decreased MFP of electrons in copper lead to its failure by as VLSI interconnect material beyond 32nm technology node for global lengths [39,42].

3.1.2 Single-walled CNT as an Interconnect Material

SWCNT is developed by rolling a single sheet of graphene in a cylindrical shape. With the diameter of the nanotube as 'd_{sw}' and length from the center of the nanotube to the ground plane as 'y_1', the physical structure of an isolated SWCNT is presented in Figure 3.4 [54].

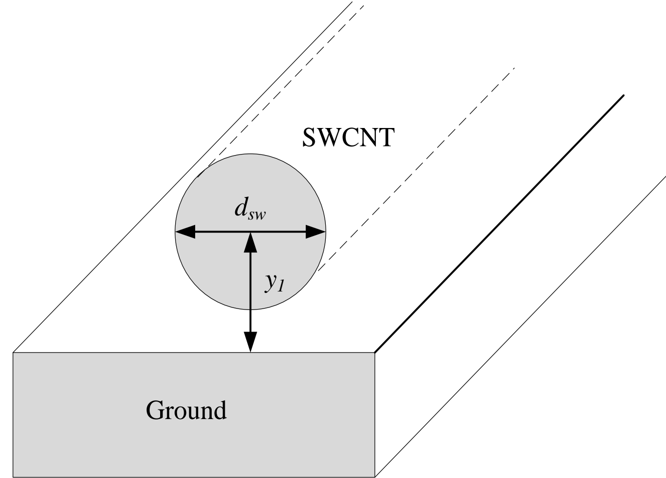


Figure 3.4 Structure of single-walled CNT placed above ground plane [55]

The identical/RLC circuit of SWCNT is presented in Figure 3.5. The four conducting channels in the nanotube are the result of spin and sub-lattice degeneracies of its conducting electrons.

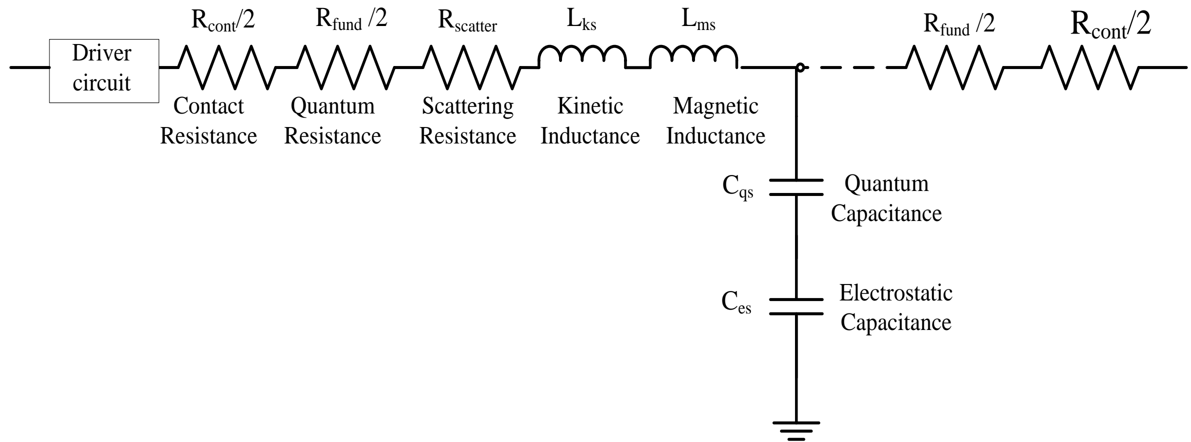


Figure 3.5 Electrical model of SWCNT [55]

The resistance comprises three components. The unavoidable resistance that exists due to incomplete metal-CNT contact greatly relies on the manufacturing procedure (here, R_{cont} is taken as 2KΩ). With 'h' as the Planck's constant ($6.62\text{x}10^{-34}$Js) and e as the electron charge ($1.6\text{x}10^{-19}$ C), the distributed fundamental resistance (R_{fund}) exists at the endpoint on both sides of the nanotube is expressed by equation (3.4) [55,56].

$$R_{fund} = \frac{h}{4e^2} \tag{3.4}$$

Scattering resistance ($R_{scatter}$) is seen when the length (L) of the nanotube exceeds MFP (λ_0) of conducting electrons and collisions are faced by electrons. It is given by equation (3.5).

$$R_{scatter} = \frac{h}{4e^2}\left(\frac{L}{\lambda_0}\right) \tag{3.5}$$

As the nanotube is placed over the ground plane, a certain charge is accumulated in the nanotube, and it results in electrostatic capacitance (C_{es}) given by equation (3.6) [57].

$$C_{es} = \frac{2\pi\varepsilon}{ln\left(\frac{y_1}{d_{sw}}\right)} \tag{3.6}$$

The quantum capacitance (C_{qSWCNT}) in the current-carrying nanotube is expressed by equation (3.7).

$$C_{qSWCNT} = \frac{2e^2}{hv_f} \tag{3.7}$$

The net quantum capacitance because of four parallel conducting channels in the nanotube is estimated by equation (3.8).

$$C_{qs} = 4C_{qSWCNT} \tag{3.8}$$

The associated magnetic inductance (L_{ms}) of SWCNT is given by equation (3.9).

$$L_{ms} = \frac{\mu}{2}\left(ln\frac{y_1}{d_{sw}}\right) \tag{3.9}$$

The accumulated kinetic energy in the channel of the nanotube gives kinetic inductance (L_{ks}) which is calculated by equation (3.10).

$$L_{ks} = \frac{h}{2e^2 v_f} \tag{3.10}$$

The large value of isolated SWCNT resistance is overcome by packing and placing nanotubes in a bundle as shown in Figure 3.6. Thus, the parallel addition of CNT resistances packed in a bundle helps in decreasing the initial high value of isolated CNT.

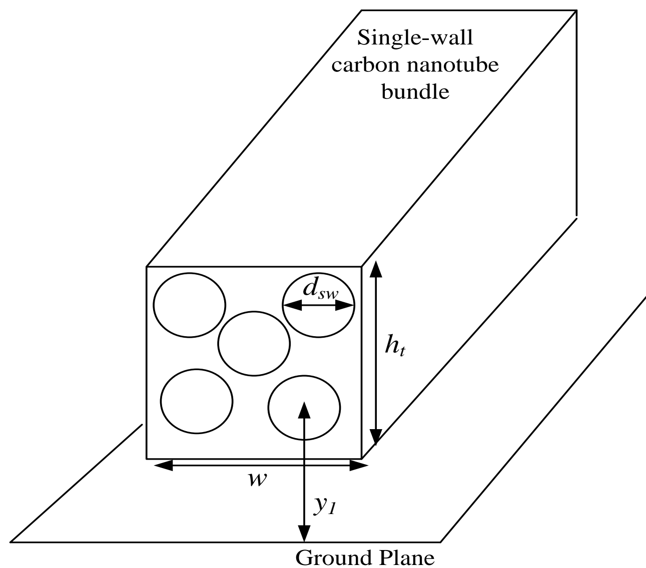


Figure 3.6 Bundled SWCNT placed over the ground plane.

Figure 3.6 shows a batch of SWCNTs. Phrases to determine the count of rows (n_r) and count of columns (n_c) of CNTs in a batch with width 'w' and height 'h_t' are given by equation (3.11) and equation (3.12) [56,57].

$$n_r = \left\{\frac{w-d_{sw}}{x}\right\} \tag{3.11}$$

$$n_c = \left\{\frac{h_t-d_{sw}}{(\sqrt{3}/2)x}\right\} + 1 \tag{3.12}$$

Depending upon the count of rows, the number of CNTs (n_{SWCNT}) placed in a nanotube batch is given by equation (3.13) or equation (3.14) [52].

$$\text{If } n_r \text{ is even, } n_{SCNT} = n_r n_c - \left(\frac{n_c}{2}\right) \tag{3.13}$$

$$\text{If } n_r \text{ is odd, } n_{SCNT} = n_r n_c - \left(\frac{n_c-1}{2}\right) \tag{3.14}$$

The electrical resistance of the Single-Walled CNT bundle is given by equation (3.15).

$$R_{SWCNT(Bundle)} = \frac{\frac{h}{4e^2}\left(\frac{L}{\lambda}\right)}{n_{SCNT}} \tag{3.15}$$

The series addition of the quantum and the electrostatic capacitance gives the resultant capacitance (C_{Bundle})the of bundle, and it is expressed by equation (3.16) [53].

$$C_{Bundle} = \frac{C_{es}^{Bundle} C_{qs}^{Bundle}}{C_{es}^{Bundle} + C_{qs}^{Bundle}} \tag{3.16}$$

The inductance of the nanotubes is estimated by equation (3.17).

$$L_{CNT} = \frac{L_{ms}+L_{ks}}{n_{SCNT}} \tag{3.17}$$

The impedance values of single-shell CNT are indexed below in Table 3.2.

Table 3.2 RLC values of SWCNT at variable lengths for various nanotechnology nodes

	Resistance (kΩ)			Inductance (nH)			Capacitance (pF)		
Length (μm)	32nm	22nm	16nm	32nm	22nm	16nm	32nm	22nm	16nm
100	0.14	0.28	0.67	0.08	0.16	0.39	0.35	0.25	0.17
200	0.27	0.55	1.34	0.16	0.32	0.78	0.70	0.51	0.33
300	0.41	0.83	2.00	0.24	0.49	1.17	1.06	0.76	0.50
400	0.54	1.10	2.67	0.32	0.65	1.57	1.41	1.02	0.66
500	0.67	1.38	3.33	0.40	0.81	1.96	1.76	1.27	0.83
600	0.81	1.65	4.00	0.48	0.97	2.35	2.11	1.53	1.00
700	0.94	1.93	4.66	0.55	1.13	2.74	2.47	1.78	1.16
800	1.08	2.20	5.33	0.63	1.29	3.13	2.82	2.04	1.33
900	1.21	2.48	5.99	0.71	1.46	3.52	3.17	2.29	1.49
1000	1.35	2.75	6.66	0.79	1.62	3.91	3.52	2.54	1.66

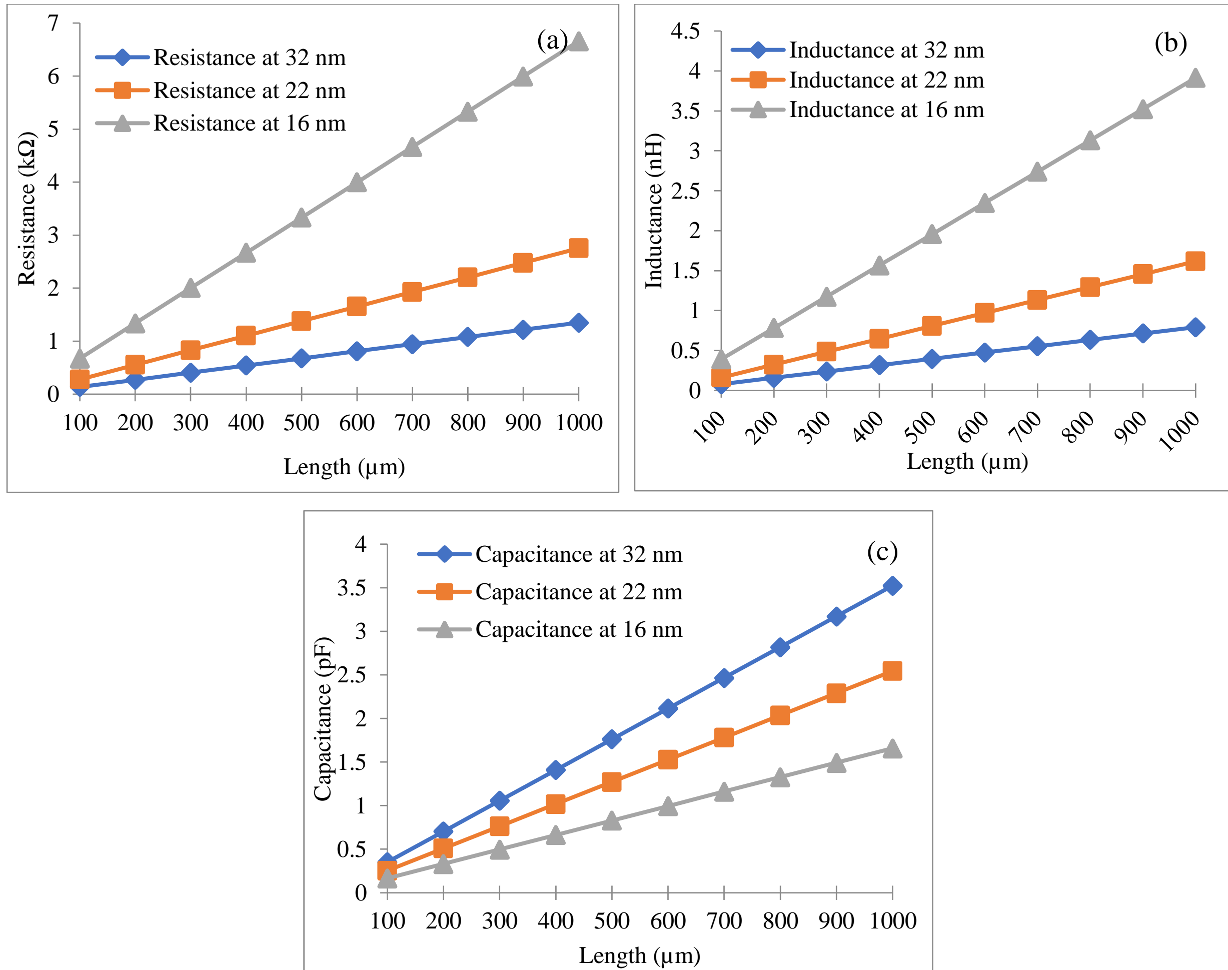


Figure 3.7 Impedance values of SWCNT at different technology nodes for length varied from 100µm-1000µm (a) Resistance (b) Inductance (c) Capacitance

Figure 3.7 (a)-(c) displays the change of resistance, inductance, and capacitance of single-wall carbon nanotube over variable lengths for various nano-technology nodes. As seen in Figure 3.7 resistance and inductance of nanotube rises with the scaling of technology; however, capacitance shows vice-versa results. This is because as we scale down the technology, the number of nanotubes that can be placed in a technology batch reduces, thereby increasing the dominance of resistance. So, with the decrease in the count of nanotubes with technological advancement, lesser tubes of a far less capacitive effect. It is concluded that all impedance (R, L, C) values of SWCNT show a rise with the rise in the length of interconnect. So, impedance values of interconnect need to be examined carefully for global lengths beyond 500µm.

3.1.3 Multi-walled CNT as an Interconnect Material

MWCNT is formed by rolling more than two graphite sheets concentrically in the shape of a cylinder. The hollow shells are placed at a Vander Wal (δ) distance of 0.34 nm from each other and the width of the innermost and the outermost shells are indicated as 'D_{max}' and 'D_{min}'

respectively [136-145]. It is situated at a distance of 'h_m' from the ground plane as presented in Figure 3.8 [59]. The electrical equivalent model of the multi-wall CNT design is displayed in Figure 3.9. The number of shells (*p*) in the MWCNT design is expressed by equation (3.18).

$$p = 1 + \frac{(D_{max} - \frac{D_{max}}{2})}{2\delta} \tag{3.18}$$

There are multiple shells in MWCNT and the diameter (D_i) of the *ith* shell can be calculated by equation (3.19) [60].

$$D_i = D_{max} - (2\delta[\mathrm{i} - 1]) \tag{3.19}$$

The count of i for shells varies from 1 to 'p'. With a= 0.0612 nm^{-1} and b=0.425 the number of conducting channels in shells of MWCNT is expressed by equation (3.20).

$$N_i = aD_i + b \tag{3.20}$$

The resistance of Multi-Walled CNTs is determined by the addition of three components i.e., contact resistance (R_c) (taken around 2 KΩ) , quantum resistance (R_{qi}), and scattering resistance (R_{si}). With n_{MWCNT} as the total number of multi-shelled CNTs in a bundle, h as Planck's constant, 'e' is the electron charge, and 'L' is the length of interconnect line, the resistance of MWCNT bundle is given below by equation (3.21) [61-63].

$$R_{MWCNT} = R_c + R_{qi} + R_{si} = \frac{R_c + \frac{h}{2N_i e^2}(1 + \frac{L}{\lambda})}{n_{MWCNT}} \tag{3.21}$$

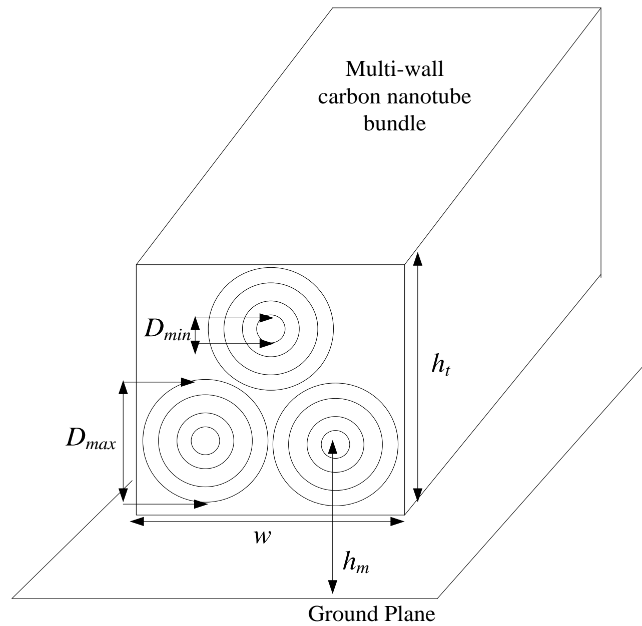


Figure 3.8 Physical structure of MWCNT placed over the ground plane.

Two inductances occur in multi-walled CNT design and the related magnetic inductance parameter of each shell with 'μ' as magnetic permeability can be determined by equation (3.22).

$$L_{mi} = \frac{\mu}{2\pi} cosh^{-1}(\frac{2h_m}{D_i}) \quad (3.22)$$

The kinetic inductance associated with each shell of multiwall CNT with 'v_f' as the fermi velocity of moving electrons can be computed from equation (3.23) [59].

$$L_{ki} = \frac{h}{2(N_i e^2 v_f)} \quad (3.23)$$

The net inductance is given by the parallel sum of kinetic and magnetic inductance in equation (3.24)

$$L_{MWCNT} = \frac{L_{mi}+L_{ki}}{n_{MWCNT}} \quad (3.24)$$

The quantum capacitance of MWCNT is estimated by equation (3.25).

$$C_{qi} = \frac{2(N_i e^2)}{hv_f} \quad (3.25)$$

The electrostatic capacitance of the MWCNT spaced at the distance h_m above the ground plane is expressed by equation (3.26) [65].

$$C_{ei} = \frac{2\pi\mathcal{E}}{cosh^{-1}(\frac{2h_m}{D_{max}})} \quad (3.26)$$

The capacitive pairing among different shells of MWCNT is shown by equation (3.27) [59].

$$C_{si} = \frac{2\pi\mathcal{E}}{ln(\frac{D_{i+1}}{D_i})} \quad (3.27)$$

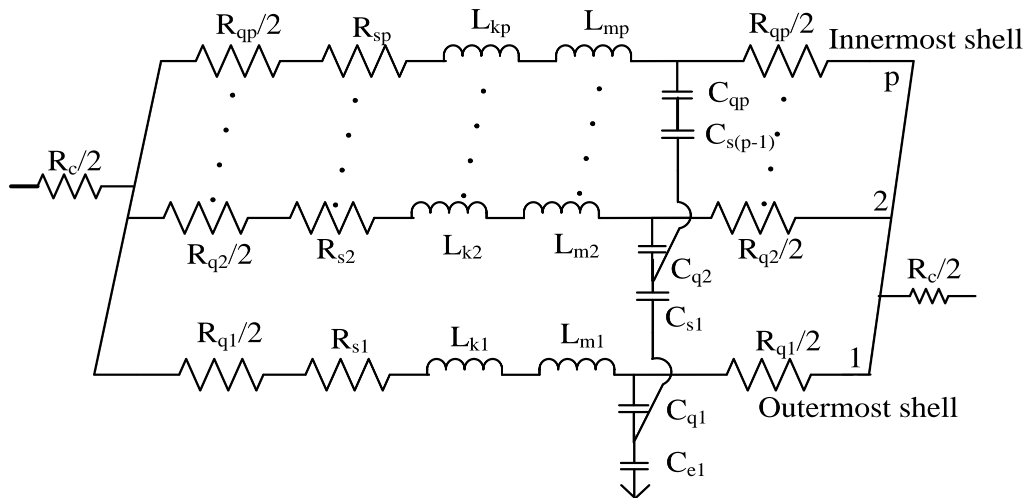


Figure 3.9 Electrical equivalent model of MWCNT [59]

The impedance parameters i.e., resistance, inductance, and capacitance of many-shell CNT called multi-wall CNT are calculated from equations listed in section 3.3 for three technology nodes by varying lengths of interconnect from 100 µm to 1000 µm and are mentioned below in Table 3.3. Different technological comparisons of electrical parameters at variable lengths of multi-wall carbon nanotubes are shown in Figure 3.10 (a)-(c).

Table 3.3 RLC values of MWCNT at different lengths for various nanotechnology nodes

	Resistance (kΩ)			Inductance (nH)			Capacitance (pF)		
Length (µm)	32nm	22nm	16nm	32nm	22nm	16nm	32nm	22nm	16nm
100	0.22	0.59	1.49	0.77	2.06	5.25	0.02	0.01	0.01
200	0.43	1.14	2.90	1.54	4.12	10.50	0.04	0.02	0.02
300	0.63	1.69	4.30	2.31	6.19	15.74	0.06	0.04	0.03
400	0.84	2.24	5.71	3.08	8.25	20.99	0.08	0.05	0.03
500	1.04	2.80	7.12	3.85	10.31	26.24	0.10	0.06	0.04
600	1.25	3.35	8.52	4.62	12.37	31.49	0.12	0.07	0.05
700	1.46	3.90	9.93	5.39	14.43	36.74	0.14	0.09	0.06
800	1.66	4.45	11.33	6.16	16.49	41.98	0.16	0.10	0.07
900	1.87	5.00	12.74	6.93	18.56	47.23	0.18	0.11	0.08
1000	2.07	5.56	14.14	7.70	20.62	52.48	0.20	0.12	0.08

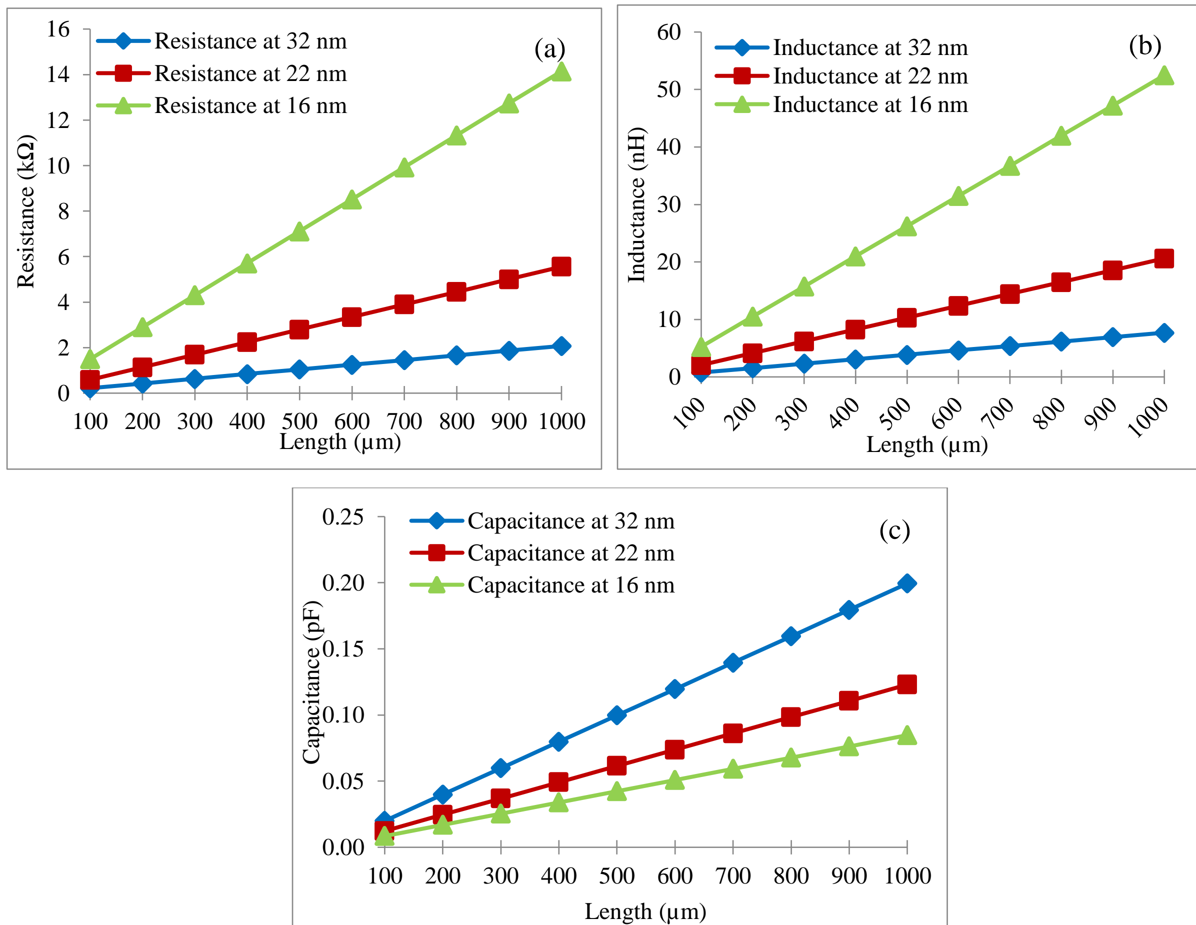


Figure 3.10 Impedance values of Multi-Walled CNT at various technology nodes for length varied from 100µm-1000µm (a) Resistance (b) Inductance (c) Capacitance

The amount of resistance and inductance offered by MWCNTs is less at the 32nm technology node than at the 14 nm node. The values of capacitance sa how vice-versa relation. Large-diameter MWCNTs are easier to fabricate than SWCNTs and have been commonly used to interconnect different nodes in integrated circuits.

3.1.4 Double-walled CNT as an Interconnect material

DWCNT is a unique case of MWCNT and is formed by rolling specifically two sheets of graphene concentrically as shown in Figure 3.11 [76,77]. SWCNTs, due to their simple structure are widely used as interconnect material but faces chirality issues which determine the metallic or semiconducting nature of nanotube. The double-shell CNT structure helps in reducing resistance because of the parallel sum of shells. It also results in more conductance in DWCNTs than in SWCNTs.

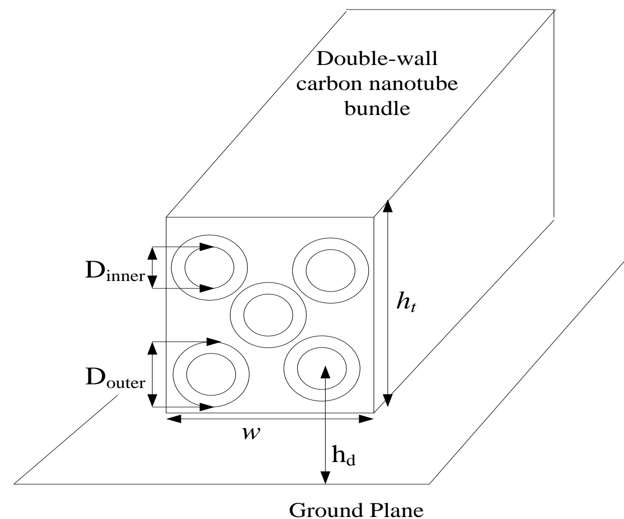


Figure 3.11 Physical structure of DWCNT

With two (inner and outer) shells placed concentrically, the electrical circuit of double wall CNT is shown in Figure 3.12.

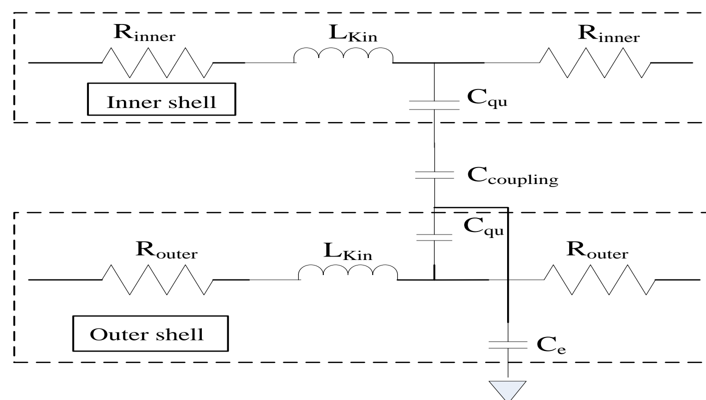


Figure 3.12 Electrical equivalent model of DWCNT interconnect [76]

The resistance of the inner *(R_{inner})* and the outer (R_{outer}) shell of the Double Walled CNT design with their respective mean free paths ($\lambda_{inner.eff}$ and $\lambda_{outer.eff}$) can be formulated from equation (3.28) and equation (3.29). The effective resistance of DWCNT (R_{DWCNT}) in a bundle with n_{DWCNT} nanotubes is figured out by the parallel sum of both shell resistances as shown in equation (3.30).

$$R_{inner} = \frac{h}{4e^2}(1 + \frac{L}{\lambda_{inner.eff}}) \tag{3.28}$$

$$R_{outer} = \frac{h}{4e^2}(1 + \frac{L}{\lambda_{outer.eff}}) \tag{3.29}$$

$$R_{DWCNT} = \frac{R_{outer}+R_{inner}}{n_{DWCNT}} \tag{3.30}$$

The coupling capacitance ($C_{coupling}$), the quantum capacitance (C_{qu}), and the electrostatic capacitance (C_e) of DWCNT can be given by equations (3.31), (3.32), (3.33) [79].

$$C_{coupling} = \frac{2\pi\mathcal{E}}{ln(\frac{D_{outer}}{D_{inner}})} \tag{3.31}$$

$$C_{qu} = \frac{2(2e^2)}{hv_f} \tag{3.32}$$

$$C_e = \frac{2\pi\mathcal{E}}{cosh^{-1}(\frac{2h_d}{D_{outer}})} \tag{3.33}$$

The net kinetic inductance of the DWCNT bundle is determined by equation (3.34).

$$L_{DWCNT} = \frac{L_{kin}}{n_{DWCNT}} = \frac{\frac{h}{2(2e^2v_f)}}{n_{DWCNT}} \tag{3.34}$$

Resistance, inductance, and capacitance of double-wall CNT are formulated from the equations shown above and are mentioned below in Table 3.4. These values are plotted against length and compared technology-wise as shown in Figure 3.13 (a)-(c).

Table 3.4 RLC values of DWCNT at different lengths for various nanotechnology nodes

	Resistance (kΩ)			Inductance (nH)			Capacitance (pF)		
Length (μm)	32nm	22nm	16nm	32nm	22nm	16nm	32nm	22nm	16nm
100	0.13	0.28	0.70	0.11	0.23	0.57	0.07	0.05	0.03
200	0.26	0.55	1.38	0.22	0.46	1.15	0.13	0.10	0.07
300	0.39	0.82	2.07	0.33	0.69	1.72	0.20	0.15	0.10
400	0.52	1.10	2.75	0.44	0.91	2.30	0.26	0.20	0.13
500	0.66	1.37	3.44	0.55	1.14	2.87	0.33	0.24	0.17
600	0.79	1.64	4.12	0.66	1.37	3.44	0.39	0.29	0.20
700	0.92	1.91	4.81	0.77	1.60	4.02	0.46	0.34	0.24
800	1.05	2.19	5.49	0.88	1.83	4.59	0.52	0.39	0.27
900	1.18	2.46	6.18	0.99	2.06	5.17	0.59	0.44	0.30
1000	1.31	2.73	6.86	1.10	2.29	5.74	0.65	0.49	0.34

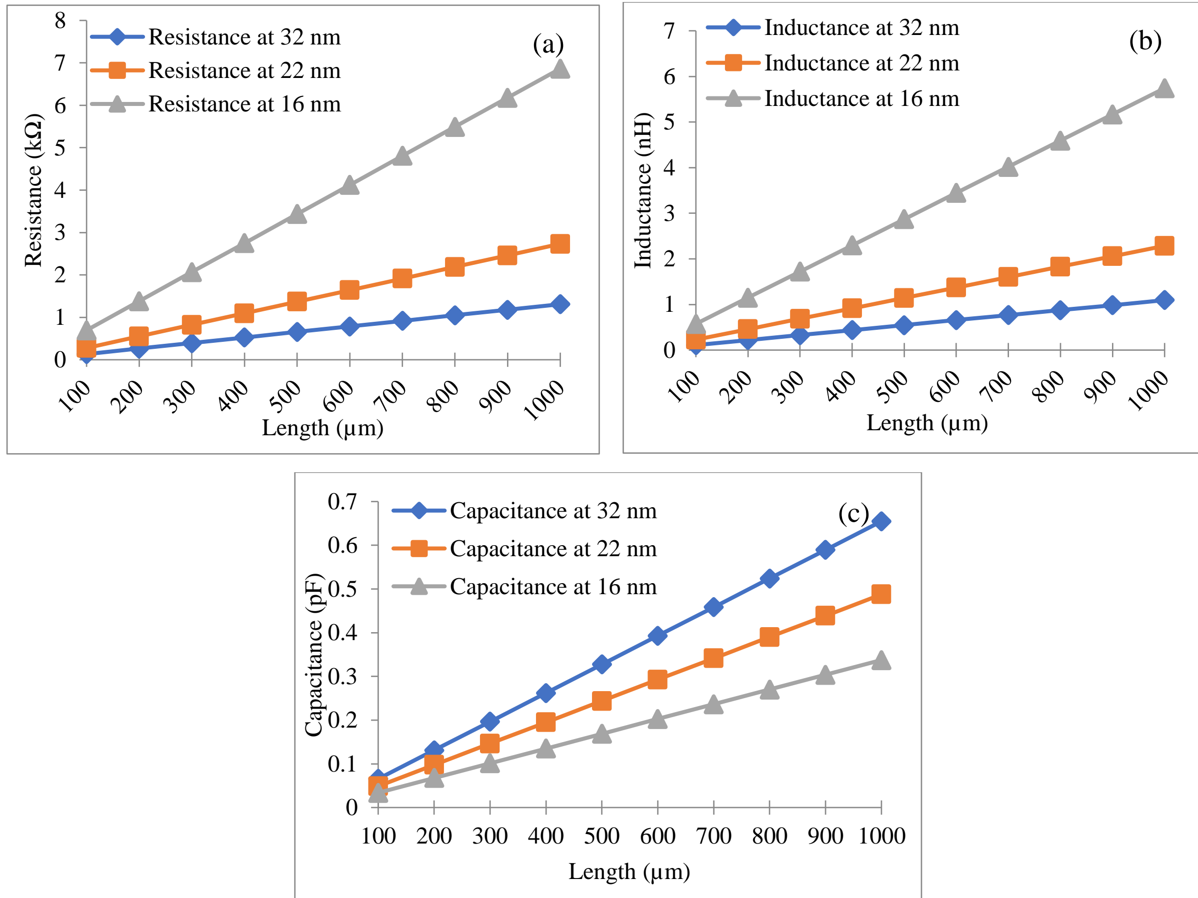


Figure 3.13 Impedance values of DWCNT at various technology nodes for length varied from 100µm-1000µm (a) Resistance (b) Inductance (c) Capacitance

3.2 Performance comparison between copper, SWCNT, MWCNT, and DWCNT

The section presents delay and PDP for copper, SWCNT, MWCNT, and DWCNT at different interconnect lengths (500µm and 1000µm) for 32 nm, 22 nm, and 16 nm technology nodes. Figure 3.14 shows the distributed element diagram employed for simulation using a CMOS driver to determine performance specifications for longer interconnect lines with a pulse-shaped input waveform [121,122].

The approach assumes equal and sectional distribution of attributes along the length. The aspect ratio of transistors is taken as 60. And the size of the PMOS transistor is 3 times the NMOS transistor. The surge time is determined as the time consumed by the resultant waveform to achieve 90% of its amplitude from 10% of the amplitude value, while the fall time is the time at which the waveform drops to 10% value from 90% of the amplitude. The net delay of the circuit is determined by an average of both (rise and fall times). The performance of the circuit is determined by T-spice analysis.

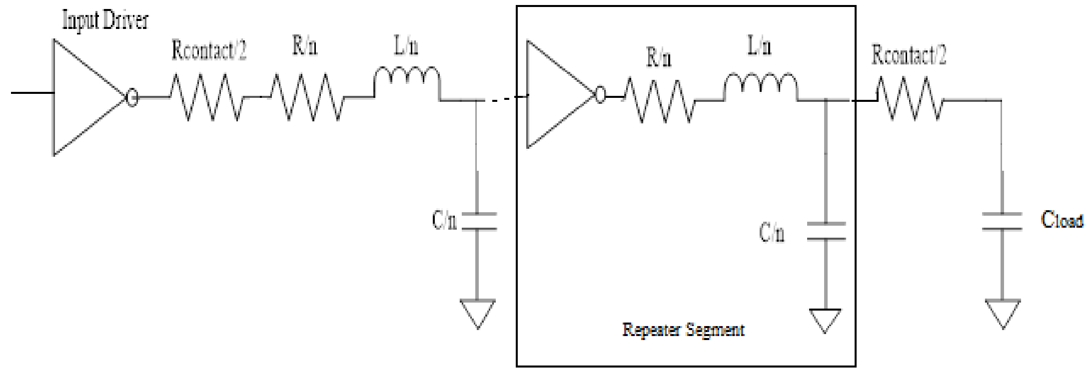


Figure 3.14 Distributed element approach setup used for determining signal delay using T-spice [14]

3.2.1 Delay-based simulation results.

Values of RLCs for interconnect materials are determined by applying equations mentioned in previous sections. The SWCNT diameter is simulated as 1 nm, the MWCNT outer diameter is simulated as 8 nm and the DWCNT outer diameter is simulated as 1.68 nm for 500µm and 1000µm interconnect lengths. Figure 3.15 (a) and (b) demonstrate delay comparison of copper, SWCNT, MWCNT, and DWCNT for 500µm and 1000µm interconnect length respectively. Due to serious issues in copper like high resistance and elevated delay due to electromigration and other surface scatterings, it shows maximum delay than nanotube structures. The delays of all interconnect materials increase with interconnect length and show a tremendous increase when we move from 32nm technology to 16nm technology. This is because resistance shows a direct relationship with the length and technology scaling.

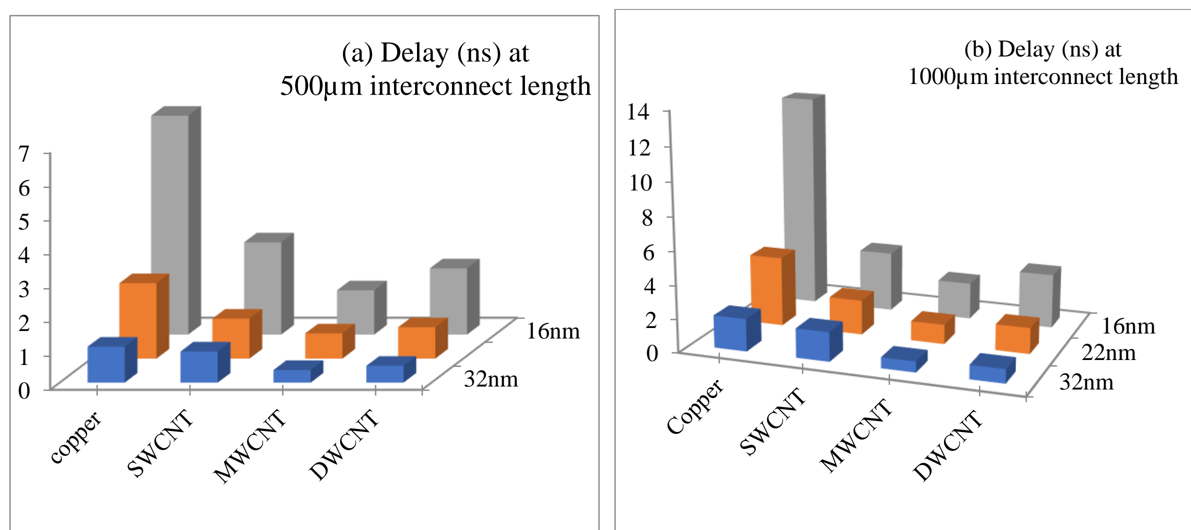


Figure 3.15 Analysis of delay between copper, Single Walled CNT, Multi Walled CNT, Double Walled CNT at different technology nodes.

3.2.2 PDP-based simulation results.

Carbon nanotubes display superior results as compared to copper in delay and figure of merit parameter i.e., PDP at and beyond 32 nm technology node as shown in Figure 3.15 and Figure 3.16 because of their excellent conducting properties at elevated temperatures. DWCNTs offer a lower amount of resistance than SWCNTs due to their double shell structure. The net resistance of DWCNTs is obtained by parallel addition of inner and outer layers and so results in a lesser delay of DWCNTs. MWCNTs and DWCNTs yield the best comparable results concerning delay and PDP than copper and SWCNTs. It is concluded from graphs that nanotubes can undoubtedly replace copper at global length by yielding less delay and PDP at various technology nodes.

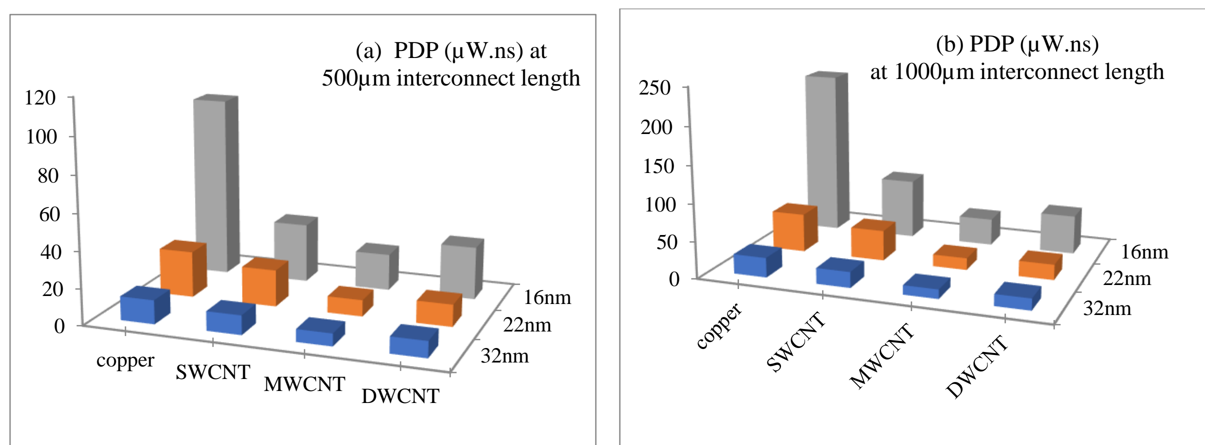


Figure 3.16 Analysis of PDP among copper, SWCNT, MWCNT, and DWCNT at various technology nodes

3.3 Mixed bundle CNT as an Interconnect material

Mixed CNTs are formed by more than one type of CNT like MWCNTs and SWCNTs or different diameter MWCNTs [98-103]. These mixed CNTs are formed to form a dense bundle for increasing the conductivity by efficiently using the space in bundles. The fabrication of metallic SWCNTs is greatly dependent on the chirality factor. So, DWCNTs (always metallic in nature) are comparatively easy to manufacture and have better conductivity due to two shells than SWCNTs are suggested to be used in mixed bundles with MWCNTs.

In this report, four types of new mixed bundle designs are developed by altering the placements of constituent CNTs as shown in Figure 3.17. In the MDCB-1 structure, DWCNTs are planted in the center and all MWCNTs are positioned along the peripheral edges of the bundle. The second MDCB design is developed by positioning Double Walled CNTs along the periphery and all Multi-Walled CNTs in the center of the structure. The third design is designed by positioning all Multi-Walled CNTs in the upper half and Double Walled CNTs in the lower

horizontal half of the bundle. MDCB-4 interconnect design is formed in which all DWCNTs and all MWCNTs are put vertically in the right and left half of the structure.

3.3.1 Development of MDCB structures

Four mixed structures are developed by positioning MWCNTs and DWCNTs at different locations to determine how the count of CNTs and their characteristic properties influence their electrical conduction and coupling. The comparison is drawn among four MDCB structures and isolated counterparts like MWCNTs and DWCNTs. Depending upon the design with the specific width and height of nanotube bundles as depicted in Figure 3.17, the count of nanotubes in a particular bundle is estimated by determining the count of rows and columns in a bundle.

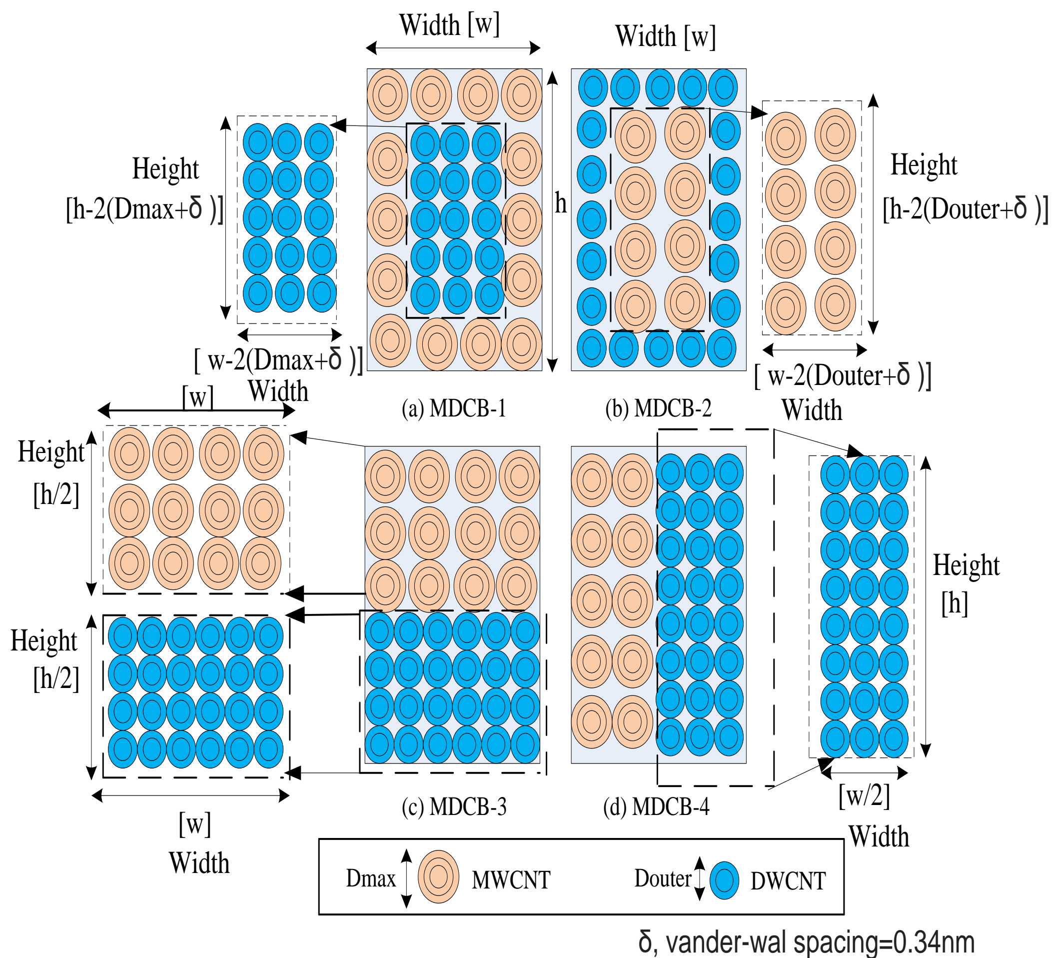


Figure 3.17 Different types of MDCB structures

The outer-most diameter of MWCNT (D_{max}) is assumed as 8 nm and for Double Walled CNT (D_{outer}) is assumed as 1.68 nm. The generalized expressions are derived and used to calculate any number and type of CNTs in a bundle. For any kind of nanotube having a diameter say 'D'

(for MWCNT, D_{max}=8nm, and DWCNT D_{outer}=1.68nm) and with width '*Width*' and height '*Height*' of bundle blocks (width and height are technology parameters [121,122]) as shown in figure 3.17, the count of nanotubes in a row (N_{Rows}) is calculated by the expression given in equation (3.35).

$$N_{Rows} = floor\left(\frac{Width-D}{D+\delta} + 1\right) \tag{3.35}$$

The column number (N_{column}) in a mixed CNT bundle can be estimated through equation (3.36).

$$N_{Column} = floor\left(\frac{Height-D}{\frac{\sqrt{3}}{2}D+\delta} + 1\right) \tag{3.36}$$

If N_{column} is even, then the count is given by equation (3.37).

$$N_{CNT} = (N_{Rows.}N_{Column.}) - (\frac{N_{Column.}}{2}) \tag{3.37}$$

If N_{column} is odd, then the count is given by equation (3.38).

$$N_{CNT} = (N_{Rows.}N_{Column.}) - (\frac{N_{Column.}-1}{2}) \tag{3.38}$$

After obtaining the number of multi-walled CNTs and double-walled CNTs in a bundle, MDCB designs can be designed. Mixed bundle CNT interconnect structure is a little more complex than individual counterparts [73-75,80,82]. The hierarchical structure of the MDCB interconnect is shown in Figure 3.18 and is thus designed with the help of MWCNTs and DWCNTs.

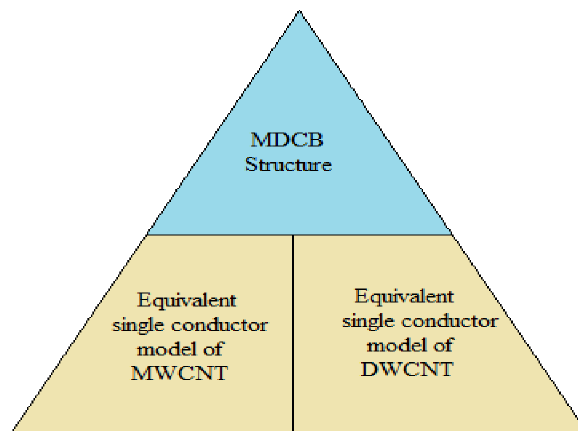


Figure 3.18 Hierarchical model of MDCB Interconnect

The electrical circuit of mixed CNT bundles is studied by analyzing electrical models of MWCNTs and DWCNTs. The electrical models of MWCNTs and DWCNTs have been covered in the previous section of this chapter. In this way, many MWCNTs and DWCNTs are

put and combined to form the MDCB structure. The detailed circuit of MDCB interconnects with multiple MWCNTs and DWCNTs placed in parallel is presented in Figure 3.19.

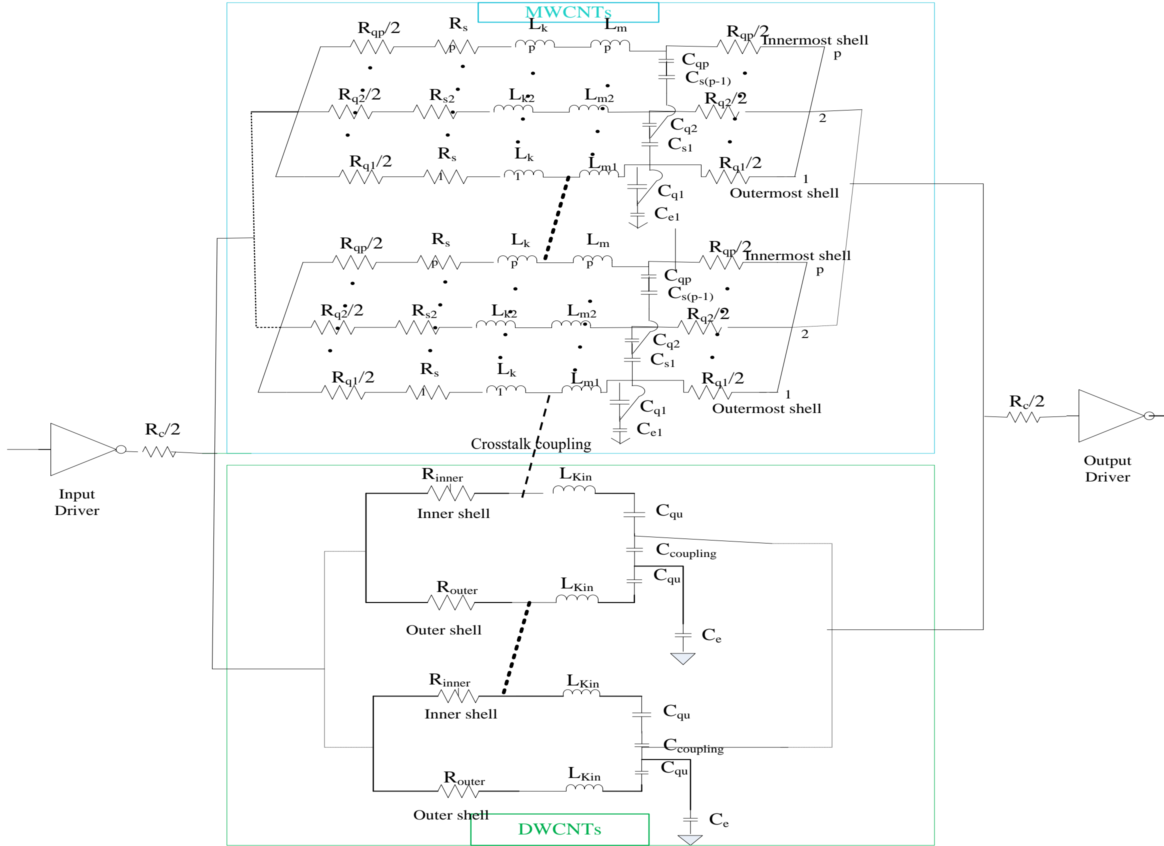


Figure 3.19 MTL model of MDCB interconnects

The total number of nanotubes in the MDCB structure (N_{MDCB}) is given by the sum of multi-wall CNTs (N_{MWCNT}) and double-wall (N_{DWCNT}) nanotubes as expressed by equation 3.39.

$$N_{MDCB} = N_{MWCNT} + N_{DWCNT} \tag{3.39}$$

The number of MWCNTs and DWCNTs in the bundle is determined by equations (3.40-3.41).

$$N_{MWCNT} = N_{Rows(MWCNT)}.N_{Column(MWCNT)} \tag{3.40}$$

$$N_{DWCNT} = N_{Rows(DWCNT)}.N_{Column(DWCNT)} \tag{3.41}$$

The generalized expression to determine the number of MWCNTs and DWCNTs in a bundle is expressed in equation (3.33) -(3.36). The structural description and formulas to find the number of conducting channels, shells, resistances, inductances, and capacitances of MWCNTs and DWCNTs in a bundle are explained in sections 3.1.3 and 3.1.4 respectively of this chapter. Further, the electrical model of the MDCB structure is simplified from MTL (by the parallel sum of all MWCNTs and the separate parallel sum of all DWCNTs) to ESC models of MWCNTs and DWCNTs and is shown in Figure 3.20.

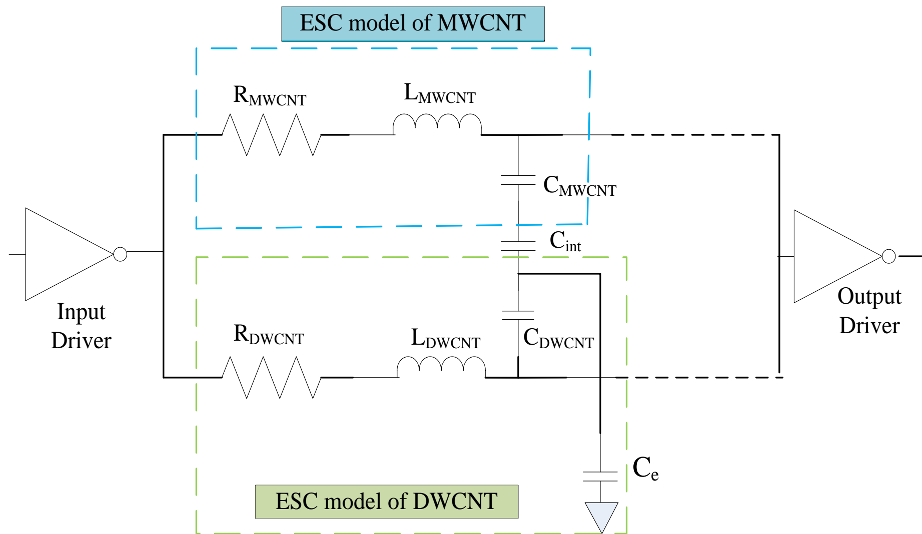


Figure 3.20 Simplified electrical structure of MDCB interconnects (stage 1)

The circuit shown in Figure 3.20 is further simplified to form an ESC model of MDCB interconnect by parallel addition of net MWCNT and DWCNT parasitic as shown in Figure 3.21.

The equivalent single conductor resistance (R_{MDCB}), inductance (L_{MDCB}), and capacitance (C_{MDCB}) of MDCB structures are calculated from the parallel sum of RLC of MWCNTs and DWCNTs as shown in equations (3.42-3.44).

$$R_{MDCB} = (R_{MWCNT}^{-1} + R_{DWCNT}^{-1})^{-1} + R_c \quad (3.42)$$

$$L_{MDCB} = (L_{MWCNT}^{-1} + L_{DWCNT}^{-1})^{-1} \quad (3.43)$$

$$C_{MDCB} = C_{MWCNT} + C_{DWCNT} \quad (3.44)$$

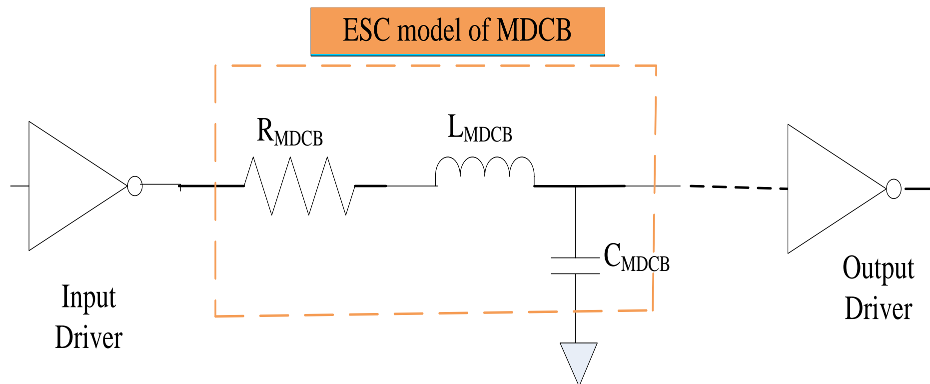


Figure 3.21 ESC model of MDCB interconnects (final stage)

Since the parasitic of long lines is a very big value. So, repeaters are used to model global interconnects at scaled technology nodes. Figure 3.22 shows distributed element model diagram for MDCB interconnects used for simulation in the Tanner tool and determining the delay-dependent performances.

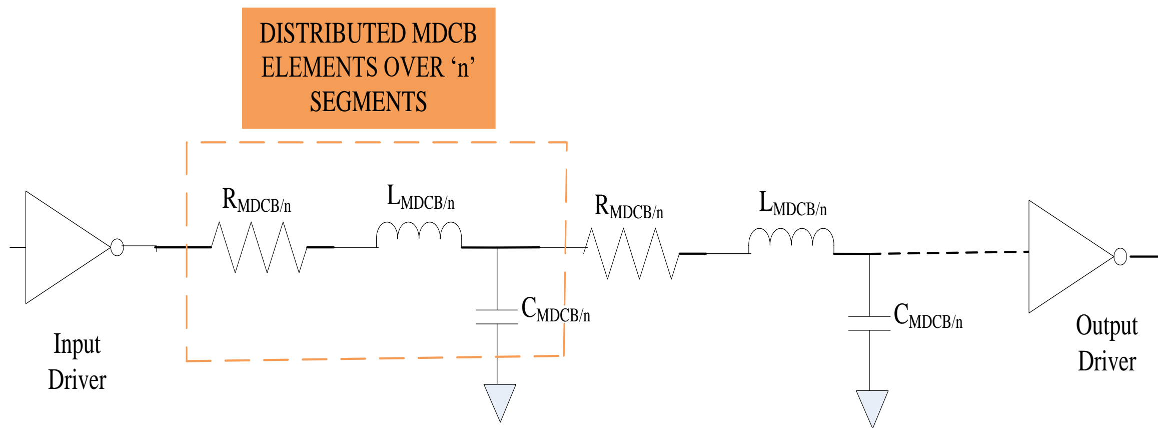


Figure 3.22 Distributed element model used for simulation of MDCB interconnects.

3.3.2 Determination of RLC values of MDCB structures

Based on equations (3.33) -(3.36), the values of resistance, inductance, and capacitance of four MDCB structures are estimated. The outer diameter of Multi-Walled CNT is taken as 8nm and the outer shell diameter of DWCNT is taken as 1.68nm.

The RLC calculated values for 500µm, 1000µm, 1500µm, and 2000µm interconnect lengths at different nanotechnology nodes are formulated with the help of MATLAB tool and are listed in Table 3.5.

Table 3.5 RLC values of Mixed CNT bundle structures at variable lengths (500µm, 1000µm, 1500µm, and 2000µm) for different nanotechnology nodes

		Resistance (kΩ)			Inductance (nH)			Capacitance (pF)		
	Length (µm)	32nm	22nm	16nm	32nm	22nm	16nm	32nm	22nm	16nm
MDCB 1	500	0.80	1.82	4.61	0.93	2.58	14.03	0.11	0.08	0.06
	1000	1.59	3.62	9.17	1.86	5.15	28.06	0.23	0.15	0.11
	1500	2.38	5.43	16.72	2.79	7.73	42.10	0.33	0.22	0.17
	2000	3.18	7.23	22.27	3.72	10.31	56.13	0.44	0.30	0.23
MDCB 2	500	1.15	2.16	6.84	2.66	4.47	8.53	0.35	0.24	0.16
	1000	2.29	4.29	9.63	5.32	8.94	17.05	0.69	0.48	0.33
	1500	3.43	6.43	20.90	7.98	13.41	30.01	0.88	0.67	0.49
	2000	4.57	8.56	27.84	10.63	17.88	40.01	1.18	0.90	0.65
MDCB 3	500	0.83	1.85	5.78	0.97	2.08	5.26	0.43	0.28	0.18
	1000	1.65	3.68	9.56	1.93	4.15	10.52	0.85	0.56	0.37
	1500	2.47	5.51	18.70	2.90	6.23	15.79	1.12	0.80	0.55
	2000	3.29	7.34	25.26	3.87	8.31	21.05	1.50	1.06	0.73

MDCB 4	500	0.91	2.08	4.66	1.05	2.18	5.37	0.20	0.13	0.09
	1000	1.82	4.14	9.29	2.09	4.36	10.75	0.39	0.26	0.18
	1500	2.73	6.21	17.91	3.14	6.55	16.12	0.51	0.37	0.28
	2000	3.64	8.27	24.54	4.18	8.73	21.50	0.69	0.49	0.37

Figure 3.23, figure 3.24, and Figure 3.25 present the results of resistance, inductance, and capacitance values of multi-wall and double-wall CNT bundle structures. The graphs are plotted to compare and develop an understanding of the electrical parasitic of different mixed CNT bundles with different lengths (500µm, 1000µm, 1500µm, and 2000µm) and technologies (32nm, 22nm, and 16nm).

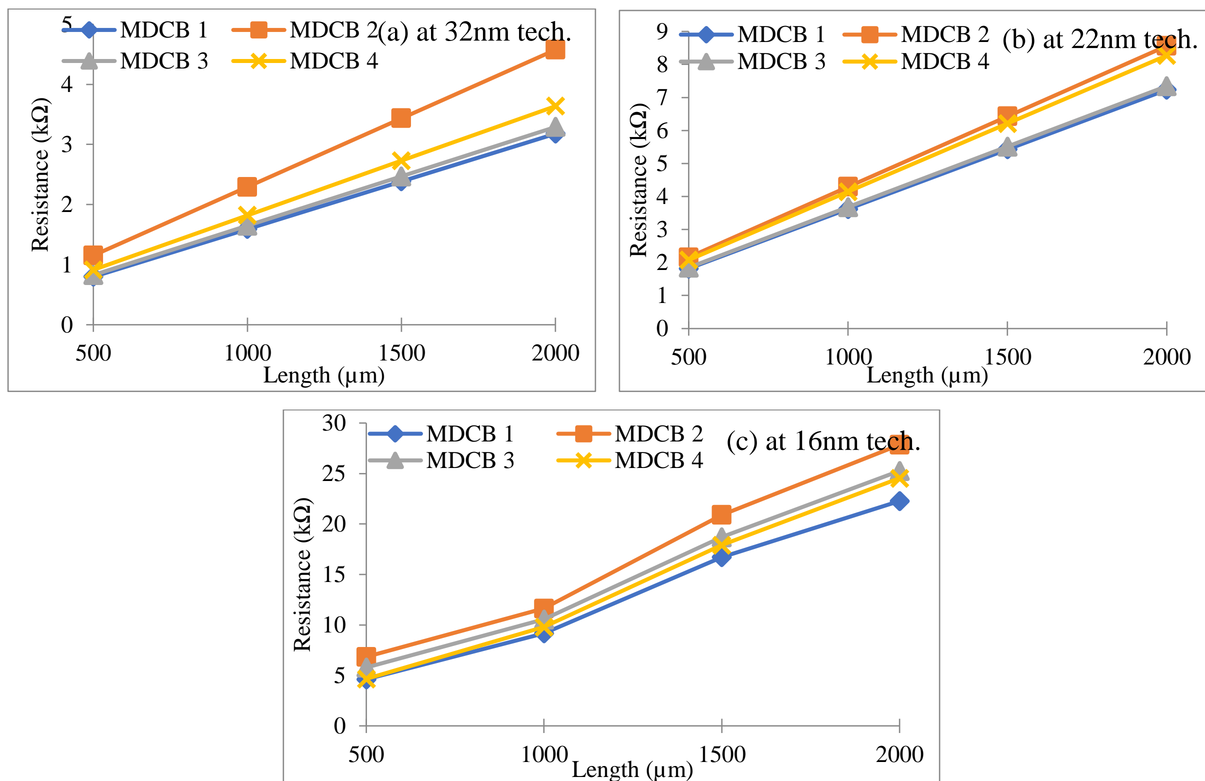
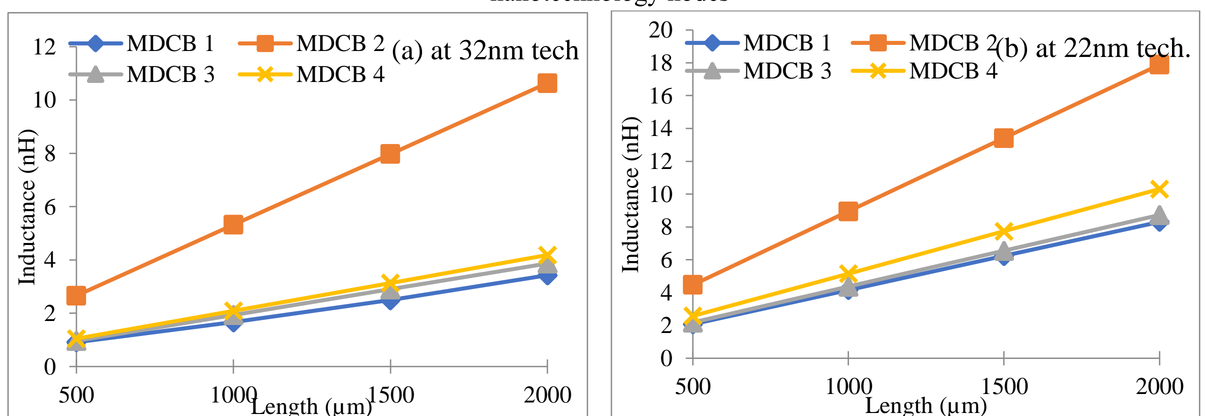


Figure 3.23 Resistance values of MDCB structures for variable global interconnect lengths at different nanotechnology nodes



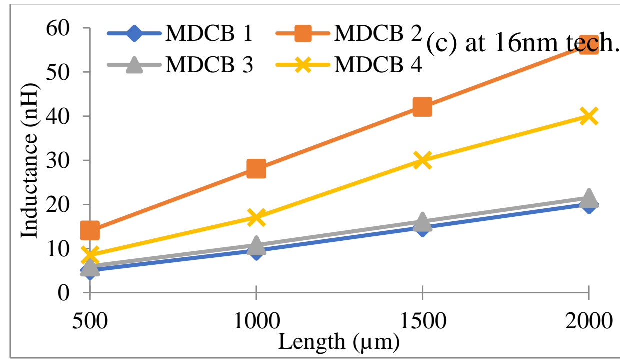


Figure 3.24 Inductance values of MDCB structures for variable global interconnect lengths at different nanotechnology nodes

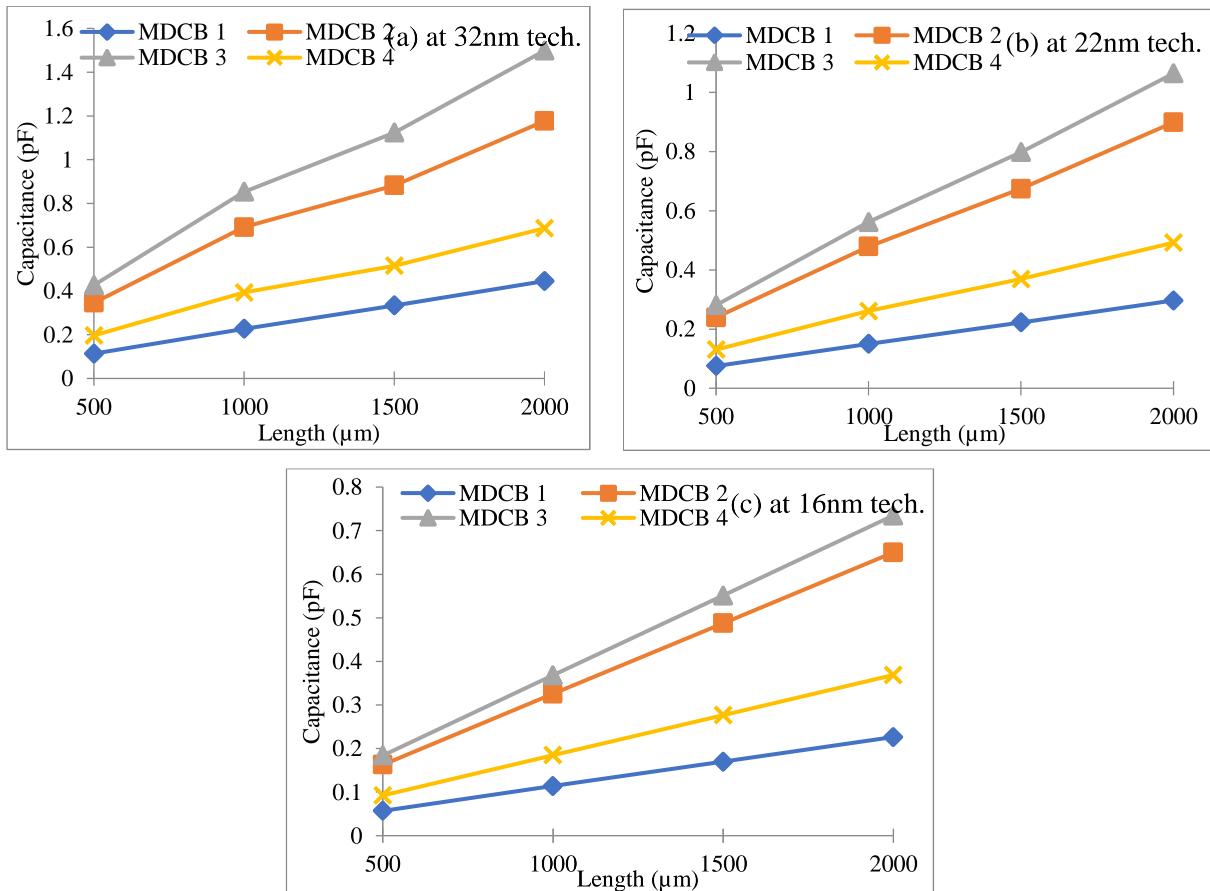


Figure 3.25 Capacitance (pF) values of MDCB structures for variable global interconnect lengths at different nanotechnology nodes

For the variable length of interconnect from 500μm to 2000μm, impedance parameters show a linear relationship. It is revealed from the charts that the MDCB 1 design yields the least value of resistance, inductance, and capacitance at all global lengths and for all technologies than the other three structures. The impedances of MDCB 1 are reduced due to the presence of double shell nanotubes (offer reduced resistance and inductance) in the center and large diameter MWCNTs (offer good conductivity and isolated coupling) at the outer side of the nanotube bundle.

3.4 Delay and PDP-based comparison between MDCB interconnects.

The values of electrical parameters shown in the previous section are put in schematic diagrams and simulations are done to find propagation delay and PDP of the circuits using MDCB (MWCNTs and DWCNTs bundle) material as interconnects. Figure 3.26 and Figure 3.27 present delay and PDP-based performance comparison of four MDCB structures at variable lengths and different technology nodes.

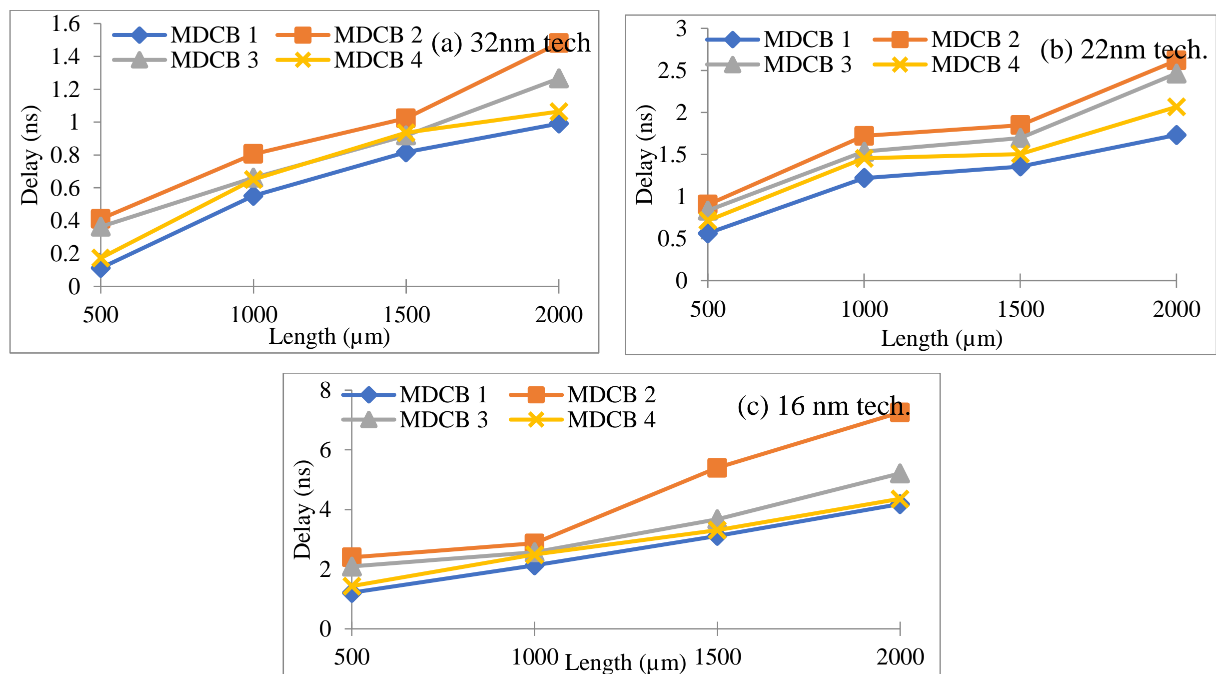


Figure 3.26 Comparison of delay (ns) between different MDCB structures at variable lengths for different nanotechnology nodes

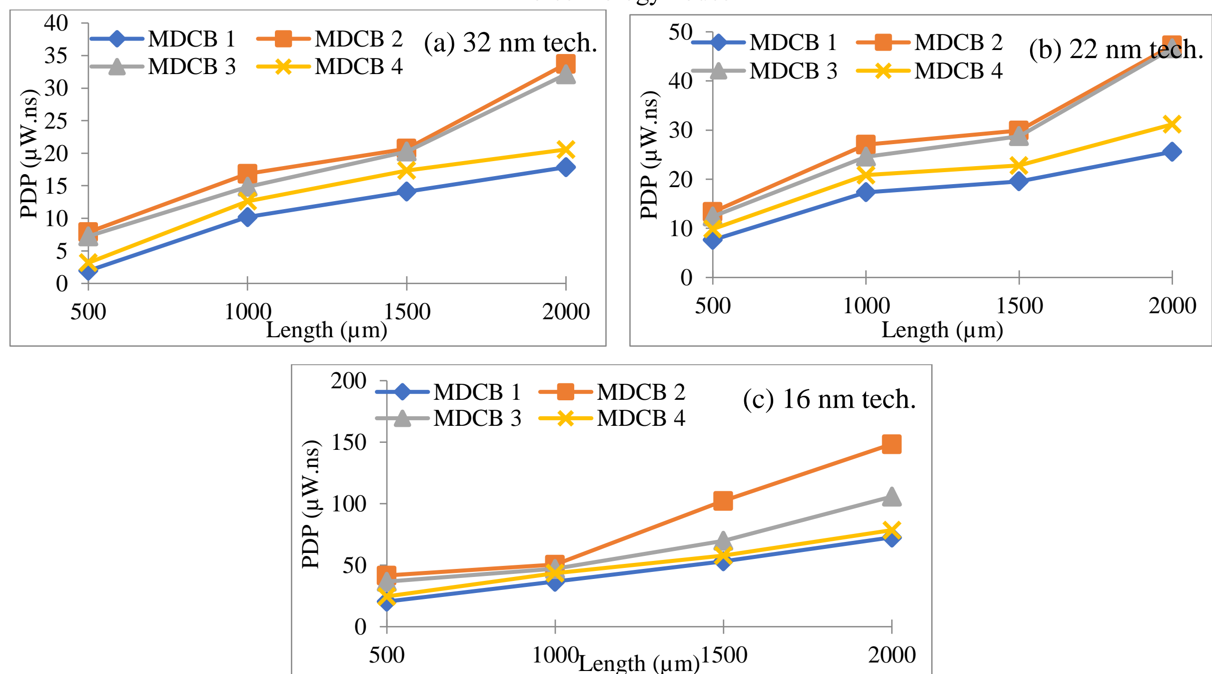


Figure 3.27 Comparison of PDP between different MDCB structures at variable lengths for different nanotechnology nodes

It can be seen from Figure 3.26 (a)-(c) that delay of all mixed CNT bundles upsurges with the rise in length. The delay offered by MDCB 1 structure remains the lowest against all structures at all lengths. The dual shell carbon nanotubes present in the middle of the MDCB 1 design help in attaining minimum resistance and good conductance due to net decreased resistance offered by the parallel addition of inner and outer layer resistances of DWCNTs. This decreased resistance reduces delay, and it helps MDCB 1 structure to become the highest-speed interconnect material with the least PDP among the other three structures at all lengths. Figure 3.28 and Figure 3.29 shows the delay-based performance of four different MDCB interconnects technology-wise at 500µm and 1000µm interconnect lengths.

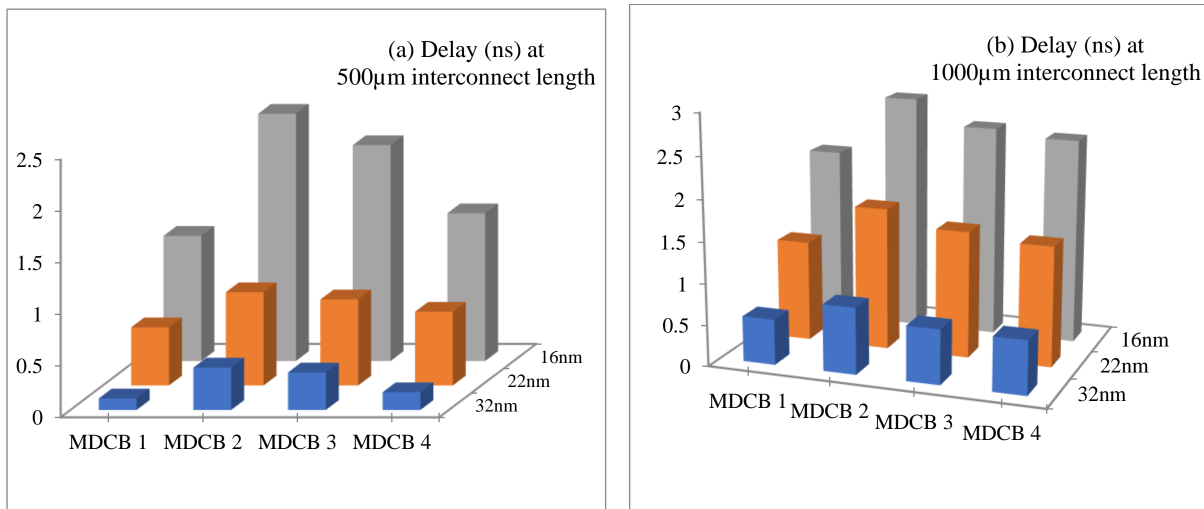


Figure 3.28 Comparison of delay between different MDCB structures at different nanotechnology nodes for (a) 500µm (b) 1000µm

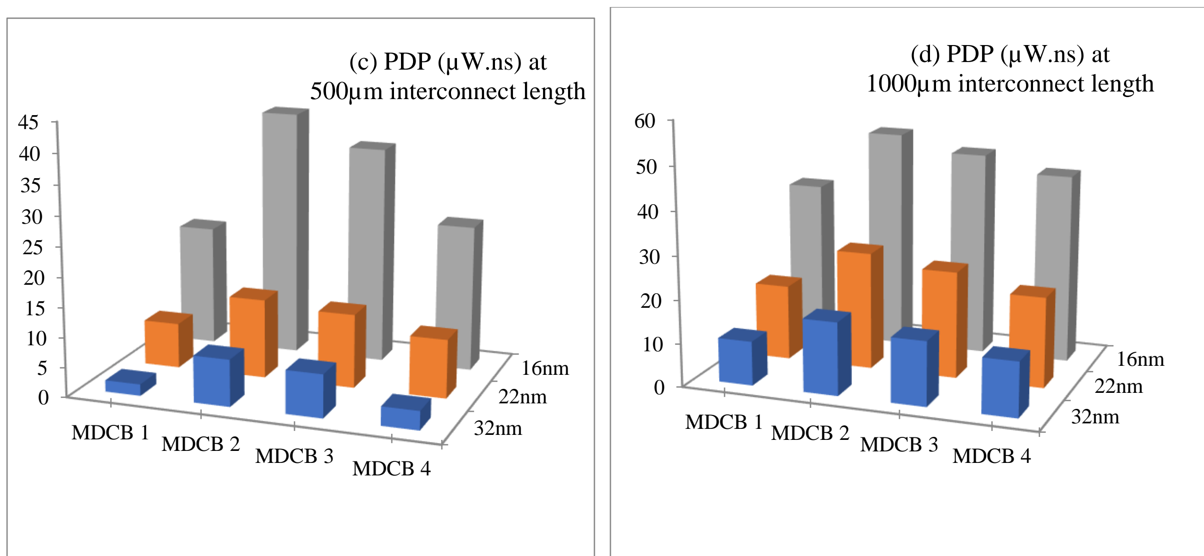


Figure 3.29 Comparison of PDP between different MDCB structures at different nanotechnology nodes for (a) 500µm (b) 1000µm

The presence of multi-wall CNTs and double-layer CNTs in the middle yields minimum delay and PDP than other mixed CNTs. The ratio of delay of CNT increases due to a sharp increase in resistances with scaling at advanced technologies. The performance is also determined by the PDP parameter. MDCB 1 attains the lowest PDP and best results at all lengths than the rest three mixed bundle structures.

3.5 Performance comparison between copper, Single Walled CNT, Multi Walled CNT, Double Walled CNT, and MDCB structures.

The concluding section of the chapter presents the results of the transient analysis performed on interconnect materials like copper, SWCNT, MWCNT, DWCNT, and different MDCB designs. The performance of these materials is decided based on parameters like delay and PDP. Different global interconnect lengths (500μm, 1000μm, 1500μm, and 2000μm) are considered at 32nm, 22nm, and 16nm technology nodes.

3.5.1 Delay-based evaluation.

The corresponding delay readings ($T_{90\%}$) of varied materials are mentioned in Table 3.6. Also, the comparison of this rise time and fall time readings is well plotted in column graphs as shown in Figure 3.30 (a)-(c).

Table 3.6 Delay-based comparison of copper, SWCNT, MWCNT, DWCNT, and MDCB structures at various lengths for different nanotechnology nodes.

Propagation delay (ns) for mixed CNT bundle structures									
	Length (μm)	Copper	SWCNT	MWCNT	DWCNT	MDCB 1	MDCB 2	MDCB 3	MDCB 4
32nm	500	1.06	0.92	0.49	0.50	0.11	0.41	0.36	0.17
	1000	1.95	1.75	0.74	0.73	0.55	0.81	0.66	0.65
	1500	2.96	2.26	0.97	0.99	0.82	1.02	0.92	0.94
	2000	3.99	3.52	1.25	1.27	0.99	1.48	1.27	1.06
22nm	500	2.23	1.18	0.74	0.93	0.56	0.90	0.83	0.71
	1000	4.18	2.08	1.17	1.55	1.22	1.72	1.53	1.45
	1500	6.40	3.32	1.57	2.21	1.36	1.85	1.70	1.51
	2000	8.86	4.98	2.07	2.84	1.73	2.62	2.46	2.07
16nm	500	6.47	1.72	1.31	1.96	1.21	2.40	2.09	1.43
	1000	12.90	3.41	2.20	3.46	2.13	2.87	2.57	2.49
	1500	19.46	5.15	3.02	5.03	3.12	5.40	3.68	3.31
	2000	27.26	7.59	3.94	6.33	4.18	7.26	5.21	4.36

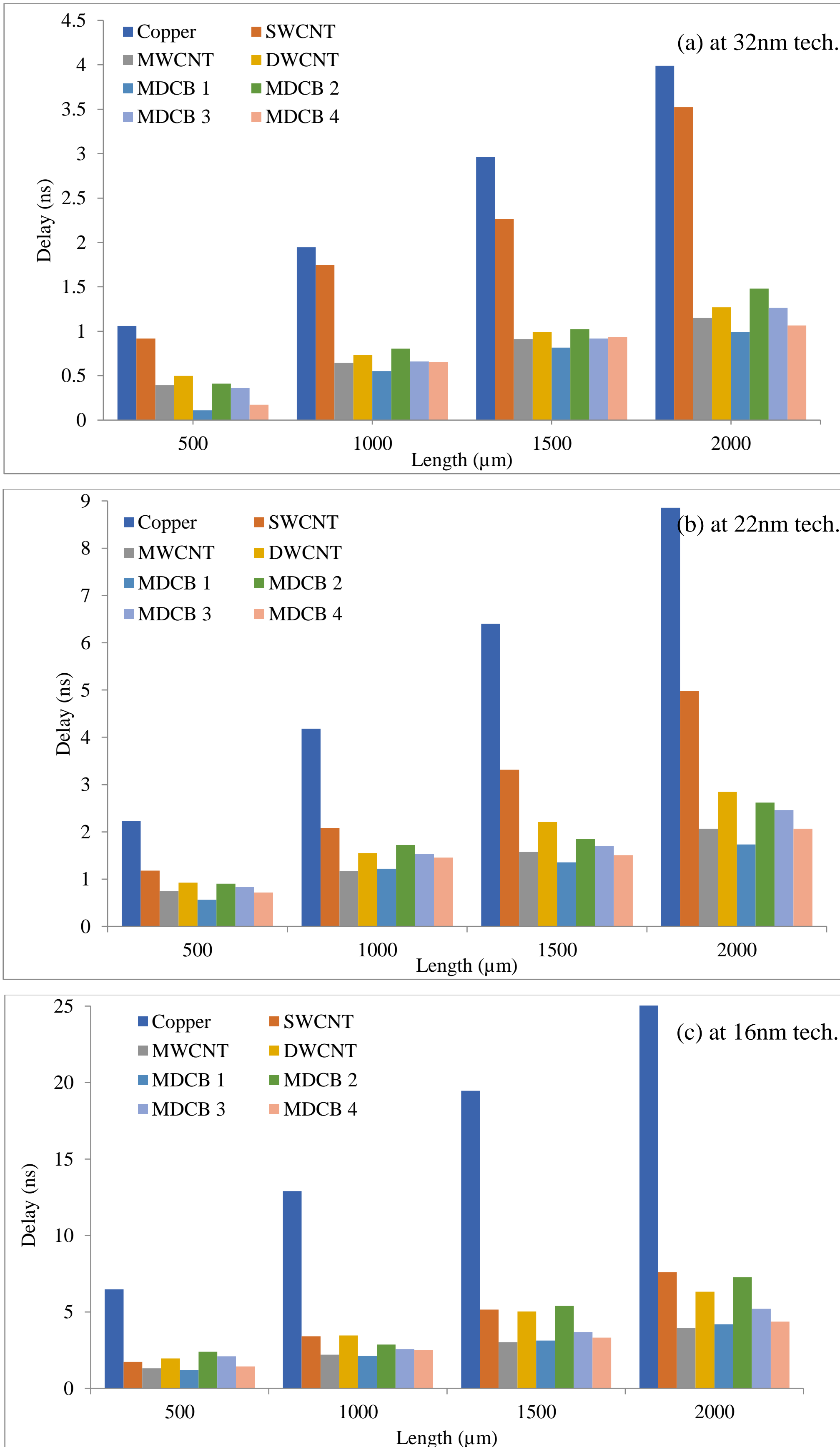


Figure 3.30 Delay comparisons between copper, SWCNT, MWCNT, DWCNT, and different MDCB structures at different global lengths for different nanotechnology nodes

The delay readings of MDCB structures are compared with their isolated counterparts (MWCNT and DWCNT bundles) at different lengths. Due to high resistance and other serious issues in copper, it exhibits maximum delay than carbon nanotube structures. Out of all CNT materials, MDCB 1 structure shows minimum delay. It is developed by joining the finest properties of its constituent CNTs. As evident from Figure 3.30 large diameter MWCNTs at the outer boundary and double-shell CNTs in the middle of the design when put together results in the best conductance and high-speed VLSI circuit at nano-regime nodes.

3.5.2 PDP-based results.

The efficiency of the integrated circuit is also decided by the figure of the merit parameter. The PDP-based results of various interconnect materials are listed in Table 3.7 and are plotted with the help of column charts shown in Figure 3.31.

Table 3.7 PDP-based comparison of copper, SWCNT, MWCNT, DWCNT, and MDCB structures at various lengths for different nanotechnology nodes.

PDP (µW.ns) for mixed CNT bundle structures									
	Length (µm)	Copper	SWCNT	MWCNT	DWCNT	MDCB 1	MDCB 2	MDCB 3	MDCB 4
32nm	500	23.59409	13.07976	6.84713	5.945553	1.94	7.86	7.25	3.17
	1000	71.14997	26.33124	12.41767	9.485986	10.19	16.82	14.83	12.62
	1500	123.765	44.05091	17.54784	13.67231	14.09	20.70	20.25	17.34
	2000	245.5967	65.79427	25.75867	18.65962	17.85	33.71	32.12	20.57
22nm	500	25.45187	22.22038	9.017303	10.13462	7.63	13.33	12.41	9.86
	1000	52.123	41.10257	16.08079	17.67617	17.35	27.02	24.60	20.83
	1500	88.45688	60.04276	23.15439	26.21517	19.57	29.91	28.74	22.79
	2000	137.5294	102.2731	33.50753	35.21091	25.58	47.20	46.66	31.17
16nm	500	100.3493	32.70867	20.24146	29.18035	20.45	41.67	36.66	24.65
	1000	222.4143	80.31821	36.28857	52.48643	36.62	50.52	47.09	43.57
	1500	384.934	148.4248	51.57219	78.23784	53.21	102.24	69.86	57.94
	2000	626.1674	258.1239	71.32207	100.9782	72.65	148.43	105.76	78.51

Carbon nanotubes prove themselves as an excellent substitute for copper for 32nm technology and beyond. SWCNTs face chirality and fabrication problems. MDCB 1 design with large diameter multi-shell CNTs at edges of the design faces the least coupling effects and therefore with minimum delay, it also gives minimum power. So, MDCB 1 interconnect achieves the least value of the power-delay product parameter resulting in the best results than all other

interconnects as shown in Figure 3.31. The results are even better than only MWCNT and only DWCNT bundle structures.

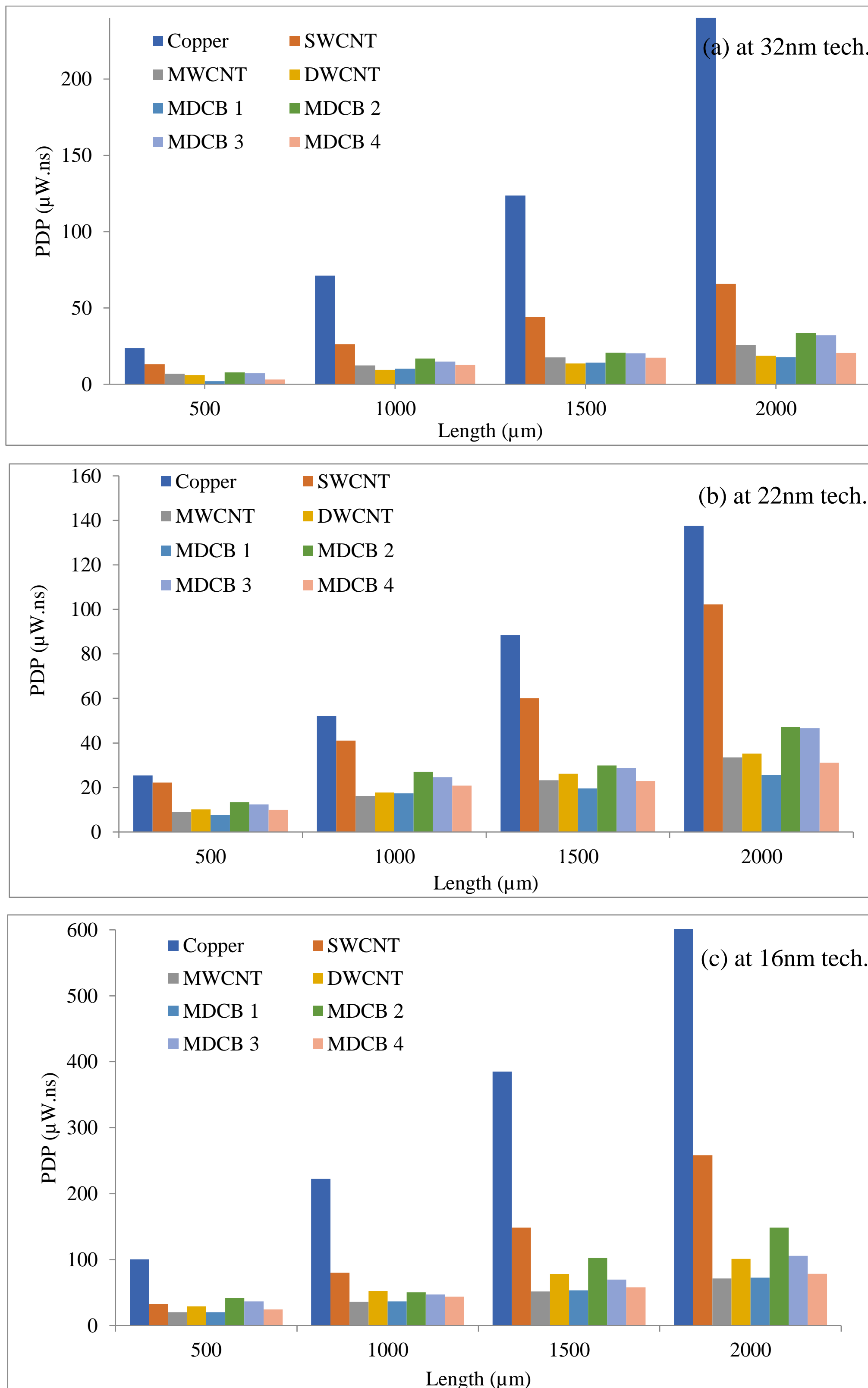


Figure 3.31 PDP comparison between copper, SWCNT, MWCNT, DWCNT, and different MDCB structures at different global lengths for different nanotechnology nodes

3.6 Chapter Summary and Contribution

The chapter presents an overview of various materials employed as VLSI interconnects. Their structures, electrical schematics, and RLC equations are well presented with proper explanations. Using these mathematical computations, the values of impedance are used to determine the transient behavior of interconnects at various global lengths and technology nodes. Results displayed in the chapter indicate that for global interconnect lengths delay and PDP plays an important role in deciding circuit performance. The delay shows a direct relationship with the length of interconnects. When the length of interconnect rises, the delay rises significantly, and the ratio of increased delay increases sharply at scaled nodes. This is because of technology scaling and surged resistance of interconnects. Copper encounters fatal issues at and beyond 32nm. So, the VLSI interconnect market moves to CNTs (with excellent conductance, and good thermal and mechanical stability) for promising results. Thus, SWCNTs, MWCNTs, and DWCNTs show better results than copper. Metallic SWCNTs are only useful as interconnects and face issues during fabrication. DWCNTs with double layers and reduced resistance give less resistance and delay than SWCNTs. Various mixed CNT bundle structures are developed by combining good properties of MWCNTs and DWCNTs. Their comparison is made with existing materials concerning delay and PDP. It is concluded that MDCB 1 structure outperforms all other types of interconnect materials. The least resistance, good conductance, and less delay of DWCNTs in the center and reduced coupling of MWCNTs at edges combine to yield the best results at semi-global and global lengths. MDCB 1 structure becomes a promising interconnect material candidate for coming generations.

Related Publications:

1. Gurleen Dhillon and Karmjit Singh Sandha, "Mixed CNT bundles as VLSI interconnects for nanoscale technology nodes," *Journal of Computational Electronics*, vol. 20, no.1, pp. 248-258, 2021. *(Impact Factor- 1.983)* (SCI indexed)
2. Karmjit Singh Sandha and Gurleen Dhillon, "Impact of Variable Interconnect length on the performance of MWCNT as VLSI Interconnect for Nanometer Integrated Circuit Design," *International Journal of Engineering and Advanced Technology (IJEAT)* 8.5 (2019): 2209-2214. (Scopus indexed)

4. TEMPERATURE-DEPENDENT MODELING OF MIXED CNTS

It is essential to know the electrical behavior of high-performance integrated circuits from the thermal issues point of view. With the thermal variations in the working condition of ICs, the performance of IC deviates due to temperature-dependent phenomena eased scaling and rise in temperature plays an indispensable role in evaluating the performance of circuits. Several scatterings are seen in devices that tend to hit their performance by decreasing their mean free paths. The upcoming sections present various electron scattering phenomena that help in deciding the actual MFP of electrons in nanotubes [66,86-97]. In this chapter, temperature-dependent simulations are performed to find out temperature-sensitive delay and PDP results for various interconnect materials.

4.1 Temperature-dependent MFP of CNTs

The optical absorption and optical emission endow scattering which acts as an indispensable factor in deciding (MFP) (λ) of graphitic-based nanotubes [87]. At lower temperatures, primarily acoustic scattering (λ_{AC}) (due to the vibrational sound of phonons) in CNTs help in determining MFPs and is expressed by equation (4.1) where graphitic-based, $D_0=1.8nm$, D_i is the diameter of ith shell, $T_0=300K$ and T is operating temperature in kelvin.

$$\lambda_{AC} = 890.D_i(\frac{T_0}{T}) \tag{4.1}$$

At higher temperatures, electrons are influenced under an electric field and attain enough energy to climb up to the optical phonon state ($N_{OP}(T)$). The expression for optical phonon state (energy state of phonon) is given by equation (4.2).

$$N_{OP}(T) = \frac{1}{[exp(h\Omega/K_BT)-1]} \tag{4.2}$$

Where K_B is the Boltzmann constant and the value of $h\Omega$ is taken as 0.16eV. The optical absorption length $(\lambda)_{OP,abs}$ with $(\lambda)_{OP,300}=15nm$ is given by expression (4.3) [92].

$$(\lambda)_{OP,abs}(T) = (\lambda)_{OP,300}\frac{D_i}{D_0}\frac{N_{OP(300)}+1}{N_{OP(T)}} \tag{4.3}$$

After crossing the threshold optical energy level, electrons suffer inelastic emission. So, the optical field emission $(\lambda)_{OP,emsfld}$ (related to the emission of phonon) is given by expression (4.4).

$$(\lambda)_{OP,emsfld}(T) = \frac{(h\Omega_{OP} - K_B T)}{qV/L} + (\lambda)_{OP,300} \frac{D_i}{D_0} \frac{N_{OP}(300)+1}{N_{OP}(T)+1} \quad (4.4)$$

Electrons also travel a specific distance after attaining optical energy and before the emission of phonons and lead to optical field absorption scattering and are expressed by equation (4.5).

$$(\lambda)_{OP,emsabs(T)} = (\lambda)_{OP,abs}(T) + (\lambda)_{OP,300} \frac{D_i}{D_0} \frac{N_{OP}(300)+1}{N_{OP}(T)} \quad (4.5)$$

Both optical field emission and optical field absorption scattering adds to give the resultant optical inelastic emission mean free path $(\lambda)_{OP,\ ems}$ and is calculated by equation (4.6) [94].

$$(\lambda)_{OP,ems} = \left(\frac{1}{(\lambda)_{OP,emsfld}} + \frac{1}{(\lambda)_{OP,emsabs}}\right)^{-1} \quad (4.6)$$

The cumulative sum of elastic acoustic scattering, inelastic optical emission scattering, and inelastic absorption scattering helps in yielding the final thermally aware effective MFP (λ_{eff}) and is calculated by equation (4.7) and represented in Figure 4.1 [87].

$$(\lambda)_{eff} = ((\lambda)_{AC}^{-1} + (\lambda)_{OP,ems}^{-1} + (\lambda)_{OP,abs}^{-1})^{-1} \quad (4.7)$$

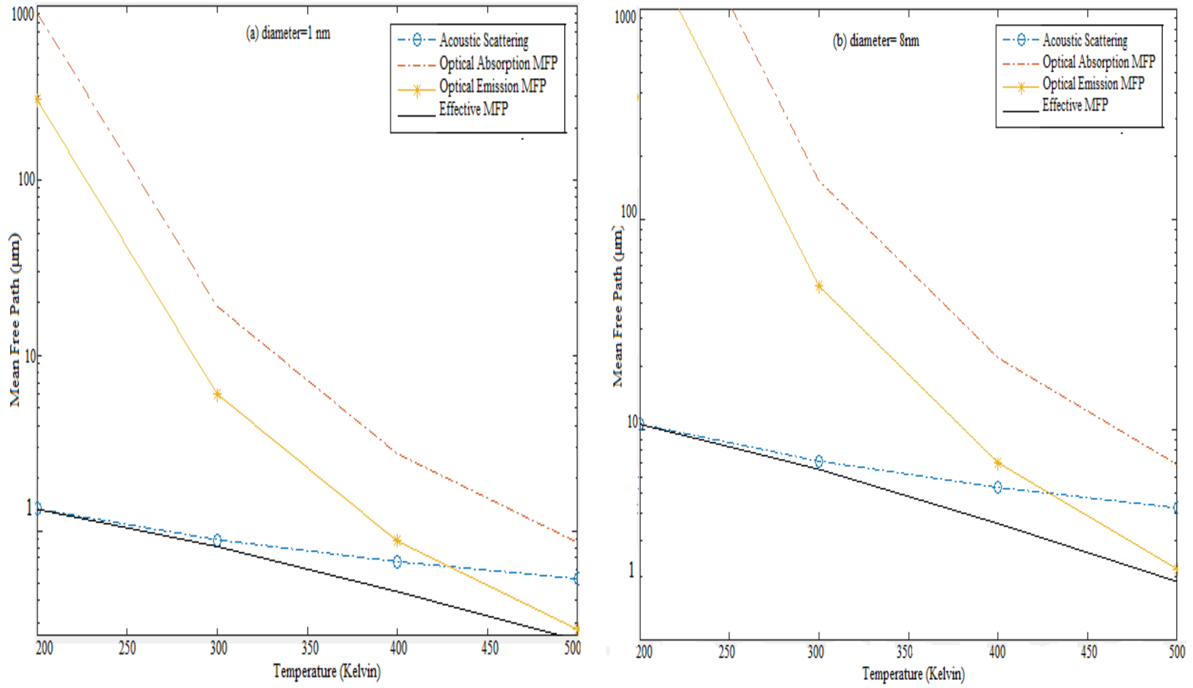


Figure 4.1 Temperature-dependent acoustic, optical absorption, emission, and effective MFP of electrons for (a) d=1nm (b) d=8nm

MFP of electrons depends upon the diameter and temperature. It can be seen from Figure 4.1 that acoustic MFPs play a significant role at lower temperatures, and it predominantly reduces net MFP. With further temperature rise, both optical emission and optical absorption MFP also decrease gradually and can't be ignored and then plays an important role in deciding MFP. As mentioned in equation (4.7), all these factors sum up to decide net the value of the MFP of

CNTs. Further, MFPs are also dependent upon the diameter of nanotubes. For reference, it can be studied from the plot obtained in MATLAB from Figure 4.1 that with a larger diameter (assumed 8nm, for MWCNT), the MFP of conducting electrons is more than that smaller diameter (assumed 1nm, DWCNT) at 22nm technology node. But with the increase in temperature, the trend of decreasing MFP holds. Since the resistance of carbon nanotube bundles shows an increase with temperature. The effect of temperature and effective MFP becomes important to determine the performance of interconnects [92].

4.2 Temperature-based delay and PDP results

This section focuses on the transient analysis of various interconnect materials at three nano-technology nodes. The effective mean free path determined from equation (4.7) helps to find the exact temperature-dependent resistance of carbon nanotubes. The simulation is done to find out the propagation delay and PDP readings of copper, SWCNT, DWCNT, MWCNT, and MDCB structures including the effect of temperature.

4.2.1 Performance of copper, SWCNT, DWCNT, and MWCNT at 500µm and 1000µm length

As learned from the previous section, different types of scattering contribute to deciding the final MFP of conducting electrons at different thermal points. The table lists temperature-dependent values of copper, single-wall CNT bundle, double-wall CNT bundle and, multi-wall carbon nanotube bundle for 500µm and 1000µm interconnect lengths at 32nm, 22nm and, 16nm technologies. For better comparison between copper and basic types of carbon nanotube bundles these values are plotted as line charts and presented in Figure 4.2-4.4.

Table 4.1 Temperature sensitive delay (ns) of copper, SWCNT, DWCNT, and MWCNT for 500µm and 1000µm interconnect lengths at various nanotechnology nodes

Temp (K)	200	250	300	350	400	450	500	200	250	300	350	400	450	500
	At 500µm							At 1000µm						
At 32nm technology														
COPPER	0.89	0.95	1.07	1.26	1.41	1.56	1.72	1.60	1.78	2.00	2.31	2.61	2.90	3.19
SWCNT	0.85	0.90	0.98	1.04	1.19	1.36	1.60	1.48	1.61	1.87	2.08	2.48	2.79	3.08
DWCNT	0.43	0.44	0.48	0.51	0.52	0.55	0.58	0.61	0.63	0.68	0.75	0.80	0.85	0.90
MWCNT	0.48	0.48	0.51	0.56	0.59	0.64	0.74	0.68	0.70	0.82	0.89	0.96	1.09	1.27
At 22nm technology														
COPPER	1.54	1.82	2.22	2.65	2.98	3.38	3.70	2.75	3.51	4.18	5.07	5.74	6.40	7.23
SWCNT	1.11	1.17	1.30	1.44	1.68	2.03	2.46	2.05	2.24	2.49	2.93	3.51	4.13	5.28
DWCNT	0.64	0.65	0.69	0.76	0.76	0.83	0.87	0.89	0.96	1.14	1.25	1.42	1.58	1.65
MWCNT	0.83	0.88	1.03	1.12	1.20	1.37	1.59	1.36	1.47	1.75	1.95	2.10	2.45	2.91

At 16nm technology														
COPPER	4.29	5.41	6.48	7.89	9.09	10.08	11.07	8.19	10.83	12.90	15.61	17.28	18.93	21.62
SWCNT	1.48	1.68	1.98	2.37	2.83	3.54	4.52	3.02	3.32	3.96	4.50	5.53	7.60	10.03
DWCNT	1.02	1.06	1.18	1.33	1.35	1.57	1.66	1.58	1.78	1.99	2.19	2.47	2.73	3.04
MWCNT	1.28	1.52	1.88	2.22	2.63	3.08	3.58	2.83	3.02	3.56	4.04	4.82	5.66	6.72

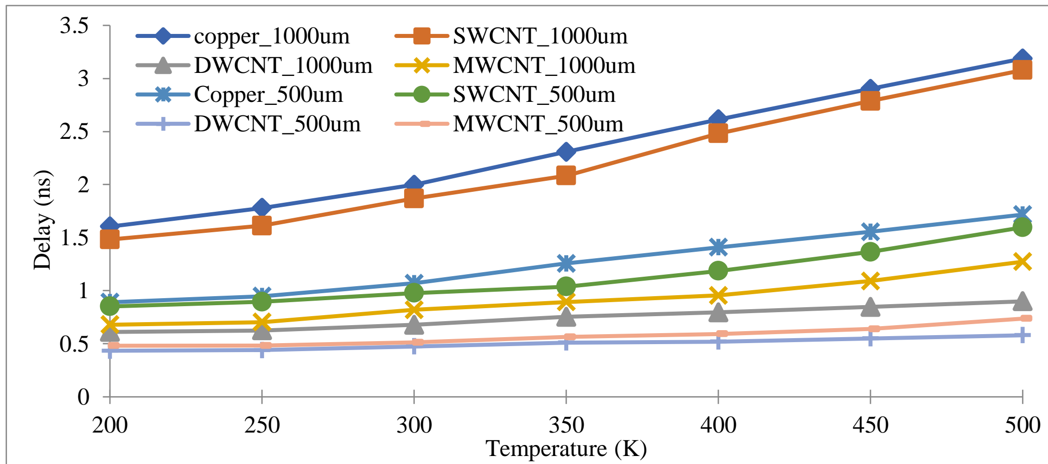


Figure 4.2 Temperature sensitive delay (ns) of copper, SWCNT, DWCNT, and MWCNT for 500µm and 1000µm interconnect length at 32nm technology node

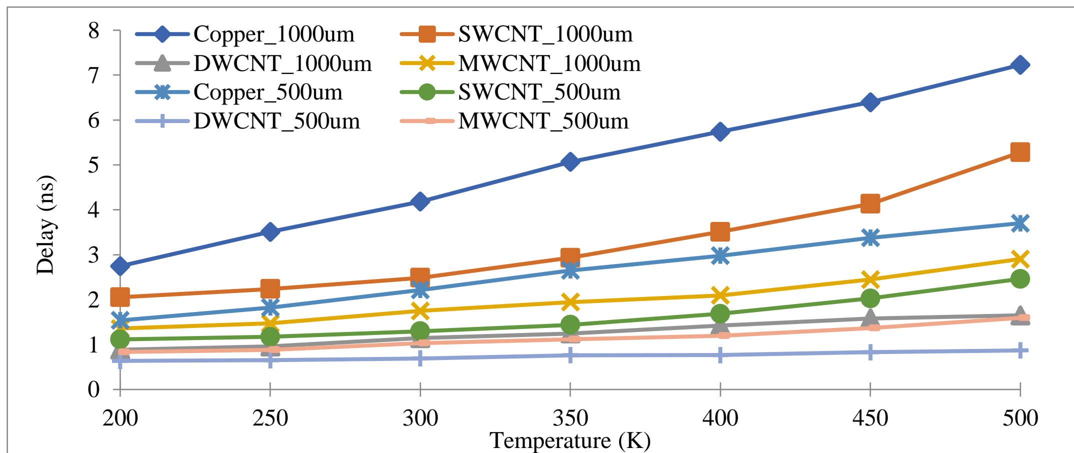


Figure 4.3 Temperature sensitive delay (ns) of copper, SWCNT, DWCNT, and MWCNT for 500µm and 1000µm interconnect length at 22nm technology node

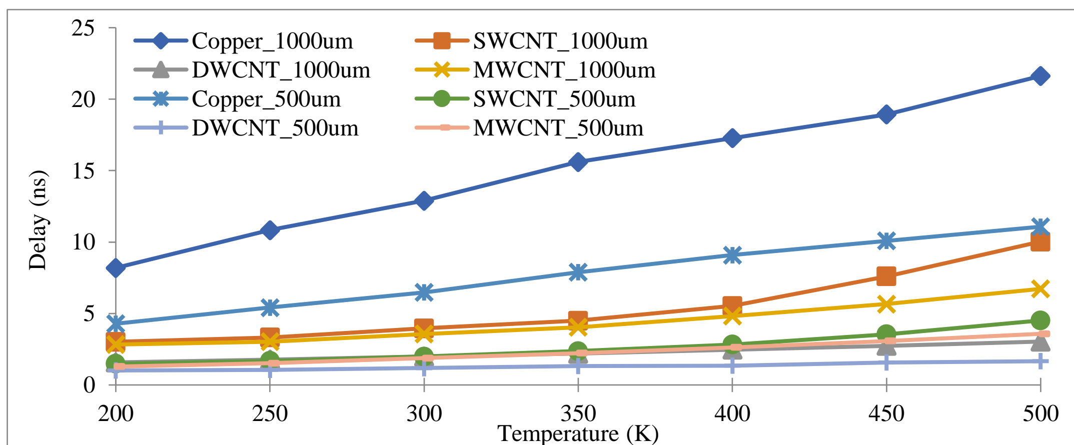


Figure 4.4 Temperature sensitive delay (ns) of copper, SWCNT, DWCNT, and MWCNT for 500µm and 1000µm interconnect length at 16 nm technology node

As concluded in the last chapter delay shows a direct relationship with the length of interconnect and scaling of technology nodes. The values in the table indicate that with the rise in temperature from 200K-500K for global lengths the delay of the circuit increases. It can be well read from figures that beyond the 32nm technology node, the delay of copper increases drastically because of its increased resistance (due to electromigration and surface scattering effects). The delay of interconnect material for larger length i.e., 1000μm is more than that at 500μm. This is because the parasitic increases with the interconnect lengths. CNTs possess very good conduction properties with excellent mechanical and thermal strength. However, with scaling, the count of tubes in a bundle decreases, so it can be said that both scaling and other scatterings due to temperature contribute to increasing the resistance of nanotubes as well. This ultimately led to an increase in propagation delay.

DWCNTs (outermost diameter taken as 1.68nm) show the least delay than copper and other CNTs. This is due to the presence of a double shell structure and its reduced resistance. Large-diameter MWCNTs (D_{max} ~8nm) also show better results than copper and SWCNTs. This holds for all lengths, temperature points, and technology nodes. Table 4.2 indicates temperature-dependent PDP values of various technology nodes. Figure 4.5-4.7 presents a line chart comparison of temperature-dependent values of interconnects at different technology nodes.

Table 4.2 Temperature sensitive PDP (μW.ns) of copper, SWCNT, DWCNT, and MWCNT for 500μm and 1000μm interconnect lengths at various nanotechnology nodes

Temp (K)	200	250	300	350	400	450	500	200	250	300	350	400	450	500
At 500μm								At 1000μm						
At 32nm technology														
COPPER	11.01	11.76	13.29	15.64	17.59	19.47	21.53	23.67	25.16	27.20	31.55	35.95	40.10	44.38
SWCNT	9.91	10.96	11.99	13.64	16.09	17.47	19.53	21.50	22.96	25.17	26.82	30.77	35.40	41.76
DWCNT	6.04	6.12	6.61	7.11	7.24	7.67	8.08	7.15	7.70	9.31	10.58	11.28	11.75	13.44
MWCNT	6.77	6.98	7.15	7.80	8.14	8.73	8.98	9.78	10.09	11.56	12.54	13.37	14.14	16.59
At 22nm technology														
COPPER	20.98	23.68	27.95	33.31	38.11	42.60	47.75	34.50	44.16	52.59	63.80	72.22	80.49	91.21
SWCNT	17.54	20.86	25.43	30.46	34.42	39.12	42.86	33.13	42.41	50.49	61.27	69.35	77.94	87.60
DWCNT	7.69	7.89	8.36	9.22	9.26	10.06	10.55	12.14	13.14	15.72	17.18	19.62	21.90	22.87
MWCNT	9.14	9.65	11.30	12.31	13.16	15.05	17.52	15.47	16.70	19.97	22.21	23.96	28.11	33.51
At 16nm technology														
COPPER	65.97	83.65	100.88	123.67	143.35	159.97	177.05	128.37	169.38	201.82	244.64	271.11	297.05	338.01
SWCNT	28.04	31.91	37.56	45.05	54.19	68.74	89.00	70.71	78.17	93.72	108.45	137.04	165.86	194.69
DWCNT	15.70	16.47	18.27	20.54	20.84	24.39	25.80	26.38	29.67	33.22	36.68	41.48	45.69	50.98
MWCNT	19.15	22.70	28.01	33.06	39.22	45.91	53.44	42.27	45.25	53.12	59.85	72.02	83.83	99.55

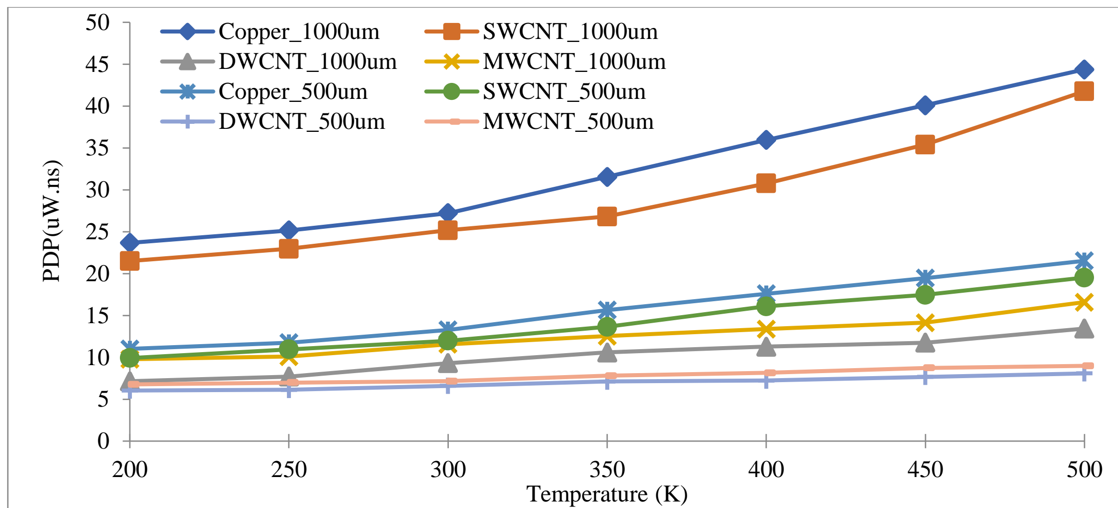


Figure 4.5 Temperature sensitive PDP (μW.ns) of copper, SWCNT, DWCNT and MWCNT for 500μm and 1000μm interconnect length at 32nm technology node

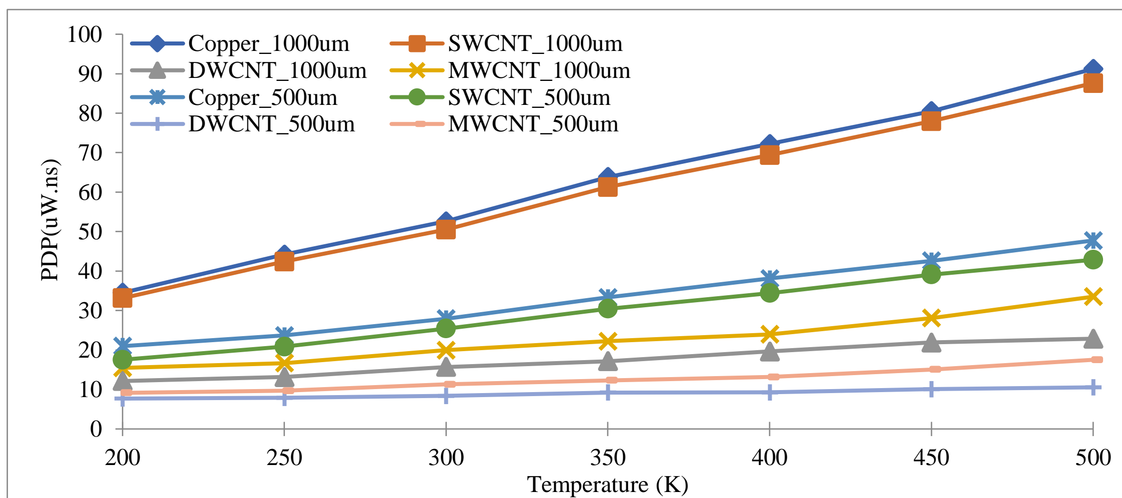


Figure 4.6 Temperature sensitive PDP (μW.ns) of copper, SWCNT, DWCNT and MWCNT for 500μm and 1000μm interconnect length at 22nm technology node

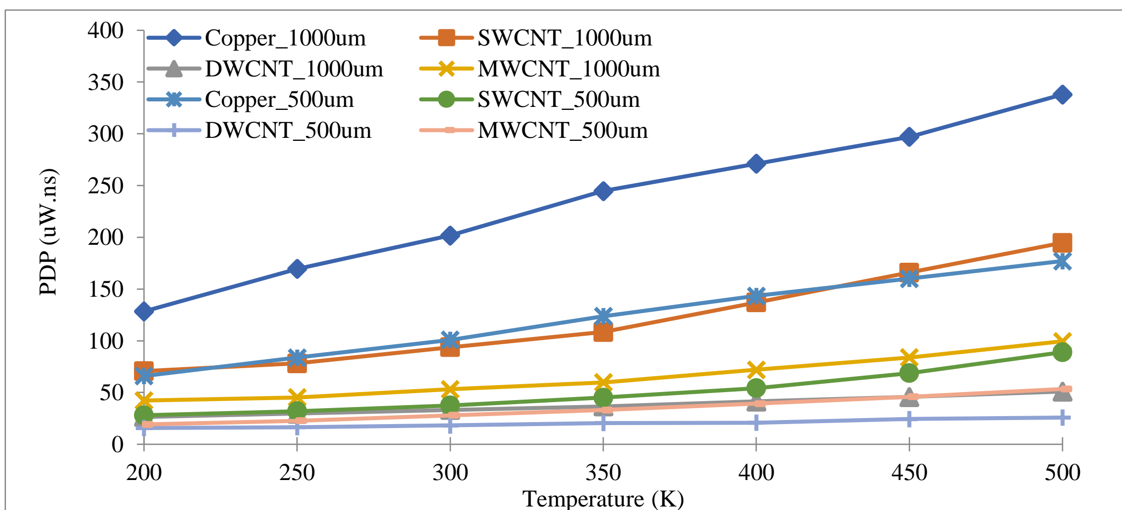


Figure 4.7 Temperature sensitive PDP (μW.ns) of copper, SWCNT, DWCNT and MWCNT for 500μm and 1000μm interconnect length at 16nm technology node

Signal delay and power are incorporated with the variation in temperature and length in the figures above to determine their overall performance. Carbon nanotubes can successfully replace copper interconnect material beyond 32nm nodes at the global length of interconnects. It can also be concluded from the graphs of the figure of merit parameter i.e., PDP values of double-wall perform the best than the other three interconnect materials (copper, SWCNT, and MWCNT) by attaining minimum value at all VLSI technology nodes and can be utilized as interconnection material for future nodes.

4.2.2 Performance of various MDCB structures at 500µm and 1000µm length

The simulated temperature-dependent delay and PDP values for MDCB (1-4) at various nano-regime nodes are mentioned in Table 4.3 and Table 4.4 respectively.

As listed in Table this increase in delay with temperature due to various scatterings can significantly impact the performance of integrated circuits [114]. The closed comparison in terms of temperature-dependent delays between four MDCB structures is made and is also presented with the help of line charts in Figure 4.8-4.10.

Table 4.3 Temperature sensitive delay (ns) of MDCB structures for 500µm and 1000µm interconnect lengths at various nanotechnology nodes

Temp (K)	200	250	300	350	400	450	500	200	250	300	350	400	450	500
	At 500µm							At 1000µm						
At 32nm technology														
MDCB1	0.07	0.07	0.10	0.11	0.16	0.21	0.28	0.37	0.39	0.43	0.53	0.64	0.75	0.79
MDCB2	0.32	0.37	0.41	0.51	0.58	0.63	0.73	0.70	0.74	0.77	0.85	0.94	1.02	1.20
MDCB3	0.19	0.24	0.30	0.40	0.46	0.52	0.59	0.56	0.60	0.64	0.67	0.72	0.82	0.90
MDCB4	0.10	0.13	0.18	0.21	0.30	0.37	0.45	0.51	0.51	0.61	0.72	0.81	0.90	1.02
At 22nm technology														
MDCB1	0.51	0.66	0.72	0.77	0.85	0.94	1.13	0.58	0.78	0.96	1.05	1.20	1.37	1.43
MDCB2	0.74	0.83	0.96	1.09	1.18	1.29	1.43	1.14	1.24	1.33	1.43	1.57	1.79	2.21
MDCB3	0.69	0.72	0.77	0.88	0.99	1.15	1.29	0.96	1.07	1.19	1.25	1.38	1.52	1.70
MDCB4	0.64	0.68	0.74	0.82	0.92	1.00	1.17	1.06	1.15	1.23	1.37	1.45	1.60	1.85
At 16nm technology														
MDCB1	1.16	1.24	1.46	1.74	1.87	2.04	2.13	1.33	1.47	1.61	1.81	2.11	2.23	2.63
MDCB2	1.55	2.00	2.12	2.31	2.46	2.57	2.85	2.51	2.76	3.36	3.91	4.38	5.28	6.15
MDCB3	1.48	1.56	1.74	1.90	1.98	2.16	2.36	1.77	1.80	2.15	2.58	2.96	3.47	3.98
MDCB4	1.32	1.36	1.55	1.94	2.15	2.36	2.59	1.86	2.07	2.23	2.38	2.61	3.09	3.78

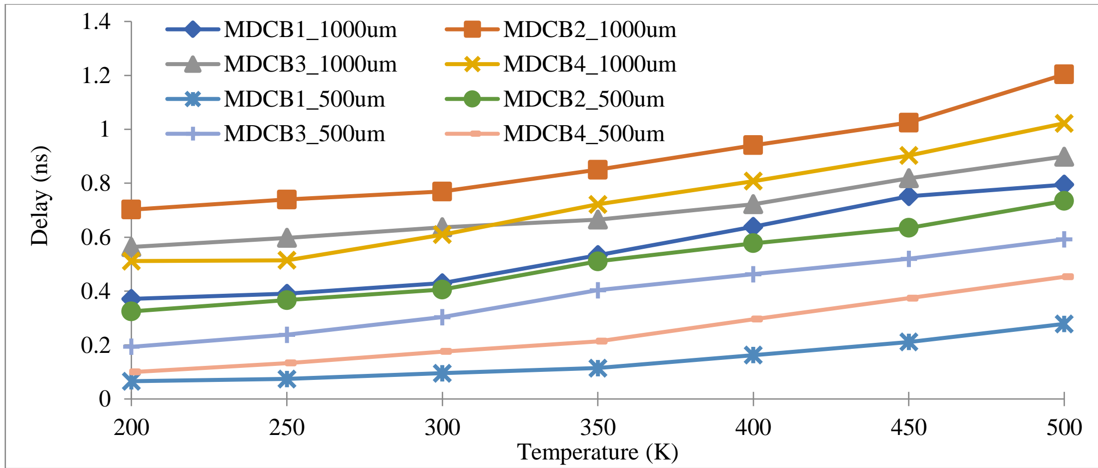


Figure 4.8 Temperature sensitive delay (ns) of MDCB structures for 500μm and 1000μm interconnect length at 32nm technology node

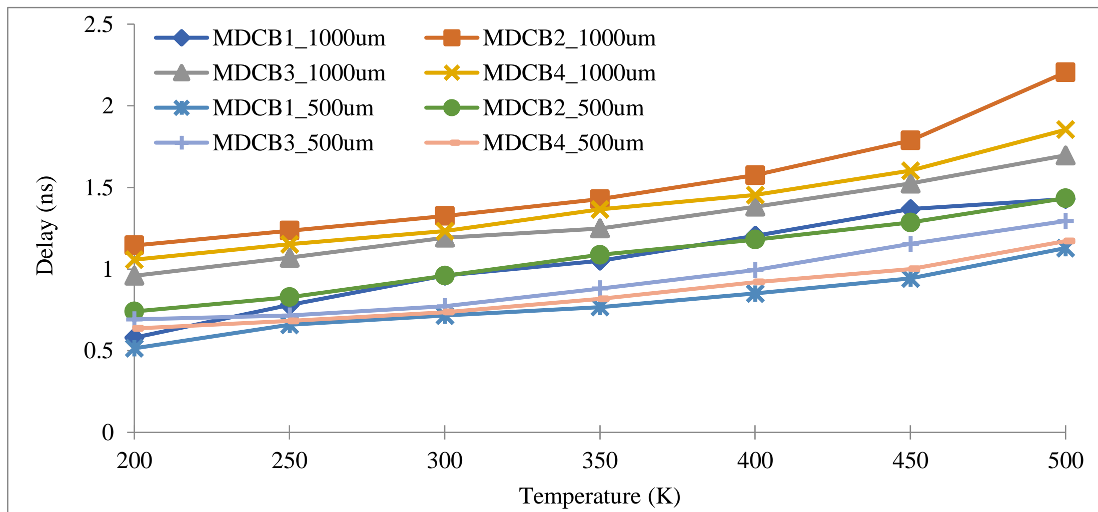


Figure 4.9 Temperature sensitive delay (ns) of MDCB structures for 500μm and 1000μm interconnect length at 22nm technology node

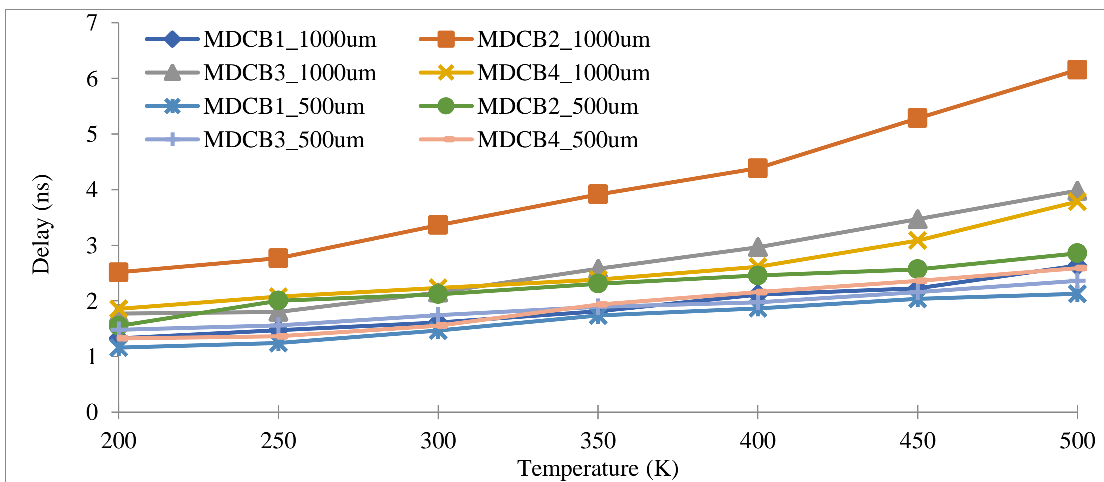


Figure 4.10 Temperature sensitive delay (ns) of MDCB structures for 500μm and 1000μm interconnect length at 16nm technology node

It is viewed from the figures that the MDCB 1 structure gives a minimum value of delay and MDCB 2 attains a maximum value of delay at all technology nodes for all levels of interconnect length at all temperature points. MDCB 1 structure (formed by positioning excellent conducting double-wall CNTs in the center and crosstalk aware large diameter multi-wall CNTs at edges) achieves the least and the best thermally aware propagation delay results than the other three possible mixed CNTs developed from multi and double-wall nanotubes for 32nm technology and Temperature-sensitive PDP values of MDCB structures for 500µm and 1000µm interconnect length is mentioned in Table 4.4.

Table 4.4 Temperature sensitive PDP (µW.ns) of MDCB structures for 500µm and 1000µm interconnect lengths at various nanotechnology nodes

Temp (K)	200	250	300	350	400	450	500	200	250	300	350	400	450	500
	At 500µm							At 1000µm						
At 32nm technology														
MDCB1	1.04	1.17	1.53	1.83	2.61	3.40	4.45	5.20	6.09	7.76	8.29	9.25	10.28	11.23
MDCB2	5.62	6.91	7.81	9.02	10.00	11.09	12.88	13.81	14.55	15.10	16.69	18.31	19.77	22.50
MDCB3	3.55	4.34	5.55	7.36	8.46	9.46	10.78	11.85	12.63	13.38	13.82	14.99	16.58	18.05
MDCB4	1.67	2.24	2.96	3.58	4.95	6.22	7.57	8.94	9.08	10.55	12.63	14.25	15.58	17.22
At 22nm technology														
MDCB1	8.08	9.04	9.84	10.54	11.76	13.10	15.43	8.90	10.24	12.63	13.74	15.69	17.90	18.65
MDCB2	10.92	11.89	13.83	15.27	17.18	18.66	20.95	18.22	18.76	20.21	22.49	25.05	28.44	34.86
MDCB3	10.39	10.98	11.73	13.45	15.11	17.43	19.28	16.64	17.85	19.32	21.20	22.54	24.36	28.91
MDCB4	9.00	9.65	10.53	11.63	13.10	14.12	16.28	15.36	16.88	18.10	20.10	21.26	23.44	27.39
At 16nm technology														
MDCB1	19.44	20.90	24.67	29.22	31.46	34.35	35.79	21.43	23.74	26.02	29.25	34.10	35.90	42.36
MDCB2	27.02	34.91	37.01	40.34	42.81	44.72	49.81	44.45	48.84	59.48	69.35	77.92	93.64	109.05
MDCB3	26.00	27.41	30.67	33.28	34.71	37.86	41.42	32.21	32.58	38.84	46.65	53.53	62.63	71.90
MDCB4	22.81	23.40	26.74	33.34	36.98	40.34	44.28	32.56	36.26	39.00	41.70	45.78	53.93	65.95

As temperature varies, there is an ignorable change in the value of capacitance due to the influence of inter-shell capacitance over quantum capacitance. The power of the first structure with MWCNTs the on outer edges remains the lowest. The impact of power is also added, and values of PDP are mentioned in Table 4.4. These values are compared and shown in Figure 4.11-4.13.

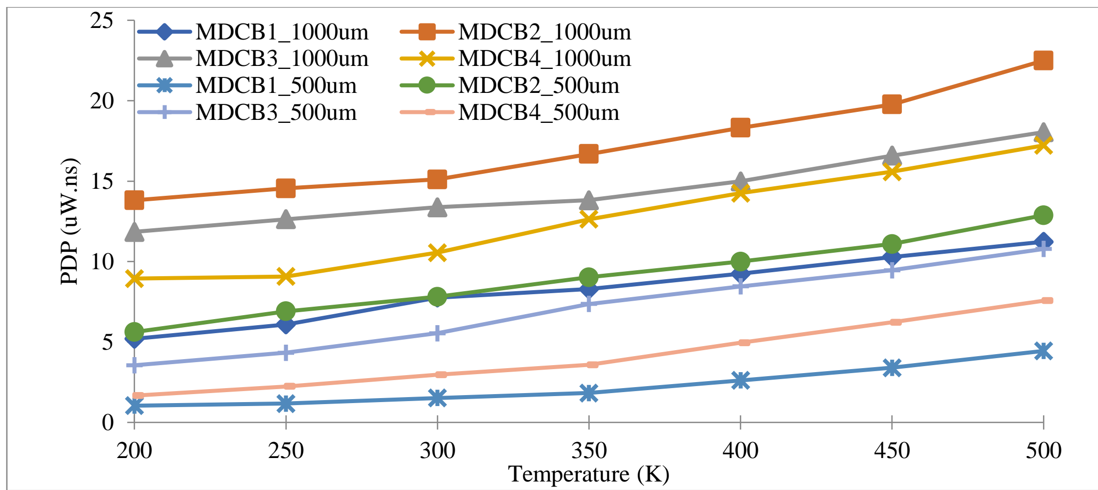


Figure 4.11 Temperature sensitive PDP (µW.ns) of MDCB structures for 500µm and 1000µm interconnect length at 32nm technology node

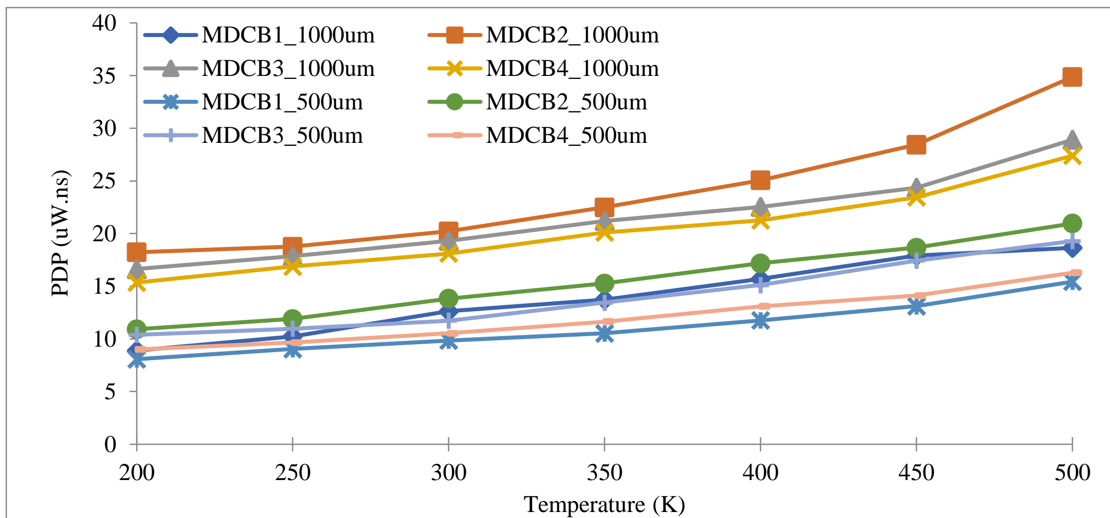


Figure 4.12 Temperature sensitive PDP (µW.ns) of MDCB structures for 500µm and 1000µm interconnect length at 22nm technology node

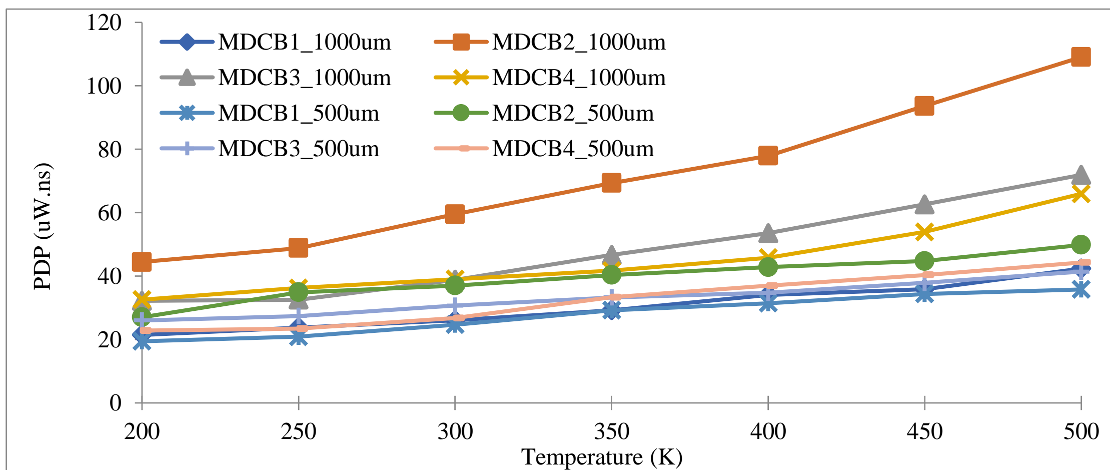


Figure 4.13 Temperature sensitive PDP (µW.ns) of MDCB structures for 500µm and 1000µm interconnect length at 16nm technology node

It is concluded from the figures above that MDCB 1 has the lowest value of the temperature-dependent power-delay product than another MDCB interconnects. This remains constant for all technology nodes and lengths. So, putting double-layered CNTs with less resistance and good conductance in the center and MWCNTs at the boundary of the bundle to overcome coupling capacitance can provide us with a thermally reliable and high-speed global interconnect material at advanced nodes.

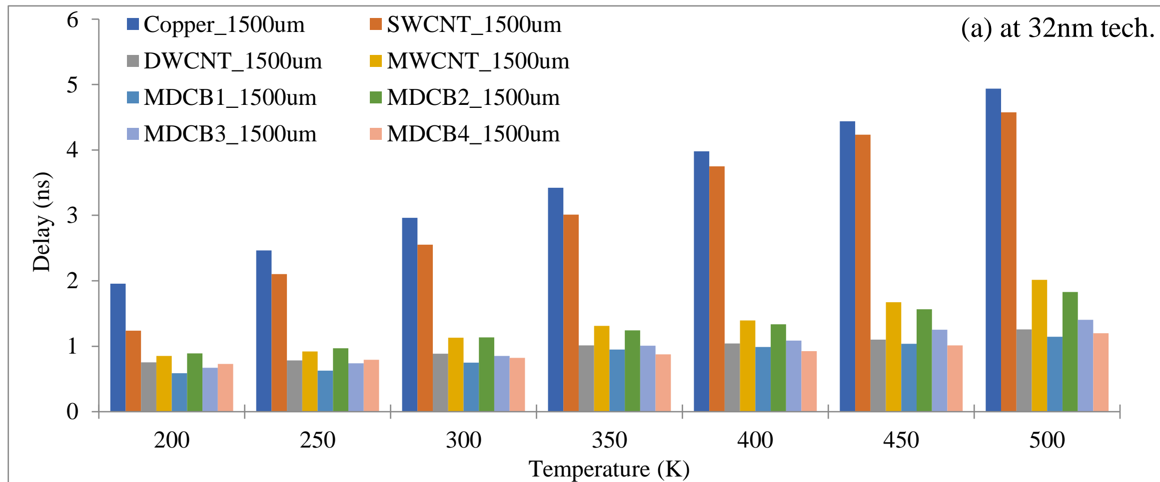
4.3 Comparison of temperature sensitive delay and PDP of copper, SWCNT, DWCNT, MWCNT, and MDCB structures

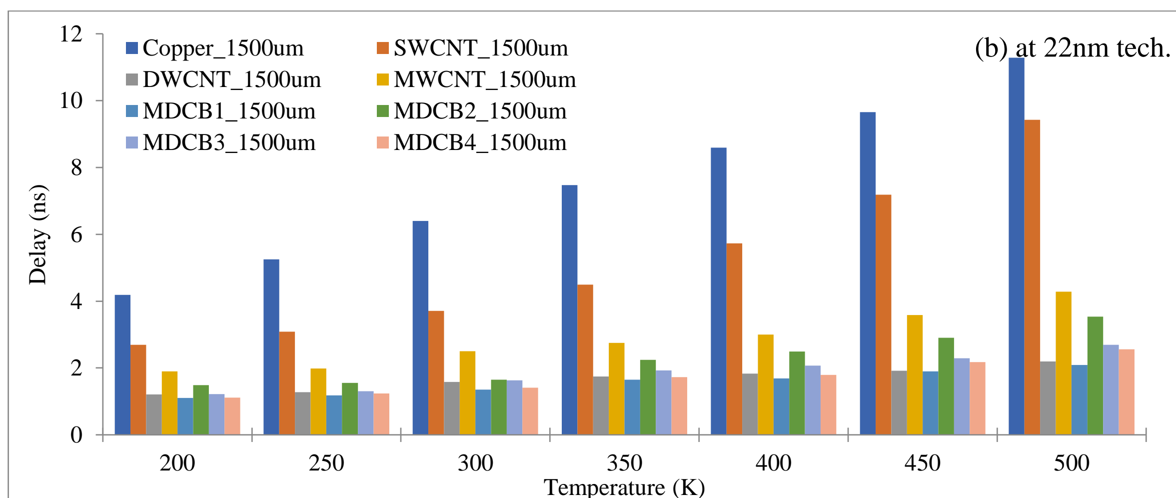
The thermally reliable result in the section compares delay and PDP values of copper with basic CNT materials (SWCNTs, MWCNTs, and DWCNTs) and mixed CNT different at global interconnect lengths. Delay readings are mentioned in Table 4.5 and are plotted for 1500µm and 2000µm lengths at different technologies against varying temperature ranges as shown in Figure 4.14(a)-(c) and Figure 4.15(a)-(c) respectively.

Table 4.5 Comparison of temperature sensitive delay (ns) of copper, SWCNT, DWCNT, MWCNT, and MDCB structures for 1500µm and 2000µm interconnect lengths

Temp (K)	200	250	300	350	400	450	500	200	250	300	350	400	450	500
	1500µm							2000µm						
At 32 nm Technology														
COPPER	1.96	2.46	2.96	3.42	3.98	4.44	4.94	2.60	3.31	3.99	4.67	5.38	6.03	6.77
SWCNT	1.24	2.11	2.55	3.01	3.75	4.23	4.57	2.33	2.96	3.52	3.91	4.26	4.95	6.02
DWCNT	0.76	0.78	0.89	1.01	1.04	1.10	1.26	0.96	1.00	1.14	1.32	1.35	1.48	1.65
MWCNT	0.85	0.92	1.13	1.31	1.39	1.67	2.01	1.23	1.34	1.56	1.87	2.04	2.46	2.89
MDCB1	0.59	0.63	0.75	0.95	0.99	1.04	1.15	0.77	0.82	0.87	0.97	1.02	1.16	1.39
MDCB2	0.89	0.97	1.13	1.24	1.34	1.56	1.83	1.07	1.16	1.41	1.56	1.69	1.96	2.30
MDCB3	0.67	0.74	0.85	1.01	1.09	1.25	1.41	1.00	1.05	1.27	1.47	1.57	1.89	2.09
MDCB4	0.73	0.79	0.82	0.87	0.93	1.01	1.20	0.76	0.77	0.99	1.15	1.23	1.35	1.62
At 22 nm Technology														
COPPER	4.19	5.25	6.40	7.48	8.59	9.65	11.28	5.65	7.27	8.86	10.24	12.21	12.98	14.54
SWCNT	2.69	3.08	3.71	4.50	5.73	7.18	9.43	4.16	4.75	5.70	6.86	8.85	11.38	13.22
DWCNT	1.21	1.27	1.58	1.75	1.83	1.92	2.20	1.38	1.48	1.74	2.16	2.32	2.85	3.12
MWCNT	1.90	1.99	2.50	2.75	3.00	3.59	4.28	2.40	2.62	3.28	3.47	3.85	4.49	5.58
MDCB1	1.10	1.18	1.35	1.65	1.69	1.90	2.09	1.36	1.45	1.69	2.11	2.19	2.64	2.81
MDCB2	1.48	1.55	1.65	2.24	2.49	2.90	3.53	2.12	2.36	2.76	3.29	3.54	4.15	4.88
MDCB3	1.22	1.31	1.63	1.93	2.07	2.30	2.69	1.71	1.90	2.33	2.77	2.96	3.44	3.98
MDCB4	1.12	1.23	1.41	1.73	1.79	2.17	2.56	1.46	1.59	1.99	2.46	2.56	2.83	3.50
At 16 nm Technology														
COPPER	12.31	16.10	19.46	23.90	26.54	30.59	34.87	16.25	21.82	27.26	32.87	37.97	41.98	46.03
SWCNT	4.09	5.07	6.17	7.52	9.62	13.06	17.52	6.04	7.32	8.97	11.09	14.49	18.37	26.45
DWCNT	2.92	3.37	4.12	4.56	5.27	6.04	6.24	4.08	4.60	5.68	6.54	6.90	8.38	10.33

MWCNT	4.14	4.76	5.76	6.46	7.01	8.47	10.22	5.97	6.87	7.83	9.27	10.12	12.24	14.40
MDCB1	2.02	2.20	2.66	3.10	3.43	3.92	4.37	2.68	2.86	3.43	4.36	4.52	5.31	5.95
MDCB2	3.82	4.19	5.23	6.39	6.46	7.59	9.60	5.37	5.95	7.13	8.54	9.45	11.07	13.09
MDCB3	2.53	2.93	3.53	4.05	4.40	5.40	5.94	3.56	4.00	4.89	5.82	6.35	7.44	8.63
MDCB4	2.31	2.54	3.19	3.68	4.07	4.54	5.69	3.07	3.31	4.12	5.27	5.42	6.29	7.61





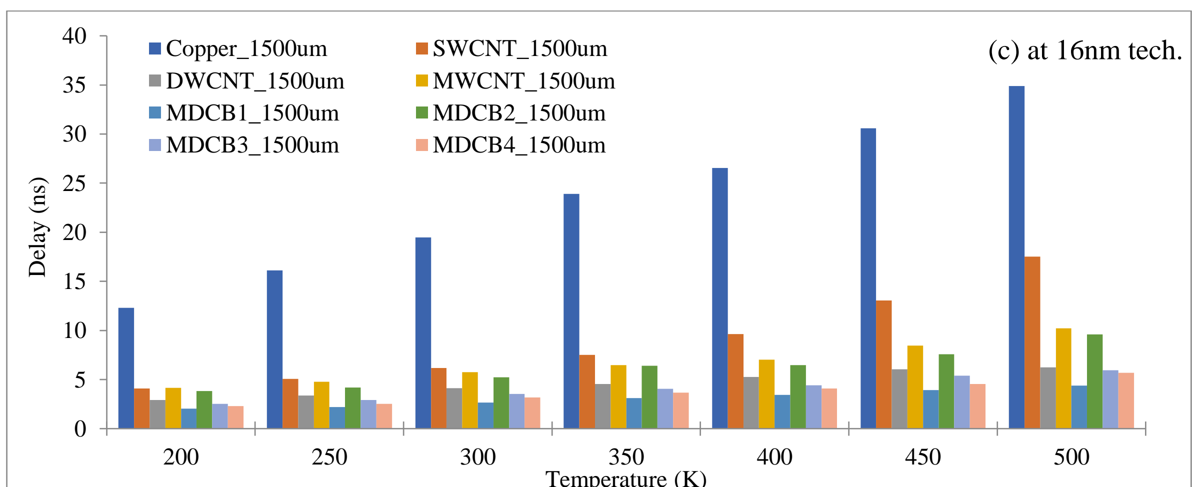
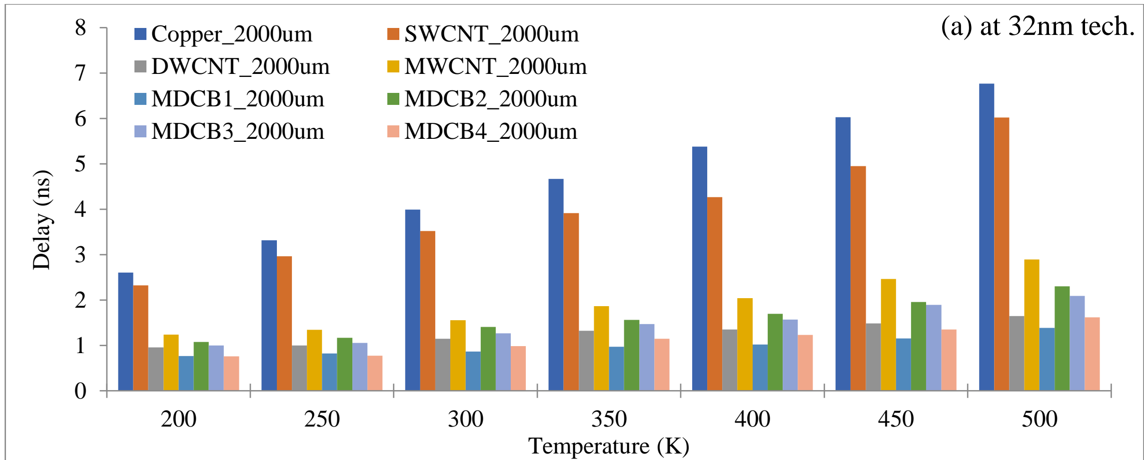
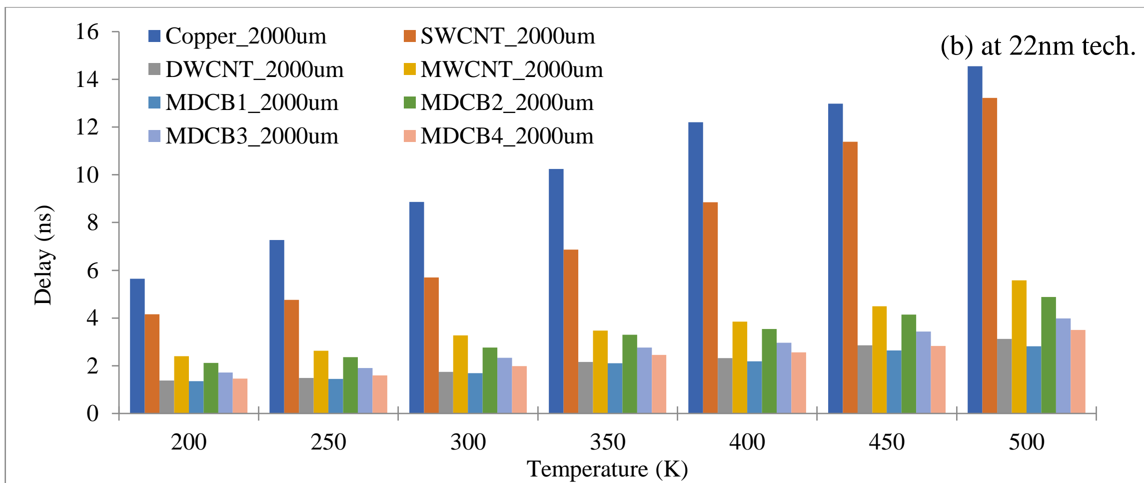


Figure 4.14 Comparison of temperature sensitive delay (ns) of copper, SWCNT, DWCNT, MWCNT, and MDCB structures for1500µm interconnect length at (a) 32nm (b) 22 nm (c) 16nm technology node





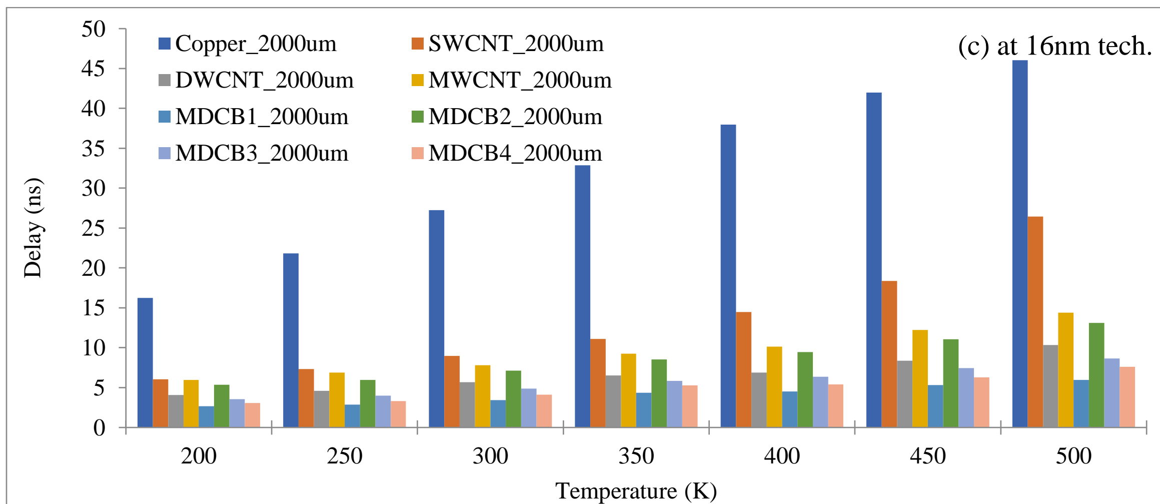


Figure 4.15 Comparison of temperature sensitive delay (ns) of copper, SWCNT, DWCNT, MWCNT, and MDCB structures for 2000μm interconnect length at (a) 32nm (b) 22nm (c) 16nm technology node

It is observed from the figures above that the MDCB 1 structure continues to give the lowest readings in terms of delay as a function of length and temperature and possibly provides a good substitute for global interconnect high-paced VLSI circuits. Also, temperature-sensitive PDP readings are mentioned in Table 4.6 and are plotted for 1500μm and 2000μm lengths at

different technologies against varying temperature ranges as shown in Figure 4.16(a)-(c) and Figure 4.17(a)-(c) respectively.

Table 4.6 Comparison of temperature sensitive PDP (µW.ns) of copper, SWCNT, DWCNT, MWCNT, and MDCB structures for 1500µm and 2000µm interconnect lengths

Temp (K)	200	250	300	350	400	450	500	200	250	300	350	400	450	500
	1500µm							2000µm						
At 32 nm Technology														
COPPER	28.63	36.16	44.00	51.38	60.94	68.65	77.35	41.21	53.58	65.79	78.26	92.27	105.44	121.29
SWCNT	22.63	30.16	39.00	45.38	55.94	61.65	71.35	38.73	46.91	55.21	69.36	86.82	96.70	104.42
DWCNT	13.68	14.17	16.08	18.42	18.98	20.06	23.02	19.61	20.35	23.45	27.35	27.92	30.75	34.41
MWCNT	12.23	13.37	15.66	17.13	18.55	21.77	25.50	14.82	16.12	19.54	21.77	23.60	27.46	32.46
MDCB1	10.23	10.95	13.08	16.29	16.99	17.77	19.46	13.81	14.76	15.65	17.27	18.10	20.72	24.69
MDCB2	17.23	18.55	22.90	26.54	28.22	34.22	41.49	27.91	30.58	35.65	43.33	48.30	59.41	72.14
MDCB3	14.86	16.38	18.79	22.24	24.02	27.83	31.46	25.12	26.45	31.88	37.46	40.17	49.41	56.31
MDCB4	13.68	14.77	15.19	16.07	17.10	18.54	22.00	15.03	15.10	19.15	21.57	23.05	25.27	30.45
At 22 nm Technology														
COPPER	55.78	71.11	88.46	105.50	124.26	142.18	170.26	82.10	109.51	137.53	164.78	203.93	224.85	260.07
SWCNT	44.09	58.95	72.38	84.61	98.27	108.93	143.33	64.61	81.45	102.49	120.91	158.06	184.32	211.17
DWCNT	17.39	18.12	22.84	24.98	26.24	27.74	31.73	23.40	24.84	28.98	34.87	35.65	43.27	46.35
MWCNT	22.46	23.58	29.85	32.86	35.91	43.28	51.84	29.52	32.48	40.81	43.39	48.28	56.87	71.64
MDCB1	15.70	16.99	18.82	23.31	24.94	28.03	31.05	20.15	22.11	25.81	31.76	33.72	39.75	43.60
MDCB2	23.90	25.03	26.64	36.60	40.73	48.50	59.56	37.74	42.08	49.87	59.71	64.59	76.58	91.63
MDCB3	20.55	21.98	27.63	32.74	35.15	39.79	46.87	31.97	35.70	44.13	52.84	56.66	66.62	78.03
MDCB4	16.97	18.90	21.37	25.99	26.74	31.19	36.69	22.03	23.87	30.05	37.07	38.72	42.82	54.45
At 16 nm Technology														
COPPER	222.55	306.25	384.93	491.86	566.32	674.62	794.53	329.90	472.90	626.24	798.41	972.53	1134.1	1299.6
SWCNT	115.24	145.74	181.38	229.24	309.20	452.34	670.23	198.53	248.10	314.83	410.07	581.06	817.77	1139.9
DWCNT	50.68	58.62	70.77	77.74	90.25	103.78	107.21	70.55	79.91	98.58	114.27	120.94	148.07	187.03
MWCNT	64.01	73.95	89.89	101.26	110.21	134.12	163.71	88.38	96.68	116.08	140.53	145.24	185.80	225.86
MDCB1	34.15	37.21	45.26	53.08	58.88	67.69	75.81	47.56	51.09	61.55	79.21	82.19	97.43	110.45
MDCB2	71.01	78.53	99.00	122.33	124.69	147.55	252.01	106.71	119.00	145.18	178.13	199.36	238.67	418.51
MDCB3	47.08	54.73	66.72	77.53	84.26	104.17	116.01	70.72	79.84	99.03	119.46	130.85	156.34	185.46
MDCB4	41.29	44.71	55.60	64.55	71.43	79.59	100.48	54.93	59.13	74.27	95.45	98.46	116.42	142.23

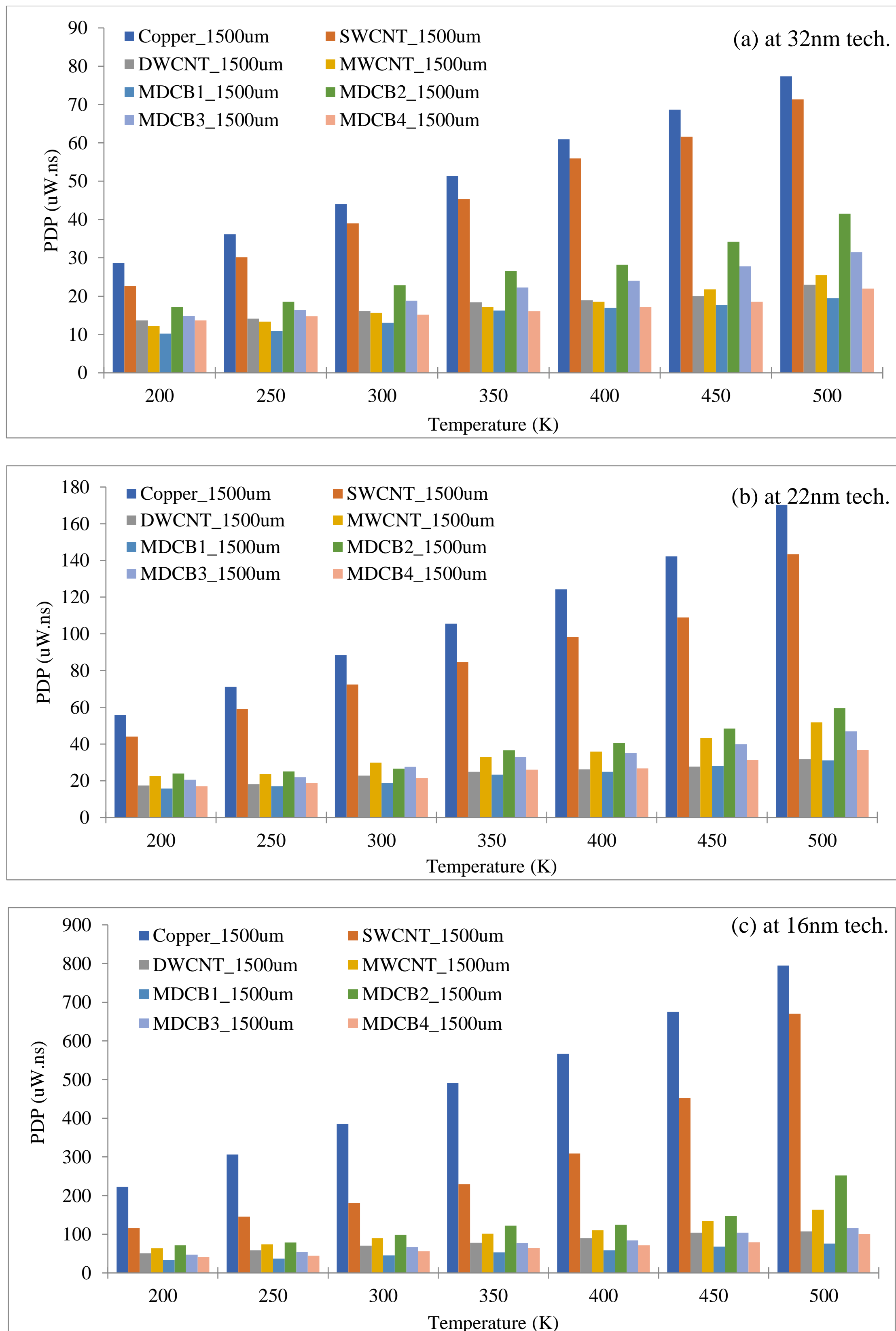
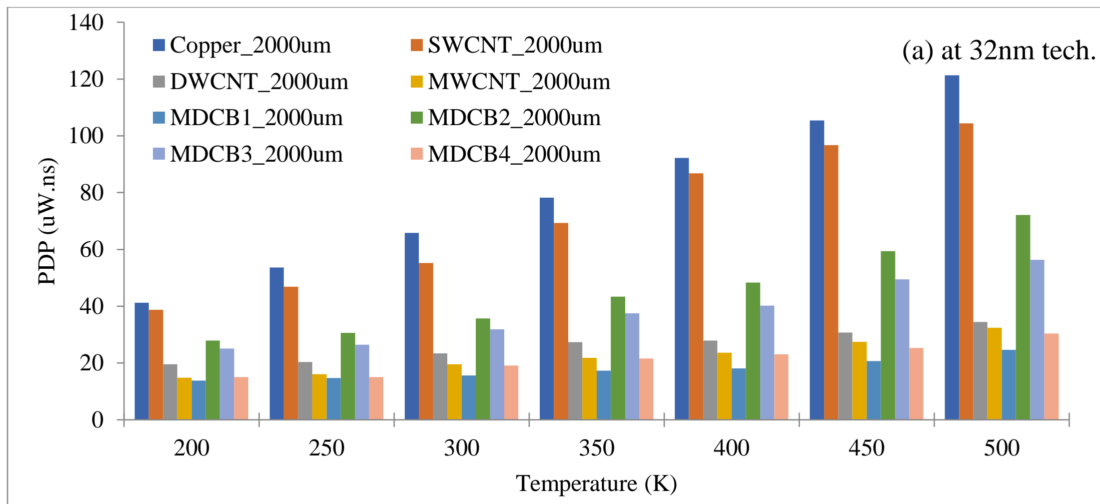
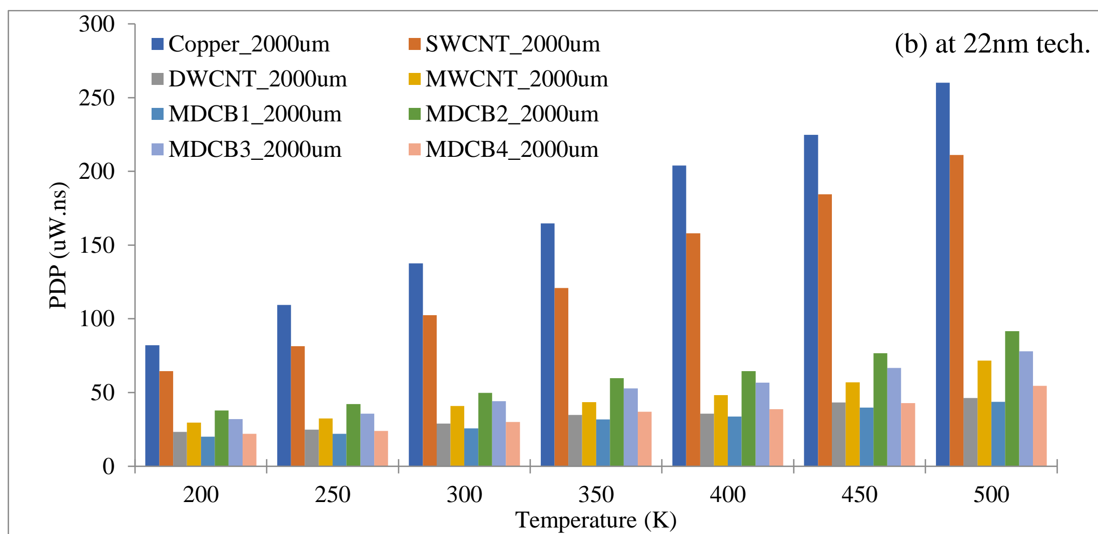


Figure 4.16 Comparison of temperature sensitive PDP (µW.ns) of copper, SWCNT, DWCNT, MWCNT, and MDCB structuresfor1500µminterconnect length at (a) 32nm (b) 22nm (c) 16nm technology node





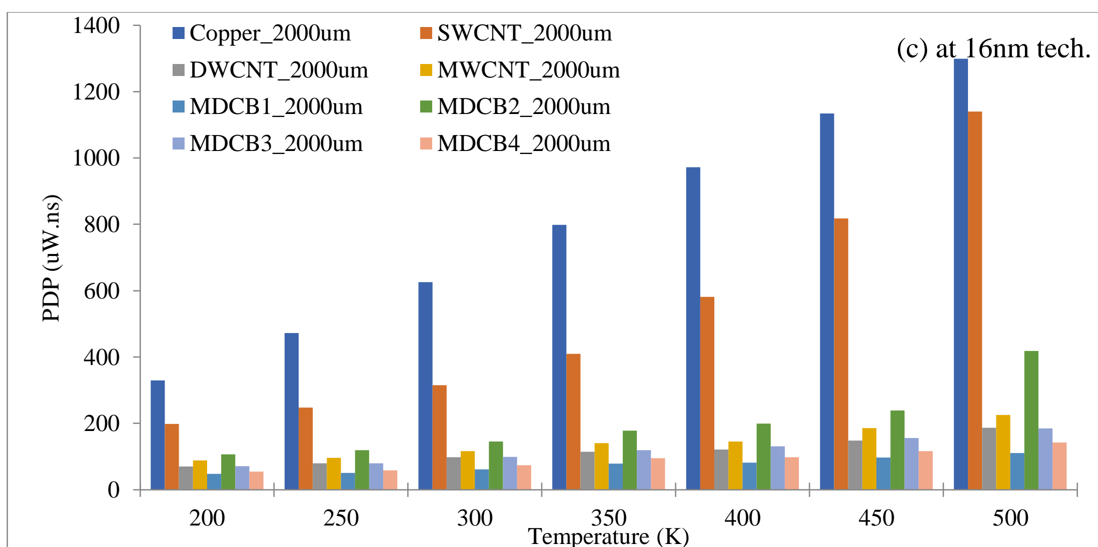


Figure 4.17 Comparison of temperature sensitive PDP (µW.ns) of copper, SWCNT, DWCNT, MWCNT, and MDCB structures for 2000µminterconnect length at (a) 32nm (b) 22nm (c) 16nm technology node

Various mixed CNT bundle structures are proposed and developed by combining the best properties and changing positions of double-wall and multi-wall carbon nanotubes. MDCB 1

offers the lowest value of PDP as shown in Figure 4.16 and Figure 4.17. The presence of DWCNTs helps in yielding good conduction due to decreased resistance offered by the addition of two shells in a parallel way. Large-diameter MWCNTs help in lowering the effect of coupling capacitance. It has been noticed that CNTs can undoubtedly oust copper at larger lengths. It is also analyzed that MDCB 1 structure is even giving better results than MWCNTs and DWCNTs and can continue to replace them as VLSI interconnect material.

4.4 Chapter Summary and Contribution

The effect of the temperature change is reflected in this chapter. It has been studied that above room temperature various electron-phonon scatterings occur in CNTs. So, the role of temperature can't be ignored while determining the performance of global interconnects. Due to the increase in scattering at high temperatures, the MFP of CNTs is affected which changes their net resistance thereby degrading the overall speed and PDP performance of the circuit. Temperature-dependent resistances are determined and used in simulations to determine the delay and PDP-based performance of copper, SWCNT, DWCNT, MWCNT, and various MDCB structures. The temperature varies from 200 Kelvin to 500 Kelvin.

The simulation is performed for various nano-technology nodes for four interconnect lengths (500µm, 1000µm, 1500µm, and 2000µm). Due to increased resistivity and electromigration in copper, it fails as a nano interconnect material for circuits. This degraded impact of copper is enhanced at further scaled nodes. Temperature-dependent delay and PDP-based comparisons are done and it has been noticed from the results shown in this chapter that the MDCB 1 structure (DWCNTs in the center and MWCNTs at the periphery of bundle) performs better than other MDCB structures. MDCB 1 structure also can replace MWCNTs and DWCNTs. This class of mixed CNT bundles gives extraordinarily good results concerning global delay and PDP at scaled nodes. Since the performance of interconnects is influenced by temperature. So, the effect of temperature can't be neglected, and it must be included to determine the accurate performance of circuits.

Related Publication:

1. Gurleen Dhillon and Karmjit Singh Sandha, "Mixed CNT bundles as VLSI interconnects for nanoscale technology nodes," *Journal of Computational Electronics*, vol. 20, no.1, pp. 248-258, 2021. *(Impact Factor- 1.983)* (SCI indexed)

5. Impact of Crosstalk and Stability in Mixed Bundle CNTs

At nano-scale technology nodes, global interconnects are cast as distributed transmission lines. These interconnect wires are situated parallel to each other on tiny chips and suffer from various capacitive and inductive coupling effects as shown in Figure 5.1. So, in this manner, unwanted crosstalk influences the performance of long connecting lines [16,76,79]. The work presented in this chapter also examines the stability of MDCB structures employed as global interconnect material for various nanotechnologies.

The undesirable coupling effects faced by interconnect lines under the influence of nearby lines are called crosstalk. In this manner, crosstalk acts as a supreme factor in judging the overall performance of integrated circuits. Crosstalk noise may lead to fatal complications like changes in signal delay, logic failure, and more which alter the operation of the designed circuit [80-83, 146-152].

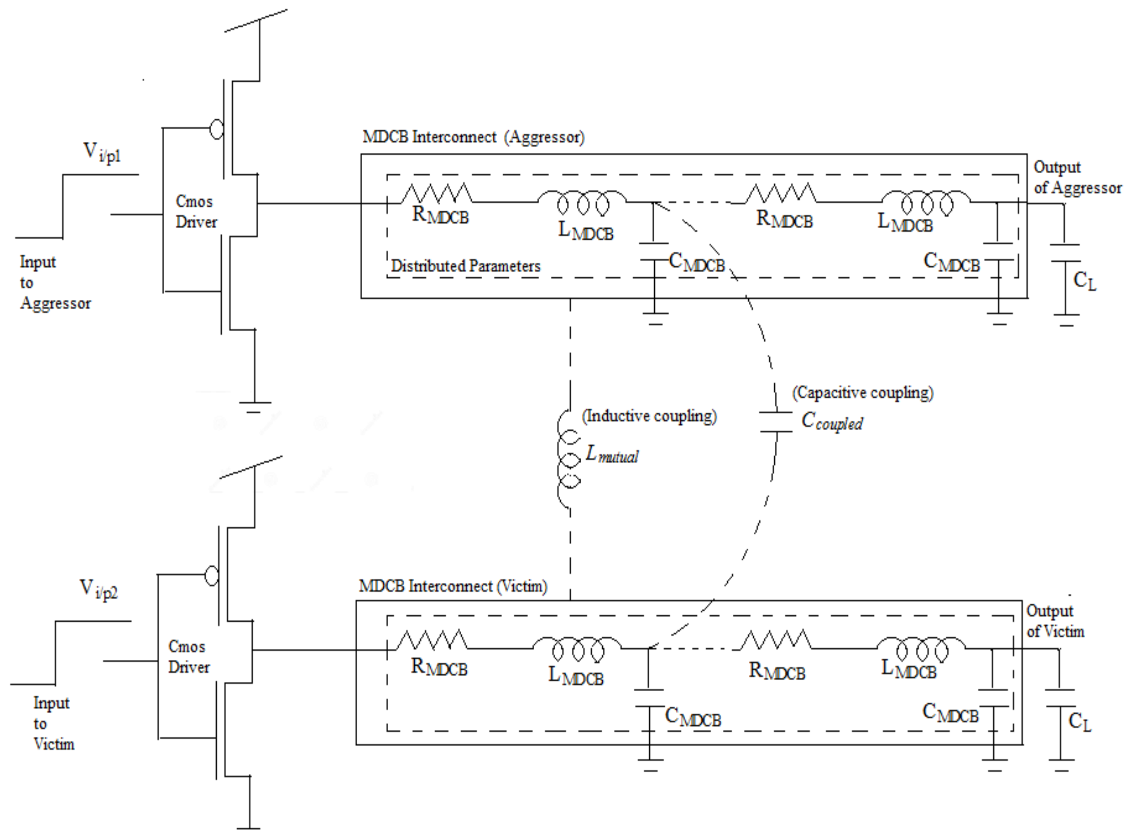


Figure 5.1 Equivalent circuit of crosstalk affected coupled global mixed CNT interconnects.

The coupling capacitance ($C_{coupled}$) between coupled interconnect wires which are separated by distance '*s*' is expressed by equation (5.1) where '*d*' is calculated from the average sum of both interconnects.

$$C_{coupled} = \frac{\pi\varepsilon}{ln\,(\frac{2s}{d})} \tag{5.1}$$

The inductive coupling or mutual inductance (L_{mutual}) between interconnects can be determined by equation (5.2) [110].

$$L_{mutual} = \frac{\mu_0 l}{2\pi}[ln\left(\frac{2l}{s}\right) - 1 + \frac{s}{l}] \tag{5.2}$$

5.1 Crosstalk in mixed bundle CNTs

In this section, the consequences of crosstalk are analyzed in detail for mixed bundle CNT structures over a large temperature range at three technology nodes for a global length (1000µm).

Two types of crosstalk can occur depending upon the type of switching in nearby lying interconnect lines [98,104,147-149].

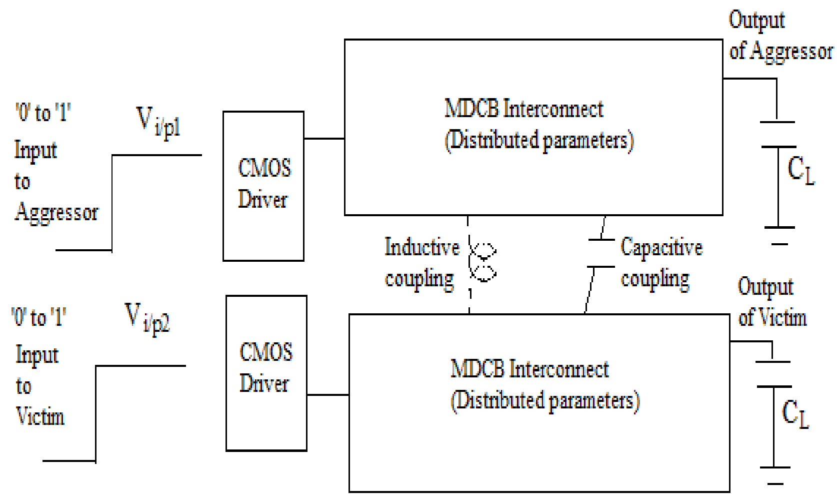
- If one interconnect line is silent or inactive or in an idle state (victim line and), and encounters a voltage spike/glitch due to some switching in a nearby line (aggressor line), it is termed as functional crosstalk.
- When the nearest interconnect lines experience an activity simultaneously, then dynamic crosstalk exists. Here, the signal delay is affected. Further in this, if the switching occurs in the same direction (0->1,0->1 or 1->0,1->0) for coupled interconnect lines, they tend to affect each other's delay and are termed to be in in-phase or even mode. When they switch in opposite directions (0->1,1->0 or 1->0,0->1), they are termed odd modes of dynamic crosstalk.

5.1.1 Dynamic Crosstalk

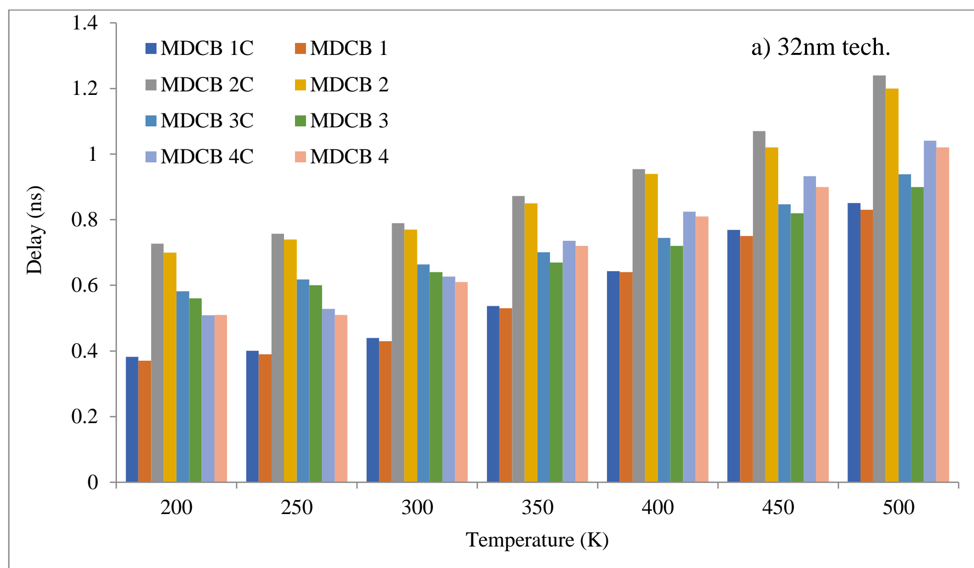
Such crosstalk exists when two interconnect lines undergo some activity and are in the vicinity of each other on an integrated chip. This sub-section focuses on different cases of switching of victim and aggressor lines for global length [98].

The simulated results of crosstalk-induced MDCB structures (MDCB 1C, MDCB 2C, MDCB 3C, MDCB 4C) are compared with structures without crosstalk at different technologies. The block diagram and values of delay are presented through charts in Figure 5.2-5.5. The structures without considering the effect of crosstalk are represented as MDCB 1, MDCB 2, MDCB 3, and MDCB 4.

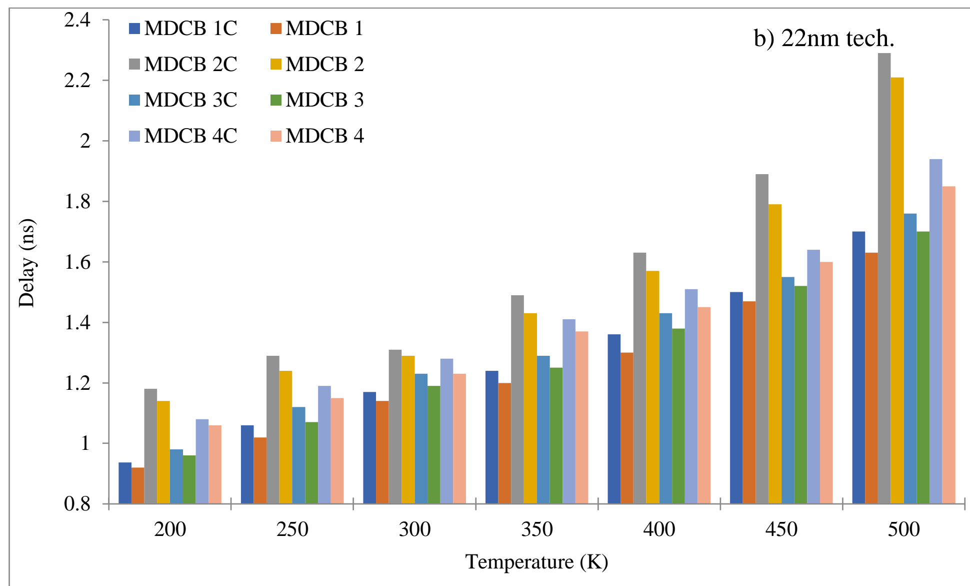
1. In-phase switching i) Aggressor: 0 → 1 and Victim: 0 → 1.



a)



b)



c)

d)

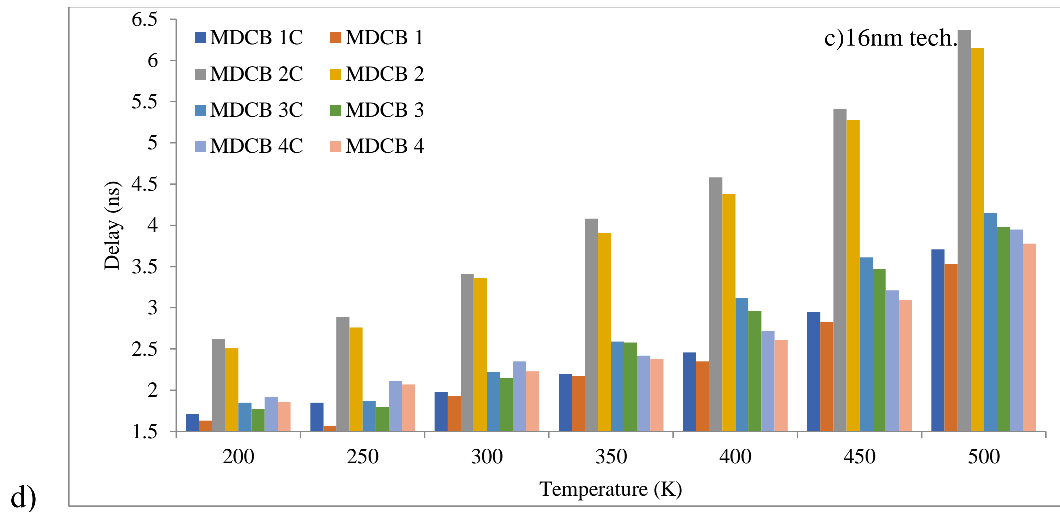
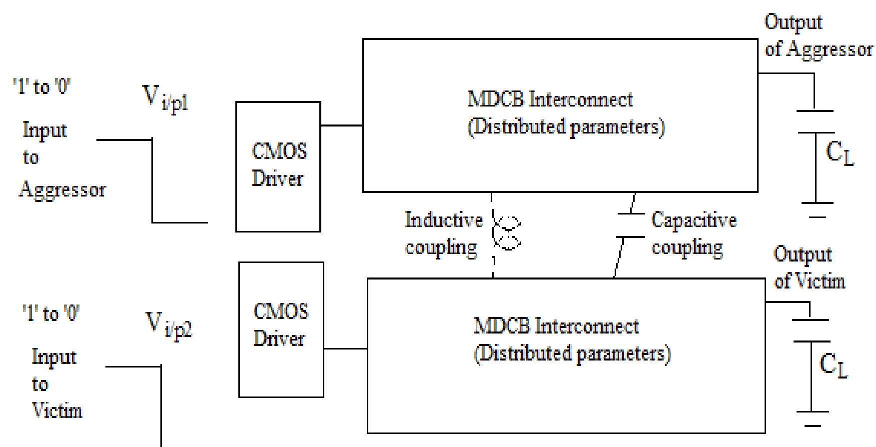
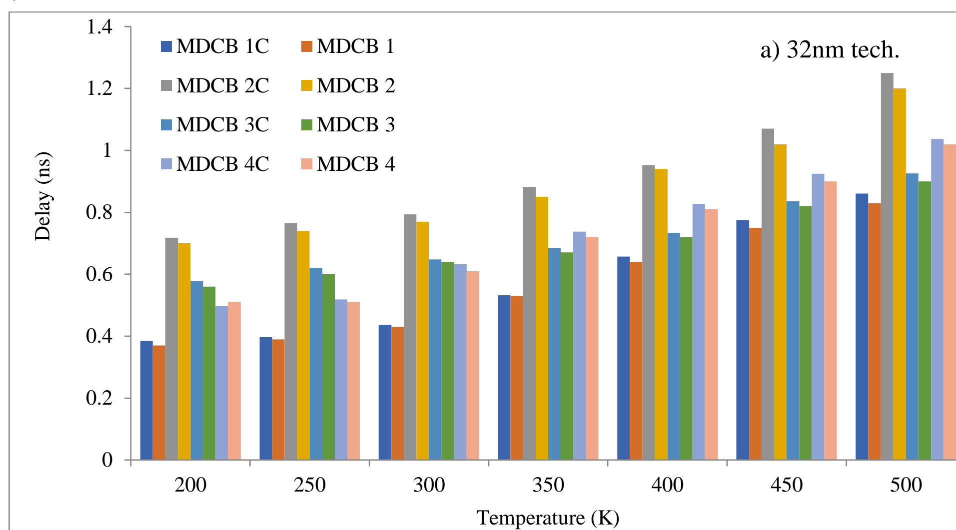


Figure 5.2 a) Block diagram representation of even/in-phase mode of dynamic crosstalk i) Aggressor: 0 → 1 and Victim: 0 → 1. Comparison of temperature sensitive delay of mixed CNTs with and without crosstalk effect b) at 32nm c) at 22nm and d) at 16nm technology node

In-phase switching ii) Aggressor: 1 → 0 and Victim: 1 → 0.



a)



b)

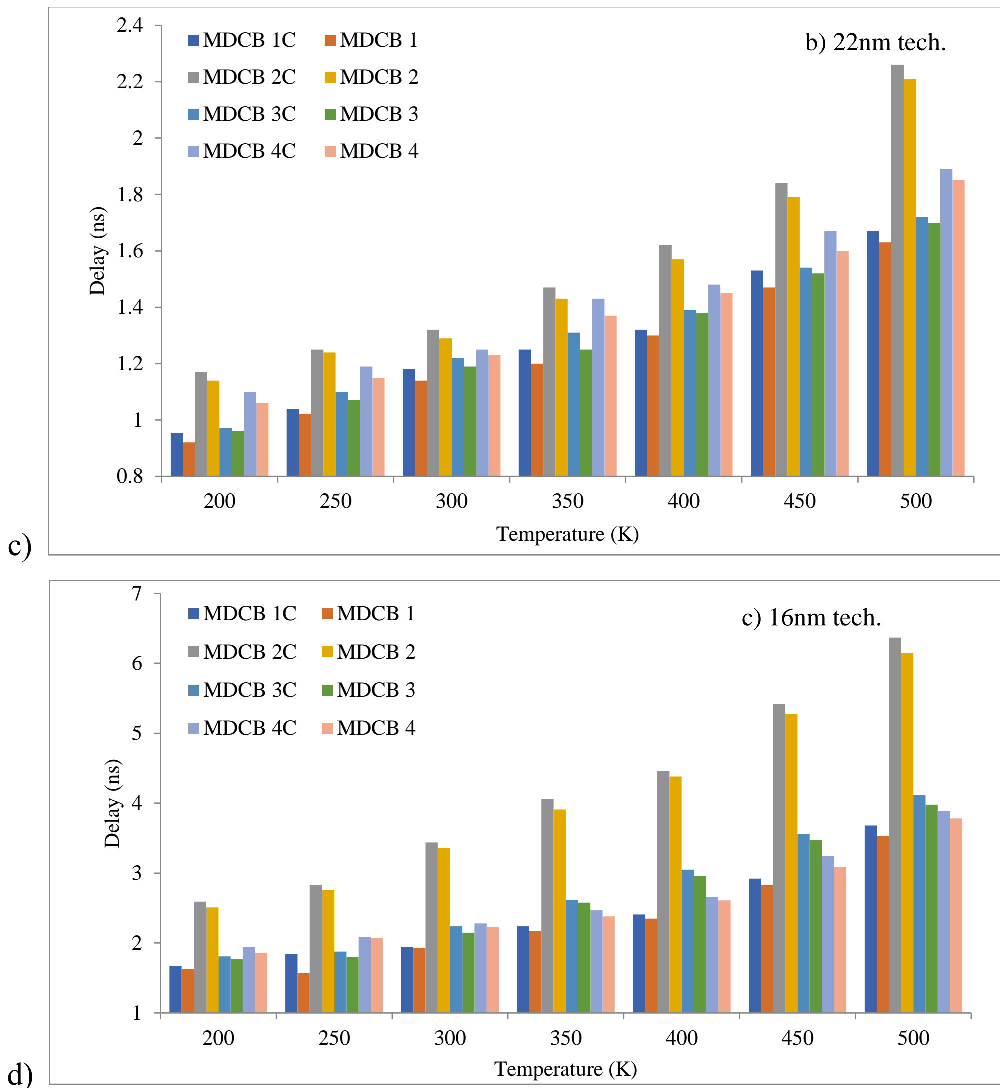
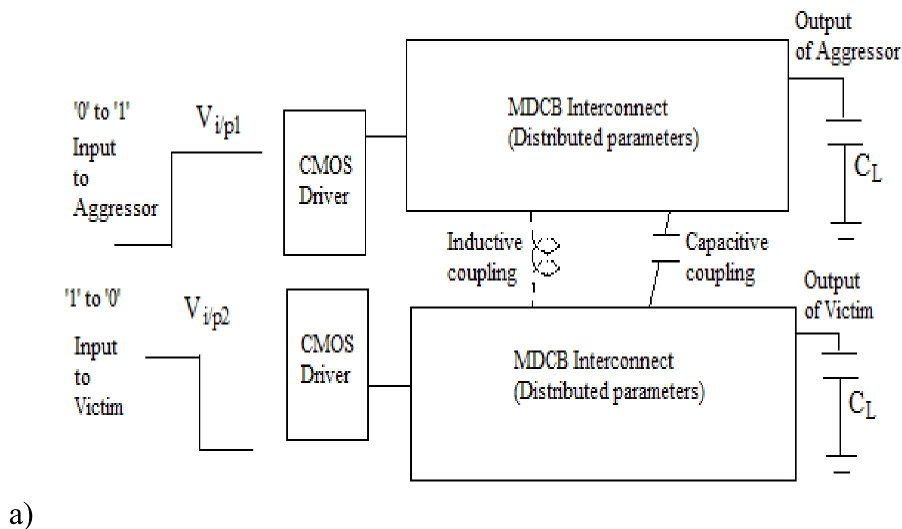


Figure 5.3 a) Block diagram representation of even/in-phase mode of dynamic crosstalk i) Aggressor: 1 → 0 and Victim: 1 → 0. Comparison of temperature sensitive delay of mixed CNT structures with and without crosstalk effect b) at 32nm c) at 22nm and d) at 16nm technology node

2. Out-phase switching i) Aggressor: 0 → 1 and Victim: 1 → 0



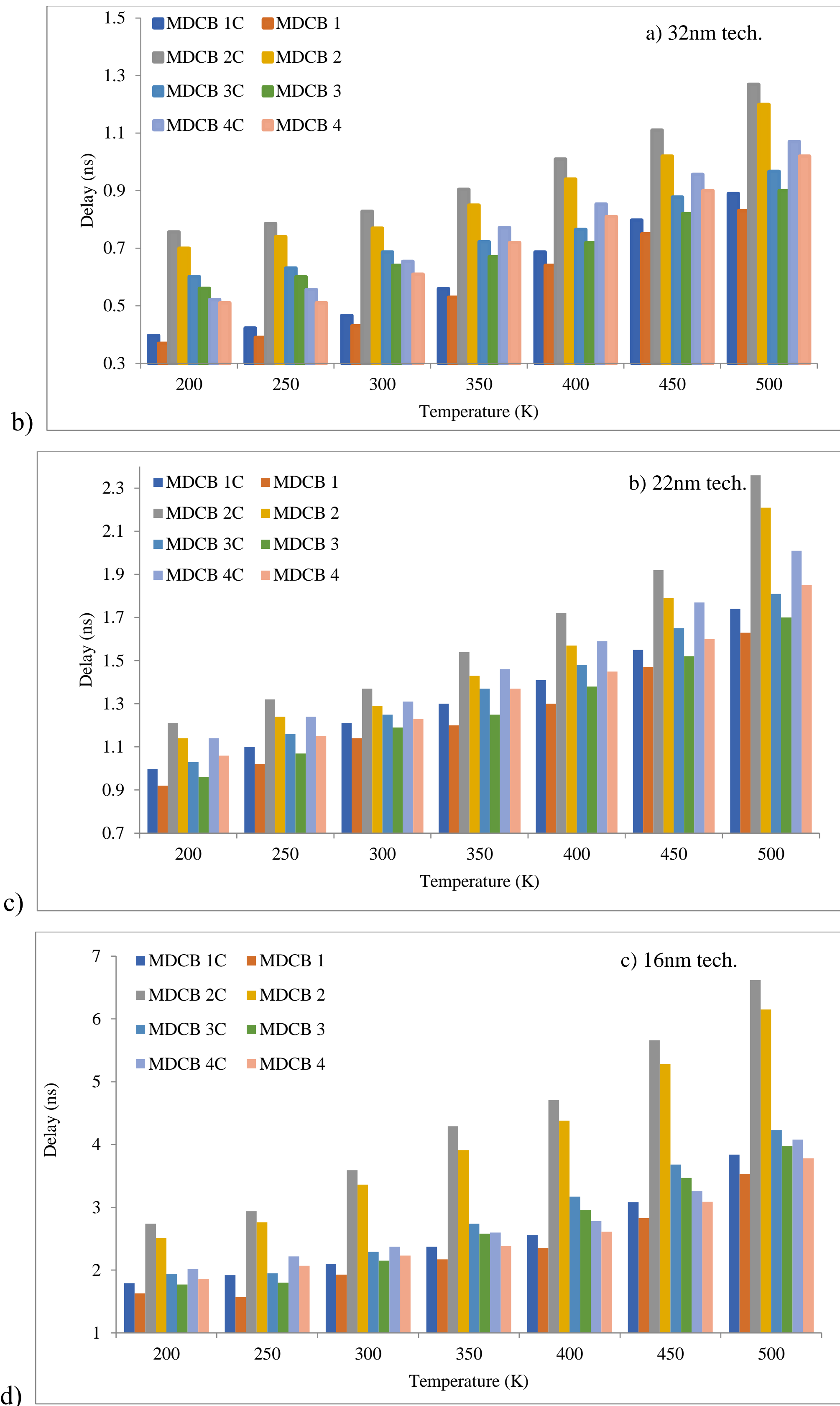
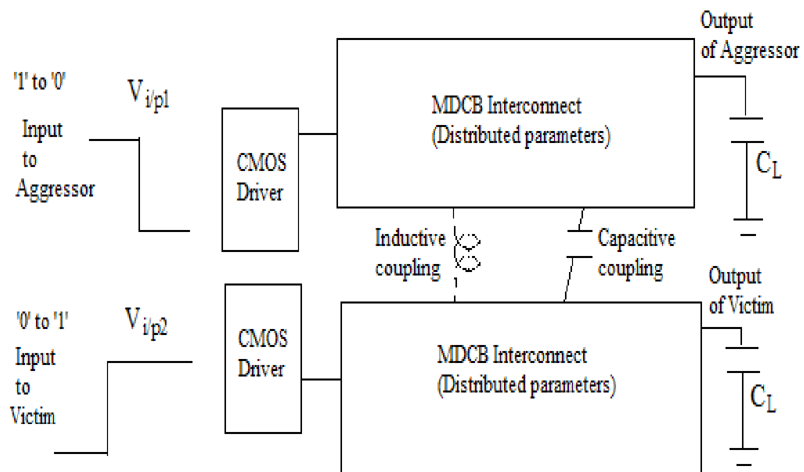
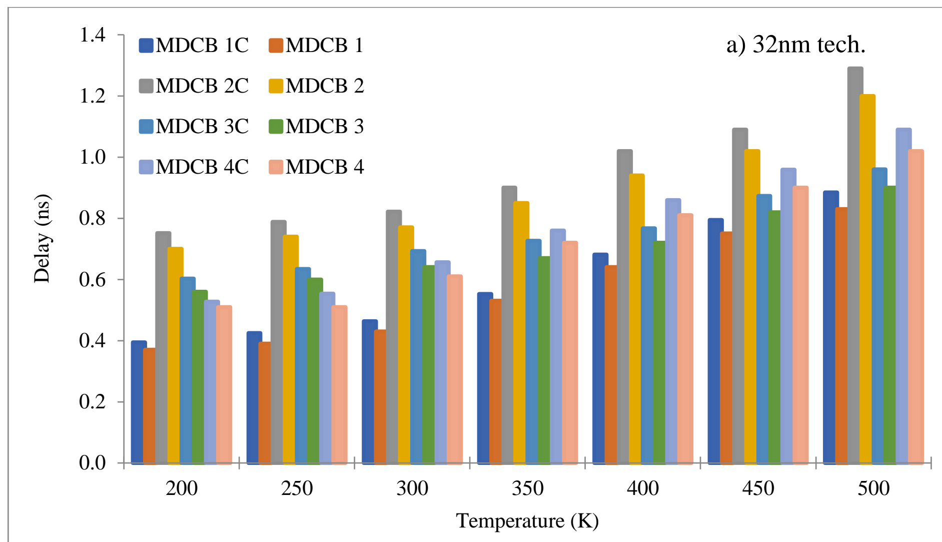


Figure 5.4 a) Block diagram representation of odd/out-phase mode of dynamic crosstalk i) Aggressor: 0 → 1 and Victim: 1 → 0. Comparison of temperature sensitive delay of mixed CNT structures with and without crosstalk effect b) at 32nm c) at 22nm and d) at 16nm technology node

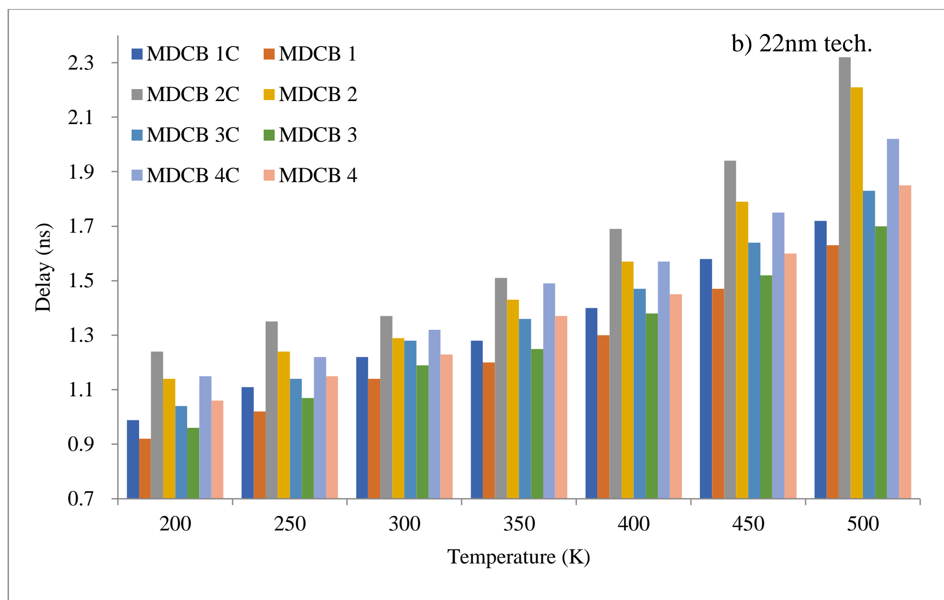
ii) Aggressor: 1 → 0 and Victim: 0 → 1



a)



b)



c)

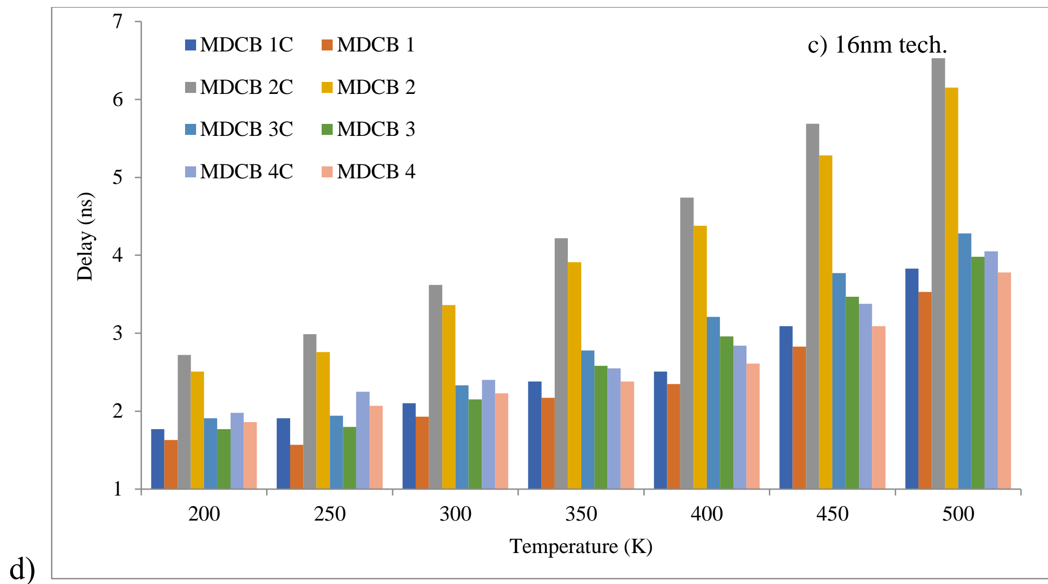


Figure 5.5 a) Block diagram representation of odd/out-phase mode of dynamic crosstalk ii) Aggressor: 1 → 0 and Victim: 0 → 1. Comparison of temperature sensitive delay of mixed CNT structures with and without crosstalk effect b) at 32nm c) at 22nm and d) at 16nm technology node

As observed from the figures above, temperature-dependent delay of all mixed CNT structures (MDCB 1C, MDCB 2C, MDCB 3C, MDCB 4C) increases with the inclusion of crosstalk effect than crosstalk unaware structures. Crosstalk is an important factor and can't be ignored while determining the performance of global interconnects at nanotechnologies. Evident from the results that the signal delay of the circuit upsurges with the rise in temperature as the MFP of the conducting electrons degrades.

The mean free path of conducting electrons is lowered and therefore, it leads to an upsurge in resistance due to scattering at high temperatures. Different parameters like length, technology, temperature, crosstalk, etc. play their role and impact the performance of interconnect. However, MDCB 1 structure with and without crosstalk continues to yield the lowest delay than all other structures and this trend remains constant for all technology nodes.

Table 5.1 lists the value without crosstalk affected (MDCB 1, MDCB 2, MDCB 3, MDCB 4) and with dynamic crosstalk induced delay for in-phase (MDCB 1C_E, MDCB 2C_E, MDCB 3C_E, MDCB 4C_E) and out-phase switching (MDCB 1C_O, MDCB 2C_O, MDCB 3C_O, MDCB 4C_O) for various MDCB (multi-wall and double-wall CNT bundle) structures. The dynamic crosstalk adds up to an unwanted delay in the circuit. It can be read that the crosstalk-aware structure shows more delay than without the crosstalk effect.

Also, the MDCB-1 structure with in-phase/even switching has less dynamic crosstalk-induced delay than the corresponding structure with out-phase/odd switching over 200-500K temperature at all three technology nodes. This holds for the other three mixed structures as

well. For the best comparison, Figure 5.6 (a)-(c) shows the value of delay of crosstalk affected (even and odd mode) and crosstalk unaware all mixed CNT bundles i.e., MDCB structures.

Table.5.1 Propagation delay (ns) values for without and with (out-phase and in-phase mode) crosstalk influenced mixed CNT structures at 1000μm interconnect length at 32nm, 22nm, and 16nm technology.

Delay (ns) at 32nm Tech.												
	Out-phase mode of switching				Crosstalk unaware				In-phase mode of switching			
Temp (K)	MDCB 1C_O	MDCB 2C_O	MDCB 3C_O	MDCB 4C_O	MDCB 1	MDCB 2	MDCB 3	MDCB 4	MDCB 1C_E	MDCB 2C_E	MDCB 3C_E	MDCB 4C_E
200	0.39	0.75	0.60	0.53	0.37	0.70	0.56	0.51	0.38	0.72	0.58	0.50
250	0.43	0.79	0.63	0.55	0.39	0.74	0.60	0.51	0.40	0.77	0.62	0.52
300	0.46	0.82	0.69	0.66	0.43	0.77	0.64	0.61	0.44	0.79	0.65	0.63
350	0.55	0.90	0.73	0.76	0.53	0.85	0.67	0.72	0.53	0.88	0.69	0.74
400	0.68	1.02	0.77	0.86	0.64	0.94	0.72	0.81	0.66	0.95	0.73	0.83
450	0.79	1.09	0.87	0.96	0.75	1.02	0.82	0.90	0.78	1.07	0.84	0.92
500	0.88	1.29	0.96	1.09	0.83	1.20	0.90	1.02	0.86	1.25	0.93	1.04
Delay (ns) at 22nm Tech.												
Temp (K)	MDCB 1C_O	MDCB 2C_O	MDCB 3C_O	MDCB 4C_O	MDCB 1	MDCB 2	MDCB 3	MDCB 4	MDCB 1C_E	MDCB 2C_E	MDCB 3C_E	MDCB 4C_E
200	0.99	1.24	1.04	1.15	0.92	1.14	0.96	1.06	0.95	1.17	0.97	1.10
250	1.11	1.35	1.14	1.22	1.02	1.24	1.07	1.15	1.04	1.25	1.10	1.19
300	1.22	1.37	1.28	1.32	1.14	1.29	1.19	1.23	1.18	1.32	1.22	1.25
350	1.28	1.51	1.36	1.49	1.20	1.43	1.25	1.37	1.25	1.47	1.31	1.43
400	1.40	1.69	1.47	1.57	1.30	1.57	1.38	1.45	1.32	1.62	1.39	1.48
450	1.58	1.94	1.64	1.75	1.47	1.79	1.52	1.60	1.53	1.84	1.54	1.67
500	1.72	2.32	1.83	2.02	1.63	2.21	1.70	1.85	1.67	2.26	1.72	1.89
Delay (ns) at 16nm Tech.												
Temp (K)	MDCB 1C_O	MDCB 2C_O	MDCB 3C_O	MDCB 4C_O	MDCB 1	MDCB 2	MDCB 3	MDCB 4	MDCB 1C_E	MDCB 2C_E	MDCB 3C_E	MDCB 4C_E
200	1.77	2.72	1.91	1.98	1.63	2.51	1.77	1.86	1.71	2.62	1.85	1.92
250	1.91	2.99	1.94	2.25	1.57	2.76	1.80	2.07	1.85	2.89	1.87	2.11
300	2.10	3.62	2.33	2.40	1.93	3.36	2.15	2.23	1.98	3.41	2.22	2.35
350	2.38	4.22	2.78	2.55	2.17	3.91	2.58	2.38	2.20	4.08	2.59	2.42
400	2.51	4.74	3.21	2.84	2.35	4.38	2.96	2.61	2.46	4.58	3.12	2.72
450	3.09	5.69	3.77	3.38	2.83	5.28	3.47	3.09	2.95	5.41	3.61	3.21
500	3.83	6.53	4.28	4.05	3.53	6.15	3.98	3.78	3.71	6.37	4.15	3.95

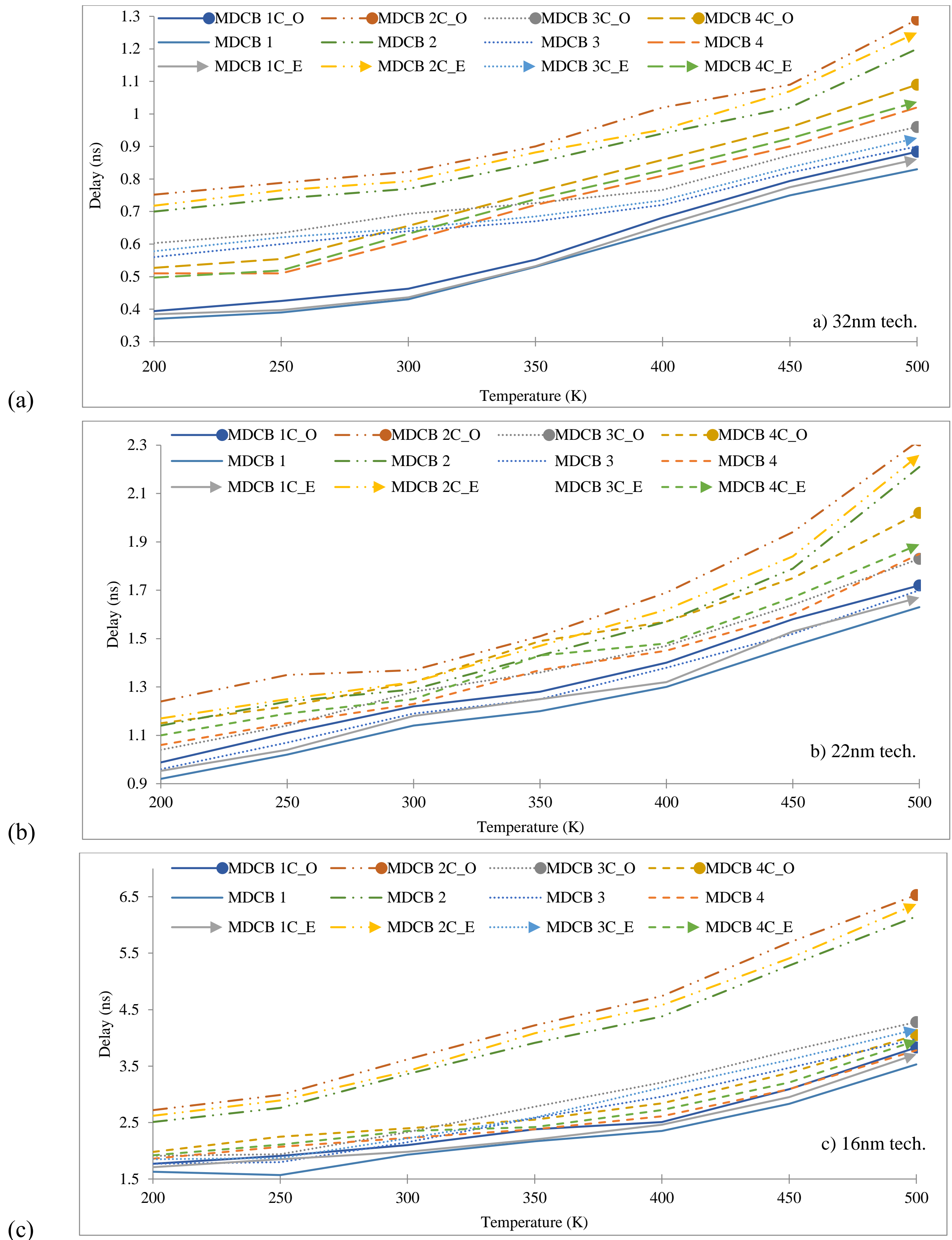


Figure 5.6 Dynamic crosstalk induced delay comparison of four MDCB structures excluding crosstalk, with even mode and with the odd mode of dynamic crosstalk switching a) at 32nm b) at 22nm and c) at 16nm technology.

Table 5.2 below indicates the percentage increase in values of propagation delay during in-phase and out-phase switching of crosstalk for mixed structures over 200K to 500K. As written in the table, the in-phase mode adds up to approximately ~3-5% more propagation delay and the out-phase mode of dynamic crosstalk switching introduces ~7-9% more delay than corresponding structures unaffected by crosstalk.

Table 5.2 Increase in delay (%) of mixed CNT structures during out-phase and in-phase mode of crosstalk switching

	Temp	Out-phase mode of switching				In-phase mode of switching			
		MDCB 1C_O	MDCB 2C_O	MDCB 3C_O	MDCB 4C_O	MDCB 1C_E	MDCB 2C_E	MDCB 3C_E	MDCB 4C_E
32nm	200K	6.09%	6.91%	7.13%	3.23%	3.70%	2.51%	3.11%	2.62%
	250K	8.24%	6.09%	5.36%	7.94%	1.76%	3.27%	3.38%	1.73%
	300K	7.13%	6.33%	7.65%	7.01%	1.38%	2.90%	1.23%	3.48%
	350K	3.99%	5.56%	7.71%	5.26%	0.38%	3.63%	2.19%	2.44%
	400K	6.02%	7.84%	6.13%	5.70%	2.59%	1.26%	1.91%	2.06%
	450K	5.54%	6.42%	6.07%	6.15%	3.23%	4.67%	1.91%	2.65%
	500K	6.11%	6.98%	6.25%	6.42%	3.60%	4.00%	2.81%	1.65%
22nm	200K	6.88%	8.06%	7.69%	7.83%	3.54%	5.65%	6.54%	4.35%
	250K	8.11%	8.15%	6.14%	5.74%	6.31%	7.41%	3.51%	2.46%
	300K	6.56%	5.84%	7.03%	6.82%	3.28%	3.65%	4.69%	5.30%
	350K	6.25%	5.30%	8.09%	8.05%	2.34%	2.65%	3.68%	4.03%
	400K	7.14%	7.10%	6.12%	7.64%	5.71%	4.14%	5.44%	5.73%
	450K	6.96%	7.73%	7.32%	8.57%	3.16%	5.15%	6.10%	4.57%
	500K	5.23%	4.74%	7.10%	8.42%	2.91%	2.59%	6.01%	6.44%
16nm	200K	7.91%	7.72%	7.33%	6.06%	3.39%	3.68%	3.14%	3.03%
	250K	17.80%	7.69%	7.22%	8.00%	3.14%	3.34%	3.61%	6.22%
	300K	8.10%	7.18%	7.73%	7.08%	5.71%	5.80%	4.72%	2.08%
	350K	8.82%	7.35%	7.19%	6.67%	7.56%	3.32%	6.83%	5.10%
	400K	6.37%	7.59%	7.79%	8.10%	1.99%	3.38%	2.80%	4.23%
	450K	8.41%	7.21%	7.96%	8.58%	4.53%	4.92%	4.24%	5.03%
	500K	7.83%	5.82%	7.01%	6.67%	3.13%	2.45%	3.04%	2.47%

Figure 5.6 represents a detailed delay comparison of mixed (multi and double-walled) CNT structures excluding crosstalk, with even and out-phase modes of dynamic crosstalk switching at 32nm, 22nm, and 16nm technology nodes. It has been noticed that the delay for the even mode of dynamic crosstalk switching is lower than the odd mode of switching and it remains valid for four structures. It is because the time of flight in even mode ($t_e = l\sqrt{CL}$) is less as

compared to the time of flight estimated during the odd mode ($t_o = l\sqrt{(C + C_{coupled})L}$). As a result, the output voltage is reached a little early for in-phase mode. So, the delay for in-phase is comparably less than odd modes over the whole temperature range at all technologies.

5.1.2 Functional Crosstalk

Block diagrams representing four cases of functional crosstalk are shown in Figure 5.7. Functional crosstalk exists when victim and aggressor lines switch differently and thus impacts the performance by introducing unwanted glitches in the output voltage waveform [110]. The values of glitches for various cases at different technologies and temperature points are mentioned in Table 5.3.

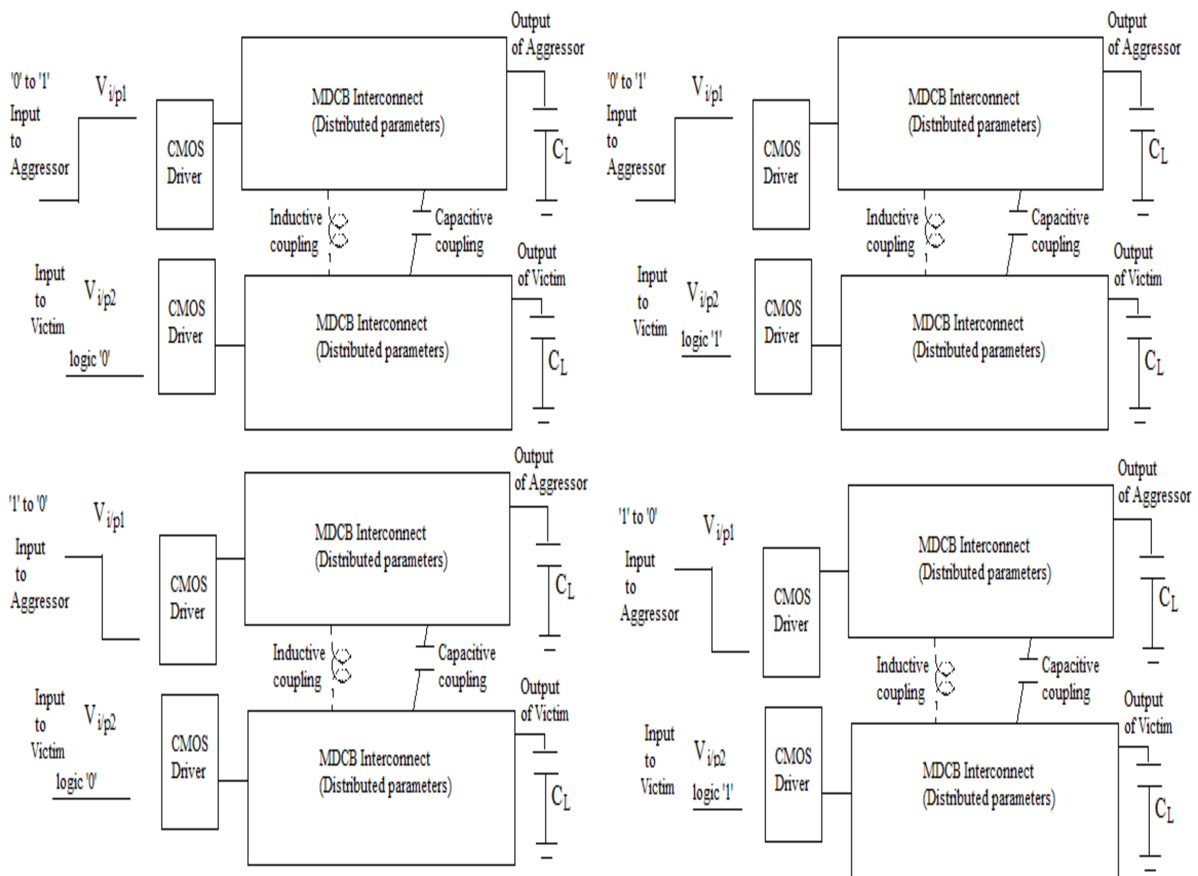


Figure 5.7 Four cases of functional crosstalk of MDCB coupled interconnects.

Table 5.3 Glitch values of mixed CNT coupled interconnects.

	Switching activity							
	Aggressor line	Victim line	Impact	MDCB 1	MDCB 2	MDCB 3	MDCB 4	Glitch
32nm	0 to 1	0	Functionality	51	89	80	74	Positive Glitch (mv)
	0 to 1	1	Reliability	684	714	704	693	Overshoot (mv)
	1 to 0	0	Reliability	36	65	58	55	Undershoot (mv)
	1 to 0	1	Functionality	680	722	693	669	Negative Glitch (mv)

22nm	0 to 1	0	Functionality	37	79	69	64	Positive Glitch (mv)
	0 to 1	1	Reliability	661	697	686	675	Overshoot (mv)
	1 to 0	0	Reliability	25	59	47	43	Undershoot (mv)
	1 to 0	1	Functionality	674	706	682	667	Negative Glitch (mv)
16nm	0 to 1	0	Functionality	22	64	49	45	Positive Glitch (mv)
	0 to 1	1	Reliability	592	632	618	612	Overshoot (mv)
	1 to 0	0	Reliability	11	40	24	21	Undershoot (mv)
	1 to 0	1	functionality	536	574	548	543	Negative Glitch (mv)

Functional crosstalk induces an undesirable voltage glitch at the output side of the victim to interconnect as listed in Table 5.3. It is also observed that MDCB-1 attains the lowest value of glitch for all transitions when compared to the other MDCB structures. The difference in percentage in glitch values of MDCB 2-4 with relation to MDCB 1 at 32nm, 22nm, and 16nm technologies are also mentioned in Table 5.4 below.

Table 5.4 Functional crosstalk noise values (percentage difference) of MDCB-1 structure with other structures.

	Aggressor line	Victim line	w.r.t. MDCB-2	w.r.t. MDCB-3	w.r.t. MDCB-4
32nm	0 to 1	0	42.72%	36.26%	31.09%
	0 to 1	1	4.21%	2.85%	1.31%
	1 to 0	0	44.63%	37.94%	34.56%
	1 to 0	1	5.83%	1.89%	1.65%
22nm	0 to 1	0	53.18%	46.39%	42.19%
	0 to 1	1	5.17%	3.65%	2.08%
	1 to 0	0	57.64%	46.82%	41.87%
	1 to 0	1	4.543%	1.18%	1.06%
16nm	0 to 1	0	65.61%	55.11%	51.12%
	0 to 1	1	6.34%	4.22%	3.28%
	1 to 0	0	72.6%	54.18%	47.63%
	1 to 0	1	6.63%	2.19%	1.29%

- Aggressor: 0 → 1 and Victim: 0

In this case of a positive glitch, there is a 42.72%, 53.18%, and 65.61% reduction for crosstalk noise values of MDCB 1 structure w.r.t mixed 2 structure, there is 36.26%, 46.39%, and 55.11% reduction for noise values of MDCB 1 structure w.r.t 3rd structure and there is 31.09%, 42.19% and 51.12% reduction for noise values of MDCB 1 structure concerning 4th structure at 32nm, 22nm, and 16nm technology respectively.

- Aggressor: 0 → 1 and Victim: 1

In this case of overshoot, there is a 4.21%, 5.17%, and 6.34% reduction of crosstalk values of MDCB 1 structure w.r.t 2nd mixed structure, there is 2.85%, 3.65%, and 4.22% reduction of

crosstalk values of MDCB 1 structure w.r.t 3rd MDCB and there is 1.31%, 2.08% and 3.28% reduction of crosstalk values of MDCB 1structure w.r.t 4th at 32nm, 22nm, and 16nm technology respectively.

- Aggressor: 1 → 0 and Victim: 0

Here for undershoot, there is 44.63%, 57.64%, and 72.6% reduction of noise values of MDCB 1 structure w.r.t 2nd MDCB structure, there is 37.94%, 46.82% and 54.18% reduction of values of MDCB 1 structure w.r.t 3rd MDCB structure and there is 34.56%, 41.87% and 47.632% reduction of noise values of MDCB 1 structure w.r.t MDCB 4 at 32nm, 22nm, and 16nm technology respectively.

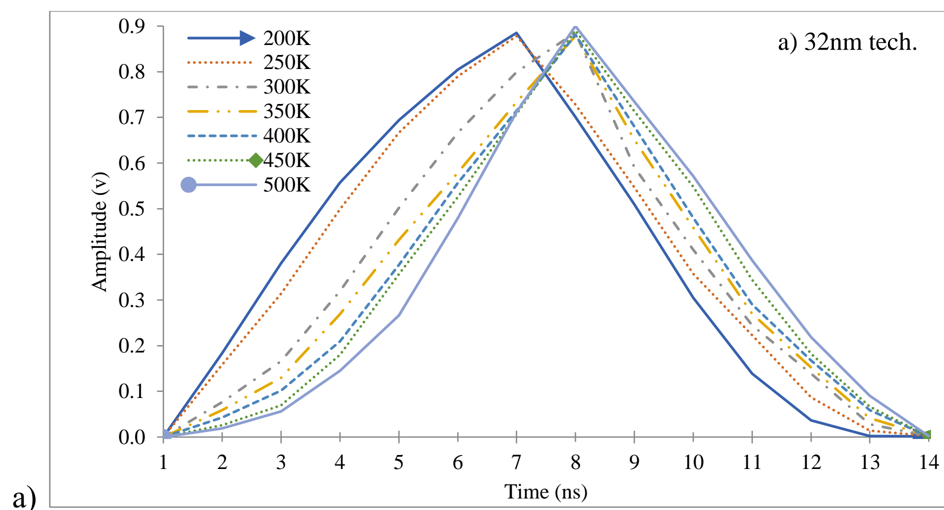
- Aggressor: 1 → 0 and Victim: 1

There is a 5.83%, 4.54%, and 6.63% reduction for crosstalk noise of MDCB 1 structure w.r.t MDCB 2, there is a 1.89%, 1.18%, and 2.19% reduction for crosstalk noise of MDCB 1 structure w.r.t MDCB 3 and there is 1.65%, 1.06% and 1.29% reduction for crosstalk noise of MDCB 1 structure w.r.t MDCB 4 at 32nm, 22nm, and 16nm technology respectively.

In this manner, functional crosstalk deteriorates the working of the integrated circuit. The positive and negative glitches influence the functioning of the circuit and overshoot and undershoot impact the reliability of the circuit.

5.2 Role of Temperature

It is evident from the results shared in the previous section that the global interconnect delay of the circuit increases due to dynamic crosstalk. To observe the effect of temperature on crosstalk, simulations are performed for variable temperature points at 32nm, 22nm, and 16nm nodes [114]. Figure 5.8 demonstrates crosstalk-induced output waveforms of MDCB 1 interconnect at a wide temperature range for 1000μm interconnect length.



a)

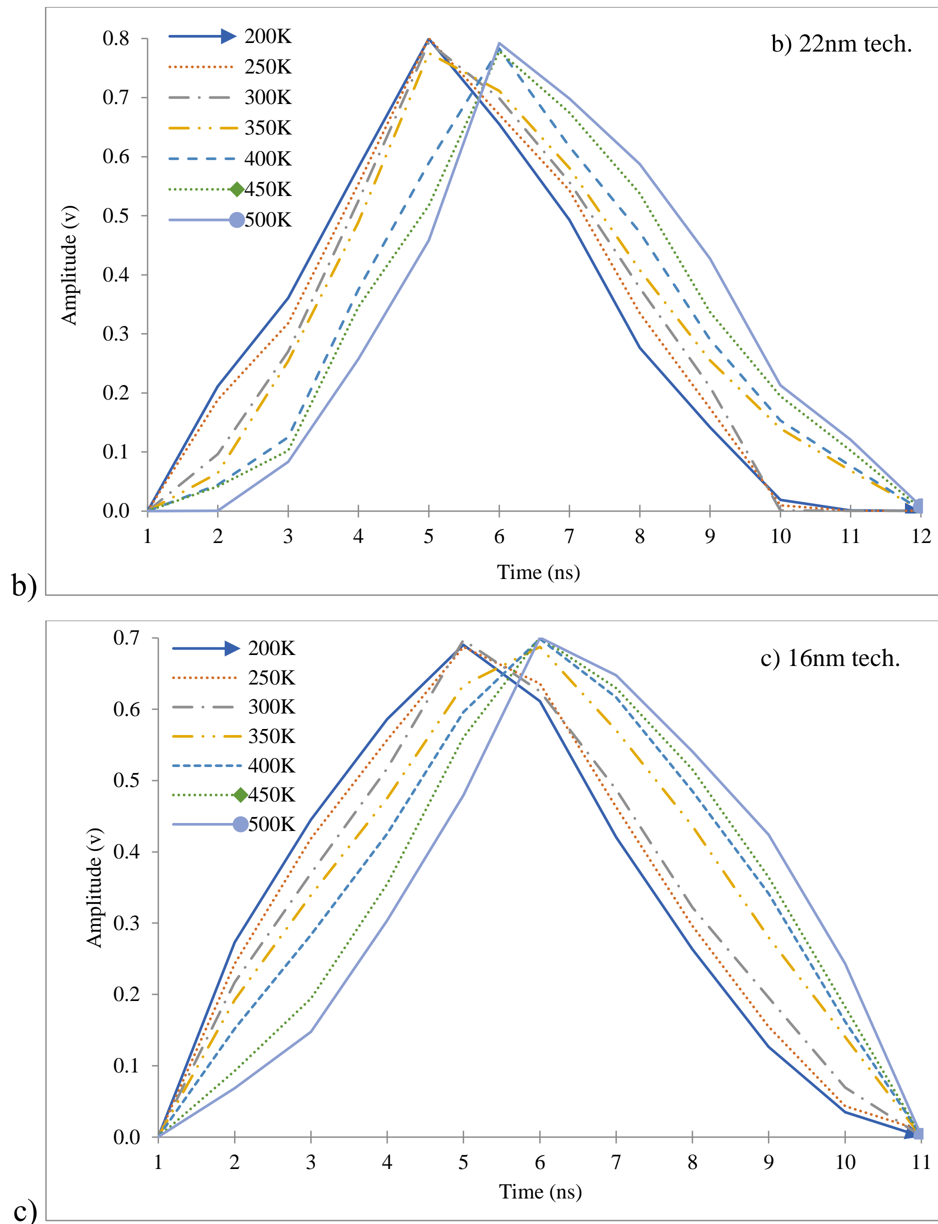


Figure 5.8 Dynamic crosstalk influenced the transient response of MDCB 1 structure for 1000µm length a) at 32nm tech. b) at 22nm tech. c) 16nm tech. the node at 200K-500K.

The dynamic crosstalk-influenced transient response at the output end of the victim is shown in Figure 5.8. Both aggressor and victim lines are assumed to be switching from 0 to 1 for different technologies. Operating temperature and resistance of material show a direct relationship. Also, as the scattering in material increases, MFP decreases, and vice versa. So, with a decrease in MFP and an increase in line resistance, the signal delay increases. It is seen from Figure 5.8 that the waveform for temperature 500 K gives a delayed response than others and the waveform with less temperature gives a comparatively quicker response. This is because the more the temperature, the more resistance due to increased scatterings and therefore more delays.

5.3 Stability analysis

Stability is also an important component that helps in examining the electrical performance of interconnects [115,116,123]. In this section, the time domain output waveform for interconnects is analyzed. Also, parameters like maximum overshot in percentage and rise time are evaluated. The relative stability study of mixed CNTs is also analyzed with Nyquist plots for a wide temperature range.

5.3.1 Transient response of mixed CNTs

The expression to find out the output voltage of a distributed transmission interconnect line can be given by equation (5.3) [116].

$$V_{out}(s) = \frac{1}{A+sC_L B} . V_{in}(s) \tag{5.3}$$

Coefficients A and B are given in equations (5.4) and (5.5) respectively. The parameters r_{esc}, $l_{esc,}$ and c_{esc} are the equivalent resistance, inductance, and capacitance of interconnect respectively. Also, R_{dr}, C_{dr}, n, x, and C_L represent driver resistance, driver capacitance, number, length of segments of interconnect, and the load capacitance respectively.

$$A = s^2 \left[\frac{l_{esc}c_{esc}(nx)^2}{2} + \frac{r_{esc}^2 c_{esc}^2 (nx)^4}{4!} + \frac{r_{esc}R_{dr}c_{esc}C_{dr}(nx)^2}{2} + \frac{r_{esc}c_{esc}^2(nx)^3(R_1+R_{dr})}{3!} + R_1 R_{dr} C_{dr} c_{esc}(nx) \right] + s\left[\frac{r_{esc}c_{esc}(nx)^2}{2} + R_{dr}C_{dr} + c_{esc}(nx)(R_1 + R_{dr}) \right] + 1 \tag{5.4}$$

The time-domain output waveforms of mixed bundle CNT structures (MD 1, MD 2, MD 3, and MD 4) modeled as distributed transmission lines at 1000µm length for temperatures ranging from 200 Kelvin to 500 Kelvin at various technology nodes are shown in the Figures 5.9-5.11 below.

$$B = s^2 \left[(2R_1 + R_{dr}) \left(\frac{l_{esc}c_{esc}(nx)^2}{2} + \frac{r_{esc}^2 c_{esc}^2 (nx)^4}{4!} \right) + R_1 R_{dr} r_{esc} c_{esc} C_{dr} (nx)^2 + \frac{2 r_{esc} l_{esc} c_{esc} (nx)^3}{3!} + \frac{r_{esc}^3 c_{esc}^2 (nx)^5}{5!} + \frac{R_1^2 r_{esc} c_{esc}^2 (nx)^3}{3!} + \frac{r_{esc}^2 R_{dr} C_{dr} c_{esc} (nx)^3}{3!} + R_{dr}C_{dr}(l_{esc} + R_1^2 c_{esc})(nx) \right] + s \left[r_{esc}c_{esc}(nx)^2(2R_1 + R_{dr}) + 2R_1 R_{dr} C_{dr} + \frac{r_{esc}^2 c_{esc}(nx)^3}{3!} + l_{esc}(nx) + R_1^2 c_{esc}(nx) + r_{esc}R_{dr}C_{dr}(nx) + R_1 R_{dr} c_{esc}(nx) \right] + \left(2R_1 + R_{dr} + r_{esc}(nx)\right) \tag{5.5}$$

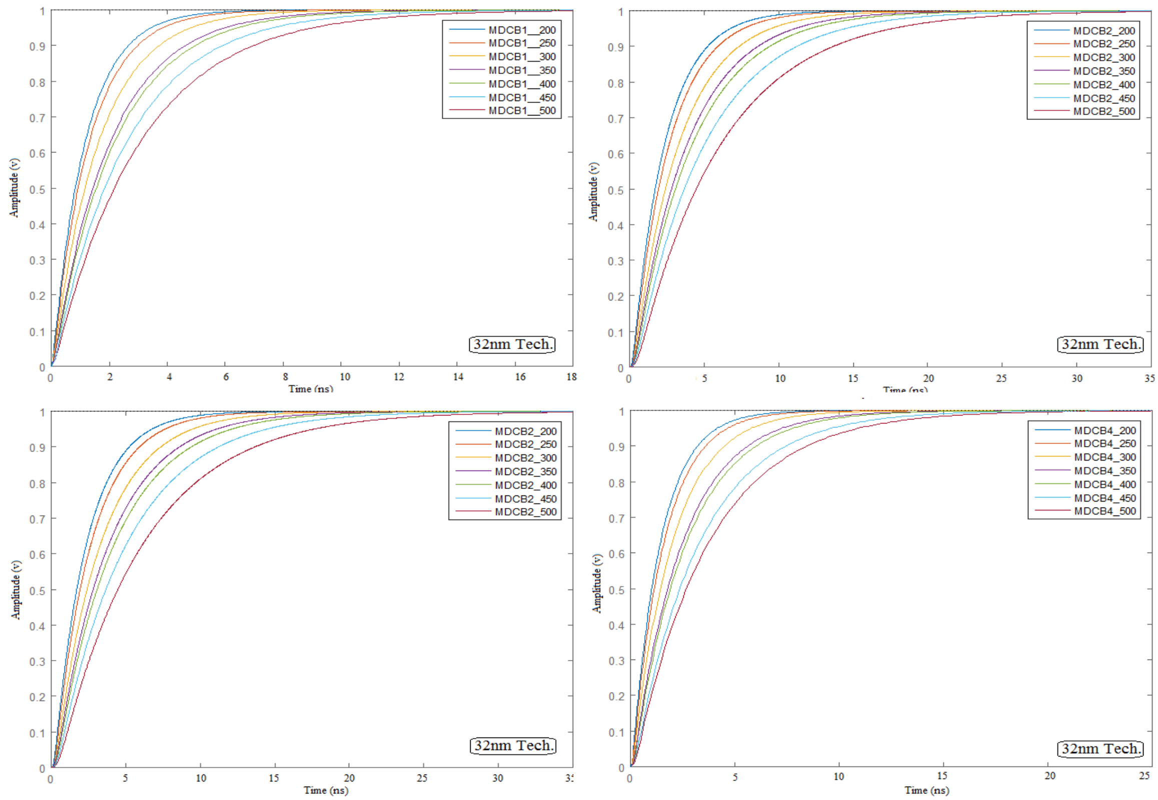


Figure 5.9 Transient response for four MDCB structures operating at temperatures ranging from 200K-500K for 32nm technology node

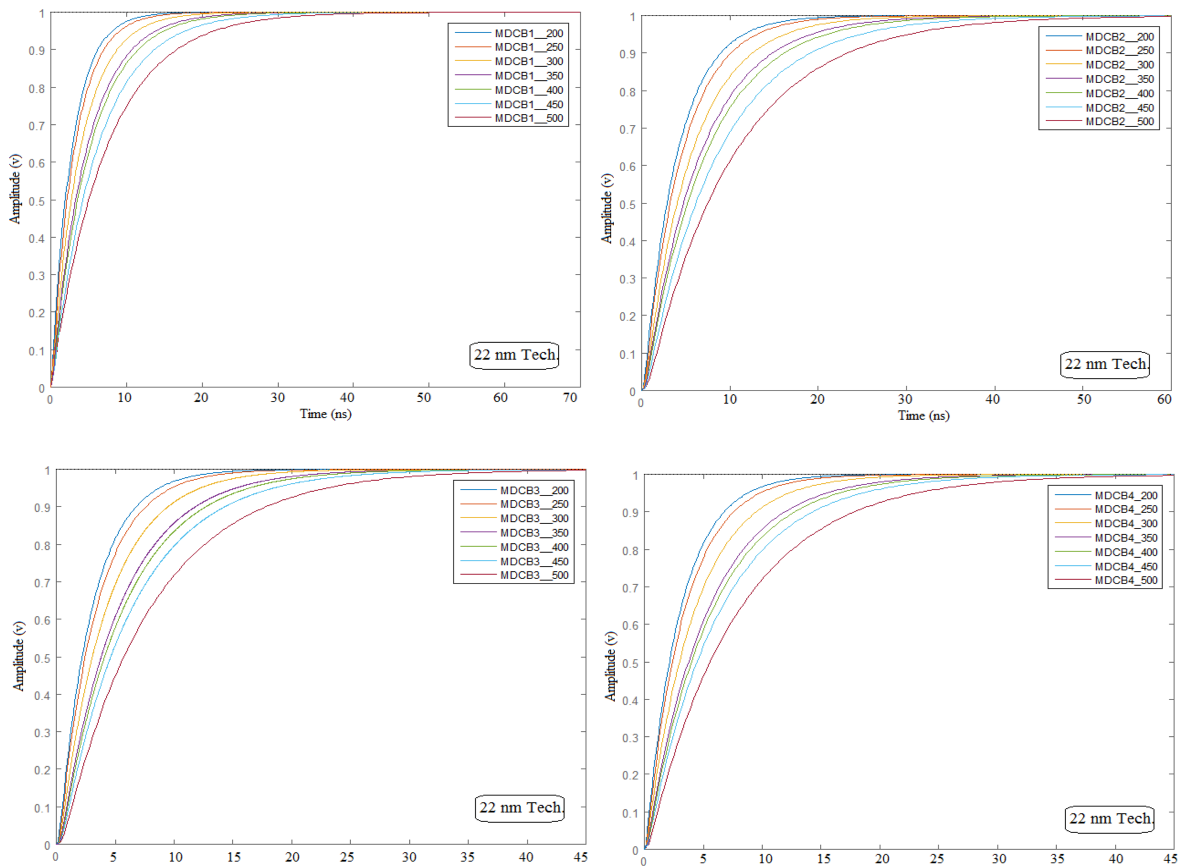


Figure 5.10 Transient response for four MDCB structures operating at temperatures ranging from 200K-500K for 22nm technology node

The values extracted from equations (5.3-5.5) are then used to plot their responses in MATLAB software. And it is seen in figures 5.9-5.11 that no overshoot exists for any mixed CNT bundle interconnect at all nodes and temperature points. They all tend to move towards equilibrium gradually. Or it can be read as that for 1000µm length, their output response tends to damp rapidly.

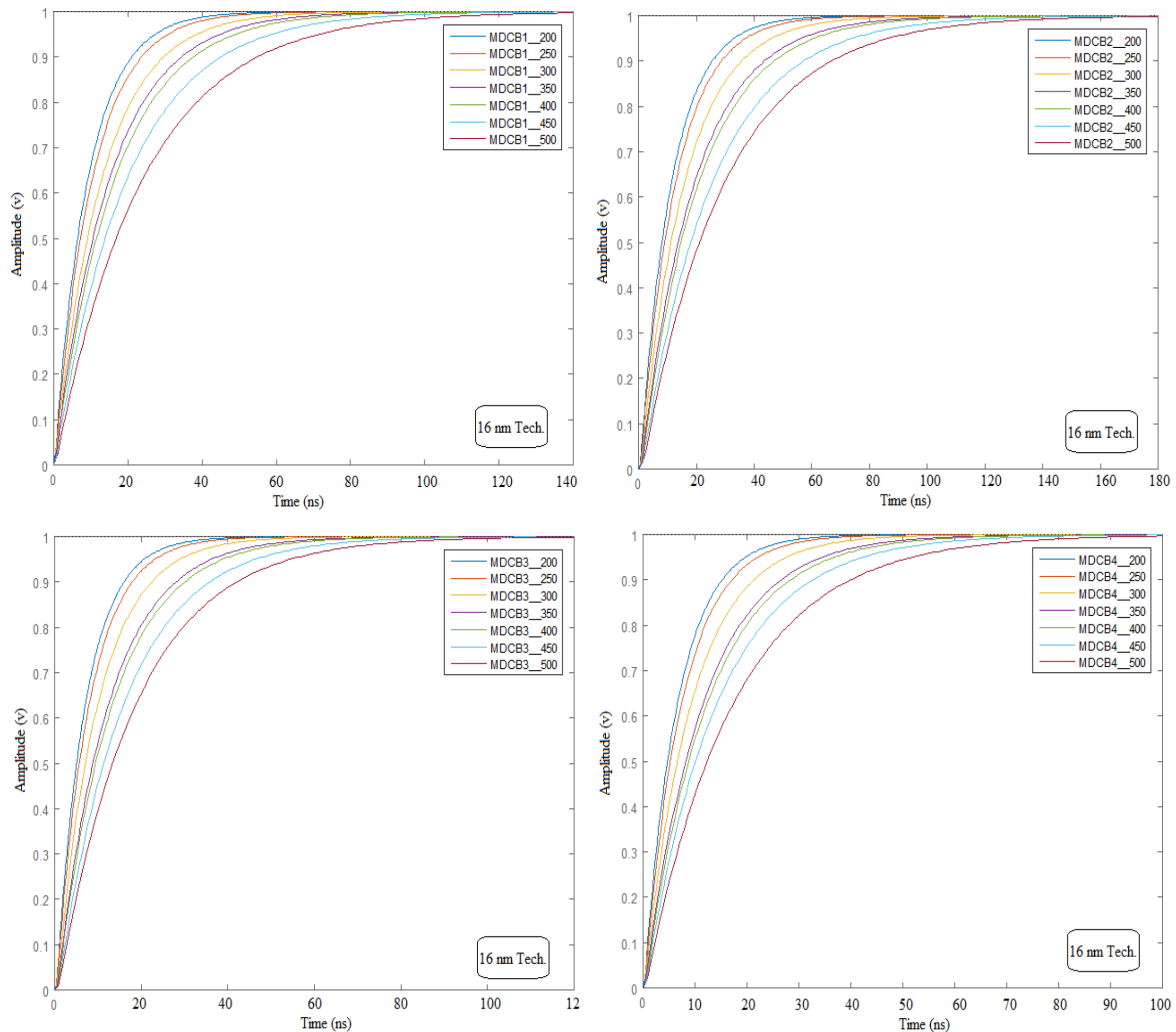


Figure 5.11 Transient response for four MDCB structures operating at temperatures ranging from 200K-500K for 16nm technology node

Of all structures again MDCB 1 interconnect shows a minimum delay to reach the final position than the rest three mixed bundles. The damping also tends to rise with the temperature rise. It is also noticed that the response waveform for 500K shows a delayed response than 450K and so on due to the obvious fact that the increased temperature delays the response due to increases scatterings and resistance. However, after studying the response graphs of four mixed structures at various nanotechnology nodes it is stated that within a span of nanoseconds, they are all reaching their final state successfully.

5.3.2 Maximum overshoot and rise-time.

This part of the chapter primarily focuses on the values of maximum overshot voltage (M_p) and rise time (T_r) of mixed CNT interconnects [116,123]. Their exact definitions and mathematical equations to determine these parameters are mentioned below.

- Peak overshoot or maximum overshoot voltage ($\%M_p$)

It is said to exist in response waveform when the value of the output signal shoots or exceeds the final/steady value. So, it is calculated by taking the difference between the first peak value of the output and the final stage value of the response. And the time of occurrence of this first peak when overshoot occurs is called peak time. With ξ as the damping coefficient, ω_n as the natural frequency of the signal, and *n* as the number of cycles respectively [116], the expression to calculate maximum overshoot voltage is given by equation (5.6).

$$\%M_p = e^{\frac{-(2n-1)\pi\xi}{\sqrt{1-\xi^2}}} .100\% \tag{5.6}$$

- Rise Time (T_r)

It is the time consumed by the output waveform to reach from 10% value to 90% of the final output value and is expressed by equation (5.7).

$$T_r = \frac{\pi - cos^{-1}\xi}{\omega_n\sqrt{1-\xi^2}} \tag{5.7}$$

ξ denotes the damping factor of the signal. The values of the damping factor are determined from equation (5.8) given below.

$$\xi = \frac{r_t}{2}\sqrt{\frac{c_t}{l_t}}.\frac{r_T+c_T+r_Tc_T+0.5}{(1+c_T)} \tag{5.8}$$

With *l* as the length of interconnect, $r_t=r_{esc}.l$, $c_t=c_{esc}.l$ and $l_t=l_{esc}.l$. Also, $c_T = \frac{C_L}{c_t}$ and $r_T = \frac{R_{dr}}{r_t}$.

The natural frequency is expressed by equation (5.9) below.

$$\omega_n = \frac{1}{\sqrt{l_t(c_t+C_L)}} \tag{5.9}$$

The values of driver resistance (R_{dr}) are taken as 12.13 KΩ (at 32nm), 16.67 KΩ (at 22nm), and 18.33KΩ (at 16nm) for nano-regime nodes. Similarly, the values of driver capacitance (C_{dr}) are taken as 0.081fF, 0.049fF, and 0.030fF for different nodes respectively. Equations (5.6-5.9) help to determine the maximum overshoot and rise time for MDCB structures at variable temperature points.

Table 5.5 lists the value of peak overshoot and delay time of mixed CNT bundles at various technology nodes.

Table 5.5 Maximum percentage overshoot and switching delay for MDCB structures at 32nm, 22nm, and 16nm technology nodes

		32nm tech.			22nm tech.			16nm tech.		
		ξ	$\%M_p$	T_r (ns)	ξ	$\%M_p$	T_r (ns)	ξ	$\%M_p$	T_r (ns)
MDCB 1	(200K)	0.44	0	0.10	0.64	0	0.20	1.19	0	0.80
	(250K)	0.49	0	0.11	0.72	0	0.22	1.33	0	1.39
	(300K)	0.59	0	0.12	0.90	0	0.31	1.66	0	1.62
	(350K)	0.73	0	0.15	1.13	0	0.49	2.03	0	1.86
	(400K)	0.78	0	0.17	1.21	0	0.65	2.19	0	2.08
	(450K)	0.98	0	0.25	1.35	0	0.89	2.67	0	2.47
	(500K)	1.11	0	0.37	1.68	0	0.97	3.11	0	2.84
MDCB 2	(200K)	0.39	0	0.20	0.55	0	0.29	0.83	0	1.44
	(250K)	0.44	0	0.21	0.62	0	0.33	0.94	0	1.69
	(300K)	0.54	0	0.24	0.77	0	0.58	1.16	0	1.83
	(350K)	0.63	0	0.28	0.90	0	0.73	1.35	0	2.35
	(400K)	0.69	0	0.31	0.99	0	2.02	1.48	0	2.79
	(450K)	0.83	0	0.43	1.17	0	2.56	1.78	0	3.12
	(500K)	1.01	0	0.70	1.43	0	2.89	2.16	0	3.46
MDCB 3	(200K)	0.40	0	0.13	0.57	0	0.22	0.93	0	0.94
	(250K)	0.44	0	0.14	0.64	0	0.25	1.05	0	1.54
	(300K)	0.55	0	0.17	0.79	0	0.36	1.31	0	1.76
	(350K)	0.69	0	0.20	0.97	0	0.57	1.63	0	1.98
	(400K)	0.74	0	0.23	1.05	0	0.83	1.75	0	2.39
	(450K)	0.92	0	0.42	1.24	0	0.95	2.09	0	2.84
	(500K)	1.04	0	0.61	1.48	0	1.48	2.46	0	3.09
MDCB 4	(200K)	0.42	0	0.12	0.59	0	0.21	0.94	0	0.93
	(250K)	0.47	0	0.13	0.66	0	0.23	1.05	0	1.47
	(300K)	0.58	0	0.16	0.82	0	0.35	1.32	0	1.71
	(350K)	0.72	0	0.19	1.03	0	0.56	1.64	0	1.95
	(400K)	0.76	0	0.21	1.10	0	0.81	1.76	0	2.21
	(450K)	0.95	0	0.40	1.24	0	0.92	2.02	0	2.66
	(500K)	1.10	0	0.59	1.55	0	1.37	2.47	0	2.98

MDCB structures have no value of maximum overshoot voltage at all technologies. It can also be visualized from response waveforms shown in section 5.3.1. The higher value of ξ i.e., the damping factor will tend to dampen the response waveform to the final state rapidly. It is observed from the values noted in Table 5.5 that the first mixed CNT structure has the highest value of damping factor than the rest of the three mixed structures. Also, it has been seen that the system with the least value of switching delay (thus taking minimum time to reach final output) and zero value of overshoot will damp the waveform more quickly and thus, will be comparatively more stable. As mentioned in the table it is also observed that the rise time of structures increases with the increase in temperature. MDCB 1 structure with no maximum percentage overshoot and minimum rise time yields the best results than the rest to obtain the final value. It is also relatively quicker than others, making such interconnect material highly recommendable for high-speed applications.

5.3.3 Nyquist Plots

These are plots in which the real parts are plotted on the horizontal (x) axis and the imaginary parts are plotted on the vertical (y) axis respectively [115,116]. Stability is found by calculating the number of encircles around the crucial point (*-1,j0*).

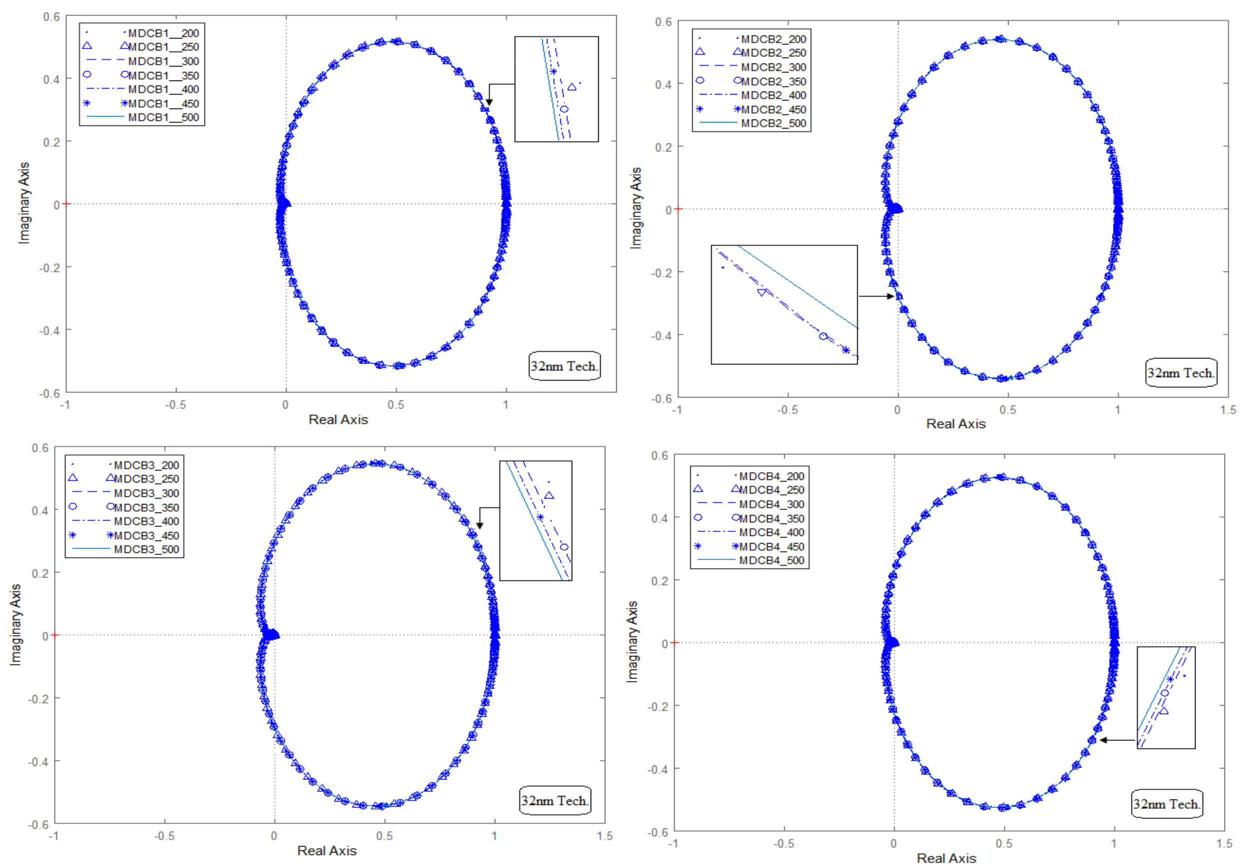


Figure 5.12 Nyquist plot of four MDCB structures for 1000µm interconnect length at 32nm technology node

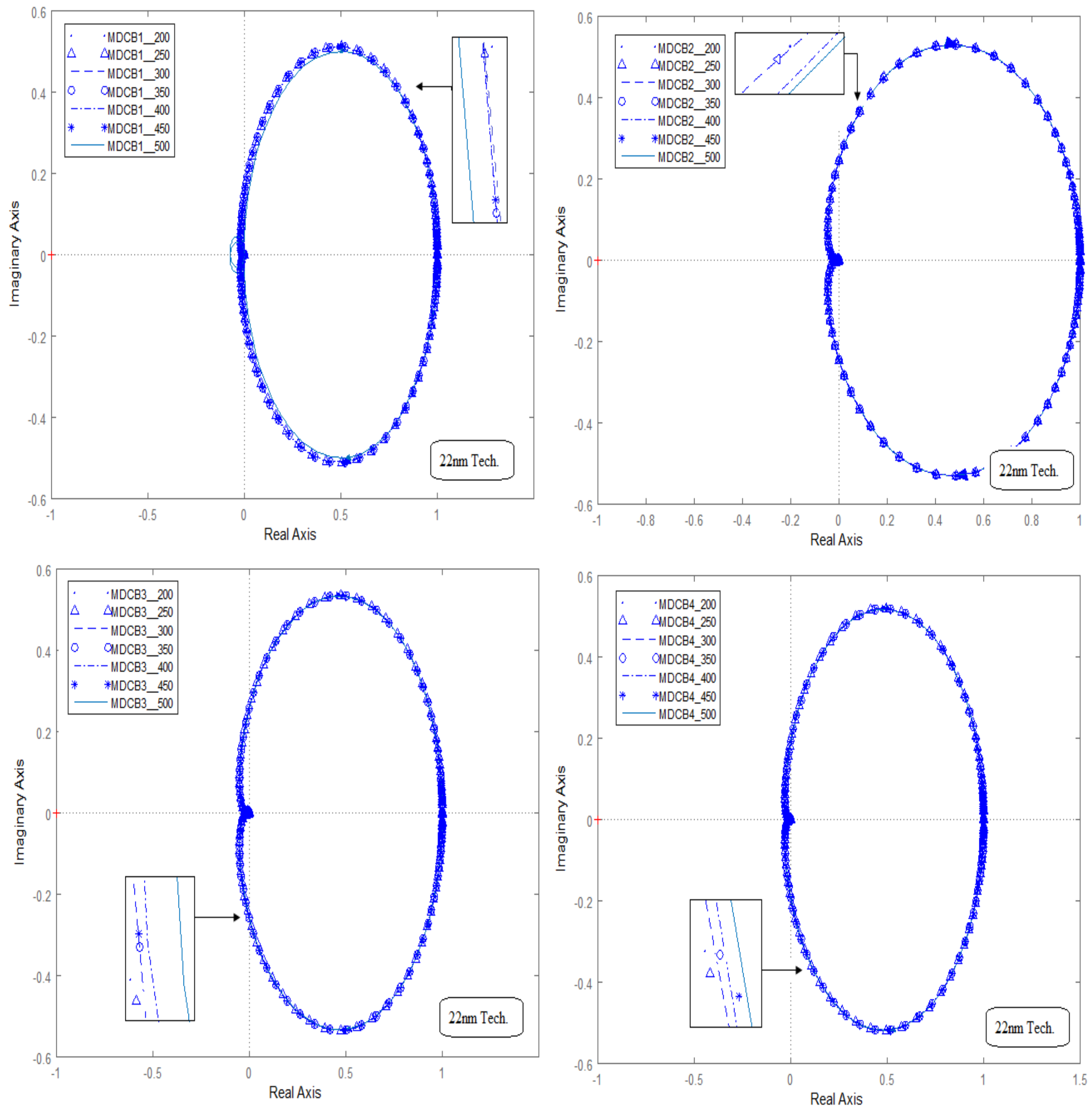


Figure 5.13 Nyquist plot of four MDCB structures for 1000µm interconnect length at 22nm technology node

To examine relative stability, Nyquist plots are plotted for various multi and double-CNT bundle structures using equation (5.3) with temperatures ranging from 200-500K and at different technology nodes and are displayed in Figure 5.12-5.14.

At advanced technology nodes and high temperatures, electrons in the material undergo many elastic and inelastic collisions, as a result, their mean free path is reduced. Due to their decreased MFP the resistance of interconnect increases which also increases circuit delay. As shown in plots for different technology nodes at global length and wide temperature range all MDCB structures tend to slip away from the final point (*-1,j0*). This makes all mixed structures stable.

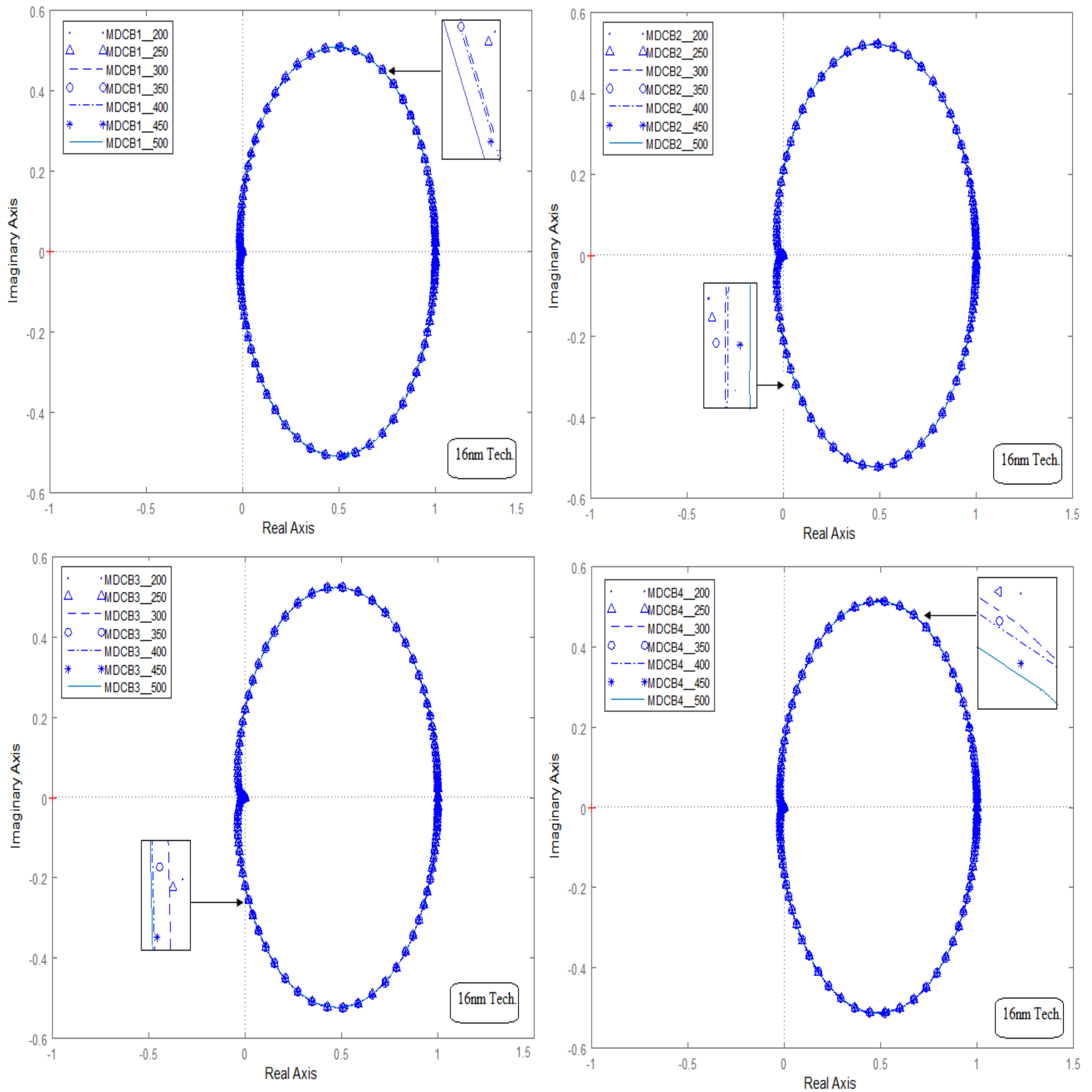


Figure 5.14 Nyquist plot of four MDCB structures for 1000µm interconnect length at 16 nm technology node

For a better understanding of mixed structures at different temperature points, the sections of the Nyquist plot are shown clearly through the zoom window provided along with each of them. The line for 200K lies outside and as the temperature increases the line lies in the inner side. So, as the temperature rises, the resistance upsurges which further enhances the stability of the interconnect structure.

5.4 Chapter Summary and Contribution

At nano-regime technology nodes, long interconnect wires lie close to each other. While operating at high frequencies, they influence the working of each other. Interconnect lines face

capacitive and inductive couplings. This unwanted crosstalk effect plays a critical role in estimating the performance of interconnects and it can't be left out. Based on the kind of activity in interconnect lines, two types of crosstalk effects can exist. If coupled lines switch synchronously, then dynamic crosstalk exists, and it introduces an additional delay in the circuit. If one line remains passive and the other line shows some activity, then a functional crosstalk effect is encountered. In this scenario, an unwanted spike is observed in the output waveform which affects the reliability of interconnects. As the temperature increases, the crosstalk-induced waveform shows more delay. Crosstalk among interconnect lines disturbs the operation of the circuit either by increasing delay, changing functionality, or hitting the reliability of the circuit. This undesirable effect must be considered for the better design of interconnects.

A stability analysis of multi and double-wall CNT bundle interconnects is presented. The transient output waveforms for mixed interconnects are plotted and studied and it is observed that all waveforms tend to damp quickly with the increase in temperature and reach their final value. Also, mathematical expressions for determining output waveform, maximum overshoot in percentage, and rise time are given. For all mixed CNTs, the value of overshoot remains zero, and rise time lies within permissible limits. To study stability, different Nyquist plots are also plotted for MDCB structures at three technologies.

Related Publication:

1. Gurleen Dhillon and Karmjit Singh Sandha, "Stability-and Crosstalk-Based Performance of Multi-and Double-walled Mixed CNT Bundles as Interconnect for Next-Generation Technology Nodes," *Journal of Circuits, Systems, and Computers*, vol. 31, no. 5, p. 2250098, 2022. *(Impact Factor- 1.278)* (SCI indexed)
2. Gurleen Dhillon and Karamjit Singh, "Impact of Functional Crosstalk on Mixed CNT Bundles for Future VLSI Nodes," *Materials Today: Proceedings (Elsevier),* 2023 (Scopus indexed)

6. Comparative Analysis and Analytical Modeling of MDCB structures

This chapter presents a comparative analysis of MDCB structures with mixed structures mentioned in the literature. The comparison concludes the performance of MDCB structures was better than the existing ones. Also, it focuses on analytical formulations and calculations to determine the $T_{90\%}$ delay of mixed CNT interconnects.

6.1 Comparison of proposed MDCB structures with literature

Figure 6.1 shows a different variety of mixed bundle structures. As displayed in Figure 6.1, the above structures are developed by changing the locations of MWCNTs and DWCNTs, and the bottom four structures are formed with MWCNTs and SWCNTs (MSCB). The impedance parameters and performance of MSCB structures are presented in existing literature [98].

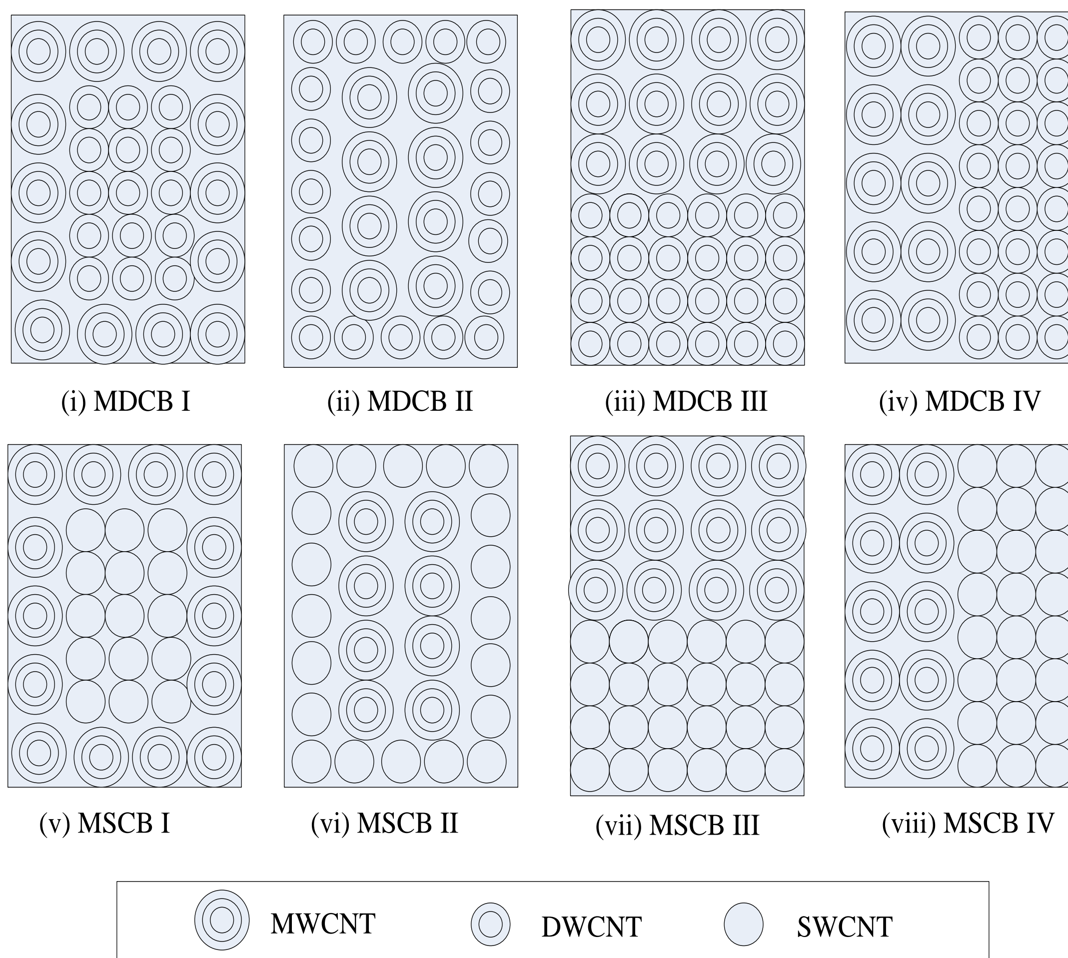


Figure 6.1 Various types of Mixed CNT structures (multi and double-wall CNT bundles (MDCB) and multi and single-wall CNT bundles (MSCB))

Tanner simulations are performed to determine the delay of all eight mixed CNTs at 22nm technology nodes for 1000µm interconnect length. Table 6.1 depicts the values of delay of all eight structures. The graphical representation of these values is plotted in Figure 6.2.

Table 6.1 Values of delay for mixed CNT structures

Delay (ns) at 22nm Tech.			
MSCB I	1.312	MDCB I	1.1912
MSCB II	2.263	MDCB II	1.2852
MSCB III	1.994	MDCB III	1.2404
MSCB IV	1.53	MDCB IV	1.2626

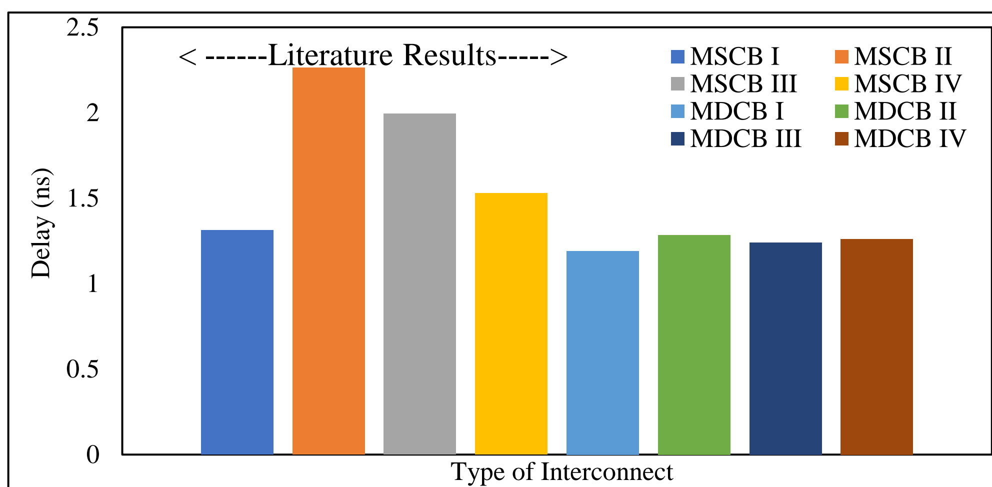


Figure 6.2 Propagation delay for various mixed CNT bundle structures at 22nm technology node for 1000µm interconnect length

It has been concluded in the literature for MSCBs, the structure with MWCNTs on the periphery and SWCNTs in the middle of the bundle performs the best by giving minimum delay than the other three structures. A similar trend has been observed for the MDCB 1 structure (with large diameter MWCNTs on edges and conductive DWCNTs in the center of the bundle) and concluded in previous chapters. From Figure 6.2 on comparing all eight mixed CNT structures, further, it has been recognized that structures formed with MWCNTs and DWCNTs i.e., MDCB structures give lesser delay than MSCB structures.

The delay of the MDCB 1 structure continues to be the minimum value and thus becomes the most efficient interconnect material in terms of delay for global interconnect length. The comparison between MSCB and MDCB structures has been further extended in the next figures to determine temperature-dependent delay, power, and PDP comparisons at different VLSI nodes. Figure 6.3 presents temperature-dependent delays of different MDCB and MSCB structures over a wide temperature range for three nanotechnology nodes. Similarly, figure 6.4 marks the values of power dissipated for mixed CNT structures.

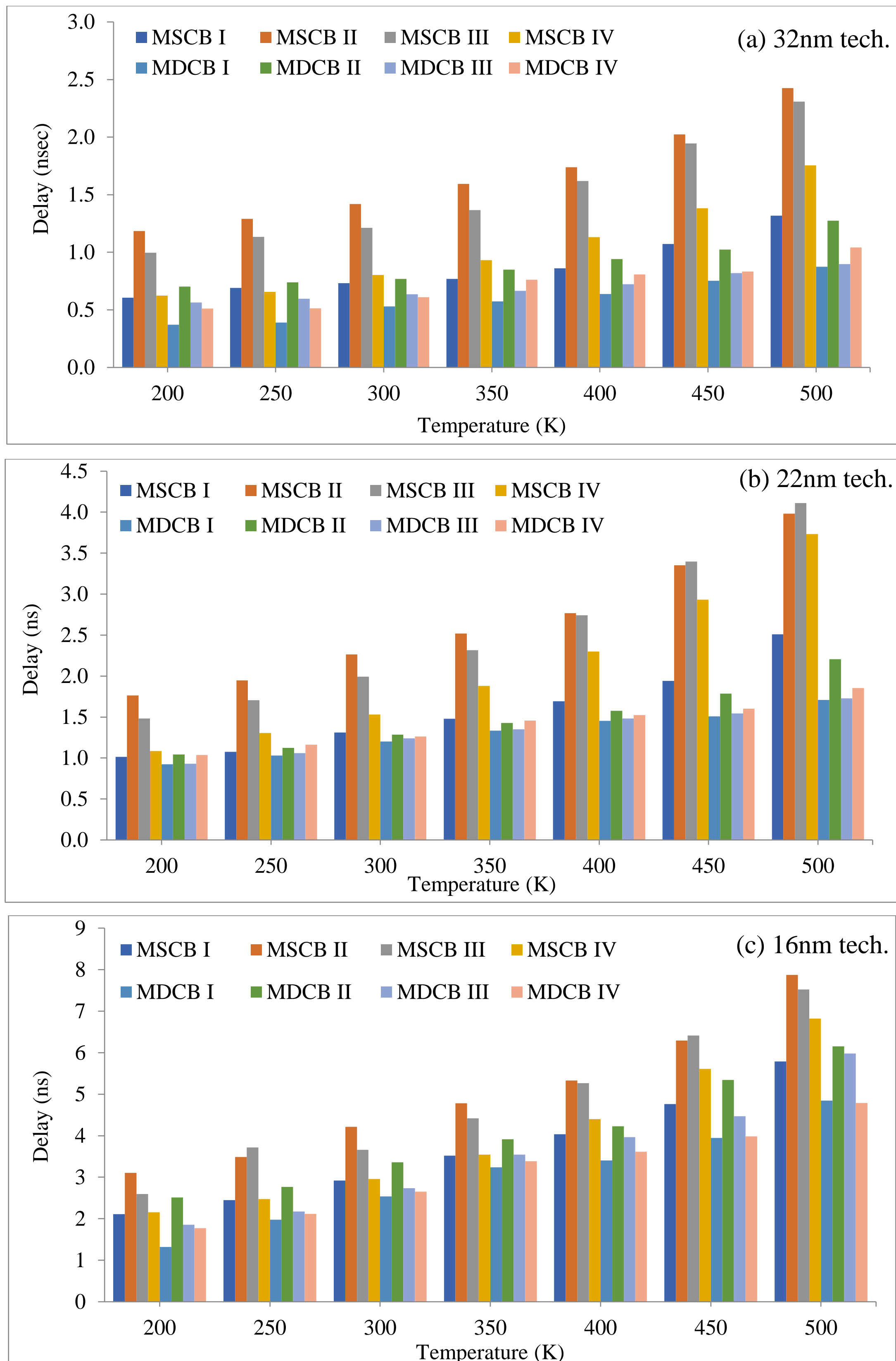


Figure 6.3 Temperature sensitive delay (ns) for various mixed CNT bundle structures (MDCBs and MSCBs) at (a) 32nm (b) 22nm and (c) 16nm technology node

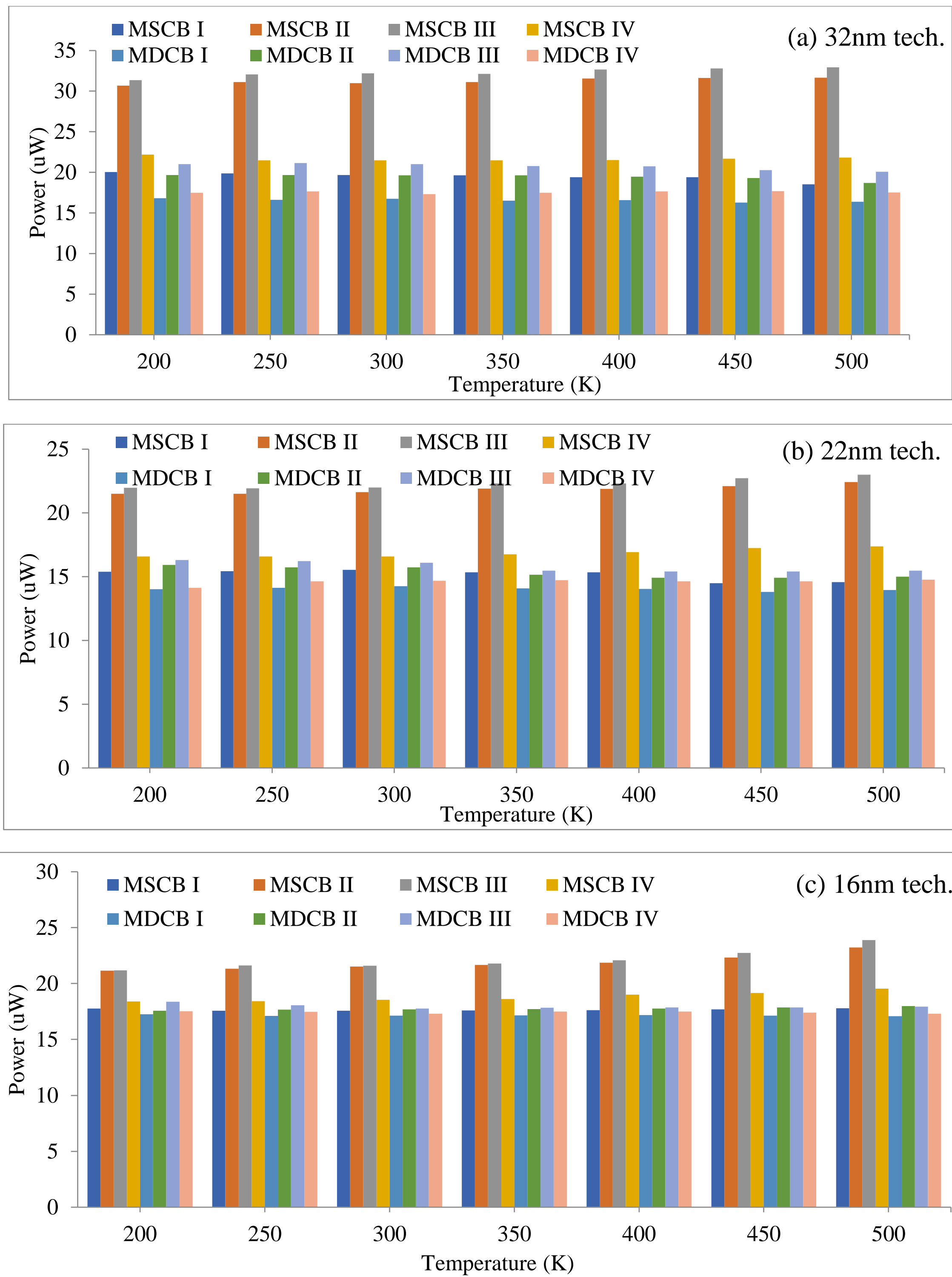


Figure 6.4 Temperature sensitive power for various mixed CNT bundle structures (MDCBs and MSCBs) at (a) 32nm (b) 22nm and (c) 16nm technology node

Figure 6.4 (a)-(c) demonstrates power dissipated for MDCB and MSCB structures for three nanotechnology nodes at global length. The structure formed by placing MWCNTs on the periphery gives the least capacitive effect. So, it (MDCB 1) offers minimum power dissipation than other structures.

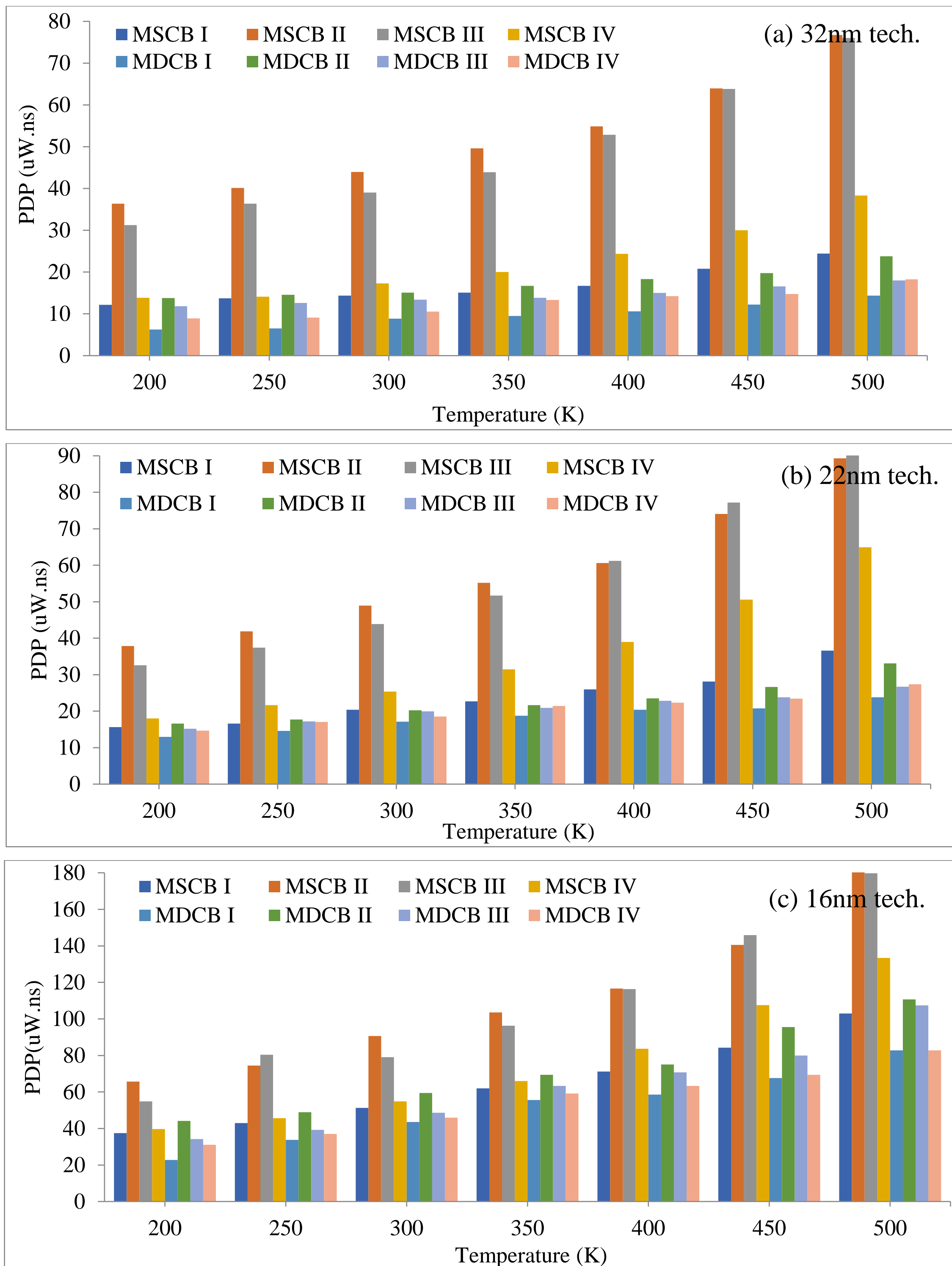


Figure 6.5 Temperature sensitive PDP for various mixed CNT bundle structures (MDCBs and MSCBs) at (a) 32nm (b) 22nm and (c) 16nm technology node

It can be viewed from Figure 6.5 (a)-(c) that the PDP values of MSCB structures are more than that of MDCB structures. The lower the value of the figure of the merit parameter i.e., the PDP (power-delay product) parameter; the better the interconnect performance. So, it can be stated that MDCB structures tend to perform better than a variety of mixed CNTs (multi and single-wall CNT bundles) existing in the literature.

6.2 Analytical delay modeling of mixed CNT bundle interconnects

This section presents the performance of interconnects modeled as distributed transmission lines based on the time response analysis of CMOS repeater circuits. The time consumed by the output waveform moving from 10% of the steady value to 90% of the final value is termed as $T_{90\%}$ [116] or vice-versa. The formulae to determine $T_{90\%}$ is given by equation (6.1).

$$T_{90\%} = \frac{2T_2 \ln\left[\frac{0.2\sqrt{4T_2 - T_1^2}}{T_1 + \sqrt{4T_2 - T_1^2}}\right]}{\left(\sqrt{4T_2 - T_1^2} - T_1\right)} \tag{6.1}$$

The coefficients T_1 and T_2 used in equation (6.1) are expressed below in equations (6.2) and (6.3) respectively.

$$T_1 = \left[\frac{r_{esc}c_{esc}(nx)^2}{2} + R_{dr}C_{dr} + c_{esc}(nx)(R_1 + R_{dr})\right] + C_L(2R_1 + R_{dr} + r_{esc}(nx)) \tag{6.2}$$

$$T_2 = \left[\frac{l_{esc}c_{esc}(nx)^2}{2} + \frac{r_{esc}^2 c_{esc}^2 (nx)^4}{4!} + \frac{r_{esc}R_{dr}c_{esc}C_{dr}(nx)^2}{2} + \frac{r_{esc}c_{esc}^2(nx)^3(R_1+R_{dr})}{3!} + R_1R_{dr}C_{dr}c_{esc}(nx)\right] + + C_L\left[\frac{r_{esc}c_{esc}(nx)^2}{2}(2R_1 + R_{dr}) + 2R_1R_{dr}C_{dr} + \frac{r_{esc}^2 c_{esc}(nx)^3}{3!} + l_{esc}(nx) + R_1^2 c_{esc}(nx) + r_{esc}R_{dr}C_{dr}(nx) + R_1R_{dr}c_{esc}(nx)\right] \tag{6.3}$$

The analytical delay obtained from the equations above is compared with the simulated delay of mixed bundle CNTs. Table 6.2 lists the analytical and simulated delay of all four MDCB interconnects at the 22nm technology node and is presented graphically in Figure 6.6. Figure 6.7 presents the comparison of simulated and analytical delays of mixed structures separately.

Table 6.2 Simulated and analytical delays for various MDCB structures at 22 nm node

Temperature (K)	MDCB 1 Simulated Delay (ns)	MDCB 1 Analytical Delay (ns)	MDCB 2 Simulated Delay (ns)	MDCB 2 Analytical Delay (ns)	MDCB 3 Simulated Delay (ns)	MDCB 3 Analytical Delay (ns)	MDCB 4 Simulated Delay (ns)	MDCB 4 Analytical Delay (ns)
200	0.58	0.49	1.14	1.06	0.96	0.80	1.06	1.02
250	0.78	0.65	1.24	1.17	1.07	1.01	1.15	1.07
300	0.96	0.91	1.33	1.29	1.19	1.13	1.23	1.09
350	1.05	1.02	1.43	1.31	1.25	1.22	1.37	1.21
400	1.20	1.14	1.57	1.42	1.38	1.30	1.45	1.32
450	1.37	1.25	1.79	1.55	1.52	1.37	1.60	1.44
500	1.43	1.37	2.21	1.89	1.70	1.42	1.85	1.67

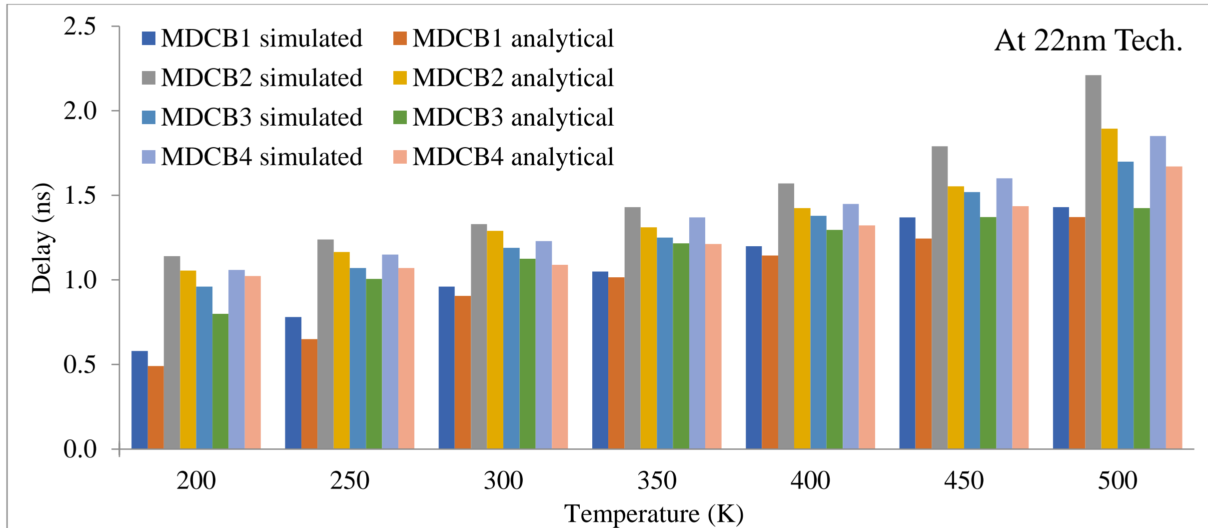


Figure 6.6 Simulated and analytical delay comparison of four mixed CNTs for 1000µm interconnect length at 22nm technology node

Figure 6.7 Delay comparisons of four mixed CNTs (MDCB 1, MDCB 2, MDCB 3and MDCB 4) for 1000µm interconnect length at 22nm technology node

Both simulated and analytical delay tends to increase with the increase in temperature. For better comparison, the graphs of individual structures of four mixed CNTs are plotted separately to view the difference between simulated and analytical data. As seen in Figure 6.7 simulated delay lines have more value and are lying above the analytical delay lines. However, the delay in analytical results lies near the simulated data for all MDCB structures.

Similarly, Table 6.3 reflects simulated and analytical delays for MDCB interconnects at 16nm technology. Figure 6.8 demonstrates the mixed interconnect delay results for 16nm technology.

Table 6.3 Simulated and analytical delays for various MDCB structures at 16 nm technology node

Temperature (K)	MDCB 1 Simulated Delay (ns)	MDCB 1 Analytical Delay (ns)	MDCB 2 Simulated Delay (ns)	MDCB 2 Analytical Delay (ns)	MDCB 3 Simulated Delay (ns)	MDCB 3 Analytical Delay (ns)	MDCB 4 Simulated Delay (ns)	MDCB 4 Analytical Delay (ns)
200	1.33	1.20	2.51	2.22	1.77	1.48	1.86	1.56
250	1.47	1.36	2.76	2.55	1.80	1.70	2.07	1.68
300	1.61	1.42	3.36	2.92	2.15	1.84	2.23	1.89
350	1.81	1.56	3.91	3.27	2.58	1.95	2.38	1.97
400	2.11	1.70	4.38	3.63	2.96	2.41	2.61	2.39
450	2.23	1.87	5.28	4.13	3.47	2.97	3.09	2.73
500	2.63	1.99	6.15	5.22	3.98	3.13	3.78	3.40

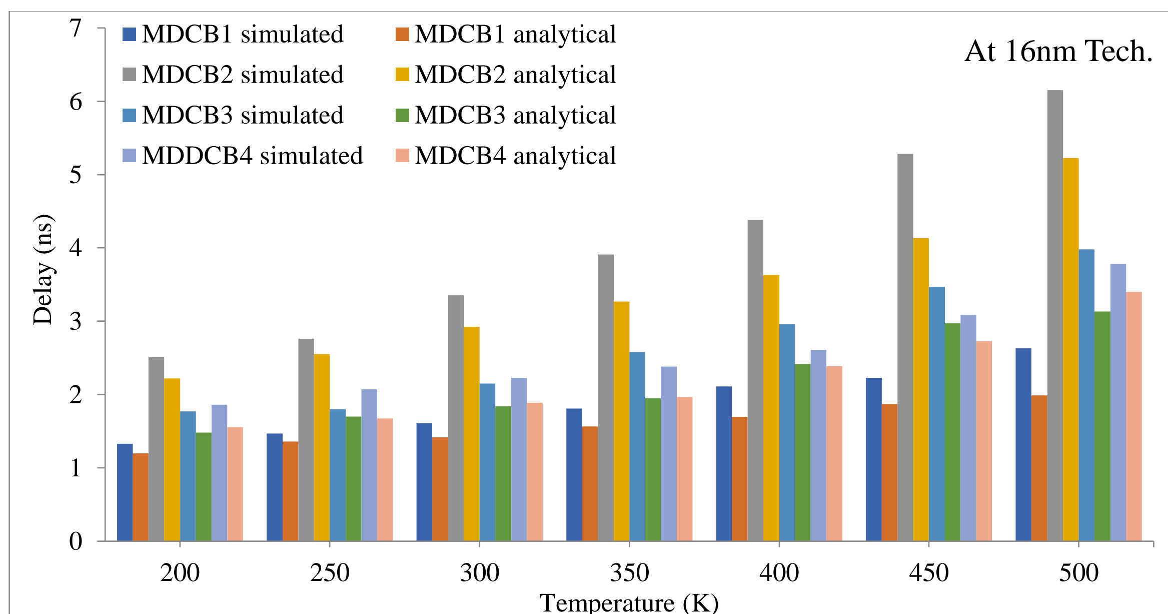


Figure 6.8 Simulated and analytical delay comparison of four mixed for 1000µm interconnect length at 16nm technology node

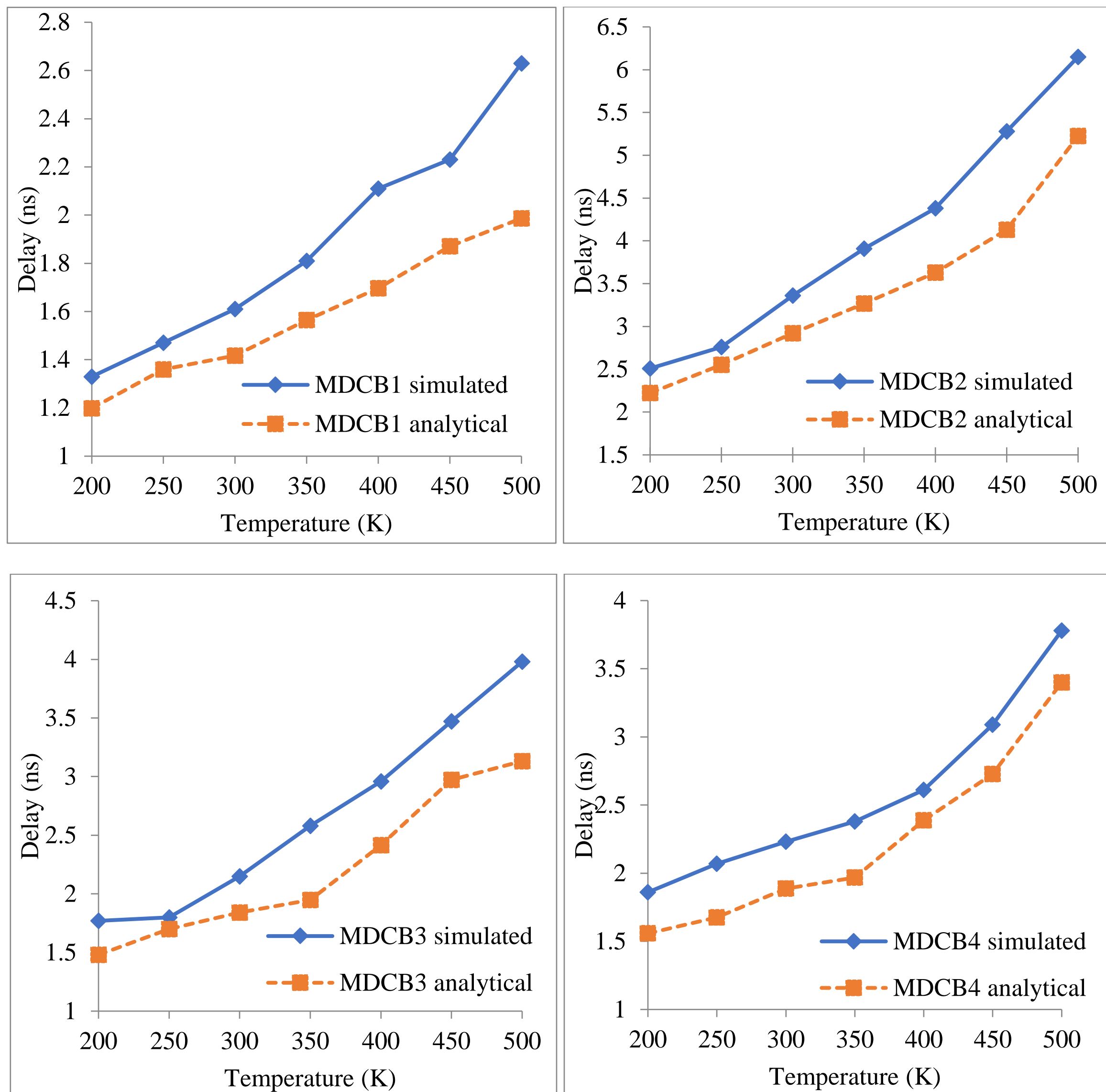


Figure 6.9 Delay comparisons of four mixed CNTs for 1000µm interconnect length at 16nm technology

Figure 6.9 focuses on and compares analytical and simulated readings of four MDCB structures separately at the 16nm technology node. The delay behaves in the same fashion. MDCB 2 interconnect structure shows a maximum delay than the other three structures. MDCB 1 structure developed with DWCNTs in the center and MWCNTs along the periphery of the bundle attains the lowest value of delay (both simulated and analytical) than all existing interconnect materials for 22nm and 16nm technology nodes.

For the MDCB structure at the 22nm technology node, the error percentage between the simulated and analytical data is ~7-8%. However, the difference/gap between the results increases to ~13-14% at the 16nm technology node. For all structures, both delays follow the same trend and lie in close relationship with each other thus validating the results.

6.3 Chapter Summary and Contribution

From the simulated delay readings mentioned in the chapter, it has been noted that MDCB structures give improved performance based on delay and PDP than existing mixed CNT structures (multi and single-wall CNT bundles) considering the impact of temperature at nano-regime nodes. This is due to the existence of DWCNTs instead of SWCNTs in considered structures which comprises two conducting shells, therefore helping in offering better conductivity than SWCNTs. So, the proposed structures have a great potential to replace them and can be used as interconnecting material for future nodes.

The closed-form expression for the $T_{90\%}$ delay is also mentioned. The analytical results are compared with the simulated data. The comparison is made for four mixed structures, and it is concluded that the error percentage between the two is bearable. Thus, both simulated and analytical readings help in validating each other. MDCB interconnects prove themselves stable and can be potentially employed as VLSI global interconnect material at nanotechnology nodes.

Related Publication:

1. Gurleen Dhillon and Karmjit Singh Sandha, "Delay Analysis of Mixed CNT Bundles as Global Interconnect for Nanotechnology Nodes," *Journal of Electrical Engineering*, vol. 74, no.1, pp.57-63, 2023. *(Impact Factor- 0.840)* (SCI indexed)

7. CONCLUSION AND FUTURE SCOPE

As technology scales down, delays related to global interconnect overcome transistor delays and the performance of interconnect plays an imperative role in determining the electrical performance of the circuit. So, interconnect material must be picked wisely for integrated circuits. Aluminum and copper have been used as interconnecting materials. However, there are several problems that occurred with an increase in scaling. Problems like electromigration and surface scattering give rise to collisions and thereby their conductivity is decreased. So, there is a dire need to replace them.

As a result, carbon nanotubes were introduced to provide an alternative to copper interconnect. Carbon nanotubes have revolutionized the domain of VLSI interconnects by showing their best performance based on electrical conductivity, mechanical strength, and thermal stability at future nanotechnology nodes. Formed with sp_2 hybridization, these graphitic hollow tubes have gained the attention of VLSI engineers. Single-wall CNTs have excellent conductivity but face chirality and manufacturing issues. Multi-wall CNTs are comparatively easy to fabricate and metallic in nature. These large-diameter nanotubes have also shown good simulation results as interconnect material. Literature reflects upon several papers indicating that these CNTs have shown good results concerning delay and PDP than copper as VLSI interconnect material at intermediate and global levels. Several types of mixed structures are developed. One is formed with SWCNTs and MWCNTs. The other is formed with different diameter MWCNTs.

7.1 CONCLUSION

The results and work in this thesis report develop and determine the performance of four mixed bundles formed with MWCNTs and DWCNTs (MDCB structures). DWCNTs are a special case of MWCNTs with only two shells. DWCNTs are metallic in nature and easier to fabricate than SWCNTs. It has been concluded that these mixed bundle CNTs also show good results concerning delay and PDP.

Different circuit simulation comparisons are drawn among copper, SWCNT, MWCNT, DWCNT, and MDCB interconnects at different interconnect lengths, technologies, and temperature points. It has been perceived that these mixed bundle CNT structures show minimum delay and PDP and can replace all existing materials soon. Among the comparison between these four MDCB structures, the structure formed by putting MWCNTs along the outer periphery and DWCNTs in the middle of the bundle gives superior performance than all

and can even compete better than MWCNTs and DWCNTs, i.e., individual counterparts. This is attained by placing MWCNTs on the outer edges which helped in overcoming coupling effects and DWCNTs in the center helped in providing good conductivity.

Various electron and phonon scattering phenomena are also studied in detail and the impact of temperature-affected mean free paths are also considered. The global interconnect lines undergo coupling effects when placed on integrated chips. The unwanted inductive and capacitive couplings are also studied. The impact of crosstalk on interconnects can't be ignored. Different cases of functional (when one line is idle and the other is active) and dynamic (when activity is taking place in both neighboring lines) are also studied and the results are presented for 1000μm interconnect line. Crosstalk either increases delay or changes the functionality of the circuit. The stability of MDCB structures is also determined. The parameters like overshoot and rise time are examined. Also, the Nyquist and response plots of these structures are analyzed.

The proposed MDCB structures are compared based on delay, power, and PDP with mixed CNT structures (multi-wall and single-wall CNT bundles) existing in the literature. MDCB structures show lesser value and perform better than existing mixed CNTs. The analytical expression for delay time (T_{90}) is used and the mathematical values are compared with SPICE simulated readings. They validate each other. It has been reported that MDCB structures (formed with MWCNTs and DWCNTs) show outstanding performance based on delay, power-delay product, and power-crosstalk induced delay product at 32nm, 22nm, and 16nm technologies for global lengths at a wide temperature range. With good stability response, these MDCB structures have proven themselves as an appropriate material for interconnect applications in circuits for future nodes.

7.2 Future Work

These mixed bundle CNT structures have the potential to replace traditional CNT materials like single-wall, multi-wall, and double-wall CNT bundles at global levels. The work presented in this report focuses on the temperature-dependent modeling of four mixed carbon nanotube bundle structures formed with MWCNTs and DWCNTs. These mixed bundle CNTs tend to capture the VLSI market at and beyond the 32nm technology node.

Some of the related topics that need detailed study for overcoming big challenges and can be looked over in the future are listed below:

- The fabrication of CNT interconnects remains a big issue in the real world. Although few existing methods exist. Yet some new, feasible, and implementable techniques need to be proposed and problems related to existing ones must be taken care of.
- With further advancement in the VLSI technology market the electrical performance of carbon nanotubes as an interconnect material based on delay and PDP can be analyzed for technology nodes like 10nm and 7nm.
- The mathematical expressions and analytical study of crosstalk coupled mixed interconnects still need to be explored in depth.
- For low-power circuit applications, sub-threshold voltage plays an important role, and such operations need to be addressed to determine the actual performance of circuits in that scenario.

LIST OF PUBLICATIONS

- **SCI indexed**
    1. Gurleen Dhillon and Karmjit Singh Sandha, "Mixed CNT bundles as VLSI interconnects for nanoscale technology nodes," *Journal of Computational Electronics*, vol. 20, no.1, pp. 248-258, 2021. *(Impact Factor- 2.1)*
    2. Gurleen Dhillon and Karmjit Singh Sandha, "Stability-and Crosstalk-Based Performance of Multi-and Double-walled Mixed CNT Bundles as Interconnect for Next-Generation Technology Nodes," *Journal of Circuits, Systems and Computers*, vol. 31, no. 5, p. 2250098, 2022. *(Impact Factor- 1.5)*
    3. Gurleen Dhillon and Karmjit Singh Sandha, "Delay Analysis of Mixed CNT Bundles as Global Interconnect for Nanotechnology Nodes," *Journal of Electrical Engineering*, vol. 74, no.1, pp.57-63, 2023. *(Impact Factor- 0.8)*

- **Scopus indexed**
    1. Gurleen Dhillon and Karamjit Singh, "Impact of Functional Crosstalk on Mixed CNT Bundles for Future VLSI Nodes," *Materials Today: Proceedings (Elseveir),* 2023. (Accepted) (https://doi.org/10.1016/j.matpr.2023.02.259)
    2. Karmjit Singh Sandha and Gurleen Dhillon, "Impact of Variable Interconnect length on the performance of MWCNT as VLSI Interconnect for Nanometer Integrated Circuit Design," *International Journal of Engineering and Advanced Technology (IJEAT)* 8.5 (2019): 2209-2214.

REFERENCES

[1]. J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, *Digital integrated circuits*, vol. 2, Englewood Cliffs, Prentice Hall, New Jersey, 2002.

[2]. S. M. Kang and Y. Leblebici, *CMOS digital integrated circuits*, Tata McGraw-Hill Education, 2003.

[3]. J. D. Meindl, "Interconnect opportunities for gigascale integration," *IEEE Micro*, vol. 23, no. 3, pp. 28-35, 2003.

[4]. V. R. Kumbhare, R. Kumar, M. K. Majumder, S. Kumar, P. P. Paltani, B. K. Kaushik and R. Sharma, "High-speed interconnects: history, evolution, and the road ahead," *IEEE Microwave Magazine,* vol. 23, no. 8, pp. 66-82, 2022.

[5]. L. W. Schaper and D. Amey, "Improved electrical performance required for future MOS packaging," *IEEE transactions on components, hybrids, and manufacturing technology*, vol. 6, no. 3, pp. 283-289, 1983.

[6]. M. Amin, P. P. Dey and Hassan Badkoobehi, "A complete electrical equivalent circuit model for biological cell," *In Proceedings of the 7th WSEAS International Conference on Applied Computer and Applied Computational Science. World Scientific and Engineering Academy and Society (WSEAS),* pp. 343-348. 2008.

[7]. P. W. Liu, W. S. Zhao, D. W. Wang, J. Wang, Y. Hu and G. Wang, "Optimal repeater insertion for nano-interconnects in current-mode signaling scheme," *Micro & Nano Letters,* vol. 15, no. 5, pp. 308-312, 2020.

[8]. F. Liang, G. Wang and W. Ding, "Estimation of time delay and repeater insertion in multiwall carbon nanotube interconnects," *IEEE transactions on electron devices*, vol. 58, no. 8, pp. 2712-2720, 2011.

[9]. A. Garbaya, M. Kotti, M. Fakhfakh and E. T. Cuautle, "Surrogate assisted optimization for low-voltage low-power circuit design," *Journal of Low Power Electronics and Application*, vol. 10, no. 2, p. 20, 2020.

[10]. K. R. Komatla and S. R. Patri, "An Ultra-Low-Power, Self-Start-Up DC-DC Boost Converter for Self-Powered IoT Node," *Journal of Circuits, Systems and Computers*, vol. 31, no. 02, p.2250026, 2022.

[11]. E. Moursy, A. Magdy and E. G. Friedman, "Optimum wire sizing of RLC interconnect with repeaters," *In Proceedings of the 13th ACM Great Lakes symposium on VLSI*, pp. 27-32. 2003.

[12]. K. C. Saraswat and F. Mohammadi, "Effect of scaling of interconnections on the time delay of VLSI circuits," *IEEE Transactions on Electron Devices*, vol. 29, no. 4, pp. 645-650, 1982.

[13]. F. Shi, X. Wu and Z. Yan, "Improved analytical delay models for RC-coupled interconnects," *IEEE Transactions on very large-scale integration (VLSI) systems*, vol. 22, no. 7, pp. 1639-1644, 2013.

[14]. H. B. Bakoglu and J. D. Meindl, "Optimal interconnection circuits for VLSI," *IEEE Transactions on Electron Devices*, vol. 32, no. 5, pp. 903-909, 1985.

[15]. K. H. Koo, H. Cho, P. Kapur and K. C. Saraswat, "Performance comparisons between carbon nanotubes, optical, and Cu for future high-performance on-chip interconnect applications," *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3206-3215, 2007.

[16]. T. Sakurai, "Closed-form expressions for interconnection delay, coupling, and crosstalk in VLSIs," *IEEE Transactions on Electron Devices*, vol. 40, no. 1, pp. 118-124, 1993.

[17]. V. Adler and E. G. Friedman, "Repeater design to reduce delay and power in resistive interconnect," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 5, pp. 607-616, 1998.

[18]. R. Chandel, S. Sarkar and R. P. Agarwal, "Repeater insertion in global interconnects in VLSI circuits," *Microelectronics International*, vol.22, no.1, pp. 43-50, 2005.

[19]. B. K. Kaushik, S. Sarkar and R. P. Agarwal, "Waveform analysis and delay prediction for a CMOS gate driven RLC interconnect load," *Integration the VLSI journal*, vol.40, pp.394-405, 2007.

[20]. W. Yang, Y. Li, Z. Wu, D. Tsamakis, D. Learmonth, C. G. Xie, S. Huang, C. Lenn, A. Cutler, "Multiphase flow measurement by electrical capacitance tomography," *In 2011 IEEE International Conference on Imaging Systems and Techniques*, pp. 108-111, 2011.

[21]. Y. I. Ismail and E. G. Friedman, "Effects of inductance on the propagation delay and repeater insertion in VLSI circuits: A summary," *IEEE Circuits and Systems Magazine*, vol. 3, no. 1, pp. 24-28, 2003.

[22]. K. Banerjee and A. Mehrotra, "A power-optimal repeater insertion methodology for global interconnects in nanometer designs," *IEEE Transactions on Electron Devices*, vol. 49, no. 11, pp. 2001-2007, 2002.

[23]. A. Khursheed and K. Khare, “Optimized buffer insertion for efficient interconnects designs,” *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 33, no. 5, p. e2748, 2020.

[24]. P. W. Liu, Z. H. Cheng, W. S. Zhao, Q. Lu, Z. Zhu and G. Wang, “Repeater insertion for multi-walled carbon nanotube interconnects,” *Applied Sciences*, vol. 8, no. 2, pp. 236 (1-12), 2018.

[25]. R. L. Graham, G. B. Alers, T. Mountsier, N. Shamma, S. Dhuey, S. Cabrini, R. H. Geiss, D. T. Read and S. Peddeti, “Resistivity dominated by surface scattering in sub-50 nm Cu wires,” *Applied Physics Letters*, vol. 96, no. 4, p. 042116, 2010.

[26]. P. Kapur, G. Chandra, J. P. McVittie and K. C. Saraswat, “Technology and reliability constrained future copper interconnects. II. Performance implications,” *IEEE Transactions on Electron Devices*, vol. 49, no. 4, pp. 598-604, 2002.

[27]. D. Akinwande, N. Petrone and J. Hone, “Two-dimensional flexible nanoelectronics,” *Nature communications,* vol. 5, no. 1, p. 5678, 2014.

[28]. J. J. Plombon, E. Andideh, V. M. Dubin and J. Maiz, “Influence of phonon, geometry, impurity, and grain size on copper line resistivity,” *Applied physics letters*, vol. 89, no. 11, p. 113124, 2006.

[29]. A. Naeemi, R. Sarvari and J. D. Meindl, “Performance comparison between carbon nanotube and copper interconnects for gigascale integration (GSI),” *IEEE Electron Device Letters*, vol. 26, no. 2, pp. 84-86, 2005.

[30]. A. K. Kureshi and M. Hasan, “Analysis of CNT bundle and its comparison with copper interconnect for CMOS and CNFET drivers,” *Journal of Nanomaterials*, p. 486979 (1-6), 2009.

[31]. H. Cho, K. H. Koo, P. Kapur and K. C. Saraswat, “Performance Comparisons Between Cu/Low-$\kappa $, Carbon-Nanotube, and Optics for Future On-Chip Interconnects,” *IEEE Electron Device Letters*, vol. 29, no. 1, pp. 122-124, 2007.

[32]. S. V. Garimella, A. S. Fleischer, J. Y. Murthy, A. Keshavarzi, R. Prasher, C. Patel, S. H. Bhavnani, “Thermal challenges in next-generation electronic systems,” *IEEE Transactions on Components and Packaging Technologies*, vol. 31, no. 4, pp. 801-815, 2008.

[33]. M. S. Sarto and A. Tamburrano, “Single-conductor transmission-line model of multiwall carbon nanotubes,” *IEEE Transactions on Nanotechnology*, vol. 9, no. 1, pp. 82-92, 2009.

[34]. N. Hamada, S. I. Sawada and A. Oshiyama, “New one-dimensional conductors: Graphitic microtubules,” *Physical review letters*, vol. 68, no. 10, p.1579, 1992.

[35]. B. Li, T. D. Sullivan, T. C. Lee and D. Badami, “Reliability challenges for copper interconnects,” *Microelectronics reliability*, vol. 44, no. 3, pp. 365-380, 2004.

[36]. M. Shefali, K. Fatima and P. Uma Sathyakam, “Frequency response analysis of CNT bundle interconnects,” *International Journal of Electronics Letters,* pp. 1-10, 2022.

[37]. D. Mann, A. Javey, J. Kong, Q. Wang and H. Dai, “Ballistic transport in metallic nanotubes with reliable Pd ohmic contacts,” *Nano Letters*, vol.3, pp.1541-1544, 2003.

[38]. R. Vajtai, B. Wei, Y. J. Jung, A. Cao, S. K. Biswas, G. Ramanath and P. M. Ajayan, “Building and testing organized architectures of carbon nanotubes,” *IEEE transactions on nanotechnology*, vol. 2, no. 4, pp. 355-361, 2003.

[39]. W. Steinhögl, G. Schindler, G. Steinlesberger, M. Traving, and M. Engelhardt, “Comprehensive study of the resistivity of copper wires with lateral dimensions of 100 nm and smaller,” *Journal of Applied Physics*, vol. 97, no. 2, pp. 023706 (1-6), 2005.

[40]. M. P. Anantram and F. Leonard, “Physics of carbon nanotube electronic devices,” *Reports on progress in physics*, vol. 69, no. 3, p. 507, 2006.

[41]. A. A. Maarouf, C. L. Kane and E. J. Mele, “Electronic structure of carbon nanotube ropes,” *Physical Review B*, vol. 61, no. 16, p. 11156, 2000.

[42]. A. Maffucci, G. Miano and F. Villone, “Performance comparison between metallic carbon nanotube and copper nano-interconnects,” *IEEE transactions on advanced packaging*, vol. 31, no. 4, pp. 692-699, 2008.

[43]. B. Xu, R. Chen, J. Zhou and J. Liang, “Recent progress and challenges regarding carbon nanotube on-chip interconnects,” *Micromachines*, vol. 13, no. 7, p.1148, 2022.

[44]. C. C. Yu and H. L. Chen, “Nanoimprint technology for patterning functional materials and its applications,” *Microelectronic Engineering*, vol. 132, pp. 98-119, 2015.

[45]. B. Q. Wei, R. Vajtai and P. M. Ajayan, “Reliability and current carrying capacity of carbon nanotubes,” *Applied physics letters*, vol. 79, no. 8, pp. 1172-1174, 2001.

[46]. P. J. Burke, “Luttinger liquid theory as a model of the gigahertz electrical properties of carbon nanotubes,” *IEEE Transactions on Nanotechnology*, vol. 1, no. 3, pp.129-144, 2002.

[47]. A. Nieuwoudt and Y. Massoud, “On the optimal design, performance, and reliability of future carbon nanotube-based interconnect solutions,” *IEEE transactions on electron devices*, vol. 55, no. 8, pp. 2097-2110, 2008.

[48]. V. Parkash and A. K. Goel, "Performance analysis of metallic carbon nanotubes as nanotechnology circuit interconnects," *Microwave and Optical Technology Letters*, vol. 53, no. 11, pp. 2505-2508, 2011.

[49]. A. Srivastava, Y. Xu and A. K. Sharma, "Carbon nanotubes for next generation very large-scale integration interconnects," *Journal of Nanophotonics*, vol. 4, no. 1, pp. 041690 (1-26), 2010.

[50]. S. J. Tans, M. H. Devoret, H. Dai, A. Thess, R. E. Smalley, L. J. Geerligs and Cees Dekker, "Individual single-wall carbon nanotubes as quantum wires," *Nature*, vol. 386, no. 6624, pp. 474-477, 1997.

[51]. A. Naeemi and J. D. Meindl, "Design and performance modeling for single-walled carbon nanotubes as local, semiglobal, and global interconnects in gigascale integrated systems," *IEEE Transactions on Electron Devices*, vol. 54, no. 1, pp. 26-37, 2006.

[52]. K. Banerjee, S. Im and N. Srivastava, "Can carbon nanotubes extend the lifetime of on-chip electrical interconnections?" *In 2006 1st International Conference on Nano-Networks and Workshops (IEEE)*, pp. 1-9, 2006.

[53]. A. Giustiniani, V. Tucci and Walter Zamboni, "Modeling issues and performance analysis of high-speed interconnects based on a bundle of SWCNT," *IEEE Transactions on electron devices*, vol. 57, no. 8, pp.1978-1986, 2010.

[54]. P. L. McEuen, M. S. Fuhrer and H. Park, "Single-walled carbon nanotube electronics," *IEEE transactions on nanotechnology*, vol. 1, no. 1, pp. 78-85, 2002.

[55]. A. Naeemi and J. D. Meindl, "Performance modeling for single-and multiwall carbon nanotubes as signal and power interconnects in gigascale systems," *IEEE transactions on electron devices*, vol. 55, no. 10, pp. 2574-2582, 2008.

[56]. N. Srivastava, H. Li, F. Kreupl and Kaustav Banerjee, "On the applicability of single-walled carbon nanotubes as VLSI interconnects," *IEEE Transactions on Nanotechnology*, vol. 8, no. 4, pp. 542-559, 2009.

[57]. M. K. Rai and S. Sarkar, "Influence of tube diameter on carbon nanotube interconnect delay and power output," *Physica status solidi (a)*, vol. 208, no. 3, pp. 735-739, 2011.

[58]. B. Liu, C. Li, C. Li and S. Zhang, "Effect of temperature and single event transient on crosstalk in coupled single-walled carbon nanotube (SWCNT) bundle interconnects," *International Journal of Circuit Theory and Applications*, vol. 49, no. 10, pp. 3408-3420, 2021.

[59]. H. Li, W. Y. Yin, K. Banerjee and J. F. Mao, “Circuit modeling and performance analysis of multi-walled carbon nanotube interconnects,” *IEEE Transactions on electron devices*, vol. 55, no. 6, pp. 1328-1337, 2008.

[60]. M. Tang and J. Mao, “Modeling and fast simulation of multiwalled carbon nanotube interconnects,” *IEEE Transactions on Electromagnetic Compatibility*, vol. 57, no. 2 pp. 232-240, 2014.

[61]. A. Naeemi and J. D. Meindl, “Compact physical models for multiwall carbon-nanotube interconnects,” *IEEE Electron Device Letters*, vol. 27, no. 5, pp. 338-340, 2006.

[62]. M. D'Amore, M. S. Sarto and A. Tamburrano, “Fast transient analysis of next-generation interconnects based on carbon nanotubes,” *IEEE Transactions on Electromagnetic Compatibility*, vol. 52, no. 2, pp. 496-503, 2010.

[63]. Y. S. Duksh, B. K. Kaushik, S. Sarkar and R. Singh, “Analysis of propagation delay and power with variation in driver size and number of shells in multi walled carbon nanotube interconnects,” *Journal of engineering, design and technology*, 2013.

[64]. D. Fathi, B. Forouzandeh, S. Mohajerzadeh and R. Sarvari, “Accurate analysis of carbon nanotube interconnects using transmission line model,” *Micro & Nano Letters*, vol. 4, no. 2, pp. 116-121, 2009.

[65]. M. Gholipour and N. Masoumi, “Efficient inclusive analytical model for delay estimation of multi-walled carbon nanotube interconnects,” *IET circuits, devices & systems*, vol. 6, no. 4, pp. 252-259, 2012.

[66]. K. Singh and B. Raj, “Influence of temperature on MWCNT bundle, SWCNT bundle and copper interconnects for nanoscaled technology nodes,” *Journal of Materials Science: Materials in Electronics*, vol. 26, no. 8, pp. 6134-6142, 2015.

[67]. J. F. Davis and J. D. Meindl, “Compact distributed RLC interconnect models. Single line transient, time delay, and overshoot expressions,” *IEEE Transactions on Electron Devices*, vol. 47, no. 11, pp. 2068-2077, 2000.

[68]. P. G. Collins and Ph Avouris, “Multishell conduction in multiwalled carbon nanotubes,” *Applied Physics A*, vol. 74, no. 3, pp. 329-332, 2002.

[69]. A. Naeemi and J. D. Meindl, “Monolayer metallic nanotube interconnects: Promising candidates for short local interconnects,” *IEEE Electron Device Letters*, vol. 26, no. 8, pp. 544-546, 2005.

[70]. F. Kreupl, A. P. Graham, G. S. Duesberg, W. Steinhögl, M. Liebau, E. Unger and W. Hönlein, “Carbon nanotubes in interconnect applications,” *Microelectronic Engineering*, vol. 64, no. 1-4, pp. 399-408, 2002.

[71]. J. Li, Q. Ye, A. Cassell, H. T. Ng, R. Stevens, J. Han and M. Meyyappan, “Bottom-up approach for carbon nanotube interconnects,” *Applied Physics Letters*, vol. 82, no. 15, pp. 2491-2493, 2003.

[72]. Y. Wu, Y. Cui, L. Huynh, C. J. Barrelet, D. C. Bell and C. M. Lieber, “Controlled growth and structures of molecular-scale silicon nanowires,” *Nano letters*, vol. 4, no. 3, pp. 433-436, 2004.

[73]. A. B. Amin, S. M. Shakil and M. S. Ullah, “A theoretical modeling of adaptive mixed cnt bundles for high-speed VLSI interconnect design,” *Crystals,* vol. 12, no. 2, p.186, 2022.

[74]. P. U. Sathyakam and P. S. Mallick, “Transient analysis of mixed carbon nanotube bundle interconnects,” *Electronics letters*, vol.47, no. 20, pp. 1134-1136, 2011.

[75]. V. R. Kumbhare, P. P. Paltani and M. K. Majumder, “Performance analysis of mixed CNT bundle interconnects at 10 nm technology,” *IET Circuits, Devices & Systems,* vol. 14, no. 7, pp. 1049-1057, 2020.

[76]. S. N. Pu, W. Y. Yin, J. F. Mao and Q. H. Liu, “Crosstalk prediction of single-and double-walled carbon-nanotube (SWCNT/DWCNT) bundle interconnects,” *IEEE Transactions on Electron Devices*, vol. 56, no. 4, pp. 560-568, 2009.

[77]. Z. Kordrostami, M. H. Sheikhi and I. Hassaninia, “Double-wall carbon nanotube interconnects: experimental measurements, physical and circuit modelling,” *International Journal of Nanomanufacturing*, vol. 5, no. 3-4, pp. 278-287, 2010.

[78]. W. Y. Yin and W. S. Zhao, “Modeling of carbon nanotube (CNT) interconnects,” *In 2011 IEEE 15th Workshop on Signal Propagation on Interconnects (SPI)*, pp. 79-82, 2011.

[79]. A. Loumi, H. Belahrach and A. Ghammaz, “Crosstalk Effect in Bundled SWCNT, DWCNT and MWCNT Carbon Nanotubes,” *Journal of electrical engineering*, pp. 344-348, 2017.

[80]. M. K. Majumder, P. K. Das and B. K. Kaushik, “Delay and crosstalk reliability issues in mixed MWCNT bundle interconnects,” *Microelectronics Reliability*, vol. 54, no. 11 pp. 2570-2577, 2014.

[81]. K. Zhang, B Tian, X. Zhu, F. Wang and J. Wei, “Crosstalk analysis of carbon nanotube bundle interconnects,” *Nanoscale research letters*, vol. 7, no. 1, pp. 1-5, 2012.

[82]. M. K. Majumder, N. D. Pandya, B. K. Kaushik and S. K. Manhas, “Dynamic crosstalk effect in mixed CNT bundle interconnects,” *Electronics letters*, vol. 48, no. 7, pp. 384-385, 2012.

[83]. V. R. Kumar, B. K. Kaushik and A. Patnaik, "Improved crosstalk noise modeling of MWCNT interconnects using FDTD technique," Microelectronics Journal, vol.46, no.12, pp. 1263-1268, 2015.

[84]. V. K. Agrawal, R. Patel, D. Boolchandani, T. Varma and K. Rangra, "Sensitivity and reliability enhancement of a MEMS based wind speed sensor," *Microelectronics Reliability*, vol.104, p.113513, 2020.

[85]. R. Maity, N. P. Maity, K. S. Rao, G. Sravani, K. Guha, S. Baishya, "Fringing Capacitive Effect of Silicon Carbide Based Nano-Electro-Mechanical-System (NEMS) Micromachined Ultrasonic Transducers: Analytical Modeling and FEM Simulation", *Transactions on Electrical and Electronic Materials*, vol.20, pp. 473–480, 2019.

[86]. J. Y. Park, S. Rosenblatt, Y. Yaish, V. Sazonova, H. Üstünel, S. Braig, T. A. Arias, P. W. Brouwer and P. L. McEuen, "Electron− phonon scattering in metallic single-walled carbon nanotubes," *Nano letters*, vol. 4, no. 3, pp. 517-520, 2004.

[87]. E. Pop, D. A. Mann, K. E. Goodson and H. Dai, "Electrical and thermal transport in metallic single-wall carbon nanotubes on insulating substrates," *Journal of Applied Physics,* vol. 101, no. 9, p. 093710, 2007.

[88]. S. K. Bagaria and C. Periasamy, "Magnetic Properties of Electroformed Ni and Ni-Fe for Micromagnetic MEMS Applications," *Journal of Superconductivity and Novel Magnetism*, vol. 28, no. 5,2015.

[89]. K. M. Mohsin, A. Srivastava, A. K. Sharma and C. Mayberry, "A thermal model for carbon nanotube interconnects," *Nanomaterials*, vol. 3, no. 2, pp. 229-241, 2013.

[90]. A. Naeemi and J. D. Meindl, "Physical modeling of temperature coefficient of resistance for single-and multi-wall carbon nanotube interconnects," *IEEE Electron Device Letters*, vol. 28, no. 2, pp. 135-138, 2007.

[91]. K. M. Liew, C. H. Wong, X. Q. He and M. J. Tan, "Thermal stability of single and multi-walled carbon nanotubes," *Physical Review B*, vol. 71, no. 7, pp. 075424 (1-6), 2005.

[92]. A. Hosseini and V. Shabro, "Thermally-aware modeling and performance evaluation for single-walled carbon nanotube-based interconnects for future high performance integrated circuits," *Microelectronic Engineering*, vol. 87, no. 10, pp. 1955-1962, 2010.

[93]. E. Pop, D. Mann, J. Reifenberg, K. Goodson and H. Dai, "Electro-thermal transport in metallic single-wall carbon nanotubes for interconnect applications," *In IEEE International Electron Devices Meeting (IEDM Technical Digest)*, 2005.

[94]. A. G. Chiariello, G. Miano and A. Maffucci, “Size and temperature effects on the resistance of copper and carbon nanotubes nano-interconnects,” *In 19th Topical Meeting on Electrical Performance of Electronic Packaging and Systems (IEEE)*, pp. 97-100, 2010.

[95]. A. Naeemi and J. D. Meindl, “Impact of electron-phonon scattering on the performance of carbon nanotube interconnects for GSI,” *IEEE Electron Device Letters*, vol. 26, no. 7, pp. 476-478, 2005.

[96]. W. C. Chen, W. Y. Yin, L. Jia and Q. H. Liu, “Electrothermal characterization of single-walled carbon nanotube (SWCNT) interconnect arrays,” *IEEE transactions on nanotechnology*, vol. 8, no. 6, pp. 718-728, 2009.

[97]. P. Gautreau, T. Ragab and C. Basaran, “Hot phonons contribution to Joule heating in single-walled carbon nanotubes,” *Journal of Applied Physics*, vol. 112, no. 10, pp. 103527 (1-6), 2012.

[98]. M. K. Majumder, B. K. Kaushik and S. K. Manhas, “Analysis of delay and dynamic crosstalk in bundled carbon nanotube interconnects,” *IEEE transactions on electromagnetic compatibility,* vol. 56, no. 6, pp. 1666-1673, 2014.

[99]. S. Subash and M. H. Chowdhury, “Mixed carbon nanotube bundles for interconnect applications,” *International Journal of Electronics*, vol. 96, no. 6, pp. 657-671, 2009.

[100]. P. U. Sathyakam and P. S. Mallick, “Towards realisation of mixed carbon nanotube bundles as VLSI interconnects: A review,” *Nano Communication Networks,* vol. 3, no. 3, pp.175-182, 2012.

[101]. M. K. Majumder, J. Kumar and B. K. Kaushik, “Process-induced delay variation in SWCNT, MWCNT, and mixed CNT interconnects,” *IETE Journal of Research*, vol. 61, no. 5, pp. 533-540, 2015.

[102]. V. R. Kumbhare, P. P. Paltani and M. K. Majumder, “Performance analysis of mixed CNT bundle interconnects at 10 nm technology,” *IET Circuits, Devices & Systems*, vol. 14, no. 7, pp.1049-1057, 2020.

[103]. K. S. Sandha and A. Thakur, “Comparative analysis of mixed CNTs and MWCNTs as VLSI interconnects for deep sub-micron technology nodes,” *Journal of Electronic Materials*, vol. 48, no. 4, pp. 2543-2554, 2019.

[104]. P. U. Sathyakam, S. Bhattacharjee 54and S. Raj, “Crosstalk analysis of triangular CNT bundle interconnects,” *Journal of Electronic Materials*, vol. 50, pp. 7017-7025, 2021.

[105]. B. K. Kaushik, S. Sarkar, R. P. Agarwal and R. C. Joshi, "Effect of line resistance and driver width on crosstalk in coupled VLSI interconnects," *Microelectronics International*, vol. 24, no. 3, pp. 42-45, 2007.

[106]. D. Rossi, J. M. Cazeaux, C. Metra and F. Lombardi, "Modeling crosstalk effects in CNT bus architectures," *IEEE Transactions on Nanotechnology,* vol. 6, no. 2, pp. 133-145, 2007.

[107]. J. A. Davis, and J. D. Meindl, "Compact distributed RLC interconnect models-Part II: Coupled line transient expressions and peak crosstalk in multilevel networks," *IEEE Transactions on Electron Devices*, vol. 47, no. 11, pp. 2078-2087, 2000.

[108]. H. Sharma, and K. S. Sandha, "Thermally aware modeling and performance analysis of MLGNR as on-chip VLSI interconnect material," *Journal of Electronic Materials,* vol. 48, pp. 4902-4912, 2019.

[109]. K. Zhang, B. Tian, X. Zhu, F. Wang and J. Wei, "Crosstalk analysis of carbon nanotube bundle interconnects," *Nanoscale research letters*, vol. 7, no. 1, pp. 1-5, 2012.

[110]. B. K. Kaushik and S. Sarkar, "Crosstalk analysis for a CMOS gate driven inductively and capacitively coupled interconnects," *Microelectronics Journal*, vol. 39, no. 12, pp. 1834-1842, 2008.

[111]. M. G. Kumar, R. Chandel and Y. Agrawal, "An efficient crosstalk model for coupled multiwalled carbon nanotube interconnects," *IEEE Transactions on Electromagnetic Compatibility*, vol. 60, no. 2, pp. 487-496, 2017.

[112]. D. Das and H. Rahaman, "Analysis of crosstalk in single-and multiwall carbon nanotube interconnects and its impact on gate oxide reliability," *IEEE transactions on nanotechnology*, vol. 10, no. 6, pp. 1362-1370, 2011.

[113]. M. K. Majumder, N. D. Pandya, B. K. Kaushik and S. K. Manhas, "Analysis of MWCNT and bundled SWCNT interconnects: Impact on crosstalk and area," *IEEE Electron Device Letters*, vol. 33, no. 8, pp.1180-1182, 2012.

[114]. M. K. Rai, H. Garg and B. K. Kaushik, "Temperature-dependent modeling and crosstalk analysis in mixed carbon nanotube bundle interconnects," *Journal of Electronic Materials*, vol. 46, no. 8, pp. 5324-5337, 2017.

[115]. M. K. Majumder, N. R. Kukkam and B. K. Kaushik, "Frequency response and bandwidth analysis of multi-layer graphene nanoribbon and multi-walled carbon nanotube interconnects," *Micro & Nano Letters*, vol. 9, no. 9, pp. 557-560, 2014.

[116]. V. R. Kumar, M. K. Majumder, A. Alam, N. R. Kukkam and B. K. Kaushik, “Stability and delay analysis of multi-layered GNR and multi-walled CNT interconnects,” *Journal of Computational Electronics*, vol. 14, no. 2, pp. 611-618, 2015.

[117]. E. T. Ogawa, K. D. Lee, V. A. Blaschke and P. S. Ho, “Electromigration reliability issues in dual-damascene Cu interconnections,” *IEEE Transactions on reliability*, vol. 51, no. 4, pp. 403-419, 2002.

[118]. A. Raychowdhury and K. Roy, “Modeling of metallic carbon-nanotube interconnects for circuit simulations and a comparison with Cu interconnects for scaled technologies,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, no. 1, pp. 58-65, 2005.

[119]. R. Mudavath, R. N. Bhukya and P. R. Jeripotula, “The mitigation of signal integrity issues in coupled MWCNT bundles and a comparison with Cu nterconnects,” *Journal of Computational Electronics,* vol. 20, pp. 1430-1438, 2021.

[120]. A. Chatzigeorgiou, S. Nikolaidis and I. Tsoukalas, “Modeling CMOS gates driving RC interconnect loads,” *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 48, no. 4, pp. 413-418, 2001.

[121]. International Technology Roadmap for Semiconductors: 2013 [online]. Edition, http://public.itrs.net.

[122]. Predictive Technology Model [online]. www.eas.asu.edu ptm.

[123]. D. Fathi and B. Forouzandeh, “A novel approach for stability analysis in carbon nanotube interconnects,” *IEEE electron device letters*, vol. 30, no. 5, pp. 475-477, 2009.

[124]. A. Svizhenko, M. P. Anantram and T. R. Govindan, “Ballistic transport and electrostatics in metallic carbon nanotubes,” *IEEE transactions on nanotechnology*, vol. 4, no. 5, pp. 557-562, 2005.

[125]. H. Li, C. Xu and K. Banerjee, “Carbon nanomaterials: The ideal interconnect technology for next-generation ICs,” *IEEE Design & Test of Computers*, vol. 27, no. 4, pp.20-31, 2010.

[126]. B. K. Kaushik, S. Goel and G. Rauthan, “Future VLSI interconnects: optical fiber or carbon nanotube–a review,” *Microelectronics international*, vol. 24, no. 2, pp. 53-63, 2007.

[127]. N. J. Ginga and S. K. Sitaraman, “Thermomechanical Reliability Investigation of Carbon Nanotube Off-Chip Interconnects for Electronic Packages,” *IEEE Transactions*

on Components, Packaging and Manufacturing Technology, vol. 12, no. 8, pp. 1282-1292, 2022.

[128]. J. Deng and H. S. P. Wong, “A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part I: Model of the intrinsic channel region,” *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3186-3194, 2007.

[129]. H. Li, W. Liu, A. M. Cassell, F. Kreupl and K. Banerjee, “Low-resistivity long-length horizontal carbon nanotube bundles for interconnect applications—Part I: Process development,” *IEEE Transactions on Electron Devices*, vol. 60, no. 9, pp. 2862-2869, 2013.

[130]. H. Li and K. Banerjee, “High-frequency analysis of carbon nanotube interconnects and implications for on-chip inductor design,” *IEEE Transactions on Electron Devices*, vol. 56, no. 10, pp. 2202-2214, 2009.

[131]. A. Nieuwoudt and Y. Massoud, “Evaluating the impact of resistance in carbon nanotube bundles for VLSI interconnect using diameter-dependent modeling techniques,” *IEEE Transactions on Electron Devices*, vol. 53, no. 10, pp. 2460-2466, 2006.

[132]. A. Maffucci, G. Miano and F. Villone, “A new circuit model for carbon nanotube interconnects with diameter-dependent parameters,” *IEEE Transactions on Nanotechnology*, vol. 8, no. 3, pp. 345-354, 2008.

[133]. A. Nieuwoudt and Y. Massoud, “On the impact of process variations for carbon nanotube bundles for VLSI interconnect,” *IEEE Transactions on Electron Devices*, vol. 54, no. 3, pp. 446-455, 2007.

[134]. M. K. Rai, R. Khanna and S. Sarkar, “Control of tube parameters on SWCNT bundle interconnect delay and power dissipation,” *Microelectronics International*, vol. 31, no.1, pp. 24-31, 2014.

[135]. P. Lamberti and V. Tucci, “Impact of the variability of the process parameters on CNT-based nano interconnects performances: A comparison between SWCNTs bundles and MWCNT,” *IEEE Transactions on Nanotechnology*, vol. 11, no. 5, pp. 924-933, 2012.

[136]. K. Singh, and B. Raj, “Influence of temperature on MWCNT bundle, SWCNT bundle and copper interconnects for nanoscaled technology nodes," *Journal of Materials Science: Materials in Electronics*, vol. 26, pp.6134-6142, 2015.

[137]. H. Li, W. G. Lu, J. J. Li, X. D. Bai and C. Z. Gu, “Multichannel ballistic transport in multiwall carbon nanotubes,” *Physical review letters*, vol. 95, no. 8, pp. 086601 (1-4), 2005.

[138]. M. Tang and J. Mao, “Modeling and fast simulation of multiwalled carbon nanotube interconnects,” *IEEE Transactions on Electromagnetic Compatibility*, vol. 57, no. 2, pp. 232-240, 2014.

[139]. K. S. Sandha and S. Sharma, “Performance analysis of different mixed-MWCNT structures as VLSI interconnects for nano-electronics IC design,” *Journal of Nanoelectronics and Optoelectronics*, vol. 13, no. 3, pp. 357-367, 2018.

[140]. B. Bourlon, C. Miko, L. Forro, D. C. Glattli and Adrian Bachtold, “Determination of the intershell conductance in multiwalled carbon nanotubes,” *Physical review letters*, vol. 93, no. 17, pp. 176806 (1-4), 2004.

[141]. Y. G. Yoon, P. Delaney and S. G. Louie, “Quantum conductance of multiwall carbon nanotubes,” *Physical Review B*, vol. 66, no. 7, pp. 073407 (1-4), 2002.

[142]. P. Litoria, K. S. Sandha and A. Kansal, “Impact of tunneling conductance on the performance of multi walled carbon nanotubes as VLSI interconnects for nano-scaled technology nodes,” *Journal of Materials Science: Materials in Electronics*, vol. 28, no. 6, pp. 4818-4827, 2017.

[143]. M. R. Khezeli, M. H. Moaiyeri and A. Jalali, “Comparative analysis of simultaneous switching noise effects in MWCNT bundle and Cu power interconnects in CNTFET-based ternary circuits,” *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, vol. 27, no. 1, pp. 37-46, 2018.

[144]. C. Schoenenberger, A. Bachtold, C. Strunk, J. P. Salvetat and L. Forro, “Interference and Interaction in multi-wall carbon nanotubes,” *Applied Physics A*, vol. 69, no. 3, pp. 283-295, 1999.

[145]. P. G. Collins, M. Hersam, M. Arnold, R. Martel and P. Avouris, “Current saturation and electrical breakdown in multiwalled carbon nanotubes,” *Physical review letters*, vol. 86, no. 14, pp. 3128-3131, 2001.

[146]. F. Liang, G. Wang and H. Lin, “Modeling of crosstalk effects in multiwall carbon nanotube interconnects,” *IEEE transactions on Electromagnetic Compatibility*, vol. 54, no. 1, pp. 133-139, 2011.

[147]. P. Sun and R. Luo, “Analytical modeling for crosstalk noise induced by process variations among CNT-based interconnects,” *In 2009 IEEE International Symposium on Electromagnetic Compatibility*, pp. 103-107, 2009.

[148]. H. Sheikhassadi, N. Masoumi and A. Hakimi, “Crosstalk modeling in multiwalled carbon nanotubes as interconnects using the compact RC model,” *In 2011 IEEE 15th Workshop on Signal Propagation on Interconnects (SPI)*, pp. 133-136, 2011.

[149]. V. R. Kumar, B. K. Kaushik and Amalendu Patnaik, “Improved crosstalk noise modeling of MWCNT interconnects using FDTD technique,” *Microelectronics Journal*, vol. 46, no. 12, pp. 1263-1268, 2015.

[150]. M. R. Khezeli, M. H. Moaiyeri and A. Jalali, “Analysis of crosstalk effects for multiwalled carbon nanotube bundle interconnects in ternary logic and comparison with Cu interconnects,” *IEEE Transactions on Nanotechnology*, vol. 16, no. 1, pp. 107-117, 2016.

[151]. M. D'Amore, M. S. Sarto and A. Tamburrano, “Transient analysis of crosstalk coupling between high-speed carbon nanotube interconnects,” *In 2008 IEEE International Symposium on Electromagnetic Compatibility*, pp. 1-6, 2008.

[152]. S. G. Hamedani and M. H. Moaiyeri, “Comparative analysis of the crosstalk effects in multilayer graphene nanoribbon and MWCNT interconnects in sub-10 nm technologies,” *IEEE Transactions on Electromagnetic Compatibility*, vol. 62, no. 2, pp. 561-570, 2019.