INVESTIGATIONS ON MULTILEVEL CONVERTER INTERFACE FOR ELECTRIC VEHICLE CHARGING

A Thesis submitted in fulfillment of the requirements for the award of the degree of

Doctor of Philosophy

Submitted By

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CERTIFICATE

I hereby certify that the work which is being presented in the Thesis entitled, ***"INVESTIGATIONS ON MULTILEVEL CONVERTER INTERFACE FOR ELECTRIC VEHICLE CHARGING"*** in fulfillment of the requirement for the award of the Degree of ***Doctor of Philosophy*** submitted in the ***Electrical & Instrumentation Engineering Department*** of the **Thapar Institute of Engineering & Technology** is an authentic record of my own work carried out under the supervision of **Dr. Sanjay K. Jain** and **Dr. Krishna Kumar Gupta** and refer other researcher's work, which are duly listed in the reference section.

The matter presented in this Thesis has not been submitted for the award of any other degree of this or any other University.

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This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

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Date: 28.07.2023

.....dedicated to
My family

Abstract

Increasing concerns over the pollution caused by the tailpipe emissions from the internal combustion engine based vehicles and the limited availability of fossil fuels have greatly paced up the adoption of Electric Vehicles (EVs). Recent advances in battery technologies, power electronics, digital controllers, electric machines and sensing technologies have laid the foundation for the development of the next generation EV technology. As such, power electronics interface plays a pivotal role in EV battery charging. The power electronics interface for both on-board and off-board EV charging generally comprises two stages: (a) AC-to-DC conversion stage with Power Factor Correction (PFC) and regulation of the intermediate DC link voltage; and (b) DC-to-DC conversion stage for regulating the charging current for the EV battery. This work deals with novel PFC converters for the AC-to-DC conversion in the futuristic and emerging EV charging systems. Multilevel Rectifiers (MLRs) have been specifically investigated as they offer numerous advantages, such as: utilization of low voltage power switches, highly improved harmonic profile of the alternating voltage at the input terminals, low dv/dt stress, modularity and so on. The major features identified for such multilevel PFC rectifiers for the upcoming two-stage EV charging systems are: (a) wide range of the output DC voltage so that a large spectrum of EV-battery voltages (typically between 72V to 800V in the commercially available EVs) can be addressed with minimal strain on the downstream DC-to-DC converter; (b) possibility of bidirectional flow of power so that Vehicle-to-Grid (V2G) mode of operation can be attained; (c) easy realization and extension of the power converter for both single- and three-phase systems; (d) possibility of multi-output operation so that multiple EVs can be simultaneously charged using a common central PFC rectifier; and (e) possibility of self-balancing of the capacitors in the MLR so that complexity in the overall control is minimized.

The conventional multilevel topologies, when operated as inverters, work with unity voltage gain. As a result, while performing AC-to-DC conversion, they work as boost rectifiers, thereby severely limiting the range of output voltage. Difficulty in voltage balancing of capacitors and extension to three-phase systems are other additional limitations of many of the MLRs proposed

till date. Thus, this work begins with the examination of topological and operational features of switched-capacitors based multilevel topologies, which have been mainly proposed as inverters (SCMLIs), in a standalone mode of operation (i.e. without being connected to the grid). SCMLIs offer inherent boost (i.e. the voltage gain is greater than unity in the inverter mode) and sensor-less self-balancing of capacitors. The question raised (and answered subsequently) in this work is: can switched-capacitors based multilevel topologies perform PFC rectification while offering wide output range (by virtue of inherent gain) and preserving self-balancing of capacitors' voltages. Therefore, to begin with, a novel grid-connected 13-level switched-capacitors' based inverter is presented. The topology is realized through 12 power switches, 2 diodes, and 3 self-balanced capacitors. It offers an overall voltage gain of six. The capacitors remain self-balanced for all values of the modulation index. The presented topology is validated experimentally and is found to be highly modular and cost-effective in comparison to other similar SCMLIs. Study of such a grid-connected SCMLI sets the stage for studying the 'role reversal' so as to perform rectifier operation.

The work on the development of a novel PFC five-level rectifier utilizes self-balanced switched capacitors. Each leg of the presented topology comprises five power switches and one switched capacitor, where the voltage ratings of power switches are equal to the output DC voltage. It does not require an additional filter capacitor on the DC side, as the load always appears in parallel with a switched capacitor of one of the legs. The five-level operation with continuous conduction leads to the elimination of the capacitive filter on the AC-side and inductive filter on the DC-side. The performance of the presented topology is discussed through operating principle, modulation strategy, closed-loop control, and design aspects and it is validated through experimental results. Its features such as buck operation with a wide output regulation, the possibility of bidirectional flow of power needed for V2G systems, and easy realization of its three-phase version by simply adding one more leg make the topology suitable for EV charging application. While this topology establishes the proposed theory of role reversal in switched capacitors based multilevel topologies, it synthesizes only five levels with a voltage gain of two. In order to further increase the number of levels and voltage gain, two seven-level rectifiers with voltage gain of three are conceptualized. The working principle, modulation strategy and applications of the proposed topologies have been discussed and are validated through experimental results. The first of these seven-level topologies use reduced number of

components, but a few of the power switches experience a voltage stress equal to thrice the output DC voltage, and hence it is not extended to its three-phase version. The second seven-level topology uses power switches with equal voltage stress and is highly modular, and hence it is investigated for three-phase operation too. This three-phase topology, however, becomes complex to be used for multiple outputs, as it requires a large number of capacitors.

Finally, a novel five-level SCs based self-balancing buck PFC MLR is proposed with a wide output voltage range, which can operate with different loads at the output terminals and also operate in both single and multiple output modes. Moreover, load voltage balancing is feasible even when the multiple loads have different values. The proposed rectifier performs buck operation and offers a wide output voltage regulation, which is suitable for EV battery charging. The performance of the presented topology has been investigated through operating principle, modulation strategy, closed-loop control and experimental validation for the operation with single-/multiple-output load variations. The load voltage stabilizes at reference DC voltage when the grid current is raised, unity power factor mode of operation is preserved. The proposed rectifier exhibits high techno-economic feasibility when compared against other such structures.

Keywords: Bidirectional, Buck-boost rectifier, Electric vehicle, Grid-to-vehicle, Multilevel converter, Power factor correction, Switched capacitor, Vehicle-to-grid, Wide output voltage range.

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Anekant Jain

Contents

List of Figures

List of Tables

Abbreviations

Acronyms

ANPC	Active Neutral Point Clamped
BEV	Battery Electric Vehicle
BF	Boosting Factor
CCM	Continuous Conduction Mode
CF	Cost Function
CHB	Cascaded H-bridge
DAB	Dual-Active-Bridge
DCM	Discontinuous Conduction Mode
EMI	Electromagnetic Interference
EPS	Electric Propulsion Systems
EV	Electric Vehicle
FC	Flying Capacitor
FCMLI	Flying Capacitor Multilevel Inverter
G2V	Grid-to-Vehicle
GHG	Greenhouse Gas
HB	H-bridge
HEV	Hybrid Electric Vehicles
ICEs	Internal Combustion Engines
LSPWM	Level-Shifted Pulse-Width Modulation
MLI	Multilevel Inverter
MLR	Multilevel Rectifier

NPC	Neutral Point Clamped
PF	Power Factor
PFC	Power Factor Correction
PHEV	Plug-in HEV
PI	Proportional-Integral
PIV	Peak-Inverse-Voltage
PLL	Phase-Lock Loop
PR	Proportional Resonant
PWM	Pulse-Width Modulation
RES	Renewable Energy Source
RMS	Root Mean Square
SC	Switched Capacitor
SCMLI	Switched Capacitors based Multilevel Inverter
SCMR	Switched-Capacitor-based Multilevel Rectifier
SCs	Switched Capacitors
SDP	Switching Device Power
SHE	Selective Harmonic Elimination
SOC	State-of-Charge
SST	Solid State Transformer
SVM	Space Vector Modulation
THD	Total-Harmonic-Distortion
TSV	Total Standing Voltage
UPF	Unity Power Factor
V2G	Vehicle-to-Grid
WBG	Wide-Bandgap

Chapter–1

Introduction

In this chapter, a brief background is presented on the power electronics interface for charging systems for Electric Vehicle (EV). Specifically, the state-of-art pertaining to the Power Factor Correction (PFC) rectifiers is discussed to explicate the research objectives of this work. A more detailed literature review on PFC rectifiers is presented in the following chapter. In addition, the organization of the Thesis is also described briefly.

1.1 GENERAL

Road vehicles are integral to the modern civilized life and they are a popular means of transportation all over the world. These vehicles mostly utilize Internal Combustion Engines (ICEs) for traction. The popularity of ICEs based vehicles is mainly because of their fast dynamic response, long range and easy and quick refueling [1]. However, these vehicles use fossil fuels and therefore are a major cause of air pollution and greenhouse gas emissions [2]. Though electric motors too are employed for traction purposes, the majority of such application is for railways [3]. In general, electric motors have better efficiency than ICEs and hence use of Electric Propulsion Systems (EPS) is also gaining importance for road vehicles. The class of vehicle that uses an EPS is referred to as EV. This class of EVs include Battery Electric Vehicle (BEV), Hybrid Electric Vehicles (HEV) and Plug-in HEV (PHEV) [4]. In the past decade, however, the BEVs have become synonymous with EVs.

Historically, the first EVs were driven in the 1830s. At that time, the battery was not a rechargeable type, and gradually the interest in EVs faded away. The concern for the environment, however, stimulated the automotive industry to renew their interest in the EVs. Of course, the advent of new battery technologies, power electronics and digital controllers has laid the foundation for the development of EV technology.

Even in its current nascent stage, the Indian EV market is growing rapidly, as depicted in Fig. 1.1, which shows the sales of EVs in various financial years. Further adoption of EVs (especially in the passenger car segment), however, will be greatly dependent on the growth of charging infrastructure in the country [5].

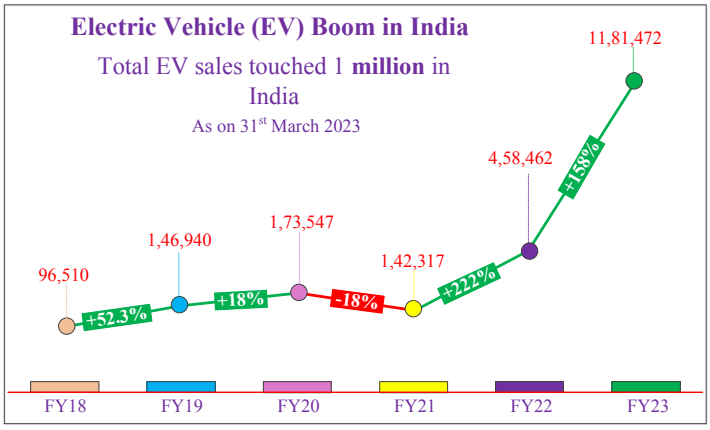


Fig. 1.1: *Total EV sales in India as on financial year 2022-23*

1.1.1 EV drivetrain and charging

The electrical drivetrain of EVs, shown in Fig. 1.2, involves various power processing stages, utilizing power converter circuits to ensure power delivery at the correct voltage during battery charging and to ensure optimum power to propel the vehicle [6].

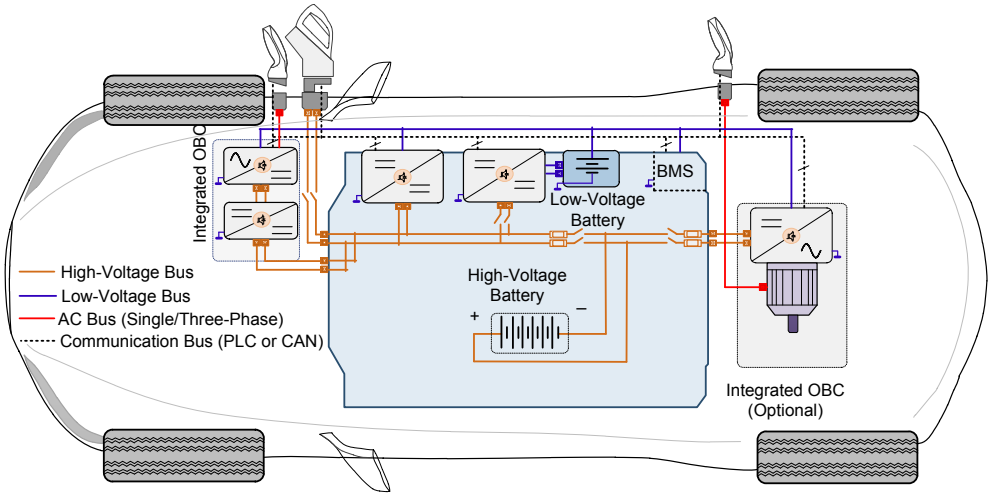


Fig. 1.2: *Basic drivetrain of electric vehicle*

Although EVs offer several environmental and economic advantages, certain factors have been affecting their widespread adoption [7, 8], range anxiety being the most prominent of them. Range anxiety can be mitigated by bolstering the charging infrastructure, as enhanced charging infrastructure can facilitate the users to recharge their vehicle more frequently. Charging infrastructure, thus, is poised to become a key factor for a significant penetration of the EV technology [9].

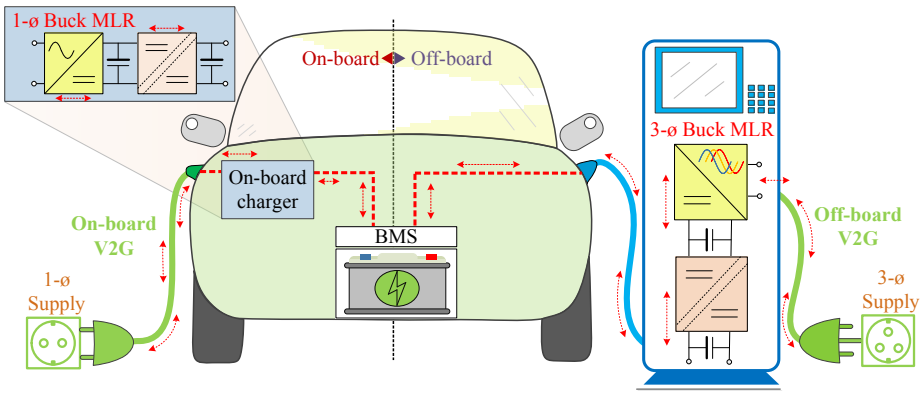


Fig. 1.3: *Basic block diagram of on-board and off-board charging*

The central role in fulfilling the charging needs of an EV is played by a power electronics interface, with the assistance of communication, sensing and protection technologies [10]. The power electronics interface of an EV charging system generally comprises two stages: a PFC rectifier stage, followed by a DC-to-DC converter [11, 12]. The PFC stage aims at synthesizing sinusoidal input current in-phase with the supply voltage and to yield a regulated DC output [13]. The DC-to-DC converter is used to regulate the current corresponding to the State-of-Charge (SOC) of the EV battery. The main focus of this research work is on the PFC rectifier stage. Many a times, an Electromagnetic Interference (EMI) filter is also used between the AC source and the PFC stage [14]. These constituents (viz. power converters and filters) can be integrated into the vehicle itself, leading to an on-board charging system, or they can be placed in a specially designed EV charging station as an off-board charging system [15]. As per power requirements, these systems are fed with single-phase or three-phase AC supply [16, 17]. As exemplified in Fig. 1.3, a single-phase supply is used for the charging power between 2 kW-8 kW, while three-phase supply is used for a charging power of 19.2 kW [18]. Thus, the conceptualization of the power converter for the PFC stage begins with the consideration of AC supply. Various charging levels and their associated powers are summarized in Table 1.1 [19].

Table 1.1. *Charging power levels, type and supply interface for EV charging*

Level	Charger Type	Input Supply	Supply Interface	Power Level
Level-1	On-board single-phase	120 V rms	Convenience outlet	1.4 kW (12 A) 2 kW (20 A)
Level-2	On-board single/three-phase	230 V rms	Dedicated charging point	8 kW (32 A) 19.2 kW (80 A)
Level-3	Off-board three-phase	415 V rms	Dedicated charging point	50 kW − 200 kW

In Fig. 1.4, a more comprehensive breakdown of the charging options is provided, revealing how various standards classify the alternatives differently. Despite these differences, there is an overarching convergence towards a common scheme. For lower power ranges, typically up to 25 kW, AC charging solutions are more common, while DC charging options are designed to handle higher power levels, up to approximately 400 kW, with projected capacities reaching as high as 900 kW. Additionally, wireless charging and battery swapping are also part of the charging ecosystem [20].

It is also worth mentioning here that in order to fully exploit a wide-spread adoption of EVs for the benefit of the grid, the power electronics interface should facilitate bidirectional power flow to allow both Grid-to-Vehicle (G2V) and Vehicle-to-Grid (V2G) modes of operations [21]. A V2G system can provide additional opportunities for grid operators [22–25], including reactive power support, active power regulation, load-balancing, peak shaving and current harmonic filtering to yield improved efficiency, stability and reliability [26].

The rated voltage of battery, a key component of an EV system, is found to be varying significantly for different types of EV [27]. In general, a battery with higher voltage is suited for longer driving range and better performance [28]. The higher voltage allows fast-charging. However, its range depends on the specific vehicle and battery technology. The usage of some of the highest-voltage batteries is found in luxury EV like the Porsche Taycan, which boasts an 800V battery pack [29].

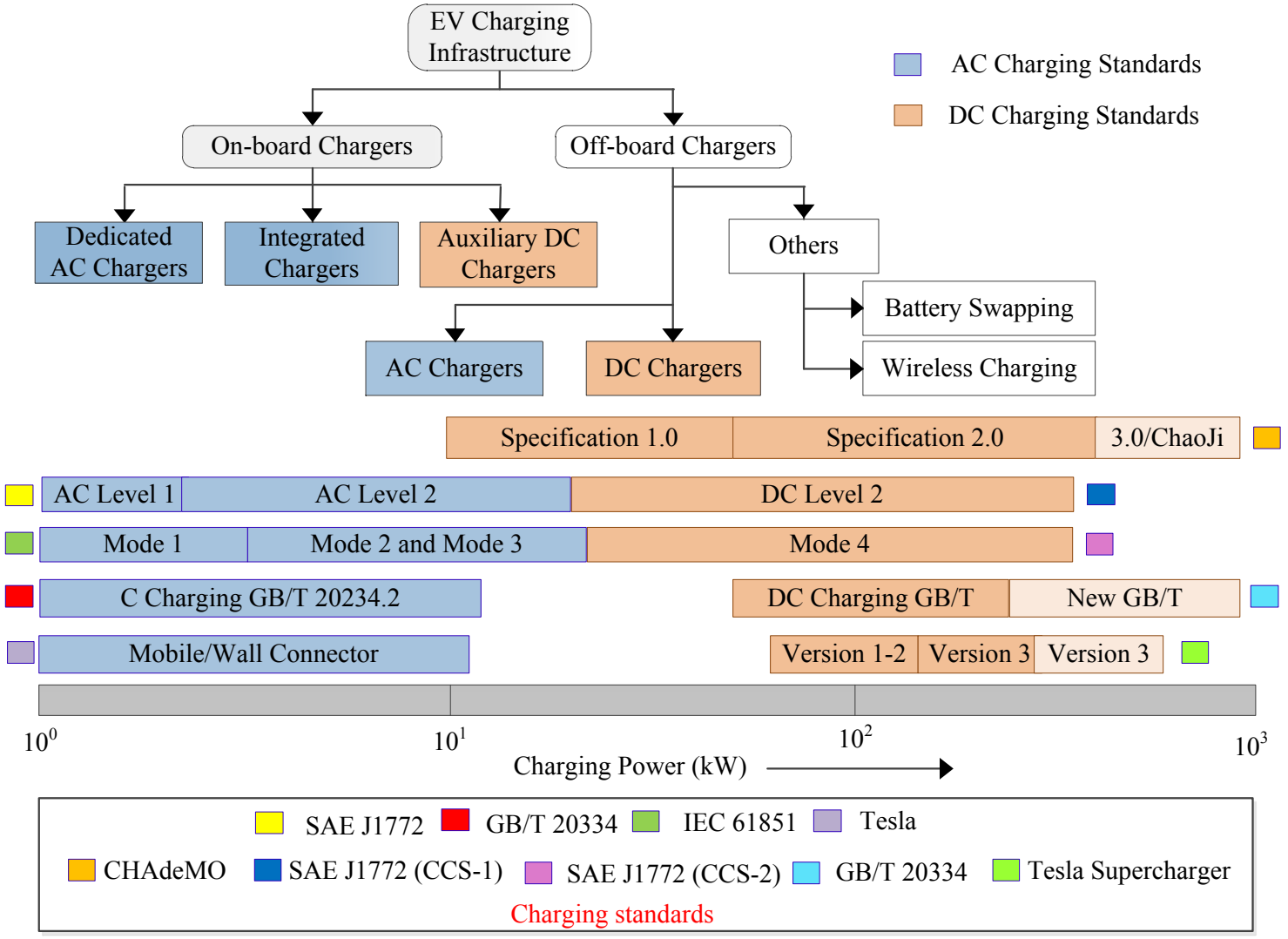


Fig. 1.4: *Classification of EV charging infrastructure*

Moreover, some lower voltage 72V batteries is found in Indian EVs like Tata Tigore. Specifications of EV models with their wide battery nominal voltage shown in Table 1.2. Higher voltages can also allow the utilization of more powerful electric motors, which can translate to faster acceleration and higher top speeds [30]. However, the usage of batteries of higher voltages require a powerful charging infrastructure or advanced battery management systems, which can make EV more expensive to produce and maintain.

In view of these discussions, a summary of the essential aspects of the power electronics interface of an EV charging system is presented in the following sub-section.

Table 1.2. *Specifications of EV models with their wide battery nominal voltage*

Model	**Manufacturer**	**Rated energy**	**On-board charging power**	**Maximum charging power**	**Battery voltage**
Tigor	Tata	26 kWh	3.3kW	25kW	72V
E Verito	Mahindra	21.2 kWh	1.8 kW	15 kW	72V
Comet	MG	25 kWh	3.3 kW	17.3 kW	220V
Nexon	Tata	30.2 kWh	3.3 kW	25 kW	320V
Ioniq	Hyundai	40.4 kWh	7.2 kW	100 kW	320V
Bolt	Chevrolet	62.2 kWh	7.4 kW	50 kW	350V
Kona	Hyundai	64 kWh	7.2 kW	77 kW	356V
Leaf	Nissan	40 kWh	6.6 kW	50 kW	360V
E-tron 55 Quattro	Audi	95 kWh	11 kW	150 kW	396V
Model S	Tesla	100 kWh	11.5 kW	250kW	400V
EQC 400 4Matic	Mercedes	85 kWh	7.4 kW	150 kW	405V
Polestar 2	Volvo	75 kWh	11 kW	150kW	450V
Taycan 4S	Porsche	79.2 kWh	11 kW	270 kW	800V

1.1.2 Key power converter features for EV charging systems

In order to effectively accommodate the specifications/battery voltages of the commercially available EVs and available power source (single- and/or three-phase), while efficiently charging the EV battery and supporting the utility grid, some essential features of the power converters are summarized herewith:

1. Power factor: A high power factor near unity is essential for EV charging to maximize energy efficiency, minimize power losses, optimize power grid utilization, and reduce overall electricity consumption and cost.

2. Single and three-phase power converters: Single-phase PFC rectifiers are commonly used for onboard EV charging due to their compactness and lightweight design, making them suitable for charging from a standard household outlet. On the other hand, three-phase PFC rectifiers are used for off-board EV charging, as they provide higher power output, making them suitable for fast charging stations with high charging demands.

3. Bidirectional power flow: A bidirectional power converter is crucial for both G2V charging and V2G discharging processes in EVs. It includes components such as an AC-to-DC converter, DC-to-DC converter, and DC-to-AC inverter. It efficiently manages the bidirectional flow of electricity, complies with safety standards, and incorporates advanced control algorithms for seamless communication between the EV, the grid, and the converter.

4. Wide voltage range: EV chargers must provide a wide range of output DC voltage to accommodate different nominal battery voltage levels. To meet this requirement, EV chargers must be designed with efficient and reliable voltage regulation and current control mechanisms, ensuring safe and optimal charging performance for different EVs and batteries.

Now, conventionally, the rectification with PFC is achieved by employing an H-bridge (HB) active converter or by using a boost DC-to-DC converter alongwith a diode rectifier [31, 32]. Recently, however, the so-called multilevel converters (i.e., Multilevel Inverter (MLI) for DC-to-AC and Multilevel Rectifier (MLR) for AC-to-DC) have emerged as attractive alternative due to numerous advantages offered by them [33].

If V_{DC} is the output DC voltage, then the HB rectifier produces three distinct voltage levels ($\pm V_{DC}$ and 0) at the input terminal, effectively functioning as a boost PFC rectifier for both single-phase and three-phase [34, 35]. The T-type rectifier topology is also applicable for three-level operation, in addition to its effectiveness as a boost PFC rectifier for both single-phase and three-phase extensions. It generates three voltage levels at the input terminal, consisting of $\pm\frac{V_{DC}}{2}$ and 0 [35, 36]. The Neutral Point Clamped (NPC) and Flying Capacitor (FC)-based rectifier topologies are suitable for five-level operation, consisting of $\pm V_{DC}$, $\pm\frac{V_{DC}}{2}$, and 0. These topologies operate in boost mode with unity power factor and are effective for both single-phase and three-phase extensions [37–40]. These conventional topologies operate in boost mode and limit the range of output voltage. Another category of PFC rectifiers based on output voltage is the multilevel buck PFC rectifier. These rectifiers operate in single-phase and are only applicable for multi-output operation. The topologies presented in [41, 42] generate five voltage levels at the input terminal (i.e., $\pm 2\ V_{DC}$, $\pm V_{DC}$, and 0) and produce two buck DC output voltages. Another topology [43] is implemented for generating nine voltage levels and produces three buck DC output voltages. This topology is also limited to single-phase operation.

In this work, Switched Capacitor (SC) based multilevel topologies have been investigated to achieve a wide range of output voltage in rectifier mode (i.e., buck and boost), and to enable both single-phase and three-phase operation. Additionally, these topologies allow for bidirectional power flow and can operate with either single or multiple outputs. The SCs-based topologies [44, 45] have been used mainly as DC-AC inverters. When used as an inverter, SC-based multilevel topologies enable inherent voltage gain greater than one, allowing for boost operation [46]. In role reversal operation, these topologies can operate as a buck for rectification.

Based on the above discussions, a summary of the research-focus of this work is presented in Fig. 1.5 which shows various categories of PFC rectifiers, taking into account the number of voltage levels, possibility of bidirectional power flow, range of the regulated DC output voltage (with buck, boost or buck-boost modes of operation), number of outputs and the type of input supply (single- or three- phase).

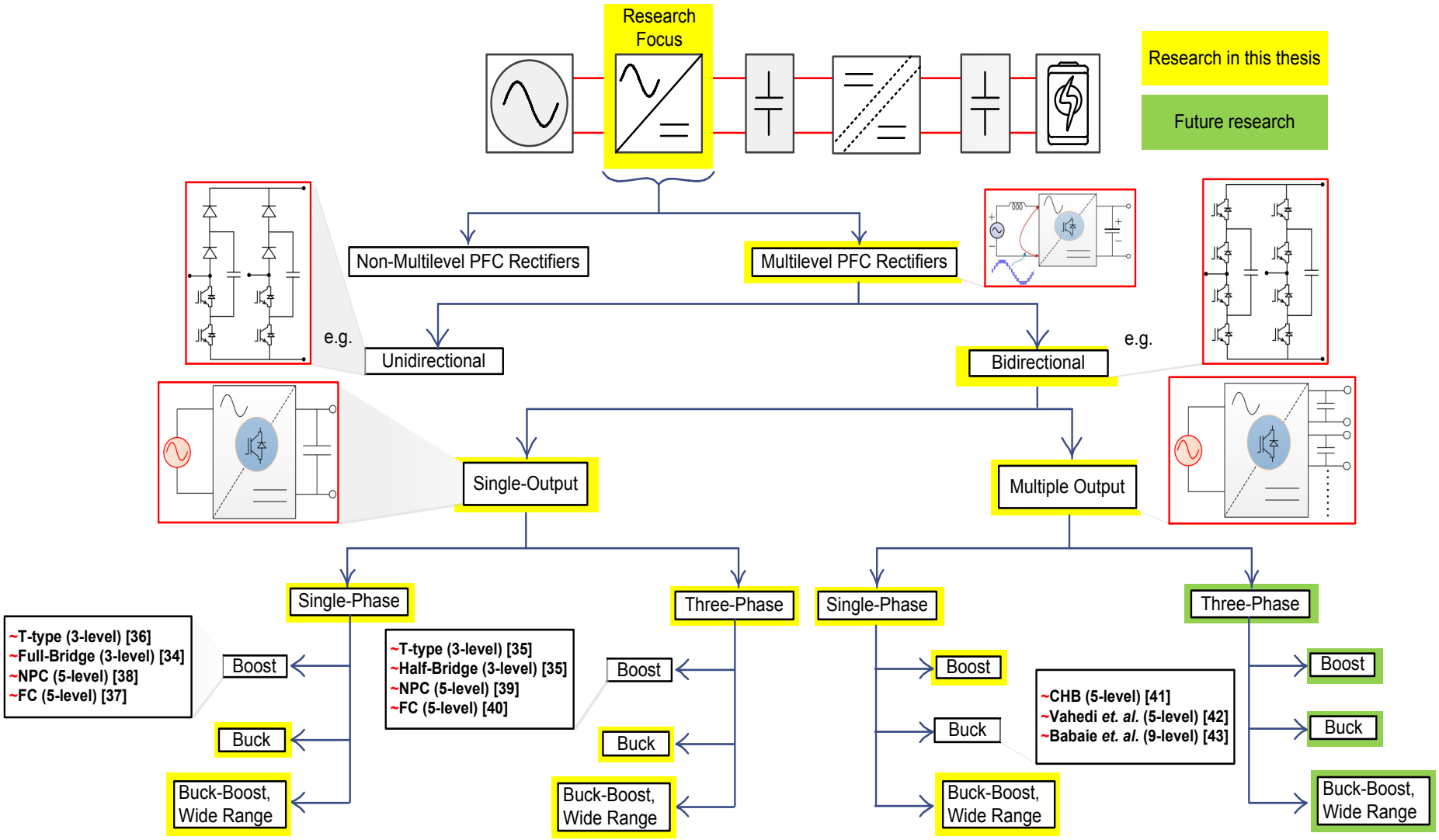


Fig. 1.5: *A classification of PFC rectifiers considering their application in the modern EV charging systems*

1.2 STATE-OF-ART: PFC RECTIFICATION

PFC rectifiers have a long history, dating back to the early days of AC power distribution. In the early 20th century, the power factor of AC power systems was typically low due to the use of inductive loads such as motors and transformers, which led to significant power losses and reduced efficiency in power transmission and distribution systems. The development of PFC rectifiers was driven by the need to improve power factor and reduce energy consumption. Early PFC rectifiers were based on passive circuits such as diode bridges and LC filters, which had limited PFC capabilities. However, in the 1970s, the development of active PFC rectifiers, using techniques such as boost converters, brought significant improvements in PFC [47]. One of the most important developments in PFC rectifiers came in the 1980s with the introduction of the Vienna rectifier [48]. This rectifier uses a three-phase input and a specially designed circuit topology to achieve near-unity PFC. The Vienna rectifier has been widely used in high-power applications, such as industrial motor drives and renewable energy systems [49].

For PFC rectification and improved power quality, the emergence of multilevel converters marked a turning point in the field of power electronics. By utilizing multiple levels of voltage, multilevel converters could significantly reduce switching losses, resulting in improved power quality and higher efficiency. One study by [50] compared a three-level NPC converter and a traditional two-level PFC converter for a 10 kW PFC rectifier, and found that the three-level NPC converter had lower harmonic distortion, lower switching loss, and higher efficiency. Multilevel converters can improve power quality in PFC rectifiers. Over the years, various multilevel topologies have been proposed and analyzed. The basic HB multilevel inverter was first introduced in the early 1980s [51]. This topology consists of a series of HB cells, with each cell containing four power switches and two capacitors. By controlling the switching of the power devices, the HB inverter can produce a staircase waveform with several voltage levels. The HB inverter is simple in structure and easy to control, making it a popular choice for low-voltage and low-power applications. The HB topology can also be implemented for bidirectional operation as a boost PFC rectifier.

The T-type multilevel inverter is another popular topology that consists of two capacitors and four power switches, and it generates a staircase waveform with several voltage levels. The T-type inverter has a lower number of components compared to the HB inverter, making it

more suitable for high-voltage and medium-power applications. The NPC multilevel inverter, also known as the diode-clamped inverter, was first proposed as a three-level converter in the early 1980s [52]. The NPC inverter uses diodes to clamp the neutral point of the DC bus to a fixed voltage level, which reduces the voltage stress on the power devices and improves the system reliability. The NPC inverter has been extended to higher voltage levels by adding more capacitors and power semiconductor switches, making it a popular choice for high-power and high-voltage applications.

The Flying Capacitor Multilevel Inverter (FCMLI) was introduced in the early 2000s as a modification of the NPC inverter [53]. The FCMLI topology reduces the number of components required in the converter by using flying capacitors to achieve the same number of output voltage levels. The FCMLI has a simpler structure compared to other multilevel topologies, making it suitable for high-frequency applications and achieve boost PFC rectification. The multilevel buck rectifier based on the Cascaded H-bridge (CHB) topology [41] provides multiple DC outputs. In the CHB structure, each module on the AC side interact with the others to obtain an almost sinusoidal current that is in phase with the grid voltage. There are two other topologies of multi-output buck MLR, five-level rectifiers with the possibility of two outputs [42], and a nine-level rectifier with three outputs [43].

In recent years, research has focused on improving the efficiency and performance of PFC rectifiers through the use of advanced semiconductor devices such as wide bandgap materials (silicon carbide and gallium nitride) and soft-switching techniques such as resonant converters. Overall, PFC rectifiers have become an essential component of modern power supplies, with significant improvements in efficiency and PFC being achieved through the use of active control techniques and advanced semiconductor devices.

1.3 RESEARCH OBJECTIVES

As discussed in the previous sections, while PFC multilevel rectification technology offers numerous advantages, it is to be seen if it fully achieves the desired features for PFC converters in EV charging systems, as pointed out in section 1.1.2. Additionally, a detailed review on multilevel converters (presented in the next chapter) also indicates certain challenges, of which

the most important is balancing the voltages of the capacitors. Hence, in this work titled as **Investigations on Multilevel Converter Interface for Electric Vehicle Charging**, following research objectives have been identified:

1. To study multilevel converter topologies suited for electric vehicle charging.
2. To design multilevel converter interface for electric vehicle charging.
3. To develop a control scheme for Unity Power Factor (UPF) operation.
4. Extend the developed topology for modular multilevel converter suited for charging station.

1.4 THESIS ORGANIZATION

After accomplishing the above-stated objectives, the thesis has been organized as per the following details:

The **Chapter 1**, summarizes a brief introduction on power conversion aspects of the EV charging system. It provides summary of onboard and off-board charging systems, state of art, research objectives and Thesis organization.

In **Chapter 2**, provides a comprehensive review on PFC rectifier topologies. Based on the output DC voltage the literature review is classified into non-multilevel boost rectifier, buck recttifier and buck-boost rectifier. The multilevel rectifiers are also classified as boost and buck rectifier. The summary of identified research areas and research contributions are also presented.

In **Chapter 3**, a newly proposed SCs based MLI is first studied as a grid-connected inverter and thereafter, it has been established theoretically that, such topologies would indeed perform buck rectification. In this chapter, a detailed analysis of the SC cell is presented, and the bidirectional operation is explained. The theoretical observations are validated through an experimental study.

In **Chapter 4**, the implementation of an SCs-based five-level PFC rectifier is presented. The analysis and design of the SCs-based single-phase five level rectifier is presented to achieve the wide range of DC output (i.e., buck and boost). The proposed single-phase topology is

further extended for a three-phase version. The theoretical observations of the single-phase and three-phase PFC rectifier are validated experimentally.

In **Chapter 5**, the PFC rectifier topology is investigated to enhance the level of terminal voltage and improve the gain. By increasing the number of levels and the gain factor, the output voltage range is also increased. Another topology is described that can be suitable for three-phase seven-level rectification. Moreover, the modularity that can describe the changes in voltage levels is shown. Finally, an experimental study is presented to confirm theoretical observations.

In **Chapter 6**, the operation is validated with single- or multiple-output load variations. The chapter explains the need for a multi-output PFC rectifier in EV charging applications and discusses the limitations of existing multi-output topologies. A solution is proposed by using an SCs-based topology. Finally, an experimental study is presented to confirm the theoretical observations.

Chapter 7 presents a summary of the conclusions of the studies presented in previous chapters. Further, the scope of further research is also summarized in this chapter.

Chapter–2

Literature Review

In this chapter, a succinct introduction is provided on the multilevel PFC rectifier. In particular, the classification of multilevel PFC rectifier topologies is presented. The chapter briefly discusses buck and boost PFC rectifiers, categorized according to the range of output voltage. Additionally, the features necessary for EV charging are discussed and compared with multilevel rectifier topologies. Furthermore, the chapter highlights identified research areas and research contributions.

2.1 GENERAL

The PFC rectifier stage is an essential component of the EV charging system and is responsible for converting AC input voltage into regulated DC voltage with high power factor and low harmonic distortion. The typical constituents of the PFC rectifier system are shown in Fig. 2.1, wherein the power converter is fed from an AC power supply (the grid voltage is shown as 'v_s') through filtering components (inductors and/or capacitors) to obtain a filtered and regulated output DC voltage (V_{DC}). The aim is to modulate the power converter in a manner that the current 'i_s' drawn from the grid acquires a sinusoidal shape and is in phase with the grid voltage, and at the same time the output voltage V_{DC} remains regulated.

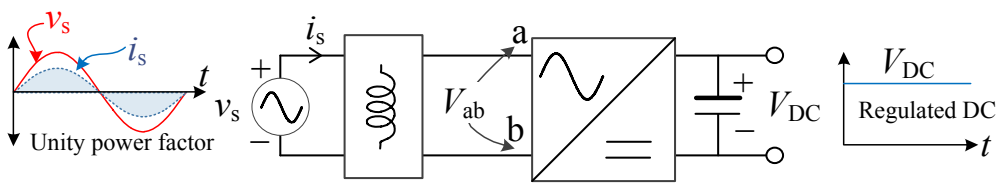


Fig. 2.1: *Structure of typical PFC rectifier*

Grid current 'i_s' is controlled by controlling the terminal voltage V_{ab}, and with a better harmonic profile of V_{ab}, a much improved shape of 'i_s' can be achieved [54]. Till date, numerous power converter topologies for PFC rectification have been proposed and implemented [55–57]. Some of these topologies are highly application-specific, such as: on-board EV chargers [54], off-board EV chargers [58], electric drives [59, 60], data centers [61], lighting [62, 63] etc.

PFC rectifiers with single and three-phase AC input are classified based on the magnitude of the output DC voltage. Buck rectifiers provide an output voltage that is lower than the grid peak voltage [64], while boost rectifiers provide an output voltage that is higher than the grid peak voltage [34]. Buck-boost PFC rectifiers, on the other hand, are capable of achieving an output voltage that spans a wide range, either lower or higher than the grid peak voltage. The possibilities for the output DC voltage are shown in the Fig. 2.2.

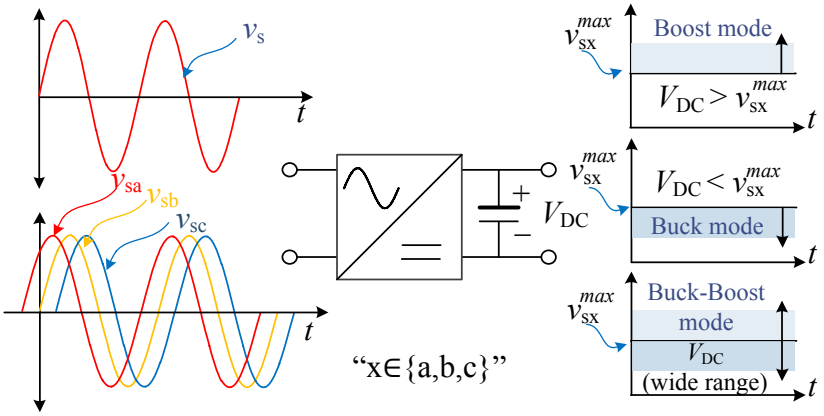


Fig. 2.2: *Possibilities of the output DC voltage for single-and three-phase power supply*

To regulate the output DC voltage and achieve unity power factor, it is important to consider the terminal voltage i.e., the synthesized voltage, which is the voltage difference between points 'a' and 'b' where the grid supply is connected with the filter as shown in the Fig. 2.1. This voltage is dependent on both the grid current and the output DC voltage [54].

A conventional bridge PFC rectifier uses a diode-bridge followed by a DC-to-DC boost converter. Without the DC-to-DC converter, the synthesized voltage 'V_{ab}' is as good as the grid voltage, but the input current is highly distorted due to the presence of a load capacitor. This capacitor charges quickly at the peak of the input voltage and discharges slowly, leading to

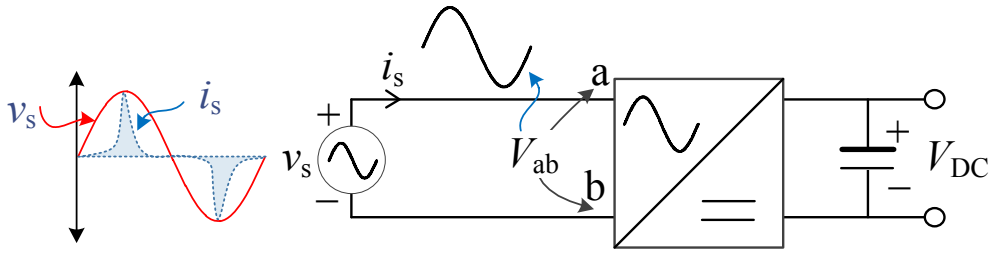


Fig. 2.3: *Conventional bridge rectifier*

non-linear current flow and multiple harmonics in the current waveform, as shown in the Fig. 2.3. As a result, a poor power factor, known as the harmonic power factor, is obtained. To overcome this, a DC-DC boost converter is used before the DC-bus capacitor [47]. This results in a two-stage PFC conversion that is suitable for low power applications [65]. However, for improved efficiency and suitability for high power applications, specific power factor correction techniques with particular topologies need to be employed. For optimal power factor, the waveforms of the voltage and current should be identical so that maximum power can be delivered under all conditions [31].

As mentioned earlier, the terminal voltage 'V_{ab}' plays an all-important role in shaping the input current and employing a multilevel converter greatly improves this terminal voltage. Consequently, the PFC rectification topologies can also be classified into two major categories: non-multilevel and multilevel topologies. These non-multilevel rectifiers are further divided into three main categories: PFC boost rectifiers, PFC buck rectifiers, and PFC buck-boost rectifiers [66, 67]. The active multilevel realization of PFC rectifiers is another class that has gained attention from researchers. The following sections provide a brief overview of this rectifier topologies:

2.2 NON-MULTILEVEL PFC RECTIFIER TOPOLOGIES

Based on the magnitude of output DC voltage, non-multilevel PFC rectifiers are classified into three categories: buck, boost and buck-boost PFC rectifiers.

'Boost' refers to the fact that in this class of rectifiers, the magnitude of output DC voltage is greater than the peak value of the input AC voltage [34, 36], which is found to be unsuitable to directly feed the DC-bus of EV battery, and hence requires either a subsequent step-down DC-DC converter at the DC side, or a step-down transformer at the AC side. Both these approaches add to the volume, costs and power losses in the system. However, the consideration of constant output DC voltage and PFC operation at the input do not require bulky filters either at the AC side or the DC side.

'Buck' refers to the fact that in this class of rectifiers, the magnitude of the output DC voltage is lower than the peak value of the input AC voltage. Such rectifiers provide a wider control range for the output DC voltage, as compared to the boost rectifiers [64, 68]. PFC buck rectifiers, however, generally exhibit Discontinuous Conduction Mode (DCM), due to which the regulation of output voltage becomes difficult and necessitates large filters on the DC side.

'Buck-boost' type of rectifiers can operate in buck as well boost modes [69]. Many a times, they employ a low number of switches and integrate the magnetic elements to reduce the total size and volume of the converter [70, 71]. In many cases, however, bridge-less buck-boost rectifiers do not offer bidirectional power flow and easy extension to three-phase module [69–71].

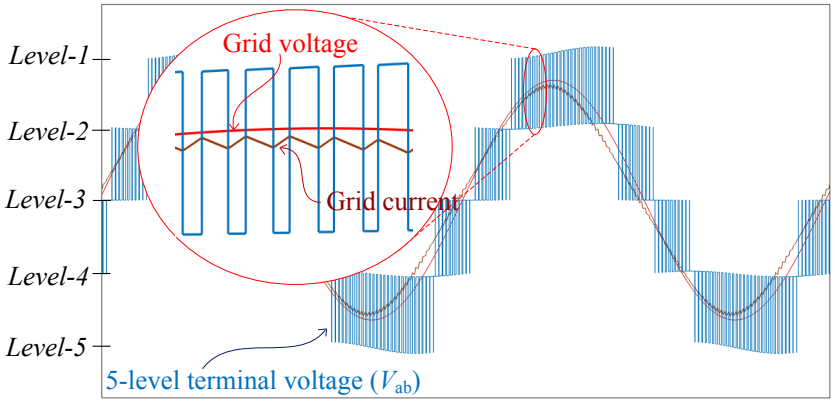


Fig. 2.4: *Pertaining to the improvement in grid current with a multilevel terminal voltage*

2.3 MULTILEVEL PFC RECTIFIER TOPOLOGIES

Another categorization of PFC rectifiers is based on the fact that a grid-connected voltage source rectifier synthesizes a voltage to control the grid current. If the synthesized voltage is improved by increasing the number of voltage levels, the grid current can be consequently improved [54], as

shown in Fig. 2.4. These rectifiers are known as MLRs, and the synthesized terminal voltage can be as high as '*N*' levels, as shown in Fig. 2.5. Multilevel converters offer numerous advantages, some of which are [53, 72, 73]:

Advantages based on waveform*:* include lower voltage ratings of power switches, a much better harmonic profile of the AC waveform, reduced dv/dt stress, small passive components, possibility of fault-tolerant operation, and so on.

Advantages based on topology*:* include bidirectional operation, wide range of output voltage, possibility of single or multiple outputs, possibility of three-phase extension, and so on.

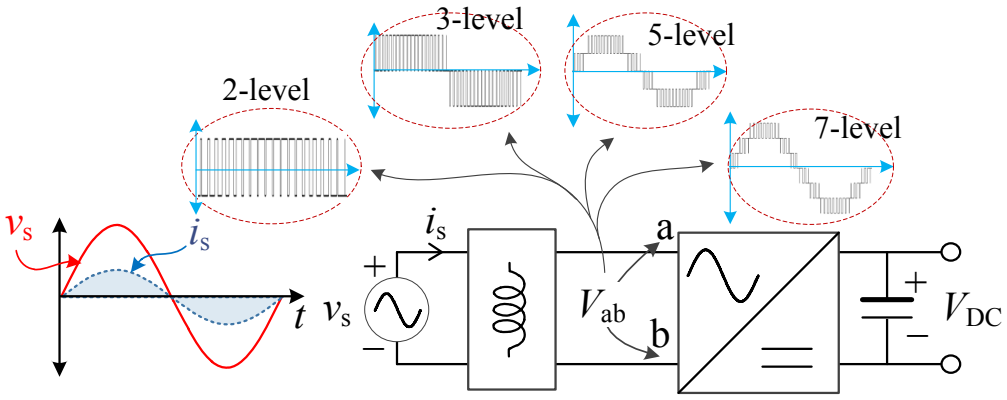


Fig. 2.5: *Possibility of multilevel voltage at the terminal of* V_{ab}

A categorization of multilevel PFC rectifier topologies based on a few important parameter is shown in Table 2.1.

Ones again, based on the output DC voltage, multilevel rectifiers are classified into three categories: buck, boost and buck-boost PFC rectifiers.

2.3.1 Multilevel boost PFC rectifier topologies

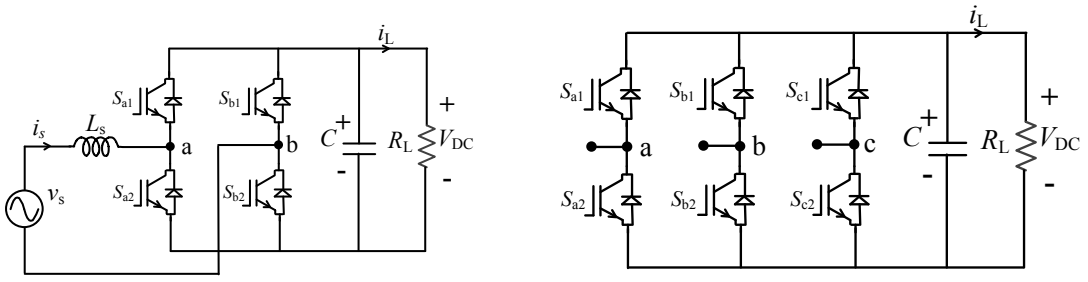
The conventional single and three-phase MLRs (viz. H-bridge, T-type, NPC and FCs) operate as boost-rectifiers [34, 36–38, 88], though some novel MLRs operate as boost rectifiers, as discussed below.

Table 2.1. *Categorization of multilevel PFC rectifier topologies*

	Parameters	**Categorization**	**Examples of topologies**
MLRs	Number of phases	Single-phase	[34, 37, 38, 42, 43, 74–77]
		Three-phase	[39, 40, 74, 77–82]
	Power flow	Unidirectional	[78, 82–87]
		Bidirectional	[42, 43, 74–77]
	Output voltage	Buck	[42, 43, 74–77]
		Boost	[41–43]
		Buck-boost	[74–77]
	Number of outputs	Single only	[34, 37, 38]
		Multiple only	[41–43]
		Single or Multiple	[74–77]
	Voltage balancing	Sensor based balancing	[41–43]
		Self-balancing	[74–77]

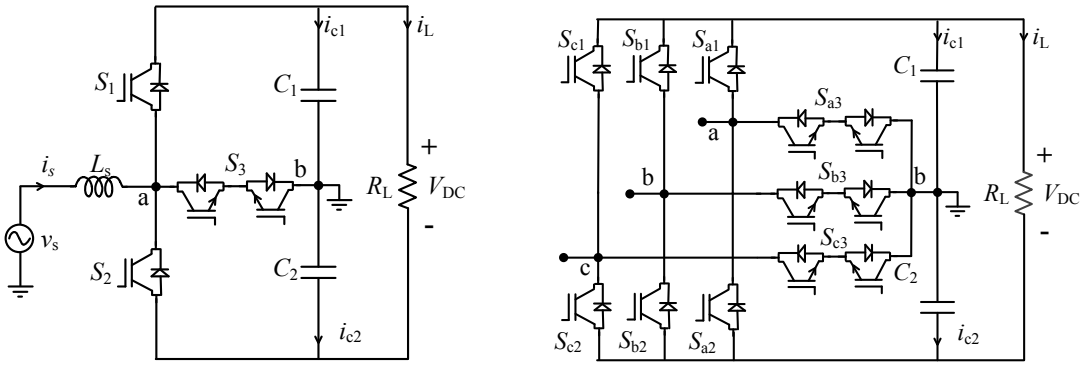
Three-level H-bridge: The HB rectifier generates three levels at the terminals 'a' and 'b', resulting in a voltage V_{ab} consisting the levels $+V_{DC}$, 0, and $-V_{DC}$ [34], where V_{DC} is the regulated output DC voltage. In HB rectifier, the modulation index M is defined as $M = \frac{v_s^{max}}{\beta V_{DC}}$ where β is '1' and v_s^{max} is the peak grid voltage in this topology. In the modulation range ($0.5<M<1$) this topology functions as a boost PFC rectifier. Moreover, it can be easily extended to a three-phase version [35], as demonstrated in the accompanying Fig. 2.6.

Three-level T-type topology: The T-type rectifier produces three distinct voltage levels at the 'a' and 'b' terminals, resulting in a voltage V_{ab} of $+\frac{V_{DC}}{2}$, 0, and $-\frac{V_{DC}}{2}$, where V_{DC} is the regulated output DC voltage [36]. In T-type rectifier, the modulation index M is defined as $M = \frac{v_s^{max}}{\beta V_{DC}}$ where β is '0.5' in this topology. As compaiered to the H-bridge topology, under the same modulation range of ($0.5<M<1$), this topology functions effectively as a high DC boost PFC rectifier and can be conveniently adapted to a three-phase version [35], as shown in the Fig.2.7.



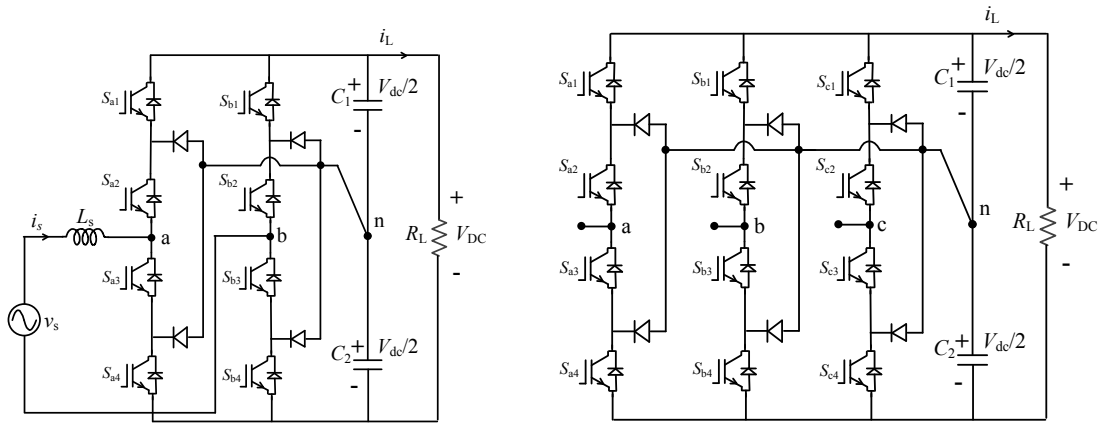
(a) Single-phase H-bridge rectifier **(b)** Three-phase H-bridge rectifier

Fig. 2.6: *Three level H-bridge boost PFC rectifier topology*



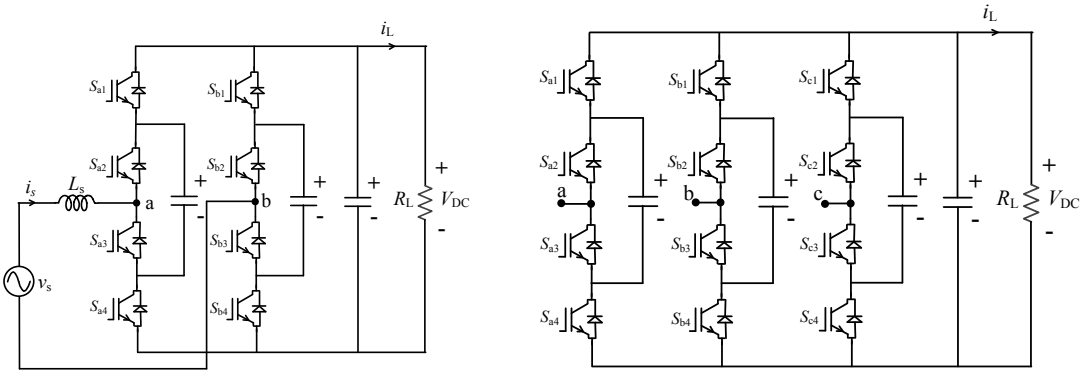
(a) Single-phase T-type rectifier **(b)** Three-phase T-bridge rectifier

Fig. 2.7: *Three level T-Type boost PFC rectifier topology*



(a) Single-phase NPC rectifier **(b)** Three-phase NPC rectifier

Fig. 2.8: *Five level neutral point clamped boost PFC rectifier topology*



(a) Single-phase FC-based rectifier **(b)** Three-phase FC based rectifier

Fig. 2.9: *Five level flying capacitor boost PFC rectifier topology*

Five-level NPC topology: The NPC rectifier produces five distinct voltage levels at the 'a' and 'b' terminals, resulting in a V_{ab} voltage that can be $+V_{DC}$, $+\frac{V_{DC}}{2}$, 0, $-\frac{V_{DC}}{2}$ and $-V_{DC}$, where V_{DC} is the regulated output DC voltage [38]. In NPC rectifier, the modulation index M is defined as $M = \frac{v_s^{max}}{\beta V_{DC}}$ where β is '1' in this topology. Under the modulation range ($0.5<M<1$) this topology functions effectively as a boost PFC rectifier and can be conveniently adapted to a three-phase version [39], as shown in the Fig.2.8.

Five-level FC topology: The FC based rectifier generates five voltage levels at the terminals of 'a' and 'b', voltage levels V_{ab} can be $+V_{DC}$, $+\frac{V_{DC}}{2}$, 0, $-\frac{V_{DC}}{2}$ and $-V_{DC}$, where V_{DC} is the regulated output DC voltage [37]. In FC rectifier, the modulation index M is defined as $M = \frac{v_s^{max}}{\beta V_{DC}}$ where β is '1' in this topology. Under the modulation range ($0.5<M<1$) this topology operates as a boost PFC rectifier and can be conveniently adapted to a three-phase version [40], as shown in the Fig.2.9.

2.3.2 Multilevel buck PFC rectifier topologies

Very limited literature is available on multilevel buck rectifiers [41–43]. These topologies proposed in [41–43] single-phase, Continuous Conduction Mode (CCM) and generate a multilevel voltage waveform at the input terminals. Due to CCM operation, commonly used AC-side capacitive and DC-side inductive filters are removed. The buck rectifier proposed in [41] is based on the CHB topology and provides multiple DC outputs as shown in Fig. 2.10. In

this topology each output terminals regulated for V_{DC} and generates voltage levels at the terminal of 'a' and 'b', voltage levels V_{ab} can be $+2V_{DC}$, $+V_{DC}$, 0, $-V_{DC}$ and $-2V_{DC}$. In [41], the modulation index M is defined as $M = \frac{v_s^{max}}{\beta V_{DC}}$ where β is '2' in this topology. For the CHB structure, on the AC side, each module must interact with the others to obtain an almost sinusoidal current in phase with the grid voltage [89]. On the DC side, each capacitor's voltage must be stable and controlled. Balancing the capacitor output voltage requires multiple voltage sensors and a complex control strategy. In [42], a five-level buck rectifier has been presented which is bidirectional in nature.

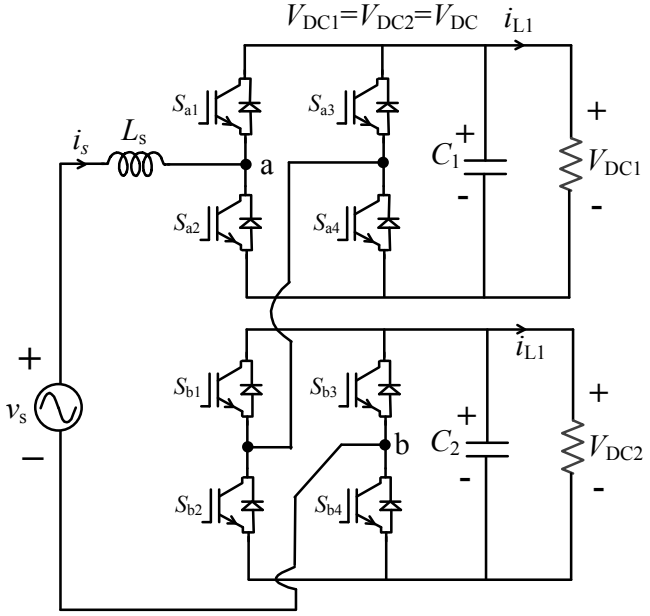


Fig. 2.10: *Five level cascaded H-bridge buck PFC rectifier*

Topological representation of [42] shown in Fig. 2.11. In [42], the modulation index M is defined as $M = \frac{v_s^{max}}{\beta V_{DC}}$ where β is '2' in this topology. In this topology each output terminals regulated for V_{DC} and generates voltage levels at the terminal of 'a' and 'b', voltage levels V_{ab} can be $+2V_{DC}$, $+V_{DC}$, 0, $-V_{DC}$ and $-2V_{DC}$.

In order to balance the voltages of the two capacitors, two DC voltage sensors are needed to implement a complex control methodology. Balancing of these voltages depend upon the switching states. Moreover, it requires power switches of high voltage ratings equal to twice the output DC voltage. In addition, the topology in [42] cannot be directly extended to its three-phase version.

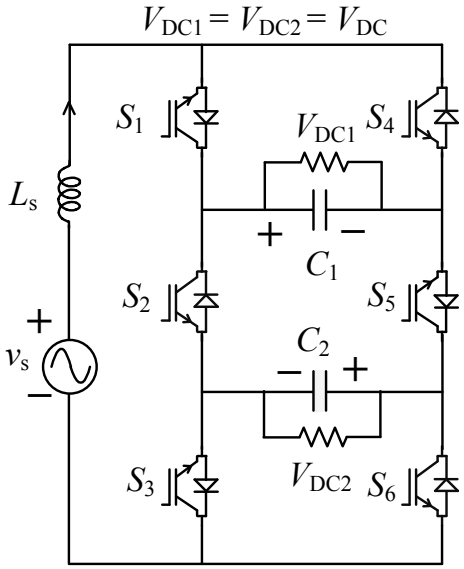


Fig. 2.11: *Five level buck PFC rectifier proposed in [42]*

Another buck topology proposed in [43] is a nine-level converter, which is primarily based on the original inverter topology described in [90]. The voltage balancing of capacitors and control methodology is challenging in [43]. Voltage levels at the terminal of 'a' and 'b', voltage levels V_{ab} can be $+2V_{DC}$, $+3\frac{V_{DC}}{2}$, $+V_{DC}$, $+\frac{V_{DC}}{2}$, 0, $-\frac{V_{DC}}{2}$, $-V_{DC}$, $-3\frac{V_{DC}}{2}$ and $-2V_{DC}$. In [43], the modulation index M is defined as $M = \frac{v_s^{max}}{\beta V_{DC}}$ where β is '2' in this topology. In [43], the authors use Finite Switching Set Mode Predictive Control to regulate the DC voltages and to track the desired reference of the input AC current. This requires four voltage sensors and four current sensors to balance the capacitor voltage and improve the PFC. Another drawback of the topology in [43] is the requirement of high voltage rated power switches and difficulty in extension to three-phase version. Hence both these rectifiers of [42] and [43] are characterized by three important limitations: voltage ratings of the switches are different and higher, balancing of voltages is extremely complex (involving multiple sensors and cumbersome real-time computation) and three-phase extensions are not possible directly. This topology functions as a buck PFC rectifier and is challenging to implement in a three-phase configuration due to its complexity.

2.3.3 Multilevel buck-boost PFC rectifier topologies

A buck-boost PFC rectifier can perform both step-up (boost) and step-down (buck) voltage conversions, making it a versatile power converter that can achieve a wide range of output

voltage levels. This makes it well-suited for applications such as electric vehicle charging, where a variety of voltage levels may be required. To achieve these objectives, the features of the so-called 'switched capacitor-based multilevel topologies'[44, 91, 92], which have been proposed as inverters thus far [46], are examined. These topologies use SCs to synthesize additional voltage levels at the output of the inverter, while at the same time, they enable an inherent voltage gain (β) greater than one, and thereby achieving a 'boost' operation as inverter. This is so because a SC is charged by bringing it in parallel with the input DC source. Thereafter, another switching combination brings it in series with the DC source while they are connected to the AC load. Hence these topologies offer the advantages of multilevel inverters, while providing additional advantages of inherent boost and self-balanced capacitors. These topologies are capable of operating in buck mode for reversal operation as an AC-DC rectifier, while maintaining a power factor near unity. By varying the modulation index, SC-based topologies can also ensure stable operation, making them suitable for a wide output voltage range.

2.4 FEATURES COMPARISON OF MULTILEVEL RECTIFIER TOPOLOGIES

As mentioned previously, typically, the EV charging system is composed of a PFC rectifier stage and a DC-DC converter stage. As this work is focused on the PFC rectifier stage using multilevel converters, it is important to highlight the features that this power conversion stage should possess. These are summarized as Features (**F#:**) :

- **Feature F#1:** It achieves buck operation along with PFC and wide range of output voltage
- **Feature F#2:** It allows bidirectional flow of power so that both G2V and V2G modes can be implemented
- **Feature F#3:** It offers an easy extension of the power circuit for a three-phase AC input
- **Feature F#4:** It offers an easy possibility of single or multiple outputs for simultaneous EV charging
- **Feature F#5:** It offers self-balancing of capacitors' voltages

Table 2.2. *Comparison of multilevel PFC rectifier topologies based on various features*

Reference	**Work**	**F#1**	**F#2**	**F#3**	**F#4**	**F#5**
[36]	T-type boost PFC rectifier	×	✓	✓	×	✓
[39]	Three-phase three-level ANPC rectifier	×	✓	✓	×	✓
[40]	Three-phase flying capacitor PFC rectifier	×	✓	✓	×	×
[41]	Cascaded H-bridge PFC rectifier	✓	✓	×	×	×
[42]	Bidirectional five level buck PFC rectifier	✓	✓	×	×	×
[43]	Triple output nine level buck PFC rectifier	✓	✓	×	×	×
[86]	Five-level boost PFC rectifier	×	×	✓	×	✓
Proposed	**Bidirectional seven-level wide range of rectifier**	✓	✓	×	✓	✓
Proposed	**Bidirectional five-level wide range of rectifier**	✓	✓	✓	✓	✓

The existing multilevel PFC rectifier topologies discussed so far have been compared based on these features and a summary is presented in Table. 2.2. In addition, the table also includes two novel topologies which are proposed in this work (described in the upcoming chapters). It can be seen that the existing multilevel PFC rectifiers (barring the topologies proposed in this work) are unable to offer most of the desired features as mentioned previously, and hence there is a scope in conceptualizing novel multilevel topologies which can offer such features. This gap forms the basis of the work carried out in this research. The identified research areas and contributions are discussed in the next sections.

2.5 IDENTIFIED RESEARCH AREAS

This chapter presents a brief review of PFC converter topologies for EV battery charging. It is noted that most of the research on multilevel PFC rectifiers focuses on the single output boost mode of operation, and is designed for either single-phase or three-phase power supply. As EV technology continues to evolve, we can expect to see even more innovation and variation in battery voltages, charging infrastructure, and other components, which will shape the future of electric mobility. Given the different aspects of power converters, the scope of this work is identified as the development of a single and three-phase multilevel PFC rectifier with a wide output voltage range for EV charging, taking the following considerations into account:

- A multilevel PFC rectifier is classified by the number of levels in the input side voltage waveform. Compared to non-multilevel rectifiers, MLRs offer several advantages such as lower voltage ratings for power switches, a much better harmonic profile of the input waveform, reduced dv/dt stress, and the possibility of fault-tolerant operation. Therefore, the scope is identified to investigate the multilevel PFC rectifier.

- The battery voltages in various types of EVs show significant variations, but the range depends on the specific vehicle and battery technology. Conventional topologies can achieve PFC rectification in boost modes only. Therefore, the scope is identified to investigate the buck PFC rectifier that can provide a wide output range.

- Existing buck PFC rectifiers require multiple capacitors for voltage regulation. Balancing these capacitors necessitates the use of multiple sensors, which adds to the complexity of controller in signal processing. Therefore, the scope is identified to develop a voltage balancing technique that can reduce the sensor requirements and the controller complexity.

- Semi-controlled multilevel topologies are applicable for boost PFC rectifiers and achieve unidirectional power flow. However, for V2G applications of EVs, a bidirectional converter is required. Therefore, the scope is identified to investigate a V2G-enabled multilevel PFC rectifier.

- Modular AC-DC conversion is preferred because of its scalability and ability to augment configurations for higher voltage and current ratings. Furthermore, it enables easy extension

to three-phase applications. Thus, the scope is identified to implement a modular topology for easy extension to three-phase systems.

- A multi-output PFC rectifier is useful for simultaneous EV charging applications. However, in existing multi-output topologies, output voltage balancing can be achieved only with the same load value. Therefore, the scope is identified to develop a multi-output rectifier topology that can operate in both single and multiple output modes and possibly result in load voltage balancing with multiple loads of different values.

2.6 RESEARCH CONTRIBUTIONS

The research contributions in the above-identified research areas are briefed herewith:

- Conceptualization, study and validation of a grid connected SC-based multilevel structure
- Development, analysis, and verification of a bidirectional five-level PFC rectifier for EV charging with wide output voltage range for single-and three-phase power supply
- Developing, analyzing, controlling, and verifying a V2G enabled seven-level buck PFC rectifier for on-board and off-board EV charging interface
- Conceptualization, analysis, controlling and validation of a single/multiple output multilevel buck PFC rectifier for simultaneous EV charging

I. Conceptualization, study and validation of a grid connected SC-based multilevel structure

The conventional multilevel topologies operate as inverters with a unity voltage gain, which limits their output voltage range during AC-to-DC conversion and causes them to function as boost rectifiers. These limitations are further exacerbated by difficulties in voltage balancing of capacitors and extension to three-phase systems. Therefore, this study investigates Switched Capacitors based Multilevel Inverter (SCMLI) that have been proposed mainly as inverters, in a standalone mode without connection to the grid. SCMLIs inherently offer boost and sensor-less self-balancing of capacitors. The research question

posed is whether SCMLIs can perform PFC rectification while maintaining wide output range and capacitor voltage self-balancing. To answer this question, a novel grid-connected 13-level switched-capacitors' based inverter is introduced, utilizing 12 power switches, 2 diodes, and 3 self-balanced capacitors. This topology provides a voltage gain (β=6) and ensures self-balancing of capacitors at all modulation index values. The experimental validation confirms that the presented topology is highly modular and cost-effective compared to other similar SCMLIs. This study of a grid-connected SCMLI paves the way for the examination of the reverse role to enable rectifier operation.

The experimental examination is carried out to validate the proposed 13-level inverter's topology and control system. Because it has a voltage boost factor of six, the input side DC voltage (V_{DC}) is set to 60 V to connect to a 230 VRMS, 50Hz single-phase grid. The proposed SCs-based topology generates 13 levels and offers a boosting factor of 6, while exhibiting a good response under dynamic conditions. With the use of a single DC source, this topology is capable of generating higher number of levels, yield high boosting gain, while uses a reduced number of switches. It enables single-state power conversion from low-voltage DC to high-voltage AC with an optimal number of active power switches. Moreover, when the power draw is from the grid at the DC side, this SCs-based inverter can operate as a buck rectifier. The variation of modulation index justifies the wide range of AC voltage with different gains that can be achieved through this topology. This variation of modulation index also enables a wide range of output DC voltage in the SCs-based rectifier topology.

II. The development, analysis, and verification of a bidirectional five-level PFC rectifier for electric vehicle charging with wide output voltage range

This study presents a SC-based rectifier topology that works as a buck rectifier with PFC and provides a wide output range. It synthesizes five levels at the input side, which greatly improves the harmonic profile of the waveform. One of the switched capacitors is in parallel with the load terminal for all the switching states, eliminating the need for additional filter capacitors at the DC output. Additionally, the capacitors are self-balanced and only one of them needs to be sensed for closed-loop control. The topology's five-level operation with continuous conduction eliminates the capacitive filter on the AC-side and inductive filter on the DC-side. The topology has several features, including buck operation

with a wide output regulation, bidirectional power flow needed for V2G systems, and easy three-phase realization by simply adding one more leg. While this topology establishes the proposed theory of role reversal in switched capacitors based multilevel topologies, it synthesizes only five levels with a β of 2. Experimental results validate the topology's performance and its suitability for EV charging applications.

This proposed SC-based rectifier generates five-level at the input terminal and the value of voltage gain β is resulted as 2. The proposed rectifier topology having two legs 'A' and 'B' . The AC input voltage is given at the input terminals (V_{ab}), while the DC output voltage is obtained between the output terminals. The output voltage is shown as 'V_{DC}'. Each leg has five active switches and one capacitor, which is maintained at a voltage equal to V_{DC}. The pole voltages have three voltage levels: $+2V_{DC}$, $+V_{DC}$ and 0 and the line voltage V_{ab} manifests five levels viz. $\pm 2V_{DC}$, $\pm V_{DC}$ and 0. Due to phase modular structure of the proposed topology, it can be easily extended to its three-phase version. This is achieved by adding a third leg which too carries a switched capacitor and five power switches. This three-phase operation is also applicable for bidirectional, buck, and wide modes of operation. It acts as a boost rectifier for low modulation index (<0.5), synthesizing only three levels at the input terminals.

III. Developing, analyzing, controlling, and verifying a V2G enabled seven-level buck PFC rectifier for on-board and off-board electric vehicle charging interface

The grid-connected voltage source rectifier produces a multilevel voltage at the input terminal to regulate the flow of current in the grid. Increasing the number of voltage levels enhances the quality of the synthesized voltage, leading to an improvement in grid current. Additionally, MLRs provide alluring benefits, such as utilizing power switches of reduced voltage ratings, yielding significantly improved harmonic profile of the input waveform, resulting lower dv/dt stress, and the possibility of fault-tolerant operation. These benefits make MLRs a highly attractive option for those seeking to optimize the performance of their power system. As the β factor increases, it improves the range of output voltage in a buck mode with a better harmonic profile. Moreover, the number of levels increases with this factor.

This study proposes a seven-level PFC rectifier topology that greatly improves the waveform's harmonic profile with a low number of power devices. It works as a buck

PFC rectifier with a β value of 3 and provides a wide output range in buck and boost mode. The capacitors are self-balanced, eliminating the need for additional balancing circuitry, and only one of the switched capacitors' voltage is required for closed-loop control. The topology allows bidirectional power flow and can be used for V2G interface in EV charging. Furthermore, a three-phase seven-level topology is specified for both buck and boost modes, providing four levels of pole voltage and seven levels of line voltage at the input terminal of the rectifier.

IV. Conceptualization, analysis, controlling and validation of a Single/Multiple Output Multilevel Buck PFC Rectifier for simultaneous electric vehicle charging

The multi-output PFC rectifier is useful for simultaneous EV charging applications. This is possible with existing cascaded H-bridge or multi-source inverter topologies. However, in these topologies, the controller complexity required to stabilize the capacitor voltage is greatly increased. Another main drawback of these multi-output topologies is that regulation can only be achieved with the same load value. For different load values, the output voltage becomes unbalanced. As a result, these topologies cannot operate satisfactorily with different loads and a single output. It is practically uncommon for EV charging to have the same load of battery charge at every output terminal. Given these limitations of the existing MLRs for buck rectification, this work proposes a novel SCs based self-balancing buck PFC MLRs with a wide output voltage range. The proposed rectifier can operate with different loads at the output terminals and also operate in both single and multiple output modes. Moreover, load voltage balancing is feasible even when the multiple loads have different values. To validate the operation with single-/multiple-output load variations, further experimental tests are performed. The load voltage stabilizes at reference DC voltage. Even though grid current is raised accordingly and the rectifier remains in UPF mode. To demonstrate applicability in single-phase EV charging with a single output, a power electronics interface consisting of the proposed PFC rectifier and a typical buck-boost DC-to-DC converter is built.

This study proposes five level topologies that enable multi-output operation in single-phase mode. These topologies work as buck PFC rectifiers with $\beta = 2$ and provide a wide output range in both buck and boost modes. Additionally, the capacitors in these topologies are self-balanced, eliminating the need for any additional balancing circuitry, and the

voltage of only one switched capacitor is required for closed-loop control. Furthermore, the capacitors can be balanced even with multiple loads of different values or types. Finally, the voltage stress across the switches in these topologies is equal to the DC output voltage.

Chapter–3

Grid Connected Switched Capacitors Based Multilevel Structure

It was discussed previously that conventional MLRs pose two principal challenges for their application as PFC rectifier in EV charging systems: (a) they are inherently boost-type rectifiers and hence do not offer a wide range of output dc voltage; and (b) the voltage balancing of capacitors require additional sensors and complex control methodologies. A recent class of multilevel inverters has attracted lot of attention because their capacitors are self-balanced. These topologies use the principle of switched capacitors to attain self-balancing, and at the same time they offer inherent voltage gain. Most of them, however, have not been investigated in grid-connected mode. Hence, the approach adopted in this work is to investigate one of such topologies for their operation as rectifier (and thus grid-connection becomes essential), through a question: while performing reverse conversion (i.e. AC-to-DC instead of DC-to-AC) can they offer buck rectification while preserving the self-balancing of capacitors' voltages? Therefore, in this chapter, a newly proposed switched capacitors based MLI is first studied as a grid-connected inverter and thereafter, it has been established theoretically that, such topologies would indeed perform buck rectification.

3.1 GENERAL

To achieve a buck and wide output voltage from a rectifier, it is possible to use inverter topologies with boosting features. For the purpose, it is necessary to use topologies based on SC or cascaded multi-sources. The problem of capacitor voltage balancing is resulted with the operation of cascaded multilevel inverter as a rectifier. The main advantage of SCMLIs is self-voltage balancing of the capacitors. This balancing is resulted due to the capacitors being in parallel

with source during charging and in series with a source during discharging. Existing SC based inverter topologies have been mainly proposed as inverters, in standalone mode of operation (i.e. without being connected to the grid) [44, 46, 91–100]. The structure of MLI-based grid integrated system is shown in Fig.3.1, with low voltage renewable sources in the input side.

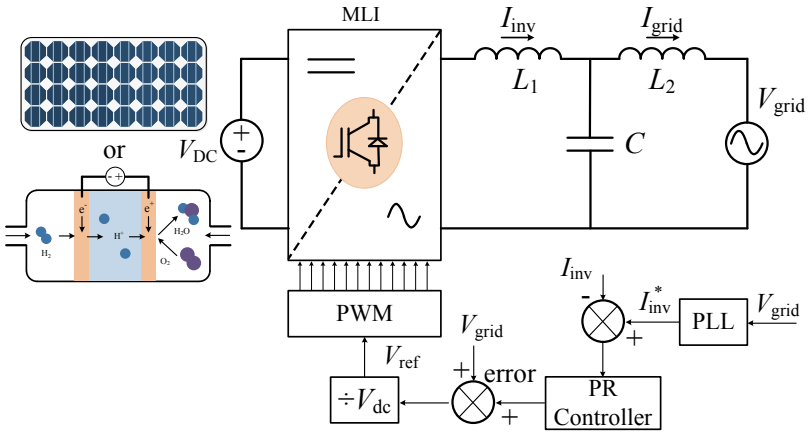


Fig. 3.1: *Schematic of grid connected boost converter*

This chapter describes a novel single-phase grid-connected, 13-level inverter to yield an inherent voltage boost and a wide range of grid output voltage. The adapted modulation technique is robust to keep the capacitors self-balanced for all values of the modulation index. The presented topology is validated experimentally with satisfactory operation in yielding input voltage boost by a factor of six. The proposed topology is modular and cost-effective in comparison to other similar typologies due to reduced device count.

The proposed SCMLI is characterized by the following merits:

- Realized with only 12 switches and 2 diodes.
- Requires only three SCs that are inherently balanced and does not require any sensors or complex control mechanism.
- Simplified Level-Shifted Pulse-Width Modulation (LSPWM) control logic (i.e., complementary switching pair designed to generate pulses)

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- Topology can be extended to yield higher voltage gain, as well as a higher number of levels in output voltage.
- Generates a high number of levels with a reduced number of switches and sources.
- Requires reduced filter size due to the better harmonic profile of output AC voltage.
- Single state power conversion from low-voltage DC to high-voltage AC with an optimal number of active and passive components.
- Ability to work as a grid-connected inverter while resulting in good dynamic response.
- Low Cost Function (CF) due to the reduced count of devices.

3.2 PROPOSED TOPOLOGY OF 13-LEVEL INVERTER

A single-stage circuit synthesizes thirteen levels with a single input source having an overall voltage gain of six. The circuit description and various switching states are discussed in this section.

3.2.1 Power circuit

The proposed thirteen-level inverter is shown in Fig. 3.2. It utilizes twelve power switches, three capacitors (C_1, C_2, C_3) and one DC source (V_{DC}). The levelled output voltage is marked as V_{ab}. The voltages V_{C1} and V_{C2} are maintained at V_{DC}, while voltage V_{C3} is maintained at $3V_{DC}$. The proposed MLI is capable of generating 13 different output levels of 0, $\pm V_{DC}$, $\pm 2V_{DC}$, $\pm 3V_{DC}$, $\pm 4V_{DC}$, $\pm 5V_{DC}$ and $\pm 6V_{DC}$.

3.2.2 Description of the voltage levels

The valid operating states v_i (i=1 to 14) for the proposed inverter are summarized in Table 3.1. The states of capacitors are represented as 'C' for charging 'D' for discharging and '-' for neutral.

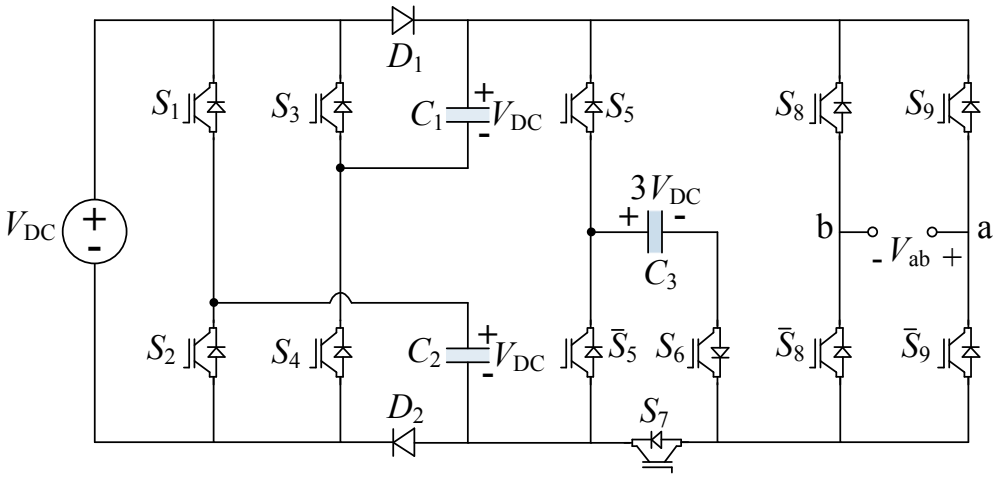


Fig. 3.2: *Proposed SC based 13-level inverter*

Table 3.1. *Switch and capacitor states ('C' for charging 'D' for discharging) for the proposed 13-level inverter*

State	V_{ab}	Switches	Capacitors		
			C_1	C_2	C_3
v_1	0	$S_2, S_3, S_5, S_6, S_7, \overline{S_8}, \overline{S_9}$	D	D	C
v_2	$+V_{DC}$	$S_4, \overline{S_5}, S_7, \overline{S_8}, S_9$	C	-	-
v_3	$+2V_{DC}$	$S_2, S_4, \overline{S_5}, S_7, \overline{S_8}, S_9$	C	D	-
v_4	$+3V_{DC}$	$S_2, S_3, \overline{S_5}, S_7, \overline{S_8}, S_9$	D	D	-
v_5	$+4V_{DC}$	$S_1, \overline{S_5}, S_6, \overline{S_8}, S_9$	-	C	D
v_6	$+5V_{DC}$	$S_2, S_4, \overline{S_5}, S_6, \overline{S_8}, S_9$	C	D	D
v_7	$+6V_{DC}$	$S_2, S_3, \overline{S_5}, S_6, \overline{S_8}, S_9$	D	D	D
v_8	0	$S_2, S_3, S_5, S_6, S_7, S_8, S_9$	D	D	C
v_9	$-V_{DC}$	$S_4, \overline{S_5}, S_7, S_8, \overline{S_9}$	C	-	-
v_{10}	$-2V_{DC}$	$S_1, S_3, \overline{S_5}, S_7, S_8, \overline{S_9}$	D	C	-
v_{11}	$-3V_{DC}$	$S_2, S_3, \overline{S_5}, S_7, S_8, \overline{S_9}$	D	D	-
v_{12}	$-4V_{DC}$	$S_1, \overline{S_5}, S_8, \overline{S_9}$	-	C	D
v_{13}	$-5V_{DC}$	$S_1, S_3, \overline{S_5}, S_6, S_8, \overline{S_9}$	D	C	D
v_{14}	$-6V_{DC}$	$S_2, S_3, \overline{S_5}, S_6, S_8, \overline{S_9}$	D	D	D

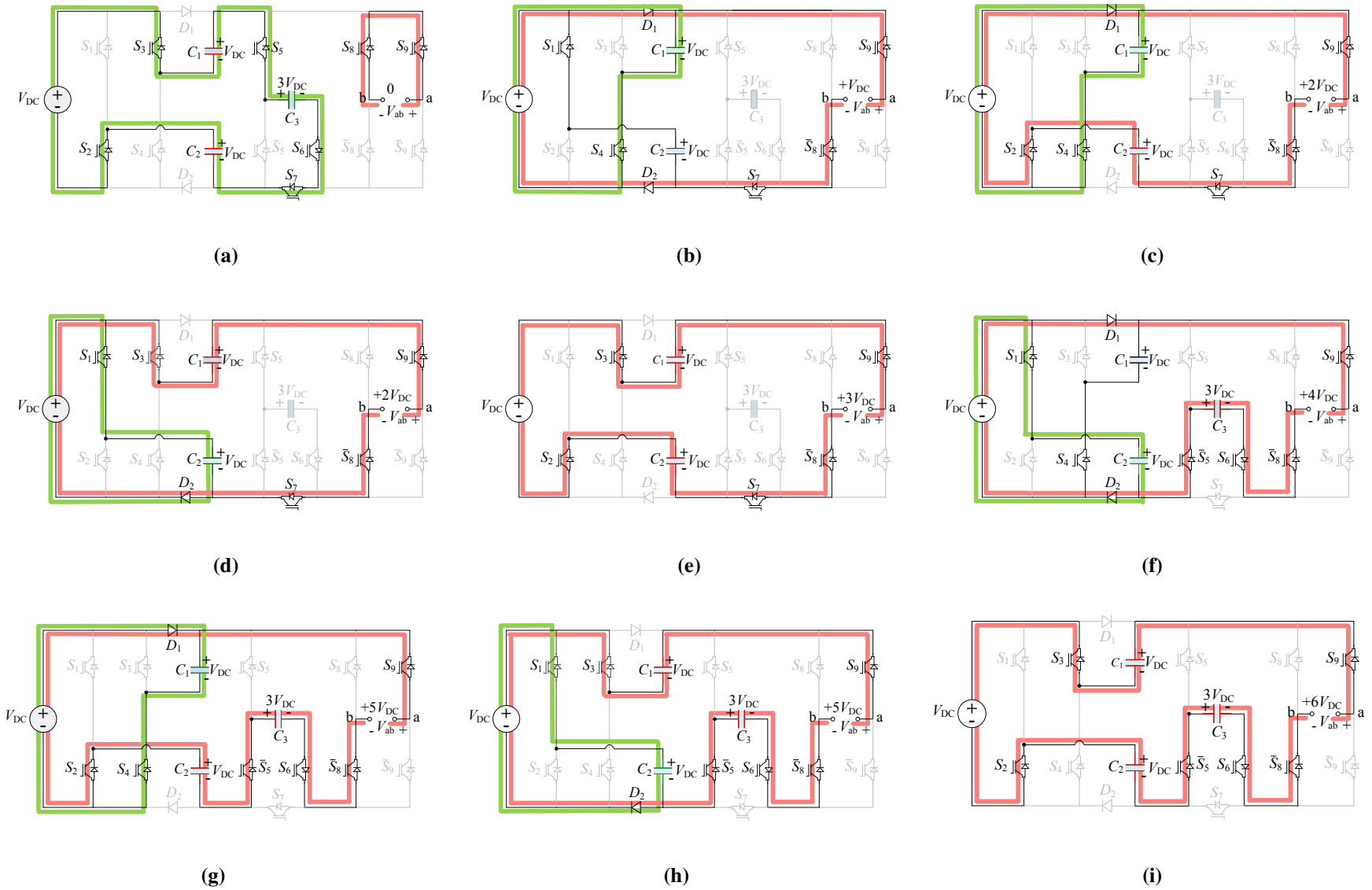


Fig. 3.3: *The states for different voltage levels of the proposed 13-L inverter*

- $\boldsymbol{V_{ab}}$**=0**: It defines states ν_1 and ν_8. Turning ON S_2 and S_3, connects both C_1 and C_2 in series with the DC source. As shown in Fig. 3.3a, the zero-output level is generated by turning ON S_8 and S_9 (or $\overline{S_8}$ and $\overline{S_9}$). The C_3 gets charged by the $3V_{DC}$ through C_1, C_2 and battery by turning on S_5,S_6 and S_7.

- $\boldsymbol{V_{ab}}$**=**$\pm\boldsymbol{V_{DC}}$: For $+V_{DC}$, $\overline{S_8}$ and S_9 are turned ON, while for $-V_{DC}$, S_8 and $\overline{S_9}$ are turned ON. The C_1 charged in both states by S_4 as shown in Fig. 3.3b. This operation defines states ν_2 and ν_9.

- $\boldsymbol{V_{ab}}$**=**$\pm\boldsymbol{2V_{DC}}$: It defines states ν_3 and ν_{10} that are shown in Fig. 3.3c and Fig. 3.3d respectively. The level $+2V_{DC}$, Fig. 3.3c, is achieved by turning on S_7, $\overline{S_8}$, S_9 and the level $-2V_{DC}$, Fig. 3.3d, is achieved by turning on S_7, S_8, $\overline{S_9}$. By turning ON S_2 and S_4, the C_1 appears across DC source, while C_2 comes in series with DC source. Similarly, by turning ON S_1, S_3, C_1 comes in series while C_2 comes in parallel with DC source.

- $\boldsymbol{V_{ab}}$**=**$\pm\boldsymbol{3V_{DC}}$: It defines states ν_4 and ν_{11} as shown in Fig. 3.3e. By turning ON S_2 and S_3; C_1 and C_2 appear in series with DC source. The level $+3V_{DC}$ is achieved by turning on $\overline{S_8}$, S_9 while level $-3V_{DC}$ is achieved by turning on S_8, $\overline{S_9}$.

- $\boldsymbol{V_{ab}}$**=**$\pm\boldsymbol{4V_{DC}}$:It defines states of ν_5 and ν_{12}. By turning ON S_1, C_2 appear across DC source and thus C_2 got charged. The C_3 comes in series with DC source by turning ON switches $\overline{S_5}$,S_6 as shown in Fig. 3.3f. The level $+4V_{DC}$ is achieved by turning on $\overline{S_8}$, S_9 while the level $-4V_{DC}$ is achieved by turning on S_8, $\overline{S_9}$.

- $\boldsymbol{V_{ab}}$**=**$\pm\boldsymbol{5V_{DC}}$:It defines states ν_6 and ν_{13} as shown in Fig. 3.3g and Fig. 3.3h respectively. By turning ON S_2 and S_4, C_1 appears in parallel while C_2 appears in series with DC source. Similarly, by turning on S_1 and S_3, C_1 appears in series while C_2 appears in parallel with DC source. The C_3 comes in series with DC source by turning ON switches $\overline{S_5}$, S_6. The level $+5V_{DC}$ is achieved by turning on $\overline{S_8}$, S_9 and the level $-5V_{DC}$ is achieved by turning on S_8, $\overline{S_9}$.

- $\boldsymbol{V_{ab}}$**=**$\pm\boldsymbol{6V_{DC}}$: It defines states ν_7 and ν_{14} shown in Fig. 3.3i. By turning ON S_2 and S_3, C_1 and C_2 appear in series with DC source and thus got discharged. The C_3 appears in series with DC source by turning ON switches $\overline{S_5}$, S_6. The level $+6V_{DC}$ is achieved by turning on $\overline{S_8}$, S_9 and the level $-6V_{DC}$ is achieved by turning on S_8, $\overline{S_9}$.

3.3 MODULATION STRATEGY

There are different techniques for modulation of MLIs. Which include high-switching-frequency techniques such as multicarrier Pulse-Width Modulation (PWM) and space vector PWM [52] and low switching- frequency techniques such as active harmonic elimination, selective harmonic elimination, and nearest level control [101], [102], [103]. The proposed SCMLI can be modulated with these techniques with appropriate adaptation. In the proposed work, a simple LSPWM scheme, as shown in Fig. 3.4, is employed for the gating signal generation. A reference waveform (V_{ref}) of amplitude (v_{ref}) and frequency (f_{ref}) is generated by voltage controller. Its absolute value $|V_{\text{ref}}|$ is compared with the six-level shifted high-frequency triangular waveforms V_{cr1} to V_{cr6} of same frequency and phase. The modulation index (M) can thereby be defined as:

$$M = \frac{v_{\text{ref}}}{6v_{\text{cr}}} \tag{3.1}$$

Where v_{cr} and v_{ref} are the amplitudes of the carrier and reference waveform respectively.

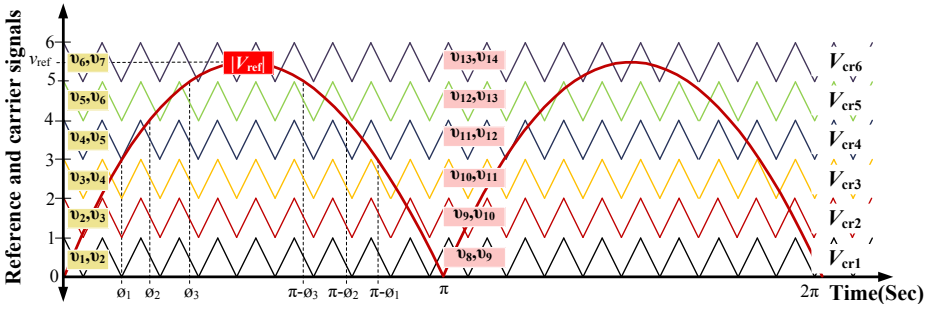


Fig. 3.4: *Modulation scheme for the proposed inverter*

In the level-shifted PWM scheme, N_L-1 carrier signals are required for N_L number of levels. However, in the proposed logic gate-based PWM scheme, the number of carrier signals reduces by half, i.e., (N_L-1)/2 carrier signals are required. In this scheme, the process involves first taking the absolute value of the reference signal and comparing it with the carrier signal. The reference signal is also compared with 0. For positive states, stages from (v_1 to v_7) are considered, and for negative states, stages from (v_8 to v_{14}) are taken into account. Each carrier signal is associated with 4 states, as depicted in the Fig. 3.4. To create this combination, NOT and AND gate operations are employed. All states are responsible for controlling every switch.

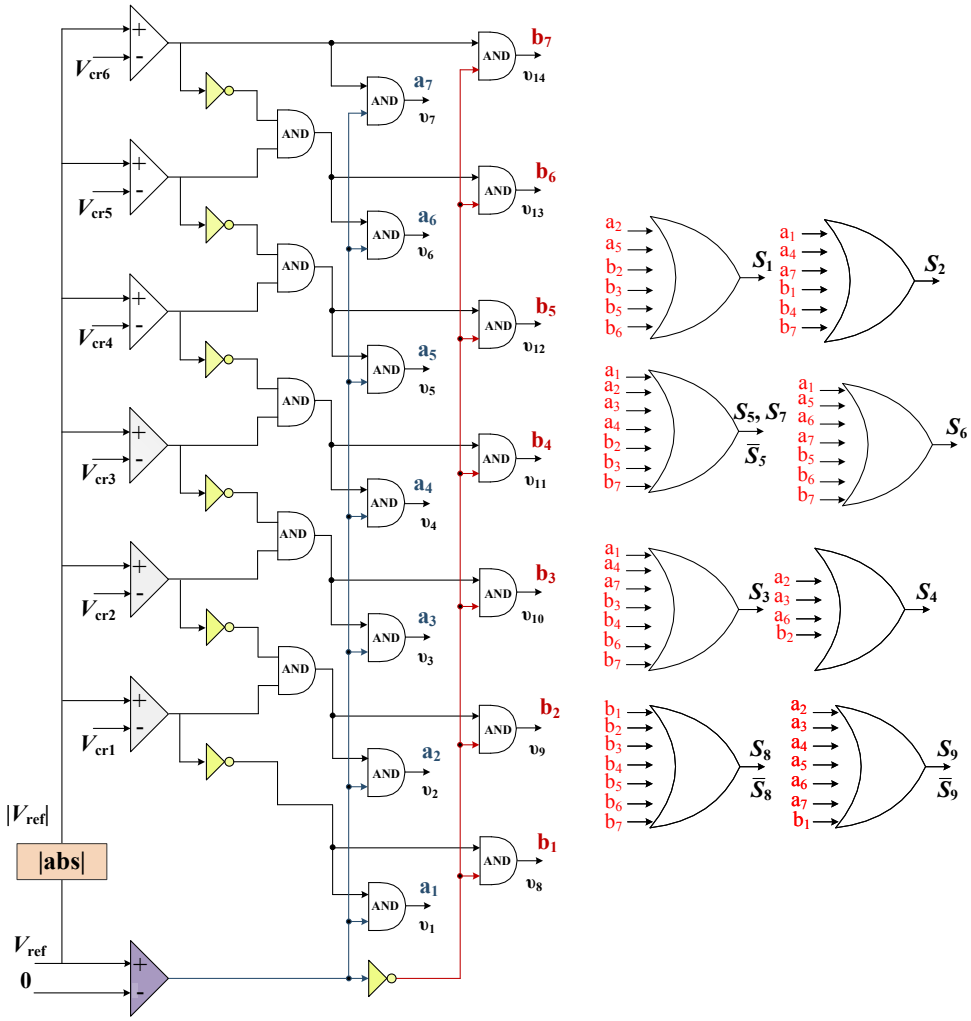


Fig. 3.5: *Logic-gates based generation of switching states*

By implementing an OR operation with these combinations, gate pulses are generated across them, as shown in the Fig. 3.5.

During $0 \leq \omega t \leq \pi$, when V_{cr1} is compared with $|V_{ref}|$, the output voltage levels are (0 and V_{DC}) which are to be obtained by generating signals for states (ν_1 and ν_2). Similarly, when V_{cr2}, V_{cr3}, V_{cr4}, V_{cr5} and V_{cr6} are compared with $|V_{ref}|$, the output voltage levels are (V_{DC}, $2V_{DC}$), ($2V_{DC}$, $3V_{DC}$), ($3V_{DC}$, $4V_{DC}$), ($4V_{DC}$, $5V_{DC}$) and ($5V_{DC}$, $6V_{DC}$) which are to be obtained by generating signals for states (ν_2, ν_3), (ν_3 , ν_4), (ν_4 , ν_5), (ν_5 , ν_6) and (ν_6 , ν_7) respectively.

For the remaining half cycle during $\pi \leq \omega t \leq 2\pi$, the state for the negative half cycle is to be generated and the zero level is to be obtained by the state ν_8. When V_{cr1}, V_{cr2}, V_{cr3}, V_{cr4}, V_{cr5} and V_{cr6} are compared with $|V_{ref}|$, the output voltage levels are (0, $-V_{DC}$), ($-V_{DC}$,

$-2V_{DC}$), ($-2V_{DC}$, $-3V_{DC}$), ($-3V_{DC}$, $-4V_{DC}$), ($-4V_{DC}$, $-5V_{DC}$) and ($-5V_{DC}$, $-6V_{DC}$) which are to be obtained by generating signals for states (ν_8, ν_9), (ν_9 , ν_{10}), (ν_{10} , ν_{11}), (ν_{11} , ν_{12}), (ν_{12} , ν_{13}) and (ν_{13} , ν_{14}) respectively. Logic gates based switching states generation are shown in Fig. 3.5.

3.4 COMPONENTS RATINGS AND DESIGNING OF CAPACITORS

In this section, the discussion covers the ratings of power switches based on voltage and current stress, as well as the design of SCs based on voltage ripples across them.

3.4.1 Voltage and current ratings of switches

For the proposed multilevel inverter, the required Peak-Inverse-Voltage (PIV) for the power switches is summarized in Table 3.2. When expressed as percentage of the peak output voltage $6V_{DC}$, these ratings are expressed as 16.5% for four switches and two diodes (S_1, S_2, S_3, $\overline{S_4}$, D_1, D_2); 33% for switch (S_6) ; 50% for three switches (S_5, $\overline{S_5}$, S_7) and 100% for four switches (S_8, $\overline{S_8}$, S_9, $\overline{S_9}$).

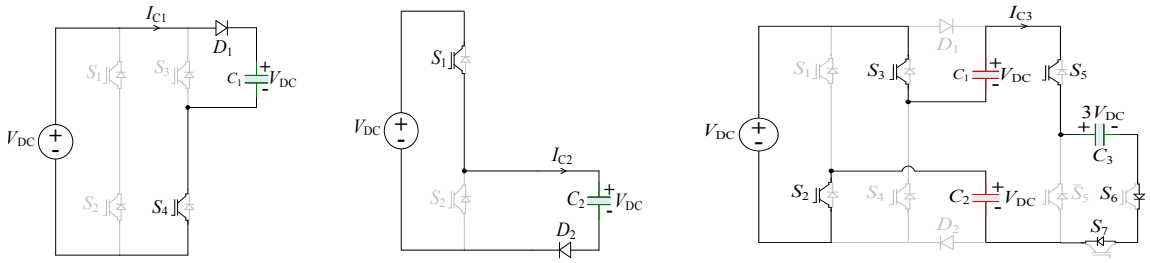
Table 3.2. *PIV across switches and diodes where V_{DC} as input and $6V_{DC}$ as peak output*

PIV	**Switches and Diodes**
V_{DC}	S_1,S_2, S_3,S_4, D_1,D_2
$2V_{DC}$	S_6
$3V_{DC}$	S_5, $\overline{S_5}$,S_7
$6V_{DC}$	S_8, $\overline{S_8}$, S_9,$\overline{S_9}$

Table 3.3, summarizes the current stress across the switches, which corresponds to peak value or amplitude of switch current. The load current i_{ac} is the minimum inverter current. It passes through the switches S_8, $\overline{S_8}$, S_9 and $\overline{S_9}$. Also, $I_{ac} + I_{C1} + I_{C2} + I_{C3}$ is the maximum current that will pass through S_2, S_3, S_5, S_6, S_7.

Table 3.3. *Current flow through the switches*

Current Stress	Switches
I_{ac}	S_8, $\overline{S_8}$, S_9, $\overline{S_9}$
$I_{ac} + I_{C1}$	S_4
$I_{ac} + I_{C2}$	S_1
$I_{ac} + I_{C1} + I_{C2} + I_{C3}$	S_2, S_3, S_5, S_6, S_7



(a) **(b)** **(c)**

Fig. 3.6: *Charging paths for (a) Capacitor C_1, (b) Capacitor C_2, (c) Capacitor C_3*

The load current (I_{ac}) depends on rated power (P), modulation index (M) and peak output voltage ($6V_{DC}$). For unity power factor injection at the grid, it is expressed as:

$$I_{ac} = \frac{\sqrt{2} \times P}{6 \times M \times V_{DC}} \tag{3.2}$$

The switch S_4 carries load current and the charging current for the capacitor C_1. Therefore, its current stress shall be dictated by ($I_{ac} + I_{C1}$). The path for I_{C1} is depicted in Fig. 3.6a, while I_{C1} is calculated as:

$$I_{C1} = \left(\frac{V_1}{R_1}\right) \times exp\left(\frac{t}{R_1 \times C_1}\right) \tag{3.3}$$

Where,

$$\begin{aligned} V_1 &= V_{DC} - V_{D1} - V_{C1} \\ R_1 &= r_{D1} + r_{S4} + R_{ESR_{C1}} \end{aligned} \tag{3.4}$$

Where, $R_{ESR_{C1}}$ is the equivalent series resistance of capacitor C_1. Similarly, current stress on switch S_1 is dictated by ($I_{ac} + I_{C2}$). The path for I_{C2} is depicted in Fig. 3.6b, while I_{C2} is calculated as:

$$I_{C2} = \left(\frac{V_2}{R_2}\right) \times exp\left(\frac{t}{R_2 \times C_2}\right) \tag{3.5}$$

Where,

$$\begin{aligned} V_2 &= V_{DC} - V_{D2} - V_{C2} \\ R_2 &= r_{D2} + r_{S1} + R_{ESR_{C2}} \end{aligned} \tag{3.6}$$

Where, $R_{ESR_{C1}}$ is the equivalent series resistance of capacitor C_2. The path for charging current I_{C3} is depicted in Fig. 3.6c. and I_{C3} is calculated as:

$$I_{C3} = \left(\frac{V_3}{R_3}\right) \times exp\left(\frac{t}{R_3 \times C_{eq}}\right) \tag{3.7}$$

Where,

$$\begin{aligned} V_3 &= V_{DC} + V_{C1} + V_{C2} - V_{C3} \\ R_3 &= r_{S2} + r_{S3} + r_{S5} + r_{D6} + r_{D7} + R_{ESR_{C2}} \\ \frac{1}{C_{eq}} &= \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} \end{aligned} \tag{3.8}$$

With Fig. 3.6c, the current stress on switch S_2, S_3, S_5, S_6 and S_7 can be expressed as $I_{ac} + I_{C1} + I_{C2} + I_{C3}$.

3.4.2 Designing of capacitors

The voltages at capacitors (C_1,C_2 and C_3) experience ripple during their discharge in series with the voltage source to boost the load voltage level. These ripples should be limited to 10% of their maximum voltages [96], which are V_{DC}, V_{DC} and $3V_{DC}$ for C_1, C_2 and C_3 respectively. These ripples although depends on capacitance value, discharging period and the load type, the maximum discharging is resulted in capacitor through resistive load R_L [94]. As evident from Fig. 3.7, capacitors C_1, C_2 experience the maximum continuous discharging from ϕ_2 to $\pi - \phi_2$ during output voltage levels of $+5V_{DC}$ and $+6V_{DC}$; the capacitor C_3 experiences maximum continuous discharging from ϕ_1 to $\pi - \phi_1$ during the output voltage levels of $+4V_{DC}$, $+5V_{DC}$, $+6V_{DC}$. Similar discharges happen in negative cycle with C_1, C_2 during output voltage of $-5V_{DC}$ and $-6V_{DC}$ and with C_3 during output voltages of $-4V_{DC}$, $-5V_{DC}$, $-6V_{DC}$

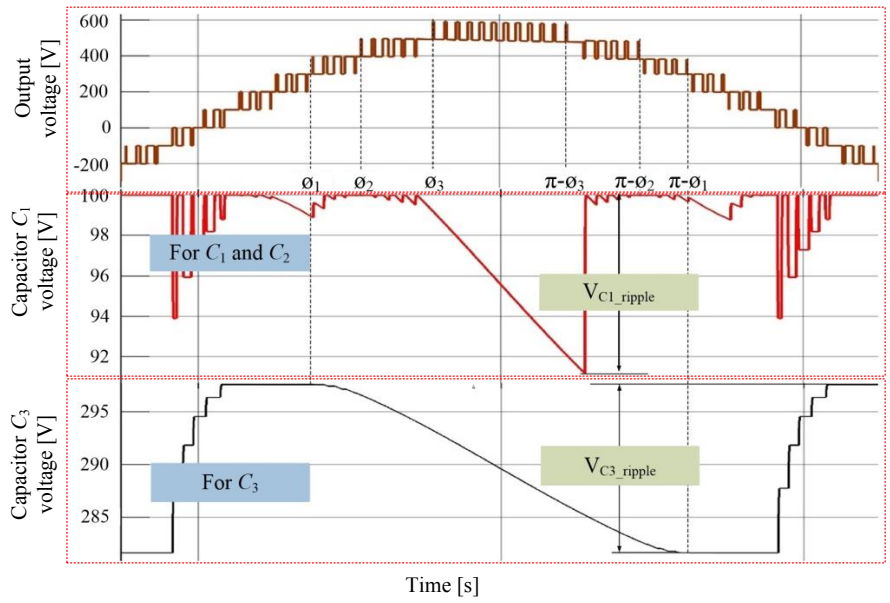


Fig. 3.7: *Voltage ripple across capacitors*

$$\Delta Q_{C1} = C_1 \times \Delta V_{C1}$$

$$= \int_{\frac{\phi_2}{\omega}}^{\frac{\phi_3}{\omega}} \frac{5V_{DC}}{R_L}\,dt + \int_{\frac{\phi_3}{\omega}}^{\frac{\pi-\phi_3}{\omega}} \frac{6V_{DC}}{R_L}\,dt + \int_{\frac{\pi-\phi_3}{\omega}}^{\frac{\pi-\phi_2}{\omega}} \frac{5V_{DC}}{R_L}\,dt \tag{3.9}$$

$$\Delta Q_{C1} = \frac{V_{DC}}{\omega \times R_L} \times (6\pi - 10\phi_2 - 2\phi_3) \tag{3.10}$$

And, it can be observed from Fig. 3.4 that,

$$\phi_1 = sin^{-1}\left(\frac{1}{2M}\right) \tag{3.11}$$

$$\phi_2 = sin^{-1}\left(\frac{2}{3M}\right) \tag{3.12}$$

$$\phi_3 = sin^{-1}\left(\frac{5}{6M}\right) \tag{3.13}$$

With a maximum allowed voltage ripple of 10%, we have:

$$\frac{100\Delta V_{C1}}{V_{DC}} \leq 10 \tag{3.14}$$

Using these equations, we have:

$$C_1 \geq \frac{10}{2\pi \times f \times R_L}\left[6\pi - 10sin^{-1}\left(\frac{2}{3M}\right) - 2sin^{-1}\left(\frac{5}{6M}\right)\right] \tag{3.15}$$

A similar analysis for C_2 would show that it is equal to C_1, i.e.,

$$C_1 = C_2 \tag{3.16}$$

Similarly, for capacitor C_3

$$\begin{aligned}\Delta Q_3 &= C_3 \times \Delta V_{C3} \\ &= \int_{\frac{\phi_1}{\omega}}^{\frac{\phi_2}{\omega}} \frac{4V_{DC}}{R_L}\,dt + \int_{\frac{\phi_2}{\omega}}^{\frac{\phi_3}{\omega}} \frac{5V_{DC}}{R_L}\,dt + \int_{\frac{\phi_3}{\omega}}^{\frac{\pi-\phi_3}{\omega}} \frac{6V_{DC}}{R_L}\,dt \\ &+ \int_{\frac{\pi-\phi_3}{\omega}}^{\frac{\pi-\phi_2}{\omega}} \frac{5V_{DC}}{R_L}\,dt + \int_{\frac{\pi-\phi_2}{\omega}}^{\frac{\pi-\phi_1}{\omega}} \frac{4V_{DC}}{R_L}\,dt\end{aligned} \tag{3.17}$$

$$\Delta Q_3 = \frac{V_{DC}}{\omega \times R_L} \times (6\pi - 8\phi_1 - 2\phi_2 - 2\phi_3) \tag{3.18}$$

With a maximum allowed voltage ripple of 10%, we have:

$$\frac{100\Delta V_{C3}}{3V_{DC}} \leq 10 \tag{3.19}$$

Using these equations, we have:

$$\begin{aligned}C_3 \geq &\frac{10}{6\pi \times f \times R_L}\Big[6\pi - 8sin^{-1}\left(\frac{1}{2M}\right) \\ &- 2sin^{-1}\left(\frac{2}{3M}\right) - 2sin^{-1}\left(\frac{5}{6M}\right)\Big]\end{aligned} \tag{3.20}$$

3.5 CONTROL AND FILTER DESIGN FOR GRID CONNECTED INVERTER

The scheme to generate reference signal for triggering the power switches is described herewith to control the injection of both the active and reactive powers to the grid. The RES is assumed as voltage source, which appears as input to inverter. A Phase-Lock Loop (PLL) is used as the synchronous unit for detecting the appropriate amplitude and phase of the local grid [102]. It generates a signal in phase with the grid voltage to draw active power. Then, based on the

reference value of the active power, the required phase and amplitude of the current to be injected in the grid, known as the reference inverter current (I_{invRef}), is calculated [103]. By comparing reference and inverter current, the error signal is generated that is sent to the current controller block for applying PR controlled technique and generating the reference signal.

3.5.1 Designing of LCL filter

The inverter current contains ripple and harmonics. When such current is injected into the grid, it results into high loss and power quality issues. To avoid these issues, an LCL filter is used at inverter output so yield harmonic free current. The filter capacitor (C) is designed based on the reactive power absorbed at the rated conditions. The reactive power (Q) absorbed by the capacitor is limited to 5% of the rated power [104].

$$Q = \frac{{V_{\text{grid}}}^2}{\frac{1}{2\times\pi\times f\times C}} \tag{3.21}$$

$$\frac{{V_{\text{grid}}}^2}{\frac{1}{2\times\pi\times f\times C}} = 5\% \text{ of Rated power}(P) \tag{3.22}$$

Similarly, value of inverter side inductor L_1 is selected based on the maximum permissible current ripple (ΔI_{ppmax}). The current ripples are limited to 20% of the rated current (I) and it is find through the rated power and grid voltage [101].

$$L_1 = \frac{V_{\text{DC}}}{4 \times f_{\text{sw}} \times \Delta I_{\text{ppmax}}} \tag{3.23}$$

The total inductance (L_1+L_2) is selected based on the maximum voltage drop across the inductor, which is limited to 10% of grid voltage.

$$V_{\text{L1+L2}} = I \times X_{\text{L1+L2}} \tag{3.24}$$

$$L_1 + L_2 = \frac{10\%\ of\ V}{I \times 2 \times \pi \times f} \tag{3.25}$$

3.5.2 Designing of controller

To accomplish zero steady-state error, a Proportional Resonant (PR) controller is realized. Because of an infinite gain at the grid frequency, it accomplishes superior performance for both the sinusoidal reference tracking and the unsettling disturbance rejection. The transfer function of PR controller is expressed as :

$$Y(S) = E(S) \times \left(K_{\mathrm{p}} + \frac{K_{\mathrm{r}} S}{S^2 + \omega^2}\right) \tag{3.26}$$

The value of K_{p} depends on the filter inductor and controller time constant i.e.

$$K_{\mathrm{p}} = \frac{\text{Inductance}}{\text{Time Constant}} \tag{3.27}$$

And the value of K_{r} depends on controller gain, resonant frequency and grid frequency,

$$\text{Gain} = \frac{K_{\mathrm{r}} \omega_{\mathrm{n}}}{{\omega_{\mathrm{n}}}^2 - \omega^2} \tag{3.28}$$

3.6 COMPARISON WITH OTHER 13-LEVEL TOPOLOGIES

The SC based multilevel inverters offer a high voltage gain, whereas conventional CHB, NPC and FC yields only unity voltage gain. The proposed new 13-level SC based multi-level inverter is compared with existing 13-level SCs-based structures. The comparison is summarized in Table 3.4 when all are supplied with only one DC source. This study is based on the number of IGBT switches (N_{S}), the number of IGBT gate drivers (N_{G}), the number of diodes (N_{D}), the number of capacitors (N_{C}), the Total Standing Voltage (TSV) of all switches and diodes, ratio of the maximum output voltage to DC voltage sources, i.e. Boosting Factor (BF), Cost Function (CF), peak inverse voltage (PIV), number of components per levels ($\frac{N_{\mathrm{c}}}{N_{\mathrm{L}}}$). The CF [99] is used to find the cost per level its represented through (3.29). It is interpreted by:

Table 3.4. *Comparison with other 13-level topologies*

Circuits	N_S	N_G	N_D	N_C	**BF**	**PIV**	**TSV**	$\frac{N_c}{N_L}$	**CF**
[93]	14	14	0	4	3	2	40	2.46	5.54
[94]	19	19	0	5	6	3	39	3.30	6.30
[95]	10	10	10	5	6	3	59	2.69	7.23
[96]	29	29	5	5	6	3	34	5.23	7.84
[97]	14	14	0	3	6	3	33	2.38	4.92
[98]	13	13	2	3	6	6	39	2.38	5.38
[99]	13	13	2	3	6	3	32	2.38	4.69
[100]	12	12	4	3	6	3	36	2.38	5.16
Proposed	**12**	**12**	**2**	**3**	**6**	**6**	**39**	**2.23**	**3.23**

$$\mathrm{CF} = \frac{N_S + N_G + N_D + N_C + N_{AD} + TSV}{N_L} \times N_{IS} \tag{3.29}$$

As evident from Table 3.4, the structures [93, 94, 96] have the minimum TSV and PIV but require more N_S and thus resulting into higher CF. Both proposed and inverter [100] are realized with least 12 switches. However, more diodes are needed in realizing the inverter [100] and thus causes higher components per level rate. The MLI of [97] and [99] although have lower TVS and a low CF but require addition switches, which cause higher number of components per level rate. Therefore, the proposed MLI is found superior in terms of number of switches, overall cost function and number of components per level rate.

3.7 RESULTS AND DISCUSSION

The experimental examination is carried out to validate the proposed 13-level inverter's topology and control system. Because it has a voltage boost factor of 6, the input side DC voltage (V_{DC}) is set to 60 V to connect to a 230 VRMS, 50Hz single-phase grid. Other parameters that are used to validate the performance are summarized in Table 3.5. The experimental set-up is presented in Fig. 3.8. It is developed with a power switch module and appropriate gate drivers. The PV emulator is used as DC power supply and OPAL-RT OP4510 real-time controller is used in

conjunction with MATLAB for produce the gating pulses. Fig. 3.9 and Fig. 3.10 display the total harmonic distortion (THD) of the output voltage and current under an inductive load. The THD of the 13-level output voltage is observed to be 11.14%, while the THD of the output current under the inductive load condition is 1.56%. In Fig. 3.9, the fundamental frequency at 50Hz exhibits the maximum components of the output voltage, measuring 330.4V. Additionally, the zoom view reveals the presence of very low amplitude components corresponding to other order harmonics. Similarly, in Fig. 3.10, the fundamental frequency at 50Hz showcases the maximum components of the output current under the inductive load condition, measuring 6.305A. The zoom view provides visibility into the low amplitude components of higher order harmonics. These results demonstrate the performance of the system under an inductive load condition, highlighting the relatively low levels of harmonic distortion in both the output voltage and current. Fig. 3.11 shows the THD of output voltage with respect to the modulation index. As the modulation index reduces, levels of the output voltage are also reduced, which therefore is resulting into higher THD in output voltage.

Table 3.5. *Parameters for experimental validation*

Parameter	**Value**	**Unit**
Input voltage (V_{DC})	60	Volt
Value of capacitor (C_1,C_2,C_3)	1600	μF
Carrier frequency	3000	Hz
Reference frequency	50	Hz
Load resistance	160,80	Ω
Load inductance	240,120	mH

The performance characteristics for close loop grid-connected system shown in Fig. 3.12. The grid voltage is in phase with the grid current and thus maintains a unity power factor, with grid voltage and grid current amplitudes of 325 V and 10 A, respectively. Fig. 3.13, 3.14, 3.15 show the experimental verifications in open-loop condition. The Fig. 3.13 presents the performance characteristics for the sudden change in inductive load. It is realized by decreasing load resistance and inductance values from 100 Ω and 100mH to 50 Ω and 50mH respectively. As expected, and seen in Fig. 13, the output current got doubled. Also, it is showing the voltages across capacitors

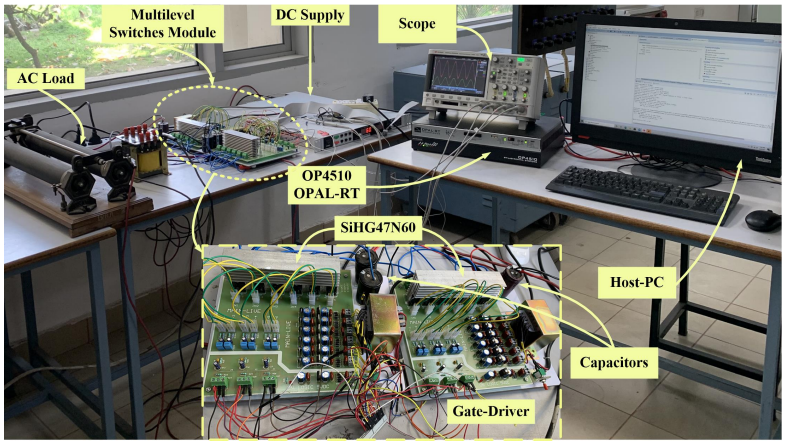


Fig. 3.8: *Experimental setup for verification of proposed work*

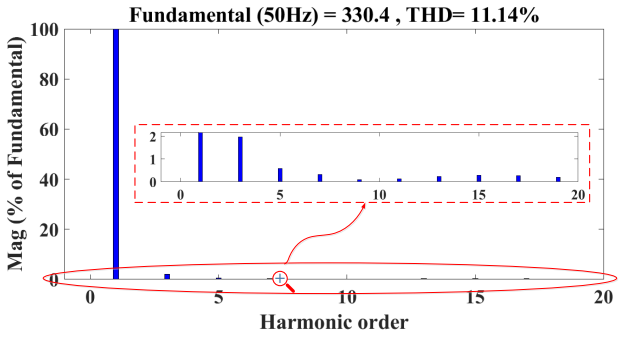


Fig. 3.9: *Total harmonic analysis of output voltage*

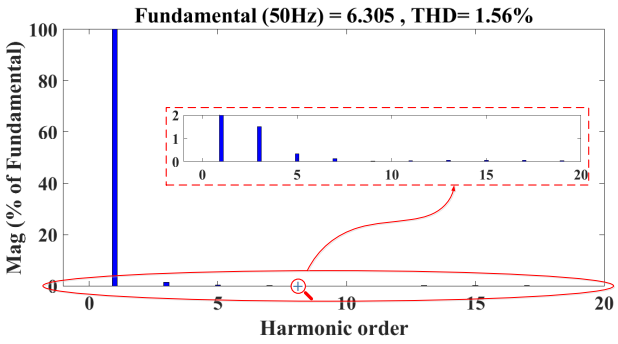


Fig. 3.10: *Total harmonic analysis of output current*

C_1, C_2 and C_3 which are balanced at 60V, 60V and 180V respectively. The capacitor's voltages are maintained within the limit of 10%. Fig. 3.14 shows the experimental results of output voltage and current for a sudden change in a resistive load. It is realized by decreasing load resistance

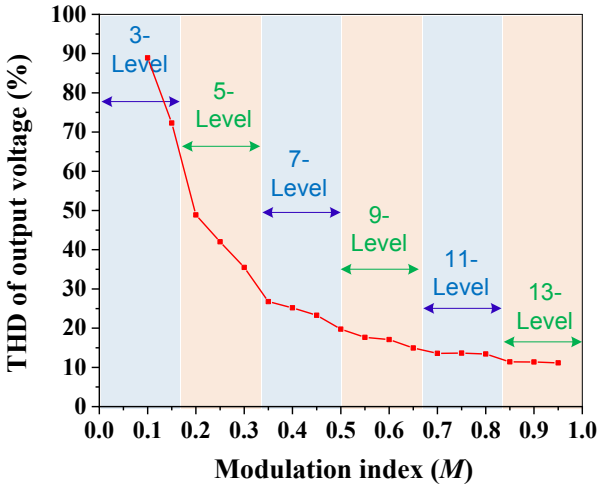


Fig. 3.11: *THD analysis of output voltage for different modulation index*

values from 100Ω to 50 Ω. Similarly, the current doubled and capacitors voltages are balanced in that case.

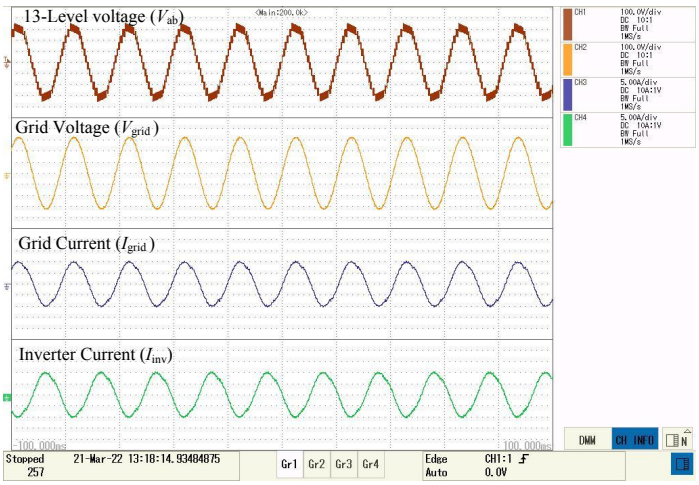


Fig. 3.12: *Experimental waveforms of grid connected system*

Fig. 3.15 shows the variations in the modulation index (*M*) with inductive load. By reducing the value of the modulation index, the peak output voltage and current are reduced. Here, three different M values are considered 0.75, 0.55 and 0.25, which generate output voltage with 11, 9 and 5 levels, respectively. Also, the voltages of the capacitors are balanced to the same value at every value of the M.

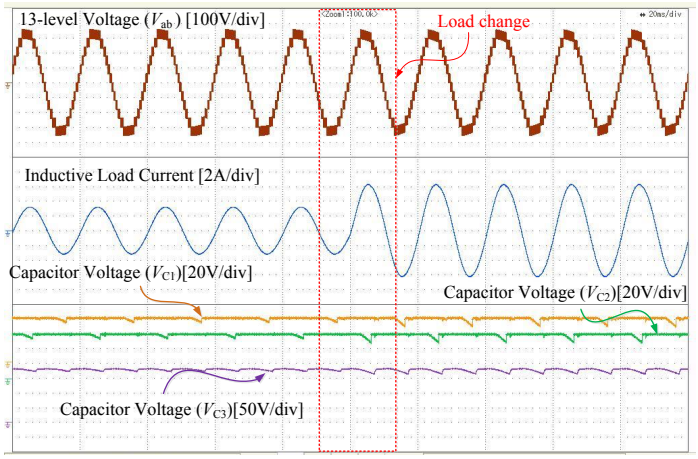


Fig. 3.13: *Output voltage and current with capacitors voltages for inductive load change condition*

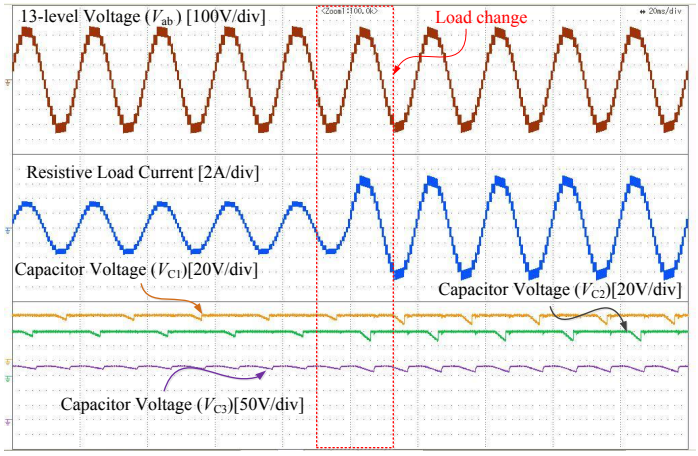


Fig. 3.14: *Output voltage and current with capacitors voltages for resistive load change condition*

The distribution of power losses for the proposed inverter under specific parameters described in Table 3.5 is shown in Fig. 3.16. The total loss in power switches and passive elements is 38.44 W for input power of 980 W, with an overall efficiency of 96.07%. The power loss distribution of the proposed topology is obtained by modelling the converters and their control in Plexim PLECS software. It is observed that switching and conduction losses are reduced. Efficiency is calculated for the different modulation index as shown in Fig. 3.17, here the upper value of the efficiency is 96.2%.

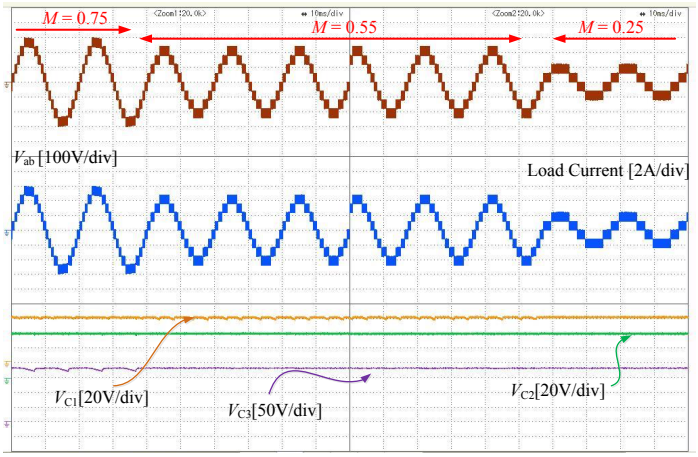


Fig. 3.15: *Experimental waveforms at different modulation indexes*

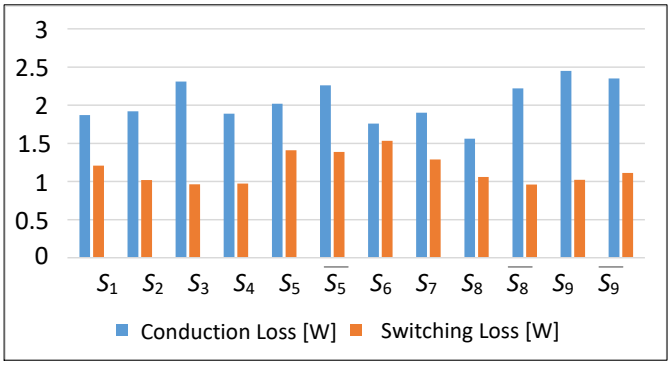


Fig. 3.16: *Distribution of power losses for 980W input power, 38.44W total loss, efficiency 96.07%*

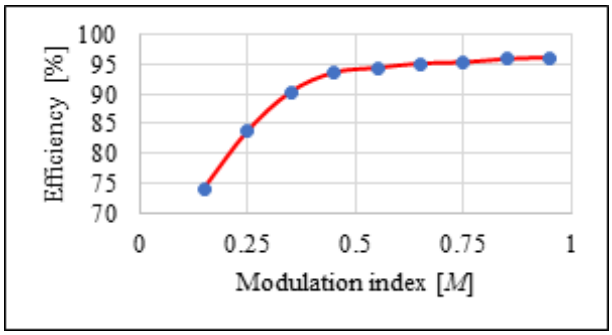


Fig. 3.17: *Efficiency versus modulation index plot*

3.7.1 Role reversal in SCMLIs

To understand the concept of role reversal in switched capacitor-based multilevel topologies, consider a simple single-phase system with V_{DC} as the DC side voltage and V_{AC} as the AC side multilevel voltage. The voltage gain is β (Fig.3.18). Then, the peak value of the fundamental component of the multilevel voltage would be given as [47, 105]:

$$v_{AC,1}^{max} = M.\beta.V_{DC} \tag{3.30}$$

Where M is the modulation index with $0.5 \leq M \leq 1$

Now, for a rectification system based on the SCs, the peak value of the grid voltage (v_g^{max}) will replace $v_{AC,1}^{max}$, while the output DC voltage (V_{DC}) can be expressed using (3.30) as:

$$V_{DC} = \frac{v_g^{max}}{M.\beta} \tag{3.31}$$

The above expression indicates that for $\beta > 1$ and value of $0.5 \leq M \leq 1$, the output DC voltage would be less than the peak value of the grid voltage, thereby allowing the AC-to-DC conversion to be of buck nature. Furthermore, if the $\beta > 1$ and value of $M \leq 0.5$, the output DC voltage would be higher than the peak value of the grid voltage, thereby allowing the AC-to-DC conversion to be of boost nature.

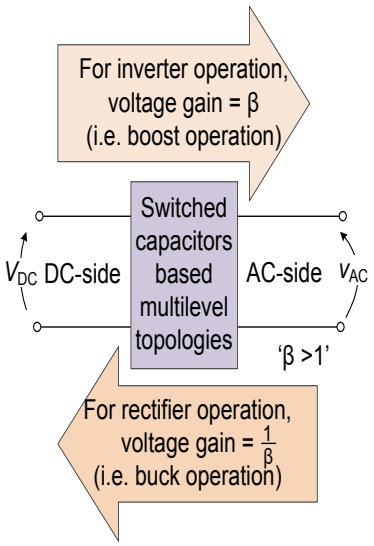


Fig. 3.18: *Role reversal in switched capacitors based multilevel topologies*

Based on (3.31), it can be said that when operated as PFC rectifier, SCs-based multilevel topologies should perform buck-boost operation and can be called as 'switched capacitors based multilevel rectifier'. Some of the SCMLIs [106], [107] can perform rectification, only if the

diodes are replaced with controlled switches. Moreover, most of the SCMLIs topologies cannot be easily extended to their three-phase version, as described in detail in [106]. While many others, which can be bidirectional and extended to three-phase versions, have limitations in terms of large PIV of power switches [108], large number of semiconductor devices, and large total-standing-voltage [108–110].

3.8 CONCLUDING REMARK

This chapter presents a novel 13-level inverter topology. The experimental results validate the proposed power circuit and control system. As it has a voltage boost factor of 6, the input side DC voltage is set to 60 V to connect with AC 230 V, 50Hz single-phase grid. The following observations are made from this study:

- The proposed SCs-based topology generates 13-levels while resulting into a boosting factor of 6 with good response under dynamic condition.
- By using single DC source, it generates 13-levels with high boosting gain and reduced number of switches.
- It maintains high power factor for grid connected application.
- Single state power conversion is achieved from low-voltage DC to high-voltage AC with an optimal number of active power switches.
- During power reversal, when power is draw from the grid, SCs-based inverter can operate as a buck rectifier.
- Variation of modulation index justifies that it can be used for the wide range of AC voltage, and different gain can be achieved through this topology.
- In SCs-based rectifier topology, this variation of modulation index gives a wide range of output DC voltage.

Chapter–4

Five-level PFC Rectifier for EV Charging

Through the investigations on grid-connected SC-based multilevel inverters in Chapter-3, it has been concluded that they perform boost DC-AC conversion with stable operation in a wide range of modulation index. This chapter presents a role reversal approach in SC-based MLR, from SC-based MLI. In this chapter, development, analysis, and verification of a novel bidirectional SC-based five-level PFC rectifier topology are presented for EV charging application for single and three-phase AC inputs.

4.1 GENERAL

The SC-based boost inverter has attracted considerable attention in the grid-connected system. During the inverter mode of operation, large currents from the source are caused because a capacitor is repeatedly connected in parallel with the DC input source. This problem is eliminated in an SCs-based PFC rectifier for EV charging applications. EV charging system under consideration is a two-stage system. Stage-I is the AC-to-DC conversion which performs two main functions: to ensure that the current drawn from the AC source is sinusoidal at unity power factor; and to obtain a regulated output DC voltage. Stage-II comprises a DC-to-DC converter which controls the charging current injected into the EV battery (and sometimes, it also provides isolation between the battery and the grid). Typically, DC-to-DC buck-boost converter or a Dual-Active-Bridge (DAB) is used for stage-II. The battery of an actual EV charging system is not directly connected to the DC side of the AC-to-DC conversion, but rather connected

The contents of this chapter are partly published in:

∗ "A Bidirectional Five-Level Buck PFC Rectifier With Wide Output Range for EV Charging Application," ***IEEE Transactions on Power Electronics***, vol. 37, no. 11, pp. 13439-13455, Nov 2022. doi: https://doi.org/10.1109/TPEL.2022.3185239

through a DC-to-DC conversion stage. Therefore, SC-based multilevel PFC rectifiers are useful for EV charging applications and can eliminate the inrush current problem.

In this chapter, a PFC five-level rectifier with self-balanced switched capacitors is proposed. Each leg of the presented topology comprises five power switches and one switched capacitor, where the voltage ratings of power switches are equal to the output DC voltage. It does not require an additional filter capacitor on the DC side, as the load appears in parallel always with a switched capacitor of one of the legs. The five-level operation with continuous conduction leads to the elimination of the capacitive filter on the AC-side and inductive filter on the DC-side. Due to phase modular structure of the proposed topology, it can be easily extended to its three-phase version. This is achieved by adding a third leg which too carries a switched capacitor and five power switches.

4.2 PROPOSED FIVE-LEVEL BUCK RECTIFIER

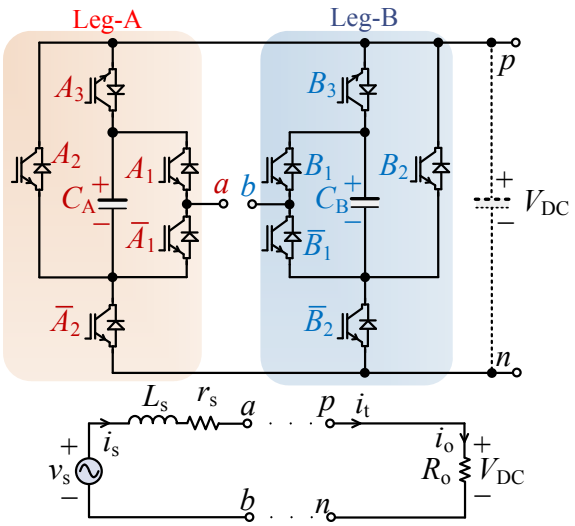


Fig. 4.1: *Proposed five-level PFC rectifier topology (single-phase)*

The proposed rectifier topology is shown in Fig. 4.1, wherein two legs 'A' and 'B' are shown. The AC input voltage is given at the terminals 'a' and 'b', while the DC output voltage is obtained between the terminals 'p' and 'n', with 'p' being the higher potential terminal. The output voltage is shown as 'V_{DC}'. Each leg has five active switches and one capacitor, which is maintained at a voltage equal to V_{DC}. The pole voltages ('V_{an}' and 'V_{bn}') thus have three voltage levels: $+2V_{DC}$, $+V_{DC}$ and 0. Of the five switches in a leg, say the leg A, the pairs (A_1, $\overline{A_1}$) and

(A_2, $\overline{A_2}$) are complementary, while the switch A_3 operates simultaneously with $\overline{A_2}$. That is, if '1' corresponds to 'ON' state and '0' corresponds to 'OFF' state of a switch,

$$\overline{A_1} = 1 - A_1$$
$$\overline{A_2} = 1 - A_2 = A_3 \tag{4.1}$$

The voltage V_{ab} can thus be expressed as:

$$V_{ab} = V_{an} - V_{bn} \tag{4.2}$$

Since the pole voltages V_{an} and V_{bn} have three levels, the line voltage V_{ab} manifests five levels viz. $\pm 2V_{DC}$, $\pm V_{DC}$ and 0.

4.2.1 Five-level buck mode (0.5<M<1)

All the valid operating states for the proposed rectifier are summarized in Table 4.1, where ON and OFF states of a power switch are shown with '1' and '0' respectively, and charging and discharging states of the capacitors are shown with 'C' and 'D' respectively. Therein, conduction paths of three currents are shown: i_o is the load current, i_c is the inter-capacitors current and i'_s is the AC component drawn from the grid. These currents are respectively shown in blue, green and red colours. Various switching states for the proposed rectifier are described herewith:

1. State St_1 ($V_{ab} = +2V_{DC}$): During this state, in the positive half cycle, the switches A_1, A_2, $\overline{B_1}$, $\overline{B_2}$ and B_3 are simultaneously turned ON, so as to achieve two simultaneous conduction paths as shown in Fig. 4.2a. In the path shown with red, it can be seen that the $V_{ab} = +2V_{DC}$. Both the capacitors get charged from the AC source.

2. State St_2 ($V_{ab} = +V_{DC}$): During this state, in the positive half cycle, the switches A_1, $\overline{A_2}$, A_3, $\overline{B_1}$, $\overline{B_2}$ and B_3 are simultaneously turned ON, so as to achieve three simultaneous conduction paths as shown in Fig. 4.2b. The capacitor C_A is in charging state and the capacitor C_B is in parallel with the load. Both the capacitors too are in parallel due to which an inter-capacitors current flows to balance their voltages.

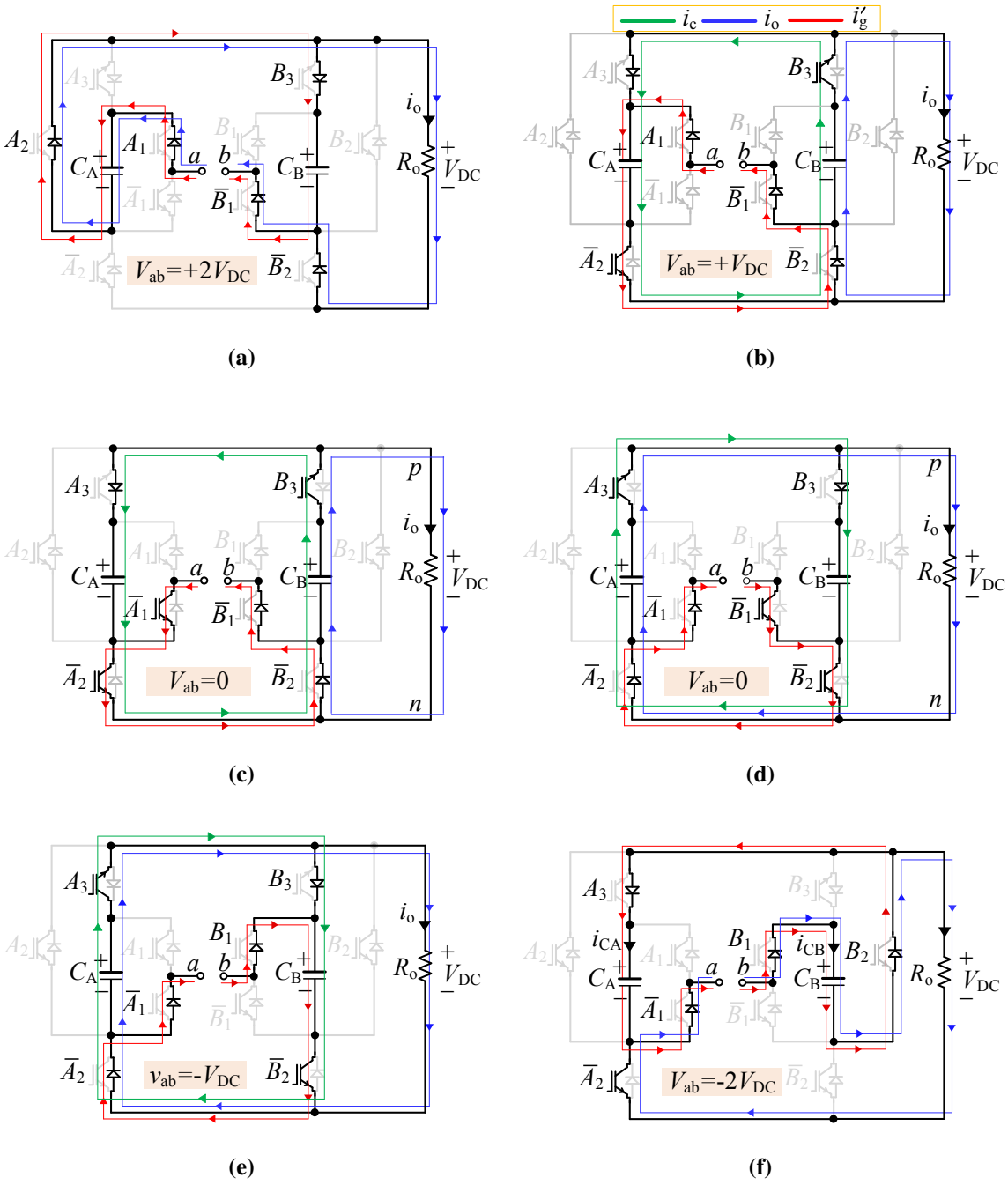


Fig. 4.2: *Switching states for the proposed five-level buck rectifier*

3. State St_3 and St_4 (V_{ab} = 0): During this state, in the positive and negative half cycle, the switches $\overline{A_1}$, $\overline{A_2}$, A_3, $\overline{B_1}$, $\overline{B_2}$ and B_3 are simultaneously turned ON, so as to achieve three simultaneous conduction paths as shown in Fig. 4.2c and Fig. 4.2d. In these states, V_{ab} = 0. For the positive half cycle, capacitor C_B is in parallel with the load, while during the negative half cycle, capacitor C_A is in parallel with the load. Once again, in both the states, the inter-capacitors current balances the voltages of the two capacitors.

4. State St_5 ($V_{ab} = -V_{DC}$): During this state, in the negative half cycle, the switches $\overline{A_1}$, $\overline{A_2}$, A_3, B_1, $\overline{B_2}$, and B_3 are simultaneously turned ON, so as to obtain $V_{ab} = -V_{DC}$. As shown in Fig. 4.2e, the capacitor C_B is in charging state and the capacitor C_A is in parallel with the load. The voltages of the capacitors are balanced by the inter-capacitors current.

5. State St_6 ($V_{ab} = -2V_{DC}$): During this state, in the negative half cycle, the switches $\overline{A_1}$, $\overline{A_2}$, A_3, B_1 and B_2 are simultaneously turned ON, so as to obtain $V_{ab} = -2V_{DC}$. As shown in Fig. 4.2f, both the capacitors are in the charging state.

In this range of modulation index ($0.5<M<1$), the proposed topology operates in buck mode and generates five voltage levels at the input terminals of the rectifier.

4.2.2 Three-level boost mode (M<0.5)

While the proposed topology is primarily a buck converter, it can perform boost operation as well, albeit with the synthesis of three levels instead of five. This warrants a discussion, especially from the point of view of switching states. The equivalent circuit for the boost mode of operation is shown in Fig. 4.3.

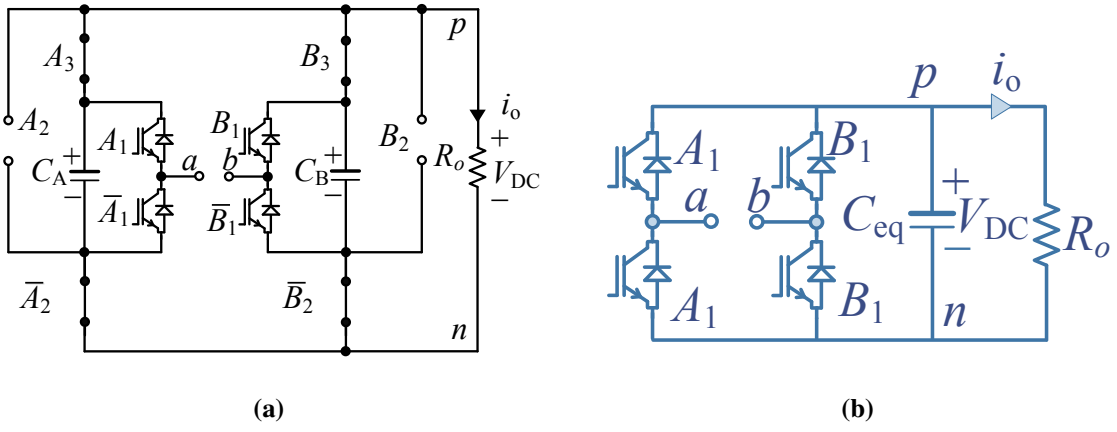


Fig. 4.3: *Equivalent circuits of the proposed rectifier for boost mode of operation ($M < 0.5$)*

Table 4.1. *Switching states of the proposed five-level rectifier*

State	i_s	**Leg-A**			**Leg-B**			$V_{ab} = V_{an} - V_{bn}$	**Capacitors**	
		Switches		$V_{an} = (A_1 + A_2)V_{DC}$	**Switches**		$V_{bn} = (B_1 + B_1)V_{DC}$			
		A_1	A_2		B_1	B_1			C_A	C_B
St_1	$i_s > 0$	1	1	$+2V_{DC}$	0	0	0	$+2V_{DC}$	C	C
St_2	$i_s > 0$	1	0	$+V_{DC}$	0	0	0	$+V_{DC}$	C	D
St_3	$i_s \geq 0$	0	0	0	0	0	0	0	D	D
St_4	$i_s \leq 0$	0	0	0	0	0	0	0	D	D
St_5	$i_s < 0$	0	0	0	1	0	$+V_{DC}$	$-V_{DC}$	D	C
St_6	$i_s < 0$	0	0	0	1	1	$+2V_{DC}$	$-2V_{DC}$	C	C

For M <0.5, the states $\pm 2V_{DC}$ are not synthesized at the input terminals. This is so, because only switches A_1, $\overline{A_1}$, B_1, $\overline{B_1}$ operate, while switches A_2 and B_2 are permanently OFF and switches $\overline{A_2}$, $\overline{B_2}$, and A_3, B_3 are permanently ON, as shown in Fig.4.2b–4.2e. Here C_A, C_B are in parallel with an equivalent capacitance of C_{eq}. It can be observed that the operating states for boost-mode are similar to the operation of the HB rectifier. Boost mode of operation generates a three-level voltage at the input of the rectifier viz. $+V_{DC}$, 0 and $-V_{DC}$. Operating states of this mode are same as St_2–St_5.

4.3 RANGE OF OUTPUT VOLTAGE

In this proposed SC-based rectifier, the value of β is 2. The output DC voltage can therefore be express as:

$$V_{DC} = \frac{v_s^{max}}{2M} \tag{4.3}$$

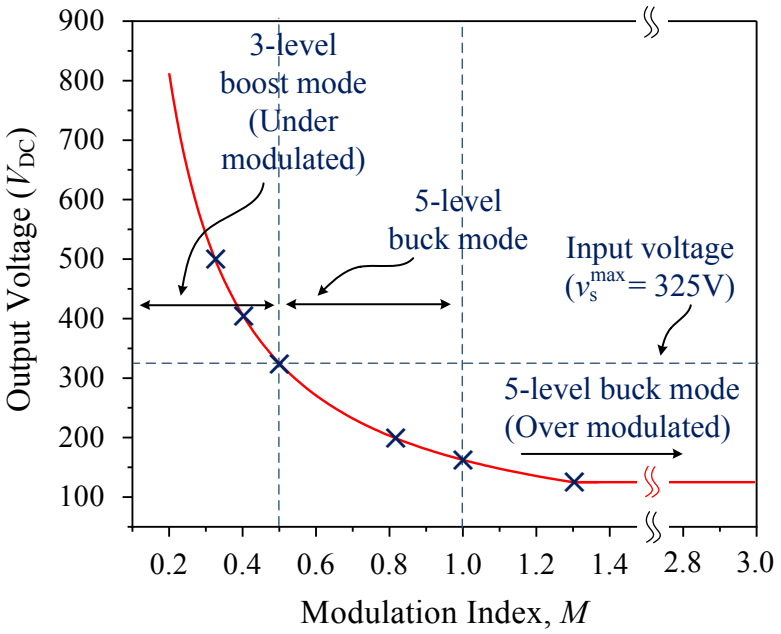


Fig. 4.4: *Variation of the output voltage with respect to modulation index*

The eq (4.3) suggests that the output DC voltage will be equal to the peak grid voltage v_s^{max} for M = 0.5. The value of V_{DC} will be less than v_s^{max} for M greater than 0.5, and therefore the proposed converter will perform buck rectification. During over modulation, where M exceeds

unity, the output voltage will approximate a square waveform, where-in the fundamental AC side waveform acquires a maximum value of $(4/\pi)$ times the peak DC side voltage (i.e. $2V_{DC}$) [47], indicating that V_{DC} can achieve a maximum value equal to $(\pi/8)$ times v_s^{max}. It is observed that V_{DC} exceeds v_s^{max} during under modulation (M <0.5) thereby performing boost operation. As described later, it will be seen that only three levels will be synthesized for M<0.5, in which the voltage V_{ab} manifests the levels viz. $\pm V_{DC}$ and 0 and hence acts as three-level boost rectifier. The above discussion can be summarized as following results for the output voltage V_{DC}:

$$\frac{v_s^{max}}{2} \leq V_{DC} \leq v_s^{max}, \tag{4.4}$$

for $0.5 \leq M \leq 1$, five-level buck operation;

$$\frac{\pi v_s^{max}}{8} < V_{DC} < \frac{v_s^{max}}{2}, \tag{4.5}$$

for M>1, five-level buck operation (overmodulation); and

$$V_{DC} > v_s^{max}, \tag{4.6}$$

for M<0.5, three-level boost operation.

Output voltage variation in terms of modulation index is shown in Fig. 4.4, for input RMS AC voltage of 230 V (i.e. peak value of 325V).

4.4 CONTROL AND MODULATION TECHNIQUE

In this section, the discussion covers the voltage and current control of a PFC rectifier with a closed-loop structure, as well as the modulation technique discussed for the generation of gate pulses.

4.4.1 Multicarrier pulse width modulation technique

For the modulation of MLRs, different techniques have been used, including high switching frequency techniques (such as multicarrier PWM and space vector PWM) and low switching frequency methods (such as active harmonic elimination, selective harmonic elimination and nearest level control). The proposed MLR can be modulated with any of these techniques with appropriate adaptation. In the proposed work, a LSPWM scheme is employed for the gating signal generation, as shown in Fig. 4.5.

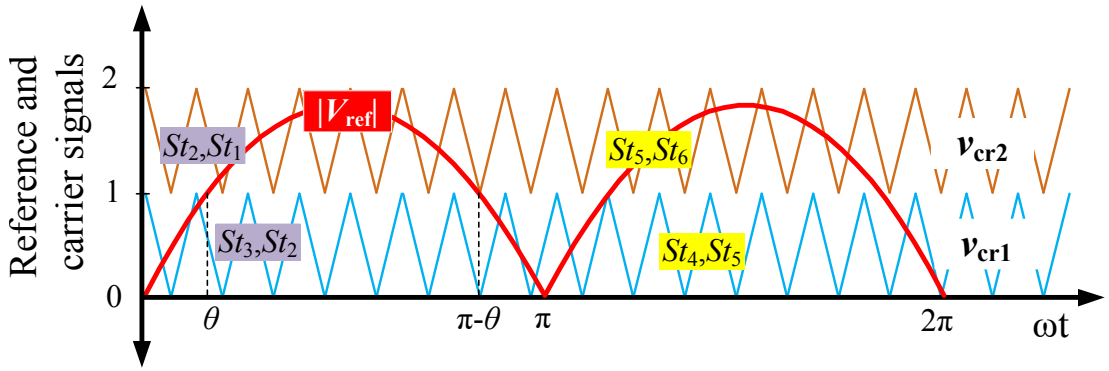


Fig. 4.5: *Level-shifted modulation scheme for the proposed rectifier*

A reference waveform (V_{ref}) of frequency (f_{ref}) is taken as the reference signal which is generated by the voltage controller and its absolute value $|V_{\text{ref}}|$ is compared with the two high-frequency triangular carrier waveforms v_{cr1} and v_{cr2}.

During $0 \leq \omega t \leq 2\pi$, requirements of various operating states are shown in Fig. 4.5. During $0 \leq \omega t \leq \pi$, when v_{cr1} is compared with $|V_{\text{ref}}|$, the input voltage levels are (0 and V_{DC}) which are to be obtained by generating signals for states St_3 and St_2. Similarly, when v_{cr2} is compared with $|V_{\text{ref}}|$, the input voltage levels are V_{DC} and $2V_{\text{DC}}$, which are to be obtained by generating signals for states St_2 and St_1. For the remaining half cycle, during $\pi \leq \omega t \leq 2\pi$, the states for the negative half cycle are to be generated. When v_{cr1} and v_{cr2} are compared with $|V_{\text{ref}}|$, the output voltage levels are 0, $-V_{\text{DC}}$ and $-V_{\text{DC}}$, $-2V_{\text{DC}}$, which are to be obtained by generating signals for states St_4, St_5 and St_5, St_6 respectively. Logic gates based switching pulse generation is shown in Fig. 4.6.

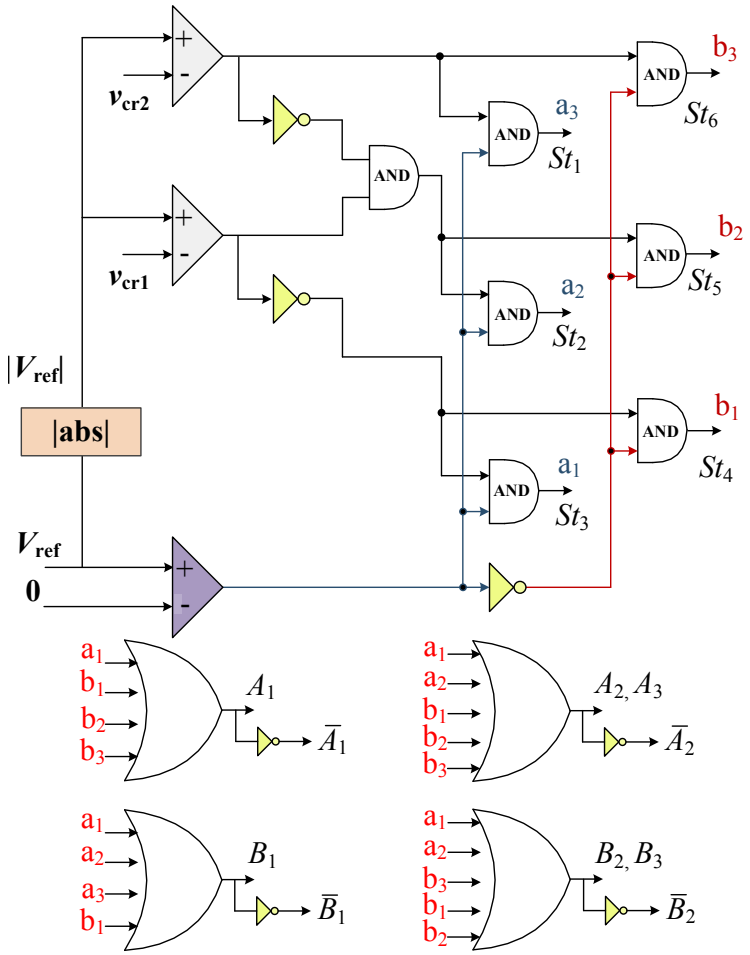


Fig. 4.6: *Logic gates-based generation of switching signals*

4.4.2 Controller design

In a rectifier circuit, using hysteresis current controller, the grid current is shaped into a sine wave. By using this controller, switching complications occurs like large and variable switching frequency which increases power losses. For the proposed rectifier topology, a simple controller including two cascaded loops is designed for the generating the switching pulses. The inner loop is used for grid-current control and the outer loop is for regulating the output voltage. Primarily, the AC grid average current is shown in:

$$L_s \frac{di_s}{dt} = v_s - r_s i_s - V_{ab}$$

$$= v_s - r_s i_s - DV_{DC} \tag{4.7}$$

Where, L_s is the grid inductor and r_s is that inductor parasitic resistance, D is the buck rectifiers duty cycle. The small-signal model of (4.7) can be converted into Laplace domain by assuming a constant value of grid voltage (v_s), and averaged value of grid current and duty cycle.

$$L_s s i_s = -i_s r_s - D V^*_{DC} \tag{4.8}$$

As the inner loop should be faster than the outer loop, it is appropriate to consider the outer loop value, which is the DC voltage, to be constant. The following transfer function is obtained for the grid-connected rectifier inner loop using a DC voltage reference value V^*_{DC}, indicating that the DC voltage output, inductive filter value, and line impedance affect the grid AC current.

$$\frac{i_s}{D} = \frac{-V^*_{DC}}{L_s s + r_s} \tag{4.9}$$

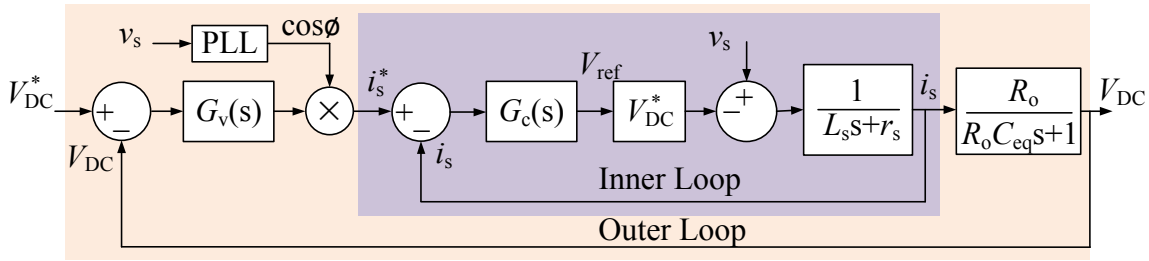


Fig. 4.7: *Inner and outer loops for voltage and current controllers*

Fig. 4.7 shows the inner and outer loops of the controller. Where, in the inner loop, current controller $G_c(s)$ can be either a simple gain as a proportional controller or a Proportional-Integral (PI) controller. It should be noted that the inner loop should have a faster dynamics than the outer loop. Therefore, in the case of a sinusoidal input current signal using a PI controller, the integral gain of that PI should be minimal enough not to change the inner loop's speed. However, the use of a PI compensator on a sinusoidal signal creates some steady-state errors that can be seen as a DC component in the current harmonic spectrum. A PR controller with an infinite gain at the grid frequency (f_{ref}), which shows zero steady-state error, is one alternative for such situation [111]. Furthermore, another loop should be added to the controller to regulate the output DC voltage. Equations from the DC side of the rectifier should be examined to obtain the system model for the outer loop:

$$i_s = i_{c_{eq}} + i_o$$

$$C_{\text{eq}}\frac{dV}{dt} = i_{\text{s}} - \frac{V_{\text{DC}}}{R_{\text{o}}} \tag{4.10}$$

Where the capacitors are parallel equivalent to C_{eq}, and load current is i_{o}. The following transfer function for the outer loop will be accomplished by small-signal modelling of (4.10) conversion to s-domain. The relationship between the output DC voltage, value of the load resistance and DC capacitor value is shown by transfer function.

$$\frac{V_{\text{DC}}}{i_{\text{s}}} = \frac{R_{\text{o}}}{R_{\text{o}}C_{\text{eq}}\text{s} + 1} \tag{4.11}$$

The voltage controller can be considered the outer loop due to the relationship between i_{s} and V_{DC} as (4.11). Such loops deliver the idea of a cascaded controller in which an input for the inner loop is the output of the outer loop. As there is no frequency in the DC signal, a PI compensator with a $G_v(\text{s})$ transfer function is used to control the voltage at the desired level. The voltage control system controls the output DC voltage at V^*_{DC}, as shown in Fig.4.7, and provides the reference current peak value as an input to the inner loop. Due to its low complexity and adequate accuracy, the controller shown in Fig.4.7 can be easily implemented with real-time controllers.

4.5 DESIGN PARAMETERS, TOTAL STORED ENERGY AND LOSS ANALYSIS

In this section, the discussion covers the design parameters of the PFC rectifier, the total energy stored, and the switching device power of the proposed rectifier.

4.5.1 Design parameters

Designing of parameters includes the designing of input filter, designing of SCs and the ratings of power switches based on voltage and current ratings.

4.5.1.1 Filter inductor (L_{s}) for the input side

Inductive filter is modelled as a series connection of an inductor L_{s} and equivalent series resistance r_{s}. As filter inductor bears the grid current i_{s}, the value of L_{s} mainly depends on the

allowable maximum input current ripple, Δi_s^{max}. The maximum input current ripple (Δi_s^{max}) is limited to 20% of the rated current. In the system under consideration, the input voltage to the proposed rectifier, designated as V_{ab}, is a five-level voltage (comprising the voltage levels 0, $\pm V_{DC}$, $\pm 2V_{DC}$). For the purpose of filter design, the system is modelled as shown in Fig. 4.8. The governing equation can be written as:

$$L_s \frac{di_s}{dt} = v_s - r_s i_s - V_{ab} \tag{4.12}$$

For a given switching cycle of period T_{sw} and duty-ratio D, the above equation is approximated as:

$$L_s \frac{\Delta i_s}{D.T_{sw}} = v_s - r_s i_s - V_{ab} \tag{4.13}$$

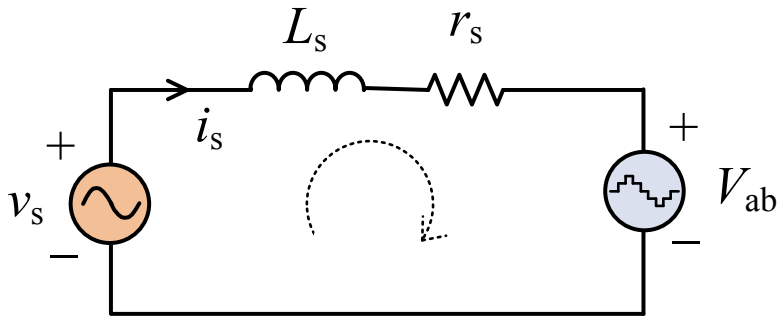


Fig. 4.8: *Model of the conversion system for inductive filter design*

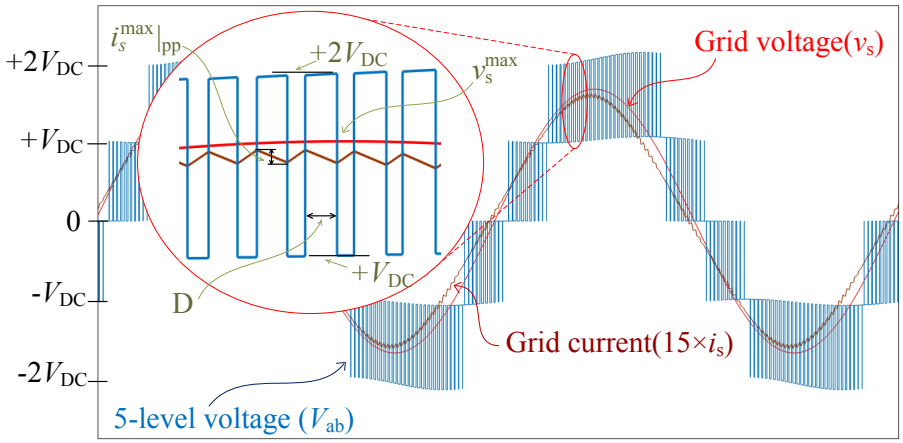


Fig. 4.9: *Waveforms pertaining to the design of filter inductor*

To determine the minimum required value of L_s, a limiting scenario may be considered with the grid voltage at its maximum value (v_s^{max}), V_{ab} being equal to V_{DC} (since V_{ab} undergoes

transitions between $2V_{DC} \leftrightarrow V_{DC}$ when v_s is in the region of its peak value), duty ratio being 50% and the resistance of the filter as negligible. Accordingly, the ripple on the inductor is maximum, with its peak-to-peak value being $\Delta i_s^{max}|_{pp}$ and the value of L_s can be obtained as:

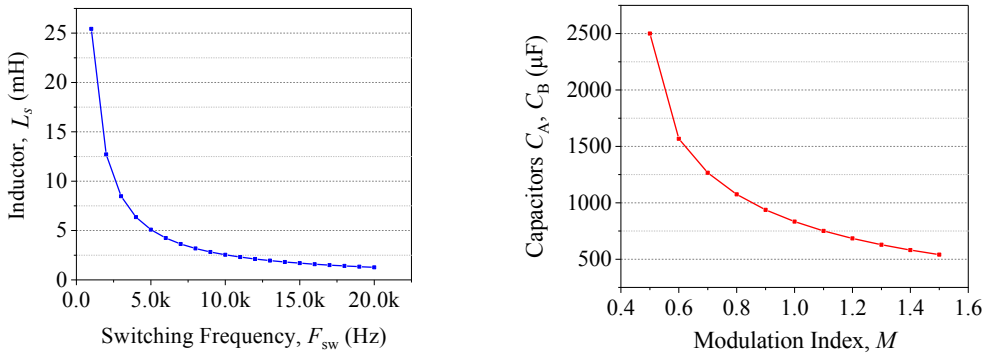
$$L_s = \frac{(v_s^{max} - V_{DC}).T_{sw}}{2\Delta i_s^{max}|_{pp}} \tag{4.14}$$

Where, in terms of the modulation index M, V_{DC} is expressed as (4.6):

$$L_s = \frac{v_s^{max}(1 - \frac{1}{2M})}{2.F_{sw}\Delta i_s^{max}|_{pp}} \tag{4.15}$$

Variation of filter inductance (for v_s^{max} =325V, V_{DC} = 200V) with different switching frequencies is shown in Fig. 4.10a.

4.5.1.2 Designing of SCs



(a) **(b)**

Fig. 4.10: *Designing of passive components: (a) variation of filter inductance with change in switching frequency; and (b) variation of capacitance with modulation index*

The proposed rectifier is working on the principle of switched-capacitor (C_X, X ∈ A, B) to maintain the voltage of capacitor C_X at V_{DC}. When this capacitor discharges to load, voltage ripples should not exceed 10% of the appropriate capacitor voltage, which are decided by discharging time and load current. Through the switching states as shown in Fig. 4.2, it is clear

that, capacitor C_X experiences the maximum continuous discharge in 0 output level occurring from 0 to θ. The maximum discharge for the load R_o can be articulated as:

$$\Delta Q_{C_X} = C_X.\Delta V_{C_X} = \int_0^{\theta} \frac{V_{DC}}{2R_o}\, d(\omega t) \tag{4.16}$$

Solving

$$\Delta Q_{C_X} = \frac{V_{DC}}{\omega.R_o}\theta \tag{4.17}$$

Where,

$$\theta = sin^{-1}\left(\frac{1}{2M}\right) \tag{4.18}$$

If 10% of maximum ripple are allowed:

$$\frac{100\Delta V_{C_X}}{V_{DC}} \leq 10 \tag{4.19}$$

Using these equations, we have:

$$C_X \geq \frac{10}{2\omega.R_o}.sin^{-1}\left(\frac{1}{2M}\right) \tag{4.20}$$

This equation is valid for $M > 0.5$ and variation of capacitors values is shown in Fig. 4.10b with different modulating indexes and R_o is taken as 20 Ω.

4.5.1.3 Component ratings

The procedure for determination of voltage and current ratings of power switches is summarized below:

Voltage Ratings of Power Switches: All the power switches need to bear a maximum voltage equal to the output DC voltage. A summary table of the voltages blocked by all the power switches during various states corresponding to Fig. 4.2 is shown in Table 4.2.

Table 4.2. *Current and voltage for the power switches during various states of the proposed topology*

Voltage level	i_{A1}, V_{A1}	i_{A2}, V_{A2}	i_{A3}, V_{A3}	$i_{\overline{A1}}, V_{\overline{A1}}$	$i_{\overline{A2}}, V_{\overline{A2}}$	i_{B1}, V_{B1}	i_{B2}, V_{B2}	i_{B3}, V_{B3}	$i_{\overline{B1}}, V_{\overline{B1}}$	$i_{\overline{B2}}, V_{\overline{B2}}$
$+2V_{DC}$	$i_o+i'_s$,0	$i_o+i'_s$,0	0,V_{DC}	0,V_{DC}	0,V_{DC}	0,V_{DC}	0,V_{DC}	i'_s,0	$i_o+i'_s$,0	i_o,0
$+V_{DC}$	i'_s,0	0,V_{DC}	i_c,0	0,V_{DC}	i'_s+i_c,0	0,V_{DC}	0,V_{DC}	i_c+i_o,0	i'_s,0	$i'_s+i_c+i_o$,0
0	0,V_{DC}	0,V_{DC}	i_c,0	i'_s,0	i'_s+i_c,0	0,V_{DC}	0,V_{DC}	i_c+i_o,0	i'_s,0	$i'_s+i_c+i_o$,0
0	0,V_{DC}	0,V_{DC}	i_c+i_o,0	i'_s,0	$i'_s+i_c+i_o$	0,V_{DC}	0,V_{DC}	i_c,0	i'_s,0	i'_s+i_c,o
$-V_{DC}$	0,V_{DC}	0,V_{DC}	i_c+i_o,0	i'_s,0	$i'_s+i_c+i_o$,0	i'_s,0	0,V_{DC}	i_c,0	0,V_{DC}	i'_s+i_c, 0
$-2V_{DC}$	0,V_{DC}	0,V_{DC}	i'_s,0	$i_o+i'_s$,0	i_o,0	$i_o+i'_s$,0	$i_o+i'_s$,0	0,V_{DC}	0,V_{DC}	0,V_{DC}

Current Ratings of Power Switches: It can be seen from various states (Fig. 4.2) that the conduction paths for the three currents are manifested in a state: *(a)* load current, i_o ; *(b)* AC component drawn from the grid, $i_{s'}$; and *(c)* inter-capacitors current, i_c (Fig. 4.11). For each working state, the total current in a power switch is determined.

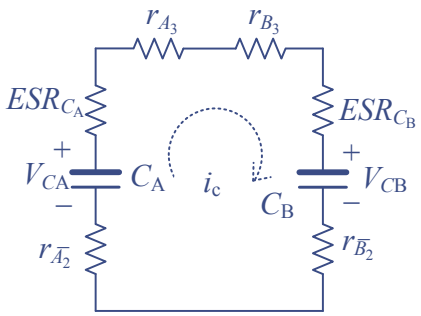


Fig. 4.11: *Pertaining to the determination of inter-capacitors current*

A summary table describing these currents is shown in Table 4.2. Peak values of these currents are:

$$i_o = \frac{V_{DC}}{R_o} \tag{4.21}$$

Where i_o is the output current, V_{DC} output voltage, R_o is the load resistance.

$$i_s^{'max} = \frac{v_s^{max}}{|\overline{Z}|} \tag{4.22}$$

$$|\overline{Z}| = \sqrt{r_s^2 + (x_L - x_c)^2} \tag{4.23}$$

Where, r_s is parasitic resistance of the inductor, x_L and x_c are the inductive reactance and capacitive reactance values.

$$i_c^{max} = \frac{\text{Specified } V_{CA} - \text{Lowest possible } V_{CB}}{R_{eq}} \tag{4.24}$$

$$i_c^{max} = \frac{V_{DC} - 0.9V_{DC}}{R_{eq}} \tag{4.25}$$

where,

$$R_{eq} = r_{\overline{A_2}} + r_{A_3} + r_{\overline{B_2}} + r_{B_3} + ESR_{C_A} + ESR_{C_B} \tag{4.26}$$

Based on these equations and Table 4.2, the maximum current for a given power switch is described and hence the current rating are determined.

4.5.2 Stored energy in passive components

The values of passive components (viz. inductors and capacitors) greatly determine the size of the power converters, which are primarily governed by the maximum current ripples and maximum voltage ripples, respectively [112]. The values of stored energies are respectively given by[113]:

$$W_{\mathrm{L}}^{\mathrm{ind}} = \frac{1}{2} L_{\mathrm{s}} (i_{\mathrm{s}}^{\mathrm{max}})^2 \tag{4.27}$$

$$W_{\mathrm{C}}^{\mathrm{cap}} = \frac{1}{2} (C_{\mathrm{A}} + C_{\mathrm{B}}) (V_{\mathrm{Cx}}^{\mathrm{max}})^2 \tag{4.28}$$

Where, the maximum voltage across capacitors $V_{\mathrm{Cx}}^{\mathrm{max}} = V_{\mathrm{DC}}$. Designing of the inductor for the proposed topology and that of[42] is the same as both are operated for five-level buck mode with 0.5 gain as seen from (4.15). Similarly, the capacitances too are same because the charging and discharging duration of the capacitors are the same as seen from (4.20). The maximum stored energy of an inductor and capacitor can be calculated by substituting (4.15) and (4.20) into (4.27) and (4.28),

$$W_{\mathrm{L}}^{\mathrm{ind}} = \frac{5}{4} \left(1 - \frac{1}{2M} \right) . W_{\mathrm{L}} \tag{4.29}$$

$$W_{\mathrm{C}}^{\mathrm{cap}} = \frac{5}{2} sin^{-1} \left(\frac{1}{2M} \right) . W_{\mathrm{C}} \tag{4.30}$$

Where,

$$W_{\mathrm{L}} = \frac{v_{\mathrm{s}}^{\mathrm{max}} . i_{\mathrm{s}}^{\mathrm{max}}}{F_{\mathrm{sw}}} \tag{4.31}$$

$$W_{\mathrm{C}} = \frac{(v_{\mathrm{s}}^{\mathrm{max}})^2}{\omega . R_{\mathrm{o}}} \tag{4.32}$$

The maximum stored energies for the proposed rectifier and that of [42] are plotted in Fig.4.12. The total maximum stored energy of the inductor in the proposed PFC rectifier and those in [42] are the same, as illustrated in Fig.4.12. It significantly decreases for the proposed

buck converter, especially for the higher modulation index. Fig.4.12 also shows that the total maximum stored energy of the capacitors C_A and C_B of both the converters increases when the gain increases. Therefore, the results presented in Fig.4.12 imply that the size of energy-storing components of the proposed converters is the same as the buck PFC rectifier proposed in [42].

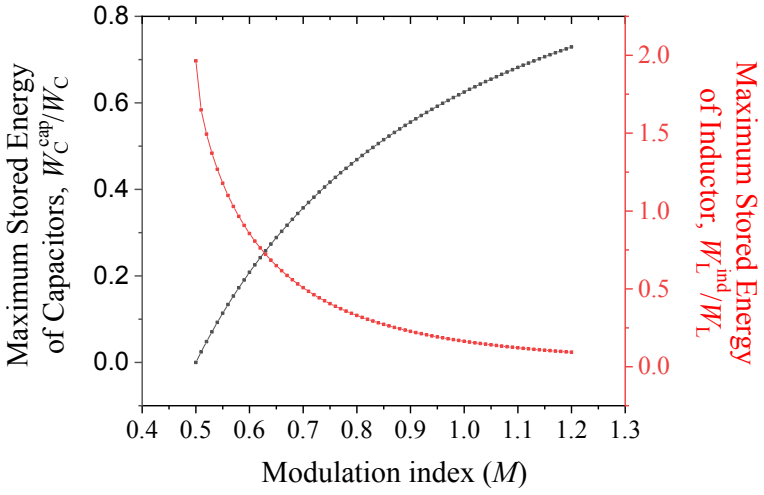


Fig. 4.12: *Total maximum stored energy of inductor and capacitors in the proposed PFC rectifier and that proposed in [42]*

4.5.3 Switching device power

As described in [114], each switching device in a PFC rectifier system must be chosen on the basis of the maximum blocking voltage across the switches and the peak and average currents passing through it. A rectifier system's voltage and current stresses are quantified in terms of the so-called Switching Device Power (SDP) [115]. The product of voltage stress and current stress is the SDP of a switching device. A rectifier's total SDP equals the sum of the SDPs of all the switching devices in the power circuit. The overall SDP is a cost indicator for a rectifier system since it estimates the total semiconductor device need [114]. These definitions are summarized as follows:

$$SDP_{\text{pk}} = \sum_{i=1}^{N_s} V_i^{\text{pk}} I_i^{\text{pk}} \tag{4.33}$$

$$SDP_{\text{avg}} = \sum_{i=1}^{N_s} V_i^{\text{pk}} I_i^{\text{avg}} \tag{4.34}$$

Where N_s is the number of semiconductors and V_i^{pk} and I_i^{pk} are their peak voltage and current stresses, respectively. The total peak and average switching device powers (SDP_{pk} and SDP_{avg}) are discussed at length in[115]. To quantify the voltage and current ratings of the switches, Table 4.2 is to be considered, which shows the voltage stress and current stress across each switch for a given state. According to [114], SDP_{pk} is used to determine the cost of converters, whereas SDP_{avg} is used to determine the semiconductors' thermal requirements and conversion efficiency.

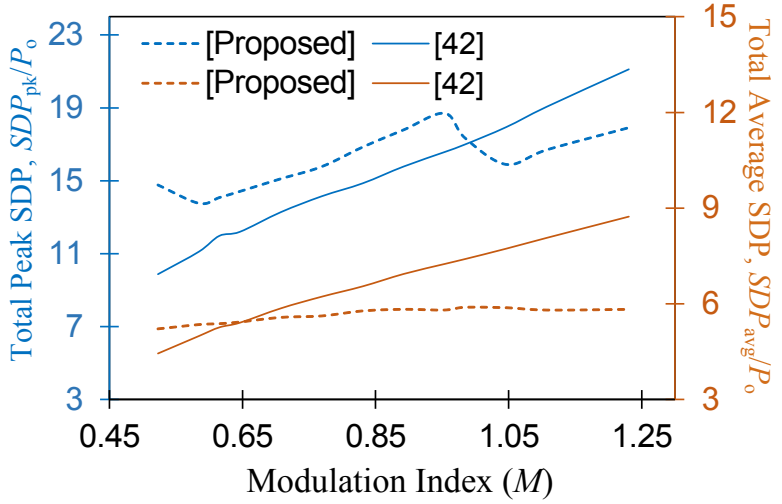


Fig. 4.13: *Total peak and average SDP for the proposed PFC rectifier and that proposed in [42]*

Both SDP_{pk} and SDP_{avg} are also calculated for the topology proposed in. Then, assuming the same output power for both the rectifiers, SDPs are plotted in Fig. 4.13 against the modulation index. As seen from Fig. 4.13, for $M < 1$ (i.e buck mode of operation of the proposed rectifier), SDP_{pk} of the proposed converter is considerably higher than that of [42]. From Fig. 4.3, for $M > 1$, boost mode of operation takes place, and the utilization of power switches is greatly reduced because the topology effectively behaves as an H-bridge converter. In the boost mode of operation, the SDP_{pk} of the proposed converter is considerably lower than that of [42]. Also, SDP_{avg} calculated for the proposed converter, is lower than in a wide range of modulation indexes. Thus, though the number of power switches in the proposed rectifier is a bit higher as compared to that of [42], the SDPs are found to be comparable.

4.6 COMPARISON WITH OTHER TOPOLOGIES

The proposed topology combines multiple dimensions, viz. (buck AC-to-DC conversion) + (multilevel power conversion) + (SCs principle). And therefore, carrying out a comparison with various other PFC topologies may not be very straight forward, as they employ one or two of the aforementioned dimensions. And hence, in this section, separate comparisons of the proposed topology with following topologies have been presented:

1. Comparison with SCs based multilevel topologies (single- and three-phase) (summarized in Table 4.3)
2. Comparison with conventional multilevel topologies (summarized in Table 4.4)
3. Comparison with bridge-less multilevel buck PFC rectifiers (which do not employ the SCs principle) (summarized in Table 4.4)
4. Comparison with some non-multilevel buck-boost PFC rectifiers (summarized in Table 4.5)

Though SCs based multilevel topologies have been studied for many years now, they have been proposed for DC-to-AC conversion. Some of the recent such topologies (both single- and three-phase) are described in [94, 116, 117], which were originally presented as inverters but can be employed as rectifiers based on (3.31). Table 4.3 shows the comparison of the proposed topology with those presented in [46, 108, 109, 118–122], in terms of crucial parameters such as[44]: number of levels (N_{L}), number of power switches (N_{s}), number of capacitors (N_{c}), number of diodes (N_{D}), PIV, voltage gain (β) and efficiency. Moreover, some other features are also discussed, such as the requirements of the DC bus capacitor, split-capacitors and possibility of extension to three phases. As can be seen from Table 4.3, the topologies presented in [118–120] synthesize five levels with lesser number of power switches than that of the proposed structure, but those in [118, 119] require power switched of high PIV (twice the DC voltage), while an additional DC link capacitor is required in [118, 120]. Topologies presented in [108, 109, 118, 121, 122] employ split-capacitors (two connected capacitors in a T-type fashion), which increases the complexity of balancing the voltages of these capacitors, especially in the rectification operation, requiring additional voltage sensors [26]. Topologies presented in [46, 108, 109] and [121, 122] respectively synthesize seven and nine levels, but are characterized

by high PIV and requirement of additional DC bus capacitors. Of these, [108, 109, 118, 121, 122] also need split-capacitors, leading to voltage balancing issues. These topologies are difficult to extend directly to three-phase structures [107]. In contrast, the proposed topology is characterized by low PIV power switches and does not require split capacitors and DC link capacitors. Also, it can be easily extended to its three-phase version by adding a leg. Thus, it shows better structural features. A comparison of the three-phase version of the proposed topology has also been shown with other three-phase SCs based multilevel topologies in Table 4.3. It can be seen that, as compared to topologies presented in [94, 116, 117], the proposed topology has a low requirement of components. Also, the presence of split-capacitors and DC bus capacitors in the topologies of [94, 116, 117] increases the controller complexity and number of voltage sensors.

In Table 4.4 , a comparison of the proposed topology with the conventional multilevel rectifiers, viz. HB [34], NPC [38] and FC[37], has been shown. As compared to the proposed rectifier, the component requirement is significantly less in these topologies, but it must be noted here that these topologies offer a unity voltage gain, and hence they function as boost rectifiers, and not buck rectifiers. Multilevel buck rectifiers have been proposed in [41–43], and they too are included in Table 4.4. MLRs are classified with respect to the output voltage, i.e., buck and boost.

A comparative analysis is done in terms of different parameters such as; N_{L}, N_{s}, N_{D}, N_{c}, PIV, in addition to the number of voltage sensors (N_{VS}), number of current sensors (N_{CS}), phase modularity and efficiency. Topology in [42] requires power switches with PIV equal to twice the output DC voltage and more number of voltage sensors. Similar is the case with topology in [43], which requires power switches with PIV equal to four times of the output DC voltage and a significantly large number of voltage and current sensors. Both these topologies possess similar limitations: difficulty in balancing of capacitors' voltages and difficulty in extension to three-phase configuration. Hence, the proposed topology manifests superior characteristics.

Table 4.5 summarizes the comparison of the proposed topology with some buck-boost PFC rectifiers [69–71, 123, 124] including the recently proposed Ferdowsi rectifiers [70]. The proposed work is based on employing capacitors to attain multilevel buck rectification, whereas the non-multilevel topologies proposed in [69–71, 123, 124] employ magnetic core(s).

Table 4.3. *A comparison of the proposed topology with some other SCs based multilevel topologies*

Topologies	N_{L}	N_{s}	N_{c}	$\mathrm{PIV}^{**}_{\mathrm{pu}}$	**Voltage Gain** (β)	**Need of DC bus capacitor(s)**	**Need of Split Capacitors**	**Efficiency** [%]
Single-phase								
[118]	5	8	2	2	2	Yes	Yes	96.80
[119]	5	9	2	2	2	No	No	98.00
[120]	5	8	2	1	2	Yes	No	97.91
[109]	7	12	2	2	3	Yes	Yes	97.70
[108]	7	12	4	4	4	Yes	Yes	97.62
[46]	7	10	2	3	3	Yes	No	96.07
[121]	9	12	2	1	2	Yes	Yes	80.61
[122]	9	11	2	1	2	Yes	Yes	NA*
Proposed	**5**	**10**	**2**	**1**	**2**	**No**	**No**	**97.50**
Three-phase								
[94]	9	36	12	4	4	Yes	Yes	98.60
[116]	13	30	8	1.5	1	yes	Yes	97.00
[117]	17	36	9	4	4	Yes	Yes	97.70
Proposed	**5**	**15**	**3**	**1**	**2**	**No**	**No**	**98.10**

∗Not available, ∗∗PIV is with respect to the DC side voltage, V_{DC}

Table 4.4. *Comparison of the proposed topology with multilevel rectifiers (single-phase)*

Parameters	Boost topologies			Buck topologies			
	HB [34]	**NPC [38]**	**FC [37]**	**CHB[41]**	**[42]**	**[43]**	**Proposed**
N_L	3	5	5	5	5	9	**5**
N_s	4	8	8	8	6	8	**10**
N_D	0	4	0	0	0	0	**0**
N_C	1	2	3	2	2	3	**2**
PIV^*_{pu}	1	1	1	1	2	3	**1**
Voltage Gain ($1/\beta$)	1	1	1	0.5	0.5	0.25	**0.5**
N_{VS}	2	2	2	3	3	4	**2**
N_{CS}	1	1	1	1	1	4	**1**
Phase modularity	Yes	Yes	Yes	Yes	No	No	**Yes**

∗PIV is with respect to the DC side voltage, V_{DC}

The comparison is carried out using the parameters of N_s, N_c and N_D, in addition to the number of magnetic cores (N_M), number of the inductors (N_{ind}), input current Total-Harmonic-Distortion (THD) and efficiency. Some other features are also discussed such as voltage stress across the switches, bidirectional capability and possibility of extension to a three-phase system. In the magnetic core-based buck rectifiers proposed in [69–71, 123, 124], voltage stress in terms of output DC voltage is very high though they require lesser number of active switches. However, the requirement of other components is significantly high in these topologies. Moreover, these topologies do not allow bidirectional flow of power and do not offer an easy possibility of implementation in three-phase systems. Hence, it can be safely concluded that the topology proposed in this work is highly competent with the considerations of buck PFC operation, bidirectional power flow, three-phase extension, voltage ratings of power switches and ease of voltage balancing of capacitors.

Table 4.5. *Comparison of the proposed topology with some non-multilevel PFC buck-boost rectifiers*

Parameters	**[69]**	**[70]**	**[71]**	**[123]**	**[124]**	**Proposed**
N_s	2	2	2	2	1	**10**
N_D	4	2	4	5	6	**0**
N_{ind}	3	3	3	3	3	**1**
N_C	3	3	3	3	2	**2**
N_M	2	2	1	3	3	**0**
Voltage stress*	High	High	High	High	High	**Low**
THD of grid current, i_s	2.60	2.00	6.55	9.70	15.80	**2.90**
Efficiency [%]	96.80	95.70	92.35	95.20	95.85	**97.50**
Bidirectional power flow	No	No	No	No	No	**Yes**
Easy extension to three-phase	No	No	No	No	No	**Yes**

*Voltage stress across switches with respect to the DC side voltage, V_{DC}

4.7 RESULTS AND DISCUSSION

For the validation of the proposed five-level rectifier and the closed loop control scheme, a laboratory setup was developed using discrete power switches (MOSFETs SiHG47N60) with Si82071AB-IS for gate driving. Hall Effect based voltage sensor (LEM LV25-P) and current sensor (HE025T01) are used to sense the output voltage and input current. A labelled photograph of the set-up is shown in Fig.4.14.

OPAL-RT OP4510 was used to generate the real time control pulses for the power switches, which was interfaced with the hardware using MATLAB/Simulink on the host computer. The controller and switching process are implemented with a sampling time of 10 micro second. Input AC is obtained from the grid as single-phase 230 VRMS, while the output DC voltage

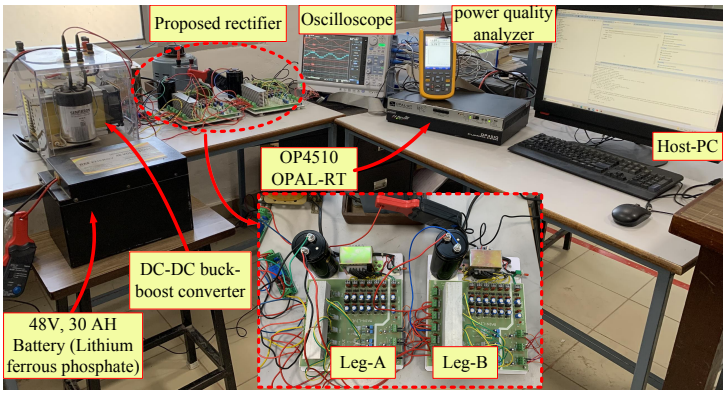
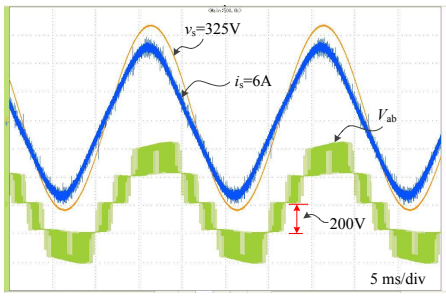
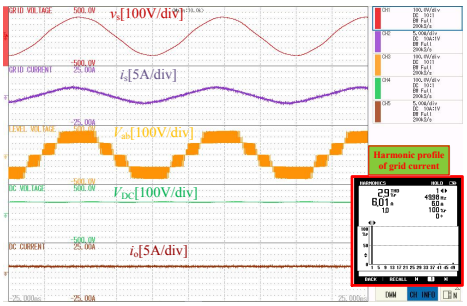


Fig. 4.14: *Photograph of laboratory set-up for validation of the proposed rectifier*

is set to 200V in buck mode of operation. Various parameters for the experimental studies are summarized in Table 4.6. Values of capacitors and inductor are chosen as per the design consideration described previously. The performance of the system is tested for both steady state and dynamic conditions (which include variations in the operating conditions, such as sudden change in DC load, sudden change in the input AC source voltage and change in the output reference voltage).



(a)



(b)

Fig. 4.15: *Waveforms pertaining to the steady-state operation of proposed rectifier*

The steady-state results are captured when the rectifier converts 325V peak AC to 200V DC (in buck mode) and supplies it to the DC load, as shown in Fig. 4.15. It can be seen that the input current (i_s) is sinusoidal and is in the same phase with the input grid voltage (v_s), indicating that the input power factor is maintained at unity. The figure also shows a five-level voltage waveform at the rectifier input with low harmonic voltage, positively impacting grid current THD. A 20Ω load is connected on the DC side and the reference output voltage is set to 200V, which is satisfactorily obtained with a tolerable voltage ripple. The voltages of capacitors C_A and C_B are balanced at 200V each, resulting in a 5-level voltage waveform of V_{ab} with levels of 0, ±200V, and ±400V.

Results related to dynamic performance are shown in Fig. 4.16. As can be seen in Fig. 4.16a, when the output current is increased suddenly by 50% (by changing the load resistance from

Table 4.6. *Various parameters/ items for the experimental set-up*

Parameters	**Value**
Input voltage (v_s)	230 VRMS
Grid frequency (f_{ref})	50 Hz
Output DC voltage (V_{DC})	200V
Switching frequency (F_{sw})	10 kHz
Switched capacitor (C_A, C_B)	1600 uF
Filter inductor (L_s)	4 mH
Semiconductor switches	MOSFETs SiHG47N6
Gate driver IC	Si82071AB-IS
Voltage sensor	LEM LV25-P
Current sensor	HE025T01
EV Battery details	48V, 30Ah, Lithium ferrous phosphate type
Oscilloscope	Yokogawa DL950 with 10:1 probes

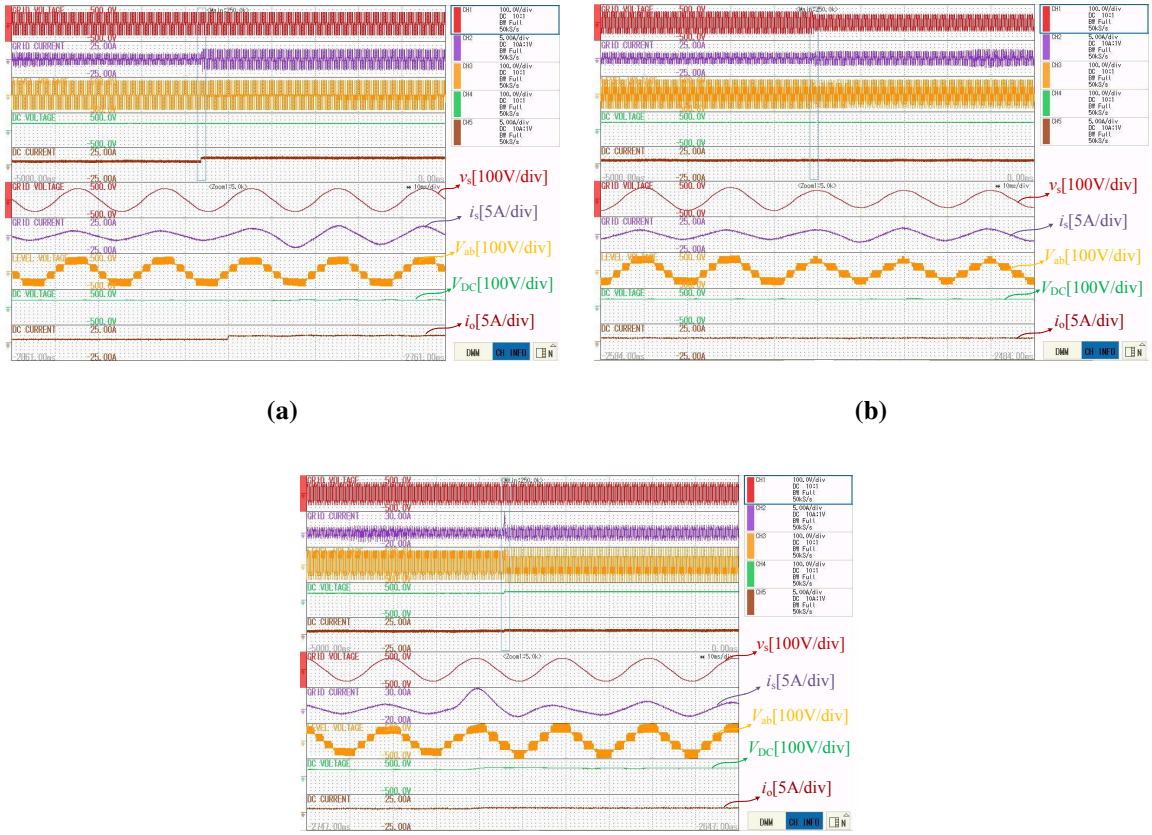
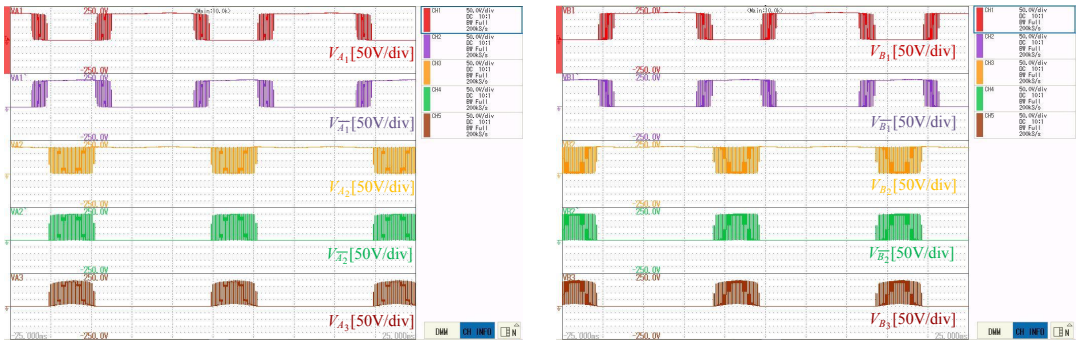


Fig. 4.16: *Experimental results for dynamic performance: (a) sudden change in load; (b) variation in input voltage; and (c) 20% rise in the output DC voltage reference*

40Ω to 20Ω), the load voltage quickly stabilizes at 200V and the rectifier is still in unity power factor mode. In another instance, the DC side power consumption ($V_{DC}.i_o$) is not changed, but v_s is suddenly decreased, and it is seen that the grid current i_s is increased proportionally and unity power factor is maintained, as shown in Fig. 4.16b. When the AC grid voltage is suddenly decreased by 25% without any change in load, then the current drawn from the grid stabilizes instantaneously to a proportionate value. The voltages of DC capacitors are not affected by the voltage sag in the grid. In another scenario, shown in Fig. 4.16c, when the output DC reference voltage is changed by 20%, it causes V_{DC} and i_o to change and the load voltage stabilizes at 240V as desired. These results also validate the tracking accuracy of the controller. Under increased output voltage, the converter continues to operate with a unity power factor and with five voltage levels at the input of the rectifier. The voltage waveforms across the switches are shown in Fig. 4.17 and as expected, it can be seen that they are limited to a value equal to the output DC voltage.



(a) **(b)**

Fig. 4.17: *Waveforms of voltages across the power switches when the output voltage is 200V*

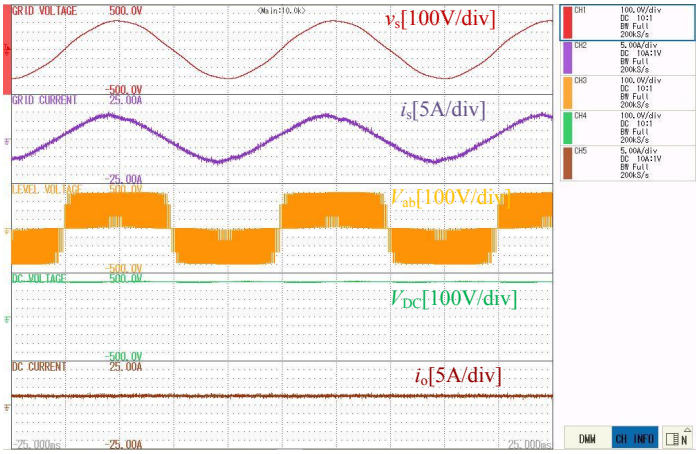
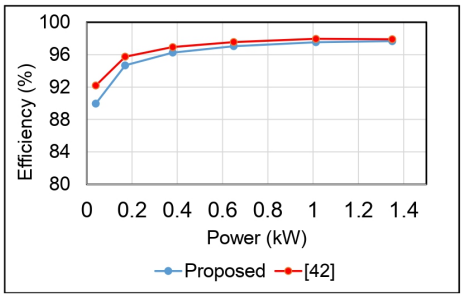


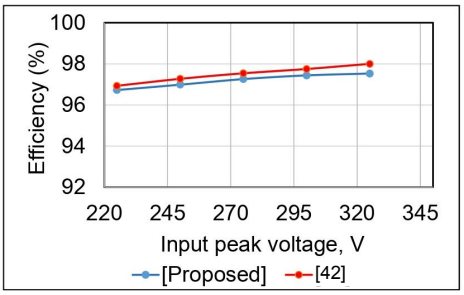
Fig. 4.18: *Experimental waveforms for steady state boost mode of operation of the proposed rectifier*

The steady-state results are also captured when the rectifier converts 325V peak AC to 400V DC (in boost mode) and supplies it to the DC load, as shown in Fig. 4.18. It can be seen that the input current (i_s) is sinusoidal and is in the same phase with the input grid voltage (v_s), indicating that the input power factor is maintained at unity. The Fig. 4.18 also shows a three-level voltage waveform at the rectifier input.

The efficiency, THD and Power Factor (PF) are calculated for the proposed work and comparisons are made with the topology proposed in [42], which has been previously discussed to be a five-level rectifier. The operating conditions for obtaining the efficiency curves for both the topologies are same, viz. input AC voltage of 325 v_s^{max}, output DC voltage 200V and carrier frequency 10 kHz. Now, it can be noticed from Fig. 4.19 below that the proposed topology



(a)



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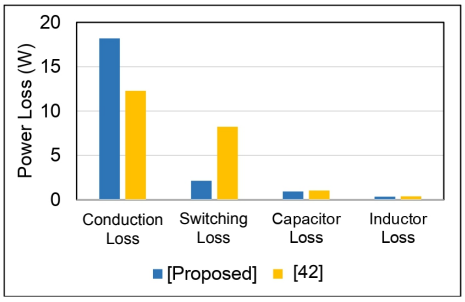
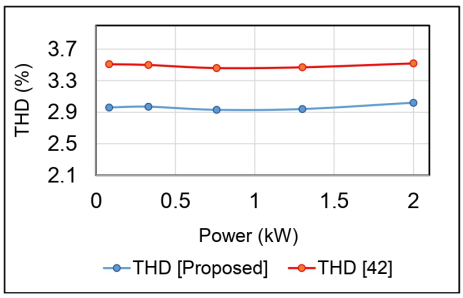
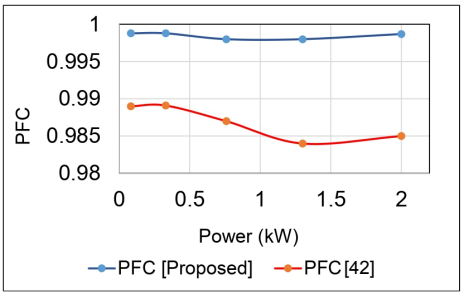


(c)

Fig. 4.19: *Efficiency comparison with existing buck PFC rectifier: (a) curves with respect to power; (b) curves with respect to input voltage; and (c) distribution of power losses*



(a)



(b)

Fig. 4.20: *Comparison with existing buck PFC rectifier: (a) THD curves with respect to power; and (b) PFC curves with respect to power*

shows slightly lesser efficiency, but at the same time, if a further comparison is carried out in terms of THD (versus power) (Fig. 4.20a) and PF) (versus power) (Fig. 4.20b) for the topologies, then the proposed topology exhibits much better performance on these parameters. Thus, the

peak efficiencies are differing slightly, which are 97.5% and 98% respectively for the proposed topology and [42] (mainly due to inter-capacitor currents in the proposed topology and lower number of power devices in [42]). It is observed that proposed rectifier yields lower THD and higher PF as compared to [42].

4.8 THREE-PHASE EV CHARGING

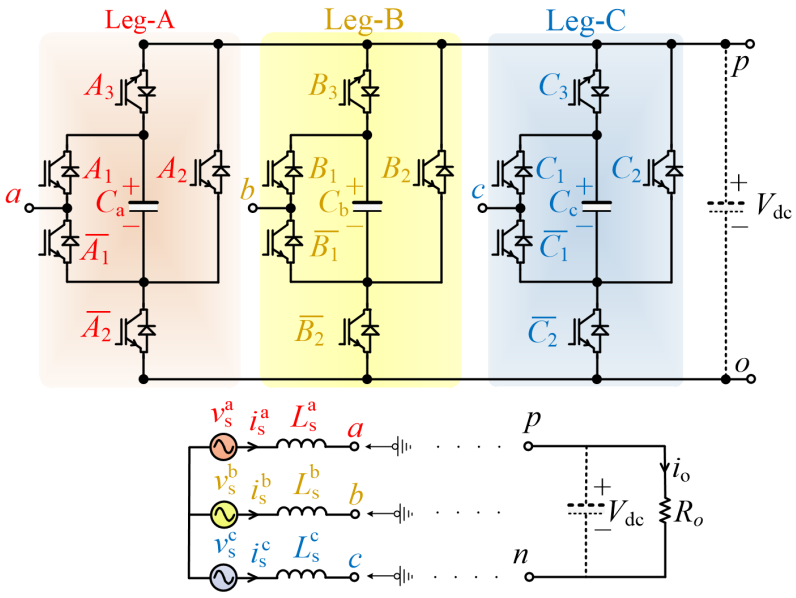
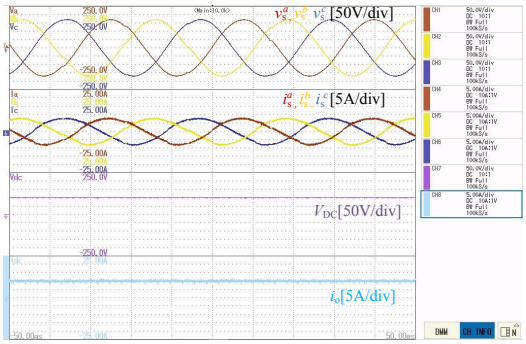


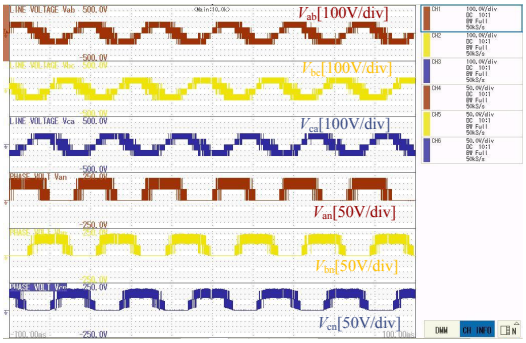
Fig. 4.21: *Three-phase version of the proposed buck PFC rectifier*

Due to phase modular structure of the proposed topology, it can be easily extended to its three-phase version. This is achieved by adding a third leg which too carries a switched capacitor and five power switches, as shown in Fig. 4.21.

Here too, a buck output voltage is obtained with UPF operation at the input. Experimental results for the three-phase MLR are shown in Fig. 4.22a, with the input AC voltage of 120 VRMS, 50 Hz and the output DC voltage being 100V. The rated power is 1 kW. Fig. 4.22b shows the line voltages with five levels (of step size 100V) corresponding to the phases a, b and c with 120° phase shift, and also the three-level pole voltages which too are phase-shifted from one another by 120°. This phase voltage generates five-level as a line voltage.



(a)



(b)

Fig. 4.22: *Experimental waveforms for the proposed three-phase buck rectifier: (a) grid voltage, grid current, DC voltage and current; and (b) line voltages and pole voltages*

4.9 CONCLUDING REMARKS

This chapter presents a new multilevel single/three-phase buck PFC rectifier based on SCs suitable for EV charging with bidirectional operation. The voltage is balanced using LSPWM and a voltage and current controller. The performance of the single-phase AC input of 230 V and DC output of 200 V for various dynamic situations has been tested using a proto-model implementation. The following observations are made from this study:

- In this proposed SC-based rectifier, the value of β is 2. It works as a buck rectifier with power factor correction, while providing a wide output range.

- It synthesizes five levels at the input side, thereby greatly improving the harmonic profile of the waveform. For all the switching states, one of the switched capacitor is in parallel with the load terminal and hence no additional filter capacitor is required at the DC output.

- It does not require any additional balancing circuitry since the capacitors are self-balanced. Moreover, the voltage of only one of the switched capacitor is required to be sensed to implement a closed loop control.
- It allows bidirectional flow of power, and hence it can be employed to implement a V2G interface for EV charging.
- Due to phase modular structure it can be easily extended to a three-phase version.
- It acts as a boost rectifier for low modulation indices (<0.5). Although in this case, it synthesizes only three levels at the input terminals.
- It achieves an efficiency of 97.50%, low THD and high power factor compared to the conventional multilevel rectifier.

Chapter–5

Bidirectional Seven Level Buck PFC Rectifier

In order to further increase the number of levels and voltage gain, two seven-level rectifiers with voltage gain of three are conceptualized in this chapter. The first of these seven-level topologies use highly reduced number of components, but a few of the power switches experience a voltage stress equal to thrice the output DC voltage, and hence it is not extended to its three-phase version. The second seven-level topology uses power switches with equal voltage stress and is highly modular, and hence it is investigated for three-phase operation too. The working principle, modulation strategy and applications of the proposed topologies have been discussed and are validated through experimental results.

5.1 GENERAL

The grid-connected voltage source rectifier produces a multilevel voltage at the input terminal to regulate the flow of current in the grid. Increasing the number of voltage levels enhances the quality of the synthesized voltage, leading to an improvement in grid current. Additionally, MLRs provide alluring benefits, such as utilizing power switches of reduced voltage ratings, yielding significantly improved harmonic profile of the input waveform, resulting lower dv/dt stress, and the possibility of fault-tolerant operation. These benefits make MLRs a highly attractive option

The contents of this chapter are partly published in:

* "A V2G-enabled Seven-level Buck PFC Rectifier for EV Charging Application," in 24^{th} *European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), Hanover, Germany, 2022*
* "A V2G Enabled Bidirectional Single/Three-Phase EV Charging Interface Using Modular Multilevel Buck PFC Rectifier," in *Electronics 2022*, vol. 11, no. 12, 1891, 2022. https://doi.org/10.3390/electronics11121891

for those seeking to optimize the performance of their power system. As the β factor increases, it improves the range of output voltage in a buck mode with a better harmonic profile. Moreover, the number of levels increases with this factor. In this chapter SCs-based rectifier generates 7-level at the input terminal and the value of β is 3.

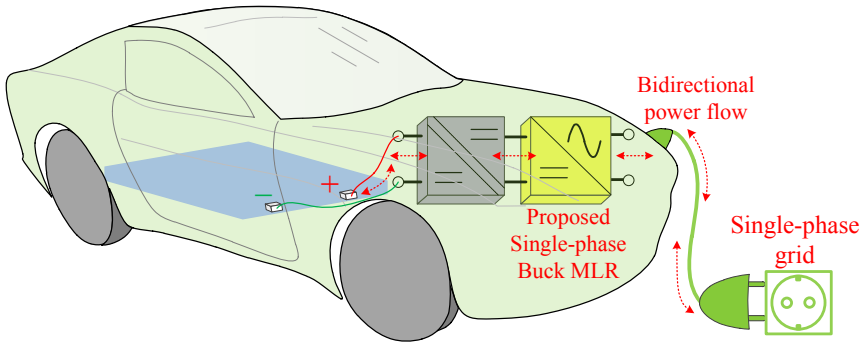


Fig. 5.1: *Schematic diagram of the proposed charging system*

This chapter is focused on V2G enabled bidirectional single-phase on-board and three-phase off-board EV charging system. The design and development of this work can charge the vehicle battery as well as offer active power support to the utility grid as described in this chapter [125]. Fig. 5.1 depicts a schematic diagram of the single-phase charging system.

The difference between the existing and proposed work with input AC and output DC voltage is depicted in Fig. 5.2. The power electronics interfaces for EV charging systems can support batteries ranging from 48V (e-bikes) to 800V (PHEV) [28], with the ability to charge the battery in both constant current and constant voltage modes, depending on the battery's SOC. A bidirectional conventional multilevel PFC converter operates in boost mode for charging (i.e., rectifier) and buck mode for discharging (i.e., inverter). For G2V application power need to flow from high AC grid voltage to low DC battery voltage. So, in the first stage of EV charging, there is no need to use a boost AC-DC rectifier. Moreover, for V2G, low EV battery voltage connects with high AC grid voltage. In that instant also, there is no need to use a buck inverter. This use is responsible for the requirement of a high voltage step-up and step-down DC-DC converter and high voltage DC-bus capacitor. A power flow of V2G enabled EV charging system with conventional and proposed PFC rectifier shown in Fig. 5.3.

In the case of three-phase boost rectifiers (e.g., the conventional active rectifier comprising three legs of complementary power switches) with an input voltage of 415 V RMS, the output

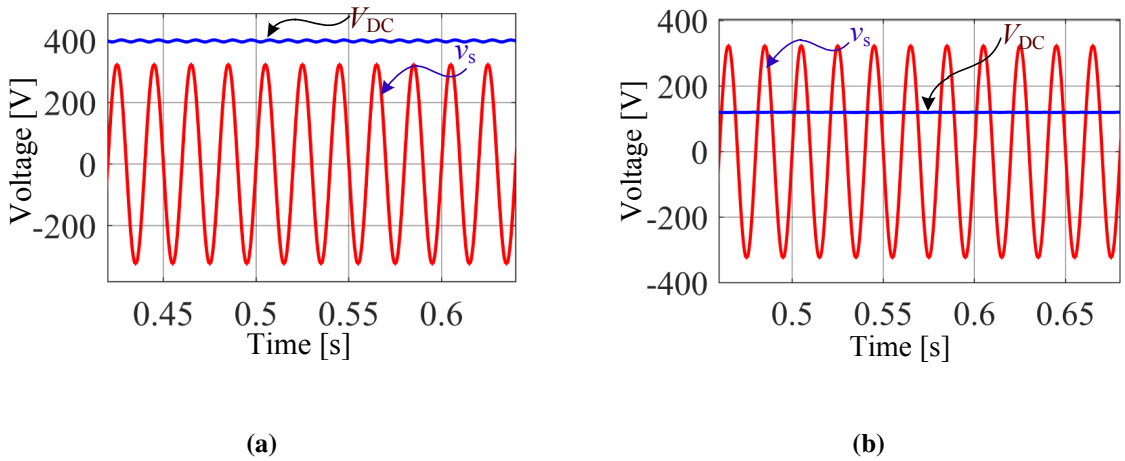


Fig. 5.2: *The basic difference in terms of input and output voltage between (a) existing MLRs topologies and (b) proposed MLR topology*

voltage ranges from 700 V_{DC} to 800 V_{DC}, which is too high to directly feed the DC-bus of EVs. In the second stage, a DC-to-DC step-down converter is required to reduce this voltage to a nominal voltage suitable for EV battery charging [28].

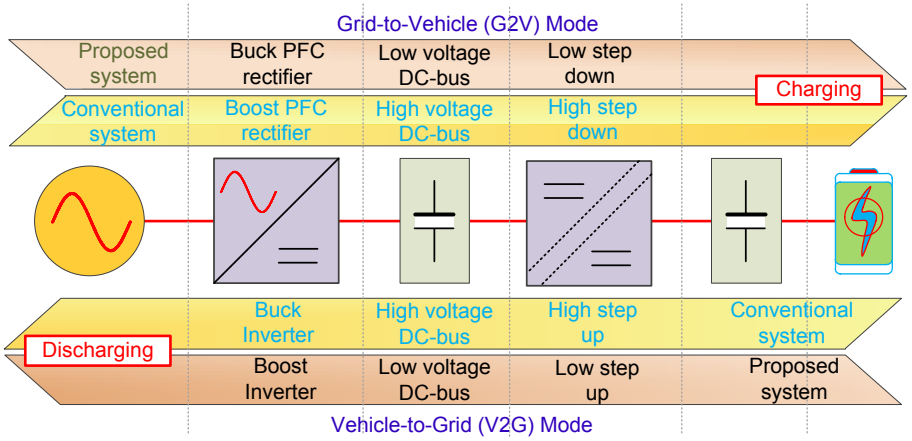


Fig. 5.3: *Basic power flow in V2G enabled charging system and comparative effects on conventional and proposed AC-DC rectifier*

The proposed topology, voltage and current controller, and LSPWM approach for producing gate pulses are all described in great depth. To verify the suggested work, experimental testing is carried out under steady-state and transient conditions.

5.2 SINGLE PHASE SEVEN LEVEL BUCK RECTIFIER TOPOLOGY

In the proposed V2G enabled single phase seven-level buck PFC rectifier the following properties to address these concerns:

1. It achieves a unity power factor and works as a V2G and G2V application.
2. On the input side, it synthesizes seven levels, greatly increasing the harmonic profile.
3. Ten switches, two SCs, and one DC link capacitor is required.
4. There is a need to balance only one DC-link capacitor voltage, the others are balanced by themselves without the use of complicated controlling methods.
5. It operates in buck mode, giving it a wide output range.
6. It works in CCM, which means no huge filters are required.
7. Six of ten switches have low peak inverse voltages that are the same as the DC-link voltage, and four switches have peak inverse voltages that are three times the DC-link voltage.

5.2.1 Circuit topology

The seven-level bidirectional buck rectifier, as illustrated in Fig. 5.4, is made up of two H-bridges with two additional switches that link to two capacitors. By switching, connecting the two capacitors C_1 and C_2 in parallel and/or series with the DC bus capacitor represents the charging and discharging states. The operations '1' and '0' denote the ON and OFF states of the relevant switch, respectively; 'C' and 'D' represent the charging and discharging states of the capacitors are shown in Table 5.1.

The front-side H-bridge comprises four transistors S_1, $\overline{S_1}$, S_2 and $\overline{S_2}$ are responsible for converting AC to inverted multilevel voltage. Because the bus voltage V_{bus} can be three distinct DC levels of $+V_{\text{DC}}$, $+2V_{\text{DC}}$, and $+3V_{\text{DC}}$, the front-side H-bridge can create seven different voltage levels at the terminals 'a' and 'b' that represents as V_{ab}, namely 0,$+V_{\text{DC}}$, $+2V_{\text{DC}}$, and $+3V_{\text{DC}}$. This H-bridge has voltage stress of $3V_{\text{DC}}$. The load-side of the seven-level rectifier has two essential

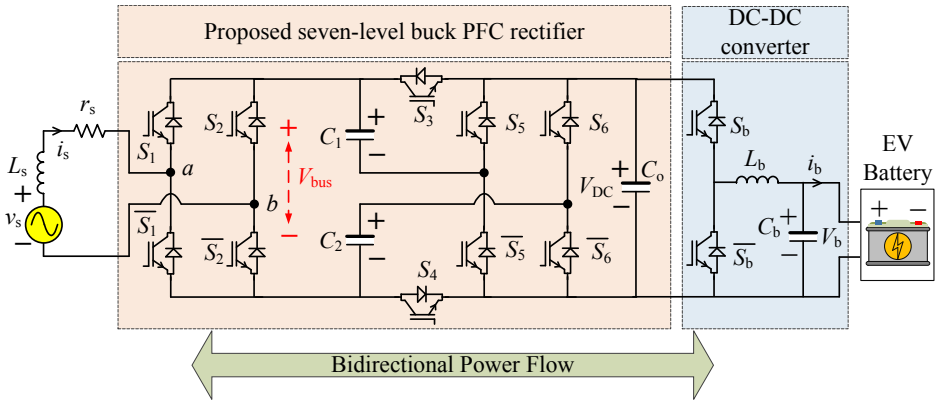


Fig. 5.4: *Single-phase seven-level buck PFC topology for bidirectional power flow*

Table 5.1. *Switching states of proposed single-phase topology*

States	i_s	V_{ab}	Power Switches						Capacitors		
			S_1	S_2	S_3	S_4	S_5	S_6	C_1	C_2	C_3
T_1	$i_s > 0$	$+3V_{DC}$	1	0	0	0	1	0	C	C	C
T_2	$i_s > 0$	$+2V_{DC}$	1	0	1	0	0	0	D	C	C
T_3	$i_s > 0$	$+V_{DC}$	1	0	1	1	0	1	D	D	C
T_4	$i_s \geq 0$	0	1	1	1	1	0	1	D	D	D
T_5	$i_s \geq 0$	0	0	0	1	1	0	1	D	D	D
T_6	$i_s < 0$	$-V_{DC}$	0	1	1	1	0	1	D	D	C
T_7	$i_s < 0$	$-2V_{DC}$	0	1	0	1	1	1	C	D	C
T_8	$i_s < 0$	$-3V_0$	0	1	0	0	1	0	C	C	C

features. One advantage is that all components can bear the same low voltage stress V_{DC}, which is advantageous for high-frequency operation. Another difference is that the two capacitors C_1 and C_2 perform the same function to create distinct output levels and balance the same voltage $+V_{DC}$ (i.e., V_{C1}=V_{C2}=V_{DC}).

Various switching states for the proposed rectifier are described herewith:

1. State T_1 and T_8 (V_{ab} = $+3V_{DC}$): During this state, in the positive half cycle, the switches S_1, $\overline{S_2}$, S_5 and $\overline{S_6}$ are turned ON. In the path shown in red, it can be seen that the capacitors C_1, C_2 and C_o are in series with the AC source, such that the voltage V_{ab}=($+V_{C1}$+V_{C2}+V_{DC})=$+3V_{DC}$. Moreover, during the negative half cycle, the switches

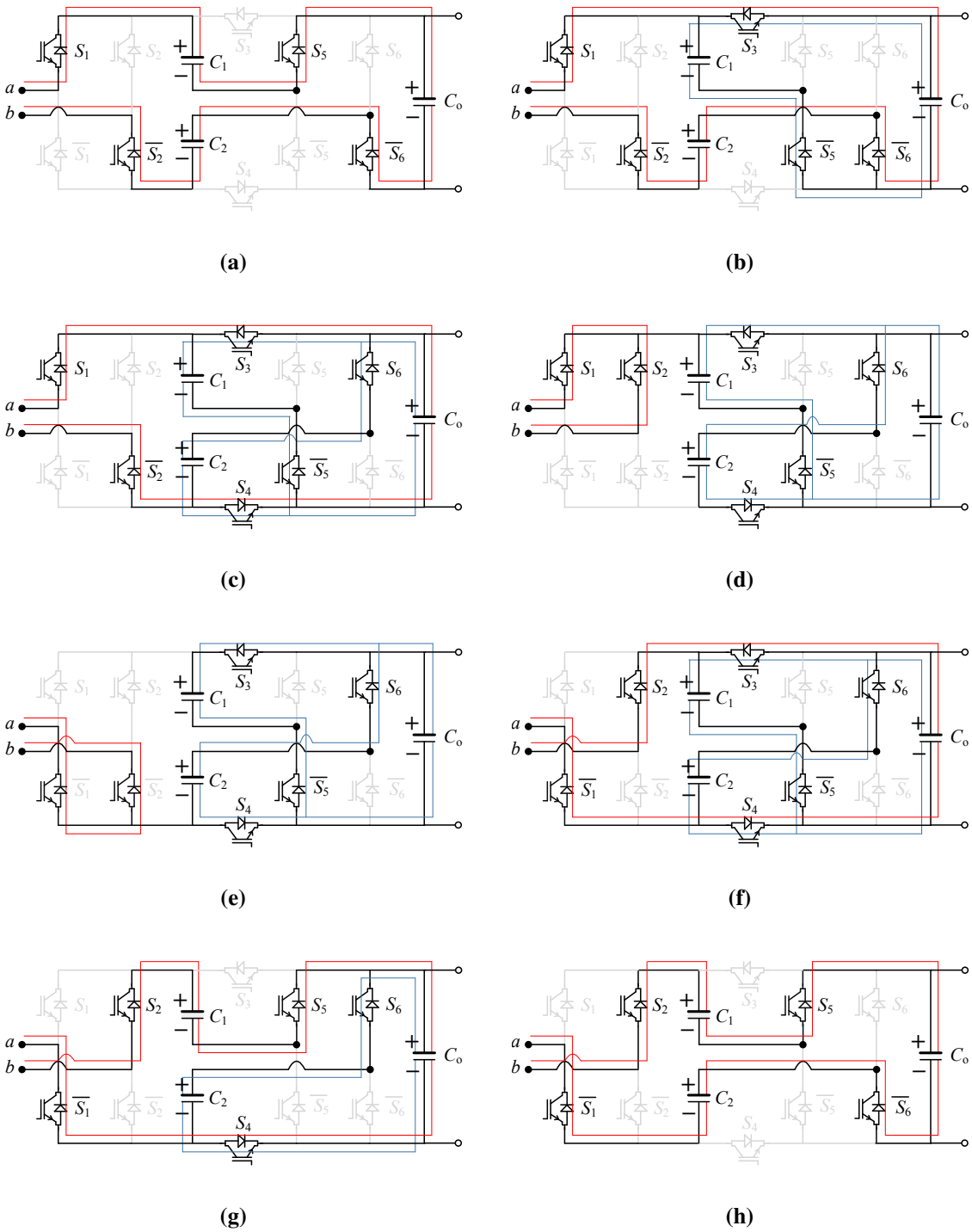


Fig. 5.5: *Switching states for the proposed seven-level buck rectifier*

$\overline{S_1}$, S_2, S_5 and $\overline{S_6}$ are turned ON, such that V_{ab}=($-V_{C1}-V_{C2}-V_{DC}$)=$-3V_{DC}$. In both states, all capacitors are charged as shown in Fig. 5.5a and 5.5h.

2. State T_2 and T_7 (V_{ab} = $+2V_{DC}$): During this state, in the positive half cycle, the switches S_1 , $\overline{S_2}$, S_3 , $\overline{S_5}$ and $\overline{S_6}$ are turned ON. In the path shown in red, it can be seen that the capacitors C_2 and C_o are in series with the AC source, such that the voltage V_{ab}=$+V_{C2}+V_{DC}$=$+2V_{DC}$. Moreover, during the negative half cycle, the switches $\overline{S_1}$, S_2, S_5 and S_6 are turned ON, such that V_{ab}=$-V_1-V_{DC}$=$-2V_{DC}$. In-state T_2 capacitors C_2 and C_o are charged and C_1 is discharged to the load. Furthermore, in-state T_7, C_1 and C_{DC} are charged and C_2 is discharged. Discharging path is shown in blue as shown in Fig. 5.5b and 5.5g.

3. State T_3 and T_6 (V_{ab} = $+V_{DC}$): During this state, in the positive half cycle, the switches S_1, $\overline{S_2}$, S_3, S_4, $\overline{S_5}$ and S_6 are turned ON. In the path shown with red, it can be seen that the capacitors C_o is in series with the AC source, such that the voltage V_{ab}=$+V_{DC}$. Moreover, during the negative half cycle, the switches $\overline{S_1}$, S_2, S_3, S_4, $\overline{S_5}$ and S_6 are turned ON, such that V_{ab}=$-V_{DC}$. In states T_3 and T_6 capacitors C_o charged and C_1, and C_2 are discharged to the load as shown in Fig. 5.5c and 5.5f.

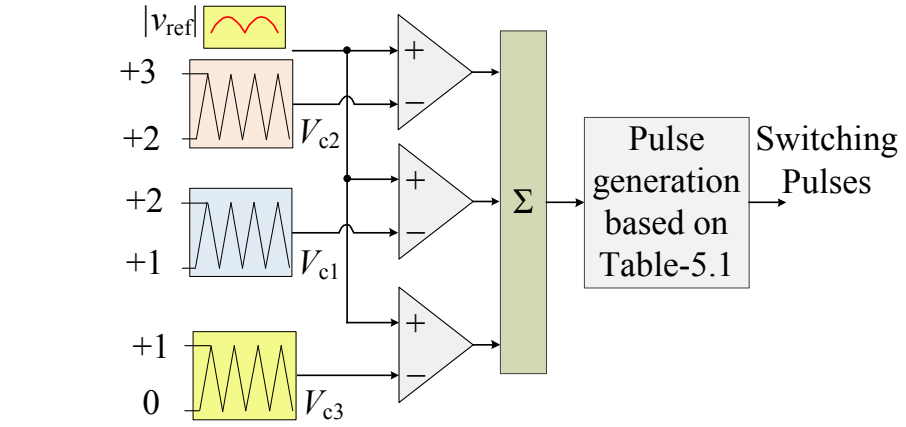
4. State T_4 and T_5 (V_{ab} = 0): During this state, in the positive half cycle, the switches S_1, S_2, S_3, S_{14}, $\overline{S_5}$ and S_6 are turned ON. In the path shown in red, it can be seen that not any capacitors are in series with the AC source, such that the voltage V_{ab}=0. Moreover, during the negative half cycle, the switches $\overline{S_1}$, $\overline{S_2}$, S_3, S_4, $\overline{S_5}$ and S_6 are turned ON, such that V_{ab}=0. In states T_4 and T_5 all capacitors are self-balanced and discharged to the load as depicted in Fig. 5.5d and 5.5e.

The modulation approach for generating the gate pulses for the switches and the reference signal created by a suitable controller is detailed in the next section.

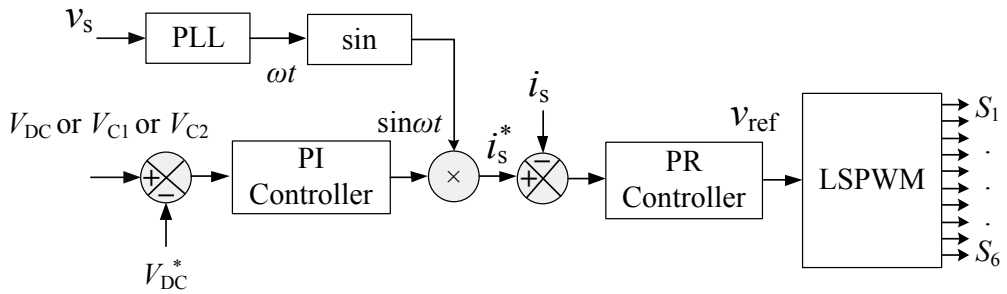
5.2.2 Modulation scheme and suitable controller

Several modulation approaches, such as multicarrier PWM and space vector modulation, can be utilized to control the output voltage of the proposed MLR. The proposed MLR is demonstrated in this part using the LSPWM approach, as seen in Fig. 5.6a. Four high-frequency level-shifted

carrier signals and reference signals produced by the controller were employed in the single-phase [126].



(a)



(b)

Fig. 5.6: *Modulation and control strategy (a) level-shifted pulse width modulation for generating switching pulses (b) output voltage and PFC controller*

In the proposed system cascaded PI and PR controllers are respectively used to control the DC voltage output (V_{DC}) and the grid current (i_s), thereby providing a regulated buck DC output voltage and UPF at the input side. The key benefit of this proposed SC-based rectifier is that control of any one of the capacitor voltages automatically balances the voltages of the remaining capacitors. The block diagram of the implemented controller is shown in Fig. 5.6b. A PLL extracts the voltage angle and generates the synchronized current reference. The outer loop of the cascaded controller is used to regulate the voltage whose output goes to the current controller (inner loop) as the reference signal. Using the PI controller, DC voltages across the capacitors are regulated to DC voltage reference (V_{DC}^*) [127], [81]. The current controller can

be a simple gain proportional controller or a PI controller, with the inner loop having a faster dynamic than the outer loop. As a result, when using a PI controller to manage a sinusoidal input current signal, the PI's integral gain should be small enough not to affect the inner loop's speed. However, when a PI compensator is applied to a sinusoidal signal, it causes steady-state errors that appear as a DC component in the current harmonic spectrum. One approach for such a situation is to use a PR controller with an infinite gain at the fundamental grid frequency.

5.2.3 Results and discussion

A laboratory setup was established using discrete power switches MOSFETs and a suitable gate driver IC to assess the proposed buck rectifier and closed-loop control. The output voltage and input current are sensed using a Hall Effect-based voltage sensor and current sensor. The MOSFET gate pulses are generated by the OPAL-RT OP4510, which interfaces to the hardware through MATLAB/ Simulink on the host computer. A 10-microsecond sample time is used to construct the controller and switching mechanism. A single-phase 230V RMS AC input is employed in buck mode, with 120V as a DC output. Experimental results are taken for the resistive load and battery. Both steady-state and dynamic situations are used to evaluate the system's performance. A sudden shift in resistive DC load, reference voltage and grid voltage are examples of operating condition variations. Moreover, sudden change in battery performance from charging (i.e., G2V) to discharging mode (i.e., V2G).

The experimental results are based on two scenarios: one with an EV battery and another with resistive load. The steady-state results are produced when the rectifier converts 325V single-phase peak AC to 120V DC (in buck mode) and is further connected to the DC-DC buck converter to the EV battery. Fig. 5.7 shows the steady-state condition when the battery is in charging condition. Whereas, a seven-level voltage (V_{ab}) is generated at the point of the input terminal of the rectifier, the bus voltage (V_{bus}), and all other capacitors voltages.

To demonstrate applicability in single-phase charging, a power electronics interface consisting of the proposed PFC rectifier and a conventional bidirectional buck-boost DC-DC converter is built. The battery's voltage and current are 48V and 20A, respectively. Fig. 5.8 shows the waveforms of the battery charging, which show that the grid voltage and current are in phase.

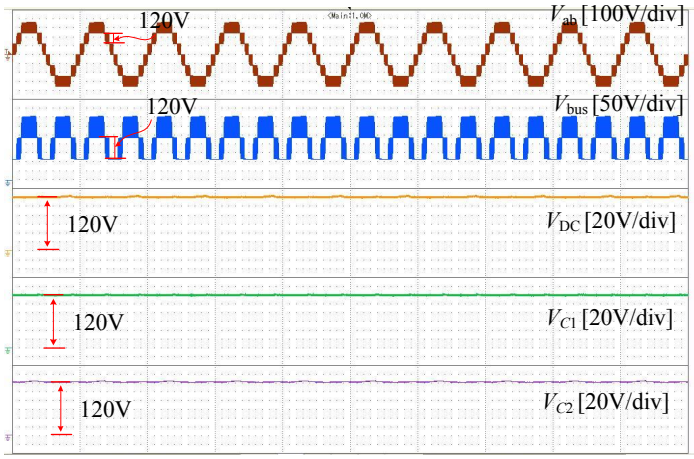


Fig. 5.7: *Steady-state condition with level voltage (V_{ab}), bus voltage (V_{bus}) and all capacitors' voltages*

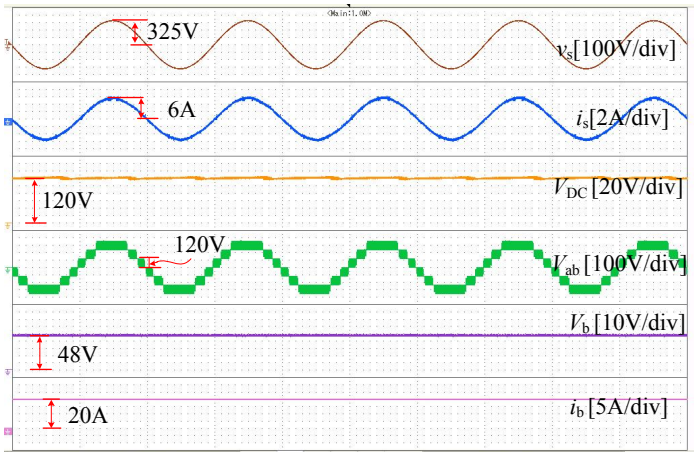


Fig. 5.8: *Steady-state response in battery charging with unity power factor, battery voltage and current*

The output voltage of the rectifier is set to 120V DC and then regulated to 48V using a DC-DC converter. The V2G mode allows battery energy to be injected back into the grid. EVs can use G2V charging and V2G discharging modes. To use V2G mode, the interface must be capable of bidirectional power flow. In its single-phase variations, the proposed topology facilitates both charging and discharging. Fig. 5.9 presents the analysis of the dynamic response, showcasing the transition from G2V (charging) mode to G2V (discharging) mode. During this transition, the battery current is controlled. When there is a positive battery current, power flows from the Grid to the vehicle, and both voltage and current are in phase at 0 degrees. Conversely, when there is a negative battery current, power flows from the vehicle back to the grid, and in this case,

the current direction is reversed, maintaining a phase with voltage at 180 degrees. Throughout both scenarios, the DC link voltage remains constant, ensuring the maintenance of seven voltage levels at the terminals.

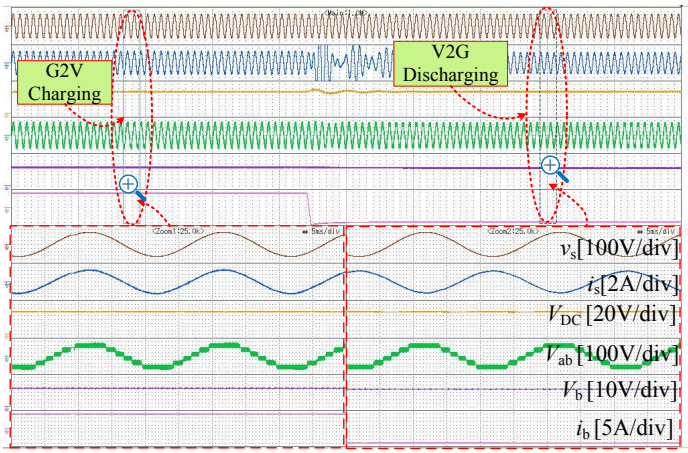


Fig. 5.9: *Sudden change in G2V charging to V2G discharging mode*

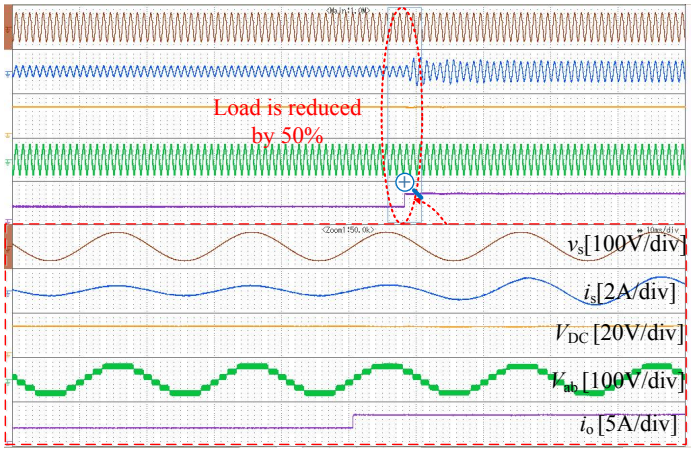


Fig. 5.10: *Transients response with resistive load; Sudden decrease in load by 50%*

The proposed rectifier's dynamic performance is validated by resistive load experimentation. A 50% load rapidly decreases, as result doubling the load current and instantaneously stabilizing the load voltage at 120V. Furthermore, as seen in Fig. 5.10, the rectifier maintains a power factor of unity. In another case grid voltage suddenly reduces by 20% as shown in Fig. 5.11, as results all other voltages and currents are stable instantaneously and achieve an unity power factor. In a different case, depicted in Fig. 5.12, if the output DC reference is increased by 120 to 160, V_{DC} and i_o will also vary, and the load voltage will settle at 120V to 160V as expected. These outcomes validate the controller's tracking ability. The

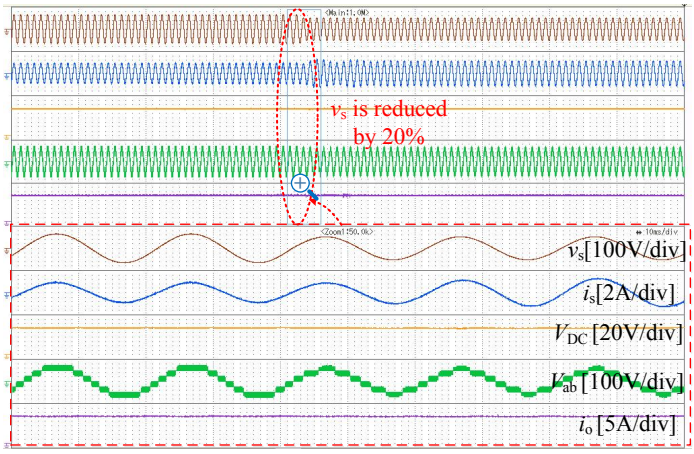


Fig. 5.11: *Transients response with resistive load; sudden decrease in grid voltage by 20%*

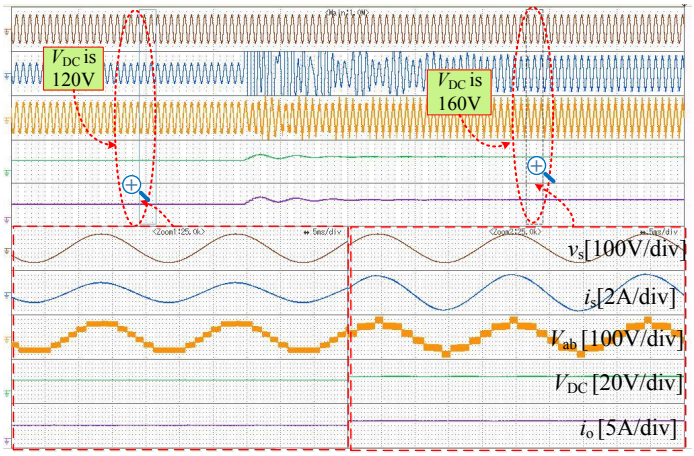


Fig. 5.12: *Transients response with resistive load; sudden increase in reference voltage from 120V to 160V*

converter maintains a unity power factor and seven voltage levels at the rectifier's input even when the output voltage is raised.

5.3 SEVEN LEVEL THREE PHASE TOPOLOGY

The proposed SCs-based MLR topology has been implemented as a single or three phase seven-level converter, though it is highly modular and can be easily scaled up. The typical voltage ranges in the conventional and proposed topologies are also indicated in Fig. 5.13, considering an input three-phase AC supply with an RMS value of 415 V. It can be seen that

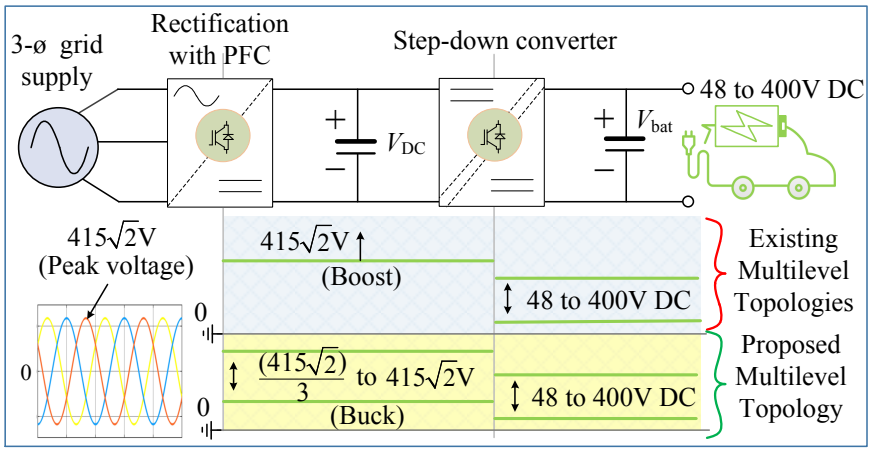


Fig. 5.13: *A general representation of voltage levels in two-stage EV charging interface with the conventional and proposed rectifier topologies*

with a step-down factor of 3, the output voltage of the proposed rectifier can be regulated in the range of 195 V to 587 V.

5.3.1 Circuit Topology

The proposed single/three-phase Switched-Capacitor-based Multilevel Rectifier (SCMR) is shown in Fig. 5.14. All three phases have a similar power circuit configuration, and an AC line voltage source powers them. The DC-bus capacitor, C_o supply to the load where the capacitor voltage is to be balanced at V_{DC}. Each phase of the proposed rectifier has two SC units inserted. The SC units consist of eight switches and two capacitors. At the input terminals of the rectifier, the proposed structure generates four levels as the pole voltage, and it synthesizes seven levels in the line voltages.

In each phase, three pairs of complementary power switches and one pair required the same gate pulse, which is to say, if '1'refers to ON state of a switch and '0'refers to the OFF state, the switching functions (where, x ∈ a, b, c) are:

$$\overline{S_{x2}} = 1 - S_{x1} \tag{5.1}$$

$$\overline{S_{x4}} = 1 - S_{x3} \tag{5.2}$$

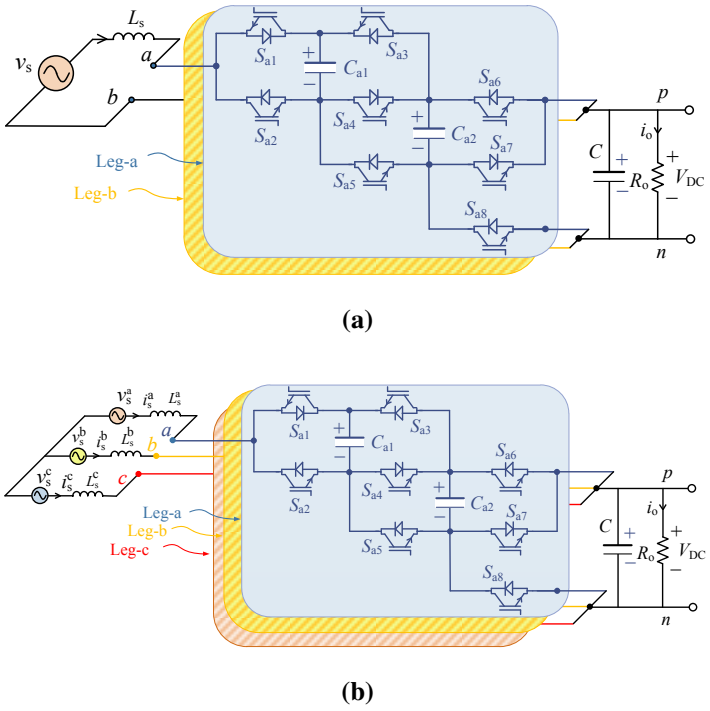


Fig. 5.14: *Proposed PFC rectifier topology with the capability of bidirectional power flow (a) single phase (b) three phase*

$$\overline{S_{x7}} = 1 - S_{x6} \tag{5.3}$$

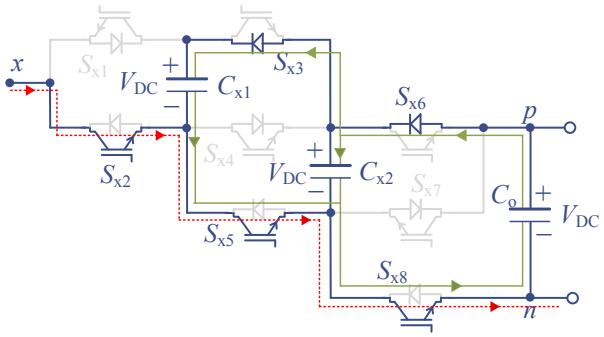
$$S_{x5} = S_{x8} \tag{5.4}$$

Each phase thus generates four levels in the voltage (V_{xn}, x ∈ a, b, c) 0, $+V_{DC}$, $+2V_{DC}$ and $+3V_{DC}$. The switching states of the proposed rectifier are shown in Table 5.2. Where the switch ON and OFF represents 1 and 0. Capacitors C_{x1}, C_{x2} and C_o are to be maintained at a voltage equal to V_{DC}. At the point of the input terminal, the voltage V_{xn} can be expressed as:

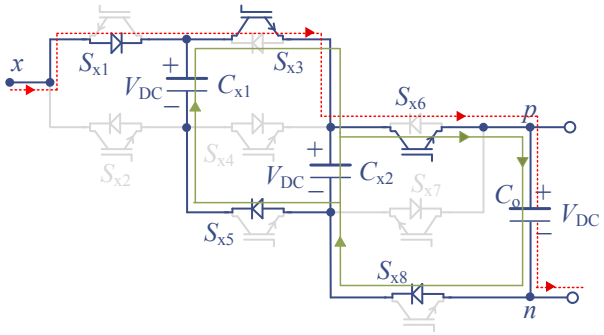
$$V_{xn} = (S_{x1} + S_{x4} + S_{x7})V_{DC} \tag{5.5}$$

Various switching states for the proposed rectifier are described herewith:

1. State 1 ($V_{xn} = 0$): During this state, the switches S_{x2}, S_{x3}, S_{x5}, S_{x6} and S_{x8} are turned ON, so as to achieve two simultaneous conduction paths, as shown in Fig. 5.15a. In the path shown with red, it can be seen that all capacitors are bypassed, such that the voltage $V_{xn} = 0$. Additionally, for the path shown in green, the capacitors C_{x1}, C_{x2} and C_o are in parallel and maintain capacitor voltage to V_{DC}.



(a)



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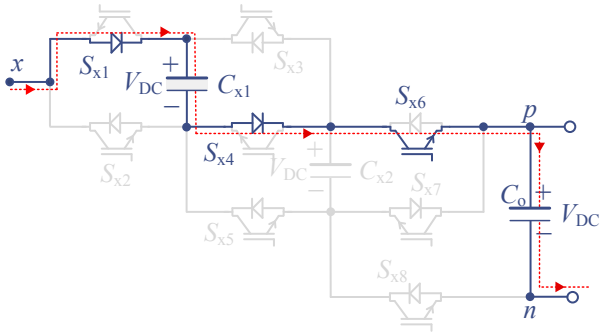

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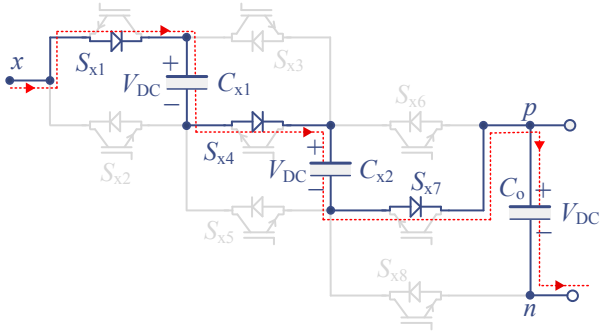

(d)

Fig. 5.15: *Switching states for the proposed seven-level buck rectifier*

2. State 2 ($V_{xn} = +V_{DC}$): During this state, the switches S_{x1}, S_{x3}, S_{x5}, S_{x6} andS_{x8} are turned ON, so as to achieve two simultaneous conduction paths, as shown in Fig. 5.15b. In the path shown with red, it can be seen that the capacitor C_o is in the path with ter-minal 'x' and 'n', such that the voltage $V_{xn} = +V_{DC}$. Additionally, for the path shown in green, the capacitors C_{x1}, C_{x2} and C_o are in parallel and balance the voltage of the capacitor to V_{DC}.

3. State 3 ($V_{xn} = +2V_{DC}$): During this state, the switches S_{x1}, S_{x4}, and S_{x6} are turned ON, so to achieve conduction paths, as shown in Fig. 5.15c. In the path shown with red, it can be seen that the capacitors C_{x1} and C_o are in the path with terminal 'x' and 'n', such that the voltage $V_{xn} = +2V_{DC}$.

4. State 4 ($V_{xn} = +3V_{DC}$): During this state, the switches S_{x1}, S_{x4}, and S_{x7} are turned ON, so as to achieve conduction paths, as shown in Fig. 5.15d. In the path shown with red, it can be seen that the capacitors C_{x1}, C_{x2} and C_o are series, such that the voltage $V_{xn} = +3V_{DC}$.

Table 5.2. *Switching states of proposed three-phase topology*

States	V_{xn}	**Power Switches**				**Capacitors**		
		S_{x1}	S_{x3}	S_{x5}	S_{x6}	C_{x1}	C_{x2}	C_{xo}
1	0	0	1	1	1	C	C	D
2	$+ V_{DC}$	1	1	1	1	D	D	C
3	$+ 2V_{DC}$	1	0	0	1	C	-	C
4	$+ 3V_{DC}$	1	0	0	0	C	C	D

Due to the simple structure, the proposed topology can be presented in a modular approach to increase the number of levels and reduce the gain. Fig. 5.16 shows the n-module where each module consists of 3 switches and one capacitor, and the output voltage gain is 1/(n + 1).

The modulation procedure to generate the gate pulses for the switches is discussed in the next section.

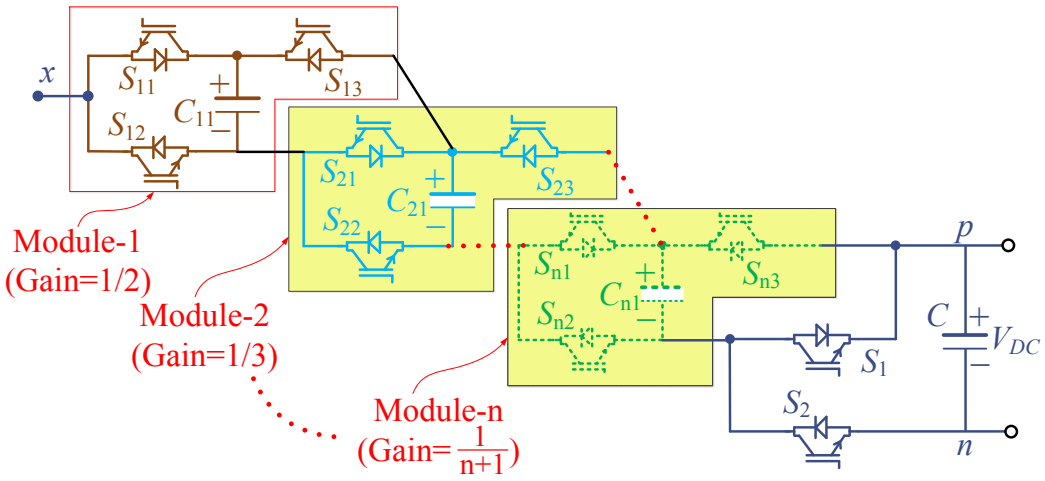

Fig. 5.16: *Modular structure of the proposed topology*

5.3.2 Range of operation

The proposed topology can operate in buck as well as boost modes depending upon the modulation signal (m_x). For the proposed topology, the modulation index depends upon the grid voltage (v_s^x), output DC voltage (V_{DC}) and the gain of the rectifier ($1/\beta$) (where β is 3 in this topology) and can be defined as:

$$m_x = \frac{v_s^{max}}{3V_{DC}} \tag{5.6}$$

The proposed topology operates as buck as well as boost mode, depending upon the value of m_x as described herewith: For the seven-level buck mode of operation:

$$\frac{v_s^{max}}{3} < V_{DC} < \frac{v_s^{max}}{2}, \tag{5.7}$$

i.e.,

$$\frac{2}{3} < m_x < 1, \tag{5.8}$$

For the five-level buck mode of operation:

$$\frac{v_s^{max}}{2} < V_{DC} < v_s^{max}, \tag{5.9}$$

i.e.,

$$\frac{1}{3} < m_x < \frac{2}{3}, \tag{5.10}$$

For the three-level boost mode of operation:

$$V_{DC} > v_s^{max}, \tag{5.11}$$

i.e.,

$$m_x < \frac{1}{3}, \tag{5.12}$$

For the seven-level buck mode of operation with overmodulation condition:

$$V_{DC} < \frac{v_s^{max}}{3}, \tag{5.13}$$

i.e.,

$$m_x > 1, \tag{5.14}$$

Output voltage variation in terms of modulating signal (m_x) is shown in Fig. 5.17, for input RMS AC voltage of 170 V (i.e., the peak value of 240 V).

5.4 COMPARISON WITH OTHER PFC RECTIFIERS

The proposed topology is capable of single/three-phase buck AC-to-DC conversion. A comparative analysis of multilevel PFC rectifier topologies classified as:

1. Single-phase PFC rectifier with buck and boost mode of operation (summarized in Table 5.3);
2. Three-phase PFC rectifier (summarized in Table 5.4).

The proposed SCMR offers a buck output voltage, which is most suitable for an EV charging application. It is a novel approach for achieving buck output voltage in multilevel

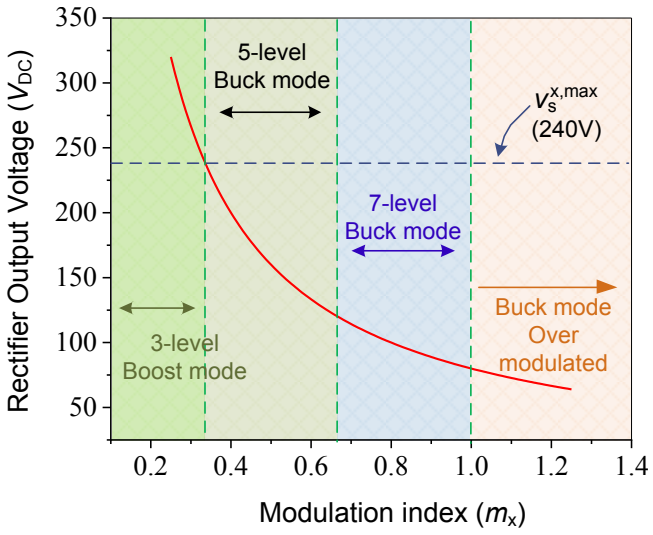

Fig. 5.17: *Variation in the output DC voltage with respect to the modulation index for the proposed multi-level rectifier*

topologies. Table 5.3 compares the proposed topology to conventional single-phase multilevel rectifiers such the HB [34], NPC [128], and FC [129]. These topologies have fewer components, but they have a unity voltage gain, making them boost rectifiers. Existing multilevel buck rectifiers proposed in [42, 43, 130] are compared to the proposed sin-gle-phase topology. These topologies are buck rectifiers with multiple output voltages. Different characteristics are compared, such as the number of levels (N_L), switches (N_s), diodes (N_D), capacitors (N_C), PIV, voltage sensors (N_{VS}), current sensors (N_{CS}) and voltage gain. Power switches with PIV equal to double the output DC volt-age are required in the [42] topology, as are additional voltage sensors. Similarly, topology in [43] necessitates power switches with PIV equivalent to four times the output DC voltage, as well as a large number of voltage and current sensors. These topologies have com-parable drawbacks, such as difficulties balancing capacitor voltages, which is only stable under balanced load conditions. Table 5.4 shows the comparison of the proposed topology with a three-phase conventional rectifier, i.e., NPC, T-type and FC based. These PFC rectifiers yield high voltage gain and achieve a boosted output voltage. The proposed work is also compared with existing multilevel three-phase topologies. This study is also based on the N_L, N_s, N_D, N_C, Gain ($1/\beta$) and the possibility of bidirectional power flow, which is possible to operate as a V2G mode and a buck or boost output voltage.

Table 5.3. *Comparative analysis with existing single-phase PFC rectifier topologies*

Parameters	**Boost Topologies**			**Buck Topologies**			
	H-Bridge [34]	**NPC [128]**	**FC [129]**	**CHB [130]**	**[42]**	**[43]**	**Proposed**
N_L	3	5	5	5	5	9	**7**
N_s	4	8	8	8	6	8	**16**
N_D	0	4	0	0	0	0	**0**
N_C	1	2	3	2	2	3	**5**
PIV	1	1	1	1	2	4	**1**
Gain (1/ β)	1	1	1	0.5	0.5	0.25	**1/3**
N_{VS}	2	2	2	3	3	4	**2**
N_{CS}	1	1	1	1	1	4	**1**

Table 5.4. *Comparative analysis with existing three-phase PFC rectifier topologies*

References	N_L	N_s	N_D	N_C	**Gain** $(1/\beta)$	**Bidirectional Capability**	**Output Voltage**
[39]	5	18	0	2	1	Yes	Boost
[36]	5	12	0	2	2	Yes	Boost
[40]	5	12	0	4	1	Yes	Boost
[81]	5	6	24	12	1	No	Boost
[82]	9	12	24	8	1	No	Boost
[78]	9	12	12	8	1	No	Boost
[79]	9	24	0	4	1	Yes	Boost
[80]	13	54	0	2	1	Yes	Boost
Proposed	**7**	**24**	**0**	**7**	**1/3**	**Yes**	**Buck**

All compared items aforementioned are listed in Table 5.4. It indicates that the proposed seven-level buck rectifier has the advantages of simple structure and buck mode capability. Overall, it is a competitive circuit to implement EV charging infrastructure, mainly on account of the buck mode of operation and capability of bidirectional power flow. The conventional PFC rectifiers implemented in [36, 39, 40] are all specified for five-level boost operation with

bidirectional power flow. To increase the levels in these converters, the number of power devices increases significantly. In the topology proposed in [81], the number of switches is low, but the number of power diodes is very high. It is useful for high voltage applications with unidirectional power flow only. The topologies discussed in [78, 82] are conceptualized for a nine-level boost operation. As evident from Table 5.4, the number of switches is low but requires a large number of diodes. Moreover, these are not applicable for a bidirectional power flow. Both the structures presented in [79, 80] operate with boost mode and offer a possibility of bidirectional power flow. The topology presented in [80] is modular and is implemented for a higher number of levels with the parallel use of Active Neutral Point Clamped (ANPC) modules. However, in this case, the number of devices is very high, increasing the rectifier controller complexity. Hence, it can be safely concluded that the topology proposed in this work is highly competent with considerations of three-phase seven-level buck operation with bidirectional power flow.

5.5 EXPERIMENTAL RESULTS

To evaluate the proposed three-phase buck rectifier and its closed-loop control, a laboratory setup was created utilizing discrete power switches MOSFETs (SiHG47N6) and an appropriate gate driver IC (Si82071AB-IS). A hall-effect-based voltage sensor (LEM LV25-P) and current sensor (HE025T01) with suitable power conditioning were used to sense the output voltage and input current. OPAL-RT OP4510, which connects with the hardware via MATLAB/Simulink on the host computer and generates the MOSFET gate pulses was used as a real-time controller. The controller and switching mechanism were developed using a 10 μs sampling period. A three-phase 170 V RMS was used as an AC input, with the output DC voltages being 100 V (in buck mode). Table 5.5 summarizes the parameters used in the experiment. Sudden changes in the DC load and the output reference voltage were used to assess the system's performance in both steady-state and dynamic scenarios.

Experimental results are taken with two scenarios, with a resistive load and another with an EV battery charging for a single/three-phase. When the rectifier converts 240 V three-phase peak AC (170 VRMS) to 100 VDC (in buck mode) and feeds it to the resistive load (R_o = 10 Ohm) with a 10 A load current, the steady-state results are achieved, as shown in Fig. 5.18. Because the input current (i_s) is sinusoidal and in phase with the input grid voltage (v_s), the input power factor is maintained at unity.

Table 5.5. *Experimental parameters*

Parameters	Value
Input voltage	170 V for three-phase and 230 V for single-phase VRMS
Input grid frequency	50 Hz
Filter inductor	4 mH
Capacitors (ALF80C162DF200)	1600 μF
Switching frequency	10 kHz
DC load	10, 20, 30 Ω
Output DC voltage	100 V for three-phase and 120 V for single-phase
Battery	48 V, 30 Ah Lithium-ion ferrous phosphate
Semiconductor switches	SiHG47N6
Gate driver IC	Si82071AB-IS
Hall effect voltage sensor	LEM LV25-P
Current sensor	HE025T01

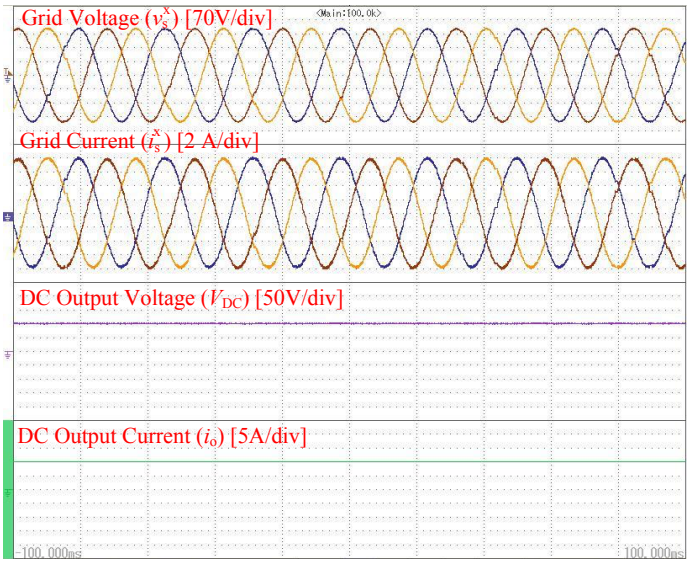

Fig. 5.18: *Steady-state experimental results in buck mode operation of the proposed rectifier*

As previously described, the proposed topology can also work in boost mode. Fig. 5.19 shows the steady-state operation where the output voltage is regulated at 280 V (in boost mode with a wide output range) and feeds it to the resistive load (R_o = 30 Ohm) with a 3 A load current.

In this mode of operation, the grid voltages (v_s) and grid currents (i_s) are in phase. The proposed multilevel rectifier operates in buck mode of operation. In the input, terminals of the rectifier generate four-level as a pole voltage (V_{xn}) with levels of 0, $+V_{DC}$, $+2V_{DC}$, $+3V_{DC}$. Moreover, seven-level is generated as a line voltage (V_{ab}, V_{bc}, V_{ca}) with levels of $+3V_{DC}$, $+2V_{DC}$, $+V_{DC}$, 0, $-V_{DC}$, $-2V_{DC}$ and $-3V_{DC}$ which improves the harmonic profile of the grid current and reduces the filter size. Three-phase pole voltages and line voltages are shown in Fig. 5.20.

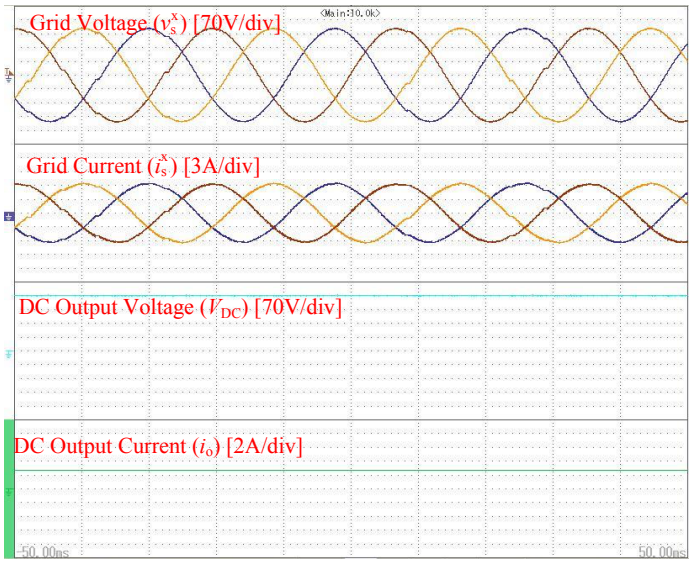

Fig. 5.19: *Steady-state experimental waveforms in the boost mode operation of the proposed rectifier*

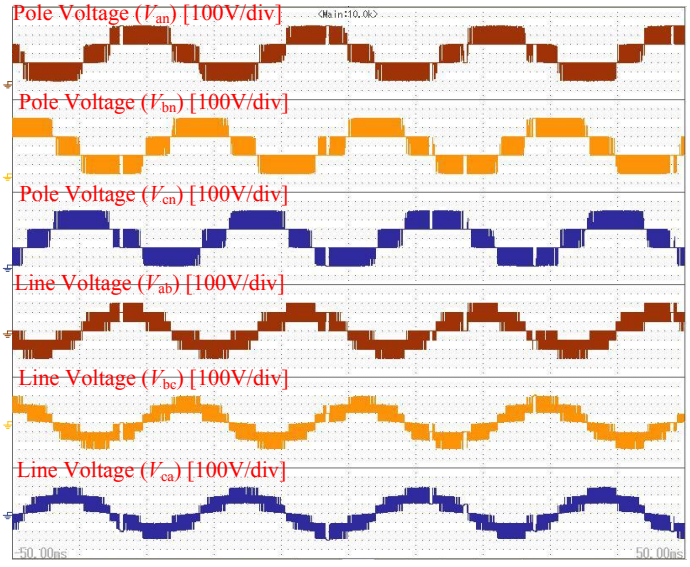

Fig. 5.20: *Experimental waveforms show four-level pole voltages and seven-level line voltages*

An experiment was carried out to validate the proposed rectifier's dynamic performance. With a sudden 50% reduction in the load resistance (R_o), raising the load current by a factor of two, the load voltage instantly stabilizes at 100 V. In addition, as indicated in Fig. 5.21, the rectifier maintains a unity power factor. In another case, the output DC reference voltage increases. As seen in Fig. 5.22, the reference voltage varies by 30%, causing V_{DC} and io to fluctuate abruptly. The load voltage stayed constant at 130 V, and the rectifier operated at a unity power factor.

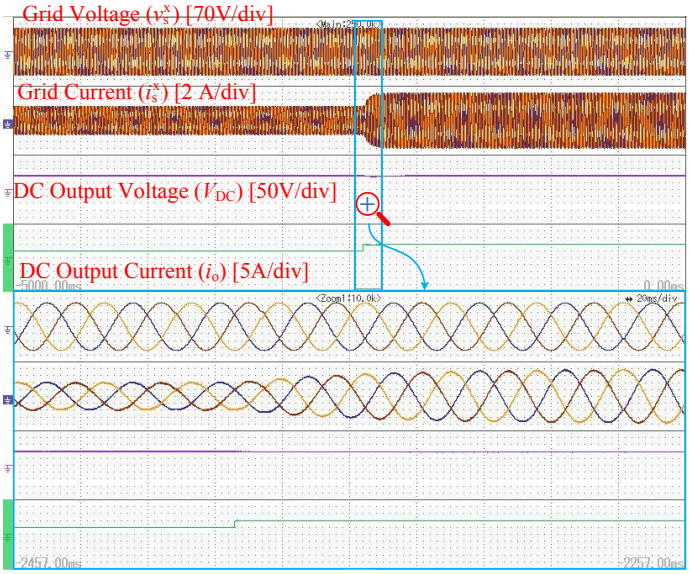

Fig. 5.21: *Experimental results during 50% decrease in load resistance*

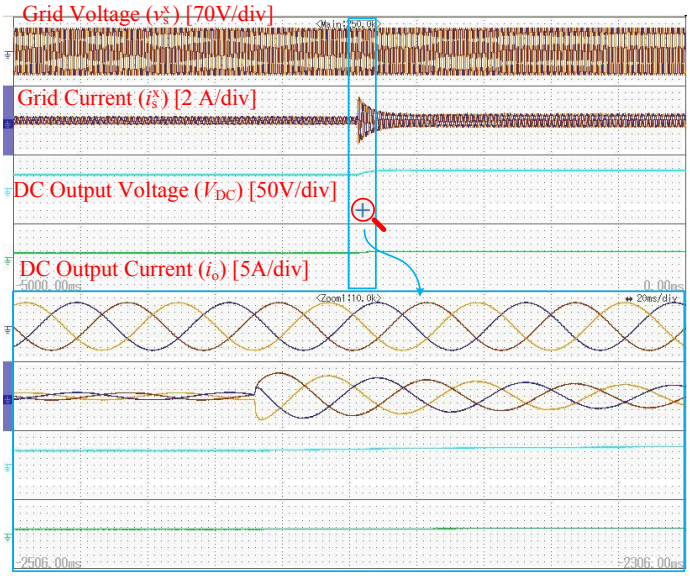

Fig. 5.22: *Experimental results during 30% rise in the DC voltage reference*

A power electronics interface consisting of the proposed PFC rectifier and a typical buck–boost DC-DC converter is constructed to illustrate application in three-phase charging. The ratings are based on a three-phase input voltage of 170 VRMS at 50 Hz and a rectifier output DC voltage of 100 V. The voltage and current of the battery are 48 V and 16 A, respectively. Fig. 5.23 depicts the battery charging, where the waveforms indicate that the grid voltage and current are in phase. The rectifier's output voltage is controlled to 100 V_{DC} and further regulated to battery voltage 48 V using a DC-DC converter.

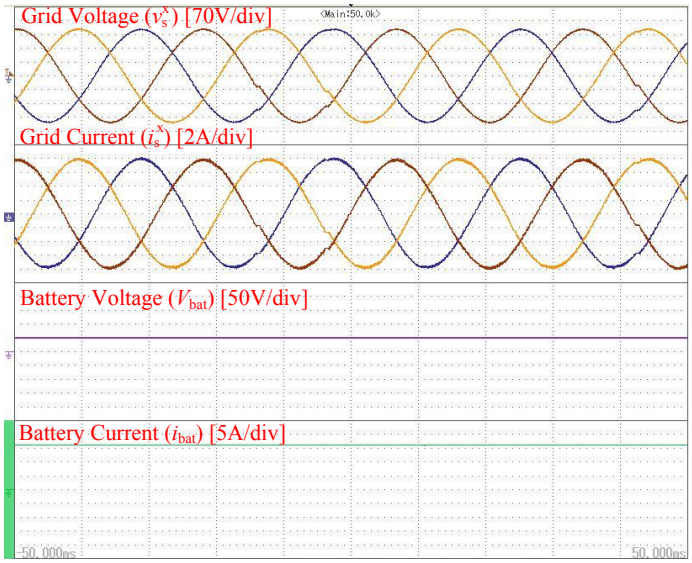

Fig. 5.23: *Experimental waveforms for three-phase battery charging*

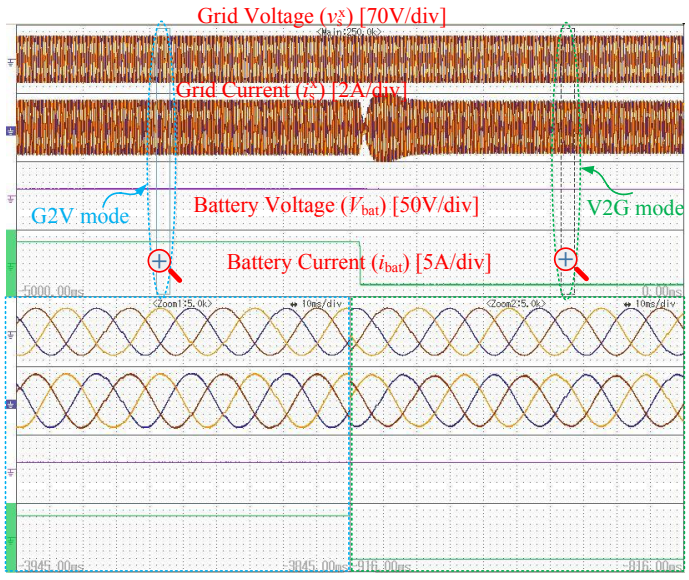

Fig. 5.24: *Bidirectional power flow with the proposed rectifier for V2G application*

The V2G mode allows the injection of battery energy back into the grid. Grid-to-vehicle (G2V) charging and vehicle-to-grid (V2G) discharging modes are available for EVs. The interface must be capable of bidirectional power flow in order to use V2G mode. The proposed topology supports charging as well as discharging in its three-phase variants. Fig. 5.24 depicts experiments in both modes of operation (G2V and V2G). When an abrupt change in the flow of the battery current is directed, the battery current is seen to be reversed. In this case, the grid current is 180 degree out of phase with the grid voltage.

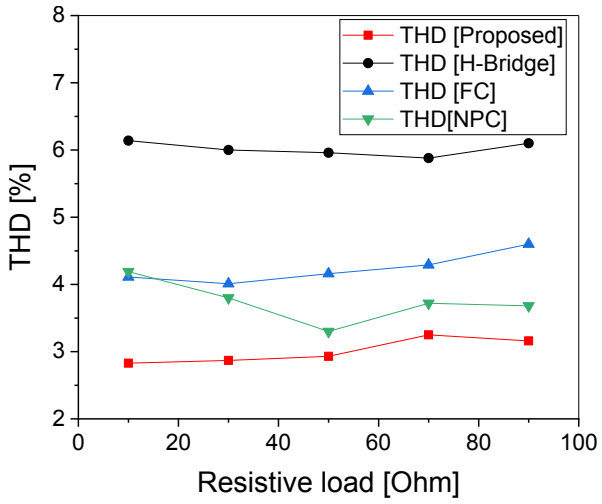

Fig. 5.25: *Comparison of THD vs. load with conventional rectifier*

A total harmonic distortion (THD) and input power factor (IPF) are estimated for the proposed seven-level rectifier, and comparisons are performed with the conventional boost rectifier. The following parameters were used for the THD and IPF calculations: carrier frequency of 10 kHz, input AC voltage of 325, output DC voltage of 400 V for conventional topologies, and 120 V for the proposed topology. When the proposed topology is compared to the others in terms of THD (vs. load) (Fig. 5.25) and Input Power Factor (IPF) (vs. load) (Fig. 5.26), the proposed topology has a low THD due to the seven-level topology and achieves a high IPF value. Fig. 5.27 depicts the distribution of power losses for the proposed IPF rectifier using the single-phase parameters listed in Table 5. With an overall efficiency of 95.46%, the total loss (switching loss and conduction loss) in power switches is 46 W. Modeling the single-phase converters and their control in Plexim PLECS software gives the proposed topology's power loss distribution.

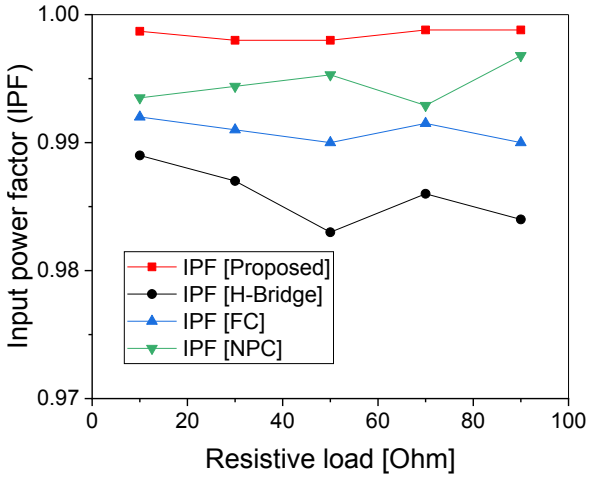

Fig. 5.26: *Comparison of IPF vs. load with conventional rectifier*

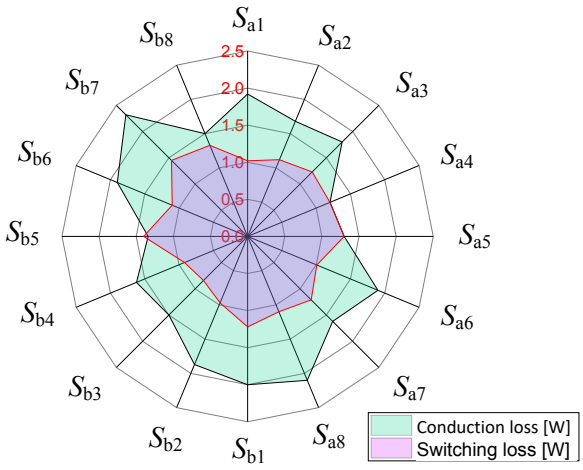

Fig. 5.27: *Distribution of power loss for 1015 W input power, power loss 46 W and efficiency is 95.46%*

5.6 CONCLUDING REMARKS

This chapter presents a new multilevel single/three-phase buck PFC rectifier based on SCs with gain $\beta = 3$. The proposed topology is suitable for on-board and off-board EV charging with bidirectional operation. It utilizes LSPWM to balance voltage and includes a voltage and current controller. The system's performance underwent testing with an AC input of 230 V for

single-phase and 170 V for three-phase, resulting in a DC output of 120 V and 100 V, respectively. Furthermore, various dynamic situations were tested using a prototype implementation. The following observations are made from this study:

- It synthesizes seven levels at the input side, thereby greatly improving the harmonic profile of the waveform.
- It requires a low number of power devices to generate seven levels at the input terminal.
- It works as a buck PFC rectifier with β is 3, while providing a wide output range in buck and boost mode.
- It does not require any additional balancing circuitry since the capacitors are self-balanced. Moreover, the voltage of only one of the SCs is required to be sensed to implement a closed loop control.
- It allows bidirectional flow of power, and hence it can be employed to implement a V2G interface for EV charging.
- The three-phase seven-level topology is also specified for buck and boost mode operation, providing four levels of phase voltage and seven levels of line voltage at the input terminal of the rectifier.

Chapter–6

A Single/Multiple Output Multilevel Buck Rectifier for EV-Battery Charging

In this chapter, a novel five-level SCs based self-balancing buck PFC MLR is proposed with a wide output voltage range, which can operate with different loads at the output terminals and also operate in both single and multiple output modes. Moreover, load voltage balancing is feasible even when the multiple loads have different values. The proposed rectifier performs buck operation and offers a wide output voltage regulation, which is suitable for EV battery charging. The performance of the presented topology has been investigated through operating principle, modulation strategy, closed-loop control and experimental validation for the operation with single-/multiple-output load variations.

6.1 GENERAL

For simultaneous EV charging in a charging station, there is a need for multiple PFC rectifiers and a DC-DC converter. However, this arrangement can also be achieved with a single PFC rectifier (i.e. a multi-output PFC rectifier) followed by individual DC-DC converters to separately control the EV battery voltage. The primary focus of this chapter is the single/multiple output PFC rectifier. The proposed topology allows for a maximum of three output voltages, with regulation that is independent of the load value and type. Voltage balancing under different load conditions is possible with an SC-based approach. The output DC voltage is regulated to a similar voltage

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with the self-balancing approach of the SC-based PFC rectifier. This chapter mainly focuses on off-board EV charging (with the proposed PFC rectifier operating in multi-output mode) and on-board EV battery charging (with the proposed PFC rectifier operating in single-output mode). A simplified and basic block diagram of the proposed system is shown in 6.1.

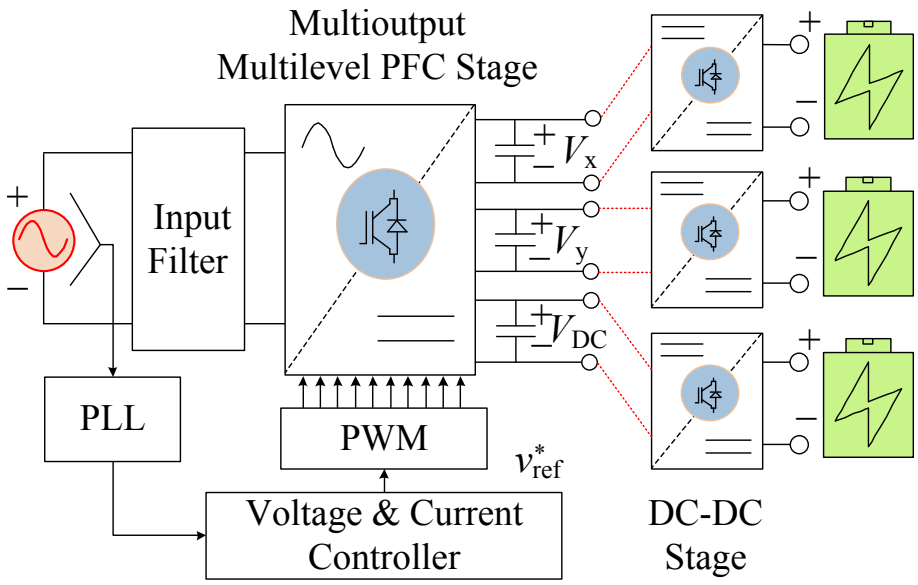

Fig. 6.1: *Basic block diagram of the proposed work.*

This work proposes a novel SCs based self-balancing buck PFC MLR topology with a wide output voltage range. A summary of some major issues related to existing multioutput rectifier topologies and the solution offered by the proposed SC-based topology is presented in Table 6.1.

From Table 6.1, it can be concluded that the proposed topology is highly competent with the considerations of buck PFC operation, single/multiple output voltage regulation, low voltage ratings of power switches and ease of voltage balancing of capacitors. Consequently, this work is applicable for EV battery charging systems. To verify the aforementioned theoretical advantages of the proposed MLR, a buck-operated prototype setup is implemented in the laboratory to feed a resistive load and to perform battery charging operation. All discussed features of the proposed rectifiers are tested through extensive experimentation on this prototype.

Table 6.1. *Summary of research gaps in existing multioutput PFC rectifiers and the proposed solution*

Major issues related to rectifiers topologies	**Proposed SC-based multilevel topology**
Need of a large number of voltage and current sensors [41–43]	Only one of the capacitor voltages is required to be sensed
High voltage stress across the switches as compared to output DC voltage [42, 43]	Voltage stress is equal to the DC output voltage
Balancing is possible only when the multiple loads are equal and are of the same type [41–43]	Balancing is possible even when multiple loads are of different values and different types

6.2 PROPOSED BUCK-PFC RECTIFIER TOPOLOGY

The proposed single-phase multi-output topology considers a three-resistive load. The circuit description and various switching states are discussed in this section.

6.2.1 Circuit topology

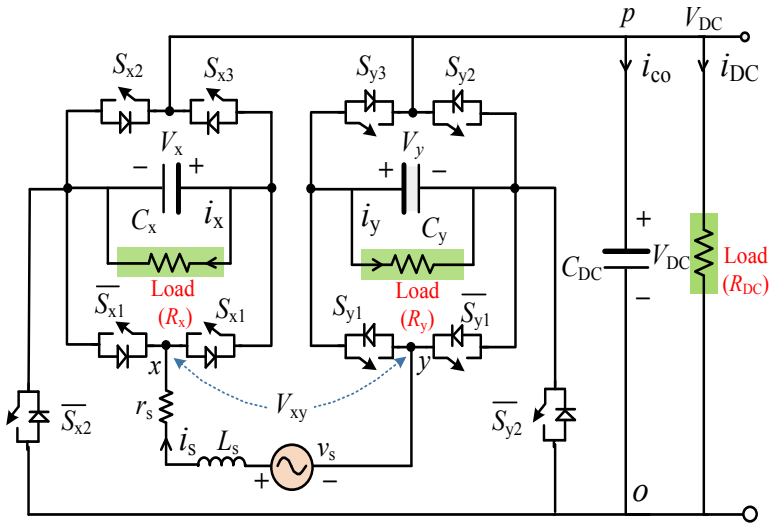

Fig. 6.2: *Circuit topology of Single/ multiple output PFC rectifier*

The proposed rectifier topology is shown in Fig. 6.2. Each leg has five active switches as well as one capacitor which is maintained at a voltage equal to V_{DC}. Each leg generates three voltage levels between the terminal pairs 'x-o' and 'y-o': 0, $+V_{DC}$ and $+2V_{DC}$. The AC input voltage is applied at terminals 'x' and 'y', whereas the DC output voltages are available at the capacitors C_{DC}, C_x and C_y. The output voltage across the capacitors are balance to V_{DC} (i.e., V_{DC}= V_{Cx}=V_{Cy}).

6.2.2 Description of various states

Table 6.2 summarizes all the valid operational states of the proposed rectifier, with ON and OFF states of a power switch denoted by '1'and '0'respectively, and charging and discharging states of the capacitors denoted by 'C' and 'D', respectively. For the proposed topology, capacitors are charged through the source and discharged through the load. All the capacitors are self-balanced due to SCs principle. The Table 6.2 summarizes the, five levels, including redundant states, that are synthesized at the input terminals.

Table 6.2. *Switching states of the proposed five-level rectifier*

State	i_s	Leg-x			Leg-y			$V_{xy} = V_{xo} - V_{yo}$	Capacitors		
		Switches		V_{xo}	Switches		V_{yo}				
		S_{x1}	S_{x2}		S_{y1}	S_{y2}			C_x	C_y	C_{DC}
σ_1	$i_s > 0$	1	1	$+2V_{DC}$	0	0	0	$+2V_{DC}$	C	D	C
σ_2	$i_s > 0$	1	1	$+2V_{DC}$	1	0	$+V_{DC}$	$+V_{DC}$	C	D	C
σ_3	$i_s > 0$	1	0	$+V_{DC}$	0	0	0	$+V_{DC}$	C	D	D
σ_4	$i_s \geq 0$	1	0	$+V_{DC}$	1	0	$+V_{DC}$	0	C	D	D
σ_5	$i_s \geq 0$	0	0	0	0	0	0	0	C	D	D
σ_6	$i_s \leq 0$	1	0	$+V_{DC}$	1	0	$+V_{DC}$	0	D	C	D
σ_7	$i_s \leq 0$	0	0	0	0	0	0	0	D	C	D
σ_8	$i_s < 0$	0	0	0	1	0	$+V_{DC}$	$-V_{dc}$	D	C	D
σ_9	$i_s < 0$	1	0	$+V_{DC}$	1	1	$+2V_{DC}$	$-2V_{DC}$	D	C	C
σ_{10}	$i_s < 0$	0	0	0	1	1	$+2V_{DC}$	$-2V_{DC}$	D	C	C

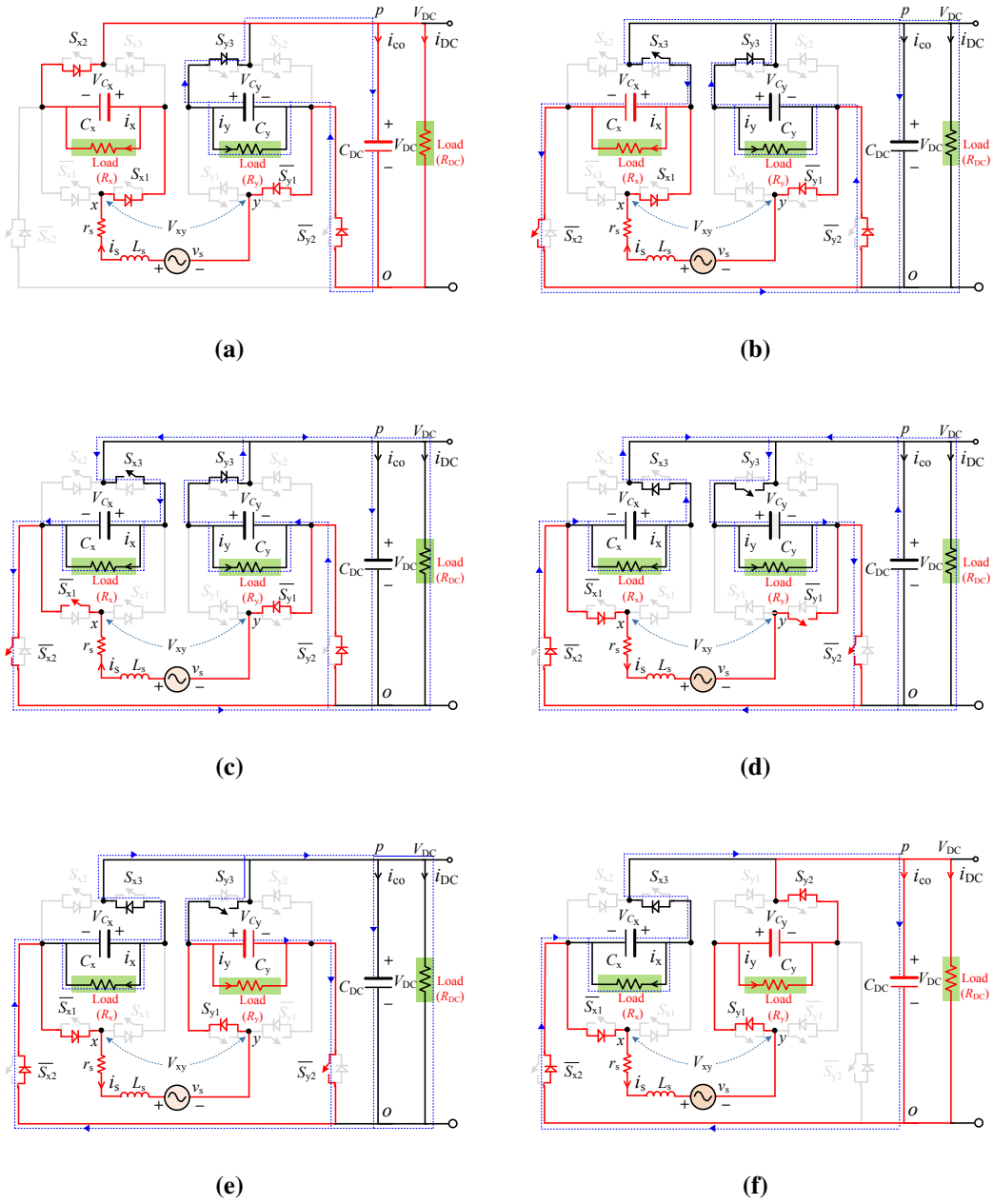

Fig. 6.3: *Switching states for the proposed five-level buck rectifier*

Following is a brief description of the various switching states for the proposed rectifier:

1. State σ_1 (V_{xy}=+2V_{DC}): In the positive half cycle, the switches S_{x1}, S_{x2}, $\overline{S_{y1}}$, $\overline{S_{y2}}$ and S_{y3} are turned ON at the same time, resulting in two simultaneous conduction paths shown in Fig. 6.3a. In the path shown in red, it can be seen that the capacitors C_x and C_{DC} are in series and thus the voltage V_{xy}=+2V_{DC}. Also, for the path shown in blue, the capacitors C_y discharges to the load, while being in parallel with C_{DC} so as to balance the capacitor voltage to V_{DC}.

2. State σ_3 (V_{xy}=+V_{DC}): In the positive half cycle, the switches S_{x1}, S_{x2},S_{x3}, $\overline{S_{y1}}$, $\overline{S_{y2}}$ and S_{y3} are turned ON at the same time, resulting in two simultaneous conduction paths shown in Fig. 6.3b. In the path shown in red, it can be seen that V_{xy}=+V_{DC} and the capacitors charge through the source. Also, the capacitors C_y and C_{DC} are discharged through the load with the path shown in blue.

3. States σ_5 and σ_7 (V_{xy}=0): During these states, in the positive and negative half cycle, the switches $\overline{S_{x1}}$, $\overline{S_{x2}}$, S_{x3}, $\overline{S_{y1}}$, $\overline{S_{y2}}$ and S_{y3} are simultaneously turned ON, so as to achieve two simultaneous conduction paths as shown in Fig. 6.3c and 6.3d. It can be observed in the red path that all capacitors are bypassed, resulting in a voltage V_{xy}=0. Also, for the path shown in blue, the capacitors C_x, C_y and C_{DC} operate in parallel, thereby balances the capacitors' voltage and discharged to the load.

4. State σ_8 (V_{xy}=−V_{DC}): During this state, in the negative half cycle, the switches $\overline{S_{x1}}$, $\overline{S_{x2}}$, S_{x3}, S_{y1}, $\overline{S_{y2}}$ and S_{y3} are turned ON at the same time, resulting in two simultaneous conduction paths shown in Fig. 6.3e. In the path shown with red, it can be seen that the capacitors C_y generate a voltage V_{xy}=−V_{DC} and charge through the source. Also, the capacitors C_x, C_y and C_{DC} operate in parallel and balances the voltage at V_{DC}, as shown in the blue path. Moreover, the capacitors C_x and C_{DC} discharge to the load.

5. State σ_{10} (V_{xy}=−2V_{DC}): During this state, in the negative half cycle, the switches $\overline{S_{x1}}$, $\overline{S_{x2}}$, S_{x3}, S_{y1} and S_{y2} are simultaneously turned ON, to achieve two simultaneous conduction paths as shown in Fig. 6.3f. In the path shown with red, it can be seen that the capacitors C_y and C_{DC} are in series such that the voltage V_{xy}=−2V_{DC} and charge through the source. Also, for the path shown in blue, the capacitors C_x and C_{DC} operate in parallel and balances the capacitor voltage at C_{DC}. Moreover, the C_x discharges to the load.

6.3 MODULATION TECHNIQUE AND CONTROLLER DESIGN

In this section, the discussion covers the voltage and current control of a PFC rectifier with a closed-loop structure, as well as the modulation technique discussed for the generation of gate pulses.

6.3.1 Pulse width modulation

Different strategies have been employed for the modulation of MLRs, including high-switching frequency techniques (such as space vector PWM and multicarrier sine-triangle PWM) and low-switching-frequency methods (such as selective harmonic elimination, active harmonic elimination and nearest level control) [131]. These strategies, with suitable adaption, can be used to modulate the proposed MLR. In this work, the gating signals are generated using a LSPWM system, as shown in Fig. 6.4.

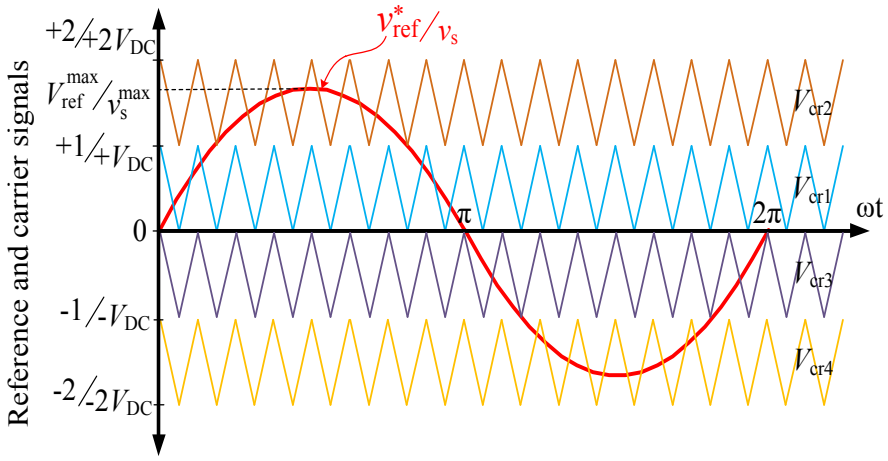

Fig. 6.4: *Level-shifted modulation scheme for the proposed rectifier*

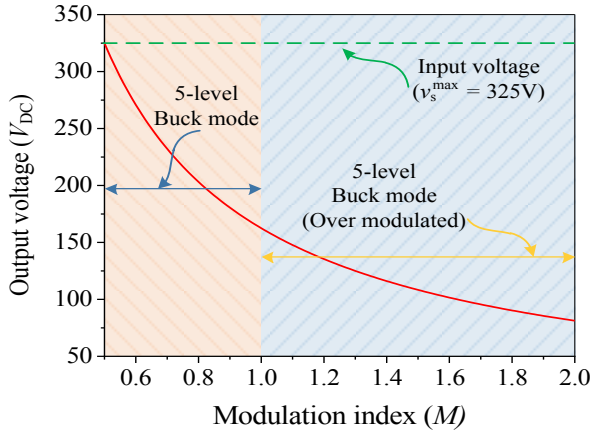

Fig. 6.5: *Variation of output voltage with modulation index*

Using the carrier signals (C_{crX}, X ∈ 1-4) and reference waveform (v^*_{ref}), the switching signals are obtained. These signals when mapped onto the corresponding voltage values, result in regions as shown in Fig. 6.4. With v_s^{max} being the peak grid voltage and V_{DC} being the output DC voltage, the modulation index M, for the proposed converter is expressed as:

$$M = \frac{v_{\mathrm{s}}^{\mathrm{max}}}{2V_{\mathrm{DC}}} \tag{6.1}$$

6.3.2 Controller design

For the proposed rectifier topology, a simple controller including two cascaded loops is designed for generating the switching pulses. The inner loop is used for grid-current control and the outer loop is for regulating the output-voltage [132]. Primarily, the grid current can be expressed in terms of other parameters as,

$$L_{\mathrm{s}}\frac{\mathrm{d}i_{\mathrm{s}}}{dt} = v_{\mathrm{l}} - r_{\mathrm{s}}i_{\mathrm{s}} \tag{6.2}$$

Where, V_{l}=V_{s}-$V_{\alpha\beta}$, L_{s} is the filter inductor, r_{s} is that inductor parasitic resistance. By applying the Laplace transform to (6.2), it is possible to obtain the following:

$$G^{\mathrm{in}}_{\mathrm{mlr}}(s) = \frac{I_{\mathrm{s}}(s)}{V_{\mathrm{l}}(s)} = \frac{1}{r_{\mathrm{s}} + L_{\mathrm{s}}.s} \tag{6.3}$$

Fig. 6.6 shows the inner and outer loops of the controller. In the inner loop, the current controller can be either a simple gain as a proportional controller or a proportional-integral (PI) controller. It should be noted that the inner loop should have faster dynamics than the outer loop. Therefore, in the case of a sinusoidal input current signal using a PI controller, the integral gain of that PI should be minimal enough not to change the inner loop's speed. However, the use of a PI compensator on a sinusoidal signal creates some steady-state error that can be seen as a DC component in the current harmonic spectrum [130]. On the contrary, a proportional + resonant regulator achieves virtually the same steady-state and transient performance as a PI regulator implemented in a synchronous rotating frame as follows:

$$G_{\mathrm{C}}(s) = k_{\mathrm{pc}} + \frac{k_{\mathrm{ic}}.s}{s^2 + \omega^2} \tag{10}$$

In this case, the open-loop transfer function of the current control loop (see Fig. 6.6) is:

$$G_{\mathrm{ol}}^{\mathrm{in}}(s) = \frac{G_{\mathrm{C}}(s)}{(r_{\mathrm{s}} + L_{\mathrm{s}}.s)\,(1 + 1.5T_{\mathrm{s}}.s)} \tag{11}$$

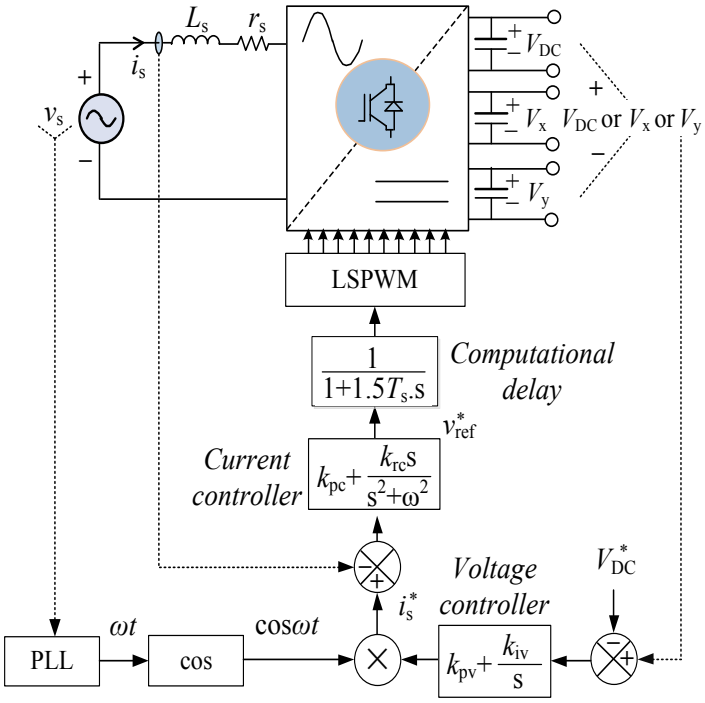

Fig. 6.6: *Close loop voltage and current controllers for the proposed multi-output PFC rectifier*

The closed-loop transfer function of the system will theoretically approach unity at the fundamental reference frequency with no phase or magnitude error in the output waveform because the magnitude of $G_{\mathrm{C}}(s)$ approaches infinity at this frequency [130]. Due to their narrowband frequency response, the resonant terms yield relatively low gain outside of their band-pass zone. As a result, a proportionate gain term must also be calibrated to ensure a satisfactory transient response.

The following equations are derived from the fundamental concepts of gain margin and phase margin:

Table 6.3. *Controller tuning and stability margin*

Specified Margin		**Resultant Margin**	
A_{m}	ϕ_{m}	k_{p}	k_{i}
2.5	45	48	1300
4	30	27.4	986

$$\left|\frac{(r_{\mathrm{s}} + L_{\mathrm{s}}.j.\omega_p)\left(1 + 1.5T_{\mathrm{s}}.j.\omega_p\right)}{\mathrm{G_c}\left(j.\omega_p\right)}\right| = A_m \tag{6.4}$$

$$arg\left[\frac{\mathrm{G_c}\left(j.\omega_p\right)}{(r_{\mathrm{s}} + L_{\mathrm{s}}.j.\omega_p)\left(1 + 1.5T_{\mathrm{s}}.j.\omega_p\right)}\right] = -\pi \tag{6.5}$$

$$arg\left[\frac{\mathrm{G_c}\left(j.\omega_g\right)}{(r_{\mathrm{s}} + L_{\mathrm{s}}.j.\omega_g)\left(1 + 1.5T_{\mathrm{s}}.j.\omega_g\right)} + \pi\right] = \Phi_m \tag{6.6}$$

$$\left|\frac{(r_{\mathrm{s}} + L_{\mathrm{s}}.j.\omega_g)\left(1 + 1.5T_{\mathrm{s}}.j.\omega_g\right)}{\mathrm{G_c}\left(j.\omega_g\right)}\right| = 1 \tag{6.7}$$

where (6.4) and (6.5) define the gain margin and (6.6) and (6.7) define the phase margin. Accordingly, as described in [133], values of these parameters are shown in Table 6.3.

Furthermore, another loop should be added to the controller to regulate the output DC voltage. As discussed previously, by regulating any one of the capacitors of the proposed rectifier, all other voltages are regulated in both single-output and multiple-output modes. Equations from the DC side of the rectifier should be examined to obtain the system model for the outer loop. That is,

$$i_{\mathrm{s}} = i_{\mathrm{C_{DC}}} + i_{\mathrm{o}} \tag{6.8}$$

$$C_{\mathrm{DC}}\frac{dV_{\mathrm{DC}}}{dt} = i_{\mathrm{s}} - \frac{V_{\mathrm{DC}}}{R_{\mathrm{DC}}} \tag{6.9}$$

The following transfer function for the outer loop device will be accomplished by small-signal modelling of (6.8). The relationship between the output DC voltage, value of the load and DC capacitor value is obtained by the following transfer function:

$$G_{\mathrm{mlr}}^{\mathrm{out}}(s) = \frac{V_{\mathrm{dc}}}{i_{\mathrm{s}}} = \frac{R_{\mathrm{dc}}}{(R_{\mathrm{dc}}C_{\mathrm{dc}}.s + 1)} \tag{6.10}$$

The voltage controller can be considered as the outer loop due to the relationship between i_{s} and V_{DC} as (6.10). Such loop delivers the idea of a cascaded controller in which the input for the inner loop is the output of the outer loop. As there is no frequency in the DC signal, a PI compensator with a $G_{\mathrm{V}}(s)$ transfer function is used to control the voltage at the desired level [132]. The voltage loop controls the output DC voltage atV_{DC}^{*}, as shown in Fig. 6.6, and provides the reference current peak value as an input to the inner loop. Due to its low complexity and adequate accuracy, the controller shown in Fig. 6.6 can be easily realized with real-time controllers.

6.4 COMPARISON WITH OTHER TOPOLOGIES

The proposed topology is capable of multilevel multi-output buck AC-to-DC conversion. A comparative analysis of multilevel PFC rectifier topologies (which are further classified as boost and buck topologies) is summarized in Table 6.4, while a comparison with other magnetic core-based PFC rectifier topologies is summarized in Table 6.5. The proposed topology is compared to conventional multilevel rectifiers such as the H-bridge (HB) [34], neutral point clamped (NPC) [128], and flying capacitors (FC) [129] in Table 6.4. The component requirement is less in these topologies, but these topologies function as boost rectifiers. Moreover, these topologies operate as single output structures. Multiple outputs are possible if these topologies operate in a cascaded manner [134].

The proposed topology is also compared with existing multilevel buck rectifiers proposed in [42], [43] and [134]. These topologies are buck rectifiers with multiple output voltages. A comparative analysis is done in terms of different parameters such as; the number of levels (N_{L}), number of switches (N_{s}), number of diodes (N_{D}), number of capacitors (N_{c}), number of voltage sensors (N_{VS}), number of current sensors (N_{CS}), number of outputs (N_{o}), peak inverse

Table 6.4. *Comparison of the proposed topology with other multilevel rectifiers*

Parameters	**Boost topologies**			**Buck topologies**			
	HB[34]	**NPC[128]**	**FC [129]**	**CHB[134]**	**[42]**	**[43]**	**Proposed**
N_{L}	3	5	5	5	5	9	**5**
N_{s}	4	8	8	8	6	8	**10**
N_{D}	0	4	0	0	0	0	**0**
N_{C}	1	2	3	2	2	3	**3**
PIV_{pu}	1	1	1	1	2	3	**1**
Gain	1	1	1	0.5	0.5	0.25	**0.5**
N_{VS}	2	2	2	3	3	4	**2**
N_{CS}	1	1	1	1	1	4	**1**
N_{o}	1	1	1	2	2	3	**3**
η (%)	99.1	98.5	NA*	NA*	98.1	NA*	**97.50**

voltage (PIV), voltage gain and efficiency (η). Topology in [42] requires power switches with PIV equal to twice the output DC voltage and more voltage sensors. Similar is the case with topology in [43], which requires power switches with PIV equal to four times the output DC voltage and requires many voltages and current sensors. These topologies suffer from a common limitation: difficulty in balancing capacitors' voltages, and the need of similar loading conditions for multiple outputs.

Table 6.5 compares the proposed topology and magnetic core-based PFC rectifiers [135–139]. The comparison is carried out using the parameters of N_{s}, N_{c}, N_{D}, N_{o}, number of magnetic cores, number of the inductors (N_{ind}), voltage stress across the components and efficiency. In the magnetic core-based buck rectifiers [135–139], voltage stress is very high, though they require fewer active switches (though the requirement for other components is significantly high). Moreover, these topologies do not facilitate multiple DC output terminals. Hence, it can be concluded that the proposed topology proposed is highly competent with the considerations of buck PFC operation, possibilities of single/multiple outputs, voltage ratings of power switches and ease of voltage balancing of capacitors.

Table 6.5. *Comparison of the proposed topology with some non-multilevel buck-boost PFC rectifiers*

Parameters	**[135]**	**[136]**	**[137]**	**[138]**	**[139]**	**Proposed**
N_s	2	2	2	2	4	**10**
N_D	5	4	5	5	4	**0**
N_C	3	3	2	2	2	**3**
N_{ind}	3	3	2	2	2	**1**
Mag. core	3	2	2	2	2	**0**
Outputs	1	1	1	1	1	**3**
Voltage stress*	High	High	High	High	High	**Low**
Efficiency (η)[%]	95.5	93.87	97	96	97.6	**97.50**

6.5 RESULTS AND DISCUSSION

A laboratory setup was established to evaluate the proposed five-level rectifier and the proposed closed-loop control system. The power circuit is built using discrete power switches (MOSFETs SiHG47N60). Hall-effect based voltage sensor (LEM LV25-P) and current sensor (HE025T01) are used to measure the output voltage and input current respectively.

The real-time control signals for the power switches were generated by OPAL-RT OP4510, which was interfaced with the hardware on the host computer through MATLAB/Simulink. The input AC is a single-phase voltage with 325V peak, while the output DC voltage is set at 200V (i.e., buck mode of operation). Table 6.6 summarizes various parameters used in the experimental verification. With a resistive load, the system's performance is tested in both steady-state and dynamic conditions (which include variations in the operating conditions, such as a sudden change in DC load, sudden change in the input AC source voltage and change in the output reference voltage). Moreover, perform the load variation condition as single/multiple loads.

The steady-state results are captured when the rectifier converts 325V peak AC to 200V DC as depicted in Fig. 6.7. The input voltage (v_s) is in phase with input current (i_s) and unity power factor is maintained. A low-harmonics five-level voltage waveform is achieved at the rectifier input, which positively impacts grid current THD. The reference output voltage is set

Table 6.6. *Various experimental setup parameters*

Parameters	**Value**
Input voltage (v_s)	230V RMS
Grid frequency	50 Hz
Output DC voltage	200V
Switching frequency	10 kHz
Power	1 kW
Capacitors	1600 µF
Filter inductor (#)	4 mH
Battery details	48V, 30Ah, Lithium-ion

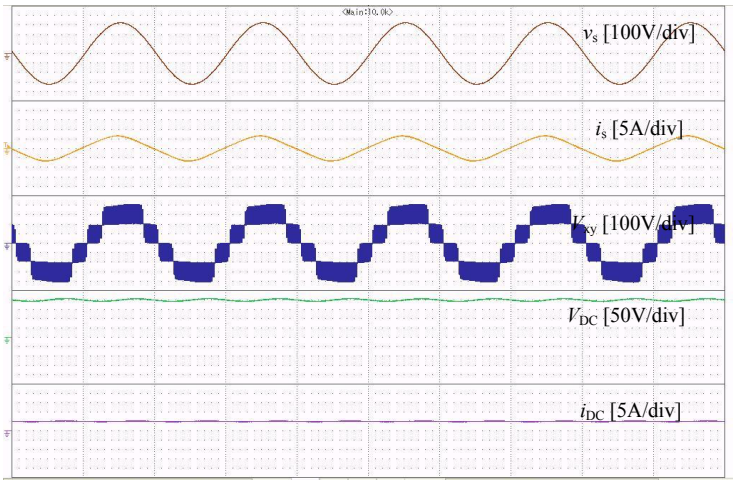

Fig. 6.7: *Waveforms for the steady-state operation of the proposed rectifier*

to 200V, achieved adequately with an acceptable voltage ripple. The capacitors' voltages are balanced at 200V each, yielding a V_{xy} voltage waveform with 0, ±200V, and ±400V.

Fig. 6.8,6.9,6.10,6.11 depict the results of dynamic performance. As shown in Fig. 6.8, when the output current is increased suddenly by 50%, the load voltage quickly stabilizes at 200V and the rectifier continues to operate in unity power factor mode. In another instance, v_s is suddenly decreased, and it is seen that the grid current i_s is increased proportionally and the unity power factor is maintained. The voltages of DC capacitors are not affected by the voltage sag in the grid, as shown in Fig. 6.9. In a different case, as illustrated in Fig. 6.10, changing the output DC reference voltage by 20% changes V_{DC} and i_{DC}, causing the load voltage to settle at

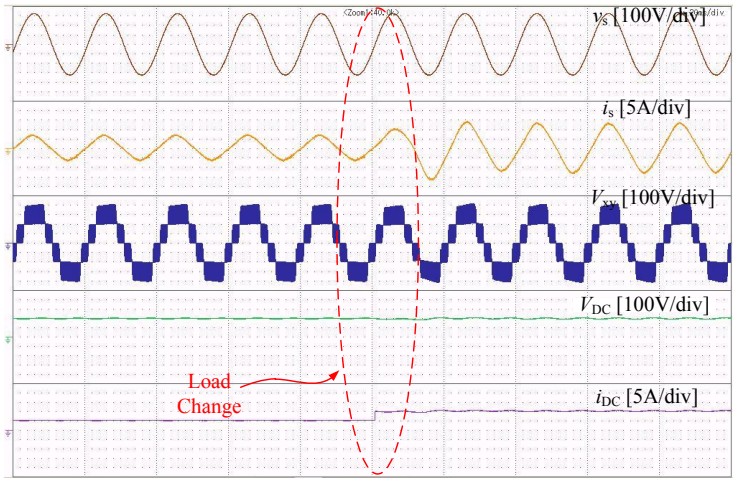

Fig. 6.8: *Results for dynamic performance: when the load is suddenly increased by 50%*

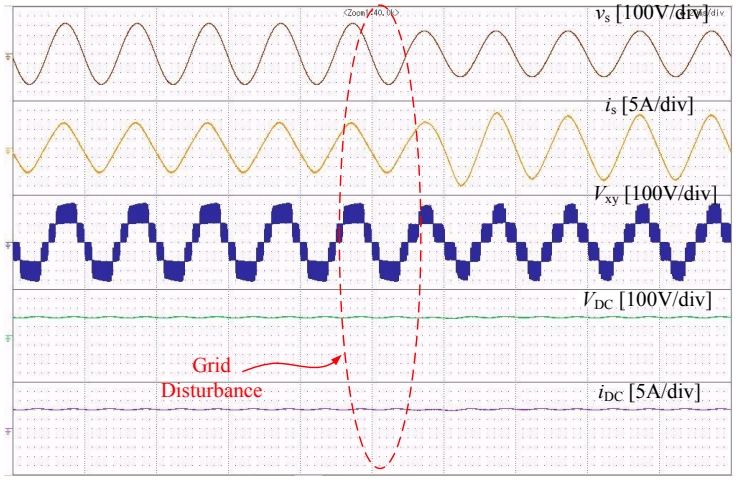

Fig. 6.9: *Experiment results for dynamic performance: when the input AC source voltage is reduced by 25%*

240V as expected. The converter maintains a unity power factor and five voltage levels at the rectifier's input. These results validate the controller's tracking accuracy.

To validate the operation with single-/multiple-output load variations, further experimental tests are performed. A 50% abrupt reduction in load R_x causes increase in the load current by a factor of 2 and the load voltage immediately stabilizes at 200V (i.e., V_{cx}= V_{cy}=V_{cDC}=V_{DC}) (please see Fig. 6.11). Even though grid current (i_s) is raised accordingly and the rectifier remains in unity power factor mode.

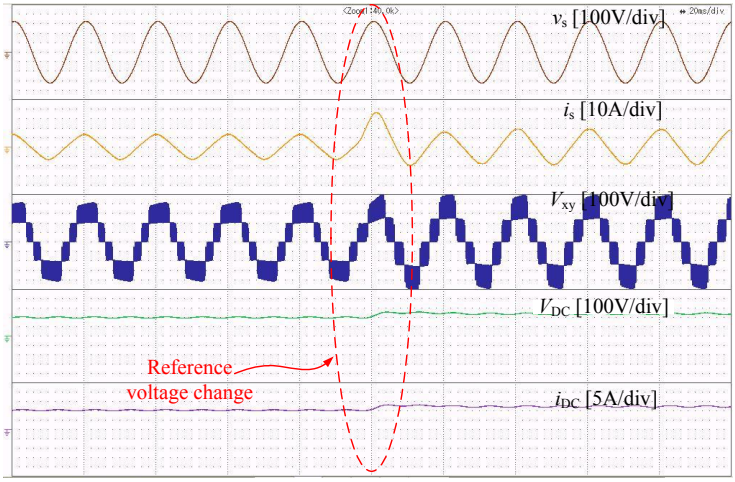

Fig. 6.10: *Experiment results for dynamic performance: when the output DC voltage reference is raised by 20%*

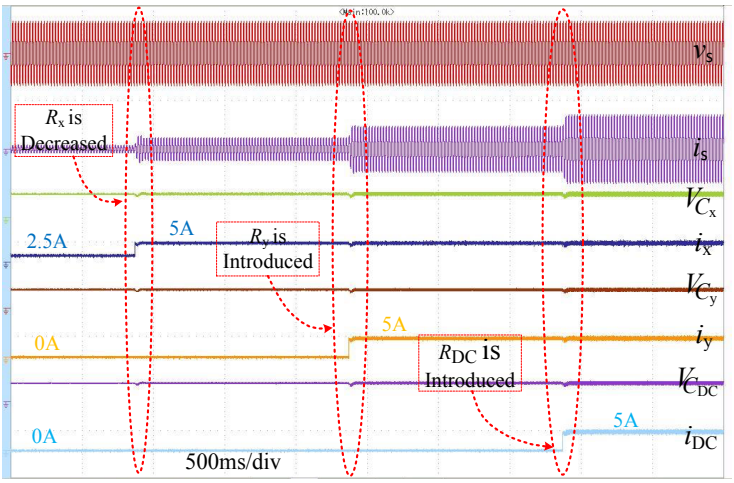

Fig. 6.11: *Experiment results in multiple-output mode*

To demonstrate applicability in single-phase EV charging with a single output, a power electronics interface consisting of the proposed PFC rectifier and a typical buck-boost DC-to-DC converter is built. The values are based on a 230V RMS, 50Hz input voltage and a rectifier output DC voltage of 200V. The battery voltage (V_b) is 48V, and the battery charging current (i_b) is 20A. The experimental results for charging battery are shown in Fig. 6.12, and it can be seen that the grid voltage and current are in phase and achieve a five-voltage level at the input terminal of the rectifier.

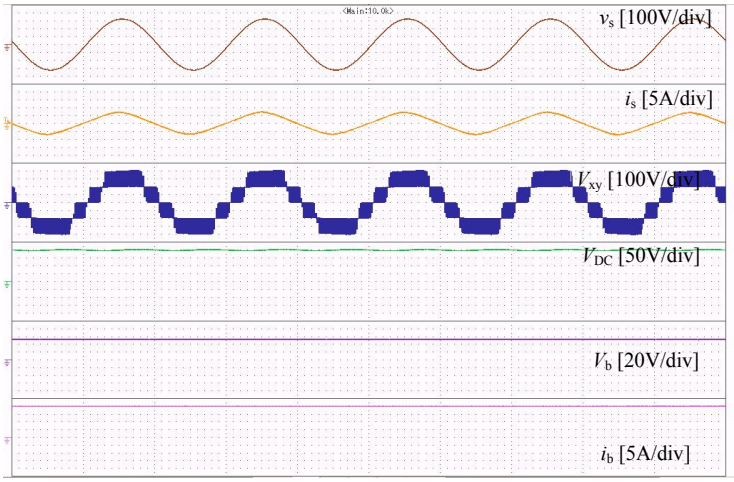

Fig. 6.12: *Experimental results for single-phase battery charging*

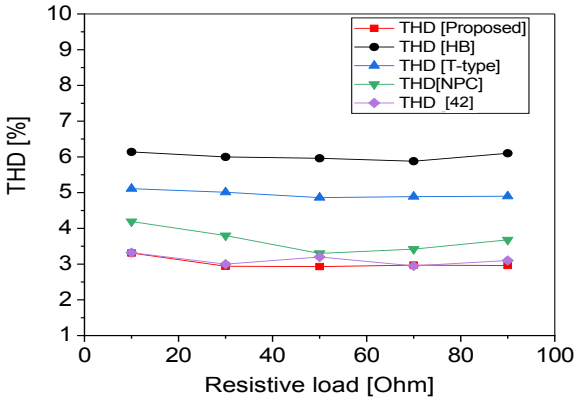

Fig. 6.13: *Comparison of THD vs. power*

The THD and PF are calculated for the proposed work and comparisons are made with the conventional boost rectifier and buck rectifier topology proposed in [42]. The following working parameters were used to achieve the THD and PFC analyses: carrier frequency of 10 kHz, input AC voltage of 325 v_s^{max}, output DC voltage 400V for conventional topologies and 200V for proposed and [42] topology. When the topologies are compared in terms of THD (versus power) (Fig. 6.13) and Power Factor (PF) (versus power) (Fig. 6.14), the proposed topology outperforms the others on these parameters. The distribution of power losses for the proposed PFC rectifier under specific parameters described in Table 6.6 is shown in Fig. 6.15. The total loss in power switches and passive elements is 25 W, with an overall efficiency of 97.5%. The power loss distribution of the proposed topology is obtained by modelling the converters and their control in

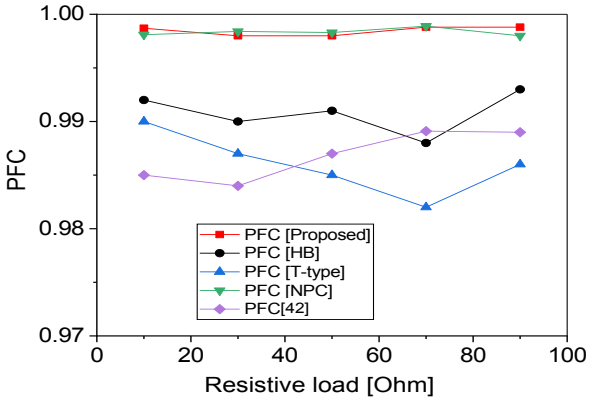

Fig. 6.14: *Comparison of PFC vs. power*

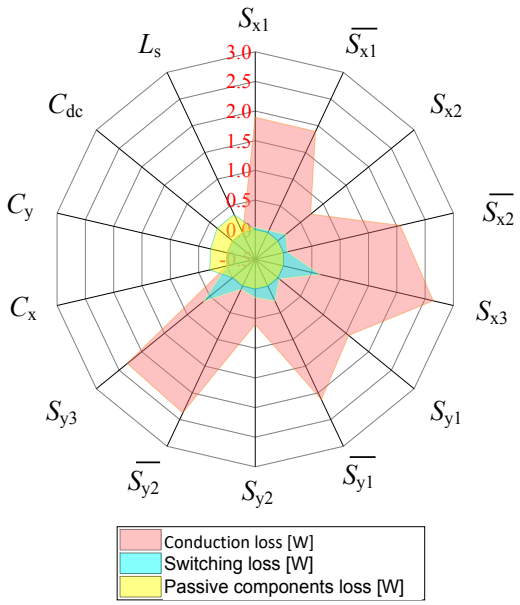

Fig. 6.15: *Distribution of power losses for 1kW input power, with 25W total loss and 97.5% efficiency*

Plexim PLECS software. It is observed that switching and conduction losses are reduced. The proposed topology also reduces passive component loss. Efficiency is calculated for the different loading conditions as shown in Fig. 6.16. The efficiency is found to be varying between 97.75% and 97.25% for change in load.

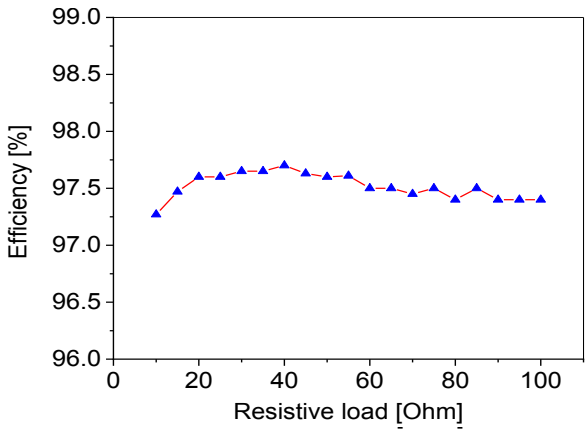

Fig. 6.16: *Efficiency curve with respect to the load resistance*

6.6 CONCLUDING REMARKS

This chapter presents a new multilevel single/multiple output buck PFC rectifier based on SCs suitable for simultaneously EV charging. The performance of the single-phase AC input of 230 V and DC output of 200 V for various dynamic situations has been tested using a proto-model implementation. The following observations are made from this study:

- Multi-output operation is possible with single-phase or three-phase operation using the proposed five or seven-level topologies.
- It works as a buck PFC rectifier with β is 2, while providing a wide output range in buck and boost mode.
- Balancing of the capacitor voltages is possible even when multiple loads have different values or are changed to different types.
- It does not require any additional balancing circuitry since the capacitors are self-balanced. Moreover, the voltage of only one of the switched capacitors is required to be sensed to implement a closed loop control.
- Voltage stress across the switches is equal to the DC output voltage.

Chapter–7

Conclusions and Scope for Future Work

7.1 MAIN CONCLUSIONS

In this work it is established that switched capacitors based multilevel topologies can effectively function as PFC rectifiers for EV charging systems with following main advantages: wide range of output DC voltage, self-balanced switched capacitors, V2G capability, compatibility with single-phase and three-phase systems, low voltage stress on power switches, low dv/dt stress, better harmonic profile of the input voltage waveform and so on. Followings are some specific concluding remarks of significant importance:

- The features of a grid-connected SC-based multilevel boost inverter have been first analyzed in Chapter 3, with the goal of achieving unity power factor and stable operation with variations in modulation index. Thereafter, it has been mathematically established that when the role is reversed, i.e. the topology is employed as rectifier, then it operates in buck mode.

- The SCs-based multilevel PFC rectifier, described in Chapter 4 as a newly proposed structure in this work, offers bidirectional power flow, enabling energy to flow from the grid to the vehicle during charging and from the vehicle to the grid during discharging. This feature is essential for V2G applications, where electric vehicles can act as mobile energy storage units to provide power to the grid during peak demand periods.

- Two novel PFC rectification buck topologies, described in Chapter 4 and 5, namely the five-level (β=2) and seven-level (β=3) configurations, are highly adaptable to different charging scenarios and grid conditions. These topologies can be easily modified for single-phase and three-phase operation, allowing for greater flexibility and versatility.

- The multilevel topologies are capable of operating at different modulation indexes, providing a wide output voltage regulation range. This feature is critical for efficient charging of different types of loads, including batteries with different voltage ratings and charging requirements.

- The SCs in the rectifier are applicable to work individually with different outputs, and their voltages are balanced through series and parallel connections. This ensures output voltage balancing even when multiple loads of different values and types are connected to the rectifier.

- Compared to other multi-output buck PFC rectifiers, the topology proposed and described in Chapter 6, requires a lower number of voltage and current sensors for capacitor balancing. This reduces the overall complexity and cost of the system, making it more affordable and easier to implement in different applications. Additionally, the reduced number of sensors results in higher reliability and lower maintenance cost.

7.2 SCOPE FOR FUTURE WORK

While this work has opened up 'switched capacitors based multilevel rectifiers (SCMLRs)' as a novel area of research to work upon, there is an ample scope for further investigations. Following are a few suggestions for future research pertaining to SCMLRs:

- The major application area of concern in this work has been the charging systems for electric vehicles. Accordingly, the newly proposed topologies have been validated. However, there are other modern systems that require PFC rectification stage, such as motor drives, LED lighting systems and so on. Future work may incorporate the specific needs of these systems for employing SCMLRs.

- A compact design and the implementation of SCs-based buck PFC rectifier using a new generation of Wide-Bandgap (WBG) semiconductor devices, e.g., GaN or SiC, has not been explored in this work. With the rapid mainstreaming of WBG devices, it would be interesting to see how the design, efficiency and performance of SCMLRs can be improved using WBG devices.

- Possibility of fault-tolerant operation is an important advantage of multilevel topologies. Such possibilities can be explored in SCMLRs with an application oriented approach for fault-detection and reconfiguration.

- Another interesting area is to minimize the surge current produced when starting the power converter. Surge current protection can be achieved through the application of soft switching techniques, which can significantly reduce the current stress on the power switches. The soft start of the power converter improves the efficiency and performance of SCMLRs, further assisting in mitigating the current stress on the power switches.

List of Publications

JOURNAL PUBLICATIONS (SCI)

1. Anekant Jain, Krishna K. Gupta, Sanjay K. Jain and Pallavee Bhatnagar, "A Bidirectional Five-Level Buck PFC Rectifier With Wide Output Range for EV Charging Application," ***IEEE Transactions on Power Electronics***, vol. 37, no. 11, pp. 13439-13455, Nov 2022. (Impact factor: 6.70) **[Chapter 4]**
   doi: https://doi.org/10.1109/TPEL.2022.3185239

2. Anekant Jain, Krishna K. Gupta and Sanjay K. Jain, "A Novel Single/Multiple Output Multilevel Buck Rectifier for EV-Battery Charging," ***IEEE Transactions on Vehicular Technology***, vol. 72, no. 4, pp. 4384 - 4393, April 2023. (Impact factor: 6.80) **[Chapter 6]**
   doi: https://doi.org/10.1109/TVT.2022.3222349

3. Anekant Jain, Krishna K. Gupta and Sanjay K. Jain, "A novel step-up topology for multilevel power conversion," ***International journal of circuit theory and applications***, vol. 51, no. 1, pp. 265- 282, 2023. (Impact factor: 2.30) **[Chapter 3]**
   doi: https://doi.org/10.1002/cta.3430

4. Anekant Jain, Krishna K. Gupta, Sanjay K. Jain, Pallavee Bhatnagar and Hani Vahedi, "A V2G Enabled Bidirectional Single/Three-Phase EV Charging Interface Using Modular Multilevel Buck PFC Rectifier," ***Electronics***, vol. 11, no. 12, 1891, 2022. (Impact factor: 2.90) **[Chapter 5]**
   doi: https://doi.org/10.3390/electronics11121891

CONFERENCE PUBLICATIONS

1. Anekant Jain, Ritika Agarwal, Krishna K. Gupta and Sanjay K. Jain, "A V2G-enabled Seven-level Buck PFC Rectifier for EV Charging Application," *24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe)*, Hanover, Germany, 2022, pp. 1-10. **[Chapter 5]**

2. Anekant Jain, Sanjay K. Jain, Krishna K. Gupta, Hani Vahedi and Pallavee Bhatnagar, "Role of Charging/Discharging in the Integration of EVs to Grid as Intermittent Energy Sources," *IEEE Electrical Power and Energy Conference (EPEC)*, Toronto, ON, Canada, 2021, pp. 550-555. **[Chapter 2]**

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Appendices

Appendix–A

More details on switched capacitors charging current

For inverter operation switched capacitors are coming in parallel to the DC source and charge to the certain level. Considering example of one capacitor charging current with resistance present in the charging path. The path for I_{C1} is depicted in Fig. A.1, while I_{C1} is calculated as:

$$I_{\mathrm{C1}} = \left(\frac{V_1}{R_1}\right) \times exp\left(\frac{t}{R_1 \times C_1}\right) \tag{A.1}$$

Where,

$$V_1 = V_{\mathrm{DC}} - V_{\mathrm{D1}} - V_{\mathrm{C1}}$$
$$R_1 = r_{\mathrm{D1}} + r_{S4} + R_{ESR_{\mathrm{C1}}} \tag{A.2}$$

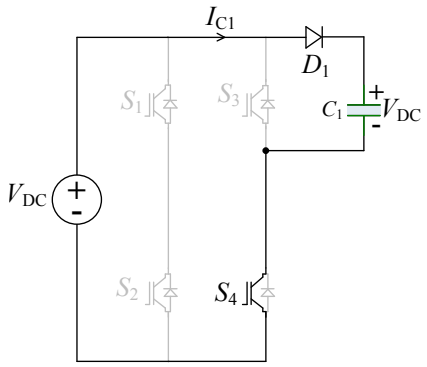
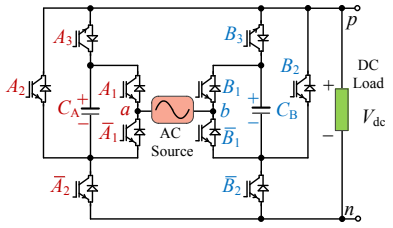
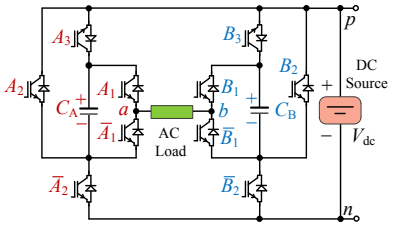
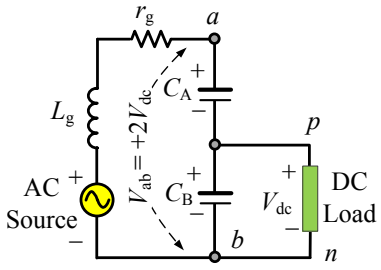
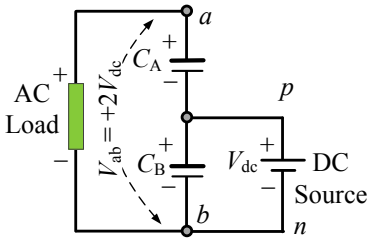
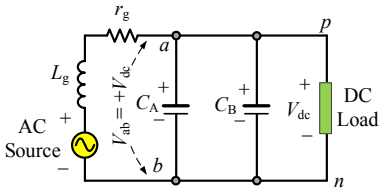
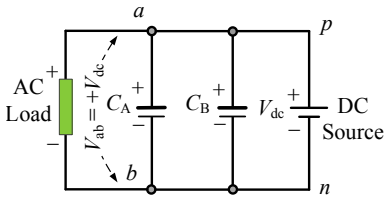
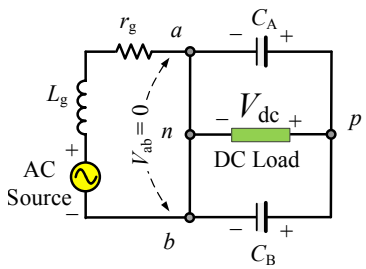
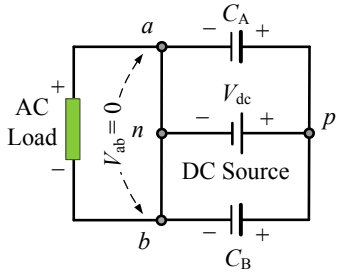


Fig. A.1: *Charging path for capacitor* C_1

Due to the capacitor being connected in parallel to the DC voltage source, a large inrush current appears across the capacitors and switches. The equivalent resistance in the path of the capacitor charging, as shown in eq A.1, can reduce the inrush current, but not up to the desired

level. This issue arises in switched capacitor-based inverters. This problem has been identified through literature, and the switched capacitor-based rectifier emerges as a potential solution for mitigating this inrush current.

Table A.1. *Equivalent states of the proposed topology as a rectifier and as an inverter*

	Five Revel Rectifier	Five Level Inverter
Topology		
For $V_{ab} = +2V_{DC}$ (State A)	 Switches $A_1, A_2, \overline{B}_1, \overline{B}_2, B_3$ are ON	 Switches $A_1, A_2, \overline{B}_1, \overline{B}_2, B_3$ are ON
For $V_{ab} = +V_{DC}$ (State B)	 Switches $A_1, \overline{A}_2, A_3, \overline{B}_1, \overline{B}_2, B_3$ are ON	 Switches $A_1, \overline{A}_2, A_3, \overline{B}_1, \overline{B}_2, B_3$ are ON
For $V_{ab} = 0$ (State C)	 Switches $\overline{A}_1, \overline{A}_2, A_3, \overline{B}_1, \overline{B}_2, B_3$ are ON	 Switches $\overline{A}_1, \overline{A}_2, A_3, \overline{B}_1, \overline{B}_2, B_3$ are ON

This can be clearly understood with the simultaneous consideration of inversion and rectification operations of a given multilevel topology based on switched capacitors. As an

example, please refer to Table A.1 below. In this table, the proposed topology is shown both as a rectifier (left column) and as an inverter (right column). For the rectifier, terminals 'a' and 'b' are connected to the AC source and terminals 'p' and 'n' are connected to the DC load. For the inverter, on the other hand, terminals 'a' and 'b' are connected to the AC load and terminals 'p' and 'n' are connected to the DC source. The subsequent rows of Table A.1 show the equivalent circuits for the switching states (marked as States A to C) which synthesize positive voltage levels viz. 0, $+V_{DC}$ and $+2V_{DC}$ at the terminals 'a' and 'b' (i.e. voltage V_{ab}) for both the rectifier and the inverter.

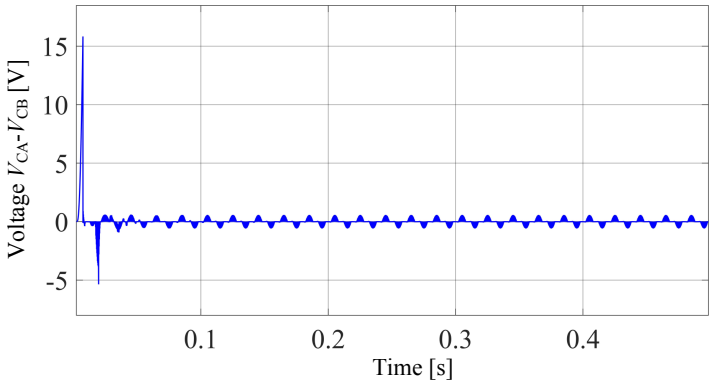


Fig. A.2: *Difference between capacitor voltages (V_{CA}-V_{CB}) for the proposed five-level rectifier*

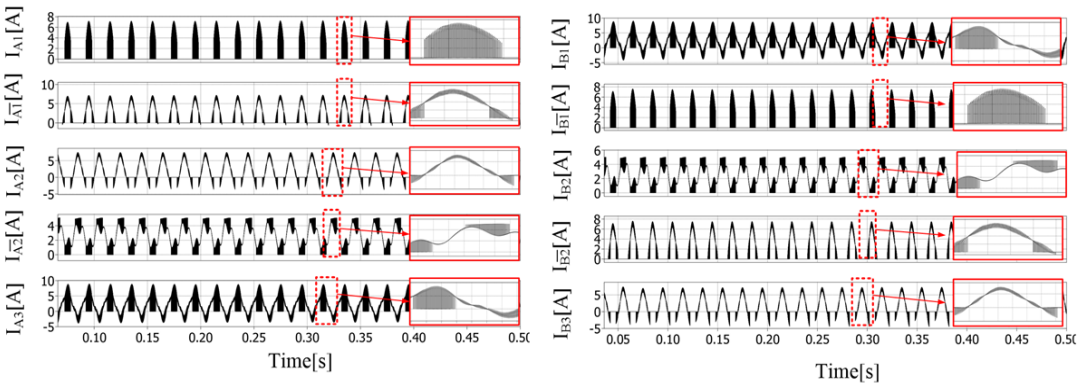


Fig. A.3: *Current waveforms through switches for proposed buck topology (1 kW system)*

It can be clearly seen from the equivalent circuits of the switching states that the large charging currents in the inverter are because a capacitor (C_A or C_B) is repeatedly brought in parallel with the DC input source. For example, in State A for the inverter, C_B is in parallel with the DC source, causing a large charging current. In State A for the rectifier, on the other hand,

the capacitors C_A and C_B are in series and are charged by the AC source, and the DC load is in parallel with the capacitor C_B, with absolutely no large charging currents. A similar look at all the states distinctly bring out this crucial difference between switched capacitors based multilevel rectifier and inverter. It may, however, be argued that for the rectifier the capacitors C_A and C_B do come in parallel (e.g. in State B), and this may cause large currents between them. But, it should be noted that these capacitors are charged to the same voltage by the AC source and the difference between their voltages, if any, will be very less and thus the consequent currents will also be very less (effectively limited by the on state resistances of the power devices, ESRs of the capacitors and resistance of the conductor). For the topology under consideration, as an example, when operated as a rectifier (230 VRMS, 50Hz, 200V DC output) the difference in the voltages of capacitors C_A and C_B is shown in Fig. A.2. It can be seen that the magnitude of this difference is very less, and hence no large currents are seen in the proposed five-level rectifier. Current waveforms across the switches are shown in Fig. A.3.