Modeling of Fowler Nordheim Tunneling current through Gate dielectric in a Double Gate MOSFET

Thesis report submission in the partial fulfillment of the

Requirement for the award of the degree of

MASTERS OF TECHNOLOGY

in

VLSI DESIGN

Submitted by

Peeyoosh Tripathi

Roll No: 601361017

Under the Guidance of

Mr. Arun Kumar Chatterjee

Assistant Professor, ECED

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

ENGINEERING

THAPAR UNIVERSITY, PATIALA (PUNJAB) – 147004

JULY-2015

CERTIFICATE

I hear by declare that the work which is being presented in the thesis entitled "**Modeling of Fowler Nordheim tunneling current through Gate dielectric in a Double Gate MOSFET**" in partial fulfillment of the requirement for the award of degree of M.Tech. (VLSI Design) at Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Mr. Arun Kumar Chatterjee, Assistant Professor, ECED.

The matter presented in this thesis has not been submitted in any other University/Institute for the award of my degree.

Date: 15/07/15

Peeyoosh Tripathi

Roll No: 601361017

It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

Arun Kumar Chatterjee. 15/07/15

Mr. Arun Kumar Chatterjee

Assistant Professor

ECED, Thapar University

Counter signed by:

Dr. Sanjay Sharma

Professor & Head

ECED, Thapar University

Patiala-147004

Dr. S. S. Bhatia

Dean of Academic Affairs

Thapar University

Patiala-147004

ACKNOWLEDGEMENT

I take this opportunity to express my profound sense of gratitude and respect to all those who helped me through the duration of this thesis. I would have never succeeded in completing my task without the cooperation, encouragement and help provided to me by various people. Words are often too less to reveal one's deep regards. I acknowledge with gratitude and humility my indebtedness to **Mr. Arun Kumar Chatterjee, Assistant Professor**, Electronics and Communication Engineering Department, Thapar University, Patiala, under whose guidance I had the privilege to complete this thesis. I wish to express my deep gratitude towards her for providing individual guidance and support throughout the thesis work.

I convey my sincere thanks to **HEAD OF THE DEPARTMENT, Dr. Sanjay Sharma** as well as **PG Coordinator, Dr. Amit Kohli** Associate Professor, **Programme Coordinator, Dr. Anil Arora** Assistant Professor**,** Electronics and Communication Engineering Department, entire faculty and staff of Electronics and Communication Engineering Department for their encouragement and cooperation.

My greatest thanks to all who wished me success especially my parents and other family members and friends without whom I would not have been able to complete my thesis work.

I would like to express my special appreciation and thanks to my advisor **Mrs. Madhu Chatterjee**. I would like to thank you for encouraging my research. Your advice on both research as well as on my career have been invaluable.

I thank and own my deepest regards to all of them and all others who have helped me directly or indirectly.

Peeyoosh Tripathi

ABSTRACT

The scaling of physical dimensions of MOSFET is accompanied by the decrease in gate oxide thickness and the doping density in the substrate increase. Due to the scaling, gate oxide thickness become less then 5nm a few amount of current flow through the oxide in conduction band of gate according to FN tunneling.

Gate leakage current in MOSFET devices caused by tunneling of carriers through the oxide where the barrier height is greater than the energy of electron. The physical mechanism of tunneling was calculated using the Fermi direct function in previous models but in proposed model the quantum phenomena has been used to calculate the charge carrier distribution on the surface.

Gate tunneling current of MOSFETs is an important factor in modeling ultra small devices. In this thesis, gate tunneling in present-generation MOSFETs is studied. In the proposed model, the electron wave function at the semiconductor–oxide interface and inversion charge and thickness of inversion layer, by treating the inversion layer as a potential well, including some simplifying assumptions have been calculated. Then we compute the gate tunneling current using the calculated wave function. The proposed model results have an excellent agreement with experimental results in the literature.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

MOSFET:	Metal oxide semiconductor field effect transistor
CMOS:	Complementary metal oxide semiconductor field effect transistor
NMOS:	N-channel metal oxide semiconductor field effect transistor
PMOS:	P-channel metal oxide semiconductor field effect transistor
SEC:	Short channel effect
DIBL:	Drain induced barrier lowering
GIDL:	Gate induced barrier lowering
FN:	Fowler Nordheim
SOI:	Silicon on insulator
PDSOI:	Partially depleted silicon on insulator
FDSOI:	Fully depleted silicon on insulator
DGSOI:	Double gate silicon on insulator
DGFET:	Double gate field effect transistor
BOX:	Buried oxide
ITRS:	International technology roadmap for semiconductor
IC:	Integrated circuit
WKB:	Wentzel-Kramers-Brillouin
ECB:	Electron tunneling from conduction band
EVB:	Electron tunneling from valence band
HVB:	Hole tunneling from valence band

Chapter 1

Introduction

1.1 MOSFET History

In 1959 M. M. (John) Atalla and Dawon Kahng at Bell Labs developed the first successful insulated-gate field-effect transistor (FET), which had been long anticipated by Lilienfeld, Heil, Shockley and others (1926 Milestone) by overcoming the "surface states" that resisted electric fields from penetrating into the semiconductor material. By investigating thermally grown silicon-dioxide layers, it has been found that these states could be reduced at the interface between the silicon and its oxide in a sandwich layers of metal (M) - gate, oxide (O) - insulating layer, and silicon (S) - semiconductor - thus the name MOSFET, also known as MOS. It was not pursued further as the device was slow and addressed no pressing needs for telephone system. In 1961, Kahng pointed out its potential "ease of fabrication and the possibility of application in integrated circuits." But researchers at Fairchild and RCA recognized these advantages. In 1960, Karl Zaininger and Charles Meuller created an MOS transistor at RCA and C.T. Sah of Fairchild built an MOS-controlled tetrode. Further, Fred Heiman and Steven Hofstein in 1962 built an experimental 16-transistor integrated device at RCA [1].

The MOS transistor conducting region is either *p*-type ("*p*-channel" device) or *n*-type ("*n*-channel" device) material. The *n*-channel are faster than *p*-channel but are more difficult to make. MOS devices was introduced in commercial market in 1964. General Microelectronics and Fairchild proposed *p*-channel devices for logic and switching applications; RCA introduced an *n*-channel transistor (3N98) for amplifying signals. In comparison to the bipolar devices, this *n* channel transistor had smaller size and low power consumption. Over 99 percent of microchips produced today use MOS transistors. Achieving such ubiquity took decades of effort. (1964 Milestone) [1].

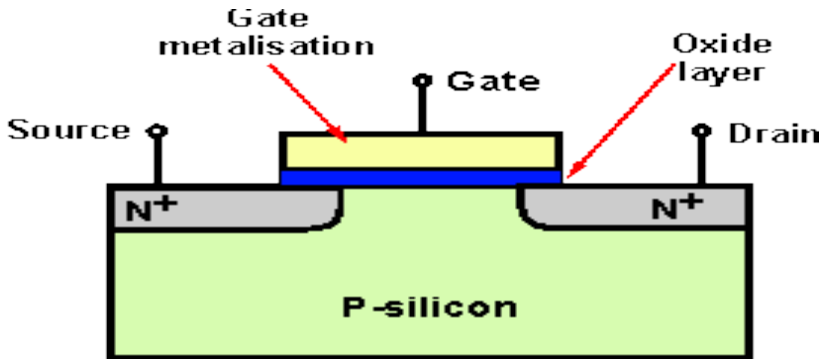


Figure 1.1 MOSFET First structure .

1.2 MOORE'S Law

The growth of the semiconductor industry is characterized by the increase of transistor count per unit area in integrated circuits (IC), well-known as Moore's Law [2]. However, this law is a rough prediction of the package density of ICs in the future. The semiconductor industry has made immense progress in the field of Metal Oxide Semiconductor Field Effect Transistor (MOSFET). MOSFETs have the great feature that as they become smaller they also become cheaper, dissipate less power, become faster, and more functions per unit area of silicon can be achieved. As a result, denser silicon integrated circuits can be realized, providing superior performance at reduced cost per function. Figure 1.2 shows the latest version of Moore's law, which shows the introduction of the world's first processor with 2 billion transistors.

The need of a more accurate estimate defined by the International Technology Roadmap for Semiconductors (ITRS) [3], which has been forecasting and driving the pace of semiconductor technology at the same time. Figure 1.3 and Figure 1.4 shows the last decade evolution of the transistors gate length , as well as the predictions made for future by ITRS Roadmap.

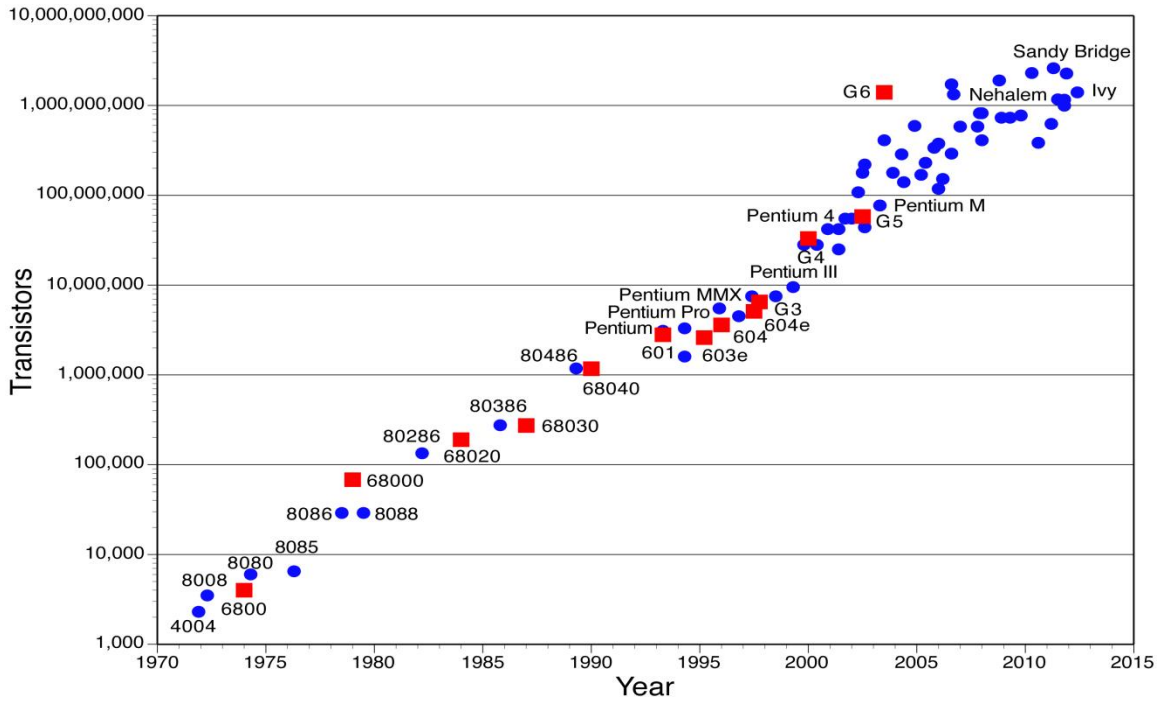


Figure 1.2 Plot of transistor count against dates of introduction – following Moore's law.

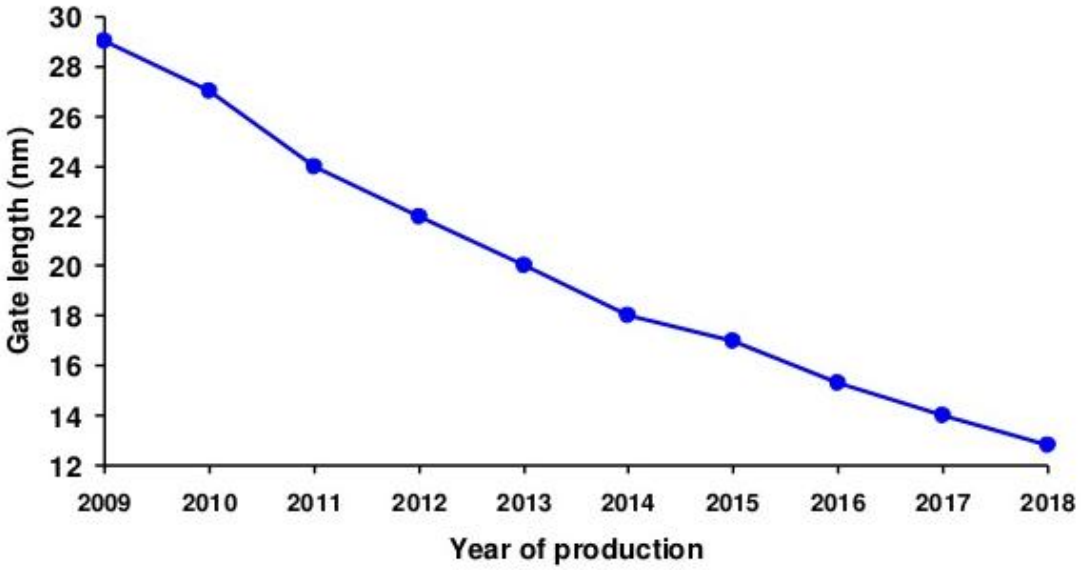


Figure 1.3 MOORE'S Law defined by the International Technology Roadmap for Semiconductors.

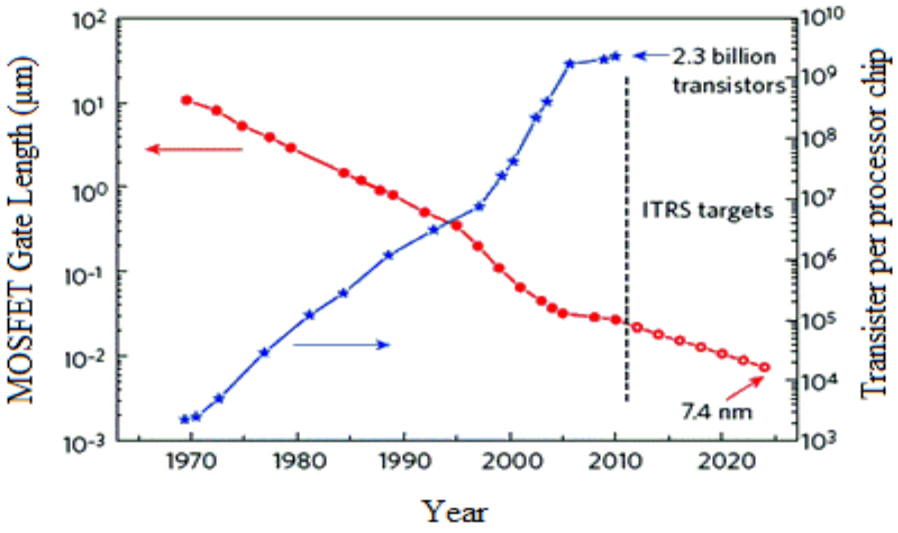


Figure 1.4 Predicted ITRS Roadmap for the next decade.

1.3 Challenges in Scaling Conventional MOSFETs

Figure 1.5 shows a schematic of a conventional MOSFET built on bulk-Si substrates. When conventional MOSFET is used in digital logic applications, the gate is used as a control terminal to switch on or off a current conduction channel between the source and drain terminals. The current carriers can be either holes (in an p-type MOSFET, called PMOS FET) or electrons (in a n-type MOSFET, called NMOS FET).

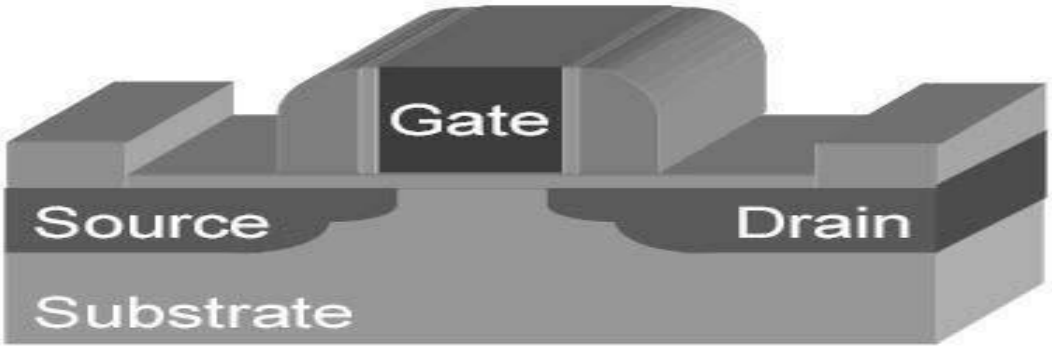


Figure 1.5 Schematic of a conventional bulk MOSFET .

In order to implement the bulk MOSFET, heavily (n or p) doped polycrystalline silicon is used to make gate electrode. It is separated from the bulk silicon substrate by a thin insulating layer of silicon dioxide. The channel region under the gate is moderately

doped. The electrode contacts are formed on source and drain regions and are heavily doped to form p-n (or n-p) junctions to the oppositely doped substrate. In the simplest scaling approach [6] the vertical and horizontal dimensions as well as the supply voltage are reduced by the same factor to keep the electric fields in the scaled MOSFET the same as before (constant-field scaling). However, in actual scaling implementations slightly modified approaches are incorporated where the geometry and voltage are reduced by different factors.

In the early generation transistors having large gate lengths (long channel MOSFETs), the vertical electric field in the channel due to the applied gate to source voltage is much larger than the lateral channel electric field due to the applied drain to source voltage. In such a case of gradual channel approximation, the transistor operation can be partitioned into two independent portions, i.e. gate-controlled charge formation in the channel, and drain-controlled charge transport. The threshold voltage V_T (at which the device turns on) is dependent only on the gate voltage and independent of the drain voltage. When gate voltage is applied it lowers a potential barrier near the source and allows carriers (electrons or holes) to flow from source to drain. The sub-threshold swing is a measure of how sharply the drain current increases as a function of gate voltage during switching from 0 V to V_T. It can be measured in mV/dec. (mV of incremental gate voltage required to change the drain current by one decade), under normal transistor operation fundamental thermodynamics constrains the subthreshold swing to be greater than 60 mV/dec. at room temperature. Degraded 2-D electrostatics at short gate lengths worsen (increase) this value – leading to higher off-state leakage current for the same V_T.

The potential barrier at the source is controlled by the gate as well as the drain because of their respective coupling capacitances to that point. The gradual channel approximation is just a simplification of the complicated two-dimensional (2-D) electro-statics in the MOSFET channel. Long channel devices are simple, as the gate length is reduced, the drain influence becomes stronger. As a result, it becomes harder for the gate to control the source barrier and turn off the channel.

The 2-D effects are manifested in various ways:

i) The reduction in threshold voltage (V_T) with shrinking gate length (V_T roll-off),
ii) The reduction in threshold voltage with increasing drain voltage (drain induced barrier lowering – DIBL),
iii) Degraded subthreshold swing.

These phenomena are known as 'short channel effects' (SCE) which tend to increase the off-state static leakage power. Thus far, device designers have tried to suppress SCE in short gate length devices by a number of methods:

i) By reducing the gate oxide thickness to improve the gate control over the channel,
ii) By lowering the source/drain junction depth (especially near the gate edge, where the source/drain regions are called 'extensions') to reduce the drain coupling to the source barrier,
iii) By increasing the channel doping to terminate the electric field lines which originate from the drain and propagate towards the source. In modern bulk MOSFETs, the channel doping is tailored to have complicated vertical and lateral profiles (super-halo doping) [30] so as to minimize the impact of gate length variations on the short channel effects.

Each of these approaches either degrades transistor performance (speed) or introduces a new static leakage mechanism:

i) As the gate oxide gets very thin, quantum mechanical tunneling allows gate leakage current to flow. In the direct-tunneling regime, the gate leakage current increases dramatically (~3x for every 1 Å thickness reduction) for oxides thinner than about 3 nm. The gate leakage can increase standby power as well as compromise proper dynamic logic operation [5]. Many papers have been proposed replacing the silicon dioxide (SiO_2) with higher permittivity (high-k) gate dielectrics such as zirconia (ZrO_2) or hafnia (HfO_2). These enable high gate capacitance with physically thick insulators through which tunneling is low. However, the introduction of new materials without the degradation of mobility and reliability is very challenging and

remains an area of ongoing research.

ii) If the source/drain junctions are made shallower, their doping have to be increased so as to keep the sheet resistance constant. The solid solubility of dopants puts an upper limit (~ 10^{20} cm^{-3}) on the doping density. Therefore, a further reduction in the junc-tion depth causes an increase in the series resistance in accessing the channel. This degrades the overall transistor performance. Thus, from a technological point of view, it becomes difficult to form ultrashallow junctions that remain abrupt after the annealing steps needed to activate the dopants and achieve low resistivity.

iii) As the doping density in the channel is increased for SCE suppression, the carrier mobility is degraded due to increased scattering from the ionized dopant atoms. Besides, the subthreshold swing gets worse due to higher depletion capacitance that 'steals' away part of the gate voltage from the surface potential. For very high channel doping near the source/drain extensions, another component of static leakage, band-to-band tunneling, becomes important. Finally, as the channel volume reduces in extremely scaled transistors, the random placement of discrete dopant atoms cause stochastic inter-device variations [10].

As a result of these problems, it is becoming clear that new materials and/or structures will be needed to supplement or even replace the conventional bulk MOSFET in future technology generations.

1.4 Recent Structural Advancements

Over the past several decades, the extraordinary evolution of microelectronics has thus been made possible together by continuously shrinking the size of the transistors and also materials used for fabrication that has changed from bulk silicon wafers to Silicon-on-Insulator (SOI) wafers. Within the SOI planar technology, two distinct families of devices are classically considered as shown in Figure 1.6, namely partially depleted (PD) and fully depleted (FD) MOSFETs. The main advantage of this wafer is the reduction of all the parasitic effects from the silicon substrate [11]. In FD MOSFETs, the thickness of the silicon film is reduced in such that the depletion region below

the inversion channel extends down to the buried oxide. In this case, the entire Si film is depleted from free carriers.

When the film is made thicker the depletion region can be stopped at certain depth within the silicon film, which leaves an un-depleted region above the buried oxide known as the body. For this reason such devices are referred as partially-depleted MOSFETs. The floating potential of the body region in PD MOSFETs is responsible for the floating body effects, which affect the device's electrical behavior. The brilliant feature of the FD MOSFET is that the current drive is higher than in bulk MOSFET and its subthreshold slope is sharper, due to a much smaller body factor [12].

FD MOSFETs presents an ideal subthreshold slope, lower junction capacitances, which enables the reduction of the threshold voltage and power consumption. For low power analog applications FD technology is much suited [13-14].

In the past decade, we have seen some remarkable technology at work, from just a few devices on a single silicon wafer, to Very Large-Scale-Integration (VLSI) and in the last few years, this has moved to what is known as Ultra-Large-Scale-Integration (ULSI), in keeping with Moore's Law. The latest trend in device scaling has almost faithfully followed a universal scaling rule [15] that is derived from the assumption of simple electrostatics and the classical physics of ideal gases for transport. However, with device sizes entering the deep sub-micron (< 0.1 mm gate length) regime, several additional elements of the detailed transport physics have required attention to understand device behavior adequately.

These range from purely classical effects caused by the onset of ballisticity in the transport, such as hot-carrier effects [8], velocity overshoot [9], and impact ionization [10], to purely quantum mechanical effects due to the wave nature of the charge carriers in semiconductors. This constant shrinking has its limits, and we have reached the point where materials and device issues are starting to arise and opening the doors for alternative device structures. The most promising SOI devices for the nanoscale range are based on multiple gate structures, such as the double-gate (DG), the triple gate or

fin- shaped field-effect transistor (FinFET), and the surrounding gate (SGT) or gate-all-around (GAA) [19]. The definition of the various multiple-gate structures can be easily mistaken if not defined properly based on their physical gate dimensions.

Figure 1.7 shows some of the multi-gate MOSFETs. The multiple-gate architecture has some interesting characteristics that are present in the section.

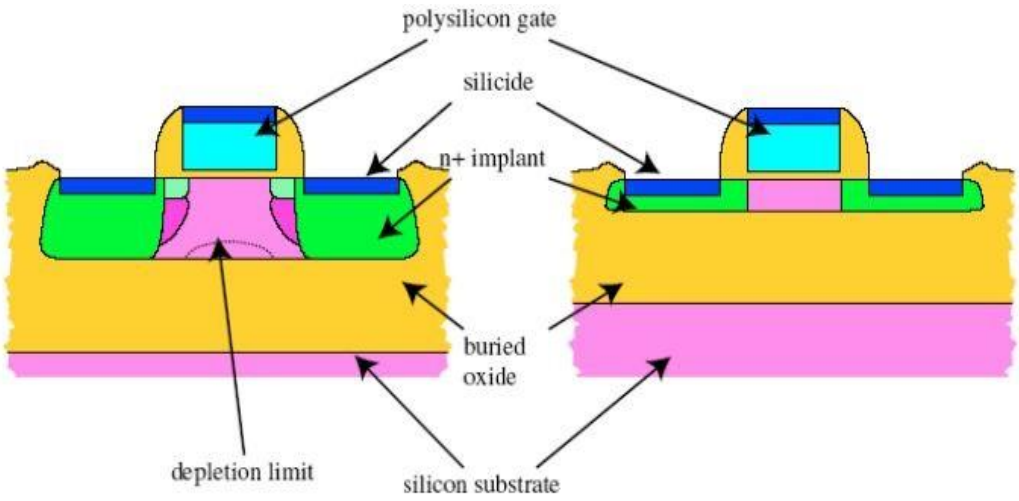
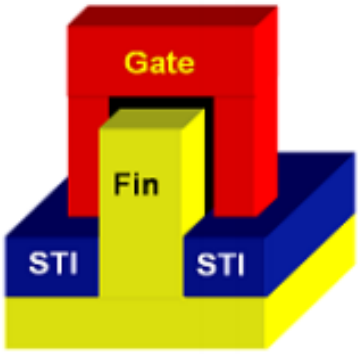
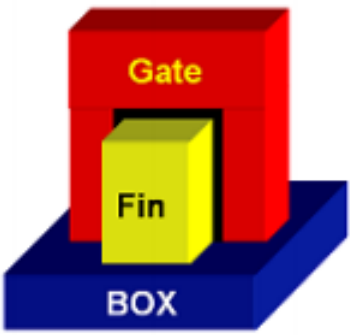


Figure 1.6 Partially depleted and Fully depleted SOI MOSFETs .

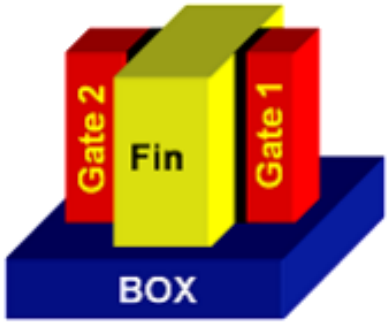


(a) Triple-gate FinFET on Bulk Si

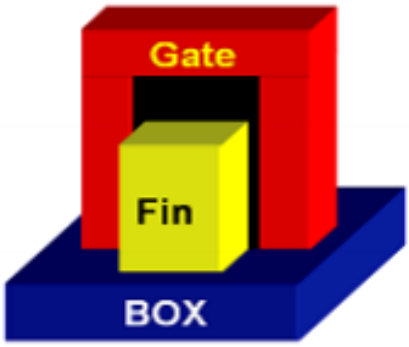


(b) Triple-gate FinFET on SOI

(c) Planar Double-gate on SOI



(d) Independent Double-gate FinFET on SOI



(e) Double-gate FinFET on SOI

(f) Gate-all-around

Figure1.7 Various structures of MOSFETs. (BOX: buried oxide; SOI: silicon-on-insulator) [21].

1.5 Advantages of Multi-gate MOSFETs

One of the most important advantage is the gate control over the electrostatic charges. The increased charge control in the channel translates into improved short channel effects [12]. Since the channel (body) is controlled electrostatically by the gate from multiple sides, the channel is better-controlled by the gate than in the conventional transistor structure. Leakage components are reduced and a small transistor can be used to continue the cost reduction through miniaturization. Lower output conductance is obtained through improved gate control. This provides greater voltage gain, which is beneficial to noise tolerance of digital circuits as well as analog circuits. Another

distinct characteristic of multiple-gate devices is the increased current and therefore faster circuit speed [23]. One of the essential advantages of using multiple-gate devices is the highly improved electrical characteristic in the subthreshold regime [24]. The drain induced barrier lowering (DIBL) characteristic of a FD multiple-gate transistor is much improved over a normal SG MOS transistor [25]. The volume inversion phenomenon can be found only in multiple-gate architectures. If a device is operating in volume inversion there is a strong coupling between two conducting channels [26]. In multiple gate devices, the use of a very thin film allows to downscale the devices without the need of using high channel doping densities and gradients [27]. In fact, undoped films can be used: the full depletion of the thin film prevents punch-through from happening. Besides, the absence of dopant atoms in the channel increases the mobility by suppressing impurity scattering . Multiple gate nanoscale devices have many advantages in circuit performance. A very high packaging density is possible because of the small size of these devices, caused by the short channel and the thin film. Transconductance cab be higher because of the higher mobility, which allows a higher operating frequency and gives more current gain. Therefore, multiple gate nanoscale devices have a big potential for RF and microwave applications . The analog performance is also remarkable. Voltage gain is much higher than in conventional bulk MOSFETs, and especially in moderate inversion.

Chapter 2

Literature Review

2.1 Scaling [28]

- Reduction in size of an MOS chip by reducing the dimensions of MOSFETs and interconnects.
- Reduction is symmetric and preserves geometric ratios which are important to the functioning of the chip. Ideally, allows design reuse.
- Assume that L is the scaling factor. Then a transistor with original dimensions of L and W becomes a transistor with dimensions L/S and W/L.
- Typical values of S: 1.2 to 1.5 per biennium.
- Two major forms of scaling

  Full scaling (constant-field scaling) – All dimensions are scaled by *S* and the supply voltage and other voltages are so scaled.

  Constant-voltage scaling – The voltages are not scaled and, in some cases, dimensions associated with voltage are not scaled.

2.2 Goals [28]

- Understand constant field and constant voltage scaling and their effects.
- Understand small geometry effects for MOS transistors and their implications for modeling and scaling.
- Understand and model the capacitances of the MOSFET as:

  Lumped, voltage-dependent capacitances.

  Lumped, fixed-value capacitances.

- Be able to calculate the above capacitances from basic parameters.

Table 2.1 MOS Scaling [39]

Quantity	Sensitivity	Constant Field	Constant Voltage
Scaling Parameters			
Length	L	$1/S$	$1/S$
Width	W	$1/S$	$1/S$
Gate Oxide Thickness	t_{OX}	$1/S$	$1/S$
Supply Voltage	V_{dd}	$1/S$	1
Threshold Voltage	V_{T0}	$1/S$	1
Doping Density	$N_{A,}N_D$	S	S^2
Area (A)	WL	$1/S^2$	$1/S^2$
β	WLt_{OX}	S	S
Device Characteristics			
D-S Current (I_{DS})	$\beta(V_{dd} - v_T)^2$	$1/S$	S
Gate Capacitance (C_g)	WL/t_{ox}	$1/S$	$1/S$
Transistor On Resistance (R_{tr})	V_{dd}/I_{DS}	1	$1/S$
Intrinsic Gate Delay (τ)	$R_{tr}C_g$	$1/S$	$1/S^2$
Clock Frequency	f	f	F
Power Dissipation	$I_{DS}V_{dd}$	$1/S^2$	S
Power Dissipation Density (P/A)	P/A	1	S^3

In constant field scaling, the voltage and all physical dimensions are reduces by the factor of S but the field remains constant. The doping concentration increased by the factor of S^2 according to the poisson's equation. In this paper [29], a latest scaling technique is proposed named Generalized scaling.

2.3 Generalized Scaling

In [29], a generalized scaling technique is proposed in which scaling of all physical dimensions and applied voltages are independent while electric field pattern remains constant. Thus the short channel effect is under control even if the field intensity is increased.

Table 2.2 Generalized Scaling [29]

Physical parameter	Generalized Scaling
Length (L)	$1/S_L$
Width (W)	$1/S_L$
Voltage (V)	$1/S_V$
On-current per device (I_{DS})	S_T/S_V^2-$S_T/(S_V S_L)$
Capacitance (C)	S_T/ S_L^2
Gate delay (τ)	S_V/ S_L^2-$1/S_L$

2.4 Short Channel Effects

In 2003, K. Roy et al. [30] introduced the leakage current mechanism known as short channel effect. This paper describes the various form of leakage current explained below:

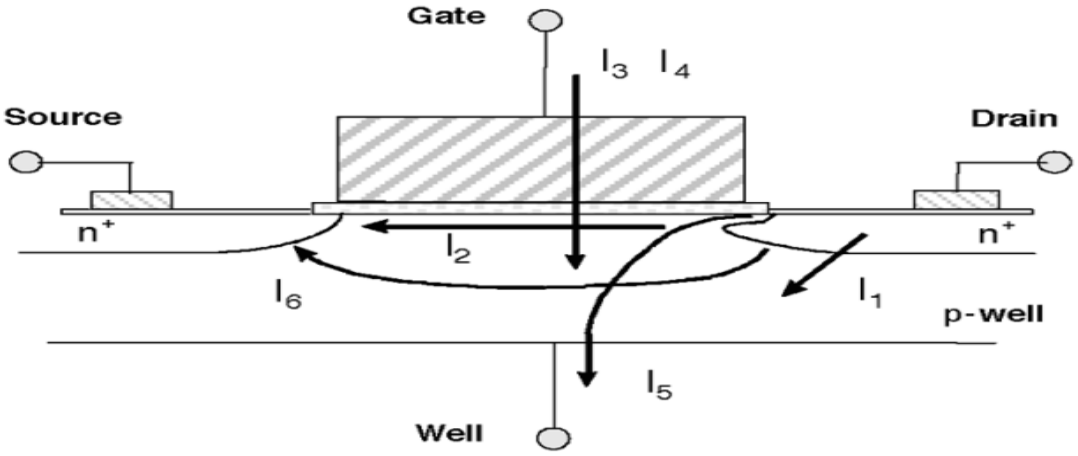


Figure 2.1 Various type of leakage current in short channel MOSFET [30]

1. PN Junction Reverse Bias Current

This type of leakage current is due to reverse biasing of drain or source to substrate junctions. A PN diode is formed at these junction, which causes a reverse biased leakage current (I_1) as shown in the Figure 2.1

2. Sub threshold Leakage Current

In MOS transistor, when the gate voltage is below threshold voltage (V_{th}), the transistor works in weak inversion mode and the drain current is considered as the leakage current also called subthreshold leakage current as shown in the Figure 2.1 as I_2.

3. Tunneling Current

This leakage current is explained by the quantum physics not by the classical physics. Due to the scaling when the gate oxide thickness decrease sufficiently the electric field of oxide is increased in drastic manner. So, the electrons tunnel from channel to gate and gate to channel through gate oxide. This current I_3 as shown in Figure 2.1 due to electron tunneling is referred as the leakage current because in ideal MOSFET the gate current is zero.

4. Injection of Hot Carriers from Substrate to Gate Oxide

Due to the high Electric field in the Si-SiO_2 interface, electrons and holes gains the sufficient energy to cross the interface potential. This effect is known as the hot-carrier injection. This current is shown in Figure 2.1 as I_4.

5. Gate-Induced Drain Leakage

High electric field in the drain junction of MOSFET causes the Gate-Induced Drain Leakage Current (I_5) as shown in Figure 2.2. Accumulation layer formed at the silicon surface is formed due to gate biasing. The surface behaves like a p region due to accumulated holes more doped then substrate causes the narrow depletion layer at the surface. This narrowing of the depletion layer increase the local electric field.

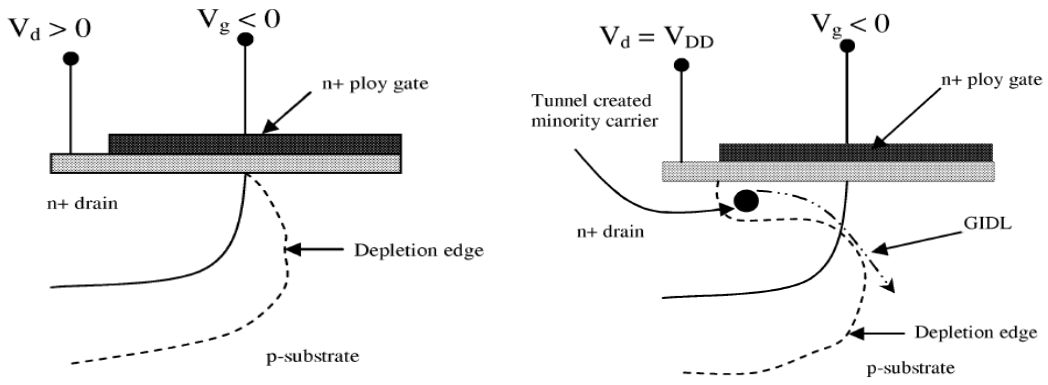


Figure 2.2 Gate-Induced Drain Leakage

6. Punchthrough Effect

The depletion regions at source-substrate and drain-substrate in the short channel devices extend to the channel. The distance between the depletion boundaries reduced as the channel length is reduced. The junctions become nearer as the reverse bias is increased across the junctions. Merging of the depletion regions due to channel length and reverse bias is called Punchthrough effect.

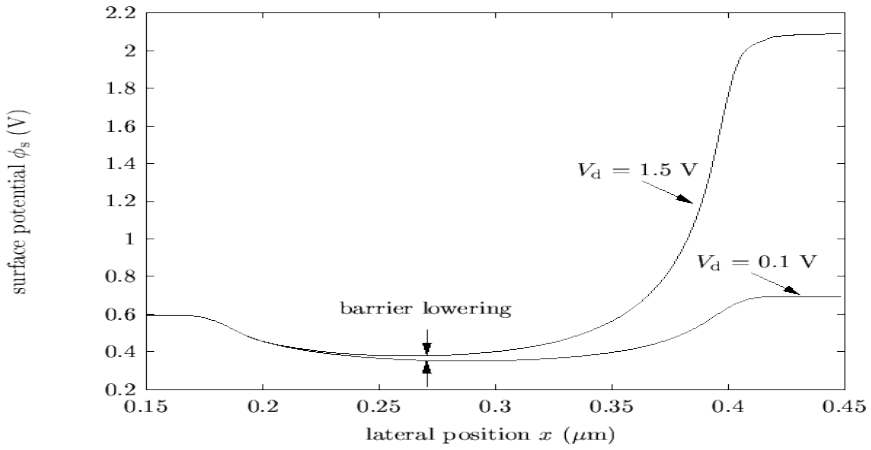


Figure 2.3 Potential distributions according to channel

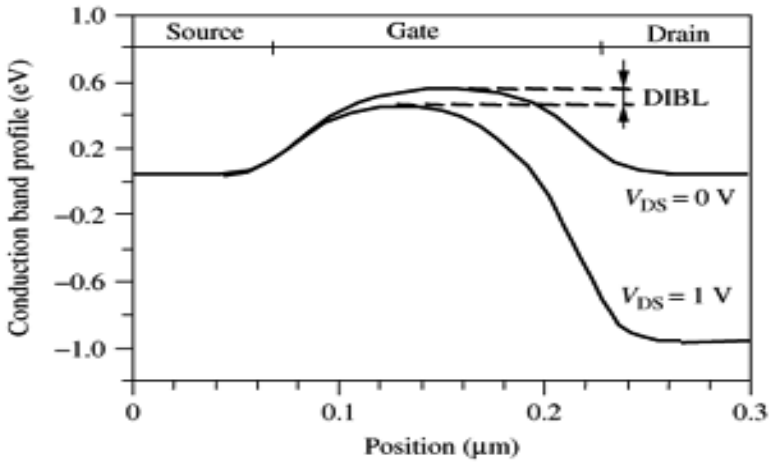


Figure 2.4 Conduction band profile

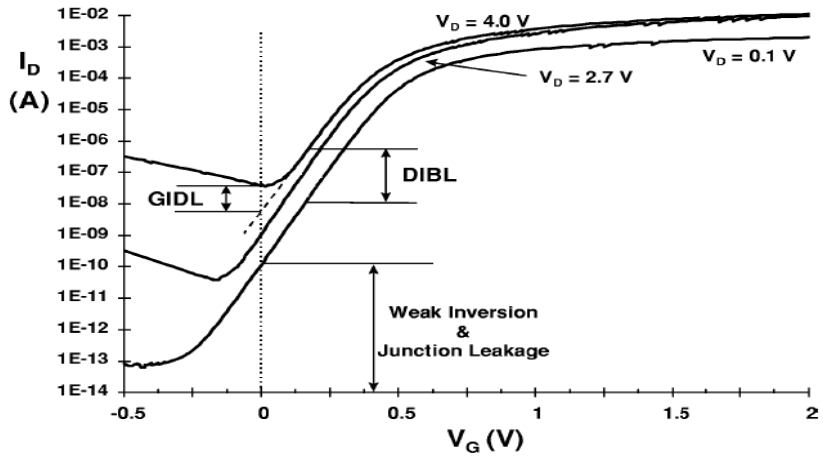


Figure 2.5 I_D-VG characteristic

2.5 Novel Device Structures

Various papers[10-13] [30][32] have been proposed to reduce the short channel effects. Technologies like SOI (Silicon on Oxide), SOS (Silicon on Suphire) and Multi-gate structures like Double Gate, FINFET and Gate all around etc. In this thesis, a double gate MOSFET has been proposed, which reduce the gate leakage current.

The novel device structures will be needed to develop scaling techniques which are explained below:

2.5.1 Double Gate MOSFET [34]

DG MOSFET is considered as the enhanced version of the FD SOI transistor with thin BOX. The Double Gate MOSFET is an evolution of the conventional bulk MOSFET structures. In DG MOSFET a second gate is introduced below the thin body in which channels are formed. While implementing DG MOSFET, same voltage is applied to both gates and the thickness of top and bottom dielectrics is same also referred to as symmetric DG MOSFET.

The main advantage of the DG MOSFET is the better electrostatic gate control over the channel because of the increased scalability. The short channel effect control is very effective due to the thin fully depleted body and gate shielding of drain electric field lines from both sides. Because of two gates devices can be scaled to shorter gate lenghts for the same body and oxide thickness.

Parasitic capacitance in DG MOSFETs

The two gates should be perfectly aligned to each other and should have the same size in order to control the extra parasitic capacitance due to the bottom gate in the DG MOSFET. The node capacitances originate from transistors as well as from the interconnections between them. The three main components of this capacitance are

1) gate to channel capacitance: this capacitance is intrinsic to any FET as it contributes to the drive current.

2) drain to substrate capacitance: this capacitance is not significant in DG MOFET due to the presence of buried oxide layer drain and substrate wafer.

3) gate to drain/source capacitance: this capacitance is source of the parasitic capacitance in DG MOSFETs.

Types of DG MOSFET:

1. Planar DG MOSFET

2. Non- Planar DG MOSFET

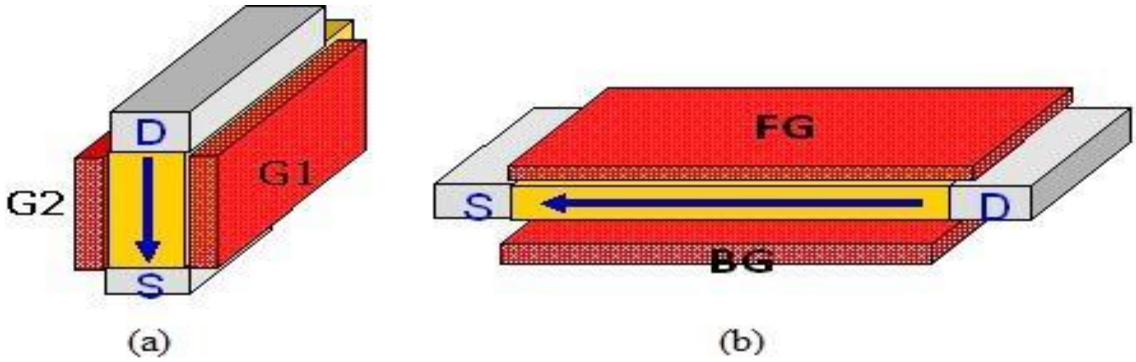


Figure 2.6 DG MOSFET (a) Non-plannar, (b) Plannar

In planar DG MOSFETs, gates are placed parallel to the horizontally oriented thin silicon layer. Any misalignment between theses gates, increased the gate to source/drain capacitance. Also, in some implementations of planar DG MOSFETs, the bottom gate may be sized somewhat differently than the top gate. This too leads to increased parasitic gate overlap capacitance.

Operation:

In order to understand the operation of the FET we consider the gate bias effect on the source body diode. In the off-state, the body doping and/or gate work function is chosen so as to have a large built-in voltage at the source-body junction. There is a huge barrier of electrons which prevents them to diffuse from source to body. Surface potential increases as the as the gate bias voltage increases which reduces the source barrier. Therefore, the gate turns on the source body junction by forward biasing it. As the source barrier is lowered, the electron injection into the body due to thermal emission over the barrier increases exponentially. This is due to the exponentially increasing number of Fermi-Dirac distributed available electrons as the barrier height is lowered. The sub-threshold current thus generated is constrained to increase at a maximum rate set by kT where k is the Boltzmann constant and T is the absolute temperature.

2.6 Gate Leakage Current [35]

With continuous down scaling the device size the gate oxides become thin and the leakage current flow from the channel to gate. The gate cannot be considered as the

ideally insulated electrode. This changes the power consumption due to the static gate current. Gate leakage current increases exponentially as the oxide thickness is reduced. In order to decrease the effective oxide thickness, high dielectric materials can be used. The thin gate oxide reduces the short channel effect and improves the driving capability of a MOSFET. There are two tunneling mechanisms responsible or gate leakage:

1. Fowler-Nordheim tunneling.
2. Direct tunneling.

2.6.1 FN Tunneling [30]

At lower gate voltages, FN tunneling takes place in which electrons tunnel from the conduction band of silicon substrate to the conduction band of polysilicon gate through the conduction band of SiO_2. In this case, the oxide conduction band is triangular in nature. FN tunneling is valid for $V_{ox} > \phi_b$ where V_{ox} is the voltage drop across the oxide and ϕ_b is Si/SiO_2 barrier height.

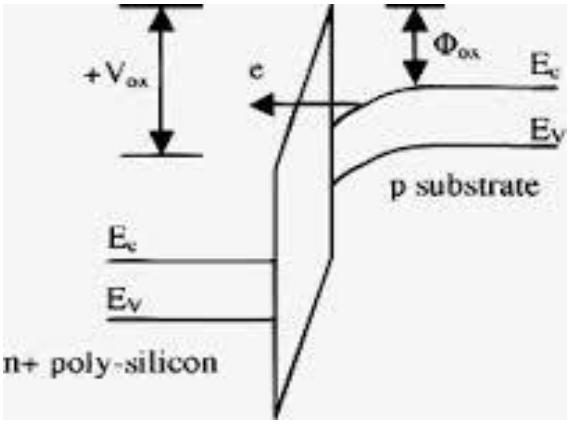


Figure 2.7 FN tunneling in a MOSFET.

2.6.2 Direct Tunneling [36]

In the case of ultrathin oxide MOSFET, the electric field across the ultrathin gate oxide is so high that direct tunneling of electrons takes place which is impossible to explain using classical physics. This tunneling is more pronounced in the thin oxides, e.g. 4nm or less. The electrons tunnel directly to the gate through the forbidden energy gap of the oxide. In this case, the oxide conduction band is trapezoidal in nature. Direct tunneling is valid for

$V_{ox} > \phi_b$. It can be modeled only by using quantum mechanical theory. In the gate oxide, net current is summation of the FN tunneling and the direct tunneling. Usually, the FN current is very small and can be neglected. So the net current is from direct tunneling only.

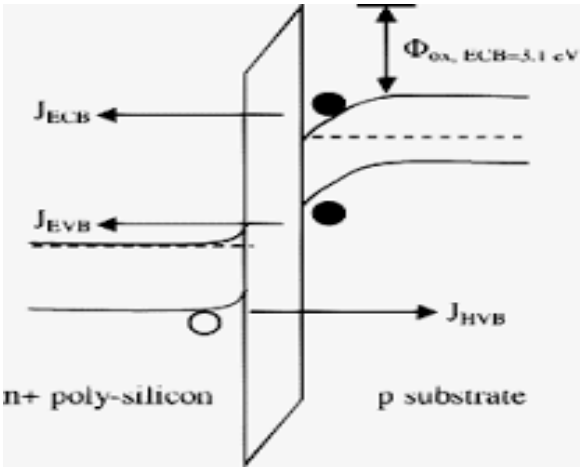


Figure 2.8 Direct Tunneling in a MOSFET.

2.7 Effects on Gate Current [11]

2.7.1 Effects of Oxide Thickness

The gate current increases with decrease in oxide thickness because as the oxide thickness decreases the probability of the carriers to tunnel through the gate insulator will increase, leading to an increase in the tunneling current.[Mohamed atif : study of tunneling current paper] Figure 2.9 shows the gate current as the function of gate voltage at different oxide thickness.

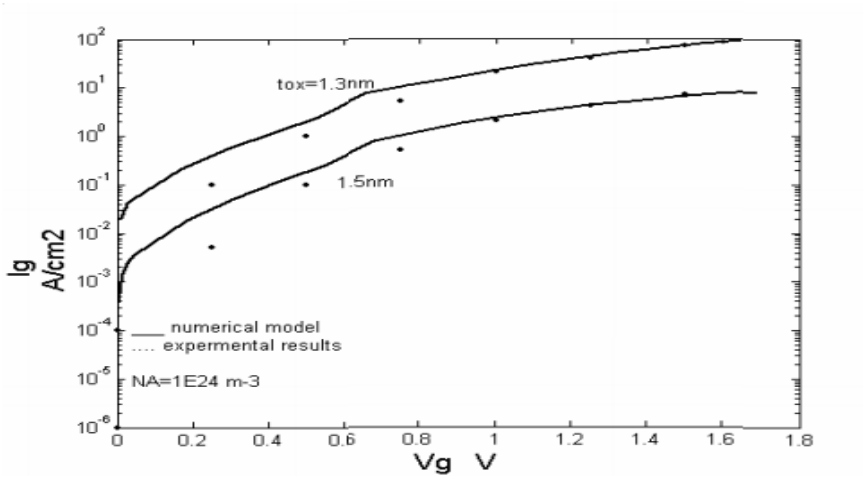


Figure 2.9 Tunneling current as the function of Vg at different values of tox.

2.7.2 Effect of drain voltage on the gate current

To consider the effect of drain voltage on gate tunneling current, the gate tunneling current is calculated as the function of drain voltage for different values of gate voltage as shown in Figure 2.10. The gate current deceases with increase in drain bias because of the increase of surface potential at the drain, which leads to a reduction in the voltage across the insulator.

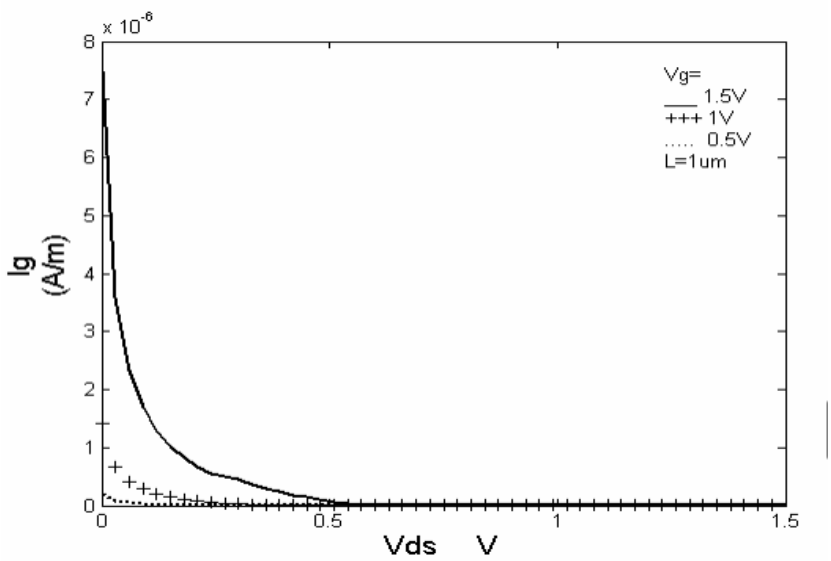


Figure 2.10 Gate current V/S drain voltage characteristic

2.7.3 Effect of Tunneling current on the drain current

The effect of gate tunneling current on drain current is less problematic for short channel MOSFETs due to much higher channel current than gate current. Gate current also decreases with reducing channel length. These gate currents may not be significant for an individual transistor but the sum of all gate currents for the entire chip may cause a serious problem. The effects are shown in the Figure 2.11 below:

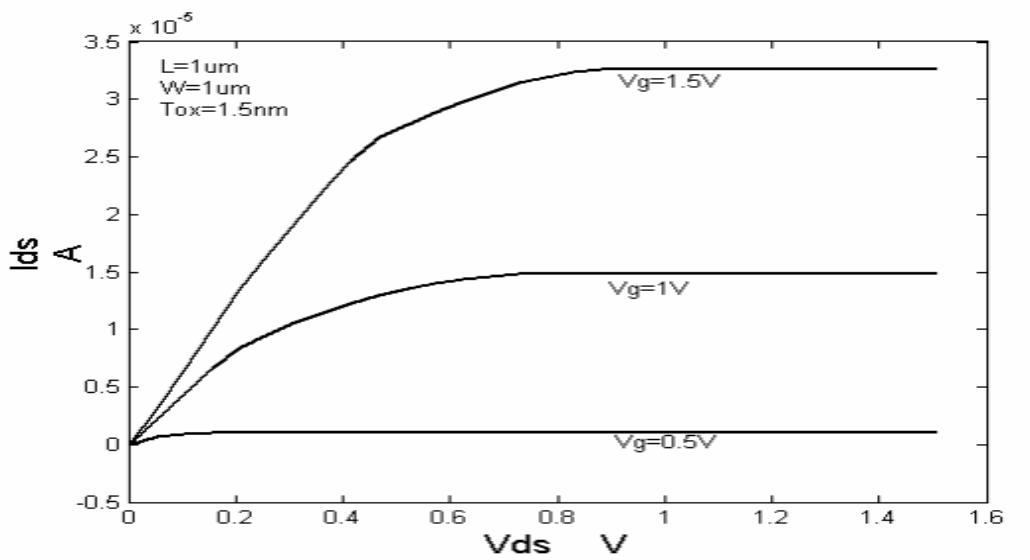


Figure 2.11 Drain current V/S drain voltage characteristic

Chapter 3

Modeling of F-N Tunneling Gate Current

3.1 F-n Tunneling Gate Current

The basic phenomena while calculating this model is that most of the electrons present in the channel region are responsible for drain current. [10] [12] [30] these papers said that the electron are present in the first energy level which is generated by its own, and it is known as quantum effect. for simplicity assume that the drain and source are connected to ground, and basis of [36] rest mass of electron in channel and oxide region have been taken by $0.48m_0$ and $0.98m_0$ respectively where m_0 is the rest mass of electron, here consider that the surface potential at strong inversion is $2\emptyset_f + 6\emptyset_t$,and the other parameter are describe in table 3.1.

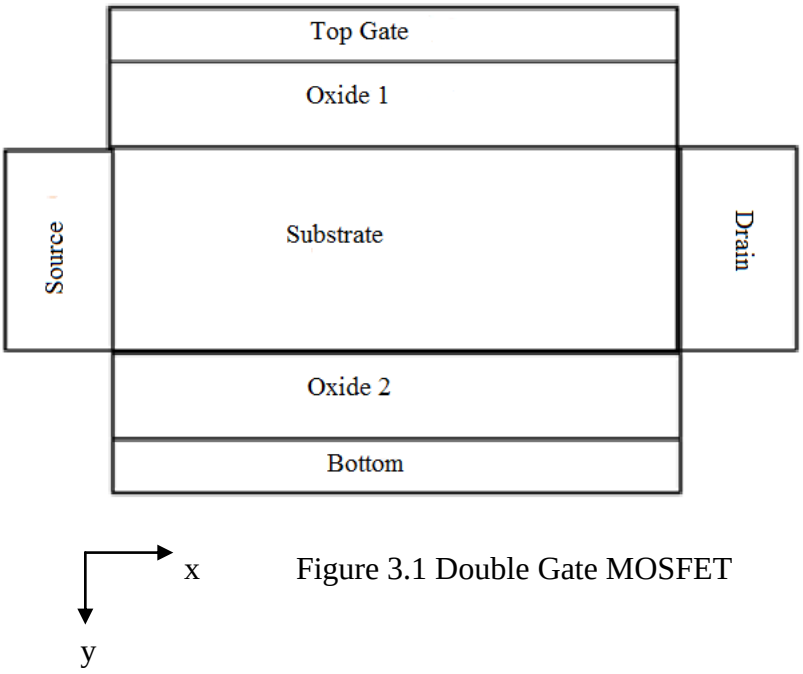


Figure 3.1 Double Gate MOSFET

Here assume that the electric field perpendicular to the channel, and the transverse electric field will be neglected.

To find out Current density in classically forbidden region, the following equation is used:-

$$J = nq|\varphi(x)|^2 vT \quad (1)$$

Where

J= current density

n = number of Electron per unit area

q = charge of the Electron

v = velocity of Electron= $\sqrt{\frac{2E}{m_{si}}}$

T = Tunneling probability

$\varphi(x)$ = Electron wave function

$|\varphi(x)|^2$ = Probability distribution function

When electric field in the interface (Si-SiO_2) is high enough then a potential well is generated near the interface surface. The electron which is present in the well region, shows the wave nature instead of particle nature. It shows that the tunneling through the oxide is purely a quantum phenomena. In the well region, the high potential energy electrons created their own energy level which is calculated by the Time independent Schrödinger one-dimension wave equation.

Here, the gate current is calculated by assuming that the mobility is constant, no trap charges present in the oxide layer and the interface layer is smooth.

So first find the number of electron/hole in the surface area of Si-SiO_2 interface. To finding out number of charges in any region, first calculate the charge distribution function or wave function or probability distribution function.

The commonly used approximation for band bending in the interface of Si-SiO_2, which leads the well known triangular potential well theory. Here assume that oxide electric field is equal to surface electric field.

3.2 Formulation of wave function

The calculation of wave function is necessary for the calculation of the tunneling from the channel conduction band in the surface of semiconductor to the gate conduction band through the oxide layer. Inversion charge and its distribution strongly dependant on the applied gate potential. As the potential on the gate increases, the carrier concentration also increases, and according to the classical physics its closer to the interface but due to the quantum confinement most of the electrons are lies on some distance from the interface.

The energy band diagram of upper gate-oxide and oxide-substrate interface are given in figure 3.2.

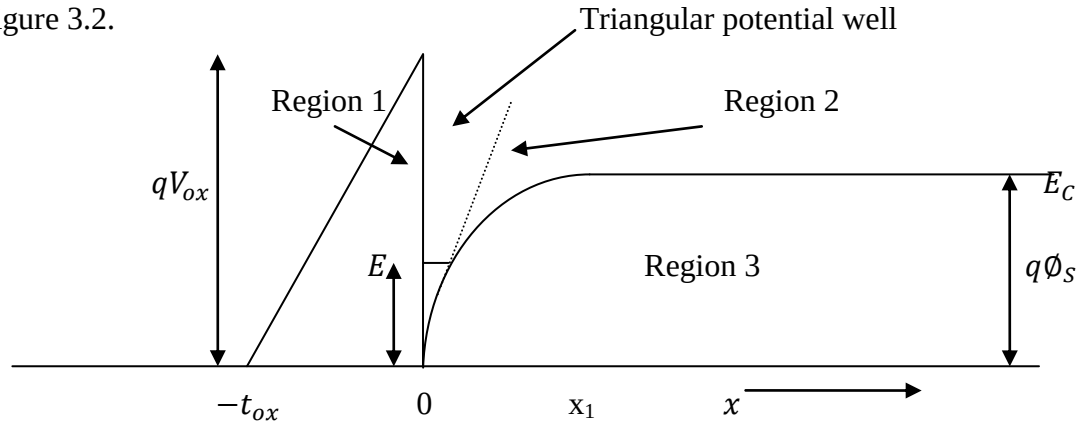


Figure 3.2 Potential Energy diagram

Time independent Schrödinger 1dimension wave equation is:-

$$\frac{\partial^2\varphi(x)}{\partial x^2} + \frac{8\pi^2 m}{h^2}\big(E - V(x)\big)\varphi(x) = 0 \qquad (2)$$

Where

$\varphi(x)$ = wave function of charge particle (electron/hole)

m = effective mass of particle (electron/hole)

h = plank constant

E = energy of particle in the well

$V(x)$ = potential energy function

The Energy of electron in a finite potential well is given by equation 3 [36]. According to the this paper the value of electron's energy in ground state level is 25 % less compare to infinite potential well.

$$E = 0.75\left(\frac{h^2}{8\pi^2 m_{si}}\right)^{\frac{1}{3}}\left(\frac{9\pi q F_s}{8}\right)^{2/3} \quad (3)$$

Where

q = charge of particle (electron/hole)

m_{si} = effective mass of electron/hole in the silicon

F_s = Electric field on the interface of Si-SiO_2

3.2.1 Calculation of Electric field

According to Gauss Law, the electric field in any close bounded region is:-

$$Electric\ Field = \frac{\partial V}{\partial x} = \frac{Q_{inside}}{\epsilon_r} \quad (4)$$

Where

ϵ_r = permittivity of region

$$F_s = \frac{(Q_b + Q_i)}{\epsilon_{si}}$$

The general expression of total charge density in the semiconductor is given by the charge balance equation .

$$Q_b = -\sqrt{(2q\epsilon_{si}N_d\emptyset_s)}$$

$$Q_i = -C_{ox}(V_G - V_{fb} - \emptyset_s - (\gamma\sqrt{\emptyset_s}))$$

$$\gamma = \frac{\sqrt{2q\epsilon_{si}N_d}}{C_{ox}}$$

Where

Q_b = Total charge in the depletion region

Q_i = Total charge due to the inversion charge

ϵ_{si} = Permittivity of silicon

N_d = Doping concentration of donor atom

$\emptyset_s$ = Potential on the surface or interface

C_{ox} = Oxide capacitance

V_G = Applied Gate voltage

V_{fb} = Flat-Band voltage

Various regions of potential energy distribution have been shown in figure 3.2. The figure has been divided into three regions. The first region describes the oxide, second region describe triangular potential well and third region describe the depletion region in a double gate MOSFET.

Region 1 $-t_{ox} < x < 0$

In this region the engery of electron is less then compare to the potential energy in the oxide($E < V_x$), the general solution of time independent Schrödinger 1-dimension wave equation is an exponential decaying function and it is :-

$$\varphi_1(x) = C_1 e^{K_1 x} + C_2 e^{-K_1 x} \tag{5}$$

Where

$K_1 = \sqrt{\frac{8\pi^2 m_{ox}}{h^2}(qV_{ox} - E)}$ = the wave number

$C_1 e^{K_1 x}$ = Forward propagating wave in (– ve) x direction

$C_2 e^{-K_1 x}$ = Diverging wave in (+ ve) x direction

C_2 will be zero because of the diverging solution and the wave function become

$$\varphi_1(x) = C_1 e^{K_1 x} \tag{6}$$

Region 2 $0 < x < w$

In this region, the electric field is constant (as mention previously) in the x direction. According to this the constant electric field, the potential energy of electron varying in a liner manner.

$$V(x) = qF_s x \tag{7}$$

$$x_1 = \frac{E}{q.F_S} \tag{8}$$

When $w > x$, then $V(x) < E$ and when $w < x$, then $V(x) > E$. The solution of Schrödinger time independent equation this time is compressed of airy function [38].

$$\varphi_2(x) = C_3 Ai\left\{\frac{a_1 x - b_1}{(a_1)^{\frac{2}{3}}}\right\} + C_4 Bi\left\{\frac{a_1 x - b_1}{(a_1)^{\frac{2}{3}}}\right\} \tag{9}$$

Where

$a_1 = \frac{8\pi^2 m_{si}}{h^2} qF_s$

$b_1 = \frac{8\pi^2 m_{si}}{h^2} E$

The *Ai* function decays in exponential manner for +ve arguments. The *Bi* function get the diverge solution for +ve values so neglect or discard it. Therefore the solution will come up with the *Ai* function.

$$\varphi_2(x) = C_3 Ai\left\{\frac{a_1 x - b_1}{(a_1)^{\frac{2}{3}}}\right\} \tag{10}$$

Region 3 $w < x < \infty$

For *x* is greater than *w* the potential energy is constant at the distance just considered in the first region. The solutions will again be exponential decay function

$$\varphi_3(x) = C_5 e^{-K_2 x} + C_6 e^{K_2 x} \tag{11}$$

Where

K_2 = wave number $= \sqrt{\frac{8\pi^2 m_{si}}{h^2}(q\emptyset_s - E)}$

In equation 11, C_6 will be zero because it is the solution of the diverging wave. In this thesis, there is no reflection of wave of electron has been assumed, due to this all the diverging coefficient become zero.

$$\varphi_3(x) = C_5 e^{-K_2 x} \tag{12}$$

3.2.2 Outline of the coefficient solving method

Step 1: Impose the boundary conditions in equations (6), (10), (12). The boundary condition of wave function shows that not only the wave functions are equal at boundary but also its derivatives are also equal at boundary due to continuity of wave. First applying the boundary condition on region 1 and region 2 with x = 0.

$$\varphi_1(0) = \varphi_2(0) \tag{13}$$

By using equation (13)

$$C_1 = C_3 Ai\left(\frac{-b_1}{(a_1)^{2/3}}\right)$$

$$\frac{\partial \varphi_1(0)}{\partial x} = \frac{\partial \varphi_2(0)}{\partial x} \tag{14}$$

By using equation (14)

$$C_1 K_1 = C_3 \left(\frac{\partial Ai\left\{\frac{a_1 x - b_1}{(a_1)^{\frac{2}{3}}}\right\}}{\partial x}\bigg|_{x=0} \right)$$

By using equation (13) and (14)

$$C_1 = C_3 a_2$$

$$a_2 = \frac{\left.\frac{\partial Ai\left\{\frac{a_1 x - b_1}{(a_1)^{\frac{2}{3}}}\right\}}{\partial x}\right|_{x=0} + Ai\left(\frac{-b_1}{(a_1)^{2/3}}\right)}{K_1 + 1}$$

Now applying boundary condition on region 2 and region 3 at x = x_1.

$$\varphi_2(x_1) = \varphi_3(x_1) \tag{15}$$

By using equation (15)

$$C_3 Ai\left(\frac{a_1 x_1 - b_1}{(a_1)^{2/3}}\right) = C_5 e^{-k_2 x_1}$$

$$\frac{\partial \varphi_2(x_1)}{\partial x} = \frac{\partial \varphi_3(x_1)}{\partial x} \tag{16}$$

By using equation (16)

$$\left.\frac{\partial Ai\left\{\frac{a_1 x - b_1}{(a_1)^{\frac{2}{3}}}\right\}}{\partial x}\right|_{x=x_1} = -C_5 K_2 e^{-k_2 x_1}$$

By using equation (15) and (16)

$$C_3 = C_5 a_3$$

$$a_3 = \frac{(1 - K_2) e^{-K_2 x_1}}{Ai\left(\frac{a_1 x_1 - b_1}{(a_1)^{2/3}}\right) + \left.\frac{\partial Ai\left\{\frac{a_1 x - b_1}{(a_1)^{\frac{2}{3}}}\right\}}{\partial x}\right|_{x=0}}$$

Step 2: Impose the normalization condition

$$\int_{-\infty}^{\infty} |\varphi(x)|^2 = 1 \tag{17}$$

Expand the equation (17)

$$\int_{-\infty}^{0} |\varphi_1(x)|^2 + \int_{0}^{x_1} |\varphi_2(x)|^2 + \int_{x_1}^{\infty} |\varphi_3(x)|^2 = 1 \tag{18}$$

Using equation (18)

$$C_3 = \sqrt{\frac{1}{a_5}}$$

$$a_5 = \left\{\frac{(a_2)^2}{2K_1} + (a_4)^2\right\}$$

$$a_4 = \int_0^{\infty} \left(Ai\left(\frac{a_1 x - b_1}{(a_1)^{2/3}}\right)\right)^2$$

3.2.3 Calculation of width of potential well (*w*)

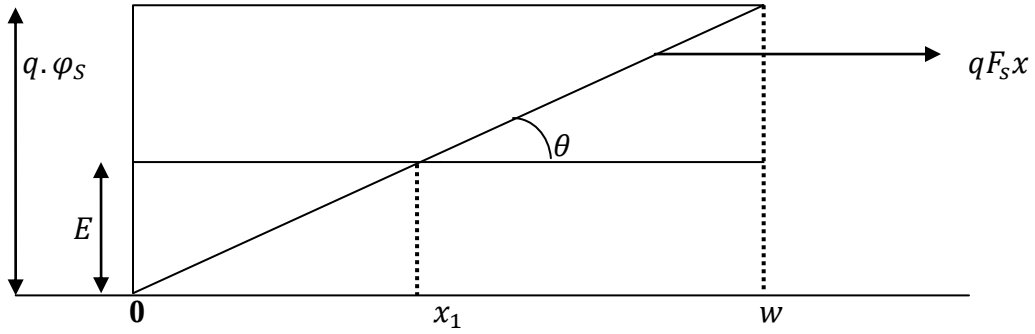


Figure 3.3 Triangular well

$$w = \frac{q.\varphi_S - E}{F_S} + \frac{E}{q.F_S} \tag{19}$$

$$\tan\theta = q.F_S$$

3.3 Number of charge particle

According to charge balance equation the value of total charge density is

$$Q = (V_G - \emptyset_{ms} - \emptyset_s).C_{ox} \tag{20}$$

Using equation (20), the electron density in channel (Q_i) is calculated. The value of (Q_i)is finding by subtracting the depletion charge (Q_d) density from total charge density.

$$Q_d = \sqrt{2q\varepsilon_{si}N_a\varphi_s}$$

$$Q_i = Q - Q_d \tag{21}$$

The number of electrons per unit volume at the channel is calculated by the equation (10) and (21).

$$n = \frac{Q_i}{q}|\varphi_2(0)|^2 \quad (22)$$

3.4 Tunneling probability

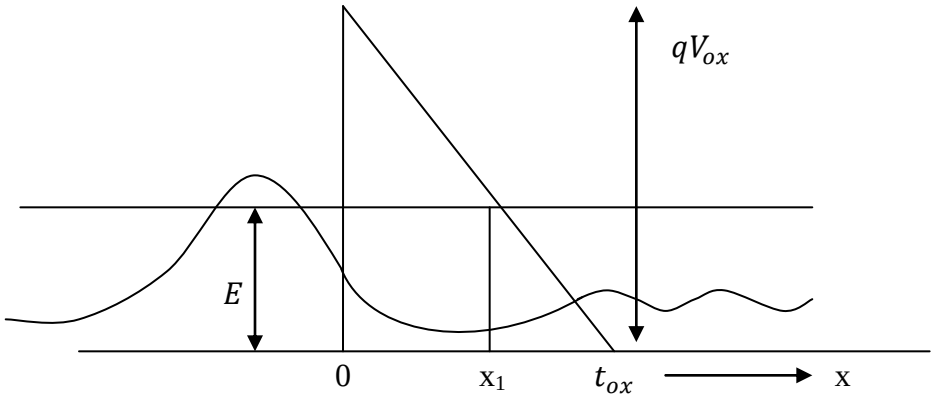


Figure 3.4 Potential energy profile

With the help of the wave function, the value of electron flux tunneling has been calculated which through from the oxide and reach at the gate metal. By using the probability of tunneling and *φ(x)*, the probability density of carriers at opposite side of oxide has been calculated. Tunneling probability given by JWKB approximation is:-

$$T = exp(-G)$$

Where $G = 2\int_{t_1}^{t_2} K'(x)d(x)$

t_2, t_1 is a turning point, and the turning point in which electron energy is equal to potential energy barrier.

$$K'(x) = \sqrt{\frac{8\pi^2 m_{ox}(V(x) - E)}{h^2}}$$

Where $V(x) = qV_{ox} - qF_{ox}x$

$t_1 = 0$

$t_2 = \frac{qV_{ox} - E}{qF_{ox}}$

So, the tunneling probability is given by :-

$$T = exp\left(\sqrt{\frac{8\pi^2 m_{ox}}{h^2}}\left\{-\frac{4}{3}\frac{(qV_{ox}-E)^{3/2}}{qF_{ox}}\right\}\right)$$

Chapter 4

Results and Discussion

In this thesis work,

1. A new model of gate leakage current has been proposed. This new model based on the quantum effect on the charge distribution at the interface.
2. The relationship between the length of triangular well and the gate voltage has been developed.

4.1 Result for modeling of charge distribution profile on the channel region

The modified model of double gate MOSFET, which is introduced in this thesis, has been tested for 40μm N^+ Poly-Si-gated NMOS. The various parameters of MOSFET which is used for these testing have been declared in table 4.1.

Table 4.1: Parameters value for double gate MOSFET

S. No	Parameter Name	Symbol	Value
1	Acceptor atom doping concentration	N_A	1e21~1e24 /cc
2	Gate voltage	V_G	0.0~5.0 V
3	Silicon thickness	t_{si}	30 nm
4	Effective mass of electron	m_0	0.42m K.g.
5	Effective mass of silicon	m_{Si}	0.9 m_0
6	Effective mass of oxide	m_{ox}	0.5 m_0

7	Oxide thickness	t_{ox}	6 nm~3 nm
8	Drain/Source Voltage	$V_{d/s}$	0.0V

4.2 Wave function versus oxide thickness characteristics

The wave function corresponding to the triangular well structure for doping concentration 10^{17}cc and the gate voltage is 2.0 volt, for four different value of oxide thickness (3nm, 4nm, 5nm, 6nm). By analyzing the figure 4.1, it can be concluded that with higher thickness the spread of wave function has increase.

4.3 Wave function versus gate voltage characteristics

The wave function corresponding to the triangular well structure for doping concentration 10^{17}cc and the oxide thickness is 5nm, as gate voltage rise from 2.0 volt to 5.0 volt. One important observation seen by the figure 4.2 is that the value of wave function increases.

4.4 Wave function versus doping concentration characteristics

The wave function corresponding to the triangular well structure for doping concentration varies from 10^{15}cc to 10^{19}cc, the oxide thickness is 5nm, and gate voltage is 2.0 volt. One important observation seen by the figure 4.3 is that the value of wave function increases.

4.5 Gate voltage versus width of triangular well characteristics

The wave function corresponding to the triangular well structure for doping concentration 10^{17}cc and the oxide thickness is 5nm, as gate voltage rise from 0.2 volt to 2.5 volt. One important observation seen by the figure 4.4 is that the inversion layer width decrease from 4nm to 1nm, and also observes that the inversion layer width is proportional to oxide thickness.

4.6 Gate voltage versus number of electron for tunneling

The observations seen in the figure 4.5 shows that with increase in Gate voltage the number of electrons for tunneling increases.

4.7 Gate current density

The results obtained from the proposed model and simulation results are identical with oxide thickness of 4 nm and doping concentration is 4.7e24 / m^3 as shown in figure 4.6. The observations in figure 4.7 and 4.8 shows that with increase in oxide thickness and dielectric material the gate current density decreases. Table 4.2 shows the values of dielectric constants.

Table 4.2 Dielectric constant

Oxide	k
SiO_2	3.9
Si_3N_4	7
Al_2O_3	9
HfO_2	25

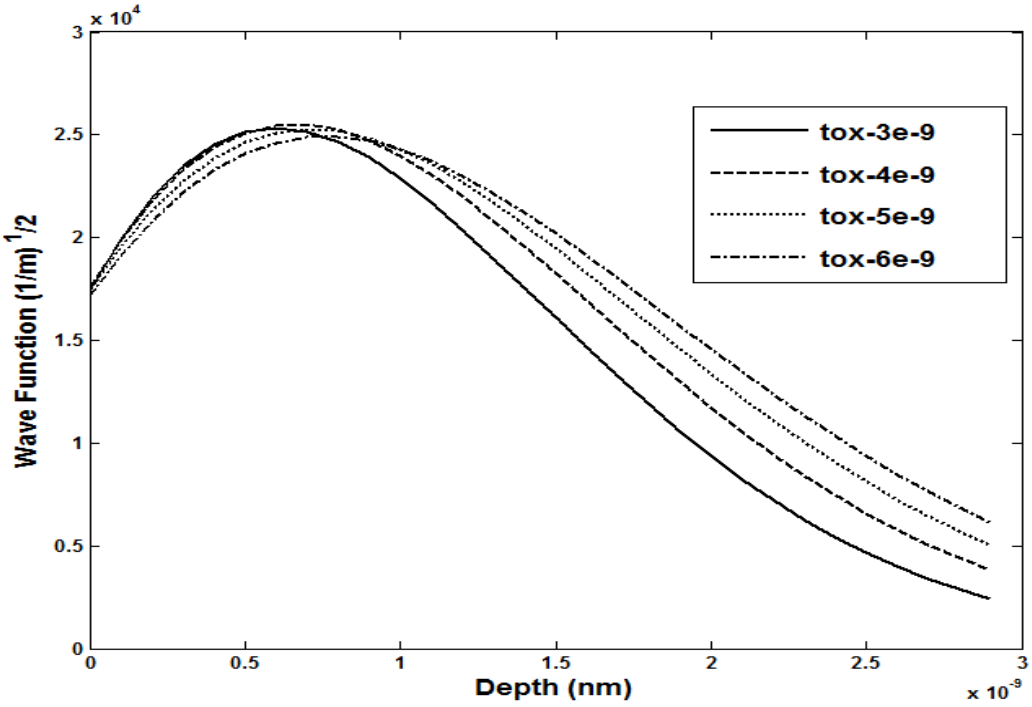


Figure 4.1 Wavefunction versus depth in the semiconductor considering different oxide thichness

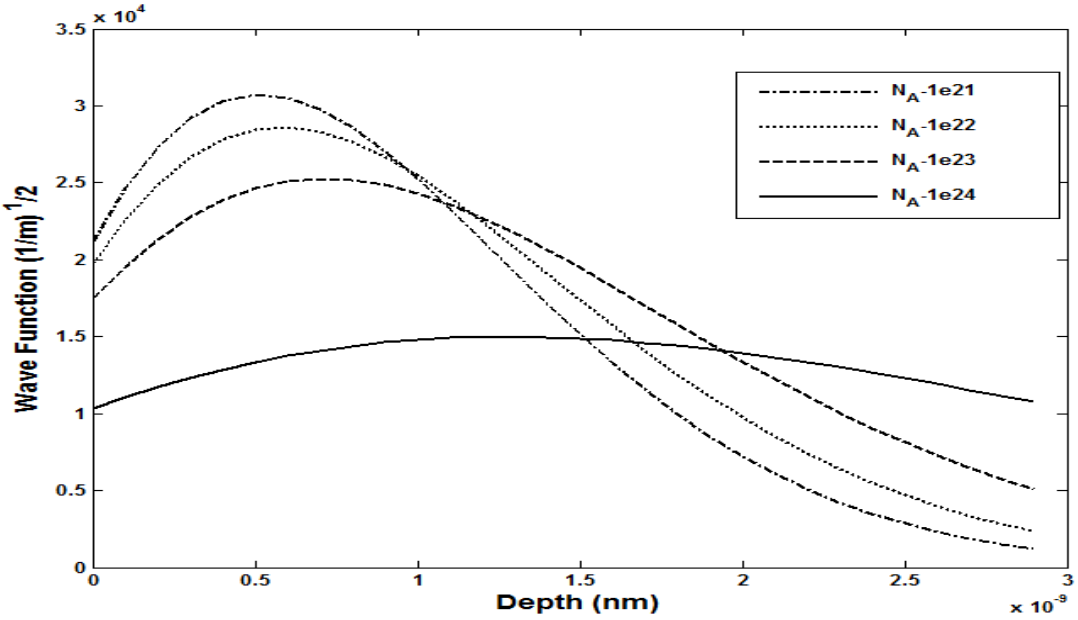


Figure 4.2 \Wavefunction versus depth in the semiconductor with different doping concentration

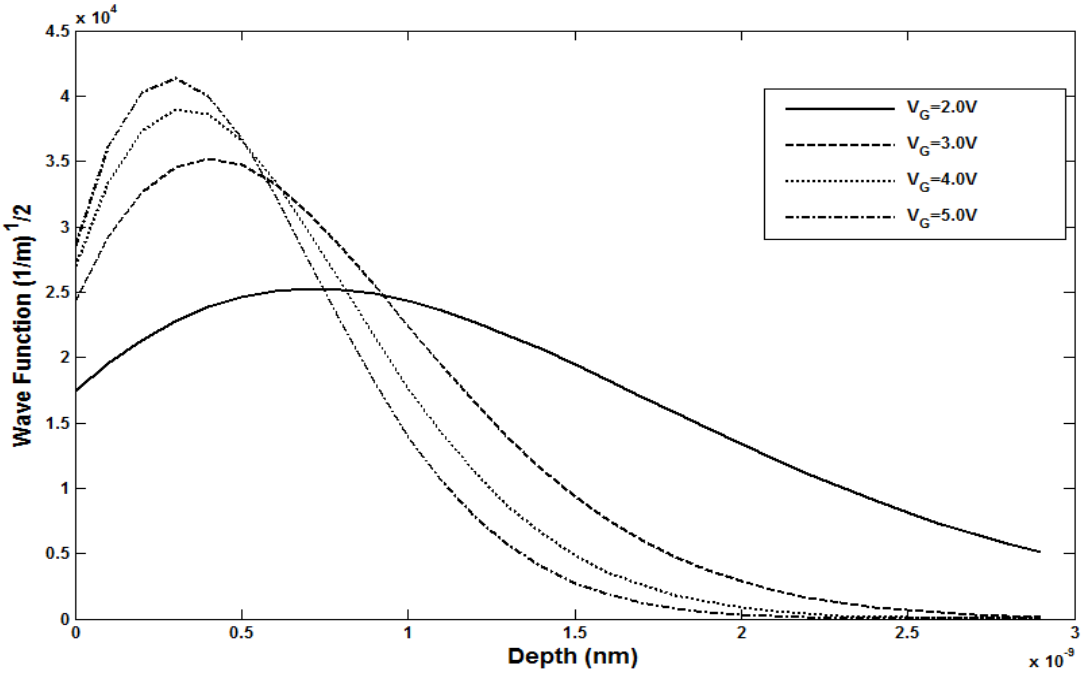


Figure 4.3 Wavefunction versus depth in semiconductor taking different gate voltage

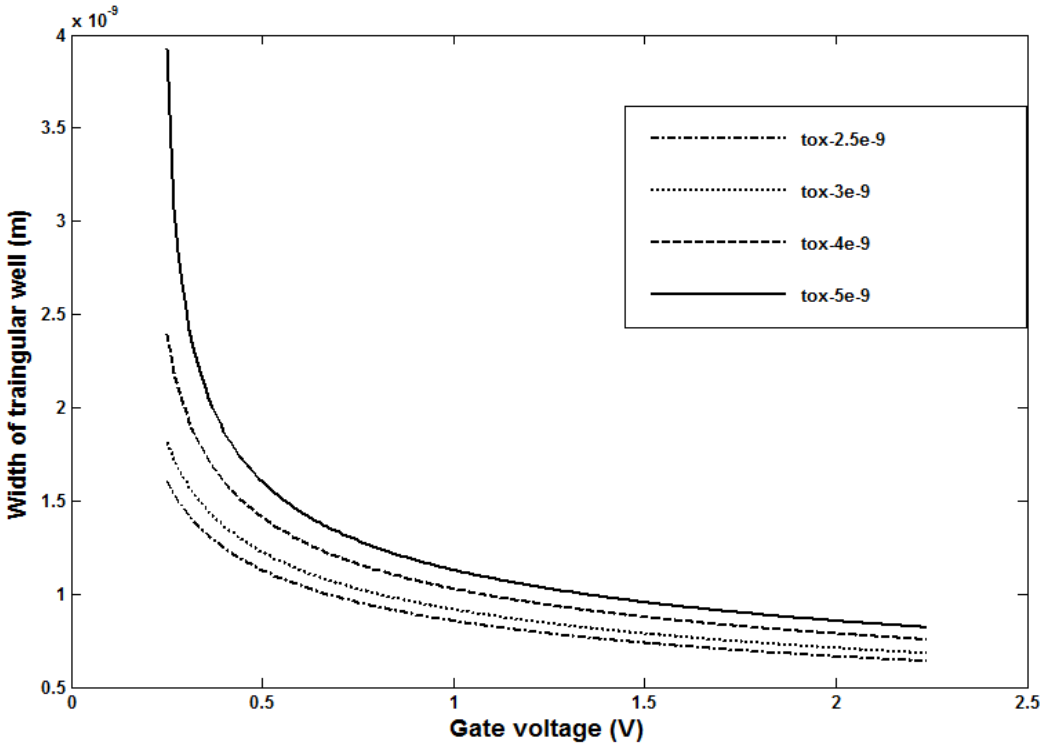


Figure 4.4 Width of triangular well versus gate voltage

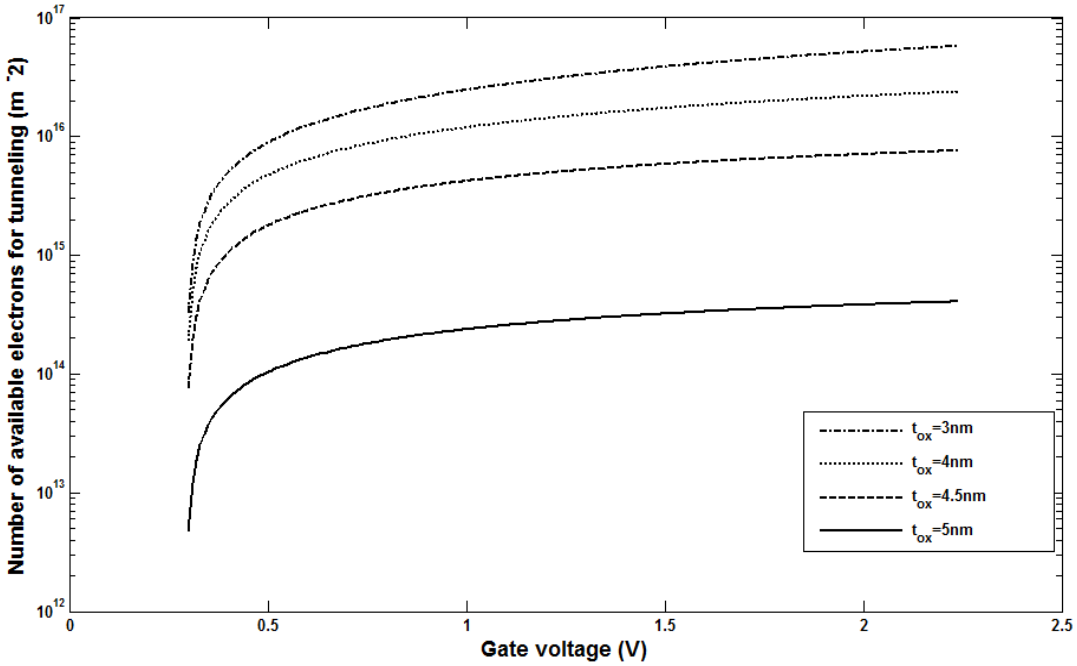


Figure 4.5 Number of available electron for tunneling versus gate voltage for different oxide thickness

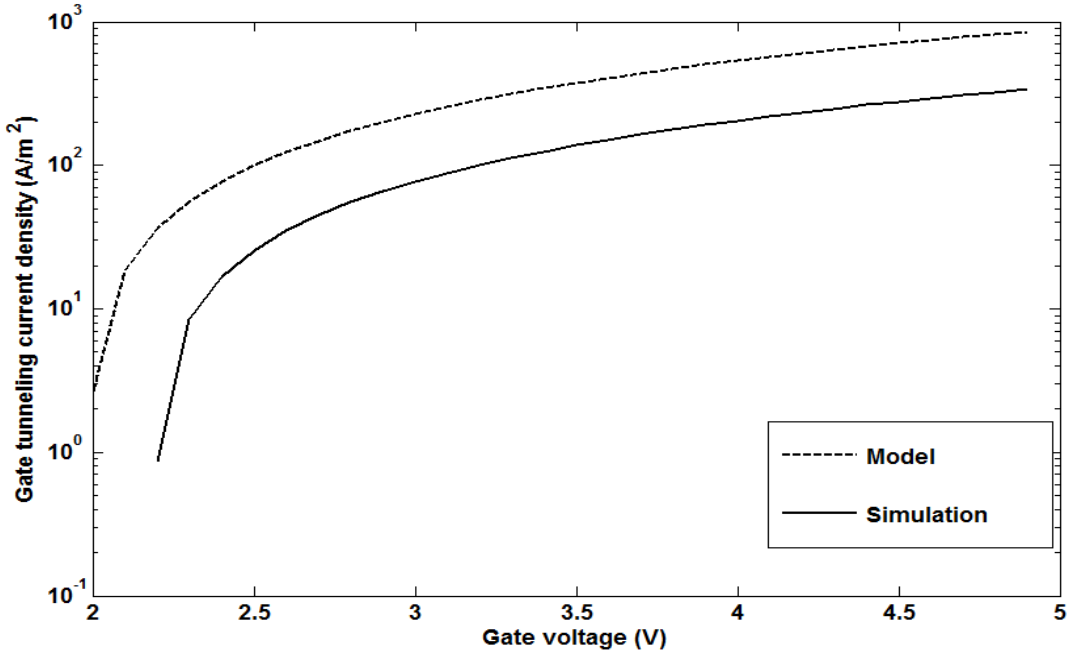


Figure 4.6 Gate tunneling current density versus gate voltage with $\mathbf{t_{ox}}$ = 4 nm and $N_A = 1x10^{22}$ /m^3

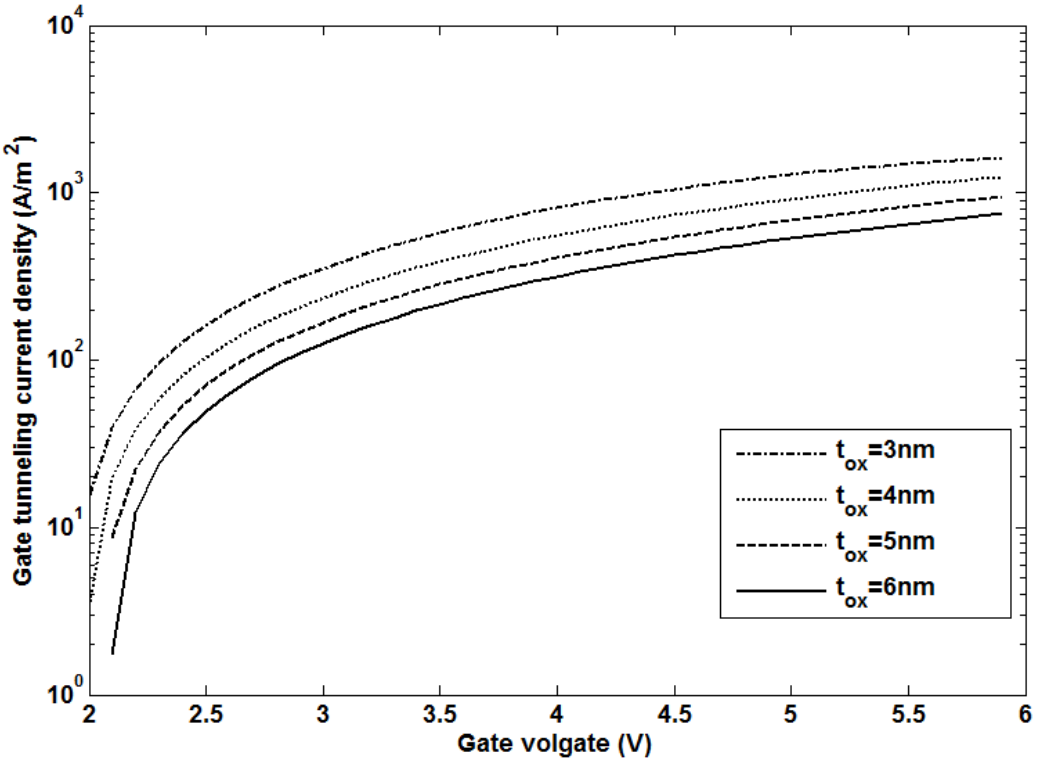


Figure 4.7 Gate tunneling current density versus Gate voltage considering different oxide thickness

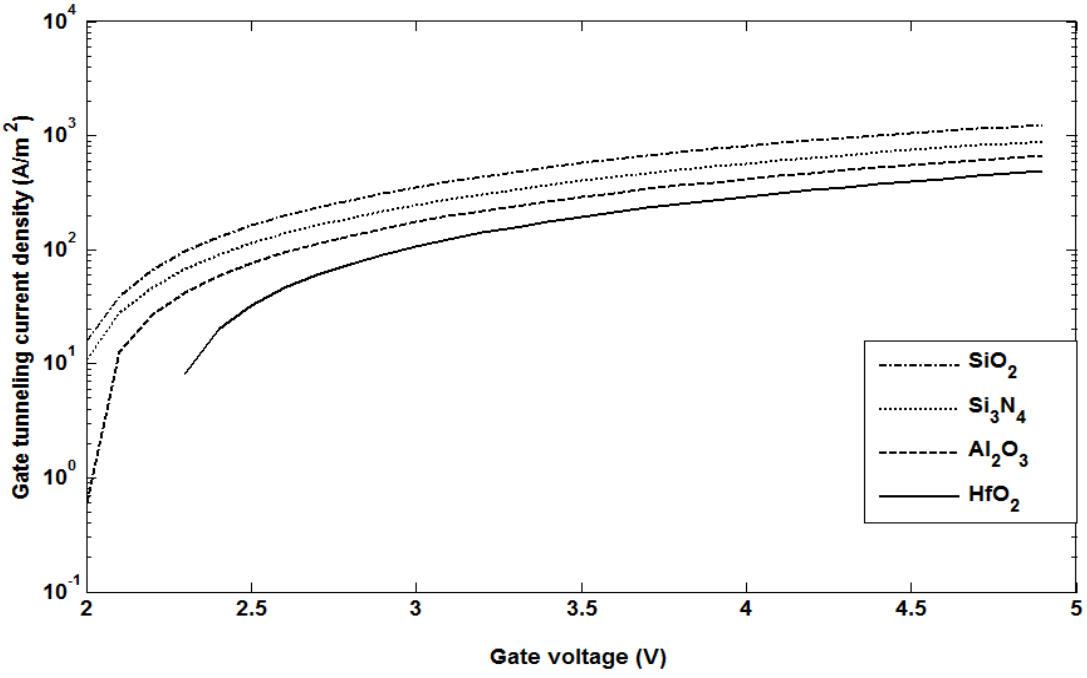


Figure 4.8 Gate current density versus gate voltage taking different dielectric material

Chapter 5

Conclusion and Future work

Conclusion

I. In this thesis work, the modeling of gate current is done using 1D Schrodinger equation of the double gate MOSFET.

II. Fowler-Nordheim (FN) tunneling gate leakage current and Direct tunneling is explained in this thesis work. The FN tunneling gate leakage current and the direct tunneling leakage current has been compensated using high k instead of oxide thickness because with increase in k the channel becomes dependent on the gate current.

III. The proposed modeling of gate current is less intense which leads to the fast response.

IV. The results obtained from modeling are in agreement with the simulation data. This indicates the technique to be cost effective.

Future work

In this thesis work, a model has been presented for determination of FN gate leakage current through the oxide for poly silicon gate as well as metal gate. It can be modified, further when the drain voltage is not tied to ground, where many other effects such as corner effect at the drain end and source end come into the picture. Quantum correction needs to be incorporated in the model to obtain more accurate result.

Also determination of drain current by using the quantum phenomena.

References

[1] D. Kahng and M. M. Atalla, "Silicon-silicon dioxide field induced surface devices," in *IRE-AIEEE Solid-State Device Research Conference* (Carnegie Inst. of Tech., Pittsburgh, PA), 1960.

[2] Gordon E. Moore, "Cramming more components onto integrated circuits", *Electronics, 38(8)*, 1965.

[3] The International Technology Roadmap for Semiconductors, www.itrs.net

[4] Chung Tsung Ming, PhD thesis: "Simulation, Fabrication and Characterization of Advanced MOSFETs: Graded-Channel and Multiple-Gate devices in SOI technology for Analog and RF applications," *Université Catholique de Louvain*, Belgium, 2007.

[5] G. Baccarani, M.R. Wordeman and R.H. Dennard, "Generalized scaling theory and its application to a ¼ micron MOSFET design", *IEEE Trans. Electron Devices, 31*,pp. 452-462, April 1984.

[6] M. Vanmackelberg, C. Raynaud, O. Faynot, J.-L. Pelloie, C.Tabone, A. Grouilet et al, "0.25 Im fully depleted SOI MOSFETs for RF mixed analog-digital circuits, including a comparison with partially depleted devices with relation to high frequency noise parameters", *Solid State Electronics, 46*, 379-382 (2002)

[7] M. Song, K.P. MacWilliams, and J. C.S. Woo, "Comparison of NMOS and PMOS hot carrier effects from 300 to 77 K", *IEEE Trans. Electron Devices, 44(2)*, February 1997.

[8] F. Assederaghi, P.K. Kop and C. Hu, "Observation of velocity overshoot in silicon inversion layers", *IEEE Electron. Dev. Letters, 14(10)*, pp. 484-486, Oct. 1993.

[9] K. Taniguchi, M. Yamaji, K. Sonoda, T. Kunikiyo, C. Hamaguchi, "Monte Carlo study of impact ionization phenomena in small geometry MOSFETs", *IEDM Technical Digest*, pp. 355-358, Dec. 1994.

[10] J. P. Colinge, X. Baie, V. Bayot, and E. Grivei, "A siliconon-insulator quantum wire," *Solid-State Electron., 39(1)*, 1996,pp. 49–51.

[11] J.P. Colinge, "Multiple-gate SOI MOSFETs", *Solid-state electronics, 48(6)*, 2004, pp. 897-905.

[12] 2003 Spring Meetings Proceedings, editor, "Evolution of SOI MOSFETs: From single-gate to multiple-gates", *MRS Proceedings*, 765, D1.6 (2003)

[13] J.P. Colinge, "Silicon-on-insulator technology: Material to VLSI", USA: *Springer* (2004)

[14] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, T. Elewa,"Double-gate silicon-on-insulator transistor with volume inversion: a new device with greatly enhanced performance", *IEEE Electron Device Letters, 8*, 1987, pp. 410-412.

[15] Y.K. Choi, K. Asano, N. Lindert, V. Subramarian, T.J. King, J. Bokor, C. Hu, "Ultrathin-body SOI MOSFET for deep subtenth micron era," *IEEE Electron device letters, 21*, 2000, pp.254-255.

[16] L. Chang, S. Tang, T.-J. King, J. Bokor, and C. Hu, "Gate length scaling and threshold-voltage control of double-gate MOSFETs," in *IEDM Technical Digest*, 2000, pp. 719-722.

[17] Q. Lu, R. Lin, P. Ranade, T.-J. King, and C. Hu, "Metal gate workfunction adjustment for future CMOS technology," in *Digest of Technical Papers – Symposium on VLSI Technology*, 2001, pp. 45-46.

[18] S.-H. Oh, D. Monroe, and J. M. Hergenrother, "Analytic description of short-channel effects in fully-depleted double-gate and cylindrical, surrounding-gate MOSFETs," *IEEE Electron Device Letters, 21(9),* 2000, pp. 445-447.

[19] D. Monroe and J. M. Hergenrother, "Evanescent-mode analysis of short-channel effects in fully-depleted SOI and related MOSFETs," in *1998 IEEE International SOI Conference Proceedings*, 1998, pp. 157-158.

[20] D. J. Frank, Y. Taur, and H.-S. P. Wong, "Generalized scale length for two-dimensional effects in MOSFETs," *IEEE Electron Device Letters, 19(10),* 1998, pp. 385-387.

[21] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependen-cies," *Proceedings of the IEEE, 89(3),* 2001, pp. 259-288.

[22] D. Monroe and J. M. Hergenrother, "Evanescent-mode analysis of short-channel effects in fully-depleted SOI and related MOSFETs," in *1998 IEEE International SOI Conference Proceedings*, 1998, pp. 157-158.

[23] H.-S. P. Wong, D. J. Frank, and P. M. Solomon, “Device design considerations for double-gate, ground-plane, and single-gated ultra-thin SOI MOSFET’s at the 25 nm channel length generation,” in *IEDM Technical Digest*, 1998, pp. 407-410.

[24] H.-S. P. Wong, D. J. Frank, P. M. Solomon, C. H. J. Wann, and J. J. Welser, “Nanoscale CMOS,” *Proceedings of the IEEE, 87(4),* pp. 537-570, Apr 1999.

[25] S.-I. Takagi, A. Toriumi, M. Iwase, and H. Tango, “On the universality of inver-sion layer mobility in Si MOSFET’s: Part 1-Effects of substrate impurity concentration,” *IEEE Transactions on Electron Devices, 41(12),* pp. 2357-2362, Dec 1994.

[26] F.-L. Yang et. al., “5nm-gate nanowire FinFET,” in *Digest of Technical Papers – Symposium on VLSI Technology,* 2004, pp. 196-197.

[27] A. Javey, Q. Wang, W. Kim, and H. Dai, “Advancements in complementary carbon nanotube field-effect transistors,” in *IEDM Technical Digest*, 2003, pp. 741-744.

[28] S. Kang and Y. Leblebici, "Cmos Digital Interated Circuits," *Tata McGraw-Hill Education*, 2003.

[29] M. R. Wordeman and R.H. Dennard, "Generalized scaling theory and its application to a 1/4 micrometer MOSFET design," *in IEEE Transactions on Electronic Devices*, 2005, pp. 452-462.

[30] K. Roy and S. Mukhopadhyay, " Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits," in Proc. of IEEE, 91(2), 2003, pp. 305-327.

[31] International Technology Roadmap for Semiconductors, 2003 edition, SIA.

[32] C. Auth, “Physics and technology of vertical surrounding gate MOSFETs,” Ph. D. Thesis, Stanford University, 1998.

[33] D. Hisamoto et. al., “Folded-channel MOSFET for deep-sub-tenth micron era,” in *IEDM Technical Digest*, 1998, pp. 1032-1034.

[34] H.-S. P. Wong, K. K. Chan, and Y. Taur, “Self-aligned (top and bottom) double-gate MOSFET with a 25 nm thick silicon channel,” in *IEDM Technical Digest*, 1997, pp. 427-430.

[35] K. F. Schuegraf, C.C. King and C.Hu, "Ultra-thin Silicon Dioxide Leakage Current and Scaling Limit," in Symposium on VLSI Technology Digest of Technical Papers, 1992.

[36] I. Mondal and A. K. Dutta, " An Analytical Gate Tunneling Current Model for MOSFETs Having Ultrathin Gate Oxides," in IEEE Transactions on Electronics Devices, 55(7), 2008, pp. 1682-1692.

[37] Operation and Modeling of the MOS transistor, Third Edition, Yannis Tsividis and Colin McAndrew.

[38] Matrix Methods and Differential Equations, First Edition, Wyanand S. Verwoerd.