Study of Impact of Parameter Variations of FinFET on DIBL and Short Channel Effects

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Submitted by

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DECLARATION

I hereby declare that the thesis report entitled '**Study of Impact of Parameter Variations of FinFET on DIBL and Short Channel Effects**' is an authentic record of my study carried out as requirement for the award of degree of M.tech (VLSI Design) at Thapar University, Patiala under the supervision of **Mr. Arun Kumar Chatterjee (Assistant Professor)**, ECED during, 2014-2016.

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Arvind Sharma

ABSTRACT

Bulk CMOS transistor technology is facing significant challenges due to several cause such as the increasing leakage current, high power dissipation, mobility degradation and short channel effects (SCEs). When channel length shrinks, gate control over channel reduces due to various SCEs such as drain induced barrier lowering, charge sharing, and surface punch-through. Silicon on insulator technology is capable of providing increased transistor speed, reduced power consumption, fine isolation between devices, significant reduction in parasitic capacitance, and extended scalability.

In this work, a thorough study of effects of parameter variations on the operation of multi gate field effect transistor has been done. For this, a triple gate FinFET structure has been design and simulated using TCAD tool. The parameters like fin-width, fin-height, channel doping and underlap length has been varied and their effects on FinFET has been observed.

The simulation results show that small increase in underlap length improves the I_{ON}/I_{OFF} ratio significantly. Further increase in fin-height, a reduction in leakage current has been observed. Also a decrease in fin-width shows a significant reduction in leakage current. All the simulations have been done on Cogenda Visual TCAD tool.

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LIST OF ABBREVIATIONS

MOSFET	Metal oxide semiconductor field effect transistor
CMOS	Complementary Metal oxide semiconductor field effect transistor
SCE	Short channel effects
DIBL	Drain induced barrier lowering
GIDL	Gate induced drain leakage
SOI	Silicon on insulator
PDSOI	Partially depleted silicon on insulator
FDSOI	Fully depleted silicon on insulator
DGFET	Double gate field effect transistor
ITRS	International technology roadmap for semiconductors
TGFET	Triple Gate field effect transistor
Wfin	Fin width
Hfin	Fin height
RSD	Source drain sheet resistance
Rcontact	Contact resistance
Rext	Extension resistance
SS	Subthreshold swing
TCAD	Technology computer aided design
UTB	Ultra thin body
ICs	Integrated circuit
SGOI	Silicon germanium on insulator
MgFET	Multiple gate field effect transistor

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CHAPTER 1

INTRODUCTION

The origin of metal-oxide-semiconductor (MOS) device was year 1959. Silicon metal oxide semiconductor field effect transistor (MOSFET) is most important devices in the semiconductor technology (Fig 1.1 NMOS device). The MOSFET used in monolithic integrated circuits (ICs) instead of bipolar junction transistors to perform basic switching operation of digital logic and used as amplifying device in analog as well as digital applications due to it's various advantages. The size of the MOSFET shrunk on very large scale over the years. Scaling was predicted by 'Moore's Law'. Figure 1.2 shows that how number of transistor for different semiconductor industry increase according to Moore's law.[1]

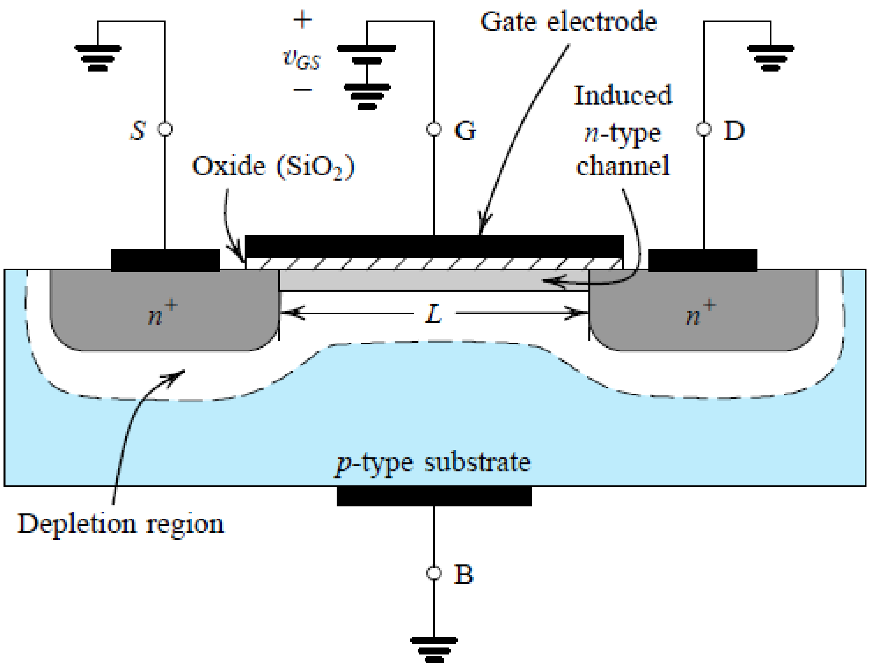

Figure1.1 Schematic of N type MOSFET

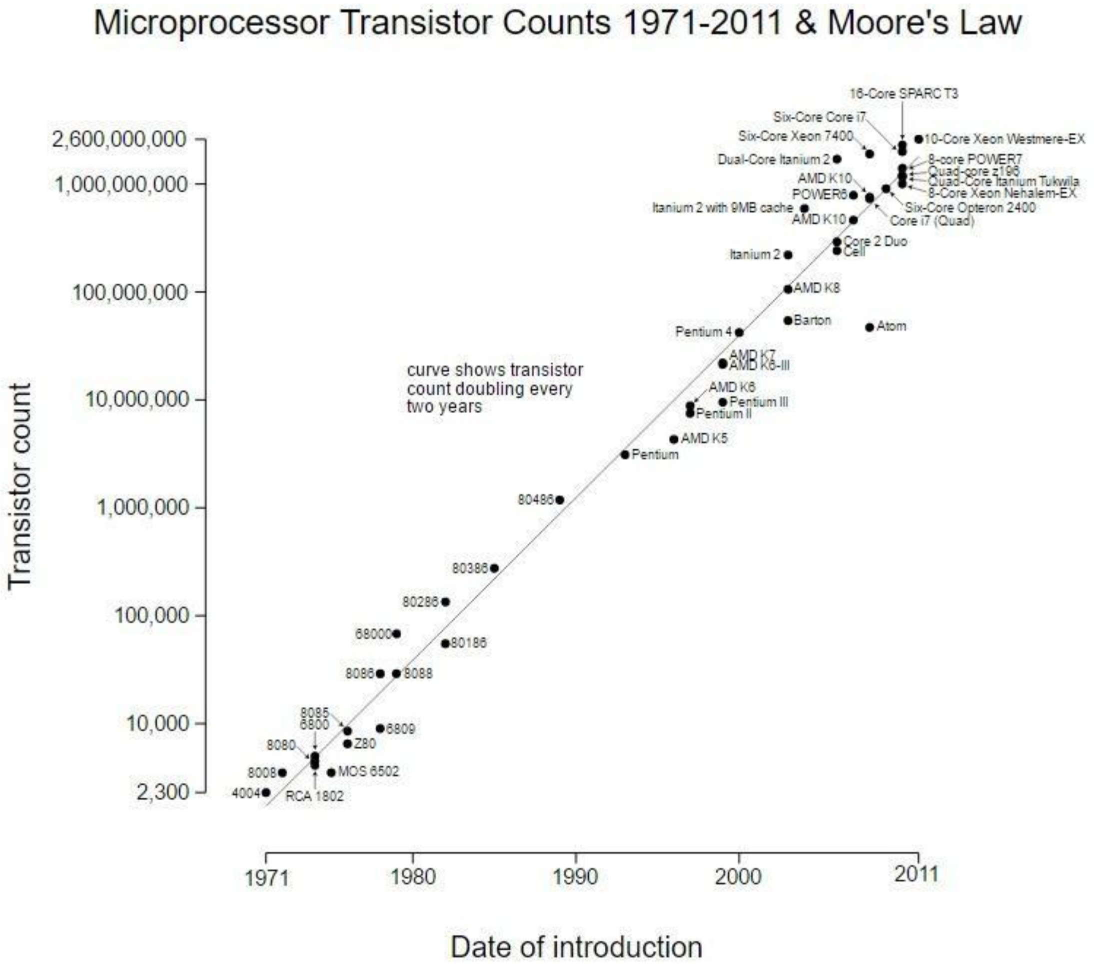

Figure 1.2plot between transistor count and date of introduction of various ICs for various firms

As technology moving from one generation to another generation, scientists observed that moor’s laws doesn’t follow as predicted by moor’s (‘the number of transistors in a dense integrated circuit doubles approximately every two years’). Basically MOSFET classify in two category depletion type MOSFET and enhancement type MOSFET, further it classify into two part NMOS and PMOS transistor. Generally we used enhancement type MOSFET, NMOS is faster than PMOS due to mobility of charge carrier.

1.1SCALING

The design of high density chips in VLSI (Very Large Scale Integration) technology needs that the packing density of MOSFETs used in the circuits is as high as possible and consequently, that the sizes of the transistors are as small as possible. The reduction of the size i.e. the dimensions of MOSFETs, is commonly referred to as scaling. It is expected that the operational characteristics of the MOS transistor will change with the reduction of its dimensions. Also, some physical limitations eventually restrict the extent of scaling that is practically achievable. There are two basic types of size reduction strategies: full scaling (also called constant-field scaling) and constant voltage scaling. Scaling of MOS transistors is concerned with systematic reduction of overall dimensions of the devices as allowed by the available technology, while preserving the geometric ratios found in the larger devices. The proportional scaling of all devices in a circuit would certainly result in a reduction of the total silicon area occupied by the circuit, thereby increasing the overall functional density of the chip.

1.2 CHALLENGES DUE TO SCALING OF MOSFET

The scaling of MOS device reached to its limit that is 22nm, beyond this limit we couldn’t scale the MOS device in order to follow moor’s law further. Beyond 22nm MOS device not only follow Newton physics but also follow quantum mechanics. So, we need to move to another device which can scale beyond bulk MOSFET. Modern integrated circuit is computer simulated with target of getting running circuit from manufactured. As transistor is miniaturized, the complication of process makes it difficult to speculate, how exact device will looks and modelling of physical process become further challenging. Additionally, microscopic changes in the device are probabilistic nature of atomic process which requires statistical predictions. Combining such factor to make proper simulation Different challenges faced in scaling MOSFET is shown below [2][3]

- **Physical challenges:** When Scaling MOS device, tunneling comes into picture which results in leakage current. Which affect the functionality and performance of device

- **Material Challenge:** Inability of dielectric material and wiring material to provide better isolation to device and conduction through continued scaling

- **Heating challenge:** As number of transistor per unit area is increasing with scaling of device which results in large heat power dissipation and consumption.

- **Economical challenge:** As technology improve , the cost of production increase, fabrication complexity increase and testing also costly which cannot be economical for common man

1.2 SHORT CHANNEL EFFECTS IN BULK MOSFET

In order to achieve higher performance, lower power consumption and higher density, MOS device is scaling more than 50 years. Transistor delay reduces by 25% per technology generation, which results in twice the speed of microprocessor every 18 months. Power supply voltage scaled down in order to maintain power consumption. So, threshold voltage of device scaled down to keep large drive current and achieve better performance. Although, threshold voltage scaling resulting in the increasing of sub-threshold leakage current. Off state current is influenced by gate oxide thickness, surface/channel doping, channel physical dimension, threshold voltage, source/drain junction depth and supply voltage. Short channel transistor needs smaller power supply voltage to decrease their internal electric field and consumption of power. This forces decrease in threshold voltage that increase in off state current.[2]

1.2.1 DRAIN INDUCED BARRIER LOWERING

Drain induced barrier lowering (DIBL) is the effect of drain voltage on output conduction and observe threshold voltage. This phenomenon occurs in device where only gate length is decrease without scaling any other dimensions. It is measured as a variation of the threshold voltage with decreased gate length. The threshold change is due to the increase in current with increase in drain voltage (“the applied drain voltage controls the inversion charge at the drain terminal”), therefore competing with gate potential. This effect occurs because of two dimensional field distributions at drain end. It can be eliminating by proper scaling of drain and source depths and increasing the substrate doping density.[2]

1.2.2 SUBTHRESHOLD LEAKAGE

Subthreshold or weak inversion current between drain and source in MOSFET occurs while gate voltage is lower than threshold voltage. In weak inversion, concentration of minority carrier is very small but not zero. Consider source of NMOS is grounded, Vg (gate voltage) < Vth (threshold voltage) and drain to source potential V_{ds} >= 0.1V. For this weak inversion, V_{ds} drops completely across reverse biased drain substrate pn junction. Result of this, variation of electrostatic potential along channel is small. Due to smaller mobile carrier and electric field, drift current component of subthreshold drain to source current very small. Weak inversion dominates device off state leakage current due to smaller threshold voltage. Subthreshold slope shows how fast MOS transistor turned off (rate of reduction of off state current) when V_{gs} (gate to source voltage) is reduced below threshold voltage. Sub threshold slope (St) value for conventional MOS transistor can range from 65 to 120mV/decade. Lower value of St desirable, it can be achieved by using thinner oxide layer or lower body doping.[2][5]

1.2.3 PUNCHTHROUGH

Punch through in a MOS is a case of channel length modulation where depletion region surrounding drain and source merge into one depletion region. The field underneath gate becomes strong dependency on the drain to source voltage, as is the drain current. Punch through can rapidly increase the current with increase in drain to source voltage. This undesirable effect increases the output conduction which limits the peak operational voltage of the device. [2][6]

1.2.4 VELOCITY SATURATION

As device size is reduced, the electric field also rises and velocity of carriers in the channel increased. Although, there is no longer linear relation middle of the electric field and velocity at high electric fields, as the velocity slowly saturates to the saturation velocity. This velocity saturation is increased due to the scattering of highly energetic electrons, primarily it is because of optical phonon emission. This impact is due to increases in transit time of carriers through inversion channel. [2][6]

1.2.5 HOT CARRIER INJECTION

In short channel MOSFET, as results of high electric field near silicon (Si) silicon oxide (SiO_2) interface, charge carriers can gain enough energy from high electric field to cross surface potential barrier and jump into the oxide region. This effect called hot carrier injection. The injection is more likely for electrons than holes because electrons have smaller effective mass than that of holes and barrier height of electron is also smaller than holes. [5][6]

1.2.6 QUANTUM EFFECTS

Quantum effect occurs in devices which include tunneling effect. When charge carrier tunnel across barriers of FET, which leads to leakage current. If scaling continues, it will leads to higher power dissipation. Higher electrostatic field ($>10^5$ V/cm)across reverse bias PN junction causes major current to flow through junction because of tunneling of electrons from valence band of p region to conduction band of n region, for tunneling to arise, total voltage drop across the junction need to be higher than band gap. So modelling at very small dimension is very crucial task. [10]

1.3 NEXT GENERATION STRUCTURES

Since the fabrication of transistor, the channel length has been shrinking. As devices shrink more and more, the problems with bulk (planar) MOSFETs are increasing. As we go to the 65nm, 45nm etc. nodes, there is no viable option for continuing forward with the traditional MOSFET. The intention behind this decrease is more interest in high speed device and very large scale integrated circuits. The continuous scaling of traditional bulk device needs innovations to circumvent the problem of fundamental physics constraining the traditional MOSFET device structure. The channel depletion width must scale with the channel length to contain smaller off state leakage I(off) . This results in high doping, that reduce charge carrier mobility and causes junction edge leakage because of tunneling further, the doping profile control as depth and steepness become more difficult. The thickness of gate oxide must scale along with channel length to maintain proper threshold voltage, gate control and performance. The thinner of gate dielectric material results into gate tunneling leakage, which degrades circuit performance, noise margin and power. [6]

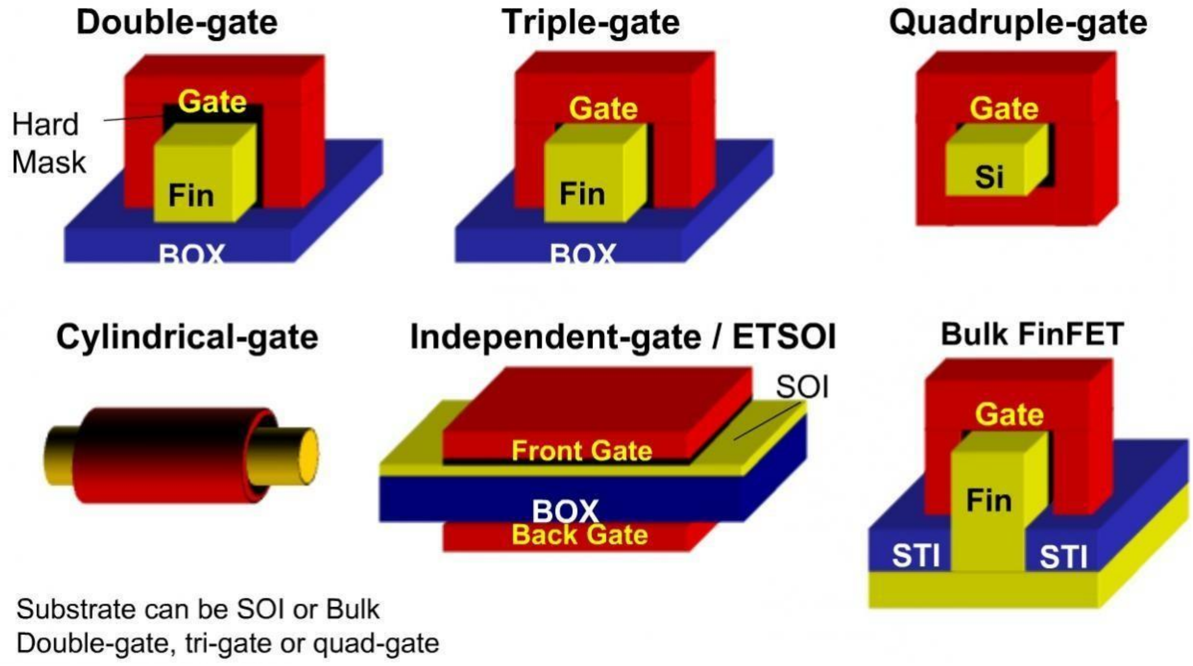

Figure 1.3 Different SOI FinFET structures

1.3.1 SOI TECHNOLOGY

Alternative of MOSFET device structure is based upon silicon-on-insulator (SOI) technology has emerged as an effective measure of extending MOS scaling beyond the limit of bulk for low-power or high-performance applications. Partially depleted SOI was the 1st SOI technology which introduced for high-performance microprocessor. The ultra thin body fully depleted SOI and non-planar FinFET device structures are promising to be potential future of technology or device choices.[6][7][8]

1.3.2 PARTIALLY DEPLETED SOI

Partially depleted silicon on insulator (PD SOI) transistor shown in Fig.1.4 is a layer of SiO_2 which separates upper device contains silicon film and rest of the Si substrate. Silicon film is comparatively thick (~90 nm or more). In the off condition, with no voltage applied to gate terminal, the maximum width of depletion region underneath gate oxide is smaller than silicon film thickness. The lower region of partially depleted SOI has a quasi-neutral region which is left noncontact. Potential of floating Si area is calculated by capacitive coupling of different electrodes dynamically and in steady state, by forward and reverse biased currents to drain and source junctions, which leads to various floating body effects like parasitic bipolar kink effect and history dependent threshold voltage. The major advantage of the partially depleted device is somewhat lower leakage and higher speed due to reduced drain and source region junction capacitances. By using ion implantation, the floating body effects could be reduced or by placing body contact. Although, from electrostatic scalability and static leakage point of view, PD SOI device looks like bulk FET. Therefore, it is not be scaled beyond what can be achieved with well design bulk FET. [4]

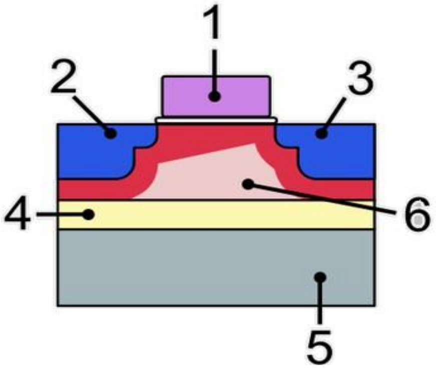

Figure 1.4 Partially Depleted SOI MOSFET

1.3.3 FULLY DEPLETED SOI

If thickness of upper silicon film in partially depleted SOI transistor is reduces, then complete Si body underneath gate deplete at zero gate voltage. This type of device is known as “FD SOI” transistor. It is also called “depleted substrate transistor”. A schematic of FD SOI is described in Fig.1.5. The thickness of film underneath full depletion situation arise depend on its body doping. By removing quasi-neutral float body, kink effect and history dependent effect can be eliminates. Short channel effects in fully depleted device have less impact compare to partially depleted device. Lower vertical depletion width enhances electrostatic control of gate on transistor. In BULK/PD SOI device, a smaller vertical depletion width can be attained by use of higher channel doping. Although, uses of higher channel doping will reduced device performance in form of degrade sub threshold swing, lessen mobility, and enhance band to band tunneling at drain. Vertical depletion thickness of FD SOI device can control through body thickness in absence of channel doping, which revamp carrier transport because mobility boost, since lower ionized impurity scattering, moreover smaller vertical electric field for same channel carrier conc. [6]

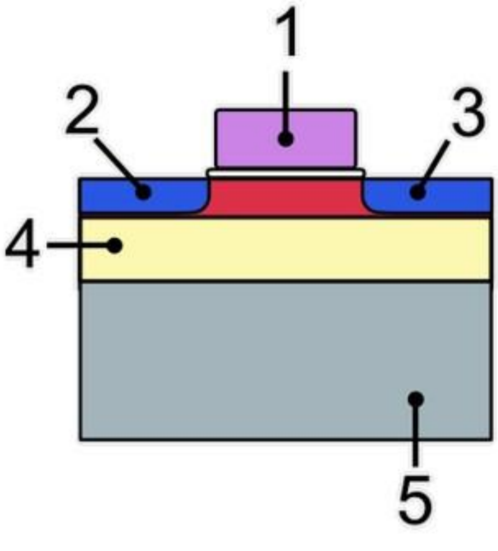

Figure 1.5 Fully depleted SOI transistor

1.3.4 MULTI GATE FINFETs

Multi gate FET in fully depleted mode activity permits superior control over short channel effect rather than one gate fully depleted FET. This is due to close coupling of capacitor of multiple gates to transistor channel area from different direction. Basic of electrostatic activity of multi gate FET is alike. Control of gate become strong as number of gate increase such as single to double to triple gate to all around gate FET as virtue of raised coupling. Double gate FET could be assumed as improved form of fully depleted SOI device with extremely narrow buried oxide "as thick as gate oxide". Next, only body is highly doped with electrically connect to gate. As, there has no capacitive voltage distribution betwixt upper and lower gate, that is both gate control substrate jointly, gate to body coupling is precise and sub threshold swing is 55 mV/dec for ideal device. Additionally, "short channel effect" (SCE) control is extremely fine as virtue of narrow fully depleted substrate and gate is shield of drain electrostatic from either side. Because of multiple gates, now transistor can scale down to smaller gate length for identical body (and "oxide thickness"). As multiple gates and thin substrate are enough to reduce SCE, so substrate kept undoped. Which enhance channel charge carrier movement since it improved mobility due to less ionized impurity scattering and smaller vertical electrostatics. Additionally, undoped substrate is highly protected from discrete doping fluctuations effect. In triple gate and all around gate FETs device, crystal orientation effect can plays significant part, as charge carrier arise along different orientation.[6][8][9][11]

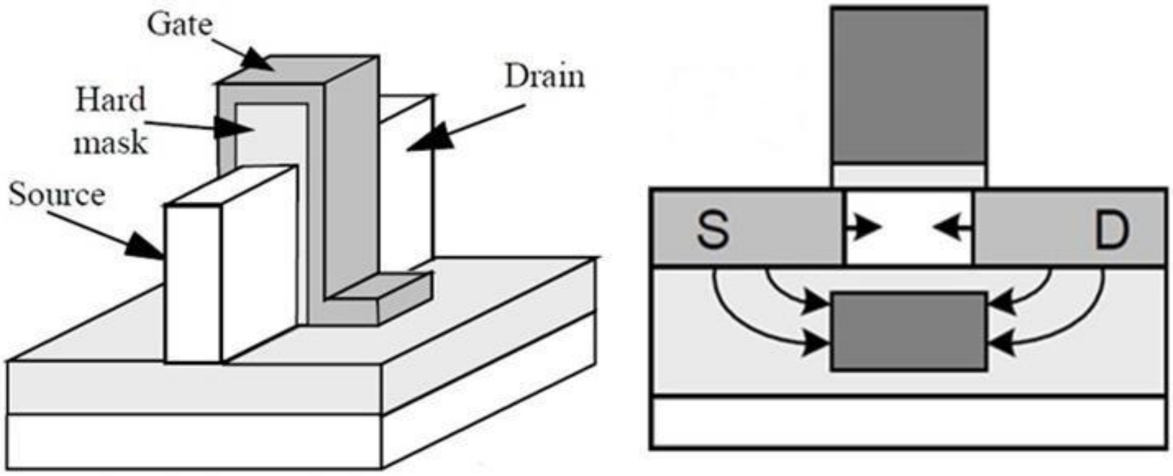

Figure 1.6 Double gate FinFETs in 2D and 3D

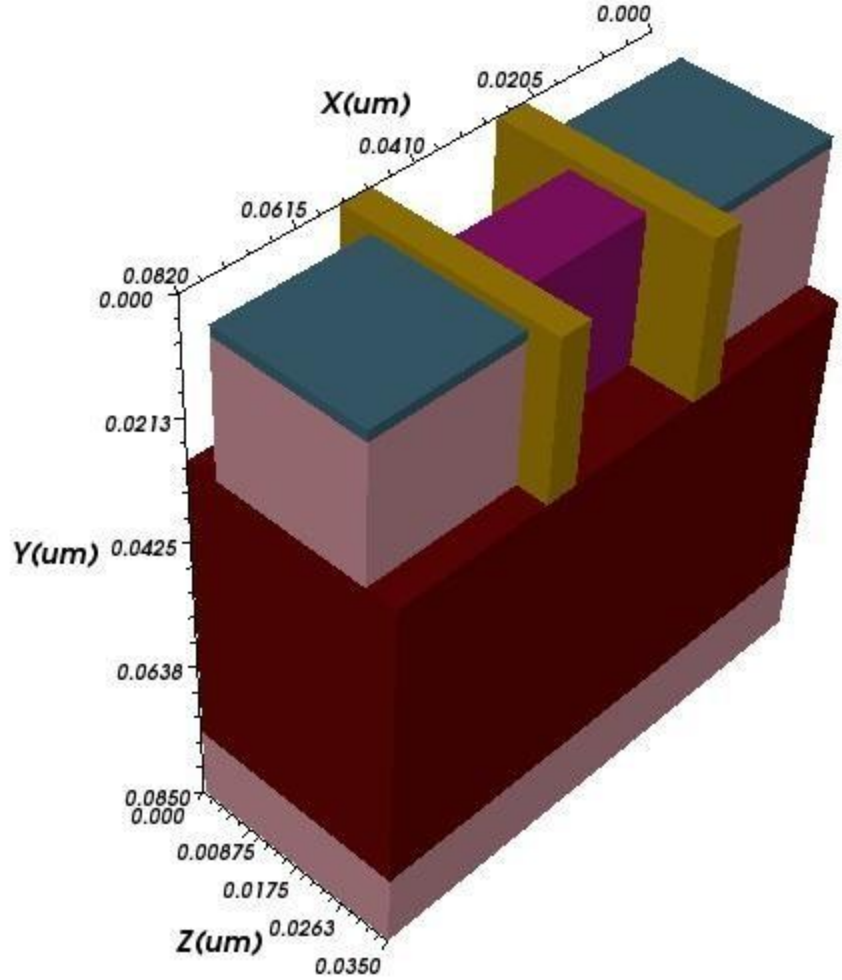

Figure 1.7 Triple gate FinFETs

.1.5 THESIS REPORT ORGANISATION

In this report, there is a five chapter. A brief description of work done by different scientist is mention in chapter two “literature survey”. Chapter three contains gaps in the literature of FinFETs based on their research priority. Chapter four contains results, which shows how underlap, fin height, fin width, doping and oxide thickness impacts on drive current , leakage current, DIBL, mobility etc. Chapter five contains conclusion and future of device technology

CHAPTER 2

LITERATURE SURVEY AND GAPS

2.1LITERATURE SURVEY

Gordon Moore in 1965 [1] proposed **Moore's law** which state that “over the history of computing hardware, the number of transistors in a dense integrated circuits doubles approximately in every two years”.

Kaushik Roy, in 2003[2] explained that why large leakage current in scaled down device become major cause to power consumption in MOS transistor while channel length, gate oxide thickness and threshold voltage reduced. Resulting, to find and modelling of various leakage elements are significant to reckon and decrease of leakage power, particularly for small power application. This paper analysis different device leakage process, comprising weak inversion, DIBL, GIDL, and tunneling through oxide. Channel engineering method comprising retrograde well and halo doping is examined to reduce SCE for constant scaling of MOS transistor. Lastly, paper analyzed various circuit methods to minimize leakage power dissipation

W. Wu1, X. Li1, in 2007[4] examined progression on **partially depleted (PD) SOI modeling** utilizing surface potential base method. Newly design model said “PSP SOI” model, which constructed within current industrial standard of conventional MOS device PSP model. Besides physics based approach and scalability inheritance from PSP, PSP SOI apprehend SOI precise effects using inclusion of floating body simulation capacity, parasitic bipolar model, and self-heating. The PSP SOI model verified over various PD/SOI technology**.**

Mehdi Saremi and Ali Afzali Kusha in 2012 [11] investigated how ground plane decrease coupling of electric field between source and drain to decrease DIBL. Ground plane (GP) method is one of the methods used to decrease the DIBL effect in SC SOI device. This method suitable if distance between GP and drain is negligible liken to channel length. GP transistor showed smaller leakage power dissipation liken to transistor with no GP. GP FinFET device, as GP remove DIBL effect, it's reliance over channel doping density is reckon weakened. Hence, to reduce random doping variation, such device used with smaller channel doping density with no concerned of DIBL.

S L Tripathi and Ramanuj Mishra in 2012[12] proposed Pie gate bulk FinFET device. Impact of gate at bottom to junction depth, misalignment investigated for deep junction and shallow junction. This explained bulk FinFET with source/drain to body (S/D) junction narrow than gate at bottom has equal or better sub threshold performance than SOI FinFET.

B. Lakshmi and R. Srinivasan in 2013 [13] suggested the impact of gate electrode work function in 30nm gate length bulk and junctionless FinFETs by "TCAD" simulator. DC parameter, threshold voltage, drive current (Ion) and output resistance are examined. Junctionless transistor being bulk conducting behave different w.r.t work function variation comparing to surface conductive traditional devices. Threshold voltage variation and drive current w.r.t work function, in junctionless transistor is slower comparing to traditional transistor. To achieve effective DIBL result, junctionless device contain large output resistance**.**

Mahender Veshala, Ramchander Jatooth, Kota Rajesh Reddy in 2013 [13] analyzed how can SCE be reduce in FinFET. Simulation shows that FinFETs device can be scale to 8 nm. Very thin fin enables to reduce SCE. The SCE is limited by physical structure and off state leakage is decrease using ultra fine Si film in FinFETs structure. For better reduction of leakage current, the thickness of Si film must be lesser then one fourth the channel length. Threshold voltage can be change by changing work function using mid gap material.

Dongil Kim, Yesung Kang in 2013 [14] suggested basic model to finding on current and off current of double gate FinFETs while changing fin shapes. Result shows as fin shape vary which result into major alters into on and off current of device. The thickness of source and drain region have uncommon effect on transistor. He proposed an ideal fin shape to decrease off state current while provides liken on current to FinFET.

Kiran Bailey and K. S. Gurumurthy in 2013 [16] showed that SOI FinFETs of Thin Fin width compare to SGOI(Silicon Germanium on Insulator) MOSFET Body thickness, provide great control to SCE and decreased power consumption because of decreased gate leakage current. Using different spacer width and Fin width, transistor performance improved. The performance of triple gate FinFETs compare to Ultra Thin Body (UTB) Recessed Source drain SGOI MOSFET in forms of delay, power dissipation and noise margin for a CMOS inverter and results indicate the better suitability of SOI FinFET structures for Low standby Power (LSTP) Application. SOI FinFET device Sensitivity to process parameters such as Gate Length, Spacer Width, Oxide thickness, Fin Width, Fin Height and Fin doping have examined and reported

Nour El Islam Boukortt in 2015 [17] analyzed simulative data achieve using TCAD tool for 3D SOI FinFET device for gate length of 8 nm at room temperature. The impact of changing device main electrical parameter, like threshold voltage, sub threshold slope, transconductance, DIBL, on current, leakage current and on/off current ratio are presented and analyzed, also explain impact of gate work function variation on device. This changes direct influence on electrical characteristic. Results describe that threshold voltage reduce as reduce the gate metal work function. Consequently, leakage current improves with increase work function.

2.2 GAPS IN LITERATURE

The traditional MOS generation is getting major difficulty because of various causes like increased off state current, large power consumption, mobility degraded and various kind of SCE. For reduction of these, severe impacts on device, various SOI devices are suggested and examined like double gate, pi gate, all around gate and omega gate. Amid all such devices, narrow fin based FET gained more popularity because of favorable exoneration to short channel effects, subthreshold swing, higher carrier mobility and higher drain current. [2][6][17][18][19]

Silicon on insulator based FinFET device has diverse benefits as compare to traditional FinFET like smaller off state current, smaller source to substrate capacitor and drain to substrate capacitor, large drain current, superior subthreshold characteristics, and less sensitiveness to doped body. Other sides, traditional FinFET has benefits of smaller price of manufacturing, smaller fault density, lower self heating, and highly stable against “negative bias temperature instability”. In conventional FinFETs difficulty of “threshold voltage roll off” could eradicate using increased under-lap length. [2][6][17][18][19]

In small channel devices, by growing of “buried oxide” layer breadth, the “subthreshold slope” will reduce. It is because of increasing “drain induced barrier leakage” effect; induce by extra penetrating of electric field inside “buried oxide layer” layer. Drain induced barrier lowering problem could be reduce performance of transistor with increased doping measure of channel, however carrier mobility degraded. “Gate and Channel engineering” method applied for FinFET devices to decrease off state current and short channel effects. Performance of Fin device can furthermore improve by decreasing fin width of transistor. Although, it introduce larger amount of parasitic resistances to source or drain region and degrade structures driving current. [2][6][17][18][19]

In triple gate devices, “threshold voltage” and “off state current” is influence by overlap of top and side gate electrics field at the corner. Due to overlap there is a “charge sharing effect” between top and side gates which cause amature channel in corner, that creates different channel for corner with different “threshold voltage”. This process is called “corner effect” and it could be removed using extra “corner implantation and/or corner rounding”. [2][6][17][18][19]

Traditional FinFETs device has sensitivity towards “DC” components such as threshold voltage, on current, output resistance, drain induced barrier leakage, subthreshold slope and not sensitive to “RF” components such as frequency, input impedance, delay when gate electrode work function is varied. Junctions less FinFETs structure is sensitive to both DC and RF components for work function variations.

Problem/effects	Priority based on research	Gaps
Current leakage Mechanisms (DIBL, SS, Tunneling)	High	High
Strained silicon, metal gate, high K dielectrics	Medium	Medium
Specific effects of PD and FD SOI architectures	High	High
Quantum effects, ultrathin oxide effects, gate tunneling models	High	High
Noise model scalable with geometry and voltage	Medium	Medium
Accurate simulation of breakdown and ESD	Low	Low

Table 1 Research gaps of FinFET

It is clear from the survey and gaps in literature is, basically most of research work taking place on DIBL, SS, tunneling, oxide thickness, leakage current. In keeping in mind the literature gaps, I reached to my objective that is as follow

2.3 OBJECTIVE

1. To reduce the short channel effects by varying the underlap length and doping,
2. To reduce leakage current and DIBL effects by varying fin height and width,
3. To reduce subthreshold leakage current by varying oxide thickness for double and triple gate FinFET

To achieve these goals, particular methodology is used. For this work cozenda TCAD tool is used and get data from simulation. These data compared with previous research work and draw the conclusion. The methodology used for this work is as follow.

2.4METHODOLOGY

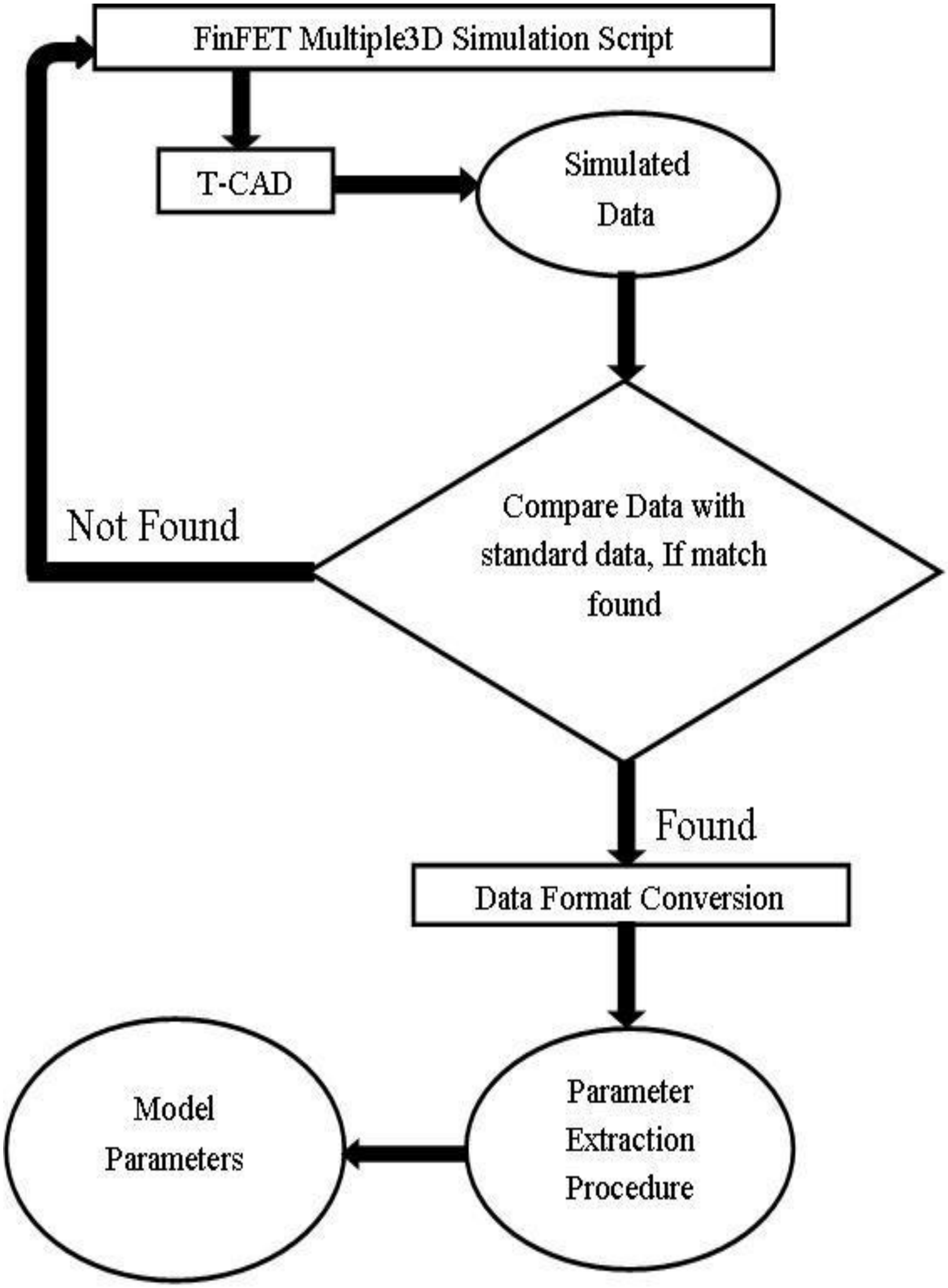

Figure: Proposed methodology

CHAPTER 3

DESIGN OF TRIPLE GATE FinFET

Technology scaling has resulted in continual improvement in the performance of digital circuits. With each technology generation, the device power supply voltage (V_{dd}) reduces by approximately 20% to 30%. The reduction in V_{dd} reduces the active power dissipation quadratically. A reduction in V_{dd} also necessitates a reduction in threshold voltage V_{th} to maintain the gate drive strength ($V_{dd} - V_{th}$). The reduction in V_{th} with each technology generation leads to an exponential increase in leakage current. Also, the number of transistors in a chip increases exponentially, resulting in an increased power density. Thus, power consumption has become a major concern for chip designers because of the increased packaging and cooling costs as well as potential reliability problems. Therefore, power efficiency has assumed increased importance. This chapter explores how circuits based on FinFETs, an emerging transistor technology that is expected to supplant bulk CMOS at the 22nm node or beyond, can be made power efficient.

The steady miniaturization of MOSFETs with each new generation of CMOS technology has provided us with improved circuit performance and cost per function over several decades. However, continued transistor scaling will not be straightforward in the sub 22nm regime because of fundamental material and process technology limits. Several innovative device structures, such as ultra thin-body silicon on insulator (SOI) and FinFETs, have been proposed to address the challenges being posed by continued scaling. [2]

3.1FinFET

Double gate MOSFET is becoming an intense subject of VLSI research because in theory, it can be scaled to the shortest channel length possible for a given gate oxide thickness. But the difficulty in fabrication of DG MOSFET) is encountered due to the misalignment of top gate and the back gate. Hence to eliminate the misalignment of gates in DG MOSFET, FinFET considered one of the most promising candidates for future generation transistor technologies due to their excellent electrostatic integrity such as Low leakage current, improved short channel effect, high performance resulting from the undoped channel structure, high carrier mobility and reduction of random dopant fluctuation. With the scaling of the devices, the fins needed to be thinner due to which scattering of dopants increases. Hence, lightly doped fins are preferred to reduce the scattering or random dopant fluctuations. [6]

3.2 Types of FinFETs

Modern FinFETs are 3D structures that rise above the planar substrate, giving them more volume than a planar gate for the same planar area. Given the excellent control of the conducting channel by the gate, which "wraps" around the channel, very little current is allowed to leak through the body when the device is in the off state. This allows the use of lower threshold voltages, which results in optimal switching speeds and power. [6]

The different ways in which the gate electrode can be wrapped around the channel region of a transistor are shown in the Figure 3.1. All the structure has its own advantages.

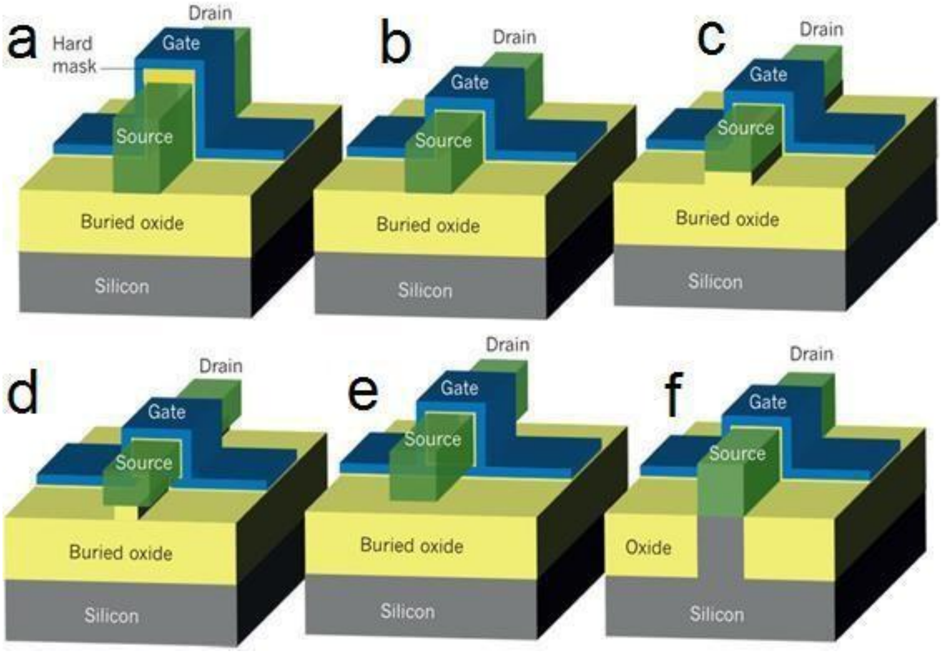

Figure 3.1 Different structures of tri gate FinFET with different configuration of gate wraping around the channel

In the above Figure:

a, A silicon-on-insulator (SOI) fin field-effect transistor (FinFET). The "hard mask" is a thick dielectric that prevents the formation of an inversion channel at the top of the silicon fin. Gate control is exerted on the channel from the lateral sides of the device

b, SOI triple-gate (or tri-gate) MOSFET. Gate control is exerted on the channel from three sides of the device (the top, as well as the left and right sides).

c, SOI Π-gate MOSFET. Gate control is improved over the tri-gate MOSFET shown in c because the electric field from the lateral sides of the gate exerts some control on the bottom side of the channel.

d, SOI Ω-gate MOSFET. Gate control of the bottom of the channel region is better than in the SOI Π-gate MOSFET. The names Π gate and Ω gate reflect the shape of the gates.

e, SOI gate-all-around MOSFET. Gate control is exerted on the channel from all four sides of the device.

f, A bulk tri-gate MOSFET. Gate control is exerted on the channel from three sides of the device (the top, the left and the right). In this case, there is no buried oxide underneath the device.

3.3 FABRICATION STEPS OF FINFETS

FinFETs broadly can be classified into two types: SOI and Bulk-Si FinFETs. Due to the presence of buried oxide, SOI FinFETs have many advantages, such as easier realization, lower leakage current, higher speed. Compared with SOI FinFETs, Bulk-Si FinFETs possess advantages of low cost, low defect density, no floating-body effect, and good heat dissipation. The fabrication steps of FinFET are shown below in Figure 3.2

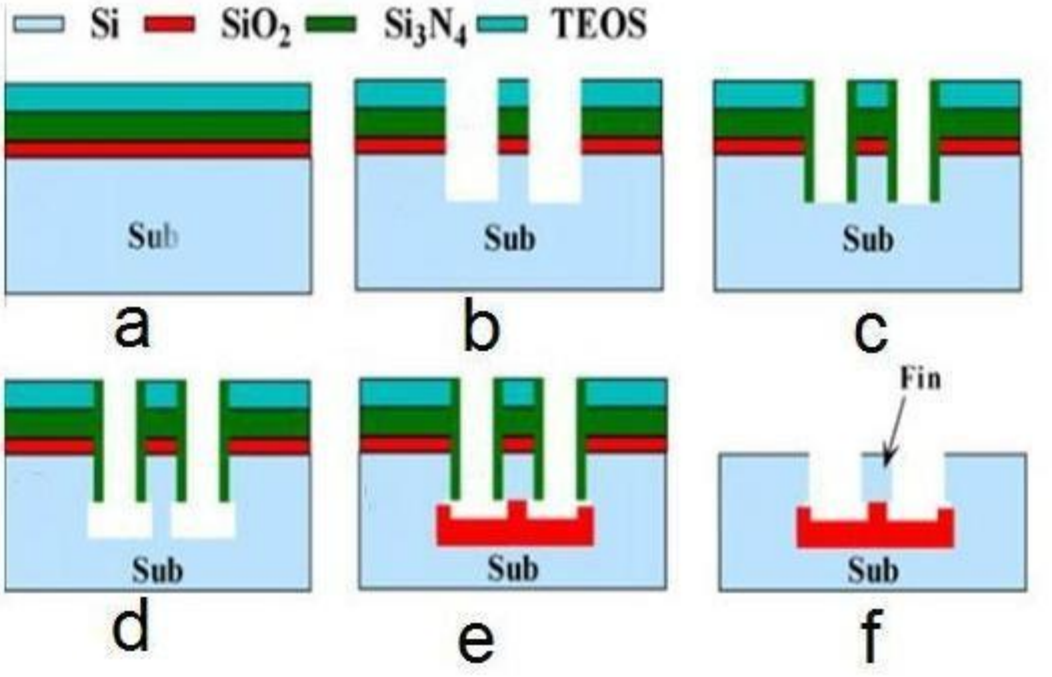

Figure 3.2 FinFET processing steps.

In the above figure 3.4 following steps are used for the manufacturing of FinFET.

a. Buffer oxide /Si3N4/TEOS layer deposition

b. E-beam lithography and etching of two neighbouring grooves.

c. Deposition and etching to form Si3N4 spacer

d. Anisotropic etching of silicon using Si3N4 as hard mask

e. Isolation oxidation using Si3N4 as the shielding layer

f. Stripping Si3N4 and TEOS to form fins

3.4 ACTIVE AREA : FINS

3.4.1 FIN WIDTH

As the MOSFET gate length (L_g) continues to shrink, year after year, the drain starts to compete with the gate electrode for control of the channel potential. The resulting “short-channel effects” (SCE) are: 1) higher sub threshold leakage, 2) a threshold voltage (V_{th}) roll-off, and 3) a form of punch-through between the drain and source when V_{ds} is equal to the supply voltage.

To reduce the drain influence in the channel scaled planar bulk MOSFETs and PDSOI MOSFETs rely on: 1) gate oxide thickness reduction and 2) higher channel doping. The use of a thinner gate oxide increases the gate-to-channel capacitance. A higher channel doping concentration reduces charge sharing between the gate and drain in the channel, and it creates a large potential barrier between source and drain.

However, in modern MOSFETs, direct tunneling current through the gate dielectric prevents further scaling of the gate oxide thickness. The use of high channel doping concentrations reduces carrier mobility and increases Gate Induced Drain Leakage (GIDL).

Another way to control SCEs is to use two or more gate electrodes and a thin, fully depleted semiconductor body. The idea is to create a large potential curvature in the source and drain direction by introducing a large electrical field gradient in the direction vertical to the gate. The key parameter in this approach is the thickness of the thin, fully depleted semiconductor body. In the case of the multi-gate technologies, the fin width is the thickness of the thin, fully depleted semiconductor body.

(3.1)

is a measure of the short-channel effect. It represents the distance of penetration of the drain electric field in the channel. A small value is desirable to minimize the SCE.

is proportional to the square root of the product of the device body thickness t_{si}, (or Fin width in multi-gate technology) and gate oxide thickness t_{ox}. Thus, one can trade off t_{ox} scaling with Fin width reduction. This approach is not possible for bulk or PDSOI MOSFETs. In a double-gate MOSFET, the center of the fin is the furthest away from the gate electrodes. Therefore, gate control is the weakest at this point. Should punch through occur, it would be in the center of the fin. This implies using a slightly different boundary condition than Equation 3.1, which assumes the punch through is along the channel surfaces.

Using Poisson's equation and Schrödinger equation, equation 3.1 modified to equation 3.2

(3.2)

For good SCE control, assume L_g = n , where n is some arbitrary number. We now have

(3.3)

When Lg = 0, equation 3.3 becomes

(3.4)

Equation 3.4 represents the intercept point of the L_g vs. $\text{Fin}_{\text{WIDTH}}$ plot for Lg = 0. Thus, one can define an effective fin width (FinW_{eff}) as

(3.5)

Equation 3.5 shows that the impact of gate oxide can be considered equivalent to a constant offset of physical fin width. A triple-gate MOSFET with enhanced gate electrostatic control of the channel provides a lower $L_g/\text{Fin}_{\text{WIDTH}}$ ratio than a double-gate FinFET for a same SCE control. $L_g/\text{Fin}_{\text{WIDTH}}$ as low as 1.0 was reported for multi gate devices in [6]. It is worthwhile noting that the minimum feature size in multi gate technology is the fin width ($\text{Fin}_{\text{WIDTH}}$), and not the gate length

3.4.2 FIN HEIGHT

Having understood the requirements on $\mathrm{Fin}_{\mathrm{WIDTH}}$ for SCE control, let us look at how fin pitch and fin height affect the drive current. For a double gate FinFET, the channels are on the sidewalls of the fins. The effective channel width is thus equal to

Where n is an integer number that is equal to the number of fins in a device. W_{eff} of multi gate devices can only be increased or decreased by a discrete amount equal to $2\times\mathrm{Fin}_{\mathrm{HEIGHT}}$. The fin pitch ($P_{\mathrm{FIN}}$) is the spacing between the fins plus the fin width. P_{FIN} is limited by the lithography pattern capability. Exactly one fin can be placed in one P_{FIN}. Therefore, the effective channel width per pitch is $2\times\mathrm{Fin}_{\mathrm{HEIGHT}}$. Figure 3.6 shows the layout comparison between a planar device and a FinFET. For the planar MOSFET, the effective device channel width, W_{eff}, is equal to the footprint on the substrate, W_{foot}. For FinFET, W_{eff} is related to W_{foot} through:

—— (3.6)

If we want the FinFET layout to be competitive, we need Weff ≥ Wfoot or $2\mathrm{Fin}_{\mathrm{HEIGHT}} \geq P_{\mathrm{FIN}}$

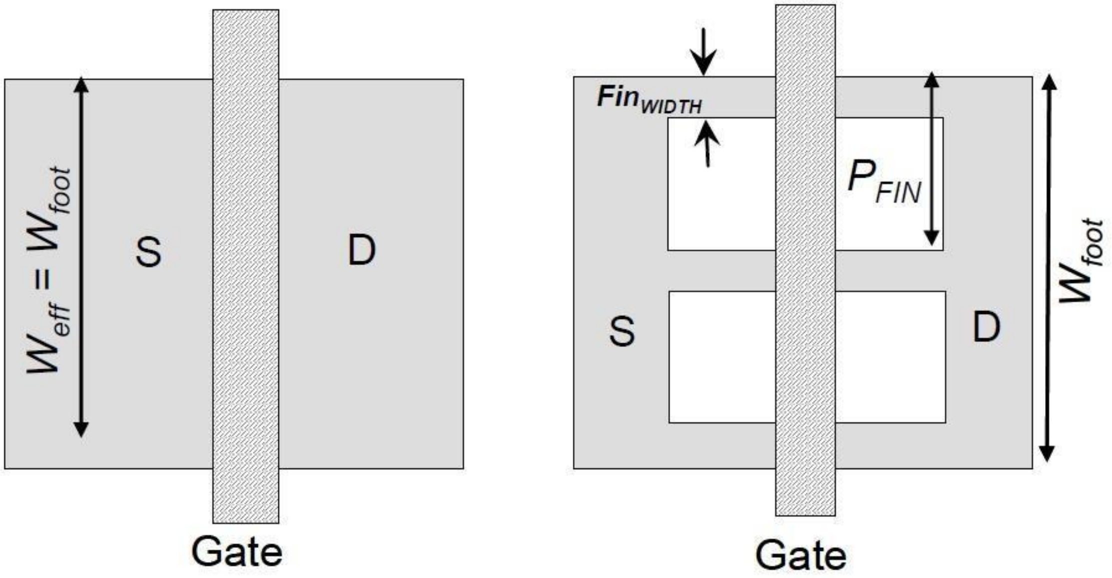

Fig. 3.6 Layout comparison between a planar MOSFET and a typical FinFET

The analysis of the tri-gate channel width is further complicated by the “volume inversion” or “bulk inversion” effect reported in [6]. For thin fins, the inversion charge is not limited to the device surfaces. A large portion of the inversion charge is in the bulk of the fins, even at high gate voltages. Thus, without activating the top gate, multi-gate devices already have a significant charge at the top surface of the fins.

CHAPTER 4

RESULTS AND DISCUSSION

In this thesis report, we have done various simulations to find effect of fin height and fin width on leakage current and drive current, also find the impact of underlap length variation on drive current and DIBL using cozenda TCAD genius simulator over 3D FinFET. Table 2 given below shows data used for simulation which is based on ITRS 2013. In this simulation, we included drift diffusion model, quantum physics, and density gradient model. These models provide deep approach to modelling quantum transport which specifically used for semiconductor device simulation and engineering. Lombardi mobility model is used to reduce mobility at silicon oxide surface.

Parameter	**Value**
Channel length	22nm
Oxide thickness	1nm
Silicon fin height	30nm
Silicon fin thickness/width	5nm
Gate work function	4.5V
Drain/Source doping	1e10^20 cm-3
Channel Doping	1e16

Table 2: Parameter used for simulation

4.1 Mobility Model

Charge carrier mobility is very vital constraint inside carrier transport model. Drift diffusion model evolved in earlier 1980, is also practice in current scenario because of advance mobility models expanded it's capability to submicron transistor. Mobility model is usually split in: small field's response, large field's response and mobility in the channel region. Small electrostatic field's responses have carriers nearly equanimity with crystal structure. Small field's mobility normally represented using μn, μp. Mobility's of charge carrier reliant on phonon scattering and impurity scattering. This phenomenon decreases lower field mobilities of carriers. [6]

4.2 Lombardi Surface Mobility Model

At oxide silicon surface, mobility of carriers could be considerable smaller compare to substrate of MOS device; it's because of scattering of charge carriers at the interface. If consider no scattering at the oxide silicon interface then the current from source to drain about may be increase 35% for MOS device simulation. This model explains mobility's of charge carriers in the channel region.

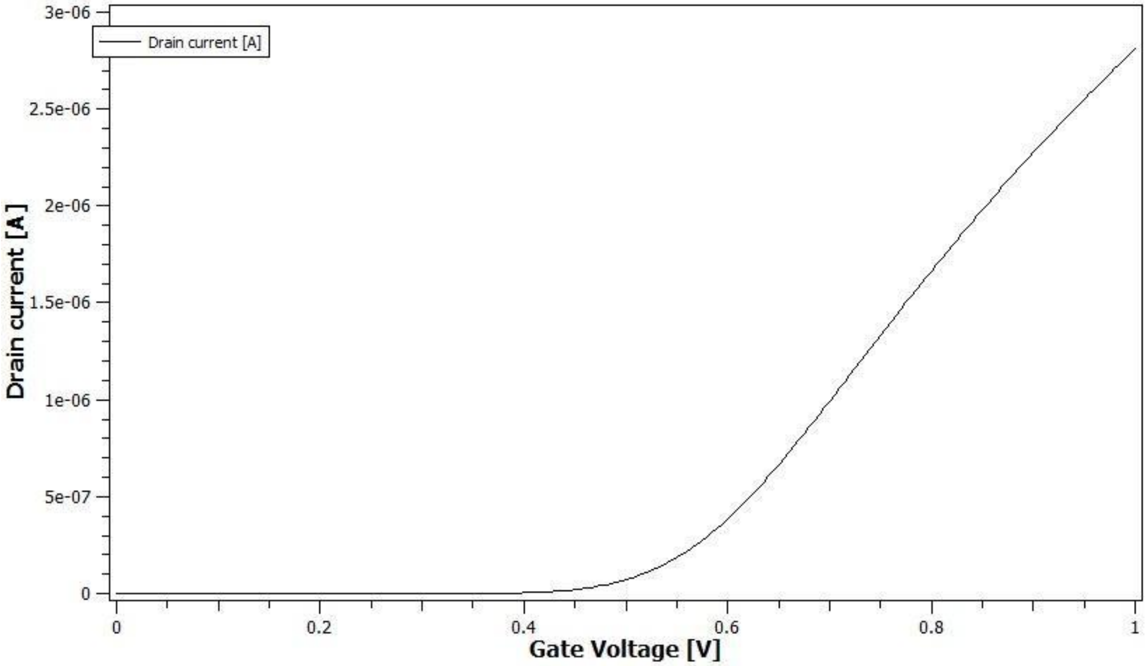

Figure 4.1 Linear scale plots between gate voltage and drain current

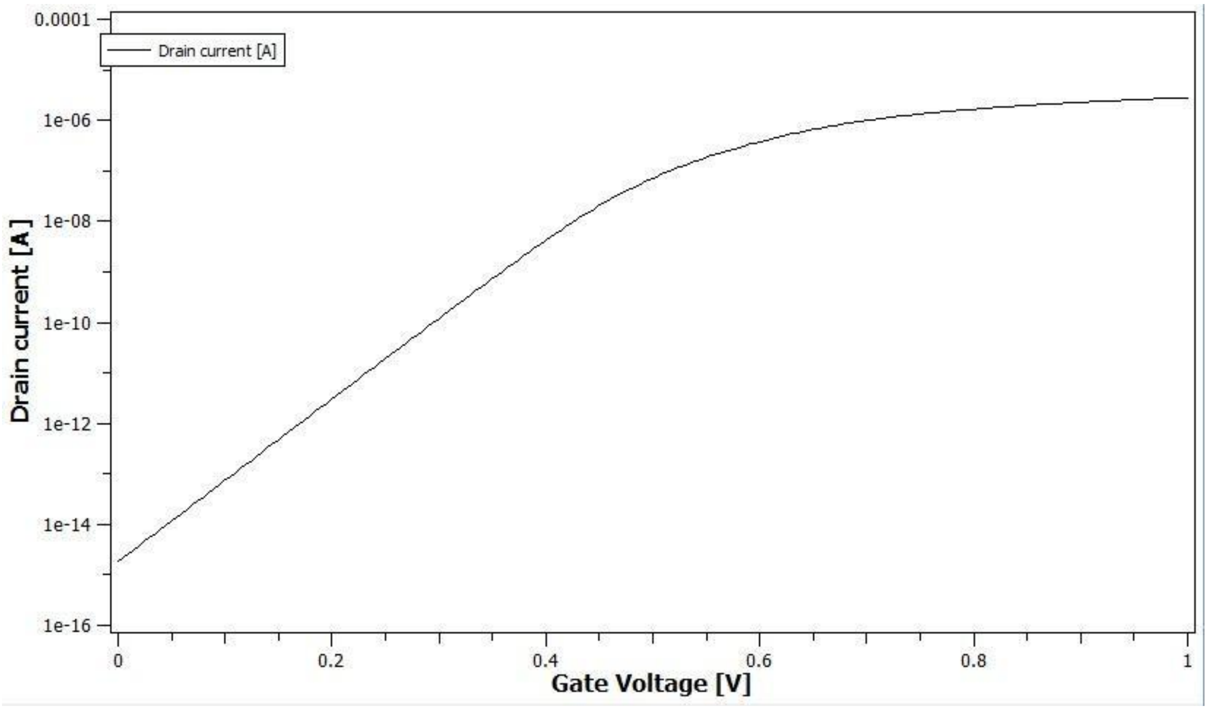

Figure 4.2 logarithmic scale plots between gate voltage and drain current

4.3 Impact of Underlap

Underlap region	**Doping 10^15**	**Doping 10^17**	**Doping 10^19**
1nm	Ioff=5.87x10^-15 Ion=3.59x10^-6 Ion/Ioff=6.1x10^8	Ioff=5.68x10^-15 Ion=3.59x10^-6 Ion/Ioff=6.3x10^8	Ioff=4.16^-15 Ion=3.08x10^-6 Ion/Ioff=7.4x10^8
5nm	Ioff=3.04^-15 Ion=3.36x10^-6 Ion/Ioff=1.1x10^9	Ioff=2.98x10^-15 Ion=3.3x10^-6 Ion/Ioff=1.1x10^9	Ioff=2.01x10^-15 Ion=2.59x10^-6 Ion/Ioff=1.28x10^9
10nm	Ioff=1.84x10^-15 Ion=2.8x10^-6 Ion/Ioff=1.52x10^9	Ioff=1.8x10^-15 Ion=2.78x10^-6 Ion/Ioff=1.54x10^9	Ioff=9.47x10^-16 Ion=1.45x10^-6 Ion/Ioff=1.59x10^9

Table 3: Impact of underlap on leakage current, drive current and Ion/Ioff ratio

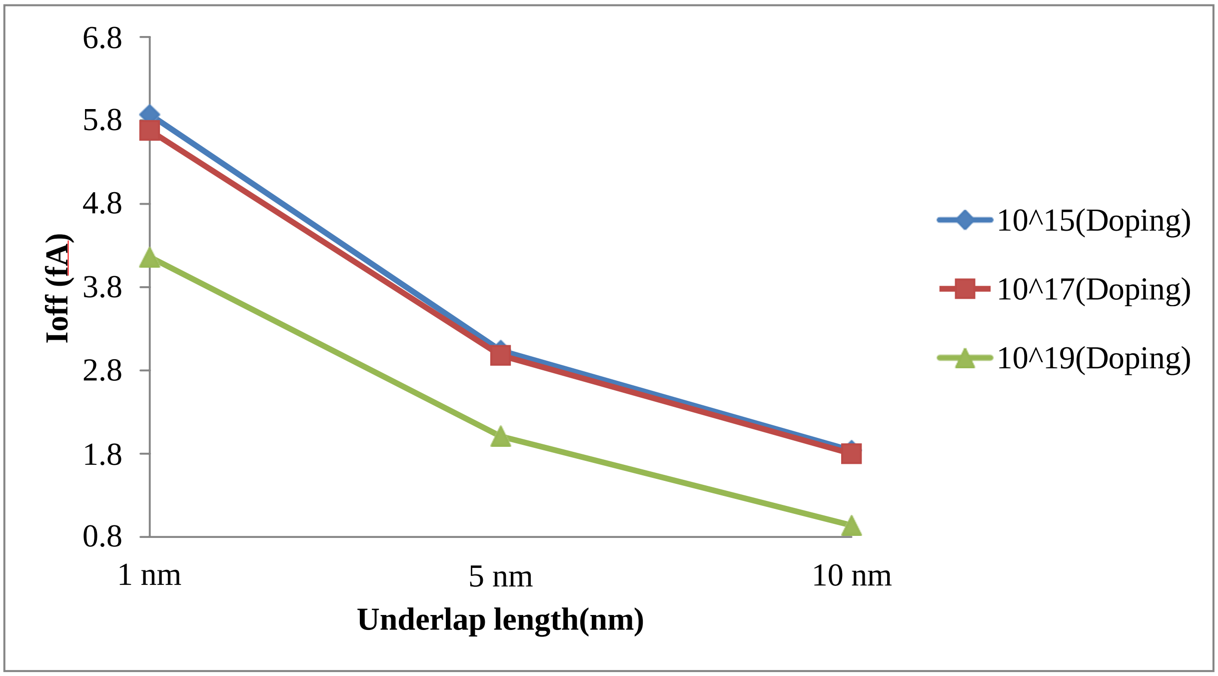

Figure 4.3 plot shows variation of leakage current with different underlap length

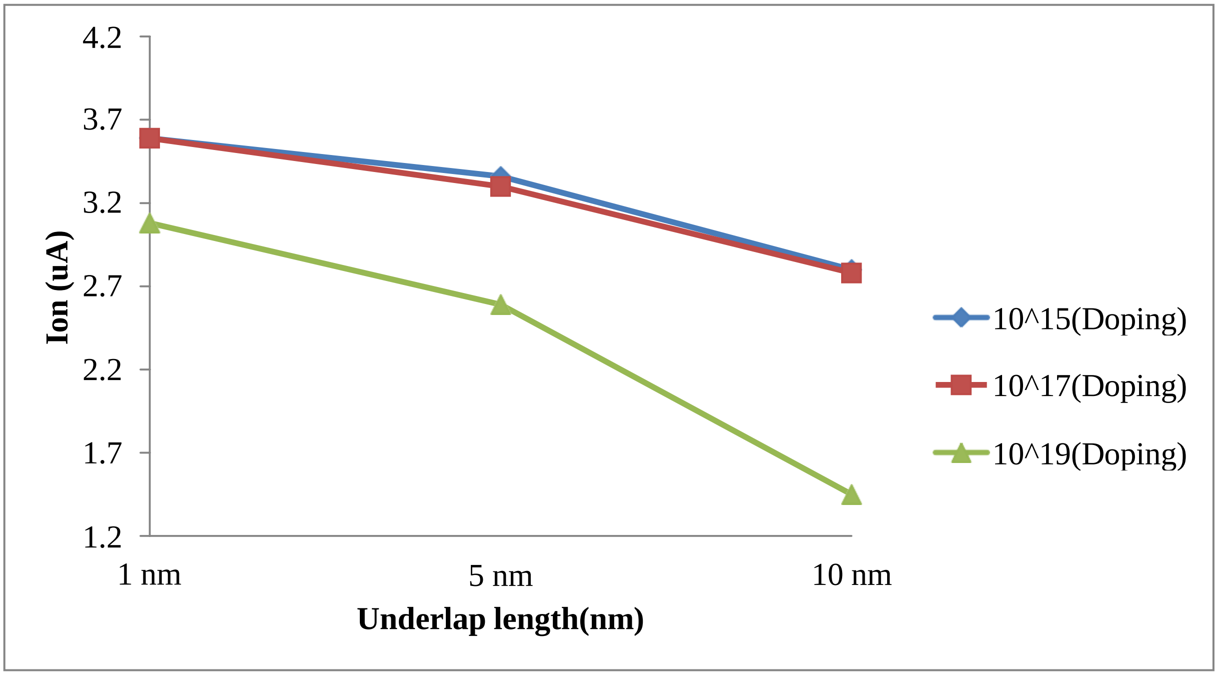

Figure 4.4 plot shows variation of drive current with respect to underlap length

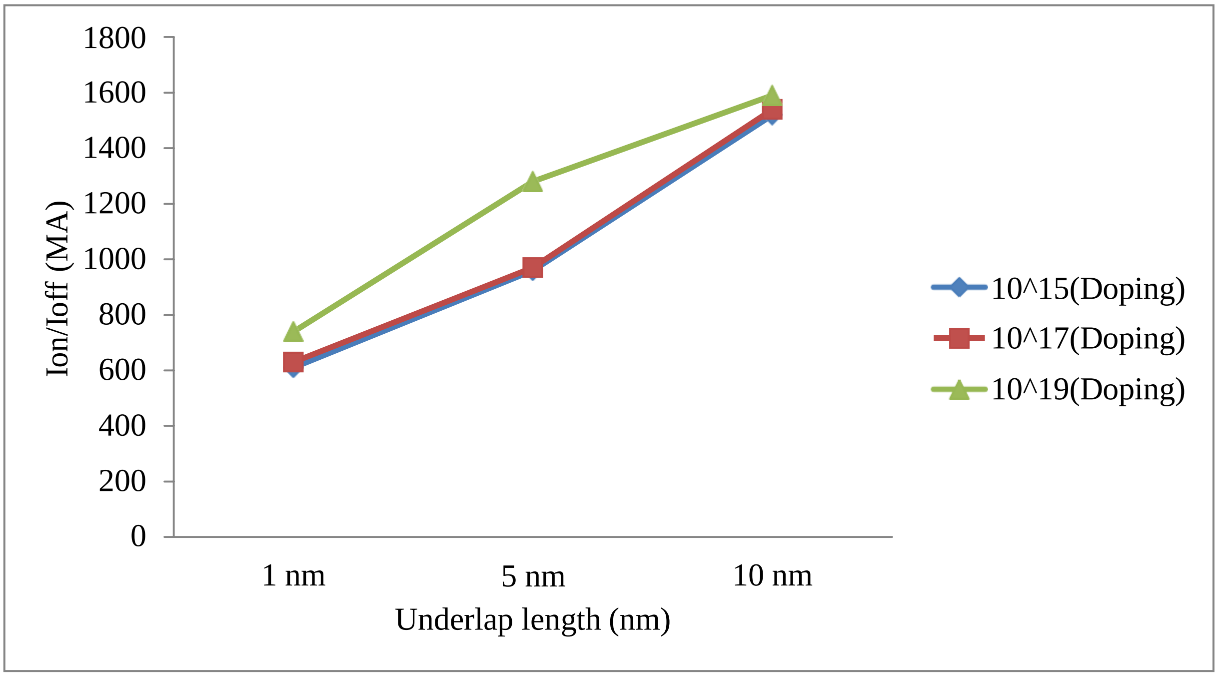

Figure 4.5 plot shows variation of Ion/Ioff with respect to underlap length

Above figures 4.3, 4.4, 4.5 shows, variation of off state leakage current, drive current and on/off current ratio for different underlap length with different channel doping. Around 60% gate capacitances contributed due to fringing electric field emerging from gate electrode to source, drain region. Gate capacitances reduced due to under lapping. Figure 4.3 depicts leakage current variation w.r.t underlap lengths, which shows that with increasing underlap length decrease off state current as increment of channel doping. As underlap length increased device drive current and leakage current reduced on. Additionally, reduce “direct source to drain tunneling component”. Diminution of direct source to drain tunneling as increased underlap is because of increased effectual barrier height which charge carrier face in tunneling from source to drain. As underlap length increased, it will enhance the SS and drain induced barrier lowering

4.4 Impact of fin height, fin width and oxide thickness

Formulae:

Parameter	For Hfin=20 nm	For Hfin=30 nm
Ioff	1.32x10^-15 A	1.811x10^-15 A
Ion	0.25x10^-5 A	0.65x10^-5 A
Ion/Ioff	1.8x10^9 A	3.5x10^9 A
Vth	0.14 V	0.13 V
SS (subthreshold swing)	70 mV/dec	65 mV/dec

Table 4: Impact of fin height in linear region for channel doping 10^16

Parameter	For Hfin=20 nm	For Hfin=30 nm
Ioff	1.5x10^-15 A	2.25x10^-15 A
Ion	1.2x10^-5 A	2.7x10^-5 A
Ion/Ioff	8.2x10^9 A	1.24x10^10 A
Vth	0.12 V	0.115 V
SS (subthreshold swing)	70 mV/dec	70 mV/dec

Table 5: Impact of fin height in saturation region for channel doping 10^16

DIBL = (0.14 – 0.12) /(0.75 – 0.05)

DIBL = 28.57 mV/V for Hfin = 20 nm

DIBL = (0.13 – 0.115) / (0.75 – 0.05)

DIBL = 21.14 mV/V for Hfin = 30 nm

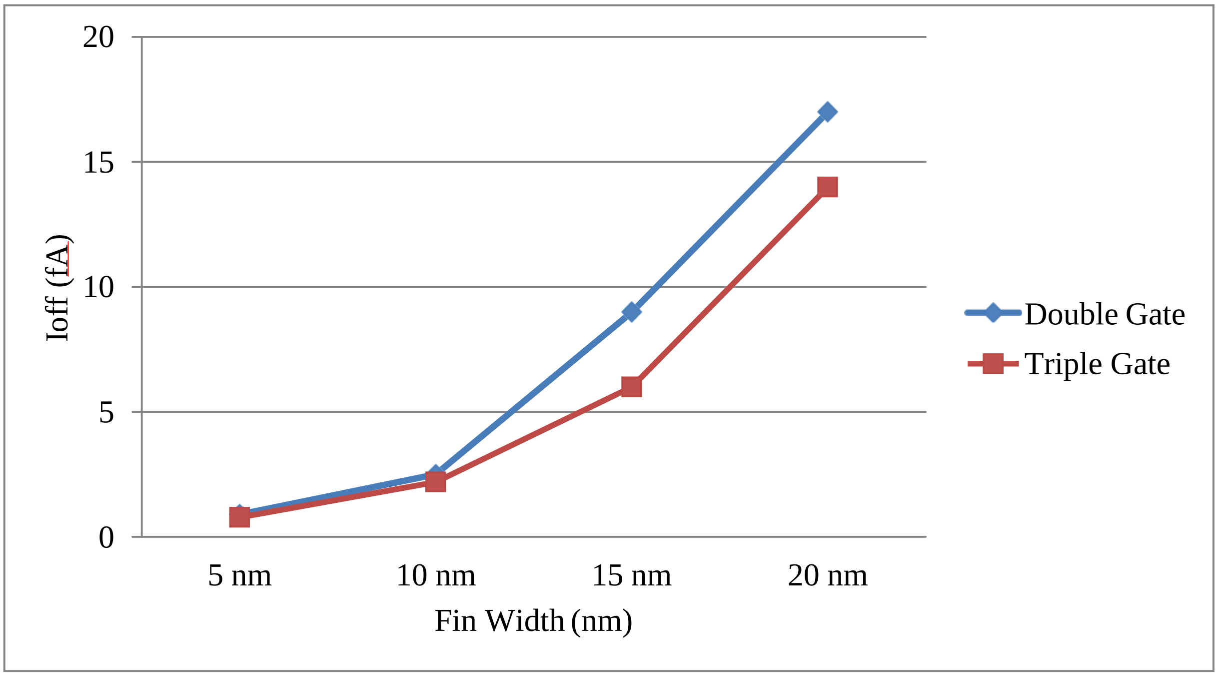

Figure 4.6 Variation of off state current (leakage current) with respect to fin width

Off current of transistor means current in device when no gate potential applied. Off state current flows in device when gate potential is zero and drain potential is highest possible i.e supplied voltage. In figure 4.6 we considered four different fin widths. Off state current increased as increased in fin breadth because of reduction in gate supremacy on channel. Subthreshold leakage current furthermore decreased with decreasing of fin breadth due to off state current occur in center of fin (volume inversion), which is far away from gate. But with decreasing of fin breadth, center part of fin getting more grips from gate, that’s why off state current reduced.

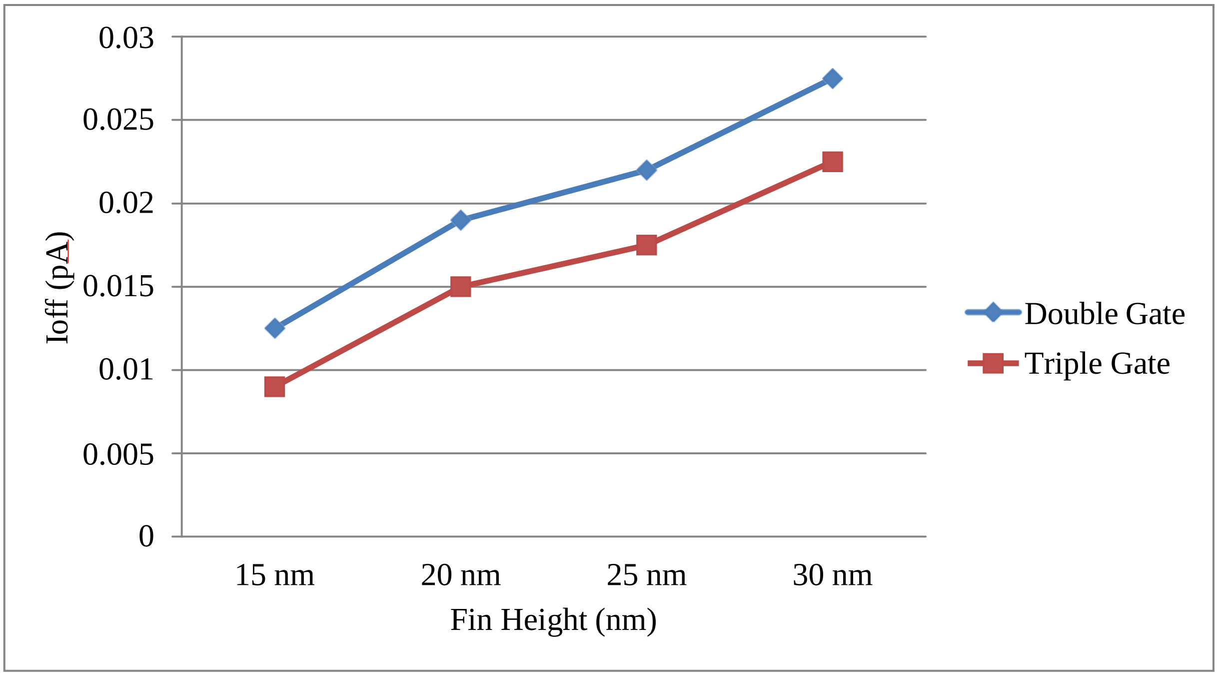

Figure 4.7 Variation of off state current (leakage current) with respect to fin height

With decreasing of “fin height”, off state current reduced due to increasing of “parasitic resistances”. Parasitic resistances divide in 3 parts, source-drain sheet resistance “RSD”, contact resistances “Rcontact”, and extension resistance “Rext”. Source-drain sheet resistance and contact resistance calculated from wafer, extension resistance for taller fin is double the smaller fin. Figure 4.7 depicts change in off state current for double gate and triple gate FinFET w.r.t fin height. Higher the fin height, lower will be off sate current. Graph shows more off state current reduction for triple gate FinFET.

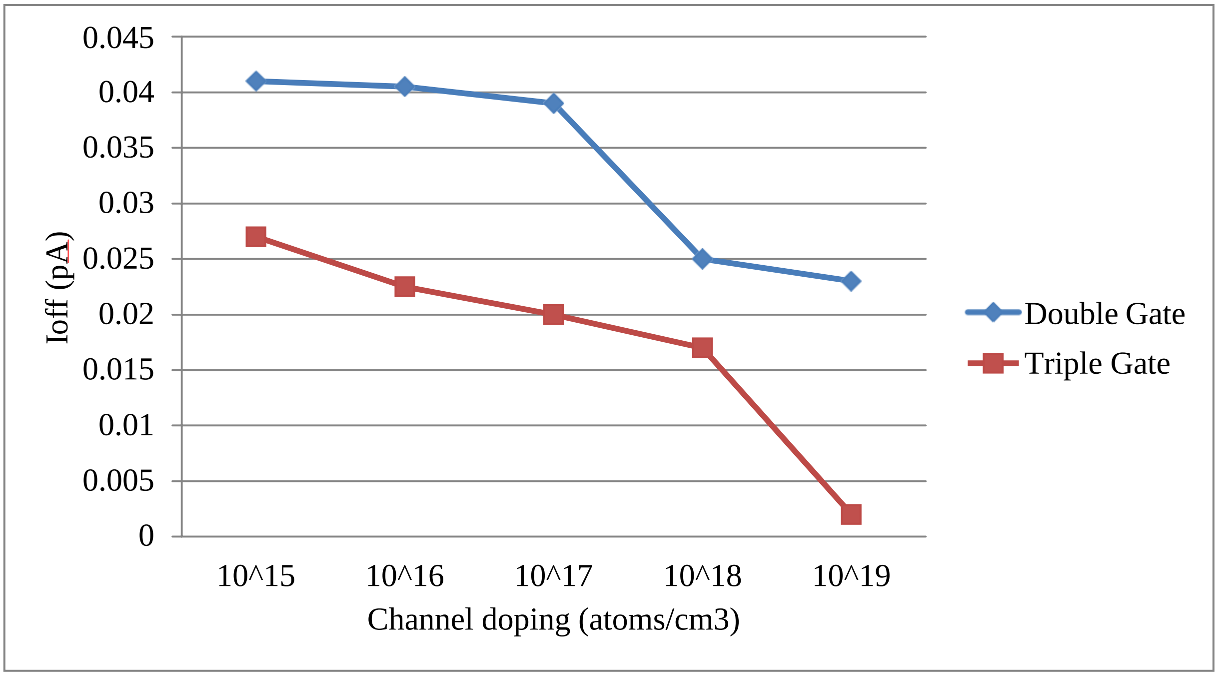

Figure 4.8 Variation of off state current (leakage current) w.r.t channel doping

As doping increased, mobilities reduced therefore drive current reduced in linear fashion but subthreshold leakage current decreased exponentially. This results into increased in on to off current ratio. Figure 4.8 show that alteration of off current in double gate and triple gate FinFET as altering channel doings. With higher channel doping, off state current reduced in double gate and triple gate FinFET. Here is large decrease for triple gate FinFET. Hence, from this graph it is clear that as number of gate increased, it provides better controlling over channel and reduced off state current. Using different dielectric and different gate electrode can reduce more off state current for double gate and triple gate FinFET.

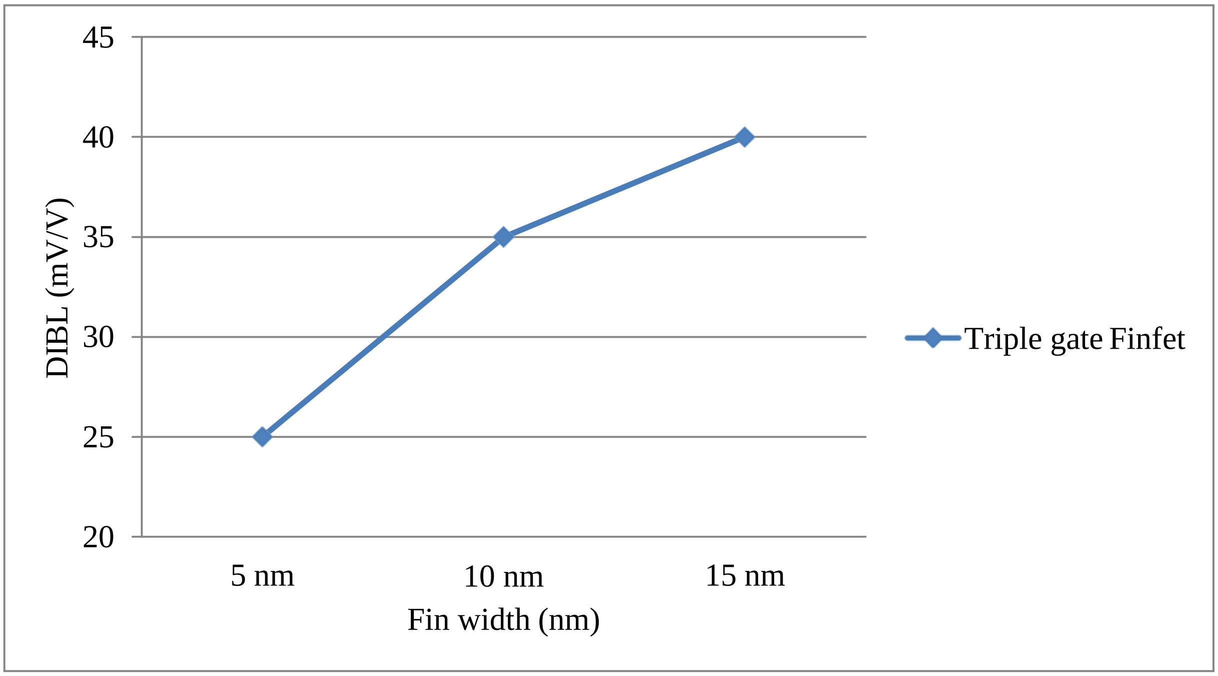

Figure 4.9 Variation in DIBL with respect to fin width

When we increased fin width (>> Lg/3), then gate lost its supremacy over the channel region which raised subthreshold leakage current where gate leakage current little bit influenced because of increased gate area. Fig. 4.8 shows impact of fin breadth on drain induced barrier lowering. “Drain induced barrier lowering” highly delicate to variation of fin width. Hence, smaller fin width has good control on "DIBL” compare large width of fin.

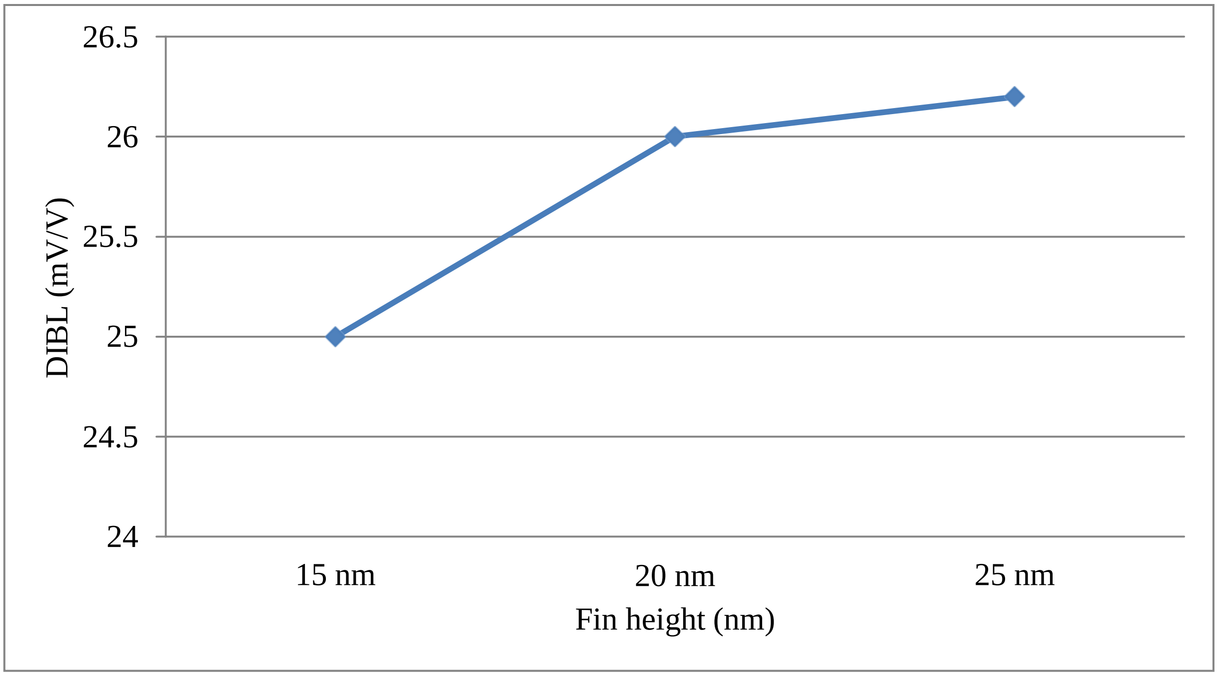

Figure 4.10 Variation in DIBL with respect to fin height

Drain induced barrier lowering rises moderately with rise of fin height because upper gate lost it's supremacy on deep down part of channel region as seen in Fig. 4.9.

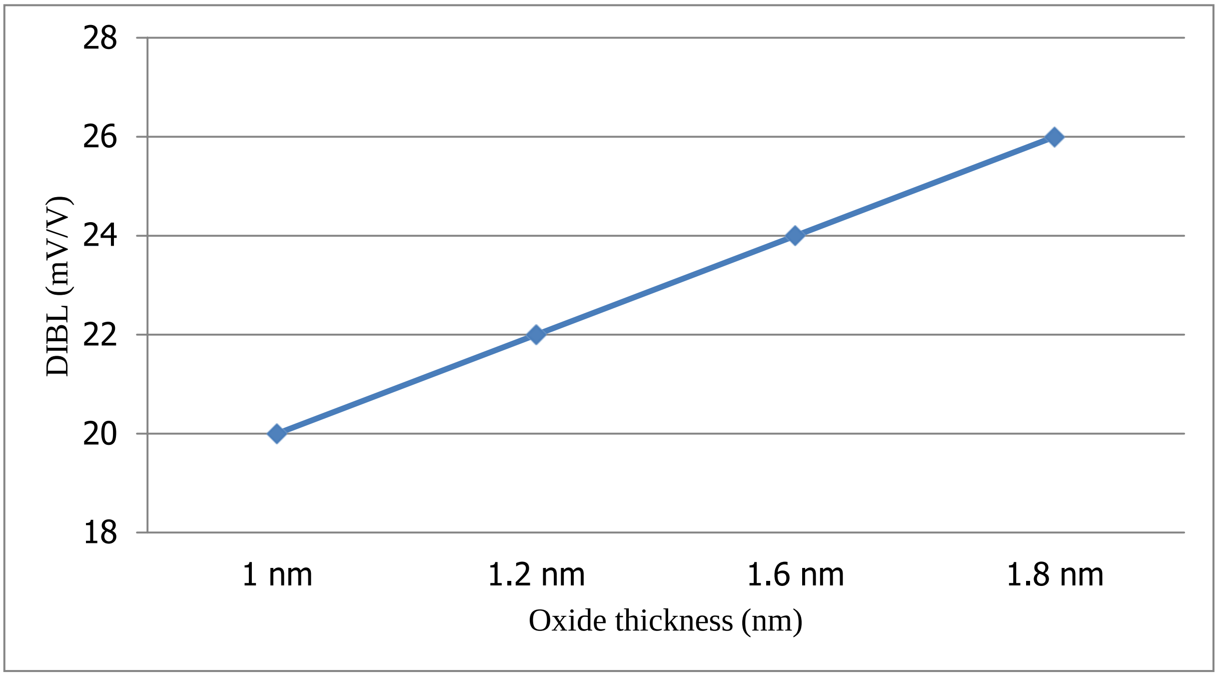

Figure 4.11 Variation in DIBL with respect to oxide thickness (nm)

Oxide width plays strong role to leakage current contributions in sub micron structures which used thinner gate dielectric. After 45 nm technologies node with the oxide width reduced beyond 2 nm, due to tunneling gate oxide, gate current increased above the subthreshold current therefore it required to improve for small power application. Impact of gate oxide thickness over SCEs is shown in Figure 4.9. Drain induced barrier lowering reduced with increased oxide width because of the raised SCEs

CHAPTER 5

CONCLUDING REMARKS AND FUTURE SCOPE

From the results, it is concluded that FinFETs are extremely fast and power efficient devices, as device dimension is scaled down to smaller technology, its drive current is very large in comparison to leakage current that means ratio of on to off current is very large. The multi-gate structures lead to great supremacy over inversion layer and give small SCEs. The FinFETs are difficult to fabricate with excellence due to its smaller size (nano scale). Changes in physical structures, dimensions and different material are utilized to achieve higher drive current, speed, and threshold voltage. Off state current increased with increased fin width due to lack of gate control over the channel area, so we need to keep fin width under control to improves DIBL. The off state current decrease with decrease in fin-width as center part of fin getting more grips from gate.

With decrease in fin height, off state current reduces due to increasing of parasitic resistances. The Extended fin height offers more resistance in comparison of smaller fin height, which leads to low off state current.

Gate capacitances due to fringing electric field reduces due to increase in underlap length and hence a decrease in off state current. Also as underlap length increases the sub-threshold slope improves and drain induced barrier lowering reduces.

To further scaled down the dimension of FinFET various short channel and nano channel effects comes in the picture. To overcome this effects the MOSFET structure are need to modified as well as channel engineering and new materials are required..

REFERENCES

[1] Gorden E. Moore, “Cramming more components onto integrated circuits,” *Proceedings of IEEE,* 1965.

[2] Kaushik Roy, Saibal Mukhopadhyay and Hamid Mahmoodi Meimand," Leakage Current Mechanisms and Leakage Reduction Techniques in Deep Sub micrometer CMOS Circuits" *Proceedings. of the IEEE,* 2003

[3] Kunihiro Suzuki and Sergey Pidin, “Short channel single gate SOI MOSFET model”, *Proceedings of IEEE,* 2003

[4] W. Wu1, X. Li1, G. Gildenblat1, G. Workman, “PSP SOI: A Surface Potential Based Compact Model of Partially Depleted SOI MOSFETs”, *Proceedings of IEEE,* 2007

[5] Sajitha Soman, D Nirmal, “Analysis of Drain Current in Short Channel Drain extended Triple Gate FinFET”, *Proceedings of IEEE,* 2013

[6] J.P. Colinge and J.T. Park, " Multiple gate SOI MOSFET: Device design guidelines”, IEEE Trans. Electron Devices, 2002

[7] Cheng Hsien Chang, Jyi Tsong Lin, “A Novel 14 nm Extended Body FinFET for Reduced Corner Effect, Self-Heating Effect, and Increased Drain Current”, World Academy of Science Engineering and Technology, 2013

[8] Aniket, A. Breed Kenneth, P. Roenker, “Comparison of the scaling characteristics of nanoscale SOI N-channel multiple-gate MOSFETs”, Springer, 2008

[9] D.Nirmal, P.Vijaya Kumar**, “**A Review of Nanoscale Channel and Gate Engineered FinFETs for VLSI Mixed Signal Applications Using Zirconium dioxide Dielectrics”, journal of engineering science and technology review, 2014

[10] Yannis Tsividis, “Operation and modeling of the mos transistor”

[11] Mehdi Saremi, Ali Afzali Kusha, Saeed Mohammadi, "Ground plane fin-shaped field effect transistor (GP-FinFET): A FinFET for low leakage power circuits", Brick nanotechnology center, 2012

[12] S L Tripathi ,Ramanuj Mishra ,Vadthiya Narendra ,R A Mishra, "Optimization of Pie gate Bulk FinFET Structure", International Journal for computer application, 2012

[13] B. Lakshmi and R. Srinivasan, "Effect of gate electrode work function in conventional and junctionless FinFETs", International Journal for Physical science, 2012

[14] Mahender Veshala, Ramchander Jatooth, Kota Rajesh Reddy, "Reduction of Short Channel Effects in FinFET", IJEIT, 2013

[15] Dongil Kim, Yesung Kang, and Youngmin Kim, *et al,* Simple and Accurate Modeling of Double Gate FinFET Fin Body Variations, *Proceedings. of the IEEE,* 2012

[16] Kiran Bailey and K. S. Gurumurthy*, et al, "*3D Device Modeling and Assessment of Triple Gate SOI FinFET for LSTP Applications", International Journal of Computer Theory and Engineering, 2012

[17] Nour El Islam Boukortt, *et al* "3-D Simulation of Nanoscale SOI n-FinFET at a Gate Length of 8 nm Using ATLAS SILVACO", Transactions on electrical and electronic material, 2015

[18] Hailiang Zhou, Bingcai Sui, *et al* ,"Numerical Study of DIBL effect in Carbon Nanotube FETs", *Proceedings. of the IEEE,* 2009

[19] Sarika Bukkawar, *et al,* **"**Low leakage Nanoscaled Source and Drain over insulator Finfet with underlap and high k dielectric", 2012, IJEST

[20] Revathy. G, Dr. Abdul Rajak, "A Survey on Finfet: Technology, Pros, Cons and Improvement Prospects, IJATES, 2014

APPENDIX

Genius cozenda software coding for 3D triple gate FinFET

```
GLOBAL    T=300 DopingScale=1e20 Z.Width=0.02 ResistiveMetal=false

# Create an initial simulation mesh

 MESH      Type = S_Tet4  tetgen="pzAq"

X.MESH    WIDTH=0.025  N.SPACES=8

X.MESH    WIDTH=0.005  N.SPACES=6

X.MESH    WIDTH=0.022   N.SPACES=10

X.MESH    WIDTH=0.005  N.SPACES=6

X.MESH    WIDTH=0.025  N.SPACES=8

Y.MESH    DEPTH=0.005  N.SPACES=3

Y.MESH    DEPTH=0.020   N.SPACES=4

Y.MESH    DEPTH=0.060  N.SPACES=10

Z.MESH    WIDTH=0.005  N.SPACES=3

Z.MESH    WIDTH=0.025  N.SPACES=14

Z.MESH    WIDTH=0.005  N.SPACES=3


#Specify oxide and silicon regions

REGION    Label=NGate     Material=NPoly   X.MIN=0.03   X.MAX=0.052   Z.MIN=0.0055
Z.MAX=0.0295 Y.MIN=0.001    Y.MAX=0.025

REGION    Label=NOxide    Material=Ox      X.MIN=0.03   X.MAX=0.052   Z.MIN=0.0085
Z.MAX=0.0265 Y.MIN=0.003    Y.MAX=0.025

REGION    Label=SPS       Material=Nitride X.MIN=0.025  X.MAX=0.030   Z.MIN=0.0
Z.MAX=0.035  Y.MIN=0.0      Y.MAX=0.025
```

```
REGION    Label=SPD       Material=Nitride X.MIN=0.052  X.MAX=0.057   Z.MIN=0.0
Z.MAX=0.035  Y.MIN=0.0      Y.MAX=0.025

REGION    Label=NSiliconL Material=Si      X.MIN=0.00   X.MAX=0.025   Z.MIN=0.005
Z.MAX=0.030  Y.MIN=0.003    Y.MAX=0.025

REGION    Label=NSiML     Material=Si      X.MIN=0.025  X.MAX=0.030   Z.MIN=0.0112
Z.MAX=0.0238 Y.MIN=0.0042   Y.MAX=0.025

REGION    Label=NSiliconM Material=Si      X.MIN=0.030  X.MAX=0.052   Z.MIN=0.0112
Z.MAX=0.0238 Y.MIN=0.0042   Y.MAX=0.025

REGION    Label=NSiMR     Material=Si      X.MIN=0.052  X.MAX=0.057   Z.MIN=0.0112
Z.MAX=0.0238 Y.MIN=0.0042   Y.MAX=0.025

REGION    Label=NSiliconR Material=Si      X.MIN=0.057  X.MAX=0.082   Z.MIN=0.005
Z.MAX=0.030  Y.MIN=0.003    Y.MAX=0.025

REGION    Label=NSource   Material=Al      X.MIN=0.0    X.MAX=0.025   Z.MIN=0.005
Z.MAX=0.030  Y.MIN=0.002    Y.MAX=0.003

REGION    Label=NDrain    Material=Al      X.MIN=0.057  X.MAX=0.082   Z.MIN=0.005
Z.MAX=0.030  Y.MIN=0.002    Y.MAX=0.003

REGION    Label=SUB      Material=Si       X.MIN=0.0    X.MAX=0.082   Z.MIN=0.00
Z.MAX=0.035  Y.MIN=0.025    Y.MAX=0.085

REGION    Label=NOxideDF  Material=Ox      X.MIN=0.0    X.MAX=0.082   Z.MIN=0.00
Z.MAX=0.0175  Y.MIN=0.025    Y.MAX=0.060

REGION    Label=NOxideBF  Material=Ox      X.MIN=0.0    X.MAX=0.082   Z.MIN=0.0175
Z.MAX=0.035  Y.MIN=0.025    Y.MAX=0.060


#Doping region define

DOPING    Type=analytic

PROFILE   Type=Uniform Ion=Acceptor  N.PEAK=1.0E18    X.MIN=0.025  X.MAX=0.057
Z.MIN=0.0104  Z.MAX=0.0246 Y.MIN=0.005 Y.MAX=0.025

PROFILE   Type=Uniform Ion=Acceptor  N.PEAK=1.0E15    X.MIN=0.0    X.MAX=0.082
Z.MIN=0.00   Z.MAX=0.035 Y.MIN=0.037  Y.MAX=0.085
```

```
PROFILE   Type=Uniform Ion=Donor    N.PEAK=1.1E20    X.MIN=0.00   X.MAX=0.025
Z.MIN=0.005  Z.MAX=0.030 Y.MIN=0.00333  Y.MAX=0.025

PROFILE   Type=Uniform Ion=Donor    N.PEAK=1.1E20    X.MIN=0.057  X.MAX=0.082
Z.MIN=0.005  Z.MAX=0.030 Y.MIN=0.00333  Y.MAX=0.025

#PROFILE   Type=analytic Ion=Acceptor N.PEAK=1.0E18    X.MIN=0.0 X.MAX=0.082
Z.MIN=0.00 Z.MAX=0.035 Y.MIN=0.037  Y.MAX=0.039 Y.Char=0.025


EXPORT   CGNSFILE=FINFET_ANU_14nm.cgns

Contact ID=NGate Type=gatecontact workfunction=4.5

#Import CGNSFile=FINFET_iv.cgns

Model Region=NSiliconM

PMI Region=NSiliconM Type=mobility Model=Lombardi Print=1

Model Region=NSiML

PMI Region=NSiML Type=mobility Model=Lombardi Print=1

Model Region=NSiMR

PMI Region=NSiMR  Type=mobility Model=Lombardi Print=1

#Contact ID=NGate Type=gatecontact workfunction=4.7

# Voltage sources are needed here.

Vsource Type = VDC    ID = GND    Vconst=0

Vsource Type = VDC    ID = VD     Vconst=0.75

Vsource Type = VDC    ID = VGATE  Vconst=1

Method Type=Poisson damping=Potential ns=Newton

Solve

METHOD Type=DDML1 NS=Newton LS=MUMPS damping=potential maxit=100

#Method Type="DDML1" NS=Basic damping=potential ls=MUMPS maxiteration=90

Solve Type=DC Label="ramp1" VScan=NDrain VStart=0 VStop=0.75 VStep=0.005
out.prefix="ramp1"
```

```
ATTACH    Elec=NDrain    Vapp=VD

Attach Electrode=NSource Vapp=GND

METHOD    Type=DDML1 NS=Newton LS=MUMPS maxiteration=50

SOLVE     Type=DC  Vscan=NGate   Vstart=0.0 Vstep=0.05 Vstop=1.0 out.prefix=gate_iv

EXPORT   VTKFILE=FINFET_iv.vtk CGNSFILE=FINF
```

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