Power-Factor Correction for AC-DC Converter

A dissertation submitted in partial fulfillment for the requirement of the degree

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Submitted by

JAHANGEER AHMAD DAR

801742013

Under the Guidance of

Dr. SANTOSH SONAR

Assistant Professor, EIED

THAPAR INSTITUTE
OF ENGINEERING & TECHNOLOGY
(Deemed to be University)

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Electrical and Instrumentation Engineering Department Thapar Institute of Engineering and Technology, Patiala

(Declared as Deemed-to-be-University u/s 3 of the UGC Act., 1956)

Post Bag No. 32, Patiala – 147004
Punjab (India)

DECLARATION

I hereby certify that the work which is presented in dissertation entitled, **"Power Factor Correction for AC-DC Converter"**, in partial fulfilment of the requirements for the award of the degree of Master of Engineering in Power Systems, submitted to Electrical & Instrumentation Engineering Department of Thapar Institute of Engineering & Technology (Deemed to be University) is as authentic record of my own work carried under the supervision of **Dr Santosh Sonar**. It refers others researcher's work which are duly listed in the reference section. The matter contained in this dissertation has not been submitted, neither in part nor in full to any other degree to any other university or institute except as reported in text and references.

Jahangeer

Place: PATIALA **(JAHANGEERAHMAD DAR)**

Date: 7-Aug-2019 **Roll No. 801742013**

It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

(Dr Santosh Sonar)

Date: 7/8/2019

Assistant Professor
Electrical & Instrumentation Engineering Department
Thapar Institute of Engineering & Technology, Patiala

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JAHANGEER AHMAD DAR

(801742013)

ABSTRACT

The conversion of A.C into D.C determines the distortion of the mains current A.C., which degrades the input power factor. The main reason for a poor power factor is the non-linear nature of the circuit. The power factor is improved by using a basic boost converter and a control technique based on the fixed off time (FOT) approach .The traditional approach to the correction of the power factor in the boost converter is the continuous conduction mode with fixed frequency (FF-CCM) and the transition mode (TM) PWM (fixed connection time, variable frequency). In the first mode, the inductor operates in continuous conduction mode (CCM) and uses the average current-mode control mode, a complex technique involves a considerable quantity of components. The second method uses the more complex control technique of the peak current mode that makes the inductor work between continuous and discontinuous mode, which uses fewer components, unstable greater than 50% duty cycle and is more cost efficient .A third approach, the fixed off time (FOT) is gaining popularity which is conditionally stable for a duty cycle of over 50% and does not need compensation.

The dissertation involves the work carried out to use the power factor correction (PFC) based with the DC-DC Flyback converter. To verify the design and operation of the circuit, the simulation is performed in PSIM. Finally, to illustrate the implementation of the proposed technique, a 24 volt battery charging circuit is selected. The CCCV charging mode is also explained using the look up table concept.

Keywords: -Fixed-Frequency continuous conduction mode (FF-CCM), Transition mode (TM), Fixed OFF Time (FOT), Power factor correction (PFC)

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LIST OF ABBREVIATIONS

ACRONYMS	FULL FORM
PFC	Power Factor Correction
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
FOT	Fixed Off Time
IEC	International Electro Technical Commission
THD	Total Harmonic Distortion
AC	Alternating Current
DC	Direct Current
CENELEC	European Committee For Electro Technical Standardization
RMS	Root Mean Square
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IGBT	Insulated-Gate Bipolar Transistor
CM	Common Mode
EMI	International Electro Technical Commission
PI	Proportional Integral
TM	Transition Mode
MAOF	Modified-Adaptive-Off-Time
COT	Constant On Time
NTC	Negative Temperature Coefficient
CRT	Cathode Ray Tube
BOM	Bill Of Material
RCD	Resistor Capacitor Diode
CCCV	Constant Current Constant Voltage

LIST OF TABLES

ORGANIZATION OF THESIS

The thesis is divided into six chapters as follow,

- **CHAPTER-1,** discusses various power factor techniques. The appropriate harmonic standards are mentioned.
- **CHAPTER-2,** presents the literature survey related to Fixed Off Time technique.
- **CHAPTER-3,** explains the working of various control techniques including peak current control and average current control.
- **CHAPTER-4,** deals with design of PFC circuit, Flyback converter and RCD clamping circuit.
- **CHAPTER-5,** validation of design and circuit is presented in this chapter.
- **CHAPTER-6,** conclusion and future scope of the work is presented here.

CHAPTER -1

INTRODUCTION

CHAPTER OVERVIEW

The chapter starts with the introduction of power factor correction techniques .The concept of power factor for linear and non linear loads is explained .Further harmonic standards for power factor correction are given.

1.1 POWER FACTOR CORRECTION

Power factor correction (PFC) circuit is used to shape the input current based on the rectified half sinusoid voltage sensed at the output of bridge rectifier. The PFC circuit helps in maximizing the amount of real power drawn from ac mains and to minimize the harmonic stress caused by current harmonics on AC system .The electrical equipment connected to the ac mains circuit should exhibit pure resistor behaviour ,but due the non linear nature of equipment connected with the AC mains the current drawn from the AC mains is not exact replica of AC voltage as some amount deviation in terms of phase difference is present between input voltage and current. Thus, PFC is needed to achieve the near unity power factor which in turn will help in mitigation of input current harmonics. There are various drawbacks associated with poor power factor such as

- High input current harmonics
- Low rectifier efficiency due to the large value of rms current
- Distortion in the input AC voltage because of the peak currents

Without PFC, input power factor at the input side is found as 0.6 and requires large inductor for high input power factor [1]

One of the other reason of adopting the PFC circuit is to follow the international standards like IEC 61000-3-2.

1.1.1 POWER FACTOR

Power factor is defined as the ratio of Real power (P) to apparent power(S) i.e.

$$cos\theta = \frac{\boldsymbol{Realpower\ (Watt)}}{\boldsymbol{ApparentPower(VA)}} \quad (1.1)$$

Where *Real power* or true power is the actual measurement of amount of power used and is represented in watts while as ***Apparent Power*** is combination of ***Real power*** and ***Reactive power*** (measured in Volt-Amps-Reactive) and is represented in Volt-Amps (VA). Power factor gives the degree of utilisation of real power from the available power.

The above definition of power factor is legitimate only if voltage and current are having similar shape i.e. sinusoidal which is possible only for linear loads (load which takes current proportionally to the voltage applied).

The input circuit of Switch mode power supply presents non linear load to ac mains. The input ac is given to the bridge rectifier, a capacitor is connected across the capacitor which maintains the voltage proportional to peak of ac input voltage as shown in Fig. 1.1.

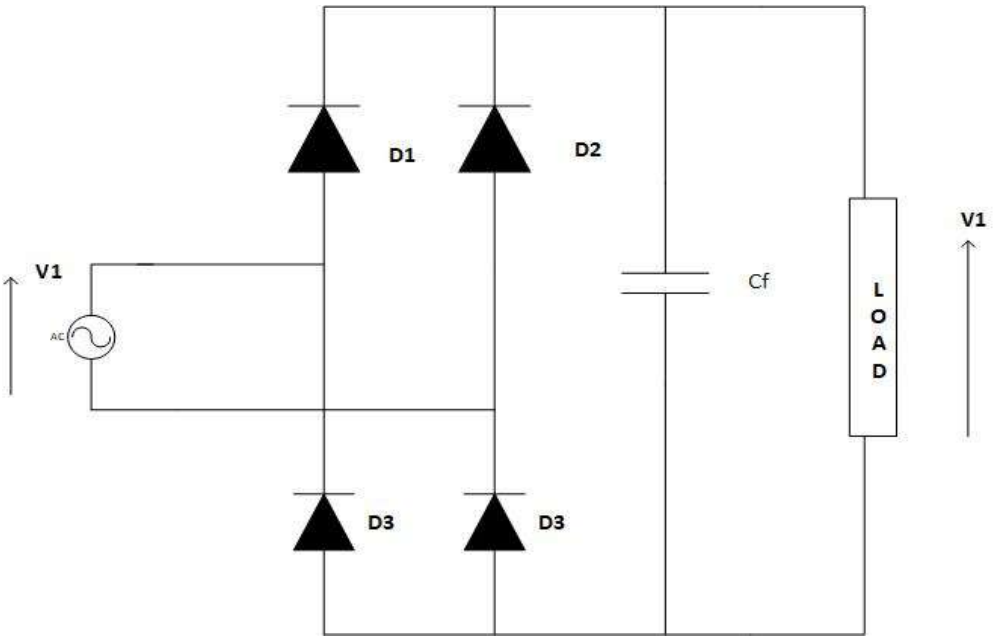


Fig. 1.1: Diode Bridge Rectifier

During each peak of ac input the capacitor gets charged. Thus, current is drawn only when the peak of input waveform and the pulse of current is large enough to sustain the load at the output till the next peak of waveform. It achieves that by dumping a large amount of charge in short interval of time. The duration of the current pulse is only 10% to 20% but the amplitude of current pulse is 5 to 10 times the average current. The phenomenon is illustrated in Fig. 1.2.

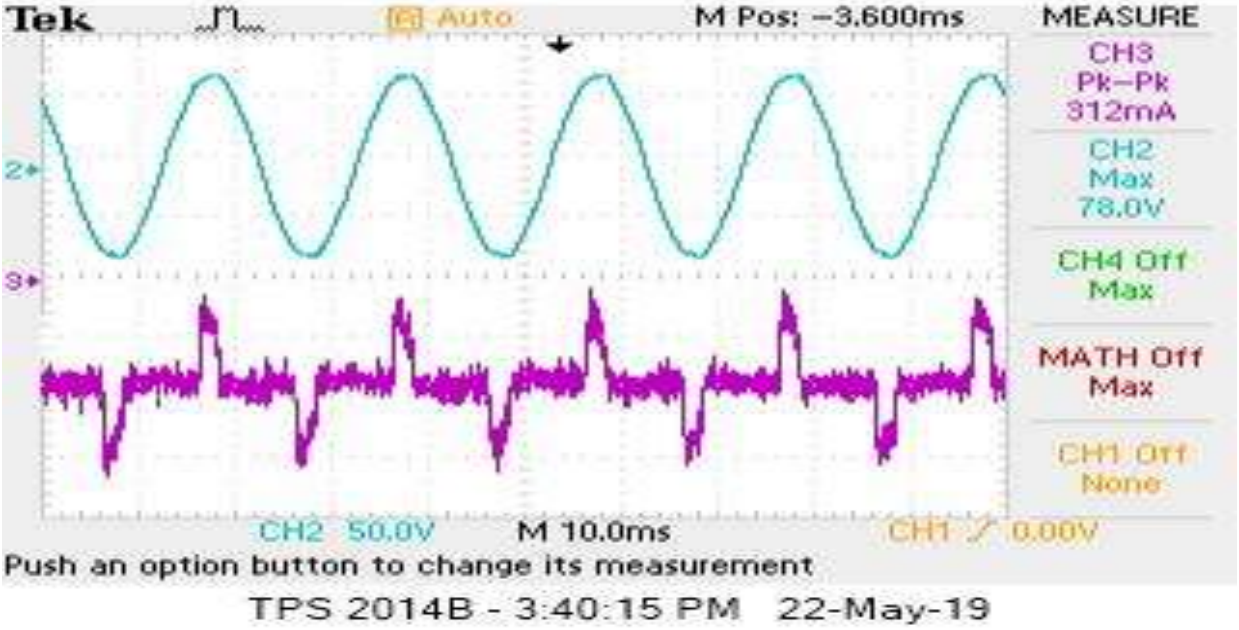
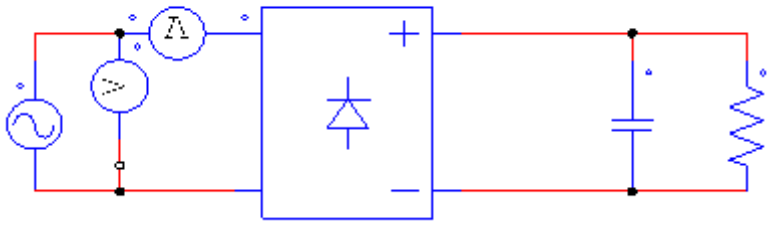
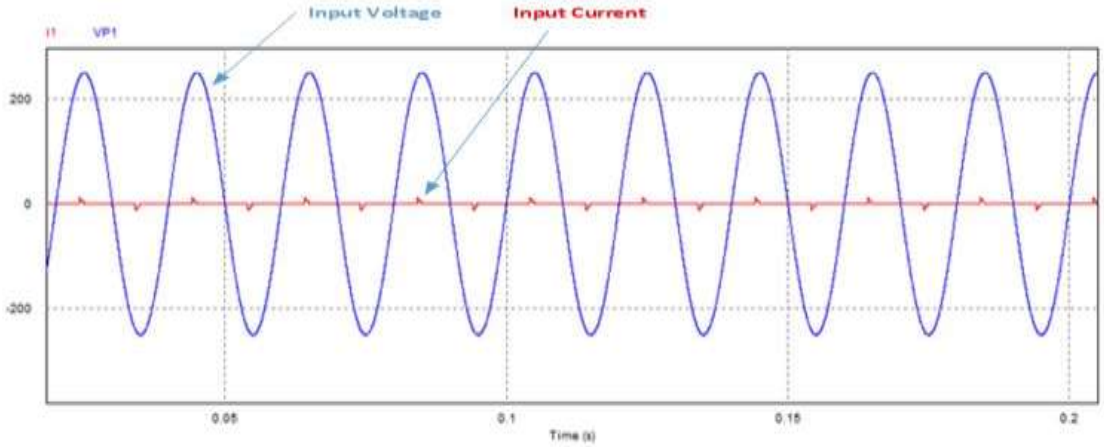


Fig. 1.2: Input current and voltage waveform of AC-DC converter without PFC

The Fig.1.2 illustrates in phase current and voltage irrespective of severe distortion present in input side current. Fig. 1.3 shows the stimulated schematic and result. The input power factor of circuit is 0.4.



(a)



(b)

Fig,1.3:Simulation of bridge rectifier without PFC (a) Schematic (b) Input line voltage and Input line current with Vin=220V, R=500Ω and Cf=470μF

If the above definition of power factor is applied it would result in unity power factor so the above definition cannot be used everywhere. The definition of power factor is modified incase of non linear loads is termed as

$$pf = \frac{Vrms1}{Vrms}\frac{I_{rms1}}{I_{rms}}\cos\theta \quad (1.2)$$

$$=\frac{I_{rms1}}{I_{rms}}\cos\theta$$

$$=Kp * \cos\theta$$

Where $Vrms1$:Fundamental component of voltage

I_{rms1}: Fundamental component of current

$\cos\theta$: Displacement factor

θ =Phase angle between voltage and current

$\boldsymbol{Kp} = \frac{I_{rms1}}{I_{rms}} = \frac{I_{rms1}}{\sqrt{I^2rms1+I^2rms2+I^2rms3+\cdots..+I^2nrms}}$ is the purity or distortion factor defined as the harmonic content of the current with respect to fundamental component of current.

Total harmonic distortion THD is defined as

$$\textbf{THD (\%)} = \frac{\sqrt{I^2rms1+I^2rms2+I^2rms3+\cdots..+I^2nrms}}{I^2rms1} \quad (1.3)$$

Hence

$$\boldsymbol{Kp} = \sqrt{\frac{1}{1+(THD\ \%)^2}} \quad (1.4)$$

Thus, power factor and harmonic reduction are inter-related. The low harmonic content results in high power factor. For e.g. in AC-DC converter the displacement factor is usually unity. Thus power factor correction is usually the reduction of harmonic content [2].

1.2 HARMONIC STANDARDS

The harmonics present in the ac line current has to be removed to meet the international standards. The work of standardization starts in early 1982.The standard IEC 555-2 was published by International Electro technical committee (IEC) which was later adopted by 1987 as the European standard EN 60555-2 by European Committee for Electro technical Standardization (CENELEC).IEC 555-2 standard was later replaced in 1995 by the IEC 1000-3-2 standard and subsequently adopted by CENELEC as the European standard EN 61000-3-2. The standard is applied to equipment with 16A RMS per phase and which is connected to the 50Hz, single-phase or 400V three-phase mains network [2-3].

Equipments can be grouped into one of 4 classes based on the following:

- Number of equipment connected
- Period of usage
- Simultaneous usage
- Power consumption
- Harmonics spectrum

Based on above factors equipments are classified as listed in Table 1.1

Table 1.1: Classification of equipments

Class A	• Balanced 3-phase equipment • Household appliances, excluding equipment identified by Class D • Dimmers for incandescent lamps • Tools without portable tools
Class B	• Handy tools • Arc welding equipment which is not professional equipment
Class C	• Lighting equipment over 25 W including dimming devices
Class D	• Equipment having an active power of less than or equal to 600W and is either a PC or PC monitor, or a television

Harmonic limit for different classes are given in Table 1.2 to Table 1.4 [4].

Table 1.2: Limits for Cass A & Class B equipment

Harmonic order (n)	Class A Max permissible harmonic current	Class B max permissible harmonic current
Odd harmonics		
3	2.3	3.45
5	1.14	1.71
7	0.77	1.155
9	0.40	0.60
11	0.33	0.495
13	0.21	0.315
$15 \leq n \leq 39$	2.25/n	3.375/n
Even Harmonics		
2	1.08	1.62
4	0.43	0.645
6	0.30	0.45
8 <= n <= 40	1.84/n	2.76/n

Table 1.3: Harmonic limits for Class C equipment

Harmonic order (n)	Maximum value expressed as a percentage of the fundamental input current of luminaries
3	30*λ
5	10
7	7
9	5
11< n <39 3	3

*****Where λ is power factor circuit

Table 1.4: Harmonic limits for Class D equipment

Harmonic order (n)	Maximum permissible harmonic current per watt mA/W	Maximum permissible harmonic current (A)
3	3.4	2.30
5	1.9	1.14
7	1	0.77
9	0.5	0.40
11	0.35/n	0.33

1.3 POWER FACTOR CORRECTION (PFC) STRATEGIES

The reason for low power factor and high circulating currents generated by switch mode power supply is the discontinuous valued input filter charging current. The problem can be solved by increasing the conduction angle of rectifier circuit. There are two types of power factor correction, Passive and active power factor correction ..

1.1.1 PASSIVE POWER FACTOR CORRECTION

In passive power factor correction, capacitor and inductors are used. These are positioned at different location to improve the power factor. Simplest one is usage of inductor at the input side of bridge rectifier as shown in Fig. 1.3 .The input power factor is 0.73 as simulated in PSIM 9.0.

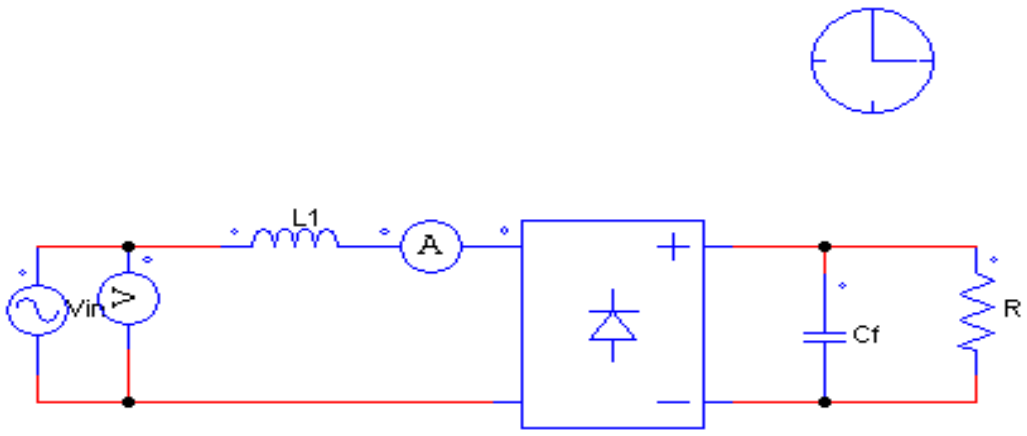
ADVANTAGES

- Simplicity
- Reliability
- Efficient

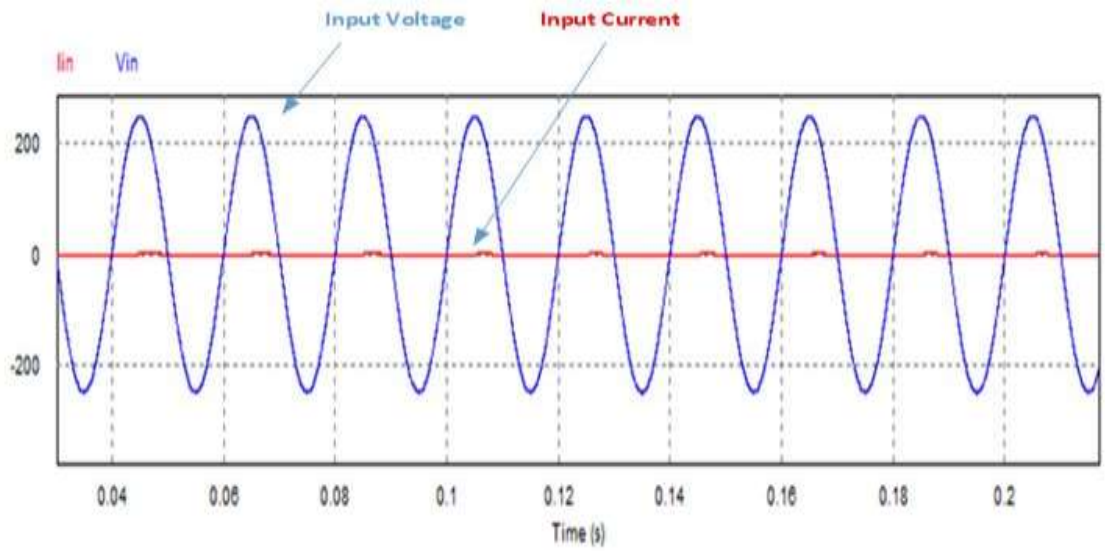
DISADVANTAGES

- Bulky size of filters
- Insufficient dynamic response
- Shape of Input Current depends on the type of load
- Lack of voltage regulation limits the use of passive power factor correction below 200W

SIMULATION RESULTS:-



(a)



(b)

Fig. 1.4: Simulation of bridge rectifier with input inductor filter (a) Schematic (b) Input line voltage and Input line current with Vin=220V; L1=130mh,resistive load R=500Ω and Cf=470µF

1.3.2 ACTIVE POWER FACTOR CORRECTION

Active power factor correction includes the shaping of input current using MOSFET and IGBT. Here the PFC stage is realised by using a bridge rectifier and DC-DC converter. To shape the input current any DC-DC converter can be used [5].

ADVANTAGES

- Low harmonic content in the input current
- Attains power factor greater then 0.95
- Small in size
- More flexible
- Greater control
- For higher power level the active PFC results smaller in size, ease of control and cost benefits

1.3.2.1 BUCK CONVERTER BASED ACTIVE PFC

The buck converter is shown in Fig 1.4. The converter operates only when instantaneous input voltage is more than the output voltage and operates in discontinuous conduction mode [6].

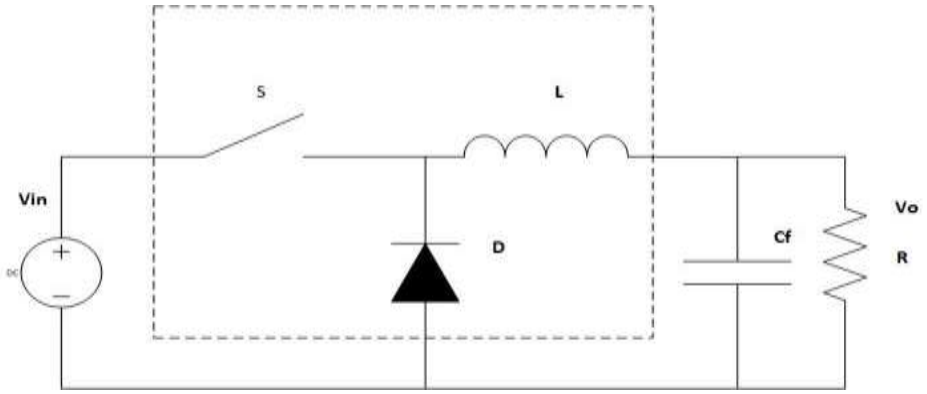


Fig 1.5: Basic Buck Converter

BUCK CONVERTER

ADVANTAGES

- There is robustness and reliability due to lower downstream voltage
- Due to low voltage at the output of PFC converter there is low CM noise
- Owing to the low voltage at downstream stage allows usage of lower voltage MOSFETs
- In buck PFC there is no need to limit the starting inrush current as it has inherent inrush limitation at start-up
- Good THD and PF due to ease of control flexibility
- In buck PFC has inherent inrush limitation at start-up
- The low output voltage of the PFC provides added advantages of usage of low cost, low voltage switches

LIMITATIONS

- The THD and PF performance are limited due to the ac line cross over current distortion
- The usage of high side drive for the buck PFC switch
- The surge management is complicated due to no direct path from AC input to output bulk storage capacitor
- Less efficient bulk capacitor for energy storage due to low output voltage
- Less holdup time

- The percentage bus ripple voltage in the buck type is more than boost PFC

1.3.1.1 BOOST CONVERTER BASED ACTIVE PFC

Boost converter is shown in Fig. 1.5.It is the most common topology used for power factor correction circuits. Here the output voltage is more than the input voltage. It operates in the continuous conduction mode (CCM) and Discontinuous conduction mode (DCM).

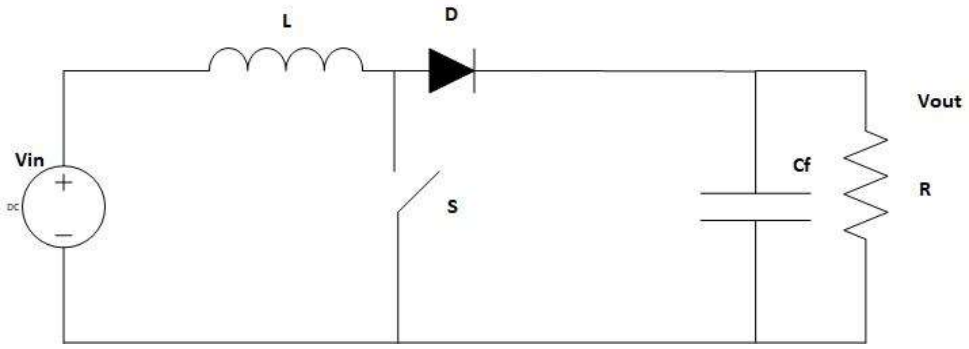


Fig 1.6: Basic Boost converter topology

The boost converter has inbuilt PFC property. The control technique used is simple PI controller. The controller output is compared with a high frequency triangular signal to generate PWM pulse as shown in Fig. 1.6 and 1.7.

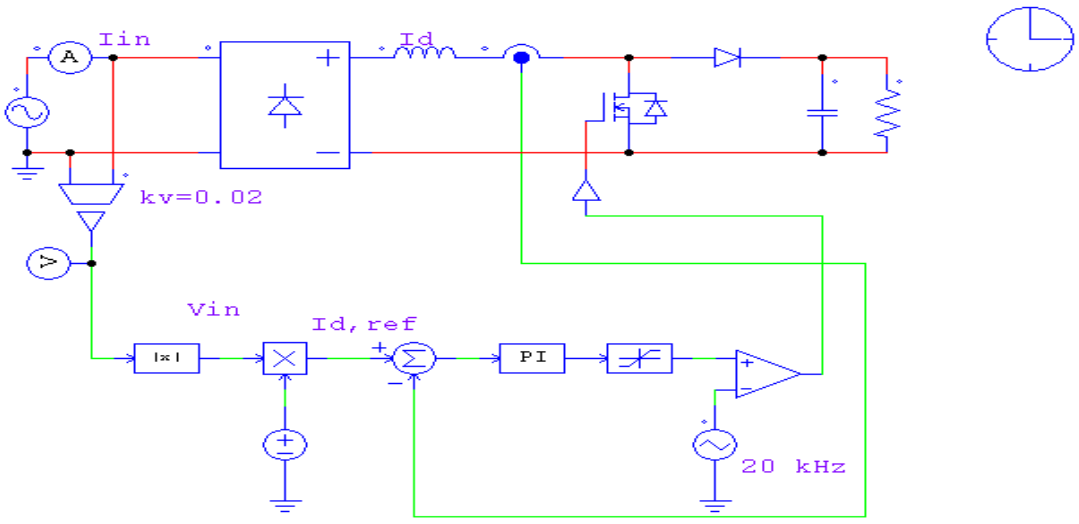


Fig 1.7: Boost PFC circuit- Schematic

SIMULATION RESULTS:-

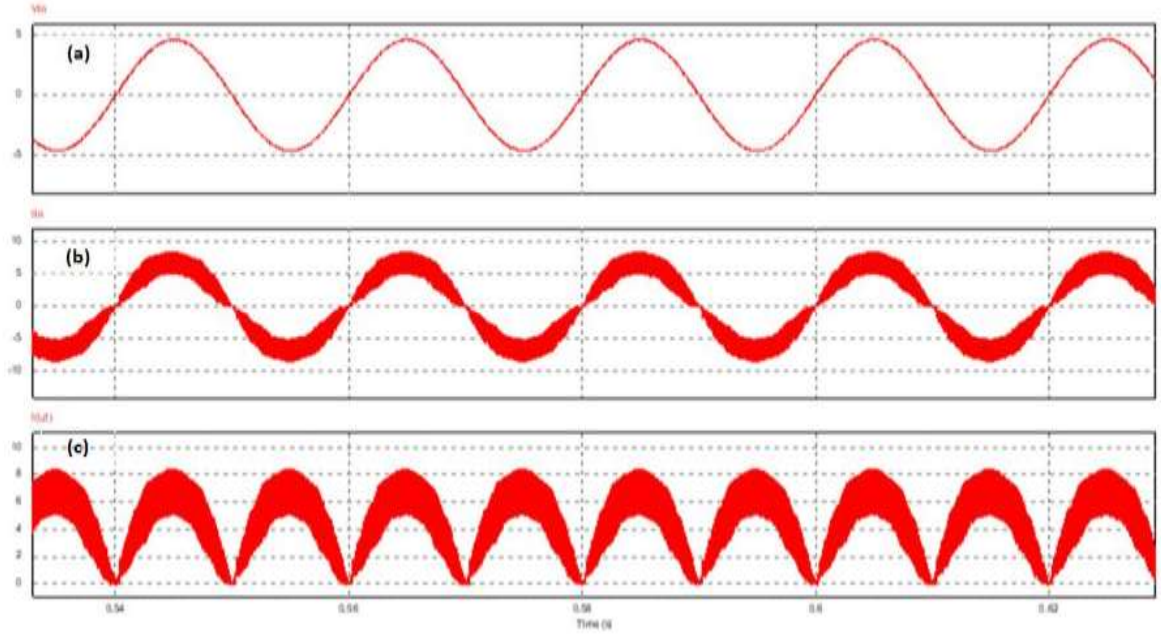


Fig. 1.8: Simulated output of PFC boost converter (a) Input voltage (b) Input current (c) Inductor current

ADVANTAGES

- Low THD and best possible Power factor
- Due to high output voltage the size of storage capacitor is efficient
- Comparatively more holdup time
- The boost switch is easy to drive and current sensing is simple
- Due to direct path between input to output capacitor provides excellent surge management
- For boost PFC there are large number of control IC and design data

LIMITATIONS

- Output voltage should always be greater than the peak input instantaneous voltage
- Require isolation stage to step down the voltage
- Due to high bus voltage the common mode noise(a noise created by stray capacitance)is more

- No inrush current limitation at the startup
- The efficiency of the converter is low owing large conduction losses at low

CHAPTER-2
LITERATURE SURVEY

2.1 POWER FACTOR CORRECTION

[1] The power factor correction converter is required to meet international standards such as IEC 61000-3-2 and IEEE-519. The PFC circuit maximizes the actual power absorbed by the AC power grid.

[2] The duration of the current pulse taken from the AC grid is only 10% - 20%, but the amplitude of the current is 5 to 10 times the average current.

2.2 HARMONIC STANDARD

In paper [3-4],the harmonic present in the AC line current must be removed to meet international standards,such as IEC 6100-3-2.The standard applies to equipment with 16A RMS per phase connected to the 50 Hz three-phase network,single-phase or 400V.The equipment is classified into four groups,Class A,Class B,Class C and Class D.

2.3 POWER FACTOR CORRECTION STRATEGIES

In paper [5], peak current and average current control are used to model the current of the input power grid. The peak current is unstable for the duty cycle above 50%. In the peak current control, the inductor operates in continuous conduction mode (CCM). The control of the average current mode is unconditionally stable for duty cycles exceeding 50%

Paper [6] presents the advantages and limitations of the boost and buck converter.

2.5 FIXED OFF TIME

The paper [7] proposes a small signal model for controlling the current mode of PWM converters (pulse width modulation) with constant on time, constant off-time control of and discontinuous conduction mode. Peak current mode control when used with the Fixed On Time or Fixed Off time becomes unconditionally stable.

Paper [8] used the Fix Off Time concept to couple the simplicity and affordability of the Transition (TM) mode with high current capacity of the Fixed-Frequency continuous Mode

resulting in peak current mode control with fixed OFF time (FOT control).. Switch-off time (FOT control). In the proposed technique, the switch-on time is modulated maintaining the switch-off time constant, which results in a large change in switching frequency

In the paper [9], the FOT technique is further modified. The change associated with the switching frequency is eliminated by modulating the switch-off time proportional to the voltage of the input line, which results in a constant switching frequency, unless the converter works in CCM mode.

The paper [10] proposes an adaptive on- time control system for DC-DC converters. The proposed technique can achieve rapid transient response without any change in switching frequency. The author has made the switching frequency fs ($f_s = \frac{1}{R_{ac_a}}$), regardless of the input voltage Vin and the output voltage Vout can be easily evaluated by the passive components Ra and Ca.

In paper [11], the author used bridgeless PFC based on the Fixed Off Time with zero voltage switching, which leads to the reduction of conduction loss. A yield increase of 2.7% is reported.

The paper [12] presents a monolithic fixed frequency DC-DC boost converter with a modified adaptive off time control (MAOF). A constant switch-off time T_{OFF} is generated by the boost converter to obtain the fixed switching frequency available in CCM and DCM operations.

The paper[14] provides quantitative analysis and provides proposed predicting correction technique (PCT) to modulate an adaptive on time for constant f_{sw} under possible different conditions, including V_{IN} , V_{OUT}, and wide-range I_{load},.Complete parasitic resistances of each component are taken into consideration without any assumption or simplification.

In paper [13], the author proposes a compensation circuit for the adaptive on-time control buck regulator to weaken the impact caused by the variation of the load current. The change in switching frequency with the proposed compensation technique is reduced to only 3.75% of fs.

The paper[14] provides a quantitative analysis and provides a proposed predictive correction technique (PCT) to modulate an adaptation time for the constant f_{sw} in different possible conditions, including V_{IN} , V_{OUT}, and wide-range I_{load},.. The complete parasitic resistances of each component are taken into consideration without any assumption or simplification.

[15] presents a quasi-fixed time controlled frequency converter (COT) reinforcement converter. The author presents a new approach to designing a hysteretic pulse converter. The switch-on time of the boost switch is predetermined by a switch-on time generator corresponding to the fixed frequency operation requirement and the switch switch on time is modulated in the traditional hysterical mode.

[16] proposes a new adaptive pulse width modulator (PWM) for AC / DC or DC / DC regulators, based on “Fixed-Off Time (FOT)” or “Constant-On-Time (COT)” control, which allows operating with an almost fixed switching frequency in all operating conditions.

2.2 REASERCH GAP

The concept of FOT (FIXED OFF TIME) is new and lot of work can be done on it. The application of FOT as proposed in [9] in the field of bridgeless PFC, Interleaved PFC and more over in the use of FOT has not yet been fully explored with the FlyBack converter. The use of zero-voltage switching is still unexplored to reduce losses and increase efficiency.

CHAPTER-3

PFC CONTROL STRATEGIES

CHAPTER OVERVIEW

The chapter deals with PFC control strategies, which include peak current control and average current control in the boost converter. Benefits and limits are exposed. Simulation results are also provided. The concept of Fixed Off Time is explained and its advantages and disadvantages are given

3.1 PFC CONTROL STRATEGIES

The power factor correction is used to shape the input current. There are different control strategies to get the power factor correction. The techniques described below for the boost converter and can also be used for other converters.

3.1.1 PEAK CURRENT CONTROL WITH CCM MODE

The peak current control strategy for the boost converter is shown in Fig. 3.1; represents the waveform of the input current that is shaped to obtain the power factor correction. In the peak current control strategy, the switch is turned on and off at a constant frequency. The switch is off when the sum of the positive ramp of the inductor current (switch current) reaches the sinusoidal reference. The sinusoidal reference is obtained by multiplying a rectified rectified half sinusoid Vg of the rectifier bridge output with the output of the error amplifier that determines the current reference. The current reference signal is naturally synchronized and is always proportional to the line voltage, which is the main condition for achieve the unit power factor. In peak current control, the converter operates in continuous Mode (CCM) mode. The additional advantage of the CCM mode is the low current voltage and the input filter requirement [17].

ADVANTAGES

- Constant switching frequency
- The input current is detected based on the current of the switch
- No need for error amplifier and its compensation network.
- The pulse current limit per pulse increases reliability and response speed

DISADVANTAGES

- For duty cycle greater than 50%, there are sub harmonic oscillations for which compensation circuit isrequired
- The Control is more sensitive to noise

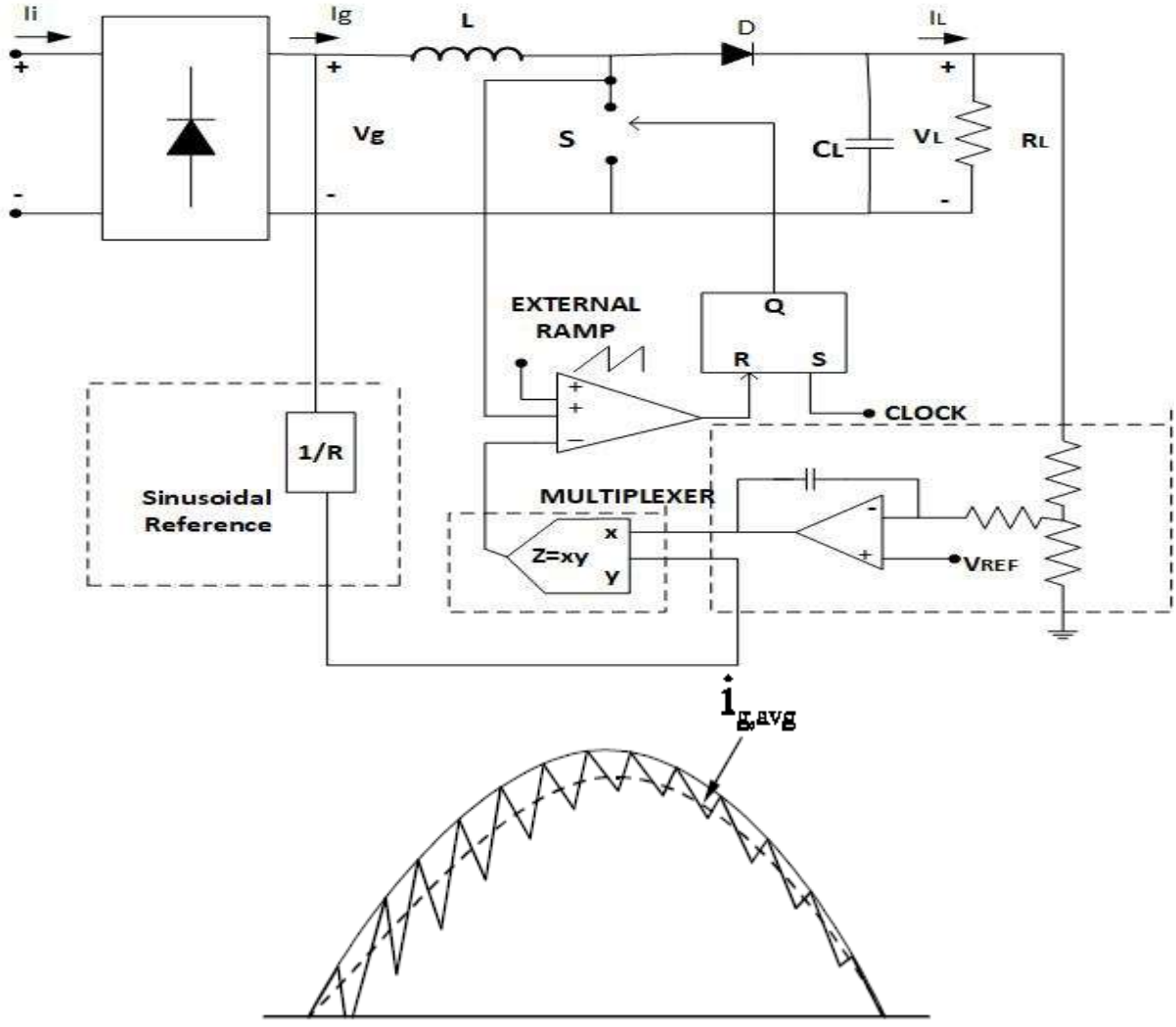


Fig. 3.1: Peak Current Control Scheme

3.1.2 AVERAGE CURRENT CONTROL

In controlling the average current, the average converter current is controlled by detecting the inductor current. The inductor current is filtered by the error amplifier whose output drives the PWM modulator. When controlling the average current, the inverter operates in continuous driving mode (CCM) [18-19].

ADVANTAGES

- Constant switching frequency
- For duty cycle greater than 50% there is no need of compensation ramp
- Control technique is less prone to communication
- The input current waveform is better than peak current control technique

DISADVANTAGES

- The inductor current must be detected
- A current error amplifier is required and its design of the compensation network must take into account the different operating points of the converter during the line cycle

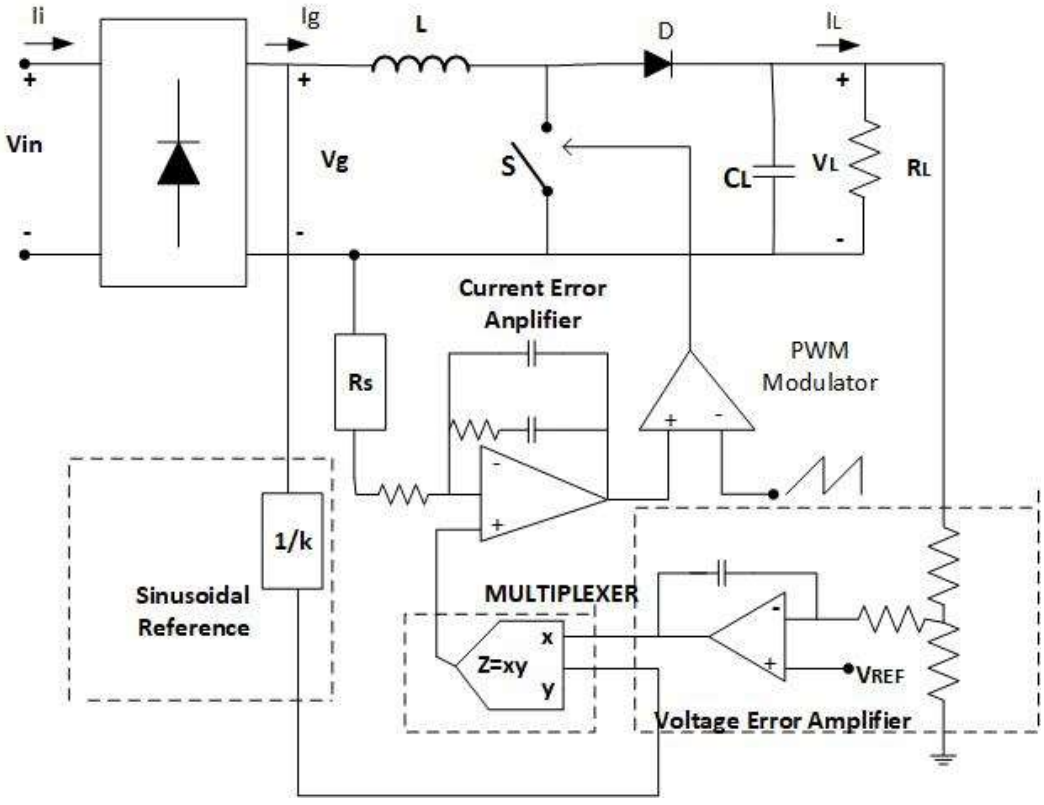


Fig.3.2: Average Current Control Scheme

3.2 FIXED OFF TIME CONCEPT

The Fixed frequency continuous conduction mode (FF-CCM) and the transition mode (TM) PWM (fixed on time, variable frequency) are the two methods used in the pre-regulators based on the boost converter. In the first mode, the inductor operates in continuous conduction mode (CCM) and uses a average current mode control, a complex technique that requires a

considerable number of components. The second mode uses more complex peak current mode and makes the inductor work between continuous and discontinuous mode, which uses fewer components, it is unstable over 50% of the duty cycle and is more economical. The transition mode (TM) involves high peak current as compared to FF-CCM as shown in Fig. 3.3 and Fig. 3.4.

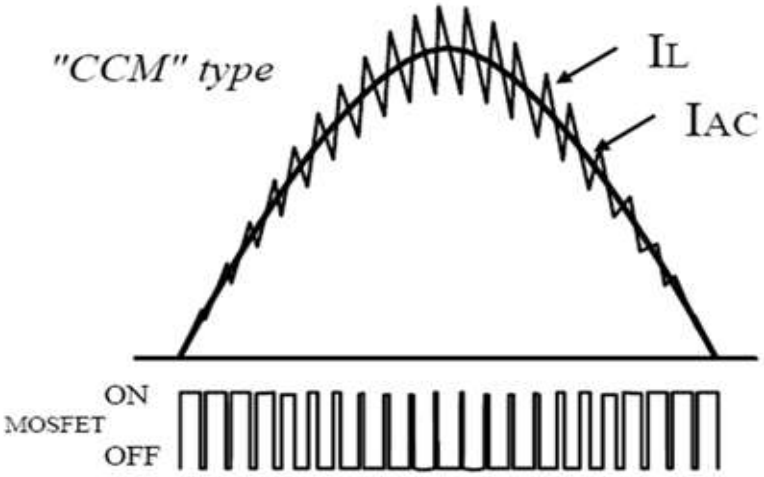


Fig. 3.3: Line and inductor current in CCM PFC

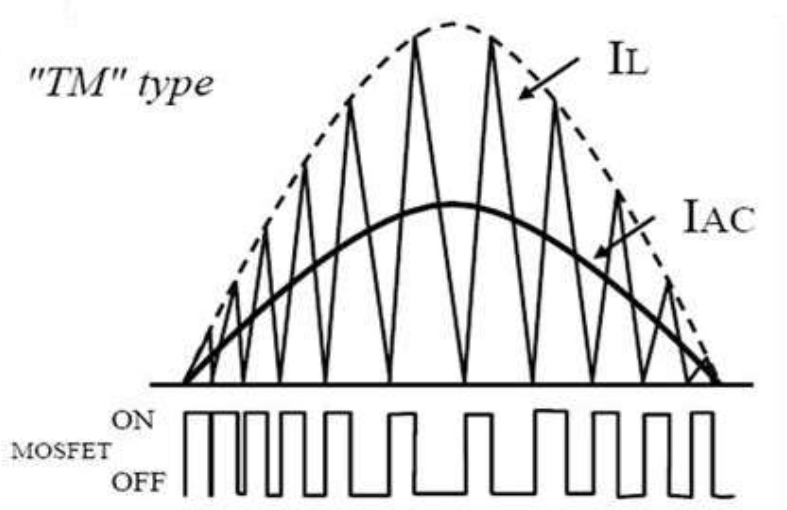


Fig. 3.4: Line and inductor current in TM PFC

A third mode of operation in the pre-regulator based on boost converter is get popularity which is Fixed Off Time (FOT). Transition mode is suitable for low power application while FF-CCM is suitable for high power application. The FOT is conditionally stable for duty cycle

greater than 50% and needs no compensation. The fixed frequency modulates the on and off times (its sum is constant by definition) and the given converter operates in CCM or DCM. The same result can be achieved with the FOT approach. A FOT incorporates the conventional peak current control, in which the switch-on time T_{ON} of the switch is determined by the peak inductor that reaches the programmed value and T_{OFF} is determined by a special fixed-time modulator in such a way resulting in constant switching frequency.

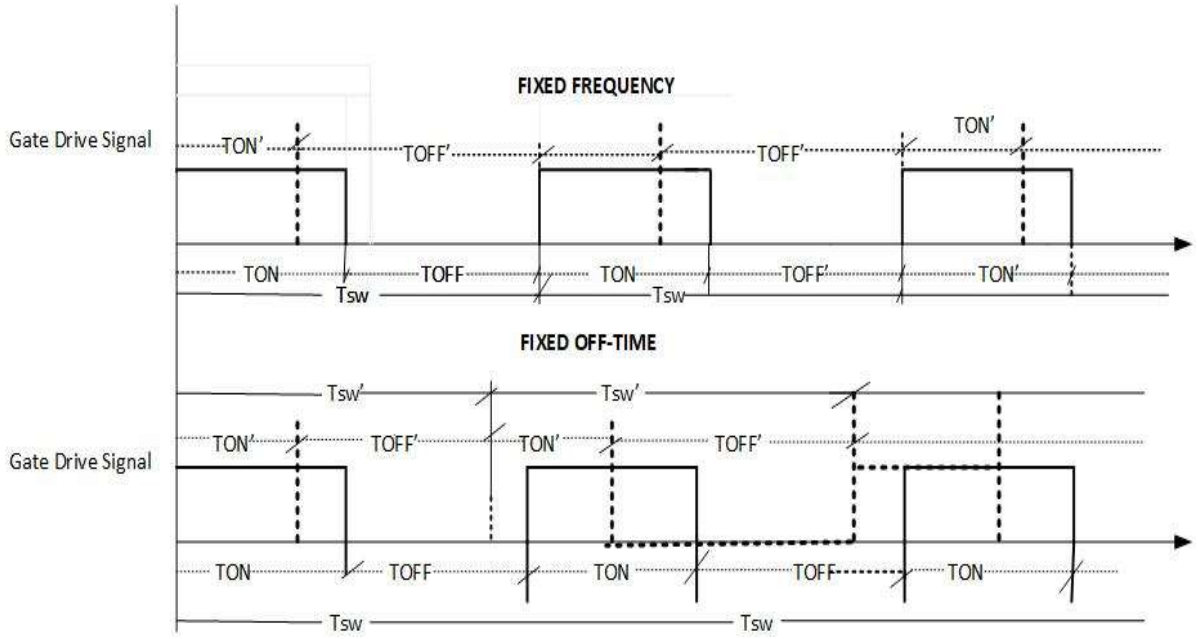


Fig.3.5: FF-PWM vs. FOT-PWM: Basic waveforms

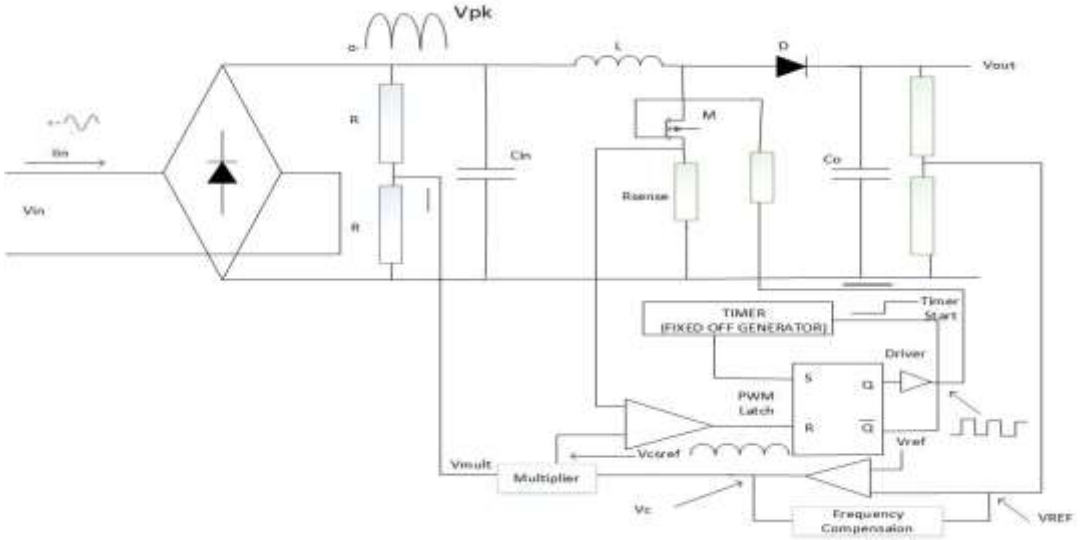


Fig.3.6: Block diagram of an FOT-controlled PFC preregulator

In FOT variable frequency is inherent, so to obtain fixed frequency system the OFF time of switch is modulated to obtain constant frequency system which is illustrated below mathematically [9]

Volt second balance equation for the boost inductor under the assumption of CCM operation

$$T_{ON}Vpk\ \sin\theta = T_{OFF}(Vout\ - Vpk\ \sin\theta) \quad (2.1)$$

Where Vpk is the peak line voltage, $Vout$ the regulated output voltage and θ the instantaneous phase angle of the line voltage. Solving for T_{ON} we get

$$T_{ON} = \left\{\frac{V_{out}}{V_{pk}Sin\theta} - 1\right\}T_{OFF} \quad (2.2)$$

Then, the switching period $Tsw = T_{ON} + T_{OFF}$ will be

$$T_{sw} = \left\{\frac{V_{out}}{V_{pk}Sin\theta} - 1\right\}T_{OFF} + T_{OFF} \quad (2.3)$$

$$= \frac{V_{out}}{V_{pk}Sin\theta}T_{OFF}$$

In the end, if *TOFF* is changed proportionally to the instantaneous line voltage, i.e. if

$$T_{OFF} = KtVpksin\theta \quad (2.4)$$

Then

$$T_{sw} = KtV_{out} \quad (2.5)$$

$$\boldsymbol{f_{sw}} = \frac{1}{\mathrm{K_t V_{out}}} \quad (2.6)$$

and, since $Vout$ is regulated by the voltage loop, also Tsw (and $fsw = 1/Tsw$) will be fixed.

ADVANTAGES

- Simple control, low part count
- Constant switching frequency
- Dynamic behavior improvement
- Reduced EMI emissions
- Mosfet losses are less

DISADVANTAGES

- Line current distortion is not negligible

CHAPTER-4
CIRCUIT DESIGN

CHAPTER OVERVIEW

This chapter focuses mainly on the design of different circuits. In the first part, design of PFC is presented where IC L4984D is used .In the last part of the chapter the design of the Flyback converter and the RCD Snubber circuit is presented..

4.1 AC-DC CONVERTER

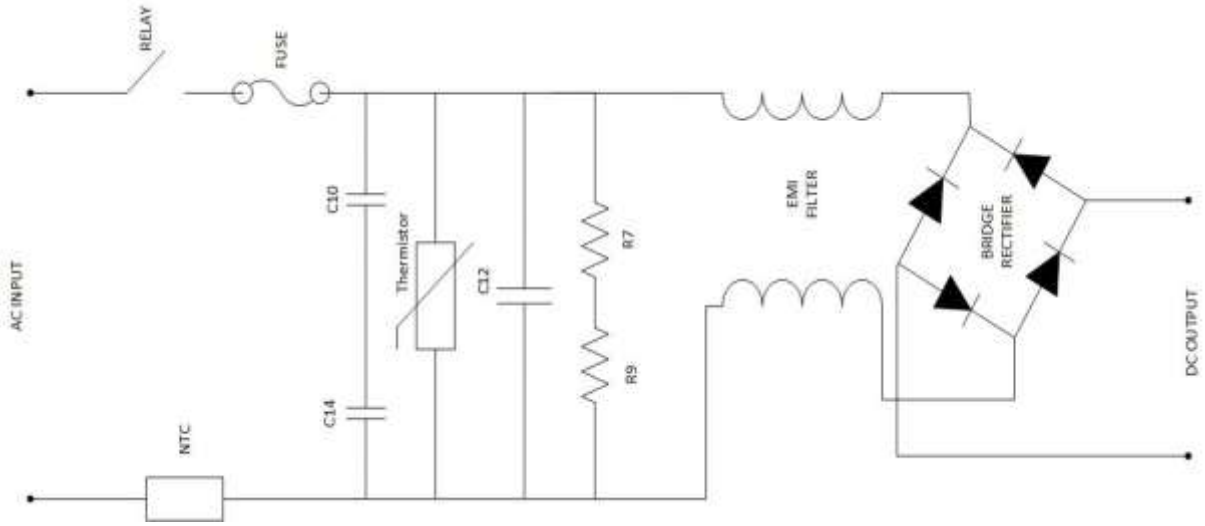


Fig. 4.1: AC-DC Converter

Following are the various components used at the input side of bridge rectifier.

- Relay
- NTC
- Varistor
- EMI Filter
- Capacitor and Resistor
- Fuse

I. RELAY

It is an electrical switch to control the circuit with a separate low-power signal with the help of the microcontroller. A DC signal is used to control the circuit with the DC signal of the microcontroller.

4.2 Relay

Relay switch Circuit

A relay coil is driven by the NPN transistor switch. When base voltage of transistor is zero then NPN transistor is in cut-off region and relay is de-energised. Similarly, if the base voltage is present the relay coil is energised, a relay is tripped. The relay switch circuit is shown in Fig. 4.3. A diode across the relay circuit is used for protection during the voltage collapse across the inductor coil.

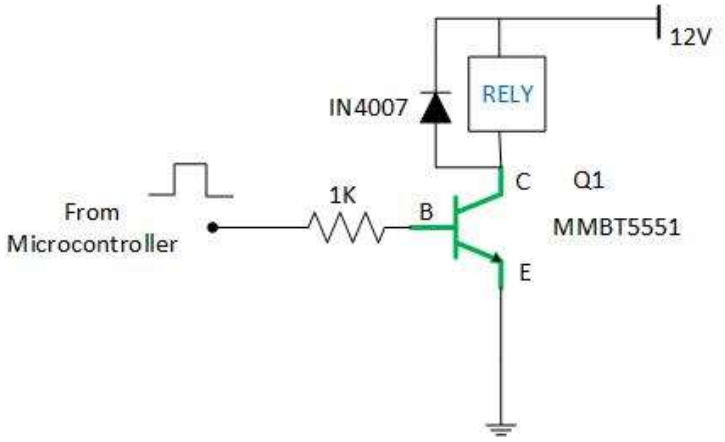


Fig. 4.3 Relay Switch Circuit

II. NTC

NTC or Thermisitor is a variable resistive element which changes its resistance when exposed to change in temperature. They are used in series with the component or device to limit the current. NTC limits the initial high staring current due to its negative temperature coefficient.

Fig. 4.4: NTC/Thermisitor

III. VARISTOR

Varistor offer overvoltage protection by means of voltage clamping just like Zener diode. It is resistance depend on applied voltage.

Fig. 4.5:Varistor

IV. EMI Filter

The EMI filter is used to suppress high frequency electronic noise that causes interference with other devices. The EMI power supply filter consists of passive components, including inductor and capacitor connected in the form of an LC network.

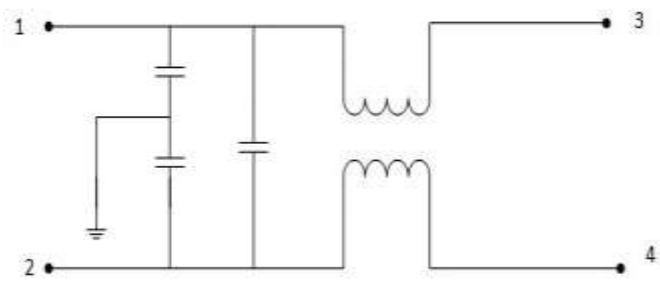


Fig 4.6 :EMI Filter

4.2 DESIGN OF PFC CIRCUIT

The Power factor correction circuit employs the L4984D IC which incorporates the use of Fixed off Time (FOT) [20-21].

There are important feature and benefits with L4984D which are given in Table 4.1

Table 4.1: Features and Benefits

FEATURE	**BENIFIETS**
Fixed frequency operation	Simple design and reduced BOM
Fast bidirectional input voltage feed forward($1/V^2$)	Mains drops and surge protection
Soft start	Inrush energy management
THD optimizer circuit	Improved performance
Protections embedded: 1. Feedback loop Failure 2. Overvoltage protection 3. Inductor saturation 4. Ac brown out	Avoid dc link capacitor burning and downstream converter damage More design reliability Avoid Mosfet damage Avoid bridge and inductor damage

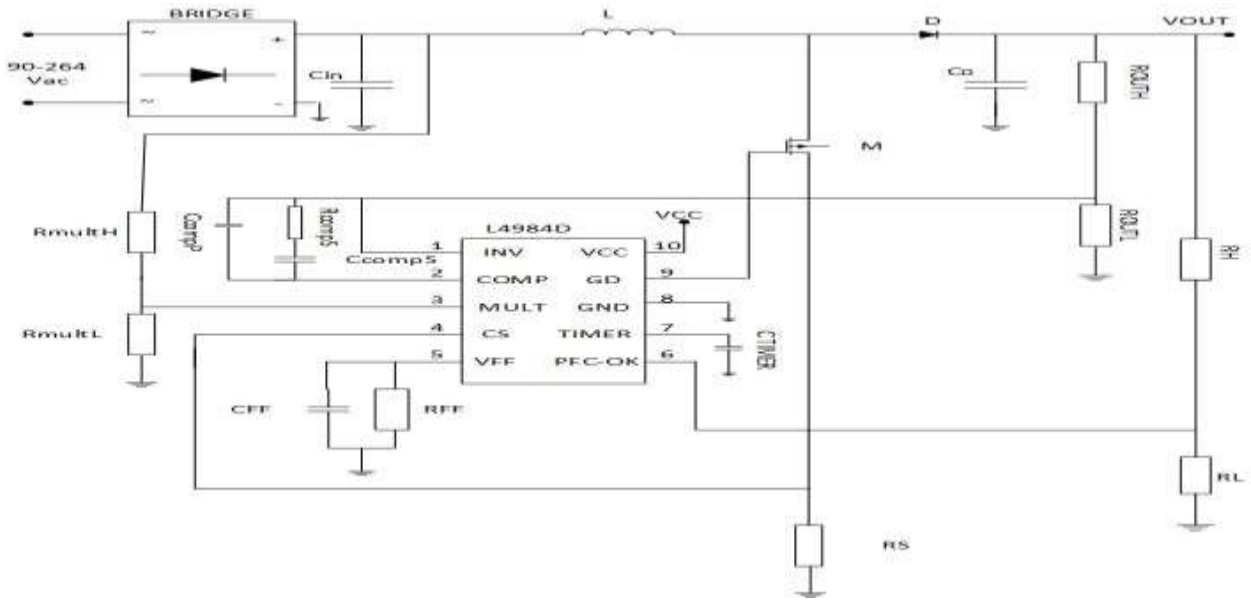


Fig. 4.7 PFC regulator based on L4984D IC

Table 4.2: Input specifications of PFC circuit

PARAMETER	VALUE
Mains Input Voltage	V(ac min)=100V :V(ac max)=300V
Minimum Mains Frequency	47-52 Hz
Rated Output Power (W)	140W
Regulated Dc Output Voltage (Vdc)	450V
Expected Efficiency (%)	92%
Expected Power Factor	0.99
Maximum Output Voltage (Vdc)	480V
Maximum Output Low Frequency Ripple (Peak-To-Peak)	22.5V
Minimum Output Voltage After Line Drop (Vdc)	350V
Hold-Up Time (ms)	15 ms
Ripple Factor(Kr)	0.3
Maximum Ambient Temperature (℃)	50℃
Switching Frequency(fsw)	50 kHz

1. INPUT PARAMETERS

This part provides detailed specifications of the circuit operating conditions required in the following sections. The input parameters are shown in Table 4.2.

I. **Mains Voltage Range (Vac_{rms}):**

Vac_{min} =100 V Vac_{max} =300 V (4.1)

II. **Minimum Mains Frequency:**

F_{line}=47Hz (4.2)

III **Rated Output Power(P_0):**

Po=140w (4.3)

IV. **Regulated Dc Output Voltage (V_{dc}) :(** higher than the maximum rectified input voltage)

$$V_{dc} = \sqrt{2} * Vac_{max} \quad (4.4)$$

$V_{dc} = \sqrt{2} * Vac_{max}$
$= \sqrt{2} * 300$
$= 425V$

***Set Value is 450V**

V. **Expected efficiency (%):**

$\eta = \frac{Po}{Pin}$=92% (4.5)

VI. **Expected Power Factor**(PF)**:**

PF=0.9 (4.6)

VII. **Maximum Output Voltage (V_{dc}):**

(4.7)

Maximum output voltage **(V_{dc}) or V_{OVP}=480 V**

VIII. **Maximum output low frequency ripple (peak-to-peak):**

The ripple in the output voltage is generally selected 2-8% .The ratio of 5% is chosen for the output voltage ripple i.e. 22.25V

$$\boldsymbol{\Delta Vout = 22.5V} \tag{4.8}$$

IX. Minimum output voltage after line drop (Vdc):

$$\boldsymbol{V_{out\ min} = 350\ V} \tag{4.9}$$

X. Hold-up time (ms):

$$\boldsymbol{tmin = 15ms} \tag{4.10}$$

XI. Ripple Factor:

$$\boldsymbol{Kr}\text{=0.30} \tag{4.11}$$

XII. Maximum ambient temperature (℃):

$$\boldsymbol{Tamb = 50}℃ \tag{4.12}$$

XIII. Switching Frequency

$$\boldsymbol{fsw = 50\ kHz} \tag{4.13}$$

2. OPERATING CONDITIONS

The first step is to define the main parameters of the circuit, using the specifications given in PART A:

XIV. RATED DC OUTPUT CURRENT:

$$\text{Iout} = \frac{Pout}{Vout} \tag{4.14}$$

$$= \frac{140}{450}$$

=0.32A

XV. MAXIMUM INPUT POWER:

$$\text{Pin} = \frac{Po}{\eta} = \frac{140}{.92} \textbf{=152.17w} \quad (4.15)$$

XVI. MAXIMUM RMS INPUT CURRENT:

$$Iin = \frac{Pin}{VACmin * PF} \quad (4.16)$$

$$Iin = \frac{152.17}{100 * 0.99}$$

=1.53A

XVII. In particular $kmin$ and $kmax$ refer to the ratio of the minimum and the maximum input voltage to the output voltage, respectively.

$$kmin = \frac{\sqrt{2} * Vacmin}{Vout} Iin \quad (4.17)$$

$$= \frac{152.17}{100 * 0.99}$$

=1.53A

$$kmax = \frac{\sqrt{2} * Vacmax}{Vout} \quad (4.18)$$

$$= \frac{\sqrt{2} * 300}{450}$$

= 0.93A

XVIII. MAXIMUM LINE PEAK CURRENT:

$$Ipkmax = \frac{2 * Pin}{Kmin * Vout} \quad (4.19)$$

$$= \frac{2 * 152.17}{0.32 * 450}$$

=2.14 A

XIX. MAXIMUM INDUCTOR PEAK CURRENT:

$$ILpkmax = \frac{\sqrt{2} * Pin}{VACmin * PF}\left(1 + \frac{Kr}{2}\right) \quad (4.20)$$

$$= \frac{\sqrt{2} * 152.17}{100 * 0.99}\left(1 + \frac{0.3}{2}\right)$$

=2.50

XX. INDUCTOR PEAK-TO-PEAK RIPPLE CURRENT:

$$\Delta\, ILpkmax = ILpkmax * Kr \quad (4.21)$$

=2.50*0.30

=**0.75**

3. POWER SECTION DESIGN

XXI. INPUT CAPACITOR

The Cin capacitor is placed at the output of bridge rectifier to smooth the high frequency ripple and must sustain maximum instantaneous input voltage.

$$Cin = 2.5 * 10^{-3}\mu F * Pout \quad (4.22)$$

$$=2.5 * 10^{-3}\mu F * 140$$

$$= \mathbf{350\ nF}$$

*** Chosen 330nF/630V**

XXII. OUTPUT CAPACITOR

The value of output capacitor (Co) depends on the regulated DC output voltage, output power, the RMS current, output ripple and hold-up time

$$\mathrm{Co} = \frac{2 * Pout * thold}{\left(Vout - \frac{\Delta Vout}{2}\right)^2 - V^2{}_{out\ min}} \quad (4.23)$$

$$= \mathbf{60\mu f}$$

*In our circuit we have chosen two **68µf/450V** capacitor

XXIII. BOOST INDUCTOR

$$\boldsymbol{L(Vacmin) = \frac{Vout-\sqrt{2}*Vacmin)}{\Delta\, ILpk(Vacmin)} Toff(Vacmin)} \quad (4.24)$$

- To find the value of L, first **TOFF** needs to be calculated.

According to the datasheet of the L4984D, the linear operating range is between 0 to 3 V, so the maximum value of the multiplier input ($VMULTmax$) is equal to 3 V.

$$kp = \frac{Vmultmax}{\sqrt{2}*\text{Vacmax}} \quad (4.25)$$

$$= \frac{3}{\sqrt{2} * 300}$$

$$=\mathbf{7.08*10^{-3}}$$

The switching frequencies determine a capacitor connected between the TIMER pin and the ground, which gives a precise internal generator **(ITIMER) of 156 µA** (typical), during the switch-off time, generating a voltage ramp.

$$Ct = \frac{\text{ITIMER}}{Kp*Vout*\text{Fsw}} \quad (4.26)$$

$$= \frac{156\mu\text{A}}{7.08 * 10^{-3} * 450 * 50khz}$$

$$\mathbf{=1\mu F}$$

The maximum OFF-time at $Vacmin$ is then:

$$Toff(Vacmin) = \frac{Ct*Kp\sqrt{2}*100}{ITIMER} \quad (4.27)$$

$$\frac{1uf*7.08*10^{-3}*\sqrt{2}*100}{156\mu\text{A}} =$$

$$=\mathbf{6.42\mu s}$$

The value of the inductance L required for the boost inductor at $VACmin$ can now be

$$\boldsymbol{L(Vacmin)} = \frac{\boldsymbol{Vout}-\sqrt{2}*\boldsymbol{Vacmin})}{\boldsymbol{\Delta\, ILpk(Vacmin)}} * \boldsymbol{Toff(Vacmin)} \quad (4.28)$$

$$= \frac{450-\sqrt{2}*100}{0.75} * 6.42\mu\mathbf{s}$$

$$\mathbf{=2700\mu H}$$

*In our design we have used 3200 µH

3. L4984D BIASING CIRCUIT

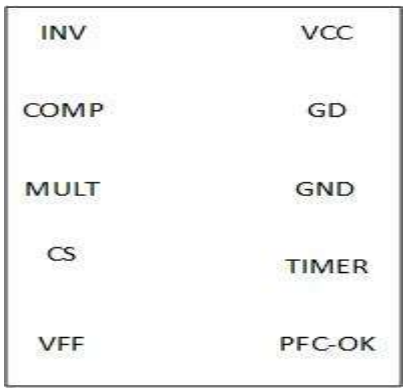


Fig 4.8: Pin Diagram of L4984D

The following sections describe the selection of the circuitry around the L4984D.

- **Feedback and Over Voltage Protection**

Pin 1(INV):

A resistive divider circuit is connected between this pin and the regulated boost voltage. RoutH and RoutL will be selected considering the desired nominal output voltage and the desired output power dissipated in the output divider.

For 25mW output divider dissipation:

$$R_{outH} = \frac{(V_{out} - 2.5V)^2}{25mW} \quad (4.29)$$

$= 8.2\ M\Omega$

Here three 2.7MΩ resistors in series have been selected.

$$\frac{R_{outH}}{R_{outL}} = \frac{V_{out}}{2.5V} - 1 = 179 \quad (4.30)$$

$$R_{outL} = \frac{V_{out}}{179}$$

$= \frac{9M\Omega}{179}$

$= 50.3k\Omega$

For R_{outL} a value of 130kΩ in parallel to an 82kΩ has been selected.

Pin 6 (PFC_OK - Feedback failure protection):

The PFC_OK pin has been dedicated to monitoring the output voltage of a separate resistance divider. This divider is selected so that the voltage on the pin reaches 2.5 V if the output voltage exceeds a preset value (Vovp), generally greater than the maximum Vout that can be expected, including worst-case the line / load transients For a maximum Voutmax output voltage of 480 V and select a current of 30µA flowing into the divider:

$$R_L = \frac{V_{REF\_PFC\_OK}}{I_{divider}} = \frac{2.5V}{30\mu A} = 83k\Omega \quad (4.31)$$

By selecting a commercial value of 82kΩ

$$R_H = R_L\left(\frac{V_{OUT_{MAX}}}{V_{REF_{PFC_{OK}}}} - 1\right) \quad (4.32)$$

$$= 82k\Omega\left(\frac{480V}{2.5V} - 1\right)$$

$$= 15.6\ M\Omega$$

*Chosen value is three 3.3MΩ resistor and one 82kΩ

- **Current Sense Resistor**

Pin 4(CS):-The pin 4 is the inverting input of the current sense comparator. Through this pin, the L4948D senses the instantaneous inductor current, converted in a proportional voltage by an external sensing resistor(R_S).

$$R_s = \frac{V_{sc(min.)}}{I_{LPK(max.)}} \tag{4.33}$$

$$R_s < \frac{0.84}{2.14}$$
$$= 0.39\ \text{m}\Omega$$

***Selected value of Shunt resistor is: 240 mΩ**

I. I_{Lpk} is the maximum peak current in the inductor

II. $V_{csm\ in}$ = 0.84V is the minimum value of the L4984D current sense reference clamp

$$IL_{pks} = \frac{0.93}{0.39} \tag{4.34}$$
$$= \frac{0.93}{0.39}$$
$$= 2.38\text{A}$$

The calculated IL_{pks} will be the value at which the boost inductor shall not saturate and it will be used for calculating the inductor number of turns and air gap length.

Pin 5(VFF): The L4984D uses capacitorC_{FF} and a resistor R_{FF}, to implement voltage feed-forward technique and to complete the internal peak-holding circuit that provides DC voltage equal to peak of the rectified sine wave applied on pin MULT(PIN3).

C_{FF} = 1µF and R_{FF} = 1MΩ

Pin 3(MULT):

$$R_{multL} = \frac{V_{MULT\ max}}{I_{MULT}} = \frac{3.00\text{V}}{64\mu\text{A}} = 47\text{k}\Omega \tag{4.35}$$

$$R_{multH} = \left(\frac{1 - k_p}{k_p}\right) R_{multL} \tag{4.36}$$

$= \left(\frac{1-7.08*10^{-3}}{7.08*10^{-3}}\right)47k\Omega$

$=6.6m\Omega$

4.3 RESULTS AND DISSCUSION

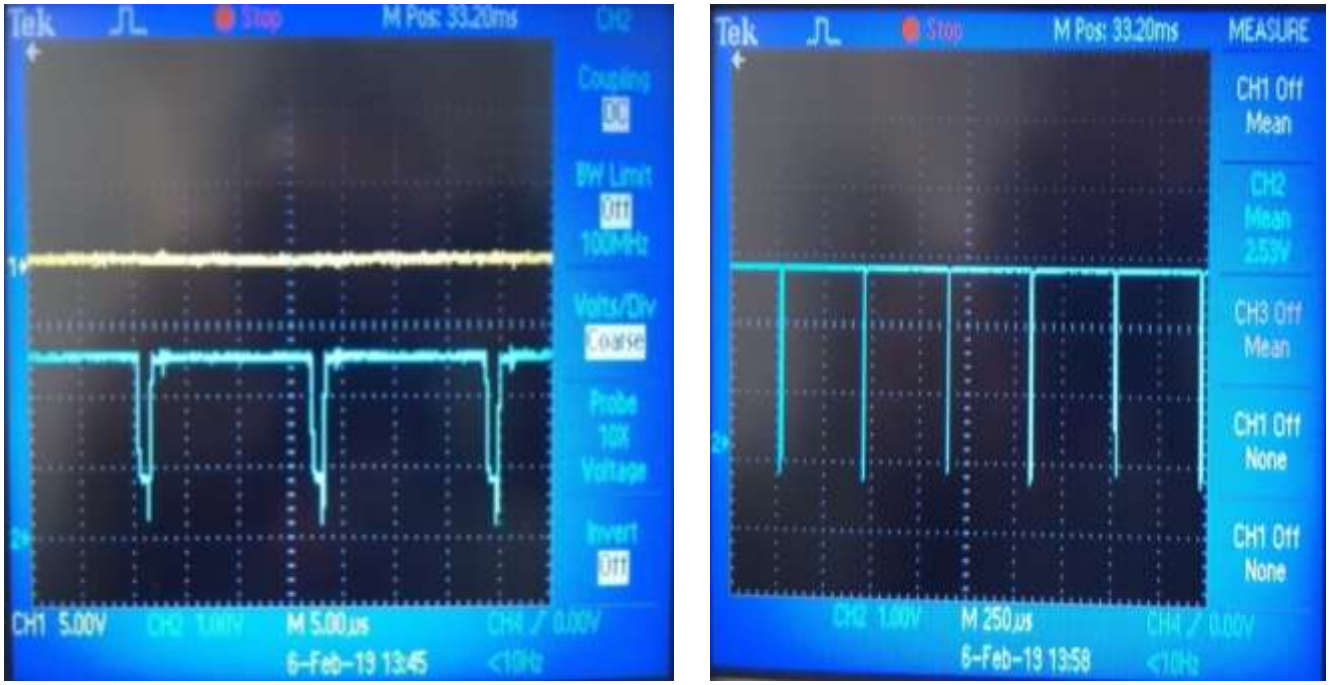
For the proper working of IC L4984D there should be proper voltage on the pins. Incase voltage sensed is out of the range, the IC l4984d gets shutdown and in some cases in burst mode. Table 4.3 summarizes all the operating conditions that can cause device malfunction.

Table 4.3: Summary of L4984D redundant states

Condition	**Caused**	**IC behavior**	**Restart Condition**
UVLO	$V_{CC}<V_{CCOFF}$	Disabled	$V_{CC}>V_{CCOFF}$
AC brownout	$V_{PFC\_OK} <V_{PFC\_OK\_D}$	Stop switching	$V_{PFC\_OK} >V_{PFC\_OK\_D}$
AC brownout	$V_{VFF}<V_{DIS}$	Stop switching	$V_{VFF}>V_{EN}$
OVP	$V_{PFC\_OK}>V_{PFC\_OK\_S}$	Stop switching	$V_{PFC\_OK}<V_{PFC\_OK\_S}$
Feedback failure	$V_{PFC\_OK}>V_{PFC\_OK\_S}$ and $V_{INV} < 1.66V$	Latched-off	$V_{PFC\_OK}<V_{PFC\_OK\_S}$ and $V_{INV} > 1.66V$
Low consumption	V_{COMP}<2.4V	Burst mode	V_{COMP}>2.4V
Saturated boost inductor	$V_{CS} > V_{CS\_th}$	Stop switching	Aut start after 300s

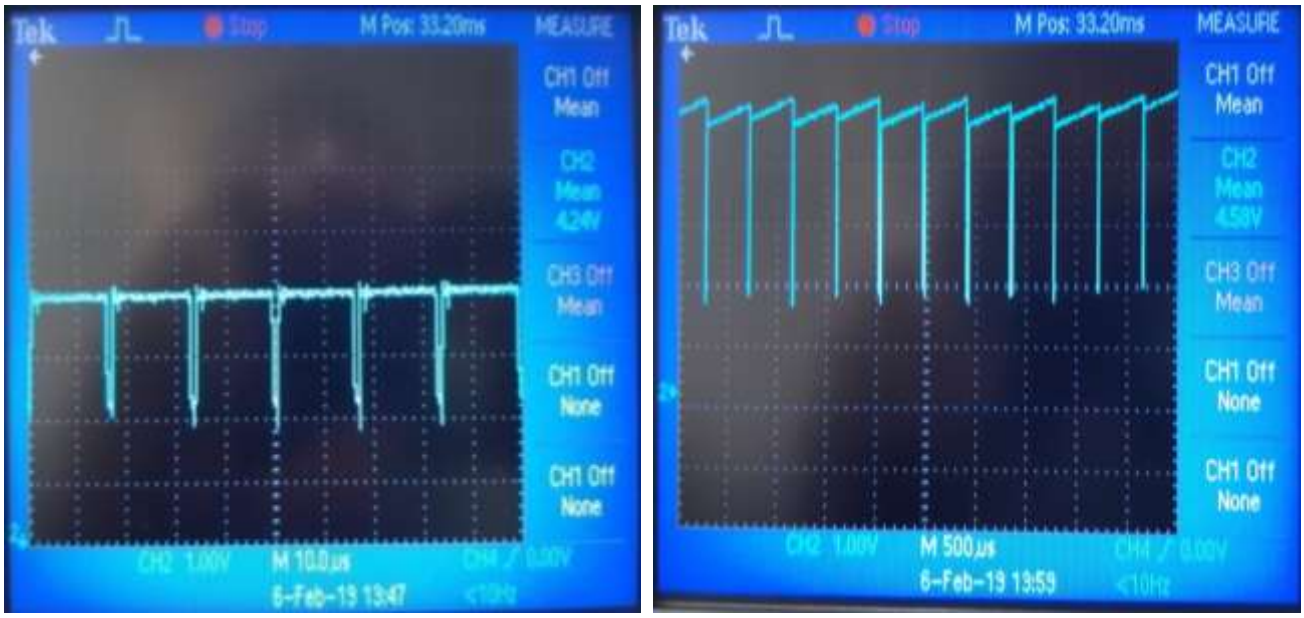
Where $V_{CCOFF} = 6V$ $V_{PFC\_OK\_D} = 0.27$ V_{PFC_OK} =0.23V_{DIS} = 0.8 $V_{PFC\_OK\_S}$ = 2.5 V_{CS_th}=1.8V

Typical waveforms are given below of each pin in the open loop condition and Loaded condition



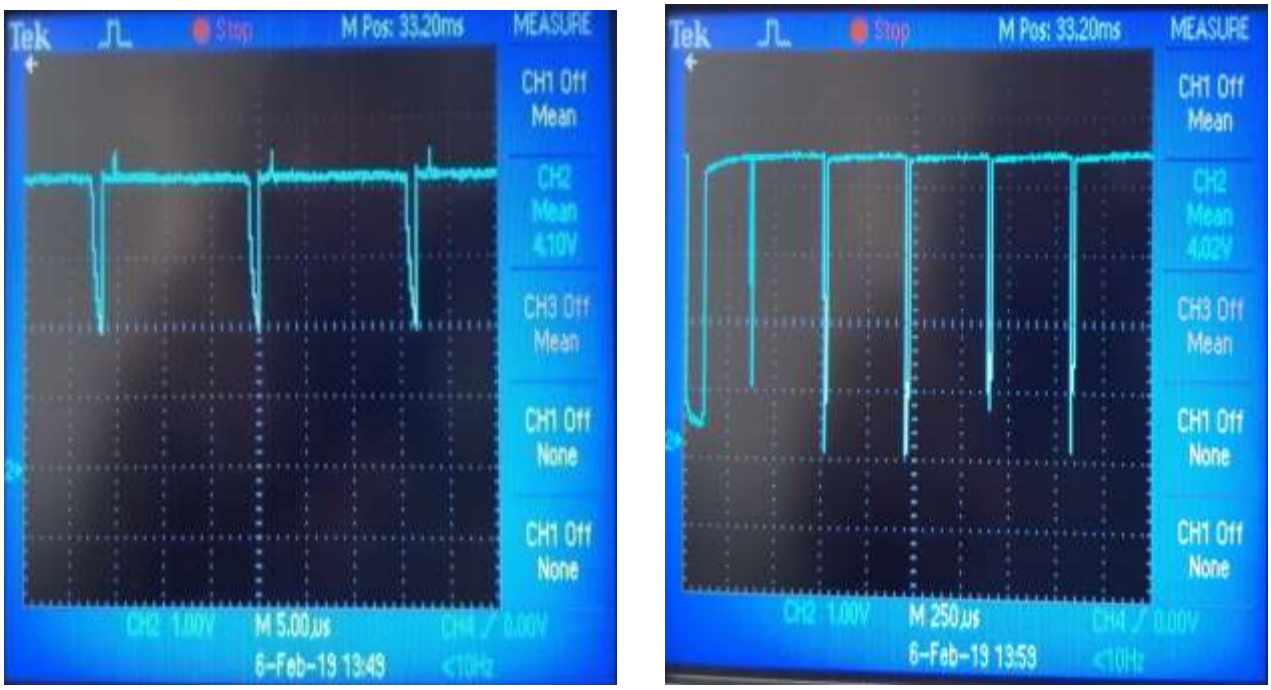
(a) (b)

Fig. 4.9: INV pin waveform (a) loaded condition (b) no load condition



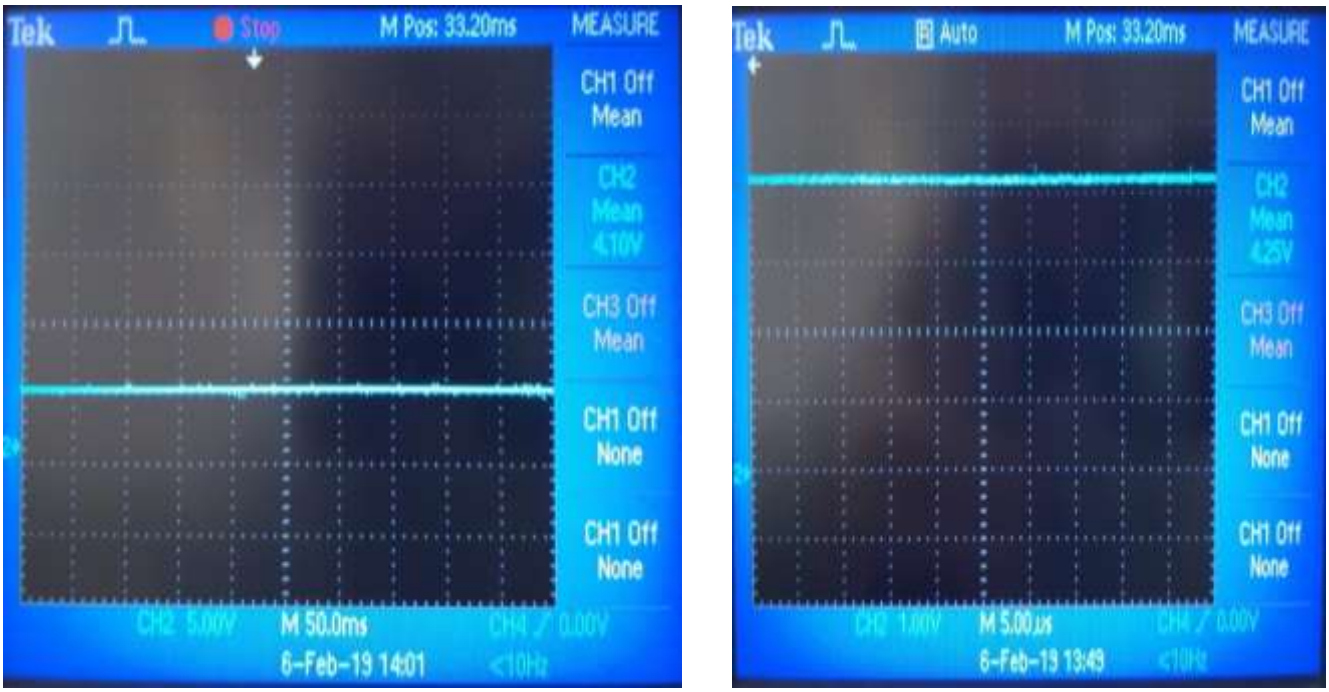
(a) (b)

Fig. 4.10: COMP pin waveform (a) loaded condition (b)no load condition



(a) (b)

Fig. 4.11: MULT Pin waveform (a) loaded condition(b)no load condition



(a) (b)

Fig. 4.12: VFF Pin waveform (a) loaded condition (b) no load condition

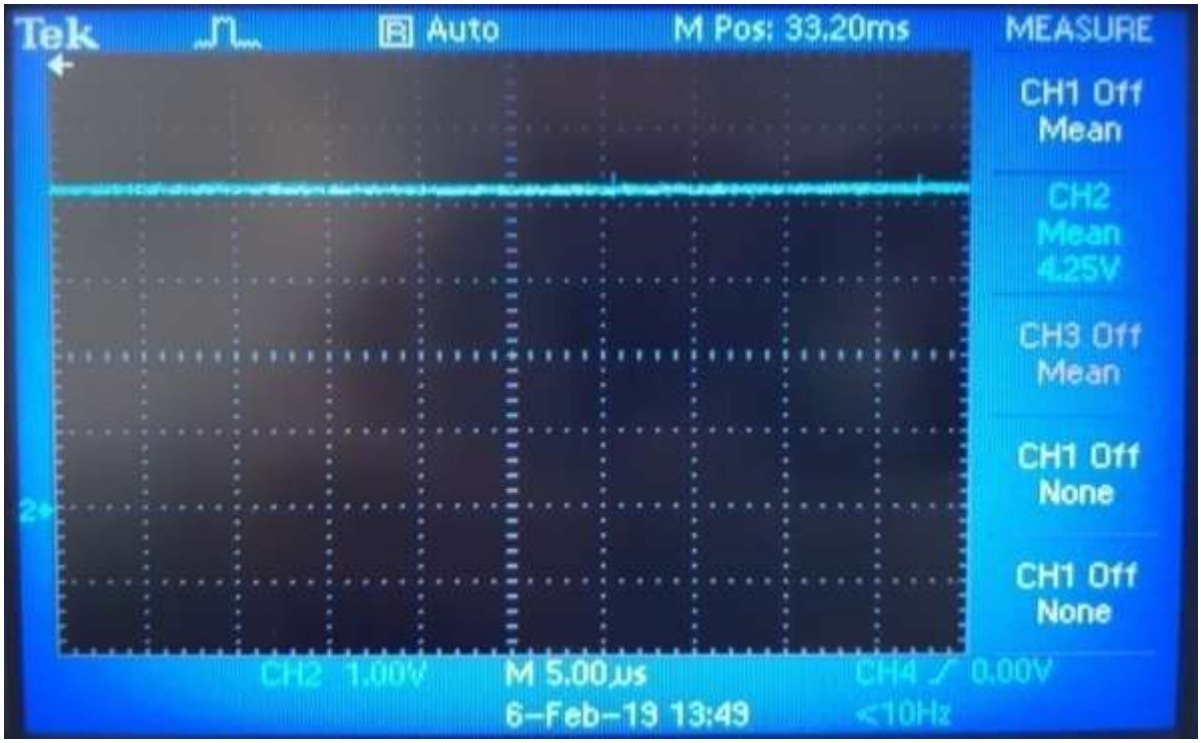


Fig. 4.13: PFC_Ok Pin waveform in loaded condition

4.4 DESIGN OF FLYBACK CONVERTER

INTRODUCTION

Flyback converter is widely used in dc-dc conversion and isolation, due its simplicity, low part count, multiple isolated outputs, high output voltages, high efficiency and low cost. The circuit is simple as illustrated in Fig. 4.14 composed of relative few components Flyback converter is especially required for low power applications (150W) [22]. Only one switch for controlling the voltage. The flyback transformer consists of one primary and secondary winding and can have multiple outputs just by increasing the number of secondary windings . [23].

Main features of flyback converters

- Simple design.
- Low component number
- Low cost
- No additional inductor at the output circuit

- Wide input range possible

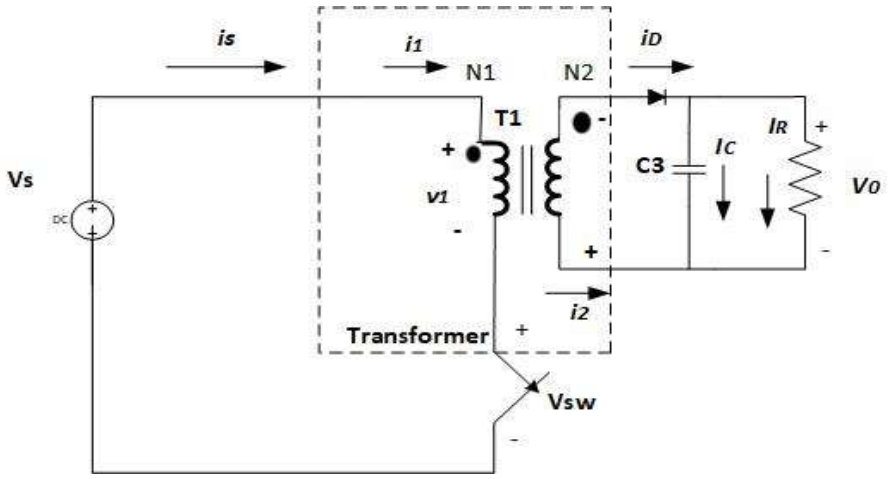


Fig. 4.14: Flyback converter

Application areas of flyback converter

- Cell phone charger, computer/laptop charger
- High voltage source for CRTs
- Xenon flash lamps, photocopies, lasers
- Isolated driver circuit

BASICS OF FLYBACK CONVERTER

The flyback operates in two periods

1) Switch on period

During the on period the primary winding is supplied by voltage which supplies a primary current to produce magnetic flux .The magnetic flux in the transformer core increases to store energy in the transformer. The output voltage on the secondary side is negative which makes diode reverse biased and no voltage is preset at output side as shown in Fig. 4.15.

Time interval 0≤t≥T i.e. Mosfet is ON

$$V1 = Vs \tag{4.37}$$

$$V2 = \frac{N2}{N1}V1 = aVs \tag{4.38}$$

During this period secondary side is open circuited and it draws only no-load magnetization current increases from $Imin$ to $Imax$ to store the energy in the transformer

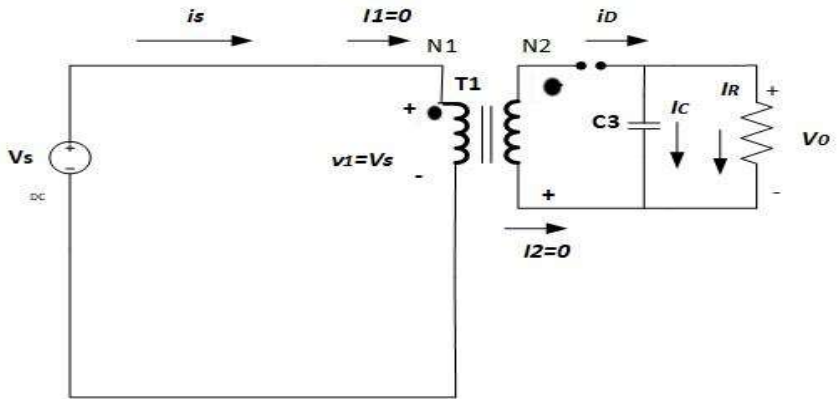


Fig.4.15: On state equivalent circuit of Flyback converter

2) Switch off period

During off period the primary current and magnetic flux drops which results in positive secondary voltage. The output diode is forward biased, and the current flow to load as shown in Fig. 4.16.

Time interval Ton ≤t≥ T i.e Mosfet is OFF

The output of the flyback converter during off time is

$$V_0 = \frac{N_2}{N_1}\frac{D}{1-D}V_S \tag{4.39}$$

Where D is the duty cycle of MOSFET switch

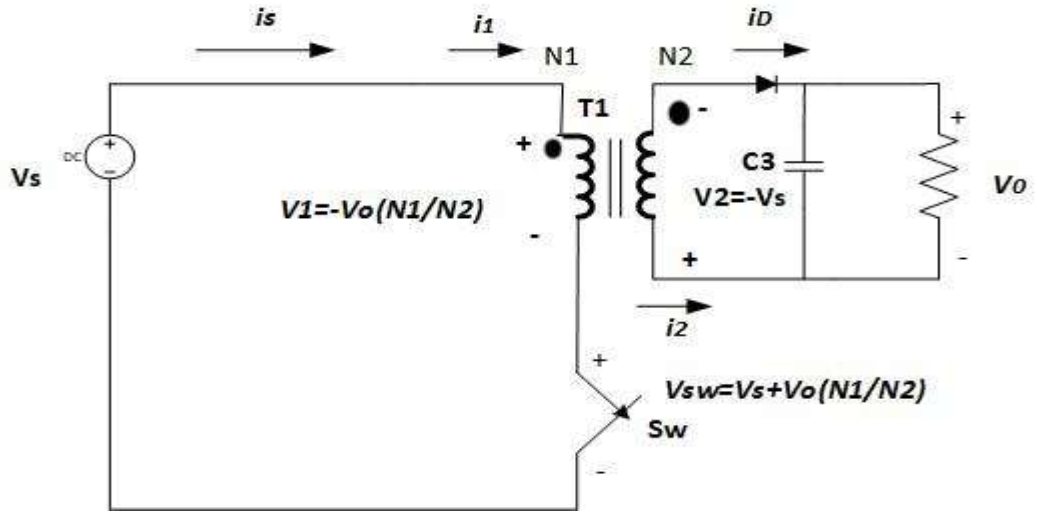


Fig. 4.16: Off state equivalent circuit

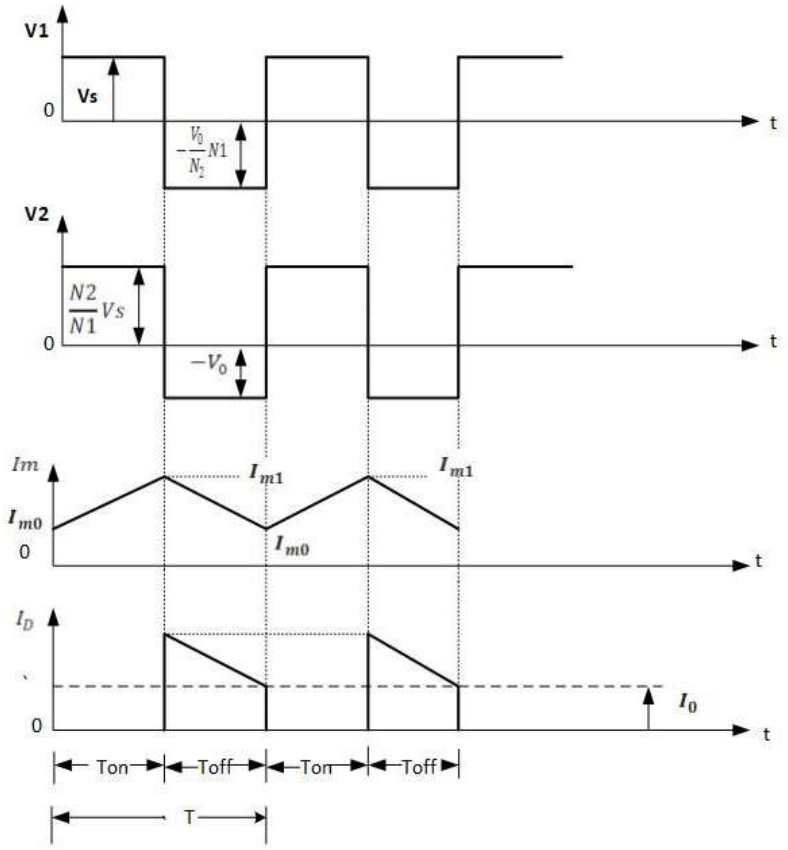
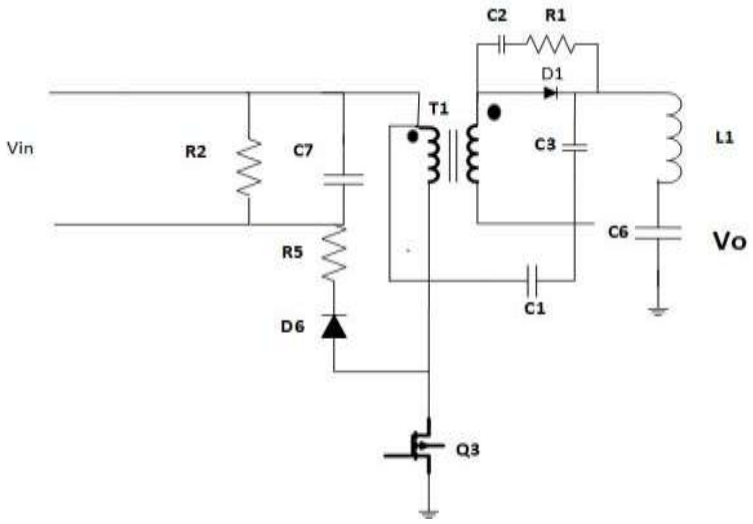


Fig. 4.17 Switching Waveforms

Every SMPS design process starts with suitable selection of components and its specifications. The following parameters need to be defined and determined.



R1, R2, R5-Resistors

C2, C7, C1,C6, C3-Capacitors

T1-Flyback transformer

Q3-MOSFET

D6, D1-Diode

Fig. 4.18: Flyback Converter

4.4.1 FLYBACK CONVERTER DESIGN (31V, 4.8A)

Input Voltage Range 336V DC -470V DC Output 31V DC, 4.8A

DESIGN PROCESS

Primary Reflected Voltage ($\boldsymbol{V_{OR}}$) $= \mathbf{139}$

Primary Inductance =470µH

Switching Frequency =60 kHz

Iprimary Peak (max-3.82A) Ipri **Rms** (max 1.19A)

TRANSFORMEER DETAILS

Core Type: ETD39TH-H-14Pin

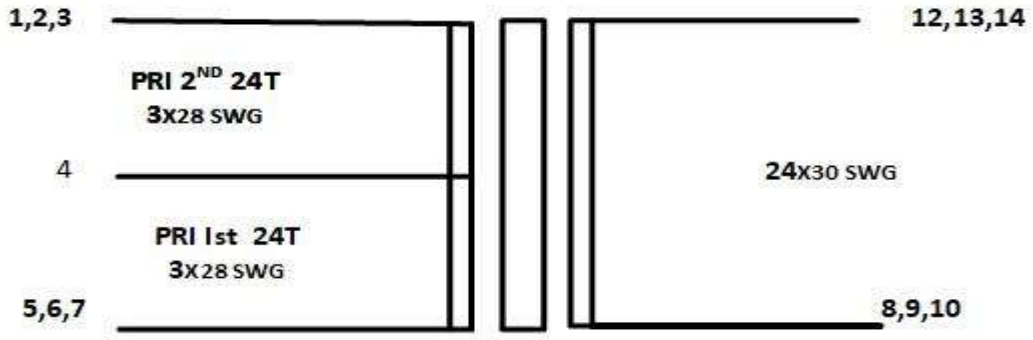


Fig. 4.19: Flyback Transformer Core

Primary Inductance: 470µH

Leakage Inductance: 4.7 µH@100KHz

Maximum Flux Density: 300mt

Required Gap Length: 0.7mm (Al: 204Nh/µH^2)

4.5 RCD CLAMPING DESIGN

INDRODUCTION

The flyback transformer consists of magnetic core with primary and secondary winding wrapped around the core. The voltage is step up or step down depending upon the number of primary and secondary turns in the transformer. When the primary winding is excited by input voltage the flux is produced in the core with some leakage out in the air termed as leakage flux. The leakage flux is modelled as a leakage inductance as shown in figure 1.Incase there is no leakage flux, there will be no leakage inductance. The effect of leakage inductance on the operation of the flyback converter is to force a voltage spike to appear across the MOSFET switch when it is turned off.

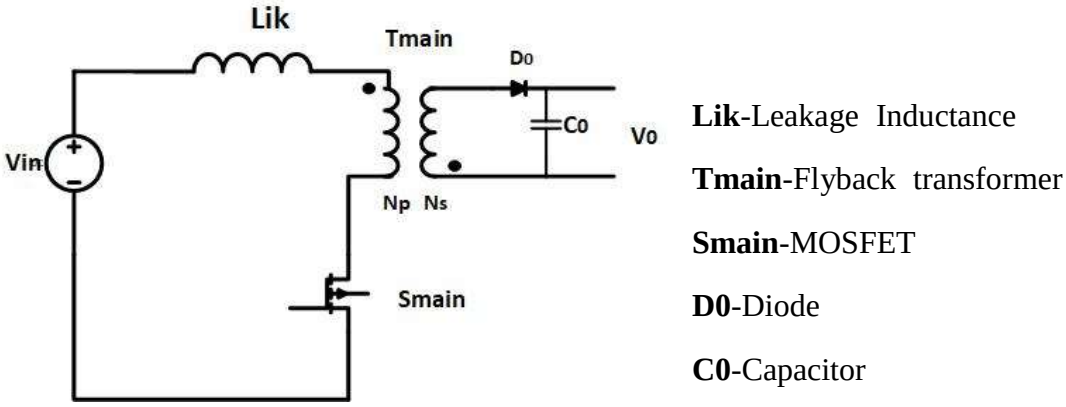


Fig. 4.20: Flyback converter with leakage inductance

The simplified circuit is shown in Fig. 3.5.The circuit shows the leakage inductor in series with the switch. During the on period of switch the current flows through the switch and inductor and during off period the energy in the transformer core is transferred to the output, but energy in the leakage inductance cannot be transferred to the output.

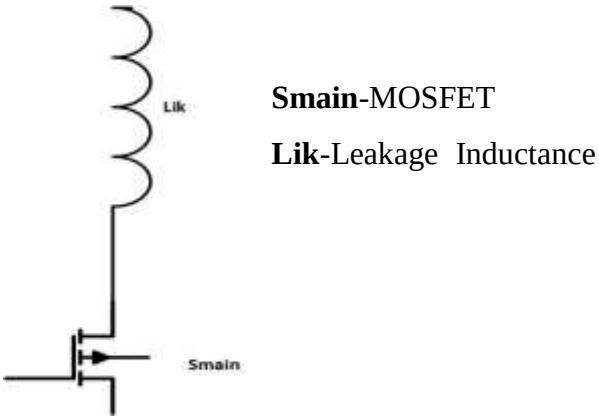


Fig. 4.21: Simplified flyback converter section with leakage inductance and switch

The leakage inductance current starts to flow through the MOSFET, thus charging the capacitor and increasing the voltage across the switch. Depending on the amount of energy stored in the leakage inductance, which is related to the amount of leakage flux in the transformer, the voltage across the device may exceed the device's ratings and a catastrophic failure of the device would happen [24].

4.5.1 DESIGN OF RCD CLAMP

The energy present in the leakage inductance should recovered and need to be converted into heat recovered and transfer to output when switch turns off, the voltage across the leakage inductance is $Vclamp - Vor$ and that cause the primary side current to slew down in an interval Δt as shown in Fig.4.22.Only after the interval delta Δt has elapsed, is the secondry side winding able to take over the entire primary side curremt and turn off transition finally gets completed[25]

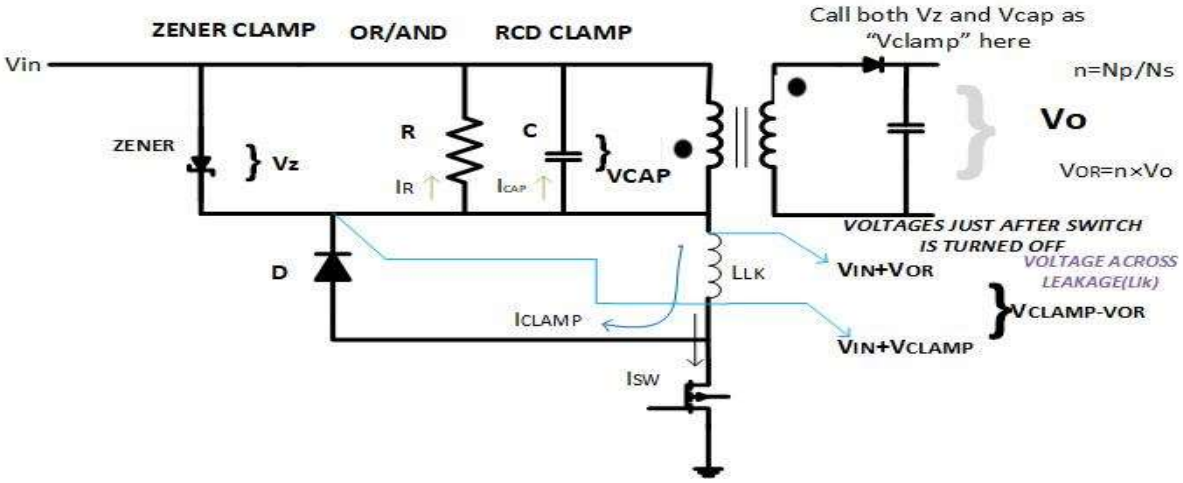


Fig. 4.22: Flyback Converter with Zener Clamp and RCD Clamp

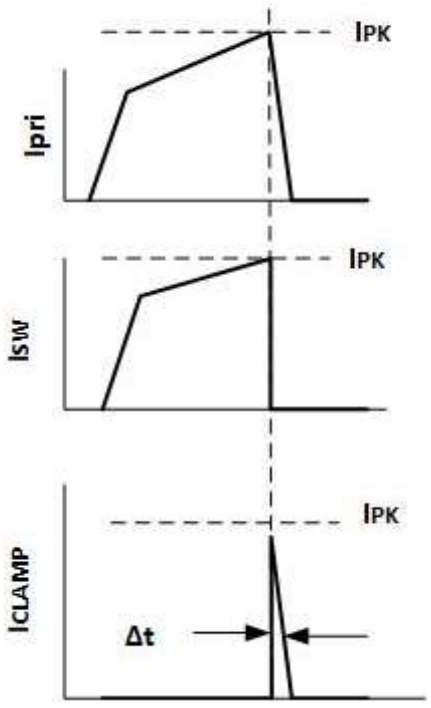


Fig. 4.23: General Clamp waveforms

Table 4.3: Input specification of Flyback converter

Input Voltage Range	336-470V DC
$\boldsymbol{Vor}$ **(Reflected Voltage)**	139
MOSFET Rating	900V, 10A
Clamping Voltage ($\boldsymbol{Vclamp/Vcap}$)	350V
Primary Peak current($\boldsymbol{I_{PK}}$)**:**	3.83
Switching Frequency ($\boldsymbol{Fsw}$)**:**	56kHz
Leakage Inductance	4.7μh

DESIGN OF CLAMP:

Finding value of R and C

Calculation R:

$$\boldsymbol{R = \frac{2 * V_{clamp} * (V_{clamp} - V_{OR})}{L_{LK} * I^2_{PK} * fsw}} \quad (4.40)$$

$$= \frac{2*350*(350-139)}{4.7\mu h*3.82*3.82*56*10^3}$$

$$= \boldsymbol{38.4Kohm}$$

Calculation C:

$$\boldsymbol{C \geq \frac{10}{R*fsw} = \frac{10}{38.4*10^3*56*10^3}} \quad (4.41)$$

$$= \boldsymbol{4.65nF}$$

Loss Calculation in RCD Clamp:

$$\mathbf{P} = \boldsymbol{\frac{1}{2} * L_{LK} * I^2_{PK} * fsw * \frac{V_{clamp}}{V_{clamp} - Vor}} \quad (4.42)$$

$$= \frac{1}{2} * 4.7 * 10^{-6} * 3.82^2 * 56 * 10^3 * \frac{350}{350-139}$$

$$= \boldsymbol{3.1W}$$

Suitable value of R and C are selected as

$$\boldsymbol{R = 40Kohm}$$

$$\boldsymbol{C = 10\ nF/1kv}$$

CHAPTER-5
RESULTS AND DISCUSSIONS

5.1PROTOTYPE & SIMULATION RESULTS

The circuit contains two important parts, AC-DC converter with Power factor correction circuit and Flyback converter. All the subsequent design calculations are given in chapter-3.The power factor correction implements the L4984D IC to accomplish Fixed OFF time technique. The PFC IC generates the pulse for Mosfet as shown in Fig.5.1.

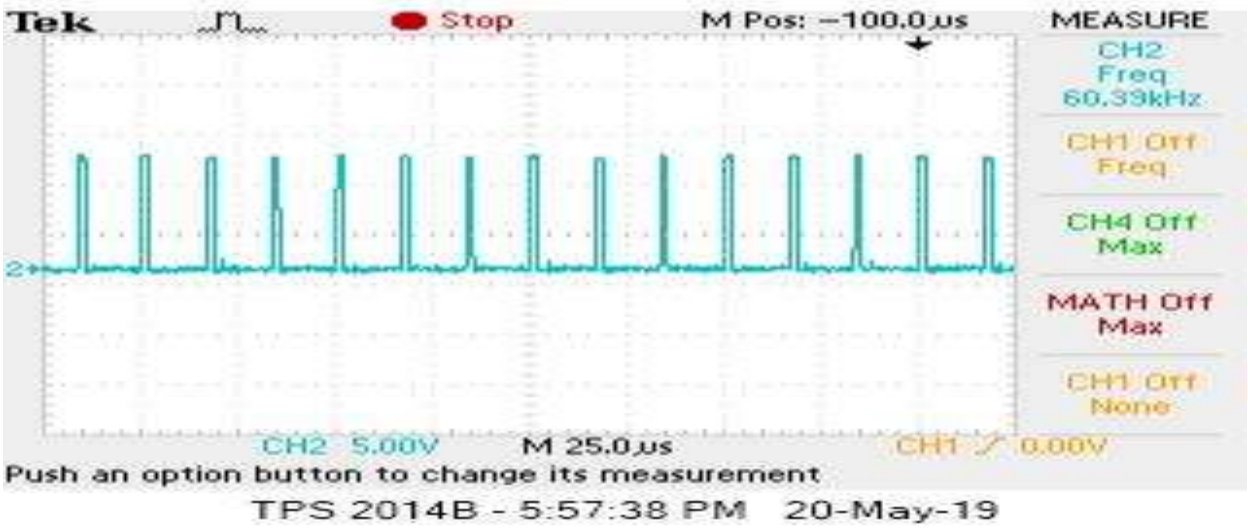


Fig. 5.1: PWM pulse for PFC MOSFET

The output of the boost converter is regulated to 450V which is more than peak of input voltage. The Fig. 5.2 shows the IC L4984D in the burst mode (mode where pulse is given to MOSFET during regular intervals) during no load.

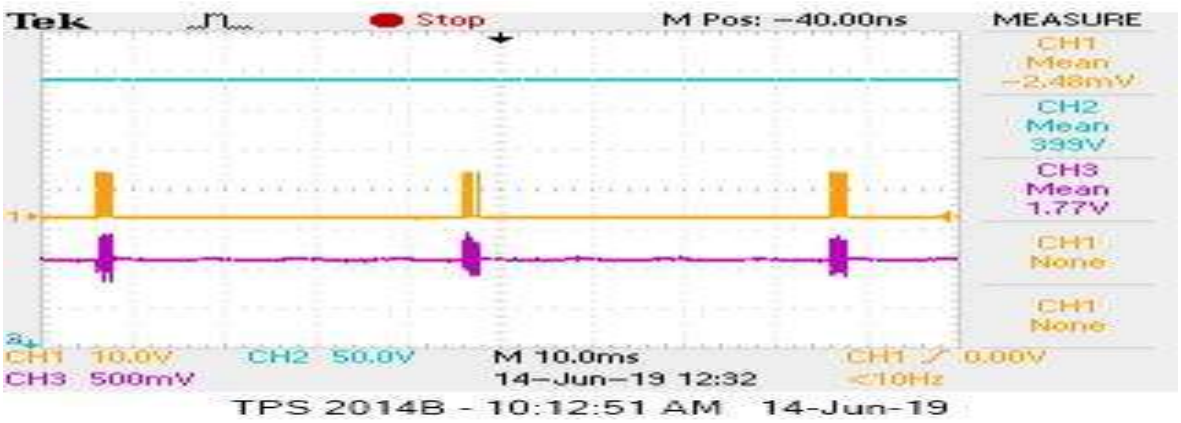


Fig. 5.2: L4984d IC in burst mode

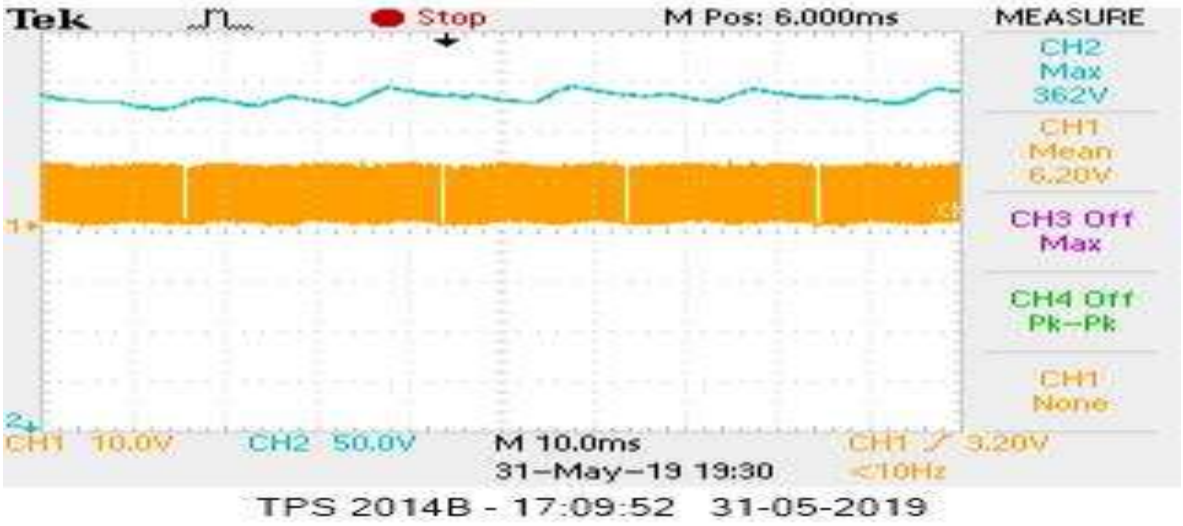


Fig. 5.3: PFC output during load condition

The flyback converter uses Mosfet which is driven by pulse generated by STM32FO70RB microcontroller as shown in Fig. 5.4.

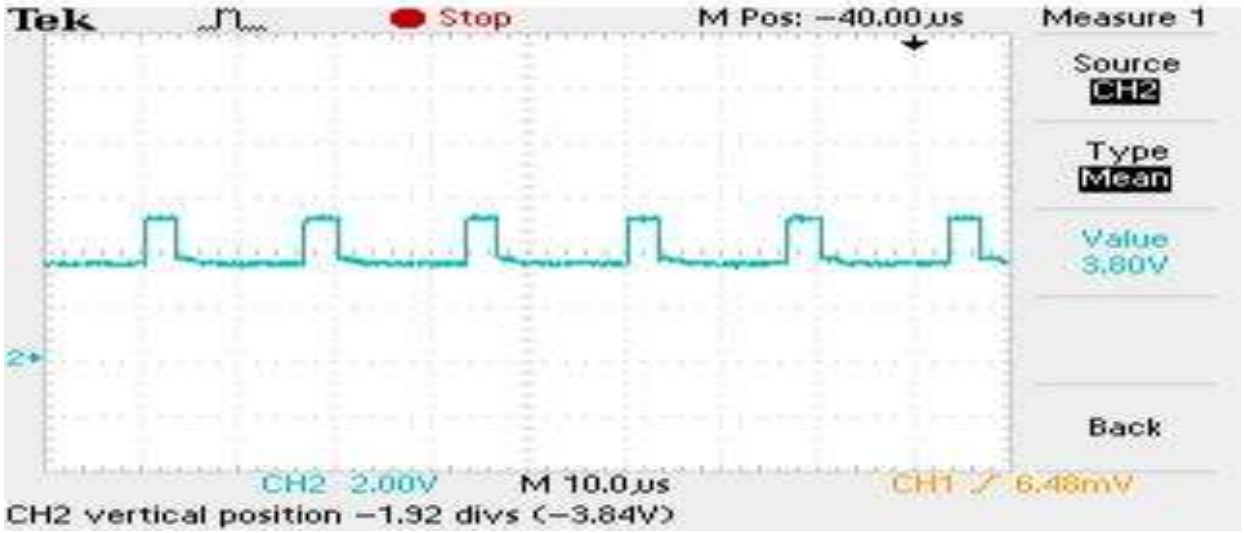


Fig. .5.4: PWM pulse from STM32FO70RB

The pulse strength is not enough to drive the Mosfet switch, so a Mosfet driver is used which generates the pulse to switch on/off the MOSFET. The pulse so generated from the driver circuit is shown in Fig. 4.17. The pulse frequency is 60 kHz.

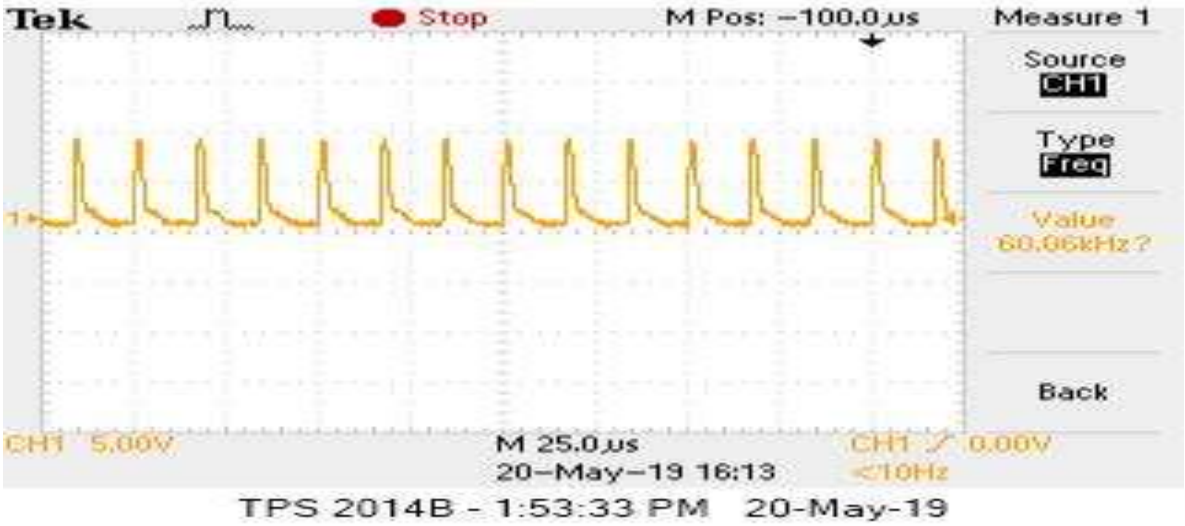


Fig. 5.5: PWM pulse from driver circuit

The Vds (drain-source voltage) as shown in the Fig. 4.18 depicts the proper working of Flyback circuit.

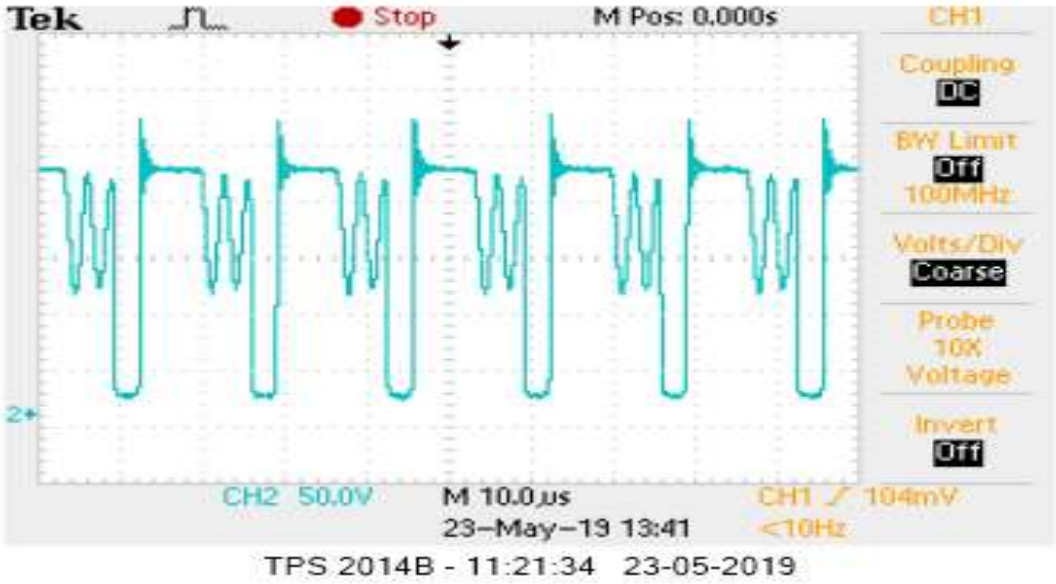


Fig.5.6: Vds (drain-source voltage) of flyback converter

The output of flyback converter is controlled by changing the duty cycle of the MOSFET. The output can be used for number of application such as battery charging, LED lighting, BLDC motor etc. In this dissertation battery charging application is considered. Since the IC L4984D used in the power factor correction is not available in the PSIM, to verify the circuit operation UC3854 IC is used for the simulation purpose as shown in Fig. 5.7 .The UC3854 is used at the output of bridge rectifier to get the regulated output voltage and near unity power factor at the input mains. Fig.5.8 sows the input current and voltage with the power factor of 0.98.The output voltage from the PFC circuit is step down with flyback converter to low voltage and isolation from the high voltage PFC circuit.

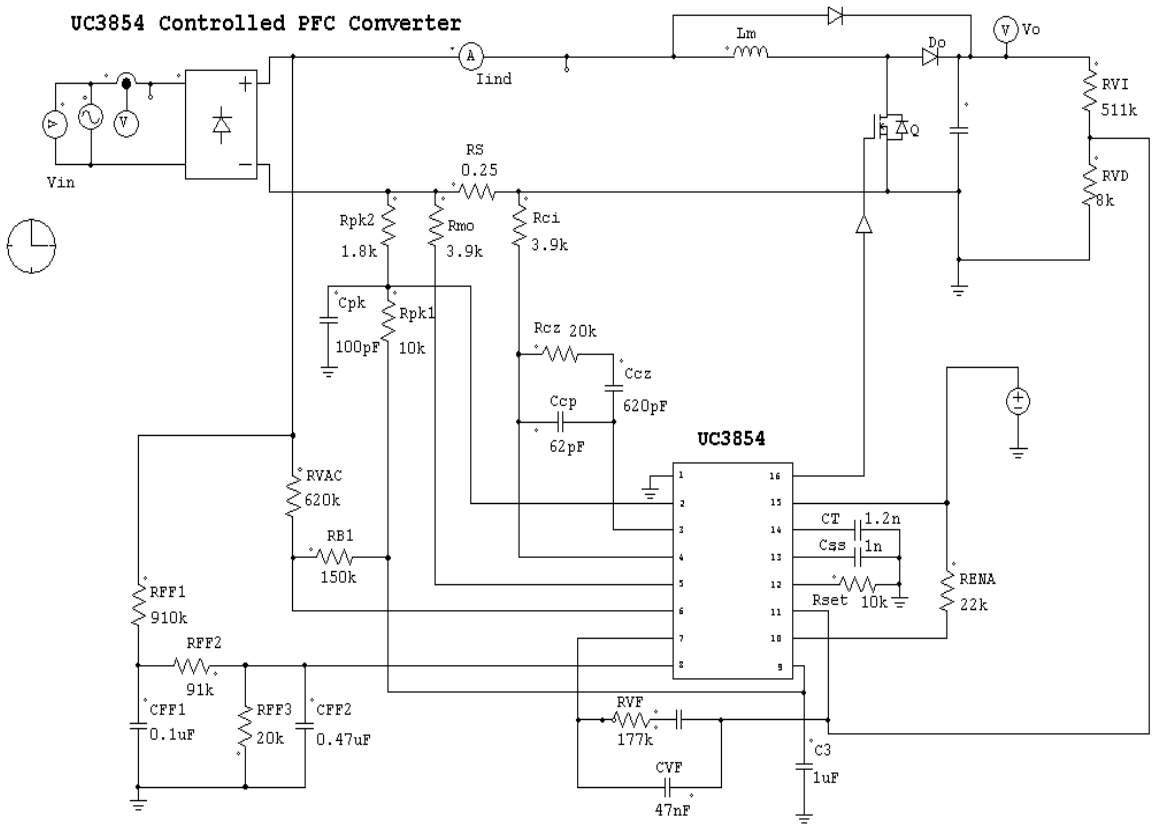


Fig. 5.7: Circuit model of AC-DC converter with PFC converter

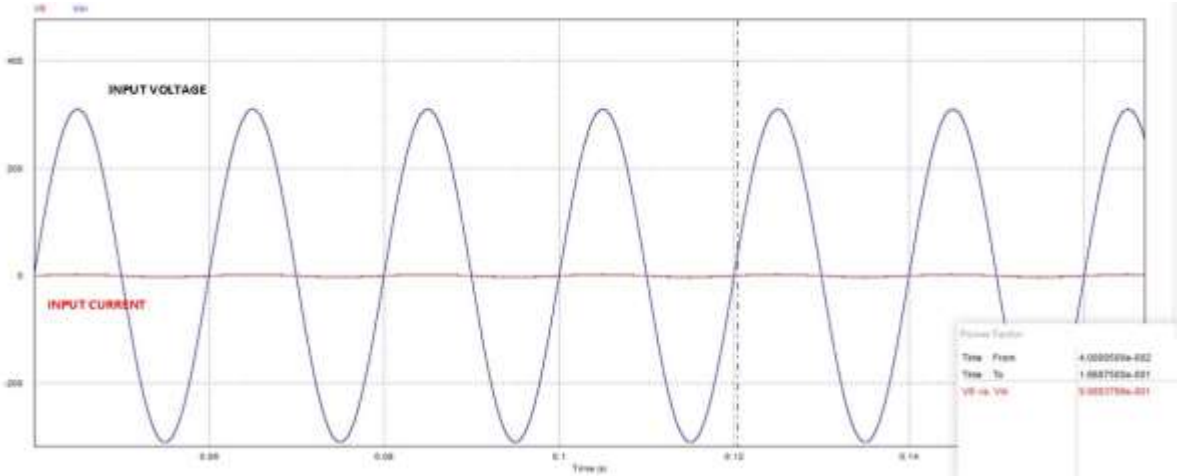
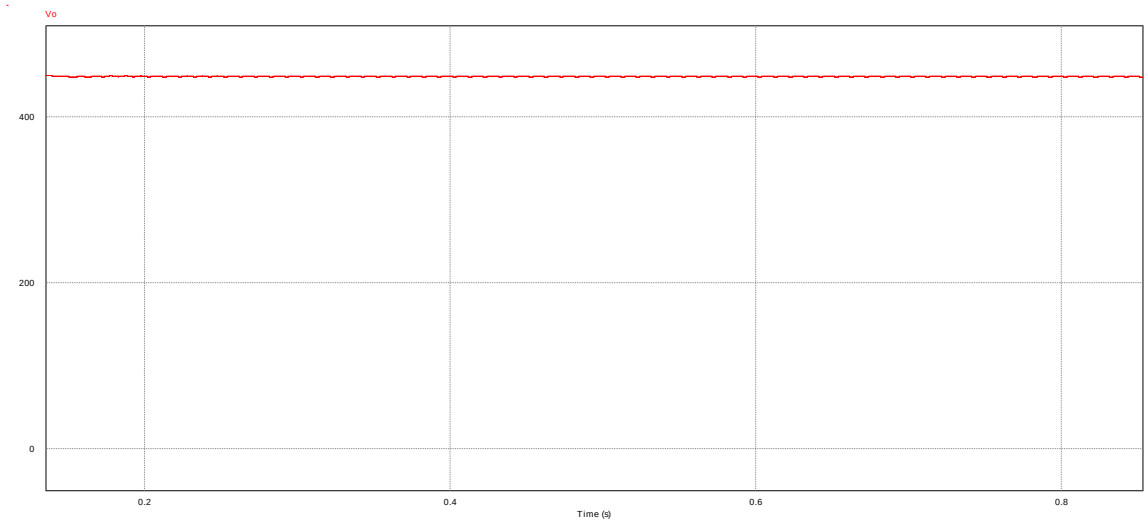
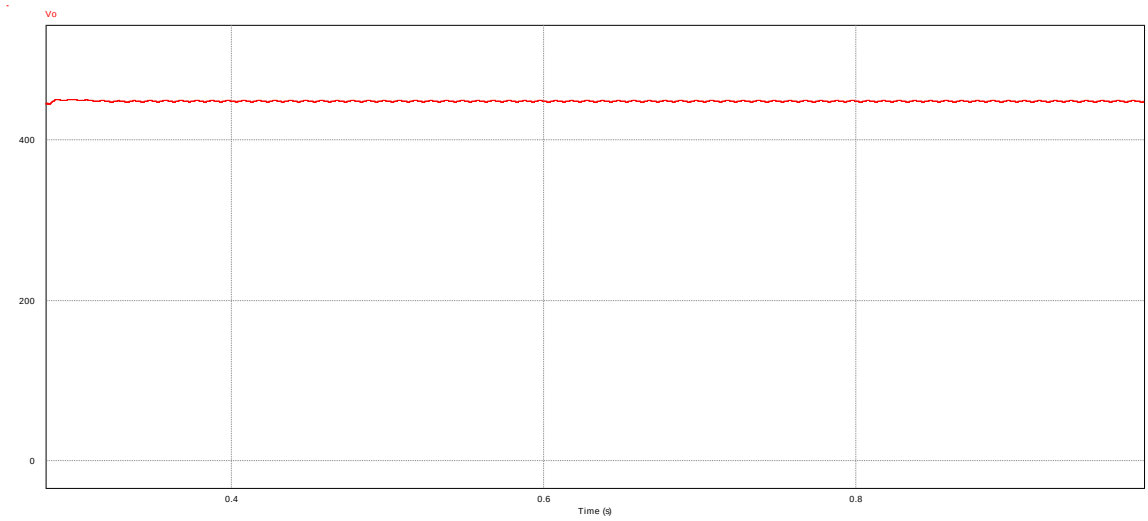


Fig. 5.8: Input Voltage and current waveforms of AC-DC Converter

Due to UC3854 the regulated voltage is obtained at the output of PFC circuit at different input voltages as shown in Fig 5.9.



(a)



(b)

Fig. 5.9: Simulated DC voltage at the output of PFC converter at (a) at input voltage 90V (b) at input voltage 220V

The flyback output voltage is fed to 24V battery. Battery load is modelled with a nominal voltage of 24V as shown in Fig. 5.10.It is connected to the output of Flyback converter and simulated at different values of Voc that represent SOC (state of charge).In the simulation CCCV mode of charging is performed by varying Voc.

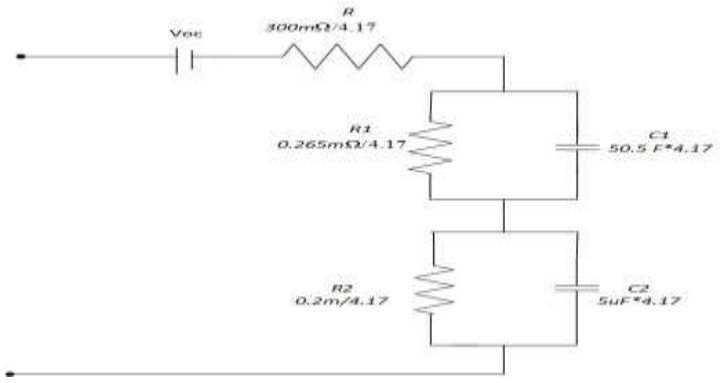


Fig. 5.10: Battery Model [25]

The complete circuit model is shown in Fig. 5.11.To perform the CCCV mode of operation the Voc in battery model is made to increase in the step changes with the increase in the duty cycle, voltage and current of Flyback converter. A look up table as given in Table 5.1 is made with two of its input are connected to the battery to sense its output voltage and other to the MOSFET switch to turned it on, regulating the current and voltage during CC and CV mode. Simulation results shown in Fig.5.12. The current waveform has spikes at transition points which can be removed by smooth change of duty cycle. The efficiency found in the simulation for AC-DC converter is 91.5% and in the Flyback Converter is 93.57% and overall efficiency for the circuit is 85.6%.

Table 5.1: Look Up Table

Battery Voltage	Duty cycle
12	0.111
14	0.119
16	0.127
18	0.136
20	0.144
22	0.152
24	0.158
26	0.163
28	0.077

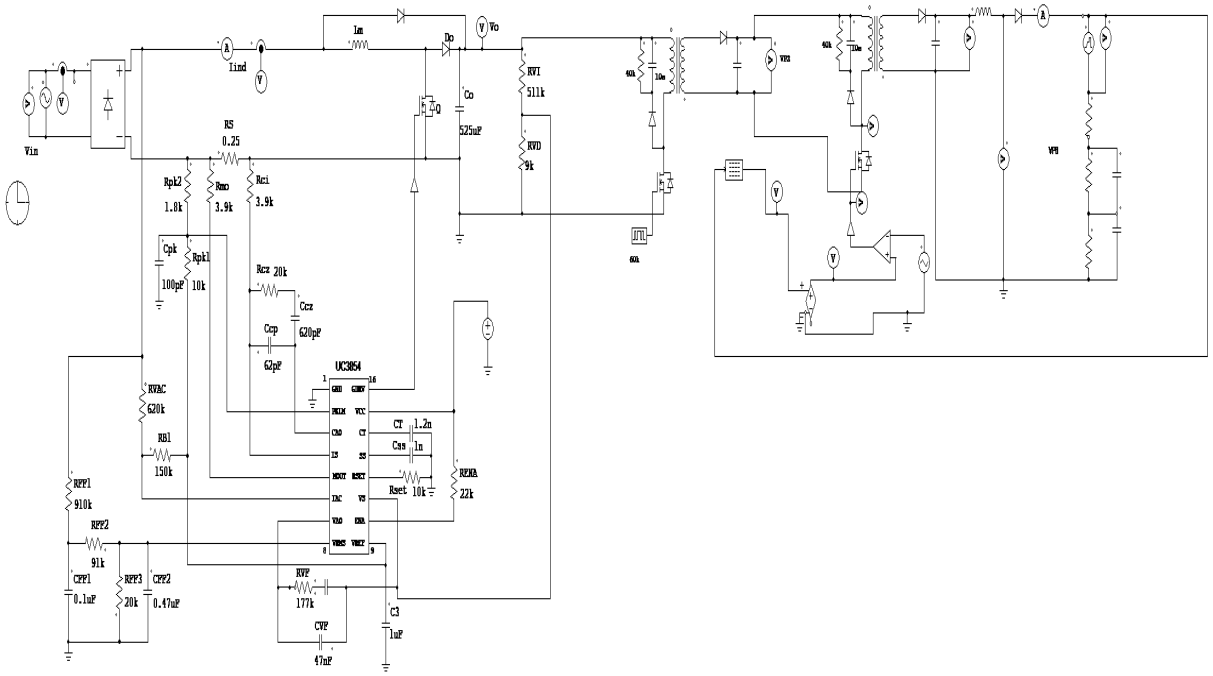


Fig. 5.11: Circuit of Modelled battery charging

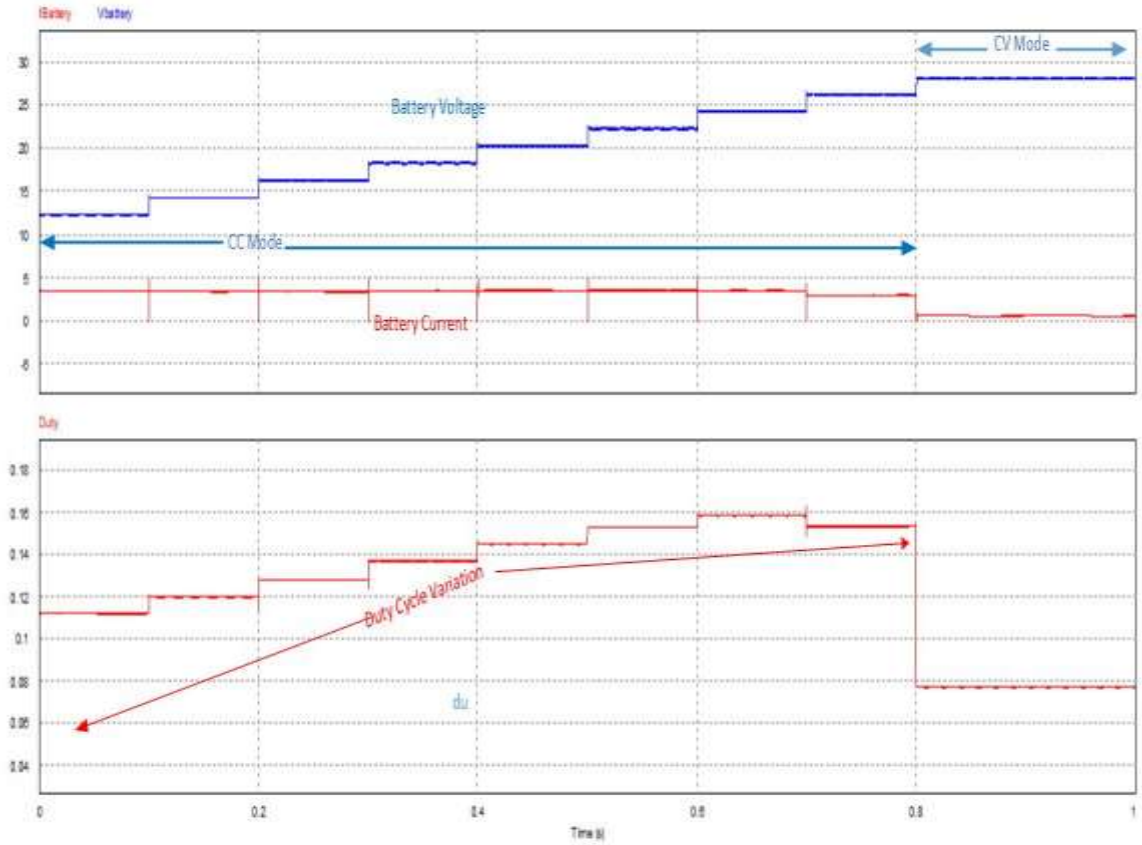
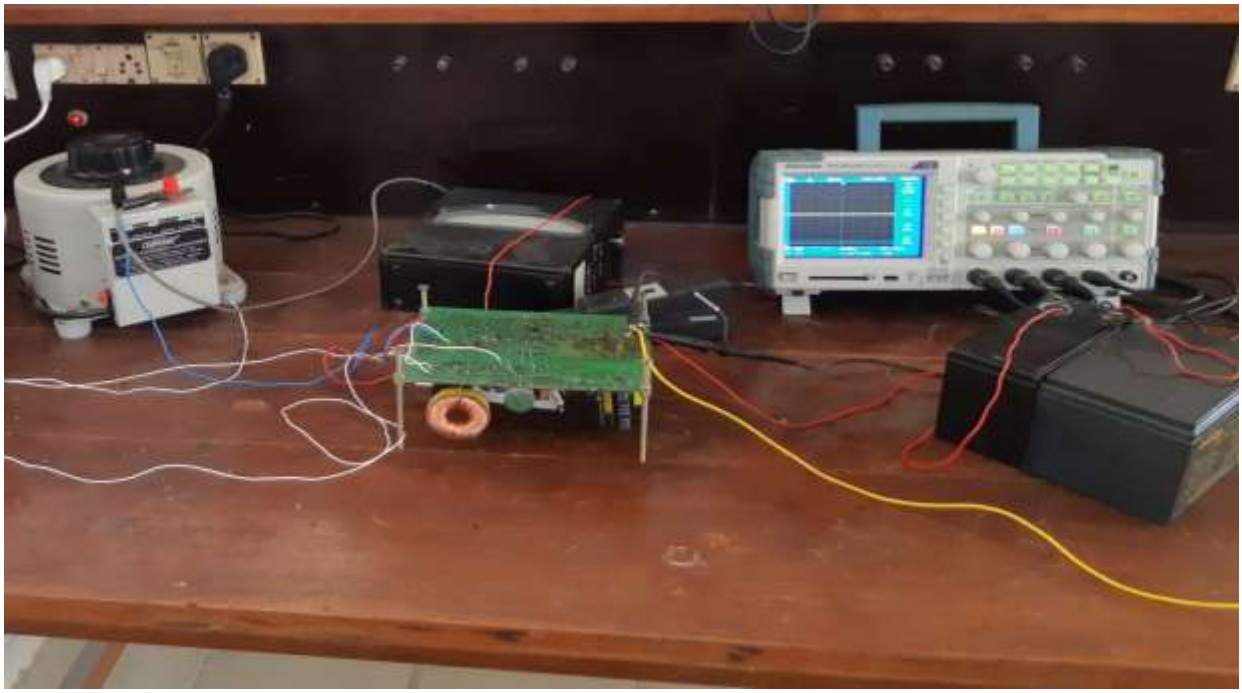


Fig. 5.12: Simulation result with CCCV mode

PROTOTYPE PHOTOGRAPH



CHAPTER-6
CONCLUSION AND FUTURE SCOPE

5.1 CONCLUSION

The power factor of the circuit is improved by using the power factor correction circuit based on the Fixed Off Time (FOT). IC L4984d based on Fixed Off Time (FOT) is used in the hardware. The operation of IC UC3854 to obtain a better power factor and a regulated output voltage is verified using PSIM. The design and simulation of the flyback converter and the RCD snubber is presented. To verify the applicability of the proposed circuit, a 24 volt charger is selected. The nominal power rating of the charger circuit is 120 watts. The battery is charged based on the constant constant current algorithm using the look up table.

5.2 FUTURE SCOPE

The future work of this project can be extended to the use of the circuit in different applications. The designed circuit can be used for various applications, such as the LED driver, the BLDC motor controller, etc. In all these applications, the need for a power factor correction unit is mandatory to meet international harmonic standards. In addition to applications, changes to the basic structure can be made to incorporate the use of zero-voltage switching and the interleaved boost converter technique.

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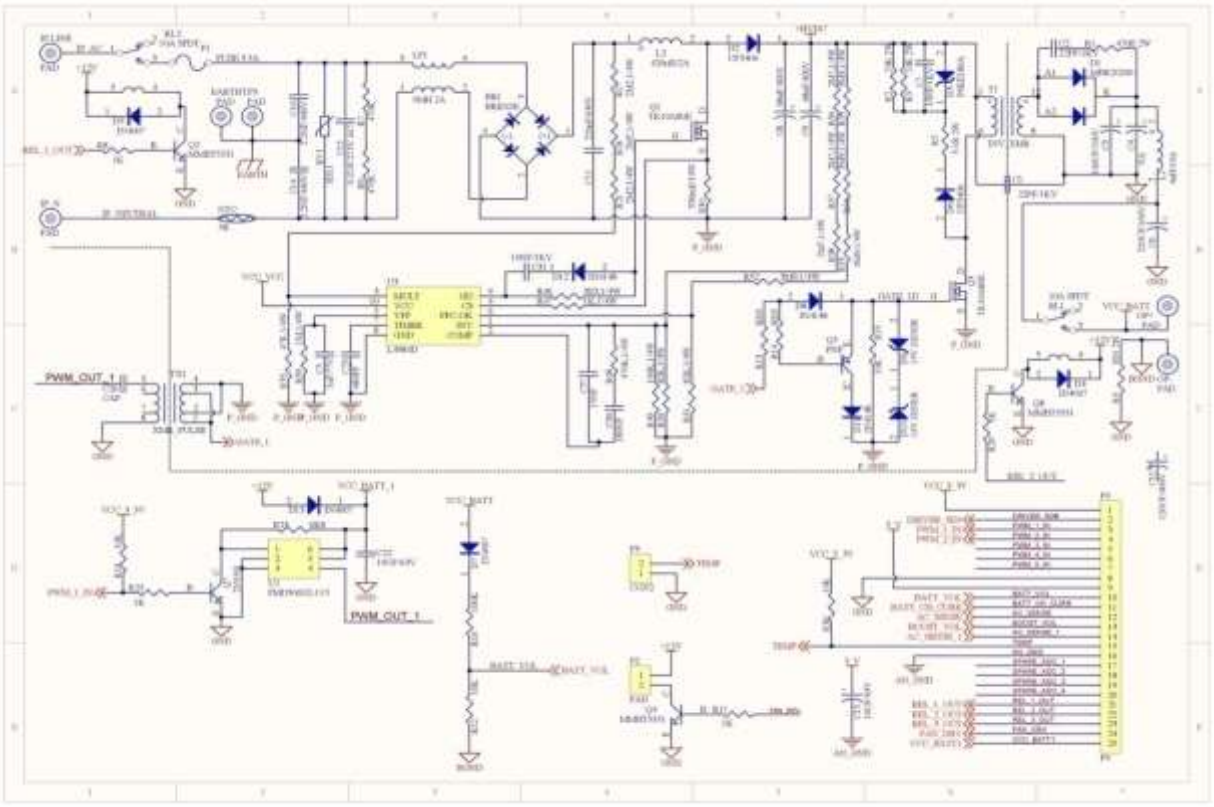
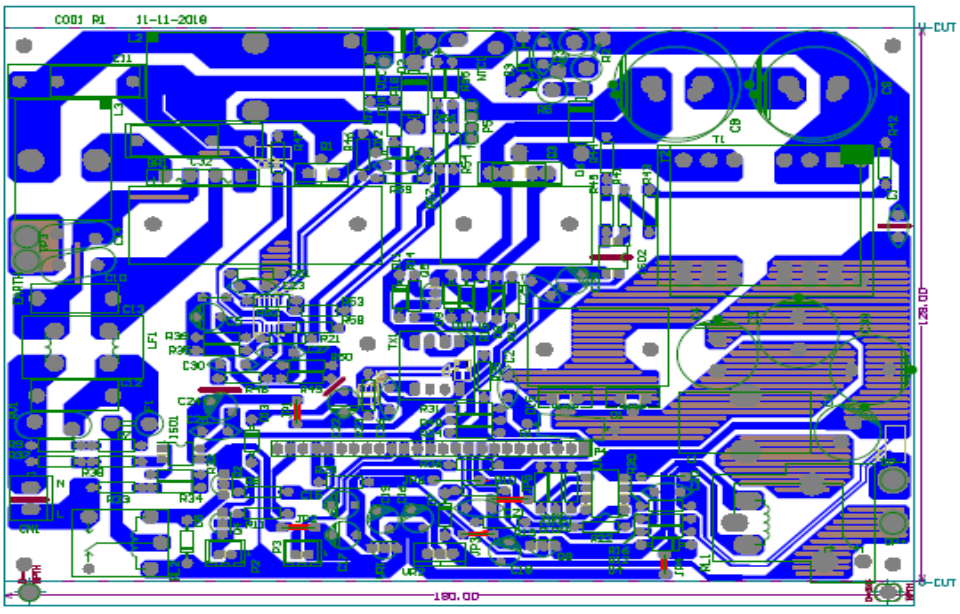
APPENDIX-A

HARDWARE SCHEMATIC



PCB DESIGN

Symbol	Hit Count	Tool Size	Plated	Hole Type
▽	98	0.9mm (35.433mil)	PTH	Round
□	186	1mm (39.37mil)	PTH	Round
○	67	1.2mm (47.244mil)	PTH	Round
⊠	9	1.3mm (51.181mil)	PTH	Round
⊠	26	1.4mm (55.118mil)	PTH	Round
○	13	1.5mm (59.055mil)	PTH	Round
▽	6	1.7mm (66.929mil)	PTH	Round
⊕	6	2mm (78.74mil)	PTH	Round
□	1	2.1mm (82.677mil)	PTH	Round
◇	5	2.2mm (86.614mil)	PTH	Round
⊠	4	2.6mm (102.362mil)	PTH	Round
▷	11	3mm (118.11mil)	PTH	Round
⊕	2	4mm (157.48mil)	NPTH	Round
	394	Total		



APPENDIX-B

LIST OF COMPONENTS

C	Designator	Type
0.1uF/50V	C20,C21,C25,C29	Capacitor
0.47uF/63V	C26	Capacitor
10NF/50V	C31	Capacitor
10NF/1KV	C7	Capacitor
2.2nF/2KV	C1	Capacitor
22PF/100V	C2	Capacitor
22NF /100V	C27	Capacitor
270NF	C30	Capacitor
680PF/50V	C23	Capacitor
10uF/63V, ALU EECTRO	C15,C22	Capacitor
1uF/16V,ALU EECTRO	C24,C28	Capacitor
1uF/63V,ALU EECTRO	C5	Capacitor
22uF/50V,ALU EECTRO	C16,,C17,C18,C19	Capacitor
220uF/50V,ALU EECTRO	C6	Capacitor
820uF/50V,ALU EECTRO	C3,C33	Capacitor
NU	C4	Capacitor
270uF/250V, ALU EECTRO	C8,C9	Capacitor
1uF/305V AC-X2 FILM CAP BOX TYPE	C12,C13	Capacitor
330nF/630V, MPP	C11,C32	Capacitor
2N2F/1KV	C10,C14	Capacitor
240mE/1W	R30	Resistor
E01 2W	R4	Resistor
100E,1/4W,MFR	R14	Resistor
100K,1/4W,MFR	R10,R49	Resistor
10E,1/4W,MFR	R13	Resistor
10K,1/4W,MFR	R12,R15,R24,R36	Resistor
1K,1/4W,MFR	R11,R16,R19,R20,R25,R26,R27,R28,R29,R47,R8	Resistor
1M,1/4W,MFR	R39	Resistor
2K4,1/4W,MFR	R31,R40	Resistor
2M2,1/4W,MFR	R17,R18,R21	Resistor
2M7,1/4W,MFR	R56,R57,R58	Resistor
300K,1/4W,MFR	R48	Resistor
33K,1/4W,MFR	R22	Resistor
3E3,1/4W,MFR	R46	Resistor
2M4,1/4W,MFR	R52,R53,R54,R55	Resistor
470K,1/4W,MFR	R7,R9	Resistor

47K,1/4W,MFR	R35,R59	Resistor
68K,1/4W,MFR	R33,R34,R37,R38,R42,R43,R44,R45,R23,R32,R41	Resistor
82K,1/4W,MFR	R51	Resistor
6K8,1/4W,MFR	R23,R32,R41	Resistor
82K,1/4W,MFR	R50	Resistor
82K,3W,MOR	R2	Resistor
NU	R3	Resistor
470E 2W/MOR	R1	Resistor
5.1R 2W,MOR	R5	Resistor
15V ZENER	D10,D9	Diode
IN4007	D13,D4,D5,D7	Diode
IN4148	D11,D12,,D8	Diode
NU	D3	Diode
IN5406	D14	Diode
STTH3R06RL OR MUR460	D2	Diode
STTH110	D6	Diode
SR20H200C	D1,D15	Diode
FUSE 4A	F1	Fuse
GBU4J OR RBU406M	BR1	Bridge rectifier
CONTROL CARD	P4	HEADER25X1
MOV,310V	RV1	PITCH,7.5MM
NTC 5R	NTC1	NTC
PC814	ISO1	Photo coupler
PC814	ISO2	Photo coupler
BA10358F-E2	U1	PDIP8
PMD3001D,115	U2	SOT23-6
BC847	Q7	SOT23-BCE
PFC INDUCTOR,1831mH/2A	L2	TOROIDAL Inductor
70uH/2A	L3	TOROIDAL Inductor
3mH EMI LINE FILTER	LF1	Emi Filter
PULSE TRANSFORMER	TX1	XMR_PULSE
4uH/10A, OUT PUT FILTER	L1	TOROIDIAL
TRANSFORMER,EER42	T1	ALSA_XMR
L4984D	U3	SSO10
2N5401	Q5	TO92-CBE
MMBT5551	Q2,Q4,Q8	TO92-CBE
LP2950	VR1	Voltage Regulator
STF18N65M5	Q1	MOSFET

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FOT based AC-DC Converter

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