TOPOLOGY AND PWM TECHNIQUE DESIGN OF Z-SOURCE INVERTERS

A Thesis

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by

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CERTIFICATE

This is to certify that the thesis entitled **"TOPOLOGY AND PWM TECHNIQUE DESIGN OF Z-SOURCE INVERTERS"** being submitted by Mr. Satwant Singh to the Department of Electrical & Instrumentation Engineering, Thapar Institute of Engineering & Technology (Deemed to be University), Patiala, Punjab, India for the award of the degree of **Doctor of Philosophy**, is a record of bonafide research work carried out by him under my guidance and supervision and has fulfilled the requirements for the submission of this thesis, which to my knowledge has reached the requisite standard.

The results embodied in the thesis have not been submitted in part or full to any other Institute or University for the award of any diploma or degree.

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ABSTRACT

The single-stage buck-boost inverter (DC-AC conversion) technology together with the two-level (2L) and multilevel output voltage topologies has a wide area of applications such as electric drives, distributed power generation (wind, PV, fuel cell, etc.), FACT devices, and electric vehicles. The continuous improvements in this technology strengthen its position in the above-mentioned applications. The concept of Z source inverter (ZSI) is most popular in the single-stage buck-boost inverter technology. As compared to the voltage source inverters (VSI), the concept of ZSI offers increased reliability because the impedance network used in ZSIs eliminates the chances of direct short-circuiting of input dc source during turn on/off transitions of power switches of the same phase leg. Therefore, the dead time requirements are nil in ZSIs.

However, the concept of ZSI still requires to be explored in its various aspects such as the size of the impedance network (IN), implementation and analysis in multilevel DC-AC topologies, methods to increase its input-output voltage gain, and suitability to various existing PWM techniques of VSI after proper modification, etc.

The research work carried out in this thesis attempt to contribute to the recent development in the field of ZSI. Starting from two-level ZSI (2L-ZSI), this research work explores the new possibilities in its PWM techniques developments. The design and experimental implementation of advanced bus clamping (ABC) PWM switching sequences in 2L-ZSI is an important contribution of this research work. It has been seen that, a properly designed space vector PWM (SVPWM) technique using ABC switching sequences reduces the size of the IN of 2L-ZSI by 34 percent as compared to the conventional PWM technique.

In case of three-level ZSI (3L-ZSI), the research work starts with the implementation of the concept of ZSI in the controlled diode bridge clamped (CDBC) VSI configuration. Here, the main advantages and drawbacks of using CDBC ZSI have been highlighted. Besides, a new version of continuous SVPWM of 3L-ZSI is proposed. The proposed SVPWM switching pattern optimizes the number of switching transitions per carrier cycle and points out the dependency of the modulation index on the switching frequency of the power switches.

Progressing forward to contribute further to the PWM techniques of 3L-ZSI, a modified SVPWM switching state diagram and two new reduced common-mode voltage (CMV) switching patterns

have been proposed. Modified three-level (3L) SVPWM switching diagram offers enhanced dc bus utilization as compared to its conventional counterpart.

An improved version of the maximum boost control (MBC) technique of voltage boosting has been also proposed based on the proposed modified SVPWM switching state diagram. The improved version of the MBC technique eliminates the problem of the sixth fundamental frequency ripple components of impedance network inductor current present in the existing MBC of voltage boosting. The proposed reduced CMV switching patterns offer the reduced size of the IN while limiting the CMV magnitude to one-sixth of the available dc-link voltage.

The above mentioned research work is successfully validated using theoretical findings, simulation, and experimental results.

Lastly, for the application of an isolated PV power generation unit, a unified closed-loop control technique has been implemented in 3L-ZSI. The theoretical findings and simulation results proves the effectiveness of the unified closed-loop control technique of 3L-ZSI.

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LIST OF ABBREVIATIONS

ABC	Advanced Bus Clamping
CDBC	Controlled Diode Bridge Clamped
CMV	Common Mode Voltage
IN	Impedance Network
IMBC	Improved Maximum Boost Control
MCB	Maximum Constant Boost Control
MBC	Maximum Boost Control
NPC	Neutral Point Clamped
NTV	Nearest Three Vector
PWM	Pulse Width Modulation
PV	Photo Voltaic
SVPWM	Space Vector Pulse Width Modulation
SBC	Simple Boost Control
VSI	Voltage Source Inverter
ZSI	Z-Source Inverter
3L	Three-Level
2L	Two-level

CHAPTER 1. INTRODUCTION AND LITERATURE SURVEY

1.1. INTRODUCTION

The share of power electronics converters in the modern power system is increasing exponentially day by day. These converters facilitate four types of power conversion such as DC-DC, DC-AC, AC-DC, and AC-AC. Each of these power conversion stages has its importance in the modern power system. The field of DC-AC conversion i.e. inverters has a key role in the major applications such as distributed power generation using renewable energy sources (PV, wind, fuel cell), electric drives/ vehicles, and FACT devices, etc. Since last two decade, the research in the field of DC-AC power conversion has resulted in many advanced inverter topologies and PWM control techniques for improvement in efficiency. The turning point in this field is the transition of the researcher's focus from two-level (2L) to multilevel inverters and invention of single-stage buck-boost inverters. The major driving factors for research and developments in dc-ac conversion are, desire to achieve better output waveform quality with improved reliability, efficiency, and the optimum cost of the overall unit.

1.2. STATE OF ART IN DC-AC POWER CONVERSION

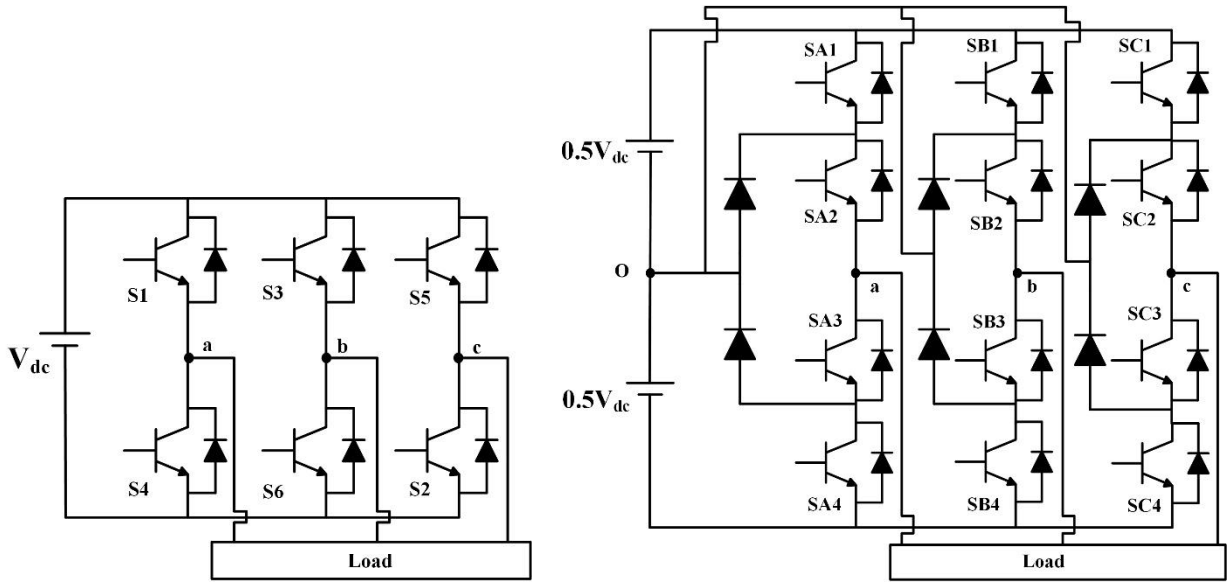
The conventional standalone configurations of dc-ac power conversion are shown in Fig. 1.1. Fig. 1.1(a) and Fig. 1.1(b) shows two-level voltage source inverter (2L-VSI) [1] and three-level (3L) neutral point clamped (NPC) VSI [2], respectively. The peak fundamental RMS line-line voltage of the conventional VSI can be written as:

$$\mathrm{V_{ab}(rms)} = \frac{\sqrt{3}.\,\mathrm{M}.\,\mathrm{V_{dc}}}{2\sqrt{2}} = 0.612.\,\mathrm{M}.\,\mathrm{V_{dc}} \qquad (1.1)$$

'M' is the modulation index and $\mathrm{V_{dc}}$ is the input dc source voltage.

The range of modulation index is $(0 < \mathrm{M} \leq 1)$ and $(0 < \mathrm{M} \leq 1.15)$ for the sine triangle and space vector PWM (SVPWM) technique, respectively. From equation (1.1) it is clear that the VSI configurations shown in Fig. 1.1 always act in voltage buck mode. The max line voltage rms value which can be achieved using the SVPWM approach is $0.70.\,\mathrm{V_{dc}}$. Also, as per the reliability concern, to avoid the direct short circuit of the input dc source, the dead time between the power

switches of the same phase legs is mandatory in these configurations. The dead time affects the inverter's performance in terms of efficiency and the output waveform quality.



(a) (b)

Fig. 1.1. Configuration of voltage source inverters (a) two-level VSI, (b) 3L neutral point clamped (NPC) VSI.

In a distributed power generation application where input is direct current (DC) and the required output is alternating current (AC), the commonly used arrangement is shown in Fig. 1.2. This arrangement uses two types of power converters, DC-DC and DC-AC.

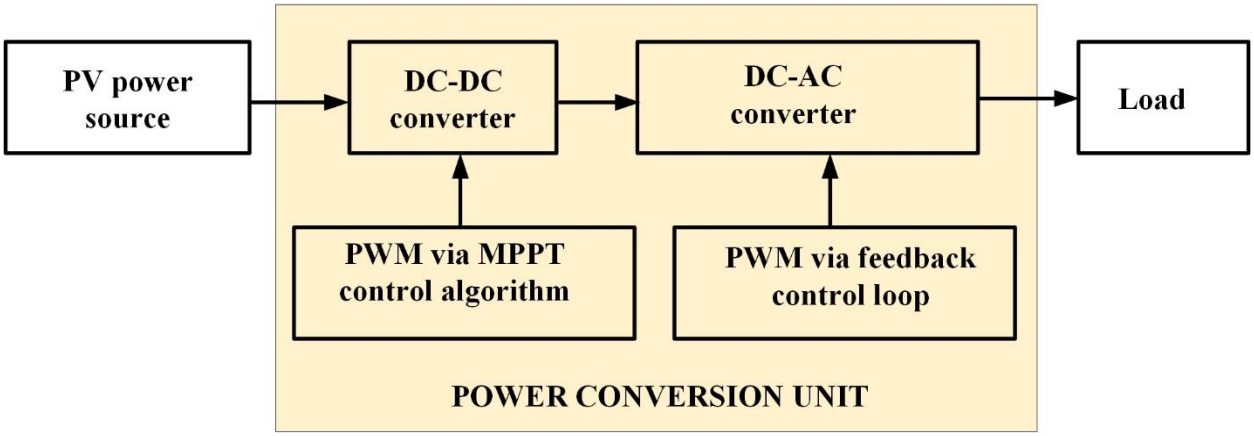


Fig. 1.2. General structure of PV power generation unit having two-stage power conversion.

To fulfill the AC voltage requirement of the load, the dc voltage at the input terminal of the inverter must be scaled to the appropriate level. Since the input DC voltage is variable in renewable sources such as PV, fuel cell, etc., the DC-DC converter stage is a must in this arrangement. DC-DC converter stage also adjusts the magnitude of DC power to be supplied to the input terminals of the inverter by changing the duty ratio of its power switches as per the maximum power point tracking (MPPT) algorithm. On the other hand, the inverter stage adjusts the output AC line voltage and current via appropriate feedback control loop to fulfill load requirement/inject power to the grid. The problems associated with this two-stage arrangement is that it requires simultaneous control of two power converters. Also, this arrangement incurs more power losses because of two-stage power conversion. The recent developments in the area of DC-AC power conversion has transformed this two-stage process into a single stage. This has been made possible by the concept of Z source inverter (ZSI). The concept of ZSI proposed two major modifications in the conventional VSI structure. These modifications are, the insertion of LC impedance network (IN) between the input dc source and the inverter switches, and insertion of shoot-through (ST) state in the existing PWM switching pattern (i.e. strategy of phase leg short circuit via IN). The conventional LC IN proposed in [3] is a combination of two inductors and two capacitors connected in a particular fashion as shown in Fig. 1.3.

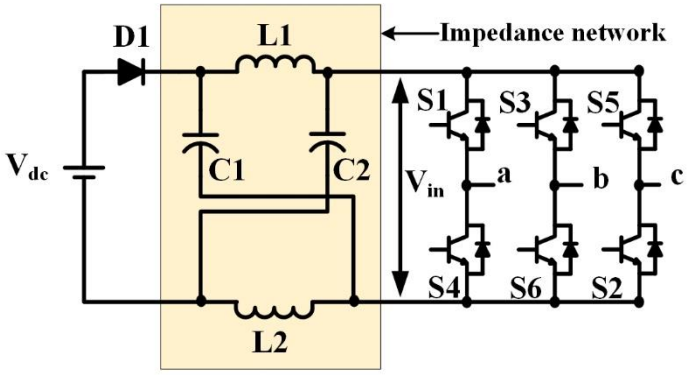


Fig. 1.3. Configuration of conventional Z-source inverter (ZSI).

The author of [3], carefully analyzed the existing null states, [111] and [000] of 2L-VSI. In null states [111] and [000] of VSI, all upper switches and all lower switches are turned ON, respectively. These states ultimately give zero line to line voltage (i.e zero power transfer to load). Therefore, these null states have been replaced with such a combination of ON power switches so that a short circuit path across the IN can be created. These states are known as ST states. ST states

help in charging of the inductors present in the IN thereby assists in the voltage buck-boost operation.Finally, using a combination of inductors and capacitors in IN and the ST states in PWM technique, the transformed VSI (i.e ZSI) offers several merits as compared to the conventional VSI. These merits include:

- Single-stage buck-boost operation
- Elimination of dead time between inverter switches of the same phase leg
- Increased reliability and improved output waveform quality

Parallel to the developments in two-level ZSI (2L-ZSI), this concept has been also investigated for multilevel VSIs to incorporate the above-mentioned advantages. Likewise in 2L-ZSI, IN is inserted before the inverter switches of a multilevel inverter circuit and the essential modifications in PWM control have been proposed in the literature. This has been discussed in detail in the literature survey of three-level ZSI (3L-ZSI). In this research work, the area of the PWM techniques of 2L-ZSI as well as PWM and topology area of 3L-ZSI have been investigated.

1.3. LITERATURE SURVEY OF TWO LEVEL ZSI (2L-ZSI)

Since its invention, the field of 2L-ZSI has seen progressive improvements in its PWM control, topology, closed-loop control techniques, and area of its applications. The analysis of the literature survey of PWM techniques of 2L-ZSI is as under.

1.3.1. PWM techniques of 2L-ZSI

In the case of 2L-VSI (Fig. 1.1(a)), there are a total of 8 possible combinations of switching states. These combinations are shown in Fig. 1.4. Out of 8 possible switching states, only 6 switching states are responsible for power flow to the load. These states are also known as active states. The remaining two switching states are known as null states as they produce zero line to line voltage. On the other hand, in 2L-ZSI, there are a total of 12 possible combinations of switching states (see Fig. 1.4). Out of 12, the 8 switching states are the same as that of VSI. The other 4 combination of switching states emerges from the concept of ST state. The ST state in ZSI can be added in two ways, single-phase shoot through (SPST) and three-phase shoot through (TPST). In SPST, only one phase leg is used for ST insertion.

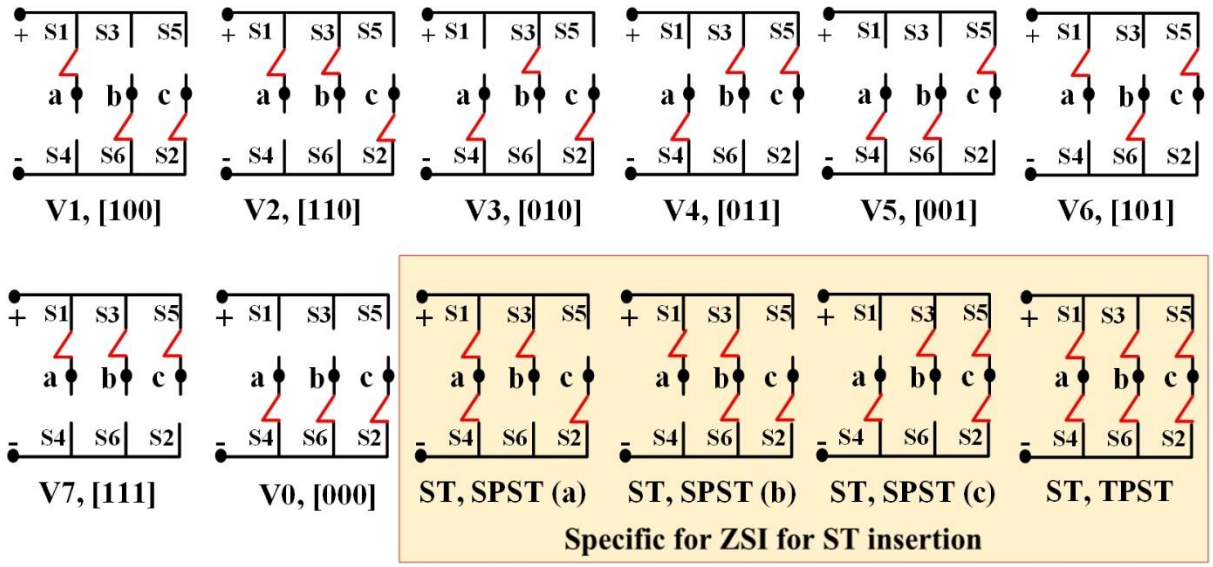


Fig. 1.4. Switching states of VSI and ZSI.

The whole ST current passes through only one phase leg which is the major drawback of SPST. In TPST, all six switches of 2L-ZSI are turned ON. Due to this, the total ST current divides into all three-phase legs. But this implementation causes increased switching transitions per carrier cycle which ultimately affects the switching frequency and losses of the power switches.

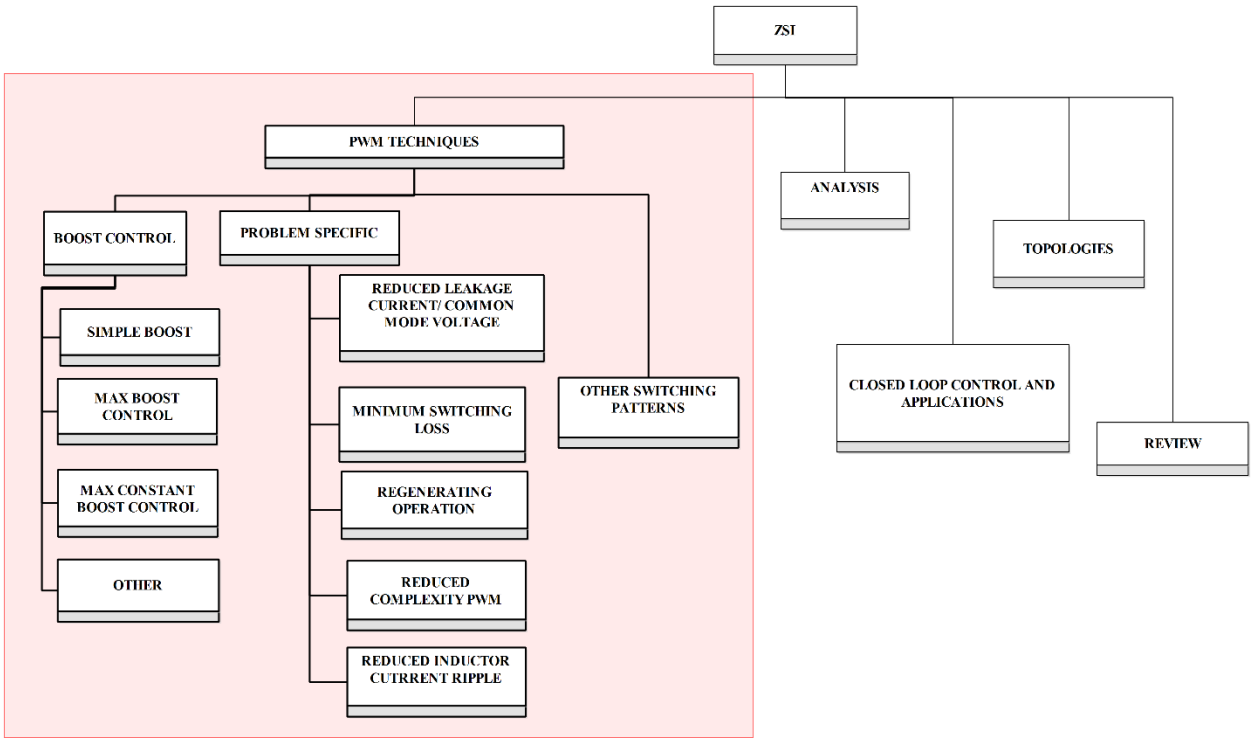


Fig. 1.5. Classification of the research fields of three-phase 2L- ZSI.

Depending upon, used duration of the null states for ST insertion, way of ST insertion, and used switching sequences, the area of PWM techniques of 2L-ZSI has been classified into three main categories in Fig. 1.5. These categories are, boost control techniques, application/problem specific PWM techniques, and other PWM switching patterns.

1.3.1.1. Type of boost control method

Depending upon the utilized duration of null states as ST states, following boost control methods have emerged in ZSI. These are Simple boost control (SBC) [3], Maximum boost control (MBC) [4], Maximum constant boost (MCB) control [5], and Method of [6]. In SBC method [3], two straight lines with magnitude equal to the peak positive and negative value of three-phase reference signals are compared with the triangular signal to embed ST states in the existing null states. This method offers easier implementation of ST state without affecting the time duration of active states. The SBC method is unable to transform the full null interval of a carrier cycle into ST states. So, ref. [4] proposes a MBC method which allows the utilization of the full duration of the null interval as an ST state without affecting active states duration. The MBC method has the advantage of reduced switching transitions per carrier cycle, increased boost factor, and reduced switching stress as compared to SBC. However, MBC has a major drawback of the sixth frequency ripple component of IN inductor current. This drawback causes an increased size of the IN. To avoid this problem, the maximum constant boost (MCB) control method has been proposed in [5]. MCB method uses a fixed duration of ST state per carrier cycle over the full fundamental line cycle period to smooth the IN inductor current. Another attempt to increase the gain of the ZSI has been found in [6]. This method works on decoupling the dependence between the ST duty ratio and modulation index for the application of PV power generation. The voltage gain of ZSI using this technique is lesser than MBC and MCB methods but more than that of SBC. In actual practice, the application of the PWM technique of [6] is limited to a very low modulation index region. It is worth mentioning that these methods (SBC, MBC, MCB, and method of [6]) have been originated with the sine triangle comparison-based method of PWM generation.

1.3.1.2. Problem/Application specific PWM techniques

Some of the PWM techniques of 2L-ZSI have been designed for a particular problem/application. These includes, reduced common-mode voltage/leakage current PWM techniques, minimum

switching frequency/loss PWMs, PWM techniques for regenerating operation, reduced complexity of implementation and reduced IN inductor current ripple PWM techniques.

The common-mode voltage (CMV) is the main cause of the ground leakage current in the transformer-less PV power generation applications. Various attempts have been made in the literature to minimize the magnitude of CMV in 2L-ZSI in [7]–[12]. In ref. [7] various possibilities of switching sequences per carrier cycle have been explored to reduce the magnitude of CMV. Depending upon the utilization of null states, the switching sequences of [7] have been classified into two groups. These include, i) null states replaced by adjacent active vectors and their complement, ii) null states replaced by adjacent active vectors. These techniques limit the CMV magnitude to 0.66Vdc by avoiding the use of one null vector (i.e. [111]). The magnitude of CMV produced by the switching vectors of 2L-VSI has the following order: Null vector ([000], 0) < odd vectors ($0.33V_{dc}$) < even vectors ($0.66V_{dc}$) < null vector ([111], $1V_{dc}$).

All odd and all even switching vectors produces the same CMV magnitude. Therefore, the concept of using only odd (OPWM) and only even (EPWM) switching vectors is proposed in [8] to maintain the magnitude of CMV constant so that the leakage current can be reduced. Ref. [8] also proposes a combination of odd and even switching vectors (OEPWM) which improves the modulation index range of ZSI as compared to the OPWM and EPWM. In addition to OPWM, EPWM, and OEPWM, this paper also proposes the use of one additional diode in series with the return path of the dc source to disconnect the inverter circuit from the PV source during ST states. The same concept of odd and even switching vectors has been analyzed in [9] for the application of AC drives where it has been shown that the odd switching vectors offer a minimum magnitude of CMV (i.e. 0.33Vdc). In [10], two new PWM techniques, active zero state PWM (AZSPWM) and active zero state/odd-even PWM (AZS/OEPWM) have been proposed to reduce the CMV magnitude. As the null vector ([111]) produce the maximum magnitude of CMV, AZSPWM replaces it with the opposite active vectors in a carrier cycle. On the other hand. AZS/OEPWM is the combination of active zero and OEPWM technique. A new modified near state PWM (MNSPWM) proposed in [11] uses switching vectors near to reference vector and its two neighbor vectors in any region of the vector diagram to reduce the CMV magnitude. MNSPWM does not use null vectors and the duration of ST vectors has been selected from the active vectors duration.

The maximum magnitude of CMV using this technique is equal to 0.66Vdc. Ref. [12], reviews various PWM techniques of ZSI based on the magnitude of CMV.

The switching losses plays a critical role in the efficiency of the inverter. The main factors on which the switching losses depends are, switching frequency of the power switches, and switching commutations during the peak forward current. To reduce the switching frequency/losses and to increase efficiency, ref. [13] proposes space vector pulse amplitude modulation (SVPAM). SVPAM method offers up to 87 percent reduction in the switching losses of the voltage fed ZSI operating under the unity power factor load. However, this method requires the sixth fundamental frequency component in the input dc voltage/ current. Therefore a special arrangement in the inverter circuit is required. The basic principle to reduce the switching losses in [14] is to reduce the number of ST states per carrier cycle. A total of 4 ST states have been used here with the MBC technique of voltage boosting. The ST states have been added using single-phase shoot through (SPST) to minimize the number of switching transitions. The improved SVPWM (IPWM) of [15] modifies the switching sequence in such a way that the effective switching frequency of the power switches is reduced to one-third of the carrier frequency. Likewise [14], the SPST scheme with MBC voltage boosting has been used here. Also, only one ST state is applied per half carrier cycle (one sample) to avoid extra switching transition. Ref. [16] proposes two new SVPWM switching techniques, simple boost modified space vector (SBMSV) and maximum boost modified space vector (MBMSV) to reduce the switching losses. These techniques also use the SPST scheme of ST insertion. The effective switching frequency of all power switches is two-third of the carrier frequency using MBMSV. On the other hand, SBMSV offers a reduction in the effective switching frequency of only upper power switches to the two-third of the carrier frequency. These techniques ultimately reduce the switching losses and improve the efficiency of the ZSI. A concept of a time-varying ST duty ratio has been proposed in [17] to reduce the switching/ conduction losses of 2L-ZSI. This technique proposes the injection of the sixth fundamental frequency signal into each phase reference modulation signal so that the instantaneous ST duty ratio and dc bus voltage during the non-peak areas of the output line voltage can be reduced. The switching pattern of this technique inserts two ST states per sample using the TPST scheme. The problem associated with this technique is that it injects ripple components in the dc-link voltage of the inverter.

The existing SVPWM techniques of ZSI may not work appropriately in the regenerating load condition. Therefore, the application area of regenerating load has been studied in [18]. This paper proposes the concept of interlock time between the PWM pulses and also replace the input diode of ZSI via a bidirectional switch to facilitate the bidirectional power flow.

The complexity of the implementation of the PWM techniques is the major concern in the practical operation of the ZSI. One cycle controller has been proposed in [19] to ease the implementation of the PWM technique. The PWM technique of [19] uses a saw-tooth carrier signal to maintain the number switching transitions same as that of VSI. In [20] one-dimensional SVPWM (ODPWM) based on a single-phase modulator has been proposed to simplify the dwell time calculations of the switching vectors. The ODPWM uses the SPST approach of ST insertion with the MBC approach of voltage boosting to reduce the number of switching transitions per carrier cycle.

The size of the IN is an important consideration in ZSI as it affects its portability and cost. The potential of PWM techniques to reduce the size of the IN have been explored in [21], [22] by using conventional switching sequence pattern (0127). The PWM technique of [21] calculates the duration of ST states depending upon the forthcoming NST states within the carrier cycle. The underlying principle of the PWM technique proposed in [22] is to equalize inductor charging and discharging current ripple at every instant so that peak to peak inductor current ripple can be minimized. The inductor current ripple of some existing PWM techniques of ZSI have been compared in the [23].

1.3.1.3. Other PWM switching techniques

There exists some other PWM techniques of 2L-ZSI in which the switching pattern per carrier cycle is different from that of the above discussed boost control methods (SBC, MBC, and MCB) and application/problem specific PWM techniques. The switching patterns of these PWM techniques differ in terms of, the basic pattern of the switching sequence, utilization of null interval for ST state, type of implementation (sine-triangle comparison or SVPWM), number of ST states per carrier cycle, placement of ST states, and boost control method used.

The basic pattern of the switching states means the existing switching sequences of VSI, which has to be modified for the case of ZSI. The conventional switching sequence of VSI is characterized by 0127. In this sequence, 0 and 7 are the null states, and 1, 2 are the active states of

a particular sector. In a discontinuous switching sequence, only one null state (either 0 or 7) is used as per the position of the reference vector. Ref. [24] modifies the conventional continuous and discontinuous PWM switching sequences of VSI by deriving appropriate modulating signals for the case of H-bridge, three-phase, and four-leg ZSI. The sine triangle comparison based technique of gating pulse generation has a major drawback of the complexity of implementation. The complexity arises because it requires several reference signals to be compared with the triangular signal to generate the gating pulses. For example, ref. [3] uses a total of five modulating and two triangular carrier signals to generate the gating pulses of ZSI. Ref. [3] inserts only two ST states per sample. However, total six modulating signals need to be compared with two triangular carrier signals if three ST states per sample are required [24]. Further, if the required modulation index value of 1.15 is desired with sine-triangle based implementation, then a $1/6^{th}$ magnitude third harmonic signal is also required to be injected in sinusoidal modulating signals to achieve the same benefits as offered by SVPWM.

A PWM technique that does not offers full utilization of null interval as ST state causes reduced boost factor/gain of the ZSI. The null state duration of the existing PWM technique of ZSI has been modified in [25] so that it can be fully replaced by the ST states. This technique has been named as a novel modified SVPWM technique.

Ref. [26], [27], and hybrid PWM technique of [28] implement the concept of space vector modulation into ZSI primarily for the applications requiring closed-loop control.

The number of ST states can be maximum three per sample without increasing the total number of switching transitions as compared to the VSI. Also, the ST state in a sample can be placed between the active states as in [24] or can occupy the extreme ends of the sample [3]–[5]. Depending upon the number and positions of ST states per sample and the choice of null state, various other PWM switching patterns have been proposed in [29]–[31]. These includes minimum switching number PWM (MSNPWM) [29], optimized switching type (OST) and Asymmetric optimize type (AOST) [30], and novel SVPWM of [31].

The use of any one boost control method with any combination of switching patterns can quantify the implementation as a novel PWM technique. For example, with the use of the MCB approach of voltage boosting, and three ST states per sample using SPST and SVPWM concept, [32] claims its switching pattern as a novel and named it as improved maximum constant boost control PWM

technique. A review of the existing PWM switching pattern has been presented in [33], [34]. Ref. [33] compares the SBC, MBC, MCB, and two modified SVPWM switching patterns in terms of line voltage/phase current harmonics, dc-link voltage/inductor current ripple, switching stress, and efficiency of ZSI. In [34] some of the existing switching patterns of PWM techniques have been grouped into five main categories. These categories have been named as, ZSVM6, ZSVM4, ZSVM2, ZSVM1-I, and ZSVM-II. All of these categories use the same conventional switching sequence (0127) for ST insertion, but differ in the placement and number of the ST states per sample.

In addition to the conventional continuous (0127) and discontinuous (012, 127) switching sequences, some advanced switching sequences (1012, 0121, 7212, and 2721) also exist in the PWM area of 2L-VSI. The proper combinations of these switching sequences over the fundamental cycle have been categorized into advanced bus clamping PWM (ABCPWM) techniques in [35]. The ABC switching sequences are characterized by the use of double switching of one phase leg and only one null state within a sample. For the case of ZSI, [36] present modification in 1012 and 0121 switching sequence with three ST states per sample. However, [36] does not provide experimental verification of these switching sequences.

Apart from the PWM techniques, the other research areas of 2L-ZSI shown in Fig. 1.5 are steady/dynamic state analysis, closed-loop control techniques, topologies development, and applications.

The steady/dynamic state analysis of ZSI is required to select the appropriate values of passive elements for its stable operation. Such an analysis has been summarized in [37]–[39]. Some hidden operating modes of ZSI have been highlighted in [40] and [41]. The leakage inductance effect in transformer-based ZSI (trans-ZSI) has been presented in [42] and the assessment of harmonics and reliability of ZSI depending upon the modulation strategy has been done in [43].

The closed-loop feedback control becomes necessary in the applications requiring control over input and output voltage and current. Ref. [27], [44]–[51] presents various types of feedback control techniques of ZSI for its successful operation in distributed power generation, electric vehicles, and reactive power control. A review of existing PWM techniques and control methods has been presented in [52].

The researcher's focus in the area of topology development [53]–[57] of 2L-ZSI is to achieve, smooth and continuous input current, increased boost factor, improved performance even during the fault condition, etc. Ref. [58] compares the various types of IN of 2L as well as multilevel buck-boost inverters present in the literature.

There are some other topologies of buck-boost inverters that work on the same principle of ST state insertion and IN [59], [60]. These configurations use active INs instead of passive ones. The active IN contains a power switch in it which helps in ST state generation.

1.4. LITERATURE SURVEY OF THREE LEVEL ZSI (3L-ZSI)

The desire to achieve better output waveform quality at an effective cost has encouraged the researcher to shift their focus towards the multilevel VSIs. Multilevel VSIs has various advantages as compared to their 2L counterpart [61]. These include lower dv/dt of output voltage, reduced input current ripple/ magnitude of common-mode voltage/output filter size, and better output waveform quality even at a lower switching frequency of the power switches. In addition to the above-mentioned advantages, the concept of ZSI inserts the feature of single-stage buck-boost operation in multilevel VSIs.

The standalone 3L buck-boost inverter configuration is a standard dc to ac power conversion units which is popular nowadays because of the improved configurations of 3L-VSIs. The cascaded multilevel configurations of inverters are also popular, but they are mostly used/cost-effective where more than three levels of the output line voltage are desired.

The research area of standalone 3L-ZSI configuration has been classified into various fields as shown in Fig. 1.6. Here, the main attention has been given to the area of PWM techniques and topology of 3L-ZSI.

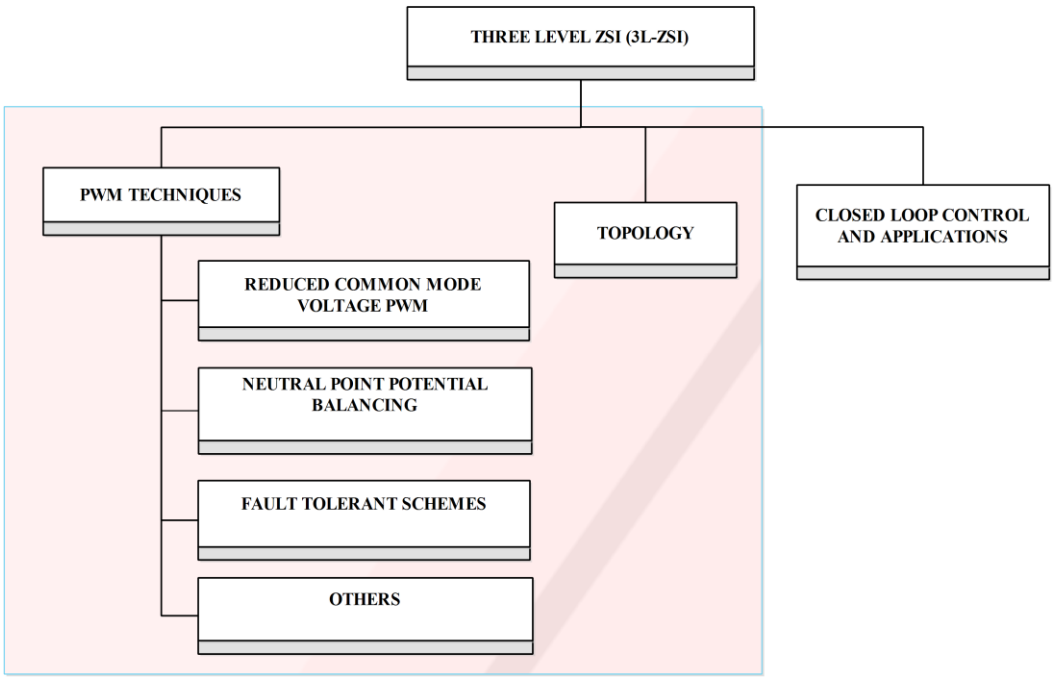


Fig. 1.6. Classification of the research fields of standalone three-phase 3L-ZSI.

1.4.1. Area of PWM techniques of 3L-ZSI

Similar to the 2L-ZSI, the PWM techniques of 3L-ZSI have been designed via modification in the existing switching patterns of 3L-VSI. The switching state selection procedure in 3L-ZSI is more complex as compared to its 2L-ZSI counterpart. The complexity arises due to increase in the number of switching states and operating modes of the inverter circuit. For example, in the case of 2L-VSI, the phase leg has only two possible voltage levels (i.e. +Vdc/2 and –Vdc/2), but in the case of 3L-VSI, each phase leg has total three voltage levels (+Vdc/2, 0, -Vdc/2). Also, there are a total of 27 switching states in 3L-VSI (3 null vectors, 6 large vectors, 6 medium vectors, and 12 small vectors) as compared to 8 in 2L-VSI. Therefore, careful integration of ST state in the switching patterns of 3L-VSI is required for successful operation as 3L-ZSI. Besides, it is worth mentioning that there is redundancy in the switching states of 3L-VSI which can be used to control the various aspects of 3L-ZSI such as neutral point potential balancing, common-mode voltage reduction, etc. The PWM techniques of 3L-ZSI have been classified into four main categories as shown in Fig. 1.6. These categories are reduced common-mode voltage (CMV) PWMs, neutral point potential balancing PWM techniques, fault-tolerant PWMs, and other PWM techniques.

Like 2L-ZSI, several attempts have been made to reduce the CMV magnitude of 3L-ZSI. These attempts includes, origin shifted 60 degree discontinuous PWM of [62], alternate phase opposition disposition (APOD) of [63], [64], reduced CMV PWMs of [65], [66] and space vector PWM (SVPWM) techniques of [67], [68].

The origin shifted 60 degrees PWM of [62] makes the use of the large, medium, and small vectors to realize the reference vector at any position in a 3L hexagon. Only those small vector have been used which offers CMV magnitude equal to one-sixth of the available dc-link voltage. This technique offers the nearest three vector (NTV) switching but causes the large inductor current ripple because of the unbalanced voltage boosting per carrier cycle. In the APOD technique of [63], [64], two vertically disposed out of phase triangular carrier signals have been compared with six reference signals to generate the ST intervals. The resulting switching pattern of this technique makes use of only large, medium, and one null vector. The maximum magnitude of CMV is equal to the one-sixth of the available dc-link voltage. This technique offers a balanced voltage boosting per carrier cycle. However, the pattern of the switching states does not follow the NTV approach which results in degraded output waveform quality. To limit the CMV magnitude to zero, the switching technique of [65], [66] proposes the use of only those switching vectors which offers zero CMV. Therefore, this technique uses only six medium vectors and one zero vector to realize the reference vector. This technique suffers with the limitation of under-utilization of dc bus and the increased number of switching transitions per carrier cycle. The under-utilization of the dc bus occurs due to the non-use of large switching vectors. Ref. [67], [68] offers SVPWM technique based implementation of the APOD switching technique. The difference between SVPWM of [67], [68], and APOD of [63] is that the former uses only one phase leg for ST insertion and the later uses a combination of the two-phase legs for the insertion of ST state.

Another main problem associated with the 3L inverters is the neutral point potential unbalance. This problem has been studied in detail in [69] for the case of 3L-VSI. The switching pattern of the PWM technique is always designed is such a way that input dc-link capacitors remain balanced during ideal operating conditions. However, due to any abnormal situation, such as semiconductor failure or unbalanced loading conditions, the input dc-link potential (at neutral point) deviates from a balanced position. Therefore, several closed-loop control techniques have been proposed in [70]–[72] to tackle this problem. These control techniques adjust the time duration of small switching

vectors for the controlled charging/discharging of the upper and lower capacitor of the input dc source.

As a preventive measure, the possibilities of successful operation during fault condition has been studied in [73]–[75].

In addition to the application-specific PWM techniques, there exist some other PWM techniques of 3L-ZSI [62] [76], [77]. These PWM techniques differ from each other in terms of, switching patterns, type of ST state (upper-lower ST or full ST), type of implementation (sine triangle or space vector PWM), etc. The PWM techniques proposed in [62] are, continuous edge insertion (CEI), continuously modified reference (CMR), and 60 degree discontinuous. The CEI uses a carrier-based implementation of ST states using 5 reference signals and two triangular carrier signals. This technique utilizes only small vectors duration for the insertion of ST states and place the ST states at the extreme ends of a sample. The problem associated with this technique is that it causes eight number of switching transitions per sample over a complete fundamental period. To limit the number of switching transitions per carrier cycle to six, the CMR PWM technique has been proposed in the same publication. The CMR PWM uses six reference signals along with two triangular carrier signals for the generation of ST states. This technique offers six number of switching transitions per sample which is the same as that of 3L-VSI operating under continuous PWM technique. CMR PWM technique uses the time duration of active vectors as well as the small vectors for the insertion of ST state. Due to this, the complexity of implementation arises in a situation when the required ST time duration is more than that of available active vector time duration in a particular sample. The 60 degree discontinuous PWM of [62] uses only one equivalent null state in a carrier cycle to achieve phase leg clamping so that the number of switching transitions can be further minimized to four per sample. This technique suffers the major drawback of unbalance voltage boosting because only one IN is shorted for a particular duration of fundamental period. The carrier-based PWM technique of [76] uses three triangular carrier signals for the generation of switching states of 3L neutral point clamped (NPC) ZSI. The comparison of three sinusoidal signals with two in-phase triangular carrier signal is used for the generation of NST states. The frequency of the third triangular carrier is double as compared to the in-phase triangular carrier signals. This third carrier signal is compared with a straight line signal to generate the ST states. The magnitude of the straight line signal decides the ST duty ratio.

Besides, in-phase triangular carrier signals have a provision of level shifting as per the magnitude of the straight line signal. Therefore, this technique is named as level shifted in-phase disposition PWM with maximum constant boost control (LS-in phase PWM with MCB). The space vector technique based implementation of ST state can be found in [77]. This switching technique simplifies the 3L vector diagram using the concept of equivalent 2L vector diagram approach of [78]. The duration of only equivalent null vectors has been used here for the insertion of ST states.

1.4.2. Area of topologies of 3L-ZSI

The improvement in the conventional topologies of 3L-ZSI is required in various aspects such as the number of components, boost factor, switching stress, input current, and conduction/switching losses, etc. To reduce the number of components, two new configurations of cascaded 3L-ZSI have been proposed in [79]. Depending upon the type of cascading structure, these are named as dc-link cascaded and dual ZSI. These configurations eliminate the requirement of clamping diodes as used in NPC ZSI. A transformer-based IN topologies, trans, and flipped trans 3L NPC ZSI has been proposed in [80] to improve the input-output voltage gain and to reduce the switching stress across the power switches. By adjusting the turns ratio of the transformer, the input-output gain of the inverter can be varied in these configurations. In ref. [81], the use of capacitors has been proposed in conjunction with the clamping diodes of NPC ZSI to automatically balance the neutral point capacitor voltages. The topology is named as hybrid clamped ZSI (Z-HC).

The IN has been again modified in [82]–[84] to improve the performance of 3L-ZSI. In [82] a 3L q-ZSI topology using NPC configuration has been proposed to reduce the IN capacitor voltage stress without affecting the boost factor. An improved q-ZSI proposed in [83] offers a higher boost factor, but, at the cost of the increased number of IN components. This configuration uses 8 inductors, 10 capacitors, 4 diodes as compared to 4 inductors, 4 capacitors, and 2 diodes in 3L q-ZSI topology of [82]. A modified Z source IN-based 3L NPC ZSI has been proposed in [84] to increase the boost factor. This configuration offers a double boost factor as compared to the conventional 3L-ZSI of [62] using just 2 inductors, 4 capacitors (including dc-link split capacitors), and 3 diodes. Modified Z source IN based ZSI offers reduced switching stress across the power switches because in this topology higher inverter gain can be achieved at the upper modulation index region.

Ref. [85], [86] studies the closed-loop control application of 3L-ZSI. Various other IN-based buck-boost 3L inverter topologies can be seen in [87]–[91]. The objective of these topologies is, to improve the performance of the inverter in any possible way.

It has been noticed from the above-discussed topologies that the primary attention has been given to the IN modification [80]–[84], [87]–[91] to improve the performance of 3L-ZSI. Means, mostly NPC configuration of 3L-VSI has been used in combination with the IN. Recently it has been found that, in low to medium power applications, the three-level T-type configuration [92], [93] is beneficial as compared to the NPC VSI in terms of efficiency and number of components count. In T-type configuration, only one switch per phase leg is ON during power flow to load as compared to the two in NPC ZSI. Also, the T-type configuration eliminates the use of clamping diodes. To achieve these advantages, the T-type configuration of 3L-VSI has been successfully integrated into the concept of ZSI in [67], [68], [70].

1.5. RESEARCH GAPS/ PROPOSED IMPROVEMENTS

1.5.1. Two-level ZSI (2L-ZSI)

It has been noticed from the literature survey of the PWM techniques of 2L-ZSI [3]-[36] that the several combinations of switching patterns exist. The conventional continuous and discontinuous switching sequence (0127, 012, 721) of VSI has been explored almost up to the full extent in ZSI. On the other hand, the advanced bus clamping (ABC) switching sequence (1012, 0121, 7212, and 2721) has been rarely studied. These switching sequences are a type of discontinuous PWMs (use only one null state for a particular region) and do not have equivalence with the sine triangle comparison-based approach. The modification in the ABC switching sequence for the case of ZSI has been found [36]. These switching sequences have the potential to improve the performance of ZSI in various aspects. For example, designing a PWM technique to, reduce the IN inductor current ripple, reduce input current ripple, reduce magnitude of CMV, improve output waveform quality, and reduce switching/conduction losses of ZSI, etc. But, it requires careful integration of these switching sequences into ZSI to achieve these goals. It can be said that the area of ABC switching sequences can be explored for various possibilities to improve the performance of ZSI.

1.5.2. Three-level ZSI (3L-ZSI)

1.5.2.1. Area of PWM techniques

The commonly used PWM techniques of 3L-ZSI have the following main problems:

- increased number of switching transitions as compared to its VSI counterpart as in continuous edge insertion of [62] and SVPWM of [67], [68]
- complexity of implementation of ST state as in continuous modified reference PWM of [62]
- degraded output waveform quality as in APOD of [63], reduced CMV technique of [64], and SVPWM of [67], [68]

It is desired that the PWM techniques of 3L-ZSI should offer better output waveform quality with reduced switching transitions and ease of implementation.
Besides, the particular problems associated with existing reduced CMV PWM techniques of 3L-ZSI are:

- the unbalanced voltage boosting with the increased size of IN [62]
- under-utilization of dc bus potential [65],[66]
- increased number of switching transitions per carrier cycle [66], [67], [68]
- degraded output waveform quality and complexity of implementation [63], [64], [67], [68]

The reduced CMV PWM techniques should be free from the above-mentioned problem as much as possible. Also, the switching vector diagram of 3L-ZSI is far more different as compared to that of 2L-ZSI. Still, the boost control methods of 2L-ZSI are being utilized in the 3L-ZSI. There can be a possibility that the switching state diagram of 3L-ZSI gives a new boost control method which can improve its performance.

1.5.2.2. Area of topologies of 3L-ZSI

For the improvement in the performance of 3L-ZSI, there are two options available from the topology aspect. The first option is the improvement in the IN and the second is the inverter circuitry. From the inverter circuitry point of view, there are three main types of configurations of 3L-ZSI. These are, cascaded configurations [79], neutral point clamped (NPC) ZSI [62], and T-type configuration [68]. Each of these configurations has its own merits/demerits. The topologies which offers better overall performance as compared to the cascaded, NPC type, and T-type are

always welcome to operate with the IN. The controlled diode bridge clamped (CDBC) configuration of 3L-VSI [94] may be analyzed in this aspect.

1.6. OBJECTIVES

The following objectives have been proposed in this research work. These objectives cover the PWM area of 2L-ZSI as well as the PWM and topology area of 3L-ZSI.

- Design of high-performance multilevel converter configuration with improved power quality features using less number of component count
- Implementation of the ZSI concept in multilevel converter configuration
- Implementation of advanced space vector based PWM sequence in multilevel ZSI
- Hardware implementation of converter configuration
- Closed-loop feedback control design and complete parameter selection for isolated/grid-connected PV.

1.7. ORGANISATION OF THESIS

This research work is organized as follows. In chapter 2 of this work, first, the principle of operation of 2L-ZSI and the conventional concept of SVPWM generation has been discussed in brief. Then, one of the existing SVPWM technique (ZSVM6) of ZSI has been analyzed based on the pattern of switching states and the IN inductor current ripple under MCB approach of voltage boosting. After that, ABC switching sequences have been selected to design a new PWM technique (ABC4_MCB) of ZSI. The switching pattern of the proposed ABC4_MCB technique has been designed particularly for the reduction in the IN inductor current ripple. Finally, the proposed and the existing PWM technique have been compared based on the various important aspects and the result section proves the theoretical findings.

In chapter 3, first, the controlled diode bridge clamped (CDBC) VSI has been discussed in comparison with the NPC and T-type configurations. Then, the concept of ZSI has been implemented in the CDBC inverter configuration followed by explanation of its principle of operation, operating modes, and type of ST states. After that, a new SVPWM switching pattern has been proposed to optimize the switching frequency of the power switches. The proposed SVPWM switching pattern has been compared with the conventional SVPWM switching pattern

in terms of various important aspects. The result section validates the operation of CDBC ZSI and its PWM technique.

For the further improvement in the performance of 3L-ZSI, chapter 4 proposes a modification in the conventional SVPWM switching state diagram. Based on the modified SVPWM switching state diagram, an improved maximum boost control (IMBC) technique of voltage boosting has been proposed. Also, two new reduced CMV switching patterns have been discussed in this chapter. The proposed switching patterns have been named as ZSVM_1TI and ZSVM_2TI PWM techniques depending upon the number of ST states per sample. Then, proposed PWM techniques are compared with the existing PWM techniques of 3L-ZSI based on, the magnitude and slew rate of CMV, available ST duty ratio, size of IN, switching frequency of the IN, inductor current ripple, line voltage waveform quality, and power loss distribution.

In chapter 5, a closed-loop feedback control technique of output voltage control has been implemented in 3L-CDBC ZSI considering its application in the islanded mode of PV power generation.

Finally, the overall conclusion and the future scope of this research work has been summarized in chapter 6.

CHAPTER 2. ADVANCED BUS CLAMPING SWITCHING SEQUENCES FOR ZSI

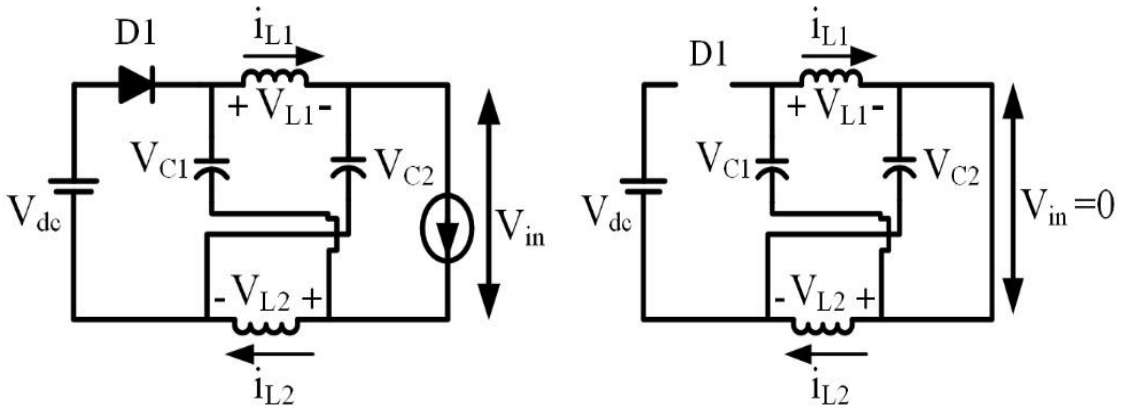
2.1. INTRODUCTION

This chapter explores the potential of the advanced bus clamping (ABC) switching sequences for the application of reduction in the impedance network (IN) inductor current ripple of ZSI. Based on the ABC switching sequences and maximum constant boost (MCB) control method of voltage boosting, a new PWM technique 'ABC4_MCB' is proposed in this chapter. It is claimed here that the proposed ABC4_MCB PWM technique offers a 34 percent reduction in the IN inductor current ripple as compared to one of the existing technique (ZSVM6) under the same boost control method and at equal average switching frequency of the power switches. To validate these claims, the following information has been provided in this chapter:

- A brief review of the principle of operation of ZSI, concept of SVPWM, and the modification required in the conventional SVPWM for the successful operation of ZSI
- The analysis of the switching pattern and IN inductor current ripple of one of the existing technique 'ZSVM6' of ZSI operating under the MCB control method of voltage boosting
- The introduction to the proposed design of the ABC4_MCB technique of ZSI and its IN inductor current ripple analysis
- Comparison of ZSVM6_MCB and ABC4_MCB in terms of various parameters.

2.2. REVIEW OF TWO LEVEL ZSI (2L-ZSI) PRINCIPLE

The conventional configuration of the 2L-ZSI has been already discussed in Fig. 1.3 of chapter 1. The switching states of ZSI have two broad categories, non-shoot through (NST) and shoot through (ST) state. The NST category contains all the switching states of VSI. The states which create the short circuit path across the IN have been grouped into the ST state category. The equivalent circuit diagrams of ZSI during NST and ST state are shown in Fig. 2.1(a) and Fig. 2.1(b), respectively. The formulas obtained after steady-state analysis of ZSI [3] in the NST and ST state have been summarized in Table 2.1.



(a) (b)

Fig. 2.1. Equivalent circuit diagrams of 2L-ZSI during, (a) NST state (b) ST state.

Table 2.1. Expressions for the conventional configuration of 2L-ZSI

Parameters	Symbol	Expression	Remark
ST duty ratio	D	$\frac{T_{sh}}{T_s}$	$T_s = T_{sh} + T_{nsh}$ T_s is the duration of one sample
Boost factor	B	$\frac{1}{1-2D}$	$B \geq 1$
Voltage across the capacitors	V_C	$\left(\frac{1-D}{1-2D}\right)V_{dc}$	V_{dc} is the input dc-source voltage; $V_{C1} = V_{C2} = V_C$
Peak dc-link voltage	$\widehat{V_{in}}$	BV_{dc}	-
Peak line-line rms voltage	V_{ab}	$\frac{\sqrt{3}}{2\sqrt{2}}.M.BV_{dc}$	M is the modulation index
Reverse voltage across diode during ST state	V_D	BV_{dc}	-
Voltage stress across power switches	V_s	$B.V_{dc}$	-

2.3. CONCEPT OF SPACE VECTOR PWM (SVPWM)

The SVPWM concept works directly on the reference line voltage signal for the generation of gating pulses of the inverter switches. As compared to the sine triangle comparison-based approach, the SVPWM offers flexibility in the selection of switching state and easier implementation on the digital platform. Fig. 2.2 shows the eight voltage vectors produced by 2L-VSI. The space vector plane is partitioned into six sectors by active vectors each of unity length normalized w.r.t dc bus voltage. The two null vectors are placed at the center of the hexagon. Depending on the sampling frequency, numbers of samples of revolving reference vector (V_{ref}) each of duration T_s, are taken over a fundamental period (50Hz). One sample is equivalent to the half carrier cycle. So, a full carrier cycle has a duration of $2T_s$.

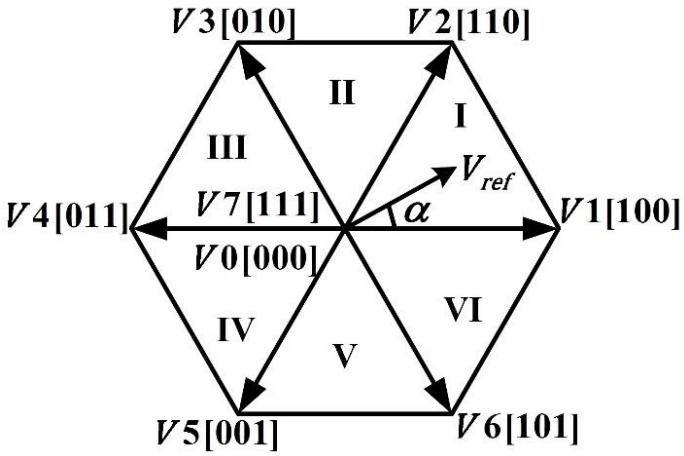


Fig. 2.2. Space vector switching state diagram of 2L-VSI.

2.3.1. Calculation of dwell time of switching vectors

As per the position of the reference vector in a sector, the inverter is switched between different switching vectors (V0 to V7) within a sample. For example, in the sector I of Fig. 2.2, the reference vector can be realized using voltage vectors V1, V2, V7, V0 along with their calculated dwell time durations. The expressions of the dwell time duration of the switching vectors in sector I can be written as [35]:

$$\left\{\begin{array}{c} T_1 = \frac{V_{ref}}{V_{dc}}.\frac{\sin(\pi/3-\alpha)}{\sin(\pi/3)}.T_s \\ T_2 = \frac{V_{ref}}{V_{dc}}.\frac{\sin(\alpha)}{\sin(\pi/3)}.T_s \\ T_z = T_s - T_1 - T_2 \end{array}\right\} \quad (2.1)$$

Total active state duration in one sample ($T_{active} = T_1 + T_2$) is:

$$T_{active} = \frac{\sqrt{3}}{2}.M.[\cos(\pi/6-\alpha)].T_s\ ; \quad 0 \le \alpha \le \pi/3 \quad (2.2)$$

Total null state duration (T_z) of a sample is:

$$T_z = \left(1 - \frac{\sqrt{3}}{2}.M.[\cos(\pi/6-\alpha)]\right).T_s \quad (2.3)$$

Modulation index 'M' is defined as [95]:

$$M = \frac{4}{3}\left(\frac{V_{ref}}{V_{dc}}\right) \quad (2.4)$$

2.3.2. SVPWM for ZSI

Duration of null vector time (T_z) is reformed for the execution of SVPWM in ZSI. Since both, null states and ST states produce zero line voltage, they can be exchanged partially or fully by each other [3]. Each ST insertion method, simple boost control (SBC), maximum boost control (MBC), and maximum constant boost (MCB) control has a particular relationship between the modulation index (M) and the ST duty ratio (D).

In the case of SBC, the modulation index is related to the ST duty ratio as

$$D = \frac{T_{sh}}{T_s} = 1 - M \quad (2.5)$$

The MBC method replaces the complete null state duration with the ST states. The expression for the average ST duty ratio for the MBC method can be found by integrating equation (2.3) for one sector as:

$$\frac{T_z}{T_s} = \frac{T_{sh}}{T_s} = \frac{1}{\pi/3}\int_0^{\pi/3}\left(1 - \frac{\sqrt{3}}{2}M[\cos(\pi/6-\alpha)]\right) \Rightarrow \frac{T_{sh}}{T_s} = \frac{2\pi - 3\sqrt{3}M}{2\pi} \quad (2.6)$$

As the null interval changes six times the fundamental frequency, the problem of lower order ripple components in the IN inductor current appears as the major drawback of MBC method.

To eliminate this drawback, MCB control method has been proposed. The principle behind the operation of MCB method is as follows. The analysis of the space vector diagram (Fig. 2.2) implies that for any particular magnitude of the reference vector ($\leq 0.866V_{dc}$), the null interval is minimum for a sample located at the center of any sector. The duration of the null interval at this position of the reference vector gives the maximum reference limit of ST state duration which can be used throughout the fundamental cycle to maximize the boost factor with ripple-free IN inductor current.

Putting $\alpha = \pi/6$ in equation (2.3) and assigning the whole expression to T_{zsc}, we get:

$$T_{zsc} = \left(1 - \frac{\sqrt{3}}{2}.M\right).T_s \tag{2.7}$$

Here T_{zsc} is the null state duration at center of any sector, or it can be said that T_{zsc} is the reference duration of ST state for each sample in a hexagon. The below equation must follow by each sample after insertion of ST state:

$$T_z = T_{zsx} + T_{zsc} \tag{2.8}$$

T_{zsx} is the remaining duration of the null state.

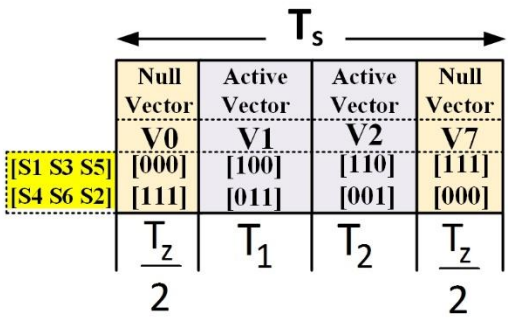
Normally, a generalized numbering is assigned to each switching state of a sector to ease the process of switching state selection. This is shown in Table 2.2.

Table 2.2. Generalized numbering of switching states for each sector

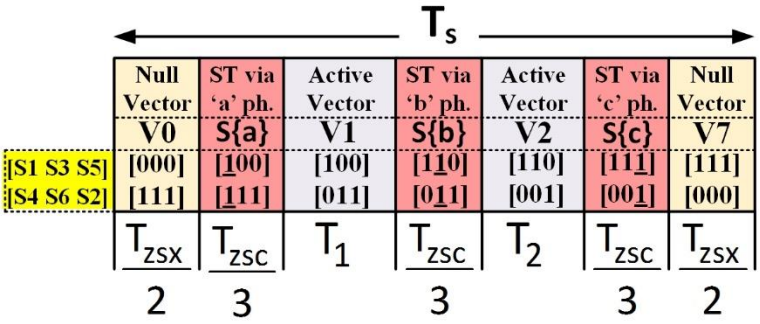
Sector	0 (null)	1 (active)	2 (active)	7 (null)
I	[000111]	[100011]	[110001]	[111000]
II		[010101]	[110001]	
III		[010101]	[011100]	
IV		[001110]	[011100]	
V		[001110]	[101010]	
VI		[100011]	[101010]	

2.4. CONVENTIONAL SVPWM OF ZSI

The conventional SVPWM technique 'ZSVM6' of [34] has been renamed here as ZSVM6_MCB under the MCB approach of voltage boosting. The conventional switching state pattern of VSI and ZSVM6_MCB technique of ZSI is shown in Fig. 2.3. One switching cycle comprises of two samples each of duration(T_s).



(a)



(b)

Fig. 2.3. Switching state pattern in the sector I of the hexagon (a) conventional pattern of VSI, (b) ZSVM6_MCB technique of ZSI.

As indicated in Fig. 2.3(b), the total T_{zsc} duration is split into three equal intervals each of $T_{zsc}/3$. Then each interval of $T_{zsc}/3$ is placed in every state transition within a sample. The remaining duration of the null state T_{zsx} is broken into two parts and applied at the starting and ending boundary of the sample. Now we have an equal duration of null plus ST state at the starting and ending boundary of each sample which offers optimal harmonics performance [96]. The MCB method offers a unity boost when the reference vector has a magnitude of $0.866V_{dc}$. Note that, any particular value of the total ST duration (T_{zsc}) per sample, which is less than the null state duration T_z of the central sample of a sector can be taken for constant boost control. But, for the

maximum constant boost, total ST duration per sample must be equal to the null state duration of the central sample of a sector.

It has been also noticed from Fig. 2.3(b) that, each switch has one transition per sample (either 0 to 1 or 1 to 0). Therefore, for 'N' number of samples over hexagon, there will be 'N' number of switching transitions in each switch. This means each switch has N/2 switching per line cycle. Two switching transitions (1-0-1) are termed as one complete switching. Mathematically, it can be written as:

$$F_{sw} = \frac{1}{2.T_s} \tag{2.9}$$

F_{sw} is the switching frequency of the power switches using the ZSVM6_MCB technique.

2.4.1. Calculation of maximum instantaneous inductor current ripple

Fig. 2.4 shows the switching sequence and the corresponding IN inductor current behavior in a sample using the ZSVM6_MCB technique. The calculation of the IN inductor current ripple components has been provided in equation (2.10). These inductor current ripple components are plotted in Fig. 2.5 with the parameters given in the figure caption. It is clear from Fig. 2.5 that the maximum instantaneous inductor current ripple is because of the discharging time of the inductor which is given by component 'c' and 'e' of equation (2.10). Referring to Fig. 2.2, before 30 degrees in a sector, the time (T_1) is more than (T_2) which makes 'c' to be greater than other components and after 30 degree (T_2) is more than (T_1) resulting 'e' to be greater than all other components.

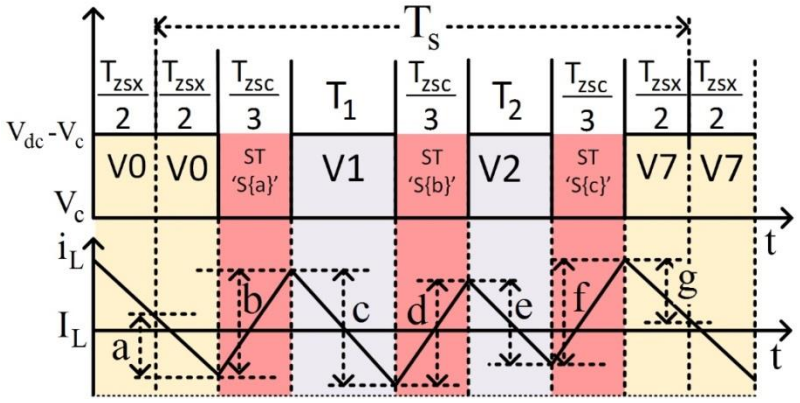


Fig. 2.4. Switching sequence and the instantaneous inductor current ripple components using the ZSVM6_MCB technique.

$$\left\{\begin{array}{c} a = g = \frac{V_{dc} - V_C}{L}\left(\frac{T_{zsx}}{2}\right) = \frac{V_{dc} - V_C}{L}\left(\frac{K}{2}\right)\left(1 - \cos\left(\pi/6 - \alpha\right)\right) \\ b = d = f = \frac{V_C}{L}\left(\frac{T_{zsc}}{3}\right) = \frac{V_C}{L}\left(\frac{1}{3}\right)(T_s - K) \\ c = \frac{V_{dc} - V_C}{L}(T_1) = \frac{V_{dc} - V_C}{L}\left(K.\sin\left(\pi/3 - \alpha\right)\right) \\ e = \frac{V_{dc} - V_C}{L}(T_2) = \frac{V_{dc} - V_C}{L}(K.\sin(\alpha)) \\ \text{Here } K = \frac{\sqrt{3}}{2}.M.T_s;\ V_C = \left(\frac{1 - D}{1 - 2D}\right)V_{dc} \end{array}\right\} \quad (2.10)$$

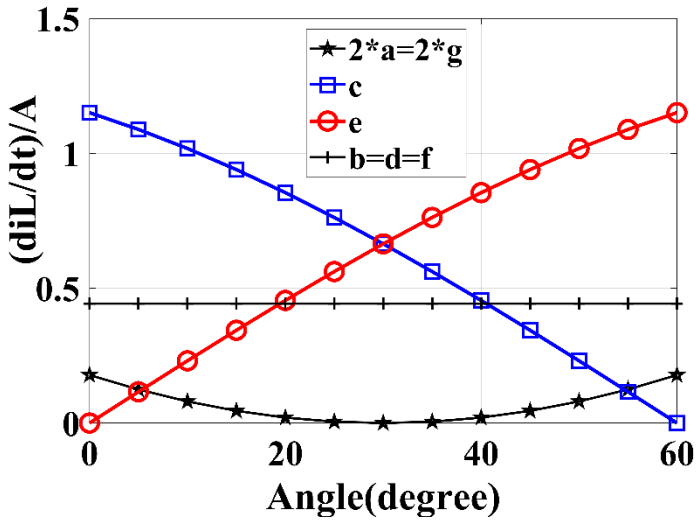


Fig. 2.5. Instantaneous values of the inductor current ripple components (given in equation (2.10) in the sector I using ZSVM6_MCB technique at, $M = 0.95; D = 0.177;\ V_{dc} = 60V;\ T_s = 196usec.; L = 2mH.$

The maximum instantaneous inductor current ripple in a sector can be expressed as:

$$\begin{aligned} i_{ZSVM6\_MCB} &= \text{maximum of } (2|a|, |b|, |c|, |d|, |e|, |f|, 2|g|) \\ &= \left\{\begin{array}{l} |c|;\ 0 \le \theta < \pi/6 \\ |e|; \pi/6 \le \theta < \pi/3 \end{array}\right\} \end{aligned} \quad (2.11)$$

The average value of the maximum instantaneous inductor current ripple components (i.e. ‘c’ and ‘e’) over one sector can be expressed as:

$$\bar{I}_{ZSVM6\_MCB} = \frac{\int_0^{\pi/6}|c|.\,dt + \int_{\pi/6}^{\pi/3}|e|.\,dt}{\pi/3} = 0.7K\left(\frac{V_{dc} - V_C}{L}\right) \quad (2.12)$$

Over the whole sector, the value of maximum instantaneous inductor current ripple is the maximum value of 'c' or 'e'. Putting $\theta = 0°$ in the equation of 'c' (equation (2.10)), we get:

$$I_{ZSVM6\_MCB(max)} = \left|\left(\frac{V_{dc} - V_C}{L}\right).K.\left(\sin(\pi/3)\right)\right| \quad (2.13)$$

The relationship between the angle(α), D, and maximum instantaneous inductor current ripple component (c and e of Fig. 2.5) is shown in Fig. 2.6. It is evident from Fig. 2.6 that, for any value of the ST duty ratio in the range 0 to 0.48, the maximum instantaneous inductor current ripple is minimum at the center and maximum at the two boundaries of the sector.

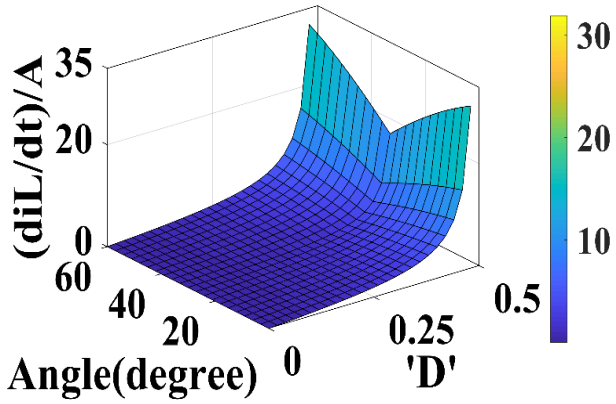


Fig. 2.6. Relationship between angle (α), 'D' and maximum instantaneous inductor current ripple using the ZSVM6_MCB technique.

2.5. PROPOSED 'ABC4_MCB' PWM TECHNIQUE OF ZSI

The advanced bus clamping switching sequences [35] are characterized by the division of active vector time into two parts and the use of only one null vector within a sample. There are four such types of switching sequences. These are 0121, 7212, 1012, and 2721. The proposed PWM technique selects 0121 and 7212 switching sequences and assign appropriate region of the vector diagram to them to reduce the IN inductor current ripple of ZSI. The proposed technique implements four ST intervals per sample using the MCB approach of voltage boosting, therefore it is named as ABC4_MCB technique.

2.5.1. Selection of region

In the ABC4_MCB technique, each sector is partitioned into two halves, and then the switching sequences has been assigned according to the conditions mentioned in Fig. 2.3.

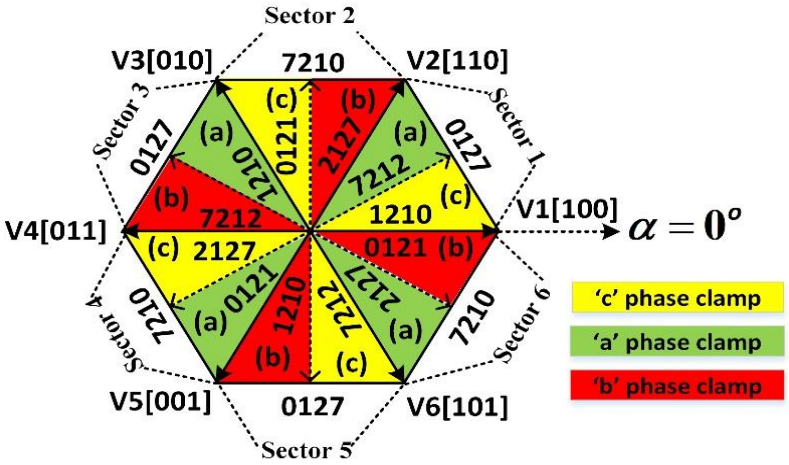


Fig. 2.7. Implementation details of the ABC4_MCB technique.

Table 2.3. Conditions to maintain symmetrical output voltage waveform and to avoid uneven power distribution

Sr.	Prescribed conditions
1.	In every sector, there must be an odd number of samples before and after the central sample. The central sample is the null-vector changing sample. It is placed at the exact middle of every sector to facilitate the transition between one null vector to another null vector.
2.	No sample is taken at the sector boundary (i.e. at $0, \pi/3, 2\pi/3, \pi, 4\pi/3, 5\pi/3$ radian)
3.	The first sample of the odd sector and even sector must start with 1210 and 2127 switching sequences, respectively.
4.	Null vectors are changing alternatively every 60-degree interval.
5.	All samples are evenly spaced over a 360-degree interval.
6.	The total number of ST states should be evenly distributed in all three-phase legs and the duration of each ST state must be same.

Fig. 2.7 shows the specific region of each switching sequence in the vector diagram. This type of implementation causes the clamping of each phase leg to the positive/negative dc bus for the one-

third period of the fundamental cycle. To ease the process of switching states selection, the generalized numbering of the switching vectors given in Table 2.2 has been used. The conditions mentioned in Fig. 2.3 have been used to maintain half-wave/three-phase symmetry, synchronization in the output voltage waveforms, and to avoid uneven power distribution in the inverter switches.

2.5.2. Implementation of ST state

From Fig. 2.7, it is clear that there are three types of switching sequences in each sector (i.e. 1210/0121, 0127/7210, and 2127/7212). For sector I, Fig. 2.8 (a), (b) and (c) shows the pattern of switching states for the samples having 1210, 7212, and 0127 switching sequences, respectively.

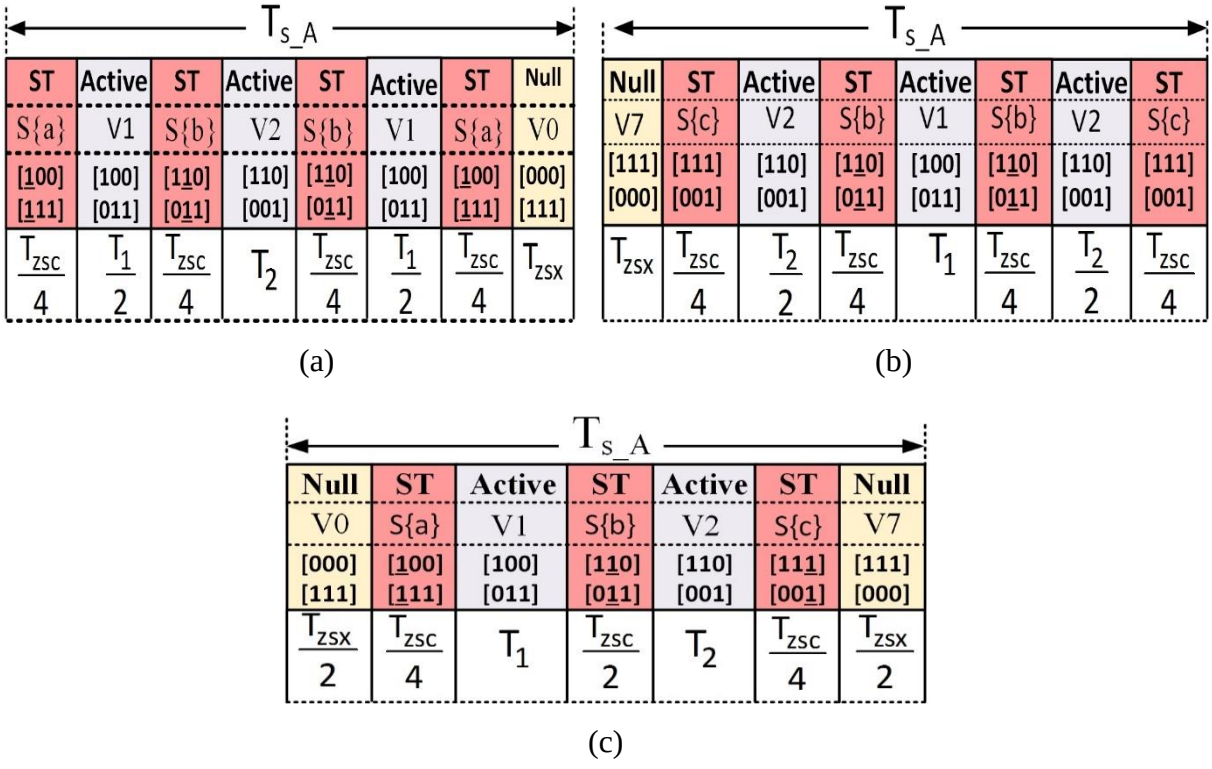


Fig. 2.8. Switching state pattern of ABC4_MCB technique for the samples of sector I having switching sequence (a) 1210, (b) 7212, (c) 0127 (central sample).

Four number of ST states have been added in the samples having 1210 and 7212 switching sequences. The total ST time has been divided into four equal parts each of duration $(T_{zsc}/4)$ and placed at an appropriate position within a sample as shown in Fig. 2.8 (a) and (b). These switching patterns causes seven number of switching transitions per sample. The central or null vector

changing sample has been realized using the 0127 switching sequence. The switching pattern of the central sample (Fig. 2.8 (c)) is the same as that of the ZSVM6_MCB technique except for the allocated duration of each ST state. The central sample of each sector causes only six switching transitions per sample.

2.5.3. Calculation of the average switching frequency

As discussed in section 2.4, for 'N' number of samples over full hexagon, there will be 'N' number of switching transitions in each switch using ZSVM6_MCB. Therefore, if 17*6=102 samples are selected over hexagon for ZSVM6_MCB, then each switch offers a total 102 switching transitions. This means each switch has 51 switching over line cycle. So, to have the same average switching frequency, the total number of transitions in each switch must be equal to 102 using the ABC4_MCB technique also. Keeping this condition in mind, the best possible number of samples per sector which offers the total number of transitions nearer to 102 comes out to be 15 for ABC4_MCB.

Table 2.4. Selection of the number of samples per sector for ABC4_MCB

Choice of number of samples per sector	Possibility (as per the conditions mentioned in Table 2.3)	Total no. of switching transition over line cycle	Best nearer to total 102 transitions over line cycle
11	Yes (5+1+5)	76	no
12,13,14	No		
15	Yes (7+1+7)	104	yes
16,17,18,	No		
19	Yes (9+1+9)	114	no

Table 2.4 has been given to illustrate why 15 samples per sector are the best choice using the ABC4_MCB technique. However, 15 samples per sector offer a total of 104 transitions in each switch which is 2 more than that of ZSVM6_MCB, but exact 102 transitions using the "ABC4_MCB" technique is not possible considering the conditions of symmetry mentioned in

Table 2.3. Therefore, 15 samples per sector and a total of 15*6=90 samples over the fundamental line cycle has been taken.

Now, the time duration of each of 90 samples to have a fixed fundamental cycle duration of 0.02sec. (50Hz) is calculated as:

$$90 \times T_{s\_A} = 0.02(50\text{Hz}) \Longrightarrow T_{s\_A} = 0.0002222\text{sec.}$$

To restrict sample time (T_{s_A}) up to six decimation places, 90 samples each of 222usec. have been taken in the proposed ABC4_MCB technique. The ratio of the sample time duration of ABC4_MCB and ZSVM6_MCB can be written as:

$$\frac{T_{s\_A}}{T_s} = \frac{222\text{usec.}}{196\text{usec.}} = 1.132 \qquad (2.14)$$

2.5.4. Calculation of maximum instantaneous inductor current ripple

Fig. 2.9 and Fig. 2.10 show the switching states and their corresponding inductor current ripple components for the sequences 1210 and 7212, respectively. Calculation of the ripple components of Fig. 2.9 and Fig. 2.10 is given in equation (2.15) and equation (2.16), respectively.

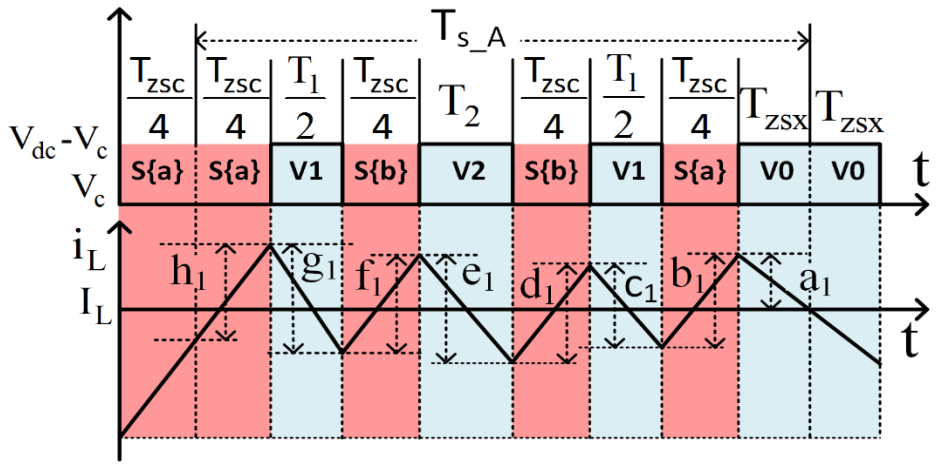


Fig. 2.9. Graphical representation of the switching pattern and inductor current ripple components of 1210 switching sequence.

$$\begin{cases} h_1 = f_1 = d_1 = b_1 = \frac{V_C}{L}\left(\frac{T_{zsc}}{4}\right) = \frac{V_C}{L}\left(\frac{1}{4}\right)(T_{s_A} - K_A) \\ g_1 = c_1 = \frac{V_{dc}-V_C}{L}\left(\frac{T_1}{2}\right) = \frac{V_{dc}-V_C}{L}\left(\frac{K_A}{2}.\sin\left(\pi/3 - \alpha\right)\right) \\ e_1 = \frac{V_{dc}-V_C}{L}(T_2) = \frac{V_{dc}-V_C}{L}(K_A.\sin(\alpha)) \\ a_1 = \frac{V_{dc}-V_C}{L}(T_{zsx}) = \frac{V_{dc}-V_C}{L}.(K_A).\left(1 - \cos\left(\pi/6 - \alpha\right)\right) \\ \text{here } K_A = \frac{\sqrt{3}}{2}.M.T_{s_A};\ V_C = \left(\frac{1-D}{1-2D}\right)V_{dc}; \\ T_{s_A} = 1.132 \times T_s \text{ (from equation (2.14))} \end{cases} \quad (2.15)$$

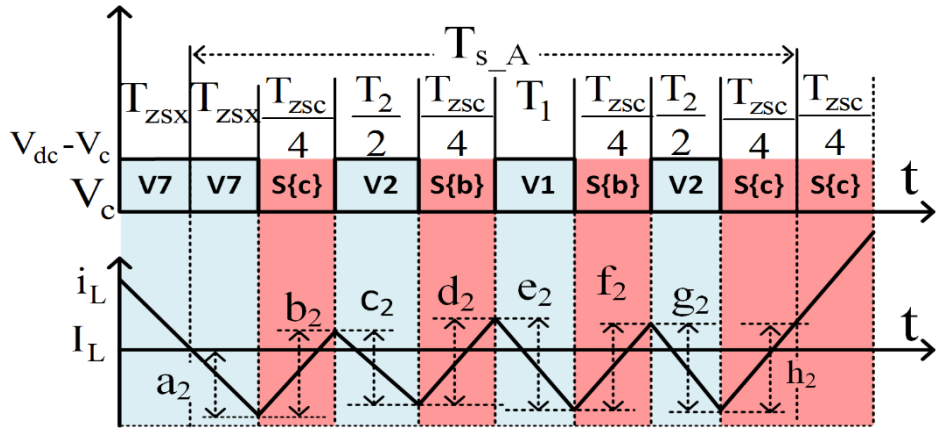


Fig. 2.10. Graphical representation of switching pattern and inductor current ripple components of 7212 switching sequence.

$$\begin{cases} a_2 = a_1 \text{ of equation (2.15)} \\ b_2 = d_2 = f_2 = h_2 = b_1 = d_1 = f_1 = h_1 \text{ of equation (2.15)} \\ c_2 = g_2 = \frac{V_{dc}-V_C}{L}\left(\frac{T_2}{2}\right) = \frac{V_{dc}-V_C}{L}\left(\frac{K_A}{2}.\sin(\alpha)\right) \\ e_2 = \frac{V_{dc}-V_C}{L}(T_1) = \frac{V_{dc}-V_C}{L}\left(K_A.\sin\left(\pi/3 - \alpha\right)\right) \\ \text{here } K_A = \frac{\sqrt{3}}{2}.M.T_{s_A};\ V_C = \left(\frac{1-D}{1-2D}\right)V_{dc}; \\ T_{s\_A} = 1.132 \times T_s \text{ (from equation (2.14))} \end{cases} \quad (2.16)$$

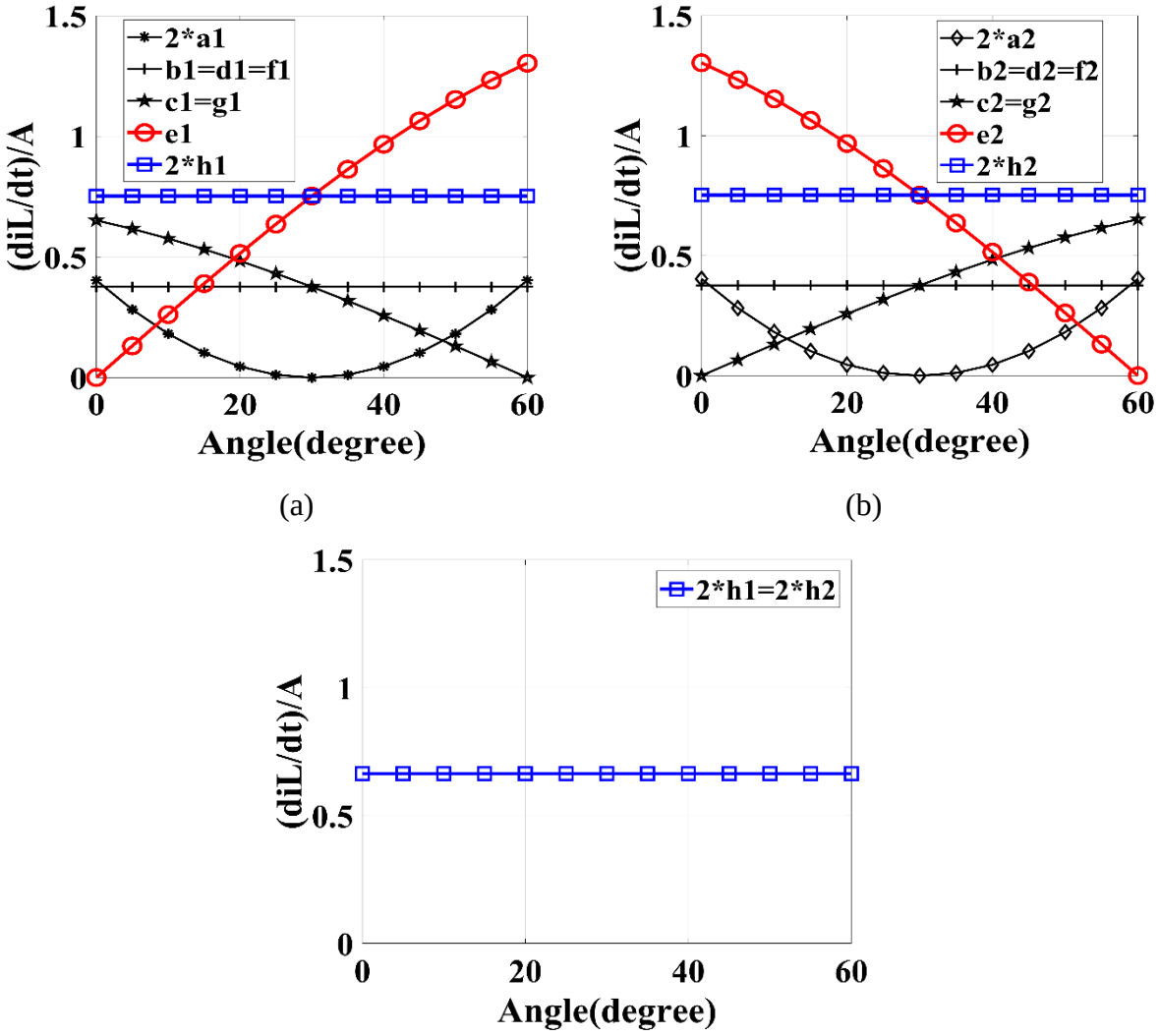


Fig. 2.11. Instantaneous inductor current ripples components at $M = 0.95, T_{s\_A} = 222\text{usec.}, D = 0.177, L = 2\text{mH}, V_{dc} = 60\text{V}$ using (a) 1210 switching sequence throughout the sector 1, (b) 7212 switching sequence throughout the sector I, (c) ABC4_MCB technique.

In Fig. 2.11, the instantaneous values of the ripple components offered by both switching sequences (1210 and 2721) have been plotted over sector I with the parameters given in figure caption. Fig. 2.11 (a) and Fig. 2.11 (b) plots the ripple components when 1210 and 7212 sequences are used separately throughout the sector.

The proposed ABC4_MCB technique uses 1210 sequence in range $0 \leq \alpha < 30°$ and 7212 sequence from $30° < \alpha < 60°$ within the sector I. Therefore, as indicated in Fig. 2.9 and Fig. 2.10,

the maximum instantaneous inductor current ripple is equal to $2 \times |h_1|$ before $\alpha = 30°$ and $2 \times |h_2|$ after $\alpha = 30°$within the sector I (Fig. 2.11 (c)). It is also clear that, $2 \times |h_1| = 2 \times |h_2| = 2 \times |h|$.

In contrast to the ZSVM6_MCB, the maximum instantaneous inductor current ripple in ABC4_MCB is due to the charging time duration applied to the inductor. The ripple components $2 \times |h_1|$ and $2 \times |h_2|$ are the result of charging time duration applied to the inductor. Consideringx$_1 = x_2 = x$; where $x = a, b, c, d, e, f, g, h$. The maximum instantaneous inductor current ripple in a sector can be expressed as:

$$i_{ABC\_MCB} = \text{maximum of } (2|a|, |b|, |c|, |d|, |e|, |f|, |g|, 2|h|)$$
$$= 2 \times |h_1| = 2 \times \left|\frac{V_C}{L}.\left(\frac{1}{4}\right).\left(T_{s\_A} - K_A\right)\right| \quad (2.17)$$

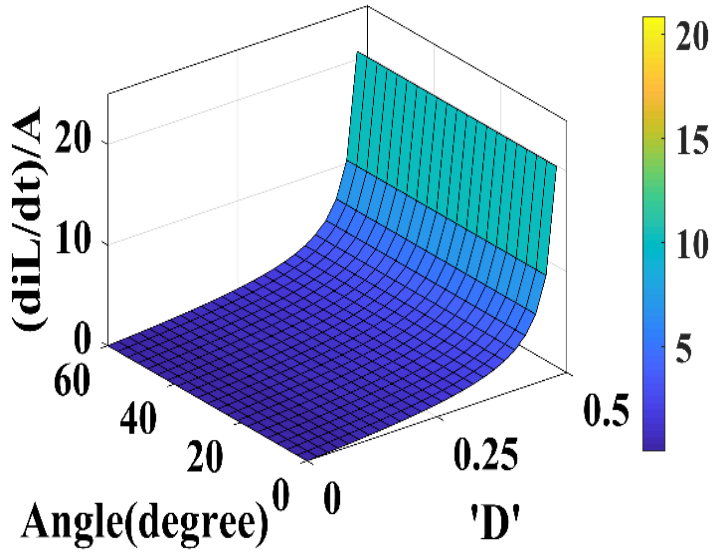


Fig. 2.12. Relationship between angle (α), ST duty ratio 'D' and the maximum inductor current ripple using ABC4_MCB technique in sector 1.

The maximum instantaneous inductor current ripple of ABC4_MCB is constant in the whole sector for any particular value of the ST duty ratio. The relationship between angle (α), ST duty ratio 'D', and the maximum inductor current ripple is shown in Fig. 2.12. It is evident from Fig. 2.12 that, for any particular value of the ST duty ratio in the range (0 to 0.48), the instantaneous, maximum, and average value of the maximum inductor current ripple is constant.

2.6. COMPARISON BETWEEN ZSVM6_MCB AND ABC4_MCB

2.6.1. Inductor current ripple comparison

The ratio of maximum instantaneous inductor current ripple (using equation (2.13) and equation (2.17)) and the ratio of the average value of the maximum instantaneous inductor current ripple (using equation (2.12) and equation (2.17)) of both techniques have been found in equation (2.18) and equation (2.19), respectively. Parameter values are: $T_s = 196\text{usec.}$ for the equation (2.12) and equation (2.13) and $T_{s\_A} = 1.132 \times T_s = 222\text{usec.}$ for equation (2.17). Rest parameters are, $V_{dc} = 60\text{V}, D = 0.134, M = 1, L = 2\text{mH}.$

$$\left\{\frac{I_{max\ \_ZSVM6\_MCB}}{I_{max\ \_ABC4\_MCB}} = \frac{|c_{\alpha=0^\circ}|}{2 \times |h_1|} = \frac{\left|\frac{V_{dc} - V_C}{L}\left(\sin\left(\pi/3\right)\right)(K)\right|}{2 \times \left|\frac{V_C}{L} \times \frac{1}{4}\left(T_{s\_A} - K_A\right)\right|}\right\} = 1.5292 \qquad (2.18)$$

$$\left\{\frac{I_{avg\ \_ZSVM6\_MCB}}{I_{avg\ \_ABC4\_MCB}} = \frac{\text{equation (2.12)}}{\text{equation (2.17)}} = \frac{\left|\frac{V_{dc} - V_C}{L}(0.7)(K)\right|}{2 \times \left|\frac{V_C}{L} \times \frac{1}{4}\left(T_{s\_A} - K_A\right)\right|}\right\} = 1.2343 \qquad (2.19)$$

From equation (2.18), it is clear that the maximum instantaneous inductor current ripple of the ZSVM6_MCB technique is 1.5292 times more than the ABC4_MCB. It means the maximum instantaneous inductor current ripple is 34.6 percent less using the ABC4_MCB technique. Also, from equation (2.19), it can be seen that the average value of the maximum instantaneous inductor current ripple components with the ABC4_MCB PWM technique is 19 percent less than that of ZSVM6_MCB. These ratios are constant for every value of the ST duty ratio in the range 0 to 0.48. The maximum instantaneous inductor current ripple of both ZSVM6_MCB and ABC4_MCB techniques is plotted in Fig. 2.13 for the range 0 to 0.48 of the ST duty ratio.

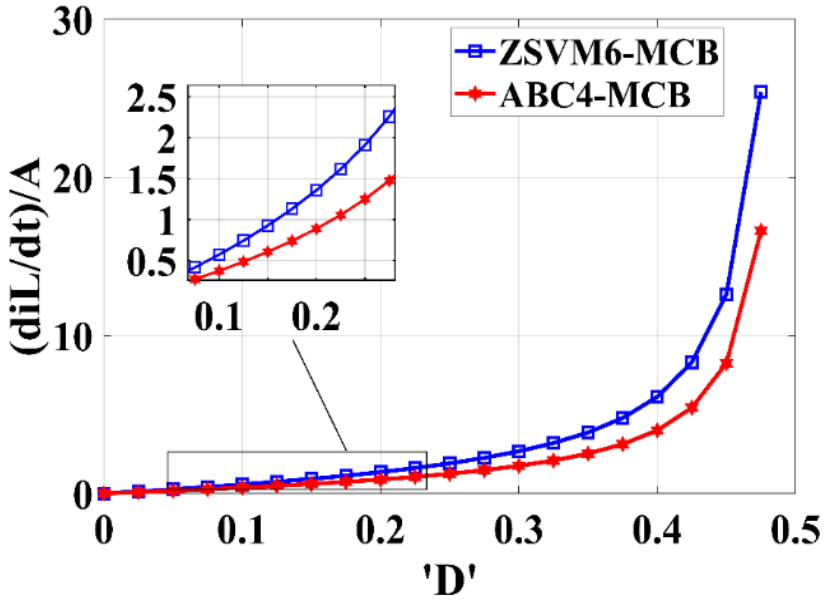


Fig. 2.13. Maximum instantaneous inductor current ripple Vs ST duty ratio of ZSVM6_MCB and ABC4_MCB technique.

Table 2.5. Important aspects of existing and proposed SVPWM of ZSI

Techniques analyzed under the MCB control approach		Switching frequency (Hz)		**	***	****	'B'; 'D'	Features
		IGBTs	diode (D1)					
Category 1 (Existing)	ZSVM4	2550	7650	306	Yes	Easy	$B = \frac{1}{1-2.D}$; $D = 1 - \frac{\sqrt{3}}{2}M.$	• Uses conventional switching sequence (0127) • 3 ST states per sample
	ZSVM6							
	Ref. [21]				No	High		
	ZSVMD6 [22]							
Proposed	ABC4	2600*	8850	354	Yes	Medium		• Uses a combination of conventional (0127) and advanced bus clamping switching sequences (1210, 7212) • 4 ST states in 1210, 7212 switching sequence and 3 ST states in 0127 switching sequence per sample

*The switching frequency of IGBTs using proposed SVPWM is not exactly the same as that of the SVPWM techniques of the category 1 because of the conditions of symmetry mentioned in Table 2.3;

** Total number of ST interval over the fundamental period; *** Does each ST state duration is equal?; **** Complexity of ST implementation

2.7. COMPARISON OF PROPOSED 'ABC4_MCB' WITH SOME EXISTING SVPWM OF ZSI

Some important aspects of the existing and the proposed SVPWM of ZSI have been tabulated in Table 2.5. These are explained as follows:

- For the approximate same average switching frequency of the IGBT switches, the number of ST interval over the fundamental line cycle offered by the ABC4_MCB is more (354) as compared to the existing PWM techniques of the category 1 (306). Therefore, the switching frequency of the input diode and IN is higher and the passive element requirements are lower using the ABC4_MCB technique.
- From category 1, the SVPWM technique of [21] and ZSVMD6 of [22] have been specifically designed to minimize the IN inductor current ripple of ZSI. But these techniques result in a variable time duration of each ST state of a sample. So, the complexity of ST implementation is high in these techniques. The time duration of each ST state is the same in ZSVM4 and ZSVM6 of category 1 and the proposed ABC4_MCB technique. The slight increase in the complexity of the implementation of the proposed technique arises only due to the selection of the appropriate region of the vector diagram for each switching sequence.
- The relationship between the boost factor and ST duty ratio is the same for all techniques.
- The common point between SVPWM techniques of category 1 is that these techniques use a conventional switching sequence (0127). On the other hand, the ABC4_MCB technique uses the combination of conventional (0127) and the advanced bus clamping switching sequences (1210, 7212).

2.8. DESIGN GUIDELINES

The IN components have been designed to limit the high-frequency ripple components of the inductor current and capacitor voltage. The maximum instantaneous charging and discharging durations affect the instantaneous slope of the inductor current and capacitor voltage, respectively.

2.8.1. ABC4_MCB

2.8.1.1. Inductor design

As found in section 2.5.4, the maximum instantaneous change in the inductor current and the capacitor voltage in the case of ABC4_MCB is due to the ST state duration. The inductor current ripple in ST state can be written as [15] [38]:

$$\Delta i_{L\_ABC4\_MCB} = \frac{V_C}{L}\left(\frac{T_{zsc\_A}}{2}\right) \tag{2.20}$$

T_{zsc_A} is the total duration of ST state in a sample using ABC4_MCB. It can be written as:

$$\frac{T_{zsc\_A}}{T_{s\_A}} = D = \left(1 - \frac{\sqrt{3}}{2}M\right) \tag{2.21}$$

Capacitor voltage 'V_C' can be written as:

$$V_C = \left(\frac{\sqrt{3}.M}{2\left(\sqrt{3}M - 1\right)}\right).V_{dc} \tag{2.22}$$

The percentage of the permissible inductor current ripple is defined as:

$$\Delta i_{L\_ABC4\_MCB} = \Delta i_{L\_ZSVM6\_MCB} = r_L\% \,.\, I_L \tag{2.23}$$

I_L is the maximum value of the average inductor current.

Substituting equations (2.21), (2.22), and (2.23) into equation (2.20) and solving for the value of inductor 'L':

$$L = \left(\frac{\sqrt{3}.M.\left(2 - \sqrt{3}.M\right)}{8.\left(\sqrt{3}M - 1\right)}\right)\left(\frac{V_{dc}}{r_L\% \,.\, I_L}\right).\left(T_{s\_A}\right) \tag{2.24}$$

2.8.1.2. Capacitor selection

The high frequency ripple components of the capacitor voltage can be written as [15] [38]:

$$\Delta V_{C\_ABC4\_MCB} = \frac{I_L}{C}\left(\frac{T_{zsc\_A}}{2}\right) \tag{2.25}$$

The percentage of the permissible capacitor voltage ripple is defined as:

$$\Delta V_{C\_ABC4\_MCB} = r_C\% \,.\, V_C \tag{2.26}$$

Substituting equations (2.21) and (2.26) into equation (2.25) and solving for the value of the capacitor:

$$C = \left(\frac{I_L\left(2-\sqrt{3}M\right)}{2.r_C\%\,.V_C}\right).T_{s\_A} \tag{2.27}$$

2.8.2. ZSVM6_MCB

In contrast to ABC4_MCB, here the maximum instantaneous change in the inductor current is due to the time duration of the NST state. In NST state inductor discharges to the load. The inductor current ripple in the ZSVM6_MCB can be written as:

$$\Delta i_{L\_ZSVM6\_MCB} = \frac{V_{dc}-V_c}{L}\left(T_{1\_max}\right) \tag{2.28}$$

T_{1_max} is the maximum duration of the NST state over one sector using the ZSVM6_MCB technique. It can be expressed as (from equation (2.1):

$$T_{1\_max} = \frac{3.M.T_s}{4} \tag{2.29}$$

Substituting equations (2.22), (2.23), and (2.29) into equation (2.28) and solving for the value of inductor 'L':

$$L = \left(\frac{\sqrt{3}.M-2}{2\left(\sqrt{3}M-1\right)}\right).\left(\frac{3.M.T_s}{4.r_L\%\,.I_L}\right).V_{dc} \tag{2.30}$$

The following parameter values have been taken in (2.24), (2.27), and (2.30):

$$T_{s\_A} = 222\text{usec.};\ T_s = 196\text{usec.};\ r_L\% = 0.35;\ r_C\% = 0.01;\ M = 0.95;\ V_{dc} = 60V$$

From equation (2.24) and equation (2.27), the values of the inductor and capacitor are 2.1mH and 51uF, respectively for the ABC4_MCB technique. From equation (2.30), the value of the inductor comes out to be 3.28mH. Therefore, the size of the inductor is around 34 percent less using the ABC4_MCB as compared to the ZSVM6_MCB technique.

2.9. SIMULATION AND EXPERIMENTAL RESULTS

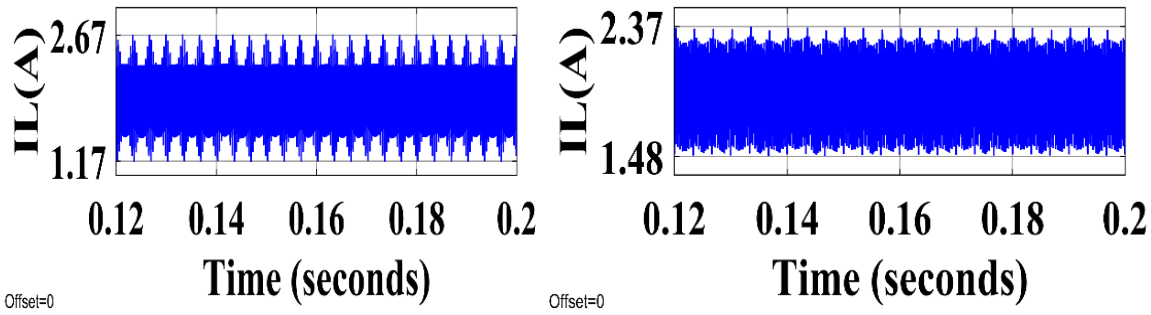
2.9.1. Simulation results

To verify the theoretical findings, ZSVM6_MCB and ABC4_MCB techniques have been simulated in MATLAB/Simulink with the parameters mentioned in Table 2.6.

Table 2.6 Parameters used for simulation and experimental verification

Simulation/ Exp. Parameters	Values/Name
Input dc source (V_{dc})	60V
Impedance network Inductor/Capacitor	2mH/100uF
Load	Resistive, 40Ω per phase
Number of samples	17 per sector for ZSVM6_MCB, 15 per sector for ABC4_MCB
Sample time (T_s)	222usec. for ABC4_MCB, 196usec for ZSVM6_MCB

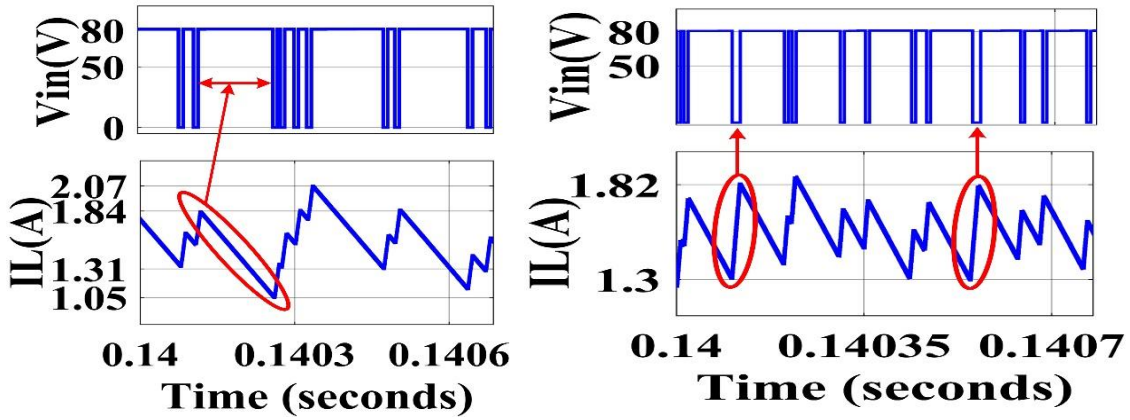
At ST duty ratio 'D' equal to 0.177, Fig. 2.14(a) and (b) shows the simulation waveform of the inductor current in line cycle using ZSVM6_MCB and ABC4_MCB, respectively. Comparing Fig. 2.14(a) and (b), the peak to peak inductor current ripple offered by the ABC4_MCB technique is 40.6 percent less than that of ZSVM6_MCB. It should be noted that this research work focuses on the maximum instantaneous change in the inductor current over the line cycle. As discussed in section 2.4, the maximum instantaneous inductor current ripple offered by ZSVM6_MCB is due to the active vector time duration T_1 (T_2) when the reference vector is closed to $\alpha = 0°$ ($\alpha = 30°$). The inductor discharges with a maximum time duration within a sample at this position.



(a) (b)

Fig. 2.14. Simulation result of the inductor current at D = 0.177, (a) ZSVM6_MCB, (b) ABC4_MCB.

At ‘D’ equal to 0.134, Fig. 2.15(a) shows waveforms of dc-link voltage and inductor current in the carrier cycles just after $\alpha = 0°$ in the sector I. The maximum instantaneous inductor current ripple is 0.79A from Fig. 2.15(a), which is because of the inductor discharging time duration ‘T_1.’



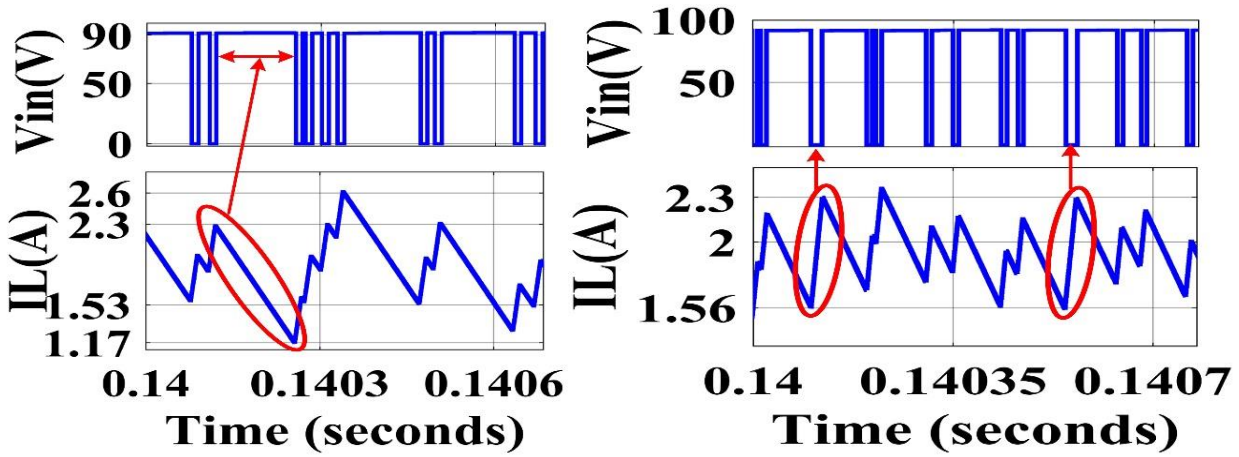
(a) (b)

Fig. 2.15. Simulation waveforms of dc-link voltage and inductor current in a carrier cycle at D= 0.134 (a) ZSVM6_MCB, (b) ABC4_MCB.

On the other hand, the maximum instantaneous inductor current ripple of ABC4_MCB occurs due to the charging time (ST state) duration applied to the inductor (Fig. 2.15(b)). One complete carrier cycle of ABC4_MCB technique starts and ends with the ST state each of time duration equal to ‘$T_{zsc}/4$’. The ending ST state of a sample and starting ST state of next sample combines and the total sum of ‘$T_{zsc}/2$’ becomes responsible for the maximum charging duration applied to the inductor. This duration is constant throughout the fundamental cycle as the maximum constant boost control has been used. Therefore, the maximum instantaneous inductor current ripple is constant with this technique. Fig. 2.15 (b) shows the dc-link voltage and inductor current in the carrier cycle using the ABC4_MCB technique at D=0.134. Two maximum charging time durations have been highlighted in the inductor current which repeats every carrier cycle. The maximum instantaneous inductor current ripple with this technique comes out to be approx. 0.52A. Comparing Fig. 2.15(a) and (b), it is found that the maximum instantaneous inductor current ripple is approx. 34 percent less with ABC4_MCB as compared to the ZSVM6_MCB technique.

Now ST duty ratio has been increased to 0.177. Fig. 2.16 shows the dc-link voltage and inductor current in the carrier cycle for both the techniques. From Fig. 2.16 (a) the maximum instantaneous

change in the inductor current comes out to be 1.13A (i.e. 2.3A-1.17A) using ZSVM6_MCB. Similarly, the maximum instantaneous change in the inductor current using the ABC4_MCB technique is equal to 0.74A (i.e. 2.3A-1.56A). The maximum instantaneous inductor ripple offered by ABC4_MCB is again approx. 34 percent less than ZSVM6_MCB. Hence, simulation results verify that the reduction factor of the inductor current ripple offered by the ABC4_PWM technique is constant at the different values of the ST duty ratio.



(a) (b)

Fig. 2.16. Simulation waveforms of dc-link voltage and inductor current in a carrier cycle at D = 0.177 using, (a) ZSVM6_MCB. (b) ABC4_MCB.

2.9.2. Experimental results

The experimental investigation has been done to have more practical insight into the above PWM techniques. A 200W prototype of ZSI has been designed in laboratory which is shown in Fig. 2.17. The IGBT switch (25Amp, 1200V), part number 'KGT25N120NDH' are used in the prototype, however, their continuous current carrying capability is subjected to the size/capability of the heat sink.Texas instrument's digital signal processor, TMS320F28379D has been used for the generation of gating pulses.

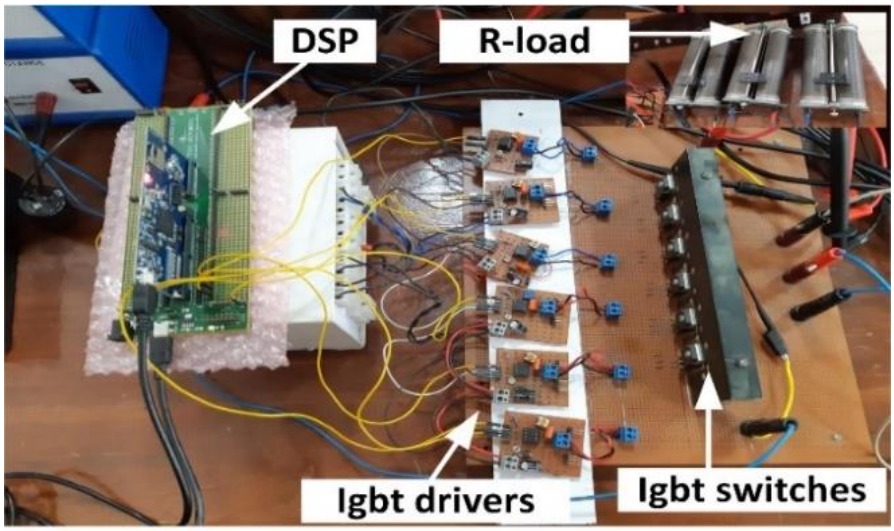
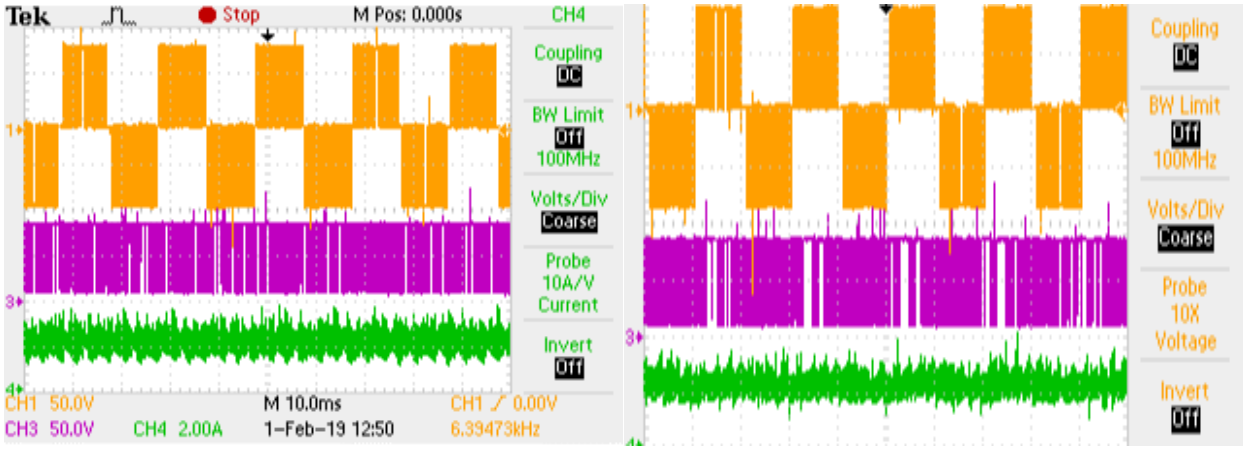


Fig. 2.17. Photograph of the laboratory prototype.



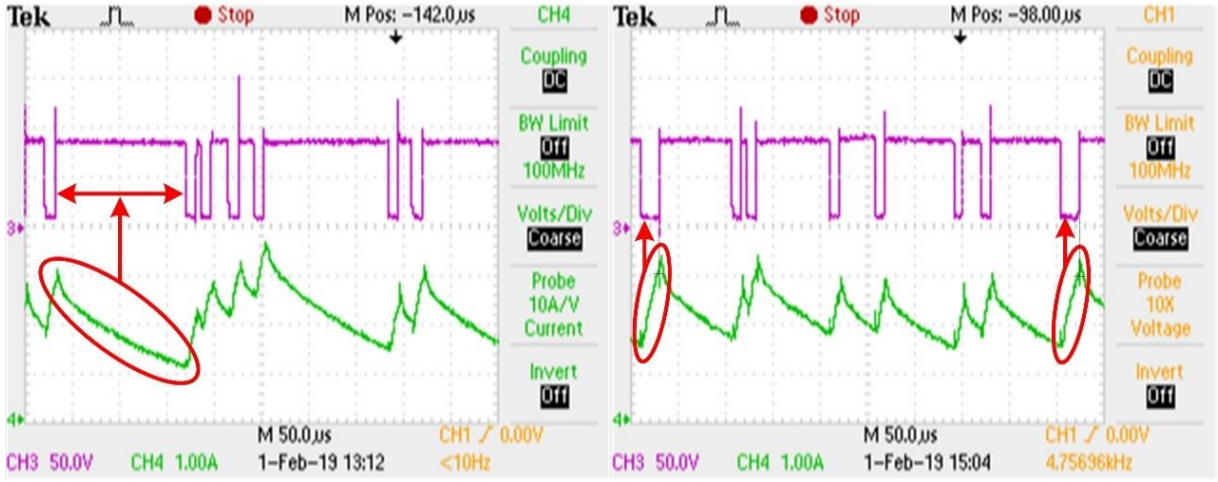
(a) (b)

Fig. 2.18. Experimental waveforms in line cycle at ST duty ratio equal to 0.177, From top: line voltage, dc-link voltage, and inductor current, (a) ZSVM6_MCB (b) ABC4_MCB.

Fig. 2.18 shows the experimental results of ZSVM6_MCB and ABC4_MCB techniques at the ST duty ratio equal to 0.177. Fig. 2.18(a) and (b) contains the experimental waveforms of line voltage, dc-link voltage, and inductor current in the line cycle for ZSVM6_MCB and ABC4_MCB technique, respectively. Since the boost factor is the same in both techniques, the output line voltage and dc-link voltage have a peak value of around 90V. The inductor current is smooth in both techniques as the maximum constant boost control approach has been used. The peak to peak

inductor current ripple using ZSVM6_MCB and ABC4_MCB (Fig. 2.18(a) and Fig. 2.18(b)) is around 1.2A and 0.72A., respectively. This validates the simulation result of Fig. 2.14 (i.e. around 40 percent reduction in peak to peak inductor current ripple using ABC4_MCB technique).

Fig. 2.19(a) and (b) shows the waveforms of dc-link voltage and inductor current in a carrier cycle for ZSVM6_MCB and ABC4_MCB, respectively. Fig. 2.19(a) highlights the maximum discharging time duration 'T_1' applied to the inductor which is similar to the simulation result of Fig. 2.16(a). Similarly, for the ABC4_MCB technique, Fig. 2.19(b) highlights the two portions of the maximum charging time durations applied to the inductor which repeats every carrier cycle. These charging time durations of inductor current are similar to the simulation result of Fig. 2.16(b). The maximum instantaneous inductor current ripple value is around 2.2A and 1.4A from Fig. 2.19 (a) and (b), respectively. These values indicate that the percentage reduction in the maximum instantaneous inductor ripple using ABC4_MCB is around 34 percent less as compared to ZSVM6_MCB. In this way, the theoretical findings, simulation, and experimental results verify that the proposed PWM technique 'ABC4_MCB' is better as compared to the conventional ZSVM6_MCB technique in terms of inductor current ripple.



(a) (b)

Fig. 2.19. Experimental waveforms in a carrier cycle at ST duty ratio equal to 0.177, From top: dc-link voltage and inductor current (a) ZSVM6_MCB, (b) ABC4_MCB.

The practical efficiency of the system has been measured using the true rms meter. The efficiency curve is plotted in Fig. 2.20 for both the techniques. It has been noticed from the efficiency plot

that the ABC4_MCB technique causes a small decrease in efficiency as compared to the ZSVM6_MCB technique under higher load conditions.

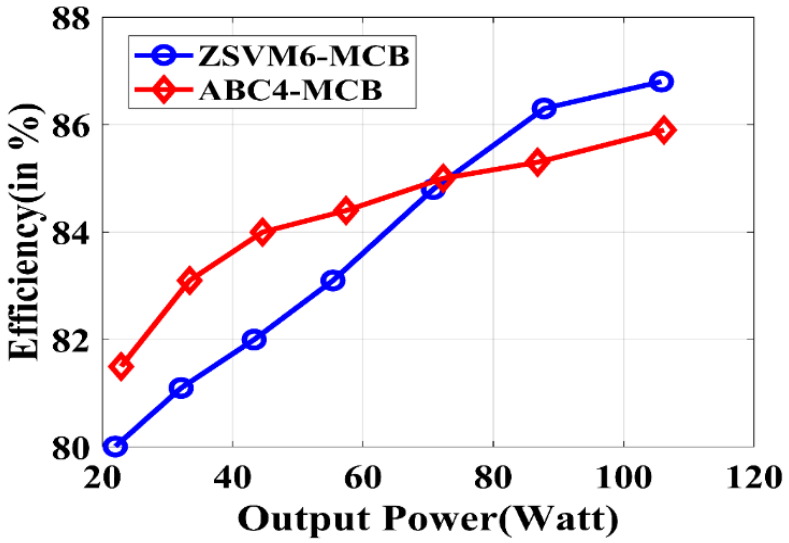


Fig. 2.20. Prototype efficiency curve using ZSVM6_MCB and ABC4_MCB techniques.

2.10. CONCLUSION

It has been proved that, at the same average switching frequency of the power switches, the proposed ABC4_MCB technique offers a 34 percent reduction in the maximum instantaneous inductor current ripple of ZSI as compared to the ZSVM6_MCB technique. The proposed PWM technique retains the main advantage of the maximum constant boost control technique which is the smooth inductor current. The full range of ST duty ratio (0 to 0.48) has been taken for the comparison of the inductor current ripple. The factor of percentage reduction in the maximum instantaneous inductor current ripple using the proposed technique is constant at any value of the ST duty ratio in a range 0 to 0.48. Theoretical findings have been verified using the simulation and experimental results. The proposed technique is equally valid for various Z-source principle derived inverter topologies.

CHAPTER 3. CONTROLLED DIODE BRIDGE CLAMPED 3L-ZSI AND ITS PWM CONTROL

3.1. INTRODUCTION

The multilevel inverters offer superior performance in terms of output waveform quality, dv/dt across power switches, and reduced output filter requirements as compared to the 2L inverters [61]. Further, the concept of ZSI inserts additional features in them, such as single-stage buck-boost operation and the absence of dead time between the power switches. However, there are some concerns associated with the topology and PWM control techniques of multilevel ZSIs. These include size/cost of the inverter circuit including impedance network (IN), and the complexity of the PWM generation.

The research area of the topological improvement has the main focus on the IN to improve the performance of 3L-ZSI in terms of the voltage gain, capacitor voltage stress, continuous input current, etc. Mainly, the neutral point clamped (NPC) [62]–[65], [71], [77], [80], [82]–[84] and T-type inverter [67], [68], [70], [72] configurations have been used with the various types of the IN. Considering low to medium voltage applications, the T-type VSI configuration is better in terms of circuit elements, switching/conduction losses, and efficiency as compared to the NPC 3L-VSI [92], [93]. Because of this, T-type is the most popular standalone configuration of 3L-ZSI nowadays.

In this chapter, a new configuration of 3L-ZSI has been proposed. The proposed configuration is based on a Controlled Diode Bridge Clamped (CDBC) 3L inverter circuit. CDBC inverter configuration is the optimized version of the T-type VSI in terms of power switches and their associated gate driver components. This chapter starts with a brief introduction to CDBC configuration based 3L-VSI. After that, CDBC configuration has been extended to the concept of ZSI.

In the case of a 3L-VSI, the maximum permissible number of switching transitions to realize reference vector at any position in the switching vector diagram are six per sample (half carrier cycle). This condition is also desired in the 3L-ZSI. The existing continuous space vector PWM techniques [70], [77], [82] of 3L-ZSI uses the combination of two types of samples. One type of samples causes six switching transitions and other types of samples causes eight switching

transitions to generate correct volt-second balance. The type of samples which cause eight switching transitions are undesirable because of the drawback of increased switching losses. In this chapter, the regions of the 3L vector diagram which causes eight switching transitions per sample are highlighted and a new switching state pattern for the samples of these regions has been proposed for optimizing the switching frequency of the power switches. The authors claim that it is not possible to have exactly six switching transitions per sample in these regions for a continuous SVPWM technique when only small vectors are used for ST state insertion. The proposed SVPWM switching pattern reduces the number of switching transitions to 7 per sample in these regions (i.e. saving in one switching per sample). Due to the proposed switching patterns, the overall SVPWM technique offers minimum switching frequency of power switches as compared to the existing SVPWM techniques of [70], [77], [82] without imposing any drawback (i.e without affecting line voltage/current THD).

The output voltage waveform quality is better when the adjacent nearest switching vectors (NTV) are used to realize the reference vector. It is found that, when the NTV switching approach is followed, the switching frequency of the power switches of 3L-ZSI depends on the modulation index value. This dependency of 'M' on the switching frequency of the power switches has been highlighted in this work. The proposed SVPWM switching pattern is equally valid for NPC and T-type ZSIs. Finally, the simulation and experimental results verify the proposed inverter configuration and its PWM technique.

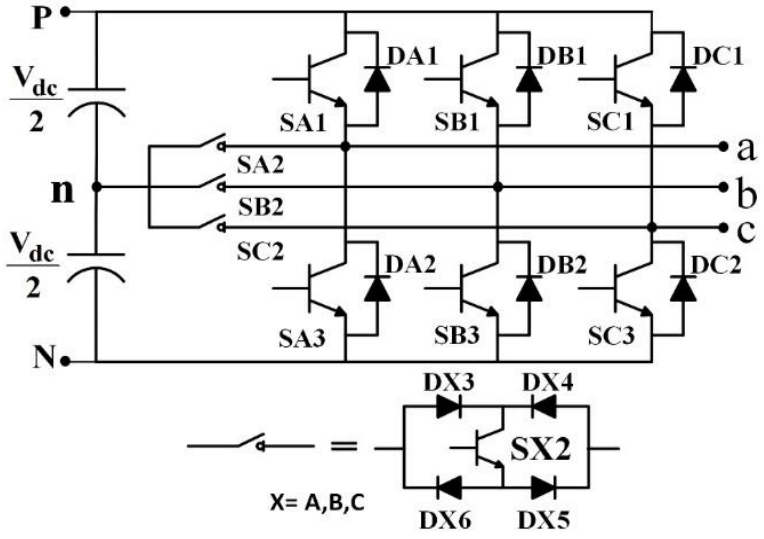


Fig. 3.1. Controlled Diode Bridge Clamped 3L-VSI.

3.2. CONTROLLED DIODE BRIDGE CLAMPED (CDBC) VSI

The configuration of the CDBC VSI [94] is shown in Fig. 3.1. In this configuration, each phase leg is connected to the dc bus midpoint using a controlled bidirectional switch. The controlled bidirectional switch is made with the combination of one IGBT and four diodes. Hence the name controlled diode bridge clamped has been given here. The operating principle of this configuration can be understood from Table 3.1.

Table 3.1. Switching states of CDBC 3L-VSI

$\mathbf{V_{Yn}}$ (pole Voltage)	Switching State/[position]	Gating Pulse	ON switches	ON Diodes
$V_{dc}/2$	P/ [100]	SX1	SX1	DX1
0	O/ [010]	SX2	SX2	DX3,DX5 or DX4,DX6
$\mathbf{-V_{dc}/2}$	N/ [001]	SX3	SX3	DX2

Where Y= (a, b, c) and X= (A, B, C)

Each phase leg offers three distinct voltage levels which are $0; \pm V_{dc}/2$. A separate switching state is assigned to each voltage level as shown in Table 3.1. For example, the switching state 'P' denotes that the upper power switch of a phase is in ON position and the switching position in this state can be denoted by [100]. '1' means the switch is ON and '0' means the switch is OFF.

Table 3.2. Switching states of NPC and T-Type VSI

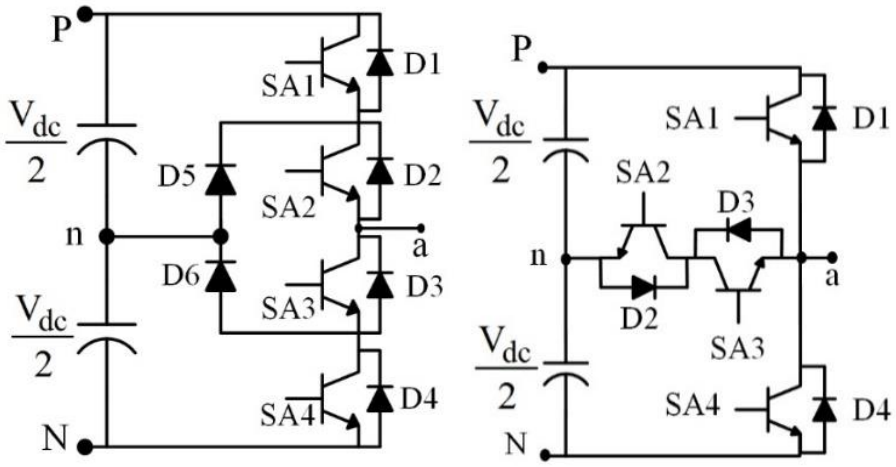
Van (pole Voltage)	Switching State/ [position]	NPC		T-type	
		Gating pulse	ON switches /Diodes	Gating pulse	ON switches/Diodes
$V_{dc}/2$	P/ [1100]	SA1 and SA2	SA1 and SA2 {or} D1 and D2	SA1 and SA3	SA1 {or} D1
0	O/ [0110]	SA2 and SA3	SA2 and D5 {or} SA3 and D6	SA2 and SA3	SA2 and D3 {or} SA3 and D2
$\mathbf{-V_{dc}/2}$	N/ [0011]	SA3 and SA4	SA3 and SA4 {or} D3 and D4	SA2 and SA4	SA4 {or} D4

Table 3.3. Average switching frequency of the power switches in CDBC, NPC and T-type VSI

Average switching frequency	CDBC VSI			NPC VSI	T-type VSI
	SX1	SX2	SX3	Switches (SX1 to SX4)	Switches (SX1 to SX4)
F_{sw}	$(1/4).T_s$	$(1/2).T_s$	$(1/4).T_s$	$(1/4).T_s$	$(1/4).T_s$

X=A, B, C; T_s is the duration of one sample or half carrier cycle.

The one phase leg of NPC [2] and T-type VSI [92], [93] is shown in Fig. 3.2.



(a) (b)

Fig. 3.2. One phase leg of 3L inverters (a) NPC VSI, (b) T-type VSI.

The working principle of NPC and T-type VSI can be understood from Table 3.2. There are four power switches associated with each phase leg of NPC and T-type VSI. Therefore, each time, four gating pulses are required. Depending upon the direction of the load current, the combination of ON switches and ON diodes have been listed in Table 3.2. The comparison of the average switching frequency of each switch of CDBC, NPC and T-type VSI is given in Table 3.3. From Table 3.3, it can be noticed that the switching frequency of the bidirectional switch (SX2) in CDBC VSI is twice, as compared to the upper and lower switch of the same phase leg and each switch of NPC and T-type VSI. Considering the case of low voltage application (<=1200V), the CDBC configuration offers the following advantages:

- It offers reduced conduction and switching losses as compared to the NPC VSI because only one switch per phase leg is conducting at any instant. But, in NPC VSI two switches per phase leg are in conduction during power flow to load (Table 3.2)
- It reduces one IGBT per phase leg and its associated gate driver ICs/circuit elements as compared to NPC and T-type VSI
- Only one gating pulse is being generated and fed to the particular IGBT at a time to turn it ON (Table 3.2). There are always two gating pulses being generated in NPC and T-type VSI (Table 3.2).

However, the main drawbacks of the CDBC inverter configuration is that, during the inverter operation in state 'O' shown in Table 3.1, two diodes and one IGBT comes in the conduction path. On the other hand, NPC and T-type VSI have one diode and one IGBT in the conduction during state 'O' (Table 3.2). Therefore, the power loss due to one extra diode in state 'O' can be seen as the drawback of CDBC VSI.

3.3. CONTROLLED DIODE BRIDGE CLAMPED 3L-ZSI

Fig. 3.3 shows the configuration of CDBC 3L-ZSI which uses a conventional single LC IN [77].

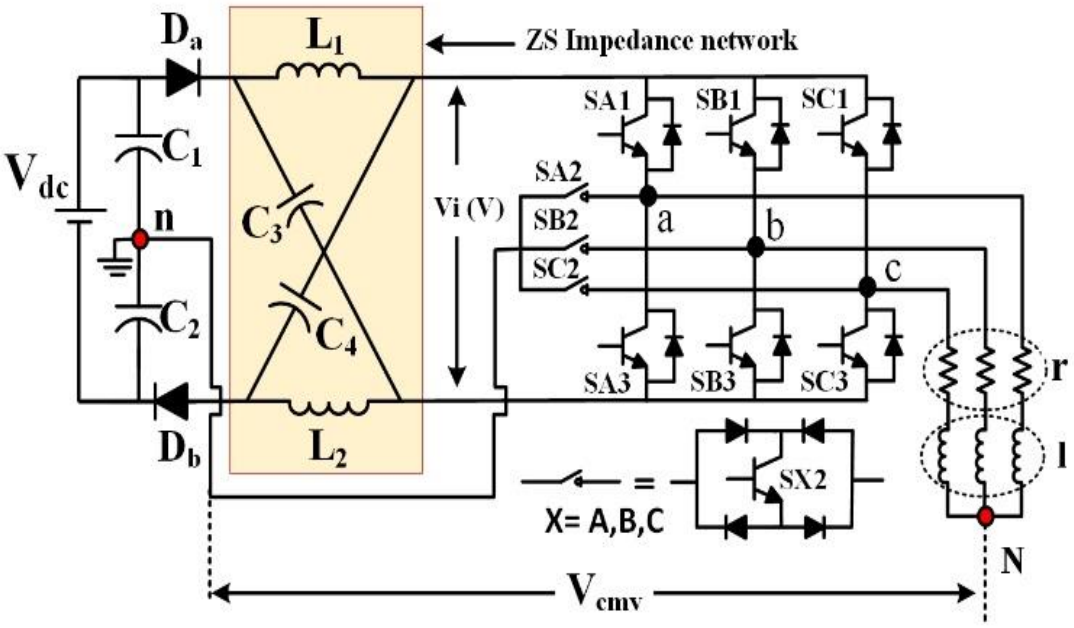


Fig. 3.3. Complete configuration of three-phase CDBC 3L-ZSI.

3.3.1. Switching states

As we know from chapter 2 that the switching states of ZSI can be broadly classified into two categories, ST and NST states [62]. In the case of 3L-ZSI, ST state is further classified into an upper shoot through (UST), lower shoot through (LST), and full dc-link shoot through (FST). Table 3.4 shows the switching states of the CDBC ZSI configuration. The switching states have been denoted using six letters, 'P', 'O', 'N', 'F', 'U', and 'L'. The letters, 'P', 'O', 'N' denotes the NST states, and 'F', 'U', 'L' denotes the ST states.

Table 3.4. Switching states of the CDBC 3L-ZSI

States	ON Switches	V_{YO}(pole voltages)	State/Switching Position
NST	SX1	$+BV_{dc}/2$	P/100
NST	SX2	0	O/010
NST	SX3	$-BV_{dc}/2$	N/001
FST	SX1, SX3	0	F/101
UST	SX1, SX2	0	U/110
LST	SX2, SX3	0	L/011

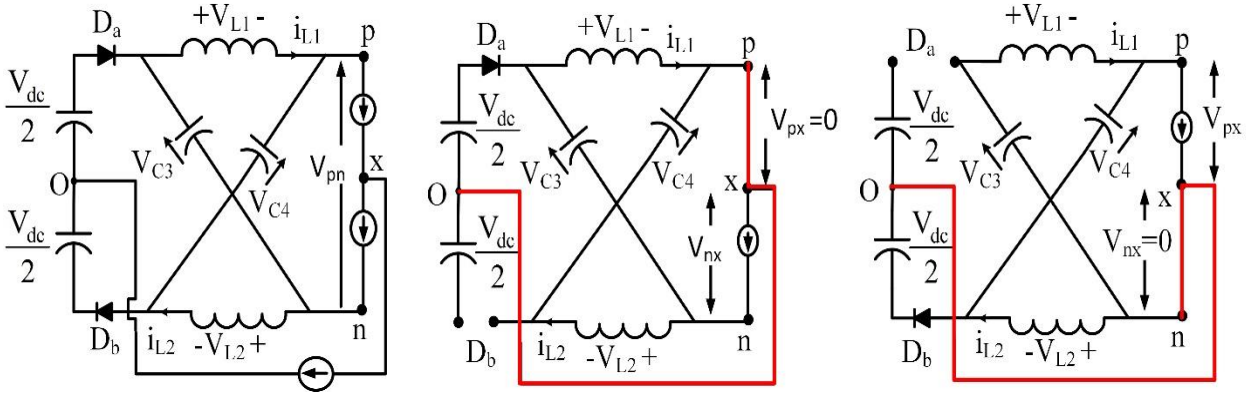
X=A,B,C and Y=a,b,c, B=boost factor

The NST state denoted by 'P' indicates that the phase leg is connected to the positive dc bus via ON upper switch of a phase leg. Similarly, the 'O'/ 'N' indicates that the phase leg is connected to the midpoint/ negative point of the dc bus via ON middle/lower switch of a phase leg. In the category of ST states, the letter 'F' indicates the inverter operation in the FST state. FST state is realized using simultaneous turning ON upper and lower switch of the same phase leg to make a short circuit path across the inverter dc-link. The letter 'U' and 'L' indicates the inverter's operation in UST and LST state, respectively. In UST/(LST), a short circuit path is created across the upper dc source capacitor/(lower dc source capacitor) by simultaneous turning ON the power switch SX1 and SX2/(SX2 and SX3) of the same phase leg.

In the case of 2L-ZSI [3], the ST state is normally applied using the time duration of null states ([000], [111]). There are two null states in the 2L PWM and both null states produce zero line voltage. Therefore, these two null states duration can be completely or partially replaced by the ST states in 2L-ZSI. ST states make short circuits across the full dc-link of 2L-ZSI.

On the other hand, in the case of 3L-ZSI, the equivalent null states (small vectors) serve the same purpose as that of null states of 2L-ZSI. But the difference here is that none of the equivalent null states produces zero line voltage. Therefore, if the nearest three vectors (NTV) switching is desired at high modulation index range (from 0.67 to 1.15), then full dc-link cannot be shorted (i.e. FST cannot be applied). This is because the FST state causes zero line voltage and no switching state (except [000]) of 3L-ZSI produces zero line voltage. The use of [000] switching state distorts the condition of NTV switching. That is why the concept of alternate upper-lower shoot through (ULST) is popular in 3L-ZSI.

The attractive feature of CDBC ZSI is that it requires only two switches to be turned ON (only two gating pulses) for the ST state insertion whether it is UST, LST, or FST. In NPC ZSI, three switches are required to be turned ON for the insertion of ST state.



(a) (b) (c)

Fig. 3.4. Equivalent circuit diagrams of 3L-ZSI during, (a) NST, (b) UST, (c) LST.

3.3.2. Circuit analysis

The equivalent circuit diagrams of 3L-ZSI during ST and NST states are shown in Fig. 3.4. In the equivalent circuit diagram of NST state (Fig. 3.4 (a)), a symbol of the current source indicates that the power is flowing from source to load via any combination of upper, lower, and middle switches of three-phase legs. The operation of ZSI in this state is similar to that of 3L-VSI. During UST (Fig. 3.4(b)) upper dc source is shorted and power to load is flowing through the bottom switches of three-phase legs. Diode 'D_b' is in blocking mode during UST. Similarly, during LST (Fig. 3.4(c)) lower dc source is shorted, and power to load is flowing through the upper switches of three-phase legs. Diode 'D_a' is in blocking mode during LST.

Assuming IN is symmetrical, which means, $L_1 = L_2 = L$ and $C_3 = C_4 = C$. The following expressions can be derived from the equivalent circuit diagrams shown in Fig. 3.4 [77]:

The voltage across the capacitors of the IN is:

$$V_C = V_{dc}\left(\frac{1-D}{1-2D}\right) \tag{3.1}$$

'D' is the shoot-through duty ratio. The expression of 'D' depends upon the type of voltage boost control used (i.e. simple boost, maximum boost, and maximum constant boost control).

Voltage during the NST state is:

$$V_{pn} = \frac{V_{dc}}{(1-2D)} = BV_{dc} \tag{3.2}$$

'B' is the boost factor which can be expressed as:

$$B = \frac{1}{(1-2D)}$$

Voltage during UST and LST state:

$$V_{nx}(UST) = V_{px}(LST) = \frac{V_{dc}}{2.(1-2D)} \tag{3.3}$$

The peak value of the fundamental ac output pole voltage $V_{xo};\ (x = a, b, c)$ can be expressed as:

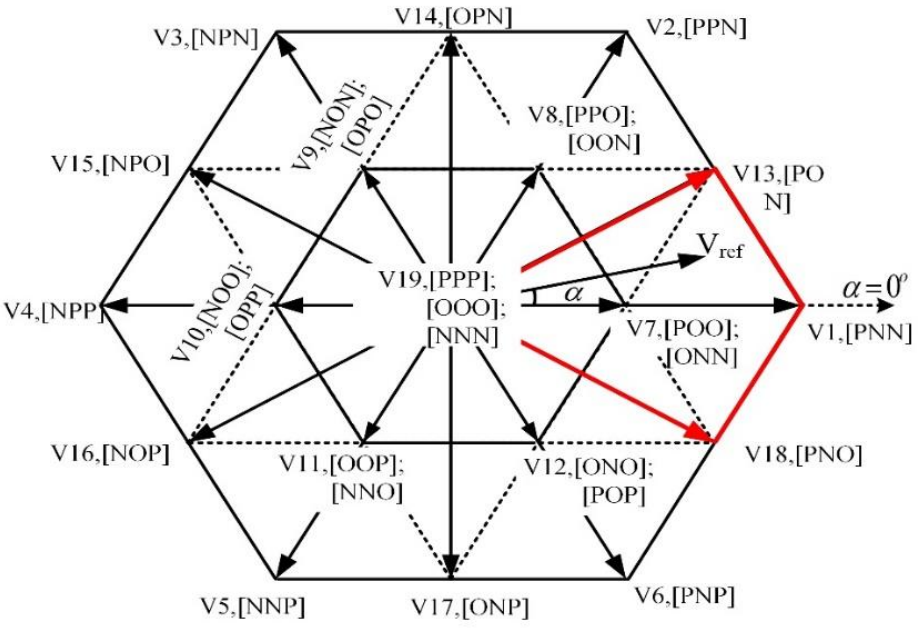
$$V_{xo} = M.B.\frac{V_{dc}}{2} \tag{3.4}$$

'M' is the modulation index.

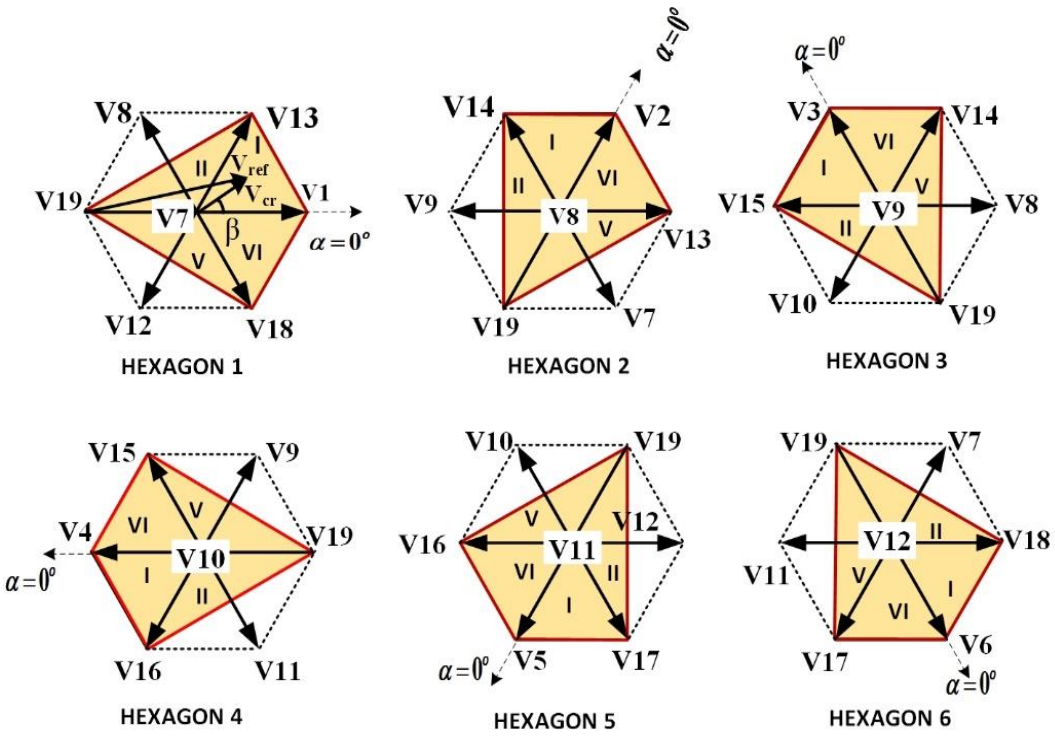
3.4. SVPWM TECHNIQUE OF CDBC ZSI

3.4.1. Review of 3L SVPWM approach

The approach of controlling 3L as an equivalent 2L inverter [78] has been used in this work. According to this approach the spatial region of the 3L vector diagram shown in Fig. 3.5(a) can be partitioned into six equivalent 2L hexagons.



(a)



(b)

Fig. 3.5. Description of 3L space vector diagram, (a) complete space vector switching state diagram, (b) equivalent 2L hexagon 1 to 6.

The equivalent 2L hexagons (1 to 6) are shown in Fig. 3.5(b). The redundant vectors located at the center of each 2L hexagon serve the same purpose as that of null vectors in the case of 2L SVPWM. These redundant vectors are termed as equivalent null vectors in this approach. For simplicity, each equivalent 2L hexagon is considered only for 60-degree interval duration as highlighted in Fig. 3.5(b).This assumption eases the selection of switching states in the overlapping region between two hexagons. Depending upon the angular position of the original reference vector 'V_{ref}', first, the equivalent 2L hexagon is selected and then the equivalent null vector corresponding to that hexagon is subtracted from the original reference vector to obtain corrected reference vector 'V_{cr}'. Next, the corrected reference vector 'V_{cr}' is mapped into subsectors of the corresponding hexagon. Finally, 'V_{cr}'is synthesized using 2L SVPWM principle. For example, the corrected reference vector in subsector I of the hexagon 1 can be synthesized by applying switching vectors V1, V13, and V7 for the duration of T_a, T_b, T_z, respectively. The formulas used for the calculation of dwell time in the subsector I of hexagon 1 are given below:

$$T_a = \frac{V_{cr}}{0.5V_{dc}} \frac{\sin(\pi/3 - \beta)}{\sin(\pi/3)} T_s \quad (3.5)$$

$$T_b = \frac{V_{cr}}{0.5V_{dc}} \frac{\sin(\beta)}{\sin(\pi/3)} T_s \quad (3.6)$$

$$T_z = T_s - T_a - T_b \quad (3.7)$$

The relationship between the corrected angle (β) and original angle (α) for hexagon 1 is:

$$\beta = a\tan\left(\frac{V_{ref.} \times \sin(\alpha)}{V_{ref.} \times \cos(\alpha) - 0.5}\right) \quad (3.8)$$

3.4.2. Considered Conditions for SVPWM of CDBC ZSI

The following conditions have been taken into consideration while implementation of SVPWM technique in the CDBC ZSI configuration:

- The total numbers of samples are even over the complete fundamental cycle and odd in each equivalent 2L hexagon
- The range of modulation index has been taken from 0.67 to 1.15 (i.e. original reference vector 'V_{ref}' has a magnitude between 0.5 and 0.86 per unit dc-link voltage)
- The subsectors of each equivalent 2L hexagon have been further classified into outer and inner subsectors of interest. Table 3.5 shows the classification of the subsectors of interest of each 2L hexagon for the range of modulation index from 0.67 to 1.15.

Table 3.5. Subsectors of interest for the range of 'M' from 0.67 to 1.15

Hexagon no.	Subsectors of interest	
	Outer	Inner
1 to 6	V, II	VI, I

The value of the modulation index and the carrier frequency cumulatively affects the number of samples of the corrected reference vector in the outer/inner subsectors of each 2L hexagon.

Table 3.6. Number of samples of corrected reference vector (V_{cr}) in the subsectors of interest Vs modulation index 'M' at various values of carrier frequencies

Carrier frequency (F_c) in kHz.	'M'	Subsectors of interest for hexagon 1 to 6			
		Outer (V)	Inner (VI)	Inner (I)	Outer (II)
1.65	1.15	0	5	5	1
	0.866	2	3	3	3
	0.733	4	1	1	5
	0.67	5	0	0	6
5.25	1.15	3	14	14	4
	0.866	6	11	11	7
	0.733	12	5	5	13
	0.67	17	0	0	18
10.65	1.15	5	29	29	8
	0.866	12	22	22	15
	0.733	24	10	10	27
	0.67	34	0	0	37

For example, Table 3.6 shows the number of samples of the corrected reference vector in the outer and inner subsectors of interest for hexagon 1 to hexagon 6. It can be noticed from Table 3.6 that, as the modulation index decreases, the number of samples of the corrected reference vector in the inner subsectors also decreases, and at the same time the number of samples in the outer subsectors of interest increases. This type of analysis may not be useful for the case of 3L-VSI because the switching frequency offered by each subsector is the same in 3L-VSI. Since the switching frequency offered by the outer and inner subsector can be different, this type of analysis is important in 3L-ZSI. This has been discussed in detail in subsequent sections/subsections.

3.4.3. Selection of ST states

In the case of 3L-ZSI, the ST states can be added in existing inverter states with partial or full replacement of equivalent null as well as equivalent active states. The following points have been carefully considered.

- The duration of UST and LST state within a sample is maintained the same to avoid unbalance in the voltage boosting offered by the upper and lower inductor of the IN

- For an ideal case, the number of switching transitions per sample is six. If this is not possible in any region of the vector diagram, the minimum increase in switching transition after six should be considered

There are two main approaches for selecting the duration of ST state in the 3L-ZSI. Each approach has its own merits and demerits.

3.4.3.1. Using equivalent null state duration only

In this approach, the ST states are applied using the time duration of equivalent null states only. The only drawback of this approach is that it causes 8 number of switching transitions per sample when implemented using a sine triangle comparison-based approach [62]. This approach is named as a continuous edge insertion (CEI) PWM technique. It offers easy and simple control of inverter switching states.

3.4.3.2. Using equivalent null and equivalent active states

In this approach, the ST states use the time duration of the equivalent null state as well as equivalent active states. This approach is termed as continuous modified reference (CMR) PWM in [62]. It offers a minimum switching transition (six) per sample. But, the complexity in the use of equivalent active states durations for the ST states in the region where the required ST interval is more than the available equivalent active states duration of a sample is the main drawback of this approach.

3.5. PATTERN OF SWITCHING STATES

In proposed work, the equivalent null states have been used for the ST insertion because of the easier and reliable implementation. The process of ST state insertion has been classified into two categories, i) ST insertion for inner subsectors, ii) ST insertion for outer subsectors of interest.

3.5.1. Understanding ST Insertion for inner subsectors of interest

Consider inner subsector VI of hexagon 1 (Fig. 3.5(b)). Table 3.7 shows the switching states for this subsector.

Table 3.7. Switching state pattern per sample for the inner subsector VI of hexagon 1

Subsector VI (Inner)					
Switching state	SA 1 2 3	SB 1 2 3	SC 1 2 3	*	**
POO	1 0 0	0 1 0	0 1 0	6	4
PLO	1 0 0	0 1 1	0 1 0		
PNO	1 0 0	0 0 1	0 1 0		
PNN	1 0 0	0 0 1	0 0 1		
UNN	1 1 0	0 0 1	0 0 1		
ONN	0 1 0	0 0 1	0 0 1		

* switching transition per sample using MCB/SBC approach of voltage boosting.

** switching transition per sample using MBC approach of voltage boosting.

In this subsector, when switching state changes from POO to PNO the switch SB2 and SB3 changes from 1 to 0 and 0 to 1, respectively. State 1 means switch is ON and state 0 means switch is OFF. The advance turn ON of switch SB3 will insert a new state PLO before the PNO. The state PLO causes the lower inductor to be shorted via ‘b’ phase leg and it is termed as an LST state. Since ‘a’ phase leg is supplied via upper dc source and ‘c’ phase leg is already connected to the zero potential, the state PLO will produce the same line voltage as that of state POO. State PLO uses the time duration of state POO. The same procedure is used for the UST state when the state changes from PNN to ONN. The ST state cannot be applied when the state changes from PNO to PNN because the UST/LST state applied in this position using any phase leg will affect the voltage produced by other phase legs. The switching transitions per sample have been also shown in Table 3.7. The MCB and SBC approach cause 6 and the MBC approach causes 4 switching transitions per sample in the inner subsectors. In the MBC approach, equivalent null states (POO, ONN) are absent from the pattern of switching states. This has been discussed in detail in the next subsection.

3.5.2. Understanding ST Insertion for the outer subsectors of interest

Consider outer subsector V of hexagon 1 (Fig. 3.5(b)). Table 3.8 shows the switching states for the outer subsector V. In this subsector when state changes from POO to PNO the procedure for LST state insertion is the same as that of inner subsectors. But, for the addition of UST, two schemes are possible.

Table 3.8. Proposed switching state pattern per sample for the outer subsector V of hexagon 1

Subsector V(outer)					
Switching state	SA 1 2 3	SB 1 2 3	SC 1 2 3	*	**
POO	1 0 0	0 1 0	0 1 0	7	6
PLO	1 0 0	0 1 1	0 1 0		
PNO	1 0 0	0 0 1	0 1 0		
ONO	0 1 0	0 0 1	0 1 0		
ONN	0 1 0	0 0 1	0 0 1		
UNN	1 1 0	0 0 1	0 0 1		

* switching transition per sample using MCB/SBC approach of voltage boosting.

** switching transition per sample using MBC approach of voltage boosting.

3.5.2.1. Scheme 1 (existing)

In Table 3.8, the UST state can be added when switching state changes from ONO to ONN in subsector V (not shown in Table 3.8). For example, the switching state [010 001 011] can be inserted between ONO and ONN. This scheme has been followed by [70], [77]. It causes 8 switching transitions per sample in the all outer subsectors of each 2L hexagon.

3.5.2.2. Scheme 2 (proposed)

In the proposed scheme, UST has been added after the equivalent null state ONN as shown in Table 3.8. This scheme causes 7 switching transitions per sample in all outer subsectors of each 2L hexagon. So, as the number of samples in the outer subsectors increases (Table 3.6), benefit in terms of switching losses reduction increases using the proposed ST insertion scheme.

It is clear from the above explanation that, when the numbers of switching transitions per sample are optimized, the position of ST state in outer subsectors of interest becomes different to the inner subsectors of interest for each 2L hexagon (Table 3.7 and Table 3.8). Therefore, outer and inner subsectors of interest have to be considered separately for the process of ST state insertion.

3.6. EFFECT OF VOLTAGE BOOST CONTROL APPROACH ON THE SWITCHING PATTERNS

The time duration and the position of the ST state within a sample depend upon the type of voltage boost control approach. The SBC, MBC, and MCB voltage boost control approaches of ZSI are analyzed here.

3.6.1. MBC

When equivalent null state duration is only used for ST state insertion, the continuous SVPWM technique of 3L-ZSI allows the insertion of only two ST states (one UST and one LST) per sample as shown in Table 3.7 and Table 3.8. If the equivalent null states durations are completely replaced by UST and LST, the approach is termed as MBC. For this case the row containing the state POO and ONN can be erased from Table 3.7 and Table 3.8. MBC allows the advantages in terms of reduced device commutation for every 2L hexagon. Similar to the case of 2L-ZSI, this technique causes the ripples in IN inductor current of 3L-ZSI also. Fig. 3.6 shows the pattern of switching states in the outer subsector II of hexagon 1 when the MBC control technique is applied. Underlined states are ST states. This switching pattern will remain the same for all subsectors (inner/outer) of each 2L hexagon over the fundamental line cycle (i.e. ST states will always occupy the extreme ends with equivalent active states placed within the center of each sample).

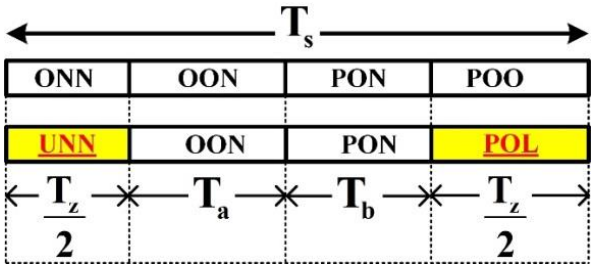


Fig. 3.6. Switching state pattern per sample in the outer subsector II of hexagon 1 for the case of 3L-VSI (top) and 3L-ZSI (bottom) operating under MBC approach of voltage boosting.

When the ULST scheme of ST insertion is used with a single LC IN, the relationship between ST duty cycle and modulation index 'M' for 3L-ZSI using MBC approach can be written as [4]:

$$D_{MBC} = \frac{T_o}{T_s} = \left(\frac{2\pi - 3\sqrt{3}M}{2\pi}\right) \tag{3.9}$$

$T_o = T_z$ for the case of MBC and D_{MBC} is the ST duty ratio offered by the MBC approach.

T_o and T_z are the total duration of ST states and the total duration of equivalent null state per sample, respectively

3.6.2. MCB and SBC

The switching pattern within a sample is the same using SBC and MCB approach.

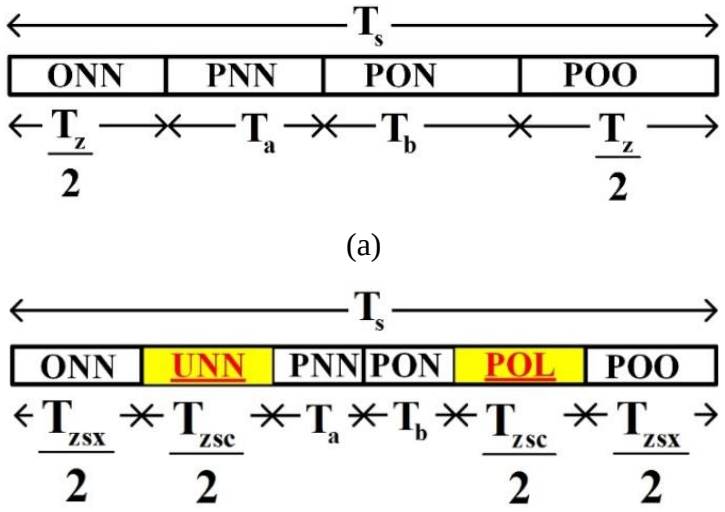


Fig. 3.7. Switching states pattern in the inner subsector I of hexagon 1, (a) case of 3L-VSI, (b) sample when MCB/SBC method applied to 3L-ZSI.

For the inner subsector I of hexagon 1, Fig. 3.7(a) shows the switching pattern for the case of 3L-VSI, and Fig. 3.7(b) shows the modified sample when MCB/SBC voltage boosting approaches of ZSI are applied. Both the switching pattern of Fig. 3.7 causes only 6 switching transitions per sample. In Fig. 3.7, 'T_{zsx}'and 'T_{zsc}' are the duration of equivalent null states and ST states per sample. For the outer subsector II of hexagon 1, Fig. 3.8(a) shows a conventional switching pattern of 3L-VSI. In the same region, the existing switching state pattern of 3L-ZSI used by [70], [77] is shown in Fig. 3.8(b). The switching pattern of Fig. 3.8(b) causes 8 switching transitions. Fig. 3.8(c) shows the proposed switching pattern of a sample in the same region. The proposed switching pattern shown in Fig. 3.8(c) causes 7 switching transitions per sample. Similarly, in all outer subsectors of each hexagon, the proposed switching pattern offers the saving of one switching transition per sample.

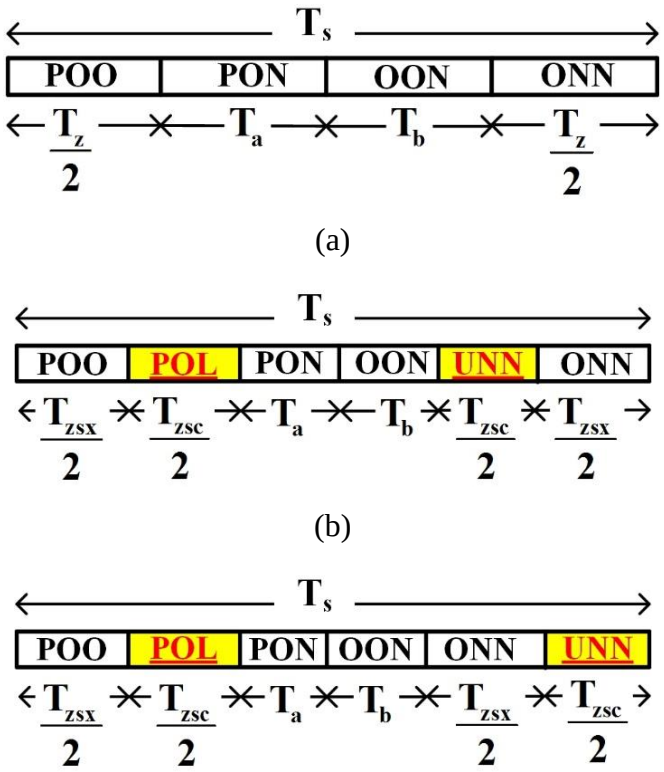


Fig. 3.8. Switching states pattern in the outer subsector II of hexagon 1, (a) case of 3L-VSI, (b) existing MCB/SBC switching pattern of 3L-ZSI [70], [77], (c) proposed MCB/SBC pattern of switching state in the same region.

Considering the conditions of NTV switching, use of only equivalent null states for the ST state insertion, and MCB/SBC method of voltage boosting, it is impossible to achieve the switching transition less than 7 in the outer subsectors of each hexagon in 3L-ZSI. Using the proposed SVPWM switching pattern, the average switching frequency of the inverter switches has been calculated considering 66 number of samples over the fundamental line cycle. Table 3.9 shows the summary of the average switching frequency of each switch for the MBC and MCB/SBC method at different values of the carrier frequency and modulation index. It can be noticed from Table 3.9 that, for a particular value of carrier frequency, the switching frequency is subjected to change with the change in modulation index. The reason behind this is, as the modulation index decreases, the outer subsectors of each hexagon have more samples (shown in Table 3.6). The switching frequency of the inverter switches is more in the outer subsectors as compared to the inner

subsectors of interest (Table 3.7 and Table 3.8). So, if the modulation index decreases, the average switching frequency of the inverter switches will increase.

Table 3.9. Calculation of average switching frequency of CDBC 3L-ZSI

Carrier freq. (F_c) in kHz. (total no. of samples over the fundamental cycle)	'M'	Average F_{sw}(Hz)		Average F_{sw}(Hz)	
		MCB/SBC		MBC	
		SX1=SX3	SX2	SX1=SX3	SX2
1.65 (66)	1	900	1700	350	1700
	0.866	1000		550	
	0.73	1100		750	
	0.67	1150		850	
5.25 (210)	1	2850	5300	1250	5300
	0.866	3000		1550	
	0.73	3300		2150	
	0.67	3550		2650	
10.65 (426)	1	5700	10700	2450	10700
	0.866	6050		3150	
	0.73	6650		4350	
	0.67	7150		5350	

For the ULST scheme of voltage boosting using a single LC IN, the relationship between ST duty cycle and modulation index for MCB is written as:

$$D_{MCB} = \frac{T_o}{T_s} = \frac{1}{2}\left(1 - \frac{\sqrt{3}M}{2}\right) \quad (3.10)$$

$T_o = T_{zsc}$ for the case of MCB. D_{MCB} is the ST duty ratio offered by the MCB approach of voltage boosting.

3.7. COMPARISON OF PROPOSED AND EXISTING SVPWM SWITCHING PATTERNS

The existing switching patterns presented in [70], [77] falls in the category of MCB/SBC category. Therefore, only the MCB/SBC category of the proposed switching pattern is compared with the

existing SVPWM switching patterns of [70], [77] in terms of switching frequency of the power switches, power losses, and total harmonic distortion (THD) in the output line voltage. The inverter configuration is considered the same i.e. CDBC ZSI is used for both cases.

3.7.1. Comparison in terms of switching frequency

The switching frequency of the inverter switches using existing and proposed switching patterns has been calculated for the different cases of carrier frequency considering the MCB/SBC approach of voltage boosting (shown in Table 3.10). From Table 3.10, it can be seen that, as the carrier frequency increases, the difference between the switching frequency offered by proposed and existing SVPWM technique increases. The switching transitions during hexagon to hexagon changeover have also been taken into account to have the exact value of switching frequency. Consider a case of Table 3.10, when the carrier frequency is 10.65 kHz and the modulation index is 1. At this condition, switching frequency (upper and lower switch of each phase leg) using the proposed and existing SVPWM technique is 5700Hz and 6025Hz, respectively. A reduction of 325Hz per switch has been achieved using the proposed technique. This indicates that the proposed SVPWM pattern (for inner and outer subsector shown in Fig. 3.7(b) and Fig. 3.8(c), respectively) is advantageous at a higher modulation index also.

Table 3.10. Comparison of switching frequency of power switches between proposed and existing SVPWM technique

Carrier freq. (F_c) in kHz. (total no. of samples over the fundamental. cycle)	'M'	Proposed SVPWM		Existing SVPWM [70], [77]	
		Average F_{sw}(Hz)		Average F_{sw}(Hz)	
		SX1=SX3	SX2	SX1= SX3	SX2
1.65 (66)	1	900	1700	900	1700
	0.866	1000		1100	
	0.73	1100		1300	
	0.67	1150		1400	
5.25 (210)	1	2850	5300	3025	5300
	0.866	3000		3325	

	0.73	3300		3925	
	0.67	3550		4425	
10.65 (426)	1	5700	10700	6025	10700
	0.866	6050		6725	
	0.73	6650		7925	
	0.67	7150		8925	

3.7.2. Power Losses

The conduction and switching losses are the two main contributors to the total power losses in the inverter. For a pulsed output voltage and current, the average conduction losses per sample in IGBT and diode can be calculated as:

$$P_{cond,IGBT} = V_{ce}(T_j, I_c) \times I_c \times T \quad (3.11)$$

$$P_{cond,Diode} = V_f(T_j, I_f) \times I_f \times T \quad (3.12)$$

Where V_{ce} is collector-emitter saturation voltage, I_c is the forward current through IGBT, V_f is the forward voltage drop across the diode, I_f is the forward current through the diode, T_j is the junction temperature, and T is the ON time duration.

The switching losses can be further classified into the turn on and turn off energy losses. The total switching losses in the case of IGBT can be defined as:

$$P_{sw,IGBT} = (E_{on} + E_{off}) \times F_{sw} \quad (3.13)$$

E_{on}, E_{off} are the energy loss during turn on and turn off transitions, respectively.

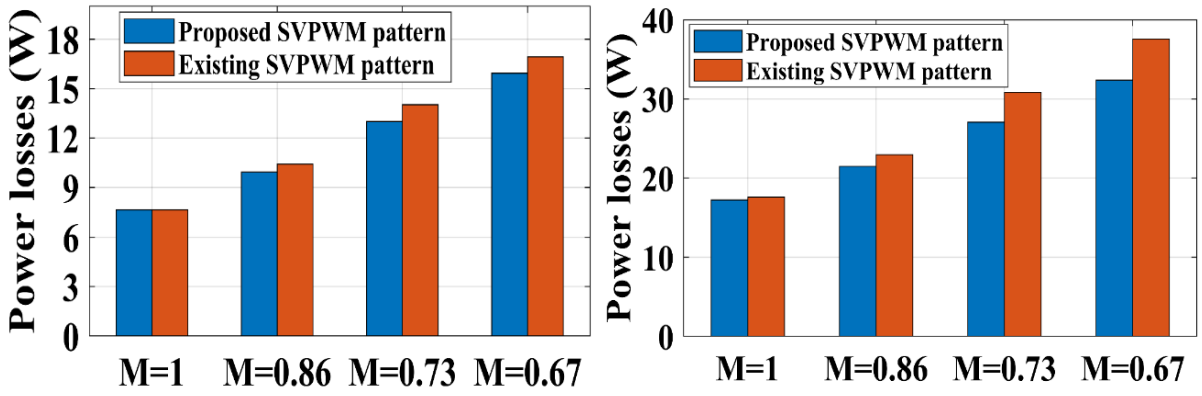
Only turn off losses (reverse recovery losses) have been considered in the case of diodes. These can be written as:

$$P_{rec,diode} = E_{rec} \times F_{sw} \quad (3.14)$$

E_{rec} is the reverse recovery energy loss of the diode

The power losses have been calculated with the help of datasheets of IGBT and diode. The total power losses using the proposed and the existing SVPWM technique have been plotted in Fig. 3.9. Fig. 3.9(a) and (b) shows the total power losses of the inverter at the carrier frequency of 1.65 kHz and 5.25 kHz, respectively. It is clear from these figures that, for any particular value of carrier

frequency, as the modulation index decreases, the difference between the total power loss of the proposed and existing SVPWM technique increases.



(a) (b)

Fig. 3.9. Comparison of power loss between the proposed and the existing SVPWM technique at a carrier frequency of, (a) 1.65 kHz, (b) 5.25 kHz.

3.7.3. Comparison in terms of THD

Since the proposed SVPWM technique offers reduced switching frequency as compared to the existing, it becomes necessary to check the effect on the total harmonic distortion (THD) of the output line voltage/current. The FFT tool of the MATLAB/SIMULINK is used to investigate the THD content in the output line voltage/current. The reported values of the THD content have been tabulated in Table 3.11 from where it can be noticed that the THD percentage in the output line voltage/current is the same using the proposed and exiting SVPWM technique.

Table 3.11. Comparison in terms of THD percentage

Modulation index 'M'	Existing SVPWM [70], [77] under MCB approach		Proposed SVPWM under MCB approach	
	Voltage THD %	Current THD %	Voltage THD %	Current THD %
1	35.23	35.26	35.23	35.26
0.86	40.14	40.17	40.14	40.16
0.73	43.24	43.19	43.51	43.55
0.67	44.91	44.87	45.92	45.94

3.8. IMPEDANCE NETWORK DESIGN GUIDELINES

The IN inductors and capacitors have been designed based on the high-frequency ripple components of the inductor current and capacitor voltage, respectively. The high-frequency inductor ripple components for MBC and MCB approach of voltage boosting can be written as:

$$\Delta i_{L\_MBC} = \frac{V_C}{L}(D_{MBC}.T_s) \tag{3.15}$$

$$\Delta i_{L\_MCB} = \frac{V_C}{L}\left(\frac{D_{MCB}.T_s}{2}\right) \tag{3.16}$$

Expression of V_C is given in equation (3.1). The expressions of ST duty ratio for MBC (D_{MBC}) and MCB (D_{MCB})approaches are given in equation (3.9) equation (3.10), respectively. The permissible value of inductor current ripple is defined as:

$$\Delta i_L = r_L.I_L \tag{3.17}$$

r_L is the permissible percentage of the average inductor current ripple.

I_L is the average inductor current and it can be expressed as:

$$I_L = \frac{P}{V_{dc}} \tag{3.18}$$

Similarly, the high-frequency capacitor voltage ripple during MBC and MCB approach can be written as:

$$\Delta V_{C\_MBC} = \frac{I_L}{C}(D_{MBC}.T_s) \tag{3.19}$$

$$\Delta V_{C\_MCB} = \frac{I_L}{C}\left(\frac{D_{MCB}.T_s}{2}\right) \tag{3.20}$$

The permissible value of capacitor voltage ripple is defined as:

$$\Delta V_C = r_C.V_C \tag{3.21}$$

r_C is the permissible percentage of average capacitor voltage ripple and V_C is the average value of the capacitor voltage. Final expressions for the IN inductor and capacitor have been summarized in Table 3.12.

Table 3.12. Expressions of 'L' and 'C' of IN for MBC and MCB approach of voltage boosting

MBC	MCB

$L = \frac{(1 - D_{MBC}).V_{dc}.(2\pi - 3\sqrt{3}M)T_s}{2.\pi.(1 - 2D_{MBC}).r_L.I_L}$	$L = \frac{(1 - D_{MCB}).V_{dc}.(2 - \sqrt{3}M)T_s}{8.(1 - 2.D_{MCB}).r_L.I_L}$
$C = \frac{I_L.(1 - 2.D_{MBC}).(2\pi - 3\sqrt{3}M).T_s}{2.\pi.V_{dc}.r_c.(1 - D_{MBC})}$	$C = \frac{I_L.(1 - 2.D_{MCB}).(2 - \sqrt{3}M).T_s}{8.V_{dc}.r_c.(1 - D_{MCB})}$

3.9. RESULTS

The configuration of CDBC 3L-ZSI and its PWM technique has been validated using simulation as well as a laboratory prototype. The parameter values have been mentioned in Table 3.13.

Table 3.13. Parameters used for experimental validation

Simulation/ Exp. Parameters	Values/Name
Input dc source (V_{dc})	230V
IN inductors, capacitors	6mH, 2200uF
Software used/Sample time of simulation/Solver used	Matlab Simulink /1usec./ Fixed step discrete
Load	Resistive, 30Ω per phase
Number of samples	11 per equivalent 2L hexagon

3.9.1. Simulation Results

Since the practical feasibility of the proposed SVPWM technique is an important concern, the simulation waveforms of gating pulses have been shown in Fig. 3.10 to compare them later with the experimental waveforms. The simulation waveforms of the gating signal are shown in Fig. 3.10(a-c) and Fig. 3.10(d-f) for the MBC and MCB approach of voltage boosting, respectively. From the waveforms of Fig. 3.10, it can be seen that, either SA1 works in conjunction with SA2 or SA3 work in conjunction with SA2. The switching frequency of the bidirectional switch ‘SA2’ is more as compared to the upper switch (SA1) and lower switch (SA3) of the same phase leg.

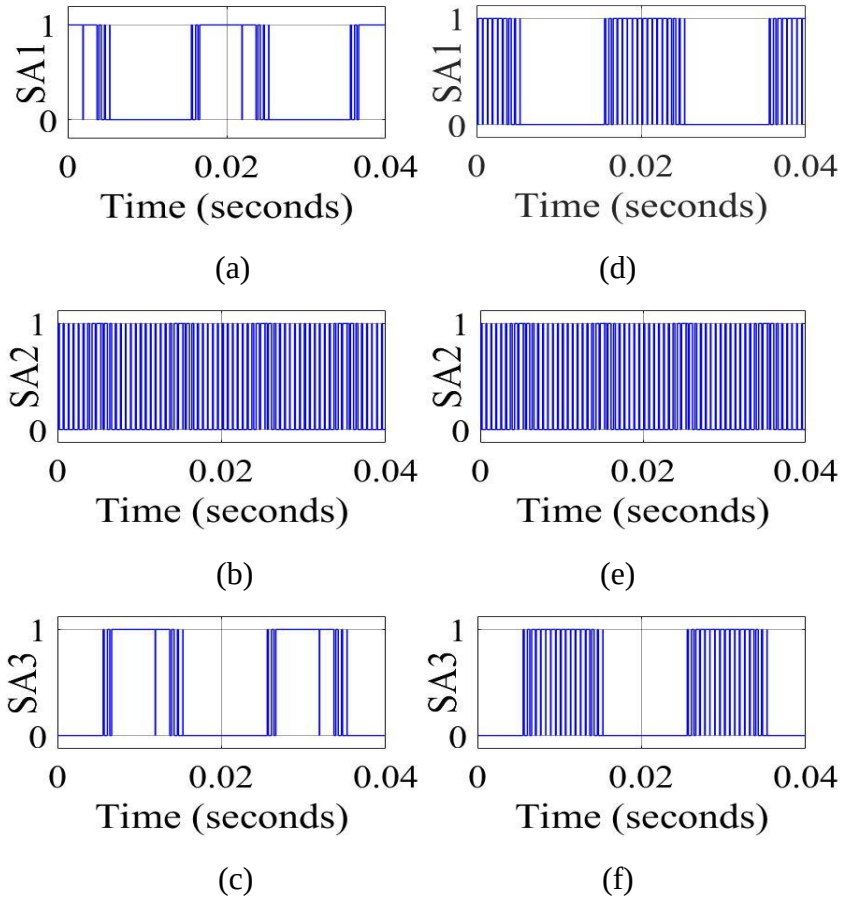


Fig. 3.10. Simulation waveforms of gating signal for the switches of 'a' phase leg at 'M=1' using, (a-c) MBC approach, (d-f) MCB approach.

3.9.2. Experimental Results

The laboratory prototype of the CDBC 3L-ZSI, having power rating of 1200W is shown in Fig. 3.11. The DSP320F28379D microcontroller has been used for the generation of gating pulses.

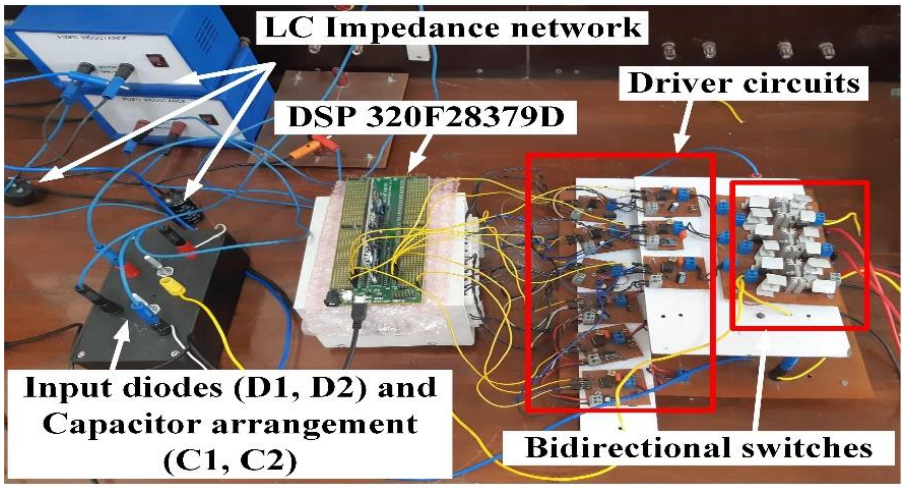
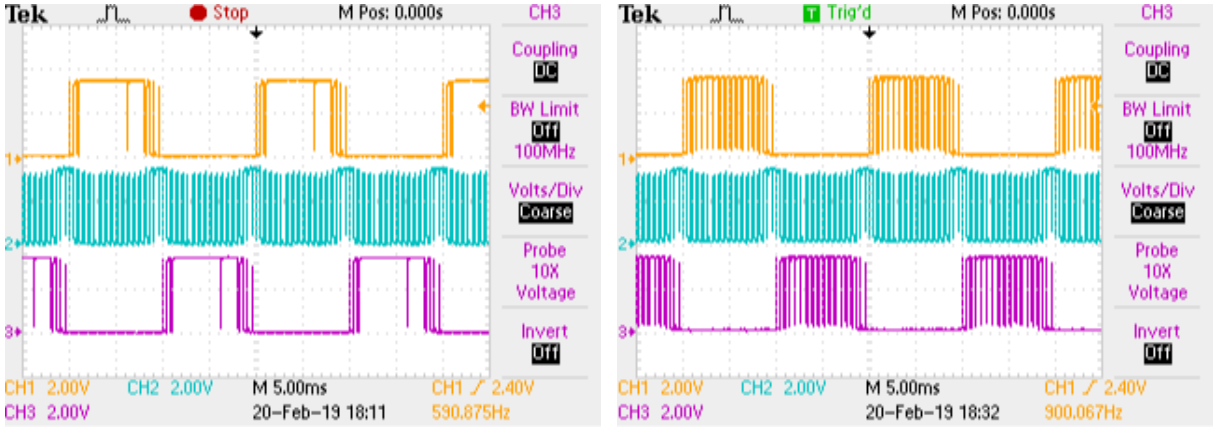


Fig. 3.11. Photograph of CDBC 3L-ZSI prototype.

The experimental pattern of the gating pulses for the three switches of 'a' phase leg is shown in Fig. 3.12 for the case of the MBC and MCB approach, respectively. The experimental pattern of gating pulses is same as that of the simulation result waveforms shown in Fig. 3.10. This ensures that the proposed SVPWM technique is feasible for the practical application point of view.

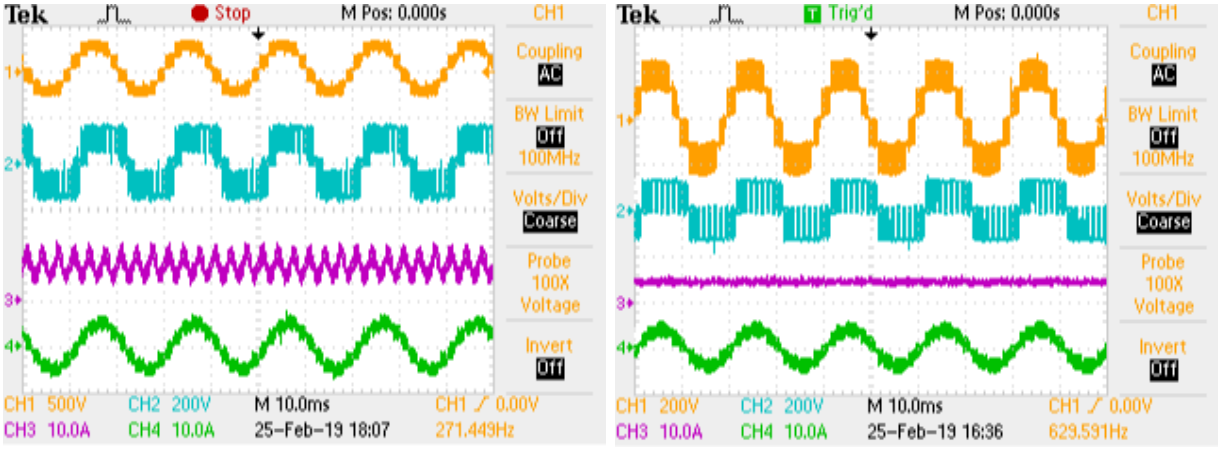


(a) (b)

Fig. 3.12. Gating pulses for the switches SA1, SA2, SA3 of 'a' phase leg at 'M'=1 (a) MBC approach (b) MCB approach.

Fig. 3.13(a) and (b) shows the experimental waveform of the line voltage (V_{ab}), pole voltage (V_{an}), inductor current (I_L) and line current (I_a) for MBC and MCB approaches, respectively. From Fig. 3.13 it is clear that the line voltage follows the NTV switching for both cases. For 'M=1', the boost factor 'B' offered by the MCB and MBC approach is equal to 1.15 and 1.52, respectively. The line voltage has a peak of around 350V when the MBC approach is used. This value matches with the

predicted theoretical value according to the equation $'B.V_{dc}'$. Similarly, the line voltage has a peak of around 260V using the MCB approach.



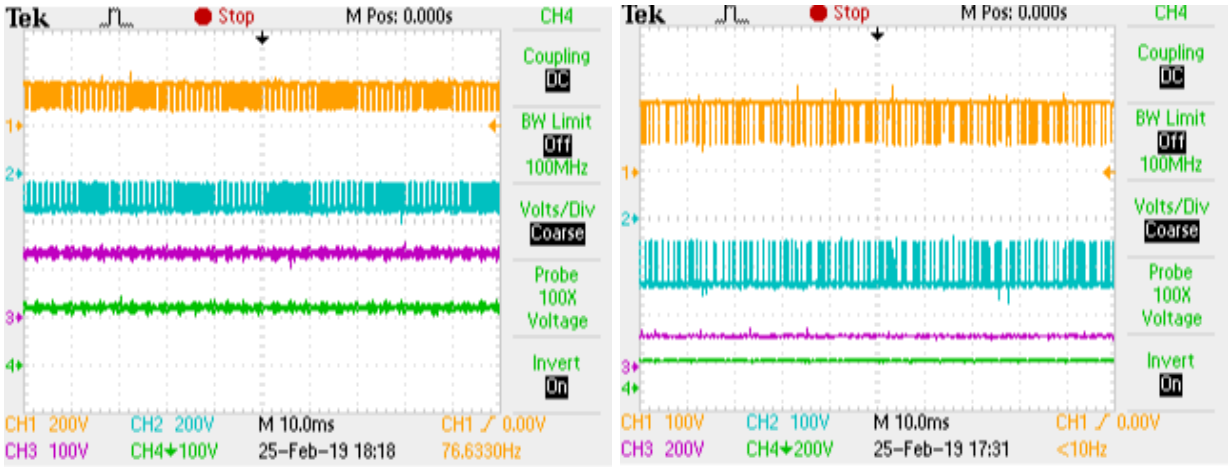
(a) (b)

Fig. 3.13. Experimental result waveforms of CDBC ZSI using MBC and MCB approach of voltage boosting at M=1, (a) MBC approach (b) MCB approach, (From Top: line voltage (V_{ab}) , pole voltage(V_{an}), inductor current (I_L), line current (I_a).

The theoretical value of peak pole voltage can be estimated by equation $(0.5.B.V_{dc})$. The experimental value of peak pole voltage comes around 170V and 130V for MBC and MCB approaches, respectively. These values matches with the expected theoretical values. Since the total duration of the equivalent null state is used for the insertion of the ST state in the MBC approach, the inductor current contains the sixth fundamental frequency ripple components (see Fig. 3.13). This is because the period of the equivalent null state is one-sixth of the fundamental period. On the other hand, the inductor current is smooth when the MCB approach is used. The reason behind the smooth inductor current in the MCB approach is that, ST time duration is constant throughout the fundamental line cycle. As the load is resistive, the line current is in phase with the line voltage in both cases.

Fig. 3.14(a) and Fig. 3.14(b) shows the experimental waveform of the input capacitor voltages (V_{C1}, V_{C2}), upper dc-link voltage (V_{px}) and lower dc-link voltage (V_{nx}). The input capacitor voltages are balanced in both approaches of voltage boosting. The upper dc-link voltage (V_{px}) has a peak of around 170V and 130V during MBC and MCB approaches, respectively. Similarly, the lower dc-link voltage (V_{nx}) has a peak of '-170V' and '-130V' for MBC and MCB approach,

respectively. Hence, the experimental results validate the CDBC ZSI inverter configuration and the proposed SVPWM technique.



(a) (b)

Fig. 3.14. Experimental result waveforms of CDBC 3L-ZSI using MBC and MCB approach of voltage boosting at M=1 (a) MBC approach (b) MCB approach, (From Top: upper dc-link voltage (V_{px}) ,lower dc-link voltage (V_{nx}), input capacitor voltage (V_{C1}, V_{C2}).

Fig. 3.15 shows the efficiency curves of CDBC 3L-ZSI when operated with the proposed and existing SVPWM switching patterns at the carrier frequency of 1.65 kHz. It can be concluded from Fig. 3.15 that the proposed SVPWM pattern offers slightly better efficiency as compared to the existing SVPWM technique.

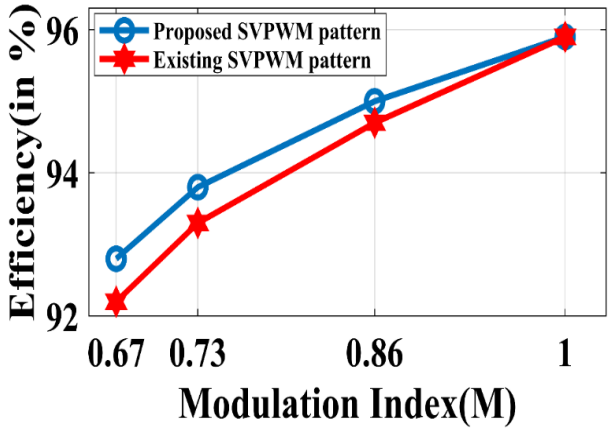


Fig. 3.15. The efficiency of CDBC 3L-ZSI using proposed and existing SVPWM technique at a carrier frequency of 1.65 kHz.

3.10. CONCLUSION

In this chapter, the working of CDBC 3L-ZSI has been verified using a laboratory prototype. This configuration offered a reduced number of semiconductor switches and associated gate driver circuit components when compared to NPC and T-type 3L-ZSI. The proposed SVPWM switching pattern effectively utilizes the freedom of switching state selection offered by the space vector approach to optimize the number of switching transitions per sample over a fundamental period. For a particular value of carrier frequency, the proposed switching pattern results in the minimum switching frequency of power switches in a similar category of existing sine triangle and space vector-based approaches. This results in reduced power losses and improved efficiency of 3L-ZSI. The output voltage/current THD is unaffected. The dependency of the average switching frequency of the power switches on the modulation index of the 3L-ZSI has been highlighted. The proposed SVPWM switching pattern is equally applicable to NPC and T-type 3L-ZSI.

CHAPTER 4. IMPROVED MAXIMUM BOOST CONTROL OF VOLTAGE BOOSTING AND REDUCED CMV SWITCHING PATTERNS FOR 3L-ZSI

4.1. INTRODUCTION

The maximum boost control (MBC) approach of voltage boosting offers the highest gain among other boost control approaches of ZSI. But this approach suffers from the lower order ripple components of the IN inductor current. For example, the experimental results waveforms of chapter 3 shows that the CDBC 3L-ZSI causes sixth fundamental frequency (6^{th} F1) IN inductor current ripple when operated under the MBC approach of voltage boosting. This drawback causes the increased size of the IN components and thereby limits the practical applications of the MBC. The main reason behind this drawback is that, in this approach, the complete null interval of each sample is fully replaced by ST states. The null interval always changes with frequency equals to six times the fundamental frequency in 2L as well as 3L-VSI/ZSI.

In this chapter, an improved MBC (IMBC) has been proposed by modifying the conventional SVPWM switching state diagram of 3L-ZSI. The modified SVPWM doubles the frequency of the null interval as compared to the conventional SVPWM. This helps in eliminating the problem of 6^{th} F1 ripple components of inductor current prevailing in existing MBC.

Next, the magnitude and the rate of change of CMV is an important concern when inverters are used in motor drives or any distributed power generation application. The major problems associated with the CMV are ground leakage current in PV power generation, shaft voltage, bearing currents, and electromagnetic interference (EMI) in motor drive applications [66], [67], [68]. The existing reduced CMV techniques of 3L-ZSI /q-ZSI have been analyzed based on some important factors. Their detailed analysis is summarized in Table 4.1.

Table 4.1. Analysis of existing reduced CMV PWM techniques of 3L-ZSI

Existing techniques	Merits	Demerits	Remarks
Origin shifted 60 degree discontinuous of [62]	➢ NTV switching ➢ CMV limited to $V_{dc}/6$	➢ Unbalanced inductor voltage boosting per carrier cycle ➢ Large inductor size requirement	➢ Used either upper or lower ST state in a sample
APOD of [63], [64]	➢ CMV limited to $V_{dc}/6$ ➢ Balanced inductor voltage boosting per carrier cycle	➢ Non -NTV switching ➢ Require synchronization of two-phase legs for ST insertion if minimum six switching transitions per sample are desired	➢ Used Full dc-link ST state, 1 per half carrier cycle
RCM of [65], [66]	➢ Ideally zero CMV ➢ Balanced inductor voltage boosting per carrier cycle	➢ Increased switching transitions (12 per sample) ➢ Non-NTV switching ➢ Large switching vectors are unused. This leads to underutilization of available dc-link	➢ Used Full dc-link ST state, 2 per sample
Switching technique of [67], [68]	➢ CMV limited to $V_{dc}/6$ ➢ Balanced inductor voltage boosting per carrier cycle	➢ Increased switching transitions (8 per sample) ➢ Non-NTV switching	➢ Used Full dc link ST, 1 per sample

Two new switching patterns of reduced CMV PWM techniques have been proposed in this chapter to avoid the following major demerits of the existing techniques.

- Unbalanced inductor voltage boosting per carrier cycle as in origin shifted 60 degree discontinuous of [62]
- Increased number of switching transitions per sample as in the reduced CMV technique of [65], [66] and switching technique of [67], [68]
- Increased complexity of implementation of ST state arises due to phase legs synchronization as in alternate phase opposition disposition (APOD) of [63], [64]
- Increased size of IN because of the its lower switching frequency [62], [63], [64], [67], [68]
- The complexity of overall implementation as the sine- triangle comparison approach of PWM generation require several reference signals for the generation of gating pulses

The operation of IMBC of voltage boosting with proposed reduced CMV switching patterns when used in 3L-ZSI results in reduced CMV magnitude (limited to one-sixth of available dc-link), reduced size of IN, increased dc bus utilization, and ease of implementation of ST states. The above-mentioned findings have been successfully validated using theoretical analysis, simulation, and experimental results.

4.2. 3L-ZSI

The configuration of CDBC 3L-ZSI already discussed in chapter 3 (Fig. 3.3) is used here for the verification of IMBC and new reduced CMV switching patterns.

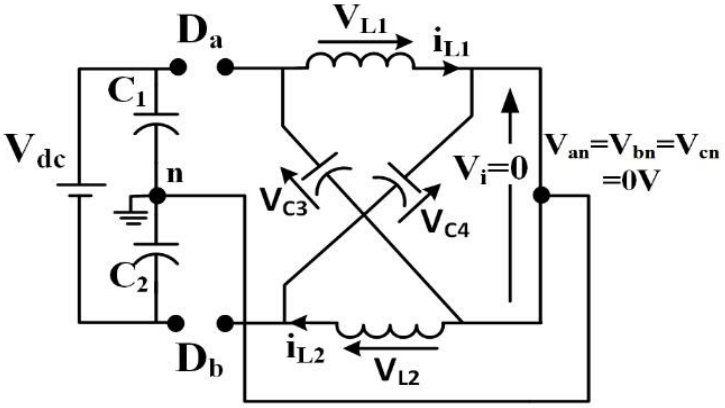


Fig. 4.1. Equivalent circuit diagram of 3L-ZSI during FST state.

The switching states and their corresponding switching position of the inverter configuration has been explained in Table 3.4 of chapter 3. The approach of FST [63] has been used for the insertion of ST states. The equivalent circuit diagram of 3L-ZSI during the FST state is shown in Fig. 4.1. Used ST vectors and their generated pole/line voltage and CMV have been tabulated in Table 4.2. These vectors produce zero pole/line voltage and zero CMV irrespective of the switching position of the individual phase legs.

Table 4.2. Description of the used ST vectors

ST vectors	Pole Voltage	Line Voltage	CMV
FON, OPF, NFO, FOP, ONF, PFO, POF, OFN, FPO, NOF, OFP, FNO	$V_{an} = V_{bn} = V_{cn} = 0$	$V_{ab} = V_{bc} = V_{ca} = 0$	$V_{cmv} = 0$

A quick review of the applicable formulas for the 3L-ZSI operating under the FST approach (considering $L_1 = L_2 = L\,;\ C_3 = C_4 = C$) is given as under [4]:

Peak dc-link voltage ($\hat{v}_i$):

$$\hat{v}_i = \left(\frac{1}{1 - 2.D}\right) V_{dc} = B.V_{dc} \tag{4.1}$$

$$B = \frac{1}{1 - 2.D} \tag{4.2}$$

'D' and 'B' are ST duty ratio and boost factor, respectively.

The voltage gain 'G' of the inverter and the switching stress across inverter switches 'V_s'can be expressed as:

$$G = M.B \tag{4.3}$$

'M' is the modulation index.

$$V_s = B.V_{dc} \tag{4.4}$$

The CMV is defined as:

$$V_{cmv} = \frac{V_{an} + V_{bn} + V_{cn}}{3} \tag{4.5}$$

where V_{an}, V_{bn}, V_{cn} are the pole voltages.

4.3. PROPOSED MODIFIED SVPWM

The conventional SVPWM and the proposed modified SVPWM technique differs in the length and dwell time duration of the switching vectors. This is explained as follows.

4.3.1. A brief review of conventional SVPWM

The switching state diagram of conventional SVPWM has been shown in Fig. 4.2.

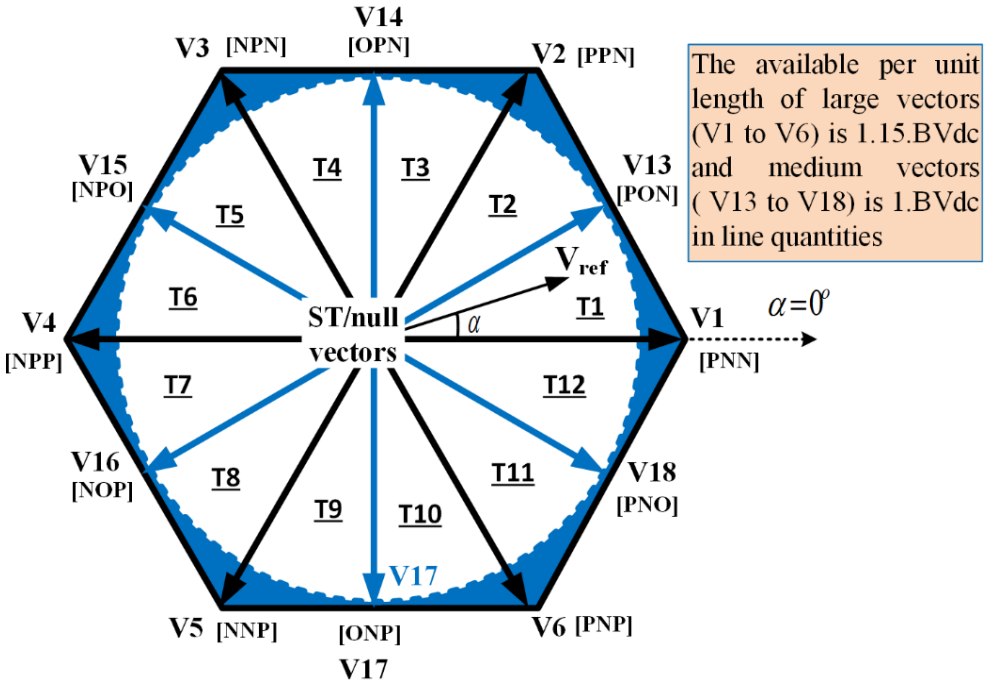


Fig. 4.2. Conventional SVPWM switching diagram of 3L-ZSI [15].

For the reference sinusoidal line voltages of peak equal to $1.\,BV_{dc}$, the magnitude of the resultant signal is always constant (i.e. $1.\,BV_{dc}$). This is shown in Fig. 4.3. Mathematically, these reference line voltage signals can be written as

$$V_{ab} = \sin\left(2\pi/3 + \alpha\right) \tag{4.6}$$

$$V_{bc} = \sin(\alpha) \tag{4.7}$$

$$V_{ca} = \sin\left(4\pi/3 + \alpha\right) \tag{4.8}$$

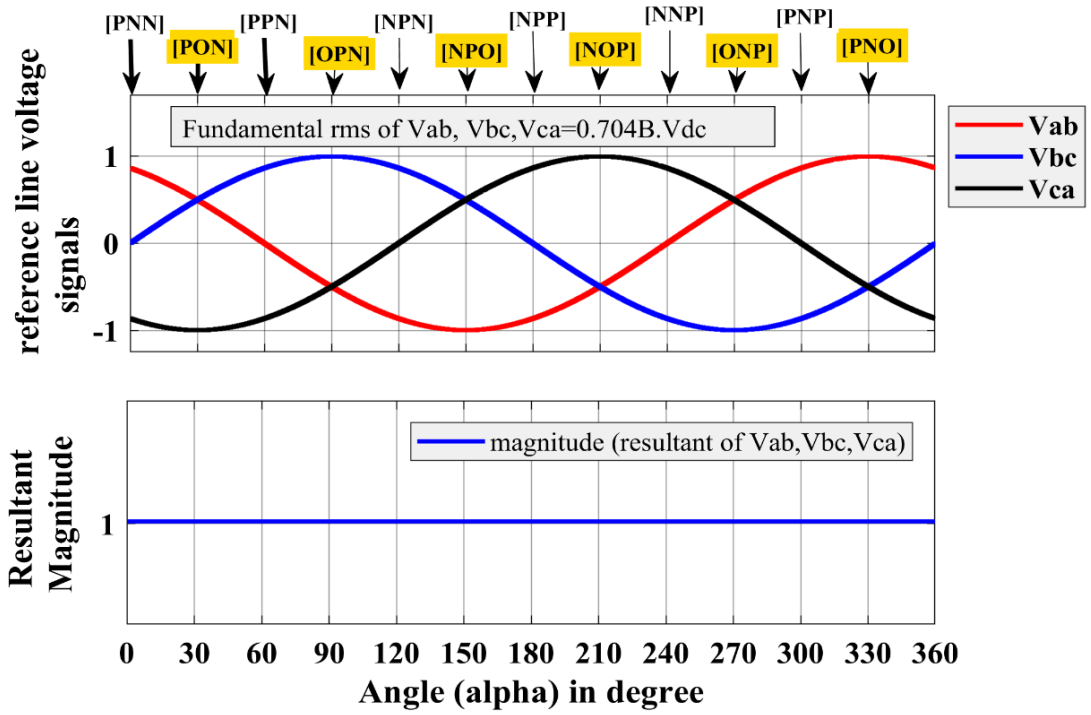


Fig. 4.3. Reference three phase line voltage signals and their resultant magnitude of the conventional SVPWM.

As per Clark's transformation, the calculated lengths (line quantities) of large (V1-V6) and medium (V13-V18) switching vectors are $1.154.\,\mathrm{BV_{dc}}$ and $1.\,\mathrm{BV_{dc}}$, respectively.

As seen in Fig. 4.2, the maximum available value of the reference vector ($\mathrm{V_{ref}}$) magnitude is equal to the length of the medium vector.

$$\mathrm{V_{ref,max}} = 1.\,\mathrm{BV_{dc}} \tag{4.9}$$

The modulation index, in this case, is defined as per[95]

$$\mathrm{M_{ex}} = \frac{2.\,\mathrm{V_{ref}}}{\sqrt{3}.\,\mathrm{BV_{dc}}} \tag{4.10}$$

The formula of modulation index is different here when compared to the equation (2.4) because the considered length of large and medium vector is 1.15 and 1 per unit dc-link. On the other hand, in equation (2.4) the considered length of large and medium vectors is 1 and 0.866 per unit dc-link. However, both implementation are correct and gives the same value of modulation index.

The maximum modulation index can be found by substituting (4.9) into (4.10). It comes

$$M_{ex,(max)} = 1.154 \tag{4.11}$$

The maximum available rms value of the fundamental line voltage can be expressed as:

$$V_{ab,rms}(max) = \frac{\sqrt{3}}{2\sqrt{2}} M_{ex,(max)}.BV_{dc} \tag{4.12}$$

Substituting (4.11) into (4.12), yields

$$V_{ab,rms}(max) = 0.707.BV_{dc} \tag{4.13}$$

The conventional SVPWM approach has been used in [67] for 3L-ZSI where the dwell time of switching vectors in triangle T1 have been calculated using the following formulas

$$T_{a\_ex} = \left(\frac{V_{ref}}{1.15.BV_{dc}}\right)\left(\frac{Sin(\pi/6 - \alpha)}{Sin(\pi/6)}\right).T_s \tag{4.14}$$

$$T_{b\_ex} = \left(\frac{V_{ref}}{1.BV_{dc}}\right)\left(\frac{Sin(\alpha)}{Sin(\pi/6)}\right).T_s \tag{4.15}$$

$$T_{z\_ex} = T_s - T_{a\_ex} - T_{b\_ex} \tag{4.16}$$

T_{a_ex}, T_{b_ex} are the active vector time durations, T_{z_ex} is the time duration of the null vector and T_s is the time duration of one sample. As shown in Fig. 4.4, the null interval (T_{z_ex}) changes six times the fundamental frequency in this case.

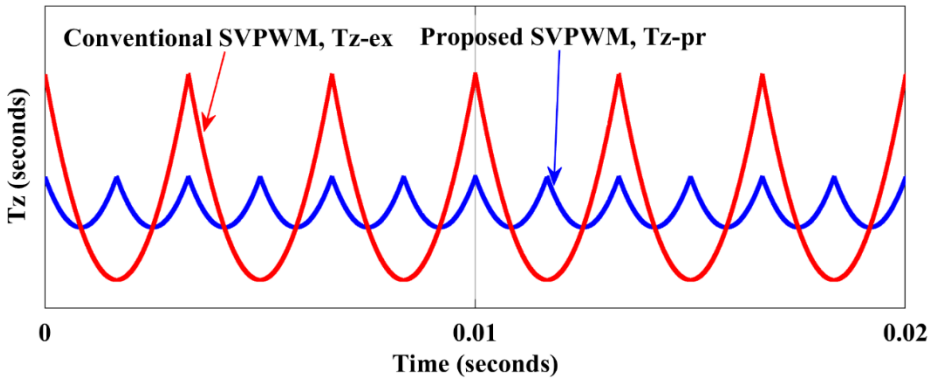


Fig. 4.4. Variation of the null interval over the fundamental cycle using conventional and proposed SVPWM.

4.3.2. Proposed modified SVPWM

The proposed modified SVPWM switching diagram is shown in Fig. 4.5. The objective of the proposed SVPWM is to double the frequency of the null interval as compared to the conventional

SVPWM. It is possible only if the length of large and medium switching vectors is equal. For this purpose, the required reference line voltage signals have been modified (shown in Fig. 4.6).

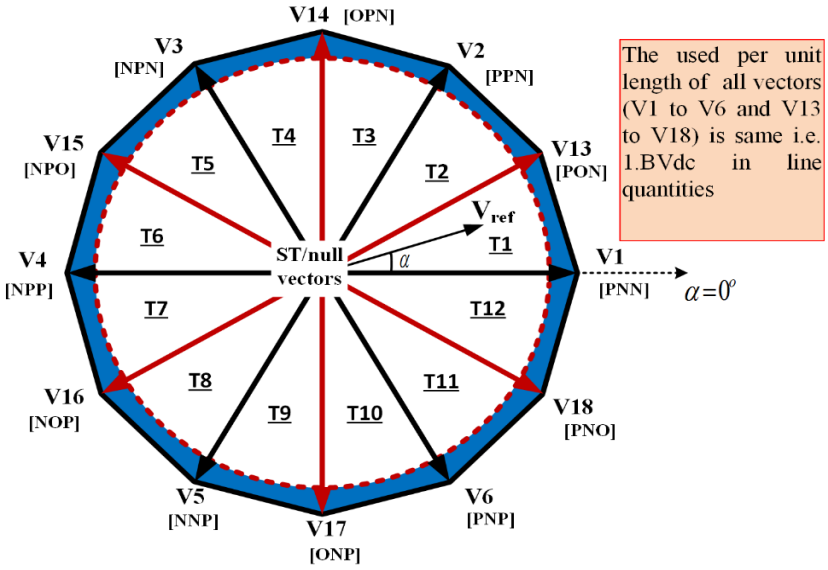


Fig. 4.5. Proposed 12 sided polygon of 3L-ZSI

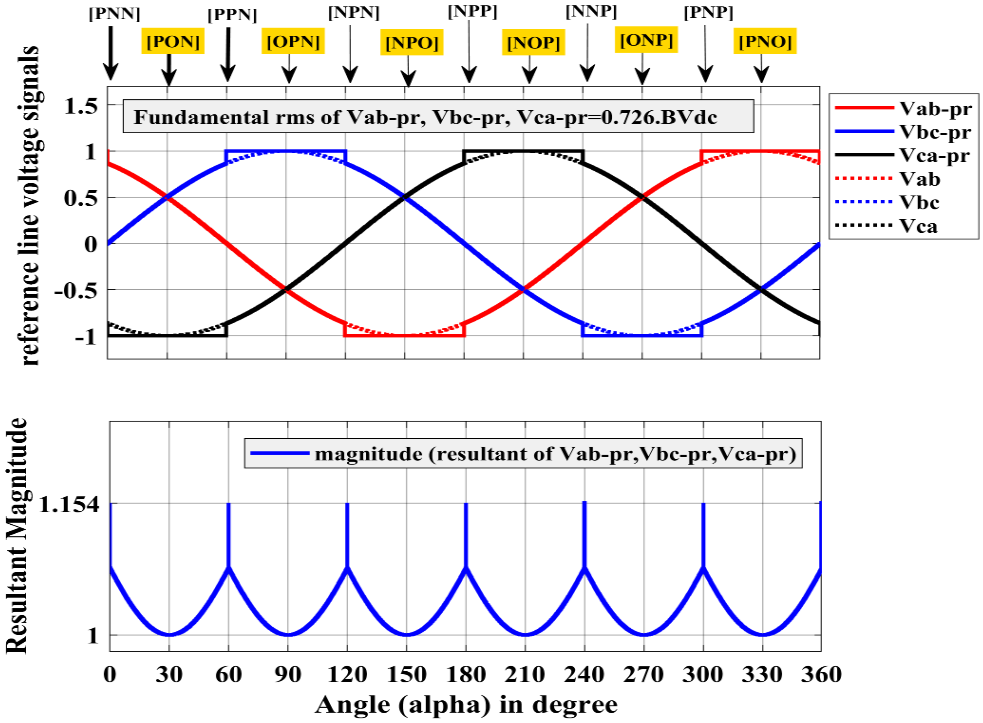


Fig. 4.6. Proposed modified reference three phase line voltage signals and their instantaneous resultant signal magnitude (IRSM).

Mathematically, the proposed modified reference line voltage signals can be written as:

$$V_{ab,pr} = \left[\left\{\sin\left({}^{2\pi}/_{3} + \alpha\right)\right\}\right]_{\alpha=0 \text{ to } \frac{2\pi}{3};\ \pi \text{ to} \frac{5\pi}{3};} + \left[\left\{\sin\left({}^{3\pi}/_{2}\right)\right\}\right]_{\alpha=\frac{2\pi}{3} \text{ to } \pi} + \left[\left\{\sin\left({}^{\pi}/_{2}\right)\right\}\right]_{\alpha=\frac{5\pi}{3} \text{ to } 2\pi} \quad (4.17)$$

$$V_{bc,pr} = \left[\left\{\sin(\alpha)\right\}\right]_{\alpha=0 \text{ to } \frac{\pi}{3};\ \frac{2\pi}{3} \text{ to} \frac{4\pi}{3};\ \frac{5\pi}{3} \text{ to } 2\pi} + \left[\left\{\sin\left({}^{\pi}/_{2}\right)\right\}\right]_{\alpha=\frac{\pi}{3} \text{ to } \frac{2\pi}{3}} + \left[\left\{\sin\left({}^{3\pi}/_{2}\right)\right\}\right]_{\alpha=\frac{4\pi}{3} \text{ to } \frac{5\pi}{3}} \quad (4.18)$$

$$V_{ca,pr} = \left[\left\{\sin\left({}^{4\pi}/_{3} + \alpha\right)\right\}\right]_{\alpha=\frac{\pi}{3} \text{ to } \pi\ ;\ \frac{4\pi}{3} \text{ to } 2\pi\ ;} + \left[\left\{\sin\left({}^{3\pi}/_{2}\right)\right\}\right]_{\alpha=0 \text{ to } \frac{\pi}{3}} + \left[\left\{\sin\left({}^{\pi}/_{2}\right)\right\}\right]_{\alpha=\pi \text{ to } \frac{4\pi}{3}} \quad (4.19)$$

Fig. 4.6 also shows the instantaneous resultant signal magnitude (IRSM) of the modified reference line voltage signals. In contrast to conventional SVPWM, the IRSM of modified reference line voltage signals has frequency equals to the six times the fundamental frequency (50Hz). Also, the resultant signal has the maximum IRSM of $1.15.\,\mathrm{BV_{dc}}$ at the position of large vectors (i.e. at $\alpha = 0, 60^{\circ}, 120^{\circ}, 180^{\circ}, 240^{\circ}, 300^{\circ}$). The lengths of switching vectors have been calculated based on the maximum available IRSM of reference line voltage signals at the position of respective switching vector. The calculations of switching vector lengths are provided in Table 4.3.

Table 4.3. Calculations of the length of switching vectors

Switching vectors	Length (per 1.BVdc), conventional SVPWM	Used length (as per available IRSM of Fig.5, Proposed SVPWM
Large(V1-V6)	$1.154 \times (1.\,\mathrm{BV_{dc}}) = 1.154.\,\mathrm{V_{dc}}$	$1.15 \times \left(\frac{1}{1.154}.\,\mathrm{BV_{dc}}\right) = 1.\,\mathrm{BV_{dc}}$
Medium (V13-V18)	$1 \times (1.\,\mathrm{BV_{dc}}) = 1.\,\mathrm{BV_{dc}}$	$1 \times (1.\,\mathrm{BV_{dc}}) = 1.\,\mathrm{BV_{dc}}$

The reduction in the length of large switching vectors in proposed SVPWM consequently results in the modification of the dwell time duration of the switching vectors. This is shown as under.

4.3.2.1. Dwell time calculation

Consider Fig. 4.5, the reference vector positioned in T1 can be realized using one large vector (V1), one medium vector (V13), and one or two appropriate ST vectors from Table 4.2. The formulas used for the calculation of dwell time of the switching vectors are mentioned below:

$$T_{a\_pr} = \left(\frac{V_{ref}}{1.\,BV_{dc}}\right)\left(\frac{\mathrm{Sin}(\pi/6 - \alpha)}{\mathrm{Sin}(\pi/6)}\right).T_s \tag{4.20}$$

$$T_{b\_pr} = \left(\frac{V_{ref}}{1.\,BV_{dc}}\right)\left(\frac{\mathrm{Sin}(\alpha)}{\mathrm{Sin}(\pi/6)}\right).T_s \tag{4.21}$$

$$T_{z\_pr} = T_s - T_{a\_pr} - T_{b\_pr} \tag{4.22}$$

T_{a_pr}, T_{b_pr} are the active vector time durations, T_{z_pr} is the time duration of the null vector and T_s is the time duration of one sample. From (4.20) to (4.22)

$$T_{a\_pr}{}_{\alpha=\pi/12} = T_{b\_pr}{}_{\alpha=\pi/12}, \text{and } T_{a\_pr}{}_{\alpha=0} = T_{b\_pr}{}_{\alpha=\pi/6} \tag{4.23}$$

As shown in Fig. 4.4, the frequency of the null interval (T_{z_pr}) is twelve times the fundamental frequency which is double as compared to T_{z_ex} (4.16) of the conventional SVPWM.

Since the large and medium vectors are of unity length (see Fig. 4.5), the simple mathematical calculation gives the maximum value of the reference vector ($V_{ref,max}$) as

$$V_{ref,max} = 0.96.\,BV_{dc} \tag{4.24}$$

The modulation index in the case of proposed SVPWM is defined as

$$M_{pr} = \frac{4.\,V_{ref}}{3.\,BV_{dc}}.(CF) \tag{4.25}$$

The correction factor (CF) is

$$CF = \frac{V_{ref,max}}{\text{Average value of maximum IRSM}} \tag{4.26}$$

The average value of the maximum IRSM is (see Fig. 4.6)

$$\text{Average value of maximum IRSM} = 1.028.\,BV_{dc} \tag{4.27}$$

Substituting (4.24) and (4.27) into (4.26) gives the value of CF as:

$$CF = 0.933 \tag{4.28}$$

The maximum modulation index using proposed SVPWM can be found by substituting (4.24) and (4.28) into (4.25)

$$M_{pr,(max)} = 1.19 \tag{4.29}$$

The maximum available rms value of the fundamental line voltage can be found using (4.29) and (4.12)

$$V_{ab}(rms) = (0.612 \times 1.19).BV_{dc} = 0.728.BV_{dc} \tag{4.30}$$

Comparing equation (4.29) and (4.30) with equation (4.11) and (4.13), respectively, shows that the modulation index and available fundamental rms line voltage using the proposed modified SVPWM is 3 percent more as compared to conventional SVPWM.

4.4. PROPOSED IMPROVED MAXIMUM BOOST CONTROL (IMBC)

The null interval (equation (4.22)) of the modified SVPWM is completely replaced by ST states in IMBC. The analysis of the IMBC is given as under.

4.4.1. Available ST duty ratio

The average value of ST duty ratio using IMBC ($\bar{D}_{IMBC}$) can be calculated using (4.20) - (4.22):

$$\begin{aligned}(\bar{D}_{IMBC}) &= \frac{6}{\pi}\int_0^{\pi/6}\left(\frac{T_{z\_pr}}{T_s}\right) \\ &= \frac{6}{\pi}\int_0^{\pi/6}\left[1-\left\{\frac{\sin(\pi/6-\alpha)}{\sin(\pi/6)}+\frac{\sin(\alpha)}{\sin(\pi/6)}\right\}\left(\frac{V_{ref}}{BV_{dc}}\right)\right]d\alpha\end{aligned} \tag{4.31}$$

Solving (4.31), we get:

$$(\bar{D}_{IMBC}) = 1 - \frac{12.(2-\sqrt{3}).V_{ref}}{\pi.BV_{dc}} \tag{4.32}$$

From (4.25), we get

$$\frac{V_{ref}}{BV_{dc}} = \frac{3.M_{pr}}{4.(CF)} \tag{4.33}$$

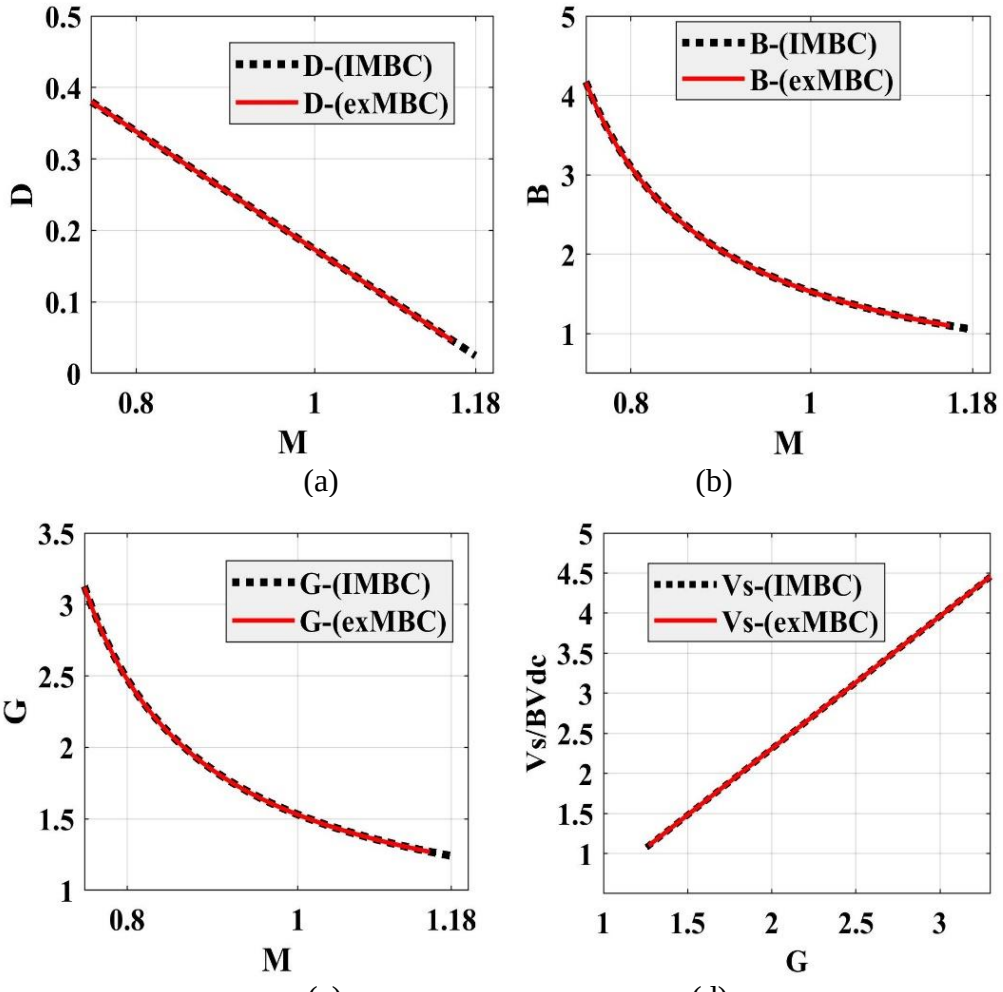
Substituting (4.33) in (4.32), the relationship between ST duty ratio and modulation index can be found

$$(\bar{D}_{IMBC}) = \frac{\pi.(CF) - 9.M_{pr}.(2-\sqrt{3})}{\pi.(CF)} \tag{4.34}$$

On the other hand, the relationship between the ST duty ratio and the modulation index when existing MBC [4] is applied in 3L-ZSI

$$\overline{D}_{exMBC} = \frac{(2\pi - 3\sqrt{3}.M_{ex})}{2\pi} \tag{4.35}$$

The plots of ST duty ratio/boost factor/gain Vs modulation index and switching stress Vs gain are shown in Fig. 4.7 to illustrate the comparison between existing MBC and IMBC. Both, existing MBC and IMBC give the same performance in terms of available ST duty ratio, boost factor, gain, and switching stress except the higher range of modulation index available in IMBC.



(a) (b) (c) (d)

Fig. 4.7. Comparison of existing MBC and IMBC, (a) ST duty ratio Vs modulation index, (b) boost factor Vs modulation index, (c) gain Vs modulation index, (d) per unit switching stress Vs gain.

4.5. PROPOSED REDUCED CMV SWITCHING PATTERNS

Depending upon the number of ST states per sample, the proposed switching patterns have been named as ZSVM_1TI and ZSVM_2TI. ZSVM_1TI and ZSVM_2TI are characterized by the use of one and two ST states per sample, respectively. The switching states pattern per sample for each triangle has been tabulated in Table 4.4 for both switching techniques. The ST states have been equally distributed in all three phase legs. The important features of these switching patterns have been discussed in the next section.

Table 4.4. Proposed reduced CMV switching states pattern

T	ZSVM_1TI		ZSVM_2TI	
	Switching pattern	*	Switching pattern	*
T1	PON-FON-PNN	a	FON-PON-POF-PNN	a, c
T2	PON-FON -PPN	a	FON-PON-POF-PPN	a, c
T3	OPN- OPF-PPN	c	OPF-OPN-OFN-PPN	c, b
T4	OPN- OPF-NPN	c	OPF-OPN-OFN-NPN	c, b
T5	NPO- NFO-NPN	b	NFO-NPO-FPO-NPN	b, a
T6	NPO- NFO-NPP	b	NFO-NPO-FPO-NPP	b, a
T7	NOP- FOP-NPP	a	FOP-NOP-NOF-NPP	a, c
T8	NOP- FOP-NNP	a	FOP-NOP-NOF-NNP	a, c
T9	ONP- ONF-NNP	c	ONF-ONP-OFP-NNP	c, b
T10	ONP- ONF-PNP	c	ONF-ONP-OFP-PNP	c, b
T11	PNO- PFO-PNP	b	PFO-PNO-FNO-PNP	b, a
T12	PNO- PFO-PNN	b	PFO-PNO-FNO-PNN	b, a

*ST phase leg

4.6. COMPARISON

It is the characteristic of MBC and IMBC that it completely replaces the null states via ST states. This affects the switching frequency of the power switches. Therefore, to have a fair comparison, existing reduced CMV switching techniques have been also considered with completely replaced null states.

After modification using existing MBC, the abbreviations used for the existing reduced CMV switching techniques are as under:

M1 = reduced CMV switching technique of [65], [66]

M2 = APOD technique of [63], [64]

M3 = switching technique of [67]

ZSVM_1TI and ZSVM_2TI are the proposed switching techniques that use the IMBC approach of voltage boosting.

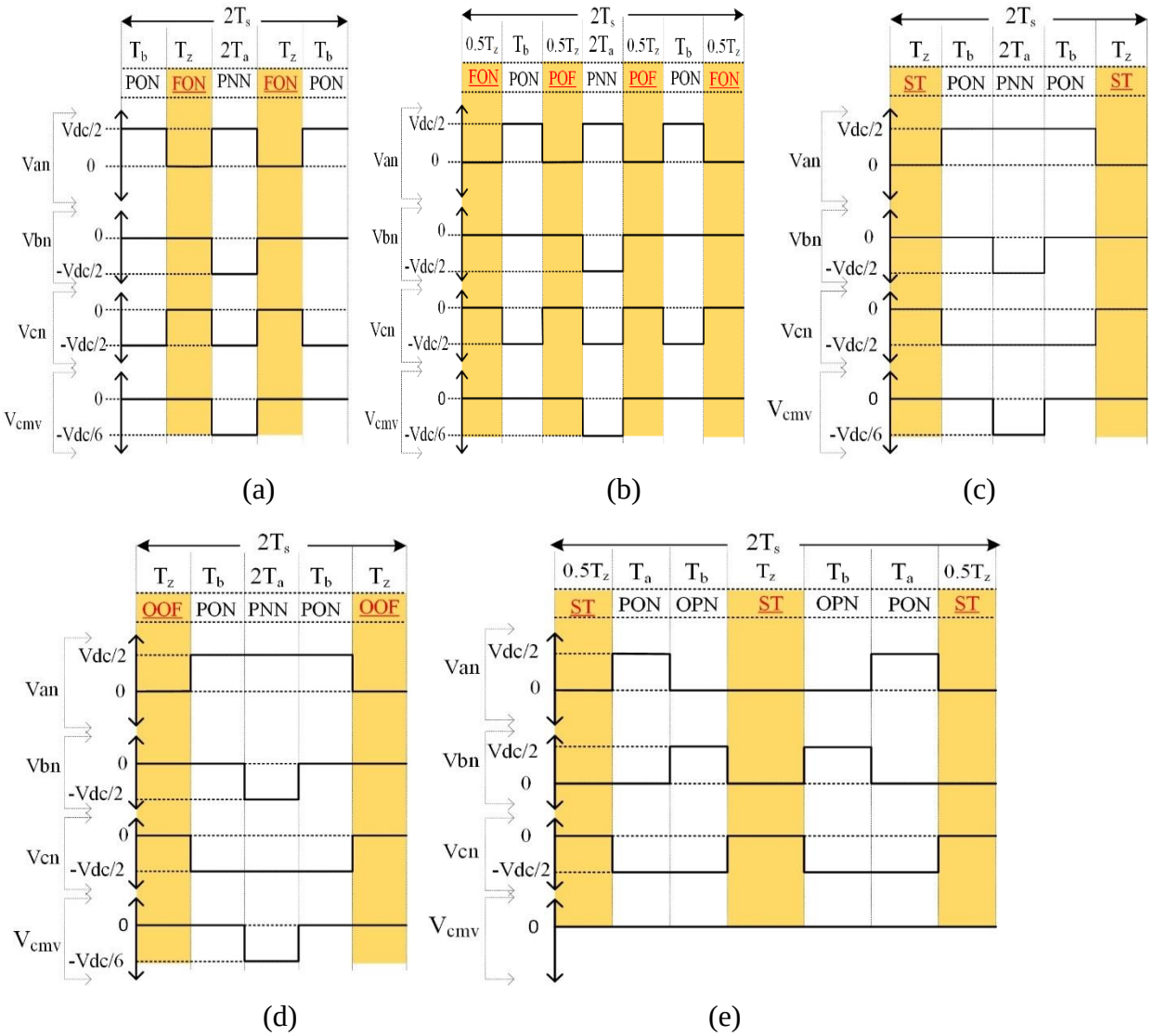


Fig. 4.8. Graphical description of switching pattern, pole voltages and CMV of different PWM techniques, (a) ZSVM_1TI, (b) ZSVM_2TI, (c) M2, (d) M3, (e) M1.

NOTE- M2 and M3 differ only in the applied way of ST state. In M2, the ST state is applied via synchronization of two-phase legs while in M3, only one phase leg at a time is used for the ST state insertion at a time. However, the output waveforms of both (M2, M3) are the same.

4.6.1. Switching frequency of the IN

The switching frequency of the IN is an important consideration while designing the size of its inductors and capacitors. Fig. 4.8 shows the graphical representation of switching patterns, pole voltage, and CMV using ZSVM_1TI, ZSVM_2TI, M1, M2, and M3 switching techniques. The position of the ST state affects the switching frequency of the IN. For example, ZSVM_1TI, M2, M3 uses only one ST state per sample. However, the switching frequency of the IN is double in the case of ZSVM_1TI when compared to M2 and M3. Depending upon the number of ST states per sample, all switching techniques have been classified into two categories in Table 4.5. Table 4.5 also contains the expressions of switching frequency of the IN. A plot between the carrier frequency (F_c) and the switching frequency of the IN ($F_{sw(IN)}$) using considered PWM techniques is shown in Fig. 4.9.

Table 4.5. Switching frequency of the IN

Switching freq. of IN	Category 1(1 ST)		Category 2(2 ST)	
	ZSVM_1TI	M2= M3	ZSVM_2TI	M1
$F_{sw(IN)}$	$2F_s$	F_s	$3F_s$	$2F_s$

$F_c = 1/(2T_s)$

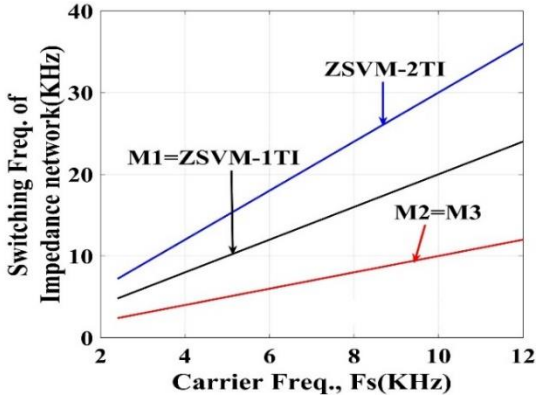


Fig. 4.9. Plot of relationship between the carrier frequency and switching frequency of the IN using various reduced CMV switching techniques.

Table 4.6. Switching frequency of power switches using various reduced CMV PWM techniques in 3L-CDBC ZSI

Carrier Freq. (F_c) in kHz	Switching frequency of the power switches (IGBTs) in Hz									
	ZSVM_1TI		ZSVM_2TI		M1		M2		M3	
	SX1=SX3, SX2	**W**	SX1=SX3, SX2	**W**	SX1=SX3, SX2	**W**	SX1=SX3, SX2	**W**	SX1=SX3, SX2	**W**
2.4	1250, 900	**1133**	1700, 900	**1433**	850, 4800	**2166**	450, 2400	**1100**	1400, 1800	**1533**
4.8	2450, 1700	**2200**	3300, 1700	**2766**	1650, 9600	**4300**	850, 4800	**2166**	2600, 3400	**2866**
7.2	3650,2500	**3266**	4900, 2500	**4100**	2450, 14400	**6433**	1250, 7200	**3233**	3800, 5000	**4200**
9.6	4850,3300	**4333**	6500, 3300	**5433**	3250, 19200	**8566**	1650, 9600	**4300**	5000, 6600	**5533**
12	6050,4100	**5400**	8100, 4100	**6766**	4050, 24000	**10700**	2050, 12000	**5366**	6200, 8200	**6866**

W is defined in (4.36), X= (A, B, C)

4.6.2. Switching frequency of the power switches

The inverter circuitry of CDBC ZSI (Fig. 3.3) has been taken for all PWM techniques. As seen in Table 3.10 of chapter 3 that, it is the characteristic of CDBC ZSI/VSI configuration that the switching frequency of the middle bidirectional switch (SX2) is different from the upper (SX1) and lower power switch (SX3) in each phase leg {X=A, B, C}. The upper and lower switches (SX1 and SX3) of CDBC ZSI have equal switching frequency. Here, the total average switching frequency (power switches) of the inverter has been compared using various PWM techniques. The formula used for calculating total average switching frequency (W) is:

$$W = \frac{3(\sum(F_{sw}(SX1) + F_{sw}(SX2) + F_{sw}(SX3)))}{9} \tag{4.36}$$

The switching frequency of power switches calculated using considered PWM techniques at the various values of the carrier frequency has been tabulated in Table 4.6. In category 1 of the switching states (defined in Table 4.5), the minimum 'W' is offered by the switching technique of M2 which is slightly (33Hz) less than that of proposed ZSVM_1TI. But it should be noted that the switching frequency of the IN is double in ZSVM_1TI as compared to M2 (Table 4.5). Similarly, in category 2, the proposed ZSVM_2TI has a lower switching frequency of power switches as compared to the switching technique of M1.

4.6.3. An important feature of CDBC ZSI

The main drawback of CDBC ZSI/VSI reported in chapter 3 (Table 3.3 and Table 3.9 of chapter 3) is that the switching frequency of the middle bidirectional switch is more as compared to the upper and lower power switch of a phase leg. But this is not true with the proposed PWM techniques. As illustrated in Table 4.6, the switching frequency of the middle bidirectional switch is even lower than the upper and lower power switch of a phase leg when proposed switching techniques are used in CDBC ZSI configuration. In the existing reduced CMV PWM techniques, the switching frequency of the middle bidirectional power switch (SX2) is always greater than the upper and lower switch of each phase leg. It is also noted from Table 4.6 that the switching frequency of the bidirectional switch (SX2) of CDBC ZSI is the same with proposed ZSVM_1TI and ZSVM_2TI.

4.6.4. Comparison of IN components size

The switching frequency of the IN and the presence of the lower order harmonic components significantly affects the size of the IN. It has been indicated in Fig. 4.9 that, for a specific carrier frequency, the switching frequency of the IN has the following order; ZSVM_2TI > ZSVM_1TI > (M2=M3).

First of all, consider important relationships of existing MBC and IMBC. In the case of existing MBC, the ST duty ratio varies six times the fundamental frequency. The ST duty ratio as a function of α using existing MBC is given by (using (4.14)-(4.16)):

$$D(\alpha)_{\_exMBC} = 1 - \frac{V_{ref}}{BV_{dc}}\left\{\sqrt{3}.\sin\left(\frac{\pi}{6} - \alpha\right) - 2.\sin(\alpha)\right\};\ \left(0 < \alpha < \frac{\pi}{6}\right) \tag{4.37}$$

To be more specific, the null intervals T_{z_ex} of (4.16) and T_{z_pr} of (4.22) are denoted by T_{z_exMBC} and T_{z_IMBC} for existing MBC and IMBC, respectively.

Similarly, the modulation index denoted by M_{ex} of (4.10) and M_{pr} of (4.25) are denoted by M_{ex_MBC} and M_{pr_IMBC} for existing MBC and IMBC, respectively.

In (4.37), $D(\alpha)_{\_exMBC}$ has the maximum value at $\alpha = 0°$. Substituting $\alpha = 0°$ in (4.37) and using (4.10), we get:

$$D(\alpha = 0°)_{\_exMBC\_max} = \frac{T_{z\_exMBC\_max}}{T_s} = \left(1 - \frac{3}{4}M_{\_exMBC}\right) \tag{4.38}$$

The modulation index of existing MBC can be written in terms of boost factor using (4.2) and (4.35) as

$$M_{\_exMBC} = \frac{(1+B)\pi}{3\sqrt{3}\,B} \tag{4.39}$$

Using (4.39) in (4.38), the maximum null interval in a sample can be written in terms of 'B' as

$$T_{z\_exMBC\_max} = \left\{1 - \frac{(1+B)\pi}{4\sqrt{3}.B}\right\}T_s \tag{4.40}$$

On the other hand, in IMBC, the ST duty ratio as a function of angle (α) is given by (using (4.31))

$$D(\alpha)_{\_IMBC} = \left[1 - \frac{2.V_{ref}}{BV_{dc}}\left\{\sin\left(\frac{\pi}{6} - \alpha\right) + \sin(\alpha)\right\}\right];\ \left(0 < \alpha < \frac{\pi}{6}\right) \tag{4.41}$$

$D(\alpha)_{\_IMBC}$ of (4.41) has the maximum value at $\alpha = 0°$.

$$D(\alpha = 0°)_{\_IMBC\_max} = \left(1 - \frac{V_{ref}}{BV_{dc}}\right) \tag{4.42}$$

Substituting (4.33) in (4.42)

$$D(\alpha = 0°)_{IMBC_{max}} = \frac{T_{z_{IMBC_{max}}}}{T_s} = \left(1 - \frac{3.M_{pr\_IMBC}}{4.(CF)}\right) \tag{4.43}$$

The Modulation index in terms of boost factor can be found using (4.2) and (4.34)

$$M_{pr\_IMBC} = \frac{(1+B).(CF).\pi}{18.B.(2-\sqrt{3})} \tag{4.44}$$

Using (4.43) and (4.44), the maximum null interval of a sample using IMBC can be expressed in terms of 'B' as

$$T_{z\_IMBC\_max} = \left\{1 - \left(\frac{(1+B)\pi}{24.B.(2-\sqrt{3})}\right)\right\} T_s \tag{4.45}$$

For the range of B' ($1.2 \leq B \leq 5$), the relationship between $T_{z\_exMBC\_max}$ and $T_{z\_IMBC\_max}$ has been plotted in Fig. 4.10.

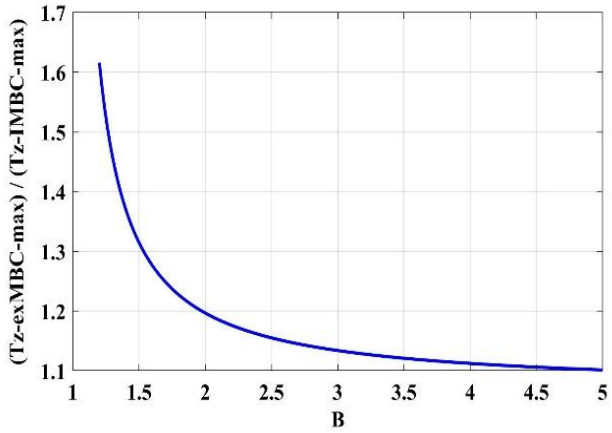


Fig. 4.10. Plot of the ratio of max duration of ST interval in a sample using existing MBC and proposed IMBC (using equation (4.40) and (4.45)).

Mathematically, it can be written as (using equation (4.40) and (4.45)):

$$\left(1.10 \leq \frac{T_{z\_exMBC\_max}}{T_{z\_IMBC\_max}} \leq 1.61\right); \quad \{5 \geq B \geq 1.2\} \tag{4.46}$$

Next, the IN inductor current ripple ($\Delta I_{L1} = \Delta I_{L2} = \Delta I_L$) and capacitor voltage ripple $\Delta V_{C3} = \Delta V_{C4} = \Delta V_C$) can be written as a sum of high frequency and low frequency components of inductor current and capacitor voltage ripple as:

$$\Delta I_L = \Delta I_{Lh} + \Delta I_{Ll} \tag{4.47}$$

$$\Delta V_C = \Delta V_{Ch} + \Delta V_{Cl} \tag{4.48}$$

Now consider the switching techniques.

4.6.4.1. Switching technique M2 and M3

From Fig. 4.8, the maximum duration of ST state seen by the IN using M2 and M3 is twice of the null interval (i.e. $2T_{z\_exMBC\_max}$.). The high-frequency ripple components of IN inductor current and capacitor voltage using M2 and M3 can be written as [5], [38]:

$$\Delta I_{Lh\_exMBC} = \frac{V_{C\_exMBC}}{L_{exMBC}} . 2. T_{z\_exMBC\_max} \tag{4.49}$$

$$\Delta V_{Ch\_exMBC} = \frac{I_{L\_exMBC}}{C_{exMBC}} . 2. T_{z\_exMBC\_max} \tag{4.50}$$

The sixth frequency components of inductor current and capacitor voltage using exiting MBC can be written as:

$$\Delta I_{Ll\_exMBC} = \frac{V_{pk2pk}}{6\omega . L_{exMBC}} \tag{4.51}$$

$$\Delta V_{Cl\_exMBC} = \frac{I_{pk2pk}}{6\omega . C_{exMBC}} \tag{4.52}$$

V_{pk2pk} and I_{pk2pk} are the peak to peak ripple across the inductor voltage and capacitor current, respectively. Using (4.47)-(4.52), the final expression for 'L' and 'C' for M2, M3 can be written as:

$$L_{exMBC} = \underbrace{\frac{V_{C\_exMBC}}{\Delta I_{Lh\_exMBC}} . 2. T_{z\_exMBC\_max}}_{\text{high freq. component}} + \underbrace{\frac{V_{pk2pk}}{6\omega . (\Delta I_{Ll\_exMBC})}}_{\text{sixth freq. component}} \tag{4.53}$$

$$C_{exMBC} = \underbrace{\frac{I_{L\_exMBC}}{\Delta V_{Ch\_exMBC}} . 2. T_{z\_exMBC\_max}}_{\text{high freq. component}} + \underbrace{\frac{I_{pk2pk}}{6\omega . (\Delta V_{Cl\_exMBC})}}_{\text{sixth freq. component}} \tag{4.54}$$

4.6.4.2. Proposed ZSVM_1TI and ZSVM_2TI

The low-frequency ripple component of the inductor current ripple and capacitor voltage ripple greater than 6th F1 have not been considered. From Fig. 4.8, the maximum duration of the ST interval seen by the IN using these techniques is equal to the maximum null interval ($T_{z\_IMBC\_max}$). The high-frequency ripple components seen by inductor current and capacitor voltage can be written as [5], [38]:

$$\Delta I_{Lh\_IMBC} = \frac{V_{C\_IMBC}}{L_{IMBC}} . T_{z\_IMBC\_max} \tag{4.55}$$

$$\Delta V_{Ch\_IMBC} = \frac{I_{L\_IMBC}}{C_{IMBC}} . T_{z\_IMBC\_max} \tag{4.56}$$

Using (4.47), (4.48), (4.55), (4.56), the final expression for 'L' and 'C' considering only high-frequency components can be written as:

$$L_{IMBC} = \frac{V_{C\_IMBC}}{\Delta I_{Lh\_IMBC}} . T_{z\_IMBC\_max} \tag{4.57}$$

$$C_{IMBC} = \frac{I_{L\_IMBC}}{\Delta V_{Ch\_IMBC}} . T_{z\_IMBC\_max} \tag{4.58}$$

For equal output power (i.e. same boost factor) the average voltage across the IN capacitors using proposed and existing PWM techniques are:

$$V_{C\_exMBC} = V_{C\_IMBC} \tag{4.59}$$

Consider $\Delta I_{Lh\_exMBC} = \Delta I_{Lh\_IMBC}$, neglecting the sixth frequency component of (4.53) and (4.54) then comparing (4.53) with (4.57) and (4.54) with (4.58), we get:

$$\frac{L_{exMBC}}{L_{IMBC}} = \frac{C_{exMBC}}{C_{IMBC}} = \frac{2. T_{z\_exMBC\_max}}{T_{z\_IMBC\_max}} \tag{4.60}$$

Using (4.46) and (4.60), for $(5 \geq B \geq 1.2)$, the ratio (even neglecting the 6th F1 components of M2, M3 techniques) of the requirement of 'L' and 'C' comes out to be:

$$\left(2.2 \leq \frac{L_{exMBC}}{L_{IMBC}} = \frac{C_{exMBC}}{C_{IMBC}} \leq 3.2\right); \quad \{5 \geq B \geq 1.2\} \tag{4.61}$$

Finally, the size of the IN 'L' and 'C' using M2 and M3 switching techniques is around 2 to 3 times more than that of the proposed ZSVM_1TI and ZSVM_2TI.

4.6.5. Switching and conduction losses

To calculate the switching and conduction losses of the power switches and diodes, the PWM techniques have been simulated using the datasheet parameters. The IGBT power switch used is 'KGT25N120NDH' which has an inbuilt antiparallel diode. The 'MUR 1560' diodes have been used in the bidirectional power switch and in the IN. For the rated output power of around 1KW, the simulated values of switching and conduction losses have been tabulated in Table 4.7. In category 1 of the switching techniques defined in Table 4.5, ZSVM_1TI has slightly increased power loss as compared to the M2 and M3. The power losses due to ZSVM_2TI are highest among the considered PWM techniques.

Table 4.7. Distribution of switching and conduction losses

Losses (W)	Switches /diodes	ZSVM_1TI	ZSVM_2TI	M2	M3
Switching losses	SX1+SX3	27.39	34.36	4.57	21.4
	SX2	0.45	0.2	19.3	1.41
	Da + Db	0.09	0.17	0.051	0.049
Conduction losses	SX1+SX3	24.74	35.23	7.54	20.5
	SX2	0.47	0.53	17.8	0.58
	Da + Db	12.71	13.39	11.4	12.9
Total (W)		65.85	83.88	60.66	56.8

X=A, B, C

4.7. RESULTS

As shown in Fig. 4.8, the switching state pattern of M2 and M3 is the same except the used combination of power switches for ST state insertion. The output waveforms of both (M2 and M3) are the same. Therefore, only M3 has been taken from the existing PWM techniques for comparison with the proposed techniques.

4.7.1. Simulation results

MATLAB/Simulink software has been used for simulation with the parameter mentioned in Table 4.8. For the same output power, the modulation index requirement of M3 and proposed PWM techniques are the same. The boost factor B is set to 2.5 and load parameters are r=25Ω and l=4mH.

Table 4.8. Parameters used for simulation/ experimentation

Parameter	Value/name
Input dc source (V_{dc})	130V
Inductors (L_1, L_2)	6mH
Capacitor C_3, C_4	330uF
Three-phase load parameters	25 Ω, 4mH 50 Ω, 2mH
Fundamental Frequency (F_1)	50Hz
Half carrier cycle duration	208usec.
Carrier frequency (F_s)	2.4kHz

The simulation waveforms of the null/ST interval has been shown in Fig. 4.11. The ST/null time duration using the M3 technique changes six times the fundamental frequency which is double as compared to the ZSVM_1TI and ZSVM_2TI. Fig. 4.11 also justifies the theoretical calculation results illustrated in Fig. 4.4.

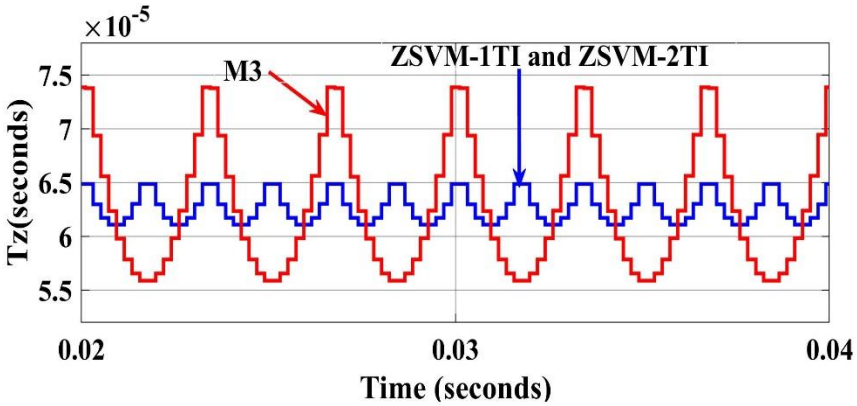
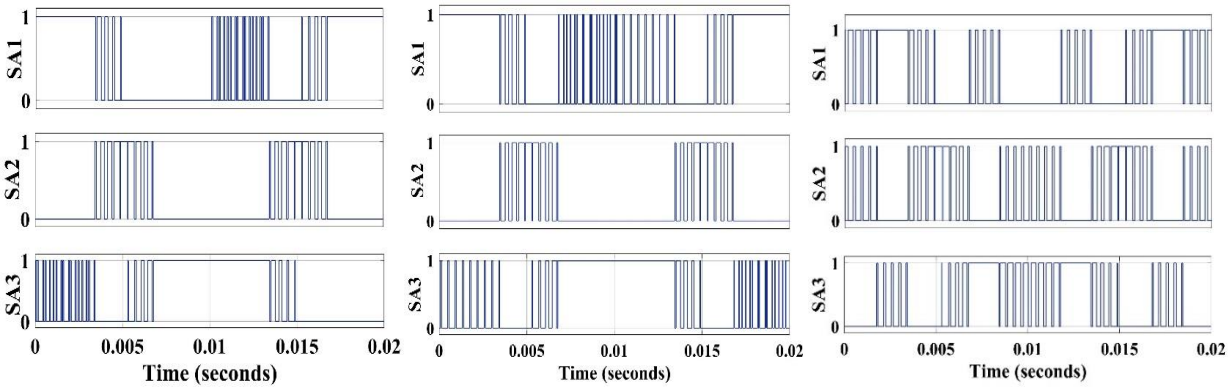


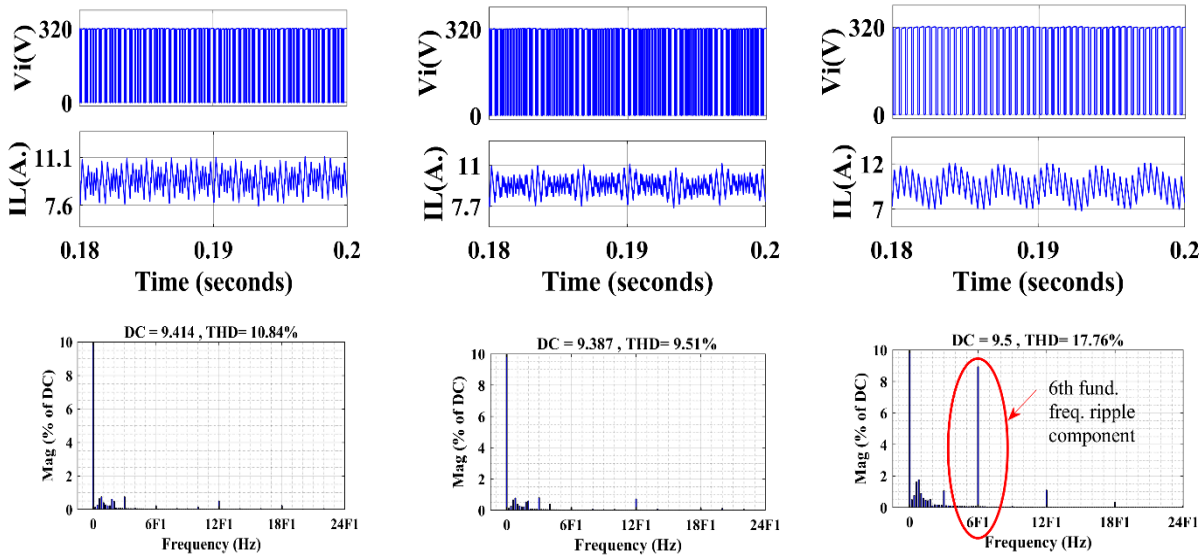
Fig. 4.11. Simulation waveform of ST/null time interval over the fundamental cycle using ZSVM_1TI, ZSVM_2TI, and M3.

The gating pulses waveforms are shown in Fig. 4.12 to illustrate the switching frequency of the power switches at the carrier frequency of 2.4kHz (as of the first row of Table 4.6). As seen in Fig. 4.12, the middle bidirectional switch has the same switching frequency using ZSVM_1TI and ZSVM_2TI.



(a) (b) (c)

Fig. 4.12. Simulated waveforms of gating signal at B=2.5, (a) ZSVM_1TI (b) ZSVM_2TI, (c) M3.

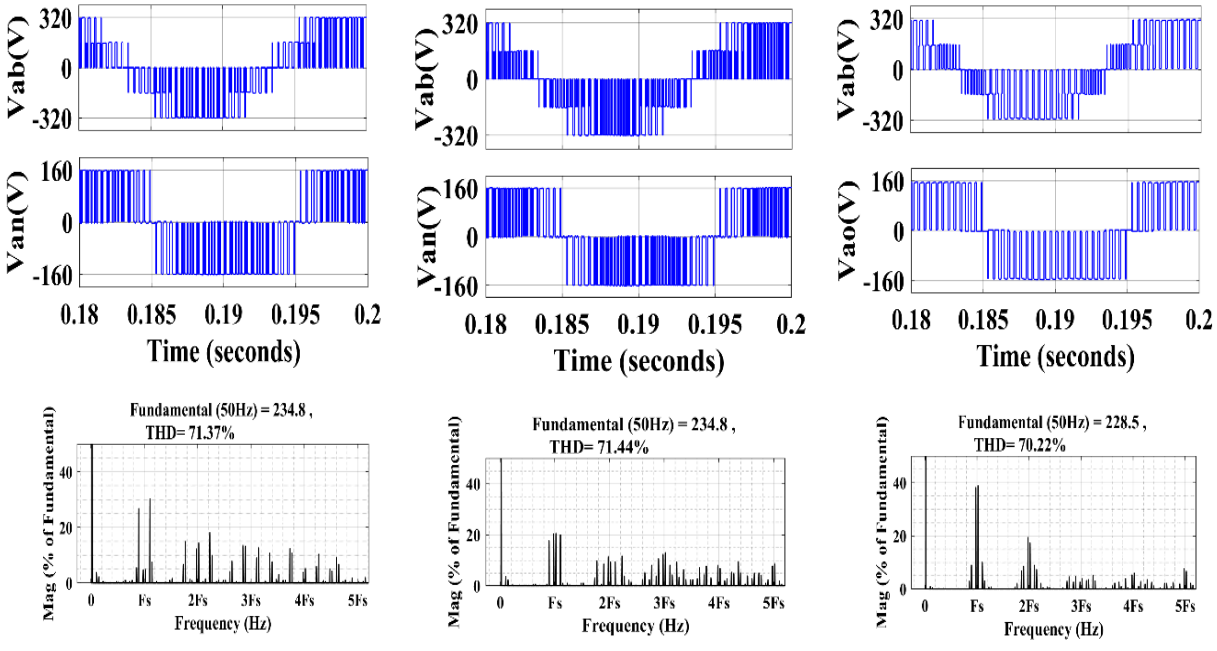


(a) (b) (c)

Fig. 4.13. Simulation waveforms of dc-link voltage (V_i), inductor current (i_L) and the spectra of inductor current at 'B=2.5', (a) ZSVM_1TI (b) ZSVM_2TI, (c) M3.

NOTE: DC link voltage of ZSVM_1TI and ZSVM_2TI looks denser just because of the increased switching frequency of the IN (Table 4.5). The total average switching frequency of the power switches using ZSVM_1TI and ZSVM_2TI is lower as compared to M3. See Table 4.6 first row for the switching frequency of the power switches using ZSVM_1TI, ZSVM_2TI, and M3 and waveforms of gating pulses in Fig. 4.12.

Fig. 4.13 shows the waveform of dc-link voltage(V_i), inductor current (i_L) and the spectra of the inductor current waveform. The dc-link voltage peak (320V) has good agreement with the theoretically predicted value as per the relationship ($B.V_{dc}$). The inductor current is smooth using proposed PWM techniques. But when the M3 technique is used, the inductor current contains the 6^{th} F1 components which are visible in Fig. 4.13(c). The harmonic spectra of inductor currents are also shown in Fig. 4.13 to strengthen the claim that the 6^{th} F1 ripples are absent when proposed PWM techniques are applied. The simulation waveforms of the line voltage(V_{ab}), pole voltage (V_{an}) and THD of line voltage are shown in Fig. 4.14.



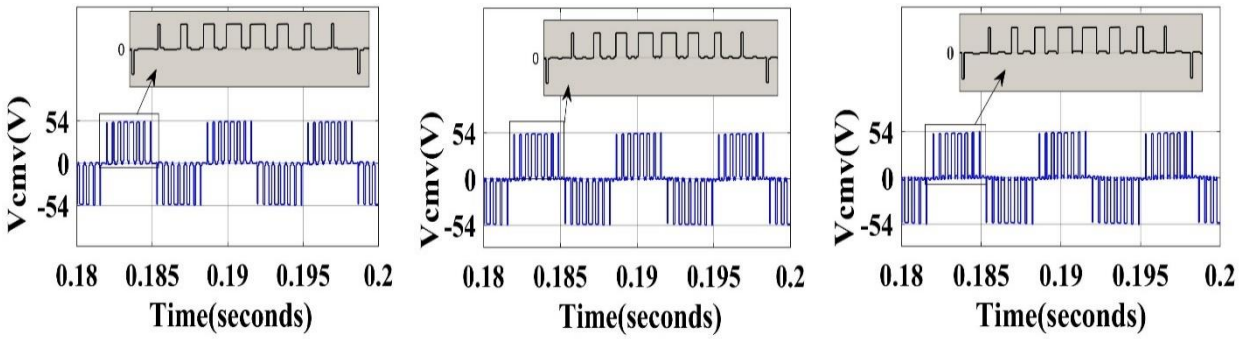
(a) (b) (c)

Fig. 4.14. Simulated waveforms of line voltage (V_{ab}), pole voltage (V_{an}) and THD spectra of line voltage at 'B=2.5', (a) ZSVM_1TI, (b) ZSVM_2TI, (c) M3.

NOTE- The total average switching frequency of the power switches using ZSVM_1TI and ZSVM_2TI is lower as compared to M3. See the first row of Table 4.6 and Fig. 4.12 of gating pulses.

Since 'B' is the same, the peak magnitude of the line voltage (V_{ab}) is approximately the same using all techniques (i.e. 320V which is as per the relationship $B.V_{dc}$.). Similarly, the peak magnitude of pole voltage is also the same (i.e. 160V) for all techniques and as per the relationship $0.5.B.V_{dc}$. The total harmonic distortion (THD) plots indicate that the harmonic distortion of the line voltage is also approximately same. It should be noted that the fundamental rms component of line voltage is less using the M3 technique as compared to the proposed techniques. This is due to the low-frequency ripple of the inductor current present in M3.

The simulation waveforms of the CMV (V_{cmv}) are shown in Fig. 4.15. The peak magnitude of CMV using all PWM techniques is around $\pm$54V which is the one-sixth of the available dc-link voltage (V_i). It is also clear from the zoomed portion of Fig. 4.15 that, all switching techniques have the same number of commutation in CMV i.e. slew rate of the CMV is unaffected with the proposed PWM techniques.



(a) (b) (c)

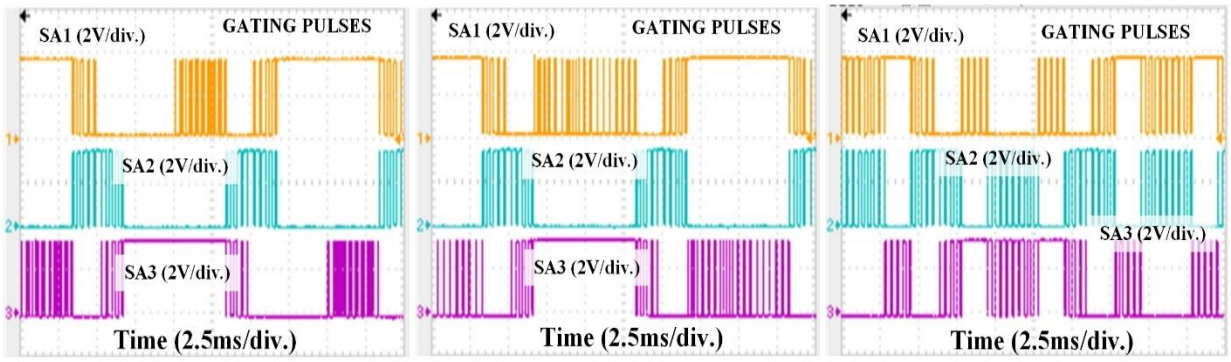
Fig. 4.15. Simulation waveforms of the CMV (V_{cmv}) at B=2.5, (a) ZSVM_1TI (b) ZSVM_2TI, (c) M3.

4.8. Experimental results

The laboratory prototype of CDBC ZSI is shown in Fig. 3.11 of chapter 3. Texas Instruments DSP, TMS320F28379D has been used for the generation of gating pulses. Two different cases of load parameters have been considered for experimental verification.

4.8.1. B=2.5, r=25Ω, l=4mH

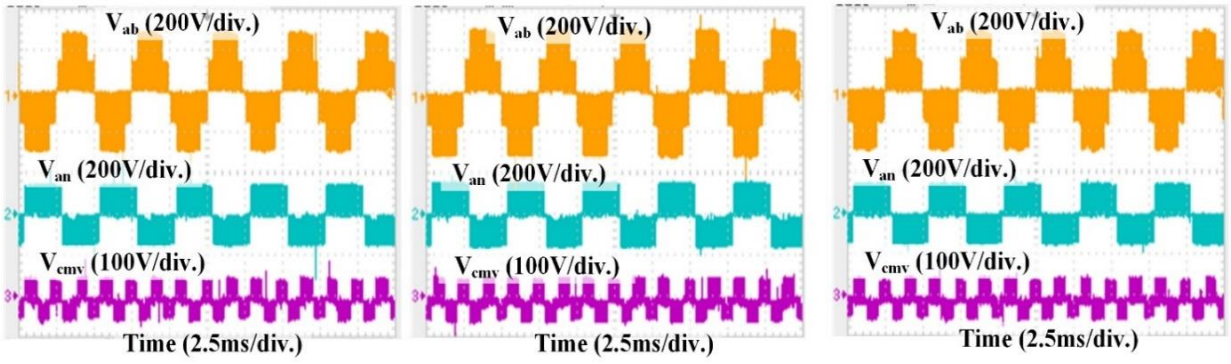
The gating pulse waveforms for this case have been shown in Fig. 4.16. These waveforms have the exact match as with the simulation waveforms of Fig. 4.12.



(a) (b) (c)

Fig. 4.16. Experimental waveforms of gating pulses at B=2.5', (a) ZSVM_1TI, (b) ZSVM_2TI, (c) M3.

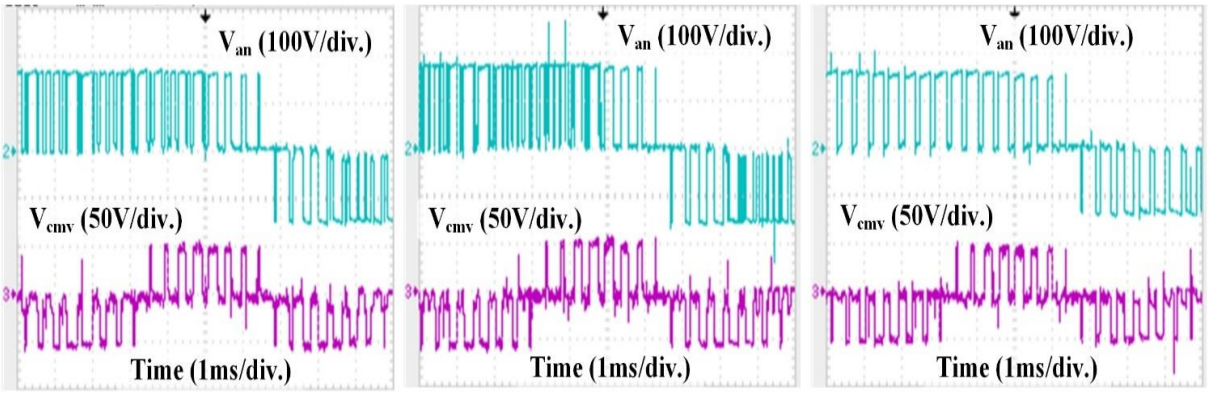
For 'B=2.5', the required modulation index value is 0.846 for all techniques. Fig. 4.17 shows the experimental waveforms of the line voltage, pole voltage, and CMV. The peak value of the line voltage (V_{ab}) and pole voltage (V_{an}) are 320V, 160V, respectively for all techniques. This satisfies the theoretical relationship of BV_{dc} for line voltage peak and $0.5.BV_{dc}$ for pole voltage peak value. The magnitude of CMV is around $\pm$54V which satisfies the relationship$\pm B\,V_{dc}/6$.



(a) (b) (c)

Fig. 4.17. Experimental waveforms of line voltage (V_{ab}), pole voltage (V_{an}) and CMV (V_{cmv}) at 'B=2.5', (a) ZSVM_1TI, (b) ZSVM_2TI, (c) M3.

The zoomed view of pole voltage and CMV is provided in Fig. 4.18 to indicate the number of commutation in the CMV. Fig. 4.18 proves that the rate of change of CMV is unaffected by the proposed switching techniques.



(a) (b) (c)

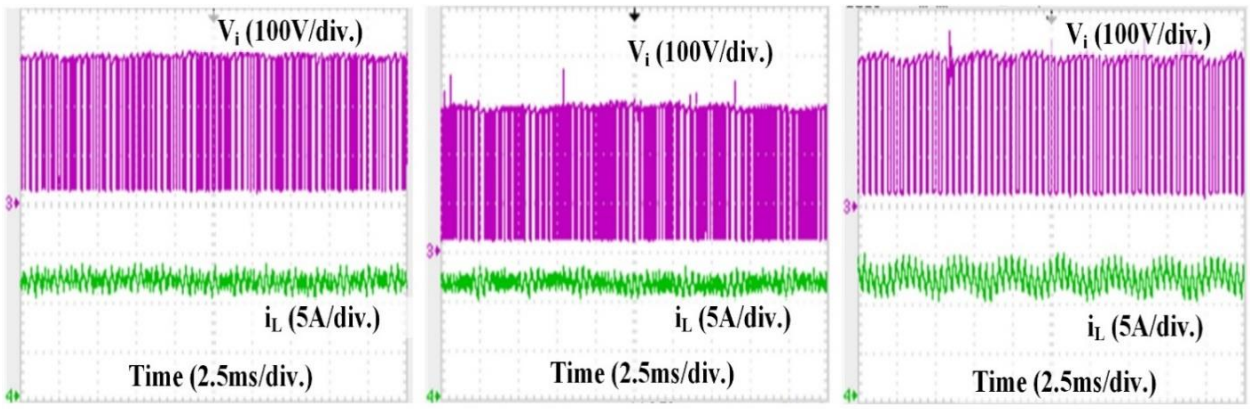
Fig. 4.18. Experimental waveforms (zoomed view) of pole voltage (V_{an}) and CMV (V_{cmv}) at 'B=2.5', (a) ZSVM_1TI, (b) ZSVM_2TI, (c) M3.

The measured rms value of the CMV for the various values of the boost factor has been provided in Table 4.9. The rms value of CMV is approximately the same using all PWM techniques.

Table 4.9. Measured values of CMV

V_{ab}(rms), B	RMS value of CMV (V)		
	ZSVM_1TI	ZSVM_2TI	M3
135, 1.5	20.8	20.9	20.1
169, 2	26.1	26.2	25.3
204, 2.5	31.5	31.5	30.5

The dc-link voltage (V_i) and the inductor current (i_L) waveforms are shown in Fig. 4.19. The peak value of the dc-link voltage satisfies the predicted theoretical value as per the relationship '$B.V_{dc}$'. It can be noticed from Fig. 4.19 that there are 6^{th} F1 ripple components in the inductor current using the M3 PWM technique. On the other hand, the inductor current using proposed techniques is smooth. This validates the claim that the IMBC technique of voltage boosting offers the elimination of the 6^{th} F1 inductor current ripple component.

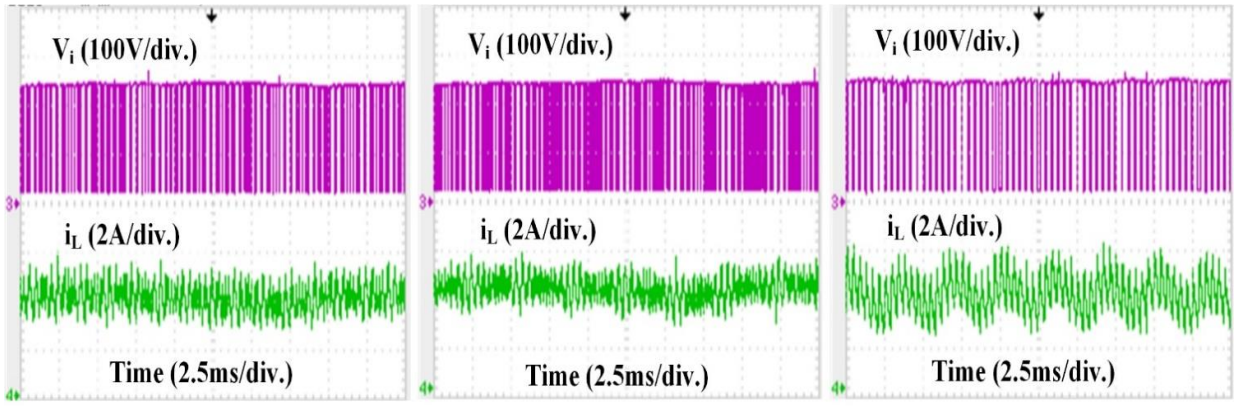


(a) (b) (c)

Fig. 4.19. Experimental waveforms of dc-link voltage (V_i) and inductor current (i_L) at 'B=2.5'for (a) ZSVM_1TI, (b) ZSVM_2TI, (c) M3.

4.8.2. B=2, r=50Ω, l=2mH

In this case, the modulation index is set to 0.906. The waveforms of dc-link voltage and inductor current for this case are shown in Fig. 4.20. The dc-link voltage has been boosted to around 250V. Again, it is visible from the inductor current waveforms in Fig. 4.20 that the 6th F1 inductor current ripples are absent with the proposed techniques.



(a) (b) (c)

Fig. 4.20. Experimental waveforms of dc-link voltage (V_i) and inductor current (i_L) at 'B=2'for (a) ZSVM_1TI, (b) ZSVM_2TI, (c) M3.

The tested efficiency of the prototype using proposed and existing PWM techniques have been plotted in Fig. 4.21.

ZSVM_1TI, M3 technique comes in the category of one ST state per sample and ZSVM_2TI comes in the category of two ST state per sample (Table 4.5).

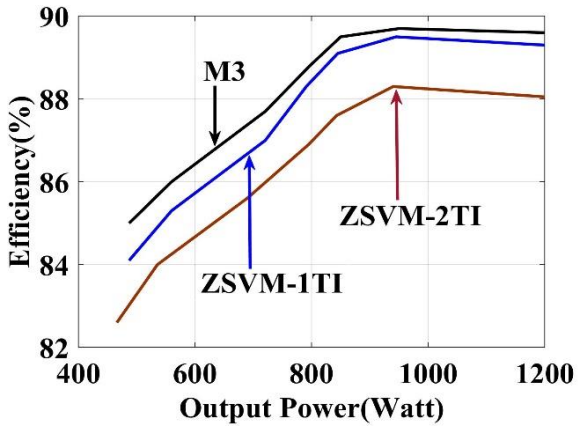


Fig. 4.21. Prototype efficiency curve.

Comparing the PWM techniques of category 1, it has been admitted that the efficiency offered by ZSVM_1TI is slightly less (around 1 percent) as compared to the M3 which can be compromised while seeing at the advantages of ZSVM_1TI. The efficiency of the inverter suffers more when the ZSVM_2TI technique is used.

4.9. DISCUSSION

The proposed PWM techniques (ZSVM_1TI and ZSVM_2TI) are a combination of three important findings. These are, modified SVPWM switching state diagram, improved maximum boost control (IMBC) approach of voltage boosting, and new reduced CMV switching patterns. The modified SVPWM doubles the frequency of the null interval based on which the IMBC has been proposed to eliminate the 6^{th}F1 ripple component of the impedance network inductor current. The proposed SVPWM switching diagram also offers an increased range of modulation index and improved dc bus utilization. The new pattern of switching states limits the CMV magnitude to $1/6^{th}$ of the available dc-link voltage without affecting the slew rate of CMV. Further, the proposed 12 sided polygon shown in Fig. 4.5 is equally valid for the case of a 3L-VSI. Similarly, the proposed IMBC can also be used with other PWM switching patterns of 3L-ZSI. The important aspects of the proposed and existing reduced CMV techniques have been summarized in Table 4.10.

Table 4.10. Important aspects of proposed and exisitng reduced CMV PWM techniques of 3L-ZSI

Aspect	Proposed (with IMBC approach)	Existing (with existing MBC approach)
	ZSVM_1TI and ZSVM_2TI	M2 and M3
Elimination of 6^{th} F1 ripple of IN inductor current	Yes, (see Fig. 4.13, Fig. 4.19, Fig. 4.20)	No, (see Fig. 4.13, Fig. 4.19, Fig. 4.20)
Range of modulation index	1.19, (Fig. 4.5 and equation (4.29)	1.15, (Fig. 4.2 and equation (4.11)
Boost factor	Both (proposed and existing) offers same boost factor in the range of M from 0.6 to 1.15. In addition, the proposed techniques also offers the enhanced utilization of the dc-link up to the range of M =1.19.	
Fundamental rms line voltage magnitude	$0.728.\,\mathrm{BV_{dc}}$, (see equation (4.30))	$0.707.\,\mathrm{BV_{dc}}$, (see equation (4.13))
Size of the IN components	As shown in equation (4.61), for the particular range of 'B', the size of IN passive elements is 2 to 3 times lower than the existing (M2, M3) techniques.	
Magnitude of CMV	Maintained within $\pm\mathrm{BV_{dc}}/6$, (Fig. 4.15 and Fig. 4.19)	
Slew rate of CMV	Same (Fig. 4.15 and Fig. 4.19)	
THD of line voltage	Almost same (Fig. 4.14)	
Switching frequency of the impedance network and power switches	See Table 4.5 and Table 4.6, The proposed ZSVM_1TI and ZSVM_2TI doubles and triples the switching frequency of the impedance network as compared to the existing (M2, M3) SVPWM techniques at competitive total average switching frequency of the power switches. This results in reduced impedance network size requirements using proposed techniques.	

Neutral point voltage (NPV) oscillation control	Mostly, the dwell time duration of the small vectors is used for balancing the upper/lower capacitors (C_1 and C_2) of the dc source in three-level inverters. But when the small vectors are not available either because they are not used or completely replaced by ST states for the implementation MBC approach, then it is not possible to apply those NPV oscillation control algorithm with proposed (ZSVM_1TI and ZSVM_2TI) as well as in existing (M2, M3) PWM techniques of 3L-ZSI. ZSVM_1TI, ZSVM_2TI, M2, and M3 PWM techniques does not use small vectors. This means that these techniques are suitable only for those applications where fixed dc sources are used at the input side of 3L-ZSI.
Power losses and efficiency	The proposed switching pattern increases the switching frequency of the impedance network. See Table 4.5 and Table 4.6 for details regarding the switching frequency of impedance network and power switches. As shown in Fig. 4.21 that the efficiency using ZSVM_1TI suffers slightly (around 1 percent) as compared to the M3. In addition to the advantages offered by ZSVM_1TI, the ZSVM_2TI technique has a better inductor current profile (Fig. 4.13) but the efficiency using ZSVM_2T suffers more as compared to the ZSVM_1TI and M3.

4.10. CONCLUSION

The conventional SVPWM switching diagram of 3L-ZSI has been successfully modified to propose the improved maximum boost control (IMBC) of voltage boosting. Modified SVPWM offers a 3 percent increase in the modulation index and fundamental rms line voltage as compared to the conventional SVPWM. Most importantly, the IMBC resolves the problem of 6^{th} F1 inductor current ripple components present in existing MBC without affecting the gain and switching stress across the power switches. The proposed reduced CMV switching patterns increases the switching frequency of the IN at a competitive switching frequency of the power switches when compared to the existing reduced CMV techniques. This results in reduced size of the impedance network while limiting the magnitude of CMV to one-sixth of the available dc-link voltage. The rate of change of CMV was also unaffected. However, a decrease in efficiency has been noticed using proposed techniques. The main demerit of the proposed as well as existing considered reduced CMV PWM technique is that the neutral point voltage balancing algorithms which adjusts the small vector duration for balancing the upper and lower capacitors of dc source are not applicable as these techniques does not use small vectors at all.

CHAPTER 5. UNIFIED CONTROL OF 3L-ZSI

5.1. INTRODUCTION

Majority of the applications of DC-AC power conversion unit requires control over output voltage/current magnitude and phase. For example, in grid tied PV inverter control over output voltage/ current is necessary to inject power to the grid at unity power factor. On the other hand, in isolated PV generation the control over the magnitude of the output voltage is sufficient. There are number of closed loop control algorithm present in the literature for the feedback control of Z-source inverters. In this chapter, a simple closed loop control has been presented for the islanded mode operation of 3L-ZSI. The presented closed-loop control is named as unified control technique.

5.2. UNIFIED FEEDBACK CONTROL TECHNIQUE

The unified feedback control technique has been implemented in the CDBC configuration of 3L-ZSI operating with the ZSVM_1TI PWM (proposed in chapter 4) technique.

5.2.1. Working

The expression for output line voltage of ZSI can be written as:

$$V_{ab} = \frac{\sqrt{3}}{2\sqrt{2}} . M . BV_{dc} \tag{5.1}$$

As discussed in equation (4.25) of chapter 4, the modulation index is written as

$$M = \frac{4V_{ref}}{3BV_{dc}} . CF \tag{5.2}$$

The value of CF is 0.933 (see equation (4.28).

Substituting (5.2) in (5.1)

$$V_{ab} = 0.761 . V_{ref} \tag{5.3}$$

The range of reference vector

$$V_{ref} = \underbrace{(0 - 0.96)}_{x} . BV_{dc} \tag{5.4}$$

The variable x defined in (5.4) contains the information of ST duty ratio and Boost factor as per the relationship:

$$D = 1 - \frac{12\left(2-\sqrt{3}\right).x}{\pi} \tag{5.5}$$

$$B = \frac{1}{1-2D} \tag{5.6}$$

Substituting (5.5) into (5.6) we get

$$B = \frac{\pi}{\left(24\left(2-\sqrt{3}\right).x\right)-\pi} \tag{5.7}$$

Substituting (5.4) in (5.3)

$$V_{ab} = 0.761.\underbrace{x.B}_{U}V_{dc} \tag{5.8}$$

The unified reference vector 'U' defined in (5.8) adjusts the output line voltage as per the change in input dc source voltage.

The relationship between x and U can be written as:

$$U = x.B \tag{5.9}$$

Also, it can be written as

$$x = \frac{\pi.U}{\left(U.\left(24.\left(2-\sqrt{3}\right)\right)-\pi\right)} \tag{5.10}$$

A plot between the unified voltage vector (U) and the range of reference vector (V_{ref}) is plotted in Fig. 5.1.

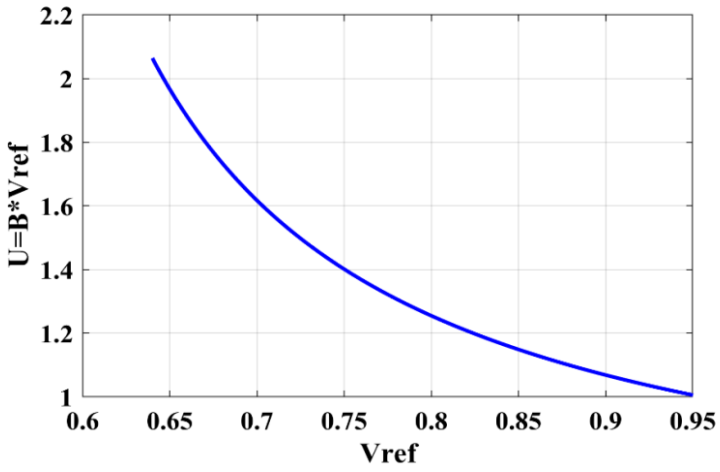


Fig. 5.1. Plot of unified reference vector (U) Vs reference vector (V_{ref}).

5.2.2. Block diagram

In this control scheme, first, the input dc source voltage is sensed. Then, for the preset value of the line voltage, the unified voltage vector is found using equation (5.8).

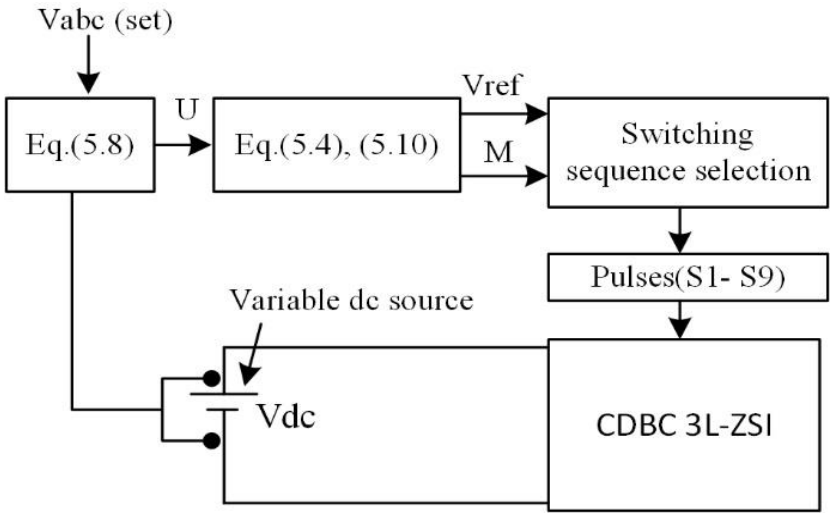


Fig. 5.2. Control block diagram of the unified closed-loop controller.

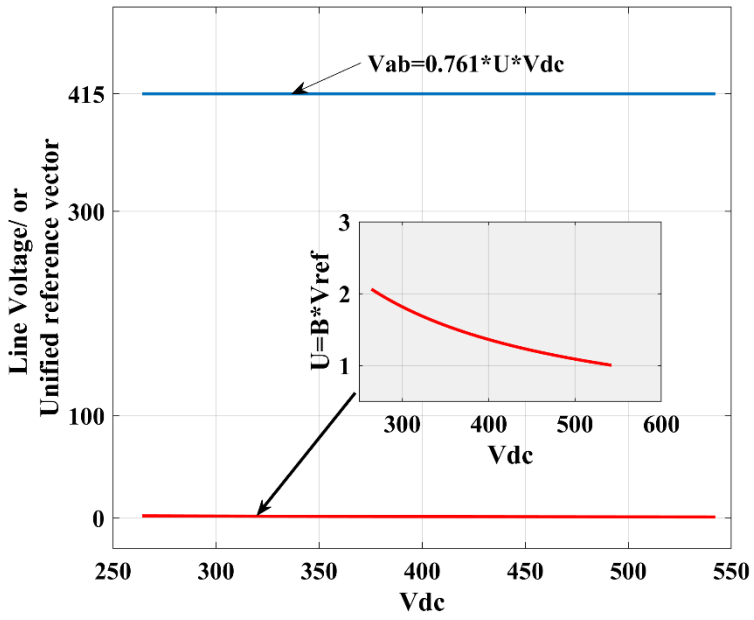


Fig. 5.3. Plot of output line voltage (V_{ab}) versus input dc source voltage (V_{dc}), and unified reference vector (U) versus input dc source voltage (V_{dc}).

From the value of 'U', the corresponding value of the reference vector and boost factor is calculated using the equation (5.9) and (5.10). It has been shown in Fig. 5.3 that for the fluctuation in the input dc source voltage, the unified control technique appropriately adjusts the unified voltage vector and the output ac voltage magnitude is maintained constant to 415V (rms).

5.3. RESULTS

The unified closed-loop control has been simulated in MATLAB/SIMULINK software using the CDBC 3L-ZSI configuration of Fig. 3.3 of chapter 3. The parameters used in the simulation have been summarized in Table 5.1.

Table 5.1. Parameters used for simulation

Parameter	Value/name
Inductors (L_1, L_2)	10mH
Capacitor C_3, C_4	600uF
Three-phase load parameters	25 Ω, 4mH
Output LC filter	10mH, 1000uF
Fundamental Frequency (F_1)	50Hz
Switching cycle	208usec.
Output line voltage (rms)	415V
PWM switching pattern	ZSVM_1TI
Boost control technique	Improved maximum boost control (IMBC)

The variable input dc source has been considered to simulate the characteristics of the PV source. The control technique has been designed to obtain the desired output line voltage rms value of 415V.

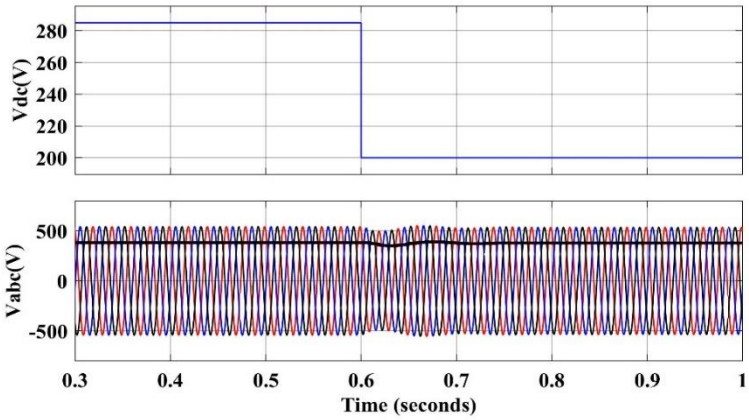


Fig. 5.4. Simulation waveforms of input dc source voltage and output line voltage using unified control of ZSI.

The simulation waveform of input dc source voltage and output line voltage is shown in Fig. 5.4. In steady-state when the input dc source voltage is 285V, the output line voltage peak and rms value of inverter are 542V and 415V, respectively. At an instant of 0.6sec., the input dc source voltage is changed from 285V to 200V. At this instant, the unified control technique automatically adjust the values of unified voltage vector to generate the output line voltage rms value of 415V (see Fig. 5.4).

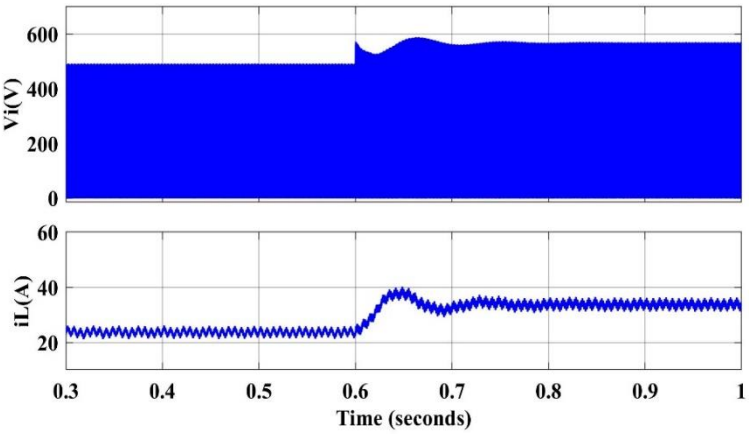


Fig. 5.5. Simulation waveforms of dc-link voltage and inductor current.

The simulation waveform of dc-link voltage and inductor current is shown in Fig. 5.5. It can be noticed from Fig. 5.5 that the dc-link voltage peak increases as the input dc source voltage decreases at 0.6sec. Also, the increase in the inductor current indicates the change in the boost factor of ZSI. In Fig. 5.6 it has been shown that the input dc source capacitors voltage is balanced.

The ripple component in the input capacitors voltage is due to the switching state of 3L-ZSI. The switching states of 3L-ZSI periodically allow upper and lower capacitor charging/discharging.

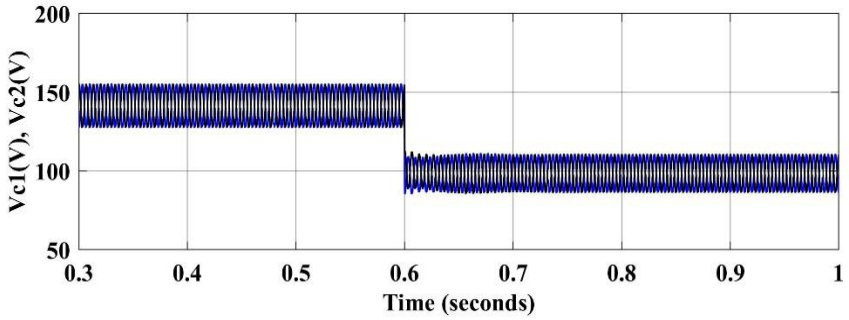


Fig. 5.6. Simulation waveforms of input dc source capacitors.

Fig. 5.7 indicates the THD percentage and peak value of the line voltage. The THD percentage of line voltage is 0.42 which indicates that the output line voltage waveforms have superior quality.

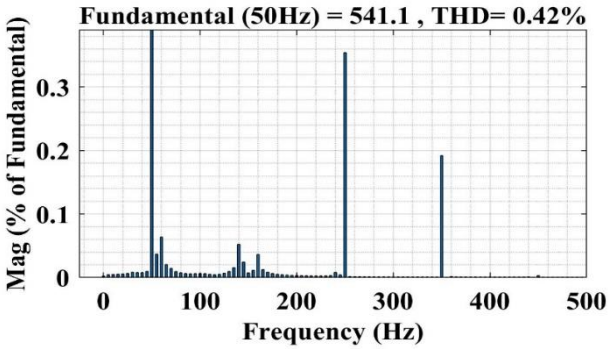


Fig. 5.7. THD plot of output line voltage.

5.4. CONCLUSION

It has been shown in this chapter that the unified control technique successfully adjusts the boost factor and modulation index to control the output line voltage of 3L-ZSI operating with variable dc source. This dc-link voltage has been fully utilized using the improved maximum boost control of voltage boosting which results in reduced switching stress across the power switches. The one control degree of freedom offered by this feedback technique offers easier implementation.

CHAPTER 6. CONCLUSION AND FUTURE SCOPE

6.1. CONCLUSION

This research work is focused on the PWM techniques of 2L-ZSI, and the topology as well as PWM technique aspect of 3L-ZSI. Chapter 2 of this work explored the application of advanced bus clamping (ABC) switching sequences for the improvement in the performance of 2L-ZSI. In this chapter, the ABC switching sequences have been designed to reduce the impedance network (IN) inductor current ripple of the conventional ZSI. It has been successfully verified that the proposed SVPWM technique (ABC4_MCB) offers around a 34 percent reduction in the IN inductor current ripple as compared to the conventional SVPWM operating with the same boost control approach and the equal switching frequency of the power switches. It has been claimed here that the proposed ABC4_MCB technique is equally valid for other advanced topologies of 2L-ZSI.

Next, a controlled diode bridge clamped (CDBC) configuration of 3L-ZSI has been successfully validated and reported in chapter 3. CDBC configuration of 3L-ZSI optimizes the number of controlled power switches as compared to the T-type and NPC ZSI. Also, a new SVPWM switching pattern is successfully verified using CDBC ZSI inverter circuitry. The proposed SVPWM switching pattern optimizes the number of switching transitions per carrier cycle when compared to the existing SVPWM switching techniques. The dependency of the modulation index on the switching frequency of the power switches has been also highlighted in chapter 3 of this research work.

An improved maximum boost control (IMBC) technique of voltage boosting is successfully verified in chapter 4. It has been proved in this chapter that the proposed IMBC technique eliminates the problem of the sixth fundamental frequency ripple components of the IN inductor current prevailing in the existing MBC of voltage boosting. Furthermore, the proposed reduced common-mode voltage (CMV) switching patterns of 3L-ZSI increases the switching frequency of the impedance network (IN) at competitive switching frequency of the power switches when compared to the existing reduced CMV PWM technique of 3L-ZSI. This results in reduced IN size of 3L-ZSI with magnitude of CMV limited to $1/6^{th}$ of the available dc-link voltage.

Finally, in chapter 5, a feedback control based on the unified control algorithm has been implemented in CDBC 3L-ZSI for the application of isolated PV power generation.

6.2. FUTURE SCOPE

The buck-boost inverters have the potential to improve the performance of the dc-ac power conversion unit used in any application such as distributed power generation, electric vehicle, and drives, etc. Based on the research work carried out in this thesis, the prospective work which can be pursued further is as under:

- The ABC PWM switching sequences can be explored further for the various other aspects of ZSI. For example, THD in the output line current, input current ripple cancellation, reduced switching and conduction losses, and reduced CMV magnitude PWM techniques.
- The modified SVPWM proposed in chapter 4 of this thesis can be investigated for higher-level configurations of ZSI. Also, the application of modified SVPWM switching state diagram can be traced for the case of multilevel VSIs.
- The neutral point potential balancing algorithms can be designed for the proposed ZSVM_1TI and ZSVM_2TI PWM techniques.

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