Analysis of the Power Dissipation of a Linearly Graded Profile in the Drift Region of a 6H-SiC DIMOSFET

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in

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CERTIFICATE

I, **Vinit Kumar (Roll No.-60661025)** hereby certify that the work which is being presented in this thesis entitled **"Analysis of the Power Dissipation of a Linearly Graded Profile in the Drift Region of a 6H-SiC DIMOSFET"** by me in partial fulfillment of requirements for the award of degree of **Master of Technology in VLSI Design & CAD** from **Thapar University, Patiala** is an authentic record of my own work carried under the supervision and guidance of **Dr. A.K. Chatterjee**, Professor & Head, Electronics & Communication Engineering Department, Thapar University, Patiala.

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ABSTRACT

In automotive, aerospace and energy production industries, the semiconductor based electronic devices that can function at ambient temperatures higher than 150^oC without external cooling system could greatly benefit a variety of application. A practical operation of silicon power devices at ambient temperature above 200^oC appears problematic, as self-heating at higher power levels results in high internal junction temperatures and leakages. Thus, most electronic subsystems that simultaneously require high-temperature and high power operation will necessarily be realized using wide bandgap devices.

The Silicon carbide (SiC) is wide bandgap semiconductor material that replaces Si material very quickly in the semiconductor industry because of its superior intrinsic properties like lower intrinsic carrier concentration (10–35 orders of magnitude), higher electric breakdown field (4–20 times), higher thermal conductivity (3–13 times), larger saturated electron drift velocity (2–2.5 times); which is suitable for fast device operation with high voltage and high switching frequency.

The present work aims at the design of high breakdown voltage 8kV 6H-SiC Double implanted metal-oxide semiconductor field-effect transistor (DIMOSFET) with uniformly and linearly graded doping profile of drift region. In linearly graded doping profile, it is found that the height of the drift region (h) decreases (148.17µm to 119.61µm), which reduces the specific on resistance $R_{on,sp}$. Here $R_{on,sp}$ (specific on resistance) equal to R_D (Specific on resistance of the drift region) for high breakdown voltages. And the power dissipation (P_D) with 8kV breakdown voltage (V_b) decreases to the value of 29.56W from 43.88W at a fixed forward current density (J_f=1000A/cm^2) and effective doping level (N_d=3.91x10^{14}cm^{-3}). The percentage power saved in linearly graded doping profile is about 32.64% as compared to the uniformly doped profile, but it decreases with further increase in the effective doping level.

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CHAPTER–1

INTRODUCTION

Silicon-based power devices have long dominated the power electronics and power systems applications. Devices such as bipolar, unipolar, controlled, uncontrolled, and MOS-gated made by Si are widely used by power electronics and power systems designers. Examples of such devices are diodes (p-i-n and Schottky rectifiers), thyristors, gate turn-off thyristors (GTOs), bipolar junction transistors (BJTs), insulated-gate bipolar transistors (IGBTs), and power metal–oxide–semiconductor field-effect transistors (MOSFETs).

Large-area devices that are capable of handling thousands of amperes and kilovolts such as IGBTs are now able to handle voltages up to 6 kV and currents up to 1200 A [1]. IGBTs are being widely used for motor drives, resonant converters, and power supplies [2–4]. GTOs and thyristors are still widely used for very high power applications, such as power systems conditioning equipment, dynamic voltage regulators, transfer switches, and large direct-current rectifiers [5–8]. MOSFETs have high conduction losses due to their high on-state resistance, R_{dson}. As the blocking voltage increases, so does their on-state resistance R_{dson}, hence, making MOSFETs less attractive for high-voltage applications (beyond 600 V). Recent enhancements in power MOSFET technology such as the Cool MOS allow for substantial reduction of the conduction losses.

But the need for faster devices with high voltage and high switching frequency capability is growing, Silicon-based devices are not able to meet these requirements without costly cooling systems, so Wide band-gap based semiconductor devices such as silicon carbide and gallium nitride offer multiple advantages for power electronic designers. The superior physical properties of these semiconductors offer a lower intrinsic carrier concentration (10–35 orders of magnitude), a higher electric breakdown field (4–20 times), a higher thermal conductivity (3–13 times), a larger saturated electron drift velocity (2–2.5 times) which is suitable for faster devices with high voltage and high switching frequency.

1.1 WBG SEMICONDUCTOR

Generally, a wide band gap (WBG) semiconductor is a semiconductor with an energy band gap wider than about 2eV. Examples of WBG semiconductors are gallium nitride (GaN, E_G = 3.4eV), aluminum nitride (AlN, E_G = 6.2eV), and silicon carbide (SiC, E_G between 2.2eV to 3.25eV depending on polytype). Polytype mean 3C, 4H, 6H, 15R-Silicon Carbide [9].

Since the electronic properties of a semiconductor are dominated by the highest partially empty band and the lowest partially filled band, it is often sufficient to only consider those bands. This leads to a simplified energy band diagram for semiconductors.

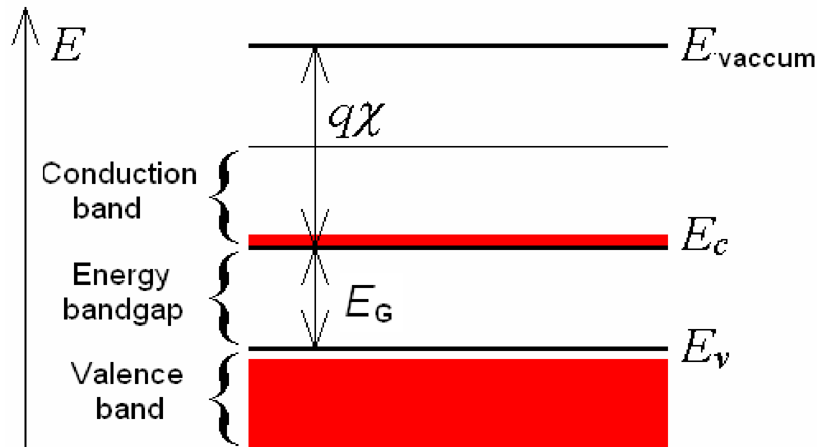


Figure-1.1: Energy band diagram where the energy band gap, E_G, valence band edge, E_v, and the conduction band edge, E_c The vacuum level, E_{vacuum}, and the electron affinity, χ.

The numerous polytypic forms of silicon carbide, 4H-and 6H-SiC electronic devices presently most useful due to the availability and quality of reproducible single crystal wafers of these polytypes. The availability of 6H-SiC and 4H-SiC polytypes in bulk wafer form has helped SiC to emerge as one of the relatively mature wide-band semiconductor technologies. SiC is a material with immense potential for use in hetero-structure electronic devices, which take advantage of differing band gaps, carrier mobilities, etc. However, there are many crucial crystal growth and device fabrication issues that have to be addressed before SiC-based devices and circuits are ready for scale up and reliable incorporation into electronic systems.

1.2 SILICON CARBIDE

Silicon carbide is a WBG semiconductor that possesses extremely high thermal, chemical, and mechanical stability. It is so thermally stable that dopant impurities cannot be diffused at any reasonable temperature; so chemically stable that it is impervious to any known chemical enchants; and so mechanically stable that it is used as a coating for drill bits and saw blades.

Single-crystal SiC forms in the hexagonal lattice, with alternating hexagonal planes of silicon and carbon atoms, as shown in Fig.1.2 Each silicon atom bonds to four nearest-neighbor carbon atoms, and each carbon atom bonds to four nearest-neighbor silicon atoms (bonds are not shown). Note that the atoms in the second silicon plane are offset with respect to the atoms in the first silicon plane. As successive planes are added, each plane must be offset with respect to the plane below. This stacking sequence leads to different flavors, or polytypes, of the basic SiC crystal. There are a large number of possible polytypes, but the most important are 3C, 4H, and 6H. The polytypes differ in band gap energy, carrier mobility, and breakdown field. For example, the E_G = 2.2, 3.25, and 3.0 eV for 3C, 4H, and 6H-SiC respectively [9].

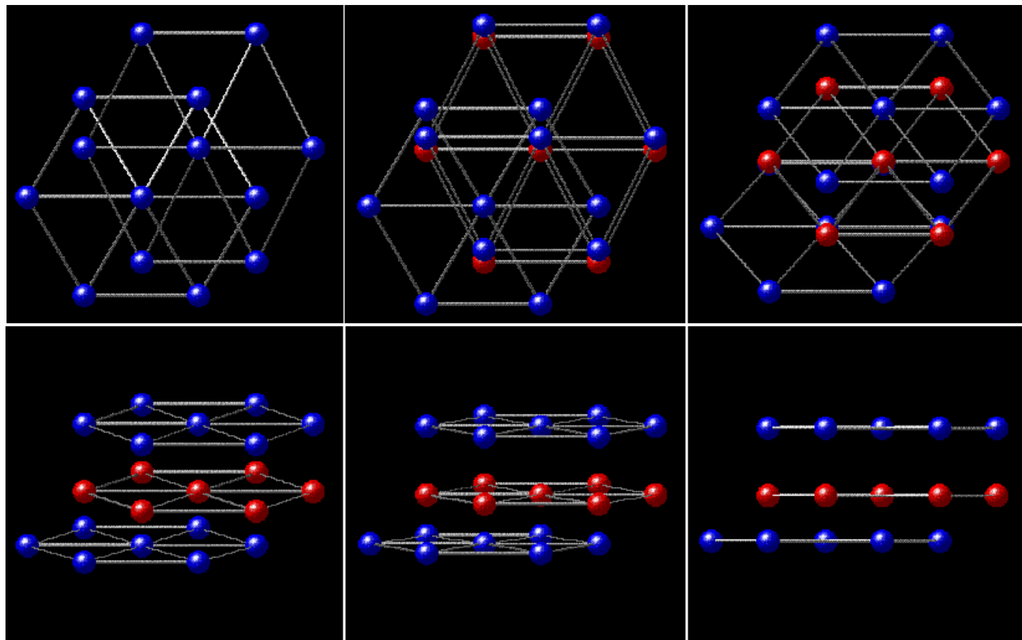


Figure-1.2: Primitive crystal structure of SiC [9].

Silicon atoms (blue) and carbon atoms (red) form alternating hexagonal planes. The sticks in this rendering are intended to emphasize the hexagonal lattice arrangement, and do not represent bonds. Each carbon atom bonds to three silicon atoms in the plane below and to one silicon atom in the plane above (bonds not shown). Note that the silicon atoms in the top plane are offset with respect to the silicon atoms in the bottom plane.

1.2.1 IMPORTANCE OF SiC

Silicon carbide is the only WBG semiconductor that possesses a high-quality native oxide suitable for use as an MOS insulator in electronic devices. Thermal oxidation of SiC produces a layer of SiO_2 on the surface, while the carbon atoms from the SiC form CO, which escapes as a gas. Thus it is possible to make all the devices found in silicon IC technology in SiC, including high quality, stable MOS transistors and MOS integrated circuits.

The breakdown field in SiC is about 8 times higher than in silicon. This is important for high-voltage power switching transistors. For example, a device of a given size in SiC will have a blocking voltage 8 times higher than the same device in silicon. More importantly, the on-resistance of the SiC device will be about 100 times lower than the silicon device [9]. Other properties shown in Fig.1.3.

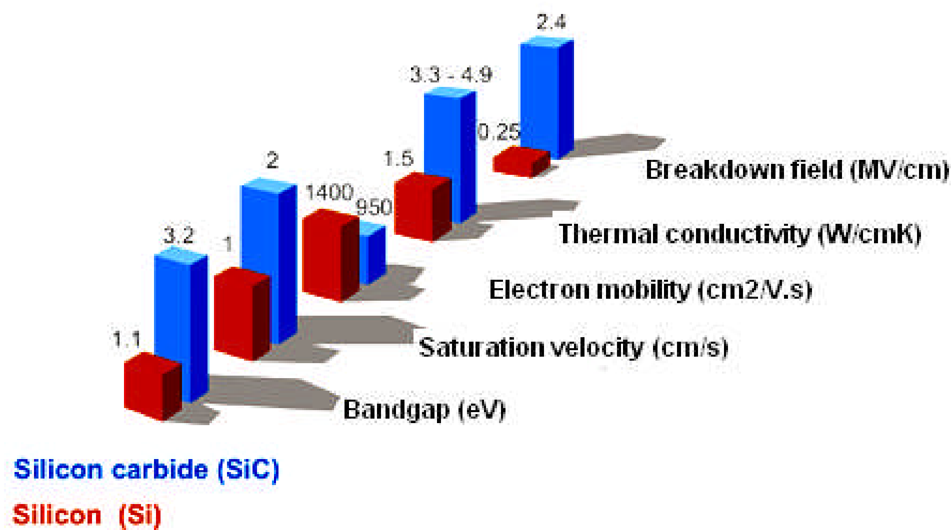


Figure-1.3: Comparison of SiC properties over Si [10].

Because the band-gap of SiC is so much wider than silicon as shown in Fig.1.3, thermal generation of electron-hole pairs is many orders of magnitude lower at any given temperature. This makes it possible to build “dynamic” memories (DRAMs) in SiC that only need to be refreshed about once every 100 years at room temperature. This also makes it possible to operate SiC devices at temperatures as high as 650°C without degradation in electrical performance.

1.2.2 SILICON CARBIDE POLYTYPES

Silicon carbide is known as a wide band-gap semiconductor existing in many different polytypes. All polytypes have a hexagonal frame with a carbon atom situated above the center of a triangle of Si atoms and underneath a Si atom belonging to the next layer Fig.1.4. The distance, a, between neighboring silicon or carbon atoms is approximately 3.08 Å for all polytypes. The carbon atom is positioned at the center of mass of the tetragonal structure outlined by the four neighboring Si atoms so that the distance between the C atom to each of the Si atoms is the same. Geometrical considerations give that this distance, C-Si, is $a(3/8)^{1/2}$ i.e. approximately equal to 1.89 Å. The distance between two silicon planes is, thus, $a(2/3)^{1/2}$ i.e. approximately 2.52 Å. The height of a unit cell, c, varies between the different polytypes. The ratio c/a, thus, differs from polytype to polytype, but is always close to the ideal for a closed packed structure. This ratio is for instance approximately 1.641, 3.271 and 4.908 for the 2H-, 4H- and 6H-SiC polytypes, respectively whereas the equivalent ideal ratios for these polytypes are $(8/3)^{1/2}$, $2(8/3)^{1/2}$ and $3(8/3)^{1/2}$, respectively. The difference between the polytypes is the stacking order between succeeding double layers of carbon and silicon atoms [11].

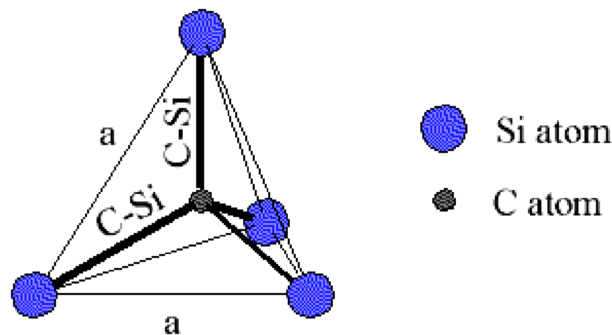


Figure-1.4: Tetragonal bonding of a carbon atom with the four nearest silicon neighbors [11].

In Fig.1.5 the stacking sequence is shown for the three most common polytypes, 3C, 6H and 4H. If the first double layer is called the A position, the next layer that can be placed according to a closed packed structure will be placed on the B position or the C position. The different polytypes will be constructed by permutations of these three positions. For instance will the 2H-SiC polytype have a stacking sequence ABAB… The number thus denotes the periodicity and the letter the resulting structure which in this case is hexagonal. The 3C-SiC polytype is the only cubic polytype and it has a stacking sequence ABCABC… or ACBACB… A common crystalline defect is the so called Double Positioning Boundary (DPB), which is commonly seen in 3C-SiC grown on on-axis 6H-SiC substrates. The defect arises when islands of the two possible stacking sequences ABCABC and ACBACB meet.

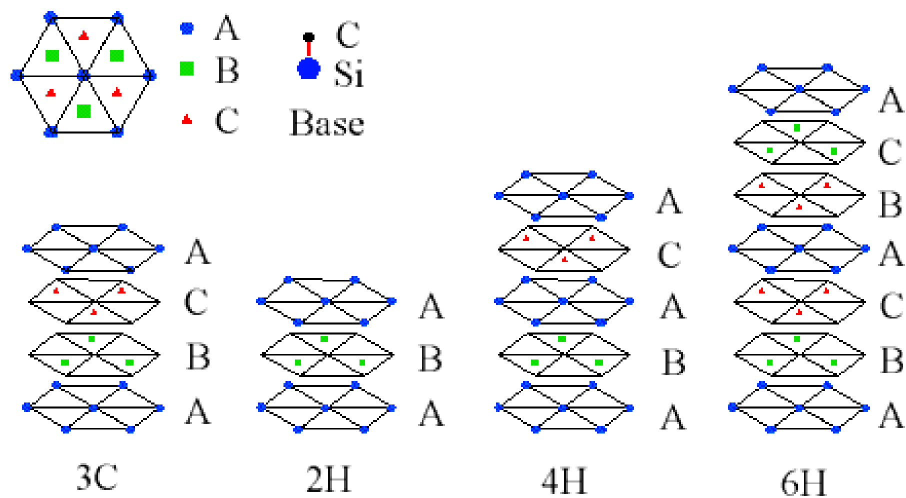


Figure-1.5: The stacking sequence of double layer of the three most common SiC polytypes [11].

There are some 200 polytypes proven in existence, some with a stacking period of several hundred double layers. It is hard to understand how these crystals grow since there has to exist some 'memory' which guides the atoms into the right stacking sequence. When for instance the 6H-SiC polytype grows each atom landing on the surface must sense at least 6 layers down in order to find its proper site. When the stacking sequence amounts to several hundred double layers it becomes even more difficult to understand how these crystals can grow. There are however growth mechanisms which aid the atoms

into finding the correct site. By looking at a SiC crystal along the c-direction all polytypes would look the same since this is the direction the layers are stacked. If one would look at the crystals from the edge, the stacking sequence would easily be seen provided one was gifted with atomic resolution eyesight. The spiral will provide a step which may show the whole or part of the stacking sequence on the side. Since the growth proceeds at the edge of the spiral, the impinging atoms will be guided both by the underlying atoms and the atoms on the side of the spiral. A similar approach is used in order to grow Chemical Vapor Deposition (CVD) layers at lower temperatures. In this case off-axis polished substrates are used in order to produce the necessary steps. It is possible to grow 6H-SiC on on-axis substrates by CVD, however, it normally requires slightly elevated temperatures. It is not established if the growth in this case proceeds as spiral growth. It is likely that the surface energy of different sites differs. This energy would be a superposition of energies ranging far down in the crystal, which would be acting as a sort of 'memory'. The impinging atoms must have a surface mobility which is high enough in order to move to the most favorable position. This energy difference between two possible positions may be very small and it is possible that the growth eventually develops into a spiral which would provide the highest growth rates at the lowest cost in energy (fewer stacking faults) [11].

By observing the SiC crystal from the side as previously proposed, the stacking sequence can be projected as in Fig.1.6 where the 6H-SiC polytype is shown. When the stacking sequence is drawn in this manner a zig zag pattern is revealed. The surrounding lattice does not, however, look the same for each position. In the Fig.1.6, the A position has a different surrounding lattice than the B and C positions. We call this position the hexagonal site, h. It is simply characterized as the turning point of the zig zag pattern. The other two positions (B and C) are called cubic, k1 and k2. An impurity replacing a host atom at one of the three sites will obtain a different binding energy depending on the site it replaces. A very illustrative example is the nitrogen donor in 6H-SiC. The hexagonal site gives rise to the P-level of the nitrogen donor with a binding energy of approximately 85 meV. The two cubic sites will give the R- and S-levels with binding energies around 138 meV and 142 meV, respectively. In the 4H-SiC polytype there are

only two in-equivalent sites, one hexagonal and one cubic (Fig.1.6). The two levels of the nitrogen donor are in this case called P and Q. In 3C there is of course only one cubic site and in 2H there is only one hexagonal site (Fig.1.6). The 6H-SiC polytype can thus be characterized as being 33% hexagonal, whereas the 4H- and 2H-SiC polytypes are 50% and 100% hexagonal, respectively.

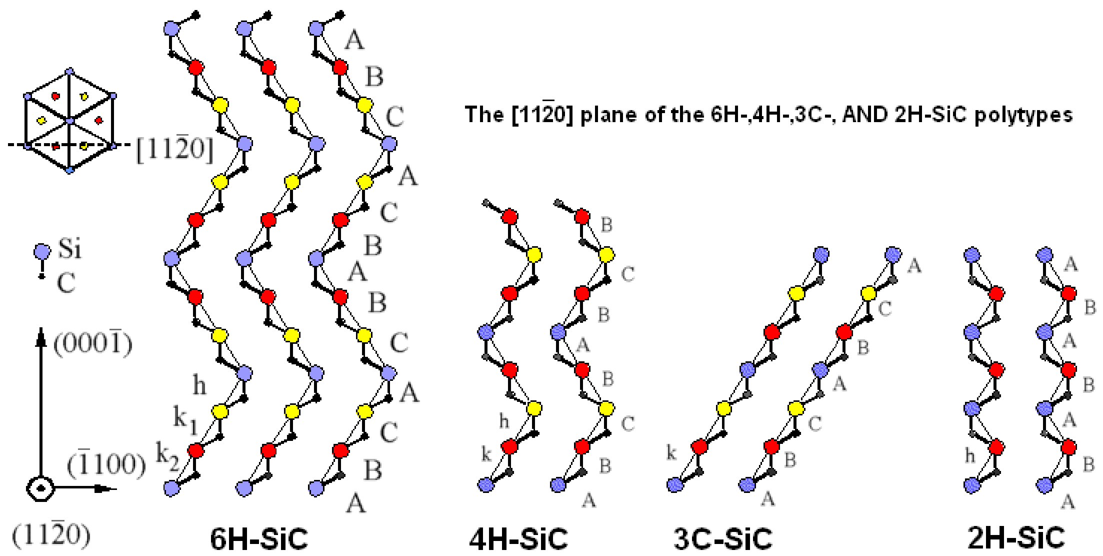


Figure-1.6: The plane of the 6H-, 4H-, 3C-, and 2H-SiC polytypes [11].

There are four hexagonal Miller indices describing the directions in all SiC polytypes except for the 3C polytype where the normal cubic notation is used. The last hexagonal index refers to the c-direction, whereas the three first describes directions in the basal plane. The angle between two adjacent basal plane axis is 120° as shown in Fig 1.7. By definition, the sum of the first three indices must be zero. One of them is thus redundant but is kept for simplicity.

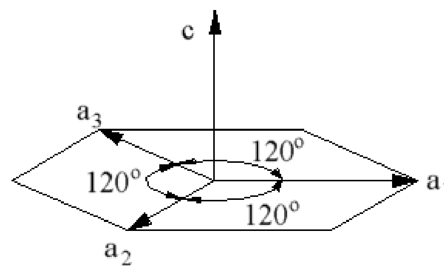


Figure-1.7: The Miller indices describing the hexagonal structure [11].

The plane formed by a bi-layer sheet of Si and C atoms is known as the basal plane, while the crystallographic c-axis direction, also known as the stacking direction or the [0001] direction, is defined normal to Si-C bi-layer plane. Fig.1.8 schematically depicts the stacking sequence of 6H-SiC polytype, which requires six Si-C bi-layers to define the unit cell repeat distance along the c-axis [0001] direction. The [1100] direction depicted in Fig.1.8 is often referred to as the a-axis direction. The silicon atoms labeled "h" or "k" in Fig.1.8 denote Si-C double layers that reside in "quasi-hexagonal" or "quasi-cubic" environments with respect to their immediately neighboring above and below bilayers. SiC is a polar semiconductor across the c-axis, in that one surface normal to the c-axis is terminated with silicon atoms while the opposite normal c-axis surface is terminated with carbon atoms. As shown in Fig.1.8, these surfaces are typically referred to as "silicon face" and "carbon face" surfaces [12].

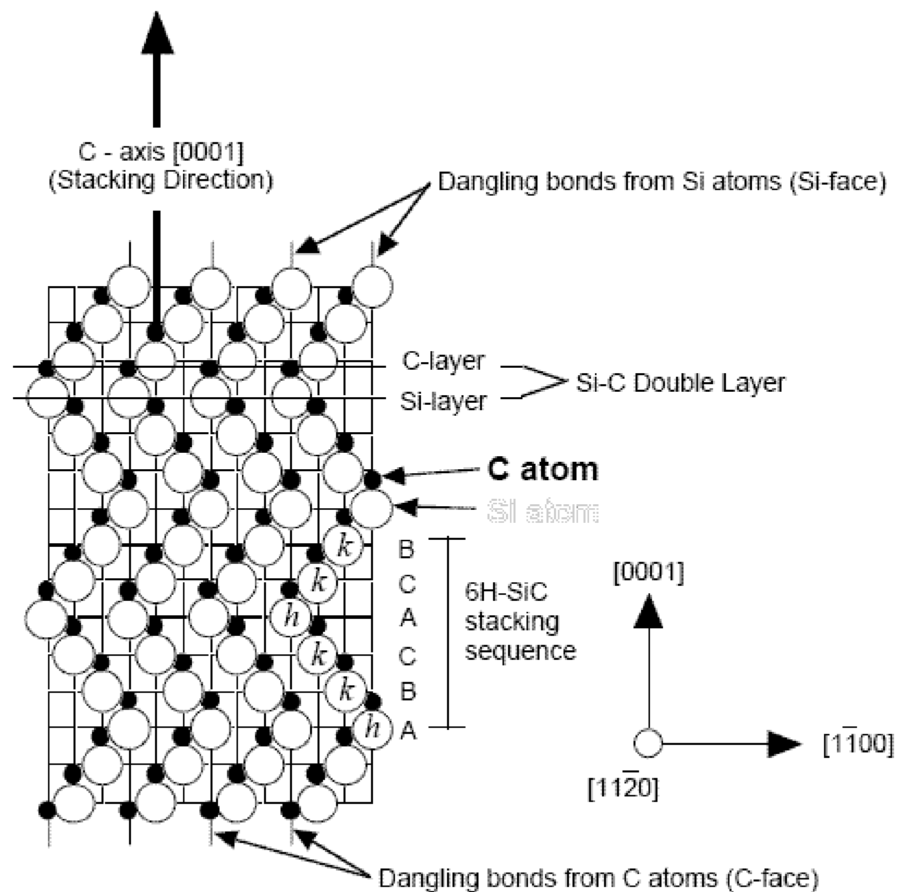


Figure-1.8: Schematic cross-section of SiC of {(1120) plane} the 6H SiC polytype [12].

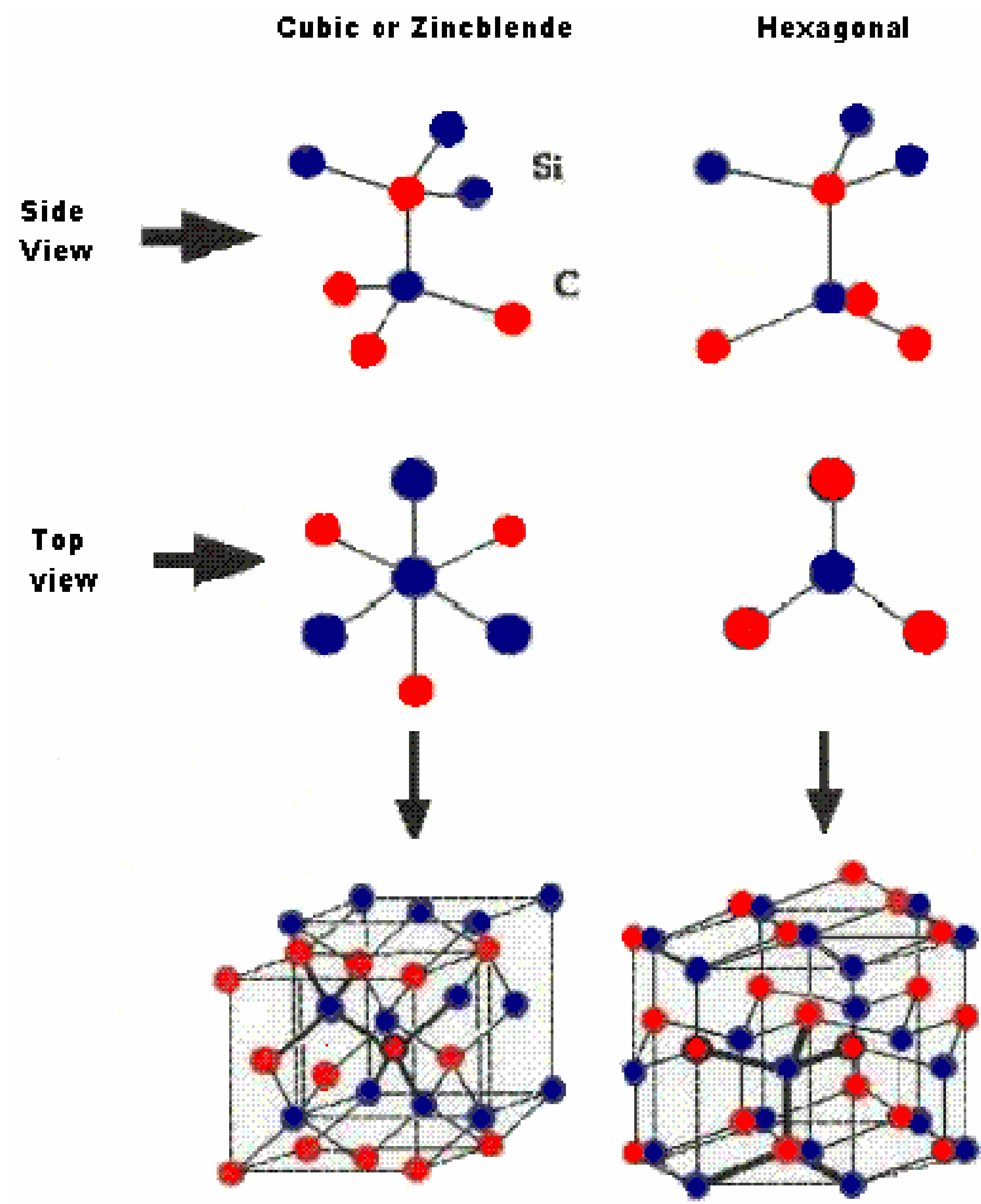


Figure-1.9: Crystal structure of Silicon Carbide [9].

1.3 COMPARISON OF PROPERTIES OF SiC, Si & GaAs

Silicon Carbide (SiC), has superior properties for power devices as compared to silicon. Silicon carbide (SiC) device development is increasing due to the need for electronic devices capable of operation at high power levels and high temperature. The main strength of silicon carbide is that it can resist high field strengths, it offers better heat-conducting capacity than copper at room temperature and it has a large energy band gap, which means that electrical components continue functioning even when the mercury starts climbing. With very high thermal conductivity (~5.0W/cm-K), high saturated electron drift velocity (~2.7×10^7cm/s) and high breakdown electric field strength (~3MV/cm), SiC is a material of choice for high temperature, high voltage, high frequency and high power applications[12]. Table 1.1 lists electrical properties of the common SiC polytypes in comparison to that of Si and GaAs [13].

The most important SiC property of all is the large bandgap, which is nearly three times larger than that of silicon. The large S-C bonding energy makes SiC resistant to chemical attack and radiation. Silicon carbide belongs to a class of semiconductors commonly known as wide band gap semiconductors, where conventional semiconductors like Si and GaAs cannot adequately perform under extreme conditions. The wider band gap of SiC also enables one to design smaller, higher density devices that will withstand high voltages. The high thermal conductivity of SiC decreases the need for special packaging and system cooling for device operation [13].

Table-1.1: Comparison of properties of SiC with Si and GaAs at room temperature [13].

Properties	Si	GaAs	6H-SiC	4H-SiC	3C-SiC
Energy Bandgap (eV)	1.1	1.42	3.0	3.2	2.3
Breakdown Field @10^{17} (MV/cm)	0.6	0.6	3.2	3.0	>1.5
Electron Mobility (cm^2/V-s)	1100	6000	370	800	750
Saturated Electron Drift Velocity (cm/s)	10^7	10^7	2×10^7	2×10^7	2.5×10^7
Thermal Conductivity (W/cm-K)	1.5	0.5	4.9	4.9	5.0
Hole Mobility (cm^2/V-s)	420	320	90	115	40

1.4 SILICON CARBIDE DEVICES

Silicon carbide has several unique properties (higher breakdown field, wider band-gap, lower thermal generation rate, and lower intrinsic carrier concentration) to enhanced performance in devices.

1. Power MOSFETs

The breakdown electric field of SiC is approximately 8x higher than silicon. This makes it possible to design power switching devices having correspondingly higher blocking voltages than their silicon counterparts. More importantly, the specific on-resistance (i.e. resistance-area product) of a power device scales inversely as the cube of the breakdown field, so the on-resistance of SiC power MOSFETs are 100-200x lower than comparable devices in silicon [9].

2. Lateral Power MOSFETs

The maximum blocking voltage of vertical power devices in SiC is presently limited by the thickness of commercially available epi-layers. The developed first lateral power MOSFETs in SiC, exhibit blocking voltages of 2.6 kV, which is a new world record.

3. Schottky Barrier Diodes

Schottky barrier diodes (SBD's) are attractive as power rectifiers because they do not store minority carriers in the on-state, and therefore can be switched off quickly with negligible reverse current. It is widely felt that SBD's will be the first SiC power devices to go into commercial production. The fabricated SBD's on 4H-SiC that exhibit blocking voltages of 1720 V, equal to the current world record.

4. Microwave Devices

The high saturated drift velocity, high breakdown field, and high thermal conductivity of SiC make it an ideal material for high-power microwave amplifiers in the 1-10 GHz regime. Two types of devices are under development: a vertical device known as a static induction transistor (SIT) and a lateral MESFET with sub-micron gate.

5. IMPATT Diode Microwave Oscillators

IMPATT diodes are two-terminal semiconductor devices that generate RF power by introducing a 180° phase shift between current and voltage waveforms at microwave frequencies.

6. CMOS Integrated Circuits

The first 6H-SiC CMOS digital integrated circuits completed in September 1996. A second generation was completed in March 1997. These are the first SiC CMOS circuits fabricated with an implanted P-well process, and the first to operate on a single 5V power supply [9].

7. Nonvolatile Memories

The thermal generation rate in semiconductors is proportional to the intrinsic carrier concentration n_i, and n_i decreases exponentially with band gap energy. Wide band gap semiconductors have dramatically lower thermal generation, with the thermal generation rate of 6H-SiC being about 16 orders-of-magnitude lower than silicon. This makes it possible to construct one-transistor memory cells in SiC which retain information for many years without power.

8. Charge Coupled Devices

CCDs are unique MOS devices in which charge packets are shifted laterally along the semiconductor surface by appropriate clocking applied to surface electrodes. CCDs are widely used as imagers in video cameras and digital still cameras. They have developed the first CCDs in SiC, where the wider bandgap makes it possible to image scenery in the UV portion of the spectrum without being overwhelmed by visible light.

9. NMOS Integrated Circuits

The low thermal generation rate in SiC makes it possible to operate integrated circuits at much higher temperatures than silicon. Their group developed the first digital integrated circuits in SiC in late 1993. These early circuits were implemented in enhancement mode NMOS.

1.4.1 SILICON CARBIDE POWER MOSFETs

Power switching devices are reaching fundamental limits imposed by the low breakdown field of silicon, and substantial improvements can only be achieved by using a semiconductor with a higher breakdown field. Power switching devices in silicon carbide (SiC), a compound semiconductor with a breakdown field about 10 times higher than silicon.

SiC is unique among compound semiconductors in that its native oxide is SiO_2, the same oxide as silicon. This means that the workhorse power devices used in silicon, i.e. the power MOSFET, insulated gate bipolar transistor (IGBT), and various types of MOS-controlled thyristors (MCTs) can all be fabricated in SiC. Because of the higher breakdown field, SiC power devices can have specific on-resistances up to 400 times lower than similar devices in silicon [9].

The WBG group is focusing on power MOSFETs in SiC. MOSFET work is centered on two types of devices: DMOS and UMOS.

1.4.1.1 DMOS

The DMOS, or “Double-implanted MOS”, power MOSFET is shown in Fig.1.10. This device is analogous to the silicon “DMOS”, or “double-Diffused MOS”, power MOSFET except that the P base and N^+ source regions are produced by ion implantation instead of thermal diffusion (diffusion is not practical in SiC because of the very low diffusion coefficients in the material).

The first SiC DMOS power transistors were developed in June 1996 [15-16]. These devices exhibited blocking voltages in excess of 760V, approximately 3 times higher than the best SiC MOSFETs up to that time. Specific on-resistance was 125mΩ-cm^2 for the 760V devices and 66 mΩ-cm^2 for 2 µm channel length devices on the 500V wafer. In June 1997 we introduced Lateral DMOS (LDMOS) power transistors in SiC [17-18]. These devices exhibited a blocking voltage of 2.6kV, which is still the highest blocking voltage for any SiC power switching device.

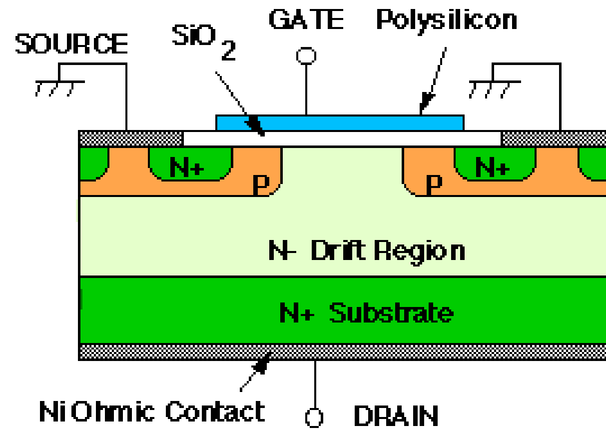


Figure-1.10: Cross section of a SiC ion-implanted "DMOS" power transistor [14].

In DMOS device, a positive bias on the poly-silicon gate creates a surface inversion layer at the interface between the SiO2 and the P-type SiC. Electrons flow from the N^+ source along the inversion layer to the N-drift region. Upon reaching the drift region, electrons flow vertically to the N^+ drain at the bottom. The thick, lightly doped N-drift region is needed for large drain voltage when the device is in the off state (gate at ground).

1.4.1.2 UMOS

Most of the previous work in SiC power transistors has been devoted to the trench-gate or "UMOS" power transistor, shown in Fig.1.11. The electric fields in the blocking state (transistor OFF) are shown at the right. Looking at the blue (right-hand) plot, we note that the electric field in the oxide at the bottom of the trench is 2.5 times higher than the peak field in the semiconductor. Such a high electric field will lead to catastrophic breakdown of the oxide. The field at the corner of the trench is even higher due to two-dimensional effects. This oxide breakdown problem represents a major limitation to the UMOSFET structure in SiC.

Fig 1.12 shows a novel UMOS structure with Integral Oxide Protection (IOP) that limits the electric field in the trench oxide while simultaneously reducing on-resistance. This structure is shown in Fig.1.12, along with the electric fields in the blocking state.

The new P-type region in the bottom of the trench reduces the electric field at the oxide/semiconductor interface to zero, thereby protecting the oxide from high electric fields in the blocking state. The new N-type epilayer beneath the P-base prevents pinch-off of the conducting channel in the on-state and facilitates lateral current spreading into the drift region. The device in Fig.1.12 also includes a lightly-doped N-type epilayer grown on the sidewalls of the trench. This layer converts the device into an accumulation-layer MOSFET, or "ACCUFET", increasing the MOSFET mobility and further reducing on-resistance.

Fig.1.13 shows the static I-V characteristics of an IOP-UMOS ACCUFET in 4H-SiC [5]. The blocking voltage is 1400V, which is 87% of the theoretical value for the 10 μm drift region in our device. Breakdown is non-destructive, indicating that oxide failure does not occur. In fact, numerical simulations show that the peak electric field in the oxide is only 3MV/cm at the blocking voltage of 1400V. The specific on-resistance is 15.7 mOhm-cm^2, and the Figure-of-merit V_{B2}/R_{on} is 125MW/cm^2, the highest value ever reported for a power MOSFET in any material system and 25x higher than the theoretical limit for silicon power MOSFETs.

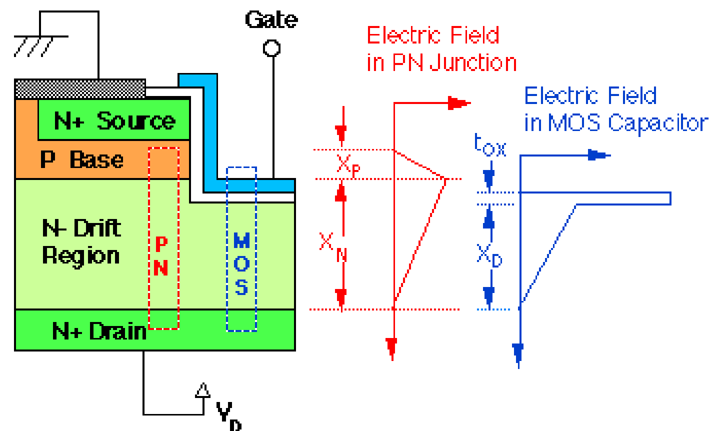


Figure-1.11: Cross section of a UMOS power transistor in silicon carbide. The electric field is illustrated on the right side for two regions within the device, the pn junction region and the MOS capacitor region. The field in the oxide at the base of the trench is 2.5 times higher than the peak field in the semiconductor because of the discontinuity in dielectric constants at the interface [14].

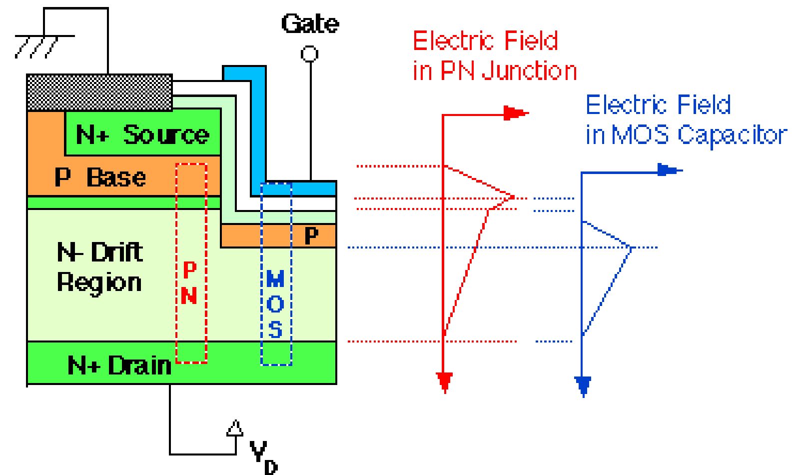


Figure-1.12: Cross section of the recently-introduced IOP-UMOS power transistor. The electric field is illustrated on the right side for two regions within the device. The P-type region under the trench reduces the field in the oxide at the base of the trench to zero [14].

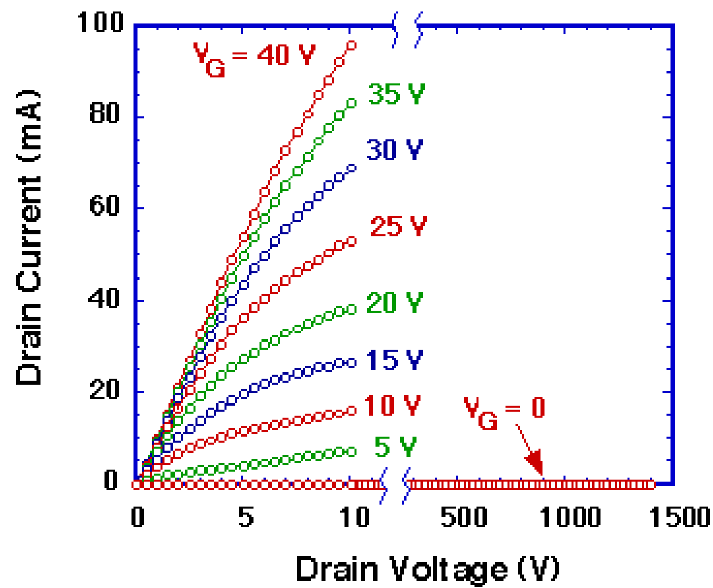


Figure-1.13: I-V characteristics of the IOP-UMOS ACCUFET in 4H-SiC at room temperature. The gate width is 3.168 mm, gate length is 1.2µm, oxide thickness is 130 nm, and the active area is 1.728x10-4 cm2. The V_G=0 curve is swept to 1400V four times, but the data points overlay one another [14].

1.4.2 SILICON CARBIDE LATERAL POWER MOSFETs

Power switching devices in SiC, both MOSFETs and thyristors, were fabricated as vertical structures, with the substrate serving as the anode terminal. In the off state, voltage is blocked by a reverse-biased pn junction. To achieve high blocking voltage, one side of this junction, the "drift region", is thick (typically around 10 microns) and lightly doped ($5\text{-}10^{15}cm^{-3}$). Fig.1.14 below shows how the blocking voltage depends on the doping and thickness of the drift region. Note that for a given thickness, there is a maximum possible blocking voltage, regardless of doping. Up until very recently, commercially available SiC epilayers were limited to about 10 microns in thickness, and the maximum possible blocking voltage for this thickness is about 1600V.

One way to avoid this limitation is to build a lateral device. The basic structure of our lateral DMOSFET is shown in Fig.1.15. In the blocking state, the depletion layer spreads mainly into the lightly doped drift region. Once the depletion region reaches the insulating substrate, it continues spreading toward the drain, which is now located on the top surface. In this device, the maximum blocking voltage is not limited by the thickness of the epilayer.

Fig.1.16 shows the room temperature current-voltage characteristics of a lateral DMOSFET having a 10 micron gate length and a 35 micron gate-to-drain spacing. As seen, the blocking voltage of this device is about 2.6kV. This voltage is not limited by electrical breakdown in the device, but rather by arcing in the Flourinert solution in which the device is immersed during testing.

It is important to realize that by implementing the device laterally rather than vertically, we do not necessarily increase the surface area required for the device. If the device design incorporates the REduced-SURface-Field (RESURF) concept, the specific on-resistance (resistance-area product) can actually be lower than that of a comparable vertical device. The present device does not incorporate RESURF features.

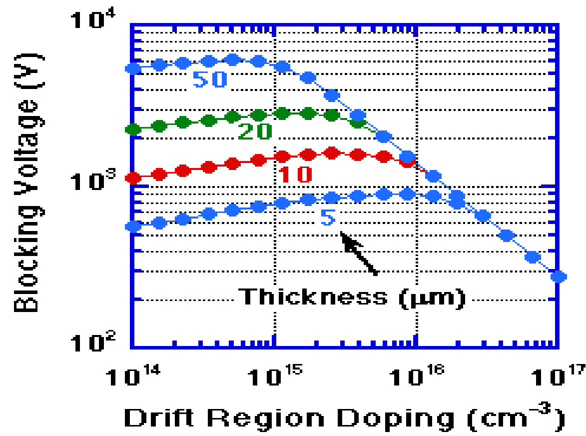


Figure-1.14: Blocking voltage as a function of drift region doping, with drift region thickness as a parameter [14].

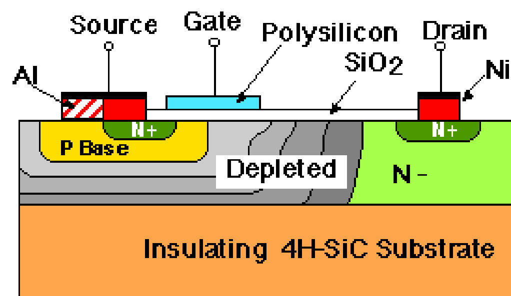


Figure-1.15: Cross section of lateral DMOSFET in the blocking state. The depletion region extends from p-base toward the drain, and blocking voltage is not limited by epi-layer [14].

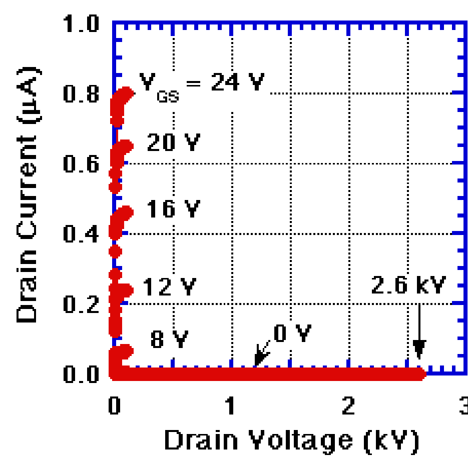


Figure-1.16: Current-voltage characteristics at room temperature. This device withstands a maximum drain voltage of 2.6kV in the blocking state. I-V curves are not measured in the "middle" of the plot because of the high power dissipation in this region [14].

1.4.3 SILICON CARBIDE SCHOTTKY BARRIER DIODES

Schottky barrier diodes (SBD's) are used as high-voltage rectifiers in many power switching applications. Whenever current is switched to an inductive load such as an electric motor, high-voltage transients are induced on the lines. To suppress these transients, diodes are placed across each switching transistor to clamp the voltage excursions. PN junction diodes could be used for this application, but they store minority carriers when forward biased, and extraction of these carriers allows a large transient reverse current during switching. Schottky Barrier Diodes are rectifying metal-semiconductor junctions, and their forward current consists of majority carriers injected from the semiconductor into the metal. Consequently, SBD's do not store minority carriers when forward biased, and the reverse current transient is negligible. This means the SBD can be turned off faster than a PN diode, and dissipates negligible power during switching.

SiC Schottky Barrier Diodes are especially attractive because the breakdown field of SiC is about 8x higher than in silicon. In addition, because of the wide bandgap, SiC SBD's should be capable of much higher temperature operation than silicon devices. They have fabricated SBD's on 4H-SiC using both Ni and Ti as Schottky metals. The cross section of the experimental device is shown in Fig.1.17

Forward and reverse I-V characteristics for the Ti and Ni SBD's are shown in Fig. 1.18. The barrier heights for Ti and Ni on 4H-SiC at room temperature are 0.8 and 1.3V, respectively. The lower barrier height Ti gives lower forward voltage drop but higher reverse leakage current as compared to the Ni barrier. The reverse blocking voltages are 1480 and 1720V, respectively. The blocking voltage of the Ni SBD is the highest yet reported for any SBD on SiC.

The recently fabricated Ni Schottky diodes on a 50μm epilayer of 4H-SiC. These diodes exhibited blocking voltages as high as 4.9kV, the highest yet reported for a SiC Schottky diode. Fig.1.19 shows forward and reverses current-voltage characteristics of a 425 μm diameter diode at room temperature.

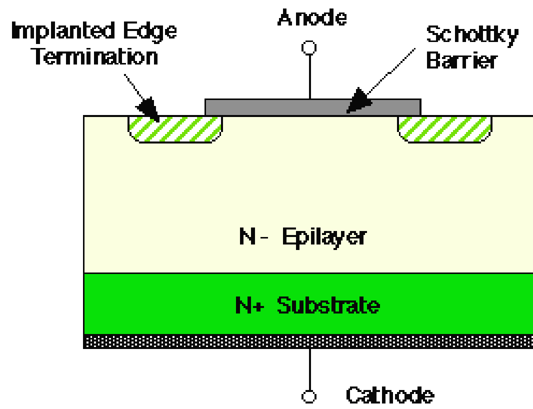


Figure-1.17: Cross section of an implant-edge-terminated Schottky barrier diode in SiC [14].

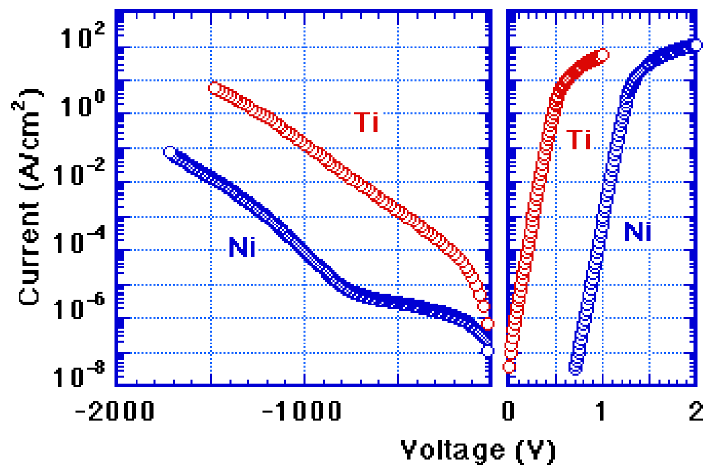


Figure-1.18: Forward and reverse current-voltage characteristics for Ti and Ni SBD [14].

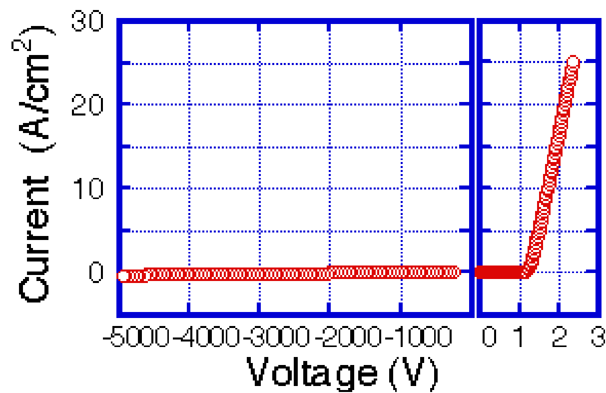


Figure-1.19: Forward and reverse current-voltage characteristics of a 425µm diameter Ni Schottky Barrier Diode on a 50µm 4H-SiC epi-layer at room temperature. Blocking voltage is 4.9kV and specific on-resistance is 43 mOhm-cm^2 [14].

1.4.4 SILICON CARBIDE CMOS INTEGRATED CIRCUITS

CMOS technology is attractive for digital logic because it offers low power consumption, full rail-to-rail output swing, and greater noise margins than NMOS circuits. CMOS also provides active current sources for linear applications. Development of CMOS technology in SiC is expected to provide low power, high temperature circuits as well as reliable control circuitry for smart power ICs.

Cree Research was the first to report CMOS ICs in 6H-SiC. Their process utilized an implanted n-well and deposited oxides, but due to other processing problems the PMOSFETs exhibited a very high threshold voltage. In this work, we use implanted p-wells and thermally grown oxides. The resulting PMOS threshold voltage is approximately -4.5V, allowing circuit operation with a 5V power supply.

Fig.1.20 shows a cross section of a completed CMOS inverter in the implanted p-well process. The fabrication sequence is as follows: First, p-wells are formed on n-type epilayers doped at 8x1015 cm-3 by boron implantation. Al and N are then implanted through polysilicon masks to form P^+ and N^+ source/drain regions, respectively. NMOSFETs are formed on p-wells while the PMOSFETs are formed on n-type epilayers. Implants are annealed at 1600°C for 40 minutes in argon, followed by an 1150°C, 2 hour wet oxidation to form a 40 nm gate oxide layer. Polysilicon is then deposited and patterned to form the gates. Al-Ni is used for p-type ohmic contacts and Ni for n-type contacts. A silicon oxynitride layer is deposited as an inter-metallic dielectric. Finally, vias are opened and interconnect metal is deposited and patterned.

The CMOS test chip, shown in Fig.1.21, contains a variety of digital circuits including inverters, NAND gates, NOR gates, XOR gates, half adders, flip-flops, and two 11-stage ring oscillators. All circuits operate properly from room temperature to 300°C on a single power supply at any voltage between 5-15V.

Fig.1.22 shows p-channel and n-channel MOSFET I-V characteristics at 300°C. Threshold voltages are 3.4V and 1.4V, respectively.

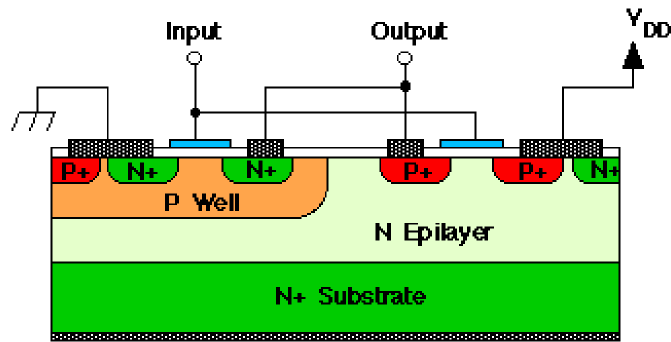


Figure-1.20: Cross section of a CMOS inverter in the implanted p-well process. The p-well, P^+ source regions, and N^+ source regions are all formed by ion implantation. Both transistors have a polysilicon gate over a thermally grown oxide [14].

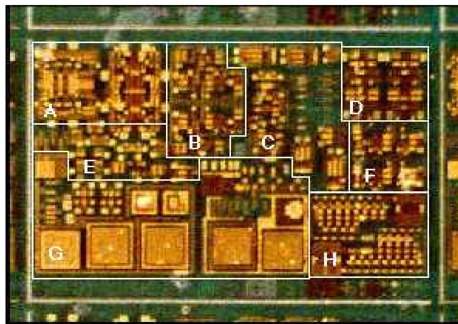


Figure-1.21: Photo of the CMOS test chip. Different regions are identified by letter, as follows: (A) differential amplifiers, (B) half adders, (C) inverters and flip-flops, (D) flip-flops, (E) NANDs, NORs, inverters, (F) XORs, (G) MOS capacitors, MOS gated diodes, TLM testers, MOSFETs, (H) ring oscillators [14].

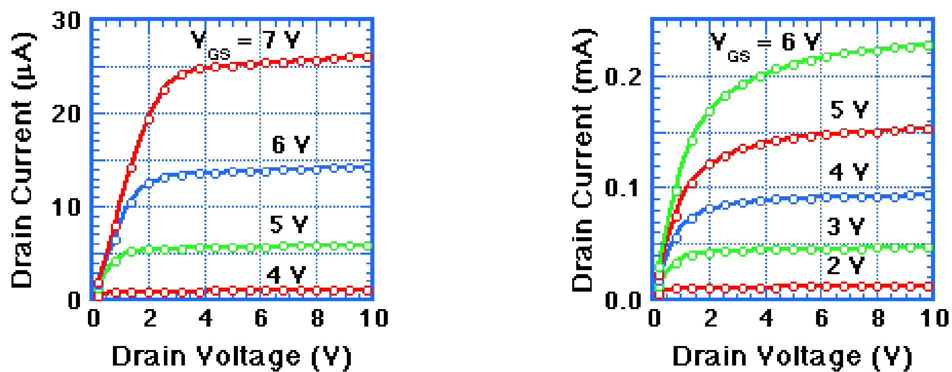
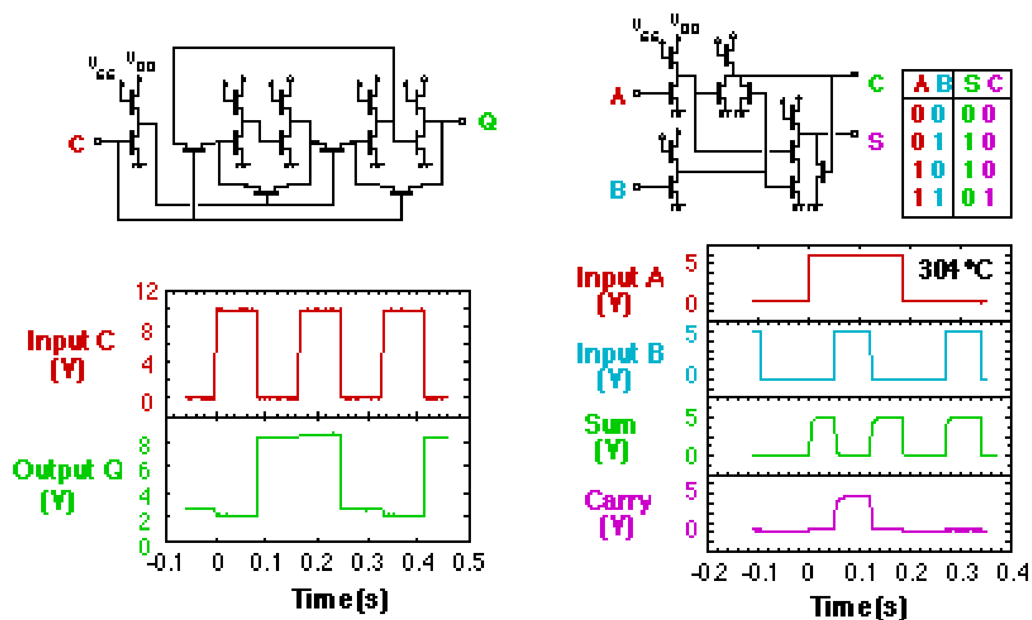


Figure-1.22: Current-voltage characteristic of a 40µm by 5µm p-channel MOSFET (left) and a similar n-channel MOSFET (right), both at 300°C [14].

1.4.5 SILICON CARBIDE NMOS INTEGRATED CIRCUITS

The circuit technology is enhancement-load NMOS, with the load transistor operated in the non-saturating mode with a separate V_{GG} supply [1]. MOS transistors are formed in p-type epilayers of 6H-SiC by wet thermal oxidation at 1150°C, followed by a 30 minutes in-situ Ar anneal. Source and drain regions are formed by ion implantation of nitrogen and are activated by a high temperature Ar anneal. N-type ohmic contacts are formed by annealed nickel. The gate and interconnect metal is Al. These circuits included inverters, NAND and NOR gates, XNOR gates, RS flip flops, binary counters, and half adders. All circuits operated properly from room temperature to above 300°C. The Fig.1.23 shows the binary counter and half adder circuits along with operating waveforms at room temperature and at 304°C.



A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Figure-1.23: Left Side: SiC NMOS binary counter circuit and operating waveforms at room temperature. This circuit is a master-slave D-type flip-flop with the Q-bar output fed back to the D input to form a binary counter. Note that the output waveform switches at half the frequency of the input waveform. **Right Side:** SiC NMOS half adder circuit, truth table, and operating waveforms at 304°C. As the A and B inputs change, note that the Sum and Carry outputs obey the binary rules in the truth table [14].

CHAPTER–2

6H-SILICON CARBIDE DIMOSFETs

Because of very high switching speeds, power MOSFETs have several advantages over power bipolar transistors for high-frequency applications where switching power losses are dominant. MOSFETs have a high input impedance which makes the gate drive circuitry very simple. Additionally, compared with power bipolar transistors they show an excellent safe operating area and better output characteristics for paralleling. These characteristics of power MOSFETs are useful for many high-frequency applications such as inverters and switch-mode power supplies. However, these advantages are offset by the high specific on-resistance ($R_{on,sp}$) associated with Si power MOSFETs for high breakdown voltages. Consequently, the use of Si power MOSFETs has been limited to breakdown voltages below 1000 V. This evaluation is in terms of the reduction in the on-resistance and consequent improvement in current-handling capability of SiC power MOSFETs at higher breakdown voltages.

The improvement in the current-handling capability of the SiC MOSFETs over the Si MOSFETs is quite significant at higher breakdown voltages where it could show approximately a twenty-fold improvement in specific on-resistance $R_{on,sp}$ for the same junction temperature and device packaging. This would allow a considerable increase in the power rating or a decrease in the chip size, for the SiC as compared with Si devices.

For this analysis we have considered two polytypes of SiC, 6H- and 3C-SiC, which are likely to be the materials of choice for SiC power device fabrication. Advantages of 6H-SiC, also known as α-SiC, are its large bandgap (2.86 eV) which results in high breakdown field strength E_c and commercial availability of 6H-SiC substrates and epilayers. Compared to 6H-SiC, 3C-SiC, or β-SiC, has a smaller bandgap (2.2 eV) and lower E_c but has higher electron mobility [19].

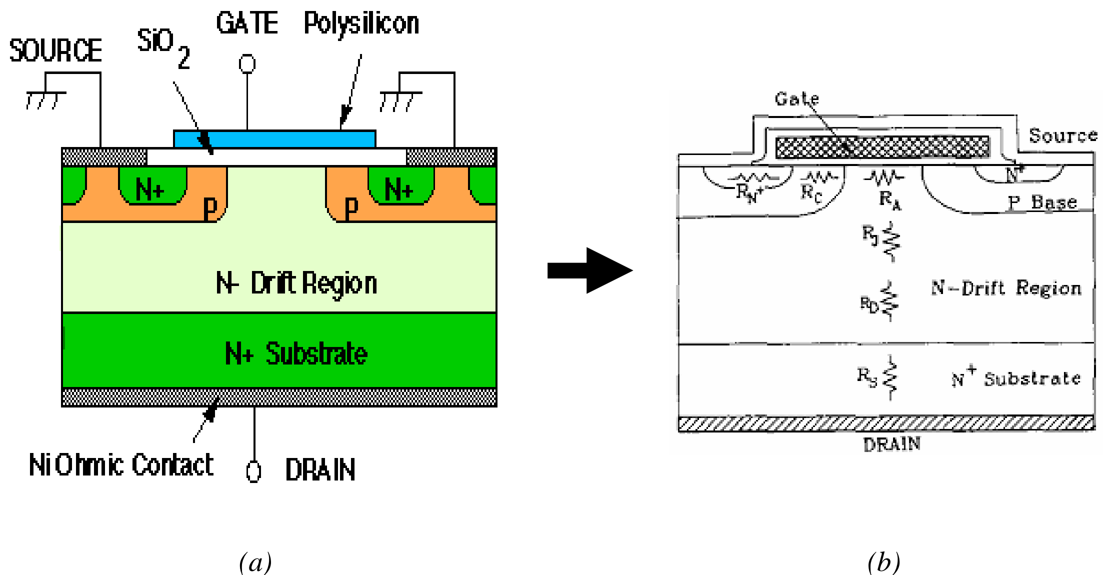
α-SiC ➡ $E_g \uparrow$ $E_c \uparrow$ $\mu_n \downarrow$ (where, ↓ indicates decreasing).

β-SiC ➡ $E_g \downarrow$ $E_c \downarrow$ $\mu_n \uparrow$ (where, ↑ indicates increasing).

2.1 STRUCTURE OF 6H-SiC DIMOS

Fig.2.1 shows a cross section of a power DIMOS structure. The DIMOS structure is fabricated by using planar diffusion technology with a refractory gate such as poly-silicon. In these devices, the P-base and N^+-source regions are diffused through a common window defined by the edge of the poly silicon gate. The surface channel region is defined by the difference in the lateral diffusion between the P-base and N^+-source region. The forward blocking capability is achieved by the PN-junction between the P-base region and the N-drift region.

During device operation, a fixed potential to the P-base region is established by connecting it to the source metal by a break in the N^+-source region. By short-circuiting the gate to the source and applying a positive bias to the drain, the P-base/N-drift region junction becomes reverse-biased and this junction supports the drain voltage by the extension of a depletion layer on both sides. However, due to the higher doping level of the P-base layer, the depletion layer extends primarily into the N-drift region. On applying a positive bias to the gate electrode, a conductive path extending between the N^+-source region and the N-drift region is formed.



(a) *(b)*

Figure-2.1: (a) and (b) Cross-section view of DIMOS showing various internal resistances associated within it [14], [19].

2.2 DEVICE THEORY AND ANALYSIS

To understand the flow of the current in the power DIMOS it is essential to analyze physics of the MOS device structure. It controls the characteristics of the channel region, which is responsible for output characteristics of the device. Physics of the power DIMOS have only majority carrier i.e. unipolar device.

2.2.1 FORWARD CONDUCTION CHARACTERISTICS

The current flow in the power DIMOS during forward conduction is achieved by the applying positive gate bias voltage for N-channel device to create the conductive path. This flow is limited by the total resistance between source and drain. This consists of several components as shown below in Fig.2.1(b). Where R_{N^+} is the contribution from the n+ -sources diffusion region, R_C is the channel resistance, R_A is the accumulation layer resistance, R_D is the drift region resistance and, R_S is the substrate resistance and the portion of the drift region that comes to the upper surface between cells contributes R_J that is enhanced at higher drain voltage due to pinch-off action of depletion layer extending from the P-base regions. This phenomenon is called JFET action.

2.2.1.1 MOS PHYSICS

When a P-type semiconductor region is assumed, then the analysis of current transport in the n-channel power MOS will be applicable. In this analysis, the oxide layer is assumed to be a perfect insulator that doesn't allow any charge carrier between gate and semiconductor. The energy-band diagrams for an ideal MOS structure is with a P-type semiconductor for different bias potential at metal is shown in Fig.2.2. The change in the inversion region plays a key role for determination of current transport in MOSFET devices. Here the ideal MOSFET has the following conditions:

a) the insulator has infinite resistivity,
b) charge can exist only in semiconductor and on the metal electrode,
c) there is no energy difference between the work function of the metal and the semiconductor.

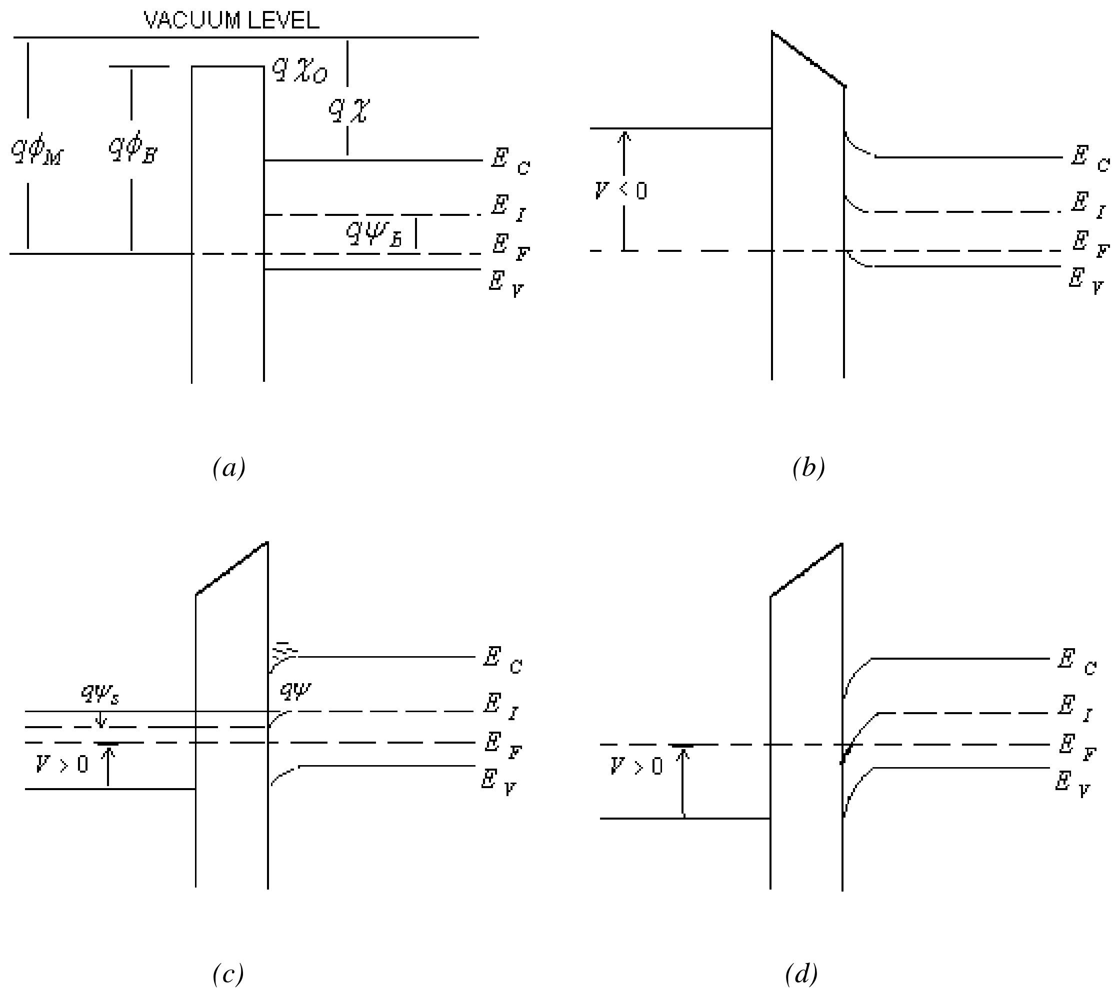


Figure-2.2: MOS structure with P-type semiconductor under different region (a) Flat-band energy band diagram (zero gate voltage), (b) accumulation (negative gate voltage), (c) depletion (positive gate voltage), (d) inversion (positive gate voltage).

2.2.1.2 ON RESISTANCE

The on resistance of a power MOSFET is the total resistance between the source and drain terminals during the on-state [20]. It is the important device parameter because it determines the maximum current rating. The cell structure with each component of the specific on-resistance ($R_{on,sp}$) is shown in the Fig.2.3. The application of a positive drain voltage results in a current flow between drain and source through the N-drift region and conductive channel. The conductivity of the channel is modulated by the gate

bias voltage and the current flow is determined by the resistance of various resistive components shown in Fig.2.3.

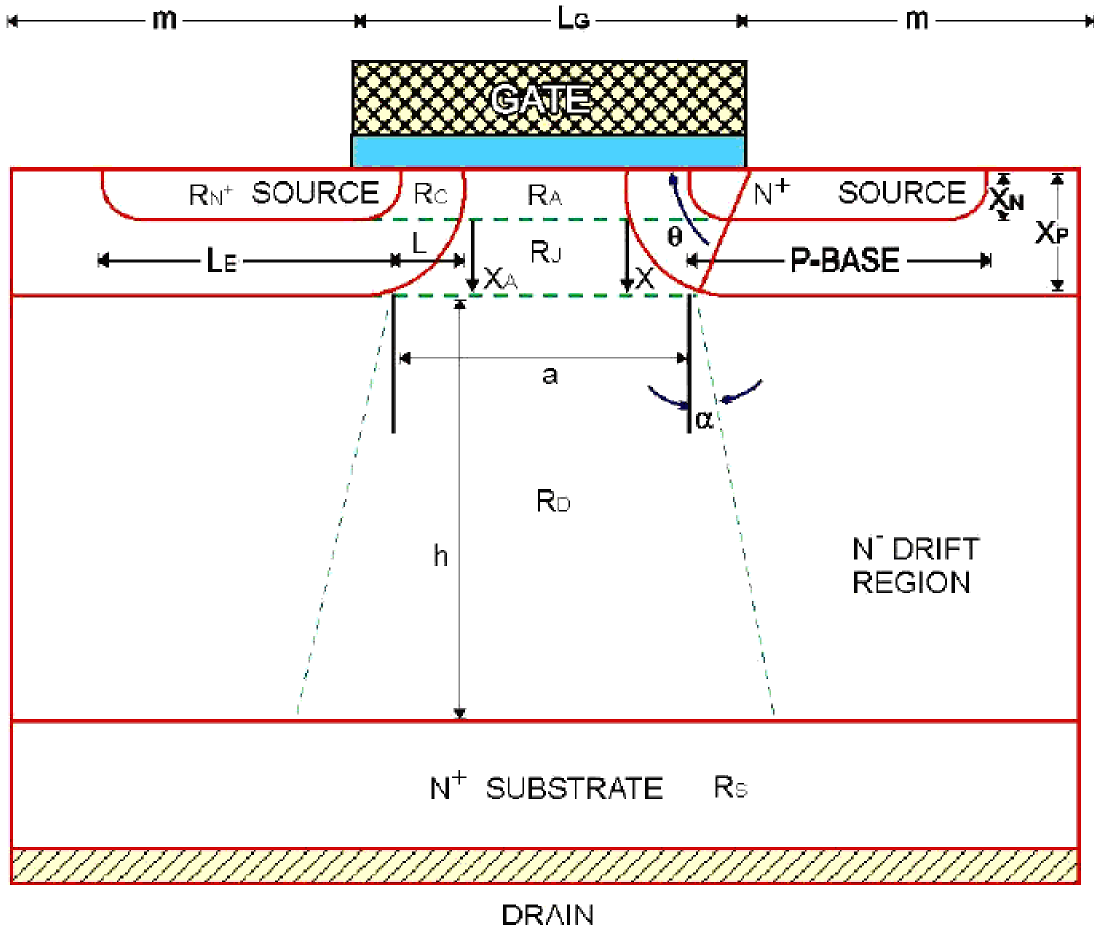


Figure-2.3: DIMOS cell structure with each components of the specific on-resistance.

The total specific on-resistance ($R_{on,sp}$) is determined as

$$R_{on,sp} = R_{N^+} + R_C + R_A + R_J + R_D + R_S \quad (2.1)$$

Where, R_{N^+} is the contribution from the n+ -sources diffusion region,

R_C is the channel resistance,

R_A is the accumulation layer resistance,

R_J is the resistance of the JFET pinch-off region,

R_D is the drift region resistance and,

R_S is the substrate resistance.

In a power DIMOS, blocking voltage is supported across the drift layer and thus, drift-region resistance is considered to be the minimum possible theoretical limit for the on-resistance of a DIMOS. For an ideal DIMOS, the resistances associated with the N^+-source, the n-channel, the JFET, the accumulation region, and the N^+-substrate are assumed to be negligible, and the specific on-resistance of the power DIMOS is determined by the drift region only. This assumption is not accurate at lower breakdown voltages where the drift-region resistance R_D is comparable to the other resistive components and these resistances should also be included in calculating $R_{on,sp}$. However, at higher breakdown voltages, R_D is significantly higher than other resistances and $R_{on,sp}$ could be approximated by R_D.

1) The **channel resistance** per square centimeter for linear cell structure having gate oxide thickness (Z = 1000 A^o) is given by

$$R_{ch,sp} = \frac{1}{2}\frac{L(L_G + 2m)}{\mu_{ns}C_{ox}(V_G - V_T)} \tag{2.2}$$

Where, L is typical channel length (2 μm),

L_G is the length of the gate electrode (20 μm),

m is the cell diffusion window,

V_G is the gate drive voltage (10V),

C_{ox} is the oxide capacitance, and

V_T is the threshold voltage.

Resulting channel resistance per square centimeter is $R_{ch,sp} = 2.5\times10^{-3}\Omega\cdot cm^2$, it can be reduced by decreasing the gate oxide thickness.

2) Now the **substrate resistance** per unit area for substrate thickness 20mils and resistivity of 0.01 Ω.cm is given by

$$R_{S,sp} = O.O1\Omega\cdot cm\times5\times10^{-2}cm = 5\times10^{-4}\Omega\cdot cm^2 \tag{2.3}$$

This can be reduced by using 0.001 Ω.cm arsenic-doped wafer and by lapping the substrate after device fabrication.

3) To calculate the **sources resistance**, if a linear cell is considered with 1-cm extension perpendicular to the cross section as shown above in Fig.2.3, the source resistance per square centimeter due to N^+-emitter region is given by [20];

$$R_{n^+,sp} = \frac{1}{2}\rho_{\square n^+} L_E \left(L_G + 2m\right) \tag{2.4}$$

Where, L_G is the length of the gate electrode (20 μm),

$\rho_{\square n^+}$ is the sheet resistance of the n^+ diffusion (10 $\Omega \cdot cm$),

2m is the cell diffusion window,

L_E is the emitter length (10 μm), and

(L_G +2m) is the cell repeat spacing (40 μm).

Resulting specific resistance per square centimeter is $R_{n^+,sp} = 2\times10^{-5}\Omega \cdot cm^2$, which is negligible as compare to all other resistances.

4) The **accumulation region resistance** determines the current flow from the channel in to the drift region. The accumulation region resistance per square centimeter is

$$R_{A,sp} = \frac{K(L_G - 2x_p)(L_G + 2m)}{\mu_{nA} C_{ox}(V_G - V_T)} \tag{2.5}$$

Where, K is the multiplying factor (3 nearly) [20],

C_{ox} oxide capacitance per unit area, and

V_T is the threshold voltage.

For x_p = 3 μm and L_G = 20 μm, the accumulation region resistance per unit square centimeter is found to be $6\times10^{-3}\Omega \cdot cm^2$.

5) Similarly **JFET region resistance** is given by the expression

$$R_{J,sp} = 2\rho_D \left(L_G + 2m\right)\left[\frac{1}{\sqrt{1-(2x_p/L_G)^2}}\tan^{-1}(0.414)\sqrt{\frac{L_G + 2x_p}{L_G - 2x_p}} - \frac{\pi}{8}\right] \tag{2.6}$$

Where, ρ_D is the resistivity of the drift region.

Resulting JFET region resistance per square centimeter, $R_{J,sp} = \rho_D \Omega.cm \times 1.334\times10^{-3} cm$

6) The **drift region resistance** per unit square centimeter is given by

$$R_{D,sp} = \rho_D \frac{(L_G + 2m)}{\tan(\alpha)} \ln\left[1 + 2\frac{h}{a}\tan(\alpha)\right] \tag{2.7}$$

Current spreading angle; $\alpha = 28^0 - \left(\frac{h}{a}\right)$ if h ≥ a (2.8)

$$\alpha = 28^0 - \left(\frac{a}{h}\right) \quad \text{if } h \le a \tag{2.9}$$

Where, h is the drift region thickness (≈ 'a') so the ratio (h/a) = 1, then

$$R_{D,sp} = \rho_D\, \Omega \cdot cm \times 0.551 \times 10^{-2} cm$$

Here the drift region resistance is largest as compare to any other resistances so only the drift region resistance would be considerable.

The specific on resistance ($R_{on,sp}$) components values are

$R_{C,sp} = 2.5 \times 10^{-3}\ \Omega.cm^2$	$= 0.250 \times 10^{-2}\ \Omega.cm^2$	Negligible
$R_{S,sp} = 5.0 \times 10^{-4}\ \Omega.cm^2$	$= 0.050 \times 10^{-2}\ \Omega.cm^2$	
$R_{N^+,sp} = 2.0 \times 10^{-5}\ \Omega.cm^2$	$= 0.002 \times 10^{-2}\ \Omega.cm^2$	
$R_{A,sp} = 6.0 \times 10^{-3}\ \Omega.cm^2$	$= 0.600 \times 10^{-2}\ \Omega.cm^2$	
$R_{J,sp} = \rho_D\ \Omega.cm \times 1.344 \times 10^{-3}\ cm$	$= \rho_D \times 0.134 \times 10^{-2}\ \Omega.cm^2$	
$R_{D,sp} = \rho_D\ \Omega.cm \times 0.551 \times 10^{-2}\ cm$	$= \rho_D \times 0.551 \times 10^{-2}\ \Omega.cm^2$	

So $R_{on,sp} \approx R_{D,sp}$

Where ρ_D is the resistivity of the drift region. Consider the ideal case where the resistance of the N^+-emitter, the N^+-substrate, the channel, the accumulation region, and the JFET region are negligible. The specific on-resistance $R_{on,sp}$ of the power DIMOS determined by drift region is identical to that derived for the ideal JFET [21]:

$$R_{on,sp} = 5.93 \times 10^{-9} (V_B)^{2.5} \quad (\Omega.cm^2) \tag{2.10}$$

for n-channel device.

$$R_{on,sp} = 1.63 \times 10^{-9} (V_B)^{2.5} \quad (\Omega.cm^2) \tag{2.11}$$

for p-channel device.

2.3 BASIC DEVICE EQUATIONS

The dependency of doping concentration, breakdown electric field, and specific on-resistance on blocking voltage and then thermal consideration for power consumption in the devices.

2.3.1 BLOCKING VOLTAGE

Consider the depletion region between the P-base and N-drift region as a one dimensional abrupt P-N junction. It can be shown that the doping level $N_d\,(cm^{-3})$ that can support a given breakdown voltage V_B (volt) and the depletion width W (cm) at breakdown can be given as [21].

$$N_d = \varepsilon \cdot E_C^2 /(2 \cdot q \cdot V_B) \qquad (cm^{-3}) \qquad (2.12)$$

$$W = 2V_B / E_C \qquad (2.13)$$

The specific on-resistance, $R_{on,sp}\ (\Omega \cdot cm^2)$ of the drift layer to support V_B is [21]

$$R_{on,sp} = W /(q \cdot N_d \cdot \mu_n) \qquad (\Omega \cdot cm^2) \qquad (2.14)$$

$$= 4V_B^2 /(\varepsilon \cdot E_C^3 \cdot \mu_n) \qquad (2.15)$$

Where, ε is the permittivity (F/cm),

E_C is the critical field (V/ cm), and μ_n is electron mobility $\left(cm^2 / V \cdot \sec\right)$.

The equation connecting the breakdown electric field strength E_C on the doping level N_d for a P^+-N diode of 6H-SiC has been derived [22].

$$E_C^{6H-SiC} = 1.95 \times 10^4 N_d^{0.131} \qquad (V / cm) \qquad (2.16)$$

Eliminating E_C between equations (2.12) and (2.15) we have,

$$N_d = (1.02 \times 10^{15} / V_B)^{1.35} \qquad (cm^{-3}) \qquad (2.17)$$

Using mobility at room temperature for low doping level

$$R_{on,sp} = 5.93 \times 10^{-9} V_B^{2.5} \qquad (\Omega \cdot cm^2) \qquad (2.18)$$

$V_B \uparrow \ \rightarrow W \uparrow \ \rightarrow R_{on,sp} \uparrow$ (where, ↑ indicates increasing).

$\rightarrow N_d \downarrow$ (where, ↓ indicates decreasing).

2.3.2 THERMAL CONSIDERATION

For power semiconductor devices, we require high input impedance, high switching speed, low on-state resistance, and large avalanche breakdown voltage and high thermal stability to minimize the possibility of thermal runaway. It is important to estimate the high-temperature performance capability of the SiC devices as compared to the Si devices [23]. SiC devices are capable of operating at temperatures up to 600°C. It was shown that at high operating temperatures, a SiC device has considerably higher on-state conductance and smaller off-state leakage current than a Si device. This resulted in a decrease in the power dissipated in the active device area and, thus the SiC devices showed better performance even at very-high junction temperature.

The junction temperature T_j depends on the packaging technology but does not depend on the semiconducting material. Since Si devices are limited in their operation up to 200 °C, so comparison of the on-state current density J_{on} and the chip size of SiC MOSFETs with Si MOSFETs at the same maximum junction temperature T_j of ~200°C. The temperature rise in the active area of the device due to heat ΔT is [19];

$$\Delta T = \theta_{th} \cdot P_D \tag{2.19}$$

Where, θ_{th} (K/W) is the thermal resistance, and P_D (W) is the total ohmic power. P_D is consisting of sum of ohmic power dissipated during the on-state P_{on} and off-state P_{off}. For a 50% duty cycle, P_D for a DIMOS is given as [19]:

$$P_D = \frac{1}{2}(J_{on}^2 \cdot A \cdot R_{on,sp} + J_L \cdot A \cdot V_B) \tag{2.20}$$

and $$\Delta T = \frac{A \cdot \theta_{th}}{2}(J_{on}^2 \cdot R_{on,sp} + J_L \cdot V_B) \tag{2.21}$$

Where, A is the area of the active device (cm^2),

J_{on} is the on-state current density (A/cm^2),

$R_{on,sp}$ is the specific on-resistance of the drift region $(\Omega \cdot cm^2)$,

J_L is the leakage current density in reverse blocking mode (A/cm^2), and

V_B is the reverse blocking voltage (volt).

The thermal resistance θ_{th} consists of two components- θ_{jc} which is the junction-to-case thermal resistance & θ_{ca} the case-to-ambient thermal resistance. θ_{jc} is relatively insensitive to the ambient environment and is mainly a function of chip material and geometry [19];

$$\theta_{jc} = \frac{d}{\lambda \cdot A} \tag{2.22}$$

Where, d (cm) is the substrate thickness,

A (cm^2) is the junction area, and

$\lambda (W / K \cdot cm)$ is the thermal conductivity.

For Si and SiC λ at 200°C is 0.8 and 2.8 W/K. θ_{jc} is quite small and θ_{ca} is the dominant component. θ_{jc} depends on the package geometry and its orientation in the specific application. A typical value of θ_{th} in the state-of-the-art packaging technology is 1 K/W. Thus the same thermal resistance can be assumed for Si and SiC devices.

The reverse leakage current density J_L has two components, due to the diffusion current J_D and due to the space-charge generation current J_G [24].

$$J_L = J_G + J_D \tag{2.23}$$

$$J_G = \frac{q \cdot n_i \cdot W}{\tau_e} \tag{2.24}$$

$$J_D = q \cdot \left(\frac{D_h}{\tau_h} \right)^{1/2} \cdot \frac{n_i^2}{N_d} \tag{2.25}$$

Where, n_i is the intrinsic carrier concentration (cm^{-3}),

W is the width of the space-charge region (cm),

τ_e is the lifetime of electrons (sec),

τ_h is the lifetime of holes (sec),

N_d is the concentration of donor atoms (cm^{-3}), and

D_h is the diffusion constant of holes in the N-type region ($cm^2 / \sec$).

Due to the large band-gap of SiC, the intrinsic carrier concentration n_i in SiC is very small and consequentially, even at high operating temperatures, SiC has much smaller reverse-leakage current than Si. So amount of power dissipated in the off-state P_{off} is negligible as compared to the on-state power dissipation P_{on}. In our calculations we have set J_{on}=(I_{DS}/ A) to calculate maximum power dissipation as I_{DS} for a MOSFET is the maximum value corresponding to current J_{on} for given gate bias. Again $J_L << J_{on}$ and the second term P_{off} in equation (2.20) can be neglected .The power dissipation is then [19]:

$$P_D = \frac{1}{2}(I_{DS}^2 \cdot R_{on,sp} / A) \qquad \text{(Watt)} \qquad (2.26)$$

Here I_{DS} given by

$$I_{DS} = (Z/L)\,\mu_n \cdot C_{OX}\,(V_G - V_T)\,V_D \qquad (2.27)$$

Where, we have evaluated I_{DS} for V_G = 40V,

The threshold voltage V_T has been set equal to 1.0 volt,

Z and L are the device dimensions shown in Fig.2.3 and

C_{OX} is the oxide capacitance.

CHAPTER–3

STRUCTURE OF DIMOSFET

As in the previous chapter specific on-resistance ($R_{on,sp}$) of the device is an important parameter to reduce the power generated by the device. And drift region resistance R_D is the main part of the specific on-resistance ($R_{on,sp}$). Now the doping level of the drift region determines the R_D. So the uniform and graded profile model effect the doping profile and its corresponding equations are explained in this chapter.

3.1 MODEL FOR DIMOSFET

The Double Implanted Metal-Oxide Semiconductor (DIMOS) field effect transistor has been frequently used in high voltage power electronics applications. The performance of the device is limited by the quasi-saturation behavior in its characteristics. It is shown that such effect is due to the carrier velocity saturation because of the high electric field, low impurity concentration in drift layer, and narrow p-body spacing. The detail of DIMOS structure identifying different regions of operation is shown in Fig.3.1. Since the diffusion process in 6H-SiC is ineffective, ion implantation is the only way to form p-body and n^+ region for the vertical structure and double diffusion is not suitable for the 6H-SiC device fabrications. The n-drift region is usually doped lightly ($\approx 5\times10^{14}$ /cc) to reduce the losses in the drift region. The n^+ regions were doped with ($\approx 1.5\times10^{20}$ /cc) Nitrogen; p-body regions were formed with ($\approx 4\times10^{17}$ /cc) Boron implantations [25]. Here,

h	drift-region height of the device (cm, depends on V_b and doping profile),
W	width of the device (cm),
$\mathbf{W_j}$	height of the p-body (cm),
$\mathbf{W_t}$	total vertical height (cm),
$\mathbf{W_d}$	depletion width (cm),
L	channel length formed under the gate and inside the p-body (cm),
$\mathbf{L_p}$	length of p-body (cm),
$\mathbf{L_{diff}}$	separation of p-bodies (cm),

Z	total length of the device (cm),
$\mathbf{t_{ox}}$	oxide thickness (cm),
$\mathbf{V_T}$	threshold voltage of the device (volt),
$\mathbf{V_{GS}}$	applied gate to source voltage (volt),
$\mathbf{v_{sat}}$	saturation velocity (cm/sec),
q	electronic charge (C),
$\boldsymbol{\alpha}$	angle of slope of the drift region narrowing (degree),
$\boldsymbol{\varepsilon_o}$	permittivity constant in free space (F/cm),
$\boldsymbol{\varepsilon_{ox}}$	oxide permittivity (F/cm).
$\boldsymbol{\varepsilon_{sic}}$	silicon carbide permittivity (F/cm),
A	cross-sectional area of the device (cm^2), and
$\mathbf{C_{ox}}$	oxide capacitance (F).

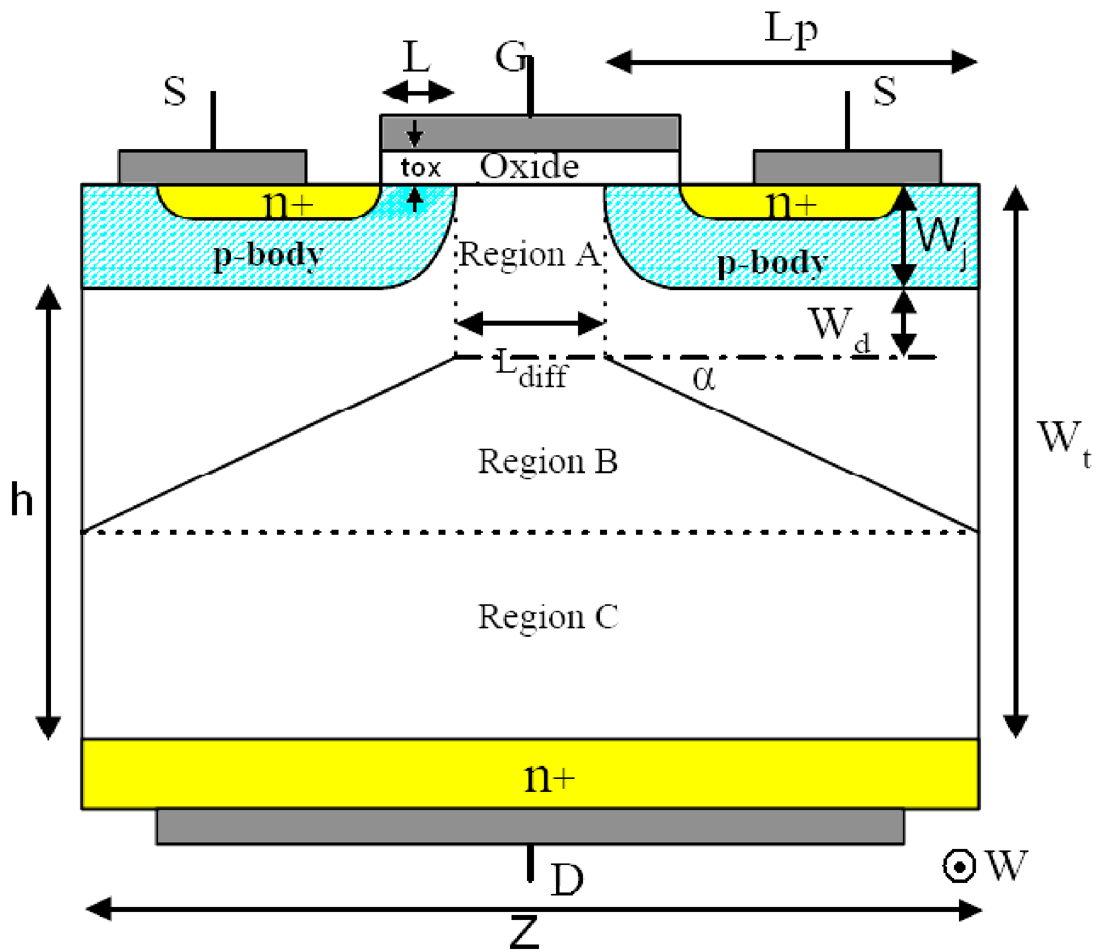


Figure-3.1: Structure of Double Implanted Metal-Oxide Semiconductor (DIMOS) [25].

3.2 MOBILITY WITH DOPING CONCENTRATION FOR 6H-SiC

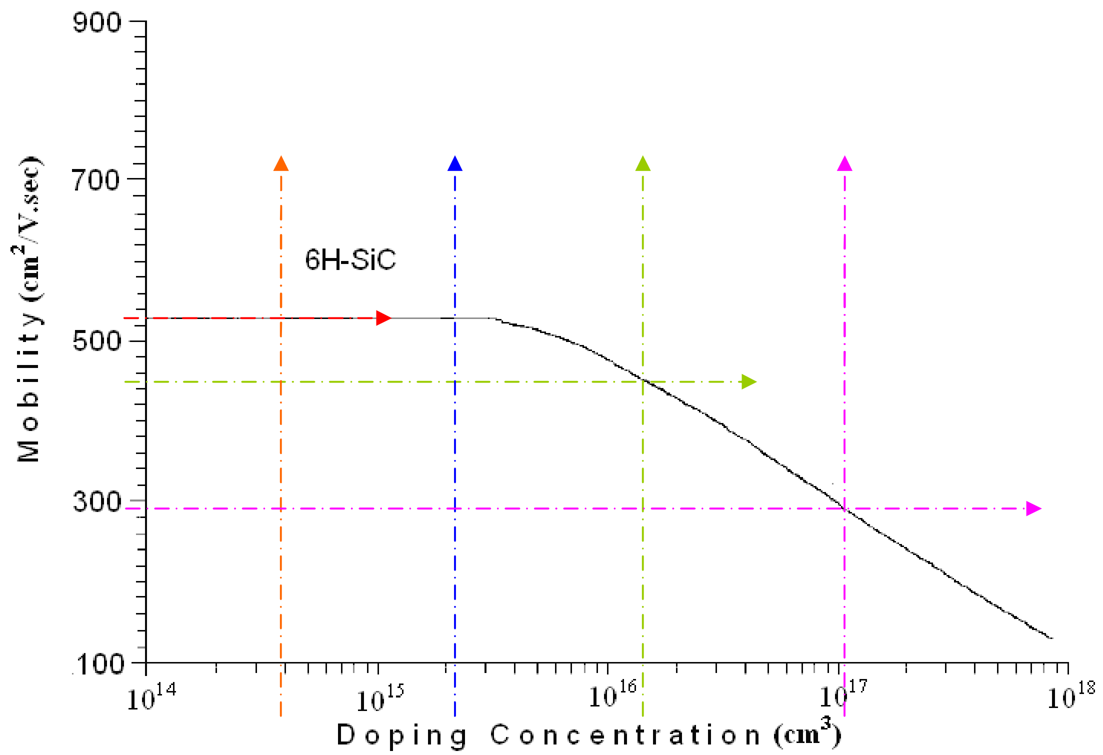


Figure-3.2: Electron mobilities of mono-crystalline bulk 6H-SiC [19].

Table-3.1: Electron Mobility of 6H-SiC for different Doping Concentration.

Concentration N_d (cm^{-3})	Mobility μ_{neff} ($cm^2/V.sec$)
3.91e14	**530**
2.15e15	**530**
1.45e16	**450**
1.09e17	**290**

CHAPTER–4

UNIFORM DOPING PROFILE IN DIMOSFET

Calculations for 8 kV uniformly doped drift region Double Implanted Metal-Oxide Semiconductor (DIMOSFET) using the basic equations and its related graphs are shown in this chapter:

4.1 BASIC EQUATIONS USED IN UNIFORMLY DOPED PROFILE

$$A = Z \cdot W \tag{4.1}$$

$$W_t = h + W_j \tag{4.2}$$

$$\varepsilon_{ox} = 3.97 \times \varepsilon_o \tag{4.3}$$

$$\varepsilon_{sic} = 9.70 \times \varepsilon_o \tag{4.4}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{4.5}$$

$$E_c = 1.95 \times 10^4 N_d^{0.131} \tag{4.6}$$

Where, E_c is the critical electric field developed in the device (volt/cm).

N_d is the doping concentration in the drift region (/cc).

$$I_{ch} = I_d = \frac{W \mu_{neff}}{2L[1 + (\mu_{neff} / 2v_{sat} L)]} V_{ch} [2C_{ox}(V_{GS} - V_T) - (C_{ox} + C_{do})V_{ch}] \tag{4.7}$$

Where, I_{ch} is the channel current (A),

μ_{neff} is the effective electron mobility (cm^2/V.s),

V_{ch} is the channel voltage (volt).

The drift region has been divided into three parts: an accumulation region A, a drift region B with varying cross section area, and drift region C with constant cross section. Voltages of these regions are given by [25],

$$V_A = \frac{I_d (W_j + W_d)}{W(L_{diff} q N_d) \mu_{neff} - I_d / E_c} \tag{4.8}$$

$$V_B = \frac{I_d}{W q N_d \mu_{neff} \cot \alpha} \log \left[\frac{W q N_d \mu_{neff} (L_{diff} + L_p) - I_d / E_c}{W q N_d L_{diff} \mu_{neff} - I_d / E_c} \right] \tag{4.9}$$

$$V_C = \frac{I_d (W_t - W_j - W_d - L_p \tan\alpha)}{W(L_{diff} + L_p) q N_d \mu_{neff} - I_d / E_c} \tag{4.10}$$

Therefore the total drifts region voltage $V_{drift} = V_A + V_B + V_C$ and voltage across the drain to source $V_{ds} = V_{ch} + V_{drift}$.

$$W_d = \sqrt{\frac{2 \cdot \varepsilon_{sic} \cdot (V_b \mp V_{F/R})}{q \cdot N_d}} \tag{4.11}$$

Where, V_b is the breakdown voltage (volt),

$V_{F/R}$ is the applied forward and reverse voltage (volt).

$$R_{on,sp} = \frac{W_t - W_j - W_d - L_p \tan\alpha}{\mu q N_d} \tag{4.12}$$

$$J_f = \frac{I_d}{A} \tag{4.13}$$

Where, J_f is forward current density (A/cm^2).

$$V_f = J_f \cdot R_{on,sp} \tag{4.14}$$

Where, V_f is forward voltage drop (volt).

$$P_d = \frac{1}{2}(J_{on}^2 \cdot R_{on,sp} \cdot A) \tag{4.15}$$

Where, P_d is the power dissipation (watt).

4.2 CALCULATIONS FOR UNIFORMLY DOPED PROFILE

In calculating the current I_{ds}, channel voltage V_{ch}, accumulation region voltage V_A, drift region voltage V_B (with varying cross-sectional area), drift region voltage V_C (constant cross-sectional area), drain to source voltage V_{ds}, depletion width W_d, specific on-resistance $R_{on,sp}$, forward voltage drop V_f, and power dissipation P_d, by using the following parameters (shown in Fig.3.1) with the value quoted against each of them as:

V_b = 8 kV,

N_d = 3.91x10^{14} , 2.15x10^{15} , 1.45x10^{16} , 1.09x10^{17} /cc

μ_{neff} = 530 , 530 , 450 , 290 cm^2/V.sec from Table.(3.1)

h = H_u = 148.17x10^{-4} cm, from equation (4.11)

W = 300x10^{-4} cm,

W_j = 10x10^{-4} cm,

$W_t = H_u + W_j = 158.17x10^{-4}$ cm,

$L = 5x10^{-4}$ cm,

$L_p = 25x10^{-4}$ cm,

$L_{diff} = 30x10^{-4}$ cm,

$Z = 80x10^{-4}$ cm,

$t_{ox} = 0.1x10^{-4}$ cm,

$V_T = 1$ V,

$V_{GS} = 40$ V,

$V_{sat} = 2x10^7$ cm/sec,

$q = 1.6x10^{-19}$ C,

$\alpha = 25^o$, and

$E_o = 8.85x10^{-14}$ F/cm.

For calculation of the device parameters set the height and the current density as in the Table (4.1) to (4.5) for different doping, then calculate the channel voltage V_{ch} and V_A, V_B, V_C by neglecting C_{do} and W_d by using above equations. Now from equation (4.11) by replacing V_b with V_A and neglecting $V_{F/R}$ voltage, calculate the value of W_d and finally calculate the $R_{on,sp}$, V_f, and power dissipation P_d.

4.3 TABLES AND GRAPHS FOR UNIFORMLY DOPED PROFILE

The set of calculations were made on the basis of equations (4.1) to (4.15). The results are quoted in the Tables-(4.1) to (4.8). And the related plots are given in Fig.(4.1) to (4.3) respectively.

The details of Tables and Figures are as follows:

Table-4.1: Values of Height for different values of Doping Concentration.

Table-(4.2) to (4.5):Values of all parameters for different values of Doping.

Table-4.6: Values of Current Density at different levels of doping for different values of Forward Voltage.

Table-4.7: Values of Power Dissipation at different levels of doping for different values of Current Density.

Table-4.8: Values of Power Dissipation at different levels of current density for different values of Doping.

Figure-4.1: Plot of Current Density against Forward Voltage for different values of doping.
Figure-4.2: Plot of Power Dissipation against Current Density for different values of doping.
Figure-4.3: Plot of Power Dissipation against Doping for different values of current density.

Table-4.1: Values of Height for different values of Doping Concentration.

Doping Concentration N_d (/cc)	Required Height of the Device H_u (cm)
3.91e14	148.17e-4
2.15e15	063.19e-4
1.45e16	024.33e-4
1.09e17	008.87e-4

Table-4.2: Values of all parameters for N_d = 3.91e14 /cm^3 Doping level.

N_d = 3.91e14 /cm^3, and μ_{eff} = 530 cm^2/V.Sec										
J_f	I_d	V_{ch}	V_A	V_B	V_C	V_{ds}	W_d	$R_{on,sp}$	V_f	P
1	24e-5	0.005	0.080	0.030	0.599	0.714	4.70e-5	0.410	0.410	4.92e-5
10	24e-4	0.055	0.805	0.296	5.990	7.146	1.49e-4	0.407	4.072	4.88e-3
100	24e-3	0.563	8.084	2.973	60.05	71.67	4.71e-4	0.397	39.75	0.4770
1000	24e-2	7.235	84.71	30.79	615.8	738.6	1.52e-3	0.366	365.7	43.888

Table-4.3: Values of all parameters for N_d = 2.15e15 /cm^3 Doping level.

N_d = 2.15e15 /cm^3, and μ_{eff} = 530 cm^2/ V.Sec										
J_f	I_d	V_{ch}	V_A	V_B	V_C	V_{ds}	W_d	$R_{on,sp}$	V_f	P
1	24e-5	0.005	0.015	0.005	0.109	0.134	8.54e-6	0.0748	0.075	8.97e-6
10	24e-4	0.055	0.146	0.054	1.089	1.344	2.70e-5	0.0747	0.747	8.96e-4
100	24e-3	0.563	1.464	0.539	10.89	13.46	8.55e-5	0.0744	7.441	0.0892
1000	24e-2	7.235	14.73	5.416	109.3	136.7	2.71e-4	0.0733	73.38	8.8065

Table-4.4: Values of all parameters for N_d = 1.45e16 /cm^3 Doping level.

N_d = 1.45e16 /cm^3, and μ_{eff} = 450 cm^2/ V.Sec										
J_f	I_d	V_{ch}	V_A	V_B	V_C	V_{ds}	W_d	$R_{on,sp}$	V_f	P
1	24e-5	0.006	0.002	9.41e-4	0.019	0.029	1.37e-6	0.013	0.013	1.56e-6
10	24e-4	0.065	0.025	0.0094	0.190	0.290	4.35e-6	0.013	0.131	1.56e-4
100	24e-3	0.664	0.255	0.0941	1.902	2.916	1.37e-5	0.013	1.306	0.0157
1000	24e-2	8.743	2.556	0.9413	19.03	31.27	4.35e-5	0.013	13.03	1.5641

Table-4.5: Values of all parameters for N_d = 1.09e17 /cm^3 Doping level.

N_d = 1.09e17 /cm^3, and μ_{eff} = 290 cm^2/ V.Sec										
J_f	I_d	V_{ch}	V_A	V_B	V_C	V_{ds}	W_d	$R_{on,sp}$	V_f	P
1	24e-5	0.010	5.2e-4	1.9e-4	0.004	0.015	2.28e-7	0.002	0.003	3.23e-7
10	24e-4	0.100	5.2e-3	1.9e-3	0.039	0.147	7.20e-7	0.002	0.027	3.23e-5
100	24e-3	1.036	0.053	0.019	0.392	1.500	2.28e-6	0.002	0.270	3.23e-3
1000	24e-2	15.30	0.527	0.194	3.926	19.95	7.21e-6	0.002	2.698	0.3237

Table-4.6: Values of Current Density at different levels of doping for different values of Forward Voltage.

J_f (A/cm^2)	V_f (volt)			
	N_d = 3.91e14 /cm^3 μ_{eff} = 530 cm^2/V.sec	**N_d = 2.15e15 /cm^3 μ_{eff} = 530 cm^2/V.sec**	**N_d = 1.45e16 /cm^3 μ_{eff} = 450 cm^2/V.sec**	**N_d = 1.09e17 /cm^3 μ_{eff} = 290 cm^2/V.sec**
1	0.4103	0.0748	0.0131	2.70e-3
10	4.0724	0.7473	0.1307	0.0270
15	6.0934	1.1204	0.1961	0.0405
20	8.1075	1.4933	0.2614	0.0540
30	12.119	2.2386	0.3921	0.0810
50	20.084	3.7272	0.6533	0.1349
75	29.957	5.5852	0.9798	0.2024
100	39.751	7.4406	1.3063	0.2699
150	59.145	11.145	1.9590	0.4048
200	78.315	14.842	2.6115	0.5397
250	97.293	18.533	3.2638	0.6746
300	116.10	22.219	3.9159	0.8095
400	153.24	29.575	5.2198	1.0793
500	189.81	36.913	6.5232	1.3491
600	225.88	44.235	7.8262	1.6188
700	261.48	51.542	9.1287	1.8886
800	296.64	58.837	10.431	2.1583
900	331.39	66.118	11.733	2.4280
1000	365.73	73.388	13.034	2.6977

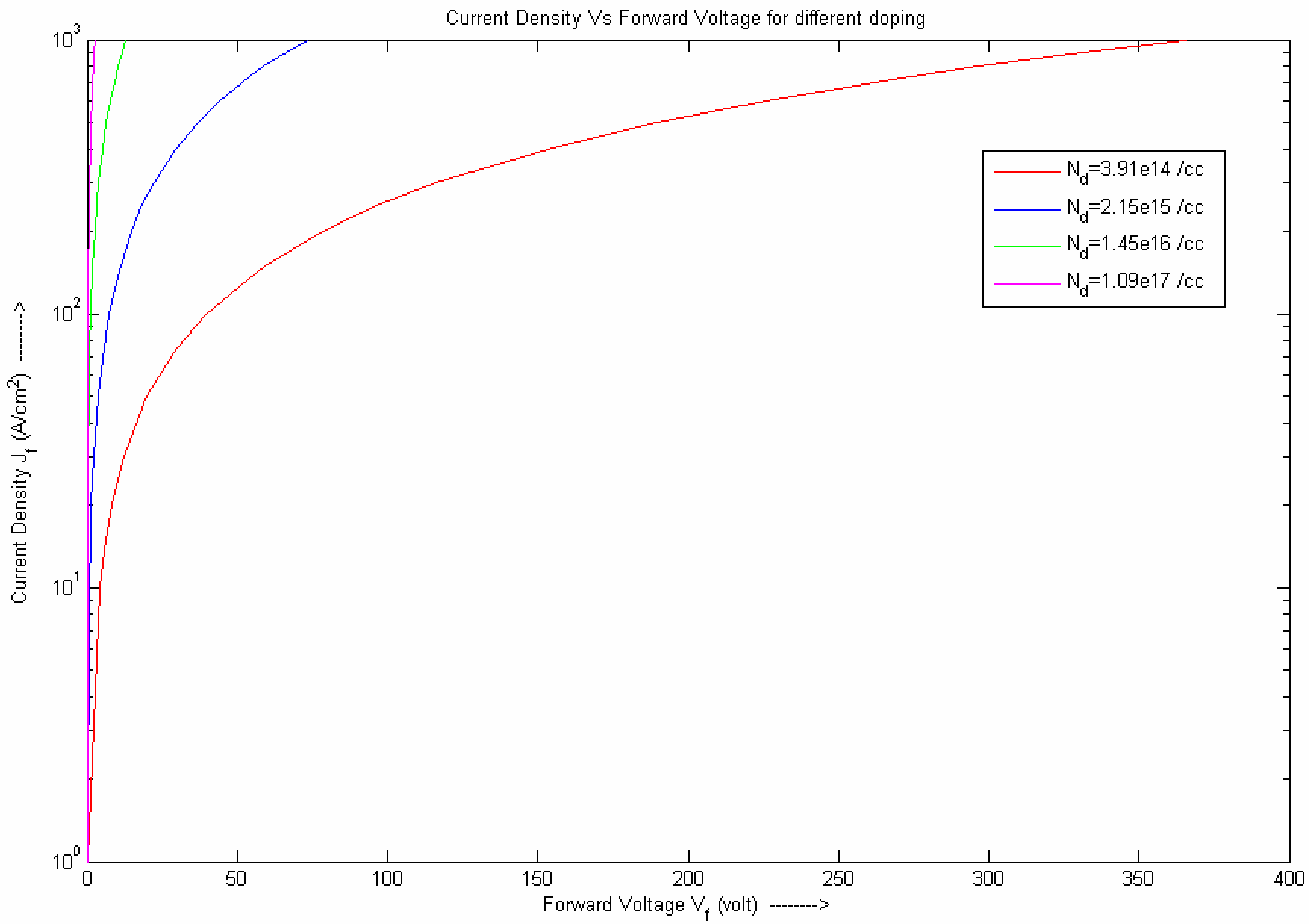


Figure-4.1: Plot of Current Density against Forward Voltage for different values of doping.

Table-4.7: Values of Power Dissipation at different levels of doping for different values of Current Density.

J_f (A/cm^2)	P (watt)			
	N_d = 3.91e14 /cm^3 μ_{eff} = 530 cm^2/V.sec	**N_d = 2.15e15 /cm^3 μ_{eff} = 530 cm^2/V.sec**	**N_d = 1.45e16 /cm^3 μ_{eff} = 450 cm^2/V.sec**	**N_d = 1.09e17 /cm^3 μ_{eff} = 290 cm^2/V.sec**
1	4.92e-5	8.97e-6	1.57e-6	3.24e-7
10	4.89e-3	8.97e-4	1.57e-4	3.24e-5
15	0.0110	2.02e-3	3.53e-4	7.29e-5
20	0.0195	3.58e-3	6.27e-4	1.30e-4
30	0.0436	8.06e-3	1.42e-3	2.91e-4
50	0.1205	0.0224	3.92e-3	8.10e-4
75	0.2696	0.0503	8.82e-3	1.82e-3
100	0.4770	0.0893	0.0157	3.24e-3
150	1.0646	0.2006	0.0353	7.29e-3
200	1.8796	0.3562	0.0627	0.0130
250	2.9188	0.5560	0.0979	0.0202
300	4.1795	0.7999	0.1410	0.0291
400	7.3553	1.4196	0.2506	0.0518
500	11.389	2.2148	0.3914	0.0809
600	16.264	3.1849	0.5635	0.1166
700	21.965	4.3296	0.7668	0.1586
800	28.478	5.6483	1.0014	0.2072
900	35.790	7.1408	1.2671	0.2622
1000	43.888	8.8065	1.5641	0.3237

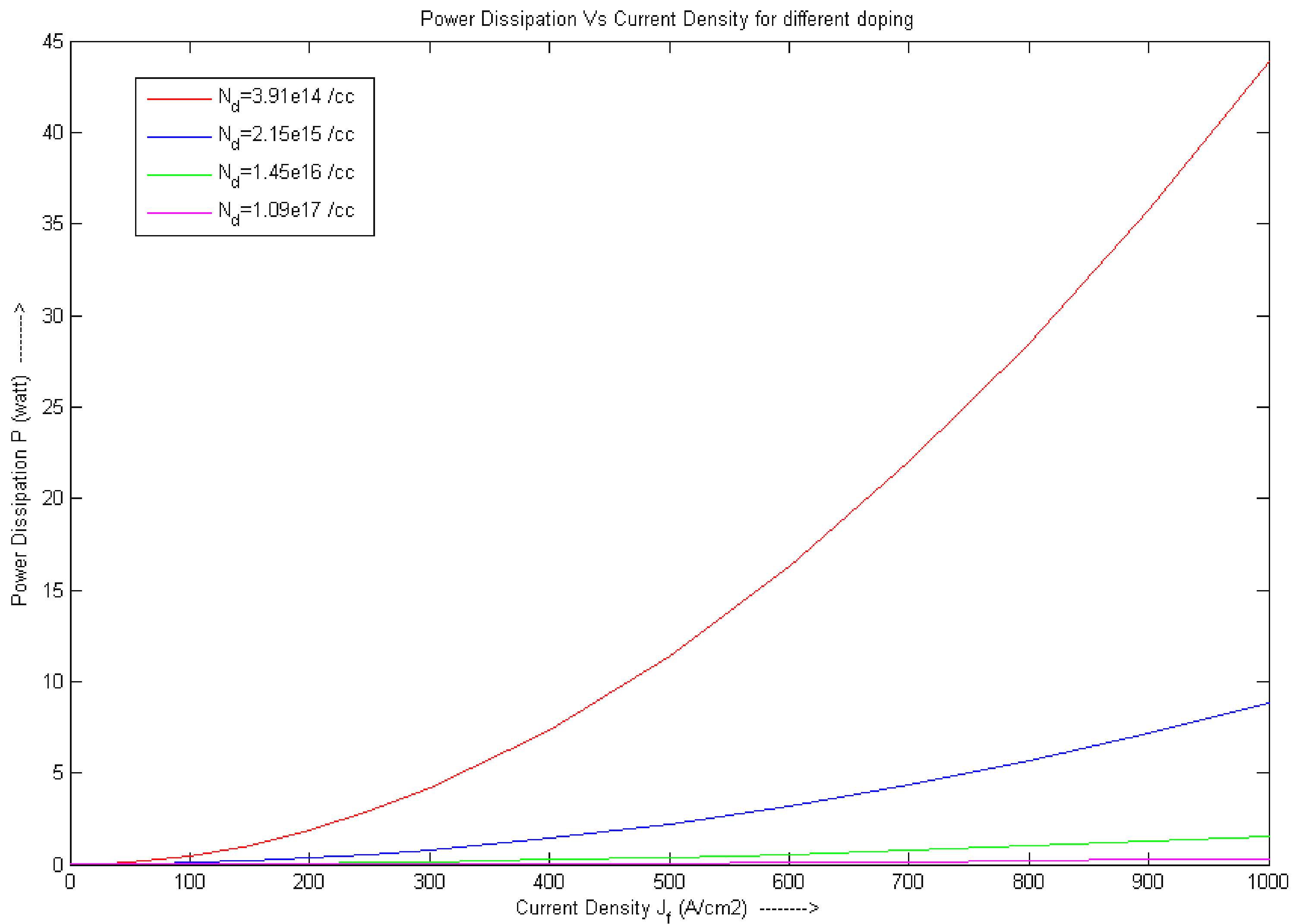


Figure-4.2: Plot of Power Dissipation against Current Density for different values of doping.

Table-4.8: Values of Power Dissipation at different levels of current density for different values of Doping.

N_d (/cc)	μ_{eff} (cm^2/V.Sec)	P (watt)			
		J_f=1 A/cm^2	J_f=10 A/cm^2	J_f=100 A/cm^2	J_f=1000 A/cm^2
3.91e14	530	4.92e-5	4.89e-3	0.4770	43.888
5.17e14	530	3.73e-5	3.71e-3	0.3639	34.231
8.00e14	530	2.41e-5	2.40e-3	0.2374	22.848
1.28e15	530	1.51e-6	1.50e-3	0.1493	14.587
2.15e15	530	8.98e-6	8.97e-4	0.0893	8.8065
3.00e15	530	6.44e-6	6.43e-4	0.0641	6.3477
5.00e15	515	3.98e-6	3.97e-4	0.0397	3.9417
7.00e15	500	2.92e-6	2.92e-4	0.0292	2.9069
9.00e15	480	2.37e-6	2.37e-4	0.0237	2.3582
1.20e16	465	1.83e-6	1.83e-4	0.0183	1.8279
1.45e16	450	1.57e-6	1.57e-4	0.0157	1.5641
1.09e17	290	3.24e-7	3.24e-5	3.24e-3	0.3237

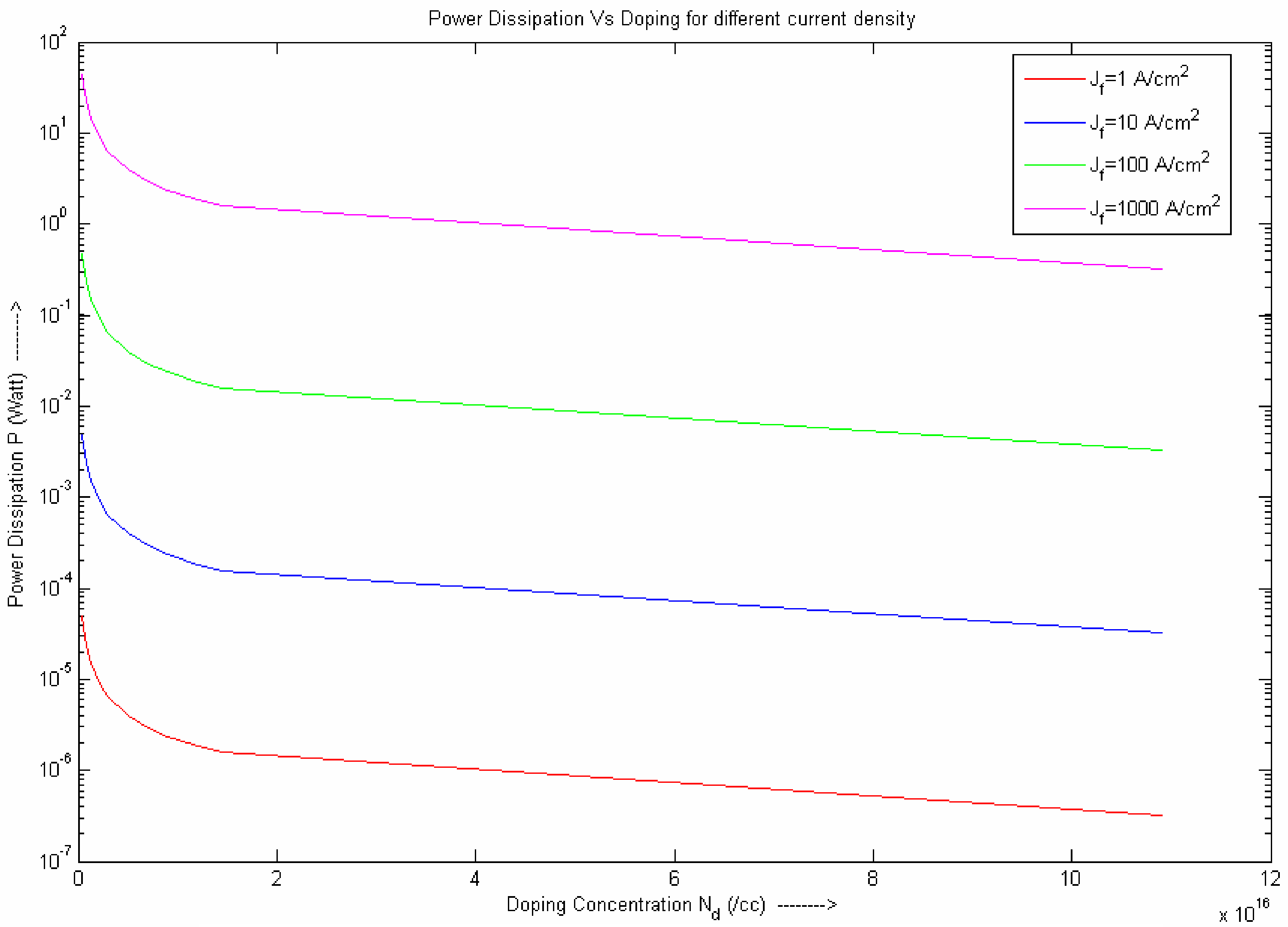


Figure-4.3: Plot of Power Dissipation against Doping for different values of current density.

CHAPTER–5

LINEARLY GRADED DOPING PROFILE IN DIMOSFET

Calculations for 8 kV linearly graded drift region DIMOS and its related graphs are shown in this chapter:

5.1 BASIC EQUATIONS USED IN LINEARLY GRADED PROFILE

All basic equations used in uniform profile from equations (4.1) to (4.10) and equations (4.12) to (4.15) are also valid for graded profile, except these equations [26]:

$$N_{eff} = \frac{N(x) - No}{\log\left(1 + \frac{N(x) - No}{No}\right)} \tag{5.1}$$

$$h = \sqrt{\frac{3 \cdot \varepsilon_{sic} \cdot \left(V_b \mp V_{F/R}\right)}{q \cdot \left(N(x) - No\right)}} \qquad [26] \tag{5.2}$$

$$G = \frac{N(x) - No}{h} \qquad \text{Where, G is the gradient of the profile} \tag{5.3}$$

$$W_d = \left(\frac{3 \cdot \varepsilon_{sic} \cdot \left(V_b \mp V_{F/R}\right)}{q \cdot G}\right)^{\frac{1}{3}} \tag{5.4}$$

5.2 CALCULATIONS FOR LINEARLY GRADED PROFILE

In calculating the current I_{ds}, $R_{on,sp}$ and power dissipation P_d. I have used the following different parameters used in the uniform doping profile and rests are same:

V_b = 8 kV,

N(x) = $1\text{x}10^{15}$, $1\text{x}10^{16}$, $1\text{x}10^{17}$, $1\text{x}10^{18}$ /cc,

N_{eff} = $3.91\text{x}10^{14}$, $2.15\text{x}10^{15}$, $1.45\text{x}10^{16}$, $1.09\text{x}10^{17}$ /cc, from equation (5.1)

μ_{neff} = 530 , 530 , 450 , 290 cm^2/V.sec,

h = H_g = $119.61\text{x}10^{-4}$ cm, from equation (5.2)

G = 7.52 $\text{x}10^{16}$, 2.75 $\text{x}10^{18}$, 8.80 $\text{x}10^{19}$, 2.79 $\text{x}10^{21}$ cm^{-4}, from equation (5.3)

W = $300\text{x}10^{-4}$ cm,

W_j = $10\text{x}10^{-4}$ cm, and

W_t = H_g + W_j = $158.17\text{x}10^{-4}$ cm.

For calculation of the device parameter firstly set the current density as in the Table (5.1) to (5.4) for different gradient G, then calculate the channel voltage V_{ch} and V_A, V_B, V_C by neglecting C_{do} and W_d by using above equations. Now from equation (5.4) by replacing V_b with V_A and neglecting $V_{F/R}$ voltage, calculate the value of W_d and finally calculate the $R_{on,sp}$, V_f, and power dissipation P_d in graded profile.

5.3 TABLES AND GRAPHS FOR LINEARLY GRADED PROFILE

The set of calculations were made on the basis of equations (4.1) to (4.10), equation (4.12) to (4.15) and equation (5.1) to (5.4). The results are quoted in the Tables-(5.1) to (5.8). And the related plots are given in Fig.(5.1) to (5.3) respectively.

The details are as follows:

Table-5.1: Values of Height for different values of Gradient.

Table-(5.2) to (5.5): Values of all parameter for different values of Gradient.

Table-5.6: Values of Current Density at different levels of gradient for different values of Forward Voltage.

Table-5.7: Values of Power Dissipation at different levels of gradient for different values of Current Density.

Table-5.8: Values of Power Dissipation at different levels of current density for different values of Gradient.

Figure-5.1: Plot of Current Density against Forward Voltage for different values of gradient.

Figure-5.2: Plot of Power Dissipation against Current Density for different values of gradient.

Figure-5.3: Plot of Power Dissipation against Gradient for different values of current density.

Table-5.1: Values of Height for different values of Gradient.

N(x)-No (/cc)	N (/cc)	H_g (cm)	G (cm^{-4})
1e15-1e14	3.91e14	119.61e-4	7.52e16
1e16-1e14	2.15e15	036.06e-4	2.75e18
1e17-1e14	1.45e16	011.35e-4	8.80e19
1e18-1e14	1.09e17	003.59e-4	2.79e21

Table-5.2: Values of all parameters for G = 7.52e-16 cm^{-4} Graded doping level.

N_{eff} = 3.91e14 /cm^3, μ_{eff} =530 cm^2/ V.Sec, and G = 7.52e-16 cm^{-4}										
J_f	I_d	V_{ch}	V_A	V_B	V_C	V_{ds}	W_d	$R_{on,sp}$	V_f	P
1	24e-5	0.005	0.080	0.030	0.473	0.589	2.58e-4	0.3177	0.318	3.81e-5
10	24e-4	0.055	0.805	0.296	4.737	5.893	5.56e-4	0.3088	3.088	3.71e-3
100	24e-3	0.563	8.084	2.973	47.49	59.11	1.20e-3	0.2893	28.93	0.3472
1000	24e-2	7.235	84.71	30.79	487.0	609.7	2.62e-3	0.2463	246.3	29.561

Table-5.3: Values of all parameters for G = 2.75e-18 cm^{-4} Graded doping level.

N_{eff} = 2.15e15 /cm^3, μ_{eff} = 530 cm^2/ V.Sec, and G = 2.75e-18 cm^{-4}										
J_f	I_d	V_{ch}	V_A	V_B	V_C	V_{ds}	W_d	$R_{on,sp}$	V_f	P
1	24e-5	0.005	0.015	0.005	0.086	0.111	4.41e-6	0.0589	0.059	7.07e-6
10	24e-4	0.055	0.146	0.054	0.861	1.117	9.50e-5	0.0587	0.587	7.04e-4
100	24e-3	0.563	1.464	0.539	8.615	11.18	2.05e-4	0.0581	5.809	0.0697
1000	24e-2	7.235	14.73	5.416	86.47	113.9	4.41e-4	0.0568	56.79	6.8144

Table-5.4: Values of all parameters for G = 8.80e-19 cm^{-4} Graded doping level.

N_{eff} = 1.45e16 /cm^3, μ_{eff} =450 cm^2/ V.Sec, and G = 8.80e-19 cm^{-4}										
J_f	I_d	V_{ch}	V_A	V_B	V_C	V_{ds}	W_d	$R_{on,sp}$	V_f	P
1	24e-5	0.006	2.5e-3	9.4e-4	0.015	0.025	7.76e-6	0.010	0.010	1.23e-6
10	24e-4	0.065	0.025	0.009	0.150	0.250	1.67e-5	0.010	0.103	1.23e-4
100	24e-3	0.664	0.255	0.094	1.504	2.517	3.60e-5	0.010	1.030	0.0123
1000	24e-2	8.743	2.556	0.941	15.04	27.29	7.76e-5	0.010	10.26	1.2319

Table-5.5: Values of all parameters for G = 2.79e-21 cm^{-4} Graded doping level.

N_{eff} = 1.09e17 /cm^3, μ_{eff} = 290 cm^2/ V.Sec, and G = 2.79e-21 cm^{-4}										
J_f	I_d	V_{ch}	V_A	V_B	V_C	V_{ds}	W_d	$R_{on,sp}$	V_f	P
1	24e-5	0.010	5.2e-4	1.9e-4	0.003	0.013	1.45e-6	0.002	0.002	2.56e-7
10	24e-4	0.100	5.2e-3	1.9e-3	0.031	0.139	3.12e-6	0.002	0.021	2.56e-5
100	24e-3	1.036	5.2e-2	0.019	0.310	1.418	6.72e-6	0.002	0.213	2.55e-3
1000	24e-2	15.30	0.527	0.194	3.105	19.12	1.45e-5	0.002	2.131	0.2557

Table-5.6: Values of Current Density at different levels of gradient for different values of Forward Voltage.

J_f (A/cm^2)	V_f (volt)			
	N_{eff} = 3.91e14 /cm^3 μ_{eff} = 530 cm^2/V.sec G = 7.52e16 cm^{-4}	N_{eff} = 2.15e15 /cm^3 μ_{eff} = 530 cm^2/V.sec G = 2.75e18 cm^{-4}	N_{eff} = 1.45e16 /cm^3 μ_{eff} = 450 cm^2/V.sec G = 8.80e19 cm^{-4}	N_{eff} = 1.09e17 /cm^3 μ_{eff} = 290 cm^2/V.sec G = 2.79e21 cm^{-4}
1	0.3178	0.0590	0.0103	2.13e-3
10	3.0880	0.5869	0.1032	0.0213
15	4.5956	0.8792	0.1548	0.0320
20	6.0887	1.1711	0.2064	0.0427
30	9.0412	1.7538	0.3095	0.0640
50	14.843	2.9160	0.5156	0.1067
75	21.952	4.3643	0.7732	0.1600
100	28.937	5.8088	1.0306	0.2133
150	42.615	8.6888	1.5451	0.3199
200	55.977	11.559	2.0594	0.4266
250	69.079	14.422	2.5734	0.5332
300	81.955	17.277	3.0871	0.6398
400	107.12	22.971	4.1142	0.8529
500	131.62	28.645	5.1406	1.0661
600	155.53	34.301	6.1665	1.2792
700	178.92	39.942	7.1920	1.4923
800	201.83	45.570	8.2170	1.7054
900	224.30	51.184	9.2416	1.9185
1000	246.35	56.787	10.266	2.1316

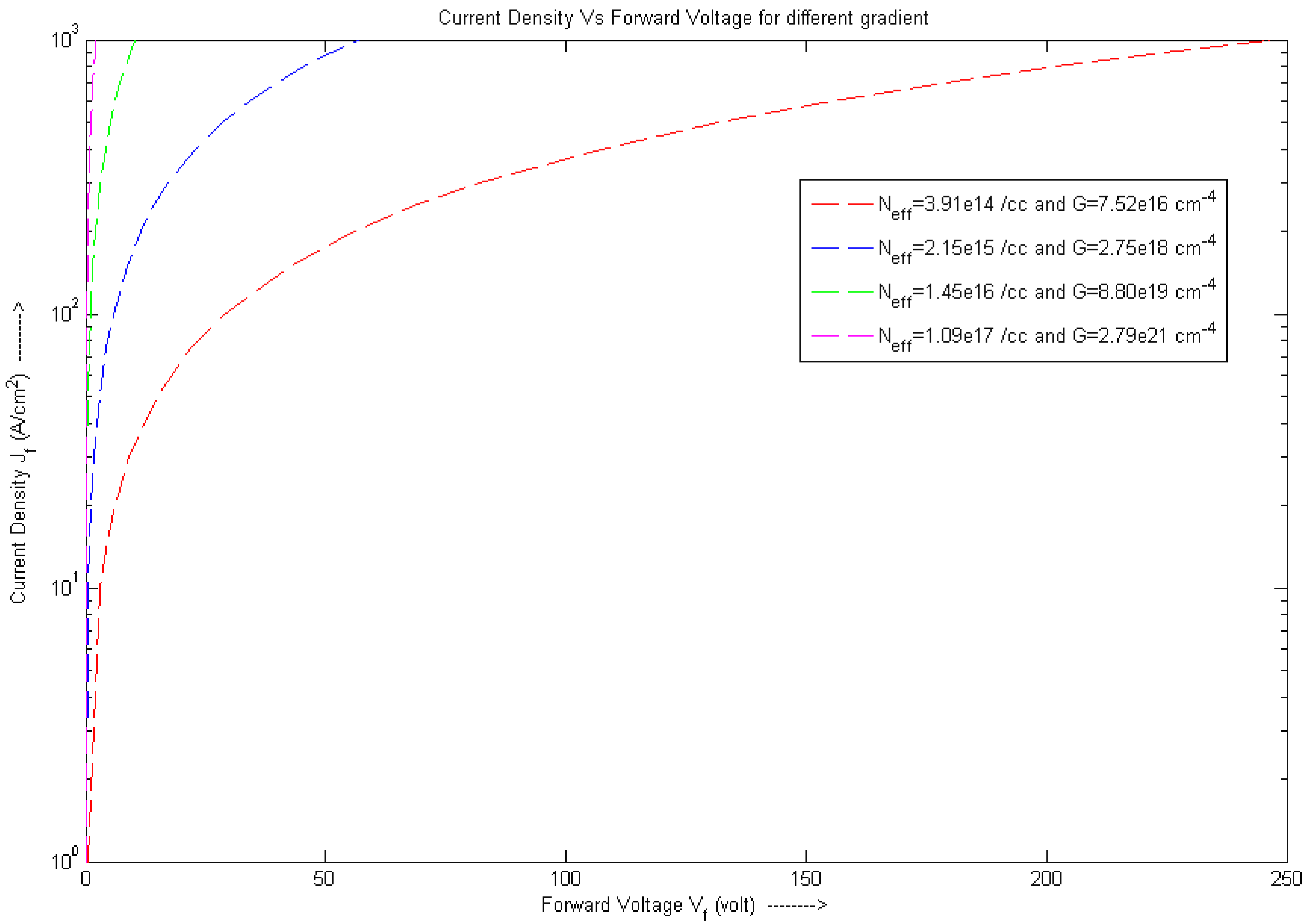


Figure-5.1: Plot of Current Density against Forward Voltage for different values of gradient.

Table-5.7: Values of Power Dissipation at different levels of gradient for different values of Current Density.

J_f (A/cm^2)	P (watt)			
	N_{eff} = 3.91e14 /cm^3 μ_{eff} = 530 cm^2/V.sec G = 7.52e16 cm^{-4}	N_{eff} = 2.15e15 /cm^3 μ_{eff} = 530 cm^2/V.sec G = 2.75e18 cm^{-4}	N_{eff} = 1.45e16 /cm^3 μ_{eff} = 450 cm^2/V.sec G = 8.80e19 cm^{-4}	N_{eff} = 1.09e17 /cm^3 μ_{eff} = 290 cm^2/V.sec G = 2.79e21 cm^{-4}
1	3.81e-5	7.08e-6	1.24e-6	2.56e-7
10	3.70e-3	7.04e-4	1.24e-4	2.56e-5
15	8.27e-3	1.58e-3	2.79e-4	5.76e-5
20	0.0146	2.81e-3	4.95e-4	1.02e-4
30	0.0325	6.31e-3	1.11e-3	2.30e-4
50	0.0891	0.0175	3.09e-3	6.40e-4
75	0.1976	0.0393	6.96e-3	1.44e-3
100	0.3472	0.0697	0.0124	2.56e-3
150	0.7671	0.1564	0.0278	5.76e-3
200	1.3435	0.2774	0.0494	0.0102
250	2.0724	0.4326	0.0772	0.0160
300	2.9504	0.6220	0.1111	0.0230
400	5.1420	1.1026	0.1975	0.0409
500	7.8973	1.7187	0.3084	0.0640
600	11.198	2.4697	0.4440	0.0921
700	15.029	3.3551	0.6041	0.1254
800	19.376	4.3747	0.7888	0.1637
900	24.224	5.5279	0.9981	0.2072
1000	29.562	6.8144	1.2319	0.2558

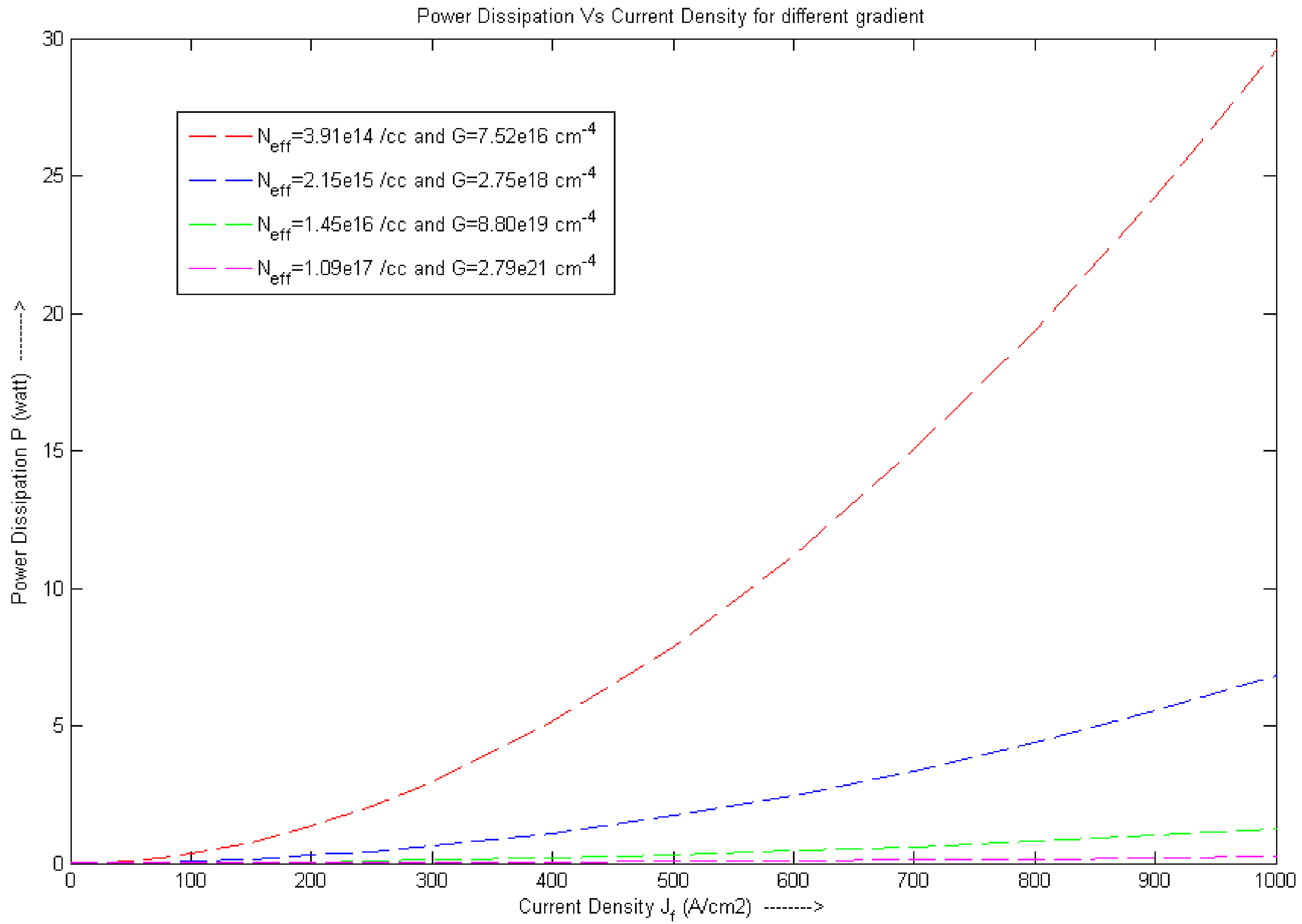


Figure-5.2: Plot of Power Dissipation against Current Density for different values of gradient.

Table-5.8: Values of Power Dissipation at different levels of current density for different values of Gradient.

N_{eff} (/cc)	μ_{eff} (cm^2/V.Sec)	G (cm^{-4})	P (watt)			
			J_f=1 A/cm^2	J_f=10 A/cm^2	J_f=100 A/cm^2	J_f=1000 A/cm^2
3.91e14	530	7.52e16	3.81e-5	3.71e-3	0.3472	29.562
5.17e14	530	1.46e17	2.90e-5	2.84e-3	0.2715	24.321
8.00e14	530	3.80e17	1.89e-5	1.86e-3	0.1812	16.983
1.28e15	530	1.00e18	1.19e-5	1.18e-3	0.1156	11.120
2.15e15	530	2.75e18	7.08e-6	7.04e-4	0.0697	6.8144
3.00e15	530	5.17e18	5.08e-6	5.06e-4	0.0502	4.9411
5.00e15	515	1.33e19	3.14e-6	3.13e-4	0.0312	3.0863
7.00e15	500	2.43e19	2.31e-6	2.31e-4	0.0230	2.2818
9.00e15	480	3.81e19	1.87e-6	1.87e-4	0.0186	1.8537
1.20e16	465	6.34e19	1.45e-6	1.45e-4	0.0145	1.4387
1.45e16	450	8.80e19	1.24e-6	1.24e-4	0.0124	1.2319
1.09e17	290	2.79e21	2.56e-7	2.56e-5	2.56e-3	0.2558

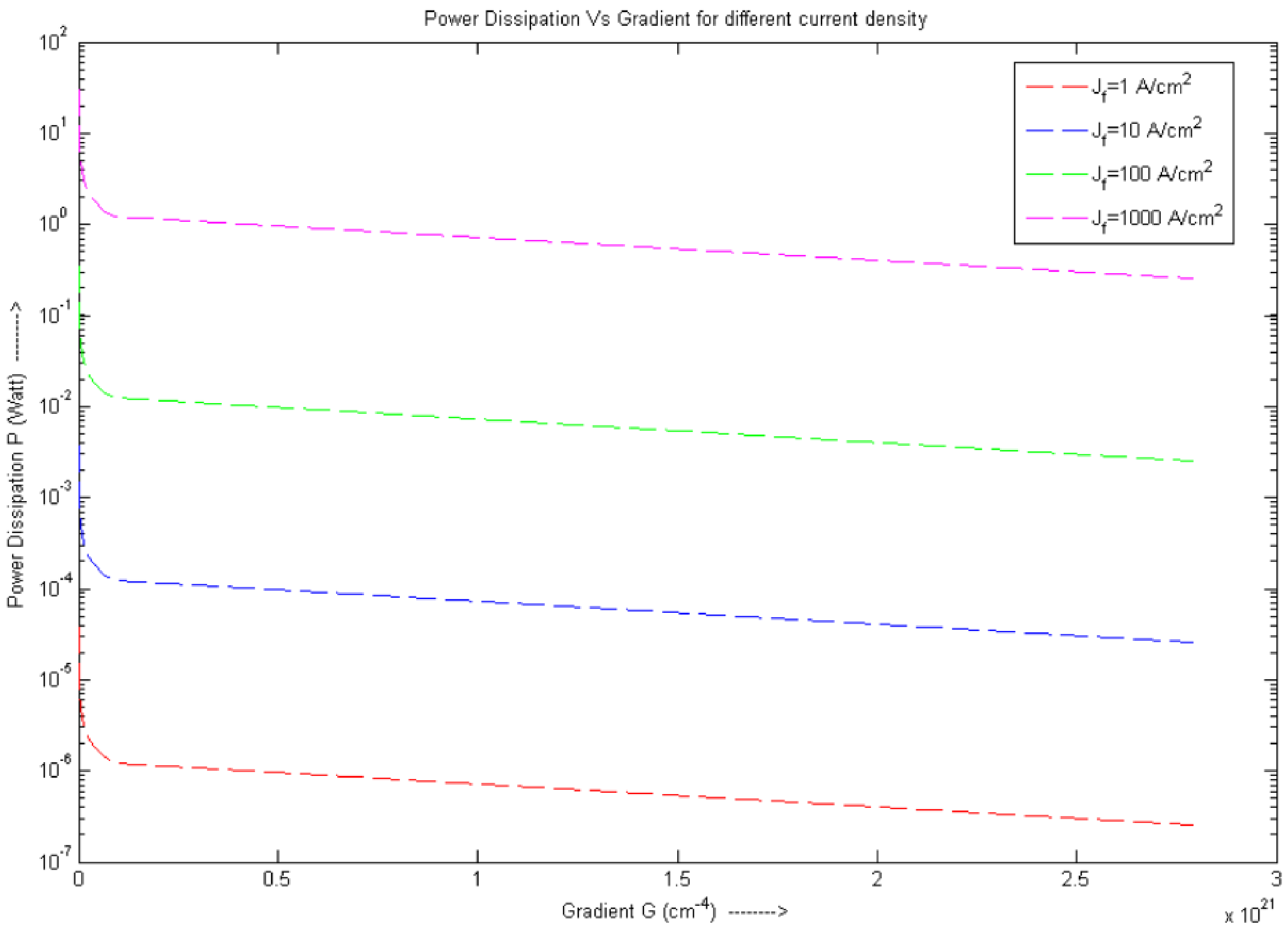


Figure-5.3: Plot of Power Dissipation against Gradient for different values of current density.

CHAPTER–6

COMPARATIVE STUDY OF UNIFORM & LINEARLY GRADED DOPING PROFILE

All calculations done in Chapter-IV and Chapter-V for uniform doping profile and linearly graded doping profile respectively are compared in this chapter to see the improvement in the power dissipation.

6.1 COMPARISON BETWEEN UNIFORM AND GRADED PROFILE

Comparison of Plots of Power Dissipation against Current Density for different values of gradient (in linearly graded profile) and Plot of Power Dissipation against Current Density for different values of doping (in uniform doping profile). Equation used for Percentage Power Saved is given by:

$$Percentage\ Power\ Saved = \left[\frac{Power\ in\ Uniform - Power\ in\ Graded}{Power\ dissipation\ in\ Uniform}\right]_{at\ fix\ J_f} \times 100 \qquad (6.1)$$

Corresponding Tables and Graphs details are as follows:

Table-(6.1) to (6.4): Values of Power Dissipation at specified doping level in uniform and graded profile for different values of Current Density.

Table-6.5: Values of Power Dissipation at different doping levels in uniform and graded both for different values of Current Density.

Table-(6.6) to (6.9): Values of Percentage Power Saved at different levels of current density for different values of Gradient.

Figure-(6.1) to (6.4): Plots of Power Dissipation against Current Density for specified values of doping in uniform and graded profile both.

Figure-6.5: Plot of Power Dissipation against Current Density for different values of doping in uniform and graded profile both.

Figure-6.6: Plot of Percentage Power Saved in Linearly Graded profile against Gradient & Effective doping level for different values of current density.

Table-6.1: Values of Power Dissipation at (3.91e14 /cm^3) doping level in uniform and graded profile for different values of Current Density.

J_f (A/cm^2)	P (watt)	
	Uniform	Linearly Graded
	N_d = 3.91e14 /cm^3	G = 7.52e16 cm^{-4} N_{eff} = 3.91e14 /cm^3
1	4.92e-5	3.81e-5
10	4.89e-3	3.70e-3
15	0.0110	8.27e-3
20	0.0195	0.0146
30	0.0436	0.0325
50	0.1205	0.0891
75	0.2696	0.1976
100	0.4770	0.3472
150	1.0646	0.7671
200	1.8796	1.3435
250	2.9188	2.0724
300	4.1795	2.9504
400	7.3553	5.1420
500	11.389	7.8973
600	16.264	11.198
700	21.965	15.029
800	28.478	19.376
900	35.790	24.224
1000	43.888	29.562

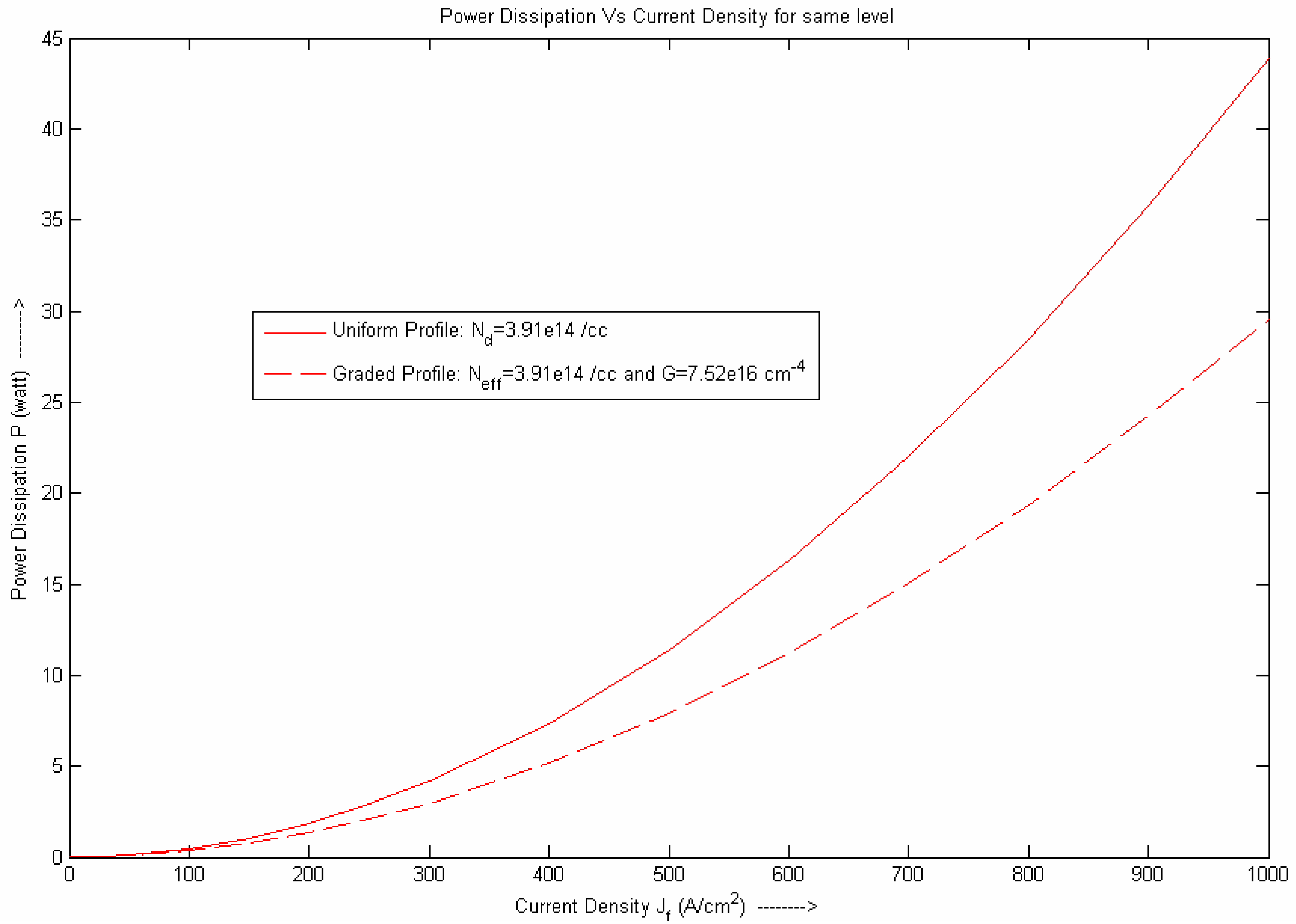


Figure-6.1: Plots of Power Dissipation against Current Density for (3.91e14 /cm^3) values of doping in uniform and graded profile both.

Table-6.2: Values of Power Dissipation at (2.15e15 /cm^3) doping level in uniform and graded profile for different values of Current Density.

J_f (A/cm^2)	**P (watt)**	
	Uniform	**Linearly Graded**
	N_d = 2.15e15 /cm^3	**G = 2.75e18 cm^{-4} N_{eff} = 2.15e15 /cm^3**
1	8.97e-6	7.08e-6
10	8.97e-4	7.04e-4
15	2.02e-3	1.58e-3
20	3.58e-3	2.81e-3
30	8.06e-3	6.31e-3
50	0.0224	0.0175
75	0.0503	0.0393
100	0.0893	0.0697
150	0.2006	0.1564
200	0.3562	0.2774
250	0.5560	0.4326
300	0.7999	0.6220
400	1.4196	1.1026
500	2.2148	1.7187
600	3.1849	2.4697
700	4.3296	3.3551
800	5.6483	4.3747
900	7.1408	5.5279
1000	8.8065	6.8144

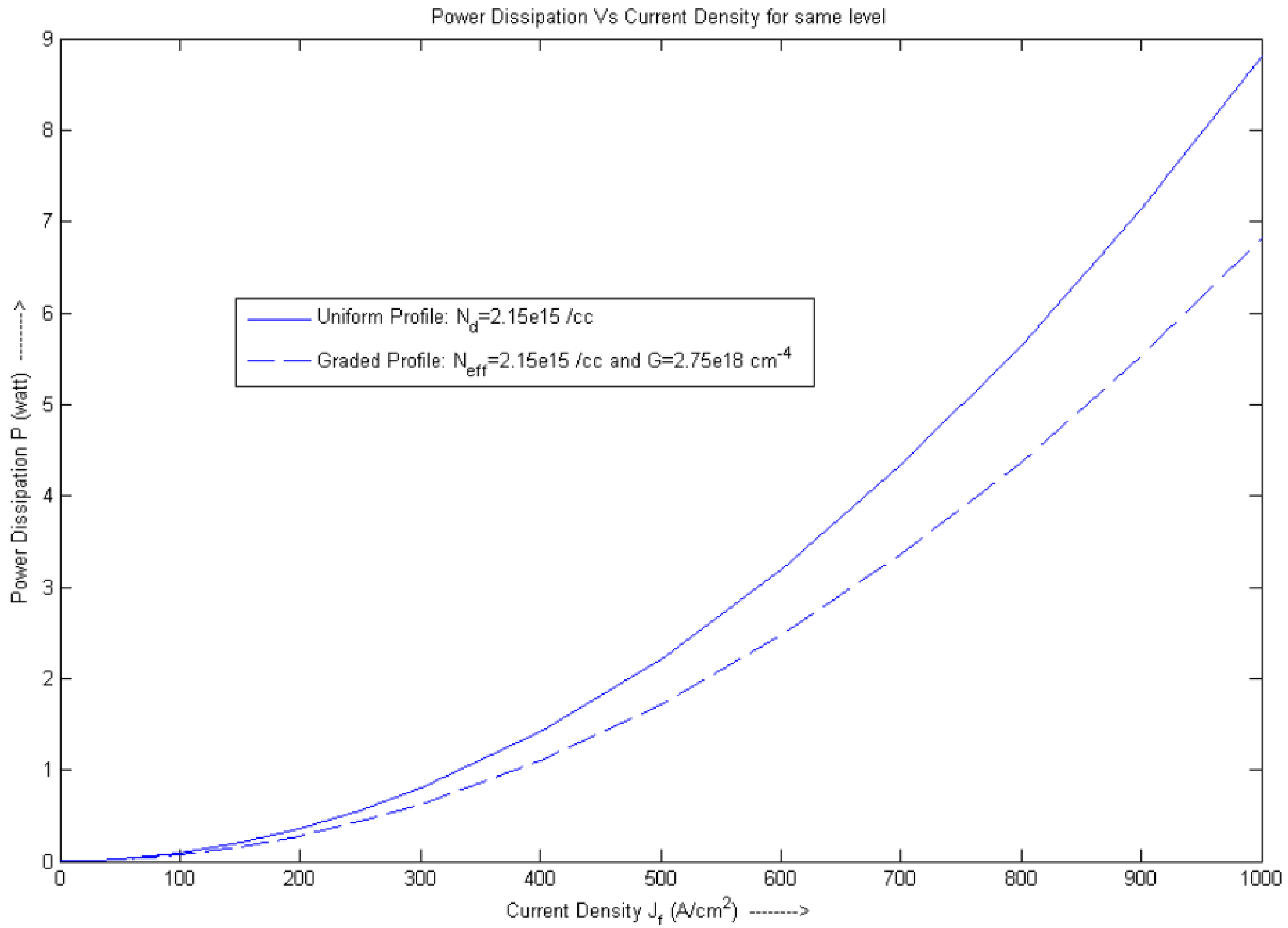


Figure-6.2: Plots of Power Dissipation against Current Density for (2.15e15 /cm^3) values of doping in uniform and graded profile both.

Table-6.3: Values of Power Dissipation at (1.45e16 /cm^3) doping level in uniform and graded profile for different values of Current Density.

J_f (A/cm^2)	P (watt)	
	Uniform	**Linearly Graded**
	N_d = 1.45e16 /cm^3	G = 8.80e19 cm^{-4} N_{eff} = 1.45e16 /cm^3
1	1.57e-6	1.24e-6
10	1.57e-4	1.24e-4
15	3.53e-4	2.79e-4
20	6.27e-4	4.95e-4
30	1.42e-3	1.11e-3
50	3.92e-3	3.09e-3
75	8.82e-3	6.96e-3
100	0.0157	0.0124
150	0.0353	0.0278
200	0.0627	0.0494
250	0.0979	0.0772
300	0.1410	0.1111
400	0.2506	0.1975
500	0.3914	0.3084
600	0.5635	0.4440
700	0.7668	0.6041
800	1.0014	0.7888
900	1.2671	0.9981
1000	1.5641	1.2319

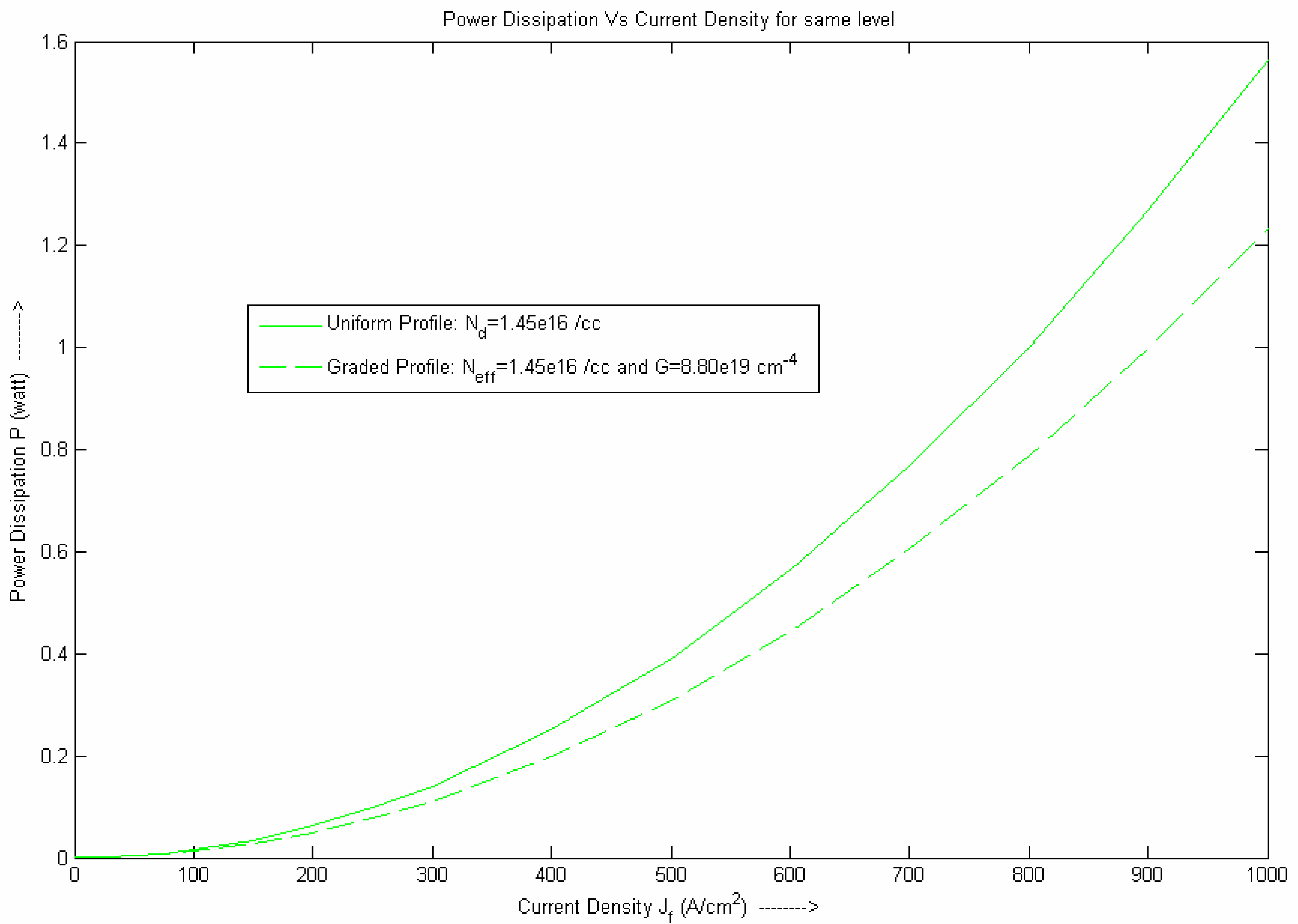


Figure-6.3: Plots of Power Dissipation against Current Density for (1.45e16 /cm^3) values of doping in uniform and graded profile both.

Table-6.4: Values of Power Dissipation at (1.09e17 /cm^3) doping level in uniform and graded profile for different values of Current Density.

J_f (A/cm^2)	P (watt)	
	Uniform	**Linearly Graded**
	N_d = 1.09e17 /cm^3	G = 2.79e21 cm^{-4} N_{eff} = 1.09e17 /cm^3
1	3.24e-7	2.56e-7
10	3.24e-5	2.56e-5
15	7.29e-5	5.76e-5
20	1.30e-4	1.02e-4
30	2.91e-4	2.30e-4
50	8.10e-4	6.40e-4
75	1.82e-3	1.44e-3
100	3.24e-3	2.56e-3
150	7.29e-3	5.76e-3
200	0.0130	0.0102
250	0.0202	0.0160
300	0.0291	0.0230
400	0.0518	0.0409
500	0.0809	0.0640
600	0.1166	0.0921
700	0.1586	0.1254
800	0.2072	0.1637
900	0.2622	0.2072
1000	0.3237	0.2558

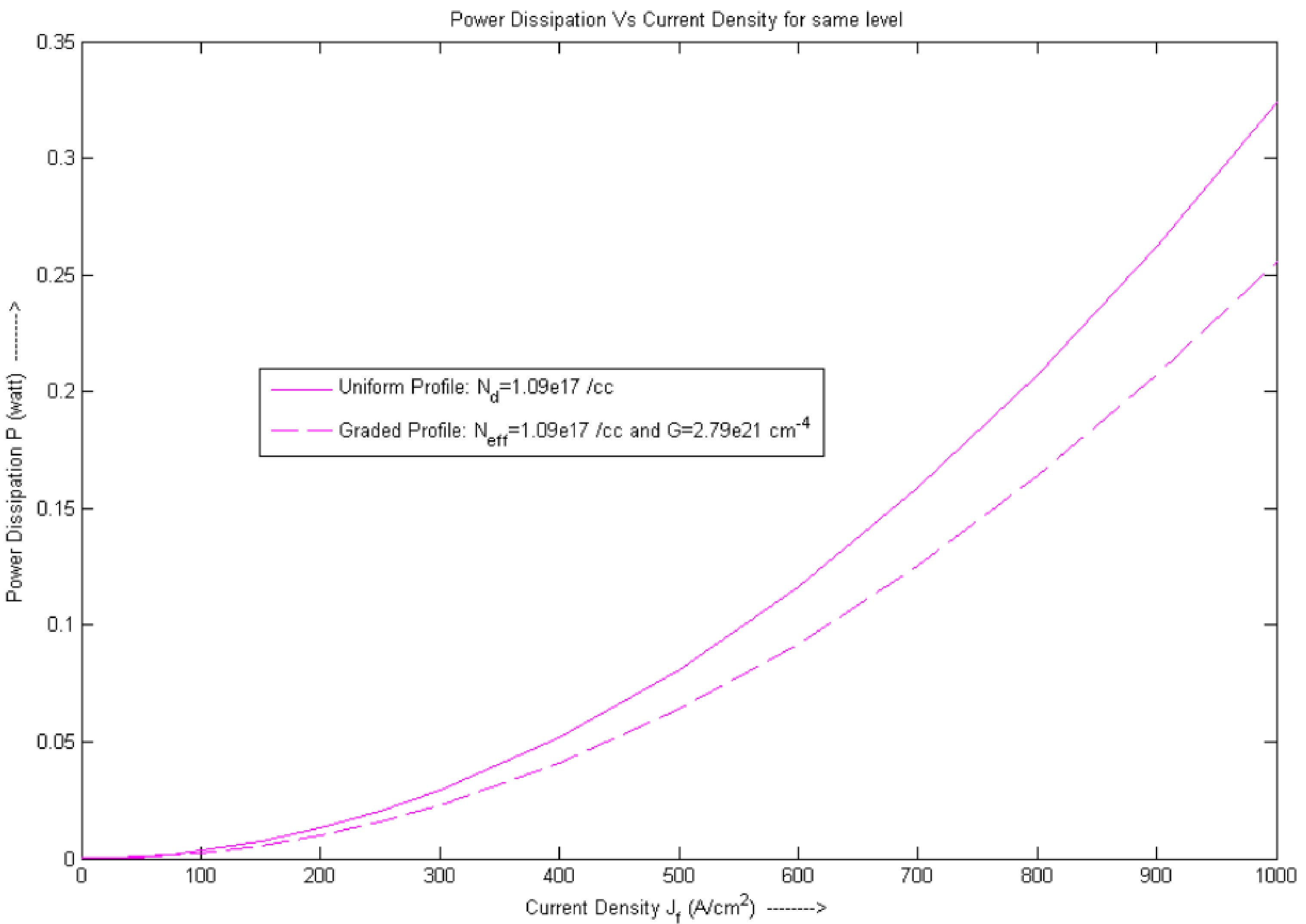


Figure-6.4: Plots of Power Dissipation against Current Density for (1.09e17 /cm^3) values of doping in uniform and graded profile both.

Table-6.5: Values of Power Dissipation at different doping levels in uniform and graded both for different values of Current Density.

J_f (A/cm^2)	P (watt)							
	Uniform				Linearly Graded			
	N_d = 3.91e14 /cm^3	N_d = 2.15e15 /cm^3	N_d = 1.45e16 /cm^3	N_d = 1.09e17 /cm^3	G = 7.52e16 cm^{-4} N_{eff} = 3.91e14 /cm^3	G = 2.75e18 cm^{-4} N_{eff} = 2.15e15 /cm^3	G = 8.80e19 cm^{-4} N_{eff} = 1.45e16 /cm^3	G = 2.79e21 cm^{-4} N_{eff} = 1.09e17 /cm^3
1	4.92e-5	8.97e-6	1.57e-6	3.24e-7	3.81e-5	7.08e-6	1.24e-6	2.56e-7
10	4.89e-3	8.97e-4	1.57e-4	3.24e-5	3.70e-3	7.04e-4	1.24e-4	2.56e-5
15	0.0110	2.02e-3	3.53e-4	7.29e-5	8.27e-3	1.58e-3	2.79e-4	5.76e-5
20	0.0195	3.58e-3	6.27e-4	1.30e-4	0.0146	2.81e-3	4.95e-4	1.02e-4
30	0.0436	8.06e-3	1.42e-3	2.91e-4	0.0325	6.31e-3	1.11e-3	2.30e-4
50	0.1205	0.0224	3.92e-3	8.10e-4	0.0891	0.0175	3.09e-3	6.40e-4
75	0.2696	0.0503	8.82e-3	1.82e-3	0.1976	0.0393	6.96e-3	1.44e-3
100	0.4770	0.0893	0.0157	3.24e-3	0.3472	0.0697	0.0124	2.56e-3
150	1.0646	0.2006	0.0353	7.29e-3	0.7671	0.1564	0.0278	5.76e-3
200	1.8796	0.3562	0.0627	0.0130	1.3435	0.2774	0.0494	0.0102
250	2.9188	0.5560	0.0979	0.0202	2.0724	0.4326	0.0772	0.0160
300	4.1795	0.7999	0.1410	0.0291	2.9504	0.6220	0.1111	0.0230
400	7.3553	1.4196	0.2506	0.0518	5.1420	1.1026	0.1975	0.0409
500	11.389	2.2148	0.3914	0.0809	7.8973	1.7187	0.3084	0.0640
600	16.264	3.1849	0.5635	0.1166	11.198	2.4697	0.4440	0.0921
700	21.965	4.3296	0.7668	0.1586	15.029	3.3551	0.6041	0.1254
800	28.478	5.6483	1.0014	0.2072	19.376	4.3747	0.7888	0.1637
900	35.790	7.1408	1.2671	0.2622	24.224	5.5279	0.9981	0.2072
1000	43.888	8.8065	1.5641	0.3237	29.562	6.8144	1.2319	0.2558

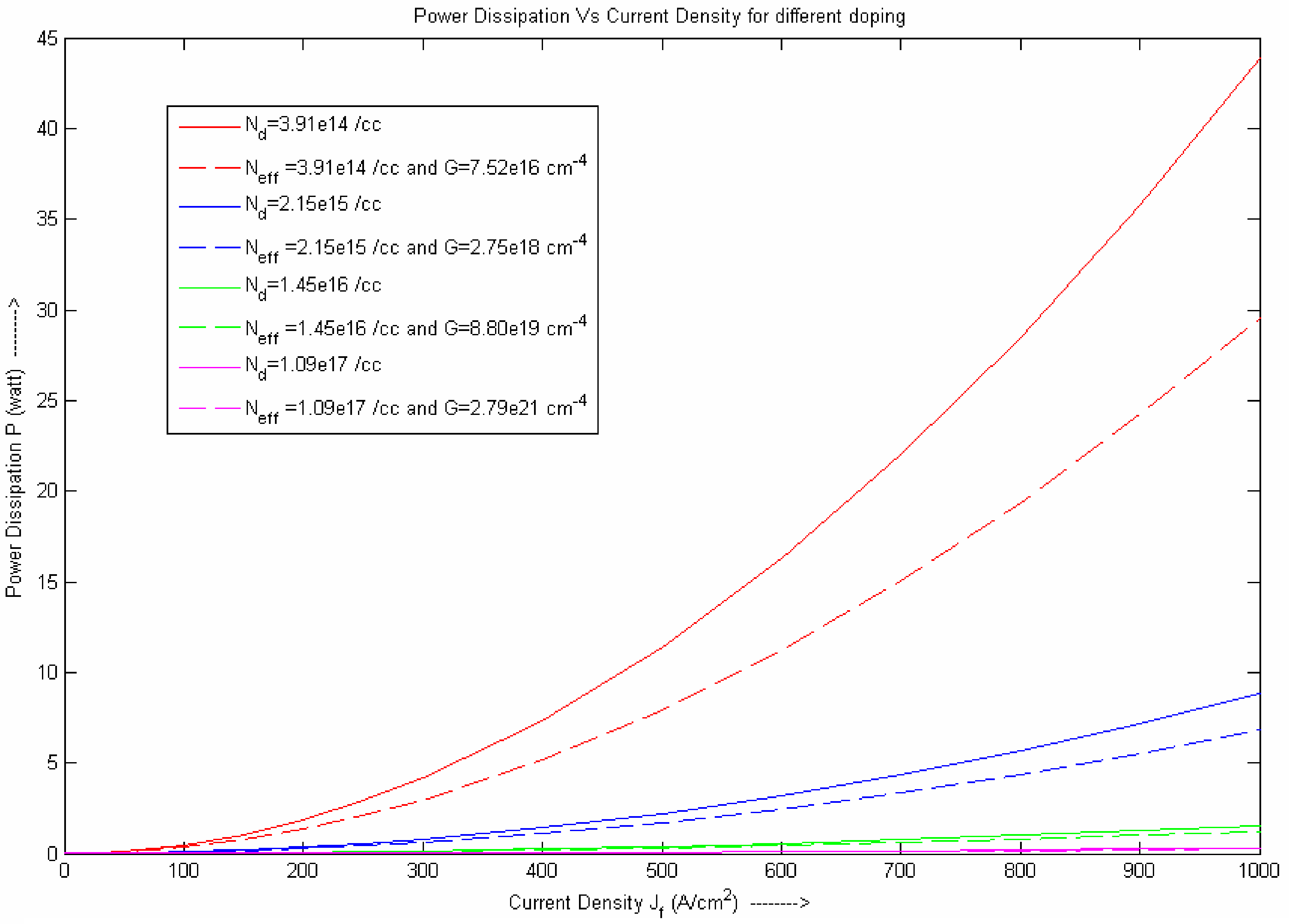


Figure-6.5: Plot of Power Dissipation against Current Density for different values of doping in uniform and graded profile both.

Table-6.6: Values of Percentage Power Saved at J_f = 1 A/cm^2 of current density for different values of Gradient.

Uniform	Graded		Power (watt) at J_f = 1 A/cm^2			
N_d (/cc)	G (cm^{-4})	N_{eff} (/cc)	Uniform	Graded	Difference	Percentage Save
3.91e14	7.52e16	3.91e14	4.92e-5	3.81e-5	1.11e-5	22.5461
5.17e14	1.46e17	5.17e14	3.73e-5	2.90e-5	8.24e-6	22.0998
8.00e14	3.80e17	8.00e14	2.41e-5	1.89e-5	5.22e-6	21.6576
1.28e15	1.00e18	1.28e15	1.51e-6	1.19e-5	3.22e-6	21.3762
2.15e15	2.75e18	2.15e15	8.98e-6	7.08e-6	1.90e-6	21.1947
3.00e15	5.17e18	3.00e15	6.44e-6	5.08e-6	1.36e-6	21.1199
5.00e15	1.33e19	5.00e15	3.98e-6	3.14e-6	8.37e-7	21.0451
7.00e15	2.43e19	7.00e15	2.92e-6	2.31e-6	6.15e-7	21.0130
9.00e15	3.81e19	9.00e15	2.37e-6	1.87e-6	4.98e-7	20.9950
1.20e16	6.34e19	1.20e16	1.83e-6	1.45e-6	3.85e-7	20.9785
1.45e16	8.80e19	1.45e16	1.57e-6	1.24e-6	3.29e-7	20.9701
1.09e17	2.79e21	1.09e17	3.24e-7	2.56e-7	6.78e-8	20.9305

Table-6.7: Values of Percentage Power Saved at J_f = 10 A/cm^2 of current density for different values of Gradient.

Uniform	Graded		Power (watt) at J_f =10 A/cm^2			
N_d (/cc)	G (cm^{-4})	N_{eff} (/cc)	Uniform	Graded	Difference	Percentage Save
3.91e14	7.52e16	3.91e14	4.89e-3	3.71e-3	1.18e-3	24.1714
5.17e14	1.46e17	5.17e14	3.71e-3	2.84e-3	8.62e-4	23.2659
8.00e14	3.80e17	8.00e14	2.40e-3	1.86e-3	5.38e-4	22.3789
1.28e15	1.00e18	1.28e15	1.50e-3	1.18e-3	3.28e-4	21.8197
2.15e15	2.75e18	2.15e15	8.97e-4	7.04e-4	1.92e-4	21.4613
3.00e15	5.17e18	3.00e15	6.43e-4	5.06e-4	1.37e-4	21.3139
5.00e15	1.33e19	5.00e15	3.97e-4	3.13e-4	8.41e-5	21.1666
7.00e15	2.43e19	7.00e15	2.92e-4	2.31e-4	6.17e-5	21.1033
9.00e15	3.81e19	9.00e15	2.37e-4	1.87e-4	4.99e-5	21.0677
1.20e16	6.34e19	1.20e16	1.83e-4	1.45e-4	3.86e-5	21.0352
1.45e16	8.80e19	1.45e16	1.57e-4	1.24e-4	3.30e-5	21.0185
1.09e17	2.79e21	1.09e17	3.24e-5	2.56e-5	6.78e-6	20.9399

Table-6.8: Values of Percentage Power Saved at J_f = 100 A/cm^2 of current density for different values of Gradient.

Uniform	Graded		Power (watt) at J_f = 100 A/cm^2			
N_d (/cc)	G (cm^{-4})	N_{eff} (/cc)	Uniform	Graded	Difference	Percentage Save
3.91e14	7.52e16	3.91e14	0.4770	0.3472	0.1298	27.2037
5.17e14	1.46e17	5.17e14	0.3639	0.2715	0.0924	25.3955
8.00e14	3.80e17	8.00e14	0.2374	0.1812	0.0562	23.6688
1.28e15	1.00e18	1.28e15	0.1493	0.1156	0.0338	22.6038
2.15e15	2.75e18	2.15e15	0.0893	0.0697	0.0196	21.9313
3.00e15	5.17e18	3.00e15	0.0641	0.0502	0.0138	21.6564
5.00e15	1.33e19	5.00e15	0.0397	0.0312	8.48e-3	21.3818
7.00e15	2.43e19	7.00e15	0.0292	0.0230	6.21e-3	21.2640
9.00e15	3.81e19	9.00e15	0.0237	0.0186	5.02e-3	21.1975
1.20e16	6.34e19	1.20e16	0.0183	0.0145	3.87e-3	21.1368
1.45e16	8.80e19	1.45e16	0.0157	0.0124	3.31e-3	21.1056
1.09e17	2.79e21	1.09e17	3.24e-3	2.56e-3	6.79e-4	20.9573

Table-6.9: Values of Percentage Power Saved at J_f = 1000 A/cm^2 of current density for different values of Gradient.

Uniform	Graded		Power (watt) at J_f = 1000 A/cm^2			
N_d (/cc)	G (cm^{-4})	N_{eff} (/cc)	Uniform	Graded	Difference	Percentage Save
3.91e14	7.52e16	3.91e14	43.888	29.562	14.326	32.6423
5.17e14	1.46e17	5.17e14	34.231	24.321	9.9101	28.9502
8.00e14	3.80e17	8.00e14	22.848	16.983	5.8653	25.6707
1.28e15	1.00e18	1.28e15	14.587	11.120	3.4674	23.7708
2.15e15	2.75e18	2.15e15	8.8065	6.8144	1.9921	22.6205
3.00e15	5.17e18	3.00e15	6.3477	4.9411	1.4066	22.1592
5.00e15	1.33e19	5.00e15	3.9417	3.0863	0.8554	21.7004
7.00e15	2.43e19	7.00e15	2.9069	2.2818	0.6252	21.5044
9.00e15	3.81e19	9.00e15	2.3582	1.8537	0.5045	21.3929
1.20e16	6.34e19	1.20e16	1.8279	1.4387	0.3892	21.2913
1.45e16	8.80e19	1.45e16	1.5641	1.2319	0.3322	21.2388
1.09e17	2.79e21	1.09e17	0.3237	0.2558	0.0679	20.9856

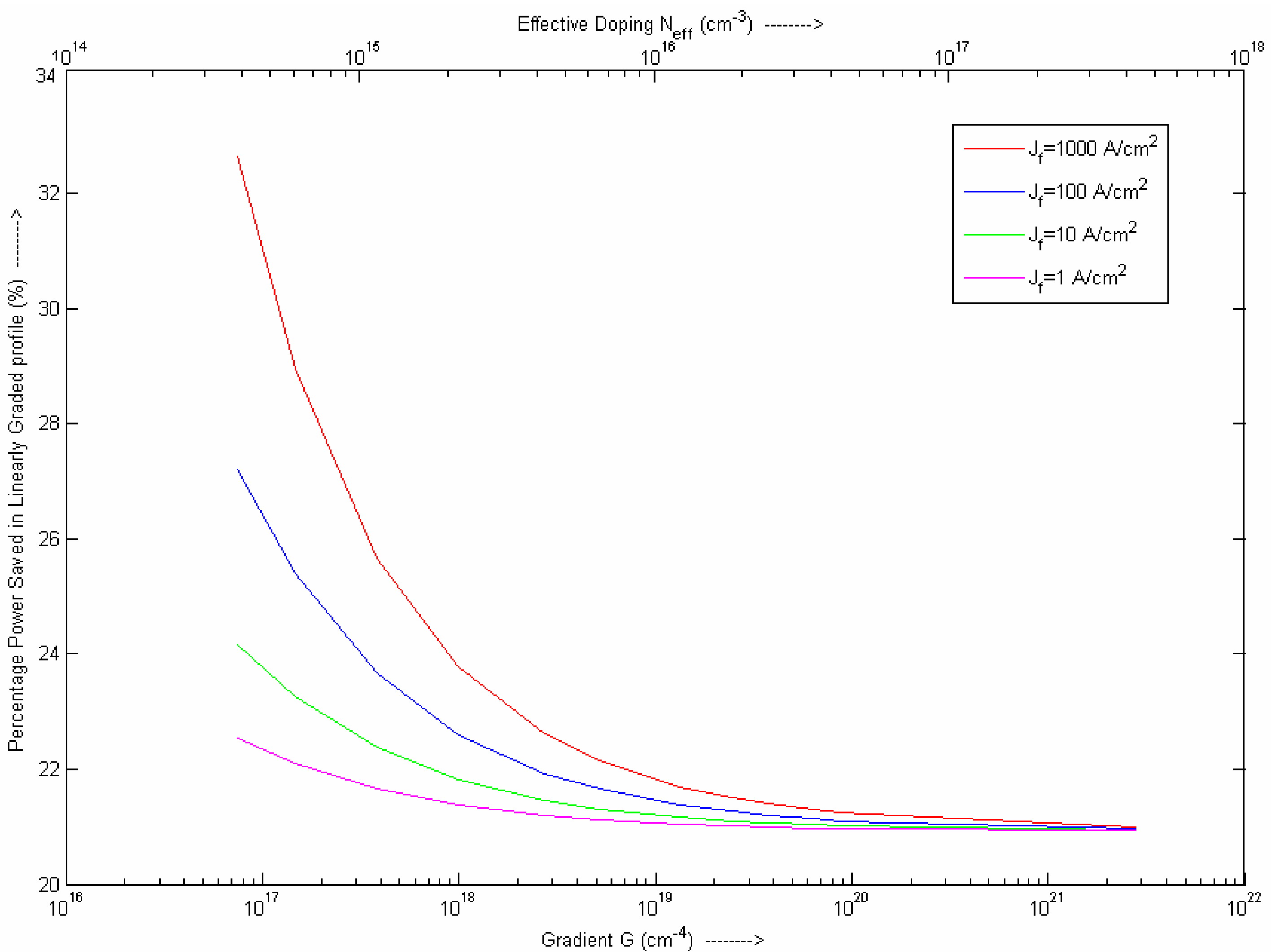


Figure-6.6: Plot of Percentage Power Saved in Linearly Graded profile against Gradient & Effective doping for different values of current density.

CHAPTER–7

CONCLUSION & FUTURE WORK

The current density versus forward voltage i.e. J_f Vs V_f characteristic of the device have been shown for various doping levels of the drift region for uniformly formed and linearly graded profile. These are shown in Fig.4.1 and 5.1 respectively. It can be seen that the uniformly doped drift region profile has a less steep gradient than a linearly graded profile. Also the current saturation for any value of gradient with an effective concentration in linearly graded profile occurs at lower values of forward voltage drop in a linearly graded profile as compare to the same doping level for the uniformly doped region.

The study of power dissipation P_D against current density J_f shown in Fig.4.2 and 5.2 for a given value of doping level, say $3.91x10^{14}cm^{-3}$, shows that the power dissipation is much greater than those of a graded profile with a gradient of $7.52x10^{16}cm^{-4}$ and N_{eff} equal to the doping level $3.91x10^{14}cm^{-3}$ of the uniformly doped device. The magnitude of P_D with these specification shows that at a current density of $1000A/cm^2$ gives a power dissipation of about 43.88W for a uniformly doped device as against 29.56W for the linearly graded DIMOSFET. There is a decline in P_D for all values of current density and all values of doping levels in the case of linearly graded device than the uniformly doped one.

The dependence of power dissipation on doping level in the case of uniformly doped drift region of the DIMOSFET is shown in Fig.4.3 and the power dissipation against gradient of a linearly graded device Fig.5.3 with the same value of effective doping concentration as the uniformly doped device shows that there is significantly low power dissipation has low values of concentration gradient in the case of the linearly graded DIMOSFET than the uniformly doped device. However the values of power dissipations are almost equal at higher values of doping levels and concentration gradients. This is found to be true for all values of current density J_f.

Finally a comparative study of power dissipation against current density for uniformly doped and linearly graded profile of a DIMOSFET is shown for various values of N_d and N_{eff} in Fig.6.5. It can be easily seen that there is significant reduction in power dissipation in the linearly graded profile than the uniformly doped one and this reduction increases with increasing magnitude of J_f. The overall percentage reduction in power is well passed 32.64% at current density of $1000A/cm^2$ this is shown in Fig.6.6. Lower current levels yield a lower percentage of power dissipation margins.

In conclusion it may be said that a DIMOSFET with linearly graded drift region can significantly lower power dissipation at high current levels at a given values of effective doping level and concentration gradient as compared to the same doping level of a uniformly doped drift region of a DIMOSFET. The calculations for this device have been made to set the device height of 148.61μm in order to accommodate a blocking voltage of 8kV.

It is expected that the linearly graded profile may also be deign to provide not only a lower power dissipation but also to provide a higher value of breakdown voltage of a DIMOSFET. This problem is being investigated as a future work for developing SiC DIMOSFETs with higher breakdown voltages.

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