Design and Analysis of Mem-element Emulators and their Applications

A thesis submitted in partial fulfilment of the requirement for the Award of the Degree of

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in

VLSI Design

by

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Declaration

I, **Dakshika Sharma**, hereby declare that the work presented in this thesis titled "Design and Analysis of Mem-element Emulators and their Applications", submitted in partial fulfilment of the requirements for the award of the Master of Technology degree, at the Department of Electronics and Communication Engineering, Thapar Institute of Engineering & Technology (Deemed University), Patiala, is an original record of research conducted under the supervision of **Dr. Shireesh Kumar Rai, Associate Professor, and Dr. Navneet Sharma, Assistant Professor, DECE**, from August 2024 to July 2025.

Dakshika

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I certify that the above statement made by the student is accurate to the best of my knowledge and belief.

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ABSTRACT

The family of mem-elements traces its origins back to the memristor, a concept introduced by Leon Chua in 1971 as the fourth fundamental passive circuit element. HP Labs fabricated the first memristor in 2008 using nanoscale titanium dioxide films. The memristor exhibits a unique memory-dependent resistance, which changes based on the applied voltage and current history. Following this breakthrough, the concept of memory-retaining properties was extended to other passive elements, leading to the development of memcapacitors, meminductors, and memtranstors.

The memcapacitor is an extension of the memristor concept, representing a capacitor with memory-dependent capacitance. Unlike conventional capacitors, a memcapacitor exhibits history-dependent charge-voltage characteristics, meaning its capacitance varies based on past input signals. Their ability to retain and dynamically adjust capacitance opens new possibilities for programmable analog circuits and chaotic oscillators. The memcapacitor emulator circuit is realized using an operational transconductance amplifier (OTA), a current differencing buffered amplifier (CDBA), and a grounded capacitor, ensuring an efficient and compact design. Simulations have been performed to validate its functionality, including transient response analysis and non-volatility testing under parametric variations.

In addition, the memtranstor emulator is proposed using a current conveyor (CCII) and a voltage differencing current conveyor (VDCC). This design emulates the memtranstor's unique flux-charge relationship and magnetoelectric-like behavior, supporting its potential use in memory-driven analog computation. The lack of commercially available mem-elements in IC form has created a need for emulator circuits replicating their characteristics. These mem-elements are utilized in various applications, including non-volatile memory, reconfigurable analog signal processing (such as filters and chaotic oscillators), and neuromorphic computing.

Both emulator circuits were simulated using LTspice, and then implemented using 180nm CMOS technology. Transient and frequency-domain analyses confirm that the circuits effectively mimic the dynamic behavior of their theoretical counterparts.

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ABBREVIATIONS

MOS-FET:	Metal-oxide-semiconductor field-effect transistor
CMOS:	Complementary metal oxide semiconductor
SPICE:	Simulation program with integrated circuit emphasis
TiO2:	Titanium dioxide
HP:	Hewlett-Packard
Op-amp:	Operational amplifier
NMOS:	N-type metal oxide semiconductor
PMOS:	P-type metal oxide semiconductor
ABB	Analog building blocks
OTA:	Operational transconductance amplifier
CDBA:	Current differencing buffered amplifier
VDCC:	Voltage-differencing current conveyors
CCII:	Second-generation current conveyors
ME:	Magnetoelectric effect
PHL:	Pinched hysteresis loop

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Chapter 1
Introduction

1.1 Introduction

The four linear components of circuit theory are the resistor, capacitor, inductor, and recently added transtor. These components are necessary to build a circuit; however, contemporary electronics require various applications, including artificial intelligence, neuromorphic computer hardware, and adaptive learning circuits, which frequently necessitate the addition of more components. As a result of their non-volatile and adaptable behaviors, memristor, memcapacitor, meminductor, and memtranstor were created.

These elements possess memory, allowing their characteristics to be dynamically adjusted based on past states. Memristors, memcapacitors, meminductors, and memtranstors serve as extensions of resistors, capacitors, inductors, and transtors, respectively. The resistor (R) defines the relationship between voltage (v) and current (i), the capacitor links charge (q) and voltage (v), the inductor relates flux (ϕ) and current (i), while the transtor (T) directly connects flux (ϕ) and charge (q). While conventional elements exhibit a linear corelation between any two fundamental variables—voltage, current, charge, and flux—their memory-based counterparts, including memristor (MR), memcapacitor (MC), meminductor (ML), and memtranstor (MT), exhibit a nonlinear response characterized by pinched hysteresis loops (PHLs). The relation of these elements is presented in Fig. 1.

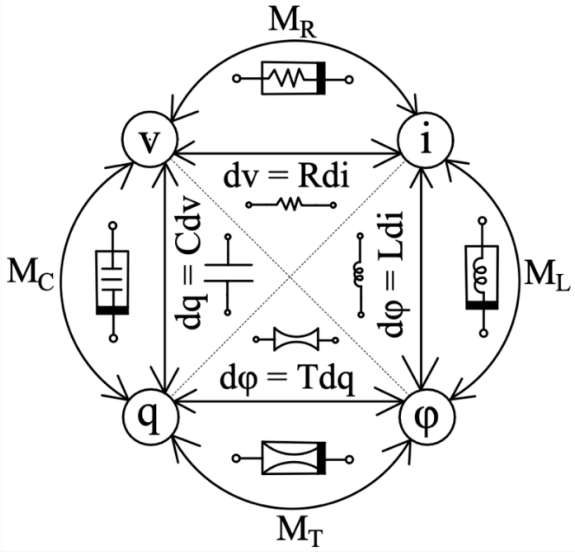


Figure 1. Interrelation of conventional elements and mem-elements

Mem-elements have several benefits, but only the memristor is commercially available; others are still unavailable. Thus, using active building blocks (ABB) such as operational transconductance amplifiers (OTAs), operational amplifiers (OPAMPs), voltage differencing current conveyors (VDCCs), current conveyors (CCs), and voltage differencing transconductance amplifiers (VDTAs), researchers and engineers continue to work on emulators that mimic the behavior of mem-elements. Although several mem-element emulators have been proposed recently, many have intricate circuit designs and lack a standardized design process. This thesis presents a simple memcapacitor emulator circuit and a memtranstors emulator circuit utilizing a current conveyor, a current differencing buffered amplifier (CDBA), an OTA, and a voltage differencing current conveyor, respectively.

The memtranstor emulator is a novel circuit element that links electric charge (q) and magnetic flux (ϕ) through the magnetoelectric (ME) effect. Unlike traditional electronic components, which typically relate voltage and current or their derivatives, the memtranstor is governed by the combined effects of electric and magnetic fields. This unique interaction allows the memtranstor to store information and perform logic operations simultaneously. It is an ideal candidate for memory-in-computation systems, where data processing and storage occur in the same unit, reducing latency and power consumption.

Each memory element, or mem-element, corresponds to a fundamental passive component. The memristor is associated with the resistor, the mem-capacitor with the capacitor, and the mem-inductor with the inductor. Similarly, the memtranstor is the memory-based equivalent of a theoretical component called the transtor, which directly relates magnetic flux and charge.

Most significant characteristic of the memtranstor is its ability to execute pinched hysteresis loops (PHLs) when subjected to alternating input signals. These loops, which can be slanted figure-eight or butterfly-shaped curves, reflect the device’s memory-dependent response and vary based on the alignment of internal domains. Another essential feature is the memtranstor’s non-volatile behaviour, which retains its state even after input removal. This property is especially beneficial in designing low-power logic and memory devices.

Although the memtranstor offers many advantages, it is not yet available as a commercial hardware component. Most existing versions are limited to research laboratories. To overcome this limitation, researchers have developed memtranstor emulators, practical circuits made from standard components that mimic an actual memtranstor's behaviour. These emulators are

valuable tools that help study the memtranstor's characteristics and test its potential in real-world applications without needing specialized or hard-to-access materials.

1.2 Motivation

This work aims to create a memcapacitor emulator and a memtranstor emulator that employs fewer active and passive components, while ensuring high performance. Several memcapacitor emulators have been created in the last ten years by combining passive components with analog building blocks (ABBs). On the other hand, for memtranstors, only limited work has taken place. To add the necessary nonlinearity, many of these systems use multipliers, which leads to intricate circuit layouts. Furthermore, the frequency ranges in which traditional memelement emulators usually function are constrained to the kHz or MHz range.

Existing designs frequently incorporate multiple active building blocks, making their corresponding ICs difficult to source. Furthermore, ABB-based implementations often require numerous passive elements and involve intricate internal circuits with many transistors. While some compact designs demonstrate improved frequency response, they rely on complex internal structures with a high MOSFET count.

In contrast, the memcapacitor emulator and memtranstor emulator proposed in this work employ a simplified yet efficient design using only two operational transconductance amplifiers, a current differencing buffered amplifier, a resistor, a capacitor, and two current conveyors (CCII), a voltage differencing current conveyor, resistors, and capacitors, respectively. This minimalistic approach significantly reduces circuit complexity while achieving electronically tunable characteristics. The proposed emulator enhances operational frequency, extending into the MHz range, and provides a more practical and scalable solution for high-frequency applications.

1.3 Structure of thesis

The thesis is structured into five chapters, with the following overview of each chapter:

Chapter 1 offers a concise overview of the mem-elements. This chapter further explores the idea behind the proposed work and outlines the problem statement.

Chapter 2 presents a literature survey on mem-elements, memcapacitor emulators, memtranstors designed using passive components, multipliers, and analog building blocks (ABBs). The identified research gaps and the formulated objectives are discussed in detail. Additionally, the chapter outlines the research methodology adopted to achieve the proposed goals.

Chapter 3 introduces a memcapacitor emulator based on OTA and CDBA. It offers a comprehensive overview and analysis of the proposed circuit, highlighting its compact design, high-frequency characteristics, and electronic tunability. Additionally, the chapter includes mathematical derivations and simulation results to validate the emulator's performance. All the simulations related to the design of the memcapacitor emulator are done using the LTspice tool. It also includes the implementation of a chaotic oscillator circuit using a memcapacitor. The fundamental Chua circuit for creating chaos is the source of these oscillator circuits.

Chapter 4 introduces a memtranstor emulator based on CCII and VDCC. It thoroughly explains and analyzes the suggested circuit, emphasizing its electronic tunability, high-frequency properties, and compact design. The chapter also provides simulation data and mathematical derivations to verify the emulator's functionality. The LTspice tool is used for all simulations pertaining to the memtranstor emulator’s design. Additionally, it displays the memtranstor-based chaotic oscillator circuit design. These oscillator circuits originate from the basic Chua circuit for generating chaotic outputs.

Chapter 5 presents the study's conclusion and explores the proposed work's future scope.

1.4 Problem statement

The exorbitant cost and limited commercial availability of mem-elements prompted an investigation into more affordable and accessible alternatives. As a result, engineers and scholars were motivated to develop emulation circuits that incorporate various active building blocks (ABB), a circuit designed to replicate the characteristics of a memristor, along with other mem components constructed using these blocks. Different elements, operational transconductance amplifier, differential voltage transconductance amplifier, current feedback opamp, voltage differencing current conveyor, and current conveyor transconductance amplifier, are referenced in the literature for the implementation of mem-element emulators. Given that these blocks are neither straightforward nor economically viable, it is essential to

construct the mem-elements, specifically the memcapacitor and memtranstor, using simpler components, while minimizing the number of passive elements involved. Moreover, creating an efficient analog and mixed-signal architecture presents significant challenges.

Chapter 2

Literature survey

Leon Chua proposed the memristor [1] as the fourth essential circuit element in 1971, and nanoscale systems with linked ionic and electronic transport have physically represented it. The hysteretic I–V characteristics [2] seen in devices such as titanium dioxide cross-point switches can be explained by this phenomenon. Memcapacitive and meminductive systems, which both display pinched hysteresis in their defining variables, have been added to the idea of memory devices. Because of their history-dependent nature, these nanoscale devices have potential for mimicking biological processes and enabling adaptive electronic circuits [3].

Simple circuits using memristor emulators that replicate memcapacitive and meminductive behavior [4], enabling the design of low-cost emulators using off-the-shelf components. By linearly altering a memristor's constitutive relation, Dalibor Biolek, Viera Biolková, and Zdeněk Kolka [5] suggested mutators for implementing memcapacitors and meminductors. They use widely available trans-impedance amplifiers (two AD844) to demonstrate a realistic and economical implementation of their MC←MR mutator based on a charge-controlled memristor.

D.S. Yu, Y. Liang, H. Chen, and Herbert H.C. Iu (2013) presented a flux-controlled memristive circuit incorporating an opamp and a multiplier. This design was modified to create a floating flux-controlled memcapacitor emulator [6] utilizing second-generation current conveyors. This emulator is significant for its utility in circuit design, particularly when grounding constraints are not applicable. A memristor emulator utilizing CCII+ [7] has been introduced, featuring a streamlined design incorporating fewer components. The results of frequency analysis and experiments validate its effective performance, indicating its suitability for practical applications and predictive modeling in memristor-based circuits.

A CMOS-based memristor-emulator utilizing a differential difference current conveyor (DDCC) was proposed. The design features a straightforward architecture, accommodates various frequency modes, removes the requirement for an additional adder in serial connections, and has been validated using SPICE simulations, showcasing its efficacy in compact and adaptive circuit applications. A circuit interface was designed to convert a memristor into nonlinear meminductive and memcapacitive configurations [8-9].

A floating memristor emulator circuit utilizing operational transconductance amplifiers [10] for the implementation of electronically tunable current conveyors (ECCIIs) has been introduced. The design replicates the TiO_2 memristor model and can be constructed using inexpensive, commonly accessible components, rendering it beneficial for educational and practical circuit applications. A novel current-controlled memristor emulator has been developed using two current controlled current conveyors (CCII), diode-connected transistors, and several passive components [11]. The design is straightforward and functional, demonstrating a strong correlation between experimental data and PSPICE results, thereby accurately mimicking the behavior of real memristors. A novel memristor emulator utilizing commercially available components has been introduced, providing continuous resistance levels rather than binary states, thereby enhancing its applicability for analog applications. The functionality was validated using a multivibrator circuit, which can be readily transformed into a voltage-controlled variant because of the emulator's low input impedance, facilitating extensive control over frequency and duty cycle. A new memristor emulator circuit has been developed utilizing solely an exponential amplifier and a CCII+ to replicate a memristor's nonlinear I–V characteristics accurately [12-13]. The design exhibits simplicity and reduced complexity compared to previous circuits, supported by mathematical modeling, PSPICE simulations, and analytical validation that confirm its accuracy and compliance with memristor fingerprints.

A method was proposed and demonstrated for emulating a floating memcapacitor [14] through piecewise linear constitutive relations combined with a switched-capacitor technique, specifically applied to a two-state memcapacitor.

A novel emulator has been introduced that can accurately replicate the dynamic behavior of coupled memcapacitors (MCs) for the implementation of ring oscillators (ROs) [15]. The coupling effect can control the oscillation period and duty cycle, facilitating flexible and wireless signal generation. However, it is essential to perform careful parameter tuning because of the nonlinear dependencies involved.

A circuit design for a floating memristor has been introduced, utilizing current feedback operational amplifiers (CFOAs), grounded capacitors [16], resistors, and diodes to attain the necessary non-linearity and time-constants. Excluding analog multipliers, ADCs, and RDACs reduces power consumption and cost. The circuit effectively demonstrates FM-to-AM signal conversion, thereby validating its functionality. A circuit designed to emulate the flux-

controlled memristor utilizing operational transconductance amplifiers (OTAs) and current conveyor integrated circuits (CCIIs) has been developed. This circuit enables the control of memristance through the transconductance parameter, which can be adjusted by applying a bias voltage [17]. The circuit is designed to support continuous memductance levels and operates effectively across various frequency ranges with straightforward capacitor adjustments. Validation is achieved through SPICE simulations and experimental measurements.

A charge-controlled memristor emulator utilizing a single CMOS-based DVCCTA [18] block has been introduced, demonstrating functionality in incremental and decremental modes via straightforward switching mechanisms. Theoretical, frequency, and non-ideal analyses were validated through simulations and PCB-based experiments, confirming functionality up to 50 kHz and demonstrating non-volatility. High-pass filter responses were analyzed in comparison to resistor behavior. Proposed memristor emulator circuits utilize a single current controlled current conveyor transconductance amplifier with a grounded capacitor, multiplier, and two resistors. The circuits provide benefits including low power consumption, utilization of grounded capacitors, low sensitivity, and reduced transistors [19]. A new memristor emulator circuit is proposed, utilizing a single MO-OTA [20] with a multiplier, a grounded resistor, and a capacitor. This compact design facilitates tunable memristance through OTA bias current, rendering it appropriate for VLSI integration and memristor-based applications, supported by simulation and experimental results confirming its functionality.

A novel floating analog memristance simulator circuit utilizing second-generation current conveyors and passive components is presented. The circuit exhibits frequency-dependent pinched hysteresis and non-volatility, with memristance characteristics that can be tuned by modifying passive elements [21]. The functionality has been validated using PSPICE simulations and experimental results, demonstrating reliable performance from 1 Hz to 40 kHz.

A universal charge-controlled mem-element emulator has been proposed, capable of replicating memristors, memcapacitors, and meminductors utilizing off-the-shelf components [22]. The design adheres to a uniform circuit topology, which promotes cost efficiency and facilitates reproducibility, validated through Multisim simulations and breadboard testing. An analog implementation of a memcapacitor utilizing a differential voltage current conveyor transconductance Amplifier has been introduced [23]. The design is centered on grounded passive elements, targeting complete monolithic integration.

A universal interface circuit has been proposed that is capable of constructing various types of mem-elements when linked to different peripheral circuits [24]. It provides advantages including floating terminals, reconfigurability, reduced area, and high working frequencies, which render it suitable for PCB-based applications. A current-mode grounded memcapacitor emulator has been proposed using a single VDTA and two grounded capacitors [25]. The system facilitates high frequency operation reaching up to 50 MHz, accommodates soft and hard switching mechanisms, and exhibits negative memcapacitance characteristics.

A VDTA-based mutator circuit has been introduced to convert a conventional memristor into a mem-capacitor. This circuit incorporates transconductance gain (gm) directly within the VDTA structure, in contrast to traditional designs [26] that depend on external elements for gm. The emulator has been experimentally validated using off-the-shelf components, providing electronic control of memcapacitance. This makes it a more efficient and superior alternative to current designs.

An integrator-based memcapacitor emulator was introduced, where key circuit parameters can be electronically adjusted. Unlike previous designs, this emulator consists solely of active building blocks, which helps reduce chip area. Its feasibility was confirmed through simulations and nonideality analysis, highlighting the main limitations. A revised technique was also proposed to increase the operating frequency range [27]. A high-frequency memcapacitor emulator was developed utilizing three operational transconductance amplifiers (OTAs), showcasing its applications in amplitude modulation, filtering, oscillator point attraction, and period doubling [28]. The circuit accommodates both incremental and decremental topologies, featuring a streamlined design. Performance validation was conducted utilizing Cadence Virtuoso Spectre with standard 180nm CMOS technology, incorporating post-layout simulations to ensure precise comparison.

A voltage-controlled floating memcapacitor was developed and executed utilizing a known memristor, highlighting its commercial viability. The model employs a limited selection of standard components to facilitate straightforward experimental replication. The analysis focused on nonlinear dynamical behaviors, which included power-off plots, dynamic route maps (DRM), and DC V-Q characteristics [29]. The findings indicated variations in DRM when a current-limiting resistor was applied.

Another memcapacitor emulator circuit has been introduced, utilizing a current conveyor transconductance amplifier (CCTA), a memristor, and a capacitor [30]. It operates within a frequency range of 0.6 Hz to 6.4 Hz and decreases PHL area as frequency increases. Compared to current designs, this approach necessitates fewer passive components and eliminates the need for analog multipliers, thereby streamlining the implementation process. Performance validation is conducted via transient analysis, non-volatility assessments, and the evaluation of PHL characteristics. An electronically controllable memcapacitor emulator has been proposed utilizing an active circuit element. This design offers enhanced connectivity compared to many grounded memcapacitor emulators, supporting serial and parallel configurations while maintaining a straightforward architecture. The circuit's behavior can be electronically adjusted utilizing VB voltage sources [31]. Simulations utilizing TSMC 0.18 μm parameters validate its alignment with actual memcapacitive behavior.

An optimized MOS-based mem-capacitor emulator was developed using active elements and a resistor. Design achieves a high operating frequency of 24 MHz while maintaining efficient area utilization (2034.65 μm^2) and low power consumption (1.86 mW), as confirmed by pre-layout and post-layout analyses in Cadence Virtuoso with TSMC 180 nm PDKs. It significantly improves frequency response, area efficiency, and power savings compared to existing designs. Its practical applicability is further validated through experimental verification using CA3080 analog ICs [32].

A novel memcapacitor emulator has been developed utilizing a single voltage differencing current conveyor (VDCC) as the primary component [33]. The design utilizes exclusively grounded capacitors, which improves simplicity and minimizes non-ideal effects. The primary benefit is electronic tunability, which allows for accurate regulation of inverse memcapacitance. The circuit operates effectively at frequencies up to 50 MHz, fulfilling the non-volatility requirement. The validation of practicality and performance was conducted via LTSpice simulations with a ±0.9 V power supply.

A grounded memcapacitor emulator was developed utilizing a fully differential second-generation current conveyor (FDCCII). The circuit includes of one FDCCII [34], a multiplier, three capacitors, and two MOSFET-based electronic resistors, facilitating electronic tuning of memcapacitance. The system accommodates incremental and decremental adjustments, employing fewer active components than traditional designs. Simulations performed in LTspice, which include frequency response, temperature variation, and Monte Carlo analysis,

exhibit a high level of correlation with theoretical predictions and validate the electronic controllability of the emulator. Shankar et al. (2023) introduced a charge-controlled memcapacitor emulator that employs two MO-OTAs [35-36], a multiplier, and four passive components. This design is distinguished by its provision of electronic tunability and its independence from memristor-based configurations, thereby removing the necessity for a separate mutator circuit. Compared to previous methods, this approach is characterized by increased simplicity and efficiency, utilizing fewer components. The circuit's performance was validated using Cadence OrCAD simulations based on 180nm TSMC CMOS parameters, and its practical feasibility was confirmed through experimental testing with commercially available integrated circuits.

A fully floating, electronically tunable memcapacitor emulator that utilizes two MO-OTAs, analog multipliers, and a smaller number of passive components [37]. The design addresses grounding and complexity limitations, rendering it appropriate for VLSI and breadboard implementations. Simulation results utilizing TSMC 0.18 μm parameters validate the precise memcapacitive behavior observed.

Ananda Y. R. and Satyanarayan (2023) introduced a compact MOS-based memcapacitor emulator that utilizes an operational transconductance amplifier (OTA), a voltage differencing transconductance amplifier (VDTA), and a buffer. The system operates at a frequency of 1.2 MHz, consumes 2.726 mW of power, and occupies an area of 2077.85 μm^2 [38], resulting in high performance metrics. The simulation and experimental results validate its appropriateness for integration with silicon.

Two novel emulator circuits were developed utilizing a single active component—VDTA for meminductor emulation and VDCC for memcapacitor emulation [39]. Both designs incorporate grounded capacitors, provide electronic tunability, and function at frequencies up to 50 MHz. Simulations and experiments confirm the non-volatile characteristics and practical applicability. A memcapacitor emulator is designed utilizing integrators, CCCII, and OTA components, incorporating electronic control through bias current adjustments [40]. The all-active design reduces chip area, facilitating efficient IC implementation and supporting high-frequency operation. Implementing a non-ideality model and an active capacitance multiplier topology contributes to improved performance metrics. Two floating memcapacitor emulators are presented—one utilizing a second-generation current conveyor and the other employing an OTA. Electronic tunability is achieved via external transistors [41] that function as controllable

capacitors and resistors, facilitating incremental and decremental characteristics. Simulations and experimental results based on PCB demonstrate non-volatility and a strong correlation with theoretical analysis.

A memcapacitor circuit is proposed utilizing operational transconductance amplifiers in a mutator configuration, effectively remodeling an OTA-based memristor into a mem-capacitor. The system provides electronic tunability of charge and frequency through the adjustment of transconductance or capacitance. Simulations validate memcapacitive behaviors, and their application in an adaptive learning circuit indicates potential for neuromorphic computing [42]. A memcapacitor emulator circuit is proposed that uses only current sources and MOSFETs, thereby eliminating passive components to achieve a compact design with an area of 617 μm^2. Simulations using Cadence Spectre with the XFAB 0.18 μm process validate high-frequency performance. Logic AND and OR gates' implementations validate the circuit's practicality through simulation and experimental methods [43].

A grounded charge-controlled memcapacitor emulator is presented, utilizing a voltage differencing current conveyor (VDCC) and four MOSFETs, thereby removing the requirement for passive components or an independent memristor emulator [44]. The design provides autonomous electronic regulation of circuit functionality.

A novel floating memtranstor (MT) [45] emulator is introduced to directly implement the ϕ–q relationship, facilitating the direct measurement of inverse memtranstance. The functionality is validated using theoretical analysis, MATLAB simulations, PSPICE simulations, and hardware experiments. The emulator effectively replicates butterfly-shaped and 8-shaped pinched hysteresis loops (PHLs) and exhibits synaptic plasticity, highlighting its applicability in non-volatile memory and neuromorphic applications.

This study introduces a new floating memtranstor emulator that utilizes four differential voltage current conveyors (DVCCs), one multiplier, and grounded passive components [46]. This design provides several benefits, including a decreased number of components, improved bandwidth, lower power consumption, and a compact form factor. The emulator has been validated through extensive PSPICE simulations utilizing 0.18 μm CMOS technology. It exhibits characteristics such as pinched hysteresis loops, memory behavior, and adaptability to incremental and decremental modes, demonstrating its potential for applications in neuromorphic and chaotic systems. For applications involving artificial synapses and

multilevel nonvolatile memory [47], the Cu/P(VDF-TrFE)/Ni-based organic memtranstor exhibits promising performance without needing a DC magnetic bias. Compared to traditional ferroelectric memories and memristors, it demonstrates reduced energy usage owing to its nondestructive reading reliant on the magneto-electric voltage coefficient (αE). The writing energy predominantly originates from polarization switching in the P(VDF-TrFE) layer. This layer can be effortlessly scaled to nanoscale thicknesses, facilitating device downsizing—the adaptable architecture of the organic memtransistor positions it as a formidable contender for forthcoming wearable electronics.

2.1 Research gaps

Although there has been notable progress in mem-element emulation, current designs encounter constraints regarding complexity, tunability, frequency range, and practical application. Various circuits depend on numerous active and passive components, resulting in design complexity and area utilization. The challenge of high-frequency operation persists, as most designs are confined to lower MHz ranges. Although certain emulators provide electronic tunability, they frequently necessitate intricate biasing or supplementary control components. Moreover, numerous studies emphasize theoretical validation via simulations, yet they fail to deliver experimental verification for practical applications. Non-ideal effects, including temperature variations and process constraints, are frequently neglected, restricting practical feasibility. Furthermore, although grounded configurations are predominant, floating implementations are essential for sophisticated applications such as neuromorphic computing.

2.2 Objectives of the thesis

Based on the identified research gaps, the primary objectives of this report are:

1. **Creating a compact memcapacitor and memtranstor emulators**

   Construct a memcapacitor emulator utilizing minimal active and passive components to streamline circuit complexity and optimize area utilization.

2. **Improving frequency performance**

Confirm that the suggested circuit functions effectively at elevated frequencies, surpassing the constraints of current designs, thus making it appropriate for high-speed applications.

3. **Ensuring the practical implementation**

Confirm the proposed design through theoretical analysis and simulations to ensure its applicability in real-world scenarios.

2.3 Research methodology

To achieve the objectives, the following research methodology has been adopted:

1. The design specifications for the proposed circuit have been developed utilizing 180nm CMOS.
2. To confirm the proposed circuit's functionality, thorough analyses have been conducted.
3. The proposed circuit has undergone simulation with the LTspice tool, and its performance has been evaluated against existing circuits documented.

Chapter 3

Proposed mem-capacitor emulator using OTA and CDBA with its application

3.1 Introduction

Several memcapacitor emulators have been examined in recent research, demonstrating improvements in their design and functionality. This chapter presents a memcapacitor emulator that utilizes OTA, CDBA, and passive components, including the memristor, to comprehensively analyze its operational characteristics and constraints. The proposed design prioritizes electrical tunability, simplicity, less use of passive elements, and a wider operational frequency range. Proposed memcapacitor emulator displays pinched hysteresis loops at frequencies up to 2MHz, indicating its memory effect. Simulations were performed with the LTspice program with 180 nm CMOS technology.

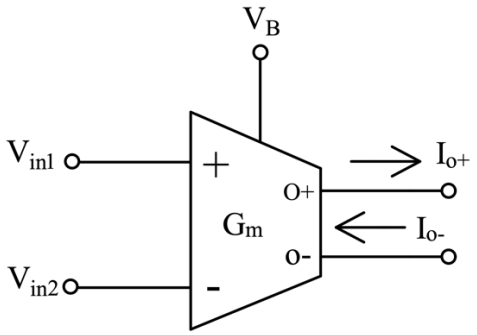
3.2 Characteristics of OTA and CDBA

Operational transconductance amplifier (OTA) and current differencing buffered amplifier (CDBA) are considered analog building blocks (ABBs) in analog circuit design. In this section, the characteristics of these components are defined for better understanding.

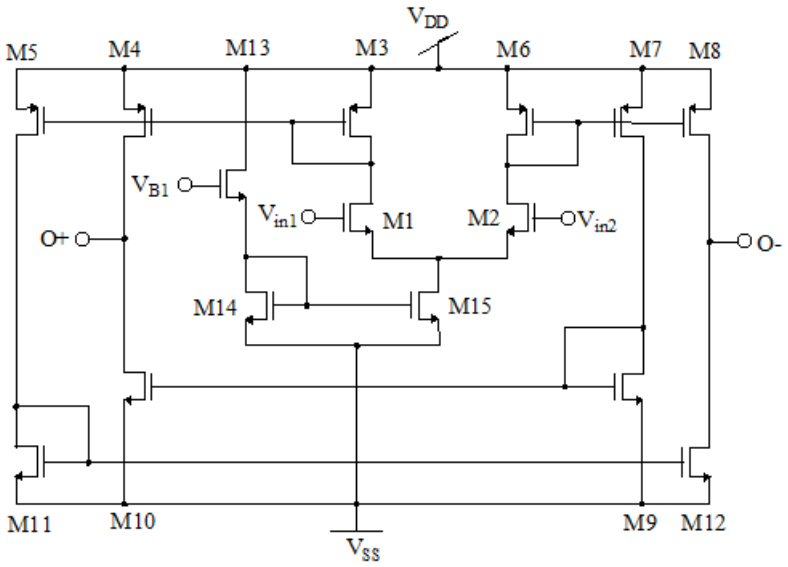
3.2.1 Operational transconductance amplifier (OTA)

Operational transconductance amplifier is an exceptionally adaptable electronic component commonly utilized in the realm of analog circuit design. One important electronically tunable parameter is the transconductance gain, or gm, which is the output current to input voltage ratio. Because of its tunability, OTAs can be used in various electronic circuits. Table 3.1 lists the aspect ratios of the MOSFETs utilised in OTA circuit design.

In adaptive systems, like the proposed memcapacitor circuit, the precise control of circuit parameters is essential, and their capacity to adjust gm renders them particularly advantageous. Figure 2 illustrates the symbol of an OTA alongside a corresponding circuit.



(a)



(b)

Figure 2. Operational transconductance amplifier (a) Symbol (b) Circuit Diagram

Table 3.1: Aspect ratios of MOSFETs (OTA)

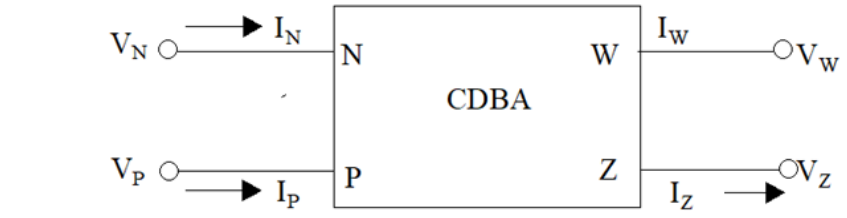
MOSFETs	W(µm)	L(µm)
M1-M2	16	1
M3-M8	9	1
M9-M12	4	1
M13	15	0.36
M14-M15	14	0.36

In this thesis, OTA is essential to implementing the memcapacitor emulator. Two operational transconductance amplifiers (OTAs), a resistor, a capacitor, and a current differencing buffered amplifier (CDBA) are other components used in the suggested design. This well-designed

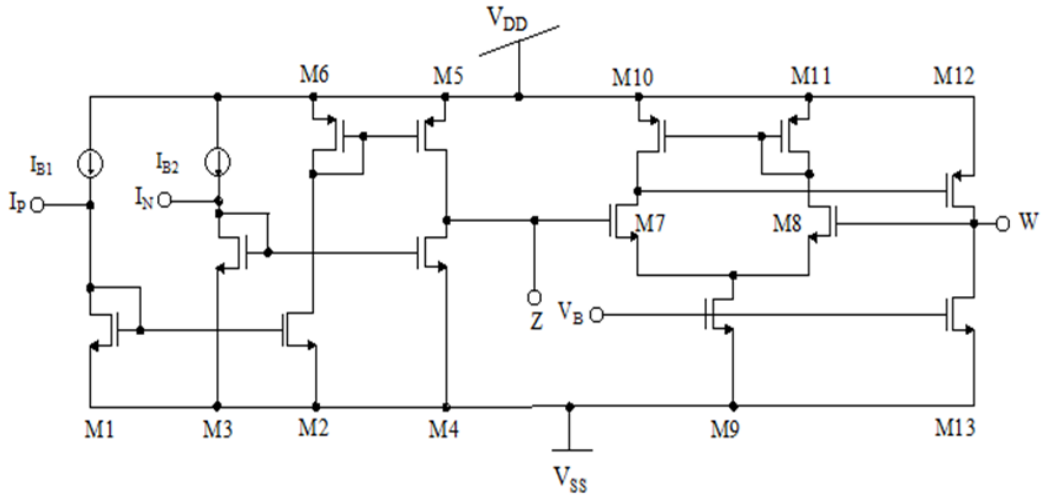
configuration allows for greater frequency response and tunable behavior, which reduces circuit complexity and improves performance. OTAs allow for a more practical, high-frequency alternative to traditional memcapacitor emulators, which require complex analog multipliers and operate in limited frequency ranges. OTAs are essential for the emulator's functionality and significantly contribute to low power, high performance memory based analog systems.

3.2.2 Current differencing buffered amplifier (CDBA)

A Current differencing buffered amplifier is a multi-terminal active component featuring two inputs and two outputs. It is a crucial element in analog circuit design, efficiently processing current and voltage signals while consuming the least power. With its low-impedance voltage output, the CDBA is widely used in modern electronics to create circuits that excel in performance and accuracy, particularly in analog and mixed signal applications.



(a)



(b)

Figure. 3 Current differencing buffered amplifier (a) Symbol (b) Circuit diagram

The circuit symbol for the current differencing buffered amplifier is illustrated in Figure 3(a). P and N symbolize the input terminals in this diagram, while W and Z indicate the output terminals. Figure 3(b) presents the circuit diagram of CDBA.

$$\begin{bmatrix} i_z \\ v_w \\ v_p \\ v_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_z \\ i_w \\ i_p \\ i_n \end{bmatrix}$$

The z-terminal is referred to as the current output because, as per the matrix equation above and the equivalent circuit depicted in Figure 3(a), the current flowing through it is equal to the difference between the currents flowing through the N and P-terminals; where P is the non-inverting and N is the inverting terminal. It is referred to as the voltage output since the voltages at the w and z-terminals are the same. When Ip and In flow through internally grounded input terminals, it is optimal for the input impedance of terminal P and terminal N to be zero internally. Table 3.2 lists the MOSFETs' aspect ratios in the CDBA circuit's design.

Table 3.2: Aspect ratios of MOSFETs (CDBA)

MOSFETs	W(µm)	L(µm)
M1-M4	32	2
M5-M6	42.5	0.36
M7-M8	0.8	0.5
M9, M12, M13	10	0.5
M10-M11	4	0.5

3.3 Working of the proposed memcapacitor emulator

The proposed emulator is composed of two operational transconductance amplifiers (OTAs) and a current-differencing buffered amplifier (CDBA). These components are interconnected to achieve the desired memcapacitive characteristics between the input voltage (Vin) and charge (q). Figure 4 presents the complete design of the proposed memcapacitor emulator.

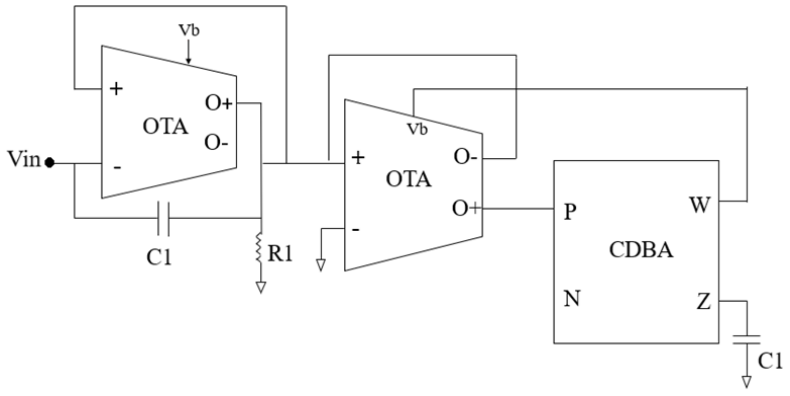


Figure 4. Proposed Memcapacitor Emulator using OTA and CDBA

3.4 Derivation of Memcapacitance of memcapacitor emulator

The circuit's analysis provides the following equations: 3.1-3.9.

From the circuit, start with the current equation:

$$I_{0+} = \pm g_m (V_1 - V_{in}) \tag{3.1}$$

The input voltage V_{in} Is given by:

$$V_{in} = V_{C_1} + V_{R_1}$$

Where:

$$V_{C_1} = \frac{q_{in}}{C_1}, \quad V_{R_1} = i_{in} R$$

Thus,

$$V_{in} = \frac{q_{in}}{C_1} + i_{in} R_1 + I_{0+} R_1 \tag{3.2}$$

Substituting I_{0+},

$$V_{in} = \frac{q_{in}}{C_1} + i_{in} R_1 + g_m (V_1 - V_{in}) R_1 \tag{3.3}$$

Substituting V_1, which is derived as:

$$V_1 = \frac{(g_m V_{in} M_R)}{(1 + g_m M_R)}$$

$$V_{in} = \frac{q_{in}}{C_1} + i_{in} R_1 - g_m V_{in} R_1 + g_m \frac{R_1 (g_m V_{in} M_R)}{1 + g_m M_R} \tag{3.4}$$

On factorizing V_{in},

$$V_{in} \left(1 + \frac{g_m R_1}{1 + g_m M_R}\right) = \frac{q_{in}}{C_1} + i_{in} R_1 \tag{3.5}$$

Rewriting:

$$V_{in} \left[\frac{1 + g_m M_R + g_m R_1}{1 + g_m M_R}\right] = \frac{q_{in}}{C_1} + i_{in} R_1 \tag{3.6}$$

$$V_{in} = \left[\frac{1 + g_m M_R}{1 + g_m M_R + g_m R_1}\right] \left[\frac{q_{in}}{C^1} + i_{in} R_1\right] \tag{3.7}$$

The inverse memcapacitance is defined as:

$$C_M^{-1} = \frac{V_{in}}{q_{in}}$$

$$C_M^{-1} = \left[\frac{1 + M_R g_m}{1 + M_R g_m + g_m R_1}\right] \left[\frac{1}{C_1} + \left(\frac{R_1}{q_{in}}\right) i_{in}\right] \tag{3.8}$$

$$C_M^{-1} = \frac{1 + M_R g_m}{C_1 (1 + M_R g_m + g_m R_1)} + \left(\frac{R_1 (1 + M_R g_m)}{1 + M_R g_m + g_m R_1}\right) \left(\frac{i_{in}}{q_{in}}\right) \tag{3.9}$$

Thus, we obtain the final expression for the inverse memcapacitance of the memcapacitor emulator circuit.

3.5 Simulation results of the proposed memcapacitor emulator design

This segment details the simulation outcomes of the proposed memcapacitor circuit, with all observations conducted utilizing LTspice. The design of memcapacitor integrates MOSFETs that leverage the parameters of the TSMC 180nm CMOS technology. The system has been supplied with a voltage of V_{DD}=0.9V and V_{SS}=-0.9V. The behavioral graphs of the proposed memcapacitor are generated utilizing capacitance values of C1 = 14pF and C2 = 4nF, with bias voltages established at V_{B1} = 0.7V and V_{B2} = -0.2V.

A key feature of memcapacitor is its capability to display a pinched hysteresis loop when exposed to a sinusoidal signal. The study starts by analysing the transient feature of the proposed memcapacitor emulator. The transient response is investigated by applying a sinusoidal input signal characterized by an amplitude of 300 mV and a frequency of 2 MHz to assess its memcapacitive behavior. The waveform demonstrates the phase shift between charge (q) and input voltage (v), thereby validating the capacitive characteristics of the proposed circuit, as displayed in Figure 5.

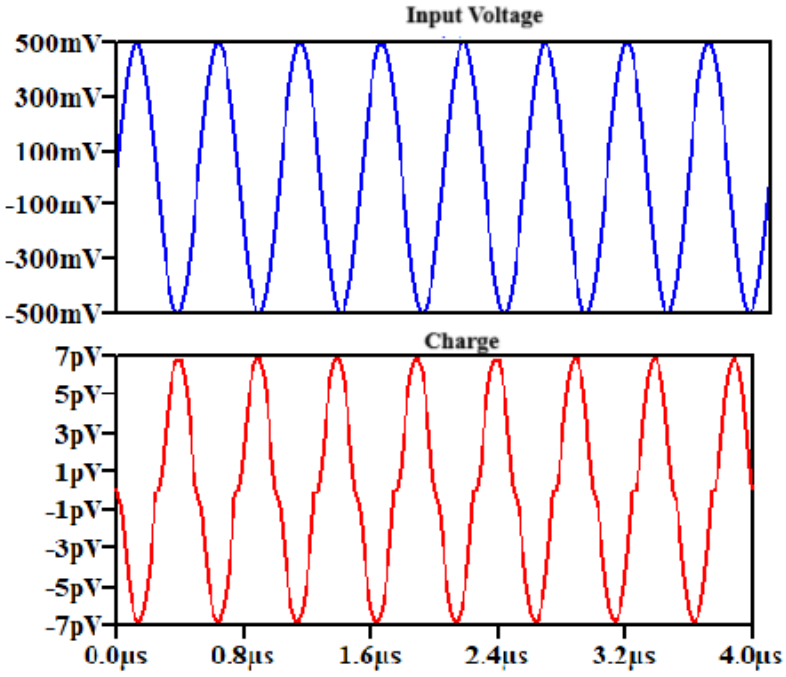


Figure 5. Transient response curves for proposed memcapacitor emulator

The proposed memcapacitor demonstrates a significant characteristic referred to as the pinched hysteresis loop when analysed under a sinusoidal signal in the charge (q) versus voltage (v)

plane. Figure 6 presents the output obtained by applying a sinusoidal signal with a 2 MHz frequency and a 300 mV amplitude to the memcapacitor emulator.

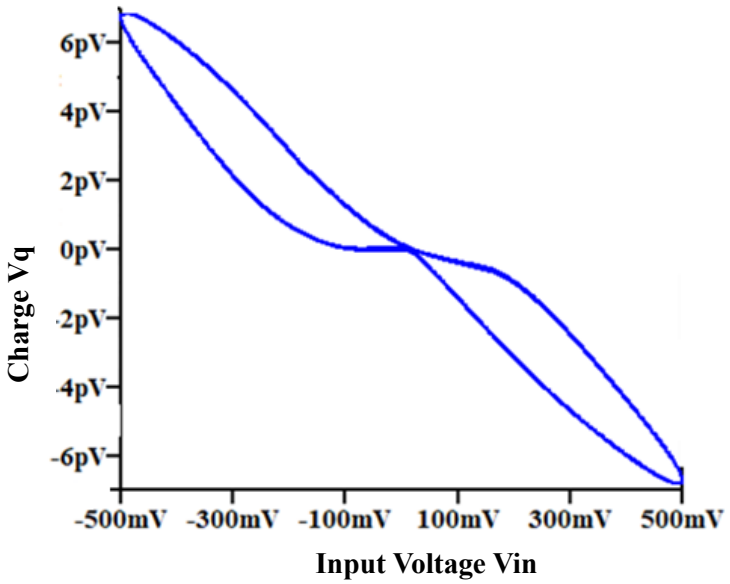


Figure 6. Pinched hysteresis loop of the memcapacitor

The performance of temperature variations across the range of -50 to +50 °C is illustrated in Fig. 7. The simulation results indicate that the formation of PHL is maintained up to a frequency of 2 MHz, and the designed memcapacitor emulator also demonstrates satisfactory performance under varying temperature conditions.

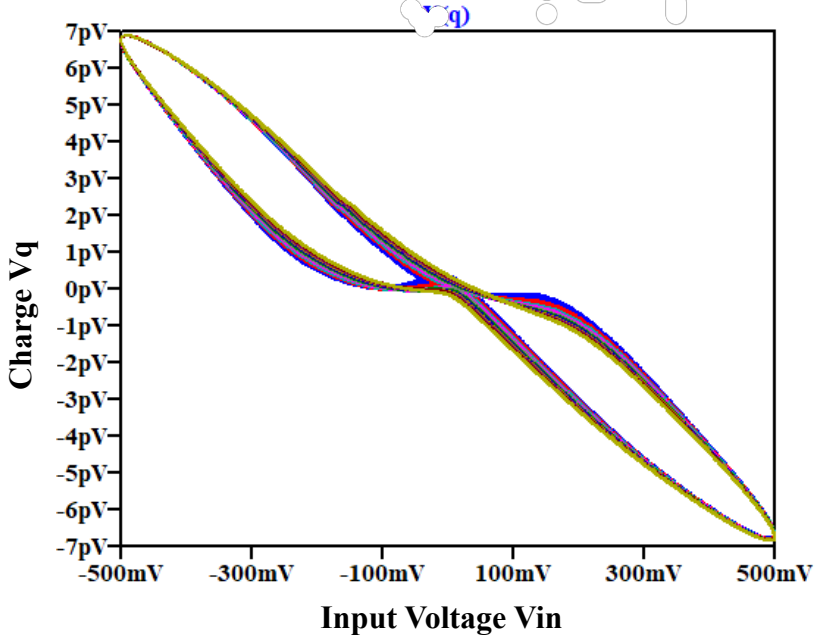


Figure 7. Effect of temperature on PHL decremental memtranstor emulator

Non-volatile behavior is a fundamental characteristic of memcapacitors. Upon application of a pulse signal, the memcapacitor is projected to modify its state during the ON phase and maintain its value during the OFF phase. A pulse signal with 20 mV amplitude, an ON duration of 45 µs, and an OFF duration of 10 µs is utilized to assess this property. The memcapacitance is determined by calculating the charge (q) ratio to the input voltage, as illustrated in Figure 7. The figure demonstrates that the memcapacitance exhibits stability during the OFF phase, while it exhibits a linear increase throughout the ON phase. This statement affirms the non-volatile characteristics of the proposed memcapacitor emulator.

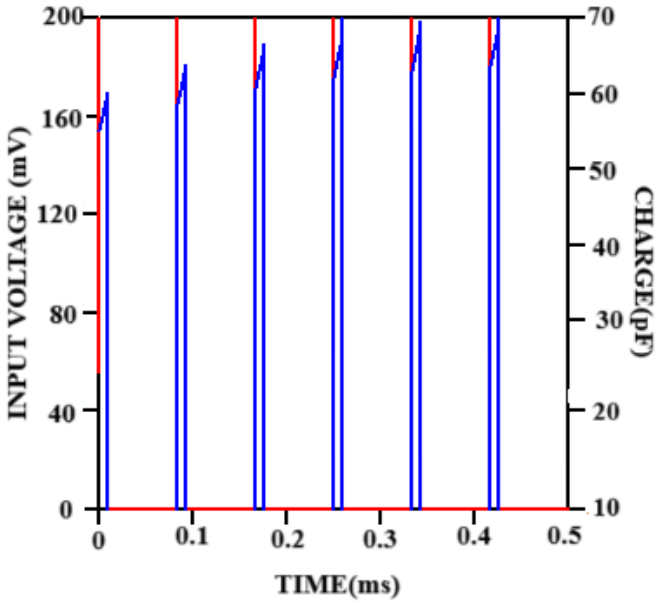


Figure 8. Non-volatile behavior of the proposed memcapacitor emulator

3.6 Chaotic oscillator circuit using the proposed memcapacitor emulator using OTA and CDBA

This segment uses the proposed memcapacitor emulator circuit to design a chaotic oscillator. One of the elementary electrical circuits that exhibits chaotic behaviour is Chua's circuit. Chaotic oscillators possess several uses, encompassing machine defect detection, secure communication, noisy signal production, and weak amplification. Incorporating mem-elements into Chua's circuit modifies its dynamic characteristics, influencing attractor configurations, bifurcation patterns, and responsiveness to initial conditions. The memory embedded in mem-

elements adds complexity, frequently leading to more elaborate attractors and increasing the circuit's reliance on its historical states.

A chaotic oscillator created using the suggested memcapacitor emulator is depicted in Figure 8. An inductor (L), two capacitors (C1 and C2), a resistor (R1), and a negative resistor (−R2) make up the oscillator circuit. An operational amplifier is used to create the negative resistance. The Op-Amp-based (AD711) negative resistor supplying energy to the system allows the circuit to sustain constant oscillations. The value of Rb is selected to match the resistance R2. Due to proper component value tuning, complex, non-repetitive waveforms are produced when the circuit enters a chaotic regime. The voltages across the capacitors (Vx and Vy) and the currents passing through the memcapacitor (I_{MC}) and the inductor (I_L) are key state variables that define the system's dynamic behavior.

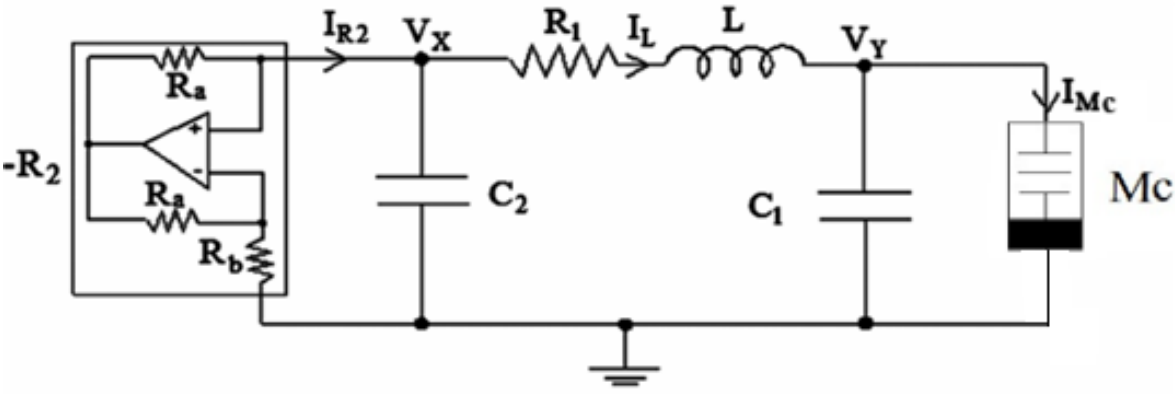
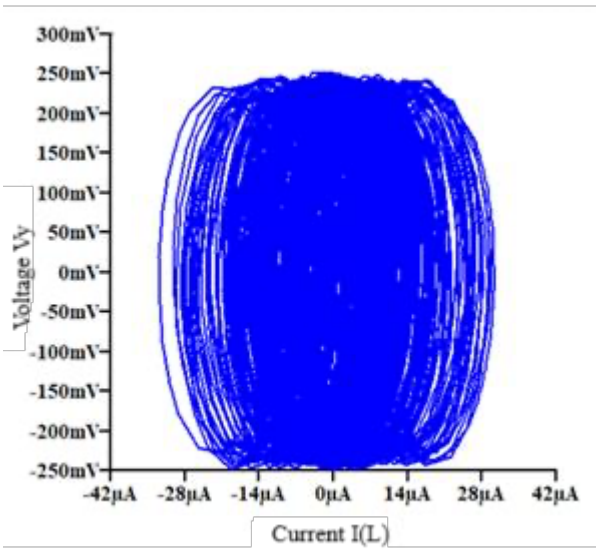


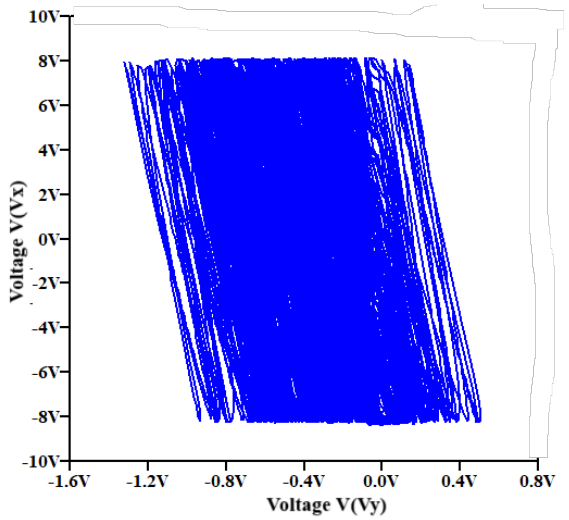
Figure 9. Chua's chaotic circuit using the proposed memcapacitor emulator

The circuit seen in Figure 9 has been observed in LTspice with passive element values chosen as L = 250 mH, R1 = 500 Ω, C1 = 200pF, C2 = 100nF, Ra1 = 1kΩ, and Rb2 = 1kΩ. The Op-Amp's (AD711) positive and negative supply voltages for realizing the negative resistor (-R2) were set as ±15V. The figure displays the mecapacitor-chaotic oscillator simulation results obtained for different space trajectories, which are (a) IL-Vy and (b) IL-Vx, and (c) Vx-Vy, respectively.

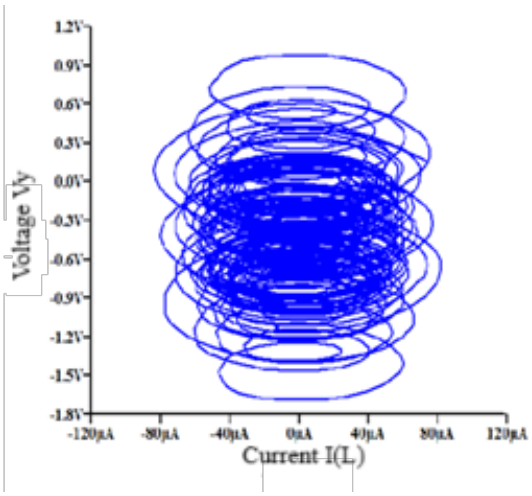
The results obtained by simulation for the memcapacitor-based chaotic oscillator are shown in Figure 10. Figure 10(c and d) shows the variation in the graphs between voltage and current for different parameters.



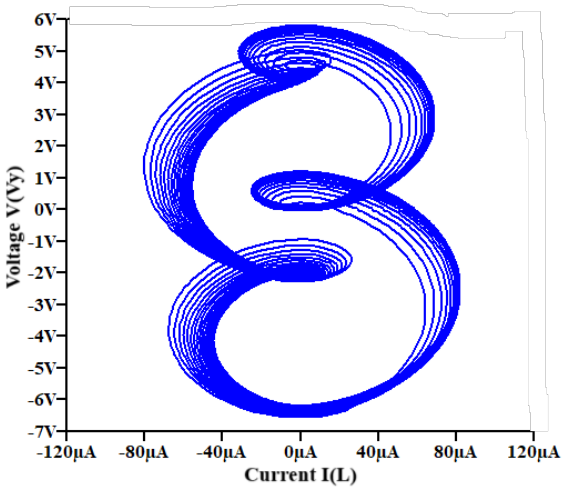
(a) IL-Vx



(b) Vx-Vy



(c) IL-Vy



(d) IL-Vy

Figure 10. Outputs of the chaotic circuit configured with the proposed memcapacitor (a) IL-Vx, (b) Vx-Vy, (c and d) IL-Vy

3.7 Conclusion

The simulation outputs validate the efficiency of the proposed memcapacitor emulator, which was developed utilizing TSMC 180 nm CMOS technology and executed in LTspice. The transient analysis confirms the memcapacitive behavior by examining the observed phase shift between charge and voltage. The PHL in the charge and voltage plane, derived from sinusoidal excitation, confirms its characteristic response. The results confirm that the proposed design is appropriate for implementation-based applications.

The emulator's non-volatile characteristics are evidenced by its capability to maintain state during the OFF phase of a pulse input. The stable memcapacitance response demonstrates its suitability for non-volatile memory applications. The results indicate that the proposed memcapacitor emulator exhibits key characteristics appropriate for integrating analog computing, neuromorphic systems, and emerging memory technologies.

Chapter 4

Proposed mem-transtor using current conveyor and voltage differencing current conveyor with its application

4.1 Introduction

A memtranstor is a newly introduced nonlinear memory component that expands the category of mem-elements, which also comprises memristors, memcapacitors, and meminductors. Conceptually described in 2015 and implemented in hardware in 2016, the memtranstor is a passive component with two terminals that exhibits a memory-dependent relationship between magnetic flux (ϕ) and electric charge (q) and is defined as follows.

$$\Phi(t) = MT \left[\int_{t0}^{t} q(t) d\tau \right] q(t) \tag{4.1}$$

The inverse of memtranstance in the flux- driven mode can be written below.

$$M_T^{-1}\, \rho(t) = \frac{q(t)}{\phi(t)} \tag{4.2}$$

Where ρ is the time integral of ϕ and is defined as the

$$\rho(t) = \int_{-\infty}^{t} \phi(t) dt \tag{4.3}$$

The memtranstor differs from conventional components that establish a relationship between voltage and current, such as resistors, capacitors, and inductors. It functions through magnetoelectric (ME) coupling, a phenomenon observed in specific materials where an electric field can affect magnetic properties, and vice versa. The memtranstor demonstrates nonlinear and history-dependent behavior, whereby the present input and previous excitations influence the current response.

When exposed to sinusoidal input, pinched hysteresis loops (PHLs) emerge in the ϕ–q plane, demonstrating the distinctive behavior of memtranstors. Depending on the internal states and arrangement, the loops may be slanted figure-eight curves or butterfly-shaped. Physical memtranstors are not yet commercially available and need complex material systems. In this work, we use standard circuit components such as voltage differencing current conveyors (VDCC) and current conveyors (CCII) to develop memtranstor emulators to work around this

restriction. Without sophisticated material production, the emulators enable the analysis and integration of real memtranstors into functional electronic systems by faithfully simulating their electrical behavior.

4.2 Characteristics of CCII and VDCC

Second-generation current conveyor (CCII) and voltage differencing current conveyor (VDCC) are considered analog building blocks (ABBs) in analog circuit design. In this section, the characteristics of these components are defined for better understanding.

4.2.1 Second-generation current conveyor (CCII)

The second-generation current conveyor is a crucial analog component widely utilized in the design of high-frequency and high-speed circuits. Known for its improved performance in analog signal processing applications, the development is an improvement over the first-generation current conveyor. The CCII uses three terminals: Y, the voltage input; X, the voltage follower; and Z, the current output. As equation (4.4) illustrates, the voltages measured at terminals X and Y are equal.

$$V\mathrm{y} = V\mathrm{x} \tag{4.4}$$

The current entering terminal Y is zero, equation (4.5)

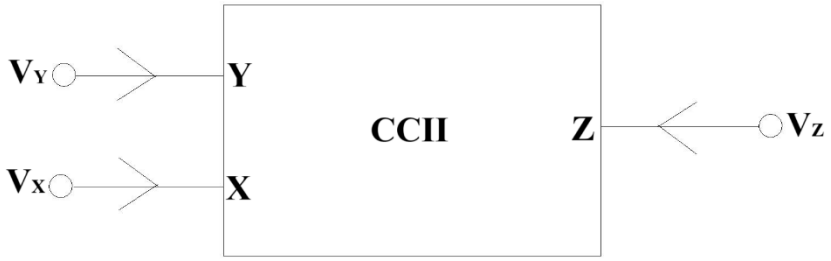
$$I\mathrm{y} = 0 \tag{4.5}$$

According to equations (4.6) and (4.7), respectively, the current at terminal Z is either the same as the current at terminal X or the opposite of the current entering terminal X.

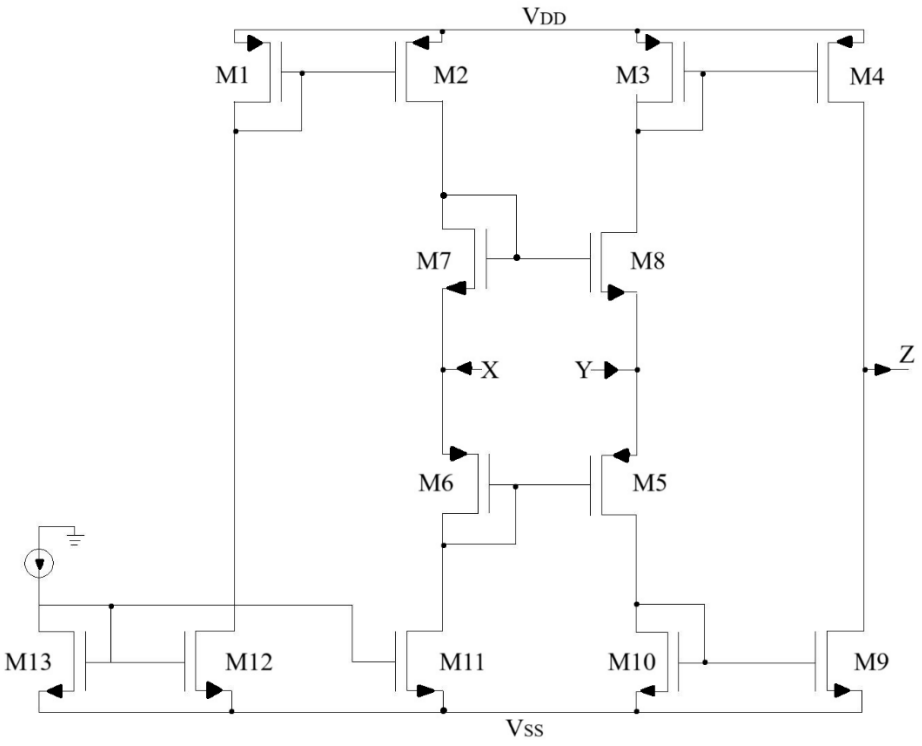
$$I\mathrm{x} = I\mathrm{z} \quad (\mathrm{CCII+}) \tag{4.6}$$

$$I\mathrm{z} = -I\mathrm{x} \quad (\mathrm{CCII–}) \tag{4.7}$$

Figure 11 shows the electrical symbol and comparable circuit for CCII. And, Table 4.1 lists the aspect ratios of the MOSFETs utilised in CCII circuit design.



(a)



(b)

Figure 11. Second Generation Current Conveyor (a) Symbol (b) Circuit diagram

Table 4.1: Aspect ratio of MOSFETs (CCII)

MOSFETs	W(µm)	L (µm)
M1-M6	0.54	54
M7-M8	0.54	7.92
M12	0.54	21
M9, M11, M12	0.54	13.68

4.2.2 Voltage differencing current conveyor (VDCC)

The voltage differencing current conveyor is a six-terminal analog building block that combines the functions of a voltage differencing unit and a current conveyor. The terminals with the designations N and P are input terminals for differential voltage. W_N and W_P are the output terminals, and Z and X are the intermediate processing terminals. Except for terminal X, which exhibits low impedance characteristics, all terminals show increased input impedance. The input currents at terminals N and P are ideally zero, as shown in equation (4.8),

which permits only voltage differences (Vp and Vn) to be applied across these terminals as given in equation (4.9).

$$I_N = I_P = 0 \quad (4.8)$$

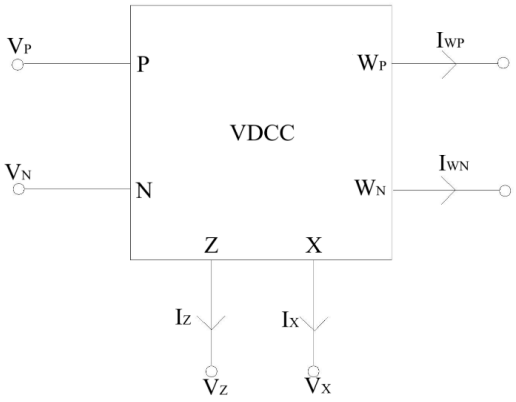
$$I_Z = G_m (V_P - V_N) \quad (4.9)$$

An external impedance connected at terminal Z receives a corresponding voltage (Vz) from the current generated by this differential voltage. The voltage is then subsequently conveyed to the X terminal. The current at terminal X (Ix) is imitated to both output terminals W_P and W_N, yielding a positive and negative version of the current, respectively, as shown in equations (4.10) and (4.11). The symbol and internal circuit configuration of the VDCC are commonly shown in circuit diagrams to convey its operational behavior effectively and are presented in Figure 12. And, Table 4.2 lists the MOSFETs' aspect ratios in the VDCC circuit's design

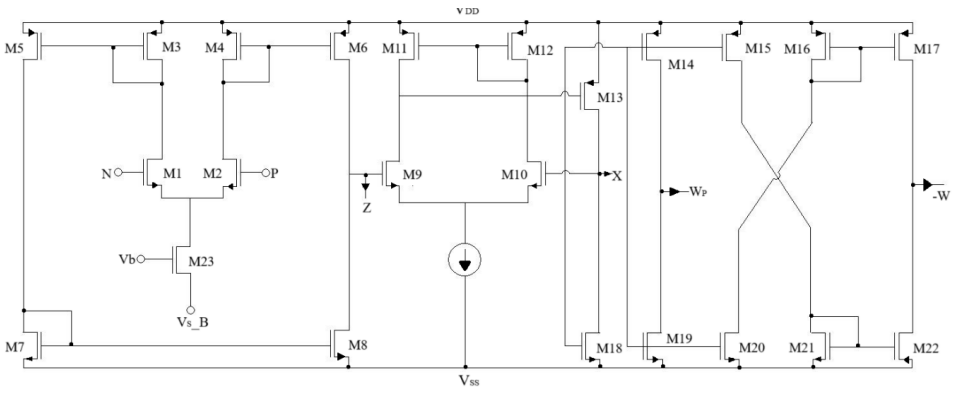
$$V_Z = V_X \quad (4.10)$$

$$I_{WN} = -I_X, \; I_{WP} = I_X \quad (4.11)$$

$$g_m = k(V_B - V_{S\_B} - V_{TH}) \quad (4.12)$$



(a)



(b)

Figure 12. Voltage differencing current conveyor (a) Symbol (b) Circuit diagram

Table 4.2: Aspect ratios of MOSFETs (VDCC)

MOSFETs	W(µm)	L(µm)
M1-M4	1.8	3.6
M4-M6	1.8	7.2
M7-M8	1.8	2.4
M9-M10	0.72	3.06
M11-M12	0.72	9
M13-M17	0.72	14.4
M18-M22	1.72	0.72
M23	1.8	3.6

4.3 Working of proposed memtranstor emulator

The proposed emulator comprises two second-generation current conveyors (CCII's), a voltage-differencing current conveyor (VDCC), three capacitors, and three resistors. These components are interconnected to achieve the desired memtranstor characteristics between the magnetic flux (φ) and electric charge (q). Figure 13 represents the complete design of the proposed memtranstor emulator. In this proposed emulator, passive components like three resistors and capacitors have been used.

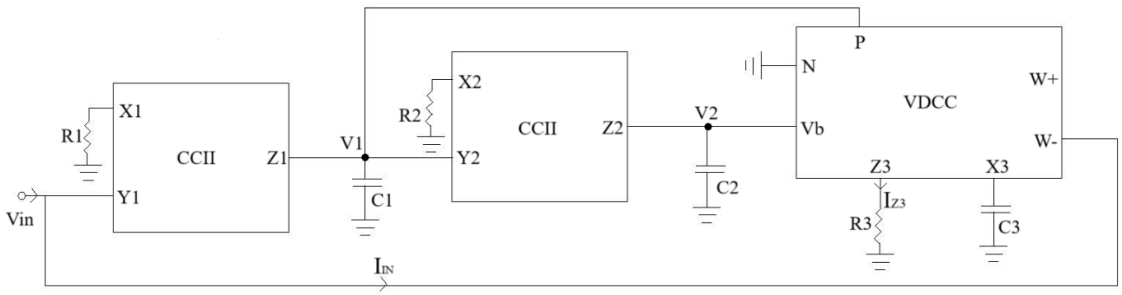


Figure 13. Proposed memtranstor emulator using CCII and VDCC

4.4 Derivation of memcapacitance of memtranstor emulator

The circuit's analysis provides the following equations: 4.13-4.22. From the circuit, we start with the current equation:

$$V_1 = \frac{1}{C1}\int \frac{Vin}{R1}dt = \frac{1}{C1\,R1}\phi in(t) \tag{4.13}$$

$$V_2 = \frac{1}{C1C2R1R2}\int \phi \text{in(t)}dt = \frac{1}{C1C2\,R1R2}\rho in \tag{4.14}$$

$$I_Z = gm.V_1 \tag{4.15}$$

$$V_{Z3} = I_{Z3}.R_3 \tag{4.16}$$

Thus, $$V_{X3} = V_{Z3} = \frac{R3k}{C1}\left[\frac{R_{31}}{C1C2R1R2}\ \rho(t) - \ Vx\right] \phi \text{ in} \tag{4.17}$$

$$V_{X3} = \frac{R3k}{C1}\left[\frac{1}{C1C2R1R2}\ \rho in(t) - \ Vx\right] \phi \text{ in} \tag{4.18}$$

$$I_{X3} = I_{C3} = C_3.\ \frac{d.Vx}{dt} \tag{4.19}$$

$$Iin = -\ I_W = I_{X3} \tag{4.20}$$

Thus, $$qin = CV_{x3} = \frac{C3R3k}{C1R1}\left[\frac{1}{C1C2R1R2}\ \rho in(t) - \ Vx\right] \phi \text{ in} \tag{4.21}$$

$$M_T^{-1} = \frac{qin}{\phi \text{in}} = \frac{C3R3k}{C1R1}\left[\frac{1}{C1C2R1R2}\ \rho in(t) - \ Vx\right] \tag{4.22}$$

Thus, we obtain the final expression for the inverse memtranstance of the memtranstor emulator circuit.

4.5 Simulation results of the proposed design of the memtranstor emulator

Simulation results of the proposed memtranstor emulator circuit are shown, with LTspice used to generate all outputs. The memtranstor design incorporates MOSFETs that utilize TSMC 180 nm CMOS technology parameters. The system has been supplied with a voltage of V_{DD} = 1.2V and V_{SS} = -1.2V. The characteristic graphs of the proposed memtranstor are generated utilizing capacitance values of C1 = 550pF, C2 = 50pF, C3 = 30pF, and resistance values of R1 = 120Ω, R2 = 150Ω, R3 = 2kΩ, with bias voltages configured at Vb = -0.9V. A key feature of the memtranstor is its capacity to demonstrate a PHL when exposed to a sinusoidal signal. Figure 14 illustrates the transient analysis of the proposed memtranstor.

The study starts by analysing the transient feature of the proposed memtranstor emulator. The transient response is investigated by applying a sinusoidal input signal characterized by an amplitude of 650 mV and a frequency of 1 MHz to assess its memtransitive behaviour. The waveform demonstrates the phase shift between voltages of V(C1) (q) and V(C3) (ϕ) with respect to time, thereby validating the characteristics of the proposed circuit, as depicted in

Figures 15 and 16. This waveform shows a sinusoidal-like waveform with different amplitudes and phases.

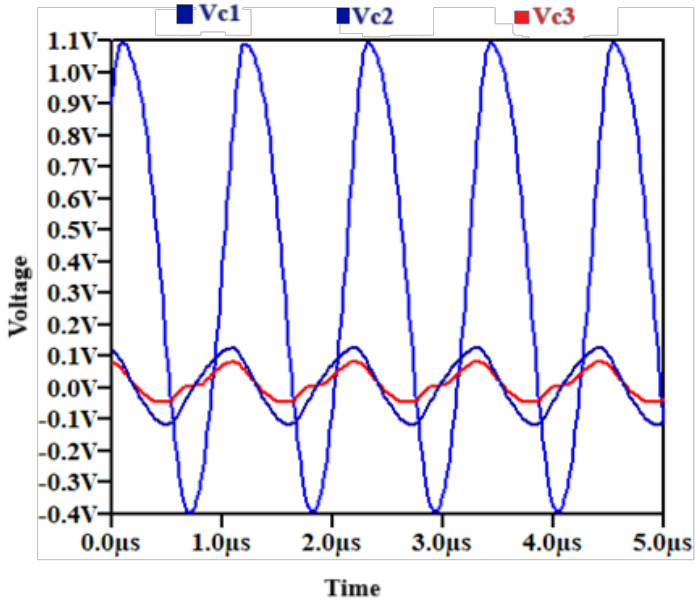


Figure 14. Transient analysis of proposed memtranstor emulator

The proposed memtranstor exhibits a key feature known as the pinched hysteresis loop (PHL) when subjected to a sinusoidal signal in the charge (q) vs. magnetic flux (ϕ) plane. The proposed incremental and decremental memtranstor emulator design is simulated in the LTspice tool using the TSMC 180nm CMOS technology model file.

In the proposed design, the input terminals of the VDCC are exchanged to transform a decremental memtranstor emulator into an incremental memtranstor emulator. For incremental and decremental type memory emulators, respectively. Figures 15a to 15f present the response obtained for increment circuits, whereas Figure 16a to 16f shows decrement circuits by applying a sinusoidal input signal with 600kHz to 1.5MHz of frequency and 600 mV of amplitude to the memtranstor emulator. Figures demonstrate how the continuous loop area for pinched hysteresis plots significantly shrinks as the frequency rises. As a result, the suggested memtranstor emulator circuits confirm the memtranstive system's fingerprint properties.

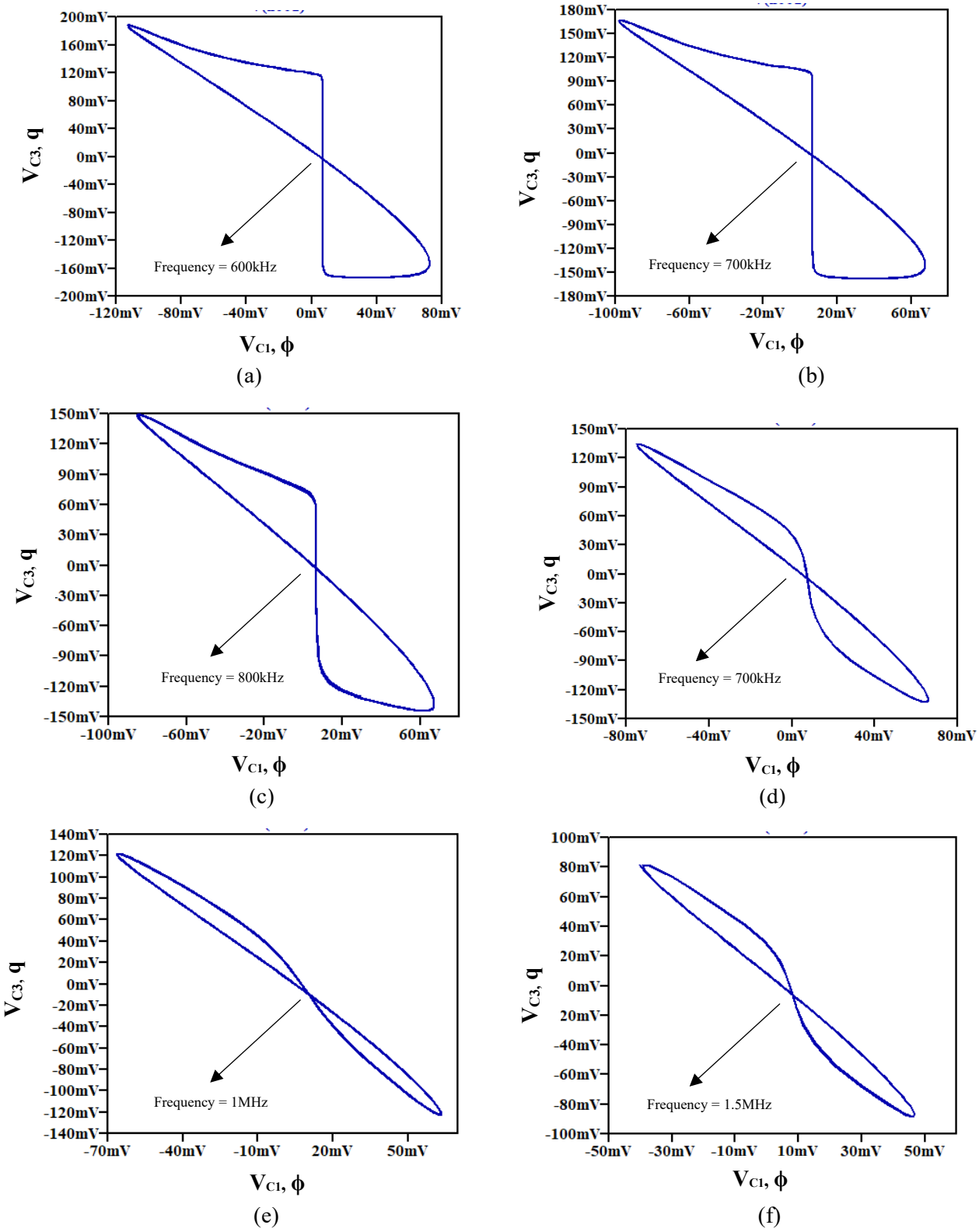


Figure 15 (a-f). PHL for the proposed Incremental type memtranstor emulator. **a** 600kHz; **b** 700 kHz; **c** 800 kHz; **d** 900 kHz; **e** 1 MHz; **f** 1.5 MHz

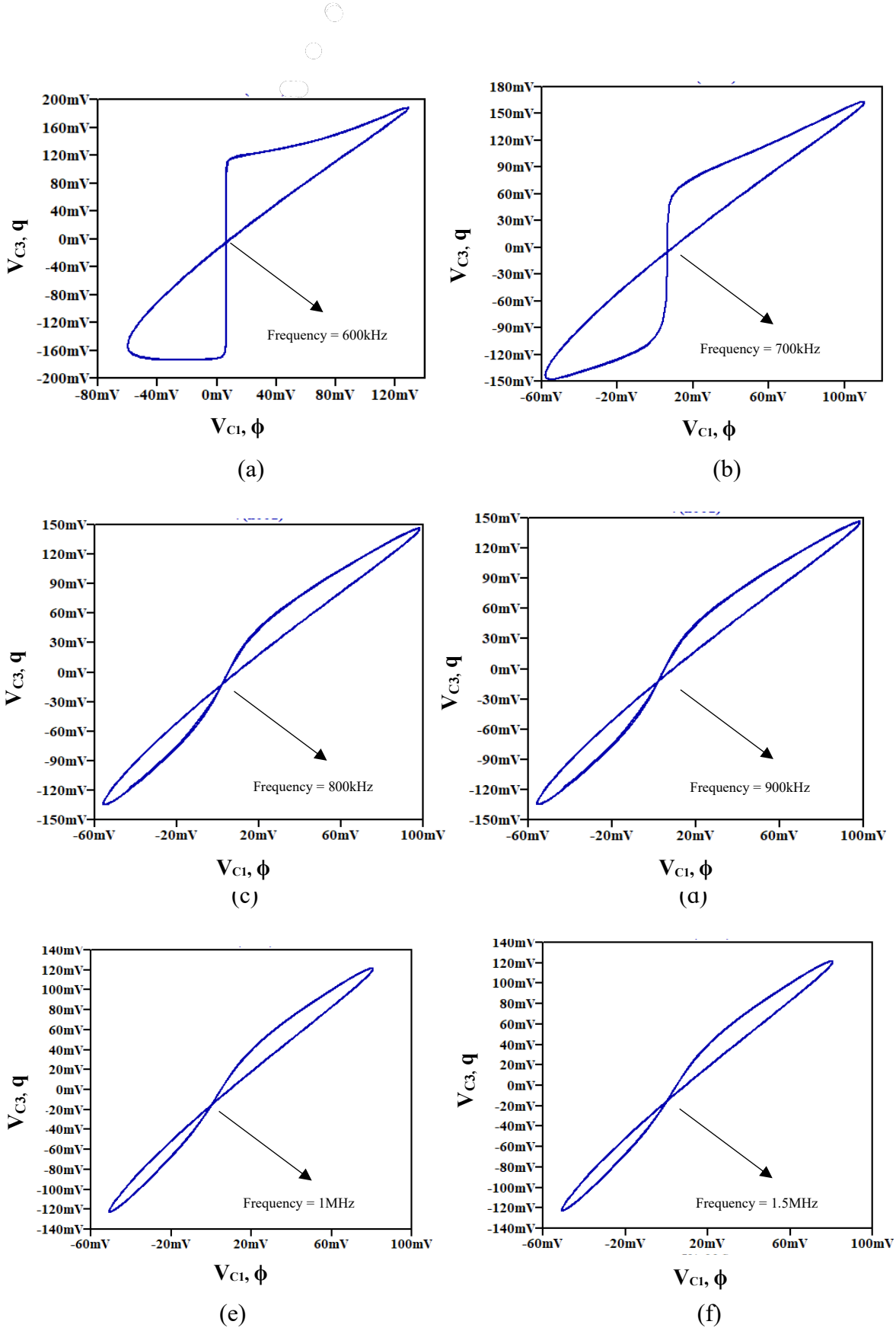


Figure 16 (a-f). PHL for the proposed decremental type memtranstor emulator. **a** 600kHz; **b** 700 kHz; **c** 800 kHz; **d** 900 kHz; **e** 1 MHz; **f** 1.5 MHz

The performance of temperature variations across the range of -40 to +40 °C is illustrated in Fig. 17. The simulation results indicate that the formation of PHL is maintained up to a frequency of 1.5 MHz, and the designed memtranstor emulator also demonstrates satisfactory performance under varying temperature conditions.

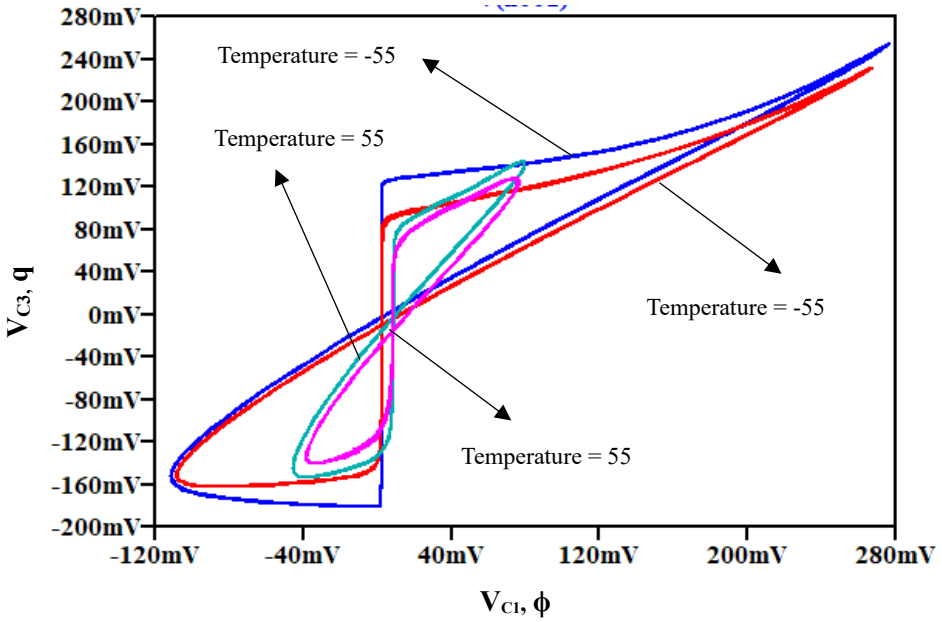


Figure 17. Effect of temperature on PHL decremental memtranstor emulator

4.6 Chaotic oscillator circuit using the proposed memtranstor emulator using CCII and VDCC

A chaotic oscillator circuit is designed using the proposed memtrastor emulator circuit shown in Figure 18. The chaotic oscillator comprises a negative resistor, a resistor, an inductor, two capacitors, and a nonlinear component called a memtrastor. The circuit gets the energy it needs to maintain the oscillations from the negative resistor, which comprises three resistors and an op-amp (AD711). The circuit shown in Figure 16 can produce chaotic oscillations with various paths by selecting suitable passive element parameters.

With flux (Φ), integral of flux (ρ) of memtranstor, the state variables are chosen as the inductor current (IL) and the capacitor voltages VC1 and VC2. The system's state equations in Figure 18 are as follows:

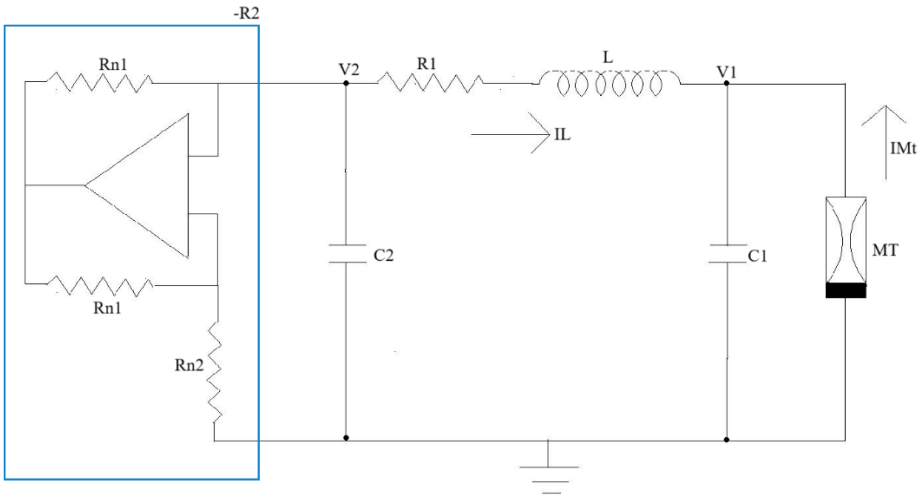


Figure 18. Chaotic oscillator circuit based on the proposed memtranstor emulator.

$$\frac{d.V1}{dt} = \frac{IL}{C1} - \frac{IMT}{C1} \quad (4.23)$$

$$\frac{d.V2}{dt} = \frac{VC2}{C2R2} - \frac{IL}{C2} \quad (4.24)$$

$$\frac{d.IL}{dt} = \frac{V2-R1I1-V1}{L} \quad (4.25)$$

Further considering, Φin = ∫Vin.dt, ρin = ∫φin dt, and using the equation of the inverse of the memtranstance equation (4.22), it can be rewritten as,

$$C1\frac{d.V1}{dt} = \text{IL - IMT} \quad (4.26)$$

$$C2\frac{d.V2}{dt} = \frac{VC2}{R2} - IL \quad (4.27)$$

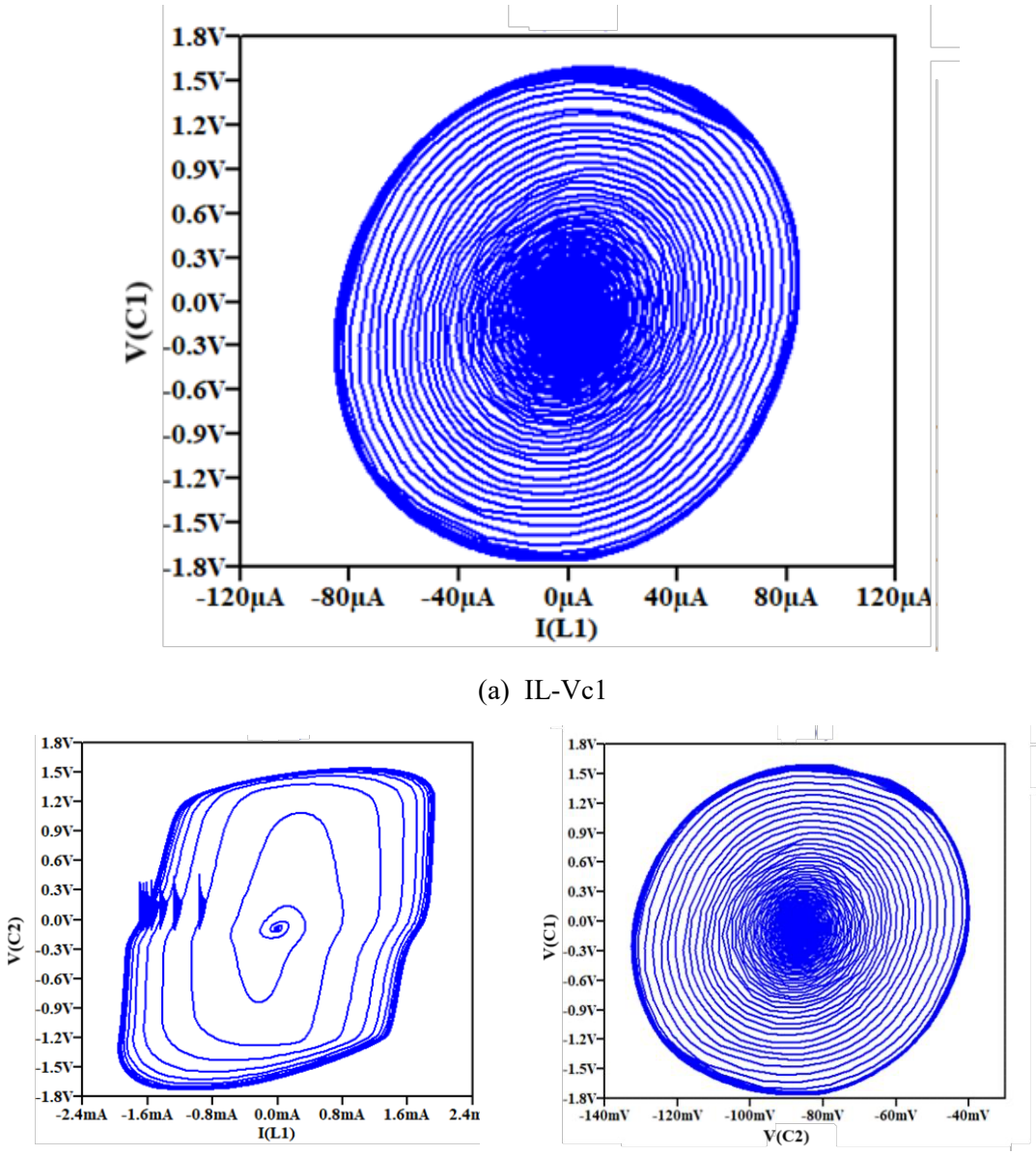
Thus, $$\frac{d.\Phi}{dt} = \text{V1} \quad (4.28)$$

And, $$\frac{d.\rho}{dt} = \Phi \quad (4.29)$$

C1 and C2 are the capacitances, L is the inductance, whereas R1 and R2 denote the resistance values of the corresponding elements of the chaotic oscillator.

The passive element values used for the memtranstor in the LTSPICE simulations of the chaotic system shown in Figure 19 were chosen as mentioned earlier. The circuit's remaining passive components were configured with L = 120 mH, R1 = 100 Ω, C1 = 10 nF, and C2 = 100 nF. Rn1 = 1 kΩ and Rn2 = 500Ω were the values assigned to the resistors of the negative impedance converter (NIC). The op-amp "AD711" SPICE macro model was used in the NIC circuit, and the positive and negative supply voltages were set to ±15 V. Figure 19a–c and Figure 20a-c

plot the graphs that illustrate the spiral attractor plots of the space trajectories for IL-Vc1, IL-Vc2, and Vc1-Vc2, respectively.

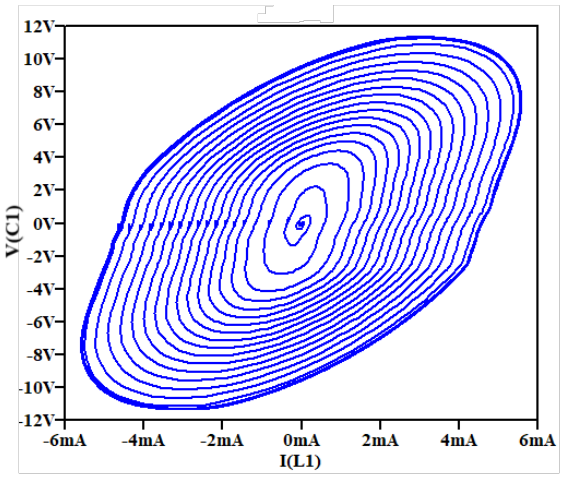


(a) IL-Vc1

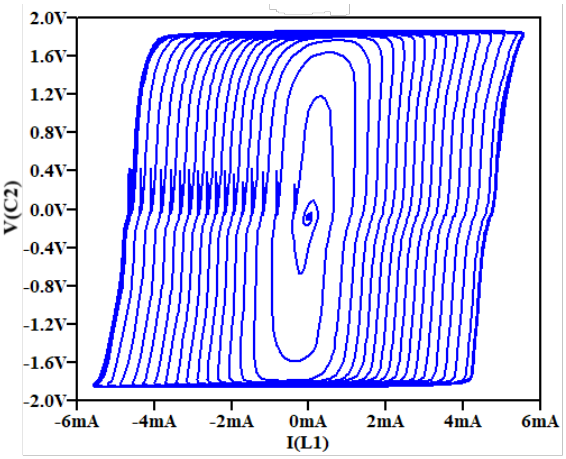
(b) IL-Vc2

(c) Vc1-Vc2

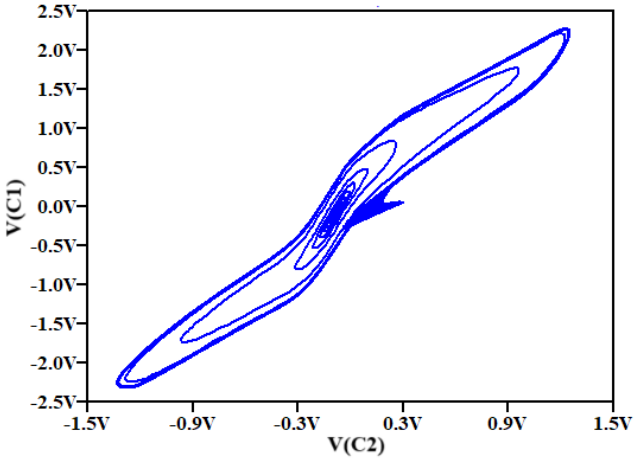
Figure 19. The spiral attractor plots for the designed chaotic oscillator with proposed memtranstors (a) IL-V1, (b) IL-V2, and (c) V1-V2



(a) IL-Vc1



(b) IL-Vc2



(c) Vc1-Vc2

Figure 20. The spiral attractor plots for the designed chaotic oscillator with proposed memtranstors (a) IL-Vc1, (b) IL-Vc2, (c) Vc1-Vc2

4.7 Conclusion

The memtranstor, as a novel fourth mem-element, presents significant potential to enhance nonlinear circuit functionalities via its unique φ–q relationship. This work presents the design of a floating memtranstor-emulator utilizing active components, specifically current conveyor II and voltage differencing current conveyor, in conjunction with grounded passive elements. The emulator demonstrates electronic adjustability, non-volatility, and power-efficient operation by using CMOS technology of 0.18 nm.

Circuit underwent thorough validation via extensive simulations, including pinched hysteresis loops (PHLs), frequency variation, confirming its accurate memtranstance behavior. The emulator supports incremental and decremental memory effects, increasing its applicability.

The design has been effectively employed to illustrate chaotic oscillations, indicating its appropriateness for advanced applications including neuromorphic systems, adaptive learning, and nonlinear dynamic systems. The proposed memtranstor emulator, equipped with versatile features, establishes a robust foundation for next-generation memory, logic, and chaos-based computing architectures.

Chapter 5
Conclusion and future scope

To sum up, this research has shown how significant the memelement emulator is in replicating the actual memelement. A memcapacitor emulator using an OTA, memristor-emulator, grounded capacitor, and resistor has been proposed and analyzed. The circuit successfully exhibits key memcapacitive characteristics, including nonlinear charge-voltage behavior, pinched hysteresis loops, and non-volatile memory effects. The simulation findings, obtained by LTspice utilizing TSMC 180nm CMOS technology variables, validates the anticipated execution of the suggested design.

The transient and frequency response analyses confirm the circuit's ability to emulate memcapacitive behavior over a wide frequency range. Additionally, the non-volatile property is verified by applying a pulse signal, demonstrating its capability to retain state information even after input removal. These features make the proposed memcapacitor emulator a strong candidate for applications in neuromorphic computing, non-volatile memory, and reconfigurable analog circuits.

Overall, the designed memcapacitor emulator provides a simple yet effective approach for studying and implementing memcapacitive systems, opening the way for further research and practical applications in next-generation electronics.

In parallel, a memtranstor emulator using two current conveyors (CCII) and a VDCC and other passive elements has also been proposed and analysed. Using TSMC 180 nm CMOS technology in LTspice, the proposed memtranstor emulator exhibits encouraging performance. Transient analysis confirms its memtranstive nature, which shows a clear phase shift between magnetic flux and charge. A ‘PHL’ in the charge–flux plane under sinusoidal excitation for 0.7 MHz to 1.5 MHz frequency further confirms its distinctive behavior. Furthermore, as the state-space trajectories demonstrate, the emulator effectively displays important chaotic characteristics, including attractors and sensitivity to initial conditions, when incorporated into a chaotic oscillator circuit. These results make the emulator a compelling contender for hardware implementation. The findings support its applicability to chaotic systems, neuromorphic designs, and analog computing.

In the next phase of this research, extensive modeling will be executed to validate the functionality of the proposed memcapacitor emulator and memtranstor emulator. To assess its robustness under parametric variations, these simulations will include non-volatility testing (for memtranstor), temperature variation studies, and Monte Carlo simulations.

With continued nanotechnology and circuit design advancements, OTA and CDBA-based memcapacitor emulators hold immense potential for next-generation computing, secure communication, and adaptive electronics. Dynamic tunability and low-power optimization will enhance scalability. For memtranstor, more study into CCII and VDCC-based designs could facilitate high-frequency and compact implementations. Future research can focus on miniaturization, CMOS integration, and hardware implementations to make these circuits viable for commercial applications.

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