Design of Fully Self Bias Continuous Time CMOS Bandpass Gm-C Filter

A Thesis Submitted in partial fulfillment of the requirements for the award of degree of

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in

VLSI Design & CAD

Submitted by

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CERTIFICATE

I hereby certify that the work which is being presented in this thesis entitled, **"Design of Fully Self Bias Continuous Time CMOS Bandpass Gm-C Filter"** submitted in partial fulfillment of the requirements for the award of degree of **Master of Technology** in **VLSI Design & CAD** at **Thapar University, Patiala,** is an authentic record of my own work carried out under the supervision of **Ms. Alpana Agarwal, Assistant Professor** and refers other researcher's work which are duly listed in reference section.

The matter embodied in this thesis has not been submitted for the award of any other degree of this or any other university.

Vaibhav Bagla.

Date: 14.07.2009 **(Vaibhav Banga)**

This is to certify that the above statement made by the candidate is correct and true to best of my knowledge.

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ABSTRACT

The present work addresses the design of fully self biased continuous-time CMOS bandpass Gm-C filter using a design methodology based on the g_m/I_D transistor characteristics. This analog module was analyzed, designed and prototyped in TSMS 0.35µm CMOS technology. Experimental results are presented, in order to validate the methodology. The filter has a pass-band central frequency of about 5.011MHz, quality factor of 19.28, Gain of 23.48 dB at center frequency and a current consumption of 288.48 µA. The circuit does not have need of any DC external biasing circuit, only need to apply V_{DD} (3.3 V). Here self biasing has been introduced with power consumption of 952µW. The results have been taken with load variations, temperature variations, power supply variations and process corner variations, LVS and PEX have been generated from the layout. This circuit used in real time high frequency applications as in RF communication.

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LIST OF ABBREVIATION

1. **OTA –** Operational Transconductance Amplifier
2. **CMFB –** Common Mode Feedback
3. **HDD –** Hard Disk Drive
4. **P-P –** Peak to Peak
5. **GB –** Giga Byte
6. **CM –** Common Mode
7. **ICMR –** Input Common Mode Range
8. **SR –** Slew Rate
9. **Q –** Quality Factor
10. $\mathbf{G_{CM}}$ **–** Common Mode Transconductance
11. $\mathbf{G_{DM}}$ **–** Differential Mode Transconductance

CHAPTER 1

INTRODUCTION

The development of ultra-scaled VLSI technologies, coupled with the demand for more signal processing integrated in a single chip, has resulted in a tremendous potential for design of analog circuits. Most VLSI systems require analog sub-systems such as amplifiers, comparators, filters, oscillators, digital-to-analog and analog-to-digital converters. Most often the target technology process imposes design tradeoffs, some of them taken based on designer's experience with the target technology to achieve a successful analog design. More critical in deep sub-micron CMOS mixed-signal ICs are the specifications of analog circuits that are sensitive to the random variations of the size and technology parameters. This work focuses on the analysis, design and implementation of a continuous-time band-pass Gm-C filter using the g_m/I_D design method. In this method, we consider the relationship between the g_m/I_D ratio and the normalized drain current I_D/(W/L) as a fundamental design information to explore in the design space. In several analog blocks [1, 2], including the Gm-C filter, were designed using this methodology. Preliminary simulation results shows that a conventional design approach (using first-order Spice level 1 transistor models) achieves a similar performance with similar area, hence incurring in much larger power dissipation than that obtained in the g_m/I_D design method. The process parameters were obtained through the library files of TSMC 0.35μm CMOS technology.

1.1 Current Trends in Filter Design

A CMOS 140-mw fourth-order continuous-time low-pass filter stabilized with a Class AB common-mode feedback operating at 550 MHz, the growing demand of portable electronic equipment and system-on-a-chip has been pushing the industry toward the design of circuits with lower power supply voltages and lower power consumption. The hard-disk drive (HDD) industry is looking for developments in read channel chips to push data rates to a higher speed, along with low power and low cost solutions. The main

requirements for the continuous-time filter are high speed, small group delay variations, good linearity, and high power efficiency. Storage devices have been divided on the basis of their performances typically specified in terms of the access time to the stored data, and cost/megabyte. Cost-sensitive applications like data distribution and entertainment music use devices like CD-ROM, which have high access time and are low price.

Tape storage and backup systems use lower performing systems. HDD systems are high-performance systems and near real time applications [1, 3]. HDD systems continue to develop at a rapid and deterministic pace to meet the emerging demands of high-performance computing and peripheral devices. As a rule of thumb, for data rates up to 1 Gb/s, we need a filter whose cutoff frequency is at least 550 MHz in low pass filter and 5 MHz in Band Pass filter. However, designing filters operating at these frequencies in pure CMOS process is a big challenge, especially in 0.35 μm CMOS technology, with f_t limited to 15 GHz for N-type devices, is employed.

In the previous generations of HDD, a seventh-order linear phase filter was used; most of the magnitude and phase equalizations were done in the analog design [2, 6]. A modern approach uses a fifth-order filter for magnitude equalization, while further equalization is done in the digital domain [7]. High speed has been achieved by minimizing the parasitics and using a complementary input stage operational transconductance amplifier(OTA); the use of complementary differential pairs allows us to reduce the power consumption. A common-mode feedback (CMFB) based on a Class AB amplifier that ensures stability at high frequencies has been developed. The parasitic poles of the CMFB loop are minimized, and the inherent positive excess phase introduced by a couple of zero-pole pairs improves its phase margin. The power consumption of CMFB circuitry is less than 50% of OTA's power. The filter has center frequency of 5 MHz achieved along with Quality factor of 25 and the Boost of 22 DB at Center frequency. The power consumption of the 5 MHz bandpass filter is 900 mW from supply voltages of 3.3 V.

1.2 Organization of Thesis

The thesis has been organized to provide design perspective for circuit techniques for high frequency filters with boost.

The focus has been kept on the analysis of the new techniques and the issues like power, bandwidth and boost have been touched.

Chapter II of this thesis analyzes previously reported types of filters, basic filter frequency responses, filter architecture, quality factor, g_m/I_D technology, OTA, common mode feedback with the aim of finding causes of power efficiency loss in different approaches. This also forms the basis of deriving a new and power-efficient architecture.

Chapter III outlines the design implementation of transconductors as basic building blocks. Different considerations regarding the design of core and boost transconductors (OTAs) are discussed. And application of OTA as a basic element for the filter, with constant input and output parasitic, is illustrated.

In Chapter IV the simulation results for AC, Transient and DC analysis with Load, Temperature and Power Supply variation have shown.

Chapter V elaborates on the Layout Design with LVS and PEX report. It is shown that the reported solution is the most power efficient structure with the highest boost and bandwidth, with self biasing, in the class of filters with similar dynamic range.

In Chapter VI conclusions and future directions are presented.

CHAPTER 2

LITRETURE SURVEY

2.1 Types of Filters

In signal processing, the function of a filter is to remove unwanted parts of the signal, such as random noise, or to extract useful parts of the signal, such as the components lying within a certain frequency range. The following block diagram illustrates the basic idea.

Fig 2.1 Signal Processing

There are two types of filter, analog and digital. They are quite different in their physical makeup and in how they work.

2.1.1 Analog Filters

An analog filter uses analog electronic circuits made up from components such as resistors, capacitors and op amps to produce the required filtering effect. Such filter circuits are widely used in such applications as noise reduction, video signal enhancement, graphic equalizers in hi-fi systems, and many other areas.

There are well-established standard techniques for designing an analog filter circuit for a given requirement. At all stages, the signal being filtered is an electrical voltage or

current which is the direct analogue of the physical quantity (e.g. a sound or video signal or transducer output) involved.

(a) Important Classes of Analog Filters

The class of a filter refers to the class of polynomials from which the filter is mathematically derived. The order of the filter is the number of filter elements present in the filters ladder implementation. Generally speaking, the higher the order of the filter, the steeper the cut-off transition between passband and stopband. Filters are often named after the mathematician or mathematics on which they are based rather than the discoverer or inventor of the filter [7].

i) Butterworth filter: Butterworth filters are described as maximally flat, meaning that the response in the frequency domain is the smoothest possible curve of any class of filter of the equivalent order. The Butterworth class of filter was first described in a 1930 paper by the British engineer Stephen Butterworth after whom it is named. The filter response is described by Butterworth polynomials, also due to Butterworth.

ii) Chebyshev filter: Chebyshev filters are analog or digital filters. A Chebyshev filter has a faster cut-off transition than a Butterworth, but at the expense of there being ripples in the frequency response of the passband. There is a compromise to be had between the maximum allowed attenuation in the passband and the steepness of the cut-off response. This is also sometimes called a type I Chebyshev, the type 2 being a filter with no ripple in the passband but ripples in the stopband. The filter is named after Pafnuty Chebyshev whose Chebyshev polynomials are used in the derivation of the transfer function.

iii) Cauer filter or Elliptical Filter: Cauer filters have equal maximum ripple in the passband and the stopband. The Cauer filter has a faster transition from the passband to the stopband than any other class of network synthesis filter. The term Cauer filter can be used interchangeably with elliptical filter, but the general case of elliptical filters can have unequal ripples in the passband and stopband. An elliptical filter in the limit of zero ripple in the passband is identical to a Chebyshev Type 2 filter. An elliptical filter in the limit of zero ripple in the stopband is identical to a Chebyshev Type 1 filter. An elliptical filter in the limit of zero ripple in both passbands is identical to a Butterworth filter. The

filter is named after Wilhelm Cauer and the transfer function is based on elliptic rational functions.

iv) Bessel filter: The Bessel filter has a maximally flat time-delay (group delay) over its passband. This gives the filter a linear phase response and results in it passing waveforms with minimal distortion. The Bessel filter has minimal distortion in the time domain due to the phase response with frequency as opposed to the Butterworth filter which has minimal distortion in the frequency domain due to the attenuation response with frequency. The Bessel filter is named after Friedrich Bessel and the transfer function is based on Bessel polynomials.

2.1.2 Digital Filters

A digital filter uses a digital processor to perform numerical calculations on sampled values of the signal. The processor may be a general-purpose computer such as a PC, or a specialized DSP (Digital Signal Processor) Chip. The analog input signal must first be sampled and digitized using an ADC (analog to digital converter). The resulting binary numbers, representing successive sampled values of the input signal, are transferred to the processor, which carries out numerical calculations on them. These calculations typically involve multiplying the input values by constants and adding the products together. If necessary, the results of these calculations, which now represent sampled values of the filtered signal, are output through a DAC (digital to analog converter) to convert the signal back to analog form. Note that in a digital filter, the signal is represented by a sequence of numbers, rather than a voltage or current. The following diagram Fig 2.2 shows the basic setup of such a system.

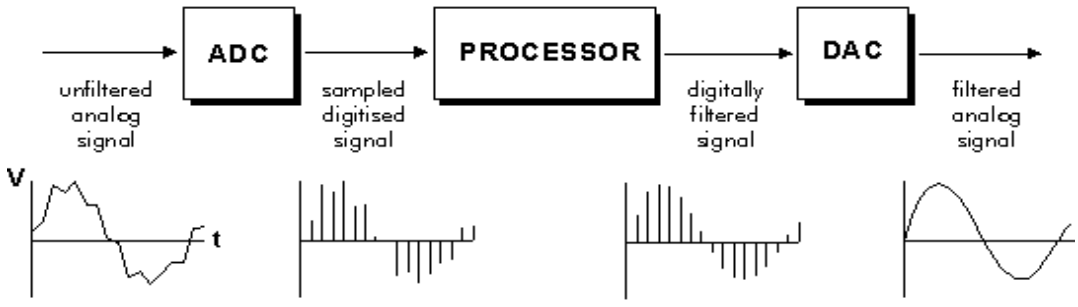


Fig 2.2 Basic setup for a digital filter

In electronics, computer science and mathematics, a digital filter is a system that performs mathematical operations on a sampled, discrete-time signal to reduce or enhance certain aspects of that signal. This is in contrast to the other major type of electronic filter, the analog filter, which is an electronic circuit operating on continuous-time analog signals. An analog signal may be processed by a digital filter by first being digitized and represented as a sequence of numbers, then manipulated mathematically, and then reconstructed as a new analog signal (see digital signal processing). In an analog filter, the input signal is "directly" manipulated by the circuit.

A digital filter system usually consists of an analog-to-digital converter (to sample the input signal), a microprocessor (often a specialized digital signal processor), and a digital-to-analog converter. Software running on the microprocessor can implement the digital filter by performing the necessary mathematical operations on the numbers received from the ADC. In some high performance applications, an FPGA or ASIC is used instead of a general purpose microprocessor.

Digital filters may be more expensive than an equivalent analog filter due to their increased complexity, but they make practical many designs that are impractical or impossible as analog filters. Since digital filters use a sampling process and discrete-time processing, they experience latency (the difference in time between the input and the response), which is almost irrelevant in analog filters.

Digital filters are commonplace and an essential element of everyday electronics such as radios, cellphones, and stereo receivers.

(a) Advantages of using digital filters

The following gives some of the main advantages of digital over analog filters.

1. A digital filter is programmable, i.e. its operation is determined by a program stored in the processor's memory. This means the digital filter can easily be changed without affecting the circuitry (hardware). An analog filter can only be changed by redesigning the filter circuit. Redesigning of a analog circuit is very tough task, it may create a lot of problems with achieved parameters.

2. Digital filters are easily designed, tested and implemented on a general-purpose computer or workstation.

3. The characteristics of analog filter circuits (particularly those containing active components) are subject to drift and are dependent on temperature. Digital filters do not suffer from these problems, and so are extremely stable with respect both to time and temperature.

4. Unlike their analog counterparts, digital filters can handle low frequency signals accurately. As the speed of DSP technology continues to increase, digital filters are being applied to high frequency signals in the RF (radio frequency) domain, which in the past was the exclusive preserve of analog technology.

5. Digital filters are very much more versatile in their ability to process signals in a variety of ways; this includes the ability of some types of digital filter to adapt to changes in the characteristics of the signal.

6. Fast DSP processors can handle complex combinations of filters in parallel or cascade (series), making the hardware requirements relatively simple and compact in comparison with the equivalent analog circuitry.

2.2 Basic Filter Frequency Responses

We distinguish the filters according to their frequency response as lowpass, highpass, bandpass, bandstop, allpass, and arbitrary frequency response (equalizers). The basic filter frequency responses are as follows [8].

2.2.1 Lowpass filter

The ideal response of a lowpass filter is shown in Fig. 2.3(a). All frequencies below the cutoff frequency ω_c pass through the filter without obstruction. The band of these frequencies is the filter passband. Frequencies above cutoff are prevented from passing through the filter and they constitute the filter stopband. However, for some reasons, the ideal lowpass filter response cannot be realized by a physical circuit. Instead, the

practical lowpass filter response will, in general, be as shown in Fig. 2.3(b). It can be seen that a small error is allowable in the passband, while the transition from the passband to the stopband is not abrupt. The width of this transition band $\omega_s - \omega_c$ determines the filter selectivity. Here ω_s is considered to be the lowest frequency of the stopband, in which the gain remains below a specified value.

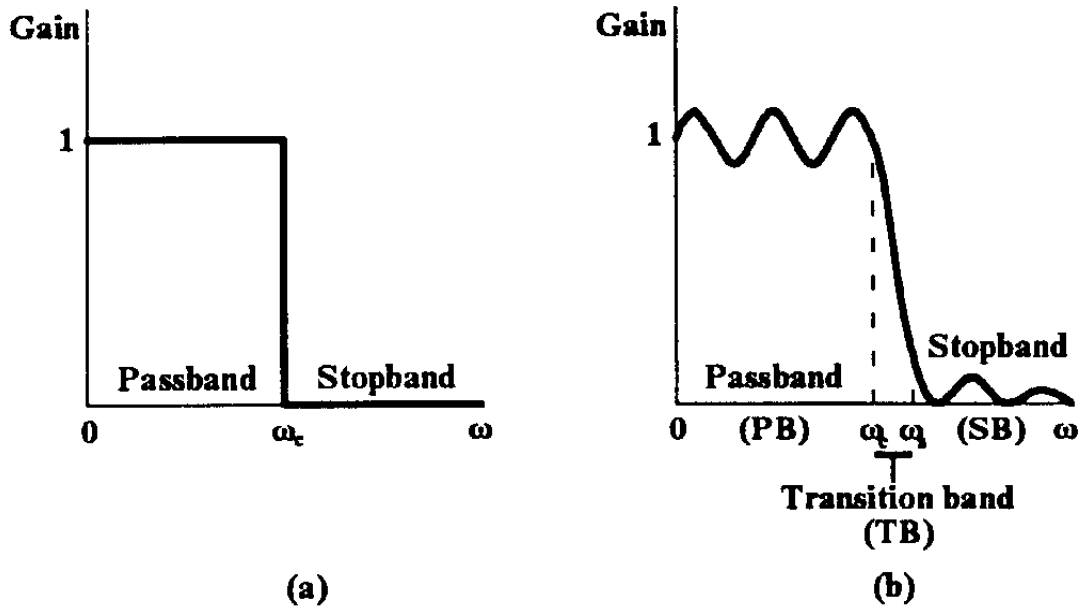


Fig. 2.3. (a) Ideal and (b) practical lowpass filter amplitude response [8]

2.2.2 Highpass filter

For reasons similar to those holding for the lowpass filter the ideal highpass filter response is unrealizable. The amplitude response of the practical highpass filter will basically be as shown in Fig. 2.4.

In the highpass filter the passband is above the cutoff frequency ω_c , while all frequencies below ω_c are attenuated when passing through the filter. A high-pass filter's task is just the opposite of a low-pass filter. To offer easy passage of a high-frequency signal and difficult passage to a low-frequency signal. As one might expect, the inductive and capacitive versions of the high-pass filter are just the opposite of their respective low-pass filter designs. The cutoff frequency for a high-pass filter is that frequency at which the output (load) voltage equals 70.7% of the input (source) voltage.

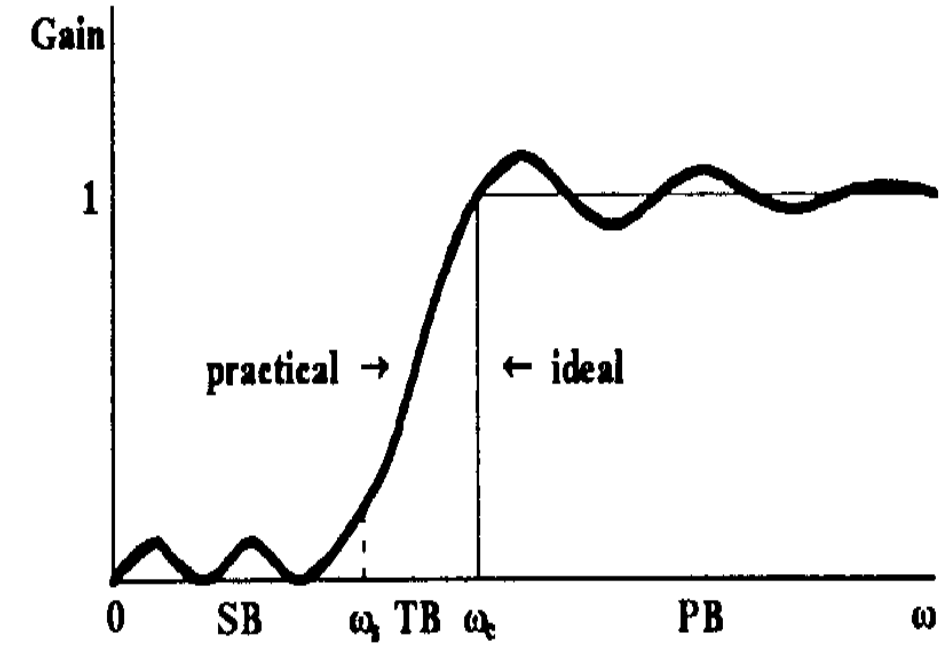


Fig. 2.4. The basic highpass ideal and practical filter amplitude response [8]

2.2.3 Bandpass filter

The ideal bandpass is again unrealizable and the amplitude response of the practical bandpass filter is as shown in Fig. 2.5. Here the passband lies between two stopbands, the lower and the upper. Accordingly there are two transition bands.

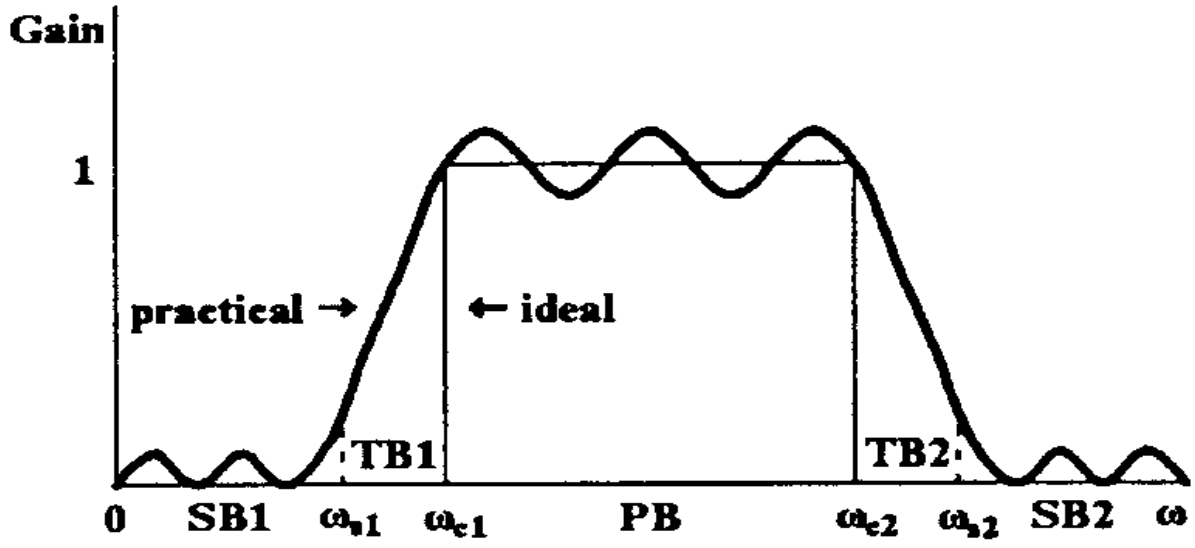


Fig. 2.5. Amplitude response of the ideal and practical basic bandpass filter [8]

2.2.4 Bandstop filter

The amplitude response of the practical band-elimination or bandstop filter is shown in Fig. 2.6, while its ideal response is again unrealizable. It can be seen that the filter possesses two passband separated by a stopband rejected by the filter. There are also two transition bands.

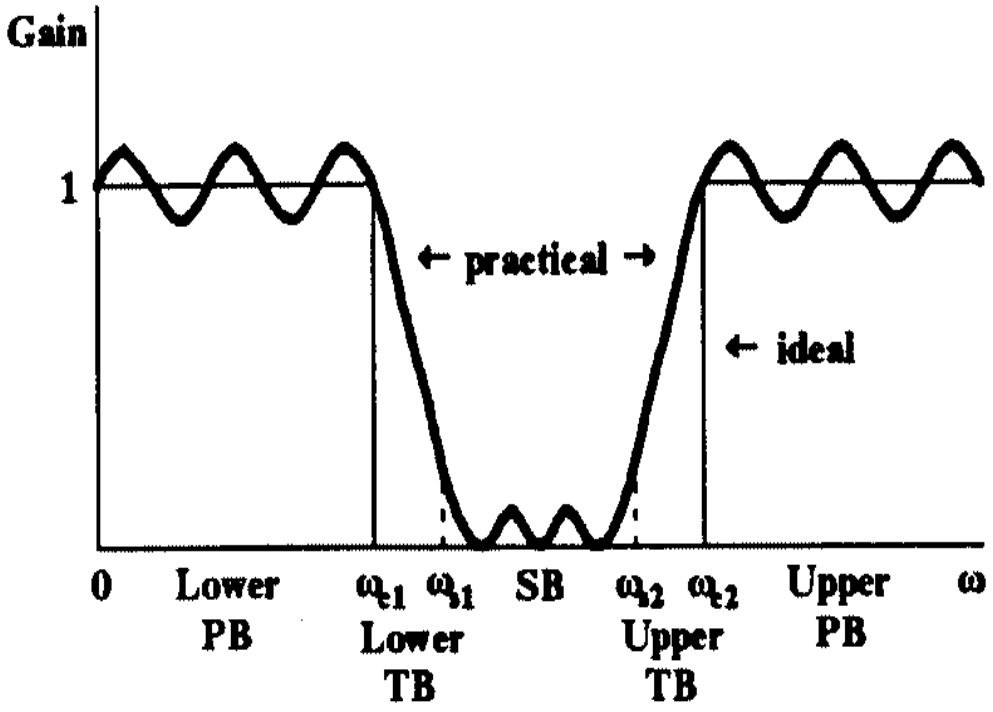


Fig. 2.6. Amplitude response of the ideal and practical basic bandstop filter [8].

2.2.5 Allpass filter

Ideally this filter passes, without any attenuation, all frequencies (0 to ∞), while its characteristic of concern is the phase response. If its phase response is linear, then it can operate as an ideal time delayer. In practice the phase can be linear, within an acceptable error, up to a certain frequency ω_c. For frequencies below ω_c the allpass filter operates as a delayer. It is useful in phase equalization.

It should be noted that allpass filters are not the only ones that may possess linear phase response. Certain lowpass filters also have similar phase response.

2.2.6 Amplitude equalizers

The amplitude equalizer has an amplitude response that does not belong to any of the filter responses considered above. It is used to compensate for the distortion of the frequency spectrum that the signal suffers when passing through a system. Its amplitude response is therefore drawn as complementary to the signal spectrum. In this sense it can be considered arbitrary being suitable for only one distorted signal.

2.3 Filter Architecture

2.3.1 Filter Architecture using OTA

Integrated continuous-time transconductance-C (Gm-C) filters have been widely used for several applications such as digital video, RF/IF filters, etc [9, 10]. Gm-C filters offer many advantages over other continuous-time filters in terms of low power and high frequency capability. The basic building block of a Gm-C filter is an integrator, basically a transconductor and a capacitor. The transconductors employed in these filters must be linear over the expected signal swing; hence the design of the transconductor is critical. Although high-frequency filters are the main aim of this topology [11], Gm- C filters can be used for integrated filters at low frequencies.

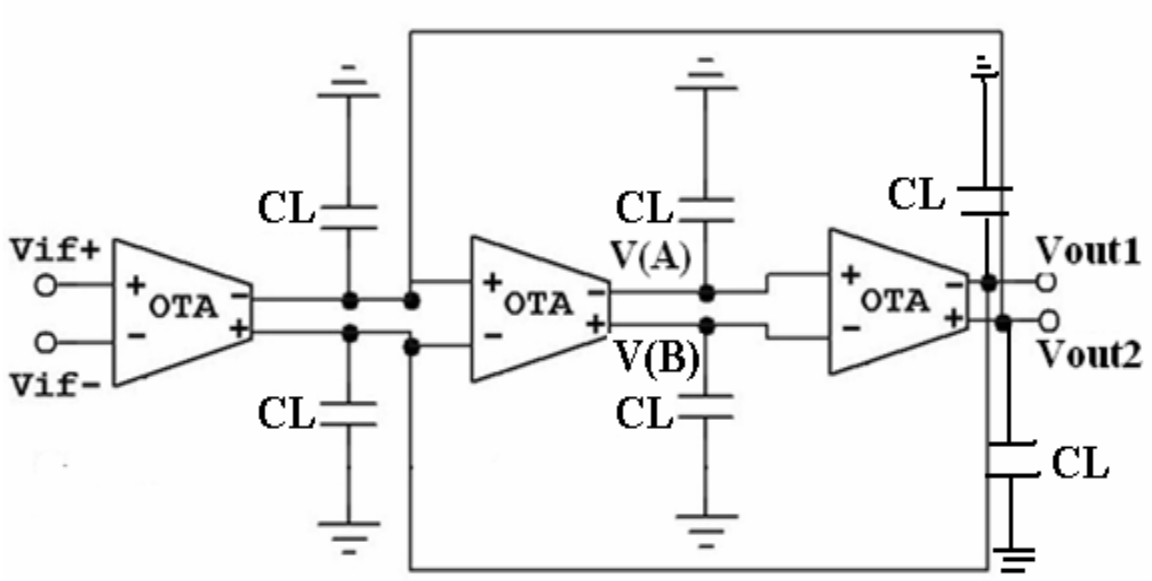


Fig. 2.7. A Gm-C band-pass biquad filter topology.

Fig 2.7 shows the fully-differential continuous-time Gm-C bandpass filter with a biquad circuit topology based on [5]. This topology was selected to provide a simple structure that demonstrates the capabilities of the technology and the filter design methodology.

2.3.2 Steps in Filter Design

Filter design, in effect, involves three separate processes or steps, these being [8]

1. Analysis of circuits

2. Curve approximation

3. Synthesis of the filter

These three steps are explained below to clarify matters.

1) Analysis of circuits—Conventionally, analysis of a circuit is the procedure to find the characteristics of the filter operation from its diagram and the values of its components. However, analysis of circuits has a more general meaning here, namely to determine general types of operational characteristics for various general types and orders of circuits. These characteristics may be formulated as rational functions of the complex frequency variables, with constraints depending on the circuit type. These rational functions will be referred to here as the permitted functions.

2) Curve approximation—Based on the knowledge of the characteristics and potentialities of the various types of circuits, we may proceed to try to find the solution of a certain design problem. Clearly the filter specifications are not given in the form of rational functions, but as lines or curves that give, for example, maxima and minima of attenuation. These lines determine the so-called specified curve. Therefore, the next step in the filter design will necessarily be the determination of the permitted rational function that best approximates the specified curve, i.e., that satisfies the conditions set by the specified curve. Usually the complexity (and consequently the cost) of the circuit increases with the order of the permitted function that is selected. It is therefore necessary to determine the simplest permitted function that satisfies the specifications. Once the suitable permitted function has been found, the basic information is available for the

determination of the corresponding circuit, i.e., the circuit whose operation characteristics are in agreement with the selected permitted function.

3) Filter synthesis—Filter synthesis refers to the process for determining a circuit, i.e., its diagram and the values of its components. Even more ambitiously, we may find all possible circuits that satisfy the specifications and among them select the best according to certain criteria (cost, available technologies, power dissipation, etc.).

2.3.3 A Self Biased Architecture

Self biased circuit is the circuit in which there is no need of any external biasing circuit at any stage, means we made circuit in such a way that it take the biasing voltage from any node of the present circuit. Self Biased Circuit is able to bias its output to an equivalent bandgap voltage without using any external voltage reference or extra pin a self-biased architecture which has an operating point independent of the process technology and environmental variations hence rendering a more robust design. The self- biased architecture also gives a constant ratio of the bandwidth to reference frequency and a constant damping factor. These ensure the stability of a filter while at the same time keeping the phase noise low across the entire reference frequency range.

Fixed bias circuits get their bias voltages from independently designed reference voltage sources (or even something as simple as a voltage divider). Often in that case the bias may be left for the end-user to give some control over the operation point of the circuit.

Self biased circuits get their bias voltages from the circuit itself often in the form of a negative feedback. This is very useful when a circuit is extremely sensitive to bias points and it becomes impractical to provide external biases that are correct to very high accuracies. This can happen in high gain amplifiers with very high impedance output nodes such as a common source amplifier with an active load. The operation of the circuit depends on the bias of the active load. It would therefore be desirable to sacrifice some of this gain by providing a negative feedback from the output to the gate of the active load. This way you would not have to bias the circuit yourself but will lose some of the gain of the circuit as a price. This is one of the trade off of analog circuits.

The circuit for OTA is shown in Fig. 2.8.

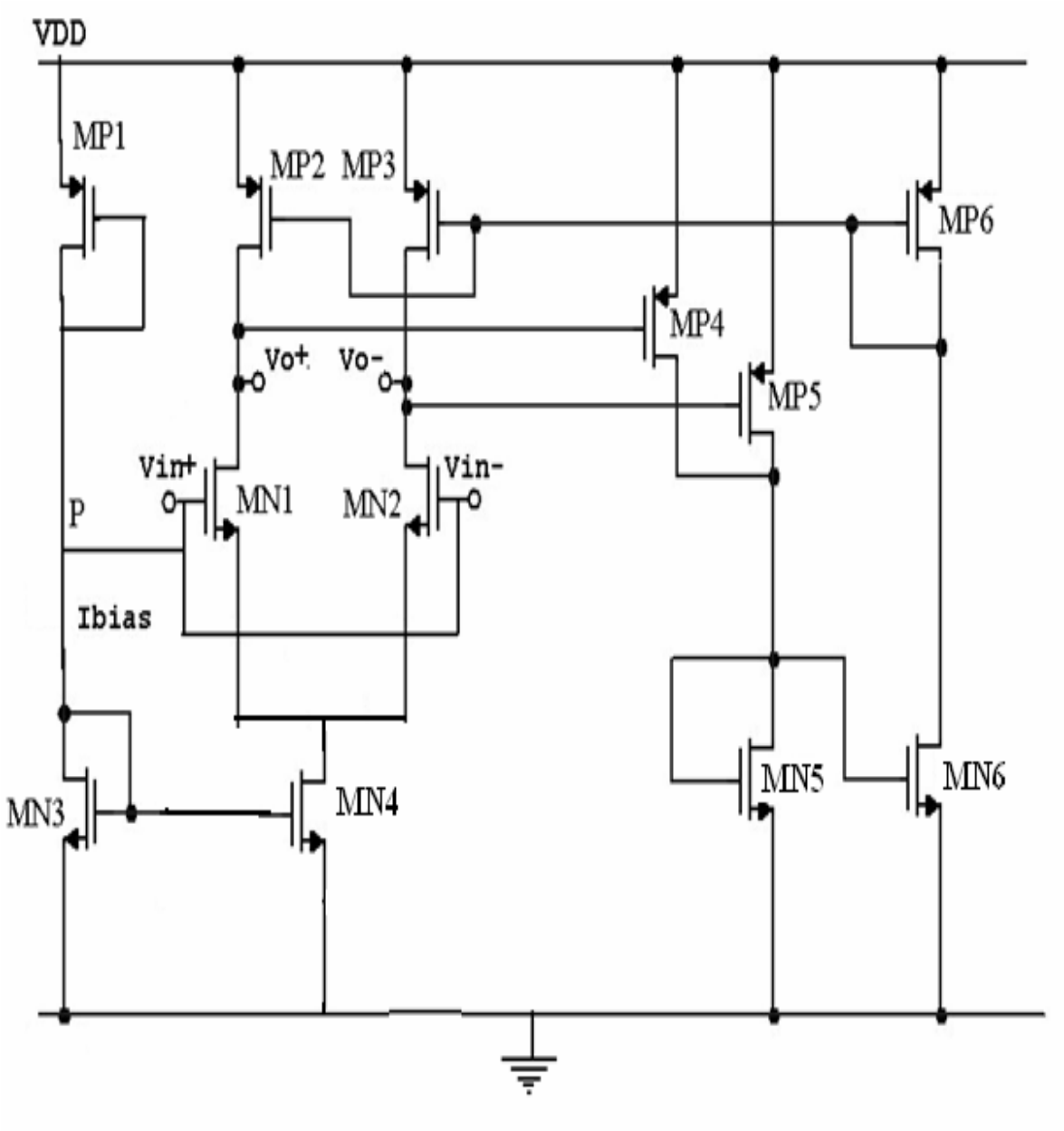


Fig 2.8. Self Biased OTA

The biasing for the input transistors MN1 and MN2 are provided by the drain terminal (node P) of MP1, there is no need of external biasing circuit is required for operating this OTA. Here, there is only need to apply AC input. Designing is in such a manner that the voltage at point P is 1.6534 Volt. Here MP1 is using also as a current source for providing current to MN3 and which is mirroring in MN4.

2.3.4 Specification of Filter

Integrated continuous-time transconductance-C (Gm-C) filters have been widely used for several applications such as digital video, RF/IF filters, etc [4, 5]. Gm-C filters offer many advantages over other continuous-time filters in terms of low power and high frequency capability [12].

The basic building block of a Gm-C filter is an integrator, basically a transconductor and a capacitor. The transconductors employed in these filters must be linear over the expected signal swing; hence the design of the transconductor is critical. Although high-frequency filters are the main aim of this topology [6], Gm- C filters can be used for integrated filters at low frequencies. Fig. 2.7 shows the fully-differential continuous-time Gm-C bandpass filter with a biquad circuit topology based on [5]. This topology was selected to provide a simple structure that demonstrates the capabilities of the technology and the filter design methodology.

The filter specifications must comply with the system requirements of the application described in [7]. The filter center frequency f_C was designed for 5 MHz, with a quality factor Q of about 25, considering a load C= 3pF.

2.3.5 Filter Parameters of Band Pass Filters

Band-pass filters are called into action to pass a range of frequencies only. How can you describe the filter shape? Here are few ways.

1) Center frequency, f_C. The center of the band, typically the peak of the frequency response curve.

2) Bandwidth, $BW = f_H - f_L$. The upper and lower frequencies, f_H and f_L, are defined as the frequencies where the gain has dropped to 0.707 of the mid-band gain.

3) Quality factor, $H = f_C / BW$. The Q tells you about the width of the pass-band: Low Q → Wide bandwidth; High Q → Narrow bandwidth.

4) Mid-band Gain, $H = V_{out} / V_{in}$. This is voltage gain at the center frequency fo [15].

2.3.6 Design of Filter Parameters

The basic building blocks in the construction of OTA-C filters are voltage integrators and amplifiers as shown in Figs. 2.9(a) and (b), respectively. The voltage transfer functions $H(s) = V_{out} / V_{in}$ (V_{in} is the differential input voltage to the OTA) of the integrator and amplifier are simply given in Eq. 2.1 and 2.2.

$$H(s) = \frac{1}{sC/g} \tag{2.1}$$

$$H(s) = \frac{g_1}{g_2} \tag{2.2}$$

respectively.

The general multiple integrator loop feedback OTA-C model with all capacitors being grounded to be addressed in this section is shown in Fig. 2.10. As depicted, this model is composed of a feedforward network consisting of n OTA-capacitor integrators connected in cascade and a feedback network that may contain OTA voltage amplifiers and/or pure wire connections [13].

To analyze the model generally, the feedback network may be described as

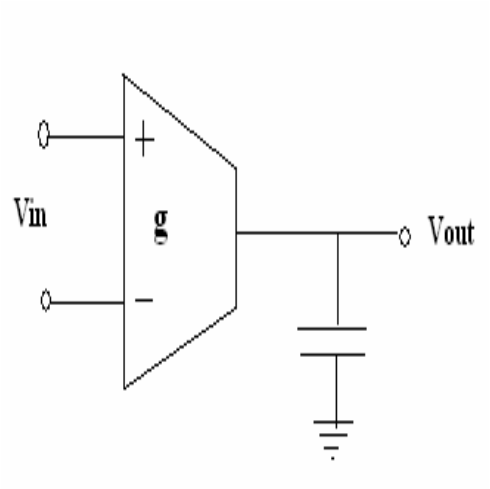


Fig. 2.9 (a) Voltage integrator

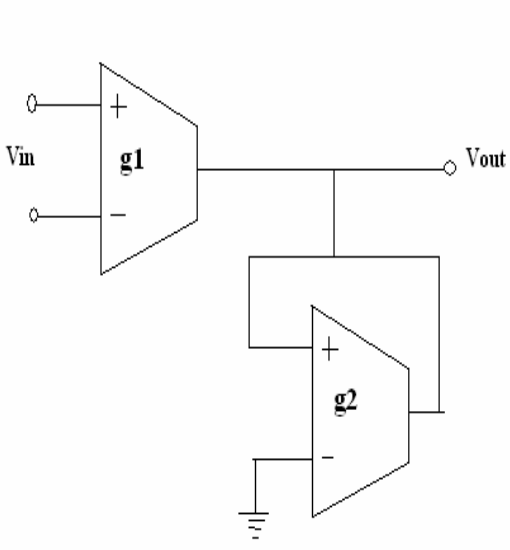


Fig. 2.9 (b) Amplifier

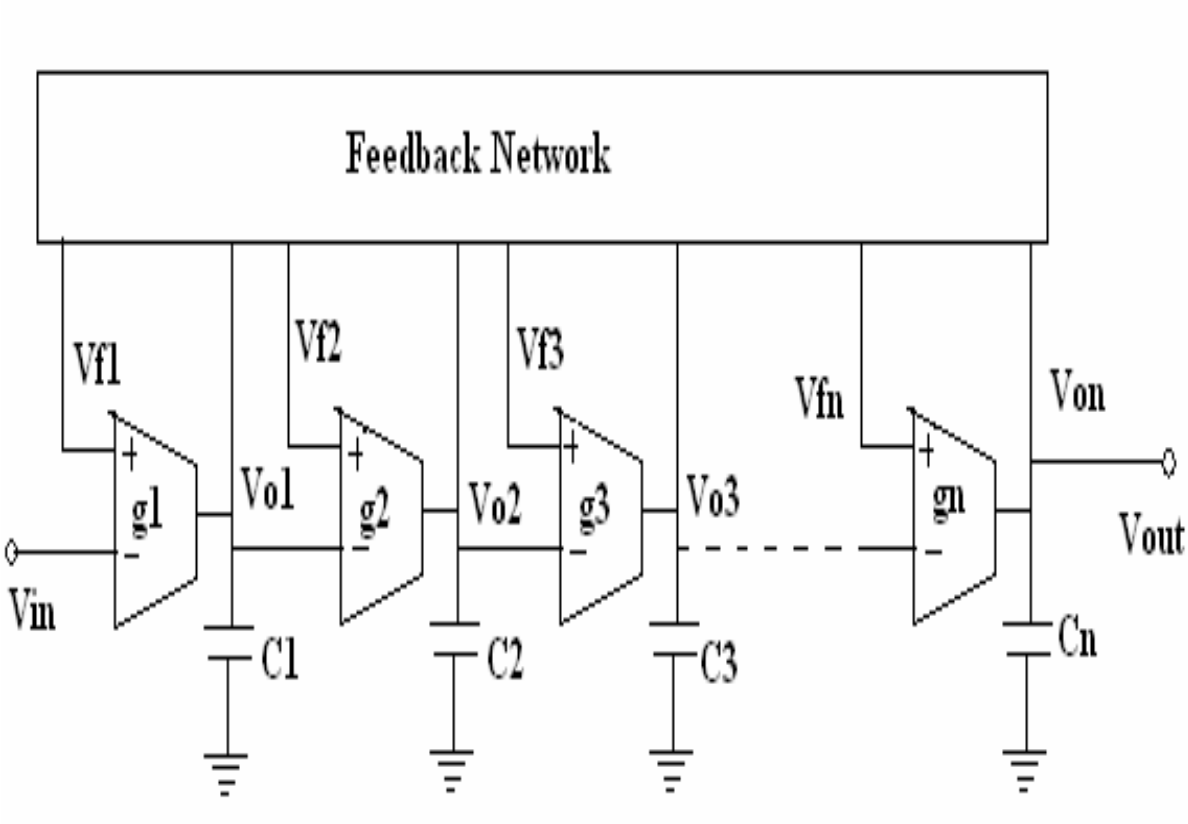


Fig. 2.10 Multiple integrator loop feedback OTA-C model.

$$V_{fi} = \sum_{j=1}^{n} f_{ij} V_{oj}, \quad \text{where } i = 1,2,3 \ldots\ldots,n \tag{2.3}$$

where f_{ij} is the voltage feedback coefficient from the output of integrator j to the input of integrator i. This coefficient f_{ij} can be realized with an open circuit or an amplifier for the zero or nonzero values, respectively. The former means no feedback exists, while the latter suits any amount of feedback, between the i^{th} and j^{th} integrators. In particular, we may also realize f_{ij} = 1, i.e., the unity feedback by direct connection, as an alternative to using a unity gain amplifier [14].

Equation (2.3) can also be written in the matrix form.

$$[V_f] = [F]\,[V_o] \tag{2.4}$$

where

$[V_o] = [V_{o1} V_{o2} V_{o3} \ldots\ldots\ldots V_{on}].t$, the output voltages of integrators,

$[V_f] = [V_{f1} V_{f2} V_{f3} \ldots\ldots\ldots V_{fn}].t$, the feedback voltages to the inverting input terminals of integrators, and

$[F] = [F_{ij}] n \times n$, the feedback coefficient matrix. The superscript t stands for transpose.

The currents flowing into and out of the feedback network all are zero, since they are related to the input terminals of the OTAs in the feedforward circuit or in the feedback network, which are ideally infinite impedance. Noting this and denoting time constants $\tau_j = C_j/g_j$, we have write the equations for the feedforward network by inspection

$$s\tau_1 V_{o1} = V_{in} - V_{f1},\ s\tau_{j+1} V_{o(j+1)} = V_{oj} - V_{f(j+1)} \tag{2.5}$$

where s is the complex frequency.

Equation (2.5) can also be condensed in a matrix form and on solving the transfer function $H(s)$ can be simplified as

$$H(s) = \frac{1}{[A(s)]} \tag{2.6}$$

2.3.7 Quality Factor

In physics and engineering, the quality factor or Q factor describes how under-damped an oscillator is. Higher Q indicates a lower rate of energy loss relative to the stored energy of the oscillator; the oscillations die out more slowly. A pendulum suspended from a high-quality bearing, oscillating in air, has a high Q, while a pendulum immersed in oil has a low one. Oscillators with high quality factors have low damping so that they ring longer.

Sinusoidally driven resonators having higher Q factors resonate with greater amplitudes (at the resonant frequency) but have a smaller range of frequencies near that frequency for which the resonate; the range of frequencies for which the oscillator resonates is

called the bandwidth. Thus, a high Q tuned circuit in a radio receiver would be more difficult to tune, but would have more selectivity; it would do a better job of filtering out signals from other stations that lay nearby on the spectrum. High Q oscillators oscillate with a smaller range of frequencies and are more stable.

The quality factors of oscillators vary substantially from system to system. Systems for which damping is important (such as dampers keeping a door from slamming shut) have Q = ½. Clocks, lasers, and other resonating systems that need either strong resonance or high frequency stability need high quality factors. Tuning forks have quality factors around Q = 1000. The quality factor of the best clocks and some high Q lasers can reach as high as 10 and higher.

There are many alternate quantities used by physicists and engineers to describe how damped an oscillator is and that are closely related to the quality factor. Important examples include the damping ratio, relative bandwidth, linewidth and bandwidth measured in octaves [16].

(a) The "Q" or Quality Factor for a band pass filter

In a Band Pass Filter circuit, the overall width of the actual passband between the upper and lower -3dB corner points of the filter determines the Quality Factor or Q-point of the circuit. This Q Factor is a measure of how "Selective" or "Un-selective" the band pass filter is towards a given spread of frequencies. The lower the value of the Q factor, the wider is the bandwidth of the filter and consequently the higher the Q factor, the narrower and more "selective" is the filter [17]. The Quality Factor, Q of the filter is sometimes given the Greek symbol of Alpha, (α) and is known as the alpha-peak frequency where:

$$\alpha = {}^{1}/_{Q} \tag{2.7}$$

As the quality factor of a band pass filter (Second-order System) relates to the "sharpness" of the filters response around its centre resonant frequency (f_r) it can also be thought of as the Damping Factor or Damping Coefficient because the more damping the

filter has, the flatter is its response and likewise, the less damping the filter has the sharper is its response. The damping ratio is given the Greek symbol of Xi, (ξ) where

$$\xi = 2\alpha \tag{2.8}$$

The "Q" of a band pass filter is the ratio of the Resonant Frequency, (f_r) to the Bandwidth, (BW) between the upper and lower -3dB frequencies and is given as

$$Q = \frac{Resonant\ Frequency}{Bandwidth}$$

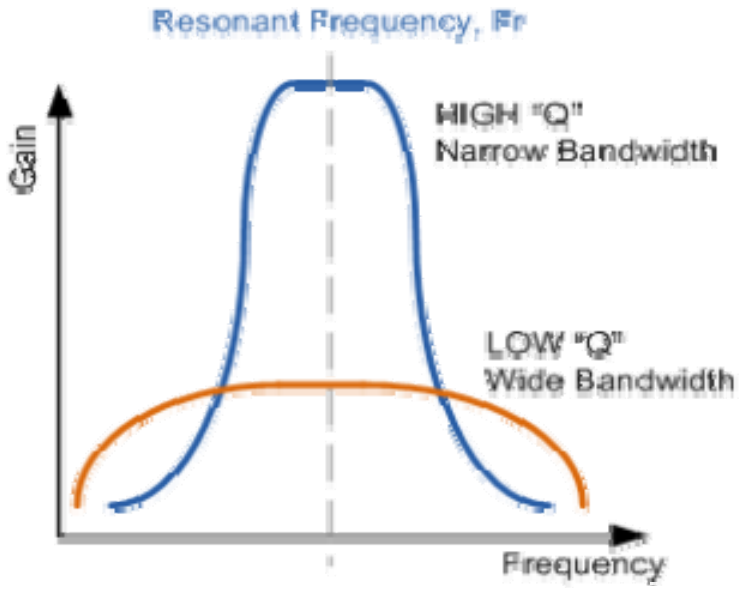


Fig. 2.11 Quality Factor [17]

2.4 Gm/Id Methodology

In the given method, we consider the relationship between the ratio of the transconductance g_m over dc drain current I_D and the normalized drain current I_O,

I_O /(W/L) as a fundamental design tool. The methodology is intended for low-power analog and digital circuits where the weak as well as moderate inversion regions are often used because they provide a good compromise between speed and power consumption.

The g_m/I_D ratio indeed is a universal characteristic of all transistors formed by the same process.

MOS transistors are either in strong inversion or in weak inversion. Mainstream methods assume generally strong inversion and use the transistor gate voltage overdrive (V_{OV}) as the key parameter, where $V_{OV} = V_{GS} - V_T$.

If we consider a simple common source amplifier, the power and bandwidth are given by following equations (2.9) and (2.10).

These two equations (2.9) and (2.10) gives the power and bandwidth.

$$P = \frac{1}{2}\frac{V_{DD}}{R_L}.A_{DC}.V_{OV} \tag{2.9}$$

$$\omega_{-3DB} = \frac{3}{2}\frac{R_L}{R_i}.\frac{1}{A_{DC}}\frac{\mu}{L^2}V_{OV} \tag{2.10}$$

With the assumed fixed design specifications, and a given technology (μ, L_{min}), both power and bandwidth of our circuit are completely determined by the choice of V_{OV}. Making V_{OV} small to save power also means that we lose bandwidth.

This makes intuitive sense since

$$\frac{W}{L} = \frac{g_m}{\mu C_{ox} V_{OV}} \tag{2.11}$$

With g_m and L fixed, smaller V_{OV} translates into a bigger (wider) device, and thus larger C_{gs}. So we conclude from this that the V_{OV} is not a good design parameter

What we really want from MOS transistor

- Large g_m without investing much current
- Large g_m without having large C_{gs}

To quantify how good our transistor works, we therefore define the "figures of merit". There are three performance metrics

1. Transit Frequency:

$$\omega_T = \frac{g_m}{C_{gs}}$$

2. Trans-conductor Efficiency:

$$\frac{g_m}{I_D}$$

3. Intrinsic Gain:

$$g_m r_o$$

We find that V_{OV} is not "directly" related to performance metric. Hence, we switch towards a strategy called "g_m/I_D design methodology", in which g_m/I_D, rather than V_{OV} is used directly as a central design variable.

2.4.1 Generation of Performance Curves

(a) F_T Simulation:

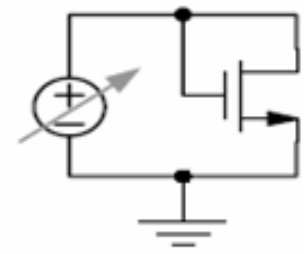


Fig. 2.12. F_T Simulation

Steps:

1) After the simulation of above circuit, we get all current and voltage plots in waveform window.
2) Plot gate overdrive $V_{OV} = V_{GS} - V_{TH}$.

3) Plot g_m curve by taking derivative of I_D Vs V_{GS}
4) Divide g_m curve by I_D curve to get g_m/I_D.
5) Divide g_m curve by C_{gs} to get F_T.
6) Plot (F_T Vs g_m/I_D) transit frequency chart by taking F_T as Y-axis and g_m/I_D as X-axis.

(b) Intrinsic Gain Simulation

$$V_{gs} = V_t + 200mv$$

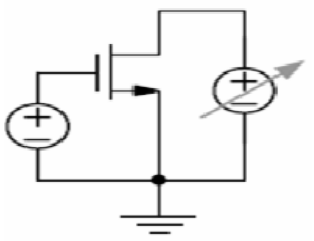


Fig. 2.13 Intrinsic Gain Simulation

Steps:

1. After the simulation of above circuit, we get all current and voltage plots in waveform window.
2. Get $1/r_o$ curve by taking derivative of I_D Vs V_{DS}.
3. To get ro plot, take the reciprocal of above curve. At very small value of V_{DS}, g_m is constant. Take that value as g_{mo}. g_{mo} can also be find out by dividing I_D by ($V_{GS} - V_{TH}$). Then plot $g_m = g_{mo} * (1 + \lambda V_{DS})$, where $\lambda = 1/(r_o * I_D)$.
4. Get $g_m * r_o$ Vs V_{DS} plot.

(c) g_m/I_D Simulation:

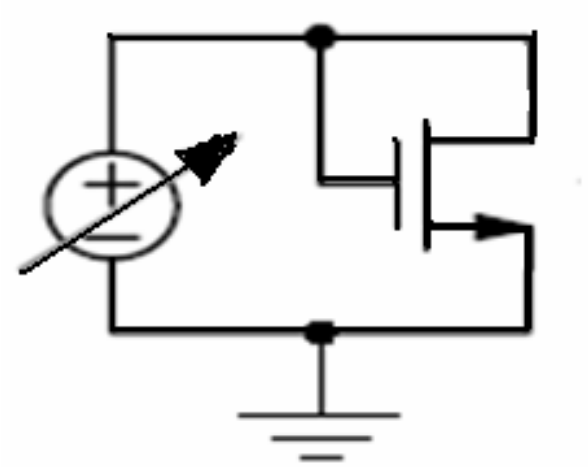


Fig. 2.14 g_m/I_D Simulation

Steps:

1. After the simulation of above circuit, we get all current and voltage plots in waveform window.
2. Find out gate overdrive $V_{OV} = V_{GS} - V_{TH}$. V_{TH} can be seen in log files after running simulation after making the transistor in saturation.
3. Plot gm curve by taking derivative of I_D Vs V_{GS}.
4. Divide gm curve by I_D curve to get g_m/I_D.
5. Divide I_D curve by W/L value to get $I_D/(W/L)$ plot.
6. Setting g_m/I_D as X-axis, plot $I_D/(W/L)$ which is called current density plot.

2.4.2 Benefits of g_m/I_D Methodology

The choice of g_m/I_D is based on its relevance for the three following reasons.

1) It is strongly related to the performances of analog.

2) It gives an indication of the device operating region.

3) It provides a tool for calculating the transistors dimensions.

In order to illustrate this, let us consider the "intrinsic gain stage" as a simple example. The intrinsic gain stage consists of a single transistor in the common source configuration

loaded by an ideal current source (delivering a dc current I_D) and a capacitance C_L. We call g_m the small-signal transconductance and V_A, the Early voltage which controls the transistor small-signal output conductance, $g_D = I_D / V_A$. The dc gain (A_O) and transition unity-gain frequency (f_T) are given by

$$A_O = -\frac{g_m}{I_D} V_A \tag{2.12}$$

and

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_L} \tag{2.13}$$

The g_m/I_D ratio is a measure of the efficiency to translate current (hence power) into transconductance; i.e., the greater the g_m/I_D value, the greater the transconductance we obtain at a constant current value. Therefore, the g_m/I_D ratio is sometimes interpreted as a measure of the "transconductance generation efficiency" [18].

The relation of the I_D ratio with the transistor operating mode can be observed from the fact that this ratio is equal to the derivative of the logarithmic of I_D with respect to V, as shown below

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{\partial I_D}{\partial V_G} = \frac{\partial(\ln I_D)}{\partial V_G} = \frac{\partial\left\{ln\left[\frac{I_D}{\left(\frac{W}{L}\right)}\right]\right\}}{\partial V_G} \tag{2.14}$$

This derivative is maximum in the weak inversion region where the I_D dependence versus V_G is exponential while it is quadratic in strong inversion, becoming almost linear deeply in strong inversion because of the velocity saturation. The maximum is equal to 1 /(nU_T) here n is the subthreshold slope factor and U_T the thermal voltage. The g_m/I_D ratio decreases as the operating point moves toward strong inversion when I_D or V_G, are increased as shown in Fig. 2.15. Therefore, the g_m/I_D ratio is also an indicator of the mode of operation of the transistor [19].

Let us now consider the dependence of g_m/I_D on transistor size. The normalized current I_n is independent of the transistors size. According to Eq. (2.14) the g_m/I_D ratio is also size independent. Therefore, the relationship between g_m/I_D and the normalized current is a unique characteristic for all transistors of the same type (nMOS or PMOS) in a given batch. Of course, this statement must be revised when dealing with short channel transistors.

The "universal" quality of the g_m/I_D versus I_n curve can be extensively exploited during the design phase, when the transistor aspect ratios (W/L) are unknown. Once a pair of values among g_m/I_D, g_m, and I_D has been derived, the W/L of the transistor can be determined unambiguously. An example of this procedure is described in the next section.

The actual g_m/I_n versus I_n curve can be obtained in two ways: either analytically, using a MOS transistor model that provides a continuous representation of the transistor current and small-signal parameters in all regions of operations or from measurements on a typical transistor [20, 21]. It is more appropriate of course to consider a mean curve which is representative of a large number of transistors in order to take into account technology spreads. We use the experimental approach for evaluation of the data that were used for the design of the SOI micropower OTA presented in the next section.

Fig. 2.15 shows the calculated and measured plots of g_m / I_D versus I_n for N and PMOS thin-film SOI fully depleted transistors as well as for bulk transistors. The calculated plain curves were obtained applying the model given in [19]. The bulk transistors curves were calculated assuming the same substrate concentration for the N and PMOS transistors.

The different evolution of N and PMOS g_m/I_D curves with I_n is related to the mobility difference. As shown in Fig. 2.15, the increased subthreshold slope of the thin-film SOI transistors provides a maximum value of g_m/I_D of about 35 V^{-1} for the SOI transistors (which corresponds to n = 1.1) while only 25 V^{-1} is found for bulk transistors (n = 1.5) [22].

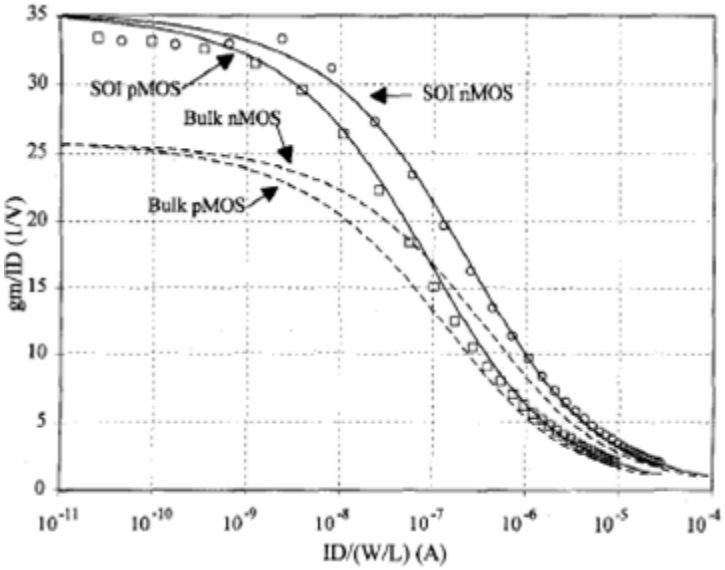


Fig. 2.15 . g_m/I_D Versus I_D/(W/L) curves for nMOS and PMOS [19]

2.4.3 Design Procedure using g_m/I_D

(a) g_m/I_D Plots

A comparative plot for g_m / I_DVs V_{OV} is given below in Fig 2.16.

Since g_m / I_DVs V_{OV} plots are very important in the design procedure, Separate plots for each L have been generated.

It had been stated earlier that the -3dB bandwidth is inversely proportional to L^2. Similar same effect can also be seen in case of F_T. From this point, several electrical simulations are executed and then the design parameters can be readjusted until the desired performance can be achieved as given in Fig. 2.16

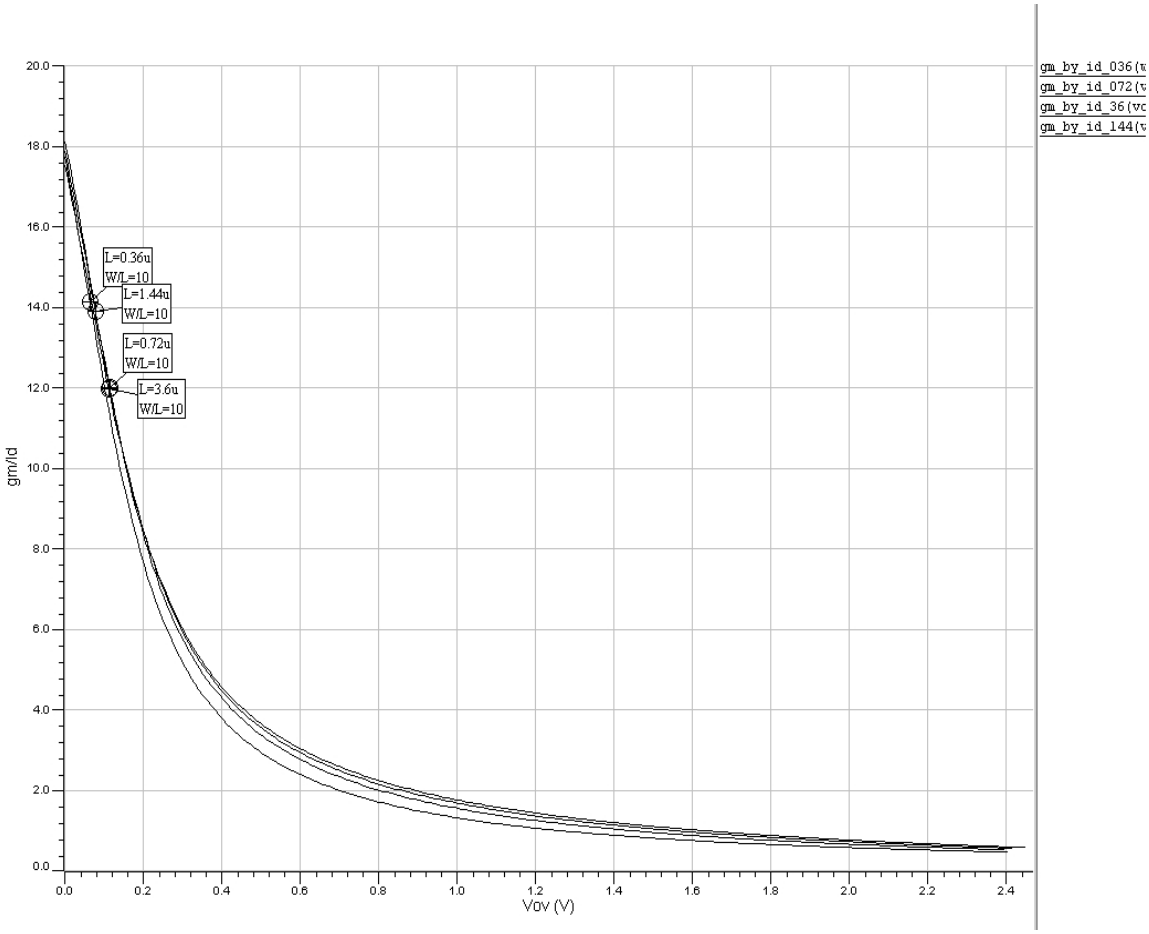


Fig. 2.16 Comparative plot for L in g_m/I_D *Vs* V_{OV}

(b) I_D/ (W/L) Vs g_m / I_D Plots

These plots help in determining the required W/L for a given current. If we have chosen the g_m / I_D values, this can also be chosen that the aspect ratio of the MOSFET from these plots. And this also can be decided that in which region, the transistor should be operated. For the desired g_m / I_D value, the corresponding value of normalize current can be chosen and find the desired W/L of a particular transistor.

First, a comparative plot is shown in Fig. 2.17. Here L varies from 0.36µm to 3.6µm.

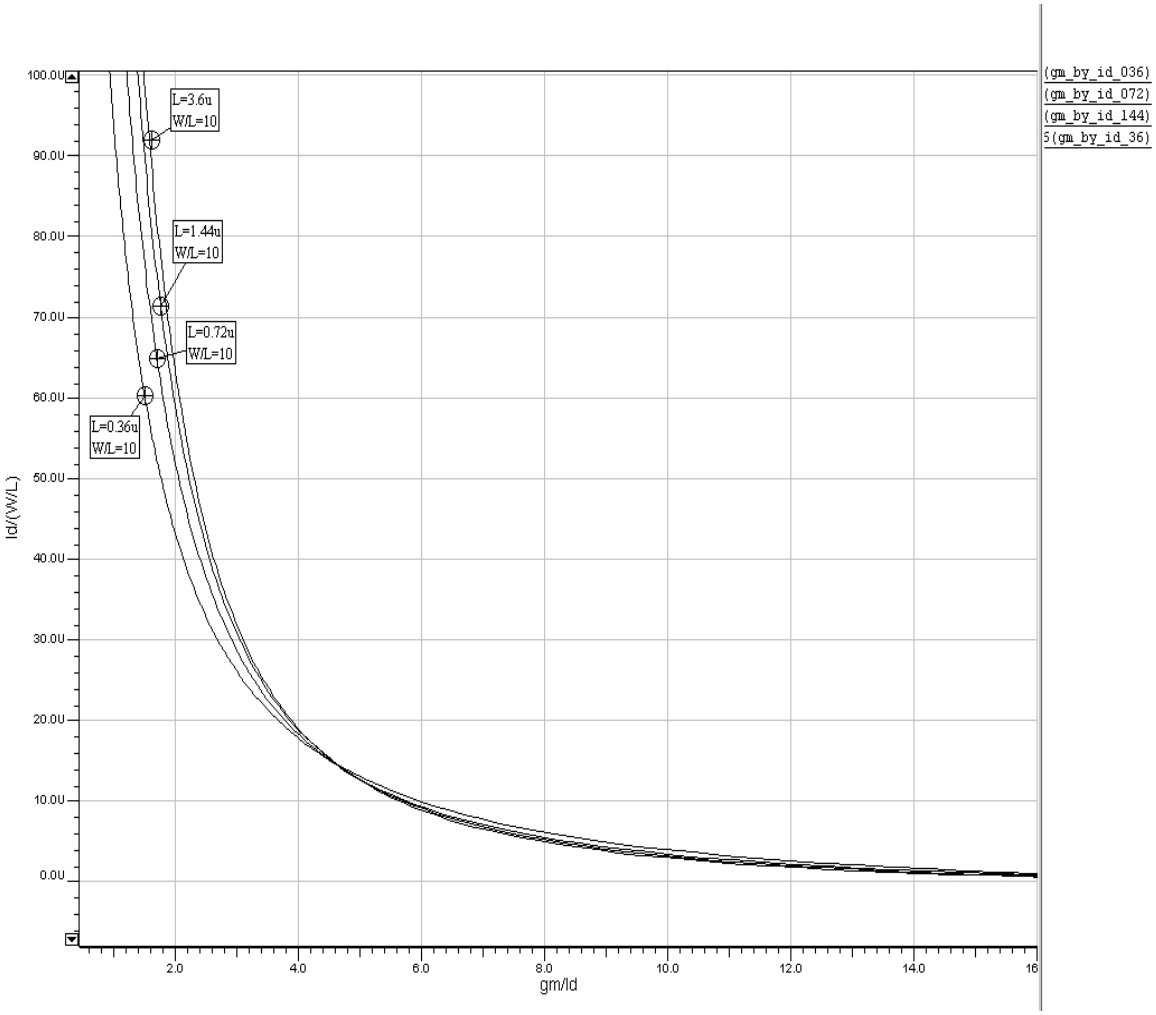


Fig. 2.17 Comparative plot for L in $I_D/(W/L)$ *Vs* g_m / I_D

Separate $I_D/(W/L)$ *Vs* g_m / I_D plots have been generated for each L (0.36µm, 0.72µm, 1.44µm, 3.6µm) Now take the value of $I_D/(W/L)$ corresponding to required g_m / I_D or I_N Then put the present value of I_D in particular transistor And find the value of W/L.

2.5 Operational Transconductance Amplifier

OTA based on CMOS inverters and application in the design of tunable bandpass filter operational transconductance amplifiers (OTA) are used to realize numerous continuous time circuits and systems [23–29, 31]. They are for example largely used to implement Gm-C (or OTA-C) filters [23–29]. Classically OTA are designed from a differential pair of two transistors. In this case the OTA differential transconductance is controlled by

modifying the current sink of its differential pair(s) [24]. Here OTA is directly voltage controlled.

Digital cells can be easily designed from CMOS logical gates and CMOS switches working under two possible electrical signal states. These two states often correspond to the electrical values 0 (ground) and V_{DD}, where V_{DD} is the power supply of all the logical gates. In an opposite way analog systems are often used to amplify continuous time signals for which the noise, sensibility, and linearity are more important than the digital counterpart. Even if they are basic universal analog functions (operational amplifiers, controlled current or voltage sources), it is relatively difficult to synthesize automatically analog systems from basic universal analog cells. The interest of using CMOS inverters to realize analog operations is that the CMOS inverter (normally used in digital operation) can be automatically synthesized on silicon from digital tools. The CMOS inverter is also currently used as transimpedance amplifier to detect the current flowing through a diode.

Here the CMOS inverter working in transconductance mode of operation. In this case the CMOS inverter operates at small-signal around a common mode voltage equal to the half of the supply voltage V_{DD} ($V_{CM} = V_{DD}/2$). In this operation the CMOS inverter simulates a negative transconductor [30].

The conventional operational amplifier (op amp) is used as the active device in the vast majority of the active filter literature. For design purposes, the assumption that the op amp is ideal $A_V = \infty$, $R_{in} = \infty$, $R_O = 0$ is generally made, and large amounts of feedback are used to make the filter gain essentially independent of the gain of the op amp. A host of practical filter designs have evolved following this approach. It has also become apparent, however, that operational amplifier limitations preclude the use of these filters at high frequencies, attempts to integrate these filters have been unsuccessful (with the exception of a few nondemanding applications), and convenient voltage or current control schemes for externally adjusting the filter characteristics do not exist [31].
With the realization that the BJT and MOSFET are inherently current and transconductance amplifiers, respectively, the following question naturally arises. Can any improvements in filter characteristics, performance, or flexibility be obtained by

using one of the other basic types of amplifiers (e.g., transconductance, current), or this question is currently difficult to answer for two reasons. First, there is a near void in the literature of active filter structures employing the alternative amplifier types. Second, the evolution of good integrated transresistance, transconductance, and current amplifiers has not kept pace with that of the voltage amplifiers, although a few devices in these alternate categories are commercially available (e.g., transconductance amplifiers such as the CA 3080 and LM 13600 and transresistance amplifiers such as the LM 3900) [33]. Comparisons of some characteristics of these amplifiers were recently discussed by Brugger et al. [34].

Here, basic first- and second-order structures using the transconductance amplifier (often termed the operational transconductance amplifier (OTA) are given. It is shown that these structures offer improvements in design simplicity and programmability when compared to op amp based structures as well as reduced component count. Many of the basic OTA based structures use only OTAs and capacitors and, hence, are attractive for integration. Component count of these structures is often very low (e.g., second-order biquadratic filters can be constructed with two OTAs and two capacitors) when compared to VCVS designs. Convenient internal or external voltage or current control of filter characteristics is attainable with these designs. They are attractive for frequency referenced (e.g., master/slave) applications. Several groups have recently utilized OTAs in continuous-time monolithic filter structures [33].

From a practical viewpoint, the high-frequency performance of discrete bipolar OTAs, such as the CA 3080, is quite good. The transconductance gain, gm, can be varied over several decades by adjusting an external dc bias current, I_{ABC}. The major limitation of existing OTAs is the restricted differential input voltage swing required to maintain linearity. For the CA 3080, it is limited to about 30 mV p-p to maintain a reasonable degree of linearity. Although feedback structures in which the sensitivity of the filter parameters are reduced (as is the goal in op amp based filter design) will be discussed, major emphasis will be placed upon those structures in which the standard filter parameters of interest are directly proportional to gm of the OTA. Since the transconductance gain of the OTA is proportional to an external dc bias current, external control of the filter parameters via the bias current can be obtained.

Most existing work on OTA based filter design approached the problem by either concentrating upon applying feedback to make the filter characteristics independent of the transconductance gain or modifying existing op amp structures by the inclusion of some additional passive components and OTA's. In either case, the circuits were typically component intense and cumbersome to tune.

2.5.1 OTA Model

The symbol used for the OTA is shown in Fig. 2.18, along with the ideal small signal equivalent circuit. The transconductance gain, g_m, is assumed proportional to I_{ABC}. The proportionality constant h is dependent upon temperature, device geometry, and the process.

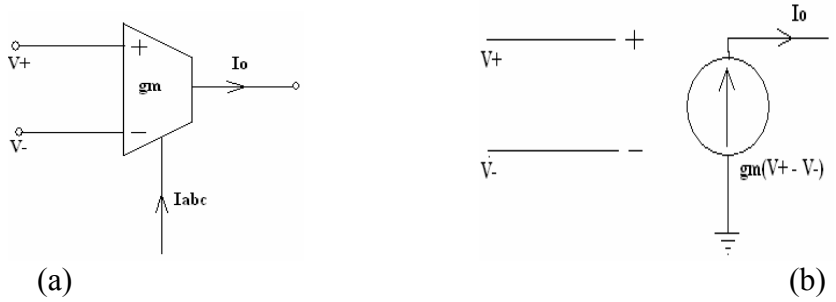


Fig.2.18 OTA. (a) Symbol. (b) Equivalent circuit of ideal OTA.

$$I_o = g_m(V_+ - V_-) \tag{2.15}$$

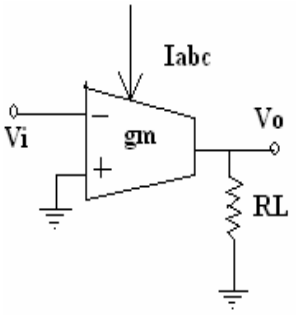
As shown in the model, the input and output impedances in the model assume ideal values of infinity. Current control of the transconductance gain can be directly obtained with control of I_{ABC} Since techniques abound for creating a current proportional to a given voltage, voltage control of the OTA gain can also be attained through the I_{ABC} input. Here, when reference is made to either the current or voltage controllability of OTA based circuits' it is assumed to be attained via control of g_m by I_{ABC}.

2.5.2 Basic OTA Building Blocks

Some of the basic OTA building blocks [35] are introduced in this section. A brief discussion about these circuits follows. Voltage amplifiers using OTAs are shown in Fig. 2.19, along with voltage gain and output impedance expressions. The basic inverting and non-inverting configurations of Figs. 2.19(a) and 2.19(b) have a voltage gain directly

proportional to g_m, which makes current (voltage) control of the gain via I_{ABC} straightforward. Furthermore, observe that a differential amplifier can be easily obtained by using both input terminals of the OTA in Figs. 2.19(a) or 2.19(b). The major limitation of these circuits is the relatively high output impedance.

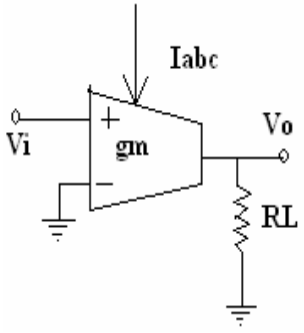
A voltage buffer, such as used in Figs. 2.19(c) and 2.19(d), is often useful for reducing output impedance. Although the gain characteristics of these circuits are ideally identical, the performance of the two circuits is not the same.



$$\frac{V_o}{V_i} = -g_m R_L$$

$$Z_o = R_L$$

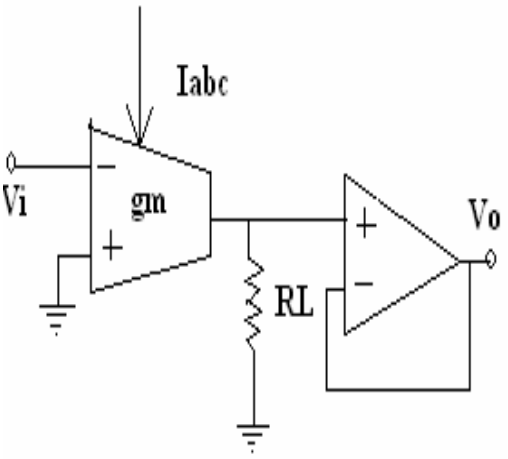
(a) Basic inverting amplifier



$$\frac{V_o}{V_i} = g_m R_L$$

$$Z_o = R_L$$

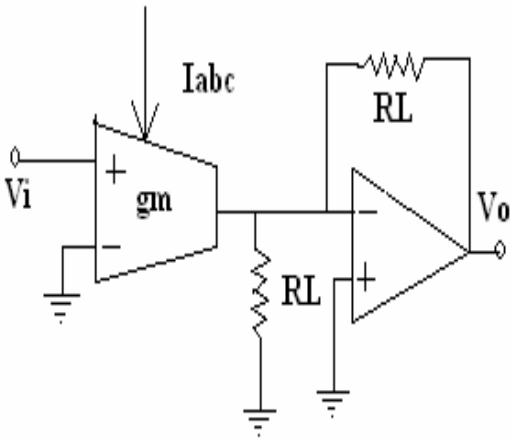
(b) Basic noninverting amplifier



$$\frac{V_o}{V_i} = g_m R_L$$

$$Z_o = 0$$

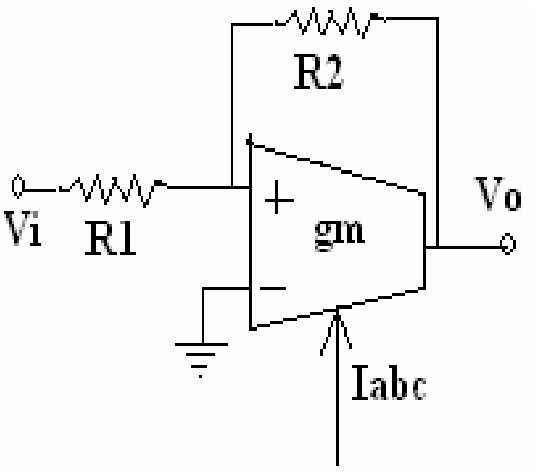
(c) Feedback amplifier



$$\frac{V_o}{V_i} = g_m R_L$$

$$Z_o = 0$$

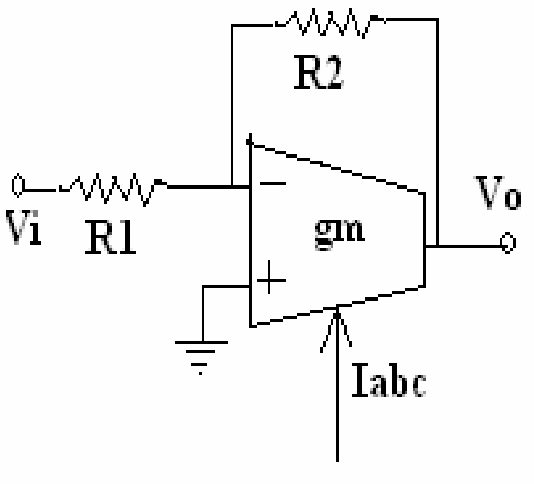
(d) Noninverting feedback amplifier



$$\frac{V_O}{V_I} = \frac{1+g_m R_2}{1+g_m R_1}$$

$$Z_O = \frac{(R_1+R_2)}{1+g_m R_1}$$

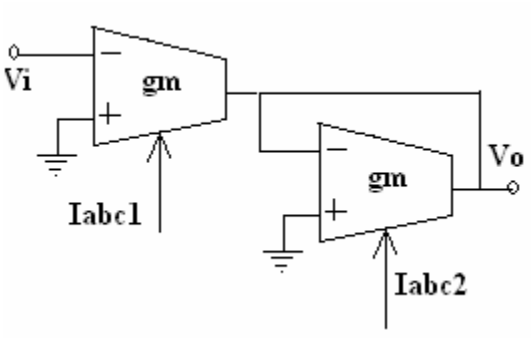
(e) Buffered amplifier



$$\frac{V_O}{V_I} = \frac{g_m(R_1+R_2)}{1+g_m R_1}$$

$$Z_O = \frac{(R_1+R_2)}{1+g_m R_1}$$

(f) Buffered VCVC feedback



$$\frac{V_O}{V_I} = -\frac{g_{m1}}{g_{m2}}$$

$$Z_O = \frac{1}{g_{m2}}$$

(g) All OTA amplifiers

Fig. 2.19. Voltage amplifiers

The performance differences are due to differences in the effects of parasitics in the circuits. Specifically, the parasitic output capacitance of the OTA in Fig. 2.19(c), along with instrumentation parasitics, parallel the resistor R_L in discrete component structures, thus causing a roll-off in the frequency response of the circuits. In the circuit of Fig. 2.19(d), the parasitic output capacitance of the OTA is connected across the null port of an op amp and thus has negligible effects when the op amp functions properly. Likewise, instrumentation parasitics will typically appear at the low impedance output of the op amp, and thus not have a major effect on the performance. As with conventional amplifier design using resistors and op amp's, the amplifier bandwidth of these structures warrants consideration. For the circuits of Figs. 2.19(c) and 2.19(d), the major factor limiting the bandwidth is generally the finite gain bandwidth product of the op amps. If the op amps are modeled by the popular single-pole roll-off model, A(s) = GB/s, and the OTAs are assumed ideal, it follows that the bandwidth of the circuits (GB) of Fig. 2.19(c) and 2.19(d), independent of the voltage gain of the amplifier. This can be contrasted to the bandwidths of GB/K and GB/(1 + K) for the basic single op amp non-inverting and inverting amplifiers of gains K and - K, respectively.

Note that the circuits of Figs. 2.19(a) and 2.19(b) differ only in the labeling of the "+" and "-" terminals. In all circuits given here, interchanging the "+" and "-" terminals of the OTA will result only in changing the sign of the g_m coefficient in any equation derived for the original circuit. Henceforth, it will be the choice to determine when such an interchange provides a useful circuit.

The circuits of Figs. 2.19(e) and 2.19(f) are feedback structures. The circuit of Fig. 2.19(e) offers gains that can be continuously adjusted between positive and negative values with the parameter gm. By interchanging the + and - terminals of the OTA, very large gains can be obtained as gm R_1 approaches 1 (as Zo approaches infinity). Gain is nonlinearly related to g_m. Control range via g_m is reduced in these structures when compared to the amplifiers of Figs. 2.19(a) and 2.19(b). If components are sized fitly, the gain of these structures can be made essentially independent of g_m (as in the conventional op amp inverting and non-inverting configurations) and the output impedances can be made reasonably small.

The amplifier of Fig. 2.19(g) is attractive since it contains no passive components. Gain adjustment can be attained with either g_{m1} or g_{m2}. The total adjustment range of the gain of this structure is double (in dB) than that attainable with the single OTA structures considered in Figs. 2.19(a) and 2.19(b). Furthermore, if both OTAs are in the same chip, the variations with temperature of the g_m's are cancelled.

2.5.3 Benefits of OTA over an OPAMP

This section demonstrates the usefulness of the operational transconductance amplifier (OTA) as a replacement for the conventional op-amp in both first and second-order active filters[37]. It is at least partially intended to acquaint the technology student with the rudiments of operation of the OTA, as well as the practicalities of using the presently available commercial OTA's. Active RC filters using the operational amplifier (opamp) have been developed. These filters have been widely used in various low frequency applications in telecommunication networks, signal processing circuits, communication systems, control, and instrumentation systems for a long time. However, active RC filters cannot work at higher frequencies (over 200 kHz) due to opamp frequency limitations and are not suitable for full integration. They are also not electronically tunable and usually have complex structures. Many attempts have been made to overcome these drawbacks [1, 8]. The most successful approach is to use the operational transconductance amplifier (OTA) to replace the conventional opamp in active RC filters. In recent years OTA-based high frequency integrated circuits, filters and systems have been widely investigated [36].

2.5.4 Requirement for the Core OTA

As seen in section 2.5.2, an ideal operational transconductance amplifier is a voltage-controlled current source, with infinite input and output impedances and constant transconductance. The OTA has two attractive features: its tranconductance can be controlled by changing the external dc bias current or voltage, and it can work at high frequencies. The OTA has been implemented widely in CMOS and bipolar and also in

BiCMOS and GaAs technologies. The typical values of transconductances are in the range of tens to hundreds of μS in CMOS and up to mS in bipolar technology.

The CMOS OTA, for example, can work typically in the frequency range of 50 MHz to several 100 MHz. Linearization techniques make the OTA able to handle input signals of the order of volts with nonlinearities of a fraction of one percent. Programmable high-frequency active filters can therefore be achieved by incorporating the OTA.

These OTA filters also have simple structures and low sensitivity. In this section we will discuss how to construct filters using a single OTA, because single OTA active filters have advantages such as low power consumption, noise, parasitic effects, and cost. Commercially widely available OTAs are very easy to access for one to build filters with resistors and capacitors.

However, single OTA filters may not be suitable for full integration as they contain resistors which demand large chip area. These filter structures may also not be fully programmable, as only one OTA is utilized. It should be emphasized that on-chip tuning is the most effective way to overcome fabrication tolerances, component nonidealities, aging, and changing operating conditions such as temperature. Therefore, in monolithic design we should also further avoid using resistors. In recent years, active filters which use only OTAs and capacitors have been widely studied. These filters are intuitively called OTA-C filters, which will also be the subject of the remaining chapters. Fortunately, the single OTA filter structures can be readily converted into fully integrated OTA-C counterparts by using OTAs to simulate the resistors. This will be shown in the chapter. It should be noted that practical OTAs will have finite input and output impedances. For the CMOS OTA, for example, the input resistance is usually very large, being neglectable, but the output resistance is in the range of 50kHz to 1MHz, and the input and output capacitances are typically of the order of 0.05pF. Also, at very high frequencies, the OTA transconductance will be frequency dependent due to its limited bandwidth. These nonideal impedance and transconductance characteristics will influence the stability and frequency performances of OTA filters. Practical OTAs will also exhibit nonlinearity for large signals and have noise, which will affect the dynamic

range of OTA filters [36]. . Linearization techniques make the OTA able to handle input signals of the order of volts with nonlinearities of a fraction of one percent.

2.5.5 Basic OTA Operation

(a) DC Operation

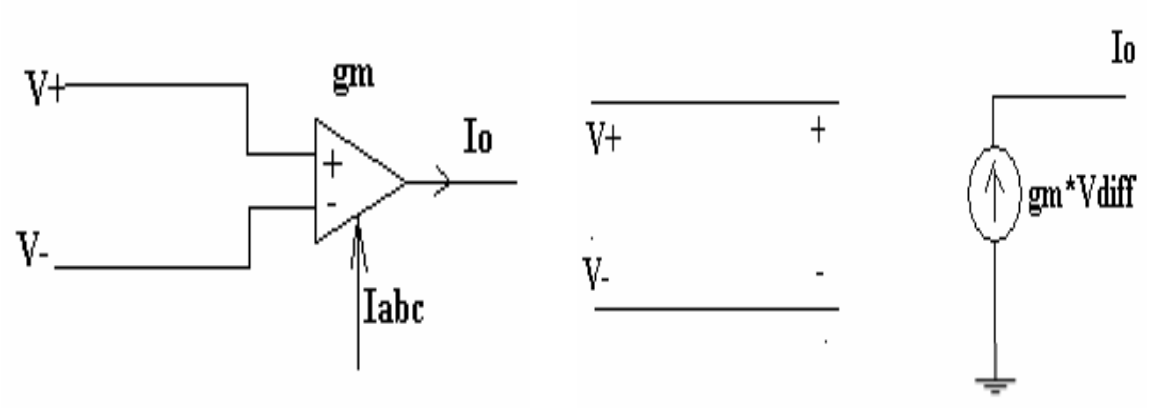
The OTA is a transconductance type device, which means that the input voltage controls an output current by means of the device transconductance, labeled g_m. This makes the OTA a voltage-controlled current source (VCCS), which is in contrast to the conventional op-amp, which is a voltage-controlled voltage source (VCVS). What is important and useful about the OTA's transconductance parameter is that it is controlled by an external current, the amplifier bias current, I_{ABC} , so that one obtains

$$g_m = \frac{I_{ABC}}{2V_T} = \frac{20}{V} . I_{ABC} \qquad (2.16)$$

From this externally controlled transconductance, the output current act as a function of the applied voltage difference between the two input pins, labeled v_+ and v_-, is given by

$$I_O = g_m (V_+ - V_-) \qquad (2.17)$$

Clearly, an output voltage can be derived from this current by simply driving a resistive load. The equivalent circuit for the OTA is shown in Figure 2.20.



(a) (b)

Fig. 2.20 Equivalent Circuit of OTA

At this point, two key differences between the OTA and the conventional op-amp must be kept in mind. First, since the OTA is a current source, the output impedance of the device is high, in contrast to the op-amp's very low output impedance. Because a low output impedance is often a desirable trait in general amplifiers used to drive resistive loads, certain of the newer commercial OTA's, such as National Semiconductor's LM13600, have on-chip controlled impedance buffers. Second, it is possible to design circuits using the OTA that do not employ negative feedback. In other words, instead of employing feedback to reduce the sensitivity of a circuit's performance to device parameters, the transconductance is treated as a design parameter, much as resistors and capacitors are treated in op-amp based circuits.

The biasing of the OTA's internal circuitry is such that the total quiescent supply current is given by $I_{SUPPLY} = 3I_{ABC}$. This seems to imply that the OTA can be used in micropower applications, even down to $I_{ABC} = 1$ μA. However, the losses in speed and bandwidth, which are controlled ultimately by I_{ABC}, can be severe at such low current levels.

(b) AC Analysis and Frequency Response

Much of the dependence of open and closed-loop bandwidth and frequency responses in the OTA are similar to those in the conventional op-amp. For a circuit employing negative feedback, a very important relationship between the closed-loop bandwidth, the amplifier bias current, and the closed-loop gain exists:

$$BW_{CL} = \left(\frac{20}{V}\right) I_{ABC} I [2\pi C_{NET} A_{CL}(0)] \qquad (2.17)$$

where C_{NET} is the sum of device junction capacitances at the output of the OTA and whatever load capacitance is attached to the circuit: $C_{NET} = C_O + C_L$. Eq. (2.17) has the interesting consequence that certain types of active networks, such as active filters, can

have their critical frequencies controlled by the external current I_{ABC}, which of course can be in turn controlled by an external voltage. External voltage is provided by external biasing circuit or self biasing. But here external voltage is provided by self biasing.

2.5.6 Active Filters with the OTA

Active filters are a standard application of the op-amp which can benefit greatly from the controllability of the OTA. What makes the OTA so attractive in these circuits is the ability to form filter circuits with voltage-variable control (via the I_{ABC} input) over a number of key performance parameters of the filter. The controlled parameter can be the midband gain of the circuit, as already realized in the simple circuits in the previous section. Alternatively, OTA-based active filters can use the external bias setting to control the location of the critical frequency, or 3-dB frequency, in a filter. The next logical step in controllability is the provision for independent gain and critical frequency setting. A number of other active filters can be realized with the OTA. These provide the ability to not only change the critical frequency, the gain, or both, but also to preserve the shape of the response. For instance, one might want to control the critical frequency of the filter, but without altering the passband ripple. It is even possible to change the type of response from lowpass to allpass to highpass by continuous adjustment of the transconductance g_m. Only a very few of these alternatives can be developed here. A very simple example of a first-order (one pole corresponding to a roll-off rate of -20 dB/decade in frequency) lowpass filter is shown in Figure 2.21. The voltage gain over the whole frequency range , and the -3 dB frequency, is given by

$$\frac{V_O}{V_i} = \frac{g_m}{sC + g_m} \tag{2.18}$$

$$f_{3dB} = \frac{g_m}{2\pi C} \tag{2.19}$$

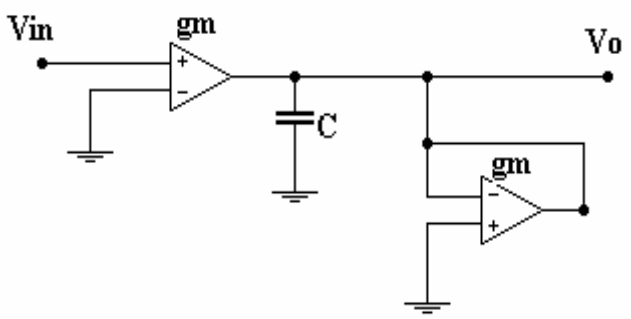


Fig. 2.21 Low Pass Filter

In the Fig. 2.21 the second OTA, labeled "g_{m2}", is configured as a voltage variable resistor. It is this variable resistor which provides the variable cut-off frequency in Eq. (2.19).

Fig. 2.22 shows a second-order filter circuit with three voltage control terminals. Depending on which two of the three terminals are set to ground, one can realize a lowpass, highpass, bandpass, or notch filter. The derivation of the general relationship between the output voltage and the three control voltages is simply obtained:

$$I_{O1} = g_{m1}(V_1^+ - V_1^-) = g_{m1}(V_A - V_{O1})$$

$$V_{C1} = I_{O1}X_{C1} + V_B = V_2^+ = \frac{I_{O1}}{sC_1} + V_B$$

$$I_{O1} = g_{m2}(V_2^+ - V_2^-) = g_{m2}\left(\left(\frac{I_{O1}}{sC_1} + V_B\right) - V_{O1}\right)$$

$V_{O1} = \frac{I_{O2}}{sC_2} + V_C$. Upon substituting I_{O1} and I_{O2} form above, obtain

$V_{O1} = \frac{g_{m1}g_{m2}(V_A - V_{O1})}{s^2 C_1 C_2} + \frac{g_{m2}}{sC_2}(V_B - V_{O1}) + V_C$. Bringing all terms in V_{O1} together and manipulating, finally obtains the transfer relation.

$$V_{O1} = \frac{g_{m1}g_{m2}V_A + sC_1 g_{m2}V_B + s^2 C_1 C_2 V_C}{s^2 C_1 C_2 + sC_1 g_{m2} + g_{m1}g_{m2}} \quad (2.20)$$

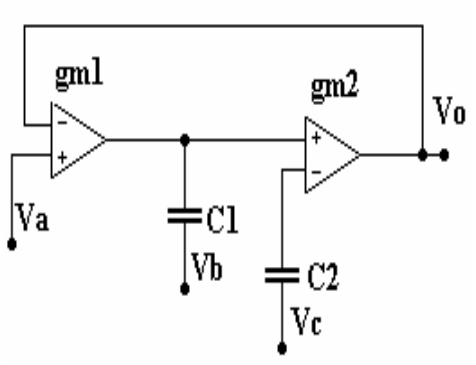


Fig. 2.22 Second Order Filter Circuit

Each of these filters has a critical or center frequency which can be set by varying the transconductance, g_m, of the two OTA's in the circuit. These filters are called adjustable frequency constant-Q filters because they preserve the value of Q while the critical frequencies are shifted.

In the above expressions, s is the complex frequency, s = jω , and I_{01} and I_{02} are the output currents for the first and second OTA's, respectively.

An example of the reduction of Eq. (2.20) to a specific filter type is provided by making the following settings:

- Set $V_{in} = V_A$, V_B and V_C are grounded. V_{O1}
- Set $g_{m1} = g_{m2} = g_m$.
- Divide through by C_1C_2 in both numerator and denominator to achieve a standard biquadratic form.

The result is the following transfer function

$$\frac{V_{O1}}{V_A} = \frac{g_m^2/C_1C_2}{s^2 + \frac{sg_m}{C_2} + \frac{g_m^2}{C_1C_2}} \tag{2.21}$$

This expression has the form of the standard biquadratic circuit [Sedra-91]

$$\frac{V_{O1}(s)}{V_A(s)} = \frac{\omega_O^2}{s^2 + s\left(\frac{\omega_O}{Q}\right) + \omega_O^2} \tag{2.22}$$

Therefore, the circuit with these particular control voltage settings is a lowpass filter with a critical frequency given by

$$f_o = \frac{g_m}{2\pi\sqrt{C_1C_2}} \tag{2.23}$$

and a constant $Q = \sqrt{\frac{C_2}{C_1}}$.

It is straightforward to show that the following transfer functions can be obtained from the indicated control voltage settings:

- $V_{in} = V_B$; V_A and V_C grounded terminal of Bandpass filter.
- $V_{in} = V_C$; V_A and V_B grounded terminal of Highpass filter.
- $V_{in} = V_A = V_C$; V_B grounded terminal of Notch filter.

2.5.7 Some Non-ideal Features of the OTA

One of the biggest drawbacks of the first versions [Harris-96, National-95] of the OTA was the limited range of the input differential voltage swing. This statement must be qualified in at least two ways. First, the limited input voltage swing applies only if the OTA is being used in the open-loop configuration. In that case, if the difference-mode voltage exceeds about 25 mV, and the load resistance is relatively low (so that the open-

loop gain is relatively small), then the circuit is no longer operating in the linear region. This results in the output signal being distorted because of a nonlinear voltage transfer function. Of course, for circuits which make use of negative feedback, i.e., are operated in closed-loop conditions, then linear behavior is maintained.

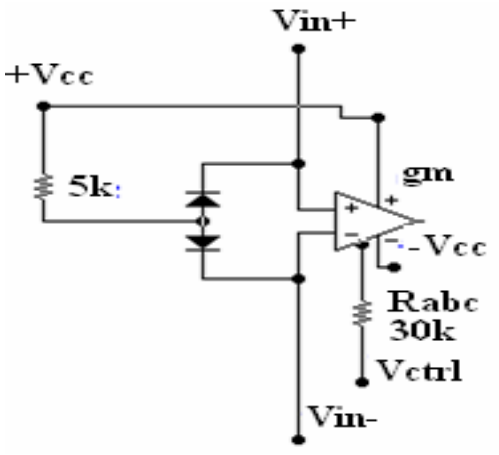


Fig. 2.23 Biasing Scheme for OTA

The second qualifying remark is that the more recent versions of the OTA, such as the Harris CA3280A, National Semiconductor's LM13600, and Philips' NE5517, all use internal linearizing diodes at the input differential pair of the OTA. These make the OTA's output current a linear function of the amplifier bias current over a wide range of differential input voltages. Fig. 2.23 displays a typical biasing scheme for a generic commercial OTA. The control voltage, V_{CTL}, is used to generate the amplifier bias current, I_{ABC}, through the resistor R_{ABC}. The linearizing diodes, which are incorporated on-chip in the commercial OTA's mentioned above, can be biased on through the positive power supply voltage, $+V_{CC}$.

2.6 Common Mode Feedback

2.6.1 Introduction

There are lot of reasons that we use CMFB

• In the past, circuits have mainly one input and one output and both referred to ground.

• Low voltage power supply make single ended circuits very difficult to perform optimally. An alternative to single-ended circuits is to use fully differential circuits.

• To double the output swing, a fully differential circuit are used.

• The output terminals of fully differential circuits are equal and opposite polarity.

• Additional properties of fully differential circuits are: improved output swing, linearity and common-mode rejection ratio.

A CMFB circuit, in a fully differential circuit, is generally needed for two reasons:

(1) To control the common mode voltage at different nodes that cannot be stabilized by the negative differential feedback. This is usually chosen as a reference voltage yielding maximum differential voltage gain and/or maximum output voltage swing

(2) To suppress the common mode components, that tends to saturate different stages, through applying common mode negative feedback.

2.6.2 Common Mode Feedback Scheme

One of the important aspects of the fully differential circuits is the common mode control. While the differential mode negative feedback is done to shape the transfer function, the common mode loop ensures that the circuits operate in a linear region. To achieve robust Q for the biquads, it is important to maintain constant operating currents for the OTAs across supply voltage variations, process corners and mismatches. To keep the current sources from entering the triode region, the common mode voltages must be maintained accurately. A typical common-mode feedback (CMFB) loop used in the context of an OTA-C filter is shown in Fig. 2.24.

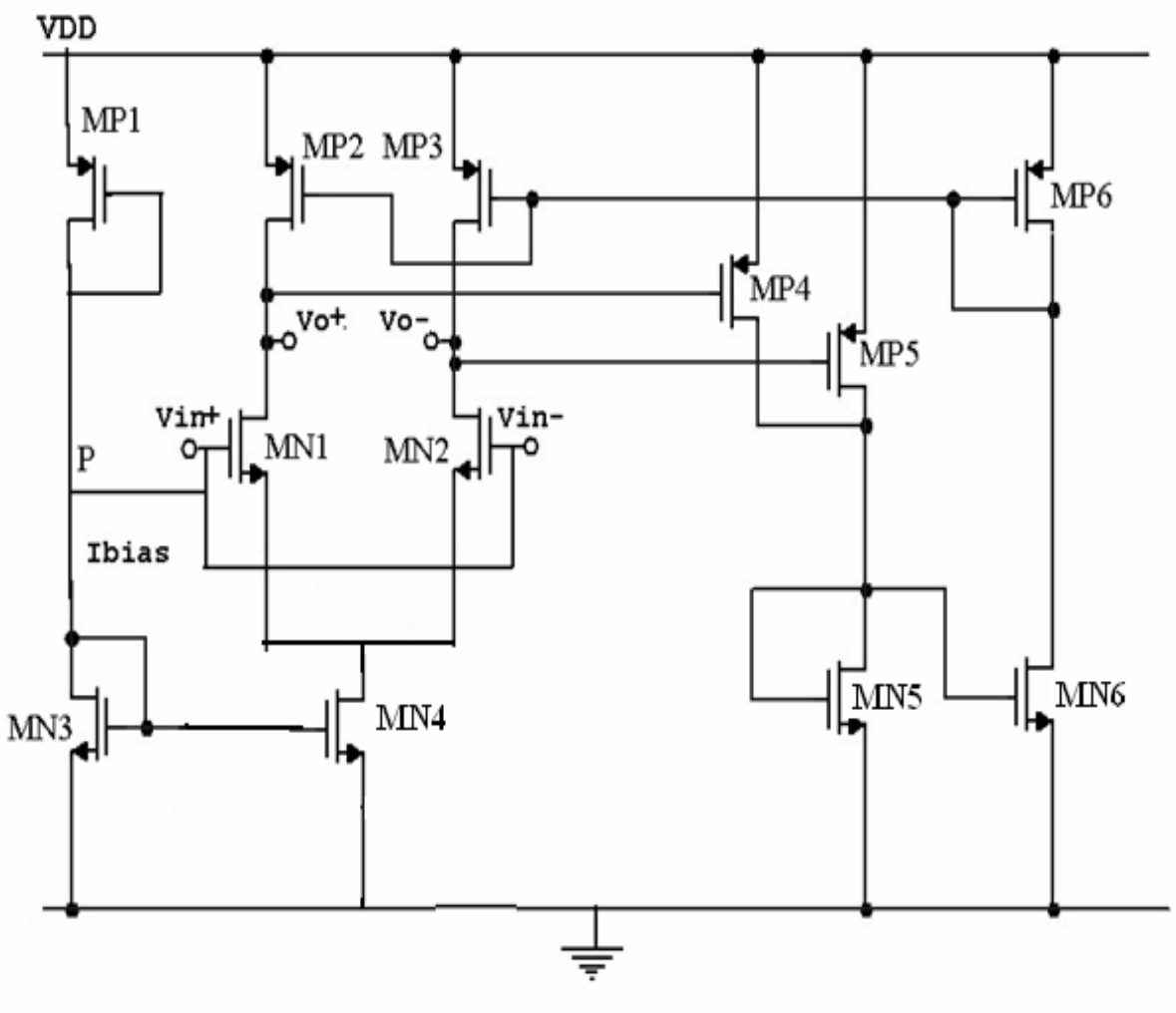


Fig. 2.24 Design Of OTA with Common Mode Feedback

Here the output common mode voltage of OTA is sensed at the common drain node of MP6 and MP7. The CMFB error amplifier (AC) compares the sensed common mode to the ideal common mode voltage and the correction voltage is applied to the gate of MP2 and MP3. This controls the gate voltage of load which adjusts the common mode voltage for OTA. The overall common mode loop is kept under negative feedback for a stable common mode operation. V_{cmref} is to be maintained lower than the ideal common mode voltage

Thus the CM accuracy of a system is determined by the common-mode transconductance gain and the fact that the OTA output has large CM gain is irrelevant [19]. This fact can be explained here. Suppose ΔI is the difference between the currents MP2 and MP3 (load

transistors of main OTA in Fig. 2.24) would pass under short circuit load condition. In other words if DI is the offset current between the NMOS and PMOS current source and AC(0) is the DC gain of the EA, the error in the output CM voltage of OTA under closed loop condition is simply given by

$$V_{CM\_ERROR} = \frac{\Delta I}{g_m * AC(0)} \tag{2.24}$$

This can be viewed as the offset current being absorbed by the offset voltage times the DC transconductance gain of the loop (gm5*AC(0)). Thus, the two important aspects of the CMFB loop design are its DC transconductance gain (gm5*AC(0)) and open loop unity-gain-bandwidth achieved for a stable loop phase margin. The DC gain of the error amplifier determines the controllability and accuracy of the DC operating point while bandwidth determines the frequency range for which the common mode noise would be effectively rejected. As a conservative specification bandwidth of the common mode loop can be kept as high as the signal band-width. This ensures that the CMFB loop would govern the common-mode rejection for the entire signal band. However, taking into account that the next stage, which is differential in nature, would also have a finite common mode rejection, the band width specifications can be relaxed. A common mode bandwidth of half the signal bandwidth can be chosen as specification.

CHAPTER 3

CIRCUIT IMPLEMENTATION

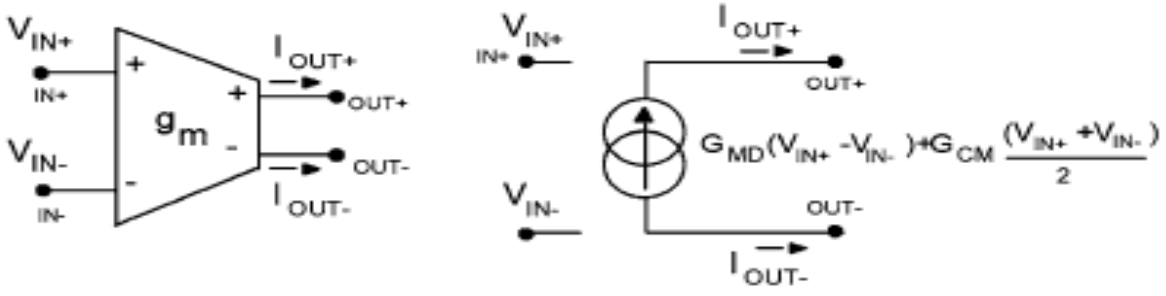
3.1 Circuit Implementation of OTA

3.1.1 Specifications for the OTA

Considering the filter design specifications and the chosen OTA architecture, the transconductor was designed using the g_m/I_D methodology. The specifications of the OTA are the following: transconductance gain = 35 dB, input common mode range ICMR = -1.15 V to 2.15 V, slew-rate SR > 25V/μs, output load C_L = 3pF, Rout > 4MΩ (for a minimum Q of 25) and V_{DD} = 3.3 V and V_{SS} = 0 V.

3.1.2 Implementation of OTA

OTA symbol and operations, even if the OTA can implement narrow band amplifiers or filters the circuit also acts as a large-band amplifier. Therefore the frequency performance of a non-ideal or real OTA is generally estimated from its -3 dB bandwidth. The OTA can then be viewed like a low-pass filter with a corner frequency (f_c) that is also equal to the OTA cut-off frequency.



(a) (b)

Fig. 3.1 Fully differential OTA. (a) Conventional symbol, (b) equivalent

circuit with common mode transconductance In this bandwidth of operation (DC to f_c) the OTA performances can be estimated with interest without taking into account the effect introduced by the parasitic capacitances. The usually symbol of the OTA is shown in Fig. 3.1(a). Fig. 3.1(b) corresponds to its equivalent electrical circuit including the non-ideal common mode transconductance effect. In Fig. 3.1(a), the ideal OTA corresponds to $G_{MD} = g_m$ and $G_{CM} = 0$. The ideal fully differential OTA is not more than a voltage controlled current source (VCCS).

Differential mode performance of the real OTA can be estimated by introducing the common mode gain effect. In case of OTA, this gain is a common-mode transconductance. The common-mode rejection ration (CMRR) is then the ratio between the common mode transconductance (G_{CM}) and the differential mode transconductance (G_{MD}). Note that for the OTA in Fig. 3.1(a) $G_{MD} = g_m$. Because a real OTA exhibits an output parasitic impedance, the load system configuration is generally made with grounded impedance. Thus the study presented here will focus on the configuration with equivalent grounded impedance connected at node OUT+ and node OUT-. In this section, all equations are given at small-signal amplitude.

Fig. 3.2 shows the operational transconductance amplifier (OTA) used in the filter implementation. Again, a simple structure was selected that demonstrated the capabilities of the technology and the transconductor design methodology. Because of the fully differential circuit, a common-mode feedback circuit (CMFB) is needed to set the DC output level of the OTA. A simple circuit is used that amplifies the common-mode signal while rejecting the differential signal. The source degeneration technique [5] was used for the transconductor linearization.

3.2 Design Implementation of the Core OTA

Considering the filter design specifications and the chosen OTA architecture, the transconductor was designed using the g_m/I_D methodology.

For each transistor, the g_m/I_D factor is chosen, and then the normalized current I_D/(W/L) is determined for each transistor from the g_m/I_D vs. I_D/(W/L) curve for the target technology. Then, with the drain current value found, the W/L of each transistor can be obtained.

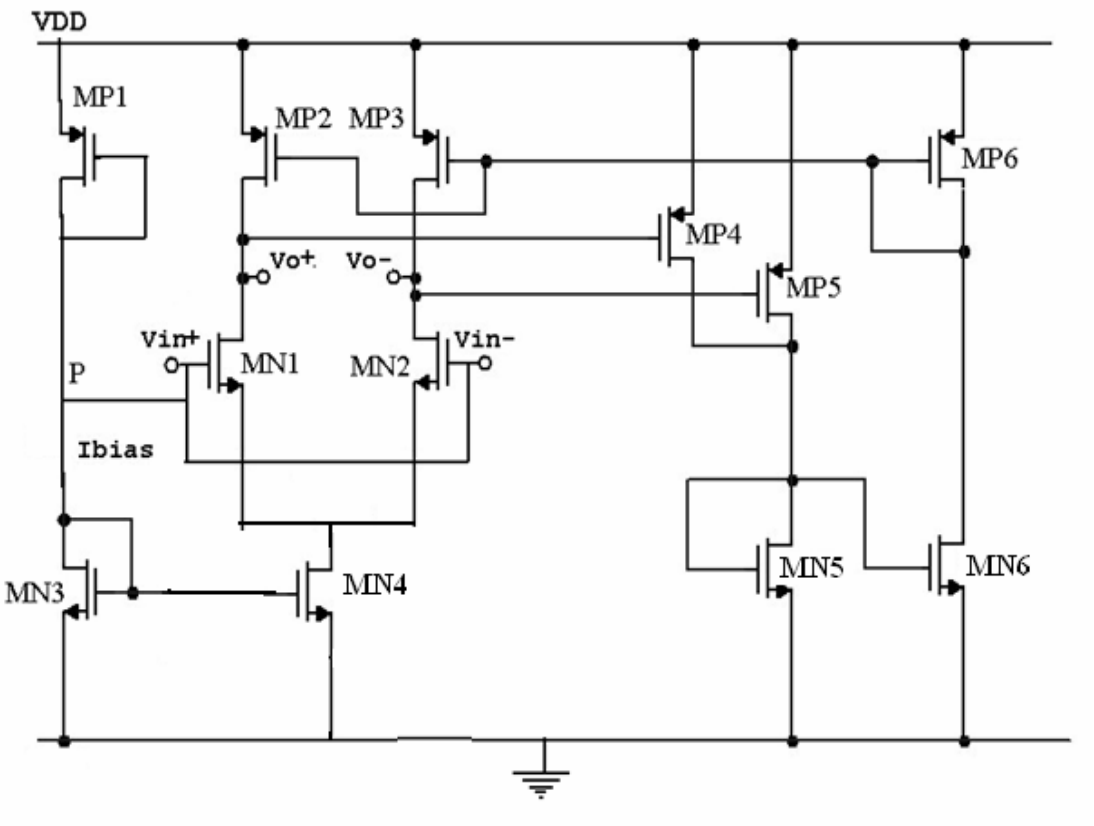


Fig. 3.2. OTA used for the filter implementation.

The complete design procedure is demonstrated as follows:

1. Considering SR specification, the bias current is determined:
   Ibias ≥ SR.C_L, Ibias → = 75µA ;
2. From the transconductance gain requirement of 35 dB and I_{D1}=12.5µA, the g_m/I_D ratio of the NMOS differential pair (MN1-MN2) can be determined:
   $(g_m/I_D)_{N1} = (g_m/I_D)_{N2} = 5 \rightarrow (W/L)_{N1} = (W/L)_{N2} = 1.29$;
3. The current mirror transistors (MN3-MN4) are operated in strong inversion to guarantee good matching and noise properties. Thus we choose:

$(g_m/I_D)_{N3} = (g_m/I_D)_{N4} = 1.70 \rightarrow (W/L)_{N3} = (W/L)_{N4} = 0.5$;

4. The load transistors (MP2-MP3) should also operate in strong inversion : $(g_m/I_D)_{P2} = (g_m/I_D)_{P3} = 9.09 \rightarrow (W/L)_{P2} = (W/L)_{P3} = 7.50$;
5. For the CMFB circuitry (MP4, MP5, MP6, MN45, MN6), to guarantee stable bias conditions we have: $GWB_{CMFB} \geq GBW_{M1,M2}$. Thus, $(g_m/I_D)_{P4,P5} = 2$, $(g_m/I_D)_{P6} = 3.5$ and $(g_m/I_D)_{N5,N6} = 2$;
6. Here transistor MP1 provides the biasing voltage of 1.65 V at input and giving the bias current of 75 µA, the value of $(W/L)_{P1} = 1.43$

The required plots for obtaining the values of (W/L)'s from g_m/I_D Methodology are giving in the Plots Fig 3.3 and Fig. 3.4.

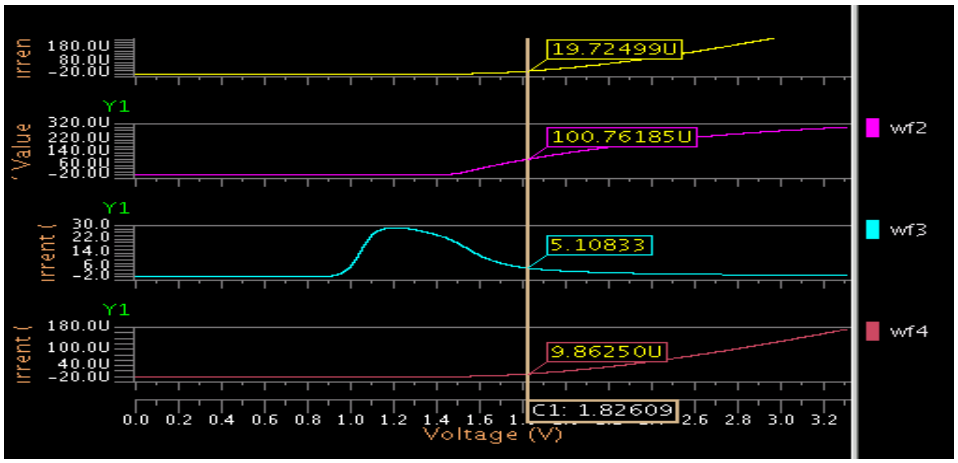


Fig. 3.3 Getting the value of MN1, MN2

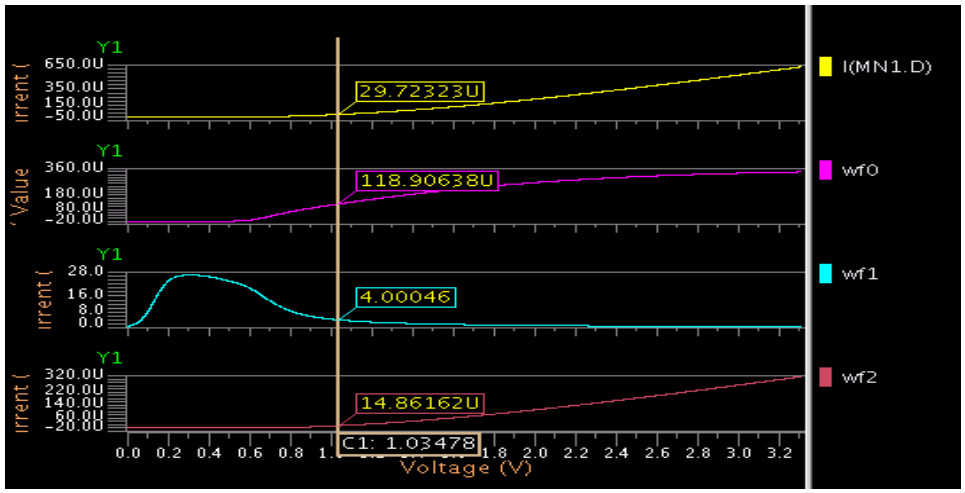


Fig. 3.4 Getting the value of MN3, MN4

By the same way the values of all (W/L)'s have been gotton.

The designed values for the transistors sizes are shown in Table 1 after iterations. Here after iterations the circuit have made circuit in such a way that the DC voltage of output node of the first stage is on 1.65 V. This will provide a DC input to the next OTA stage.

Table 3.1. OTA transistor dimensions obtained through the design methodology

Name of Transistor	(W/L)
MN1, MN2	36.28
MN3, MN4	0.714
MN5, MN6	0.714
MP1	1.428
MP2, MP3	1.285
MP4, MP5	0.714
MP6	2

The fully-differential continuous-time Gm-C band-pass filter was then implemented according to the topology showed in Fig. 3.5, using the design OTA as transconductors. All transconductors operate with one common bias generating circuit, which improves the matching between the filter's stages over the tuning range.

3.2 Circuit Implementation of Filter

The full design of Filter has been made by using the following architecture.Fig.

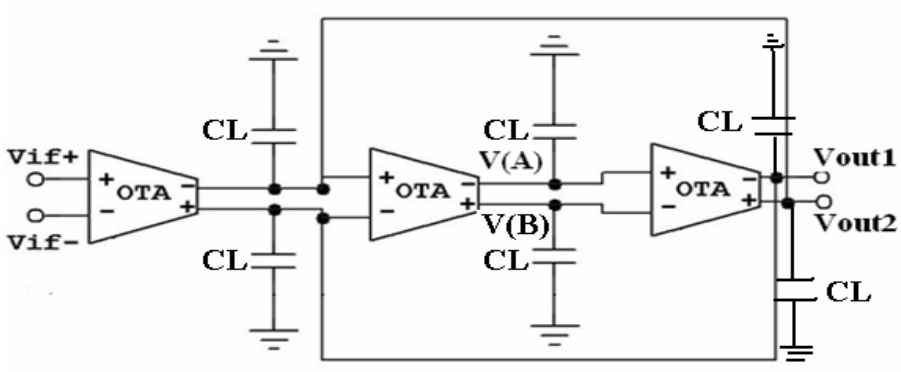


Fig. 3.5 Filter Design using OTA

Here the DC voltage of all output nodes of each stage is almost equal to 1.65 V

CHAPTER 4

SIMULATION AND RESULTS

In this Chapter the schematic of the circuit has been simulated for various parameters. All values have been measured at load capacitance of 3pF. Prepared circuit of filter is simulated at mentor graphics ASIC design kit, design architect IC tool at 0.35µ technology. This filter is to be powered from a 3.3 volts power supply and with a power dissipation of 952µW. The current sources/sinks required for biasing are used from output stage.

Based on the OTA, input stage is fully self biased, a Gm-C bandpass filter has been designed. The simulations include AC response, Transient analysis, DC Response. The responses have been checked for temperature variation, Load capacitance variation and power supply variation. There is no need to give any DC at the input because this circuit is fully self biased that's why there is no need to make any biasing circuit.

4.1 AC Analysis:

On applying AC of 10 mv and DC of 0 V at input terminal of designed filter. (here V_{DD} is 3.3V with respect to ground),

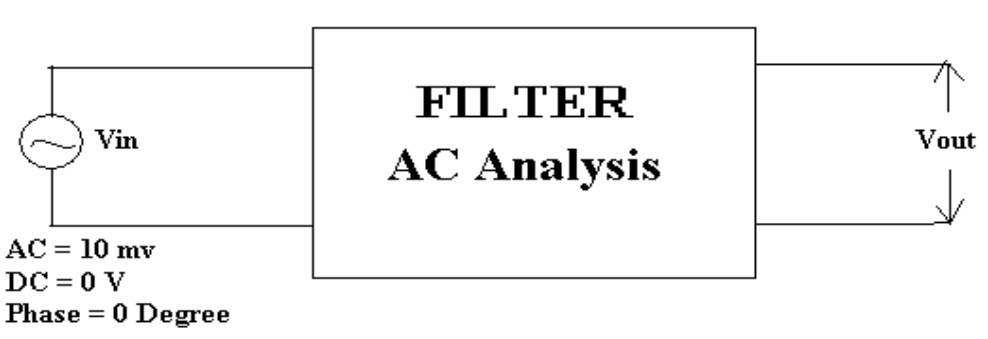


Fig. 4.1 AC Analysis for a Filter

the netlist and the simulated AC results for the gain (magnitude in dB) with respect to frequency(Hz) has been plotted by using TSMC 0.35µm on ELDO tool(Mentor Graphics), is given in Fig.4.2 (a) and (b) respictevely.

4.1.1 Simulation Details of AC Analysis

```
***** ANALYSIS ....

***** 0  error(s).
***** 0  warning(s).


***** GENERATION ...

***** 0  error(s).
***** 0  warning(s).

INFORMATION ABOUT COMPILATION...

Memory space allocated (bytes): 4676469
44 elements
18 nodes
1 input signals

Eldo VERSION : ELDO v6.9_1.1 Production(64 bits) Wed Jun 13 08:32:47 GMT 2007

*** DATE: 11-Jul-2009 13:42:20

*** TITLE: * Component: /home/vaibhav/filter21  Viewpoint: tsmc035a

TEMPERATURE : 27.000000 degrees C

Performing DC analysis...

--> Partitioning circuit...

***> DC CPU TIME 0s 080ms <***

DC:67 iterations FOR DC analysis
A               688.6765M
B               1.8540
E               748.2010M
N$1             1.3346
N$10            1.6561
N$11            844.2461M
N$12            748.2010M
N$15            1.6561
N$16            1.8506
N$18            1.8540
N$2             1.3384
N$3             1.3346
N$625           1.5069
N$8             847.8673M
VDD             3.3000
VIN             1.5069
VOUT1           1.6606
VOUT2           1.6606

   TOTAL POWER DISSIPATION:  952.1001U   WATTS

Connecting to JWDB server, please wait...
connected to wdb server : -jwdbhost VLSI_SMDP11_3 -jwdbport 33049


***>AC analysis starts

***>AC analysis completed

***>CPU TIME 0s 010ms <***


***>Current simulation completed
```

4.1.2 Plot for AC Analysis

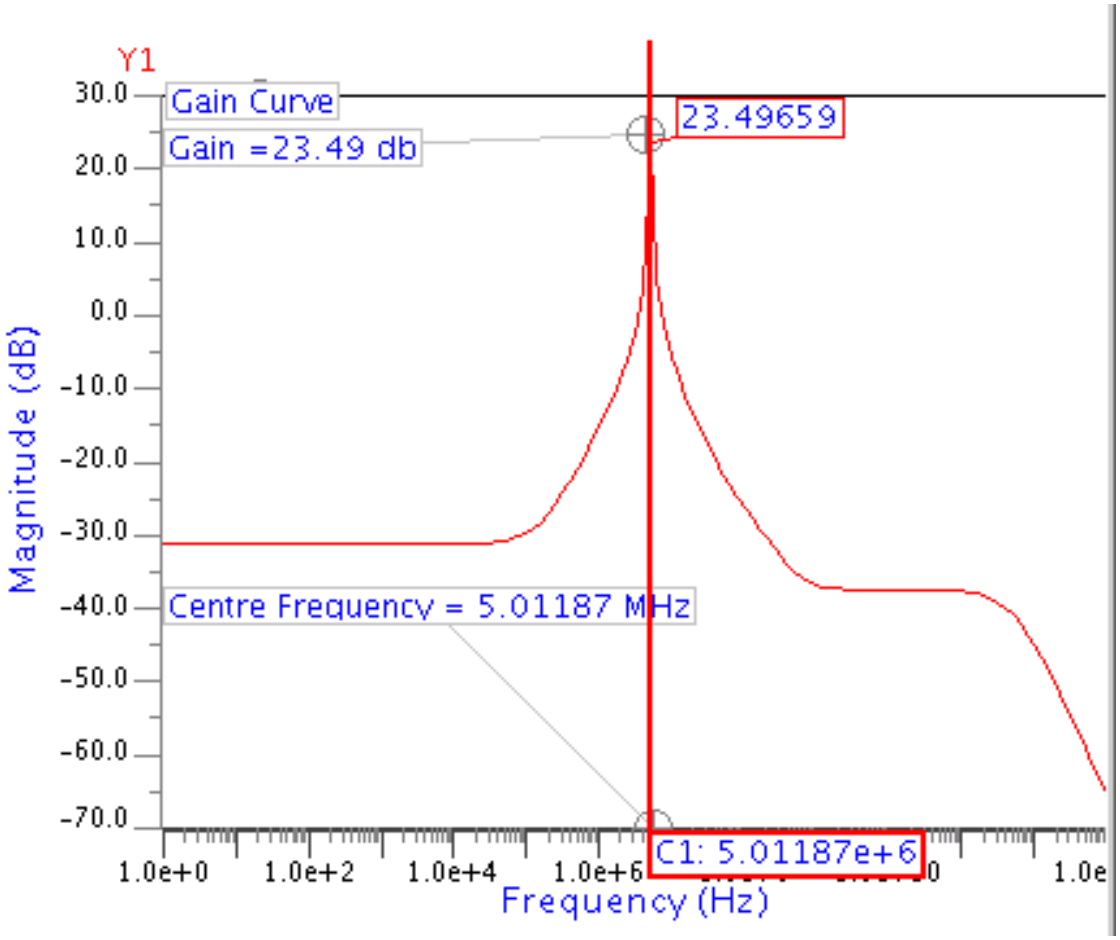


Fig 4.2 Plotted AC Response of Filter

From Fig 4.2, plotted waveforms, the following parameters have been obtained as in Table 4.1.

Table 4.1 Obtained Parameters for AC Analysis

Centre Frequency	**5.01187 MHz**
Gain at the centre frequency	**23.49659 dB**
Lower Bandwidth	**4.90 MHz**
Upper Bandwidth	**5.16 MHz**
Quality Factor	**19.2844**
Power Dissipation	**952 µW**

4.2 Transient Analysis

For observing the transient response of the filter the test setup of Fig. 4.3 must be used. In this setup sinusoidal signals are applied to the two inputs and the effective value of input signal is the difference of the voltage at the two terminals. No DC potential is applied along with the sinusoidal signal because the circuit is fully self biased.

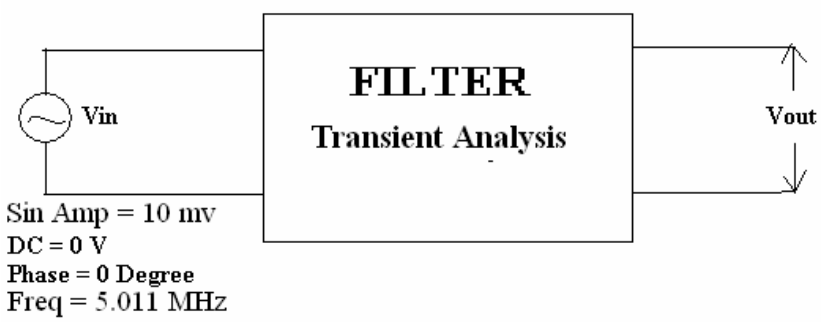


Fig 4.3 Transient Analysis for a Filter

4.2.1 Simulation Details for Transient Analysis

```
****** ANALYSIS ....

****** 0  error(s).
****** 0  warning(s).


****** GENERATION ...

****** 0  error(s).
****** 0  warning(s).

INFORMATION ABOUT COMPILATION...

Memory space allocated (bytes): 4675038
44 elements
18 nodes
2 input signals

Eldo VERSION : ELDO v6.9_1.1 Production(64 bits) Wed Jun 13 08:32:47 GMT 2007

*** DATE: 11-Jul-2009 13:46:20

*** TITLE: * Component: /home/vaibhav/filter21  Viewpoint: tsmc035a

TEMPERATURE : 27.000000 degrees C

Performing DC analysis...

--> Partitioning circuit...

***> DC CPU TIME 0s 080ms <***

DC:67 iterations FOR DC analysis
```

```
A               688.6765M
B               1.8540
E               748.2010M
N$1             1.3346
N$10            1.6561
N$11            844.2461M
N$12            748.2010M
N$15            1.6561
N$16            1.8506
N$18            1.8540
N$2             1.3384
N$3             1.3346
N$625           1.5069
N$8             847.8673M
VDD             3.3000
VIN             1.5069
VOUT1           1.6606
VOUT2           1.6606

   TOTAL POWER DISSIPATION:  952.1001U   WATTS


Eldo NEWTON: VNTOL=1.000000e-06 RELTOL=7.500000e-04

Connecting to JWDB server, please wait...
connected to wdb server : -jwdbhost VLSI_SMDP11_3 -jwdbport 33085

Compute from 0.000000 Nano to 1.000000E+05 Nano
++++++++++++++++++++++++++++++++++++++++++++++++
Simulation progress           : 10%
Elapsed CPU time              : 0h 0mn 0s 230
++++++++++++++++++++++++++++++++++++++++++++++++
Simulation progress           : 20%
Elapsed CPU time              : 0h 0mn 0s 450
++++++++++++++++++++++++++++++++++++++++++++++++
Simulation progress           : 30%
Elapsed CPU time              : 0h 0mn 0s 660
++++++++++++++++++++++++++++++++++++++++++++++++
Simulation progress           : 40%
Elapsed CPU time              : 0h 0mn 0s 880
```

```
++++++++++++++++++++++++++++++++++++++++++++++++++++++++
Simulation progress                : 60%
Elapsed CPU time                   : 0h 0mn 1s 330
++++++++++++++++++++++++++++++++++++++++++++++++++++++++
Simulation progress                : 70%
Elapsed CPU time                   : 0h 0mn 1s 550
++++++++++++++++++++++++++++++++++++++++++++++++++++++++
Simulation progress                : 80%
Elapsed CPU time                   : 0h 0mn 1s 770
++++++++++++++++++++++++++++++++++++++++++++++++++++++++
Simulation progress                : 90%
Elapsed CPU time                   : 0h 0mn 1s 990
++++++++++++++++++++++++++++++++++++++++++++++++++++++++
Simulation progress                : 100%
Elapsed CPU time                   : 0h 0mn 2s 220

***>Current simulation completed



SIMULATION INFORMATION
memory size allocated in bytes 5472318
Latency: 0.000000%
average number of newton iterations: 2.988836
nb of components: 116
nb of nodes: 90
nb of MOS or BIP calls: 214500
Number of steps computed: 5016

***>CPU TIME 2s 220ms <***

***>GLOBAL CPU TIME 2s 330ms <***

***>GLOBAL ELAPSED TIME 3s <***

Press the return key to continue.
```

4.2.2 Peak to Peak Voltage

The simulated transient results for the magnitude in volt with respect to time(sec) has been plotted in Fig. 4.4. On applying the input voltage peak to peak of 20mv, output voltage **peak to peak of 269.76 mv** has been obtained.

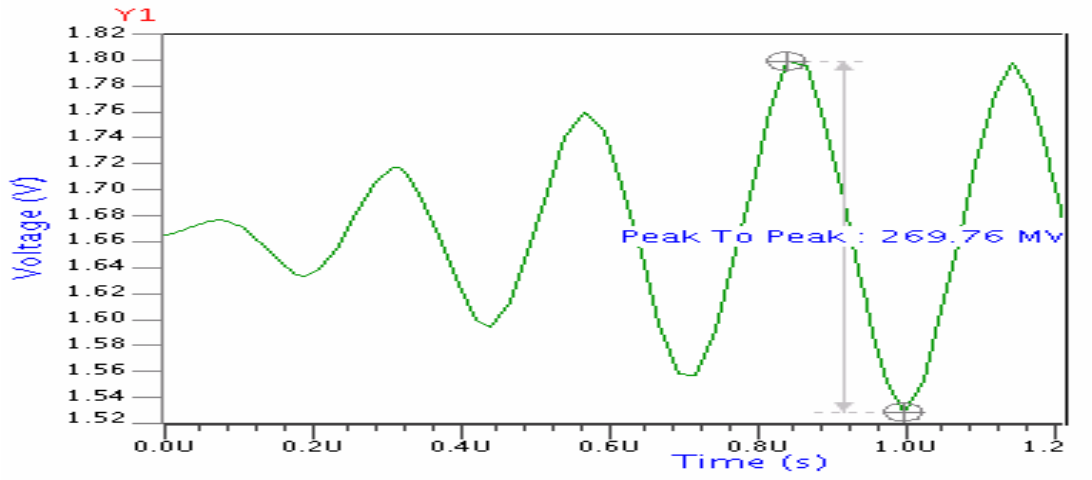


Fig 4.4 Simulated Transient Response for the Filter

4.2.3 Settling Time

The simulated transient results for the magnitude in volt with respect to time(sec) has been plotted in Fig. 4.5. On applying the input voltage peak to peak of 20mv, **settling time of 9.992 µs** has been obtained.

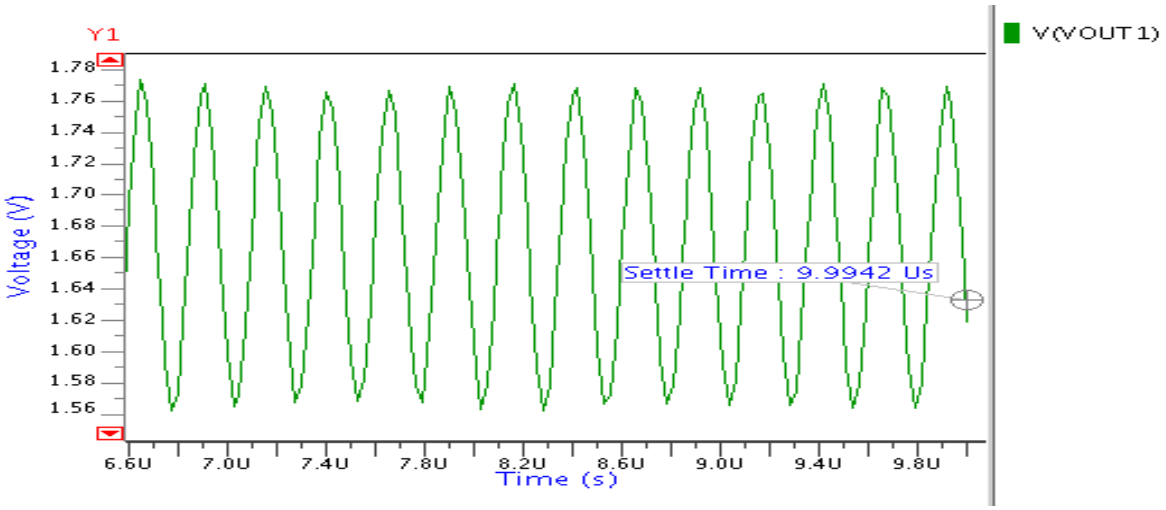


Fig. 4.5 Simulated Transient Response for the Filter

4.3 DC Analysis:

The main response of this circuit is the DC response. As no biasing voltage at the input is used , single voltage source i.e; power supply (V_{DD}) provides the necessary DC voltage at the input. Here the voltage of every node is almost equal to 1.65 volt.

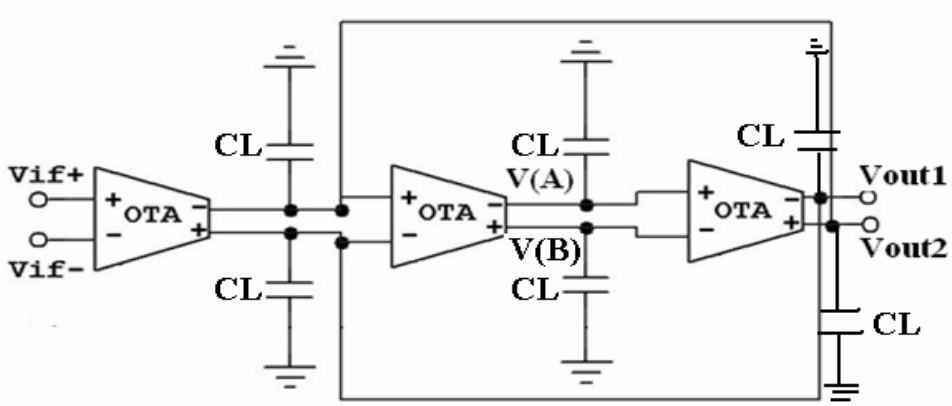


Fig 4.6 DC Analysis of Filter

The plot have V_{DD} variations on X axis and Voltages of these points (V(A), V(B), V_{OUT1} V_{OUT2}) on Y axis.

4.3.1 Simulation Details for DC Analysis

```
***** ANALYSIS ....

***** 0  error(s).
***** 0  warning(s).


***** GENERATION ...

***** 0  error(s).
***** 0  warning(s).

INFORMATION ABOUT COMPILATION...

Memory space allocated (bytes): 4676044
44 elements
18 nodes
1 input signals

Eldo VERSION : ELDO v6.9_1.1 Production(64 bits) Wed Jun 13 08:32:47 GMT 2007

*** DATE: 11-Jul-2009 13:44:14

*** TITLE: * Component: /home/vaibhav/filter21  Viewpoint: tsmc035a

TEMPERATURE : 27.000000 degrees C

Connecting to JWDB server, please wait...
connected to wdb server : -jwdbhost VLSI_SMDP11_3 -jwdbport 33060


--> Partitioning circuit...

***>Current simulation completed
```

4.3.2 Plots for DC Analysis

(a) DC Value of V(A)

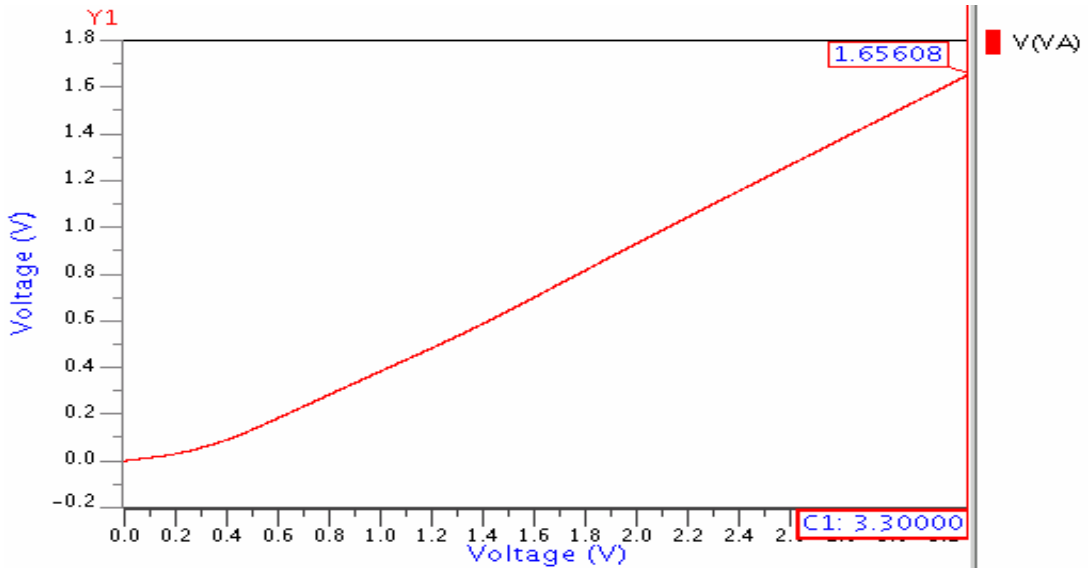


Fig 4.7. Voltage of Node V(A) of the above Fig 4.6

The voltage of node V(A) is plotted in Fig 4.7, When the value of V_{DD} is 3.3 volt, then on this value, the voltage at node V(A) is **1.65608 Volt**.

(b) DC Value of V(B)

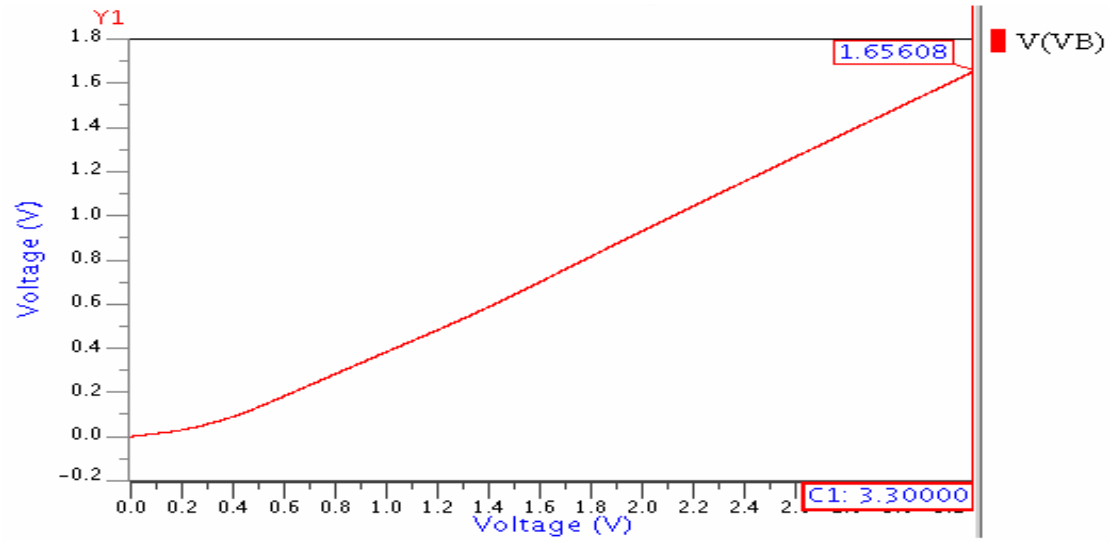


Fig 4.8. Voltage of Node V(A) of the above Fig 4.6

The voltage of node V(B) is plotted in Fig 4.8, When the value of V_{DD} is 3.3 volt, then on this value, the voltage at node V(B) is 1.65608 Volt.

(c) DC Value of V_{OUT1}

The voltage of node V_{OUT1} is plotted in Fig 4.9, When the value of V_{DD} is 3.3 volt, then on this value, the voltage at node V_{OUT1} is **1.66059 Volt**.

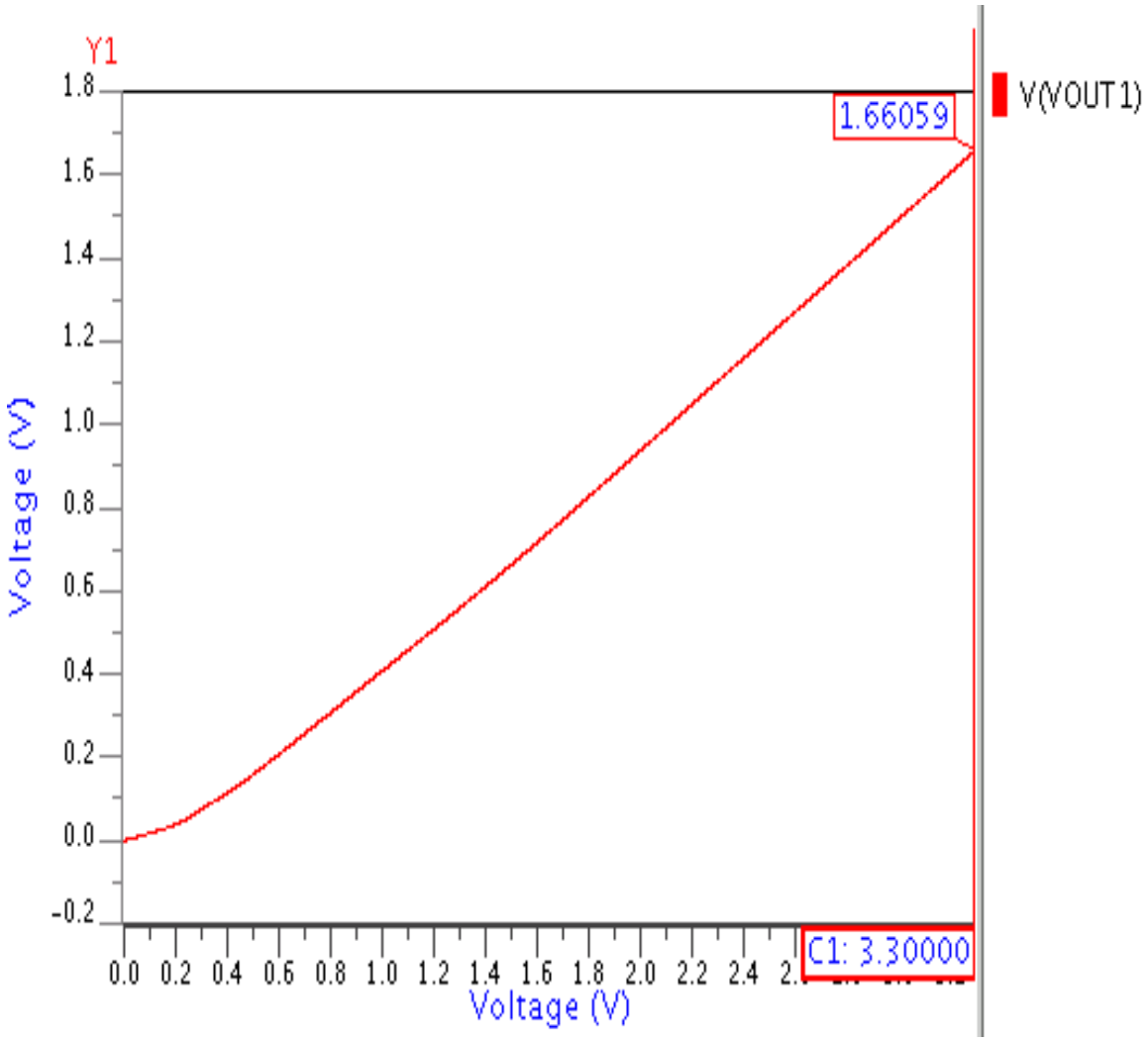


Fig 4.9. Voltage of Node V_{OUT1} of the above Fig 4.6

(d) DC Value of V_{OUT2}

The voltage of node V_{OUT2} is plotted in Fig 4.10, When the value of V_{DD} is 3.3 volt, then on this value the voltage at node V_{OUT2} is **1.66059 Volt**.

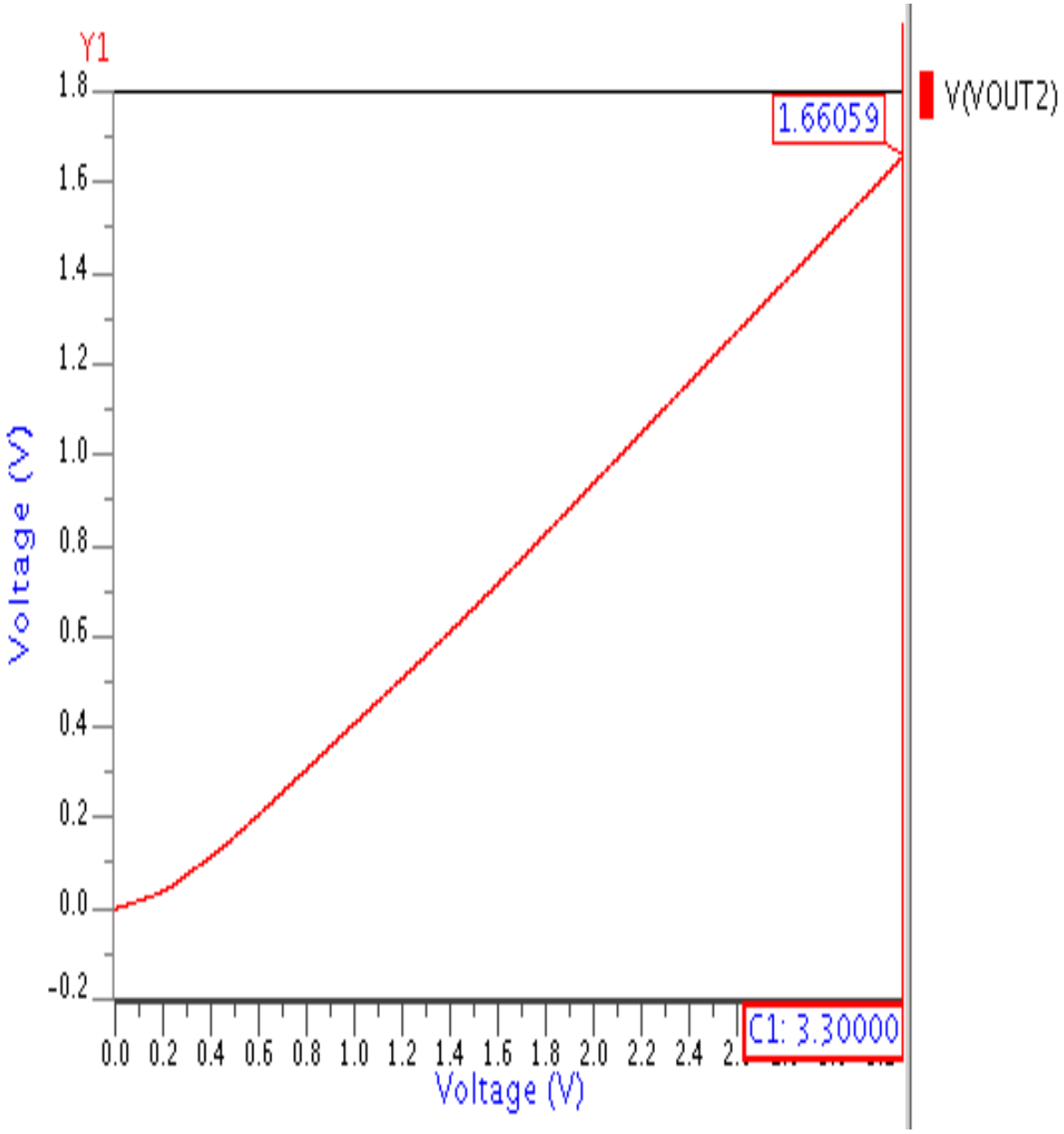


Fig 4.10. Voltage of Node V_{OUT2} of the above Fig 4.6

4.4 Load Variations

On applying different values of load capacitance differences in all the achieved parameters have been obtained. The achieved parameters has been plotted in the following figures for three different (2.5 PF, 3 PF, 3.5 PF) values.There may be load variations due to paracitics on the output node.

4.4.1 At C_L = 2.5 PF

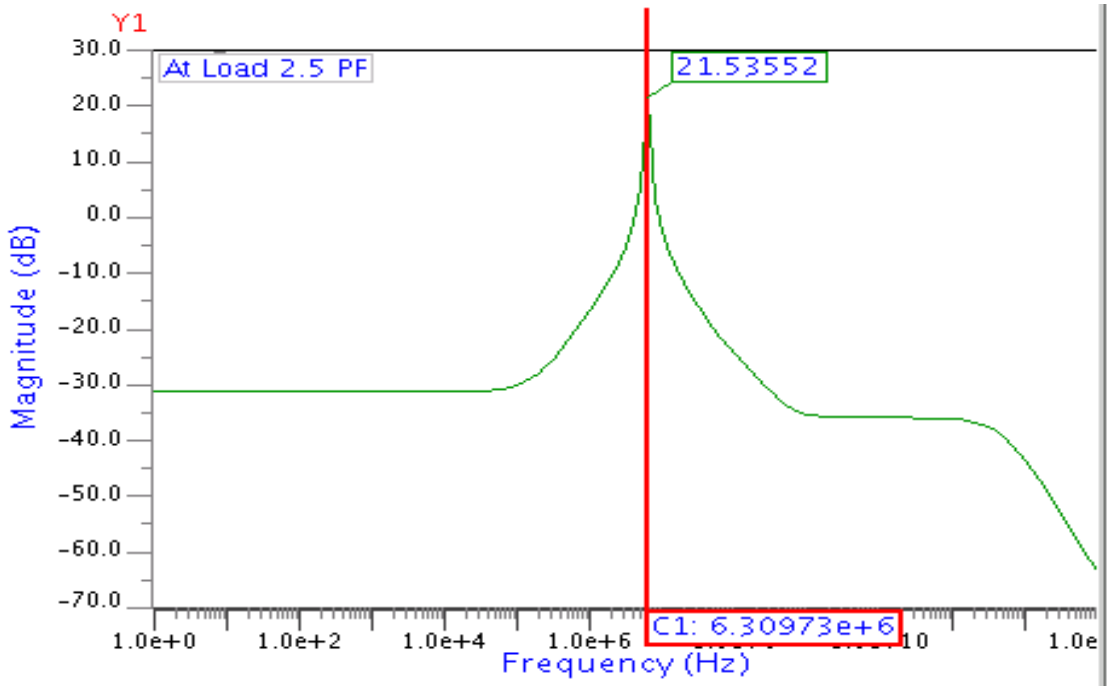


Fig 4.11 AC Analysis at C_L = 2.5 PF

4.4.2 At CL = 3

PF

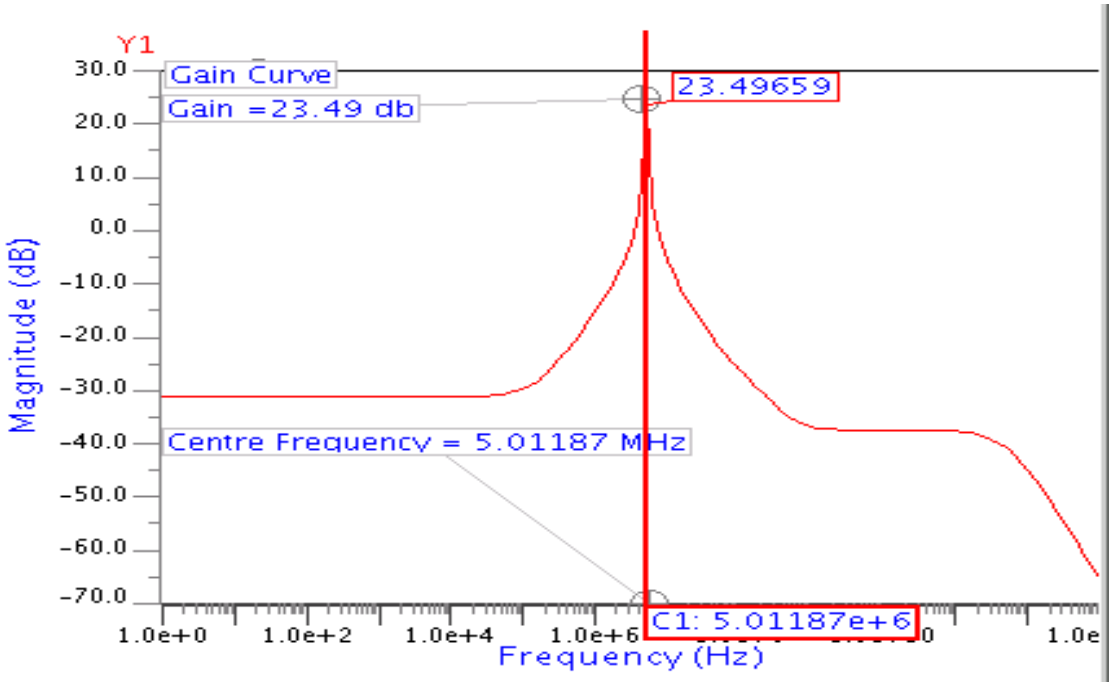


Fig 4.12 AC Analysis at C_L = 3 PF

4.4.3 At CL = 3.5 PF

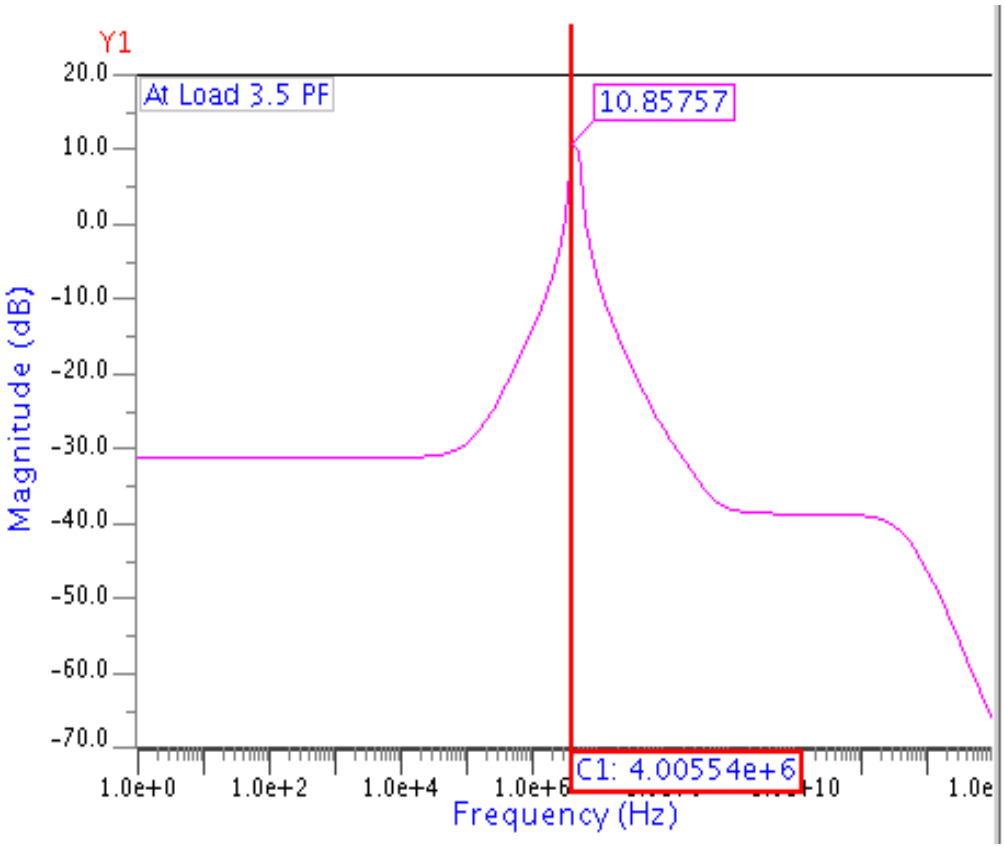


Fig 4.13 AC Analysis at C_L = 3.5 PF

From Figs 4.11, 4.12 and 4.13, plotted waveforms, the following parameters have been obtained as in Table 4.2.

Table 4.2. Obtained Parameters for different Loads

Achieved Parameters	**C_L = 2.5 pF**	**C_L = 3 pF**	**C_L = 3.5 pF**
Centre Frequency	6.3097 MHz	5.01187 MHz	4.0055 MHz
Gain at the centre frequency	21.53 dB	23.49659 dB	10.85757 dB
Lower Bandwidth	6.48 MHz	4.90 MHz	3.81 MHz
Upper Bandwidth	6.15 MHz	5.16 MHz	5.12 MHz
Quality Factor	19.1203	19.2844	2.0646

According to Table 4.2 this has to be seen that at the value of C_L = 3.5 pF, the performance decreases in all parameters, but at the value of C_L = 3 pF this circuit gives the best performance.

4.5 Temperature Variations

On applying different values of temperature there are changes in all achieved parameters. Thae achieved parameters has been plotted in the following figures for three different (25^0C, 27^0C, 29^0C,) values of temperatures.i.e,

4.5.1 AC Analysis

AC analysis have been done first for all three temperatures.

(a) At 25^0C

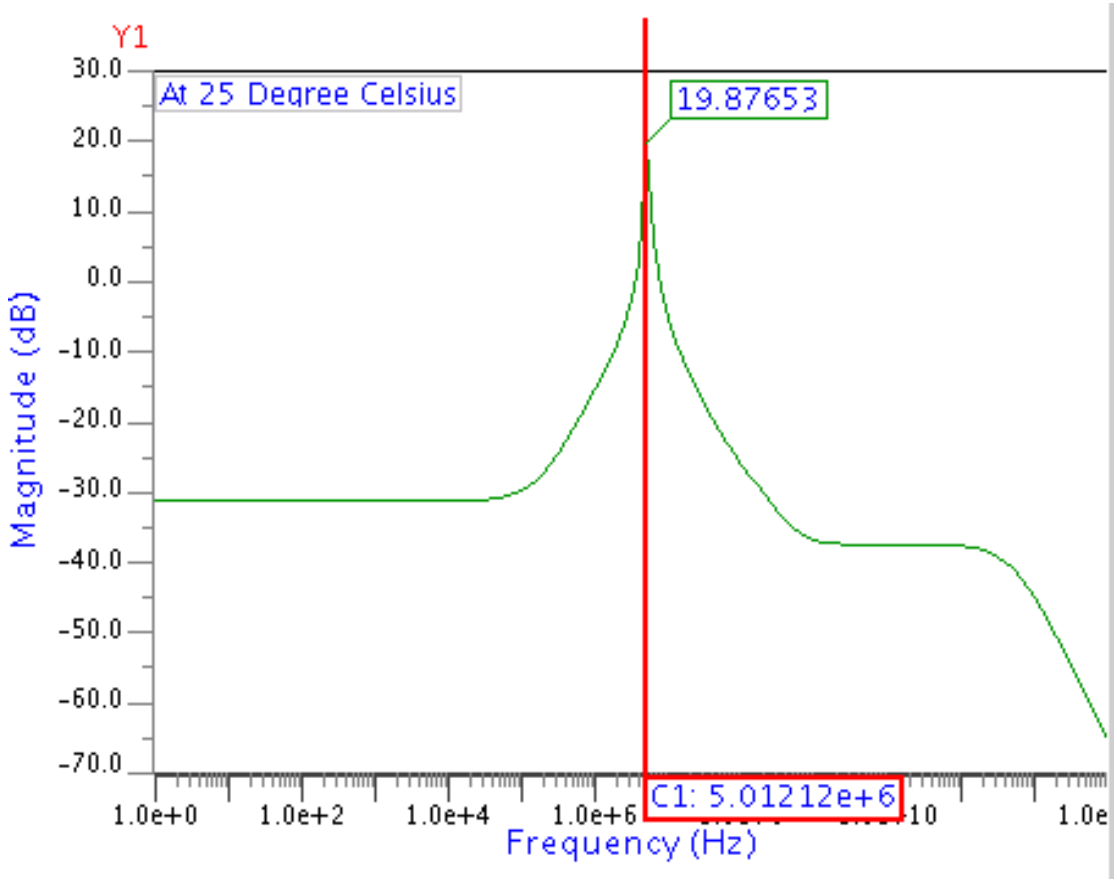


Fig 4.14 AC Analysis at T = 25^0C

(b) At 27^0C

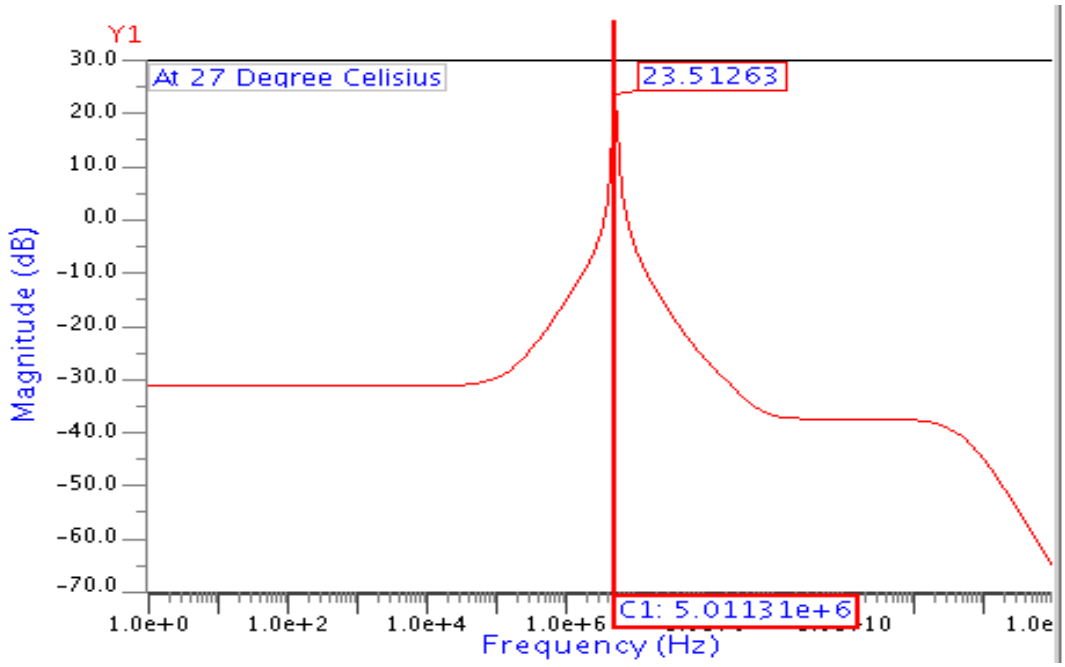


Fig 4.15 AC Analysis at T = 27^0C

(c) At 29^0C

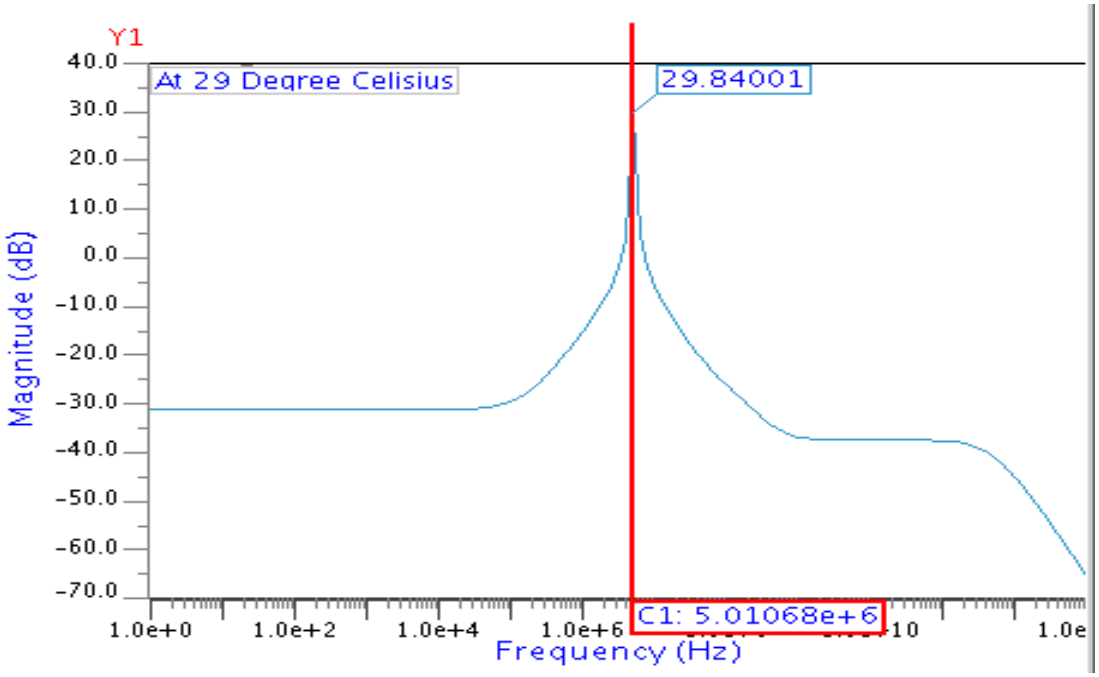


Fig 4.16 AC Analysis at T = 29^0C

From Figs 4.14, 4.15 and 4.16, plotted waveforms, the following parameters have been obtained as in Table 4.7.

Table 4.3. Obtained Parameters for different Temperatures

Achieved Parameters	**T = 25^0C**	**T = 27^0C**	**T = 29^0C**
Centre Frequency	5.012 MHz	5.01187 MHz	5.01068 MHz
Gain at the centre frequency	19.87653 dB	23.49659 dB	29.84001 dB
Lower Bandwidth	4.88 MHz	4.90 MHz	4.93 MHz
Upper Bandwidth	5.195 MHz	5.16 MHz	5.113 MHz
Quality Factor	16.1677	19.2844	27.3807

According to Table 4.3 this has to be seen that as temperature is increasing, every parameter is improving. Gain and Quality factor is maximum at 29^0C.

4.5.2 DC Analysis

The DC analysis have been done for all three temperatures and the values for all three nodes have been plotted.

(a) Effect on V_A

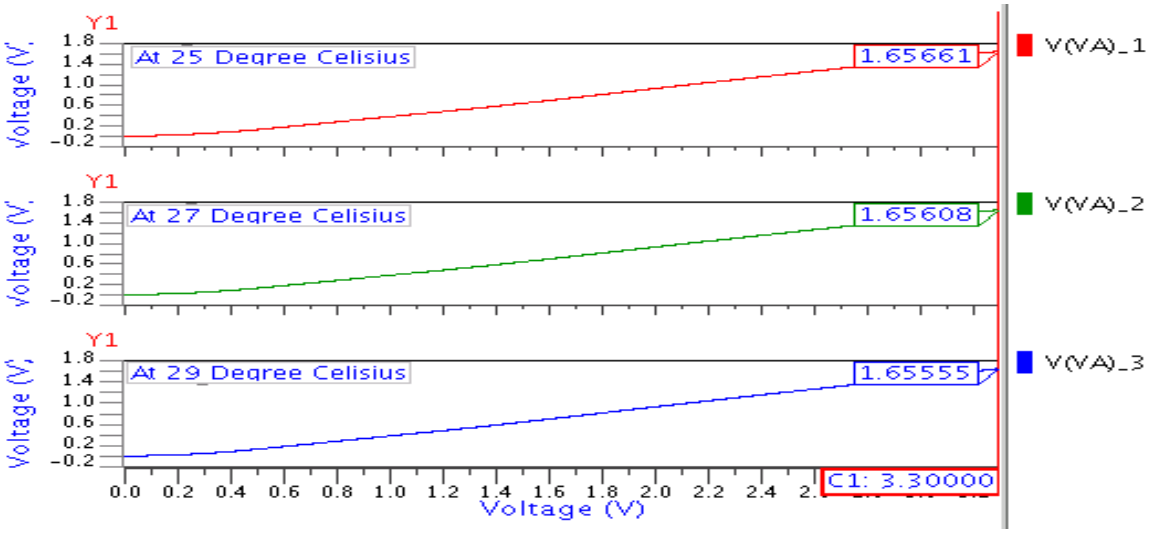


Fig 4.17 DC Analysis on Node V_A

(b) **Effect on V_{OUT1}**

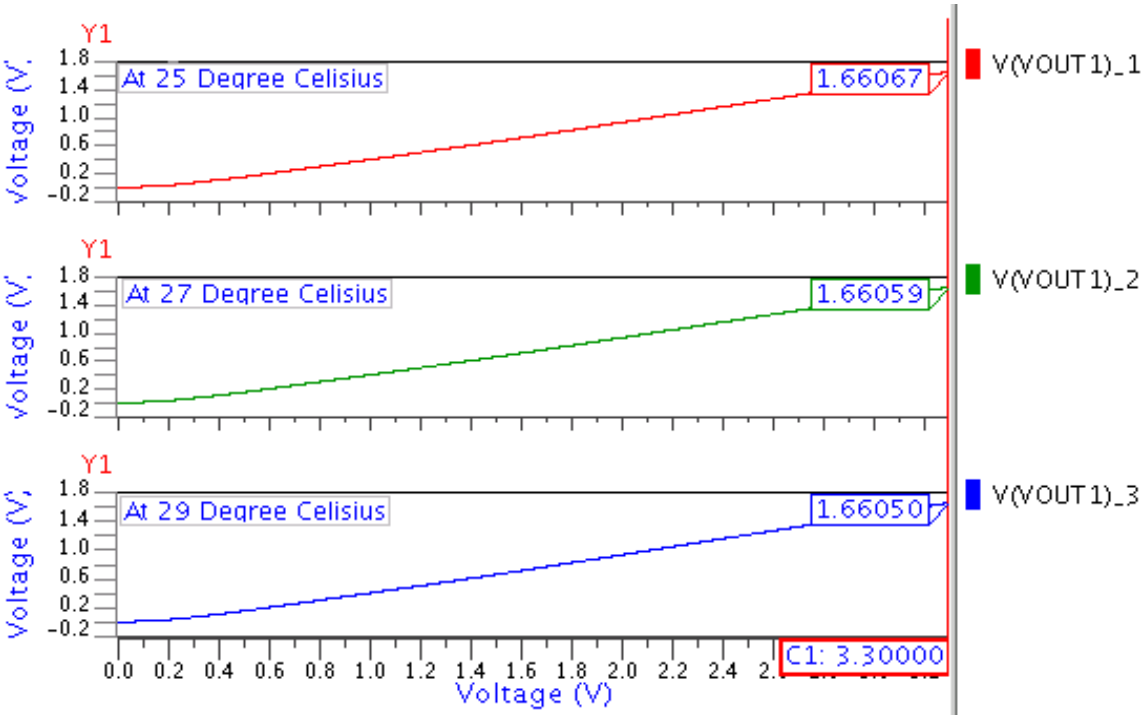


Fig 4.18 DC Analysis on Node V_{OUT1}

(c) **Effect on V_{OUT2}**

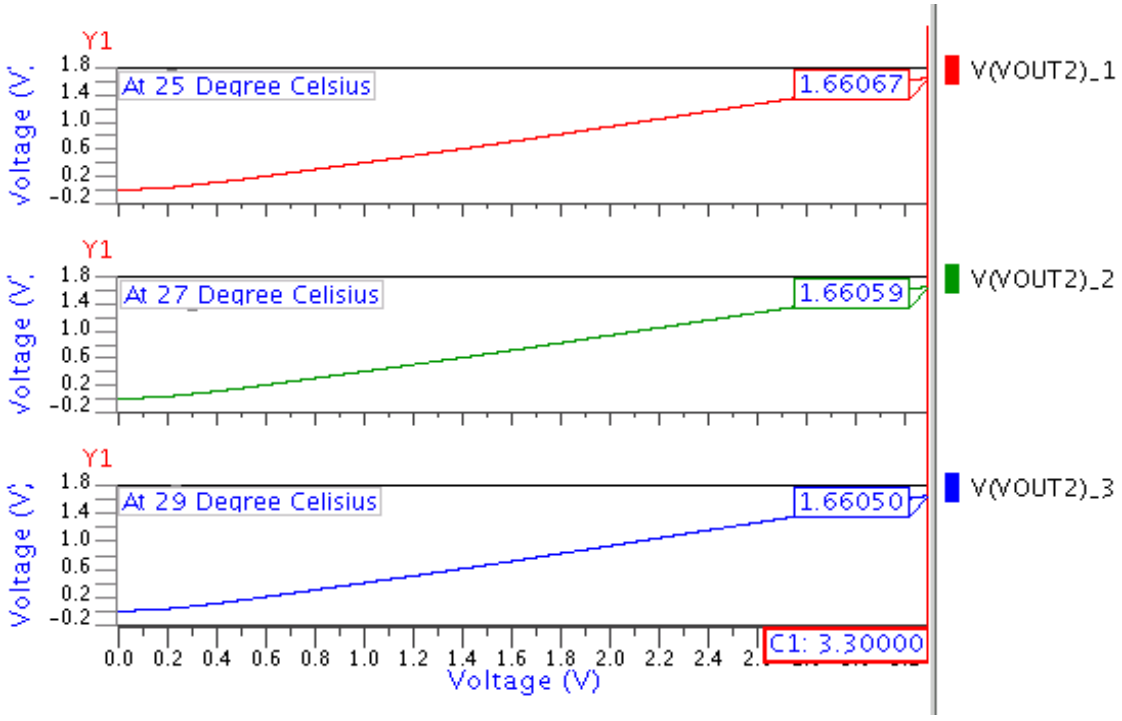


Fig 4.19 DC Analysis on Node V_{out2}

According to the Figs 4.17, 4.18 and 4.19 this has to be seen that there is no effect on the DC voltages of all nodes. So this has to be said that the circuit is resistant for common mode signal and can be operated on different temperatures.

4.6 Power Supply Variations

The effect of the variation in power supply have been plotted.

4.6.1 At V_{DD} = 3 V

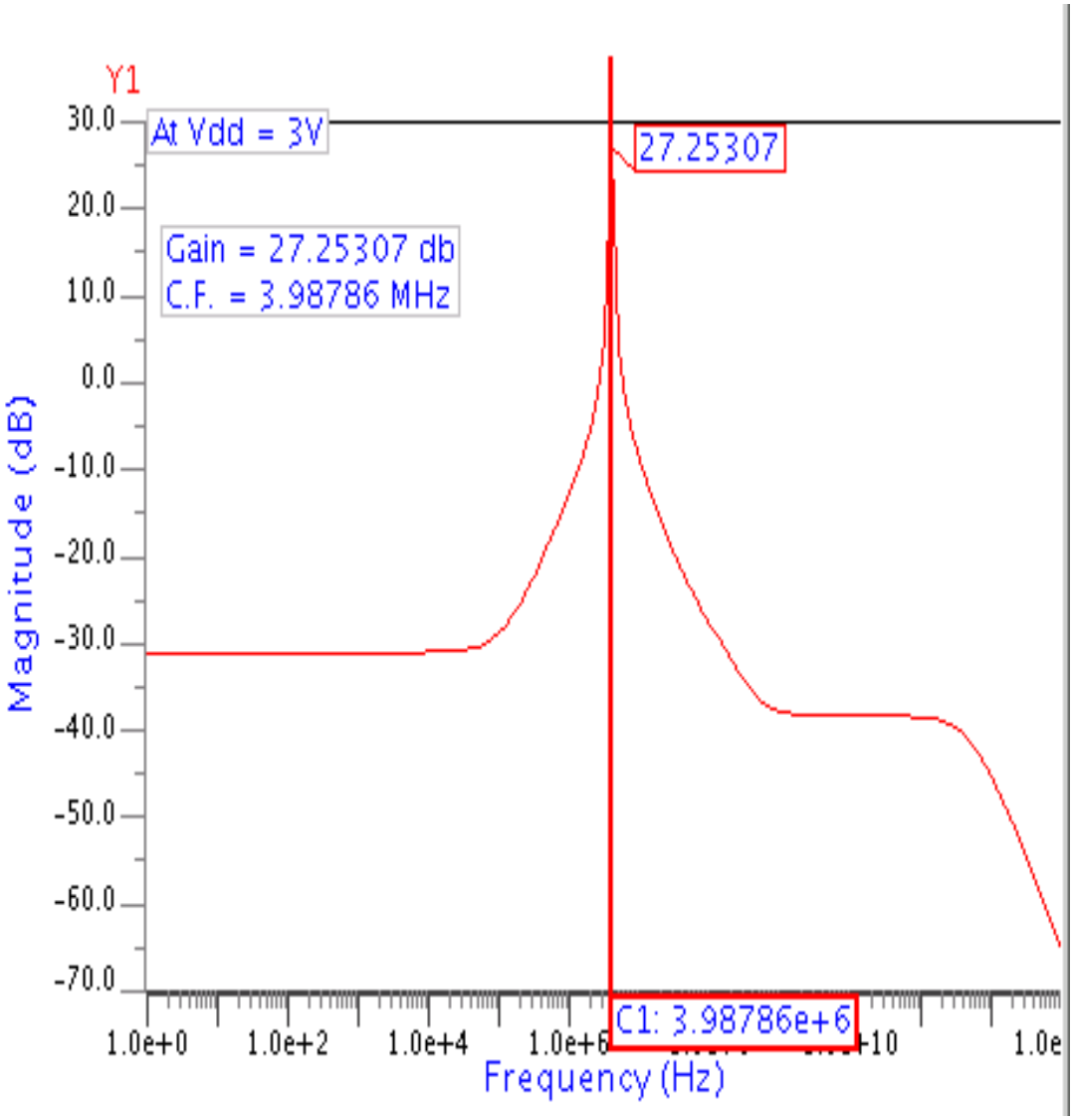


Fig 4.20 AC Analysis at V_{DD} = 3 V

4.6.2 At V_{DD} = 3.3 V

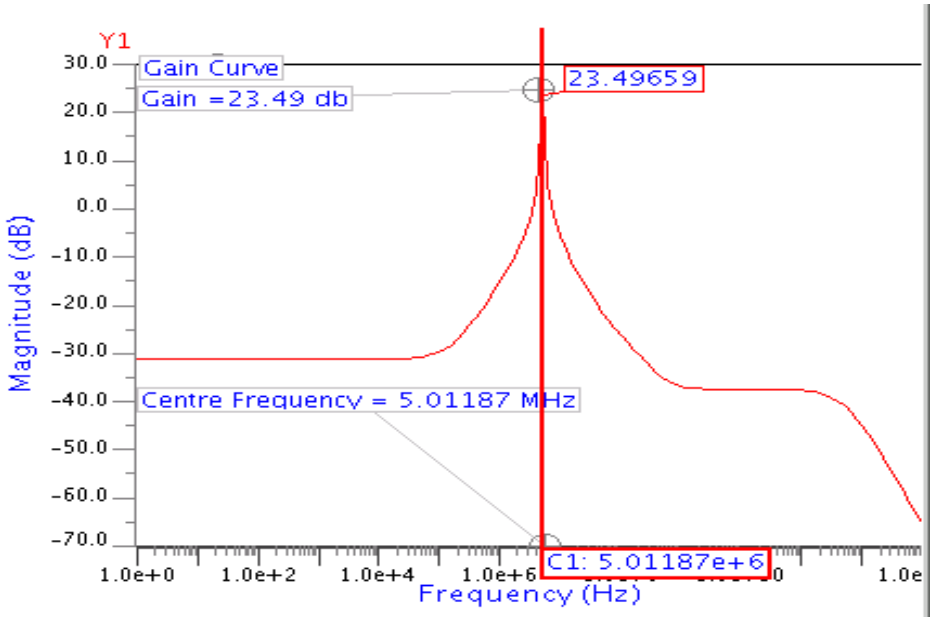


Fig 4.21 AC Analysis at V_{DD} = 3.3 V

4.6.3 At V_{DD} = 3.6 V

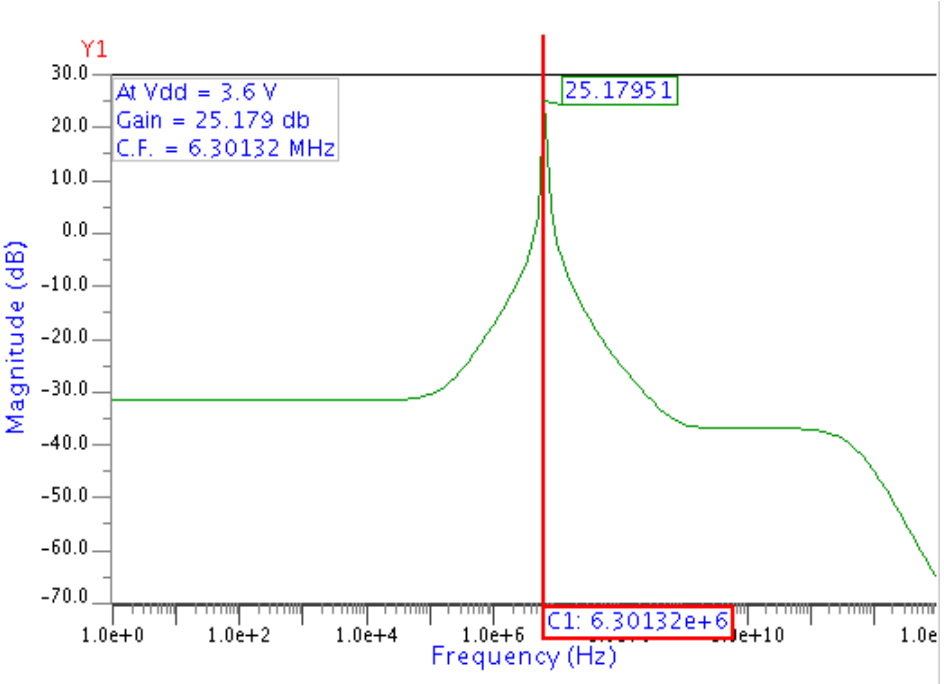


Fig 4.22 AC Analysis at V_{DD} = 3.3 V

From Fig 4.22, plotted waveforms, the following parameters have been obtained as in Table 4.4

Table 4.4. Obtained Parameters for different Power Supplies

Achieved Parameters	**V_{DD} = 3 V**	**V_{DD} = 3.3 V**	**V_{DD} = 3.6 V**
Centre Frequency	3.98103 MHz	5.01187 MHz	6.30132 MHz
Gain at the centre frequency	27.40723dB	23.49659 dB	25.179 dB
Lower Bandwidth	3.90 MHz	4.90 MHz	6.18 MHz
Upper Bandwidth	4.07 MHz	5.16 MHz	6.46 MHz
Quality Factor	23.4178	19.2844	22.5047
Power Dissipation	641.1818 μW	952.1001 μW	1.3408 mW

According to the Table 4.4 this has to be seen that the overall performance of the circuit is increasing for lesser value of power supply.

4.7 Process Corner Simulation

By varying the process parameters (threshold voltage, oxide thickness and transconductance parameter), the variation in achieved parameters have been observed., the change is taken as 10 % increase and 10 % decrease. The AC and DC results have been plotted. By changing the above three process parameters we can make the transistor fast or slow. For making the transistor fast, the value of mobility should be increased and the values of threshold voltage and oxide thickness should be decreased. Similarly, for making the transistor slow, the value of mobility should be decreased and the values of threshold voltage and oxide thickness should be increased. There are four process corners as follows:

1. Fast NMOS and Fast PMOS (FF)
2. Fast NMOS and Slow PMOS (FS)
3. Slow NMOS and Fast PMOS (SF)
4. Slow NMOS and Slow PMOS (SS)

4.7.1 AC analysis

(a) Fast NMOS and Fast PMOS

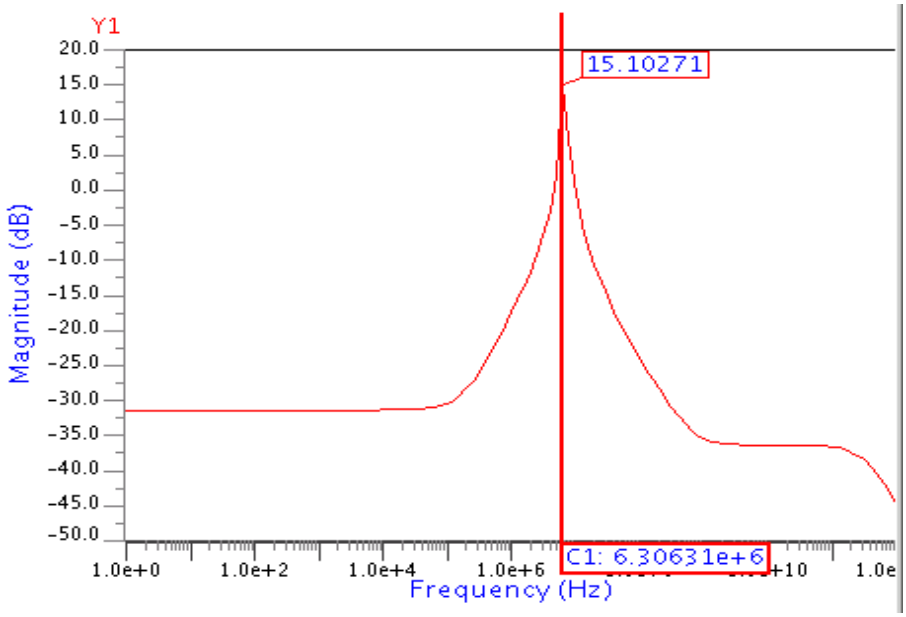


Fig 4.23 Plotted AC Response of Filter in FF Corner

(b) Fast NMOS and Slow PMOS

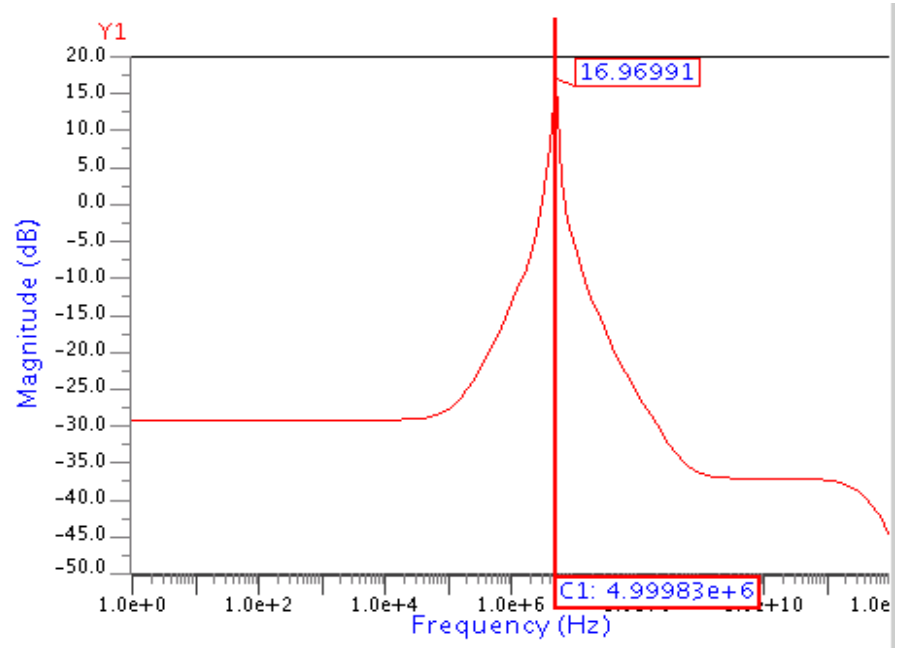


Fig 4.24 Plotted AC Response of Filter in FS Corner

(c) Slow NMOS and Fast PMOS

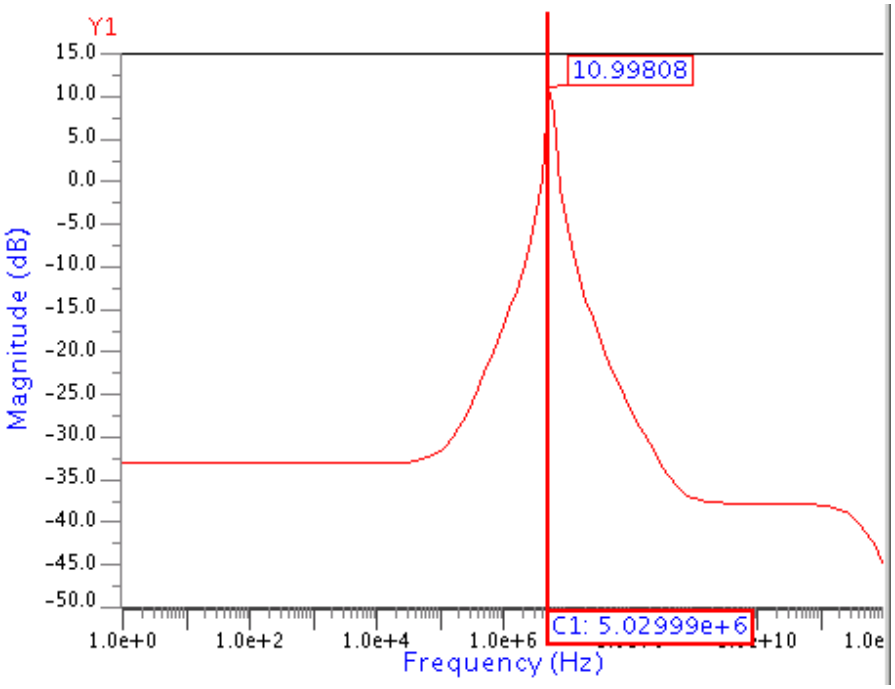


Fig 4.25 Plotted AC Response of Filter in SF Corner

(d) Slow NMOS and Slow PMOS

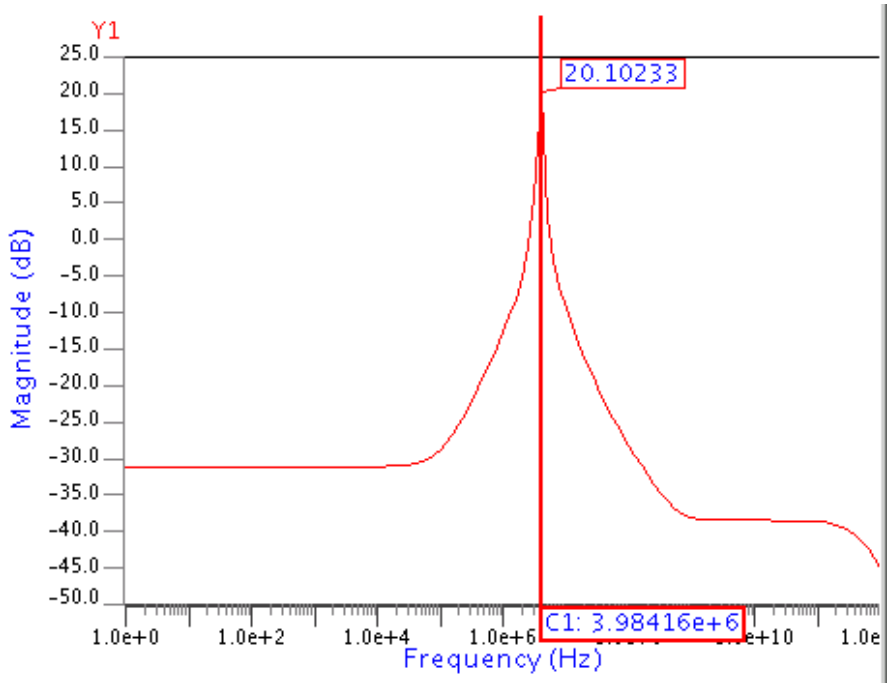


Fig 4.26 Plotted AC Response of Filter in SS Corner

From Figs 4.23, 4.24, 4.25 and 4.26, plotted waveforms, the following parameters have been obtained as in Table 4.5

Table 4.5. Obtained Parameters for different Process Corners

Achieved Parameters	FF	FS	SF	SS
Centre Frequency(MHz)	6.30631	4.99983	5.02999	3.97802
Gain at the CF (dB)	15.1027	16.9699	10.9980	20.1000
Lower Bandwidth(MHz)	6.11573	4.76716	4.80094	3.86513
Upper Bandwidth(MHz)	6.73125	5.21272	5.86626	4.10159
Quality Factor	10.245	11.221	4.72	16.82
Power Dissipation (µW)	1249.5	872.5151	1027.6	711.6731

According to Table 4.5 the best performance achieved in Fast NMOS and Slow PMOS (FS) process corner.

4.7.2 DC Analysis

Here the voltages of all nodes have been plotted.

(a) Fast NMOS and Fast PMOS

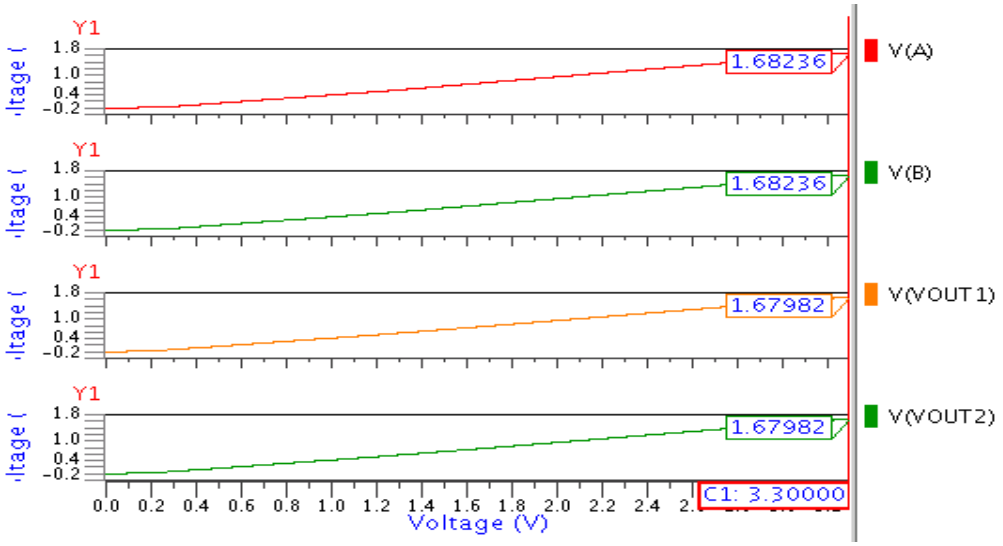


Fig 4.27 Plotted DC Response of Filter for FF Corner

(b)Fast NMOS and Slow PMOS

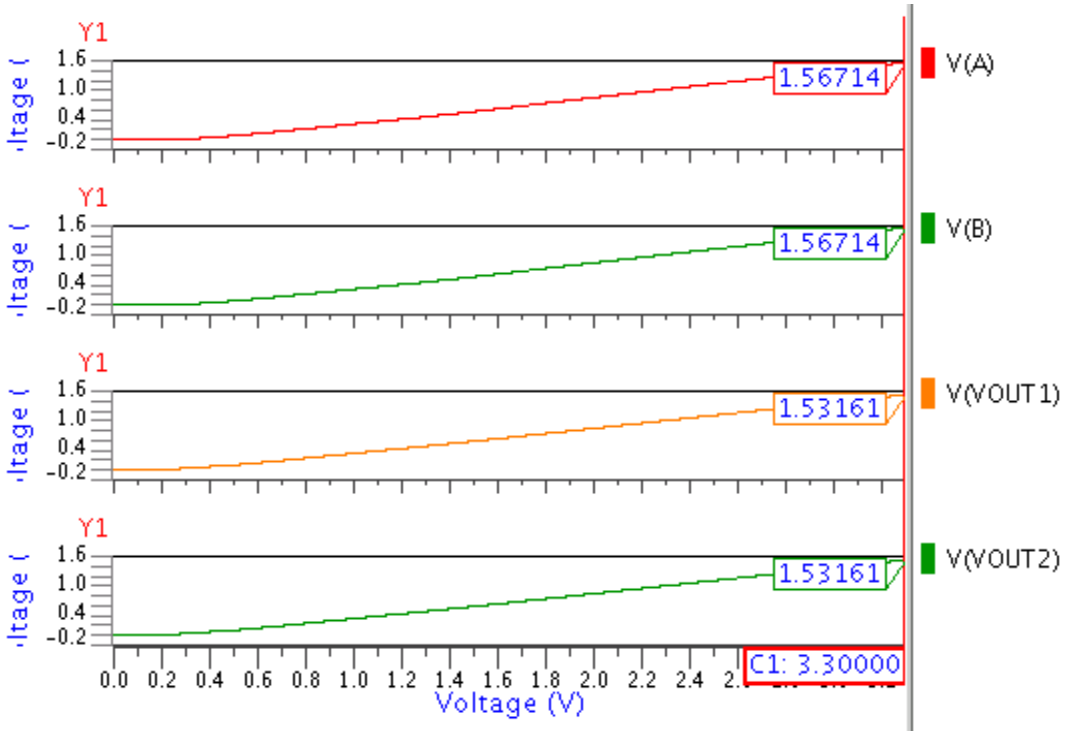


Fig 4.28 Plotted DC Response of Filter for FF Corner

(c) Slow NMOS and Fast PMOS

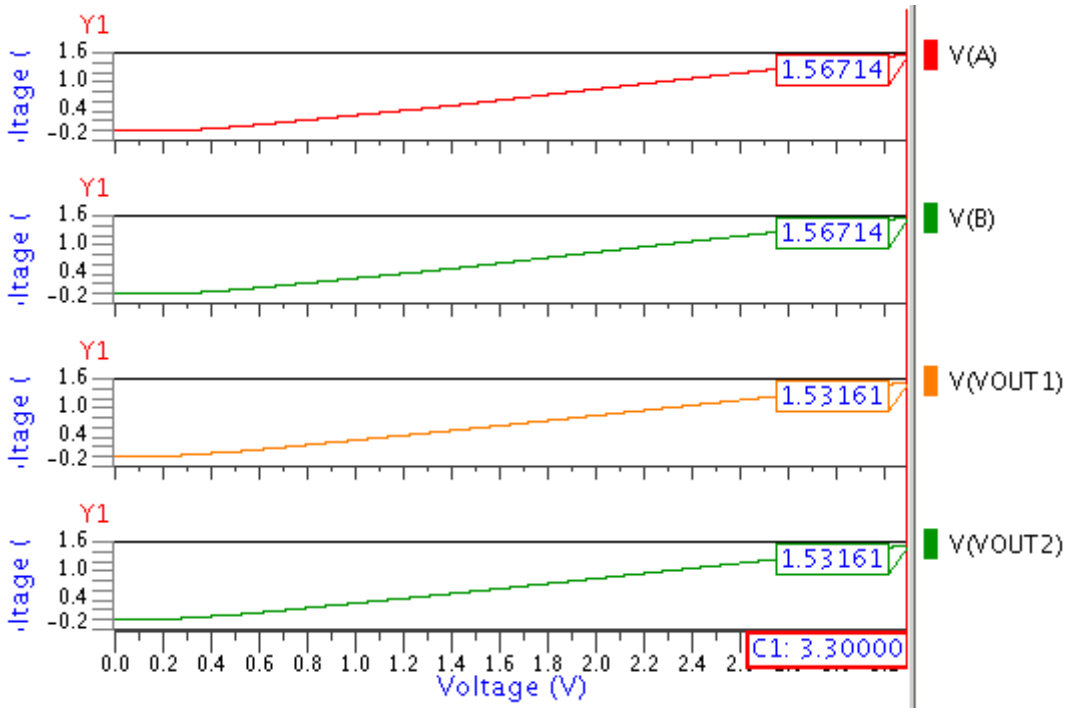


Fig 4.29 Plotted DC Response of Filter for SF Corner

(d) Slow NMOS and Slow PMOS

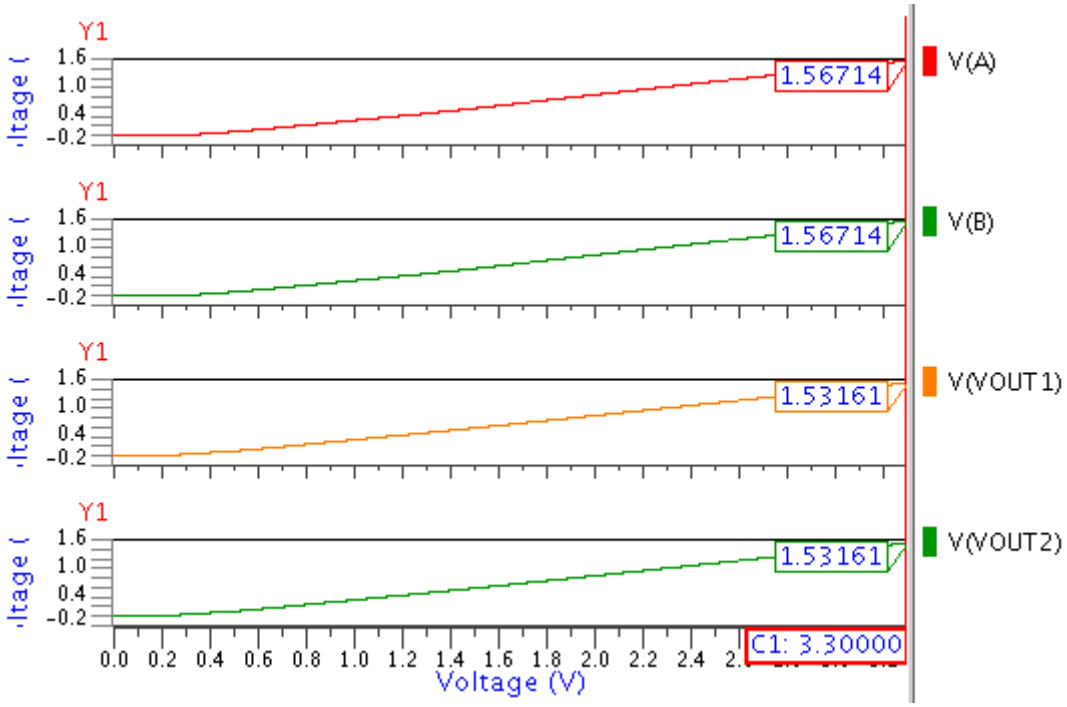


Fig 4.30 Plotted DC Response of Filter for SS Corner

The DC voltage is much closer to 1.65 volt in FF corner and all in other corners this is almost equal, and almost 1.55 volt.

CHAPTER 5

LAYOUT

5.1 Analog Layout

When low-level or high-precision circuitry is being designed, a lot of care is usually given to the details of the circuit schematic and how the signal runs are routed. In layouts for digital circuits, the speed and the area are the two most important issues. In contrast, the layout for analog circuits, everything should be considered simultaneously.

In addition to the speed and the area, other equally critical considerations should be taken into account. In analog layout more care has to be given as the circuit performance changes drastically due to noise, mismatches, crosstalk and shielding required to protect critical nodes from being disturbed. Without proper layout, the mismatches and the coupled noise would be quite large and would significantly degrade the performance of the amplifiers.

5.1.1 Analog Layout Issues

Device mismatch is too often treated as part of the black art of analog design. Random device mismatch plays an important role in the design of accurate analog circuits. The device mismatch is due to number factors like local process variation, global lithographic variations, local lithographic variations and process gradients. These factors affect all devices transistors, resistor, capacitors, and therefore similar techniques can be used to match all elements. During fabrication phase mismatch in physical parameters like doping concentration (Na), mobility (μ), oxide thickness (t_{ox}) and layout dimensions (W,L) gives origin to mismatch in electrical parameter like V_T and β and thus mismatch in I_D.

Matching of individual devices is of paramount concern in analog circuit design. Infact almost all of the 'analog layout techniques' are actually methods for improving matching between different devices on a chip. Matching is important because most of the analog circuit designs use a ratio based design technique. Some common techniques that helps to

improve device matching are MULTI-GATE FINGER LAYOUT and COMMON-CENTROID LAYOUT.

Use of transistor fingering for large and critical transistors is always beneficial. In fingering, the transistor is “fingered” into multiple transistors that are connected in parallel. The folded transistors reduce the source/drain junction area and the gate resistance. The gate resistance can be reduced by decomposing the transistor into more parallel fingers.

Dynamic range is limited by noise and so it is an important parameter to be considered in all analog circuits. In general there are two types of noise, random noise and environmental noise. Random noise consists of a large number of transient disturbances with a statistically random time distribution. Thermal noise is an example of random noise. Random noise dealt at the circuit design level. However there are some layout techniques which can help to reduce random noise. The gate resistance of the poly-silicon and the neutral body region, which are both random noise sources, is reduced by multi-gate finger layout.

Other noise considers is environmental noise. Environmental noise also dealt at the circuit level. One of the common design technique used to minimize the effects of environmental noise is to employ a 'fully-differential' circuit design, since environmental noise generally appears as a common-mode signal. However substrate plugs are also very useful for reducing 'substrate noise', which is a troublesome form of environmental noise encountered in highly integrated mixed-signal systems and Systems-On-a-Chip (SOC).

5.2 Layout of OTA

Due to huge aspect ratio, some transistors are divided into multiple fingers. Fig 5.1 shows all the transistors with fingerings. Aspect ratio of MN1 and MN2 is 50.2/1.4. Since $50.2 = 4 \times 12.55$, so a single transistor is divided in to 4 fingers with width of 12.55µm.

There is no need to make fingers of other transistors of OTA, because sizes of these transistors are very small.

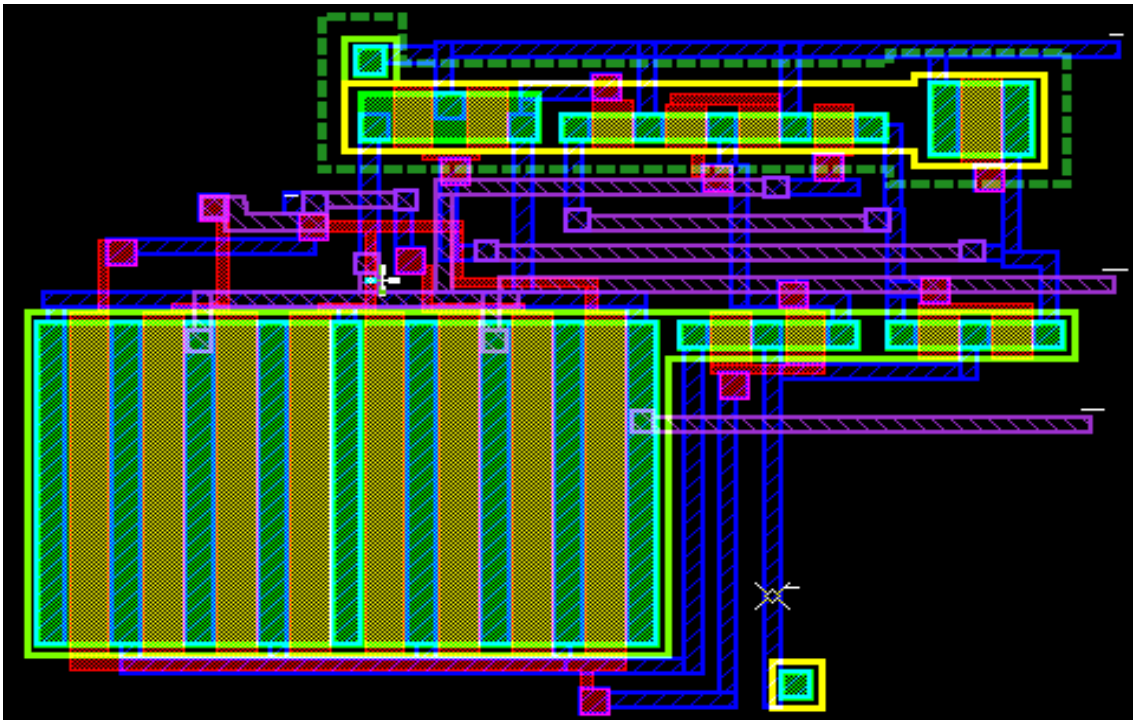


Fig.5.1 Layout of OTA

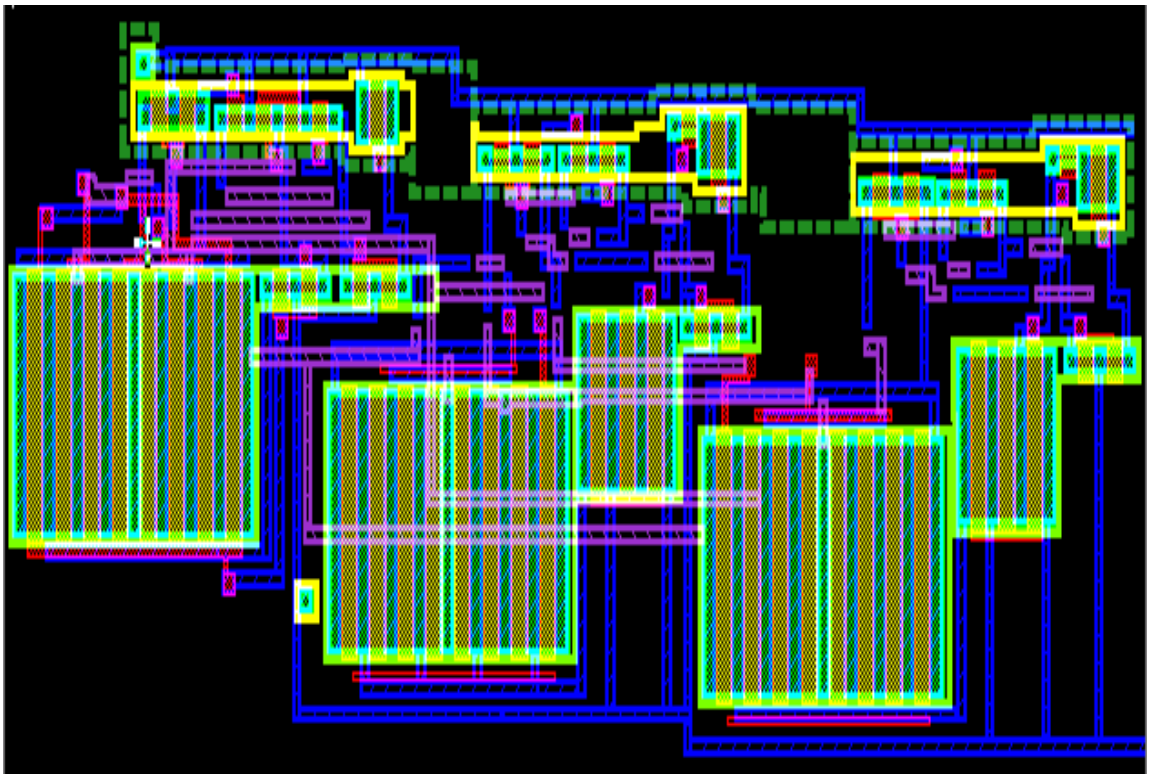


Fig.5.2 Layout of Complete Filter without Capacitive Load

5.3 Layout of the Filter

In the layout of a filter, we are using three OTAs of almost made by the transistors of same size, But due to self biasing voltage of each node have to be same as 1.65V.Thats why there are some difference in the sizes of load transistors and tail current transistors of different OTAs. The layout of the filter without capacitors is shown in Fig. 5.2.

The whole layout of the filter with the capacitors is shown in Fig. 5.3.

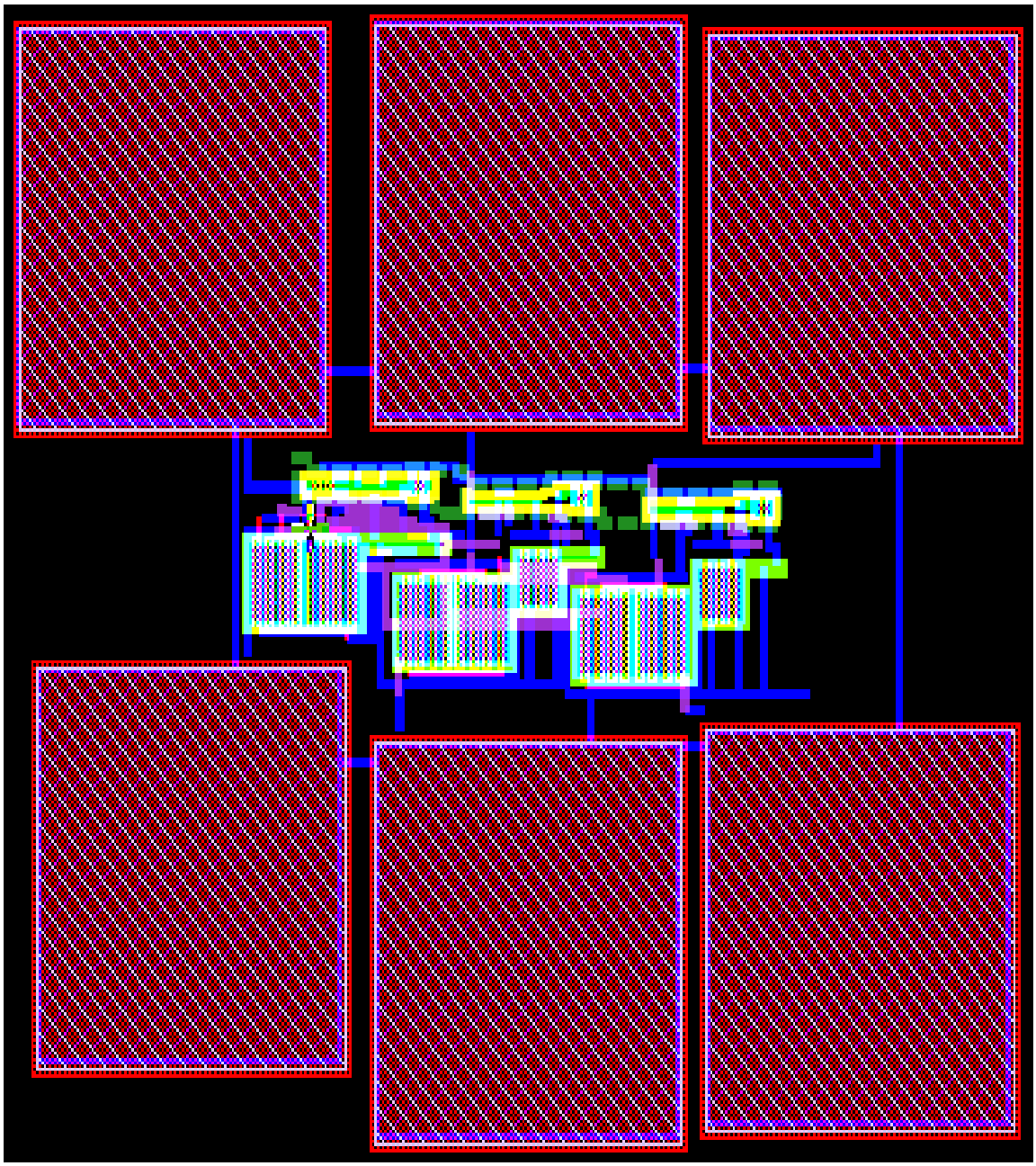


Fig.5.3 Layout of Complete Filter with capacitive load

5.4 LVS Report

After completing layout, LVS has to be matched with the schematic. The LVS report is given in Appendix A.1.This checks all the connections in schematic with layout.

5.5 PEX Report

After the successful competon of the LVS, PEX has to check which verifies all the components values in schematic with layout and gives information about parasitic if they come in to picture. The PEX report is given in Appendix A.2.

CHAPTER 6

CONCLUSION AND FUTURE PROSPECTIVE

6.1 Conclusion

Self biasing is the area of biasing, which reduces the area requirement of the circuit. As the technology is scaled down it is more important for a filter to work at any CM level. Here in this thesis work, fully self biased continuous time CMOS bandpass Gm-C filter using a design methodology based on the g_m/I_D transistor characteristics is designed and simulated with the layout of the circuit.

The circuit achieves pass-band central frequency of about 5.011MHz (with a small tuning range), quality factor of 19.28, Gain of 23.48 dB at center frequency and a current consumption of 288.48 μA. The circuit does not required any DC external biasing circuit, only need to apply V_{DD} (3.3 V).

The operation of the input stage under different supply voltages and temperature are simulated and analyzed. Simulation result for temperature variation, power supply variations and load variations shows that the circuit can be used for wide range of temperature, power supply and load variation. The main feature of the circuit is the self biasing with low power consumption of 952 μW.

6.2 Future Prospective and Areas of Improvement

There are several areas of improvement in this circuit. This circuit can be made for reduced low power and with high gain and improved Quality factor with different order. This circuit can also be implement with tuning capability also.

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APPENDIX

A.1 LVS Report

After completing layout, LVS has to be matched with the schematic. The LVS report is as follows:

```
                  ##################################################
                  ##                                              ##
                  ##        C A L I B R E   S Y S T E M           ##
                  ##                                              ##
                  ##            L V S   R E P O R T               ##
                  ##                                              ##
                  ##################################################


REPORT FILE NAME:         91.lvs.report
LAYOUT NAME:              91.calibre.gds
SOURCE  NAME:                    /home/vaibhav/filter20/filter20.src.net
('filter20')
RULE FILE:                /home/vaibhav/_tsmc035.rules_
LVS MODE:                 Mask
RULE FILE NAME:           /home/vaibhav/_tsmc035.rules_
CREATION TIME:            Thu Jun 18 10:30:54 2009
CURRENT DIRECTORY:        /home/vaibhav
USER NAME:                vaibhav
CALIBRE VERSION:          v2006.2_30.26    Fri Jul  7 22:37:10 PDT 2006

**********************************************************************
**************************************
                              OVERALL COMPARISON RESULTS
**********************************************************************
**************************************

                       #       ###################       _   _
                      #        #                 #       *   *
                   #   #       #     CORRECT     #         |
                    # #        #                 #       \___/
                     #         ###################

  Warning:  Ambiguity points were found and resolved arbitrarily.
```


INITIAL NUMBERS OF OBJECTS

	Layout	Source		Component Type
Ports:	5	5		
Nets:	70	18	*	
Instances:	38	18	*	MN (4 pins)
	19	18	*	MP (4 pins)
	6	6		C (2 pins)
Total Inst:	63	42		

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	5	5	
Nets:	18	18	
Instances:	18	18	MN (4 pins)
	18	18	MP (4 pins)
	4	4	C (2 pins)
Total Inst:	40	40	

* = Number of objects in layout different from number in source.

****
****
LVS PARAMETERS
****
****

o LVS Setup:

```
   // LVS COMPONENT TYPE PROPERTY
   // LVS COMPONENT SUBTYPE PROPERTY
   // LVS PIN NAME PROPERTY
   // LVS POWER NAME
   // LVS GROUND NAME
   LVS CELL SUPPLY                      NO
   LVS RECOGNIZE GATES                  ALL
```

```
LVS IGNORE PORTS                        NO
LVS CHECK PORT NAMES                    NO
LVS IGNORE TRIVIAL NAMED PORTS          NO
LVS BUILTIN DEVICE PIN SWAP             YES
LVS ALL CAPACITOR PINS SWAPPABLE        NO
LVS DISCARD PINS BY DEVICE              NO
LVS SOFT SUBSTRATE PINS                 NO
LVS INJECT LOGIC                        NO
LVS EXPAND UNBALANCED CELLS             YES
LVS EXPAND SEED PROMOTIONS              NO
LVS PRESERVE PARAMETERIZED CELLS        NO
LVS GLOBALS ARE PORTS                   YES
LVS REVERSE WL                          NO
LVS SPICE PREFER PINS                   NO
LVS SPICE SLASH IS SPACE                YES
LVS SPICE ALLOW FLOATING PINS           YES
LVS SPICE ALLOW UNQUOTED STRINGS        NO
LVS SPICE CONDITIONAL LDD               NO
LVS SPICE CULL PRIMITIVE SUBCIRCUITS    NO
LVS SPICE IMPLIED MOS AREA              NO
// LVS SPICE MULTIPLIER NAME
LVS SPICE OVERRIDE GLOBALS              NO
LVS SPICE REDEFINE PARAM                NO
LVS SPICE REPLICATE DEVICES             NO
LVS SPICE STRICT WL                     NO
// LVS SPICE OPTION
LVS STRICT SUBTYPES                     NO
LAYOUT CASE                             NO
SOURCE CASE                             NO
LVS COMPARE CASE                        NO
LVS DOWNCASE DEVICE                     NO
LVS REPORT MAXIMUM                      50
LVS PROPERTY RESOLUTION MAXIMUM         32
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                        YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE

// Reduction

LVS REDUCE SERIES MOS                   NO
LVS REDUCE PARALLEL MOS                 YES
LVS REDUCE SEMI SERIES MOS              NO
LVS REDUCE SPLIT GATES                  YES
LVS REDUCE PARALLEL BIPOLAR             YES
LVS REDUCE SERIES CAPACITORS            YES
LVS REDUCE PARALLEL CAPACITORS          YES
LVS REDUCE SERIES RESISTORS             YES
LVS REDUCE PARALLEL RESISTORS           YES
LVS REDUCE PARALLEL DIODES              YES
LVS REDUCTION PRIORITY                  PARALLEL

// Filter
```

```
   LVS FILTER  sch_filter_direct_open  OPEN SOURCE DIRECT
   LVS FILTER  sch_filter_direct_short  SHORT SOURCE DIRECT
   LVS FILTER  sch_filter_mask_open  OPEN SOURCE MASK
   LVS FILTER  sch_filter_mask_short  SHORT SOURCE MASK
   LVS FILTER  lay_filter_direct_open  OPEN LAYOUT DIRECT
   LVS FILTER  lay_filter_direct_short  SHORT LAYOUT DIRECT
   LVS FILTER  v  OPEN
   LVS FILTER  i  OPEN
   LVS FILTER  e  OPEN
   LVS FILTER  f  OPEN
   LVS FILTER  g  OPEN


*************************************************************************
************************************
                              INFORMATION AND WARNINGS
*************************************************************************
************************************


                  Matched        Matched       Unmatched       Unmatched
Component
                   Layout      Source        Layout        Source     Type
                  -------     -------     ---------     ---------     -----
----
   Ports:              5           5             0             0

   Nets:              18          18             0             0

   Instances:         18          18             0             0    MN(N)
                      18          18             0             0    MP(P)
                       4             4                0                0
C(NOTCHEDROW)
                  -------     -------     ---------     ---------
   Total Inst:        40          40             0             0


o Statistics:

   52 isolated layout nets were deleted.

   30 layout mos transistors were reduced to 9.
     21 mos transistors were deleted by parallel reduction.

   4 parallel layout capacitors were reduced to 2.
   4 parallel source capacitors were reduced to 2.

   1 net was matched arbitrarily.


o Isolated Layout Nets:

      (Layout nets which are not connected to any instances or ports).

   19(2.000,26.000)          20(15.000,26.000)          21(50.000,26.000)
22(76.000,26.000) 23(102.000,23.000)
```

24(159.000,16.000) 25(173.000,16.000) 26(194.500,16.000) 27(207.500,16.000)
28(258.500,13.000) 29(333.000,8.000) 30(347.000,8.000) 31(381.500,8.000) 32(432.500,5.000)
33(-55.000,-73.000) 34(-42.000,-73.000) 35(-29.000,-73.000) 36(-16.000,-73.000)
37(-3.000,-73.000) 38(10.000,-73.000) 39(23.000,-73.000) 40(36.000,-73.000)
41(58.000,-15.000) 42(71.000,-15.000) 43(89.000,-101.500) 44(94.500,-15.000)
45(102.000,-101.500) 46(107.500,-15.000) 47(115.000,-101.500) 48(128.000,-101.500)
49(141.000,-101.500) 50(154.000,-101.500) 51(167.000,-101.500) 52(180.000,-101.500)
53(203.500,-62.000) 54(216.500,-62.000) 55(229.500,-62.000) 56(251.000,-25.000)
57(261.000,-112.500) 58(264.000,-25.000) 59(274.000,-112.500) 60(287.000,-112.500)
61(300.000,-112.500) 62(313.000,-112.500) 63(326.000,-112.500) 64(339.000,-112.500)
65(352.000,-112.500) 66(377.500,-70.000) 67(390.500,-70.000) 68(403.500,-70.000)

o Initial Correspondence Points:

Ports: GND vout1 Vin vout2 VDD

o Ambiguity Resolution Points:

(Each one of the following objects belongs to a group of indistinguishable objects.
The listed objects were matched arbitrarily by the Ambiguity Resolution feature of LVS.
Arbitrary matching may be prevented by assigning names to these objects or to adjacent nets).

Layout	Source
Nets	
4(32.500,10.000)	N$12

****
SUMMARY
****

Total CPU Time: 0 sec
Total Elapsed Time: 0 sec

A.2 PEX report

```
* File: 91.pex.netlist
* Created: Thu Jun 18 10:46:45 2009
* Program "Calibre xRC"
* Version "v2006.2_30.26"
*
.include "91.pex.netlist.pex"
.subckt filter20  VIN VOUT1 VOUT2 VDD GND
*
* GND GND
* VDD VDD
* VOUT2     VOUT2
* VOUT1     VOUT1
* VIN VIN
MN2__1 N_VOUT1_MN2__1_d N_VIN_MN2__1_g N_A_MN2__1_s N_GND_MN2__1_b n
L=1.4e-06
+ W=1.26e-05 AD=1.386e-11 AS=1.512e-11
MN1__1 N_VOUT2_MN1__1_d N_VIN_MN1__1_g N_A_MN1__1_s N_GND_MN2__1_b n
L=1.4e-06
+ W=1.26e-05 AD=1.512e-11 AS=1.512e-11
MN1__2 N_VOUT2_MN1__2_d N_VIN_MN1__2_g N_A_MN1__2_s N_GND_MN2__1_b n
L=1.4e-06
+ W=1.26e-05 AD=1.512e-11 AS=1.512e-11
MN2__2 N_VOUT1_MN2__2_d N_VIN_MN2__2_g N_A_MN2__2_s N_GND_MN2__1_b n
L=1.4e-06
+ W=1.26e-05 AD=1.512e-11 AS=1.512e-11
MN2__3 N_VOUT1_MN2__3_d N_VIN_MN2__3_g N_A_MN2__3_s N_GND_MN2__1_b n
L=1.4e-06
+ W=1.26e-05 AD=1.512e-11 AS=1.512e-11
MN1__3 N_VOUT2_MN1__3_d N_VIN_MN1__3_g N_A_MN1__3_s N_GND_MN2__1_b n
L=1.4e-06
+ W=1.26e-05 AD=1.512e-11 AS=1.512e-11
MN1__4 N_VOUT2_MN1__4_d N_VIN_MN1__4_g N_A_MN1__4_s N_GND_MN2__1_b n
L=1.4e-06
+ W=1.26e-05 AD=1.512e-11 AS=1.512e-11
MN2__4 N_VOUT1_MN2__4_d N_VIN_MN2__4_g N_A_MN2__4_s N_GND_MN2__1_b n
L=1.4e-06
+ W=1.26e-05 AD=1.386e-11 AS=1.512e-11
MN4 N_A_MN4_d N_VIN_MN4_g N_GND_MN4_s N_GND_MN2__1_b n L=1.4e-06 W=1e-
06
+ AD=1.1e-12 AS=1.2e-12
MN3 N_VIN_MN3_d N_VIN_MN3_g N_GND_MN3_s N_GND_MN2__1_b n L=1.4e-06
W=1e-06
+ AD=1.1e-12 AS=1.2e-12
MN7__1 N_N$335_MN7__1_d N_VOUT2_MN7__1_g N_N$328_MN7__1_s
N_GND_MN2__1_b n
+ L=1.4e-06 W=1.26e-05 AD=1.386e-11 AS=1.512e-11
MN17 N_N$12_MN17_d N_N$12_MN17_g N_GND_MN17_s N_GND_MN2__1_b n L=1.4e-
06
+ W=1e-06 AD=1.1e-12 AS=1.2e-12
MN8__1 N_N$330_MN8__1_d N_VOUT1_MN8__1_g N_N$328_MN8__1_s
N_GND_MN2__1_b n
+ L=1.4e-06 W=1.26e-05 AD=1.512e-11 AS=1.512e-11
MN18 N_N$338_MN18_d N_N$12_MN18_g N_GND_MN18_s N_GND_MN2__1_b n L=1.4e-
06
```

```
+ W=1e-06 AD=1.1e-12 AS=1.2e-12
MN8__2 N_N$330_MN8__2_d N_VOUT1_MN8__2_g N_N$328_MN8__2_s
N_GND_MN2__1_b n
+ L=1.4e-06 W=1.26e-05 AD=1.512e-11 AS=1.512e-11
MN7__2 N_N$335_MN7__2_d N_VOUT2_MN7__2_g N_N$328_MN7__2_s
N_GND_MN2__1_b n
+ L=1.4e-06 W=1.26e-05 AD=1.512e-11 AS=1.512e-11
MN7__3 N_N$335_MN7__3_d N_VOUT2_MN7__3_g N_N$328_MN7__3_s
N_GND_MN2__1_b n
+ L=1.4e-06 W=1.26e-05 AD=1.512e-11 AS=1.512e-11
MN8__3 N_N$330_MN8__3_d N_VOUT1_MN8__3_g N_N$328_MN8__3_s
N_GND_MN2__1_b n
+ L=1.4e-06 W=1.26e-05 AD=1.512e-11 AS=1.512e-11
MN8__4 N_N$330_MN8__4_d N_VOUT1_MN8__4_g N_N$328_MN8__4_s
N_GND_MN2__1_b n
+ L=1.4e-06 W=1.26e-05 AD=1.512e-11 AS=1.512e-11
MN7__4 N_N$335_MN7__4_d N_VOUT2_MN7__4_g N_N$328_MN7__4_s
N_GND_MN2__1_b n
+ L=1.4e-06 W=1.26e-05 AD=1.386e-11 AS=1.512e-11
MN10 N_N$328_MN10_d N_e_MN10_g N_GND_MN10_s N_GND_MN2__1_b n L=1.4e-06
+ W=8.4e-06 AD=9.24e-12 AS=1.008e-11
MN9__1 N_e_MN9__1_d N_e_MN9__1_g N_GND_MN9__1_s N_GND_MN2__1_b n
L=1.4e-06
+ W=8.4e-06 AD=1.008e-11 AS=1.008e-11
MN9__2 N_e_MN9__2_d N_e_MN9__2_g N_GND_MN9__2_s N_GND_MN2__1_b n
L=1.4e-06
+ W=8.4e-06 AD=1.008e-11 AS=9.24e-12
MN11 N_N$2_MN11_d N_N$2_MN11_g N_GND_MN11_s N_GND_MN2__1_b n L=1.4e-06
W=1e-06
+ AD=1.1e-12 AS=1.2e-12
MN13__1 N_VOUT1_MN13__1_d N_N$335_MN13__1_g N_N$331_MN13__1_s
N_GND_MN2__1_b n
+ L=1.4e-06 W=1.26e-05 AD=1.386e-11 AS=1.512e-11
MN12 N_N$336_MN12_d N_N$2_MN12_g N_GND_MN12_s N_GND_MN2__1_b n L=1.4e-
06
+ W=1e-06 AD=1.1e-12 AS=1.2e-12
MN14__1 N_VOUT2_MN14__1_d N_N$330_MN14__1_g N_N$331_MN14__1_s
N_GND_MN2__1_b n
+ L=1.4e-06 W=1.26e-05 AD=1.512e-11 AS=1.512e-11
MN14__2 N_VOUT2_MN14__2_d N_N$330_MN14__2_g N_N$331_MN14__2_s
N_GND_MN2__1_b n
+ L=1.4e-06 W=1.26e-05 AD=1.512e-11 AS=1.512e-11
MN13__2 N_VOUT1_MN13__2_d N_N$335_MN13__2_g N_N$331_MN13__2_s
N_GND_MN2__1_b n
+ L=1.4e-06 W=1.26e-05 AD=1.512e-11 AS=1.512e-11
MN13__3 N_VOUT1_MN13__3_d N_N$335_MN13__3_g N_N$331_MN13__3_s
N_GND_MN2__1_b n
+ L=1.4e-06 W=1.26e-05 AD=1.512e-11 AS=1.512e-11
MN14__3 N_VOUT2_MN14__3_d N_N$330_MN14__3_g N_N$331_MN14__3_s
N_GND_MN2__1_b n
+ L=1.4e-06 W=1.26e-05 AD=1.512e-11 AS=1.512e-11
MN14__4 N_VOUT2_MN14__4_d N_N$330_MN14__4_g N_N$331_MN14__4_s
N_GND_MN2__1_b n
+ L=1.4e-06 W=1.26e-05 AD=1.512e-11 AS=1.512e-11
MN13__4 N_VOUT1_MN13__4_d N_N$335_MN13__4_g N_N$331_MN13__4_s
N_GND_MN2__1_b n
+ L=1.4e-06 W=1.26e-05 AD=1.386e-11 AS=1.512e-11
```

```
MN16 N_N$331_MN16_d N_N$332_MN16_g N_GND_MN16_s N_GND_MN2__1_b n
L=1.4e-06
+ W=8.4e-06 AD=9.24e-12 AS=1.008e-11
MN15__1 N_N$332_MN15__1_d N_N$332_MN15__1_g N_GND_MN15__1_s
N_GND_MN2__1_b n
+ L=1.4e-06 W=8.4e-06 AD=1.008e-11 AS=1.008e-11
MN15__2 N_N$332_MN15__2_d N_N$332_MN15__2_g N_GND_MN15__2_s
N_GND_MN2__1_b n
+ L=1.4e-06 W=8.4e-06 AD=1.008e-11 AS=9.24e-12
MN5 N_N$1_MN5_d N_N$1_MN5_g N_GND_MN5_s N_GND_MN2__1_b n L=1.4e-06
W=1e-06
+ AD=1.1e-12 AS=1.2e-12
MN6 N_B_MN6_d N_N$1_MN6_g N_GND_MN6_s N_GND_MN2__1_b n L=1.4e-06 W=1e-
06
+ AD=1.1e-12 AS=1.2e-12
MP15 N_VOUT2_MP15_d N_N$338_MP15_g N_VDD_MP15_s N_VDD_MP15_b p L=1.4e-
06
+ W=1.8e-06 AD=1.98e-12 AS=2.16e-12
MP14 N_VOUT1_MP14_d N_N$338_MP14_g N_VDD_MP14_s N_VDD_MP15_b p L=1.4e-
06
+ W=1.8e-06 AD=1.98e-12 AS=2.16e-12
MP17 N_N$12_MP17_d N_VOUT1_MP17_g N_VDD_MP17_s N_VDD_MP15_b p L=1.4e-06
W=1e-06
+ AD=1.1e-12 AS=1.2e-12
MP1__1 N_VIN_MP1__1_d N_VIN_MP1__1_g N_VDD_MP1__1_s N_VDD_MP15_b p
L=1.4e-06
+ W=1e-06 AD=1.2e-12 AS=1.2e-12
MP1__2 N_VIN_MP1__2_d N_VIN_MP1__2_g N_VDD_MP1__2_s N_VDD_MP15_b p
L=1.4e-06
+ W=1e-06 AD=1.2e-12 AS=1.2e-12
MP16 N_N$12_MP16_d N_VOUT2_MP16_g N_VDD_MP16_s N_VDD_MP15_b p L=1.4e-06
W=1e-06
+ AD=1.1e-12 AS=1.2e-12
MP18 N_N$338_MP18_d N_N$338_MP18_g N_VDD_MP18_s N_VDD_MP15_b p L=1.4e-
06
+ W=2.8e-06 AD=3.08e-12 AS=3.08e-12
MP9 N_N$330_MP9_d N_N$336_MP9_g N_VDD_MP9_s N_VDD_MP15_b p L=1.4e-06
W=9e-07
+ AD=1.18e-12 AS=1.36e-12
MP8 N_N$335_MP8_d N_N$336_MP8_g N_VDD_MP8_s N_VDD_MP15_b p L=1.4e-06
W=9e-07
+ AD=1.18e-12 AS=1.36e-12
MP11 N_N$2_MP11_d N_N$335_MP11_g N_VDD_MP11_s N_VDD_MP15_b p L=1.4e-06
W=1e-06
+ AD=1.1e-12 AS=1.2e-12
MP10 N_N$2_MP10_d N_N$330_MP10_g N_VDD_MP10_s N_VDD_MP15_b p L=1.4e-06
W=1e-06
+ AD=1.1e-12 AS=1.2e-12
MP7 N_e_MP7_d N_e_MP7_g N_VDD_MP7_s N_VDD_MP15_b p L=1.4e-06 W=7e-07
+ AD=1.14e-12 AS=3.22e-12
MP12 N_N$336_MP12_d N_N$336_MP12_g N_VDD_MP12_s N_VDD_MP15_b p L=1.4e-
06
+ W=2.8e-06 AD=3.08e-12 AS=3.22e-12
MP2 N_VOUT2_MP2_d N_B_MP2_g N_VDD_MP2_s N_VDD_MP15_b p L=1.4e-06
W=1.1e-06
+ AD=1.32e-12 AS=1.54e-12
```

```
MP3 N_VOUT1_MP3_d N_B_MP3_g N_VDD_MP3_s N_VDD_MP15_b p L=1.4e-06
W=1.1e-06
+ AD=1.32e-12 AS=1.54e-12
MP4 N_N$1_MP4_d N_VOUT1_MP4_g N_VDD_MP4_s N_VDD_MP15_b p L=1.4e-06
W=1e-06
+ AD=1.1e-12 AS=1.2e-12
MP5 N_N$1_MP5_d N_VOUT2_MP5_g N_VDD_MP5_s N_VDD_MP15_b p L=1.4e-06
W=1e-06
+ AD=1.1e-12 AS=1.2e-12
MP13 N_N$332_MP13_d N_N$332_MP13_g N_VDD_MP13_s N_VDD_MP15_b p L=1.4e-
06
+ W=7e-07 AD=1.14e-12 AS=3.22e-12
MP6 N_B_MP6_d N_B_MP6_g N_VDD_MP6_s N_VDD_MP15_b p L=1.4e-06 W=2.8e-06
+ AD=3.08e-12 AS=3.22e-12
C5__2 N_VOUT2_C5__2_pos N_GND_C5__2_neg 3.00758p
C4__2 N_VOUT1_C4__2_pos N_GND_C4__2_neg 3.00758p
C3 N_N$335_C3_pos N_GND_C3_neg 3.00758p
C6 N_N$330_C6_pos N_GND_C6_neg 3.00758p
C4__1 N_VOUT1_C4__1_pos N_GND_C4__1_neg 3.00758p
C5__1 N_VOUT2_C5__1_pos N_GND_C5__1_neg 3.00758p
*
.include "91.pex.netlist.91.pxi"
*
.ends
*
*
```