Analysis of Breakdown Voltages and Depletion Region Width of 4H-SiC Vertical Double Implanted MOSFET with Gaussian Profile in Drift region

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CERTIFICATE

I hereby certify that the work, which is being presented in the thesis, entitled **"An Analysis of Breakdown Voltages and Depletion Region Width of 4H-SiC vertical double implanted MOSFET with Gaussian profile in drift region"** in partial fulfillment of the requirements for the award of degree of Master of Engineering in Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the guidance of **Dr. A.K.Chatterjee**.

I have not submitted the matter presented in the thesis for the award of any other degree of this or any other university.

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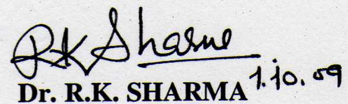

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ABSTRACT

The semiconductor based electronic devices that can function at ambient temperatures higher than 150^0C without external cooling system could greatly benefit a variety of application. When Silicon Power device work at a temperature above 200^0C then it is problematic because of the self heating is increased, also the internal junction temperature and leakage increased. To work in high temperature with ease it is required to used high band gap devices. For all of these requirements Silicon devices are the optimum choices.

Due to various properties of Silicon carbide like lower intrinsic carrier concentration (10–35 orders of magnitude), higher electric breakdown field (4–20 times), higher thermal conductivity (3–13 times), larger saturated electron drift velocity (2–2.5 times) it replaces Si material very quickly in the semiconductor industry.

The fact that wide band gap semiconductors are capable of electronic functionality at much higher temperatures than silicon has partially fueled their development, particularly in the case of SiC. 4H-SiC is a potentially useful material for high temperature devices because of its refractory nature, high thermal conductivity, wide band gap (2.2 eV) and high electron mobility comparable to that of Si.

The present work aims at the design of high breakdown voltage 10kV 4H-SiC DIMOSFET with Gaussian profile in drift region to show its characteristics and various properties. In Gaussian doping profile it is found that the height of drift region h at 10 KV is 102 µm. At that particular point the avalanche breakdown voltage is about 9.063 KV. The calculation of Depletion region Width at different breakdown voltage and at different height is to be done and corresponding graph is shown.

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LIST OF USED ACRONYM

CVD	: Chemical Vapor Deposition
eV	: Electron Volt
HTCVD	: High Temperature Chemical Vapor Deposition
LPE	: Liquid Phase Epitaxy
MESFET	: Metal-Semiconductor Field Effect Transistor
MOSFET	: Metal-Oxide Semiconductor Field Effect Transistor
SBD	: Schottky Barrier Diode
SBH	: Schottky Barrier Height
SiC	: Silicon Carbide
SiO_2	: Silicon dioxide
VPE	: Vapor Phase Epitaxy
E_g	: Energy bandgap
E_C	: Energy Conduction Band
E_{fm}	: Metal Fermi Level
ϕ_m	: Metal Work Function
ϕ_S	: Semiconductor Work Function
E_{fs}	: Semiconductor Fermi Level
E_0	: Vacuum Level
ϕ_{Bn}	: Barrier height of n-type semiconductor
ϕ_{Bp}	: Barrier height of p-type semiconductor
ϕ_B	: Barrier height
V_{bi}	: Built in voltage
χ_S	: Electron affinity of semiconductor
$\in_S$	: Permittivity of semiconductor
$\in_0$	: Permittivity of free space

V_a	: Applied voltage to Schottky Contact
N_d	: Doping concentration of semiconductor
J	: Current Density
J_F	: Forward Current Density
V_F	: Forward Voltage Drop
η	: Ideality Factor
A^*	: Richardson's constant
k	: Boltzmn constant
T	: Temperature
q	: Electronics Charge
$\Delta\phi_b$	: Potential lowering
n_i	: Intrinsic Carrier Concentration
A	: Schottky Contact Area
V_n	: Potential between conduction band and Fermi level under flat band Conditions
δ	: Interfacial film width
R_S	: Series Resistance
V_B	: Breakdown Voltage
$\in_{cr}$	: Critical electric field
R_{on-sp}	: Specific on-resistance
μ_n	: Electron mobility
W_d	: Depletion width
J_L	: Leakage Current Density
E_m	: Maximum Electric Field
V_R	: Reverse Bias Voltage
P_d	: Power Dissipation
α	: Gradient

CHAPTER 1

INTRODUCTION

1.1 General Introduction

At present, focus of the SiC crystal growth development is on improving the crystalline quality without polytype inclusions, micro pipes and the occurrence of extended defects. High-quality substrates will significantly improve device performance and yield. The present activity in wide band-gap semiconductors has arisen from the need for electronics devices capable of operation at high power levels, high temperatures and harsh environments and separately from a need for optical materials, especially emitters which are active in the blue and ultraviolet wavelengths[1].

Silicon carbide (SiC) a material long known with potential for high-temperature, high-power, high-frequency, and radiation hardened applications , has emerged as the most mature of the wide-band gap ($2.0 \text{ eV} < E_g < 5.0 \text{ eV}$) [1] materials since the release of commercial 6H-SiC bulk substrates in 1991 and 4H-SiC substrates in 1994. The unique thermal and electronic properties of silicon carbide provide multiplicative combination of attributes which lead to one of the highest figure of merit for any semiconductor material for use in high-power,-speed, temperature, and frequency and radiation hard environments.

To meet the requirements for high voltage blocking devices such as high voltage Schottky diodes and MOSFETs, 4H-SiC epitaxial layers have to exhibit low doping concentration in order to block reverse voltages up to few keV and at the same time have a low on-state resistance. High Ron leads to enhanced power consumption in the operation mode of the devices. In growth of thick layers for high voltage blocking devices, the conditions to achieve good on-state characteristics become more challenging due to the low doping and pronounced thicknesses needed, preferably in short growth periods. In case of high-speed epitaxy such as the sublimation, the need to apply higher growth temperature to yield the high growth rate, results in an increased concentration of background impurities in the layers as well as an influence on the intrinsic defects [2].

Metal-Oxide-Semiconductor (MOS) capacitors were fabricated and characterized on 4H-SiC epilayers grown by PVT (sublimation) epitaxial and compared to the two properties of similar structures on CVD grown layers [2].

The successive development of any material for semiconductor applications depends to a large degree on the capability of producing high quality single crystals of that material with controlled electronic properties. The development of SiC had long been hindered by a lack of suitable crystal growth technology. Two significant factors in SiC's crystal growth problems are its ability to grow in many different crystal structures, called polytypes and its inability to be melted at a reasonable pressure [2].

1.2 Overview of SiC

1.2.1 Brief history of SiC

Silicon-based power devices have long dominated the power electronics and power systems applications. Devices such as bipolar, unipolar, controlled, uncontrolled, and MOS-gated made by Si are widely used by power electronics and power systems designers.

Silicon Carbide (SiC) was discovered in 1824 by the Swedish scientist Jons Jacob Berzelius , who received part of his education at Linkoping. SiC is also known as carborundum or moissanite, in natural form it is found in meteorites . The first electroluminescence has been reported in 1907 , when a SiC light emitting diode was made[2]. One method for growing high quality SiC crystals was presented by J.A. Lely in 1955. The method was based on sublimation and enabled growth of SiC platelets.

This invention has initiated a lot of research on SiC electronic applications. However, due to unsteady crystal supply, limited crystal size and the fact that most often 6H polytype was grown, the research ceased at the early 70's although it was maintained in the Soviet Union. The breakthrough was made in 1978.

The modified Lely method was reported by Tairov and Tsvetkov . The method uses a seeded sublimation process and reduces the problems with yield and polytype control, even though crystalline quality was low. The method is commonly termed physical vapor transport (PVT). The seeded sublimation technique is used to grow SiC boules from which wafers are commercially produced today. In 1987 Cree Research Inc. was founded and it was the first commercial vendor of SiC wafers. Nowadays, the commonly used method to grow SiC

epitaxial layers is chemical vapor deposition (CVD)[2]. It provides good structural quality and excellent doping control, however it suffers from low growth rates of about 3-5 µm/hour, thus growth of very thick layers is time consuming and creates a need for long-term process control.

Due to the increased interest that SiC received, series of conferences was introduced, such as the International Conferences on Silicon Carbide and Related Material (ICSCRM) and the European Conferences on Silicon Carbide and Related Materials (ECSCRM). The rapid growth in SiC research is reflected in the number of contributions, which increased from 28 at the first ICSCRM conference held in Washington, D.C. in 1987 (by that time called as First International Conference on Amorphous and Crystalline Silicon Carbide and Related Materials) to 430 at the latest one in Lyon, France 2003, making this conference the largest meeting of its kind worldwide.

The need for faster devices with high voltage and high switching frequency capability is growing, Silicon-based devices are not able to meet these requirements without costly cooling systems, so Wide band-gap based semiconductor devices such as silicon carbide and gallium nitride offer multiple advantages for power electronic designers. The superior physical properties of these semiconductors offer a lower intrinsic carrier concentration (10–35 orders of magnitude), a higher electric breakdown field (4–20 times), a higher thermal conductivity (3–13 times), a larger saturated electron drift velocity (2–2.5 times) which is suitable for faster devices with high voltage and high switching frequency.

1.2.2 Chemical bonding and crystal structure

The physical and electronic properties of SiC make it an excellent semiconductor material for high temperature, radiation resistant, and high-power/high-frequency electronic devices. Electronic devices based on SiC can operate at extremely high temperatures without suffering from intrinsic conduction effects because of the wide energy bandgap. Also, this property allows SiC to emit and detect short wavelength light, which makes the fabrication of blue light emitting diodes and UV photo detectors possible, even though the indirect band gap makes the efficiency low.

SiC can withstand an electric field over eight times greater than Si or GaAs without undergoing avalanche breakdown. SiC is an excellent thermal conductor. At room

temperature, SiC has a higher thermal conductivity than any metal. This property enables SiC devices to operate at extremely high power levels and still dissipate the large amounts of excess heat generated. SiC devices can operate at high frequencies (RF and microwave) because of the high-saturated electron drift velocity in SiC.

SiC is a IV-IV compound semiconductor with a covalent bonding of about 12% ionicity. It exist in more than 200 polytypes . The main building block for all forms is a tetrahedron consisting of a carbon atom bonded to four silicon atoms as shown in Fig.1.1

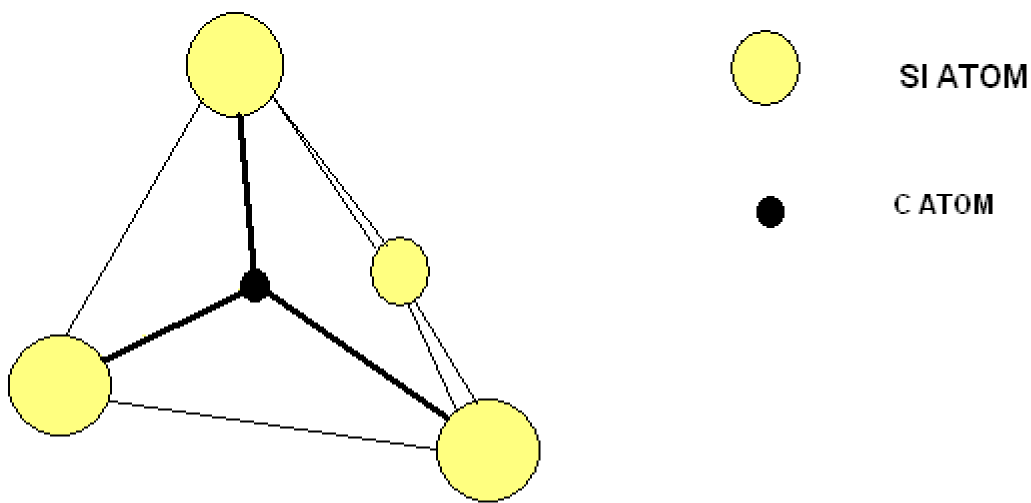


Figure: 1.1 Chemical bonding in SiC

1.3 SiC Material Properties

1.3.1 Crystal Structures and Polytypes

SiC consists of both the Si and C atoms, which are group IV element materials. Each Si atom shares electrons with four C atoms, which means that each atom is bonded covalently to four neighbors, and vice versa. The basic structural unit is already shown in Fig.1.1 The approximate bond length between Si and C atoms is 1.89 Å and the length between Si-Si or C-C atoms is 3.08 Å.

SiC has a properties known as a polytypism. It means that the material can possess more than one crystal structure. Each crystal structure is called a polytype. The different polytypes are defined by the stacking sequence. For instance, 2H, 4H, and 6H is hexagonal structure and has an AB, ABAC, ABCACB stacking sequence, respectively. Similarly, 3C is cubic with ABC stacking sequence.

In Fig. 1.3 the stackings equence is shown for the three most common polytypes ,3C,6H and 4H. If the first double layer is called the A position ,the next layer that can be placed according to a closed packed structure will be placed on the B position or the C position. The different polytypes will be constructed by permutations of these three positions.For instance will the 2H-SiC polytype have a stacking sequence ABAB … The number thus denotes the periodicity and the letter the resulting structure which in this case is hexagonal. The 3C- SiC polytype is the only cubic polytype and it has a stacking sequence ABCABC …or ACBACB …A common crystalline defect is the so called Double Positioning Boundary(DPB), which is commonly seen in 3C-SiC grown on on –axis 6H- SiC substrates. The defect arises when is lands of the two possible stacking sequences ABCABC and ACBACB meet.
When the stacking sequence is drawn in this manner a zig zag pattern is revealed. The surrounding lattice does not, however, look the same for each position. In the Fig.1.5, the A position has a different surrounding lattice than the B and C positions. We call this position the hexagonal site, h. It is simply characterized as the turning point of the zig zag pattern.
The other two positions (B and C) are called cubic, k1 and k2. An impurity replacing a host atom at one of the three sites will obtain a different binding energy depending on the site it replaces. A very illustrative example is the nitrogen donor in 6H-SiC. The hexagonal site gives rise to the P-level of the nitrogen donor with a binding energy of approximately 85 meV. The two cubic sites will give the R- and S-levels with binding energies around 138 meV and 142 meV, respectively. In the 4H-SiC polytype there are only two in-equivalent sites, one hexagonal and one cubic (Fig.1.5). The two levels of the nitrogen donor are in this case called P and Q. In 3C there is of course only one cubic site and in 2H there is only one hexagonal site (Fig.1.5). The 6H-SiC polytype can thus be characterized as being 33% hexagonal, whereas the 4H- and 2H-SiC polytypes are 50% and 100% hexagonal, respectively.

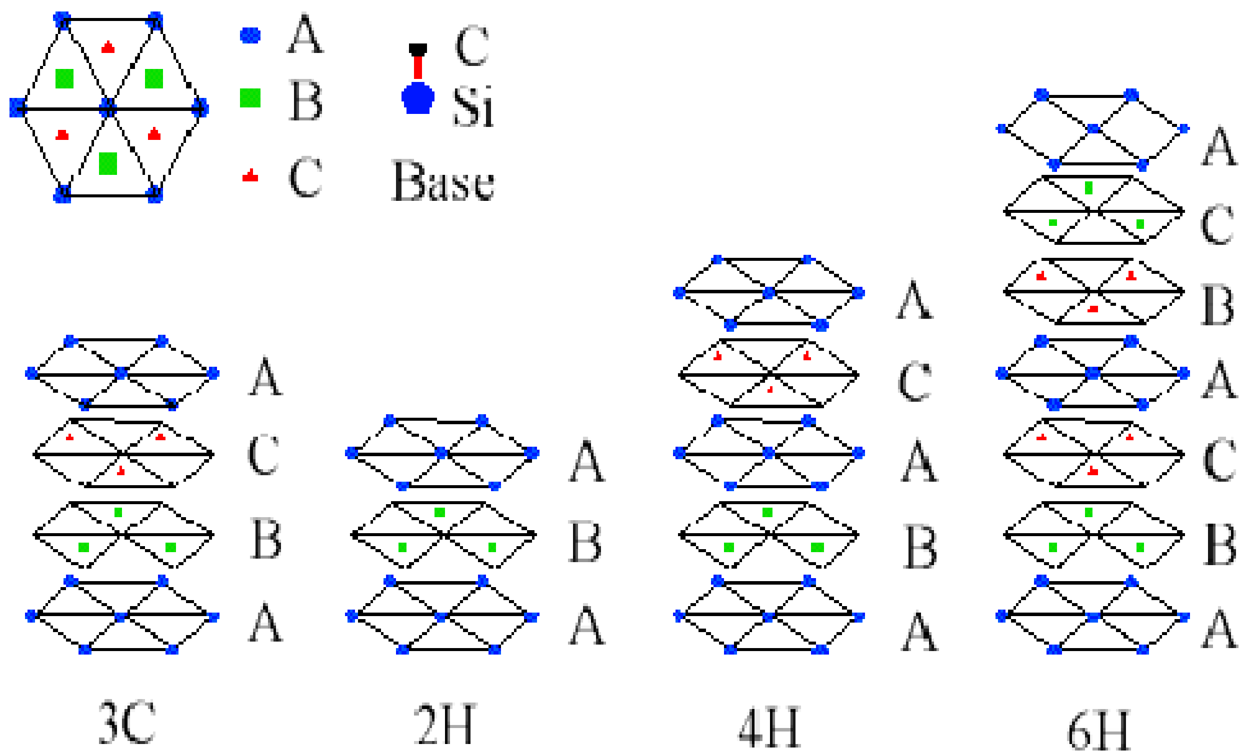
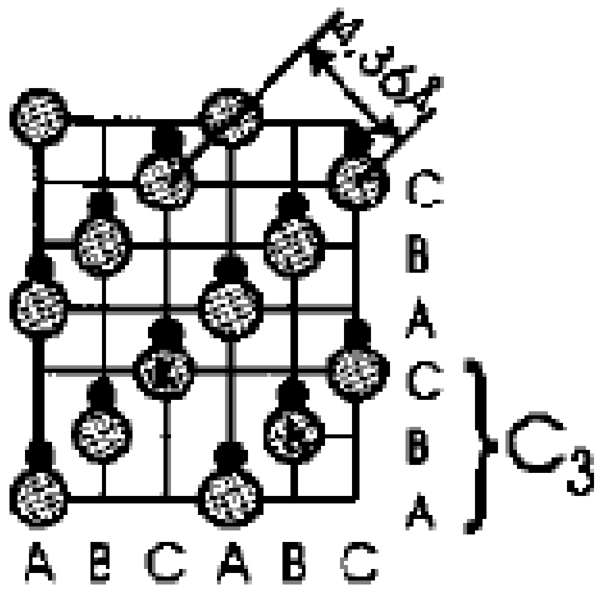


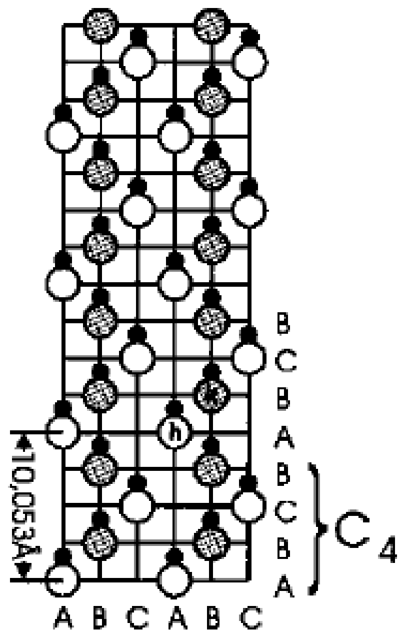
Figure-1.2:The stacking sequence of double layer of the three most common SiC polytypes [3].

There are basically three types crystal polytypes of Silicon namely 3C ,4H, 6H. The structure is shown below in Fig. 1.3:-

a) 3C



b) 4H



c) 6H

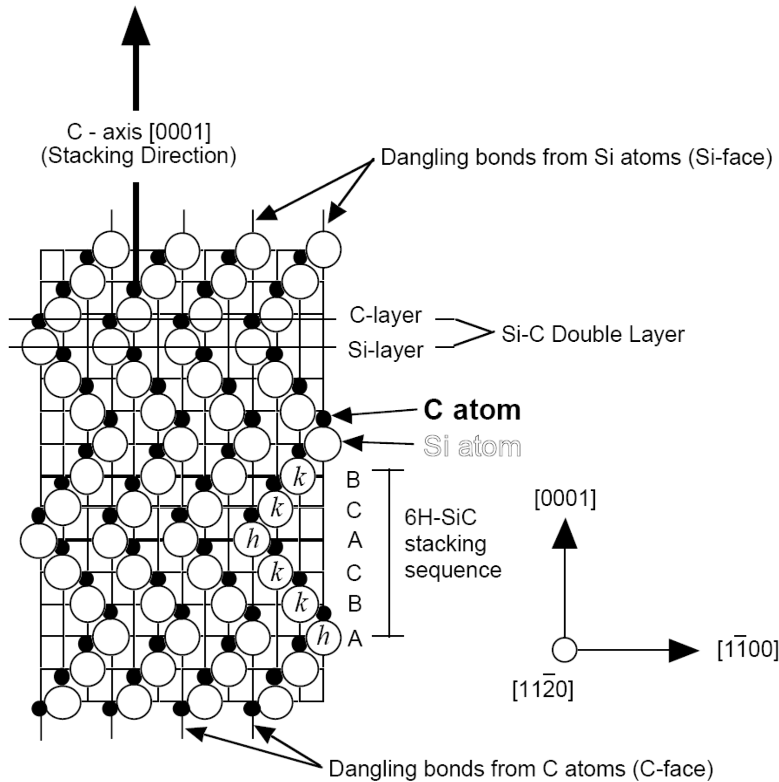


Figure:1.3 Structure of 3C,4H,6H[4]

1.3.2 SiC Electrical Properties

Due to the differing arrangement of Si and C atoms within the SiC crystal lattice, each SiC polytype exhibits unique fundamental electrical and optical properties.

SiC has a high critical field of about 2·106V/cm, a high thermal conductivity of 3-4 W/cmK, and a high saturated carrier velocity of 2·107 cm/s. Thanks to these properties, SiC devices have a large potential for high power, high temperature, and high frequency applications. Even within a given polytype, some important electrical properties are non-isotropic, in that they are a strong functions of crystallographic direction of current flow and applied electric field . Dopants in SiC can incorporate into energetically in equivalent quasi-hexagonal (*h*) C-sites or Si-sites, or quasi-cubic (*k*) C-sites or Si-sites. While all dopant ionization energies associated with various dopant incorporation sites should normally be considered for utmost accuracy.

The most important SiC property of all is the large band gap ,which is nearly three times larger than that of silicon. The large SC bonding energy makes SiC resistant to chemical attack and radiation. Silicon carbidebe longs to a class of semiconductors commonly known as wide bandgap semiconductors, where conventional semiconductors like Si and GaAs cannot adequately perform under extreme conditions. The wider band gap of SiC also enables one to design smaller ,higher density devices that will with stand high voltages. The high thermal conductivity of SiC decreases the need for special packaging and system cooling for device operation.

Some important parameter related to the electrical properties of SiC ars shown in below table:-

Table 1.1

Properties of common semiconductors SiC Structure GaAs 4H-SiC 3C-SiC 6H-SiC[5]

Property	**Silicon**	**GaAs**	**4H-SiC**	**6H-SiC**	**3C-SiC**
Bandgap (eV)	1.1	1.42	3.2	3.0	2.3
Relative Dielectric Constant	11.9	13.1	9.7	9.7	9.7
Breakdown Field $N_D = 10^{17}$ cm^{-3} (MV/cm)	0.6	0.6	//c-axis: 3.0	// c-axis: 3.2 ⊥c-axis: > 1	> 1.5
Thermal Conductivity (W/cm-K)	1.5	0.5	3 - 5	3 - 5	3 - 5
Intrinsic Carrier Concentration (cm^{-3})	10^{10}	1.8 x 10^6	~ 10^{-7}	~ 10^{-5}	~ 10
Electron Mobility @ $N_D = 10^{16}$ cm^{-3} (cm^2/V-s)	1200	6500	//c-axis: 800 ⊥c-axis: 800	//c-axis: 60 ⊥c-axis: 400	750
Hole Mobility @ $N_A = 10^{16}$ cm^{-3} (cm^2/V-s)	420	320	115	90	40
Saturated Electron Velocity (10^7 cm/s)	1.0	1.2	2	2	2.5
Donor Dopants & Shallowest Ionization Energy (meV)	P: 45 As: 54	Si: 5.8	N: 45 P: 80	N: 85 P: 80	N: 50
Acceptor Dopants & Shallowest Ionization Energy (meV)	B: 45	Be, Mg, C: 28	Al: 200 B: 300	Al: 200 B: 300	Al: 270
1998 Commercial Wafer Diameter (cm)	30	15	5	5	None

1.3.3 SiC Structural Defects

In this world there is no any crystal which is perfect. All crystal has some defacts. Crystal structure contains point defects by the absence of atoms or presence of extra atoms. In a compound semiconductor such as SiC, antisite defect, i.e. Si substitutes for C sites and vice versa, will be also present. These defects may alter the electrical and optical properties.

If a host atom is removed from the lattice, a vacancy is formed. This results in four unsaturated bonds, which have impact on electrical properties of the crystal. If the atom is inserted (either host or impurity atom) into an interstitial site, *Schottky* interstitial is formed. In the case of the interstitial atom staying in the vicinity of the vacancy, the *Frenkel* interstitial is formed. Dislocation is another type of defect which is of two types namely screw (Figure1.3.3) and edge (Figure1.3.2) character.

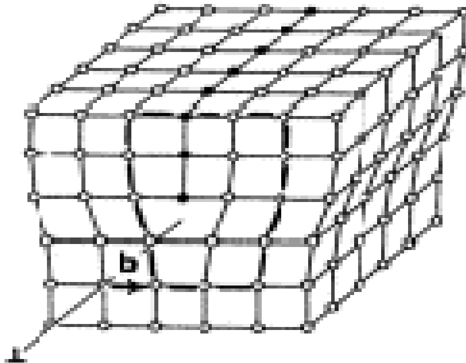


Figure1.4a *Edge dislocation*

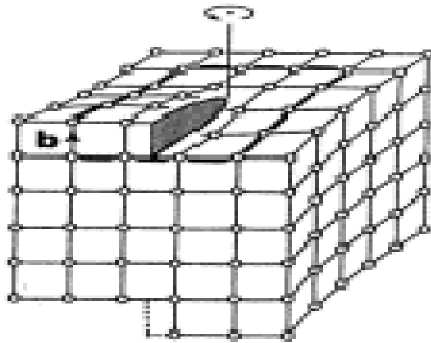


Figure1.4b *Screw dislocation*

1.4 Silicon Carbide Devices

Silicon carbide has several unique properties (higher breakdown field, wider band-gap , lower thermal generation rate, and lower intrinsic carrier concentration) to enhanced performance in devices [6].

1.4.1 Power MOSFETs

The break down electric field of SiC is approximately 8x higher than silicon. This makes it possible to design power switching devices having correspondingly higher blocking voltages than their silicon counterparts. More importantly , the specific on-resistance (i.e. resistance-area product) of a power device scales inversely as the cube of the breakdown field, so the on-resistance of SiC power MOSFETs are 100-200x lower than comparable devices in silicon.

1.4.2 Lateral Power MOSFETs

The maximum blocking voltage of vertical power devices in SiC is presently limited by the thickness of commercially available epilayers. The developed first lateral power MOSFET sin SiC, exhibit blocking voltages of 2.6 kV, which is a new world record.

1.4.3 Schottky Barrier Diodes

Schottky barrier diodes (SBD's) are attractive as power rectifiers because they donot store minority carriers in the on-state, and therefore can be switched off quickly with negligible

reverse current. It is widely felt that SBD's will be the first SiC power devices to goin to commercial production. The fabricated SBD's on 4H-SiC that exhibit blocking voltages of 1720V,equal to the current world record.

1.4.4 Microwave Devices

The high saturated drift velocity, high break down field, and high thermal conductivity of SiC make It an ideal material for high-power microwave amplifiers in the 10GHz regime. Two types of devices are under development :a vertical device known as a static induction transistor (SIT) and a lateral MESFET with sub-micron gate[6].

1.4.5 IMPATT Diode Microwave Oscillators

IMPATT diodes are two-terminal semiconductor devices that generate RF power by introducing a 180° phase shift between current and voltage waveforms at microwave frequencies**.**

1.4.6 CMOS Integrated Circuits

The first 4H-SiC CMOS digital integrated circuits completed in September 1996. A second generation was complete d in March 1997. These are the first SiC CMOS circuits fabricated with an implanted P-well process, and the first to operate on a single 5V power supply

1.4.7 Non volatile Memories

The thermal generation rate in semiconductors is proportional to the intrinsic carrier concentration ni, and ni decreases exponentially with band gap energy. Wideband gap semiconductors have dramatically lower thermal generation, with the thermal generation rate of 4H-SiC being about 16 orders- of-magnitude lower than silicon. This makes it possible to construct one-transistor memory cells in SiC which retain information for many years with out power.

1.4.8 Charge Coupled Devices

CCDs are unique MOS devices in which charge packets are shifted laterally a long the semiconductor surface by a ppropriate clocking applied to surface ectrodes. CCDs are widely used as imagers in video cameras and digital still cameras. They have developed he first

CCDs in SiC, where the wider band gap makes it possible to image scenery in the UV portion of the spectrum without being over whelmed by visible light [6].

1.4.9 NMOS Integrated Circuits

The low the rmal generation rate in SiC make s it possible to operate integrated circuits at much higher temperatures than silicon. Their group developed the first digital integrated circuits in SiC in late 1993 .The seearly circuits were implemented in enhancement mode NMOS.

1.5 Crystal Growth Basis of SiC

At present the research in crystal growth centers around increasing the growth rate, increasing the wafer diameter, and reducing material defects. In 1955, a laboratory sublimation process for growing a-SiC crystals was developed. In this process the nucleation of individual crystals is uncontrolled and the resulting crystals are randomly-sized hexagonal-shaped a-SiC platelets[7].To avoid this type of defect the modified sublimation process for growing SiC single crystals is introduced.

In 1987, a research group under R. F. Davis at North Carolina State University (NCSU) announced the successful implementation of a seeded growth sublimation process , a modification to the original sublimation process[8].

In the modified sublimation process, only one large crystal is grown, and this crystal consists of a single polytype. In this process, which is the basis of current commercial growth systems, a charge of polycrystalline SiC is heated in a graphite crucible containing argon at 200 Pa. A temperature gradient is established, with the polycrystalline SiC at about 2400 C and a seed crystal at about 2200 C. At these temperatures, SiC sublimes from the polycrystalline source and condenses on the cooler seed crystal.

The students from the NCSU group founded a small company, Cree Research, to produce SiC wafers commercially. In 1990 ,25 mm single crystal wafers of 6H-SiC were introduced. At present, 35 mm diameter wafers of both 4H and 6H SiC are commercially available from Cree Research (Durham, NC, USA) and from Advanced Technology Materials, Inc. (Danbury, CT, USA) [9].

The modified method is currently used to produce commercial grade 4H-SiC. Limited progress has been made in producing 3C-SiC substrates in the laboratory using 3C-SiC seeds grown by chemical vapor deposition (CVD) on Si wafers. Difficulties in producing 3C-SiC wafers by sublimation method may be due to the high temperatures used in the sublimation method, which promote the crystallization of hexagonal and rhombohedral polytypes. Polycrystalline SiC wafers can be fabricated using sintered pressed powders or using CVD.

1.5.1 Epitaxial Growth

Chemical Vapor Deposition (CVD) is undoubtedly the most common technique for growing epitaxial SiC films. 6H-SiC and 4H-SiC are grown homoepitaxially on 6H-SiC and 4H-SiC wafers respectively. 3C-SiC is usually grown heteroepitaxially on Si or on 6H-SiC. Growth of 3C-SiC on Si substrates has been demonstrated in the 1960s using processes that were based on carbonization of Si at high temperatures in a hydrocarbon gas. The carbonization process is self limiting; therefore growth of only very thin films, of the order of hundreds of nanometers is practical. For a thicker film, a two step deposition process is employed where; step two involves film growth using silicon containing precursor gas. Modified CVD technique capable of growing films up to 100 microns thick with a background doping level of 1x10e14 cm-3. However single crystalline 3C-SiC grown on Si substrates has a lot of defects due to lattice mismatch etc.

1.5.2 Selective Doping

Since the diffusion coefficients of aluminum and nitrogen are so low that thermal diffusion is impractical due to this Selective doping of SiC is accomplished by ion implantation. The two common p-type dopants, aluminum and boron, produce relatively deep acceptor levels (211 meV and 300 meV respectively), but aluminum is generally used because of its smaller ionization energy[10]. To minimize amorphization during implantation, it is common to implant at elevated temperatures, typically around 650 C for nitrogen and up to 1100 C for aluminum. Boron can be successfully implanted at room temperature [11].

1.5.3 Ohmic Contact Formation

Ohmic contacts are of great importance to power devices, since the high current densities give rise to intolerable voltage drops across even small resistances. Ohmic contacts to n-type

material are typically formed by annealed nickel. The contacts are annealed at high temperatures, typically between 850 - 1050 C, in argon or vacuum.

Specific contact resistivities < $5x10^{-6}$ Ohm-cm^2 can be obtained to heavily doped n-type layers .Contacts to p-type material have been more difficult. The p-type contacts are typically formed by annealed aluminum, or by a bilayer of aluminum covered with titanium. Anneal temperatures are similar to those used for nickel contacts, but the contact resistivities are in the 10^{-3} to 10^{-5} Ohm-cm^2 range, depending on doping density . Very recently, Ostling and Lundberg reported contact resistivities to p-type 6HSiC in the mid-10-6 Ohm-cm2 range using sequential electron beam evaporation of cobalt and silicon, followed by a two step vacuum annealing process at 500 C and 900C. The thermal integrity of the metallization system is of importance for high temperature applications. Nickel ohmic contacts used for n-type material have been shown to be stable to very high temperatures (negligible change in resistance after 329 hours at 650 C or after short thermal cycles to 1300 C) but aluminum p-type contacts will not be capable of high temperature operation.

1.5.4 Silicon Carbide Production

Silicon Carbide is derived from powder or grain, produced from carbon reduction of silica. It is produced as either fine powder or a large bonded mass, which is then crushed. To purify (remove silica) it is washed with hydrofluoric acid.

There are three main ways to fabricate the commercial product. The first method is to mix silicon carbide powder with another material such as glass or metal, this is then treated to allow the second phase to bond. Another method is to mix the powder with carbon or silicon metal powder, which is then reaction bonded. Finally silicon carbide powder can be densified and sintered through the addition of boron carbide or other sintering aid. It should be noted that each method is suited to different applications.

1.6 Advantage of SiC Devices

The most beneficial advantages that SiC-based electronics are in the areas of high temperature device operation and high-power device operation.

1.6.1 High Temperature and Power Operation

Silicon carbide is not attacked by any acids or alkalis or molten salts up to 800°C. In air, SiC forms a protective silicon oxide coating at 1200°C and is able to be used up to 1600°C. The

high thermal conductivity coupled with low thermal expansion and high strength give this material exceptional thermal shock resistant qualities. The wide band gap energy and low intrinsic carrier concentration of SiC allow SiC to maintain semiconductor behavior at much higher temperatures than silicon .

The high breakdown field and high thermal conductivity of SiC coupled with high operational junction temperatures theoretically permit extremely high power densities and efficiencies to be realized in SiC devices. Figures 1.5 and 1.6 demonstrate the theoretical advantage of SiC's high breakdown field compared to silicon in shrinking the drift-region and associated parasitic on-state resistance of a 3000 V rated unipolar Power MOSFET device [20]. The high breakdown field of SiC relative to silicon enables the blocking voltage region to be roughly 10X thinner and 10X heavier-doped, permitting a roughly 100-fold decrease in the dominant blocking region (N-Drift Region) resistance R_D of Figure1.5 for the SiC device relative to identically rated 3000 V silicon Power MOSFET [12].

CHAPTER 2

METAL OXIDE FIELD EFFECT TRANSISTOR DEVICE INTRODUCTION

2.1 Theory of MOSFET

2.1.1 MOSFET Construction and Symbols

Power MOSFETs employ semiconductor processing techniques that are similar to those of today's VLSI circuits, although the device geometry, voltage and current levels are significantly different from the design used in VLSI devices. The metal oxide semiconductor field effect transistor (MOSFET) is based on the original field-effect transistor introduced in the 70s. Figure shows the device schematic, transfer characteristics and device symbol for a MOSFET. The invention of the power MOSFET was partly driven by the limitations of bipolar power junction transistors (BJTs) which, until recently, were the device of choice in power electronics applications[13] .

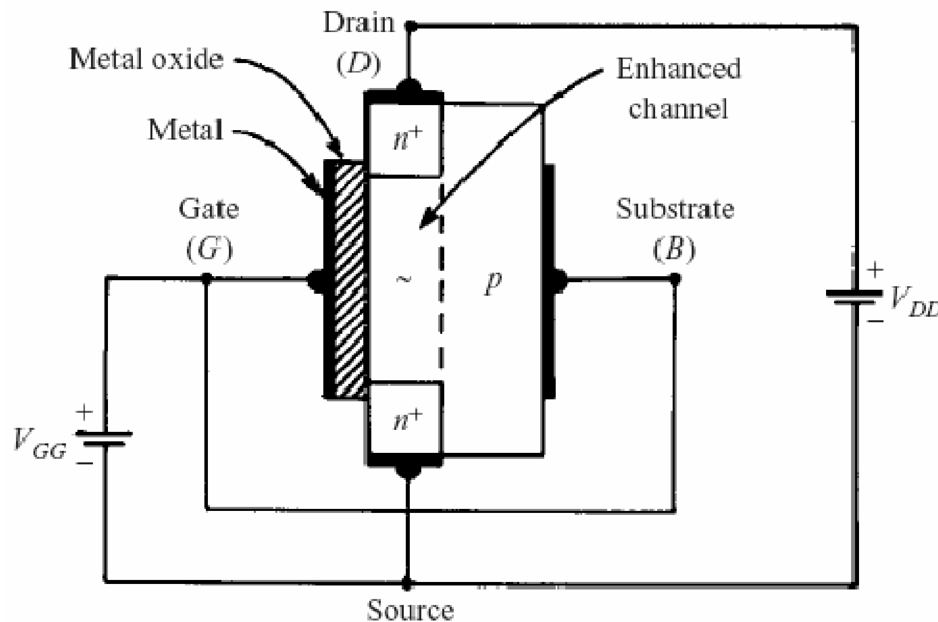


Figure 2.1 MOSFET Structure [13]

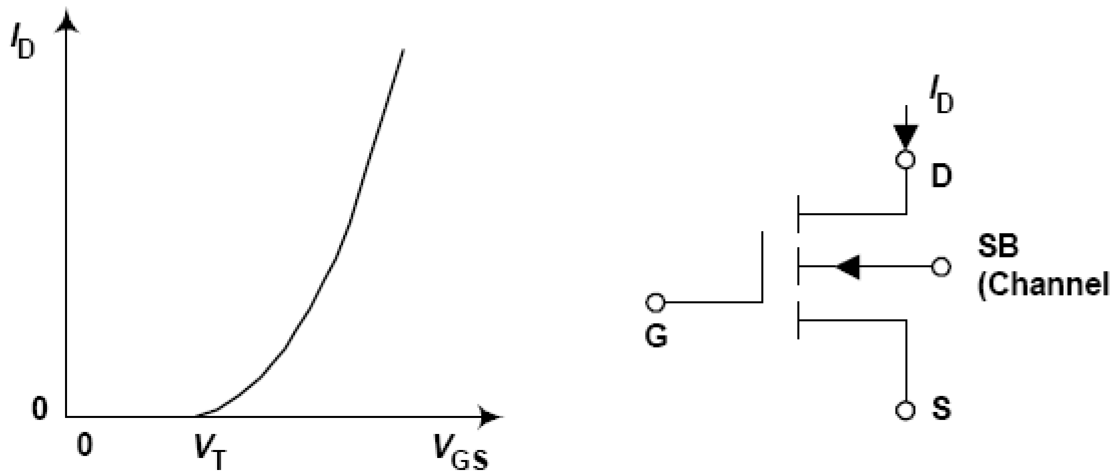


Figure 2.2 Transfer characteristics [13]

2.1.2 MOSFET Terminal Characteristics

In an n-channel MOSFET, the gate (positive plate), metal oxide film (dielectric), and substrate (negative plate) form a capacitor, the electric field of which controls channel resistance. When the positive potential of the gate reaches a threshold voltage VT (typically 2 to 4 V), sufficient free electrons are attracted to the region immediately beside the metal oxide film (this is called enhancement-mode operation) to induce a conducting channel of low resistivity. If the source-to-drain voltage is increased, the enhanced channel is depleted of free charge carriers in the area near the drain, and pinch off occurs as in the JFET.

2.1.3 Ideal MIS Diode

The metal-insulator semiconductor (MIS) structure is shown in fig 2.3, where d is the thickness of the insulator and V is the applied voltage on the metal field plate. The energy band diagram of an ideal MIS structure of p-type semiconductor for V=0 is shown in fig 2.3. An ideal MIS diode is defined as follows.

(1) At zero applied bias energy difference between metal work function _m and the semiconductor is zero, or the work-function difference _ms is zero.

(2) The only that can exist in the structure under any biasing condition are those in the semiconductor are and those with the equal but opposite sign on the metal surface adjacent to the insulator.

(3) There is no carrier transport through the insulator under dc biasing conditions or the resistivity of the insulator is infinity.

When the ideal MIS diode is biased with positive or negative voltages, basically three cases may exist at the semiconductor surface as shown in fig 2.3.

The three cases are as follows:

(a) Accumulation

(b) Depletion

(c) Inversion.

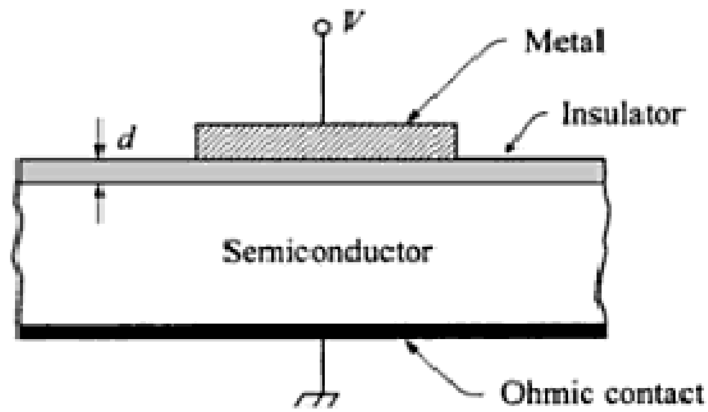


Figure 2.3: Metal-Insulator-Semiconductor (MIS) diode[13]

2.2 MOSFET Characteristics

2.2.1 Breakdown Voltage

Breakdown voltage, BV_{DSS}, is the voltage at which the reverse-biased body-drift diode breaks down and significant current starts to flow between the source and drain by the avalanche multiplication process, while the gate and source are shorted together [13].

For drain voltages below BV_{DSS} and with no bias on the gate, no channel is formed under the gate the surface and the drain voltage is entirely supported by the reverse-biased body drift p-n junction.

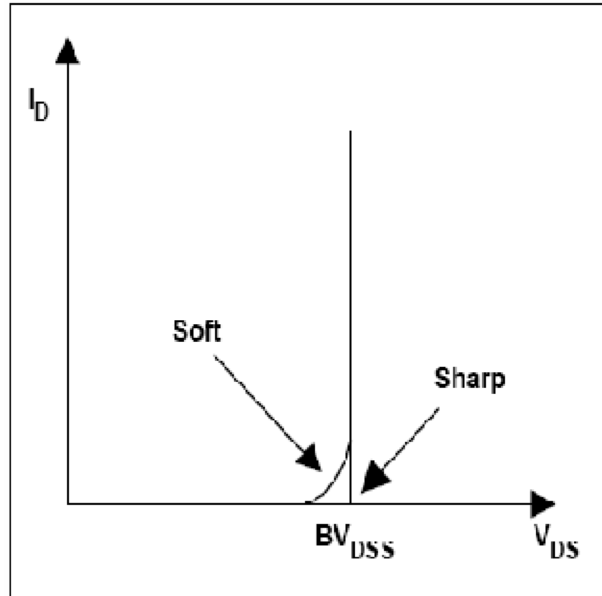


Figure 2.4 Drain voltages

2.2.2 On Resistance

The on resistance of a power MOSFET is the total resistance between the source and drain terminals during the on- state. It is the important device parameter because it determines the maximum current rating .The cell structure with each component of the specific on-resistance is shown in the Figure.

The on-state resistance of a power MOSFET is made up of several components as shown in Figure: 2.4 [13]

Where:

Rsource = Source diffusion resistance

Rch = Channel resistance

R_A = Accumulation resistance

R_J = "JFET" component-resistance of the region between the two body regions

R_D = Drift region resistance

Rsub = Substrate resistance

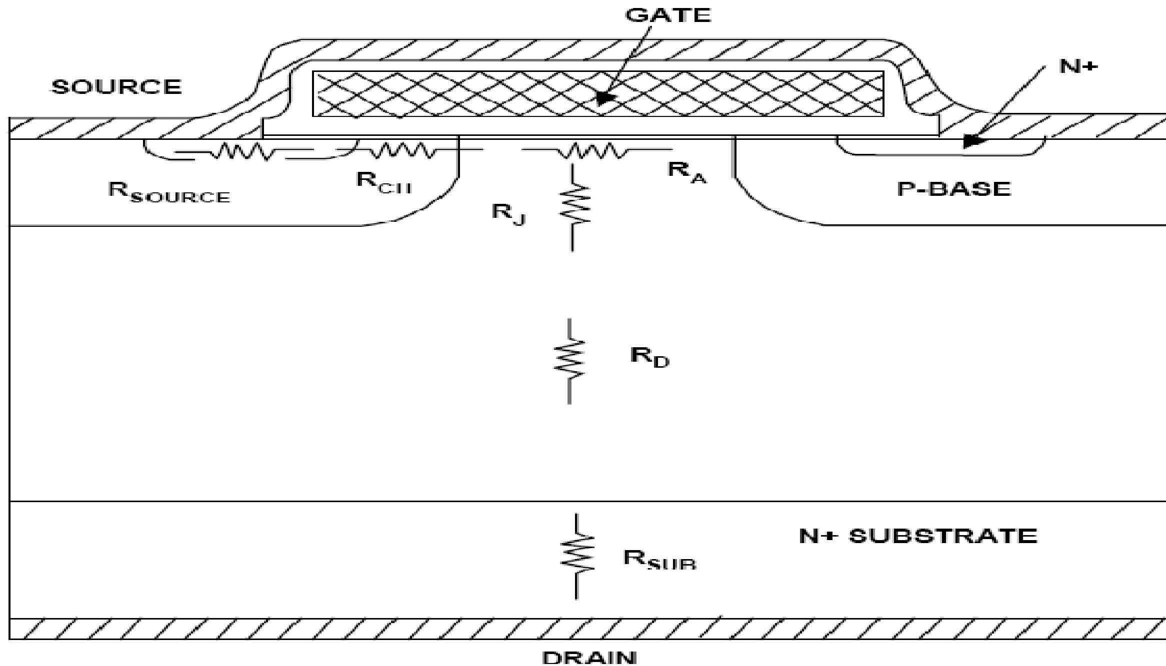


Figure 2.5 MOS Resistance [13]

2.2.3 Threshold Voltage

Threshold voltage, Vth, is defined as the minimum gate electrode bias required strongly inverting the surface under the poly and forming a conducting channel between the source and the drain regions. Vth is usually measured at a drain-source current of 250mA. Common values are 2-4V for high voltage devices with thicker gate oxides, and 1-2V for lower voltage, logic compatible devices with thinner gate oxides [13].

2.2.4 Power Dissipation

The maximum allowable power dissipation that will raise the die temperature to the maximum allowable when the case temperature is held at 250C is important [13]. It is give by Pd

$$P_d = \frac{T_{j\max} - 25}{R_{thjc}}$$

Where:

T_{jmax} = Maximum allowable temperature of the p-n junction in the device (normally 1500C or 1750C)

R_{thJC} = Junction-to-case thermal impedance of the device.

2.2.5 Diode Forward Voltage

The diode forward voltage, V_F, is the guaranteed maximum forward drop of the body-drain diode at a specified value of source current. P-channel devices have a higher VF due to the higher contact resistance between metal and p-silicon compared with n-type silicon [13].

2.2.6 Breakdown Voltages

There are basically two types of breakdown voltages, namely:

Avalanche breakdown

The junction formed by the substrate and drain or source region will conduct a large current if the reverse bias applied to them exceeds a certain value (because the field in the junction near the surface is influenced by the presence of the gate, the above value depends on the gate potential and can be different from the predicted common pn junction theory). When the device is on, carriers, moving fast in the channel can impact on silicon atoms and ionize them, producing electron-hole pairs; this is referred to as *impact ionization.* The newly generated pairs can gain enough energy to impact on silicon atoms and produce more electron-hole pairs. This is called *avalanche effect* and is more pronounced in the pinch-off region near the drain where field can be high. Currents larger than those predicted by common device model will then flow, and the phenomenon is referred to as *channel breakdown*.

Punch-Through breakdown

It occurs in devices with relatively short channels when the drain voltage is increased to the point that the depletion region surrounding the drain region extends through the channel to the source. The drain current then increases rapidly. Normally, punch-through does not result in permanent damage to the device.

2.3 The Characteristics of a MOSFET

2.3.1 Advantages

1. *High input impedance* - voltage controlled device - easy to drive. To maintain the on-state, a base drive current which is 1/5th or 1/10th of collector current is required for the current controlled device (BJT). And also a larger reverse base drive current is needed for the high speed turn-off of the current controlled device (BJT). Due to these characteristics base drive circuit design becomes complicated and expensive.

2. *Unipolar device* - majority carrier device - fast switching speed. As there are no delays due to storage and recombination of the minority carrier, as in the BJT, the switching speed is faster than the BJT by orders of magnitude. Hence, it has an advantage in a high frequency operation circuit where switching power loss is prevalent.

3. *Wide SOA* (safe operating area). It has a wider SOA than the BJT because high voltage and current can be applied simultaneously for a short duration. This eliminates destructive device failure due to second breakdown.

4. *Forward voltage drop with positive temperature coefficient* - easy to use in parallel. When the temperature increases, the forward voltage drop also increases. This causes the current to flow equally through each device when they are in parallel. Hence, the MOSFET is easier to use in parallel than the BJT, which has a forward voltage drop with negative temperature coefficient

2.3.2 Disadvantage

In high breakdown voltage devices over 200V, the conduction loss of a MOSFET is larger than that of a BJT, which has the same voltage and current rating due to the on-state voltage drop.

2.4 Power MOSFET

The Power MOSFETs that are available today perform the same function as Bipolar transistors except the former are voltage controlled in contrast to the current controlled Bipolar devices. Today MOSFETs owe their ever-increasing popularity to their high input

impedance and to the fact that being a majority carrier device, they do not suffer from minority carrier storage time effects, thermal runaway, or second breakdown.

The breakdown electric field of SiC is approximately 8x higher than silicon. This makes it possible to design power switching devices having correspondingly higher blocking voltages than their silicon counterparts. More importantly, the specific on-resistance (i.e. resistance-area product) of a power device scales inversely as the cube of the breakdown field, so the on-resistance of SiC power MOSFETs are 100-200x lower than comparable devices in silicon.

2.4.1 Types of Power MOSFET

1) *DIMOSFET*

DMOS transistors are common in silicon power device technology where the p-base and n+ source regions are formed by diffusion of impurities through a common mask opening. However, impurity diffusion is impractical in SiC because of the very low diffusion coefficients at any temperature. The diagram of DMOS is shown below in fig.[14]

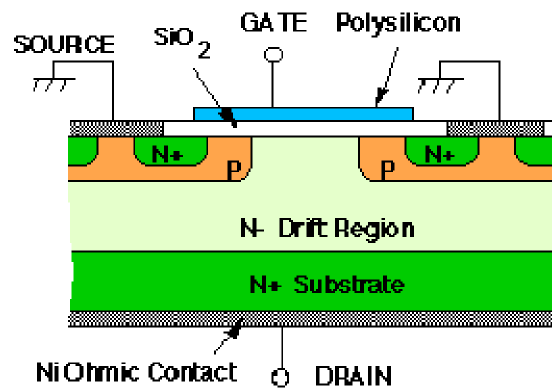


Figure 2.6 DIMOSFET

2) *UMOSFET*

The UMOSFET is formed by reactive ion etching, and the substrate acts as the drain electrode. The p-type base layer is grown by epitaxy and is grounded. As shown in Figure the UMOS forms the pn junction and the MOS channel. The large drain voltage is supported by the reverse-biased junction and the MOS capacitor. The electric fields in the pn junction and the MOS capacitor are shown to the right of the figure. In UMOSFETs the maximum blocking voltage depends on oxide breakdown and not on the semiconductor breakdown. The maximum breakdown voltage provided by the device is 260V [14].

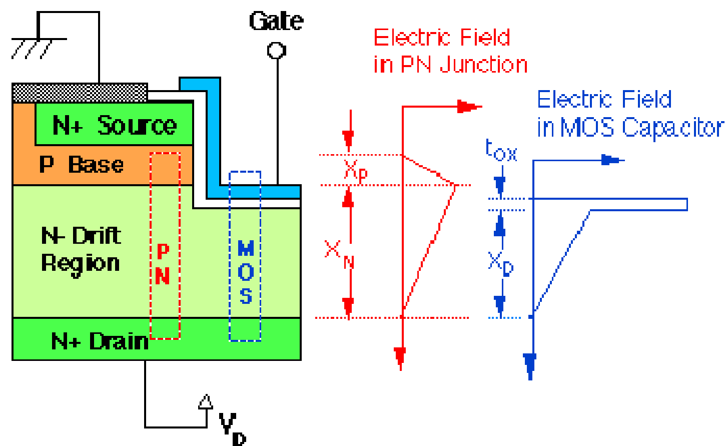


Figure 2.7 UMOSFET [14]

3) *Lateral or LDMOSFET*

In order to overcome the limitations of vertical-type MOSFETs we use the lateral type MOSFET . The structure of lateral DMOSFET is as shown in Figure in this the depletion layer spreads mainly into the lightly-doped drift region. Once the depletion region reaches the insulating substrate, it continues spreading toward the drain. Here, the maximum voltage is not limited by the thickness of the layer [15].

The maximum blocking voltage of vertical power devices in SiC is presently limited by the thickness of commercially available epilayers. The first lateral power MOSFETs developed in SiC devices exhibit blocking voltages of 2.6 kV, a new record.

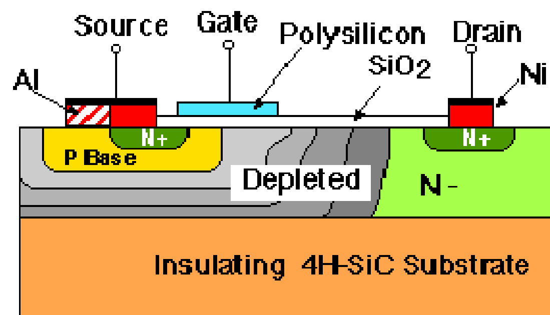


Figure 2.8 Lateral or LDMOSFET [15]

2.4.2 Applications of Power MOSFETs

Power MOSFETs are ideally suited for use in many applications, some of which are listed below [16].

- Switched mode power supplies (SMPS)
- Variable speed motor control.
- Automotive switching applications.

CHAPTER 3

4H-SiC DMOSFET

3.1 Introduction

The Double Implanted Metal-Oxide Semiconductor (DIMOS) field effect transistor has been frequently used in high voltage power electronics applications. Power switching devices are reaching the upper limits imposed by low breakdown field of silicon, and high breakdown voltage can be achieved only by using a semiconductor with a higher breakdown field. SiC is unique among compound semiconductors since its native oxide is SiO_2, the same oxide as of silicon. This means that power devices used in silicon can all be fabricated in SiC. DMOS transistors are common in silicon power device technology where the p-base and n+ source regions are formed by diffusion of impurities through a common mask opening.

3.1.1 DIMOS structure for modeling

An analytical model for a DIMOS field effect transistor is developed using 4H-SiC material. The model is developed based on the methodology for a vertical double diffusion MOS model. The proposed DIMOS model incorporates the effect of SiC device behavior [17].
The detail of DIMOS structure identifying different region of operation is shown in Figure 3.1.

Where:

h drift-region height of the device (cm)(depends on Vb and doping profile),

W width of t he device (cm),

W_j height of the p-body (cm),

W_t total vertical height (cm),

W_d depletion width (cm),

L channel length formed under the gate and inside the p-body(cm),

L_p length of p-body (cm),

L diff separation of p-bodies (cm),

z total length of the device (cm),

T_{ox} oxide thickness (cm),

V_T threshold voltage of the device (volt),

V_{GS} applied gate to source voltage (volt),

V_{sat} saturation velocity (cm/sec),

q Electronic charge (C),

α angle of slope oft he drift region narrowing (degree),

Eo permittivity constant in free space (F/cm),

E_{ox} oxide permittivity (F/cm).

E_{sic} silicon carbide permittivity (F/cm),

A cross-sectional area of the device (cm2), and

C_{ox} oxide capacitance (F).

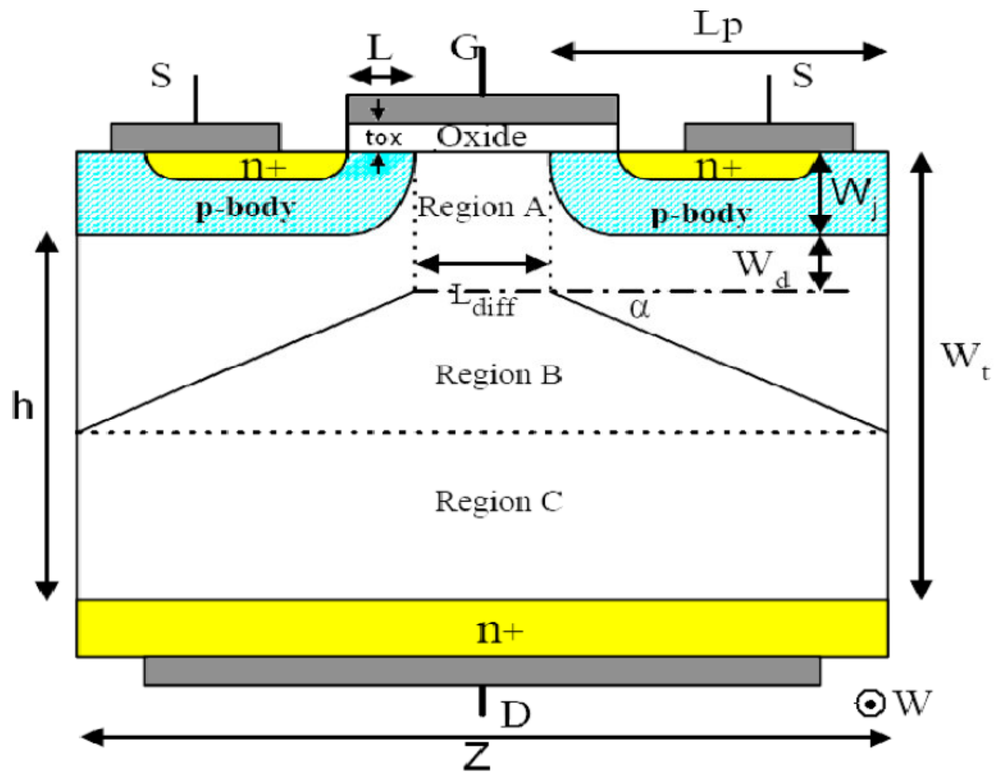


Figure 3.1 DIMOS structure

The drift region is divided into three parts: an accumulation region- A, a drift region-B with a varying cross-section area, and a drift region-C with constant cross-section. The

corresponding voltages to these regions are VA, VB, and VC for regions A, B, and C, respectively and they are given by the following equations [17].

$$V_A = \int_0^{W_j+W_d} E_y dy = \frac{I_D\left(W_j + W_d\right)}{WqN_d L_s \mu_n - I_d / E_c}$$

$$V_B = \frac{I_D}{WqN_d \mu_n \cot\alpha} \log\left[\frac{W_q N_d \mu_n \left(L_s + 2L_p\right) - I_d / E_c}{WqN_d L_s \mu_n - I_d / E_c}\right]$$

$$V_C = \frac{I_D\left(W_t + W_j + W_d - L_p \tan\alpha\right)}{WqN_d \mu_n \left(L_s + 2L_p\right) - I_d / E_c}$$

where W_j is the depth of n+ contact region,
W_d is the depth of depletion region,

W_t is the total thickness of epilayer,

L_s is th e length of accumulation region, and

L_p is the length of p-body.

The current/voltage characteristic in the triode region is given by Eq.

$$I_{ch} = \frac{W\mu_n}{2L\left[1 + \left(\mu_n / 2V_{satL}\right)V_{ch}\right]} V_{ch}\left[2C_{ox}\left(V_{GS} - V_T\right) - \left(C_{ox} + C_{do}\right)V_{ch}\right]$$

A summary of the device structure and doping levels is shown in table below:

Device Dimensions for the Proposed 4H-SiC DIMOS

Device dimensions		
Channel width		400 µm
Channel length		1 µm
Oxide thickness		500 Å
p-bodies separation		20 µm
Epilayer thickness		25 µm
Doping		
Region	*Doping level*	*Impurity*
n-drift	$4x10^{15}cm^{-3}$	Nitrogen
p-bodies	$4x10^{17}cm^{-3}$	Aluminum
n+ region	$1.5x10^{20}cm^{-3}$	Nitrogen

Table 3.1[17]

The proposed device structure and the device dimensions are selected in such a way that a practical device can be built on the basis of currently available SiC technology[17].

3.1.2 Fabrication of the DiMOSFET

The fabrication of the DiMOSFET begins with an n-type SiC wafer with a 2.5 · 1015 cm-3 doped, 20 µm thick epitaxial layers. The p-wells are formed by aluminum implantation followed by a heavy-dose nitrogen implant for the n+ source regions. A heavy-dose of aluminum is implanted to form the p+ contacts to the p-wells, in addition to the floating guard rings that terminate the edges. All implants are performed at 1600 ºC in Ar. A 2 µm oxide layer is deposited and patterned to serve as the field oxide, which is followed by gate oxidation. A 500 Å thick gate oxide is thermally grown at 1200 ºC in dry O2, then annealed in NO at 1175 ºC for 2 hours, as described in [18]. Next, a 0.25 µm molybdenum layer is sputtered and patterned for the gate metal. The contacts to the source, drain, and p+ regions are formed with alloyed Ni. The gate is then metalized with a 0.25 µm thick Ni/Au layer to reduce the gate resistance. Plasma- Enhanced Chemical Vapor Deposition (PECVD) oxide layers is then deposited as an inter-metallic dielectric, and via holes are opened for the

contacts. Finally, a 2 μm thick Ti/Pt/Au layer is deposited using e-beam evaporation and then lifted off as the final metal layer [18].

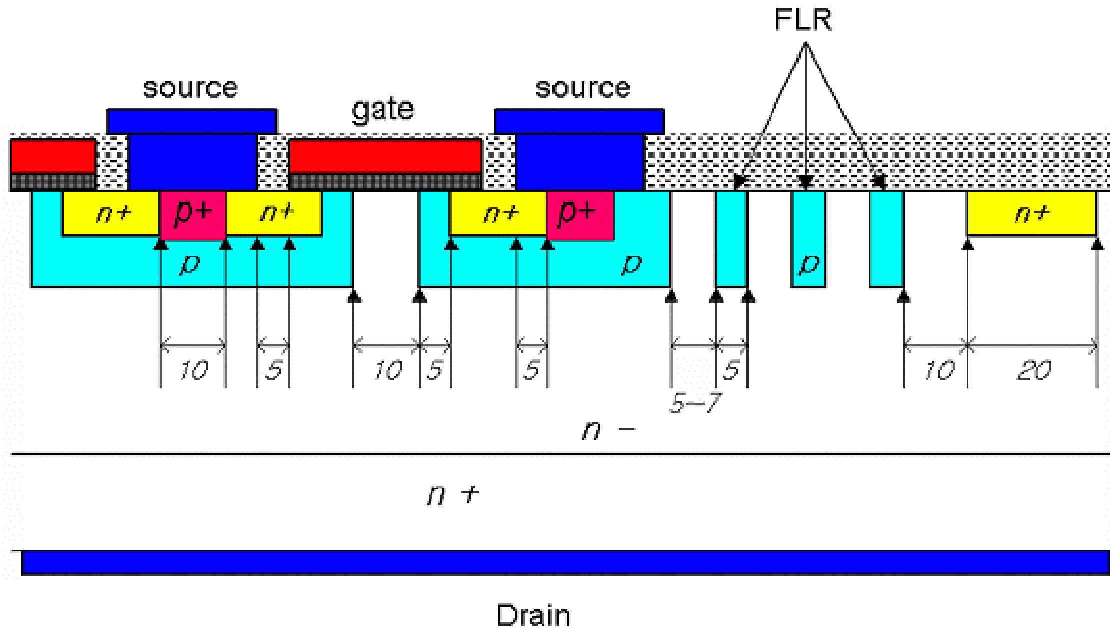


Figure 3.2 Cross-section of simplified 4H-DiMOSFET.

3.1.3 Device Theory and Analysis

To understand the flow f the current in the power DIMOS it is essential to analyze physics of the MOS device structure. It control s the characteristics of the channel region, which is responsible for output characteristics of the device. Physics of the power DIMOS have only majority carrier i.e. unipolar device [19].

3.1.4 MOS Physics

When a P-type semiconductor region is assumed, then the analysis of current transport in the n-channel power MOS will be applicable. In this analysis, the oxide layer is assumed to be a perfect insulator that doesn't allow any charge carrier between gate and semiconductor. The energy-band diagrams for an ideal MOS structure is with a P-type semiconductor for different bias potential at metal is shown in Fig. The change in the inversion region plays a key role for

determination of current transport in MOSFET devices. Here the ideal MOSFET has the following conditions:

a) The insulator has infinite resistivity,

b) Charge can exist only in semiconductor and on the metal electrode,

c) There is no energy difference between the work function of the metal and the semiconductor.

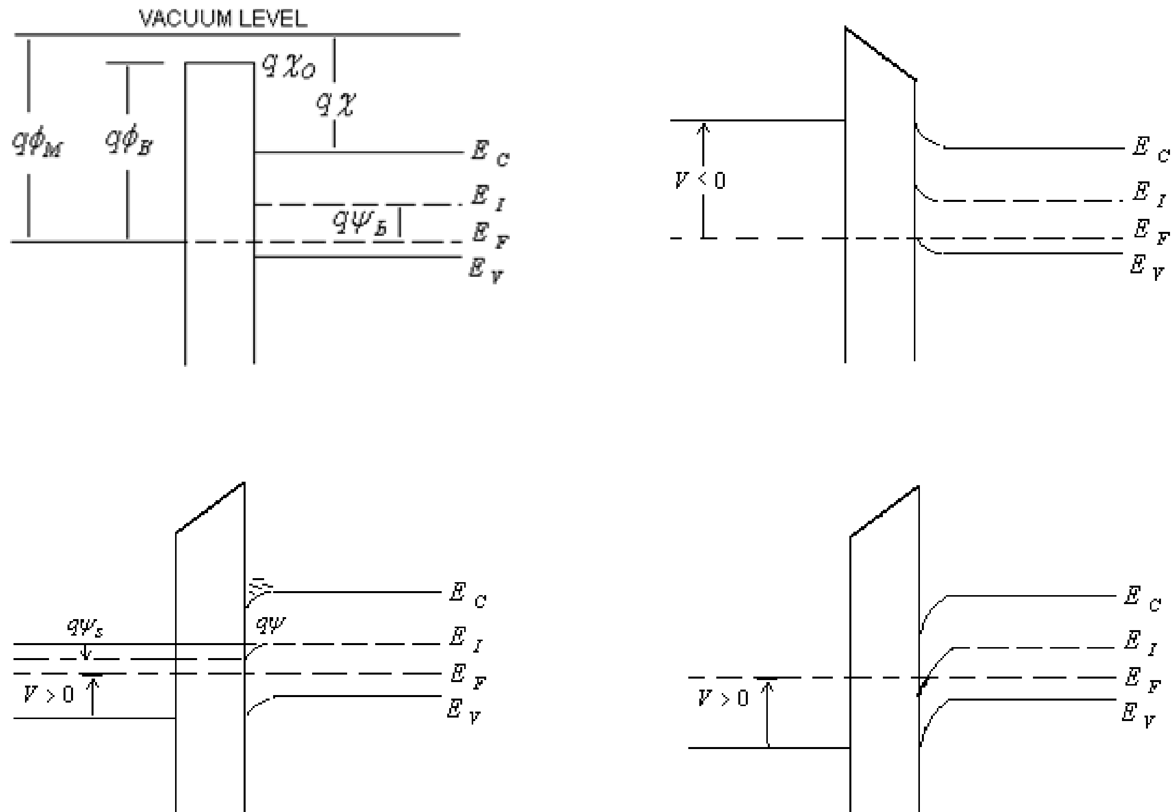


Figure-: 3.3 MOS structure with P-type semiconductor under different region (a) Flat-band energy band diagram (zero gate voltage) , (b) accumulation (negative gate voltage),(c) depletion (positive gate voltage) , (d) inversion (positive gate voltage)[19].

3.1.4 Forward Conduction Characteristics

The current flow in the power DIMOS during forward conduction is achieved by the applying positive gate bias voltage for N-channel device to create the conductive path. This

flow is limited by the total resistance between source and drain. This consists of several components as shown below in Fig. Where $R_{N.}$ is the contribution from then+- sources diffusion region ,CR is the channel resistance ,R_A is the accumulation layer resistance ,R_D is the drift region resistance and ,Rs is the substrate resistance and the portion of the drift region that comes to the upper surface between cells contributes R_J that is enhanced at high e drain voltage due to pinch – off action of depletion layer extending from the P-base regions. This phenomenon is called JFET action.

3.2 Basic Device Equations

3.2.1 On Resistance

The on resistance of a power MOSFET is the total resistance between the source and drain terminals during the on-state. It is the important device parameter because it determine s the maximum current rating.

The application of a positive drain voltage results in a current flow between drain and source through the N-drift region and conductive channel. For an ideal DIMOSFET, the resistances associated with the n+-source, the n-channel, the accumulation region and the n+-substrate are usually neglected and the specific on-resistance of the power MOSFET is determined by the drift region alone. In a power MOSFET, the blocking voltage appears across the drift layer and so the drift-region resistance is considered to be the minimum possible theoretical value for the on-resistance of a MOSFET.

The total specific on-resistance [6] is determined as

$$R_{on\text{-}sp} = R_{n}+ \ R_C + R_A + R_J + R_D + R_S$$

where

$R_{on\text{-}sp}$ is the specific on-resistance,

Rn+ is the contribution from the n+ -source,

R_C is the channel resistance,

R_A is the accumulation layer resistance,

R_J is the resistance from the drift region between the p-base regions by virtue of the JFET pinch off action,

R_D is the drift region resistance and RS is the substrate resistance.

DIMOS cell structure with each components of the specific on – resistance is shown below in figure.

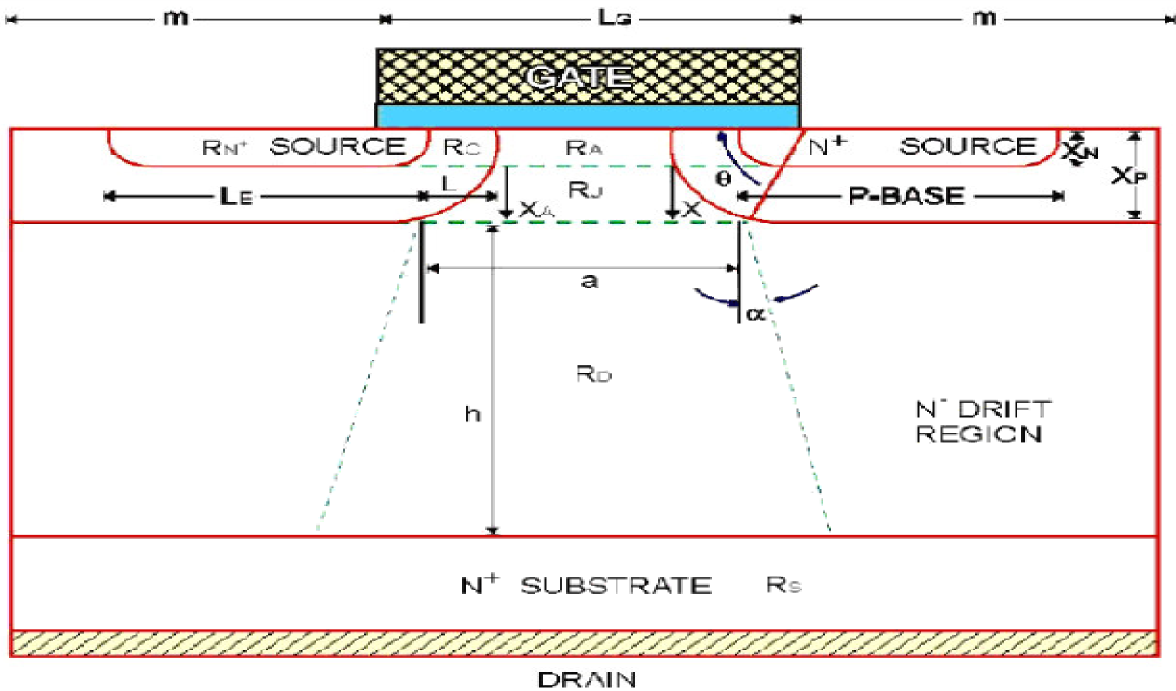


Figure 3.4: DIMOS cell structure [19]

The drift region analysis for an ideal DIMOSFET structure can be performed by taking the depletion layer in the drift region as an abrupt one-dimensional junction fabricated in a uniformly doped semiconductor. The doping level NB (cm-3) required to support a given breakdown voltage VB and the depletion width W (cm) [20] can be given by

$$N_B = \varepsilon \frac{E_c^{\,2}}{2qV_B}$$

$$W = \frac{2V_B}{E_c}$$

The specific on-resistance associated with the drift layer to support B V [21] is given by

$$R_{on-sp} = \frac{W}{qN_B \mu_n}$$

By the help of the above two equation we have to derive the equation for Ron in term of Vb and Ec:-

$$R_{on-sp} = \frac{4V_B^{\ 2}}{\varepsilon E_c^{\ 3} \mu}$$

Where € is the permittivity in F/cm, EC is the breakdown field in V/cm, q is the electronic charge in C and μ_n is the electron mobility in cm2/V-sec [22]. From the equations, it has been confirmed that both the mobility μ_n and breakdown field EC depend on N_B

3.2.1.1 The channel resistance per square centimeter for linear cell structure having gate oxide thickness is [26]

$$R_{ch,sp} = \frac{1}{2} \frac{L(L_G + 2m)}{\mu_{ns} C_{ox} (V_G - V_T)}$$

Where, L is typical channel length L_G is the length of the gate electrode,
m is the cell diffusion window,
V_G is the gate drive voltage (10V),
C_{OX} is the oxide capacitance, and
V_T is the threshold voltage.

3.2.1.2 To calculate the sources resistance, if a linear cell is considered with 1-cm extension perpendicular to the cross section as shown above in Fig.2.3, the source resistance per square centimeter duet o Ṇ-emitter region is given by

$$R_{n^+,sp} = \frac{1}{2} \rho_{n^+} L_E (L_G + 2m)$$

Where, L_G is the length of the gate electrode,

ρ_{n^+} is the sheet resistance of then diffusion,

2m is the cell diffusion window,

L_E is the emitter length and

($L_G + 2m$) is the cell repeat spacing.

3.2.1.3 The **accumulation region resistance** determines the current flow from the channel into the drift region. The accumulation region resistance per square centimeter is

$$R_{A,sp} = \frac{K(L_G - 2x_p)(L_G + 2m)}{\mu_{nA} C_{ox}(V_G - V_T)}$$

Where, K is the multiplying factor (3nearly) ,

C_{ox} Oxide capacitance per unit area, and

V_T is the threshold voltage.

3.2.1.4 Similarly JFET region resistance is given by the expression

$$R_{J,sp} = 2\rho_D(L_G + 2m)\left[\frac{1}{\sqrt{1+(2x_p/L_G)^2}}\tan^{-1}(.414)\sqrt{\frac{L_G+2x_p}{L_G-2x_p}} - \frac{\pi}{8}\right]$$

Where, ρ_D is the resistivity of the drift region.

3.2.1.5 The **drift region resistance** per unit square centimeter is given by

$$R_{D,sp} = \rho_D \frac{(L_G + 2m)}{\tan(\alpha)} \ln\left[1 + 2\frac{h}{a}\tan(\alpha)\right]$$

Where h is the drift region thickness

The drift region resistance is largest as compare to any other resistances so only the drift region resistance would be considerable.

3.2.2 Current Equation

The current/voltage characteristic in the triode region is given by Eq.

$$I_{ch} = \frac{W\mu_n}{2L\left[1+\left(\mu_n/2V_{satL}\right)V_{ch}\right]} V_{ch}\left[2C_{ox}\left(V_{GS}-V_T\right)-\left(C_{ox}+C_{do}\right)V_{ch}\right]$$

3.2.3 V-I characteristics of DIMOSFET

The V-I characteristics of DIMOSFET are shown in Figure

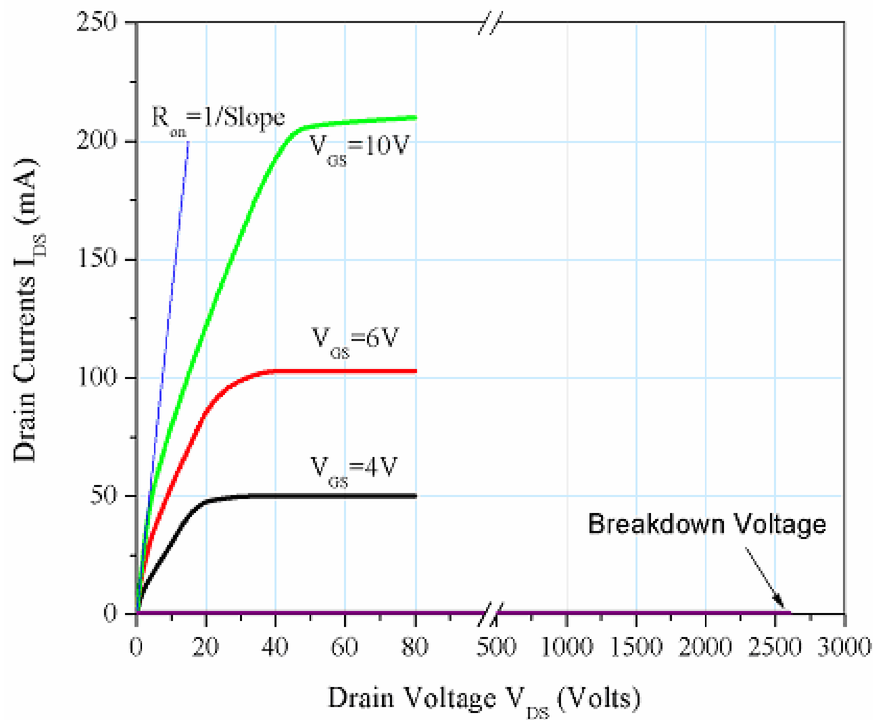


Figure 3.5 V-I characteristics of DIMOSFET

The blocking voltage of SiC DIMOSFETs is 760V[23] for 6H-SiC, this voltage is also use for fabrication purpose of SiC. But in 4H-SiC it is considerably high near about 2500V. To obtain the blocking voltage greater than 760 V for 6H-SiC depends on the drift region thickness, doping level, specific on-resistance and electric field strength. By adjusting all

these parameters we propose to get the blocking voltage greater than 760V [23]. The gate voltage has control over the drain currents as long as the drain current enters the saturation region before the velocity saturation occurs.

The safe operating area of MOSFET is divided into three regions:

(i) Maximum permissible drain current,

(ii) Maximum power dissipation limit, and

(iii) Maximum drain source voltage limit.

The safe operating area of MOSFET does not contain any second breakdown as seen in the BJT. This is because of the majority carriers present in the MOSFET

3.3 Mobility Vs Doping Concentration for 4H - SiC

This graph shows the variation of mobility with respect to doping concentration in 4H – SiC.[24]

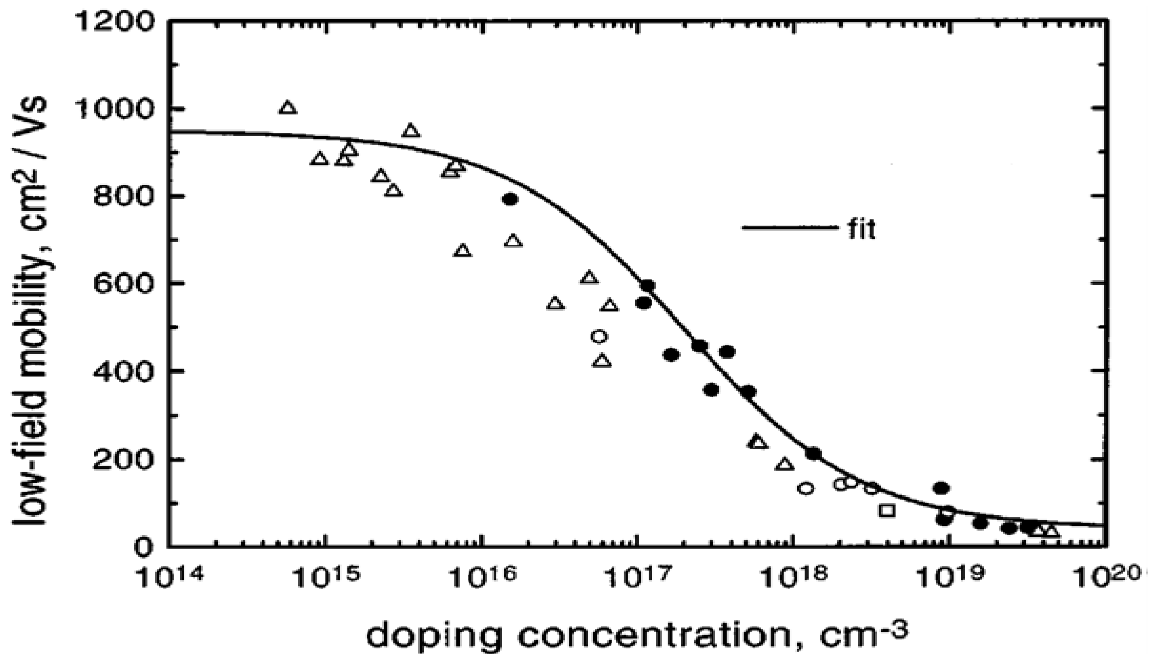


Figure: 3.6 Mobility Vs Doping Concentration for 4H - SiC

CHAPTER 4

4H-SIC VERTICAL DIMOSFET WITH GAUSSIAN PROFILE IN THE DRIFT REGION

The 4H-SiC is the preferred polytype since the bulk mobility is higher and more isotropic, compared to 6H-SiC [25]. Among many wide-band-gap semiconductor materials, 4H silicon carbide (4H-SiC) has great potential for use as a material for power devices owing to its crystal maturity and superior electrical properties such as nearly isotropic low-field mobility and high avalanche breakdown electric field [26].

The 4H-SiC DIMOSFET need for low voltage analysis has a Gaussian profile as its impurity content in the drift region. This profile has been generated by taking different value of height h and calculating the different value of depletion region width. The mathematical analysis for evaluation the depletion region width has been evaluated by integrating the Gaussian profile over the length of the drift region.

4.1 Structure of the 4H-SiC Power MOSFET

DMOS transistors are common in silicon power device technology where the p-base and n+ source regions are formed by diffusion of impurities through a common mask opening. However, impurity diffusion is impractical in SiC because of the very low diffusion coefficients at any temperature.

The Purdue group fabricated the first DMOS transistors in SiC using ion implantation to introduce dopants for the p-base and the n+ source [27]. The implanted DMOSFET requires that separate masks be used to define the p-base and the n+ source. The construction is a vertical structure with a drift layer built on a highly conductive n+ layer. The n-drift region is designed to give the forward blocking capabilities. The forward blocking capability is achieved by the pn junction between p-base region and n-drift region. During the device operation, a fixed potential to the p-base region is established by connecting it to the source metal by the break in the n+- source region. By short-circuiting the gate to the source and

applying a positive bias to the drain, the p-base/n-drift region junction becomes reverse-biased and this junction supports the drain voltage by the extension of depletion layer on both sides. However, due to the higher doping level of the p-base layer, the depletion layer extends primarily into the n-drift region.

On applying the positive bias to the gate electrode, the conductive path between the n+-source region and the n-drift region is formed. The application of positive drain voltage results in a current flow between drain and source through the n-drift region and conductive channel.

Figure 4.1 shows a cross section of a power MOSFET that has been fabricated using the process of diffusion using Silicon as substrate. The planar diffusion technology uses a infractory gate such as polysilicon. The P-base and N+- source region are diffused through a common window that is determined by the edge of the polysilicon gate. The difference in the lateral diffusion of these two regions determines the surface channel region. The p-base and N-drift region gives the forward blocking capability. The N-drift region is normally grown epitaxially on an N+ substrate of 4H-SiC crystal, where the P-base and N+ source regions are formed by ion-implantation.

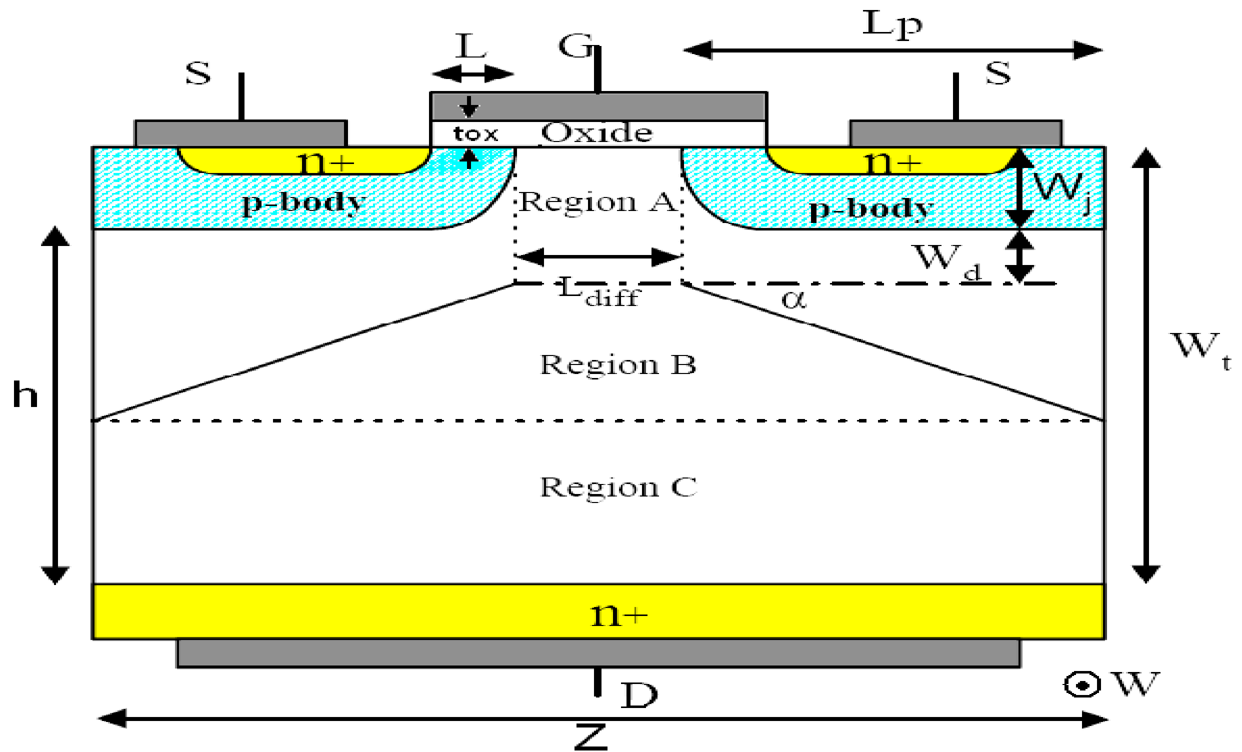


Figure-:4.1 Structure of Double Implanted Metal – Oxide Semiconductor (DIMOS)

Structure of Double Implanted Metal – Oxide Semiconductor (DIMOS) using Gaussian profile in drift region is shown in figure 4.2. Let the carrier concentration is N_o at x=0 Gaussian profile concentration is given by

$$N(x) = N_o \exp\left(-\left(\frac{h-x}{m} \right)^2 \right)$$

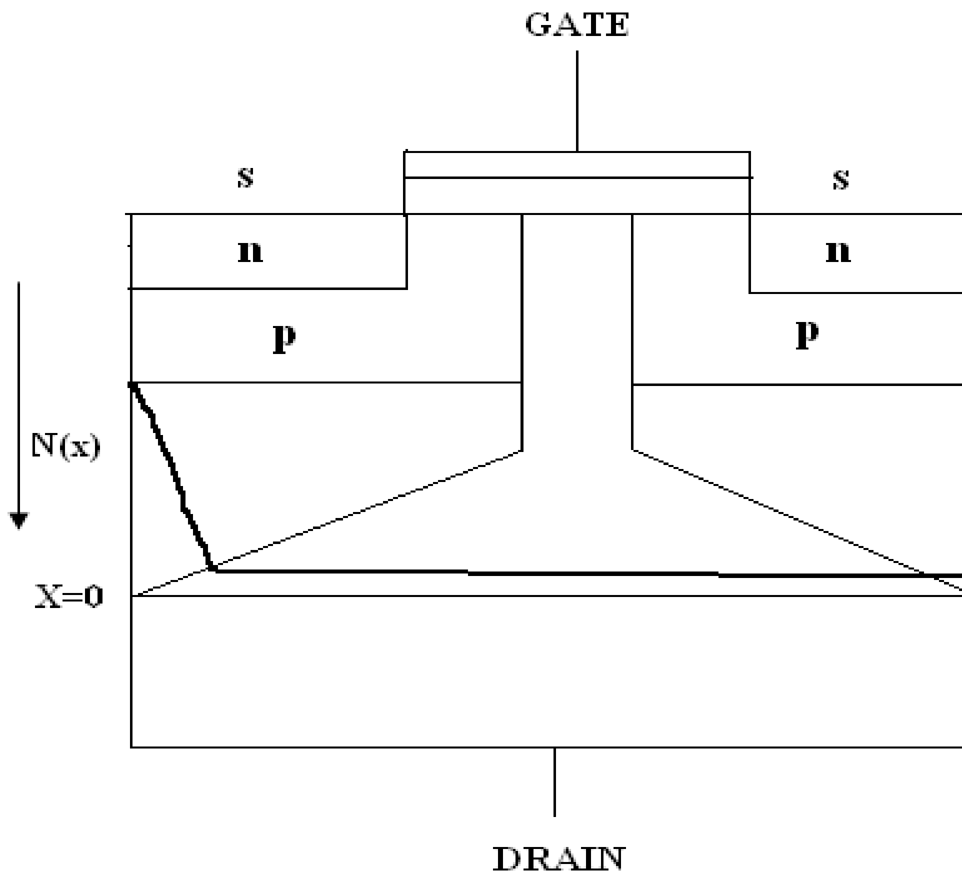


Figure 4.2 DIMOS using Gaussian profile in drift region.

From this fig the effective concentration is come out to be

Neff=0.8847× 10e15

4.2 Basic equations used in Gaussian doped profile

In this section the basic device equation and derivation for depletion region width has been derive.

Starting from Poisson's equation,

$$-\frac{\partial^2 V}{\partial x^2} = \frac{\rho}{\varepsilon} \tag{4.1}$$

Where ε the permittivity of semiconductor is, ρ is electric charge density and V is the potential developed in drift region.

We know ,

$$\rho = eN(x) \tag{4.2}$$

Where N(x) is the doping distribution

Putting the equation (4.2) to equation (4.2)

$$-\frac{\partial^2 V}{\partial x^2} = \frac{eN(x)}{\varepsilon} \tag{4.3}$$

But

$$N(x) = N_o \exp\left(-\left(\frac{h-x}{m}\right)^2\right) \tag{4.4}$$

Where h is device height and m is constant.

From equation (4.3) and (4.4)

$$-\frac{\partial^2 V}{\partial x^2} = \frac{e}{\varepsilon} N_o \exp\left(-\left(\frac{h-x}{m}\right)^2\right) \tag{4.5}$$

Now expanding exponential function

$$-\frac{\partial^2 V}{\partial x^2} = \frac{e}{\varepsilon} N_o \left[1 + \left(-\left(\frac{h-x}{m}\right)^2\right) + \frac{1}{2!}\left(-\left(\frac{h-x}{m}\right)^2\right)^2 + \frac{1}{3!}\left(-\left(\frac{h-x}{m}\right)^2\right)^3 + \dots\dots\dots\right]$$

Neglecting the higher order term and expanding

$$-\frac{\partial^2 V}{\partial x^2}=\frac{e}{\varepsilon}N_o\left[1-\left(\frac{h^2+x^2-2hx}{m}\right)+\left(\frac{h^4+x^4+6h^2x^2-4h^3x-4hx^3}{2m^2}\right)\right] \tag{4.6}$$

Now integrating w.r.t x

$$E=-\frac{\partial V}{\partial x}=\frac{e}{\varepsilon}N_o\left[x-\left(\frac{xh^2+\frac{x^3}{3}-hx^2}{m}\right)+\left(\frac{h^4x+\frac{x^5}{5}+2h^2x^3-2h^3x^2-hx^4}{2m^2}\right)\right]+C_1 \tag{4.7}$$

E is electric field developed in drift region of DIMOSFET.

Using boundary condition,

At x=h, E=0

From equation (4.7) we get,

$$C_1=-\frac{e}{\varepsilon}N_o\left[h-\frac{h^3}{3m}+\frac{h^5}{10m^2}\right]$$

Put the value of C_1 in equation (4.7)

$$E=-\frac{\partial V}{\partial x}=\frac{e}{\varepsilon}N_o\left[x-\left(\frac{xh^2+\frac{x^3}{3}-hx^2}{m}\right)+\left(\frac{h^4x+\frac{x^5}{5}+2h^2x^3-2h^3x^2-hx^4}{2m^2}\right)\right]-\frac{e}{\varepsilon}N_o\left[h-\frac{h^3}{3m}+\frac{h^5}{10m^2}\right] \tag{4.8}$$

Now again integrating w.r.t x

$$-V=\frac{e}{\varepsilon}N_o\left[\frac{x^2}{2}-\left(\frac{\frac{x^2}{2}h^2+\frac{x^4}{12}-h\frac{x^3}{3}}{m}\right)+\left(\frac{h^4\frac{x^2}{2}+\frac{x^6}{30}+h^2\frac{x^4}{2}-2h^3\frac{x^3}{3}-h\frac{x^5}{5}}{2m^2}\right)\right]-\frac{e}{\varepsilon}N_o\left[hx-\frac{h^3x}{3m}+\frac{h^5x}{10m^2}\right]+C_2$$

(4.9)

Using boundary condition,

At x=0, V=0

Hence $C_2=0$

If the depletion region width is w then

At x=w, V= V_{bi}

V_{bi} is the built in potential

$$-V_{bi}=\frac{e}{\varepsilon}N_o\left[\frac{w^2}{2}-\left(\frac{\frac{w^2}{2}h^2+\frac{w^4}{12}-h\frac{w^3}{3}}{m}\right)+\left(\frac{h^4\frac{w^2}{2}+\frac{w^6}{30}+h^2\frac{w^4}{2}-2h^3\frac{w^3}{3}-h\frac{w^5}{5}}{2m^2}\right)\right]-\frac{e}{\varepsilon}N_o\left[hw-\frac{h^3w}{3m}+\frac{h^5w}{10m^2}\right]$$

(4.10)

In reverse bias condition equation (4.10) reduce to

$$-(V_{bi}+V_R)=\frac{e}{\varepsilon}N_o\left[\frac{w^2}{2}-\left(\frac{\frac{w^2}{2}h^2+\frac{w^4}{12}-h\frac{w^3}{3}}{m}\right)+\left(\frac{h^4\frac{w^2}{2}+\frac{w^6}{30}+h^2\frac{w^4}{2}-2h^3\frac{w^3}{3}-h\frac{w^5}{5}}{2m^2}\right)\right]$$

$$-\frac{e}{\varepsilon}N_o\left[hw-\frac{h^3w}{3m}+\frac{h^5w}{10m^2}\right] \quad (4.11)$$

But in reverse bias

$V_R >> V_{bi}$

So that V_{bi} is neglected and rearranging the equation yield,

$$V_R \frac{\varepsilon}{eN_o} = w\left(h - \frac{h^3}{3m} + \frac{h^5}{10m^2}\right) + w^2\left(-\frac{1}{2} + \frac{h^2}{2m} + \frac{1}{12m} - \frac{h^4}{4m^2}\right) + w^3\left(-\frac{h}{3m} + \frac{h^3}{3m^2}\right)$$

$$+ w^4\left(-\frac{h^2}{4m^2}\right) + w^5\left(\frac{h}{10m^2}\right) + w^6\left(-\frac{1}{60m^2}\right) \tag{4.12}$$

At the breakdown point

$$V_R = V_B$$

$$V_B \frac{\varepsilon}{eN_o} = w\left(h - \frac{h^3}{3m} + \frac{h^5}{10m^2}\right) + w^2\left(-\frac{1}{2} + \frac{h^2}{2m} + \frac{1}{12m} - \frac{h^4}{4m^2}\right) + w^3\left(-\frac{h}{3m} + \frac{h^3}{3m^2}\right)$$

$$+ w^4\left(-\frac{h^2}{4m^2}\right) + w^5\left(\frac{h}{10m^2}\right) + w^6\left(-\frac{1}{60m^2}\right) \tag{4.13}$$

After drawing the profile between source and drain it looks similar to the uniform doping profile for particular value of depletion region width.

So the critical field is electric field developed at breakdown point and its value

$$E_c = 1.95 \times 10^4 \times N_o^{0.131} \tag{4.14}$$

The breakdown voltage V_B for uniform doping profile can be calculated from the equation,

$$V_B = \frac{E_c W}{2} \tag{4.15}$$

CHAPTER 5

CALCULATIONS AND RELATED GRAPHS

To calculate the breakdown voltage and depletion region width for Gaussian doped profile in drift region Double implanted Metal- Oxide Semiconductor (DIMOSFET) using the derived and basic equations and its related graphs are shown in this chapter:

5.1 Parameter used to calculate the breakdown voltage

Permittivity of semiconductor in free space ε_0 = 8.85 x 10^-14

Doping concentration N_o =10^15/cm^3

Permittivity of SiC semiconductor ε = 9.7 ε_0

Electron charge e = 1.6 x 10^ -19 coulomb

Constant m=3.2

Let us suppose the punch through breakdown voltage V_B =10 kV

Now rewrite the equation 4.13

$$V_B \frac{\varepsilon}{eN_o} = w\left(h - \frac{h^3}{3m} + \frac{h^5}{10m^2}\right) + w^2\left(-\frac{1}{2} + \frac{h^2}{2m} + \frac{1}{12m} - \frac{h^4}{4m^2}\right) + w^3\left(-\frac{h}{3m} + \frac{h^3}{3m^2}\right)$$

$$+w^4\left(-\frac{h^2}{4m^2}\right) + w^5\left(\frac{h}{10m^2}\right) + w^6\left(-\frac{1}{60m^2}\right)$$

For punch through breakdown voltage, depletion region width is equal to maximum height between source and drain.

Rearranging the equation 4.13

$$V_B \frac{\varepsilon}{eN_o} = h^2\left(\frac{1}{2}+\frac{1}{12m}\right)+h^3\left(-\frac{1}{3m}\right)+h^4\left(-\frac{1}{3m}+\frac{1}{2m}\right)+h^6\left(\frac{1}{10m^2}+\frac{1}{3m^2}-\frac{1}{4m^2}\right) \quad (5.1)$$

Now putting all above parameter

$$5.36\times10^{-5} = 0.52h^2 - 0.104h^3 + 0.052h^4 + 0.01786h^6$$

After solving it, we get,

h = 102.68 µm

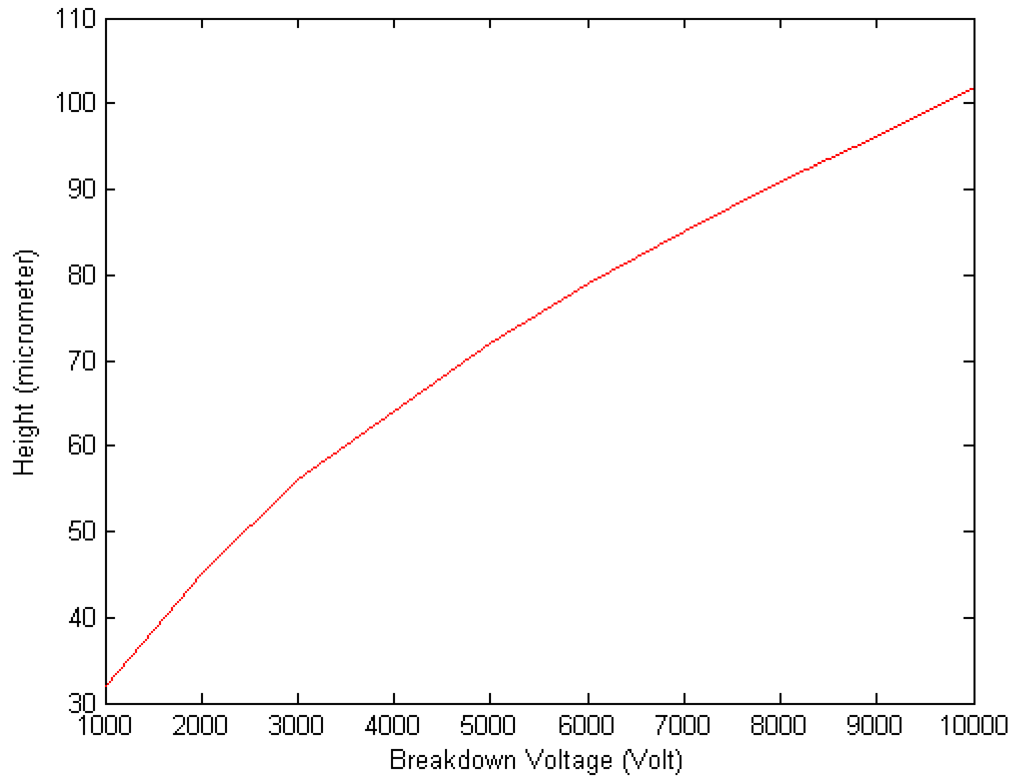
This is the minimum height between source and drain which we take for further analysis

Now calculating h for different value of breakdown voltage.

Table 5.1 Value of height h for different value of breakdown voltage.

S.No.	Blocking voltage V_B (Volt)	Height h (µm)
1	1000	32
2	2000	45
3	3000	56
4	4000	64
5	5000	72
6	6000	79
7	7000	85
8	8000	91
9	9000	96
10	10000	102

Figure 5.1 Plot of height h for different value of breakdown voltage.



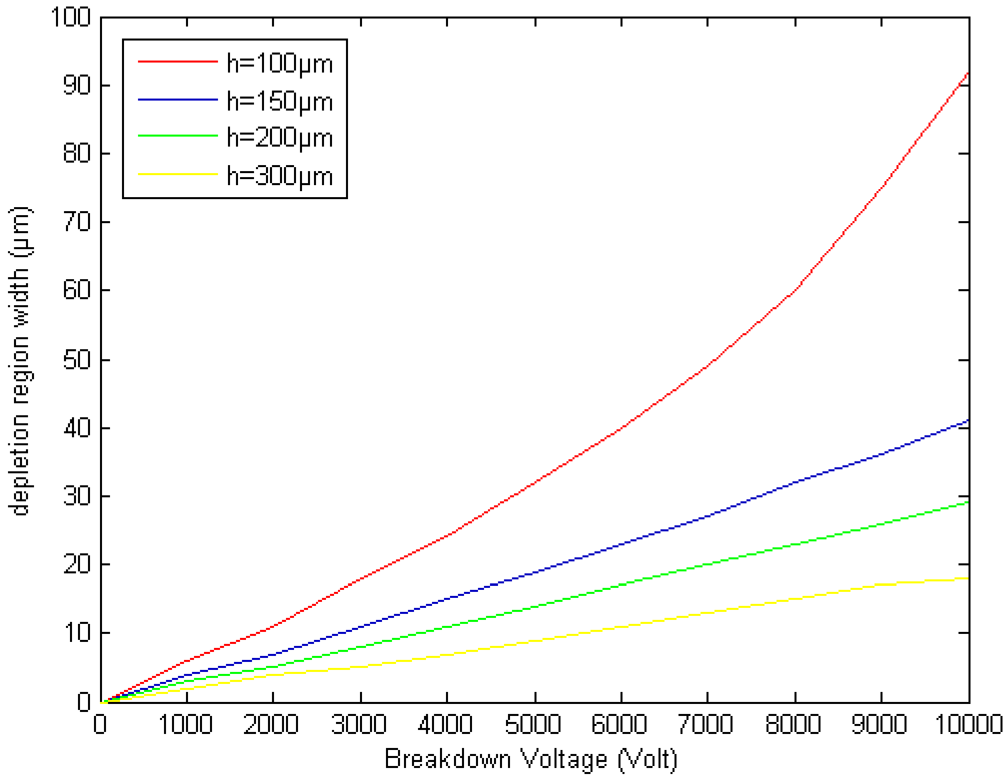
Now let us calculate depletion region width at different value of blocking voltage of different h.

For this we have again use the equation 4.13

Table 5.2 Variation of depletion region width with blocking voltage at different value of height h

S.No.	Blocking voltage V_B (Volt)	h=102 µm w(µm)	h=150 µm w(µm)	h=200 µm w(µm)	h=300 µm w(µm)
1	1000	5	4	3	2
2	2000	11	7	5	4
3	3000	17	11	8	5
4	4000	24	15	11	7
5	5000	31	19	14	9
6	6000	38	23	17	11
7	7000	47	27	20	13
8	8000	57	32	23	15
9	9000	70	36	26	17
10	10000	92	41	29	18

Figure 5.2 Plot of depletion region width with blocking voltage at different value of height h



Calculation of depletion region width with breakdown voltage for different value of concentration No and the constant value of height h=350µm.

Table 5.3 Depletion Region Width with breakdown voltage for different value of Concentration No

S.No.	Blocking voltage V_B (Volt)	No=10^14 w(µm)	No=10^15 w(µm)
1	1000	16.78	2.43
2	2000	32.64	3.24
3	3000	49.52	5.47
4	4000	68.21	6.84
5	5000	87.12	8.14
6	6000	108.2	9.74
7	7000	131.4	11.17
8	8000	156.32	12.48
9	9000	177.54	14.78
10	10000	198.14	16.53

Figure5.3 Plot for Depletion Region Width with breakdown voltage for different value of Concentration No

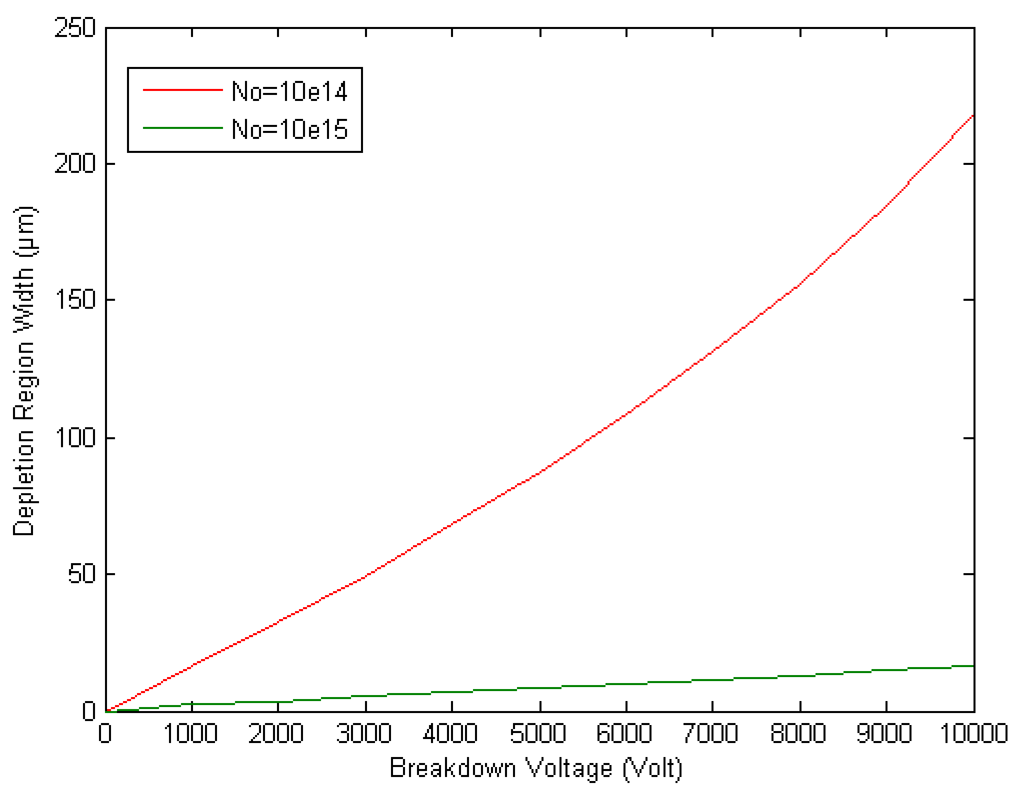
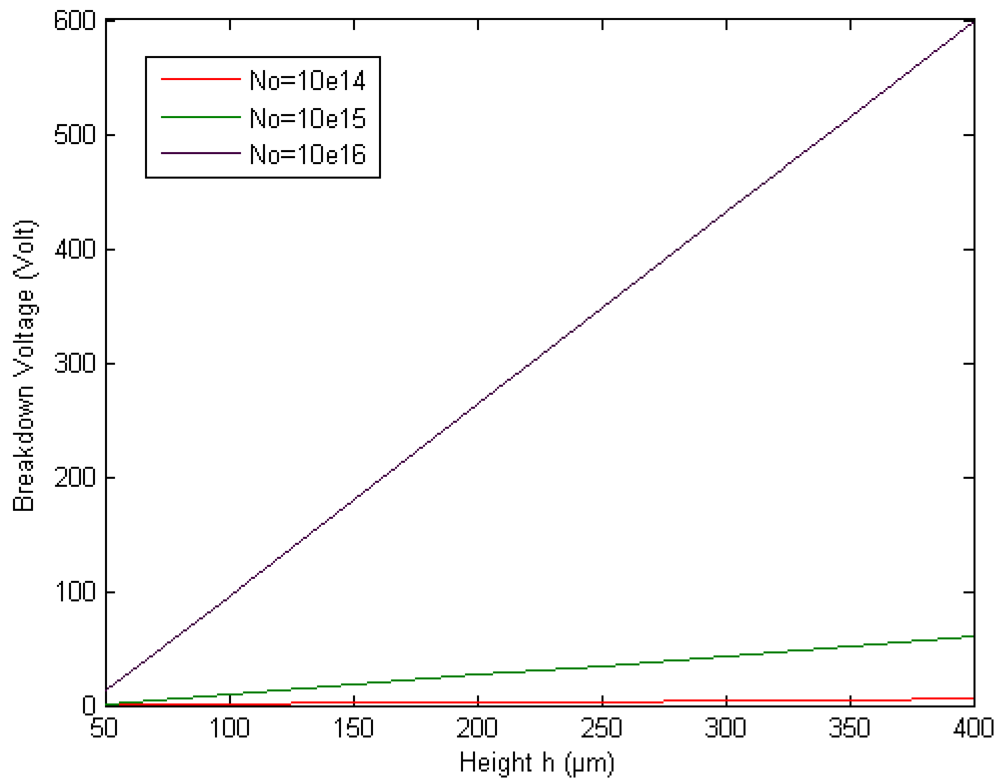


Table 5.4 Variation of Breakdown voltage for different value of height h and impurity concentration No

height (µm)	No=10^14 V_B (KVolt)	No=10^15 V_B (KVolt)	No=10^16 V_B (KVolt)
50	0.1233	1.233	12.33
100	0.963	9.63	96.3
150	1.8025	18.025	180.25
200	2.6416	26.416	264.16
250	3.4801	34.801	348.01
300	4.318	43.18	431.8
350	5.1551	51.551	515.51
400	5.9912	59.912	599.12

Figure 5.4 Plot of Breakdown voltage for different value of height h and No



Now calculate the value of avalanche Breakdown Voltage with the help of impurity concentration which is determine from the Gaussian doping profile and its value is about $0.8847\times10^{15}/cm^3$

Table 5.5 Value of blocking voltage at different value of depletion region width for uniform doping

S.No.	Blocking voltage V_B (Volt)	width w (µm)	V_B for Uniform doping (Volt)
1	1000	5.8	513.78
2	2000	11.7	1044.5
3	3000	17.87	1581.8
4	4000	24.76	2193.4
5	5000	31.65	2809.3
6	6000	38.5	3498.4
7	7000	49.6	4372.6
8	8000	62.3	5523.4
9	9000	0.8	7155.6
10	10000	102.4	9063.9

Figure 5.5a Plot of depletion region width for different value of breakdown voltage

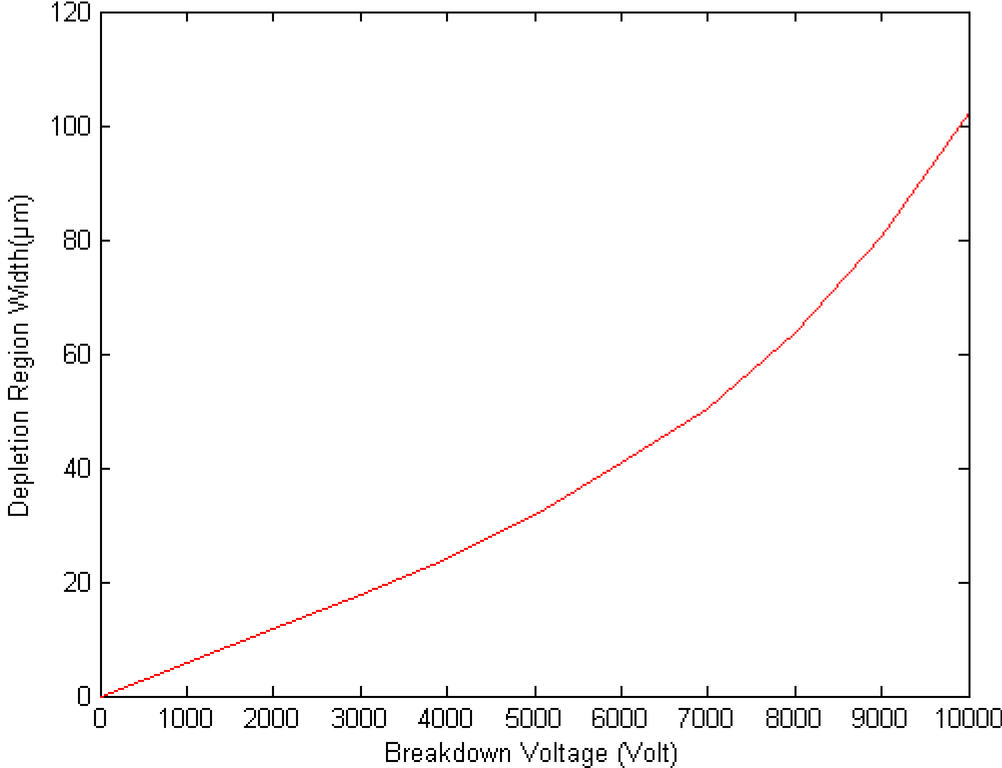


Figure 5.5b Plot for Avalanche and Punch through Voltage for different value of depletion region width

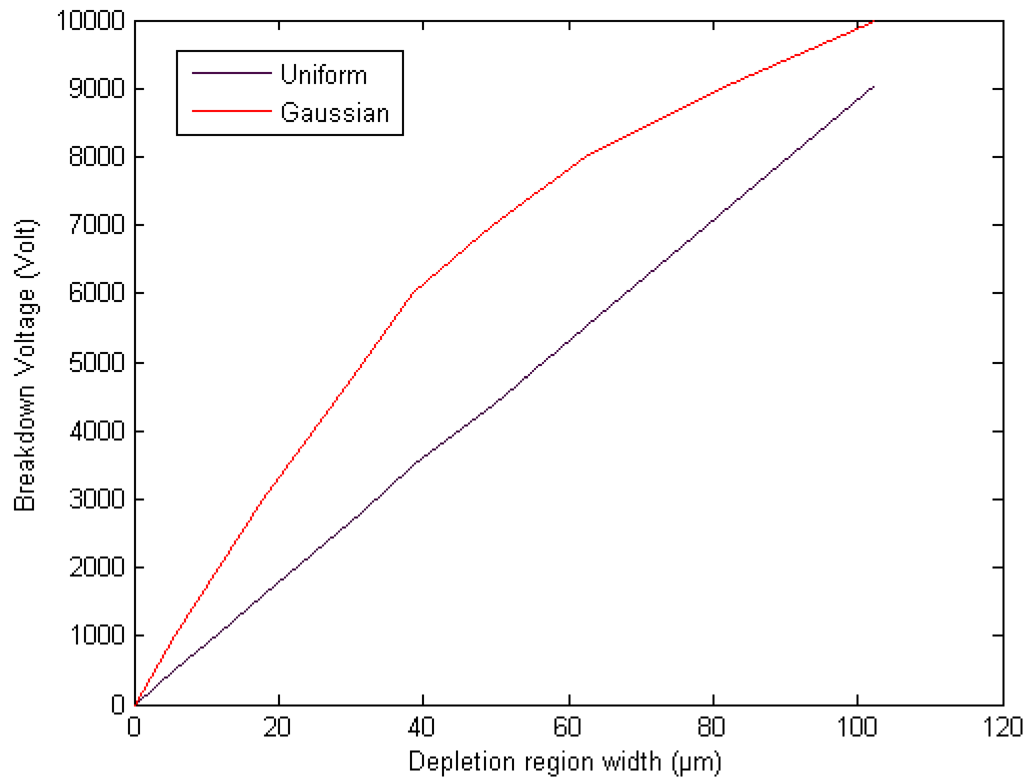
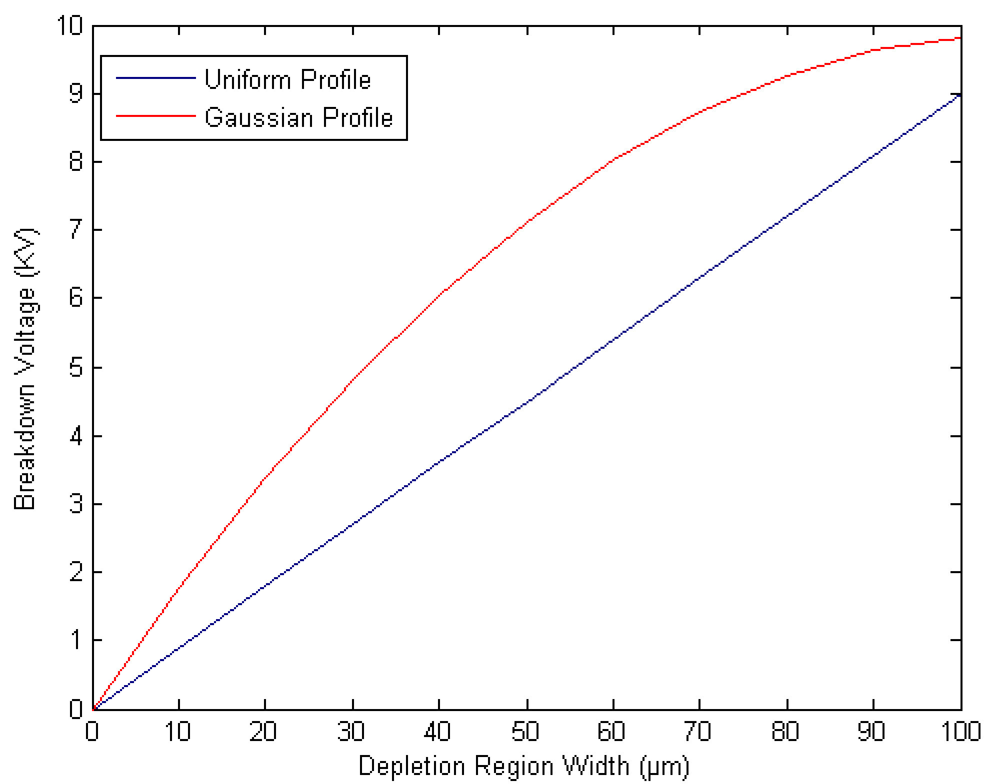


Table 5.6 Variation of Breakdown Voltage for different value of Depletion Region Width with impurity concentration No=10^15

Width (µm)	No=10^15 Uniform V_B (kVolt)	No=10^15 Gaussian V_B (kVolt)
0	0	0
10	0.899	1.77
20	1.799	3.37
30	2.698	4.87
40	3.598	6.049
50	4.497	7.112
60	5.397	8.012
70	6.2965	8.728
80	7.1961	9.268
90	8.0956	9.6304
100	8.99	9.8156

Figure 5.6 Plot of Breakdown Voltage for different value of Depletion Region Width with impurity concentration No=10^15



CHAPTER 6

CONCLUSION

For calculating the value of Breakdown voltage and Depletion Region width in 4H-SiC DIMOSFET, using Gaussian doping profile in drift region, the equation was derived. From this equation it is obvious the Breakdown voltage and Depletion Region width depends upon the device height h of drift region and doping level.

For different value of height h and doping level N_o the Depletion Region width is calculated and related calculation and graph is shown in Table 5.2 and Figure 5.2 respectively.

For different value of Depletion Region width (w), breakdown voltage (Avalanche and Punch through) was calculated and plotted. For value of doping level N_o = 10^15/cc , the punch through breakdown voltage was found to be 10 kV and at the same point the avalanche breakdown voltage was 9.063 kV. Hence, Avalanche breakdown will occur before Punch through.

In conclusion it may be said that a 4H-SiC DIMOSFET with Gaussian doping profile in drift region can give significantly higher value of breakdown voltage at a given values of effective doping level as compared to the same doping level of a uniformly doped drift region of a DIMOSFET.

The calculations for this device have been made with the device height of 102.32µm in order to accommodate a blocking voltage of 10 kV.

It is expected that the 4H-SiC DIMOSFET using Gaussian doping profile may also be designed to provide not only a higher value of breakdown voltage but also to provide a lower power dissipation. This problem is being investigated as a future work for developing SiC DIMOSFETs with lower power dissipation.

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