ALGORITHM AND ARCHITECTURE DESIGN OF DDS SYNTHESIZERS FOR IMPROVED PERFORMANCE OF PLL

A THESIS

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GOVIND SINGH PATEL

SUPERVISOR

Dr. SANJAY SHARMA

(PROFESSOR & HEAD)

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

THAPAR UNIVERSITY, PATIALA-147004 (INDIA)

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CERTIFICATE

I, **Govind Singh Patel,** hereby declare that the thesis entitled, "**Algorithm and Architecture Design of DDS Synthesizers for Improved Performance of PLL,**" submitted to Thapar University, Patiala, in partial fulfilment of the requirement for the award of the Degree of **Doctor of Philosophy** in **Electronics and Communication Engineering,** is a record of original, bonafide, and independent research work done by me during 2009-2015. The research work has been conducted under the supervision and guidance of **Dr. Sanjay Sharma**, Professor and Head, Electronics and Communication Engineering Department, Thapar University. It has not formed the basis for the award of any Degree/Diploma/Associate-ship/Fellowship or other similar title to any candidate of any university.

Govind Singh Patel Date: 27/10/15

This is to certify that above statement made by the candidate is correct to the best of my knowledge.

Dr. Sanjay Sharma 27/10/2015

Professor & Head (Supervisor)

Electronics and Communication Engg. Deptt.

Thapar University, Patiala

ABSTRACT

High speed wireless data communication is playing major role in fast development of modern communication systems. In dealing with this remarkable development, novel technologies and architectures are required to improve the performance of the system and to reduce the cost of equipment. Considering these constraints, hybrid frequency synthesis architectures and techniques have been used to overcome these constraints.

The main objective of this thesis is to provide new and efficient ways to design a phase locked loop (PLL), direct digital synthesis (DDS), and hybrid PLL synthesis techniques. These techniques are generally used in various radio frequency (RF) applications, wireless communication, decoding, modulation, demodulation, etc. In the first proposed technique, the emphasis is on reducing phase noise of PLL for pure signal synthesis. For this a mathematical and modeling approach of the system has been furnished, and then output phase noises in terms of its parameters have been predicted. Based on the performance analysis, a new architecture of PLL for the reduction of phase noise is described and its operation has been verified with advanced design system (ADS) simulation tool. With the help of the proposed architecture, the phase noise has been reduced to 33.33 % at 1 Hz, 7.3 % at 100 Hz and 19 % at 100 kHz. The simulation results demonstrate the better performance as compared to the existing techniques.

In digital signal processing, PLL is not capable to store and convert phase into its corresponding amplitude for the further processing. Hence, there is need to use digital technique for the synthesis in the feedback loop. This work has introduced a new direct digital frequency synthesizer (DDFS) technique using piecewise linear approximation. The proposed technique allows successive read access to memory cells per one clock cycle using time sharing. The output values will be temporarily stored and read at a later time. The output of this system is a reconstructed signal that is a good approximation of the desired waveform.

As a result, the DDFS technique needs only to store fewer coefficients which reduce the hardware complexity significantly. The proposed DDFS technique has been analyzed using MATLAB. The results obtained show improvement of around 1.43 % in spurious free dynamic range (SFDR) over existing results. The results obtained depict the improved performance in comparison with the existing architectures. This technique solved the clock sharing problem, but still it was not suitable for high frequency synthesis. Therefore, new architecture of the DDFS technique has been proposed using Lagrange interpolation and modified quasi linear methods to reduce the area of look up table (LUP) with high resistor transistor logic (RTL) level synthesis. It is used to generate sine waves of different frequencies with the help of a reference input frequency using digital data. Specifically, it has been shown that Lagrange interpolation technique can be employed to yield better class of parabolic functions that can be used to approximate a pure sine wave. This approximation is further corrected by the use of linear interpolation polynomials that suitably reduces the DDFS Lagrange interpolation complexity and helps to get reasonably better results. The proposed design scheme is implemented on XILINX field programmable gate array (FPGA) and suitable hardware analysis has been carried out.

The single architecture of DDS was not suitable for high speed based applications to fulfil the requirement of industries. Therefore, fractional sigma delta modulator (SDM) PLL has been proposed for pure signal synthesis. It has been widely used in wireless communication systems because of the high frequency resolution and the short locking time. Based on the theoretical analysis, the design schemes for optimizing the phase noise performance have been proposed and verified by simulation. Finally, an effective technique has been proposed for noise reduction in fractional PLL by CPPSIM simulator. The output phase noise has been reduced to 6.5 %.

In the aforementioned research work, the PLL, DDS, and fractional PLL have been explored and simulated with the help of various configurations, Lagrange interpolation, piecewise linear approximation, SDM, and time sharing technique using ADS, XILINX, MATLAB, and CPPSIM tools.

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Govind Singh Patel

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ACRONYMS AND ABBREVIATIONS

ADPLL	:	All Digital Phase Locked Loop
AFC	:	Automatic Frequency Control
AM	:	Amplitude Modulation
ANSI	:	American National Standard Institute
AVG	:	Average
BiCMOS	:	Bipolar Complementary Metal Oxide Semiconductor
BW	:	Bandwidth
CCO	:	Current Controlled Oscillator
CLB	:	Configurable Logic Block
CMOS	:	Complementary Metal Oxide Semiconductor
CO	:	Controlled Oscillator
COS	:	Carrier Operating System
CORDIC	:	Coordinate Rotation Digital Computer
CP	:	Charge Pump
DAC	:	Digital/Analog Converter
DAD	:	Digital /Analog Differentiator
DDFS	:	Direct Digital Frequency Synthesizer
DDS	:	Direct Digital Synthesis
DEM	:	Dynamic Element Matching
DIV	:	Divider
DPLL	:	Digital Phase Locked Loop
DSP	:	Digital Signal Processing
DTL	:	Diode Transistor Logic
DLL	:	Delay Locked Loop

FC	:	Frequency Control
FET	:	Field Effect Transistor
FIR	:	Finite Impulse Response
FLL	:	Frequency Locked Loop
FM	:	Frequency Modulation
FPGA	:	Field Programmable Gate Array
FPD	:	Frequency Phase Detector
FSK	:	Frequency Shift Keying
GPU	:	Graphics Processing Unit
GPS	:	Global Positioning System
GSM	:	Global System for Mobile Communication
HDL	:	Hardware Description Language
IC	:	Integrated Circuit
ILT	:	Inverse Laplace Transform
I/P	:	Input
LUT	:	Look Up Table
LVP	:	Laser Voltage Probing
MASH	:	Multi-Stage Noise Shaping
MOSFET:		Metal Oxide Semiconductor Field Effect Transistor
MUX	:	Multiplexer
NCO	:	Numerical Controlled Oscillator
OFDM	:	Orthogonal Frequency Division Multiplexing
O/P	:	Output
OPAMP	:	Operational Amplifier
OS	:	Operating System
PA	:	Phase Accumulator
PAC	:	Phase-Amplitude Convertor

PD	:	Phase Detector
PFD	:	Phase Frequency Detector
PI	:	Perfect Integrator
PLL	:	Phase Locked Loop
PN	:	Phase Noise
PSD	:	Power Spectral Density
PSRR	:	Power Supply Rejection Ratio
QLIP	:	Quasi Linear Interpolation
RLS	:	Recursive Least Squares
RMS	:	Root Mean Square
ROM	:	Read Only Memory
R & S	:	Rohde & Schwarz
RTI	:	Referred to Input
RTO	:	Referred to Output
RTL	:	Resister-Transistor Logic
SAW	:	Surface Acoustic Wave
SCA	:	Subsidiary Communications Authorization
SDM	:	Sigma Delta Modulator
SFDR	:	Spurious Free Dynamic Range
SNR	:	Signal to Noise Ratio
SOM	:	Self Organizing Map
TDC	:	Time to Digital Converter
TF	:	Transfer Function
TRF	:	Tuned Radio Frequency
TTL	:	Transistor-Transistor Logic
UIRMS	:	Unit Interval Root Mean Squared
UMTS	:	Universal Mobile Telecommunication Services

VCO	:	Voltage Controlled Oscillator
VCV	:	VCO Correction Voltage
VCXO	:	Voltage Controlled Crystal Oscillator
VHDL	:	Very High Speed Integrated Circuit Hardware Description Language
VLSI	:	Very Large Scale Integrated
WLAN	:	Wireless Local Area Network
XCO	:	Crystal Controlled Oscillator

CHAPTER 1

INTRODUCTION BASED ON LITRETURE REVIEW

1.1 INTRODUCTION

Wireless high speed data communication is experiencing drastic changes in terms of technologies and architectures as the emphasis of designers is to improve the performance of the modern communication system. In dealing with this remarkable development, significant efforts have been made to limit both capital expenditure and operating expenditure of the communication systems.

In the present era, almost all signal processing problems are resolved in digital domain because of the availability of well-known very large scale integrated (VLSI) circuits. These circuits permit us to carry out complex processes in the real time, without knowing restraints of the analog implementations. The operations like signal filtering, locking time, phase /frequency resolution, mixing etc. are carried out in the digital domain, and its analog equivalence conversion can be done. A very significant and fundamental operation in signal processing is frequency synthesis. This research work deals with various frequencies synthesis techniques such as direct digital synthesis (DDS), phase locked loop (PLL), and hybrid PLL. These techniques find applications in radio frequency (RF), wireless communication, decoding, modulation, demodulation etc. These techniques have various parameters like phase, frequency, amplitude, noise, spur, power etc. These parameters are analyzed by various techniques of frequency synthesis.

Frequency synthesizer is a piece of equipment which produces frequencies from a particular source. The output of the frequency synthesis shows stability and accuracy for long time. In analyzing signal, one can determine one or more output from one or many sources.

There are three frequency synthesis techniques that are being currently used throughout the industry to generate sine wave for further analysis. First one is PLL which is widely used in various communication systems including clock signal recovery, modulation, demodulation etc. It is also used in control system as a feedback mechanism to lock the output to input. It gained popularity because of its economic function, simplicity, low power, and high spectral purity.

The other technique is DDS, which comes under the digital signal processing (DSP) discipline, is commonly used to create, modulate, and generate digital signal and sometimes it is used to convert digital signal to analog signal. It also finds applications in industry due to its small size, reliability, low power, fast switching speed, and good frequency resolution. The main advantage of DDS lies in combining it with DSP processor which can control various parameters such as phase and amplitude. It has applications in military radar and other systems. Its other parameters like phase resolution, frequency hopping, and frequency resolution are analyzed to improve performance of communication system.

The last technique is fractional or hybrid PLL which overcomes the limitation of PLL and DDS. It operates as a DDS inside PLL and some time as a feedback input device.

1.2 MOTIVATION OF THESIS

Communication is area of innovation and research, in which high speed is the major constraint to communicate data from one place to another via wired or wireless media. To fulfil demand of high speed internet and cellular phones, wide bandwidth is required. The new techniques and protocols have been proposed to increase bandwidth and to communicate data over media at higher frequencies with high signal accuracy. Considering above requirements, various new techniques and their parameters have been analyzed to fulfil recent industrial demand. The incredible amount of research about PLLs

in the past decade reflects its importance to high-speed communication as well as the large number of challenges that still exist in PLL design and implementation [1].

In this thesis, the primary aim is to design and implement efficient structures for the hybrid PLL. To accomplish this goal, the cost efficiency and optimal performance designing for PLL and DDS are of main concern. Therefore, an exhaustive literature review has been carried out related to the titled work. Abstracts of some of the most relevant researches are reported in the following paragraphs:

In the era of early 1930's, the super heterodyne receiver was generally used in most of the field of radio communication engineering. Edwin Howard Armstrong was one of the contributors in the same field. His contributions are in the field of regenerative feedback circuits, super heterodyne radio receiver, and frequency modulation radio broadcasting system. The tuned radio frequency (TRF) receiver was also invented by Armstrong in 1918. Afterward, regenerative feedback was incorporated into a broad engineering science developed by H. Black, H. Nyquist, H. Bode and others in the period between 1914 and 1945. In advancement of feedback system, PLL technology came in market, which has communicated significantly towards the technology advancement in the communication system in the past 40 years. This technology has become important system component due to its novel integration circuit technology.

Hsich and Hung [2] presented review on basics of various PLLs with their configuration which is useful in communication based applications. In the continuation of the basic detail of PLL, the different types of PLL have been reviewed by Prasad and Sharma in [3]. The problem associated with the different PLL architectures like analog, digital, linear, and all digital have been implemented in Simulink. The author also reviewed PLL techniques, which is applicable to latest day to day application for the communication system. Therefore, Lata and Kumar in [4] presented great contribution in digital

communication. This work provides basic principles and details of each component of digital PLL in control system and digital communication system. The simulation results show the comparative analysis of each component. After reviewing history and basic detail of PLL, other parameters have been analyzed in the next section.

1.2.1 Estimation of phase noise and their reduction techniques of PLL & ADPLL

Smedt and Gielent [5] proposed evaluation of phase noise spectrum. The behaviour modeling has been used for voltage controlled oscillator (VCO) to find highly accurate loop analysis. The authors performed the corroboration between output of spectrum of VCO model and output of transistor level VCO spectrum, in which voltage has been taken as an input. The results were simulated and compared with existing techniques.

Considering the previous work, self injection of VCO has been presented by Chang [6] to minimize noise. This technique was also based on feedback loop analysis. In this case, an elevated Q factor resonator and a time hold-up have been used to illustrate results. The output noise may be diminished at offset frequency in vicinity area of carrier. It also returns to VCO noise when input is zero and far away from carrier with stable loop condition. This technique may be used to reduce the phase noises. Besides phase consideration, frequency locked loop (FLL) is also proposed by Juan et al. [7] to reduce phase noise of wideband VCO. The author derived design equations to reduce noise and find stability of the system. The results showed better performance as compared with the previous techniques. Another wide band voltage locked feedback loop was designed in bipolar complementary metal oxide semiconductor (BiCMOS) [8] and which achieve up to 20 dB reduction of VCO phase noise.

Takagi proposed a new method to reduce phase noise of PLL based on subtraction of correlated noise [9] from its average current noise. The theoretical and experimental results have been compared. This work obtained 7 dB reductions in phase noise

approximately. Another technique which is also used to reduce VCO phase noise is called frequency steered technique. This work presented digital VLSI integrated circuit (IC) technology. The implementation of VCO and analysis of its phase noise characteristics have been done using this technique. The parameters of system were identified and the performance of system has been characterized. The result showed that system can lock easily to confine in particular region of frequency to reduce VCO noise. This technique also allows improvement of poor quality of VCOs for the industrial applications.

Wicpalek et al. [10] presented a frequency discriminator in ADPLLs for radio frequency synthesis to fulfil requirement of industrial applications like global system for mobile-communication (GSM) and universal-mobile-telecommunication system (UMTS). One of the requirements is in-band phase noise performance, which was analyzed theoretically and practically respectively. The results showed improvement in the performance of the PLL. This work was implemented using two bit frequency discriminator in complementary metal oxide semiconductor (CMOS) technology. This discriminator was also used in profitable CMOS Bluetooth radio based applications. The measured phase noise was -86 dBc/Hz for GSM application. The mathematical and operational details of the same have been presented.

Considering other requirements, the minimum acquisition time and maximum noise rejection in the presence or absence of frequency drift has been analyzed by Sandoz and Steenaart [11]. This work proposed a new aided acquisition technique to improve the performance of ADPLL. The numerical values of pseudo-two dimensional random-walk filter and phase error variance were analyzed. These results show comparison between theoretical and experimental analysis, which were very satisfactory. Drift frequency was tracked for feedback modified loop to improve the ability of system. This technique also reduced signal to noise ratio as compared to the other. The phase noise of digital

frequency dividers were investigated by Kroupa in [12] and found good as compared to the previous work [11].

Mishra et al. [13] proposed behaviour and mathematical modeling of PLL at -450 MHz, which is used in various communication applications like frequency synthesizers, computer, radio, clock generator, recovery, global positioning system (GPS), demodulation, etc. This work presents analysis of third order PLL with their industrial applications. The key parameters such as timing jitter, lock time, locking range, and bandwidth are tested and calculated by MATLAB Simulink tool. Timing jitter is the important parameter, which can mortify the response of the PLL. The method was presented for minimization of timing jitter of PLL, in which, two PLLs were connected in cascade form [14], where first one has been used as a voltage controlled crystal oscillator PLL and other used as a wide band PLL to reduce jitter. The simulation results presented better performance as compared with the existing methods.

Signal-to-noise ratio (SNR) and unit interval root mean squared (UIRMS) have been presented in [15] to focus on output jitter of various synchronizers. This work was divided into two groups, the first was filter with carrier PLL and the second was based on symbol PLL. The prototype of each group was analyzed to reduce output jitter of the proposed system. Considering clock recovery, Kim and Kim [16] proposed dual digital PLL (DPLL), which is used in digital transmission to process frequency and phase as input parameters and results showed reduction in substantial jitter and adjust DPLL loop bandwidth accordingly. The work presented adaptive algorithm, which adjusts bandwidth to allow fast acquisition and jitter reduction at various noise environment. This algorithm was based on recursive least square criterion to control parameter of dual loop DPLL. This work achieves fastest acquisition time to minimize jitter at any given time instant.

This short preamble duration is useful in various applications like wireless communication, networks, storage devices etc.

Liao et al. proposed a mitigation technique [17] with laser voltage probing to minimize jitter. This technique presents PLL IC, which has probing circuitry to allow detecting small amount of excess jitter that was masked due to large jitter to detect at output of system. The details of probing setup jitter analysis jitter mitigation methodology and timing measurement were presented in this work. Instead of direct estimation of jitter, an indirect on chip method has been presented in [18] to estimate PLL charge pump (CP) jitter. The spectral purity of the system is an important parameter to measure directly within a production test environment. These sets of work focus a new framework to implement methodology that can detect block level errors and minimize spectral degradation. This provides a platform where jitter is tested on fully embedded CP-PLL. In addition to above frame work, another substrate noise also affected the performance of charge pump. This work was estimated and simulated in 0.15 μm technology. The results showed a reduction of 12.5 dB in the system output spur level at an offset of 5 MHz. The results suggested that mixed signal with other isolation technique are used to reduce noise on radio frequency circuits.

Gao et al. [19] proposed spur reduction technique for the PLL. This technique was based on sampling phase detector, in which clock input was fed to sample signal for VCO. At this reference input, the periodic disturbances of the other sources of VCO were sampled. Dummy sampler and isolation buffer were described to minimize sampling spur of oscillator. The buffer and delay of system were presented to tune frequency to reduce spur level. This design demonstrates effectiveness of spur level, in CMOS technology and its reference spur was around less than -80 dBc, which is used in low bandwidth. Considering above periodic disturbance in oscillator, a new method [20] presented by

Stensby to limit sweep rate of VCO, which is used for serving industrial applications like receivers, transponders, decoders etc. To limit effect of noise, band width of feedback loop should be kept small and make their phenomenon too reliable. The loop frequency error is decreased with sweep voltage. The results analyzed and compared with existing techniques.

Jinghui [21] presented analysis of 5-8 GHz PLL using discrete Z domain. The transfer functions of various order of the PLL in Z domain were presented. Predicted values of jitter were compared with its existing architectures. Considering previous jitter reduction architecture, a new programmable PLL architecture is proposed by Sulaiman et al. in [22], which is implemented on field programmable gate array (FPGA) platform. As programmable architecture designers are free to change their design at implementation level also, so the performance can be improved in various forms such as low output jitter, lower power, and clock control. Finally, architecture presented low power high performance system. Moreover, stability is another constraint to check performance of the system. Paemel [23] described a model to check stability of second order charge pump PLL. There are two conditions to find the stability, first loop is lock and second is loop out of lock. This work presented transient behaviour with its well defined state variables for that particular model. This work determined stability and overloads limits and verified their validity for various applications. Another technique also presented by Tillman and Stensby [24] using various tracking phenomenon, but in this phenomenon, input was taken as a sum of two sinusoidal signals. However, the previous analysis was incomplete and further analysis of the PLL response to the sum of sinusoidal signals was presented. The amplitude ratio and frequency response were defined to track stability of the system.

Gokc et al. proposed an adaptive estimator [25] which is embedded into a conventional PLL. An adaptive frequency estimator was used to predict its performance with the help

of Linear and nonlinear model. These models provide guidelines to designer for increasing efficiency of the system. The results showed improved performance for the same. Another adaptation method presented by Roche et al. in [26], which is used to minimize error and maintain stability using locking phenomenon and loop bandwidth of the system. The charge pump current is controlled by adaptive technique to enhance loop bandwidth. After analysis, the phase error, loop bandwidth, and locking status were achieved. This work was simulated and implemented in CMOS technology. Unwanted signal was the main constraint, which was introduced in feedback loop, described by Saito et al. [27]. This work was presented to alleviate concerned clock pulse, which was generated due to unwanted signal. This clock pulse controls whole process without timing skew. The large incident noise was also realized by adding filters. The validity of stable system was determined using simulation results.

Moreover, analog analysis, digital frequency steering method [28] has been implemented by Hill and Cantoni to stabilize the system. In this method, frequency of closed loop has been compared with reference input and applied to VCO to control stability. The output recognized disturbances of digital frequency steering loop. These disturbances and errors have been rectified using this method. This work was implemented for high speed clock information recovery and compared with existing techniques.

Hanumolu et al. [29] proposed an impulse invariant transformation method, which is used to determine state variables and state equations for analysis of tracking behaviour. This method described lock acquisition process and linear behaviour of large and small signal respectively. The noise transformation and state equations were derived to realize linearization method for signal conditions. An impulse invariant transformation method was analyzed and compared with existing methods. Also, feedback loop parameters like frequency and phase, with their effects on phase margin and stability have been derived

and analyzed. The results were verified by simulation tool MATLAB. Moreover stability, transient characteristics like locking time, output jitter, capture, and locking ranges are presented by Chan et al. [30]. This work used bang-bang type PLL, which described behaviour model. Result showed how the application of this model in a simulator can speed up simulation time by four to five orders of magnitude. The simulation results were analyzed and compared with conventional methods.

Considering previous work, Stork [31] proposed a novel architecture in the form of digital components that can be used to enhance performance of the PLL. This design consists of up-down counter, shift registers, and frequency generators, which are an appropriate design to find stability and used it for other applications like frequency synthesizer, clock recovery etc. But this architecture is limited to low frequency base applications, so these limitations can be overcome using fractional frequency synthesizer. The detailed analysis of PLL and fractional PLL are described and compared to stabilize the system.

Kumm et al. [32] also proposed a new algorithm for digital PLL and its implementation on FGPA to enhance the performance. All digital components have been realized with their functions and parameters have been derived for analysis. Besides digital system, the coordinate rotational digital computer (CORDIC) algorithm and Hilbert transforms are used to unwrap phase component for extending range. This work maintains locking time for frequency changes and also analyzed frequency and stability range with their processing delay. All transfer functions and details of each components of system were derived. Finally, Zhang et al. [33] presented research and application of ADPLL for the communication system. This work also provides time domain analysis of each digital components of ADPLL. Mathematical models of the first and the second order systems have been presented using linear approximation method. These results were simulated by XILINK and implemented on FGPA platform. This architecture can also be used in an

inductive heating system, control system, and other communication system. In this section, it has been found that these techniques are not suitable to overcome phase noise of the PLL at higher order. Therefore, it is essential to comprehend and quantify jitter so that their outcomes on upper stage artefact are reduced. The effects of these noises should be minimized using various PLL configurations and also with the effect of poles and zeros of the filters with the same.

1.2.2 Efficient Implementation of Piecewise and Lagrange Interpolation Methods of Direct Digital Synthesis

Direct digital synthesis (DDS) is another type of frequency synthesizer, which is used in low power, fast switching speed, and good frequency resolution based applications. Larson [34] described and compared theoretical and practical analysis of various parameters. The limitations of traditional analogy PLL are overcome by proposed architecture. The results show that this architecture is useful for high speed communication. Considering previous work, Caro and Strollo [35] proposed a new technique that used piecewise polynomial approximation. This method analyzed error, SNR, and spur free dynamic range (SFDR). The polynomial reduced effort to maximize the SFDR with the help of coefficients. The quadratic and piecewise linear methods have been realized to design the proposed system. Conventional and proposed techniques have been discussed and compared. The results showed reduced area and less complexity of the system. The performance can also be improved after combining width arithmetic and single summation tree architectures. The results obtained show that piecewise quadratic design is more effective than piecewise linear design to measure SFDR. Generally third order system is used to design good DDFS in terms of SFDR. Another piecewise continuous linear interpolation method is proposed by Langlois and Khalili in [36]. In this method, sine function is approximated with desired linear segments to fulfil the

requirements of memory storage and computational complexity. The number of linear segments and resolution of slope are correlated with each other to achieve desired output. The memory storage requirements of proposed DDFS were identified and implemented. Considering the previous work, read only memory (ROM) less quadrature DDFS was presented in [37]. Because of ROM look up table (LUT), it was very difficult to store huge amount of data in conventional system. To avoid this problem, low power ROM-less technique was used to design suitable system for portable wireless communication applications. Mortezapour and Lee also proposed [38] a new ROM less DDFS using digital to analog converter (DAC). Here, ROM LUT was replaced with nonlinear DAC for conversion of phase to sine amplitude. Two quadrature DDFS were used to implement the proposed system. This work was demonstrated and implemented by nonlinear resister strings DAC and current mode DAC both. The results found that there are around 4 mW and 92 mW power dissipation for non linear resister string DAC and current mode DAC respectively. Instead of two DACs, this work described [39] low power DDFS with an on chip DAC. This technique included accumulator, two phases to sine converters and DAC. This parallelism method increases conversion process for high speed operation of the system. Inter-chip interconnection helped to save delay and power consumption in the on chip DACs. This technique was implemented in CMOS technology. Considering the previous work [35], Ashrafi and Adhami [40] proposed a new model of DDFS. In this work, the first quadrant of a sine signal has been interpolated using even and linear piece-wise parabolic polynomial. These techniques found to be helpful to maximize SFDR and solve the problem of complexity of the system. The proposed design is called as quasi linear because the first quadrant of signal is approximated by even parabolic polynomial method. The results showed an improvement in SFDR with respect to existing techniques. Another work presented a smaller LUT for sine function. This function is interpolated

with the help of their coefficient by using piecewise parabolic interpolation method [41]. The results found that ROM size is reduced around 1 K bits at the 80 dBc of SFDR.

Considering the work [37], Saber et al. [42] proposed a new architecture of DDFS based on quadrature piecewise interpolation. This work was employed without ROM as already discussed in [37], but this was implemented on FPGA to avoid high power consumption of the system. This work consumed around 4 mW and SFDR was better than previous work. Considering the previous work, another ROM compression technique of DDFS has been proposed in [43]. The work presented multiple segments piecewise polynomial technique to store values of sine function for the LUT. The phase is mapped with amplitude for the required output bits of the ROM. The results found reduced ROM size and good spectral purity of the signal. The compression ratio was good as compared to other technique. Considering work [37], Khan et al. [44] also proposed ROM less quadrature architecture. This technique reduced the complexity of the system. This ROM less technology was more efficient that existing work [37]. The results showed an improvement in term of area. Another ROM less architecture of DDFS has been proposed by Hegazi et al. [45], which is based on sampling ratio. This technique reduced settling time for the DAC. The results were simulated and compared with existing architectures.

Considering previous work, Vankka [46] presented a new architecture, which was based on mapping of phase to sine amplitude. This mapping increased the resolution of LUT. Bramble [47] also presented a novel technique which is used to convert wave shape of phase accumulator into desired accumulative address of ROM LUT. The limitations of previous work have been eliminated. Various memory compression techniques have been compared.

Nieznanski [48] proposed an alternative approach for the DDS which is the extension of previous work [37]. This approach eliminated pulse position jitter, which also originated

from the accumulator. Besides this low jitter, low power ROM less system has been analyzed by Fahim [49]. Analog interpolation method and circuit topologies were used by Fahim to reduce jitter of the system. This work has been implemented in CMOS technology. Considering low jitter in previous work, the work [50] - [53] also presented low jitter clock of DDFS. This work analyzed phase error that incorporate with time to reduce jitter at the output. Better results have been found in terms of jitter and compared with other existing technologies. In this section, it is found that access to memory cells at specific time is the main cause, so there is need to introduce new technique to access more memory space in less time and minimize noise at high speed for the communication system.

1.2.3 Noise reduction of Hybrid PLL using Sigma Delta Modulator

Fractional PLL is the hybrid frequency synthesizer. It is similar to the divide-by-N PLL. Marques et al. [54] presented an overview of the evolution of fractional PLL. Analog PLL, digital PLL and DDS are having some limitations which are overcome using fractional PLL. The parametric analysis of the fractional PLL has been described by Stork and Kaspar in [55]. In this work, output of the VCO is not restricted to only multiple reference input but also its locking mechanism which is used for the fractional multiples frequency tuning. This frequency has been controlled by predicted value of band width of PLL, at the same pass band. The high frequency and less settling time synthesizers have been analyzed to fulfil the requirements of modern applications. Considering previous work, the various parameters like phase noise, band width, locking time etc. have been analyzed by Riley et al. [56] and Zarkeshvari et al. [57]. This work also described linearity of components and band phase noise of the same. These techniques are useful for recent trend industrial applications. This work also reviewed various techniques of the system with their advantages and disadvantages.

Perrott [58] proposed a modeling approach based on sigma delta modulator (SDM) fractional PLL. This model has been incorporated with fractional divide value for various components. This work analyzed noise and dynamic characteristics of SDM which is implemented in CMOS technology. Another linearization method for a wide band sigma delta fractional PLL has been presented [59]. This work used two techniques; the first one is modulation for noise reduction and the second is charge pump linearization. These techniques have been presented and demonstrated to detect component error and enable them for wide band fractional system based applications. The results obtained were better than previous works.

A linearized charge pump technique to reduce error in the system was proposed by Su & Pamarti [60]. This technique has been divided into two parts; first, suppressed spurious tone and the second reduced phase noise, which occurs due to mismatching of the charge pump process. The theoretical and practical results have been calculated and compared. Zhang et al. proposed finite modulo [61] high order SDM fractional system. This method generates less spur which is achieved by compensating voltage and current in various domain. This work is implemented in CMOS technology and its results are good as compared to previous architectures. Considering previous work, Arora et al. [62] proposed mathematical model of fractional PLL, which determines spur and phase error at the output. This work calculated sources of noise of each component and presented its effects on the output of system. The results showed the comparison of various existing techniques.

A linearized model of the fractional system has also been presented by Venerus & Galton [63] and Jin et al. [64], which is based on sigma delta frequency to digital converter. These techniques determined linearity requirement of system and also resulted in reduction of area. This method also reduced quantization noise of sigma delta modulator

in the feedback loop. It is very difficult to choose correct type fractional SDM PLL to get less noise, high speed, and good frequency resolution. This work has reviewed several systems with its parameters by Kit et al. [65] for the communication system. The results were simulated using CPPSIM simulator. The design parameters such as phase noise, frequency resolution, and settling time have been presented and compared. These parameters already have been analyzed in previous works, but Riley et al. [66] also proposed a new multi-stage noise shaping (MASH) modulation concept, in which low phase noise and fast settling time with their effect on the system, have been presented. Besides [64], Park et al. [67] proposed a novel architecture, which achieves low noise and suppress quantum noise of the sigma delta modulator. This work consumes less power around 32 mW using charge recycling technique, which has been implemented in CMOS technology. Another dual reference frequency technique has been described by Feng [68] to reduce phase noise and spur. This work resulted in better frequency resolution and short locking time, which is useful in wireless communication systems.

Considering references [61] & [64], novel fractional-N PLL architecture has been proposed by Jian et al. [69], which is used for multi band communication using binary weighted differential and offset frequency modulator. Quantization noise and spur are minimized using these techniques. Firstly, binary weighted method has been utilized for mismatched shaping to minimize quantization noise. Secondly, offset frequency modulator has been utilized to reduce in-band spur. Yang et al. developed phase compensation technique [70], which can reduce fractional spur of the system. It's operational frequency ranges from 1.5 GHz to 2.7 GHz and found better divide ratio. This work adopted on-chip phase compensation using delay locked loop which is simulated and implemented in CMOS technology with its power dissipation is around 6.9 mW.

Moreover, Richard and Ramaswamy [71] proposed multi-stage noise shaping and single loop modulator which are used for wireless application to reduce spur. These techniques analyzed various parameters to minimize the spur. The parameters have been analyzed and compared with existing techniques. After considering various limitations which were not rectified by analog architecture, all digital fractional PLL has been proposed in [72]. This architecture is an enhanced architecture of the fractional PLL. The main component of this design is dual modulus divider controlled by modulator output which is used to minimize spur level of the system. The results were studied and comparisons were done among various existing techniques. Considering other limitations, which were not overcome by single architecture of PLL or DDS? Then, new hybrid concept came in the market to fulfil such type of requirements. Hu et al. [73] designed a new PLL-DDS-PLL based hybrid architecture for various types of applications. This work described low spurious, which was around 65 dBc. The comparative results were better than previous existing techniques.

The bandwidth is important parameter to improve the performance of fractional PLL. Pu et al. [74] described loop bandwidth of the system to manage jitter and spurious performance. A circuit component is added along signal path which improves bandwidth. The results have been discussed and compared with the conventional architecture. Another work has been proposed by Meninger and Perrott [75], extending bandwidth of the fractional PLL. The issues of bandwidth in term of quantization noise of design have been explained. This model is reframed to analyze system noise to achieve high bandwidth. The methodology has been demonstrated and compared. A new fractional hybrid PLL has applications [76], [77] in both narrower and wider bandwidth which operate in two modes, firstly using integer phase lock and secondly using fractional PLL transient. Fractional PLL achieves fast locking as compared to integer PLL, this fast

locking is benefited in various important applications. This work is implemented in CMOS technology.

Ferriss and Flynn [78] proposed all digital phase detectors, which includes filip-flop. These flip-flops have been used to reduce phase quantization noise using oversampling method. This digital scheme increases modulation rates much larger than loop bandwidth, which determines accuracy of output signal.

Considering previous work, another digital automatic calibration circuit has been embedded in [79], [80]. This work extended oversampling concept which was presented in [77]. This work presented sigma delta modulator for non sinusoidal waveforms. The clock generation and dynamic adjustment of their free running frequency are determined to lock PLL in suitable lock range to find stability of the system. The results are simulated and demonstrated. In previous work, it was described that how to find stability by locking concept. In this work, a novel digital building circuit has been presented by Stork [81] to determine stability of the system. This design includes registers, frequency generators, and other components. This work determines stability and generates pure signals. This architecture is much simpler and suitable to design VLSI based applications. Its advantages, disadvantages and future scope have been presented. Besides VLSI technology, signal processing based applications have been presented by Song and Ignjatovic in [82]. This design includes new threshold DDS based delta modulator. The loop decomposition of sigma delta is configured to increase throughput of modulator. The results found low power fractional-N PLL. Rhee et al. [83] also described aspect of finite impulse response (FIR) with fractional-N PLL. This method describes spur generation and nonlinearity issues of the PLL. This fractional PLL is used in embedded systems.

Fractional synthesizers can be simulated and implemented in various platforms. One of the languages is hardware description language (HDL), which can be used for both

simulation and synthesis. The behaviour modeling on HDLs have been proposed with their applications in [84], [85]. This work described source noise of different components and showed that it affects at output of the PLL. The various specifications of configuration of the system have been described and compared. The results are obtained and compared by VHDL simulation tool and implemented by XILINX tool.

Hybrid architecture of the PLL is very useful to overcome limitations of single PLL and DDS architecture. Considering these limitations, Linn [86] developed hybrid PLL for the communication system. This work presented methodological approach to design and implement hybrid PLL. The various configurations and types of PLL have been presented. Another new DDS-based-PLL has been proposed by Bonfanti et al. [87] to achieve better frequency resolution, fast settling time, and spectral purity. The DDS is used as feedback components with VCO. Output of VCO and DDS are mixed to complete closed path. The complete output of VCO is used to determine spectral purity of the system. This work is implemented and compared with various existing techniques. The different parameters with their configurations have been analyzed. This work finds application in various fields like wireless local area network (WLAN) [88], orthogonal frequency division multiplexing (OFDM) receiver [89], and distributed generator [90]. On the basis of previous literature, it is found that clock plays important role to process information in the communication system. It determines hard and soft variation of input and output of VCO. The small random variation of input voltage of VCO is one of important factors that cause output phase noise. It is necessary to employ a mechanism for smoothing the variations. For smoothing the variation of input voltage of VCO, there is a need to use new technique, which can limit and reduce phase noise of the system. For that a fractional - SDM - PLL can be designed to reduce noise for the better performance of the communication system.

1.3 PROBLEM FORMULATION

The modern communication system is experiencing a rapid expansion. To meet the tough real time requirements posed by modern wireless communication systems, high performance, and low cost signal processing architectures must be developed. The new algorithms and techniques are required to improve system performance while reducing the cost of equipment. One of the important devices of the modern communication system is PLL. The purpose of the PLLs is to increase signal processing speed at low noise. These systems are helpful for the signal analysis, de-noising, compression, and so forth. To consider the increasing cost pressures on many wireless equipment makers, significant efforts are being made to reduce complexity, low noise, high processing speed, flexibility etc. The high speed wireless communication system can be efficiently realized with the help of hybrid PLL. However, the disadvantage of a PLL is that, this technique is not suitable to overcome phase noise of the PLL at higher order. So, there is a need to introduce the techniques which can improve the performance of PLL at the high speed. Another difficulty arises in the DDS to access the memory cells using clock pulse. So, there is need to develop new technique that will allow accessing memory twice at one clock cycle using time sharing at the high speed for the communication systems.

However, the PLL and DDS are unsuitable for those practical applications, where fractional divider value is required at high speed. As an interesting remedy for the problem, the sigma delta modulators are extensively used in practice for attaining the fractional value. The single architecture of PLL and DDS are efficient for communication of low order frequency. For the high order communication, the hybrid PLLs are preferred because single architecture does not offer effective response. However, the hybrid design increases the complexity of the system. For such scenarios, there is need to develop a technique for the efficient realization of the hybrid PLL. Moreover, better design and

implementation of hybrid PLLs can result in low cost and low noise communication system with improved performance.

1.4 RESEACH OBJECTIVES

In the light of aforementioned aspects, the research objectives for the investigation are as follows:

1. To study the existing PLL and DDS techniques.
2. To propose novel algorithm in which PLL & DDS technologies can be conjoined by design of synthesizers to achieve improved performance of PLLs.
3. To implement and validate the proposed system on FPGA platform.

1.5 THESIS OUTLINE

The thesis has been organized in five chapters. The details of the contents of each chapter of the thesis are as follows

- Chapter one presents the introduction and motivation based on the literature survey, problem formulation, objectives of the thesis, and organization of thesis.
- Chapter two describes the parametric analysis to minimize noise of frequency synthesizers for wireless communication systems. The noise contributions of frequency synthesis are described based on presented analysis. The results have been simulated with the help of Agilent's Advanced Design System.
- Chapter three describes DDFS based on piecewise linear approximation, Lagrange interpolation, and modified quasi linear methods. The proposed techniques allow successive read access to memory cells per one clock cycle using time sharing. The desired waveforms have been approximated to get reconstructed signal at the output. As a result, the DDFS technique needs only to store fewer coefficients and the hardware complexity is significantly reduced with its spectral purity. The results have been simulated with the help of MATLAB & impulse C.

- Chapter four deals with the parametric analysis of a novel architecture of fractional PLL for communication system. This work proposed a mathematical model to take care of noise of the components and to calculate predicted noise. Finally, the effect of these noises for the fractional synthesizer has been simulated using CPPSIM.
- Finally, the chapter five sums up the research work. Further, a brief description about the future work/scope has been presented as a motivational seed for the germination of research work. The thesis concludes with the research publications as well as the list of references found useful during the course of investigation.

1.6 SUMMERY OF THE CHAPTER

This chapter acts as a capsule for the motivation of the thesis. An exhaustive literature survey has been presented about phase noise, jitter, area, high speed etc. of PLL, DDS, and hybrid PLL. Based on this, the objectives of the thesis have been identified, in which the main motive is to increase efficiency and to reduce noise, area and complexity of the PLL. In the next chapter, the effects of phase noise of PLL for wireless communication system have been presented.

CHAPTER 2

PHASE NOISE REDUCTION TECHNIQUE OF PLL FOR COMMUNICATION SYSTEM

2.1 INTRODUCTION

This chapter focuses on the analysis and design techniques for low phase noise of Phase Locked Loop (PLL). In this work, phase noise generation mechanism is analyzed and analytical relationship between its phase noise performance and circuit design parameters has been derived. Based on theoretical analysis, the design schemes for optimizing phase noise performance have been proposed and verified by simulation.

A PLL is an electronic feedback loop device which compares phase/frequency variation among reference input & feedback loop signal. This is widely used in radio, communication, computer, control system, and other electronic systems. It has various parameters like band width (BW), area, phase noise, locking time, stability, etc. which are used to improve performance of the same. Out of these parameters, phase noise is of utmost importance as its presence degrades performance of the system. The unwanted entities such as oscillators and signal generators are present in wireless communication instruments. The phase noise is introduced due to phase fluctuations by a random frequency signal. It also results in loss of information, which is received by the receivers at the time of high speed communication. The problem that synthesizer designers are facing is due to occurrence of phase noise. It means, it is important to understand phase noise and then analyze various techniques to minimize its effects on higher level products. Literature review of some of the most relevant researches has been reported in the following paragraphs:

To study noise and its impact on performance of PLL has been reviewed in [91], [92]. In traditional PLL, two and tri-state type charge pumps were used. But it has some limitations. One limitation is that it could be used only for low frequency synthesis in discrete-time system mode. But after some time compact integrated circuit (IC) design came in the market with filter. This combined architecture exploits characteristics of phase noise, which is measured at the output of VCO in locking mode. The few noises were reduced by techniques provided by Emre et al. [93]. The spectral density of output signal can be affected by various noise sources like reference, filter, charge pump, VCO, and divider.

Another new tunable VCO PLL architecture has been proposed by Woogeun, which describes linearization technique [94]. This technique is used to linearize band width for common clock serial link based applications. A single input dual path type oscillator tune sinusoidal input and finds constant gain for phase detector. The results obtained show that PLL band width and phase noise variations are well regulated and controlled. Considering previous work, another linearization method has been proposed, which decreases phase noise of system. Instead of phase, frequency locked loop has been implemented on-chip with their applications in the communication system. Out of various components, phase noise of phase detector has been investigated by using linearization technique.

Limitation of Shannon capacity and its remedial has been presented by Eitan et al. [95]. A new linear approximation method has been described to analyze signal-to-interference-plus-noise ratio to improve the quality and security of the communication system. This work uses codec that can adapt transmission rate in linear manner for wide range and long distance with constant throughput. The validity of work has been checked. The results have been calculated and compared with existing work [96], [97]. In this section, it has been found that these techniques are not suitable to overcome phase noise of PLL at

higher order. Therefore, it is essential to identify and compute phase noise. The effects of these noises should be minimized using various PLL configurations and also with the effect of poles and zeros of the filters with the same. The analysis of basic components of PLL has been presented in next section.

2.2 ARCHITECTURE OF PHASE LOCKED LOOP

This section describes mathematical analysis of each component of PLL. This architecture is also being used as frequency synthesizer to analyze the various parameters like phase, frequency, amplitude, bandwidth, and stability. It consists of phase/frequency detector (PFD), VCO, filter, and divider. The architecture of PLL is shown in figure 2.1. The various components of the same are described in the next sub-sections.

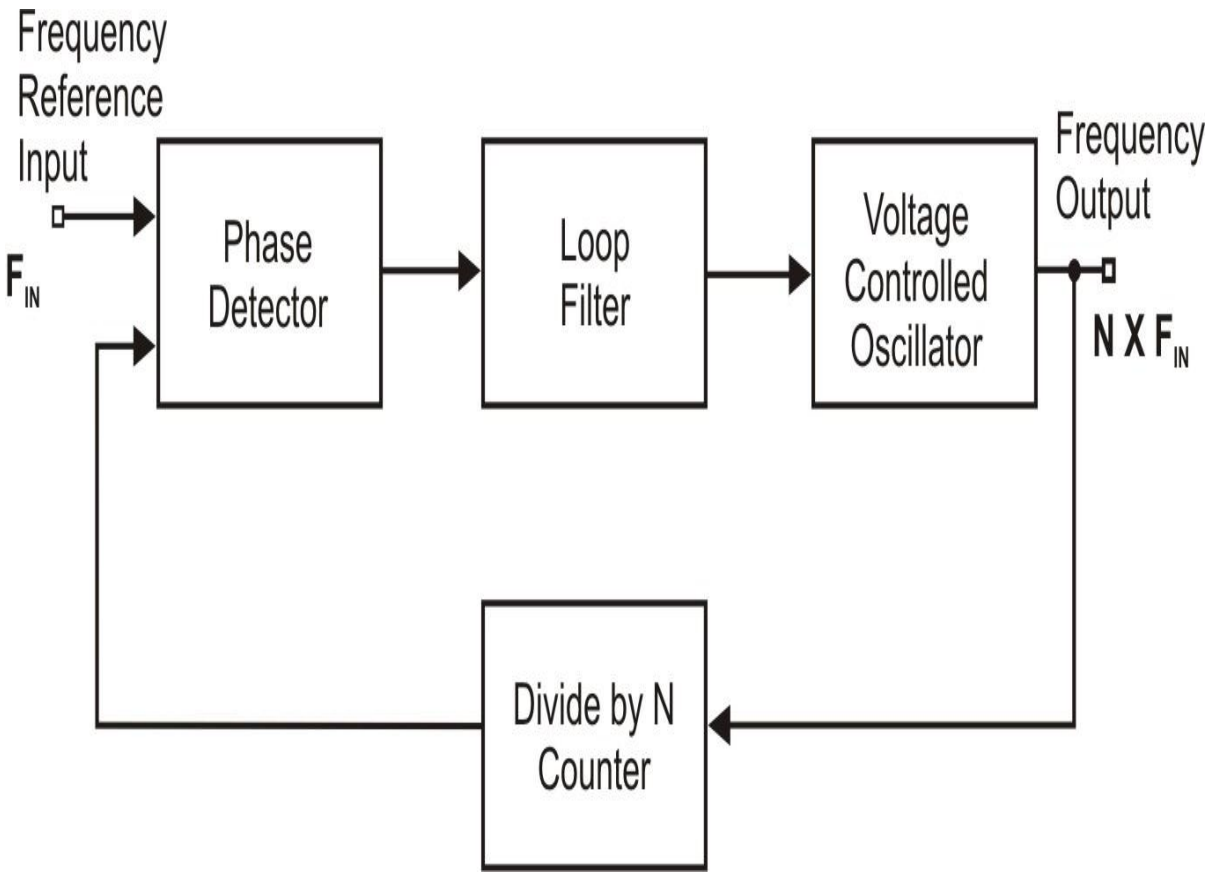

Figure 2.1: Architecture of phase locked loop

2.2.1 VCO and PFD

PFD is a circuit which detects and compares both phase of reference input and loop output of VCO. Figure 2.2 shows output of phase detector when XOR gate is used as a phase detector. The output in terms of state machine and waveform are presented in figures 2.3 and 2.4 respectively. The output of phase detector is up, when reference input leads and the same charge pump delivers charges to filter corresponding to reference input and gives feedback to VCO output. The VCO is a special type of oscillator that has a frequency which is controlled by an applied voltage. The frequency of the VCO without any control signal applied is called free running frequency.

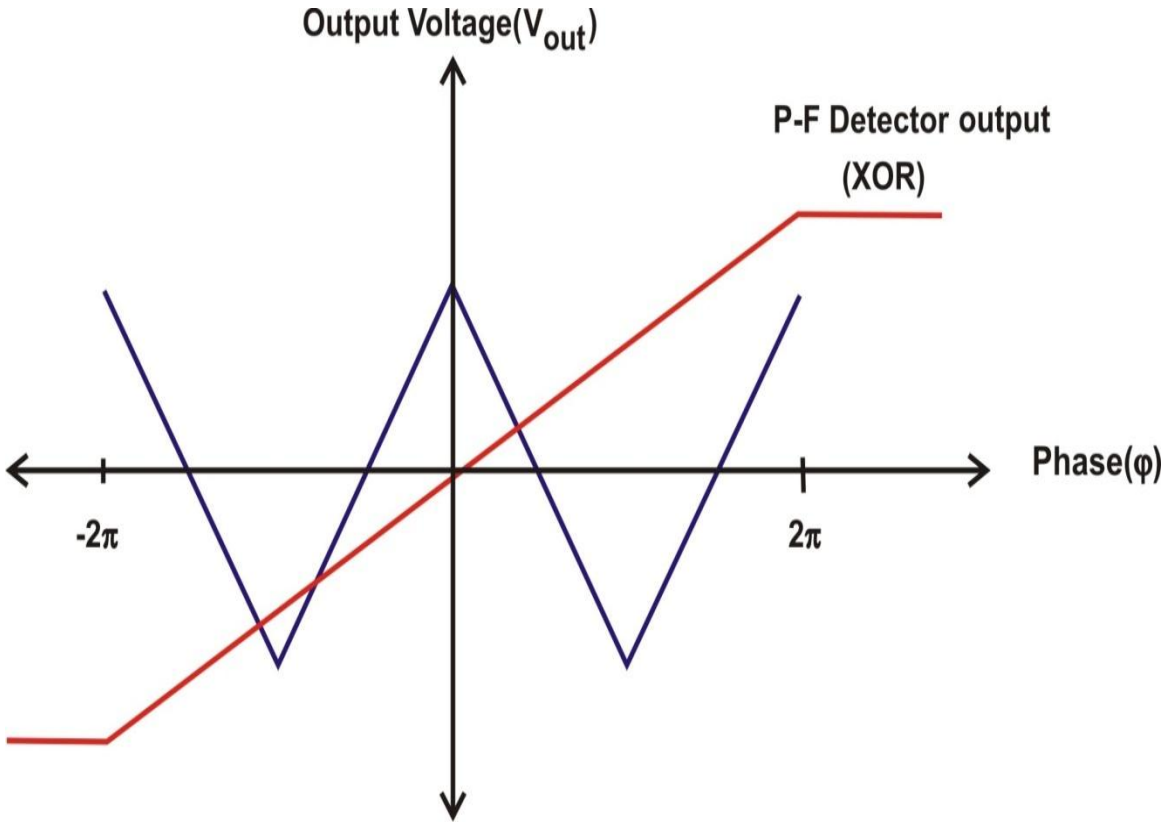

Figure 2.2: Phase/frequency detector output

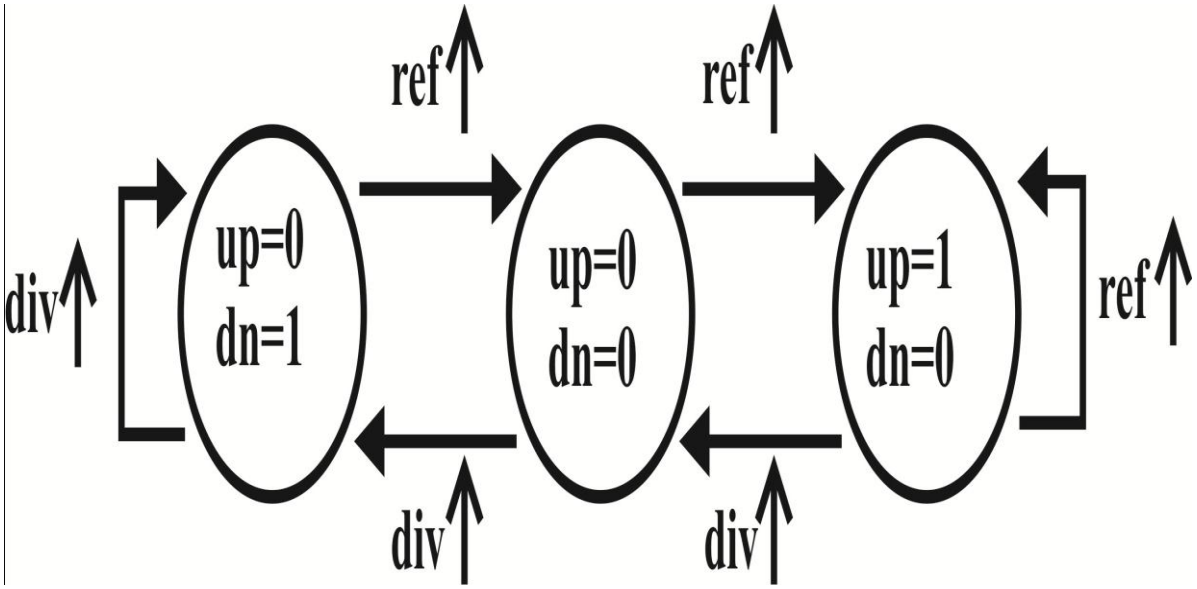

Figure 2.3: State machine diagram of phase/frequency detector

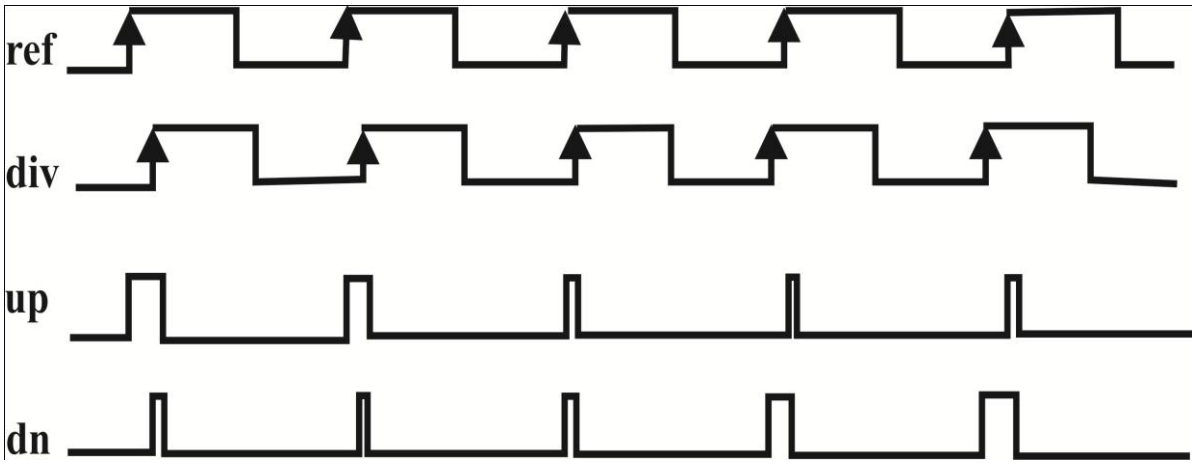

Figure 2.4: Signal waveform of phase/frequency detector

2.2.2 Charge Pump and Filter

Charge pump is a device that is used to convert output of phase difference into corresponding current pulses to control VCO output, which is as shown in figure 2.5. It consists of P_0 (p-type) and N_0 metal oxide semiconductor (n-type) field effect transistor (MOSFET) to their corresponding current sources I_p and I_n. These sources produce constant current I_0. P_{INC} and P_{DEC} output signals are received from PFD output, which will be input to the gate of P_0 and N_0, respectively. The capacitor C will charge and

discharge according to logic low and high respectively, which in turn switches on and off the field effect transistor (FET). The constant current I_0 depends upon corresponding currents I_p and I_n. The output of VCO depends upon capacitor voltage V_c. It means frequency of VCO is proportional to the V_c. The phase detector output will decide the frequency of oscillator. The frequency of oscillator is increased corresponding to negative pulse width of P_{INC}. And also it is decreased corresponding to positive pulse width of P_{DEC}. The content current I_0 originates from I_p and I_n current. Turning on-off of P_0 and N_0 determine the charging and discharging of the capacitor. This duration pumps capacitor to increase control voltage of VCO. If PFD requires decreasing frequency of VCO, then negative pulse width is decreased and corresponding charging and discharging can take place to pump out capacitor to decrease control voltage V_c. The pulse width of P_{INC} and P_{DEC} also determines the charging and discharging of the capacitor to fulfil essential requirements of system. Figure 2.6 depicts the transfer function attribute of phase frequency detector (PFD). The range of input variable is $-2\pi \sim +2\pi$ as shown in figure 2.6.

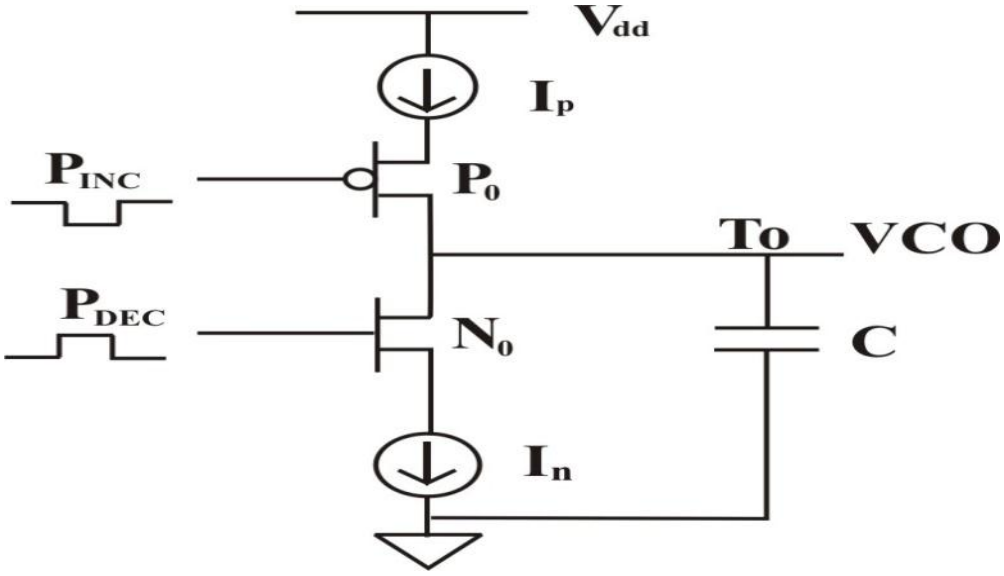

Figure 2.5: Schematic diagram of charge pump and filter

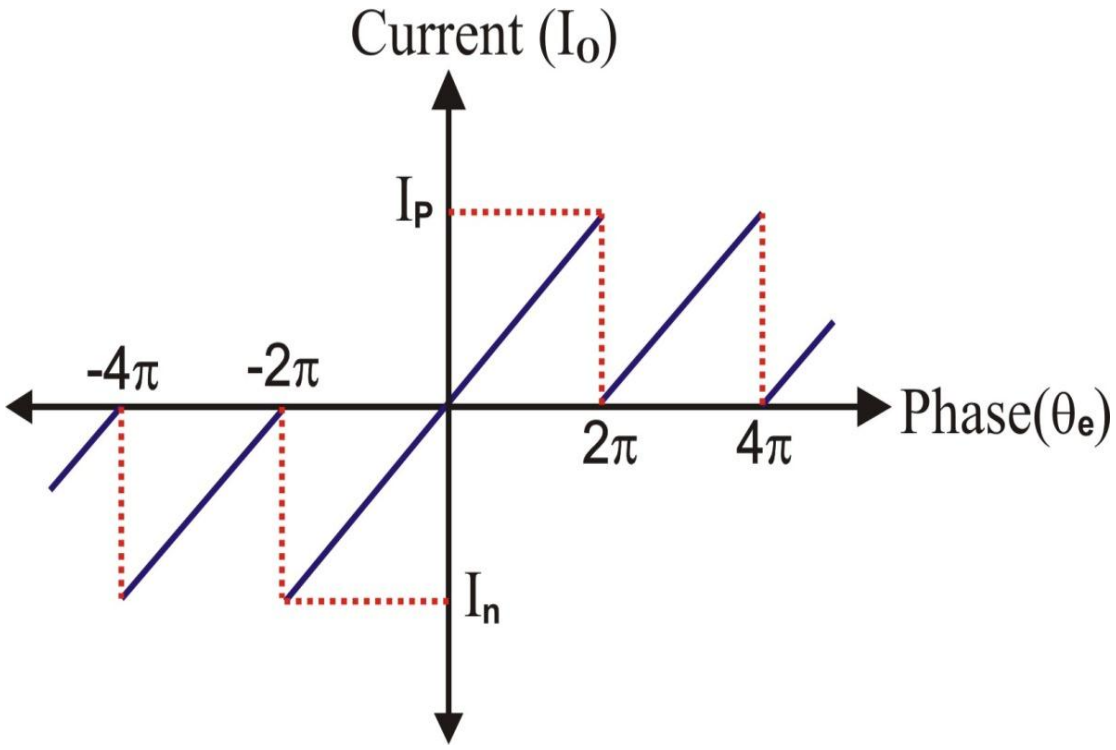

Figure 2.6: Phase/frequency detector /charge pump transfer function characteristic

Mathematical expression of the same has been presented in next section.

2.2.3 Mathematical Approach of PLL

In this section, mathematical analysis of the each component has been described. The linear and non-linear characteristics of VCO have been presented, in figure 2.7. The loop parameters are affected with variation of control characteristics and its loop compensation is widely used for wireless applications. Output of VCO may be shown as:

$$A_o[t, \omega(v)] = A(t, v)[sin\{\omega(v)t + \varphi\}] \quad (2.1)$$

$$A_o[t, \omega(v)] = A(t, v)[sin\{\omega(v)t\, cos(\varphi)\}] + A(t, v)[cos\{\omega(v)t\, sin(\varphi)\}] \quad (2.2)$$

$$A_o[t, \omega(v)] = A(t, v)\, sin\{\omega(v)t\} \cdot A(t, v)\, cos(\varphi) + A(t, v) cos\{\omega(v)t\} \cdot A(t, v) sin(\varphi) \quad (2.3)$$

Where,

$A =$ Amplitude, ω = Angular frequency and φ = Initial phase

The values of A and ω are varied corresponding to value of time t and control voltage v.

Further Eq. (2.3) can be explained as under:

$$A_o(t) = A\, sin[(\omega_1 + K_v v)t + \varphi] \quad (2.4)$$

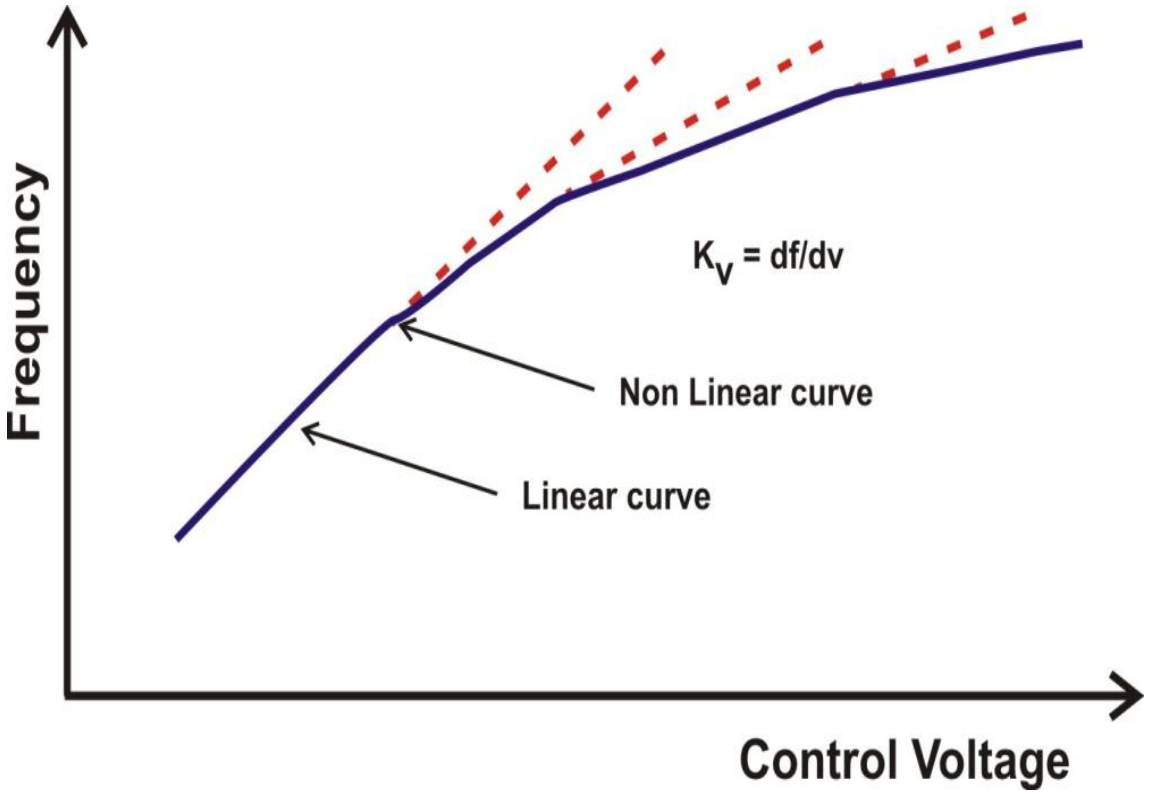

Figure 2.7: VCO characteristics and piecewise linearization

Where K_v is constant and it is assumed that frequency is linear and it is dependent on voltage v. Output frequency is determined as:

$$\omega(v) = \omega_1 + K_v v \tag{2.5}$$

As mentioned, the justification of linearization has been achieved, which can be used for a simple analysis. If frequency variation is small, then loop is locked. Let us assume that phase can be found after integration of angular frequency, which can be approximated as:

$$\varphi_{out}(s) = \frac{K_v v}{s} \tag{2.6}$$

$$\frac{\varphi_{out}(s)}{v} = \frac{K_v}{s} \tag{2.7}$$

The VCO output phase can be calculated by Laplace transfer function. This VCO voltage is determined corresponding to the reference input and loop feedback phase difference. It is a nonlinear function of input. Hence, it can be assumed to be linear, when it is close to locked position. Hence

$$K_{fd} = \frac{V_d}{\varphi_{in} - \varphi_{out}} \quad (2.8)$$

$$\varphi_{diff} = \varphi_{in} - \varphi_{out} \quad (2.9)$$

$$V_{fd} = K_{fd}(\varphi_{diff})\, V/rad \quad (2.10)$$

where V_{fd} = is output voltage of detector. The transfer functions of loop can be determined as:

$$V_{fd} = K_{fd}[\varphi_{diff}(s)]\, V/_{rad} \quad (2.11)$$

Let

$$V_c = V_{fd}(s)F(s) \quad (2.12)$$

The output of VCO (V_c) depends upon loop filter transfer function $F(s)$. After simplification, equation will be:

$$K = K_{fd}K_v \quad (2.13)$$

$$\varphi_{out}(s) = \frac{\varphi_{in}(s)K\,F(s)}{s+KF(s)} \quad (2.14)$$

$$H(s) = \varphi_{out}(s)/\varphi_{in}(s) \quad (2.15)$$

$$H(s) = \frac{K_{fd}K_vF(s)}{s+K_{fd}K_vF(s)} \quad (2.16)$$

The error function is defined as:

$$H_{error}(s) = \frac{\varphi_{diff}(s)}{\varphi_{in}(s)} \text{ is given by} \quad (2.17)$$

$$H_{error}(s) = \frac{s}{s+K_{fd}K_vF(s)} \quad (2.18)$$

Let us assume that all components are linearized and error depends upon K_v, K_{fd} and $F(s)$[98], [99]. The details of conventional architecture and their mathematical expression have been described in this section. The various configuration of PLL have been discussed in next section.

2.3 VARIOUS CONFIGURATION OF THE PLL

The effect of various noises should be minimized using different PLL configurations with effect of poles and zeros of the filters. The analysis of the various components of PLL has been presented in the sub-section discussed below:

2.3.1 Analysis of Loop Filter

In this sub section, first order loop parameters have been analyzed. The gain of the filter does not depend upon the frequency. The phase detector and VCO output requires constant gain to control the system. Since $F(s)$ is constant. The transfer function may be shown as:

$$\frac{\varphi_o(s)}{\varphi_i(s)} = H_1(s) \tag{2.19}$$

$$H_1(s) = \frac{K_v K_d A}{S + K_v K_d A} \tag{2.20}$$

For simplicity

$$K_1 = K_d K_v A \tag{2.21}$$

The first order loop transfer function is:

$$H_1(s) = \frac{K_1}{S + K_1} \tag{2.22}$$

These loop parameters like VCO constant (K_v), detector constant (K_d), and amplitude A have been analyzed to complete feedback mechanism. In this loop, phase is integrated to obtain frequency for the further analysis. The output phase will be given in terms of input phase φ_i as:

$$\varphi_o(t) = \varphi_i \left(1 - e^{-\frac{t_1}{K_1}}\right) \tag{2.23}$$

The phase error may be explained as:

$$\varphi_o - \varphi_i = \varphi_i e^{-t_1/K_1} \tag{2.24}$$

where, φ_i= Input phase

This assumes that the input phase is fixed. Then another parameters K_v, K_d, and A are determined to calculate stable loop output and its noise band width.

$$BW = \int_0^{\infty} |H_1(j\omega)|^2 \, df \tag{2.25}$$

The characteristics of RC filter and first order loop are similar in few conditions. After the settlement of transient error, transfer function has been analyzed which is given by following expression:

$$e_1(s) = H_1(s)\varphi_i(s) \tag{2.26}$$

$$e_1(s) = \frac{s\varphi_i(s)}{s+K_1} \tag{2.27}$$

$$\frac{e_1(s)}{\varphi_i(s)} = \frac{s}{s+K_1} \tag{2.28}$$

The final value theorem is used to calculate error function for phase step. Its steady state and transfer function have been analyzed by time and frequency domain. After this analysis, final value of the error for the phase step φ_i has been analyzed as:

$$\int_{-\infty}^{+\infty} x_1(t) = lim_{s\to 0}\, sX_1(s) \tag{2.29}$$

This equation determines that $X_1(t)$ is the Laplace transfer of $x_1(t)$.

$$lim_{s\to 0} \frac{s\varphi_i}{s+K_1} = 0 \tag{2.30}$$

Since output is determined corresponding to the input of the phase shift, which is represented in the form of phase ramp as:

$$lim_{s\to 0} \frac{d\omega}{s+K_1} = \frac{d\omega}{K_1} \tag{2.31}$$

The transfer function of phase with first order loop may be shown as:

$$H_1(s) = \frac{K_1(sT_2+1)/(T_1)}{s^2+\frac{s(1+K_1T_2)}{T_1}+K_1/(T_1)} \tag{2.32}$$

Natural frequency and damping ratio can be calculated as:

$$\omega_n = \sqrt{\frac{K_1}{T_1}} \qquad \& \qquad \varepsilon = \frac{\omega_n T_2}{2} \tag{2.33}$$

Then transfer function for the above equations, may be shown as:

$$H_1(s) = \frac{2\varepsilon\omega_n s+\omega_n^2}{s^2+2s\omega_n\varepsilon+\omega_n^2} \quad (2.34)$$

Natural frequency and damping factor are two important parameters, which are used to determine characteristics of the system. Now band width of loop can be calculated as:

$$BW_L = \frac{\omega_n}{2(\varepsilon+\frac{1}{4\varepsilon})} \quad (2.35)$$

An active integrator and passive networks are used to realize loop parameters for the system. The equation for the same may be shown as:

$$\omega_n = \sqrt{\frac{K_1}{T_1}} \quad (2.36)$$

and

$$\varepsilon = \frac{\omega_n T_2}{2} \quad (2.37)$$

and passive network can be represented as:

$$\omega_n = \sqrt{\frac{K_1}{T_1+T_2}} \quad (2.38)$$

and

$$\varepsilon = \frac{\omega_n(T_2+1/K_1)}{2} \quad (2.39)$$

In PLL synthesizers, the output of the VCO is usually followed by a divider. In lock conditions, the output frequency will be given by NF_{ref} and so by changing N, the output frequency changes. Finally, transfer function of higher order and type of PLL can be analyzed for further analysis. The passive loop filter and its parameters are described in the next sub-section.

2.3.2 Analysis using Passive Loop Filter

In this sub section, many technical issues of loop filter have been discussed. The parameters such as the proper loop topology, loop filter orders, pole ratios, bandwidth, and phase margin are determined to improve the performance of the system. After choosing particular topology or order of filter, sub parameters have been analyzed in the next sub-section.

2.3.2.1 VCO Gain adjustment

The loop gain (K) is very important, which is determined by VCO gain, charge pump gain, and N value. The equation for loop gain is given as:

$$K = \frac{K_{\emptyset} V_{vco}}{N} \tag{2.40}$$

If loop gain is very low or constant, then it is not critical for loop design perspective. Since the value of the N counter varies by a factor of two. The geometric mean of its minimum and maximum values is determined by loop gain in order to minimize how much the loop band width can vary from the desirable design value.

$$K_{new\_design} = \sqrt{K_{min} K_{max}} \tag{2.41}$$

The charge pump current can adjust this value, if loop gain is not specified. Since VCO gain and charge are constant, and then N is responsible to the geometric mean of the minimum and maximum values.

$$N_{new\_design} = \sqrt{N_{min} N_{max}} \tag{2.42}$$

If the loop gain varies more than a factor of two, then add more consideration to lower order loop filters, because they are more resistant to changes in the loop gain. If the loop gain varies by more than two, a second order filter can handle this, but higher order problems could start having issues.

2.3.2.2 Impedance of Loop Filter

The 3rd order loop filter is useful in filtering spurs or noise originated by the PLL that is at an offset frequency of ten times the loop band width or greater.

The band width is ω_c, and phase margin is $\emptyset$, the user also has to specify the pole ratio T_{31}. This parameter can range from zero to one. A good starting value for this parameter is 0.5. The impedance for the filter is given by:

$$Z_3(s) = \frac{1+sT_2}{sA_0(1+sT_1)(1+sT_3)} \quad (2.43)$$

$$= \frac{1+sC_2R_2}{s(A_2s^2+A_1s+A_0)} \quad (2.44)$$

$$A_1 = A_0(T_1 + T_3);\ \ A_2 = A_0T_1T_3 = C_1C_2R_2C_3R_3\ ;\ T_2 = R_1R_2C_2\ ; \quad (2.45)$$

Finally, the loop filter is defined as the output voltage at the VCO divided by current injected at the PLL charge pump.

2.3.2.3 Time Constants

Time constants are used to determine position of poles and zeros and also it helps to the designer to design the filter.

Assume phase margin$= 0$, the equation may be written as:

$$T_2 = \frac{\gamma}{\omega_c{}^2T_1(1+T_{31})} \quad (2.46)$$

where γ = Optimization factor

The phase margin is given by:

$$\emptyset = tan^{-1}(\omega_cT_2) - tan^{-1}(\omega_cT_1) - tan^{-1}(\omega_cT_3) \quad (2.47)$$

$$\emptyset = tan^{-1}\left(\frac{\gamma}{\omega_cT_1(1+T_{31})}\right) - tan^{-1}(\omega_cT_1) - tan^{-1}(\omega_cT_1T_{31}) \quad (2.48)$$

This can either be solved numerically or approximately as:

$$tan(x) \approx x \approx tan^{-1}\,x$$

$$T_1 \approx \frac{sec(\emptyset)-tan(\emptyset)}{\omega_c(1+T_{31})} \quad (2.49)$$

$$T_3 = T_1T_{31} \quad (2.50)$$

$$T_2 = \frac{\gamma}{\omega_c{}^2(T_1+T_3)} \tag{2.51}$$

The total capacitance:

$$A_0 = \frac{K_\emptyset K_{vco}}{\omega_c{}^2 N} \sqrt{\frac{1+\omega_c{}^2 T_2{}^2}{(1+\omega_c{}^2 T_1{}^2)(1+\omega_c{}^2 T_3{}^2)}} \tag{2.52}$$

The true impedance of the filter is given by:

$$Z(s) = \frac{1+sT_2}{s(1+sT_1)(1+sT_3)} \frac{1}{A_0} \tag{2.53}$$

Recall that the loop filter components relate the time constants in the following manner for a passive filter.

$$A_2 = A_0 T_1 T_3 = C_1 C_2 C_3 R_2 R_3 \tag{2.54}$$

$$A_1 = A_0(T_1 + T_3) \tag{2.55}$$

There are many possible choices, but the optimal choice is the one that maximizes the capacitor C_1. This is desirable because it minimizes the impact of the VCO capacitance and also resistor thermal noise due to R_3. Although the choice of C_1 that minimizes R_3 is slightly different than the choice of C_1 that maximizes C_3, these two values are very close, and making C_3 larger which attenuates the noise due to resistor R_3. The choice of C_1 is given as:

$$C_1 = \frac{A_2}{T_2{}^2}\left(1 + \sqrt{1 + \frac{T_2}{A_2}(T_2 A_0 - A_1)}\right) \tag{2.56}$$

Combining these equations yields:

$$A_1 = T_2 C_1 - \frac{A_2 A_0}{T_2 C_1} - \frac{A_2 C_3}{T_2 C_1} \tag{2.57}$$

The above equation can be solved in order to express C_3 in terms of C_1:

$$C_3 = \frac{-T_2{}^2 C_1{}^2 + T_2 A_1 C_1 - A_2 A_0}{T_2{}^2 C_1 - A_2} \tag{2.58}$$

C_2 and the other components can now be easily found.

$$C_2 = A_0 - C_1 - C_3 \tag{2.59}$$

$$R_2 = \frac{T_2}{C_2} \tag{2.60}$$

$$R_2 = \frac{A_2}{C_2 C_3 T_2} \tag{2.61}$$

The time constant plays major role to design passive loop filter for the PLL. Further, transfer function of higher order and type of passive filter can be analyzed for further analysis. The topology of passive filter and their parameters have been described in this sub section.

2.3.3 Analysis using Active Loop Filter

In Active loop filter, the proper loop topology, loop filter order, operational amplifier (OPAMP), band width, phase margin, and pole ratios are the main parameters, by which performance of the filter can be determined. Generally, at the output of phase detector, two classes of active filters are used which use various topologies for the same. The approaches are used to boost the charge pump output voltage, to add gain stage before the VCO and put component in loop of active filter.

2.3.3.1 Gain approach

Placing of OPAMP in front of the VCO is very instinctive approach to be generally used. A non-inverting configuration of op-amp is used to produce gain A. The value of resistor R_x should be larger enough so that the current consumption is not excessive. Choosing R_x excessively large would lead to problems due to the resistor thermal noise. To control the thermal noise, the capacitance of the capacitor C_b can be reduced drastically. The negative gain A is given by the expression:

$$A = -\left(1 + \frac{R_a}{R_b}\right) \tag{2.62}$$

2.3.3.2 Feedback approaches

The feedback approach is the commonly used to eliminate the problem, which is generally due to gain of gain stage. This approach introduces an inversion, which can be found by the phase detector of PLL to change the polarity to negative. It is necessary to establish bias voltage by the resistive divider in the non-inverting op-amp. Since the resistors are chosen too small, it will consume excessive current, whereas, in case of too large resistor, it will generate excessive resistor noise. Considering these conditions, the resistors will bias the CP output at half the power supply. The equation for bias voltage is as:

$$V_b = \frac{v_s \cdot R_b}{R_a + R_b} \tag{2.63}$$

where

v_s= Charge pump supply

R_a and R_b = Bias resistors

2.3.3.3 OP-AMP selection

The selection of op-amp depends on the various parameters like offset voltage, noise voltage, noise current, input rails, output rails, and slew rate, which affects the system performance.

2.3.3.4 Impedance and Loop Gain of Filter

Impedance is the essential parameter of filter to design system. It is defined as the output voltage of VCO which is produced by a charge pump current. The transfer function of the impedance may be given as:

$$Z(s) = \frac{1+sT_2}{sA_0} \frac{A}{(1+sT_1)(1+sT_3)(1+sT_4)} \tag{2.64}$$

Assuming that charge pump polarity is inverted, the open loop gain becomes:

$$\frac{G(s)}{N} = -\frac{K_\emptyset K_{VCO} A}{\omega^2 N} \frac{1+ST_2}{sA_0(1+sT_1)(1+sT_3)(1+sT_4)} \tag{2.65}$$

2.3.3.5 Time Constants

The time constant is the main parameter, the loop filter components can be calculated from these time constants.

2.3.3.6 Loop Filter Coefficient

The value of A_0 can be calculated by setting the open loop gain and band width.

$$A_0 = \frac{K_\emptyset K_{vco} A}{{\omega_c}^2 N} \sqrt{\frac{1+{\omega_c}^2 {T_2}^2}{(1+{\omega_c}^2 {T_1}^2)(1+{\omega_c}^2 {T_3}^2)(1+{\omega_c}^2 {T_4}^2)}} \quad (2.66)$$

This section described active filter topology and their parameters of the conventional system. Therefore, transfer function of higher order and type of active filter can be analyzed for further analysis.

2.4 PHASE NOISE ESTIMATION

The basics & behaviours of 1/f phase noise, loop transfer function noise, flat noise, N divider noise, and VCO phase noise have been analyzed [99] in this section.

2.4.1 Noise of Loop Transfer Function and N Divider

A parameter that has the largest impact on phase noise is N counters value. The value of N counters increases phase noise. Loop band width is the main constraint with their offset frequency to approximate transfer function by N divider. Noise voltage due to phase noise and noise power is also proportional to square of N value.

$$PLL_{noise_{flat}}(offset) = PhaseNoiseFloor + 10\,log\,N^2 \quad (2.67)$$

The transfer function cannot be approximated if phase noise is out of loop band width.

$$PLL_{noise_{flat}}(offset) = PhaseNoiseFloor + 20\,log|ClosedLoop(offset)| \quad (2.68)$$

2.4.2 Flat Noise

It is flat phase noise. The comparison frequency (F_{comp}) is inversely proportional to N. Therefore, noise due to phase detector degrades in accordance with $10\,log(F_{comp})$. The phase noise can be predicted using $1\,Hz$ normalized phase noise $(PN\ 1\,Hz)$, which is part-specific and assumes the highest charge pump current. PLL phase noise within Band width is:

$$PLL_{noise_{flat}} = PhaseNoise\ 1\,Hz + 10\,log\,N^2 + 10\,log\left|F_{comp}\right| \quad (2.69)$$

In case of outside of Band width:

$$PLL_{noise_{flat}} = PhaseNoise1Hz + 20\,log|ClosedLoop(offset)| + 10\,log\left|F_{comp}\right| \quad (2.70)$$

2.4.3 1/f Noise

It is a type of noise, normally it is decremented by $10\ dB/decade$ and normalizes at $10\ kHz\ offset, 1\ GHz$ output and $PN\ 10\ kHz$. It is not affected by N counters value. It is multiplied by roll-off. The sum of various noises is approximated as:

$$CN = 20\,log\left|\frac{F_{out}}{1\ GHz}\right| \quad (2.71)$$

$$CN = 20\,log\ (F_{out}) - 20\,log\ (1\ GHz) \quad (2.72)$$

$$FN = 10\,log\ (offset) - 10\,log\ (10\ kHz) \quad (2.73)$$

$$PLL_{noise_{flat}}(F_{out,}offset) = PhaseNoise\ 10\ kHz + CN - FN \quad (2.74)$$

Where CN =Noise due to comparison frequency

FN = Flat noise

2.4.4 Voltage Controlled Oscillator Phase Noise

The VCO is main component of PLL. Phase noise of VCO degrades performance of system. This noise is divided into three regions. The first region is close to carrier, and phase noise drops off at $30\ dB/decade$. This is often due to flicker noise of transistors. The second region is $1/f^3$ noise and in third region, it decreases around $20\ dB/decade$.

It is controlled by many factors. This equation describes phase noise in this region and is called Lesson's equation which is given as:

$$L(f) = 10\ log\left(\frac{1}{2}\ \frac{F \cdot k \cdot T}{P}\ \left(\frac{f_{vco}}{2Q_L f}\right)^2\right) \quad (2.75)$$

where,

$L(f)$ = Phase noise in dBc/Hz

f = Offset frequency

F = Noise figure

T = Temperature in Kelvin

k = Boltzmann's constant

P = Power at input of active device

Q_L = Inductor quality factor (Loaded)

f_{vco} = Operating frequency of oscillator

Noise is determined using slope of $20\ dB/decade$. However, it only works in one region of the VCO and neglects noise contribution due to noise resistance of the Varactor diode. The formula below is an expanded version of Lesson's equation that shows phase noise in all three regions.

$$L(f) = 10\ log\left(\frac{1}{2}\left[\left(\frac{f_{vco}}{2Q_L f}\right)^2 + 1\right]\left[\frac{f_{1/f^3}}{f} + 1\right]\left[\frac{F\ k\ T}{P}\right] + \frac{2\ k\ T\ R_{var}\ {K_{vco}}^2}{f^2}\right) \quad (2.76)$$

where

f_{1/f^3} = $1/f^3$ flicker noise

R_{var}= Noise resistance of the Varactor diode

K_{vco} = VCO gain

This section described various noise estimations with their transfer function and mathematical expression. Besides these noises, another noise sources have been presented in the next section.

2.5 CONSTANT-TIME LINEAR PHASE ANALYSIS

PLL is considered as linear system. It includes PFD, CP, filter, and oscillator. Here PFD and charge pump are combined together to analyze linear phase of given model. Output is affected by their sources of noise in each block that is shown in figure 2.8.

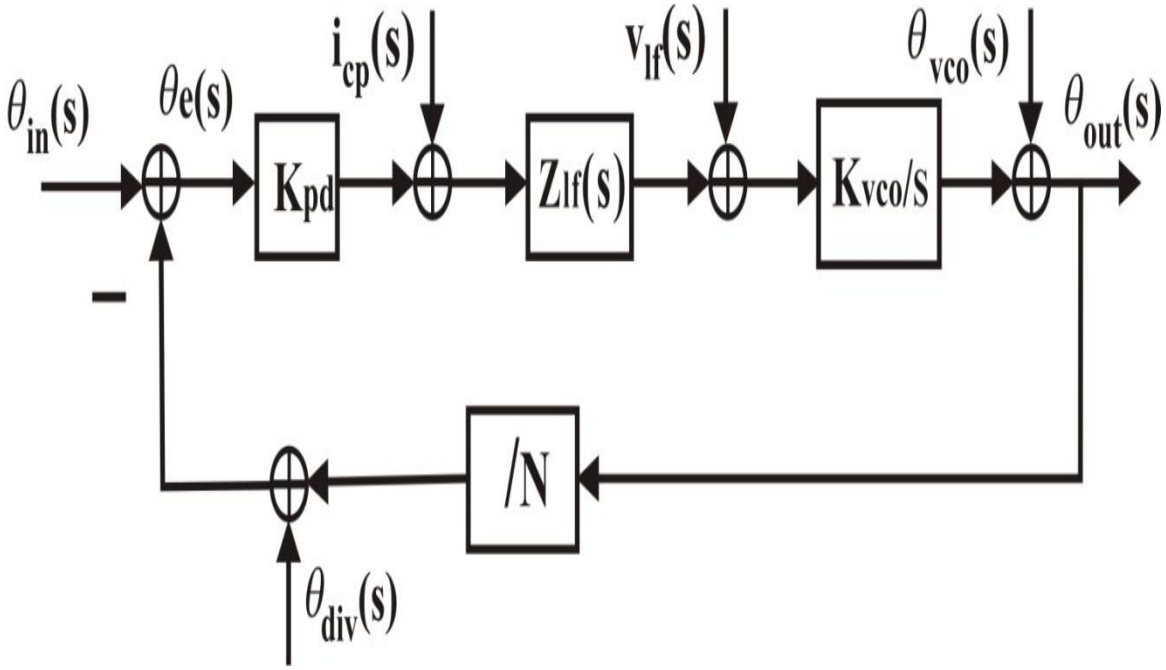

Figure 2.8: Linear phase noise sources

PN = Phase noise

CP = Charge pump

DIV = Divider

VN = Voltage noise

LPF = Low pass filter

θ_{in} =Input PN

$i_{cp}(s)$ = Current noise originated by PFD CP

$v_{lf}(s)$ = VN

$\theta_{vco}(s)$= VCO output PN

$\theta_{div}(s)$ = Phase noise by DIV

K_{pd} =Gain of PFD

K_{vco} =VCO Gain

$Z_{lf}(s)$ = Transimpedance of LPF

N = Frequency division ratio

Open loop phase noise transfer functions:

$$\mathrm{H_{inputnoise}}(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_{vco}}{s} \cdot \frac{1}{1+H_{ol}(s)} \quad (2.77)$$

$$\mathrm{H_{PFDnoise}}(s) = \frac{\theta_o(s)}{i_{cp}(s)} = \frac{N}{K_{fpd}} \cdot \frac{H_{ol}(s)}{1+H_{ol}(s)} \quad (2.78)$$

$$\mathrm{H_{LFnoise}}(s) = \frac{\theta_o(s)}{v_{lf}(s)} = \frac{K_{vco}}{s} \cdot \frac{1}{1+H_{ol}(s)} \quad (2.79)$$

$$\mathrm{H_{VCOnoise}}(s) = \frac{\theta_o(s)}{\theta_{vco}(s)} = \frac{1}{1+H_{ol}(s)} \quad (2.80)$$

$$\mathrm{H_{DIVnoise}}(s) = \frac{\theta_o(s)}{\theta_{div}(s)} = -N \cdot \frac{H_{ol}(s)}{1+H_{ol}(s)} \quad (2.81)$$

Where

$$H_{ol}(s) = \frac{K_{fpd}K_{vco}Z_{lpf}(s)}{N \cdot s} \quad (2.82)$$

$H_{ol}(s)$ = Open loop transfer function

2nd & 3rd order filters are generally employed in the most PLL. Mathematical expressions for the various filters are described below. Circuit diagram of 3rd order passive filter is depicted in figure 2.9.

The loop filter consists of various parameters like poles and zeros that are calculated from the PLL open as shown in figure 2.10. Phase margin $\emptyset_m$and cross over band width ω_c projected using Bode plot for the open loop of PLL is shown in figure 2.11.

Dynamic characteristics of the closed loop have been analyzed that are used to determine damping factor ζ and natural frequency ω_n for the 2nd order system. Impedance may be expressed as:

$$Z_f(s) = \frac{V_c(s)}{I_{cp}(s)} = R_1 \frac{1+sR_1C_1}{sR_1C_1} = R_1 \frac{\omega_z+s}{s} \quad (2.83)$$

where

$$\omega_z = \frac{1}{R_1 C_1} \tag{2.84}$$

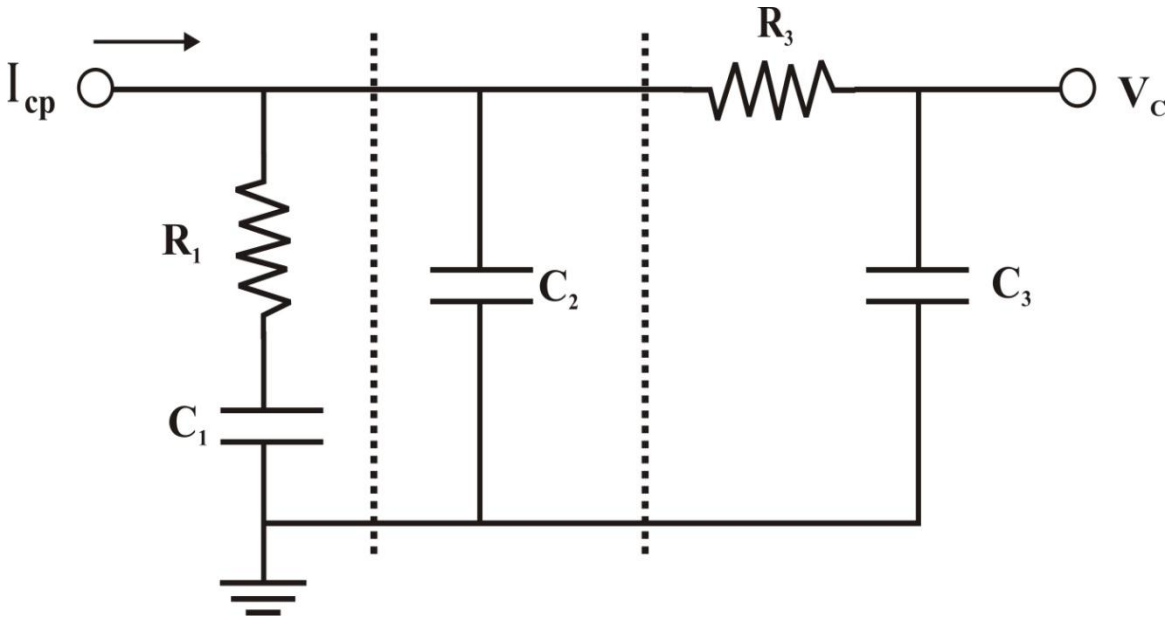

Figure 2.9: Third order loop filter

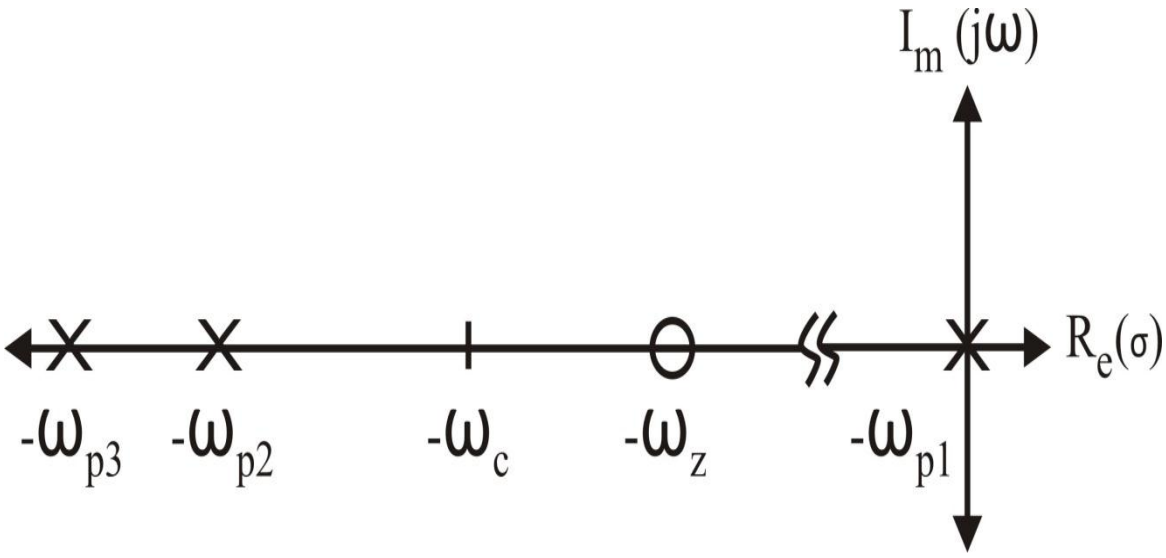

Figure 2.10: Pole zero locations

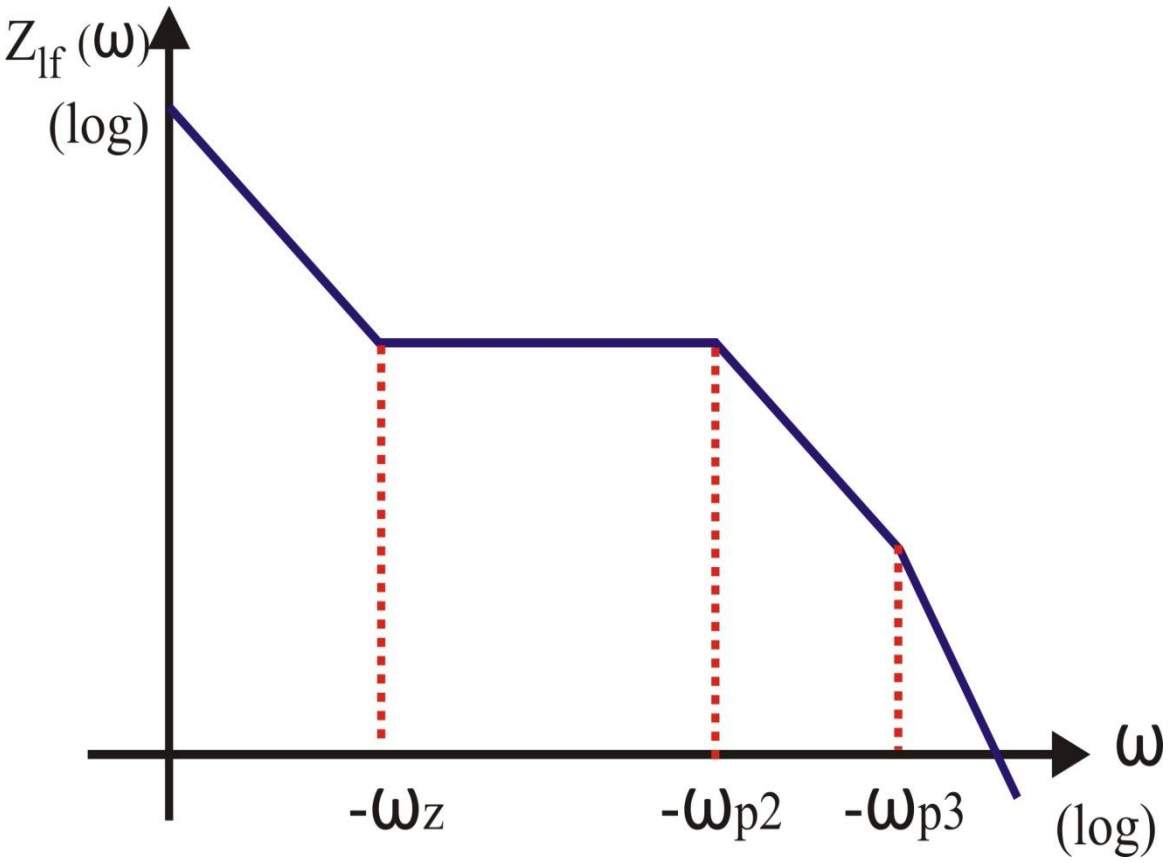

Figure 2.11: Bode plot of transimpedance

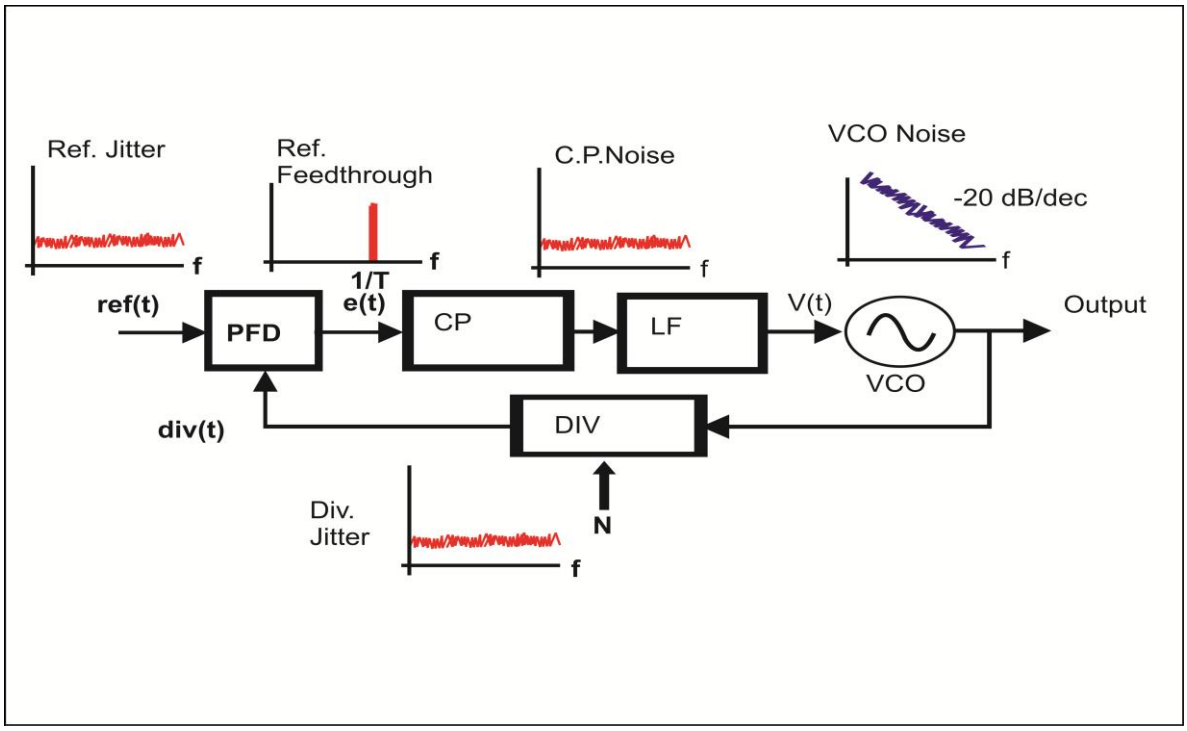

Figure 2.12: Noise sources of PLL

It is stable if ω_z is zero. If $\omega_{p1} = 0$, then

PLL open loop gain is:

$$H_{olg}(s) = \frac{K_{fpd}K_{vco}R_1}{Ns} \cdot \frac{1+sR_1C_1}{sR_1C_1} = K\frac{1+sR_1C_1}{s^2R_1C_1} \quad (2.85)$$

where $H_{olg}(s)$ = Open loop gain

Gain is given as:

$$K = \frac{K_{fpd}K_{vco}R_1}{N} \quad (2.86)$$

Open loop gain is 1 at the crossover frequency:

$$\omega_c = \sqrt{\frac{K^2+K\sqrt{K^2+4{\omega_z}^2}}{2}} \quad (2.87)$$

Phase margin is given by:

$$\emptyset_m = tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) \quad (2.88)$$

Closed loop gain of second order is given by the expression:

$$H_{clg}(s) = \frac{\theta_o(s)}{\theta_i(s)} = N\frac{K(s+\omega_z)}{s^2+Ks+K\omega_z} \quad (2.89)$$

where $H_{clg}(s)$ = Closed loop gain

Assume $R_3 = 0$ & $C_3 = 0$

Transimpedance of passive loop filter (second order) is given by:

$$Z_f(s) = R_1\frac{1+sR_1C_1}{sR_1(C_1+C_2)+s^2R_2C_1R_1C_2} = R_1\frac{1+s/\omega_z}{s(1+s/\omega_{p2})/\omega_z}\frac{b-1}{b} \quad (2.90)$$

i.e. $b = 1 + C_1 + C_2$

$$\omega_{p2} = \frac{1}{R_1\frac{C_1C_2}{C_1+C_2}} = b\omega_z \approx \frac{1}{R_1C_2} \quad (2.91)$$

Then the open loop gain becomes:

$$H_{clg}(s) = K\frac{1+s/\omega_z}{s^2(1+s/\omega_{p2})/\omega_z}\frac{b-1}{b} \quad (2.92)$$

The band width of third order charge pump can be expressed as:

$$\omega_c = K\ \frac{b-1}{b}\ \frac{cos(\emptyset_{p2})}{sin(\emptyset_z)} \quad (2.93)$$

Where $\emptyset_z = tan^{-1}\left(\frac{\omega_c}{\omega_z}\right)$

And $\emptyset_{p2} = tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right)$. The open loop phase margin now becomes:

$$\emptyset_m = \emptyset_z - \emptyset_{p2} = tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right) \quad (2.94)$$

2nd order passive filter's transfer function is described by:

$$H_{clg}(s) = N\frac{1+s/\omega_z}{1+\frac{s}{\omega_z}+s^2/(\omega_z\omega_c)+s^3/(\omega_z\omega_c\omega_{p2})} \quad (2.95)$$

The transimpedance of third order passive loop is given by the following expression:

$$Z_f(s) = \frac{1}{s}\frac{(1+sR_1C_1)/(C_1+C_2+C_3)}{1+s\frac{R_1C_1(C_2+C_3)+R_3C_3(C_1+C_2)}{C_1+C_2+C_3}+s^2\frac{R_2C_1R_3C_2C_3}{C_1+C_2+C_3}} \quad (2.96)$$

Usually, $C_1 \ll C_2, C_3$ and $R_1 \gg R_3$

$$Z_f(s) = \frac{1}{s(C_1+C_2+C_3)}\frac{1+s/\omega_z}{(1+s/\omega_{p2})(1+s/\omega_{p3})} \quad (2.97)$$

$$\omega_{p2} = \frac{1}{R_1(C_3+C_2)} \quad ; \quad \omega_{p3} = \frac{1}{R_3C_2C_3/(C_3+C_2)} \quad (2.98)$$

Band width of fourth order charge pump is given below:

$$\omega_c = K\frac{C_1}{C_1+C_2+C_3}\frac{cos(\emptyset_{p2})\cdot cos(\emptyset_{p3})}{sin(\emptyset_z)} \quad (2.99)$$

And $\emptyset_{p3} = tan^{-1}\left(\frac{\omega_c}{\omega_{p3}}\right)$. Open loop phase margin becomes:

$$\emptyset_m = \emptyset_z - \emptyset_{p2} - \emptyset_{p3} = tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right) - tan^{-1}\left(\frac{\omega_c}{\omega_{p3}}\right) \quad (2.100)$$

From the mathematical analysis discussed above, it is clear that how the parameters of filter are used to suppress noise and to stabilize the system for improving the performance. Here various order and type of the filter topologies have been presented for analysis. Considering above noise, another sources of noise have been presented in figure 2.12. Analysis of above noise has already been discussed in detail. In the next section, new techniques have been proposed to overcome those limitations.

2.6 PROPOSED SCHEMATIC ANALYSIS

This section presents a novel technique to contribute source noise removal using various configurations for the PLL. The architecture and algorithm have been proposed to reduce phase noise of output of system.

There are various components which originate the noise in the form of reference input, charge pump, VCO, filter, and divider noise. This work has calculated phase noises and found their effect on the power spectral of output signal of PLL. The calculated values for the same have been given in table 2.1. Filter is an important component to analyze noise. Active and passive filters originate various types of noises. White noise is originated due to resistors in passive filters and 1/f noise examines in active filter. The noise in the active filter can be determined by increasing the order of filter. It will be better for a designer to select various filter parameters, but on the other hand instability of the loop will be increased. That's why in terms of cost, simplicity, and phase noise, passive filters were recommended over the active filters. Third order active filters were generally recommended, when added pole reduces the phase noise and where the VCO required a higher tuning voltage than PLL so that charge pump could operate. This higher tuning voltage is capable of tuning over broader frequency ranges and better phase noise than their lower tuning voltage can be achieved. Other noise due to small random variations on oscillator's input and above mentioned noises are the important factors that cause output phase noise. The variations on VCO input voltage has to be reduced to propose advanced loop filter (with active and passive components) before VCO. Oscillator noise effects are more in a particular frequency range to reduce output noise, which is originated by VCO. The phase detector and VCO are overriding noise sources within loop band width and outside loop band width. The various transfer functions and algorithms have been presented for better performance.

Table 2.1: Noise Sources of PLL

Frequency (Hz)	Noise sources with passive 3 pole configuration (dBc/Hz)			Noise sources with passive 4 pole configuration (dBc/Hz)			Noise sources with active 3 pole configuration (dBc/Hz)		
	Ref.	PFD	VCO	Ref.	PFD	VCO	Ref.	PFD	VCO
1 Hz	-30.33	-108.01	-129.34	-30.08	-88.31	-160.08	-45.01	-112.00	-115.90
10 Hz	-58.21	-108.10	-120.06	-58.66	-87.10	-149.71	-67.12	-112.01	-95.88
100 Hz	-80.54	-108.55	-109.90	-82.90	-87.22	-137.75	-87.20	-114.02	-85.46
1 kHz	-90.12	-109.89	-98.65	-88.56	-86.90	-120.20	-92.34	-119.53	-88.97
10 kHz	-89.98	-105.45	-120.23	-96.00	-82.65	-100.00	-105.01	-120.22	-98.11
100 kHz	-125.00	-125.02	-112.77	-121.89	-110.23	-119.60	-139.13	-150.76	-118.75

Transfer functions and impedances of proposed configurations:

The basic mathematical approach of the system has already been discussed in the mathematical approach of architecture. This section describes transfer functions those are being used in the proposed system.

Assume that the input signal is

$$v_{in}(t) = A_i \sin[\omega_o t + \theta_i(t)] \quad (2.101)$$

and that the VCO output signal is

$$v_o(t) = A_o \cos[\omega_o t + \theta_o(t)] \quad (2.102)$$

Where

$$\theta_o(t) = K_v \int_{-\infty}^{t} v_2(\tau) d\tau \quad (2.103)$$

K_v = Gain constant

$\theta_i(t)$ = Input phase

Then Phase detector output is

$$v_1(t) = K_m A_i A_o \sin[\omega_o t + \theta_i(t) \cos[\omega_o t + \theta_o(t)] \quad (2.104)$$

Where

K_m = PFD Gain

So output of filter is

$$v_2(t) = K_d[\sin\theta_e(t)] * f(t) \quad (2.105)$$

This depends upon levels of the A_i (input signal) and A_o(level of oscillator signal).

$$K_d = K_m A_i A_o/2 \quad (2.106)$$

K_d = Equivalent phase detector constant

$$\theta_e(t) \triangleq \theta_i(t) - \theta_o(t)$$

where

$f(t)$ = Impulse response of the filter

$\theta_e(t)$ = Phase error

The overall equation describing the operation of the PLL may be obtained by taking derivative of equation.

$$\frac{d\theta_e(t)}{dt} = \frac{d\theta_i(t)}{dt} - K_d K_v \int_0^t [\sin\theta_e(\lambda)]\, f(t-\lambda)d\lambda \quad (2.107)$$

Where $\theta_e(\lambda)$ is the unknown and $\theta_i(t)$ is the forcing function

If gain is large, so that the loop is locked and the error $\theta_e(t)$ is small. In this case,

$$\sin\theta_e(t) \approx \theta_e(t)$$

And the resulting linear equation is

$$\frac{d\theta_e(t)}{dt} = \frac{d\theta_i(t)}{dt} - K_d K_v \theta_e(t) * f(t) \quad (2.108)$$

The closed loop transfer function is:

$$H(f) = \frac{\Phi_o}{\Phi_i} = \frac{F[\theta_o(t)]}{F[\theta_i(t)]} = \frac{K_d K_v F(f)}{j2\pi f + K_d K_v F(f)} \quad (2.109)$$

There are three filter topologies which have been incorporated with the transfer functions.

Charge pump detector with passive 3 poles topology:

Impedance of second order filter is:

$$Z_{3p}(s) = \frac{s\,C_2R_1+1}{s^2C_1C_2R_1+s\,C_1+s\,C_2} \quad (2.110)$$

Charge pump detector with passive 4 poles topology:

$$Z_{4p}(s) = \frac{Z_{3p}(s)\left(\frac{1}{s\,C_3}\right)}{Z_{3p}(s)+R_3+\left(\frac{1}{s\,C_3}\right)} \quad (2.111)$$

Charge pump detector with active 3 poles topology:

Active filter's 3rd order transfer function may be shown as:

$$Z_1(s) = \frac{1}{sC_1} \quad (2.112)$$

$$Z_2(s) = \frac{R_1\frac{1}{sC_2}}{R_1+\frac{1}{sC_2}} \quad (2.113)$$

$$Z_{3a}(s) = Z_1(s) + Z_2(s) \quad (2.114)$$

$$Z_{3a}(s) = \frac{1}{sC_1} + \frac{R_1\frac{1}{sC_2}}{R_1+\frac{1}{sC_2}} \quad (2.115)$$

$$Z_{3a}(s) = -\frac{1+R_1(1+sC_2)}{sC_1(1+sR_1C_2)} \quad (2.116)$$

$$\frac{V_{fo}}{I_o} = -\frac{Z_{3a}(s)}{Z_{cp}} \quad (2.117)$$

Where

$Z_{3a}(s)$ = Feedback impedance of OPAMP

Z_{cp} = Impedance of CP

V_{fo} = Output voltage of filter

I_o = Constant current

Above transfer functions and their component values have been incorporated with their respective algorithms to find optimum result.

Algorithm for proposed configurations:

There are few algorithms which are used to calculate phase noise at various points using passive 3 poles topology:

The algorithms of various components like reference chain PN, reference input PN, divider PN, VCO PN, VCO free running PN, and total PN have been described as below:

Reference chain phase noise is the type of noise which can be calculated by reference divider and reference source as:

$$Noise\ Ref\ Chain = \sqrt{VCO_{out} \times (Ref_{src1})^2 + VCO_{out} \times (Ref\_Div_{src2})^2} \quad (2.118)$$

and phase noise of reference can be determined after taking its logarithm as:

$$Ref\ Phase\ Noise = 10 \times log\ \left(0.5 \times \left(Noise_{Ref\_Chain}\right)^2\right) \quad (2.119)$$

where

VCO_{out} = Output of VCO for passive 3 poles topology

Ref_{src1} = Series components of reference source for passive 3 poles topology

Ref_Div_{src2} = Series components of divider of reference for passive 3 poles topology

Divider phase noise depends upon the output of VCO and their component is given as:

$$Div\ Phase\ Noise = 10 \times log\ (0.5 \times VCO_{out} \times (DIV_{src2})^2) \quad (2.120)$$

where

DIV_{src2} = Series components of divider for passive 3 poles topology

Here charge pump has been used as phase frequency detector; their noise can be calculated as:

$$PFD\ Phase\ Noise = 10 \times log\ (0.5 \times VCO_{out} \times (CP_{sr})^2) \quad (2.121)$$

where

CP_{sr} = Series component of charge pump for passive 3 poles topology

VCO free running is the condition when input to VCO is zero. VCO phase noise and total phase noise can be calculated using their free running condition and topology as:

$$VCO\ Free\ Run\ Phase\ Noise = 10 \times log\ (0.5\ \times (VCO\_FR\_Noise)^2) \quad (2.122)$$

$$VCO\ Phase\ Noise = 10 \times log\ (0.5 \times VCO_{out} \times (VCO_{src1})^2) \quad (2.123)$$

$$Total\ Phase\ Noise = 10 \times log\ (0.5 \times (VCO_{outnoise})^2) \quad (2.124)$$

where

VCO_FR_Noise = VCO free running phase noise for passive 3 poles topology

VCO_{src1} = Series components of VCO for passive 3 poles topology

$VCO_{outnoise}$ = Output of VCO noise for passive 3 poles topology

Considering above algorithms, their corresponding results have been presented in the results section.

The algorithms of various components have been described using passive 4 poles topology as below:

Reference chain and reference phase noise are the noise which can be determined using algorithm:

$$Noise\ Ref\ Chain = \sqrt{VCO_{out} \times (Ref_{src1})^2 + VCO_{out} \times (Ref\_Div_{src2})^2} \quad (2.125)$$

$$Ref\ Phase\ Noise = 10 \times log\ \left(0.5 \times \left(Noise_{Ref\_Chain}\right)^2\right) \quad (2.126)$$

where

VCO_{out} = Output of VCO for passive 4 poles topology

Ref_{src1} = Series components of reference source for passive 4 poles topology

Ref_Div_{src2} = Series components of divider of reference for passive 4 poles topology

Divider phase noise for passive 4 poles topology depends upon the product of VCO output, divider noise, and their logarithm as:

$$Div\ Phase\ Noise = 10 \times log\ (0.5 \times VCO_{out} \times (DIV_{src2})^2) \quad (2.127)$$

where

DIV_{src2} = Series components of divider for passive 4 poles topology

Phase frequency detector noise for passive 4 poles topology can be calculated as follows:

$$PFD\ Phase\ Noise = 10 \times log\ (0.5 \times VCO_{out} \times (CP_{sr})^2) \quad (2.128)$$

where

CP_{sr} = Series component of charge pump for passive 4 poles topology

The condition in which input to VCO is zero is called VCO free running condition. For calculating VCO phase noise and total phase noise, the algorithms as:

$$VCO\ Free\ Run\ Phase\ Noise = 10 \times log\ (0.5\ \times (VCO\_FR\_Noise)^2) \quad (2.129)$$

$$VCO\ Phase\ Noise = 10 \times log\ (0.5 \times VCO_{out} \times (VCO_{src1})^2\ ) \quad (2.130)$$

$$Total\ Phase\ Noise = 10 \times log\ (0.5 \times (VCO_{outnoise})^2\ ) \quad (2.131)$$

where

VCO_FR_Noise = VCO free running phase noise for passive 4 poles topology

VCO_{src1} = Series components of VCO for passive 4 poles topology

$VCO_{outnoise}$ = Output of VCO noise for passive 4 poles topology

Considering above algorithms, their corresponding results have been presented in the results section.

The algorithms of various components have been described using active 3 poles topology as below and their corresponding results have been incorporated in results section.

Reference phase noise is the main noise which changes output of the PLL. The algorithms for the reference and reference chain are given as:

$$Noise\ Ref\ Chain = \sqrt{VCO_{out} \times (Ref_{src1})^2 + VCO_{out} \times (Ref\_Div_{src2})^2} \quad (2.132)$$

$$Ref\ Phase\ Noise = 10 \times log\ \left(0.5 \times \left(Noise_{Ref\_Chain}\right)^2\ \right) \quad (2.133)$$

where

VCO_{out} = Output of VCO for active 3 poles topology

Ref_{src1} = Series components of reference source for active 3 poles topology

Ref_Div_{src2} = Series components of divider of reference for active 3 poles topology

Divider compensates high frequency ratio for further processing. Its noise for active 3 poles topology depends upon the VCO output and divider noise.

$$Div\ Phase\ Noise = 10 \times log\ (0.5 \times VCO_{out} \times (DIV_{src2})^2) \quad (2.134)$$

where

DIV_{src2} = Series components of divider for active 3 poles topology

Besides active components, more poles have been added to minimize the noise. Phase frequency detector noise for active 3 poles topology can be calculated as:

$$PFD\ Phase\ Noise = 10 \times log\ (0.5 \times VCO_{out} \times (CP_{sr})^2) \quad (2.135)$$

where

CP_{sr} = Series component of charge pump for active 3 poles topology

VCO is the main component that controls feedback loop of the PLL. Its free running condition and total PN of PLL are determined. An algorithm is employed to compute VCO PN and total PN.

$$VCO\ Free\ Run\ Phase\ Noise = 10 \times log\ (0.5\ \times (VCO\_FR\_Noise)^2) \quad (2.136)$$

$$VCO\ Phase\ Noise = 10 \times log\ (0.5 \times VCO_{out} \times (VCO_{src1})^2) \quad (2.137)$$

$$Total\ Phase\ Noise = 10 \times log\ (0.5 \times (VCO_{outnoise})^2) \quad (2.138)$$

where

VCO_FR_Noise = VCO free running phase noise for active 4 poles topology

VCO_{src1} = Series components of VCO for active 3 poles topology

The advanced filter (active & passive components) topology has been incorporated with CP and oscillator to suppress noise at output. Above algorithms and design configurations have been incorporated with their results in the next section.

2.7 DESIGN EXAMPLE OF PROPOSED CONFIGURATION OF THE PLL

The analysis of new configuration approaches is important to predict different values. The results of various configurations have been presented in next sub sections.

2.7.1 Simulation results of phase noise response of synthesizer using a charge pump detector with passive 3 poles

The specifications for passive 3 poles are as follows:

- $C_1 = 44.42$ pF
- $C_2 = 7.8\,58$ nF
- $R_1 = 2.658$ kΩ
- Charge pump current $(I_d) = 0.001$ A
- VCO timing coefficient ratio $(K_v) = 24$ MHz

Simulation results of synthesizer using a charge pump detector are as follows.

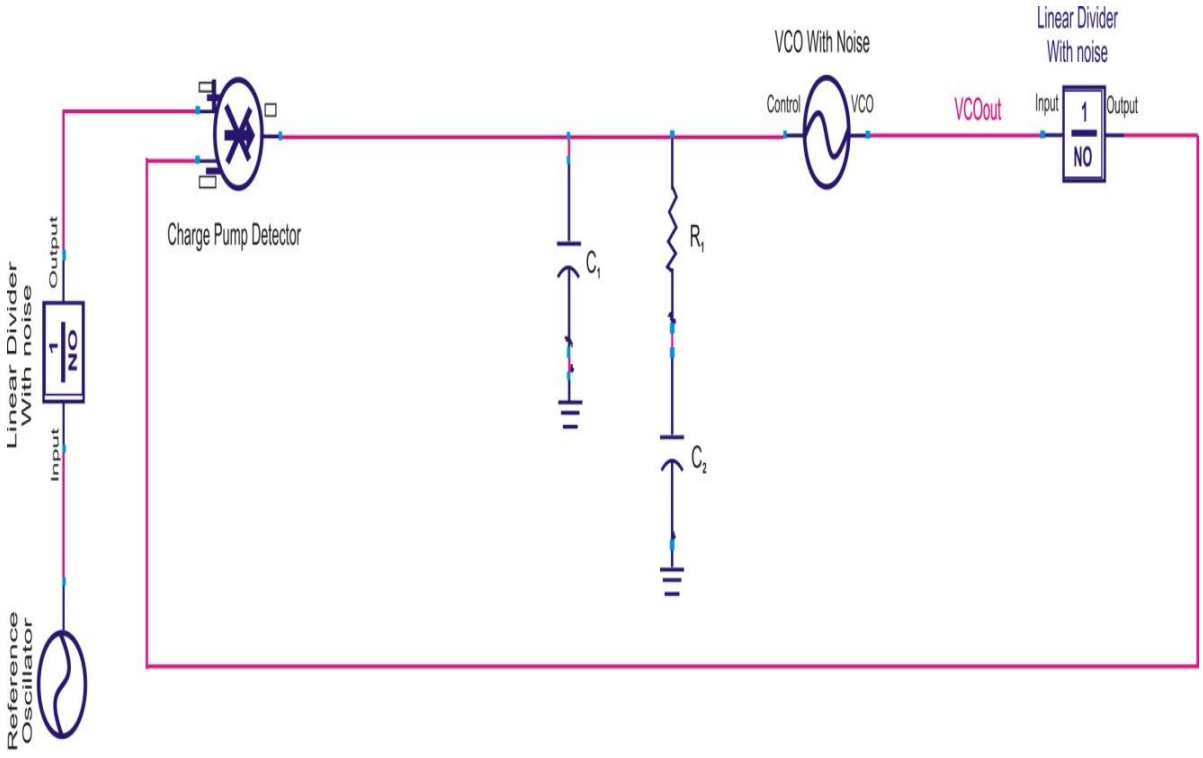

Figure 2.13: Synthesizer using charge pump with passive 3 poles

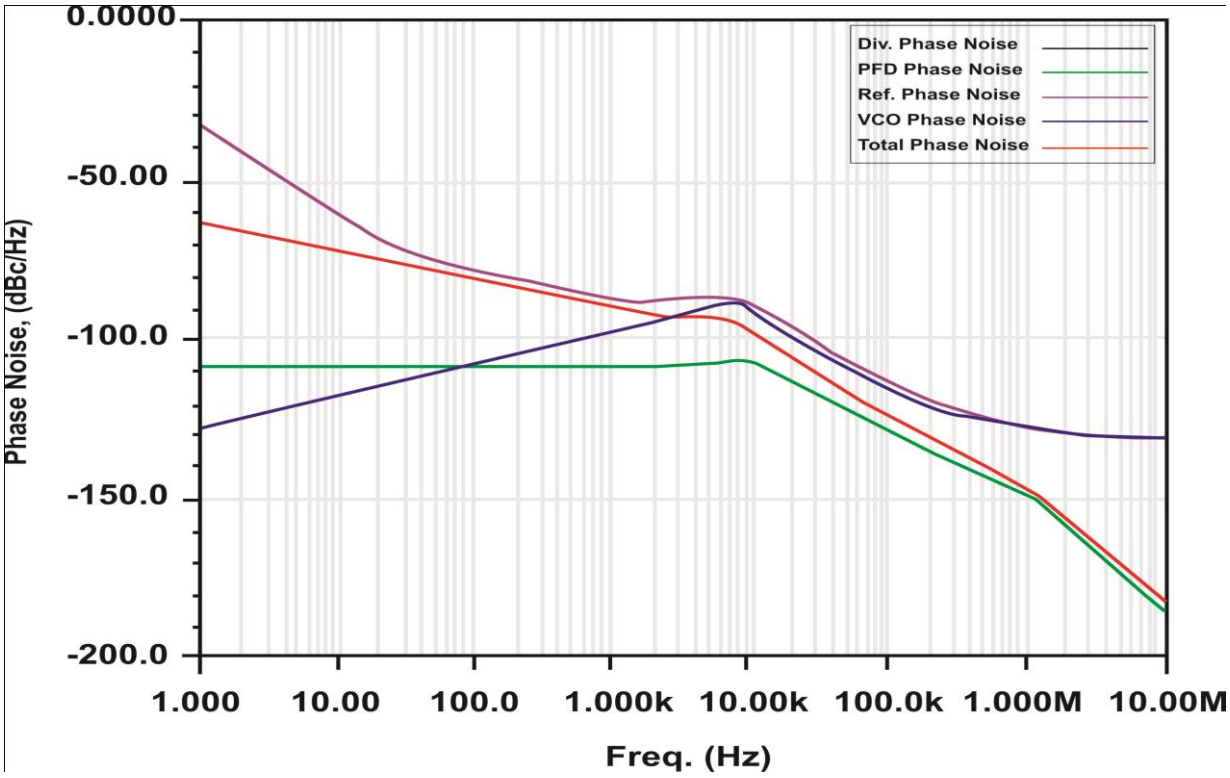

Figure 2.14: Contributions to VCO phase noise with passive 3 poles

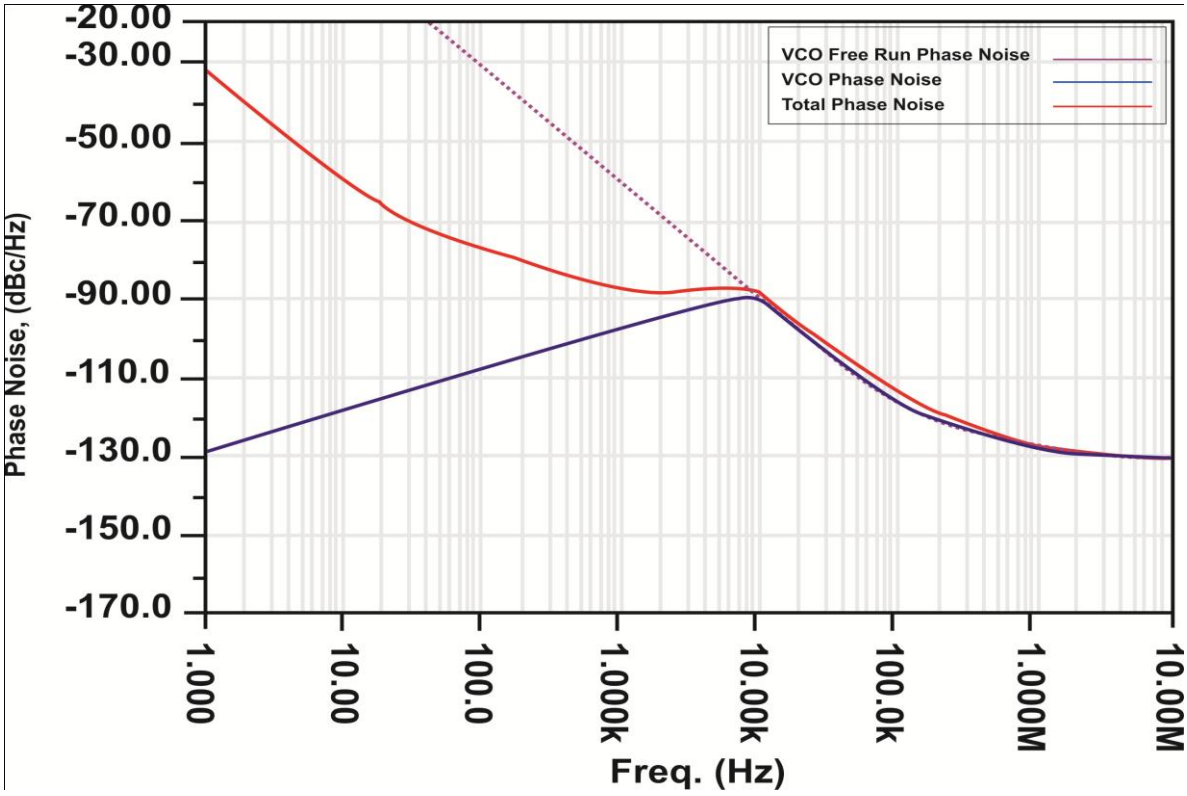

Figure 2.15: Loop reductions of VCO phase noise with passive 3 poles

The results have been analyzed to check the performance of system. The system will track VCO output frequency and reference input frequency inside or outside loop band width. Figures 2.13, 2.14, & 2.15 show phase noise detection with passive 3 poles. The results found that total phase noise at various offset frequencies like – 29.94 dBc/Hz when frequency is 1 Hz, – 76.55 dBc/Hz when frequency is 100 Hz & – 112.59 dBc/Hz when frequency is 100 kHz. This work provides better results because the architecture included charge pump phase detector with passive 3 poles filters topology. This topology reduces phase noise of various components of PLL as shown in figures 2.14 and 2.15.

2.7.2 Simulation of phase noise response of synthesizer using a charge pump detector with passive 4 poles

The specifications for passive 4 poles are as follows:

- $C_1 = 40\ pF$
- $C_2 = 6.2\ nF$
- $C_3 = 76.2\ pF$
- $R_1 = 2.67\ k\Omega$
- $R_2 = 3.8\ k\Omega$
- Charge pump current $(I_d) = 0.001\ A$
- VCO timing coefficient ratio $(K_v) = 0.001\ MHz$

Simulation results of synthesizer using a charge pump detector are as follows.

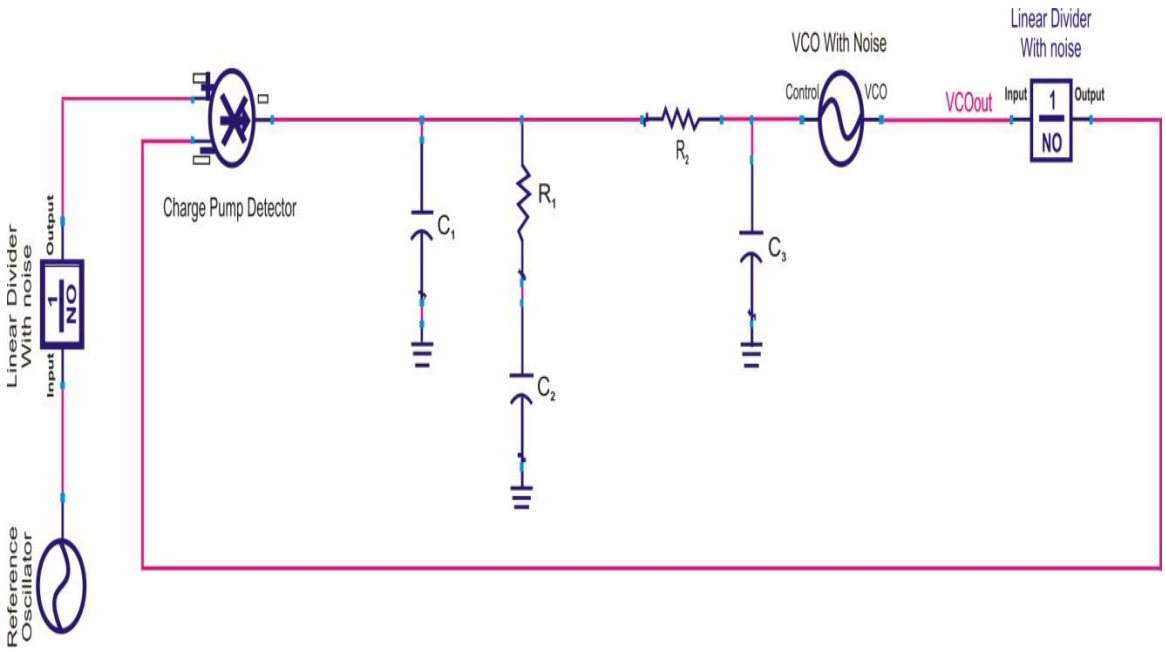

Figure 2.16: Synthesizer using charge pump with passive 4 poles

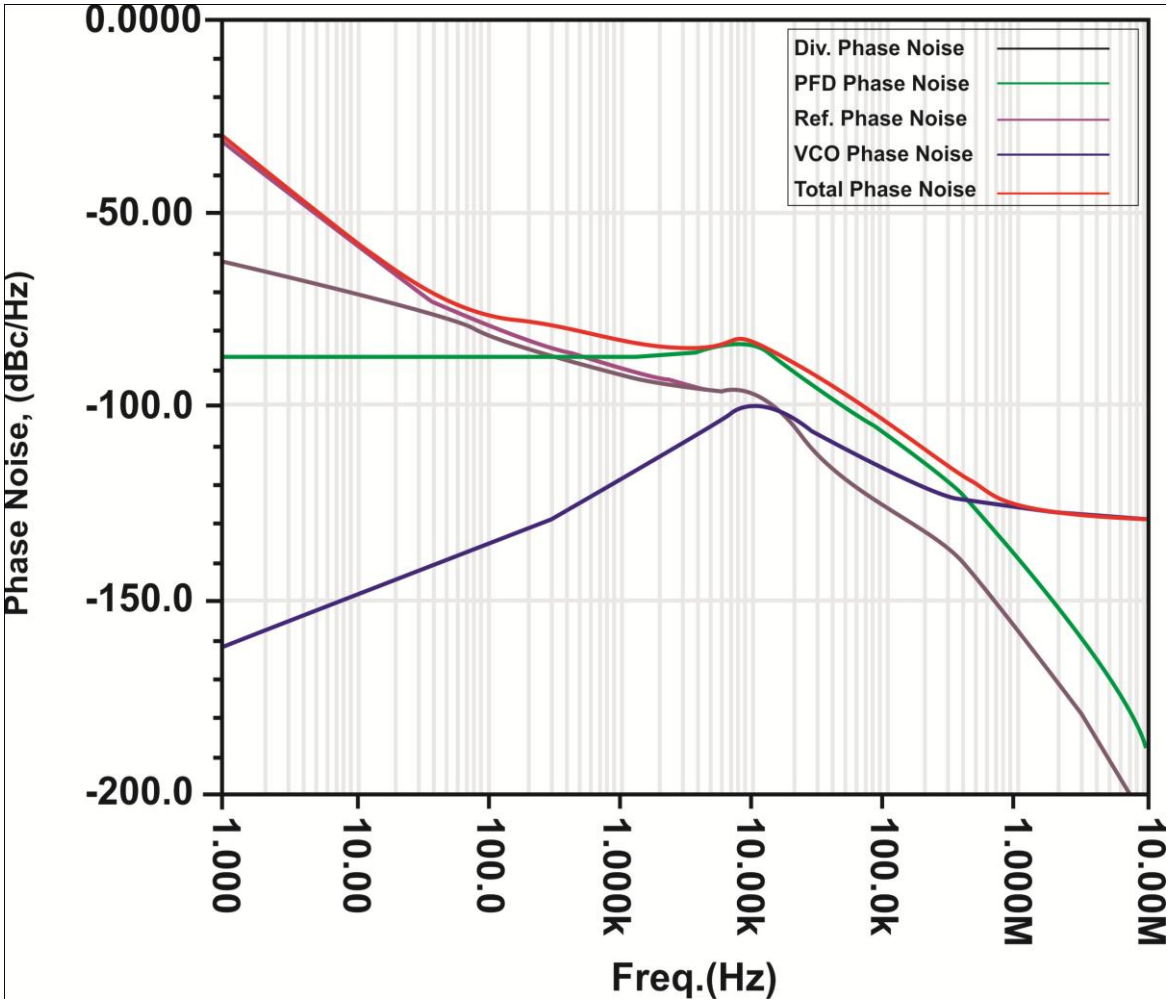

Figure 2.17: Contribution to VCO phase noise with passive 4 poles

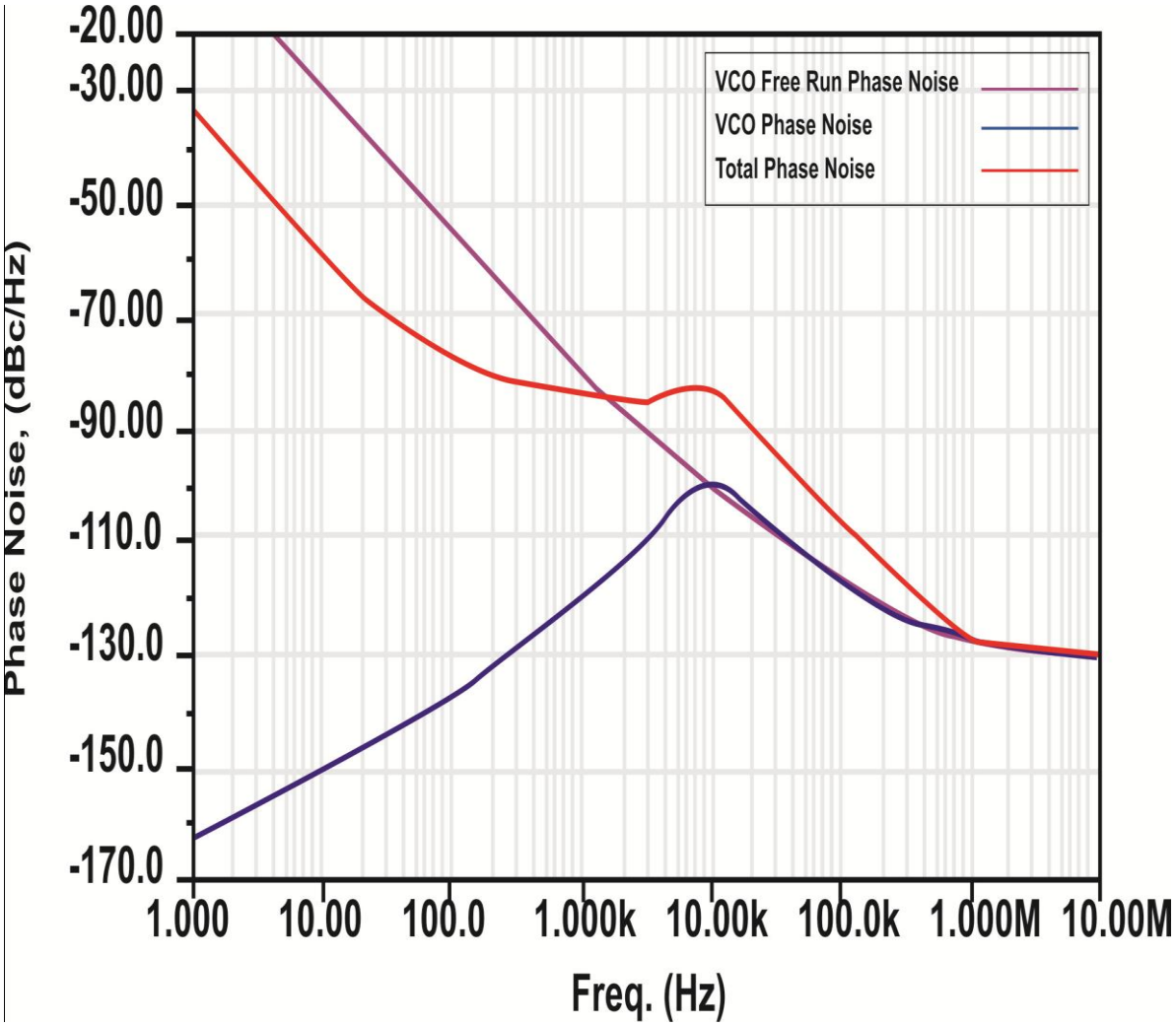

Figure 2.18: Loop Reduction of VCO phase noise with passive 4 Poles

Figures 2.16, 2.17, & 2.18 show phase noise detection with passive 4 poles. The results found total phase noise at various offset frequencies like – 29.94 dBc/Hz at 1 Hz, – 76.18 dBc/Hz at 100 Hz and – 105.96 dBc/Hz at 100 kHz. Here one more pole has been added into the previous architecture to minimize PN of the system. This work gives superior results because this architecture used charge pump based phase detector with passive 4 poles filters topology.

2.7.3 Simulation of phase noise response of synthesizer using a charge pump detector with active 3 poles

The specifications for active 3 poles are as follows:

- $C_1 = 1.076\ nF$
- $C_2 = 100\ nF$
- $R_1 = 11.52\ k\Omega$
- Charge pump current $(I_d) = 0.003\ A$
- VCO timing coefficient ratio $(K_v) = 3.37\ MHz$

Simulation results of synthesizer using a charge pump detector are as follows.

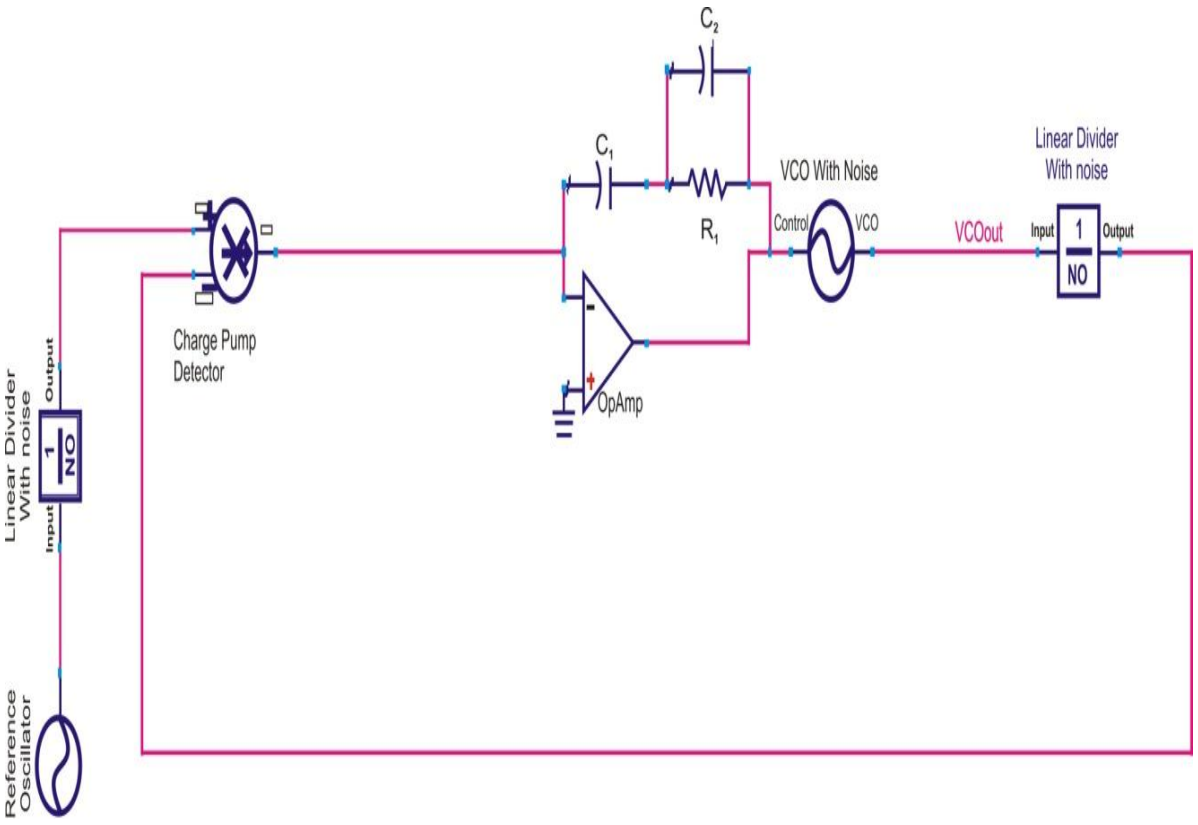

Figure 2.19: Synthesizer using charge pump with active 3 poles

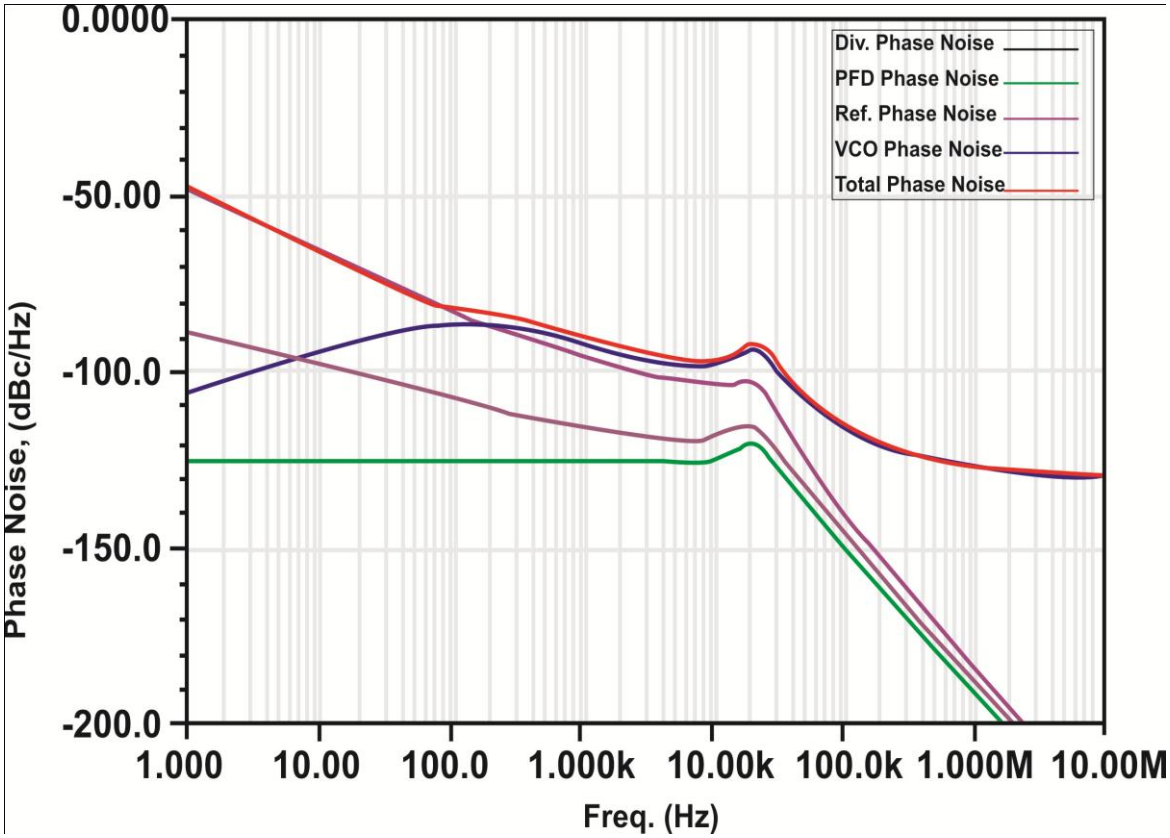

Figure 2.20: Contribution to VCO phase noise with active 3 poles

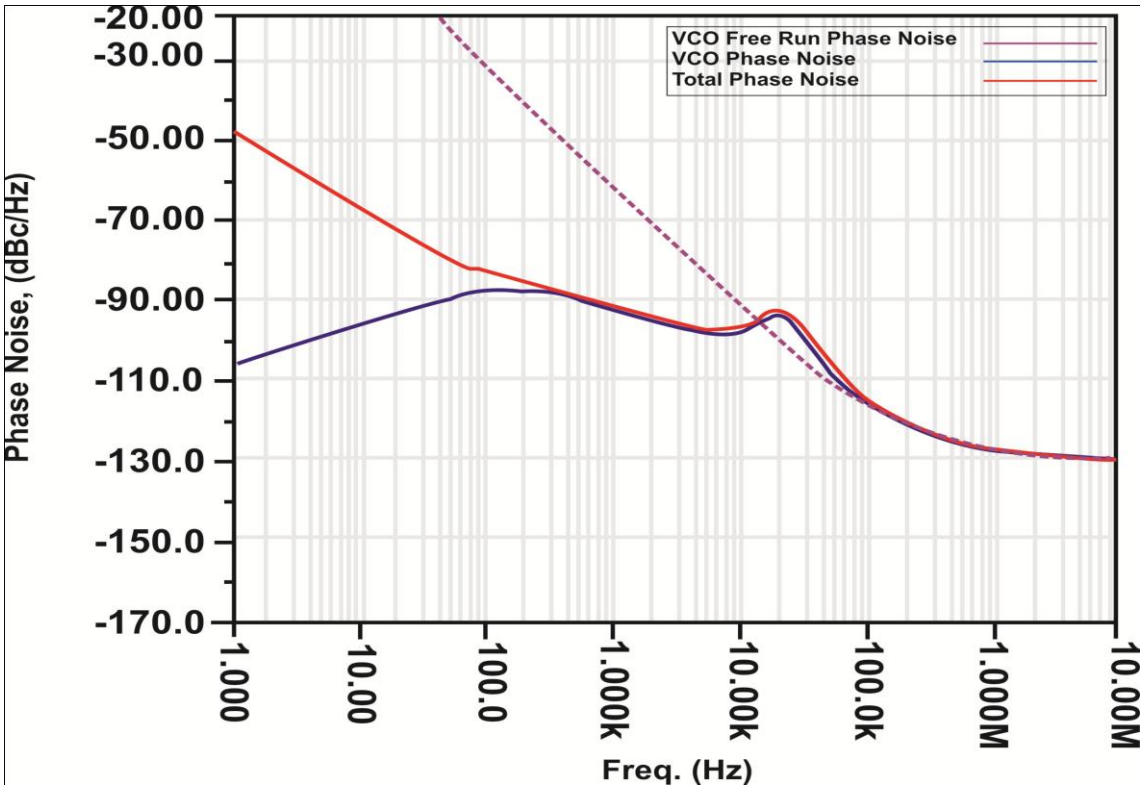

Figure 2.21: Loop reduction of VCO phase noise with active 3 poles

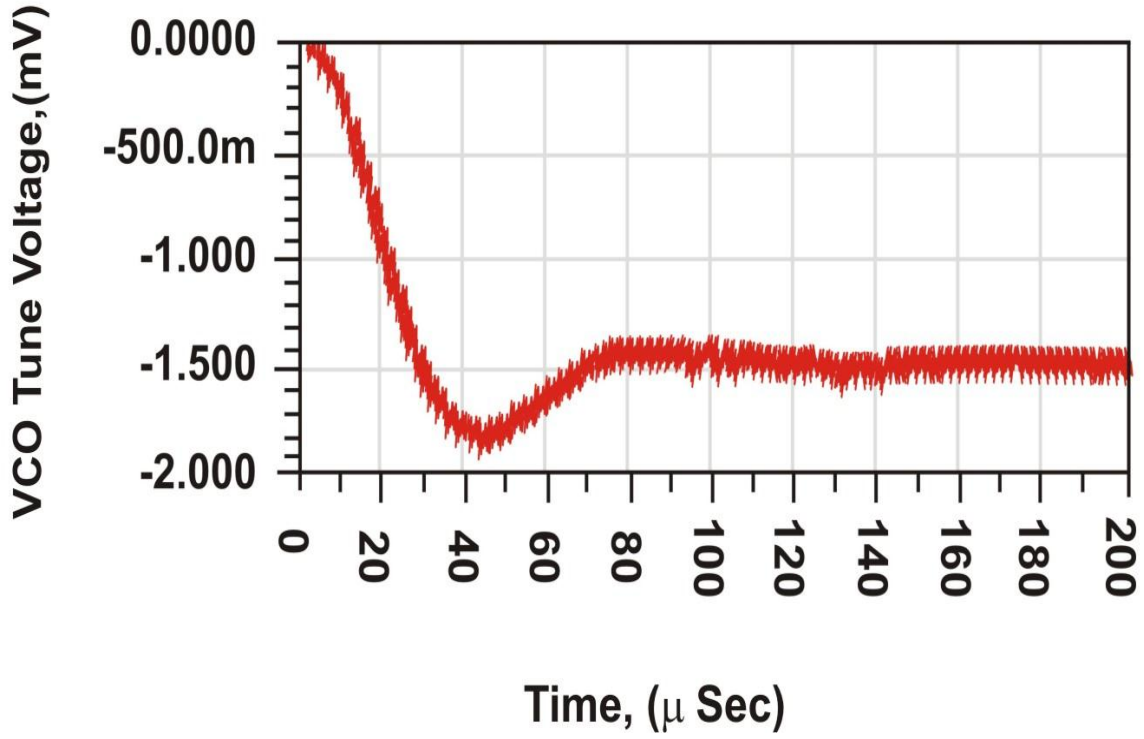

Figure 2.22: Transient response of VCO tune using charge pump with active 3 poles

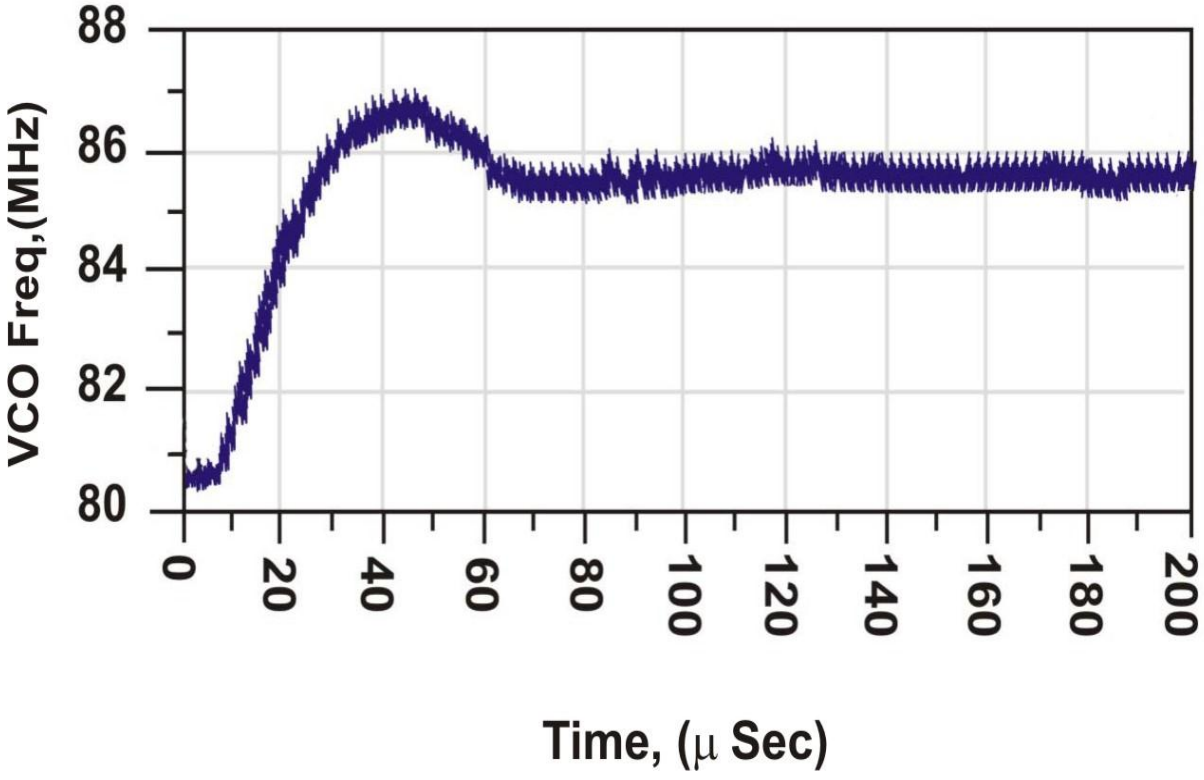

Figure 2.23: Transient response of VCO frequency using charge pump with active 3 poles

Active filter is most important component in the system. In this work, composite block of charge pump and active 3 poles filter have been used which suppresses noise. Its noise effects already have been analyzed. Figures 2.19, 2.20, & 2.21 show phase noise detection of active 3 poles.

Table 2.2: Initial values of different components

Description	Passive 3 pole	Active 3 pole	Passive 4 pole
Charge pump	6.283 µV	1.012 µV	62.83 µV
Loop Div (SRC2)	1.244 mV	64.18 µV	1.244 mV
Resistors	2.651 nV	11.02 nV	2.096 nV,2.517 nV
RefDiv (SRC1)	1.244 mV	---	1.244 mV
Ref (SRC1)	30.66 mV	5.778 mV	30.66 mV
VCO (SRC1)	660.7 nV	9.464 µV	16.81 nV
VCO (SRC4)	0 V	0 V	0 V
AMP	----	2.613 µV	----
Total	30.71 mV	5.778 mV	30.71 mV

Table 2.3: Comparative results of overall noise performance

Frequency(Hz)	Passive 3 pole(dBc/Hz)	Passive 4 pole(dBc/Hz)	Active 3 pole(dBc/Hz)
1.00 Hz	-29.948	-29.948	-45.63
10.00 Hz	-58.860	-58.853	-65.79
100.00 Hz	-76.553	-76.188	-82.13
1.00 kHz	-86.338	-86.332	-97.24
10.00 kHz	-87.962	-87.944	-102.41
100.00 kHz	-112.597	-105.960	-139.62

The results show that total phase noise at various offset frequencies like -45.63 dBc/Hz at 1 Hz, -82.13 dBc/Hz at 100 Hz and -139.62 dBc/Hz at 100 kHz. The initial set of values for proposed system is given in table 2.2. The unchanged settling time for proposed system are shown in figures 2.22 and 2.23, which depict stability of system. The system regains its stability after the time of 130 μ Sec at frequency 45.7 MHz of VCO as shown in figure 2.23. From the comparison of various results, it has been found that charge pump detector with active 3 poles technique is better than other technique. The comparison of overall noise performance of PLL is given in table 2.3. The results obtained show that active 3 poles configuration has less phase noise than any other. The work has investigated the causes of phase noise and has provided an accurate model of how to predict it. Finally, simulation results showed the improved performance of the proposed architecture.

2.7.4 Comparison of proposed architecture with the existing loop filter architectures

In this section, a new architecture has been compared with the existing architecture. Resistors and capacitors are the building blocks of passive filter. The prime capacitor may be too wearisome for integration and moreover the frequencies of zero and pole are prone to process deviation. Active filters are relatively more flexible and can provide superior tuning choice on the cost of more power consumption and induction of active noise. Factor of current or resistance ratios scale down the prime capacitor being used in passive filter.

Table 2.4: Comparison of existing loop filter architectures

Architecture	Silent features	Performance	Remark
Passive	R & C	No active noise	Large C
Active	OPAMP	Large voltage, more flexibility	More power, active noise
Dual-path [99]	OPAMP	Smaller C	More power, active noise
Sample-reset [100]	Two charge pump, OPAMP	Less ripple, smaller C, less sensitivity	More power, active noise, clock feed through, charge sharing
Proposed work	R, C, charge pump, OPAMP	Less noise, more flexibility	More power, charge sharing

The resistor can be replaced by a switched capacitor, and it introduces some loop factors which depend upon the capacitance ratios and is less vulnerable to process variation. On the other hand, switched capacitors initiate clock feed-through and charge sharing. Assessment of various loop filter designs has been presented in the table 2.4. Finally, it has been found that proposed architecture is better than other existing architectures.

2.8 SUMMERY OF THE CHAPTER

This work proposed PLL frequency synthesizer to reduce phase noise which can be used in GSM applications. The transfer functions of individual source noise and output phase noise have been calculated with their parameters. A new architecture has been proposed based on performed analysis, and reduced phase noise using simulation tool. The results show improved performance of the proposed architecture as compared with any other existing techniques. In the next chapter, the effect of time sharing of clock on LUT for DDS has been presented.

CHAPTER 3

THE PERFORMANCE OPTIMIZATION OF DDFS BY A NOVEL APPROXIMATION TECHNIQUE

3.1 INTRODUCTION

The chapter focuses on analysis and design techniques for direct digital frequency synthesizer (DDFS). Read only memory (ROM) compression algorithm has been presented to optimize DDFS using piecewise linear approximation. The proposed technique allows successive read access to memory cells per one clock cycle using time sharing. The output values will be temporarily stored and read at a later time. The desired waveform has been approximated to get reconstructed signal of the output. In this work, a new design technique has also been proposed for DDFS based on Lagrange interpolation and modified quasi linear methods.

DDFS is a device that is generally used to generate sine wave for various applications at different frequencies for various applications. It is also regarded as being the most suitable for portable low battery drains transceivers. It is capable of being incorporated with different digital modulations by using digital processing methods. Mixed signal processing blocks and digital information are incorporated with reference input to generate required wave. It holds an important position in modern electronics science and engineering. Their requirement in digital communication systems can hardly be underestimated. The parameters like frequency resolution, good spectral purity, and fast switching have also been analyzed.

This digital frequency synthesis also provides a stable source of frequency to describe time for the sampled values for the look-up table. Later on, these samples are converted

into analog signal after filtering. DDFS consists of phase accumulator (PA), ROM, and digital/analog converter (DAC). Frequency word of PA determines the periodicity of the accumulator. The values of PA are varied in accordance with the tuning or control word at each clock. The output of PA is fed to ROM for further process. After that, output of memory is converted into analog signal by DAC converter. The length of PA determines the size of the ROM. If the length of the PA is large, ROM becomes large. This will consume more power and reduces the speed of the system. To minimize size of ROM, various techniques have been presented by researchers. Therefore, an exhaustive literature survey has been carried out related to the titled work to find out the current research which has been mentioned in the literature review.

Besides this, other techniques like trigonometric identity and Nicholas methods are used to analyze and implement ROM compression techniques in [101] - [105]. In this section, from the literature review, it is clear that there is need to introduce a new technique to access more memory space in less time and minimize noise at high-speed for communication system. Details of the basic components have been presented in the next section.

3.2 CONVENTIONAL DDFS ARCHITECTURE

Direct digital frequency synthesizer includes PA, LUT, and DAC that is shown in figure 3.1. The PA is controlled by clock. Phase of the accumulator is accumulated by each clock to address ROM.

The phase is converted into corresponding amplitude of the signal. This address of ROM is fed to DAC to produce analog signal. The various components have been analyzed in next sub-section.

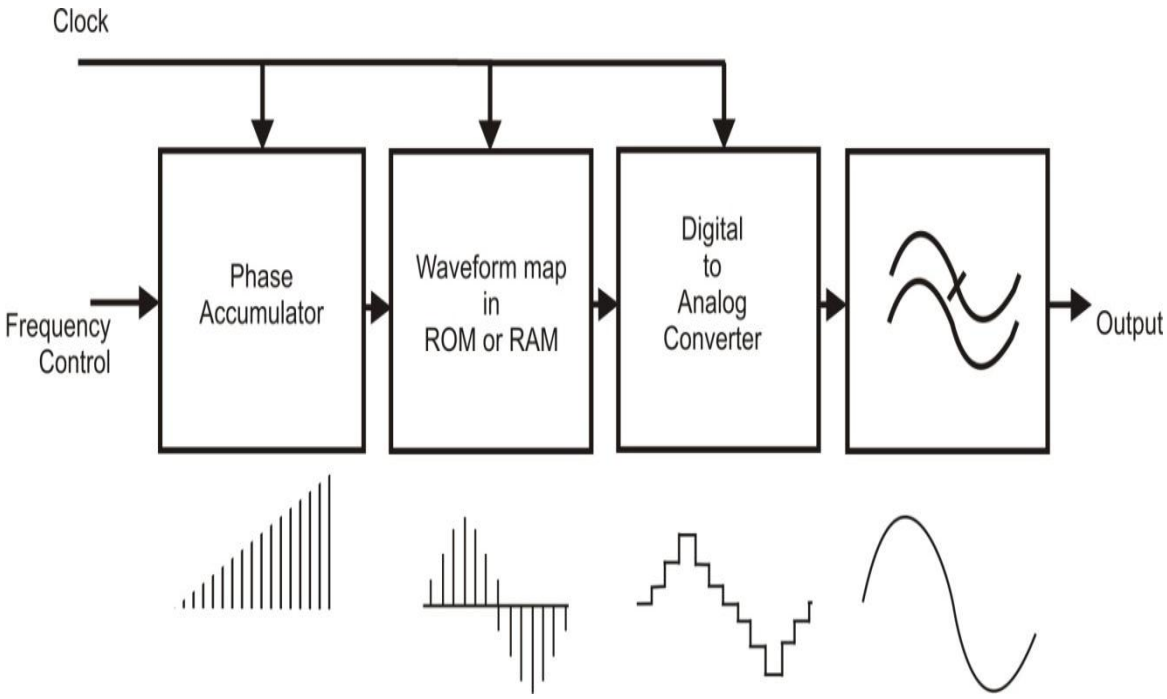

Figure 3.1: Block diagram of DDFS

3.2.1 Phase Accumulator (PA)

Phase accumulator (PA) is a device which is used to convert sinusoidal signal into repetitive phase angular (range 0 to 360 degrees). PA works as modulo M counter to store number and increases it after receiving a clock pulse. The resolution of PA determines discrete phase point on the wheel of DDFS. The tuning equation for the output is given as:

$$f_{out} = \frac{FIW}{2^M} f_c \quad (3.1)$$

Where

f_{out} =Frequency output

FIW = Frequency input word

f_c = Clock frequency

M = Accumulator length

T = Clock period

Output frequency depends upon frequency input word and accumulator length.

The accumulator output is given as:

$$S(n) = S(n-1) + FIW \tag{3.2}$$

where,

$S(n)$ = Accumulator output

n = Clock tick

3.2.2 Phase-Amplitude Converter (PAC)

A PAC is a device that is used to convert digital phase into its corresponding amplitude. It takes input from the accumulator and generates corresponding output amplitude for the look-up table. This output is in the form of phase of wave and address to a word. The ROM converts the phase information to its amplitude presentation, i.e., performs the transformation

$$FIW\ n\ T => \sin(FIW\ n\ T) \tag{3.3}$$

where

FIW = Frequency input word

n = Clock tick

T = Clock period

The ROM serves as a look up table, converting its index (phase) input to sine amplitude samples.

3.2.3 Digital/Analog Converter (DAC) and Loop Filter

DAC is the device that converts digital value to its corresponding analog voltage or current. Output of the ROM (or the multiplier) is then connected to a DAC that transforms all the digital information to an analog signal. Note that the DAC is not directly generating the analog output. It uses delta function which follows sample-and-hold technique for the conversion, is given by

$$\frac{\sin \pi f T}{\pi f T} \tag{3.4}$$

and the power spectrum by

$$\left(\frac{\sin \pi fT}{\pi fT}\right)^2 \tag{3.5}$$

where

f = Frequency

T = Time period

Filters are the circuits that execute signal processing functions, particularly to get rid of unwanted frequency components from the signal and to improve quality of desired signals. Now compression techniques have been analyzed in the next section.

3.3 QUADRANT COMPRESSION TECHNIQUE

There are many other compression technique like direct Taylor approximation, Hutchison algorithm, variations and randomization, auxiliary function ROM approximation, and coordinate transformation compression techniques. These techniques may be adapted to compress the ROM size Out of these techniques quadrant compression technique is generally used for compression of the same. This technique reduces ROM size by more than 75% by taking advantage of the fact that only one quadrant of sine (cosine) needs to be stored since sine (cosine) has symmetric property as shown in figure 3.2.

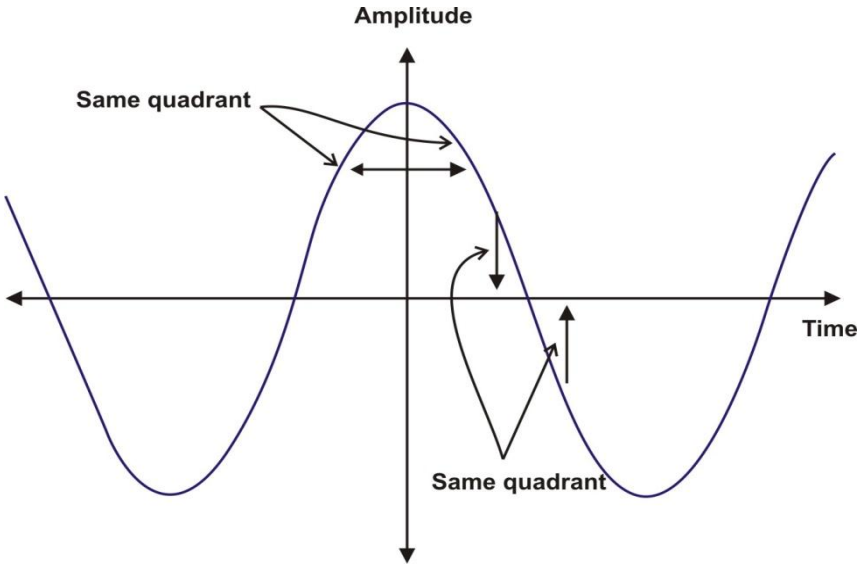

Figure 3.2: Sine quadrant symmetry

Table 3.1: Quadrants Table

Phase	MSB	MSB-1	Sine
$0^0 < A < 90^0$	1	0	$sin\, A$
$90^0 < A < 180^0$	1	1	$sin(90^0 - A)$
$180^0 < A < 270^0$	0	0	$-sin\, A$
$270^0 < A < 360^0$	0	1	$-sin(90^0 - A)$

Thus, for

$0^0 \leq \alpha \leq 90^0, sin(90^0 - \alpha) = sin(90^0 + \alpha)\,, sin(270^0 - \alpha) = sin(270^0 + \alpha)$

$sin(\alpha) = sin(-\alpha)\, and\ \ sin(\alpha) = -sin(180^0 + \alpha)$ (3.6)

The presentation of $sin\,\alpha$ only across the first quadrant $0^0 \leq \alpha \leq 90^0$ is sufficient to reconstruct all quadrants from the first.

Where

W = Word size of the input (2^W combinations)

D = Output word

Thus the 2 MSBs of W (the input word) are needed only to control the quadrant and the values of the quadrant are needed to be manipulated as shown in table 3.1. Thus, given sin α over the first quadrant and remaining portion of sine function is given as follows:

It means that there is no need to repeat the same process for remaining quadrants.

Quadrant 1: $1/2 + 1/2 \sin$ i , i is running index from 0 to $2^{W-2} - 1$

Quadrant 2: $1/2 + 1/2 \sin$(i complemented), every bit inverted

Quadrant 3: $1/2 + 1/2 \sin$(i complemented)

Quadrant 4: $1/2 + 1/2 \sin$ i

For all quadrants, i run from 0 to $2^{W-2} - 1$

The most significant bit is inverted to output corresponding to the sine function.

ROM size is reduced by quadrant symmetry technique. It is mapped with input bits and complements the output, as shown in figure 3.3. Size of ROM is given as:

$$\frac{2^{W-2}(D-1)}{2^{W}D} = \frac{0.25(D-1)}{D} \approx 75\% \text{ saving} \quad (3.7)$$

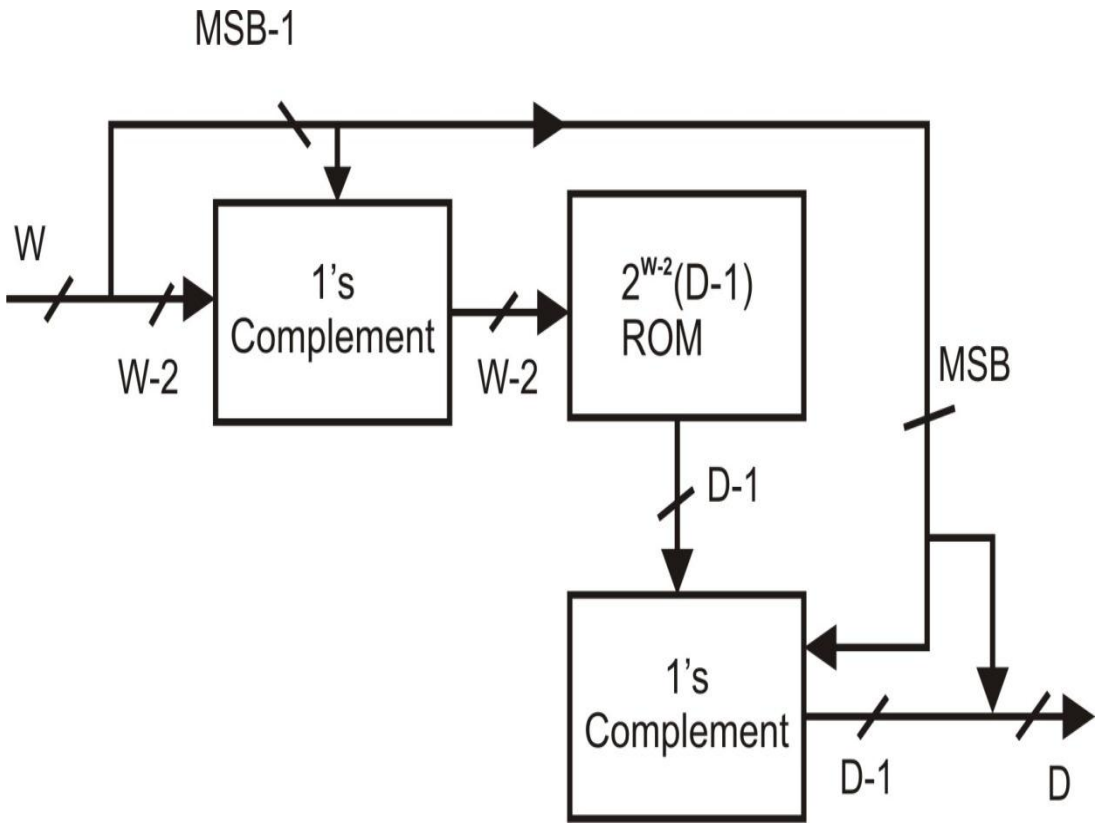

Figure 3.3: Sine quadrant compression

The emphasis is on designing the ROM compression algorithms along with paradigm equations mandatory to produce the perfect sine wave pattern for given input and output bit size. Beyond that, other methods and algorithms like trigonometric identity, Nicholas method, Taylor series, Hutchison algorithm, and CORDIC algorithm have been reviewed in [1] & [106] - [110]. This work presented and investigated a novel DDFS architecture that is based on piecewise linear method and has been described in the next section.

3.4 PIECEWISE LINEAR APPROXIMATION TECHNIQUE

A piecewise linear function consists of straight line segments in which pieces are affine functions. An approximation curve can be found by sampling the curve and interpolating linearly between the points.

Sine amplitudes should be calculated for angles in the interval [0, π/2]. The first quadrant to be approximated is:

$$Q(x) = Sin[\pi/2(x + 1/2^{W+1})] \quad (3.8)$$

Where

- x is a fraction in the interval [0, 1] and is expressed with W bits and
- $1/2^{W+1}$ equal to ½ LSB of x, is the required phase shift to exploit quadrant symmetry.

Let the quadrant of the signal is divided into $S = 2^n$ (n is the integer number) segments and each of the given segments are approximated by a linear polynomial of the form:

$$P_i(x) = V_i x + K_i + e(x_i);\ \ 1 \leq i \leq S\ , 0 \leq x \leq \Delta x \quad (3.9)$$

where,

V_i = Slope of i^{th} segment

K_i= Initial amplitude of i^{th} segment

$e(x_i)$= Error from the linear approximation

The approximated function can be written as:

$$Z(x) = \sum_{i=1}^{i=S} P_i(x) = \sum_{i=1}^{i=S} V_i x + K_i + e(x_i) \quad (3.10)$$

From the previous work, it is found that access to memory cells at a specific time was the main cause, so there is need to develop a new method to access more memory space in less time and minimize noise at high speed for communication system [111] - [114]. After

discussing the limitations of the conventional system, the proposed system has been analyzed in the next section.

3.5 PROPOSED DDFS ARCHITECHTURE BASED ON APPROXIMATION TECHNIQUE

The concept of this technique is the same as that used in quadrant compression technique in previous section. But, this new architecture replaced ROM with various components like multiplexer, adder, subtractor, and registers, which are described in detail in the next sub-section.

3.5.1 Design Approach of DDFS

The proposed technique allows successive read access to memory cells per one-clock-cycle using time sharing. The output values will be temporarily stored and read at a later time; thereby, the slope is simply derived from these sinusoidal points at successive phase angles. Flow of the input signal and selection control of quarter wave has been shown in figures 3.4 and 3.5. The most significant bit 2 (MSB2) of FIW is used to select the quadrants of sine wave, while first most significant bit (MSB1) of FIW is used to control the format converter. The remaining $W - 2$ bits are fed into 1's complement block whose output is split into two parts, MSB part with A bits long represents S segments and LSB part with B bits long represents an angle x in the interval $[0, \pi/(2S)]$. Multiplexer inputs and their coefficients are used to generate amplitudes of segments with their bits. The proposed architecture also incorporates pulse forming circuit that controls fetching and loading process of successive Q_i coefficients. The multiplexer, storage registers, subs-tractor, and adder are used to perform the task of slope derivation during segment interval.

Linear approximation is a method that is used to approximate sine function of the first quadrant. The first quadrant is divided into S straight lines with their individual coefficients P_i and Q_i. The coefficient P_i represents the slope of i^{th} element.

The first quadrant of sine function approximation segment can be calculated from the sine function as:

$$P_i = \{\sin[i\,\Delta x] - \sin[(i-1)\,\Delta x]\}/\Delta x\,,\ 1 \leq i \leq S \qquad (3.11)$$

Where,

Δx = Segment length

$sin[i\,\Delta x]$ = Successive phase angles.

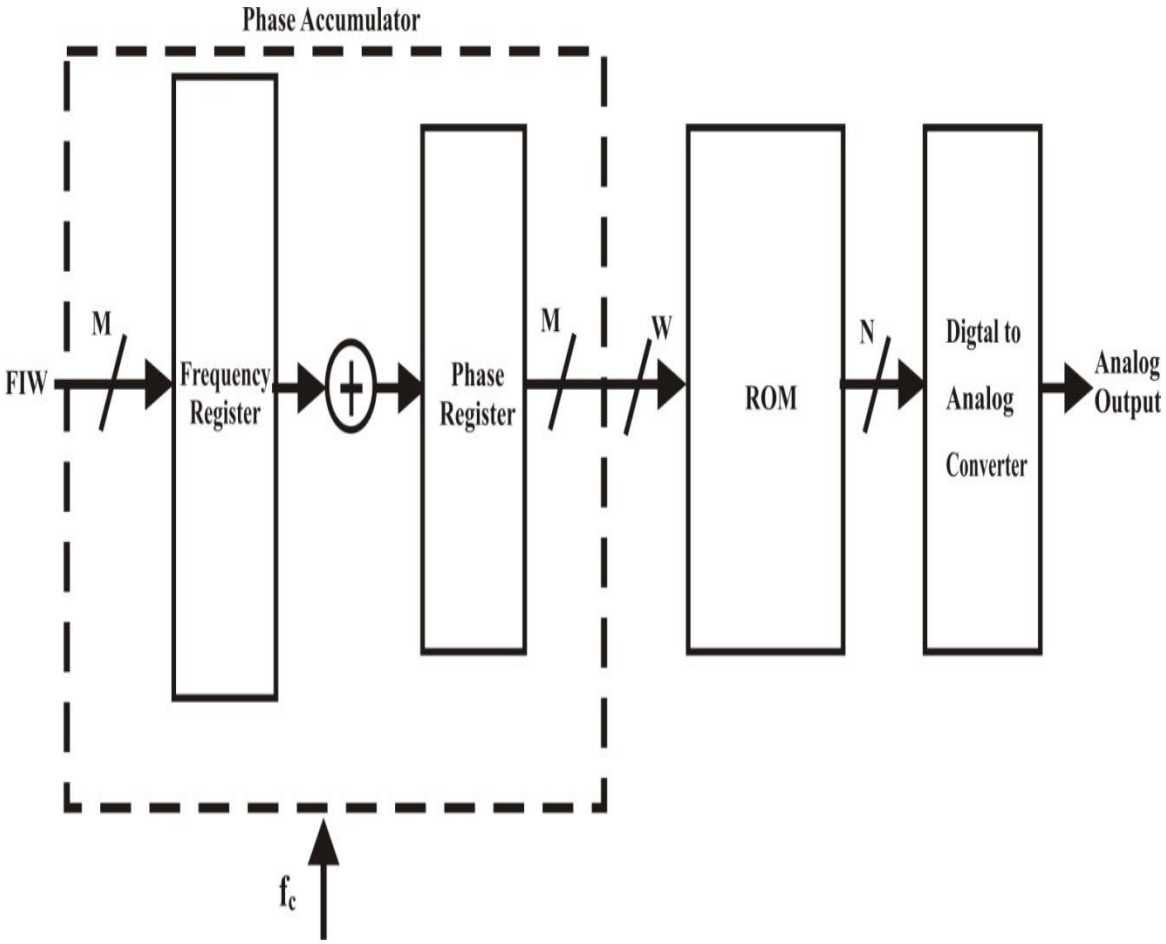

Figure 3.4: Data flow architecture of DDFS

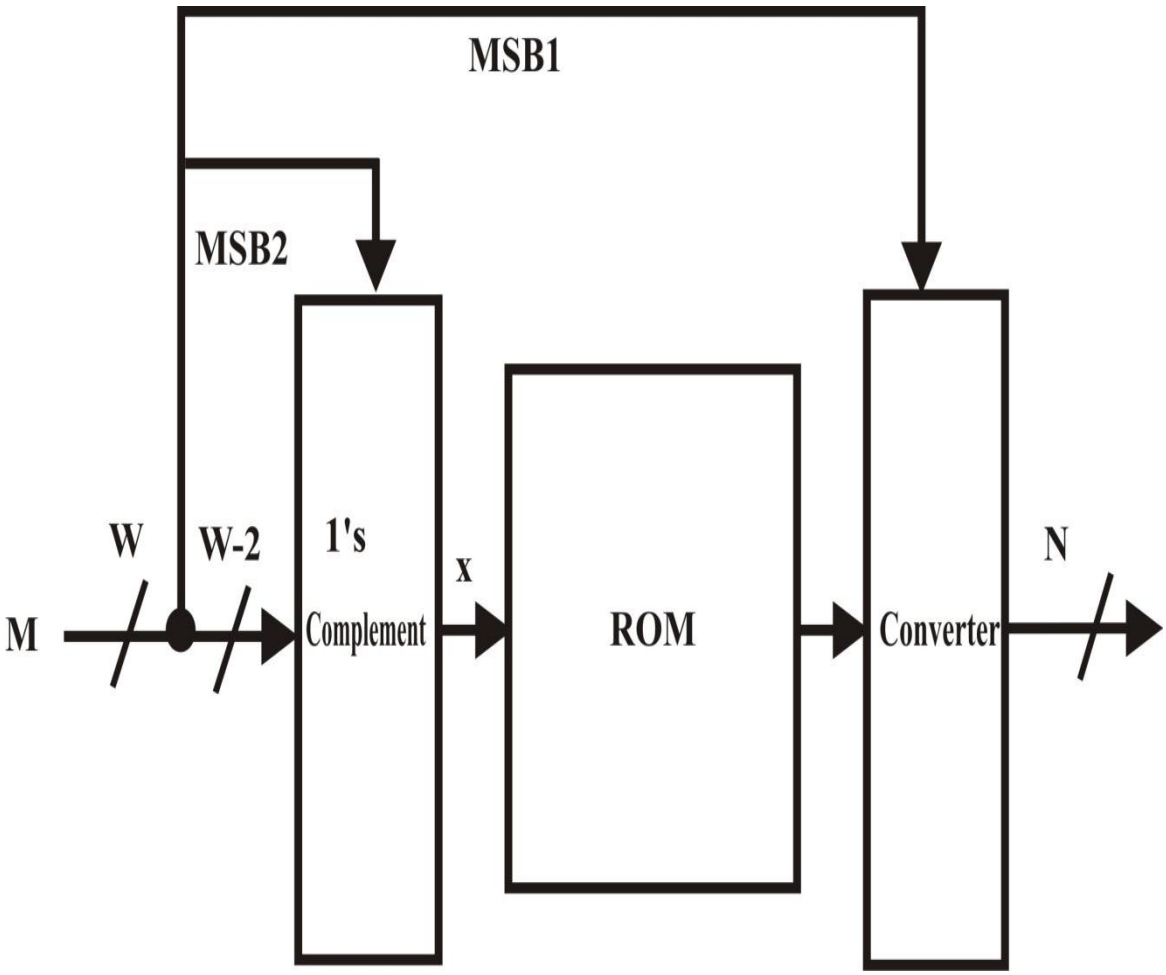

Figure 3.5: Quarter wave symmetry

For example second slope can be calculated as:

$$M_2 = P_2 x + K_2 \quad (3.12)$$

$$P_2 = (sin\, 2\Delta x - sin\, \Delta x)/\Delta x \;\; , K_2 = sin\, \Delta x \quad (3.13)$$

As Δx is unsigned constant coefficient, the division can simply be realized by binary operation. The coefficients Q_i is equal to $sin[(i-1)\,\Delta x]$ points, and for segment number 1, $(Q_1 = 0)$, yields $M_1 = P_1 x$, and for segment number 2 , $(Q_1 = sin\, \Delta x)$, in general, $(Q_i = sin[(i-1)\,\Delta x)]$ for the i^{th} segment, and it can be realized by delaying the pervious $sin(i\,\Delta x)$ by one clock period, hence realization of the whole M_i function is accomplished as shown in figure 3.6.

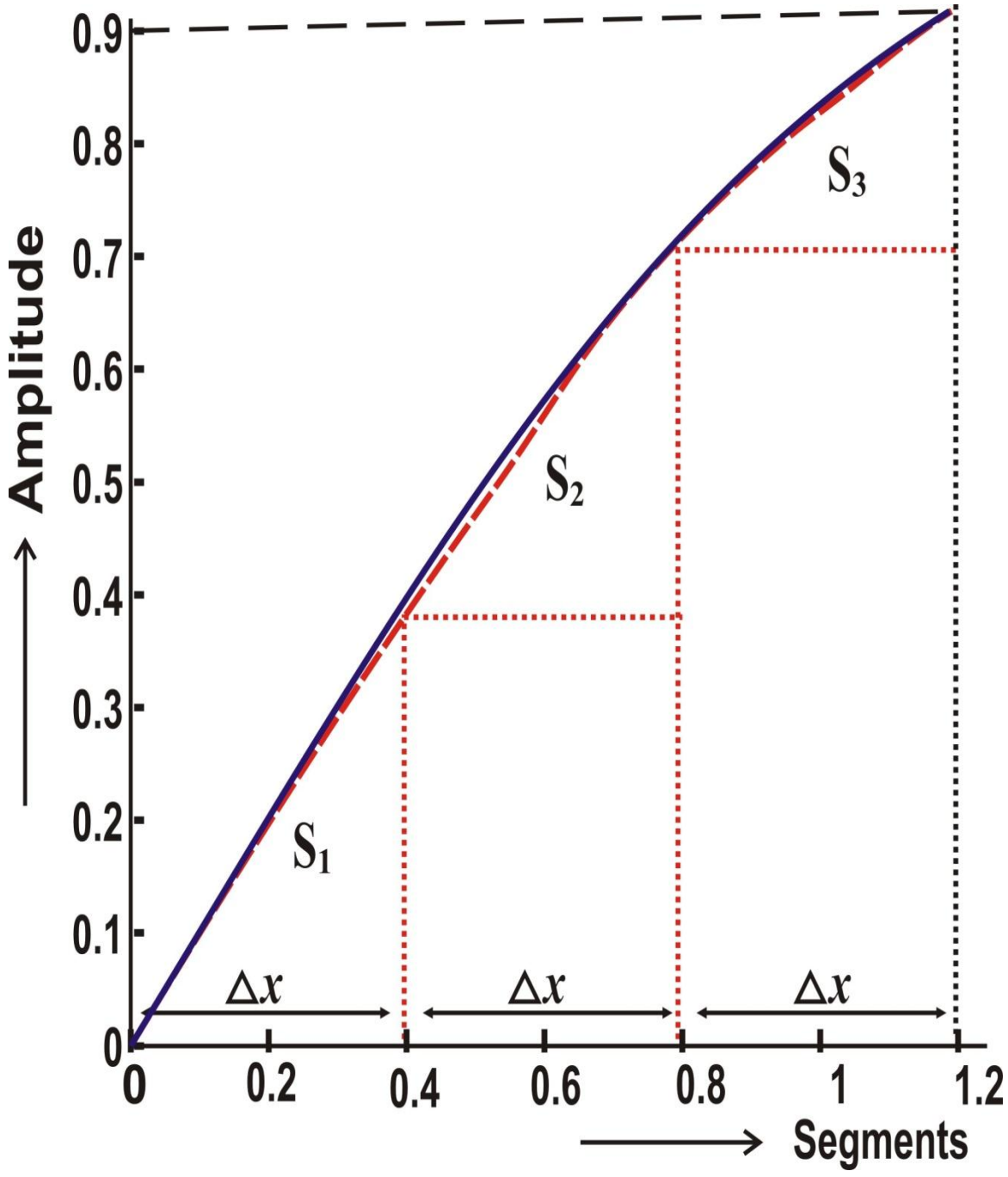

Figure 3.6: Sample of segments

It is clear that it must get two consecutive sine points at the same time to conduct the process of subtraction and extraction of the slope later. These two sine points can be

obtained only when the corresponding phase angles point simultaneously to their addresses in the sine LUT and that is an inconsequent assumption.

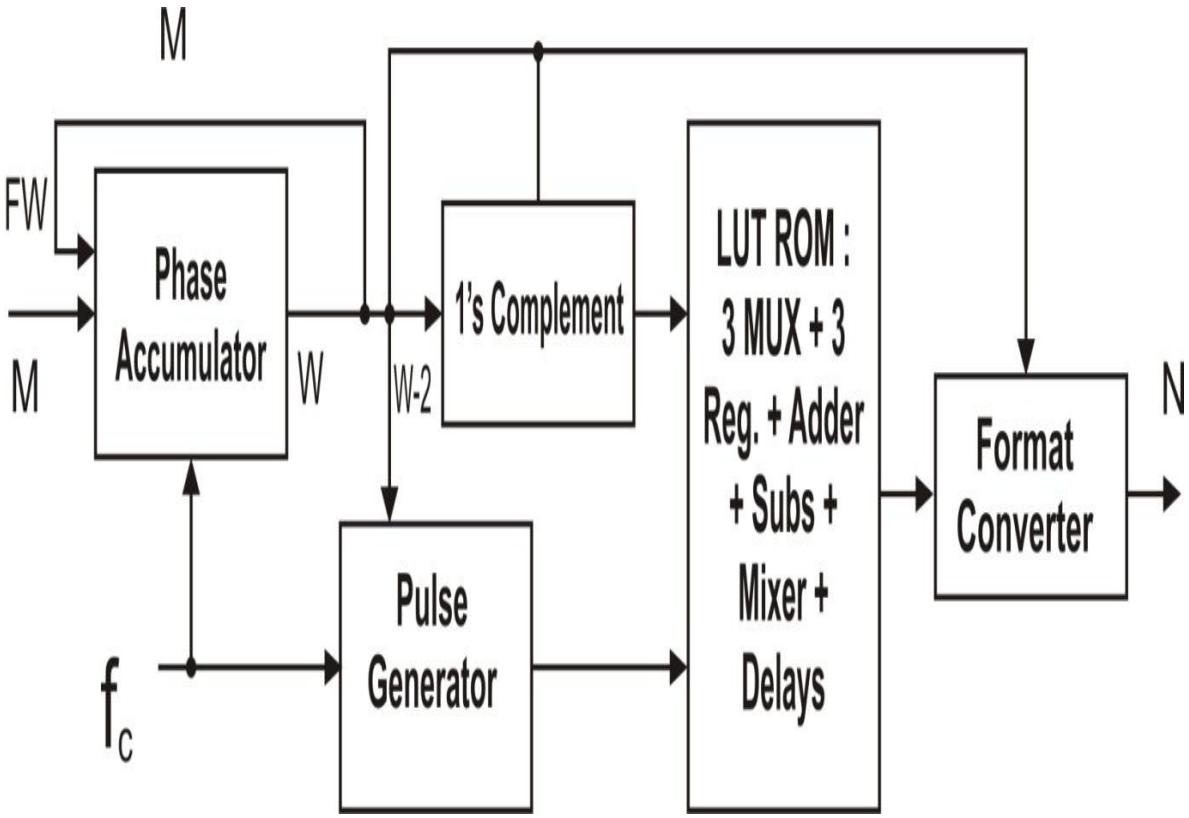

Figure 3.7: Proposed block diagram of DDFS

As mentioned earlier, accessing of memory is valid only once at a specific clock cycle. This work presents pulse generator circuit that is performing the task of time sharing.

The value of phase register at any clock period represents the required function. No other samples of the sinusoid are stored, only the first A bits of $W-2$ phase accumulator output are used to select segment initial amplitudes Q_i i.e. it represents multiplexer (MUX) address inputs. The remaining B LSB bits ($B = W - 2 - A$) represent an angle x in the interval Δx and are used to calculate value of the interpolated sine point. The pulse generator circuit performs three functions such as data comparison, pulse control, and delay. At each clock cycle, digital comparator examines transitions between segments. The detected signal will be applied to the pulse narrowing circuit to produce a Δt pulse width signal i.e. trigger 1 (T_{g1}), that is usually a fraction of $1/f_{clk}$. This signal, T_{g1} gives

an order to advance the data select inputs of MUX by 1; hence the output of the MUX during this time slot is $sin\ [(i+2)]$.

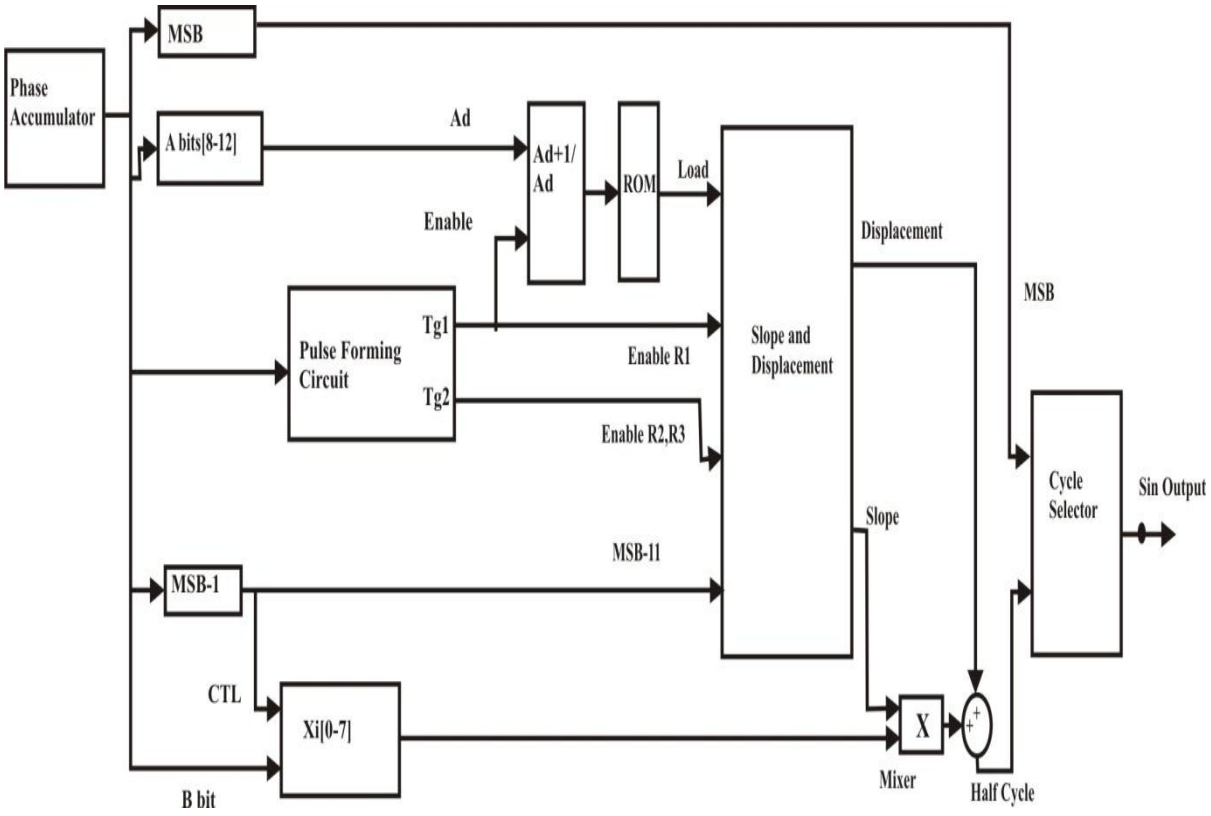

Figure 3.8: Proposed Simulink model of DDFS

At the same time, the T_{g1} is used to load this value in register 1 (R_1). After Δt, the data select inputs get back to the previous address value, so the output of MUX will be $sin\ [(i+1)\Delta x]$. Trigger 2 (T_{g2}) enables register 2 (R_2) to load this value. The content of R_2 will be subtracted from the content of R_1 and the result will be loaded in register 3 (R_3), after a specific time which is precisely sufficient to give a chance for signals to be propagated through all gates and settle down. Hence, the slope is simply derived and kept unchanged during segment interval.

The main feature of this proposed technique is that there is no need to derive the slope at each clock cycle, as shown in figures 3.7 and 3.8. In this work, the slope is approximated in each first sample interval and remains unchanged during the entire interval. The ROM address bus toggles between two values during this interval. These needless read cycles can consume unjustified excessive power. In contrast, the proposed work conducts one read cycle per segment and gets back to the idle mode during the rest of the interval.

The errors of the various points have been calculated as:

$$Z(x) = V_i x + K_i + e(x_i) \tag{3.14}$$

$$e_i(x) = Z(x) - (V_i x + K_i) \tag{3.15}$$

$$e_i(x) = A \sin\left[\frac{\pi}{2}\left(x + \frac{1}{2^{W+1}}\right)\right] - (V_i x + K_i) \tag{3.16}$$

The values of $e_i(x)$ is maximum for i^{th} interval, x_{is} can be found by equating the first derivative of equation to 0:

$$\frac{\partial e(x_{is})}{\partial x} = \frac{\partial z(x_{is})}{\partial x} - P_i = 0 \tag{3.17}$$

$$x_{is} = \frac{2}{\pi \cos^{-1}\left[\frac{2P_i}{A\pi}\right]} - \frac{1}{2^{W+1}} \tag{3.18}$$

Memory compression ratio depends upon W, S, input, and output width of the accumulator. This technique improves efficiency of the system better than other techniques as discussed in [115] - [119].

3.5.2 Simulation and Results

Figure 3.9 shows 256 generated samples of sine wave. These samples are used to analyze the conversion process. Based on the concept of previous section, this work has designed a DDFS with 83.9 dBc of SFDR that is better than existing techniques and theoretical calculation which is calculated by Nyquist as given below:

$$\text{SFDR} = 24\ \text{dBc} + 20 \log S^2 \qquad (3.19)$$

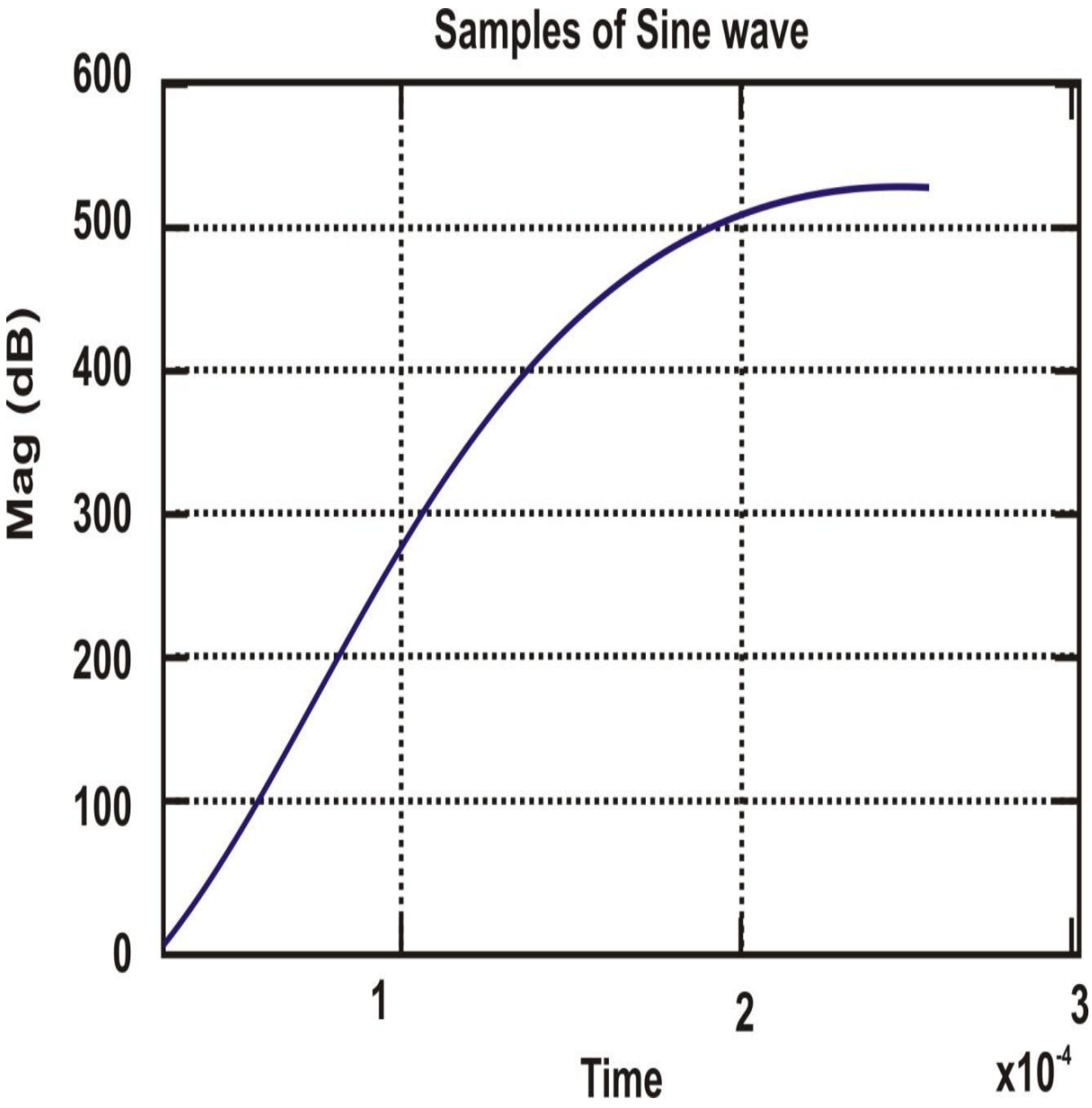

Figure 3.9: Samples (256) of Sine wave

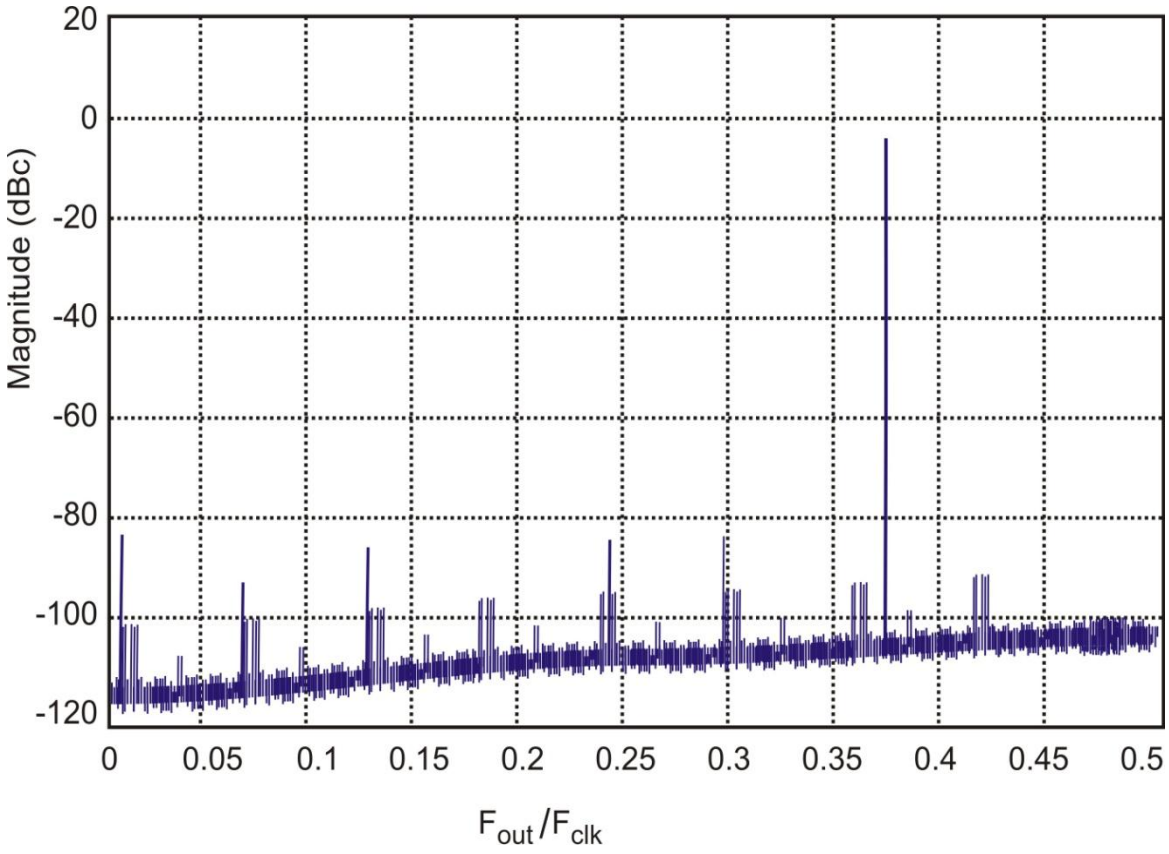

Figure 3.10: Output spectrum at 24%

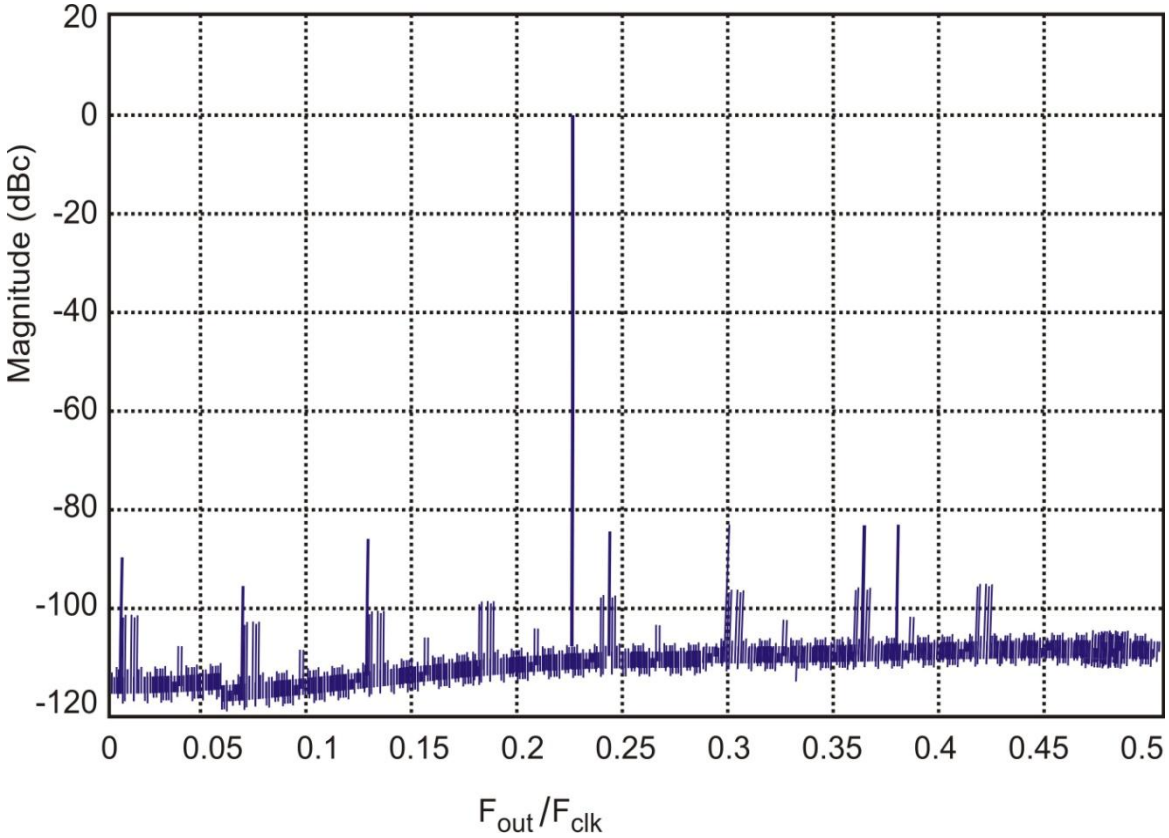

Figure 3.11: Output spectrum at 40%

Table 3.2: Comparison with other architectures

Architecture	Compression Ratio	ROM	SFDR	Additional Circuitry	Remarks
Ashkan A., Reza A. And Aleksandar M. [40]	-	Without ROM	82.7 dBc	Adder, multiplexers, register, converter	Number of multipliers & adders needed
Lia Lin-hui, Li Xiao-Jin and Zong-sheng [104]	$2^{11}\times12$	328	-	Adder, ROM, shift register, multiplier	Two ROM & slightly more circuitry needed
Chen Y. H and Chau [105]	-	Without ROM	-	Multiplier, adder, shift registers	Number of multiplier needed
Proposed DDFS Architecture	$2^{13}\times14$ ROM	Register ($2^5\times14$)	83.9 dBc	Multiplier, adders, register, shift register, delay, pulse generator	Best compression ratio

Spurious level for DDFS are shown in figures 3.10 and 3.11 for output frequency of 24% and 40% of clock rate and the input is positioned up to be FIW (7537) & FIW (12454) correspondingly.

This work was analyzed using MATLAB Simulink with 15 bits phase accumulator and 32 segments where bit length is A 5, and that of B is 8 whereas amplitude resolution is 14 bit, then total memory size will be $2^5\times14 = 448$ bit. Because 5 bit is the input to the ROM and 14 bit is the output of the ROM.

Table 3.2 presents a comparison between the proposed architecture and different implementations reported in recent literature. This work has used other components instead of ROM to minimize storage capacity and noise at the output. The comparison shows significant improvements in all features. The proposed DDFS can simultaneously achieve an excellent spectral purity without additional circuitry.

3.6 PROPOSED DDFS ARCHITECTURE BASED ON LAGRANGE INTERPOLATION AND MODIFIED QUASI-LINEAR TECHNIQUES

This work proposed a new technique for DDFS based on Lagrange interpolation and modified quasi linear methods. A novel technique has been proposed in which RTL synthesis on FPGA has been implemented using Lagrange interpolation. Specifically, it has been shown in figure 3.12 that better interpolation techniques can be employed to yield a better class of parabolic functions that can be used to approximate a pure sine wave. This approximation is further corrected by use of linear interpolation polynomials that suitably reduces DDFS complexity and helps get reasonably better results. The proposed design scheme has been implemented on XILINX FPGA and suitable hardware analysis has been carried out. Further discussions on its use in real-time applications have also been given that serve as performance evaluation of the proposed DDFS architecture.

DDFS holds an important position in modern communication system. Their requirement in digital communication systems can hardly be underestimated. A wide band, high resolution, good spectral purity, and fast switching have been presented [120] by using linear phase and frequency techniques.

Digital frequency synthesis was first proposed by Tierney et al. in 1971 [121] that is being used to generate discrete samples and convert them into sine wave of different frequencies, originated from one or more sources of reference inputs.

Various parameters of DDFS like output frequency, amplitude, frequency hopping, phase, and phase resolution have been analyzed [122]. Manipulation of these parameters is useful in DSP and digital communication applications.

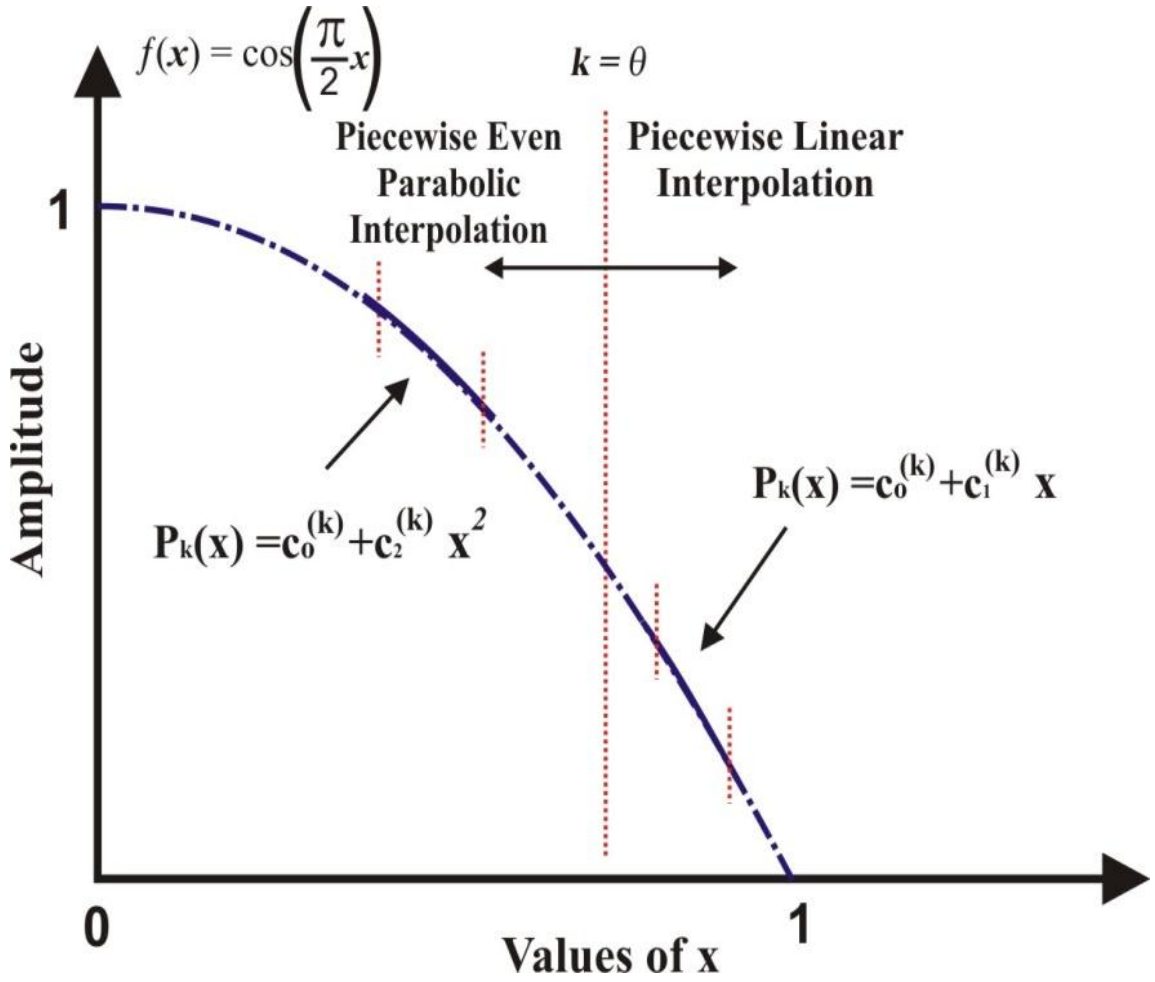

Figure 3.12: Interpolation regions of cosine wave

Most DDFS architectures have an address counter, a LUT followed by registers, and DAC. Some reconstruction filters are also provided for better spectral tuning. Often the address counter is implemented as phase accumulator whose input and tuning word length determines its required output, as given in equation (3.1).

As can be ascertained and easily understood from prevailing discussions, the size of LUT memory and frequency resolution is related to each other. If size is more; resolution will be more. A size of accumulator also affects the size of memory. Subsequently, the

accumulator and the LUT consume the largest area in any DDFS architecture and therefore, a lot of work has been done to suitably optimize these blocks [123] - [134].

In this work, techniques have been proposed to optimize the PA and the size of the LUT based on Lagrange interpolation and quasi-linear methods with a sincere hope to bring down the design complexity of the DDFS architecture while maintaining at the same time better performance with respect to generated output and spectral purity. This work is extension of [134]. RTL synthesis of DDFS has been implemented using Lagrange interpolation and quasi-linear methods. In the next sub-section, the above mentioned interpolation techniques have been explained.

3.6.1 Polynomial Interpolation Technique

Polynomial interpolation technique is an efficient technique for the interpolation by an arbitrary factor. This technique is called polynomial interpolation because it reproduces the given interpolation signal. Polynomials can be used to approximate complicated curves like the shapes of letters, evaluation of natural logarithm, and trigonometric functions.

Given a set of $n+1$ data points (x_i, y_i) where x_i and y_i are two points on the respective axis; one is looking for a polynomial p of degree at most p with the property

$$p(x_i) = y_i, \qquad i = 0, \dots\dots\dots, n. \tag{3.20}$$

The Unisolvence theorem states that such a polynomial p exists and is unique, and can be proved by the Vandermonde matrix.

The theorem states that for $n+1$ interpolation nodes (x_i), polynomial interpolation defines linear bijection

$$L_n = K^{n+1} \rightarrow \Pi_n \tag{3.21}$$

where

Π = Vector space (n degree polynomial)

Assume that interpolation polynomial is

$$p(x) = a_n x^n + a_n x^{n-1} + \cdots + a_n x^2 + a_n x + a_n \quad (3.22)$$

The assertion that n interpolates the information points indicates

$$p(x_i) = y_i \quad \text{for all } i \in \{0,1, \ldots\ldots, n\} \quad (3.23)$$

After combining above equations, the linear equation system provides coefficients a_k which may be shown in matrix vector form as.

$$\begin{bmatrix} x_0^n & x_0^{n-1} & \ldots & x_0 & 1 \\ x_1^n & x_1^{n-1} & \ldots & x_1 & 1 \\ . & . & . & . & \\ . & . & . & . & \\ x_n^n & x_n^{n-1} & \ldots & x_n & 1 \end{bmatrix} \begin{bmatrix} a_n \\ a_{n-1} \\ . \\ . \\ a_0 \end{bmatrix} = \begin{bmatrix} y_0 \\ y_1 \\ . \\ . \\ y_n \end{bmatrix} \quad (3.24)$$

The interpolant $\mathrm{p(x)}$ can be determined by coefficient $\mathrm{a_k}$. This matrix is also known as Vandermonde matrix.

There are two types of interpolation:

- Lagrange interpolation method
- Linear interpolation method

As, the Lagrange polynomial give exact reconstruction of the input samples, they are desirable than the linear interpolation.

3.6.2 Lagrange Interpolation & Function Approximation

Lagrange interpolation technique is used for polynomial interpolation. The mathematical equations and their relation with approximation are given as discussed below:

Generally stated, f is the function with gird N, n is the given points with polynomial order $n-1$ that passes all points. With few details of defining the properties f and N must possess, we can see that the general solution of this problem for linear case would be:

$$f(x) = \sum_{n \in N} W(x,n) f(n) \quad (3.25)$$

Where,

x = Values on the curve

$W(x, n)$ = Linear weight function.

For this reason, this work tries the Lagrange interpolation polynomials which can be roughly defined as $P(x)$ is the polynomial; n is the number of points, where polynomial passes through it.

Let $(x_1 , y_1 = f(x_1)), (x_2 , y_2 = f(x_2)), \ldots\ldots\ldots\ldots (x_n , y_n = f(x_n))$, and so on.

$$P(x) = \sum_{j=1}^{n} P_j(x) \tag{3.26}$$

where

$$P_j(x) = y_j \prod_{\substack{k=1 \\ k \neq j}}^{n} \frac{x - x_k}{x_j - x_k} \tag{3.27}$$

Polynomial $P_j(x)$ has the property that

$$P_i(x_j) = 0 \ ; \ j \neq i \quad \& \quad P_i(x_j) = 1 \ ; j = i \tag{3.28}$$

Where $P_j(x)$ Lagrange polynomial and $x_0, x_1, \ldots\ldots x_n$ are the interpolation points

$\{(x_0, 0), \ldots . (x_{i-1}, 0), (x_i, 0), (x_{i+1}, 0), \ldots . . (x_n, 0), \}$

The Lagrange polynomial $P(x)$ is given as:

$$P(x) = \sum_{i=0}^{n} y_i \cdot P_i(x) \tag{3.29}$$

It means that this polynomial has degree $\leq n$

By property of polynomial $P(x_i) = y$

Note that the Lagrange polynomial $P(x)$ is unique. If there were two such polynomials, $P(x)$ and $Q(x)$, then $P(x) - Q(x)$ would be a polynomial of degree $\leq$ n with $n + 1$ zero. Thus, it must have $P(x) \equiv Q(x)$.

The benefit of having Lagrange interpolation can be seen in figure 3.13 that shows a function passing through points defined at specific locations on the grid.

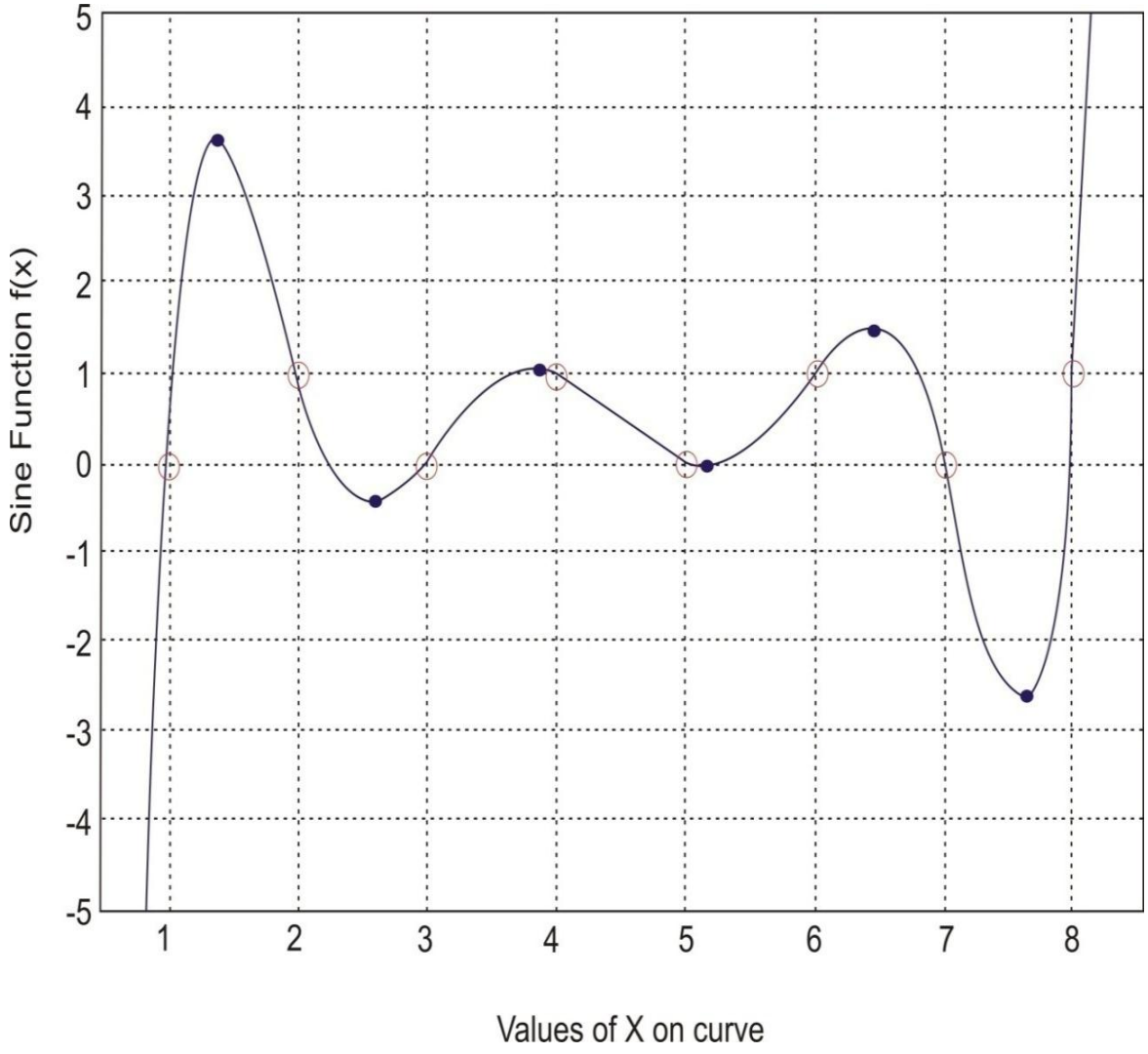

Figure 3.13: A plot between sine function f(x) and values of x on curve

This tells that given any function which is defined at discrete intervals of time, it can always be approximated suitably through Lagrange interpolation. Lagrange interpolation function is given as:

$$function[x] = lag\_interpol(x, s, r, t_{01}) \quad (3.30)$$

where,

x = Signal

s = Sampling rate of the original signal

r = Desired sampling rate of the resample signal

t_{01} = Optional argument that controls precision of rounding

xr = Resample signal

$$p = s/r \tag{3.31}$$

$$x = interp(x, 1/p) \tag{3.32}$$

$$x = resample(x, 1/t_{01}, round(p \times 1/t_{01}) \tag{3.33}$$

$$y = \sin(x) \tag{3.34}$$

These Lagrange interpolation functions are used to find an approximation of a sine wave. Coming to application of Lagrange interpolation for the problem considered here, it would be interesting to show here that how good Lagrange interpolation is for approximation of a sine wave. The results obtained in this context would then determine whether it would be feasible enough to proceed for a complete DDFS architecture based on this idea. Consider the portion of sine wave as shown in figure 3.14.

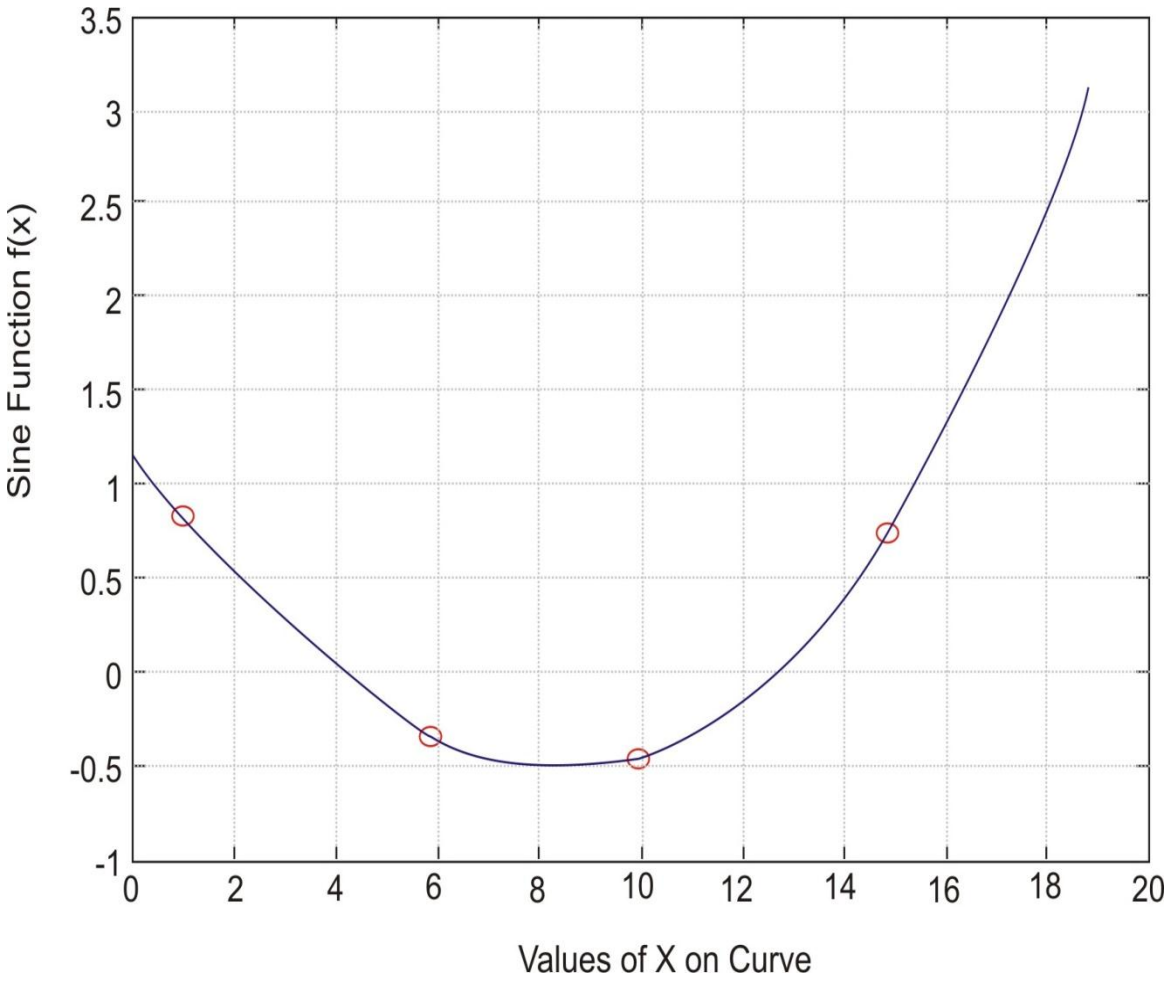

Figure 3.14: Portion of sine wave for interpolation

It shows that the points that have been provided are beautifully interpolated by the equations (3.26) and (3.29) that show that it can be further extended to reproduce the complete sine wave. However, when more number of points is provided, result seems drastically different.

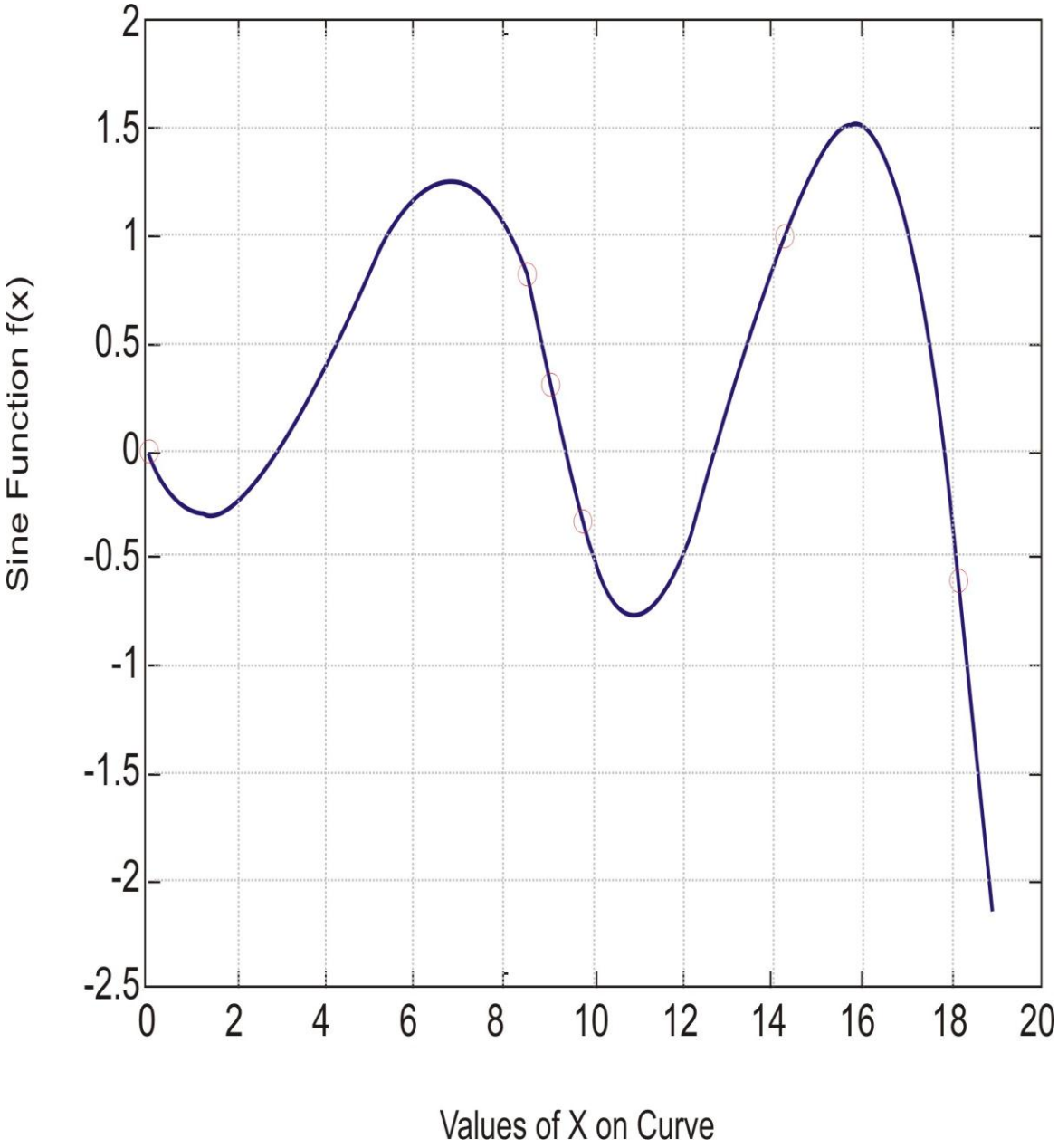

Figure 3.15: Sine wave for interpolation

Although equations for Lagrange interpolation have done a fantastic job of approximating the function with given points, as shown in figure 3.15, it shows that there are possibilities that the resulting interpolated function may not be a pure sine wave with a

single frequency. Naturally, providing more number of points would enhance the interpolation quality, the objective is to reduce memory requirements of hardware. Hence to further enhance accuracy of the system, it employs quasi-linear methods as described beautifully in [133]-[135].

3.6.3 Quasi-Linear Interpolation Method

This method proceeds by first considering the positive half of a sine or cosine wave that can be defined as:

$$f(x) = cos\left(\frac{\pi}{2}x\right) \tag{3.35}$$

This function is then divided into $s = 2^n$ number of segments.

Further each of the given segments are approximated by required polynomial of the form (3.24)

$$P_k(x) = \begin{cases} c_o^{(k)} + c_2^{(k)}x^2; 1 \le k \le \theta \\ \qquad\qquad 0 \le x \le 1 \\ c_o^{(k)} + c_1^{(k)}x\ ; 1 \le k \le s \end{cases} \tag{3.36}$$

Where k represents segment number, $c's$ denote the coefficients & θ provides knowledge about segment, in cases of the polynomial varying from parabolic curve to linear curve. As cosine function can be taken as parabola when it is nearer to zero and similar to a line when it is nearer to one. Above equations can be used to determine or choose particular segment of cosine function and appropriate interpolation can be applied.

Following above refinements in interpolation equations, it can suitably modify earlier approach of using just Lagrange interpolation. $P(x)$ that was defined by equation (3.26), will now have to satisfy additional constraints imposed by equation (3.36) and the interpolation will have to be applied in a piece-wise manner corresponding to s segments. Sine function approximated in this manner has been shown in figure 3.16:

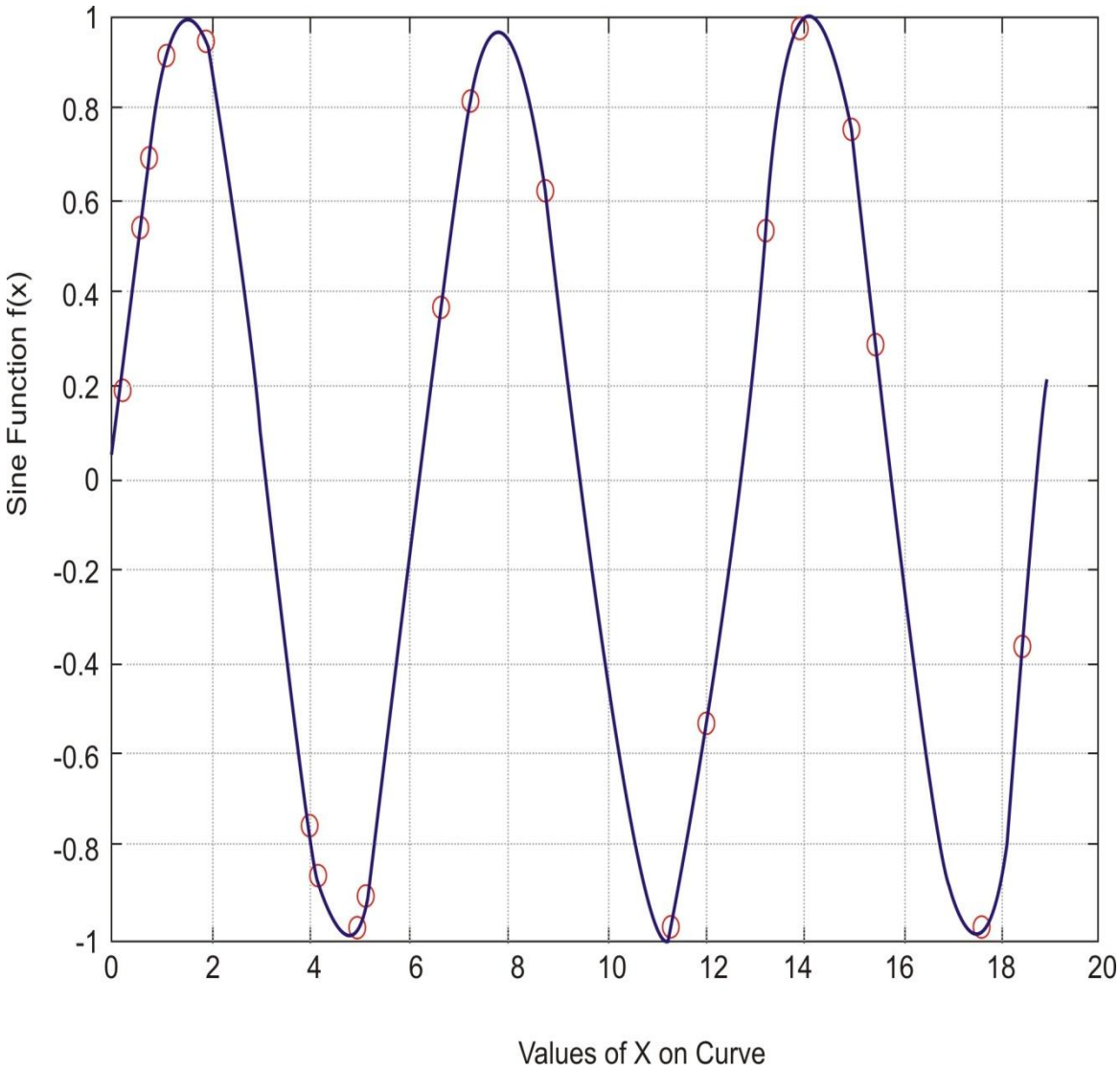

Figure 3.16: Approximated sine function

The results are much better and hence it can easily approach towards its further implementation in the form of digital hardware [40] & [133]-[134]. The reason behind choosing obviously stems from the statement that the cosine wave acts more similar to a parabola when it is nearer to zero and behaves similar to a line when it is nearer to one.

The combined equation can be found using equations (3.26) & (3.36) and the proposed system may be given as below:

$$P_k[n] = \begin{cases} qk + \sum_{j=0}^{r} h_{jk} \langle \frac{n^2}{2^{W-2}}, g_{jk} \rangle ; 1 \leq k \leq \frac{3x}{4} \\ qk + \sum_{j=0}^{r} h_{jk} \langle n, g_{jk} \rangle ; \frac{3x}{4} + 1 \leq k \leq s \end{cases} \quad (3.37)$$

where

h_{jk} = Multiplier for multiplexer

g_{jk} = Coefficients

x = Phase

m = Number of segments

k = Segment number

The parameter qk can be obtained by

$$qk = \left[2^{D-1} c_0^{(k)}\right] \tag{3.38}$$

where

$c_0^{(k)}$ = Coefficient

D = Output word length

The above expressions are incorporated with RTL synthesis, hardware implementation and simulation results. Other mathematical expressions have already been explained in [134]. The hardware implementation and correlation with proposed mathematical model have been explained in the next section.

3.6.4 Hardware Implementation

Hardware implementation of the proposed DDFS architecture based on Lagrange interpolation and quasi-linear methods is accomplished using XILINX Virtex 6 FPGA and the entire algorithm was implemented using impulse C. This language is also standardised by American national standard institute (ANSI), which is used to synthesize embedded and high performance computing applications. It works as co-design simulation tool. It has advantages for designing hardware to provide system level pipelining and instruction scheduling which saves the clock cycles. The more no. of clock rate accelerates performance [134] of the PLL. The code of impulse C can be converted into equivalent VHDL code. These codes can be used for simulation and synthesis of the system.

This work does not include all mathematical expressions because it is already explained by A. Ashrafi et al. in [134]. Here the emphasis has been given on synthesis work. RTL synthesis on FPGA is a work which has been synthesized first time using Lagrange interpolation. In the next section, results and discussion have been presented.

3.6.5 Results and Discussion

In this section, simulation and resister-transistor logic (RTL) level implementation on FPGA have been done using XILINX ISE tool. RTL level analysis is a method that is used to synthesize frequency signal at high level. General hardware RTL schematic as derived in XILINX ISE Design Suite 14.1 is shown in figure 3.17. Choice of FPGA was governed primarily for its availability of on-chip resources that if properly managed can result in high speed DDFS solution.

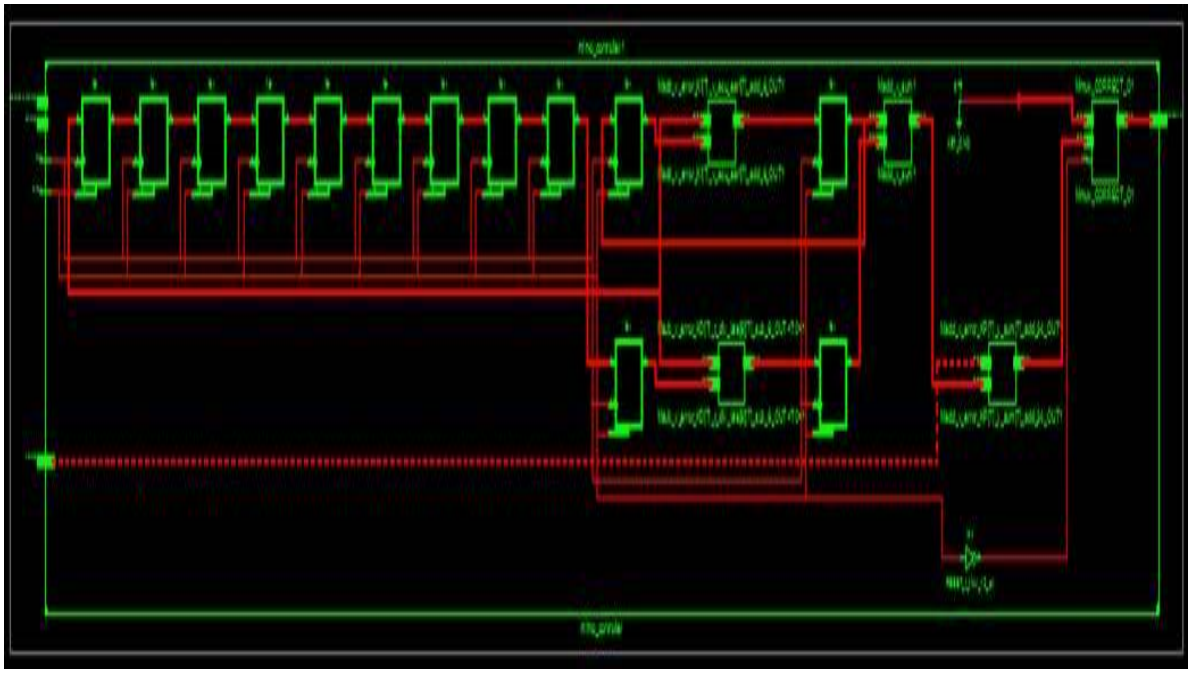

Figure 3.17: Hardware RTL schematic

Rectangular blocks on left hand side are Lagrange interpolator and blocks in the middle are quasi-linear interpolators. Once Lagrange interpolator approximates the function, quasi linear interpolator is utilized to increase the accuracy of the approximation which leads to better output. Final signal is then passed through phase to sine on-chip memory

and ultimately digital values are obtained that when converted to analog values result in pure sine wave.

This work needs result in both forms analog and digital. Therefore, corresponding digital output of DDFS architecture is exposed in figure 3.18.

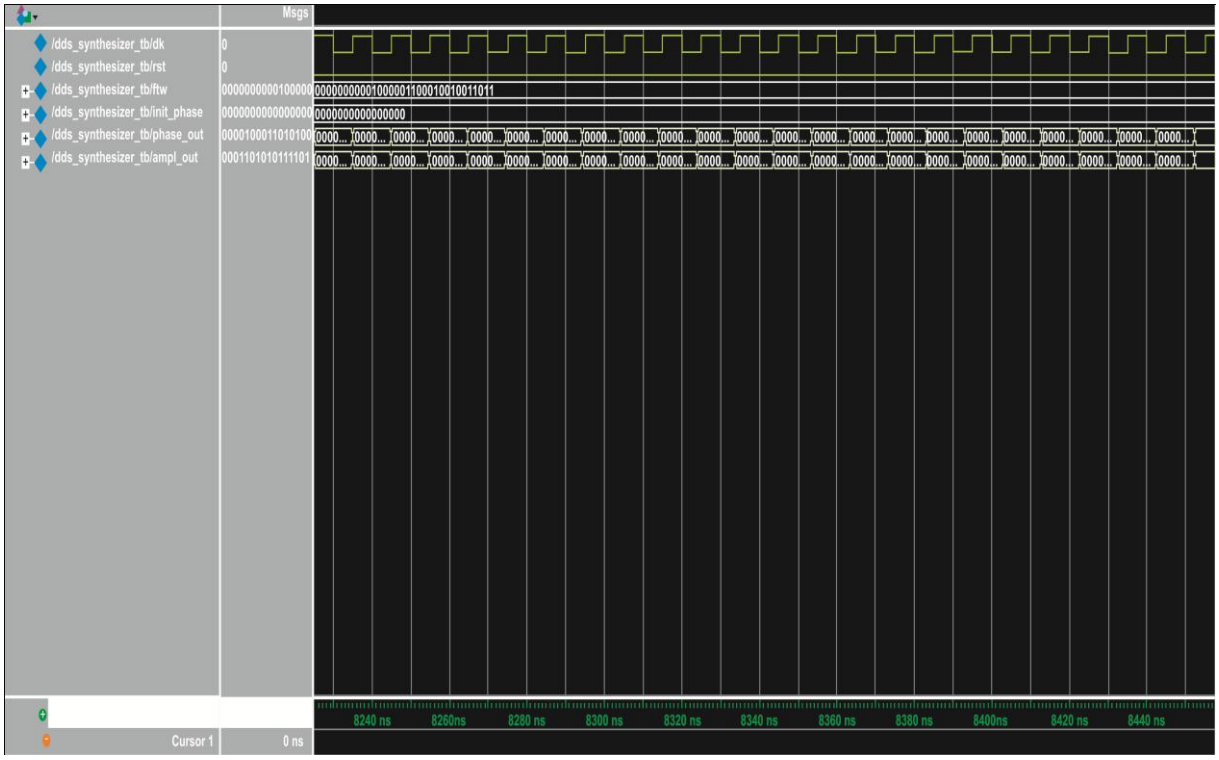

Figure 3.18: Digital output of DDFS

From the above result, it has been found that phase is varied corresponding to amplitude of input signal. Sine wave signal is approximated using Lagrange interpolation and quasi linear interpolation methods which produce phase and amplitude at a particular clock. DDFS is a digital device, but it produces analog signal corresponding its digital values. If these values are converted to analog values through DAC, a sine wave would result as has been shown in figure 3.19 using analog waveform viewer in ModelSim.

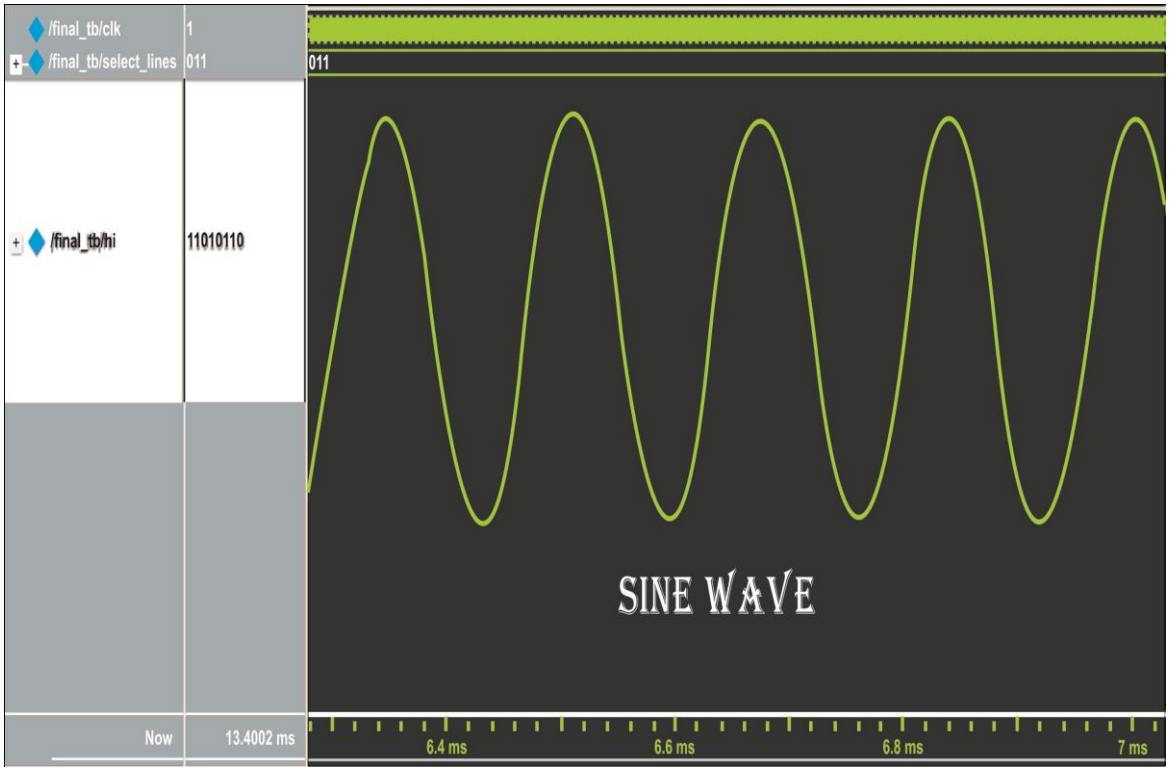

Figure 3.19: Analog output of DDFS

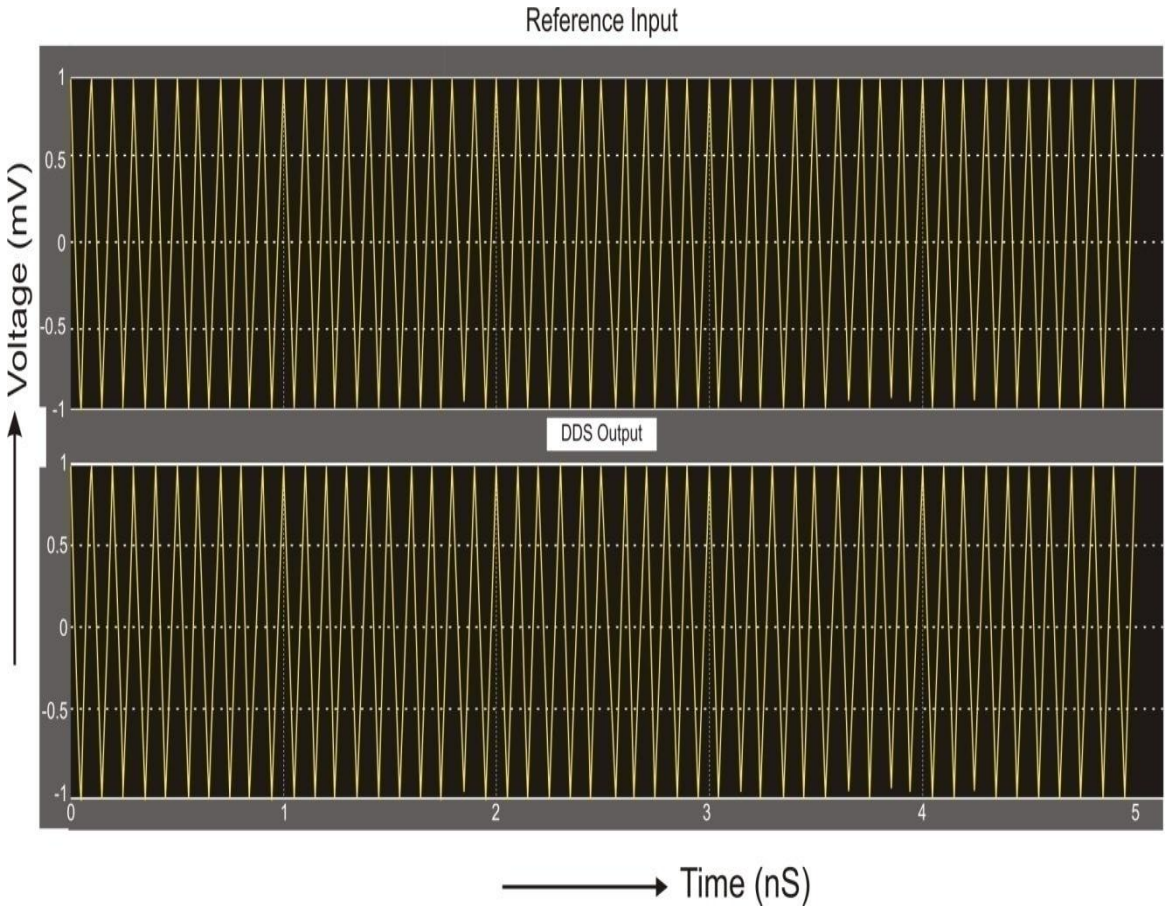

Figure 3.20: Compared output of DDFS with reference input

Results show that first quadrant of sine wave is straighter as compared to other quadrant; it means that first quadrant used more values of x on curve. Finally, it found improved performance as compared to existing architecture. An equivalent hardware was also designed in MATLAB R2012a using Simulink and embedded MATLAB functions. Output of DDFS compared to reference input signal is exposed in figure 3.20. From results, it is found that output wave form has similar response as reference input.

The synthesis summary of the hardware as generated in XILINX ISE Design Suite 14.1 is presented in table 3.3.

Table 3.3: Comparison table of proposed design with existing design

Property	**Proposed design**	**N. Prasad et al. [113]**	**J. Lee and X. Yang [112]**
Number of Slice (CLB) Registers	8% Logic Utilization	17 % Logic Utilization	10 % Logic Utilization
Number of Slice (CLB) Look Up Table	24 % Logic Utilization	34 % Logic Utilization	38 % Logic Utilization
Max. Frequency	739.437 MHz	107.216 MHz	116.67 MHz

From the comparison table 3.3 it has been found that the performance of proposed design is better as compared to existing techniques in terms of device utilization and speed.

The configurable logic block (CLB) consists of an n-bit LUT, a flip flop, and a 2×1 MUX. The value of n is manufacturer specific. Increase in value n can increase the performance of a FPGA. The number of slices registers means sums of numbers of slice LUT flip flop pair and numbers of slice registers and divide it by 4 approximately. The number of slice LUT means numbers of LUT in it. Maximum frequency (739.437 MHz) can be improved for the analysis. Real time between starting and finishing the processing

can be reduced for the same. Finally, merits of the design have been presented in the next section.

3.6.6 Merits of the Design

Few merits of proposed design approach are as follows:

1. Spectral resolution of DDFS can be changed in real-time to suit almost any design specification as the word length can be changed and FPGA can be field-programmed.

2. Phase continuity of signal will be preserved even if frequency is changed.

3. The design is speed-efficient and also suitably area optimized.

4. Use of impulse C resulted in hardware implementation capable of running at high clock frequency.

3.7 SUMMERY OF THE CHAPTER

ROM compression algorithm has been presented to optimize DDFS using piecewise linear approximation. The proposed technique allows successive read access to memory cells per one clock cycle using time sharing. Output values will be temporarily stored and read at a later time. The desired waveform has been approximated to get reconstructed signal of output. As a result, DDFS only needs to store fewer coefficients and hardware complexity is significantly reduced. The resulting hardware is less complex primarily because of use of better parabolic interpolation based on Lagrange's interpolation technique and also by using quasi-linear methods. The proposed DDFS has been analyzed using MATLAB and impulse C. The results obtained show improvement of around 1.43 % in spurious free dynamic range (SFDR) over existing results. The results show better performance than other existing techniques. In future, it can also be used to improve the performance of hybrid DDS-PLL synthesizers. In the next chapter, the novel architecture of fractional sigma delta modulator PLL has been presented.

CHAPTER 4

PARAMETRIC ANALYSIS OF A NOVEL ARCHITECTURE USING FRACTIONAL-N PLL

4.1. INTRODUCTION

Fractional-N PLL synthesizer is similar to N-integer PLL. The only difference is that fractional PLL uses the highest frequency input as reference and the lowest division ratios. Also, the higher frequency input reference is easier to filter out and allows a lower division ratio that produces better phase noise, lower spurious signal response, and better switching time. Fractional-N PLL is also called as hybrid PLL that is used in receivers, transmitters, radar, frequency alteration device etc. The quality of high speed transmission and bandwidth are the main features for improvement of spectral purity and output frequency spectrum. These qualities are used for optimization and frequency resolution of the system. There are many challenges to be analyzed in fractional-N PLL. One of the challenges is to reduce the noise. Literature review of some of the most relevant researches has been reported in the following paragraphs:

In this work, different parameters of loop filter have been taken into consideration to reduce the noise of VCO in locked condition. Other noise sources are input reference, filter noise, charge pump noise, divider, and oscillator. Output signal and power spectrum densities (PSD) of system are affected by these phase noise sources. Transfer function of each component has been derived and analyzed. An individual model has been developed corresponding to their transfer function to achieve noise effect [136] on output of fractional PLL. Kyoungho et al. proposed a new fractional-N hybrid PLL that was used in wider bandwidth during transient condition of system. Fast-locking system has been achieved for various applications in [137]. Digital protocols are used to compensate

divider fractional value to control different applications. Considering the previous work, Rhee et al. [138] proposed a novel fractional-N PLL that is based on a sigma delta modulation technique. Spurs and nonlinearity issues have been discussed with proper results. Many papers were reviewed in chapter one for substituting low cost design and to reduce spurs in the finite-modulo fractional-N PLL. Besides phase analysis, frequency domain analysis has been described by Herzel et al. [139]. This work presented various noise components like reference input, input buffer, VCO, filter, charge pump, and sigma delta modulator (SDM). But out of above, only noises due to charge pump thermal device and constant current have been calculated. These noises can be reduced by using bipolar complementary metal oxide semiconductor (BiCMOS) and metal oxide semiconductor field effect transistor (MOSFETs) technologies. This work uses two CMOS charge pumps. These are combined together to achieve noise optimization for the proposed system. Considering above limitations, it is needed to employ a technique for smoothening the VCO input & output voltage to reduce noise in the fractional PLL. The mathematical expressions of noise, jitter, and other components have been explained in next section.

4.2 NOISE AND JITTER

Noise and jitter are the important parameters to analyze performance of the system. Let us assume that input is sinusoidal wave which is produced by frequency synthesizer

$$V(t) = V_o \, sin(2\pi f_o t) \tag{4.1}$$

Effect of amplitude and phase are given as:

$$V(t) = (V_o + v(t)) \, sin(2\pi f_o t + \emptyset(t)) \tag{4.2}$$

where

V_0= Amplitude

$v(t)$ =Amplitude varied with time

f_o= Carrier frequency

$\emptyset(t)$=Phase

f_m=Offset frequency

Above equation shows fluctuation effect of $v(t)$ and $\emptyset(t)$

Phase fluctuation has been explained in equation (4.2), but periodic variation produces spurious tone. This can be derived in term of offset frequency and carrier frequency.

$$V(t) = V_o \sin(2\pi f_o t + \Delta\emptyset sin(2\pi f_m t)) \quad (4.3)$$

$$V(t) = V_o[sin(2\pi f_o t)cos(\Delta\emptyset sin(2\pi f_m t)) + cos(2\pi f_o t)\, sin(\Delta\emptyset sin(2\pi f_m t))] \quad (4.4)$$

where

$\Delta\emptyset$ = Change in phase

Let us assume phase modulation is small, then, $\Delta\emptyset \ll \pi/2$

$cos\big(\Delta\emptyset sin(2\pi f_m t)\big) \cong 1$

$sin\big(\Delta\emptyset sin(2\pi f_m t)\big) \cong \Delta\emptyset sin(2\pi f_m t)$

From above equation

$$V(t) = V_o[sin(2\pi f_o t + \Delta\emptyset cos(2\pi f_o t) sin(2\pi f_m t)] \quad (4.5)$$

$$V(t) = V_o\left[sin(2\pi f_o t) - \frac{\Delta\emptyset}{2} sin\big(2\pi(f_o - f_m)\big) + \frac{\Delta\emptyset}{2} sin\big(2\pi(f_o + f_m)\big)\right] \quad (4.6)$$

It is observed that the two spurious tones are at $f_o + f_m$ and $f_o - f_m$. These are $-20\ log\left(\frac{\Delta\emptyset}{2}\right) dB$ below carrier frequency.

The arbitrary phase deviation generates noise and its spectral density is given as:

$$S_\varphi(f) = \int_{-\infty}^{+\infty} R_\varphi(\tau) e^{-j2\pi f\tau} d\tau \quad (4.7)$$

$R_\varphi(\tau)$ = Auto-correlation

$\varphi(t)$ = Random phase variation

$$R_\varphi(\tau) = E[\varphi(t)\varphi(t-\tau)] \quad (4.8)$$

Assume $\varphi(t) \ll 1$ radian, and then power spectrum density $S_v(f)$ is given as:

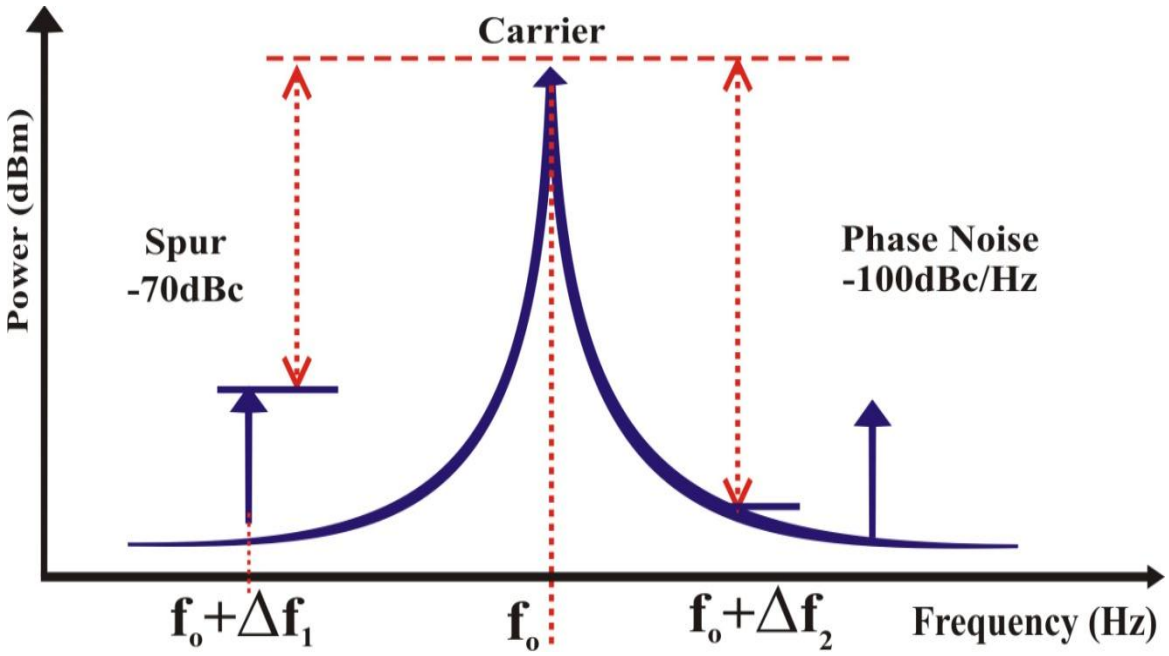

Figure 4.1: Phase noise with spur level

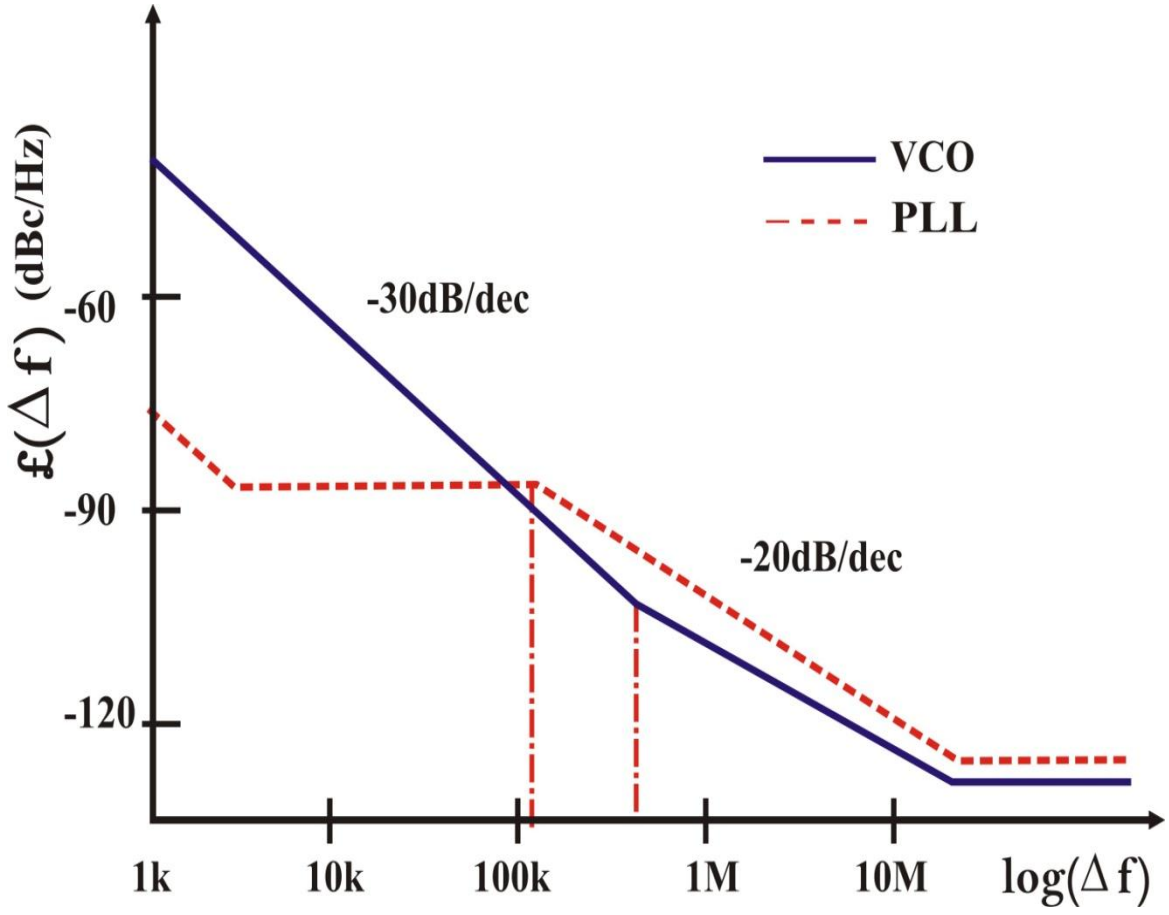

Figure 4.2: Phase noise level of PLL and VCO

$$S_v(f) = \frac{{V_o}^2}{2}\left[\delta(f - f_o) + S_\varphi(f - f_o)\right] \quad (4.9)$$

where

f_0 = Carrier frequency

Ratio noise power at frequency offset from the carrier to carrier power is defined as follows:

$P_n =$ Phase noise at 1 Hz offset frequency

$P_c =$ Carrier Frequency

$$£(\Delta f) = 10\ log\frac{P_n}{P_c} = 10\ log\frac{S_\varphi(\Delta f)}{2}\ \ dBc/Hz \quad (4.10)$$

Spur and noise of amalgamated signal frequency f_o has been presented in figure 4.1. The phase noise Δf_2 is $-100\ dBc/Hz$ and spur Δf_1 is $-70\ dBc/Hz$ at offset frequency.

Phase noise of VCO and PLL has been illustrated in figure 4.2. The VCO's noise demonstrate three sections with their slope as, -20 dBc/Hz and -30 dBc/Hz. In in-band condition, phase noise of PLL is flat in accordance with their input signal, but in out band condition, it pursues phase noise of VCO.

4.3 TIMING JITTER

Jitter is a phase fluctuation in the time domain that has n^{th} cycle at time T_n and its average period is T_{avg}.

Classification based on their properties as follows:

- Mathematical expression of cycle jitter is defined as:

  $$\Delta T_{cj} = T_n - T_{avg} \quad (4.11)$$

  $cj =$ Cycle jitter

  The σ_{cj} in terms of RMS value is described as:

  $$\sigma_{cj} = lim_{n\to\infty}\sqrt{\frac{1}{N}\sum_{n=1}^{N}(\Delta T_{cj})^2} \quad (4.12)$$

- Mathematical expression of cycle to cycle jitter (ccj) is given as under:

$$\Delta T_{ccj} = T_{n+1} - T_{avg} \quad (4.13)$$

$ccj =$ Cycle to cycle jitter

The RMS of the ccj may be expressed as:

$$\sigma_{ccj} = lim_{n\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N}(\Delta T_{ccj})^2} \quad (4.14)$$

- Mathematical expression of absolute jitter of the n^{th} cycles can be expressed as:

$$\Delta T_{abs}(N) = \sum_{n=1}^{N}\left(T_n - T_{avg}\right) = \sum_{n=1}^{N}\left(\Delta T_{cnj}\right) \quad (4.15)$$

abs = Absolute jitter

From the above expression, it is found that absolute timing jitter of PLL and oscillator depends upon time interval. For white noise sources, absolute jitter is measured with interval Δt, which is related to σ_{ccj}. An absolute jitter accumulates continuously with specified interval.

4.4 SETTLING TIME

Settling time is also known switching time or locking time. Settling time is the main parameter to determine the stability of the system and to manage locking process of channel switching. Channel switching is used to change divide ratio when PLL is in locked condition. It also determines errors corresponding to locking time. Transimpedance of third order filter is given as:

$$Z_f(s) = \frac{1+s\gamma_0}{s(\gamma_1 s^2+\gamma_2 s+\gamma_3)} \quad (4.16)$$

Where $\gamma_0 = R_1C_1$, $\gamma_1 = R_1R_3C_1C_2C_3$, $\gamma_2 = R_1C_1(C_2+C_3) + R_3C_3(C_1+C_2)$,

$\gamma_3 = C_1 + C_2 + C_3$ and $Z_f(s)$= Trans-impedance

Here γ_0 ,γ_1 , γ_2 , γ_3 are constants

Transfer function of the phase and frequency becomes:

$$H_{clg}(s) = \frac{K_{fpd}K_{vco}(1+s\cdot\gamma_0)}{s^2+\frac{K_{fpd}K_{vco}\gamma_0}{\gamma_3 N}s+\frac{K_{fpd}K_{vco}}{\gamma_3 N}} \quad (4.17)$$

$H_{clg}(s)$= Closed loop transfer function

N= Loop frequency divide ratio

Damping factor (ζ) and natural frequency (ω_n) are given by:

$$\zeta = \frac{\gamma_0}{2}\sqrt{\frac{K_{fpd}K_{vco}}{\gamma_3 N}} \quad (4.18)$$

$$\omega_n = \sqrt{\frac{K_{fpd}K_{vco}}{\gamma_3 N}} \quad (4.19)$$

Equation becomes:

$$H_{clg}(s) = \frac{N(2\zeta\omega_n s+{\omega_n}^2)}{s^2+2\zeta\omega_n s+{\omega_n}^2} \quad (4.20)$$

Output frequency varies from f_1 to f_2 with change of c and reference input. If value of N is small then error will be calculated as less because N is multiplied with the error occurred at the output. Final value theorem and Laplace transform are used to evaluate lock time of PLL that is given by expression

$$\lim_{t\to\infty}\theta(t) = \lim_{s\to 0} s\,\theta(s)$$

Output corresponding to input becomes:

$$f_o(s) - f_1(s) = \frac{f_2-f_1}{N\cdot s}H_{clg}(s) \quad (4.21)$$

Frequency error is determined by inverse Laplace transform (ILT):

$$\in_2(t) = \frac{f_o(t)-f_2}{f_1-f_2} = \left\{e^{-\zeta\omega_n t}\left[cos\left(\omega_n t\sqrt{1-\zeta^2}\right)+\frac{-\zeta}{\sqrt{1-\zeta^2}}sin\left(\omega_n t\sqrt{1-\zeta^2}\right)\right]\right\}\ for\ \ 0<\zeta<1 \quad (4.22)$$

If $\zeta = 1$ then,

$$\in_2(t) = e^{-\omega_n t}(1-\omega_n t) \quad (4.23)$$

If $\zeta > 1$ then,

$$\in_2(t) = \left\{e^{-\zeta\omega_n t}\left[cosh\left(\omega_n t\sqrt{\zeta^2-1}\right)+\frac{-\zeta}{\sqrt{1-\zeta^2}}sinh\left(\omega_n t\sqrt{\zeta^2-1}\right)\right]\right\} \quad (4.24)$$

where

$\in_2 (t)$ = Frequency error function

Here $\omega_n t$ is calculated on X-axis with different damping values. There are three conditions as follows:

$0 < \zeta < 1$ is called under damped response

$\zeta = 1$ is called critical damped response

$\zeta > 1$ is called over damped response

It concludes that locking time is longer if $0 < \zeta < 1$ for charge pump or VCO.

Transfer function of phase and output voltage is calculated in charge pump as follows:

$$H_{vc}(s) = \frac{V_c(s) - V_{c1}}{\theta_i(s)} = \frac{H_{c1}(s)s}{K_{vco}} \quad (4.25)$$

where

$H_{vc}(s)$= Transfer function with respect to VCO and charge pump

$V_{c1}(s)$= VCO at f_1

$V_c(s)$= Control voltage of VCO

$\theta_i(s)$= Input phase noise

$H_{c1}(s)$= Transfer function corresponding to output frequency f_1

Output frequency is determined corresponding to V_{c1}. Transient response of VCO is varied with change of frequency from f_1 to f_2. The difference of frequencies is given below:

$$V_c(s) - V_{c1} = H_{vc}(s)\,\theta_i(s) = \frac{2\pi(f_2 - f_1)}{K_{vco}}\,\frac{H_{c1}(s)}{Ns} \quad (4.26)$$

By inverse Laplace transformation

$$V_c(t) - V_{c1} = \frac{2\pi(f_2 - f_1)}{K_{vco}}[1 - \in (t)] \quad (4.27)$$

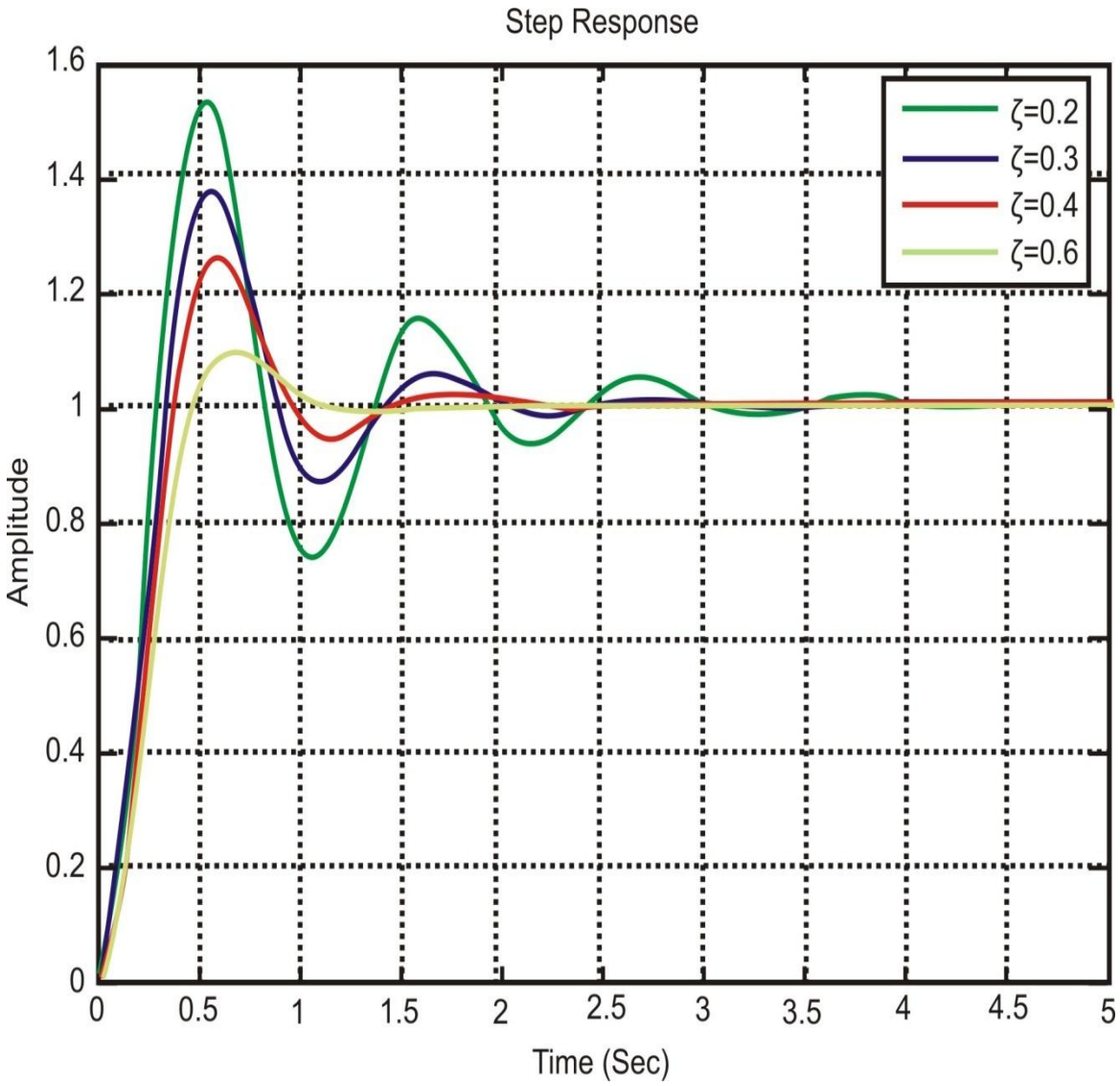

Figure 4.3: Step response at various values of damping factor

Overshoot will be increased if value of damping factor will decrease, as shown in figure 4.3. The variation of overshoot is around 10% (from 20% to 30%) corresponding to control voltage of 2nd & 3rd order PLL in that order at $\zeta = 0.707$.

4.5 TRACK & ATTAINMENT

It is a process in which phase is in locked state to determine transient response of output. Another acquisition technique is used to capture from condition of unlock to lock of the PLL. Both techniques are incorporated to each other to control feedback loop with help of PFD and CP. Operating range of CP is given in table 4.1. Details of operation of PLL may be shown as:

- $\Delta\omega_H$: The PLL frequency range is able to lock-in, after starting from an unlocked state. The array is generally less than lock range and depends on phase frequency detector. It is known as hold range.
- $\Delta\omega_L$: The PLL frequency range to remain locked. Primarily given through the oscillator range. For this frequency lock-in time is $T_L \approx \frac{2\pi}{\omega_n}$
- $\Delta\omega_p$: This is pull in range in which PLL will become locked.
- $\Delta\omega_{po}$: This is pull-out range in which PLL will lose the track.

$$\Delta\omega_{\mathrm{po}} = 2\pi\omega_{\mathrm{n}}\exp\left(\frac{\zeta}{\sqrt{1-\zeta^2}}\tan^{-1}\frac{\sqrt{1-\zeta^2}}{\zeta}\right) \quad (4.28)$$

If $\zeta = 1$ then,

$$\Delta\omega_{\mathrm{po}} = 2\pi\omega_{\mathrm{n}} \quad (4.29)$$

If $\zeta > 1$ then,

$$\Delta\omega_{\mathrm{po}} = 2\pi\omega_{\mathrm{n}}\exp\left(\frac{\zeta}{\sqrt{\zeta^2-1}}\tan^{-1}\frac{\sqrt{\zeta^2-1}}{\zeta}\right) \quad (4.30)$$

This determines approximation as:

$$\Delta\omega_{po} = 11.55\omega_n(\zeta + 0.5) \quad (4.31)$$

Table 4.1: Operating ranges of charge pump PLL

Parameter		**Frequency Range**	**Time**
Acquisition	Hold range	$\Delta\omega_H \to \infty$	NA
	Lock range	$\Delta\omega_L \approx 4\pi\zeta\omega_n$	$T_L \approx \frac{2\pi}{\omega_n}$
	Pull-in range	$\Delta\omega_p \to \infty$	$T_p = \frac{2C \cdot \Delta\omega}{I_{cp}}$
Tracking	Pull-out range	$\Delta\omega_{po} = 11.55\omega_n(\zeta + 0.5)$	NA

The table 4.1 shows operating ranges of a second order CP PLL. Operating ranges of other phase detectors like analog multiplexer, XOR gate, and JK flip-flop can be found in [96].

4.6 FRACTIONAL-N PHASE LOCKED LOOP

The ∑Δ fractional-N PLL synthesizer is similar to N-integer PLL. The main component of this fractional PLL is SDM. It compensates spur that is determined in digital domain. SDM is utilized to compensate frequency divide value.

Average (avg) fractional divide value may be expressed as:

$$N = N_b + n_{Qavg}(t) \tag{4.32}$$

Average output of modulator is $n_{Qavg}(t)$.

$$n_{Qavg}(t) = k/M \tag{4.33}$$

Where

N = Average fractional division ratio

k = Input to modulator

M = Modulus for modulator

When PLL is in steady state, output frequency is given by:

$$f_{out} = Nf_{ref} = \left(N_b + \frac{k}{M}\right) f_{ref} \tag{4.34}$$

Now frequency resolution becomes:

$$\Delta f = \frac{1}{M} f_{ref} \tag{4.35}$$

Frequency resolution depends on the reference frequency and modulus of modulator.

It means that its output is in accordance to given input and contrariwise to modulus of modulator. This modulator is also used in a frequency synthesizer to suppress fractional spurs for communication system.

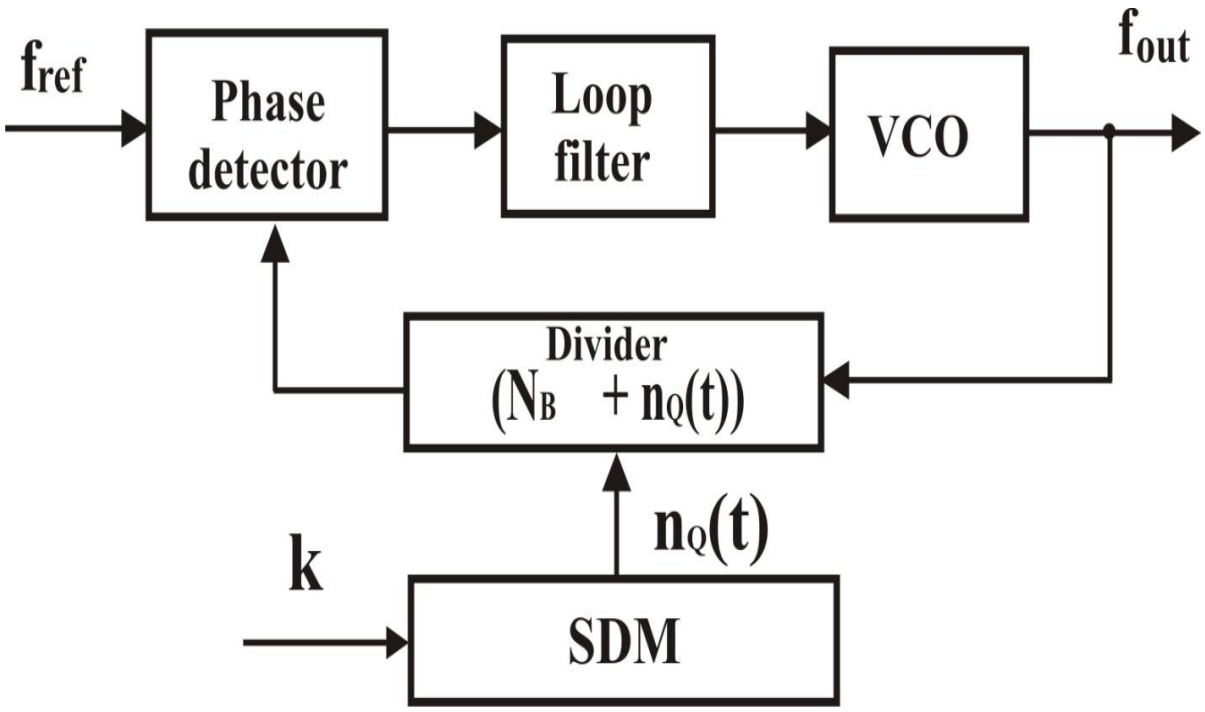

Figure 4.4: Quantization noise

Conventional diagram of the SDM quantization noise has been depicted in figure 4.4. It has advantages in phase noise for high frequency transmission [140], [141].

4.6.1 SDM Quantization Noise

Sigma delta modulator quantization noise is mapped with output of PLL. This modulator also connects VCO output and divider frequency to reduce the PN in feedback system. Frequency divider noise is given as:

$$S_{\theta div}(f) = \left[\frac{f_{ref} \cdot Q(f)}{f \cdot N}\right]^2 \ rad^2/Hz \tag{4.36}$$

$Q(f)$ = Root mean square spectral density

$$Q(f) = \sqrt{\frac{1}{12 f_{ref}} |H_{NTF}(z)|_{z=e^{j2\pi f}}} \tag{4.37}$$

where,

$H_{NTF}(z)$ = Noise transfer function

Let order of SDM is L^{th}

$$Q(z) = (1 - z^{-1})^L / \sqrt{12 f_{ref}} \quad (4.38)$$

Then,

$$S_{\theta div}(f) = \frac{f_{ref}}{12(Nf)^2} \left[2sin\left(\frac{\pi f}{f_{ref}}\right) \right]^{2L} \ rad^2/Hz \quad (4.39)$$

Output noise originates from closed loop noise and SDM noise, which is given by:

$$S_{\theta o}(f) = S_{\theta div}(f) \cdot |H_{cl}(f)|^2 \ \ rad^2/Hz \quad (4.40)$$

The assumption i.e. $H_{cl}(f) = N$ is within Band width.

Phase noise is generated in-band $\sum \Delta$.

$$S_{\theta o}(f) = \left[\left(\frac{f_{ref} \cdot Q(f)}{f} \right) \right]^{2L} \ rad^2/Hz \quad (4.41)$$

If band width of PLL is not large, then, the noise of the system is not dominated by the SDM.

Since locking time is zero, PSD can be derived as follows:

$$S_{\theta o}(f) = \frac{[2\pi Q(f)]^2}{|1 - z^{-1}|^2}, z = e^{j2\pi f / f_{ref}} \quad (4.42)$$

If $|1 - z^{-1}| \approx 2\pi f / f_{ref}$

$$S_{\theta o}(f) = \left[\frac{f_{ref} Q(f)}{f} \right]^2 \ rad^2/Hz \quad (4.43)$$

Let us consider order of SDM is L^{th}

$$S_{\theta o}(f) = \frac{(2\pi)^2}{12 f_{ref}} \left[2 \ sin\left(\frac{\pi f}{f_{ref}}\right) \right]^{2(L-1)} \ rad^2/Hz \quad (4.44)$$

It can be calculated as:

$$S_{\theta o}(f) = \frac{(2\pi)^2}{12 f_{ref}} \left[\left(\frac{2\pi f}{f_{ref}} \right) \right]^{2(L-1)} \quad rad^2/Hz \quad (4.45)$$

Equation (4.45) shows noise at low offset frequency.

Extended formula is as follows:

$$S_{\theta o}(f) = 10log \left\{ \frac{f_{ref}}{12(Nf)^2} \cdot \left| H_{NTF}\left(e^{j2\pi f / f_{ref}}\right) \right|^2 \right\} \ dBc/Hz \quad (4.46)$$

Since band width is within range,

$$S_{\theta o}(f) = 10log\left\{\frac{f_{ref}}{12(f)^2} \cdot \left|H_{NTF}\left(e^{j2\pi f/f_{ref}}\right)\right|^2\right\}\ dBc/Hz \quad (4.47)$$

From the above discussion, it has been found that output of PLL completely depends upon the SDM quantization noise, which is mapped with other noise sources. These expressions are used to determine and minimize the phase noise in the feedback loop.

4.6.2 Mapping of SDM Noise and Jitter

Phase error of SDM is given as:

$$f_c < \left[\left(\frac{\theta_{rms}}{\sqrt{2}}\right)^2 \cdot \frac{L+0.5}{(2\pi)^{2L}}\right]^{1/(2L-1)} \cdot f_{ref} \quad (4.48)$$

where,

L = The order of $\sum\Delta$ modulator

It is very difficult to find phase error of SDM, because that error also consists of feedback loop error and divider error. Therefore, hybrid mechanism is used to minimize that type of error in the proposed system.

4.6.3 Charge Pump PLL and its effect

Charge pump is a device that is used to convert output of the phase difference into corresponding current pulses to control VCO output. It consists of P_0 (p-type) and N_0 (n-type) MOSFET to their current sources I_p and I_n. These sources produce constant current I_0. Turn on-off of P_0 and N_0 are determined by charging and discharging of the capacitor. A –ve pulse size of P_0 & +ve pulse size of N_0 should be too small to maintain locked condition of PLL. Pulse width of P_{INC} & P_{DEC} are controlled to charge and discharge capacitor to fulfil essential requirements of system.

This work has considered a PLL with type II and order of II that are fairly standard values for practical PLLs. Therefore, as shown in figure 4.5, equation of loop filter will be in the following form:

$$Z(s) = K\frac{1+s/\omega_z}{s(1+s/\omega_p)} \quad (4.49)$$

where,

$K = 1/(C_1 + C_2),\ \omega_z = 1/RC_1\ , \omega_p = (C_1 + C_2)/RC_1C_2.$

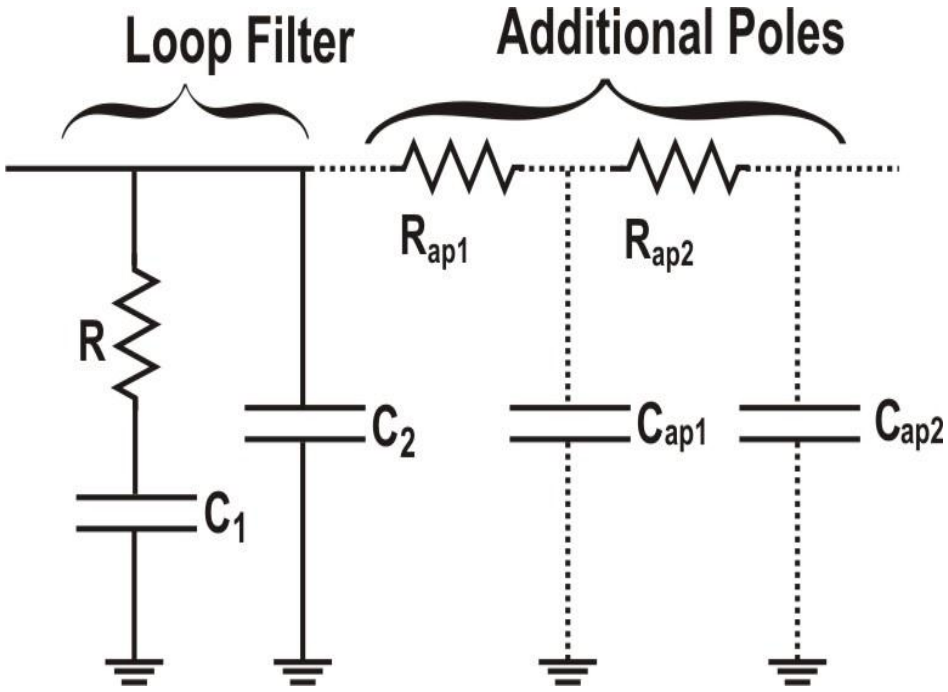

Figure 4.5: Filter with two additional poles

This loop filter is convenient in almost every application where PLL is being used because it does not require high complexity to obtain higher order type.

The proposed technique takes into account only changes in system frequency which are due to minute variations in divide value. If value is huge then cycle slip can occur and thereby it can invalidate the proposed modelling assumptions. It has been discussed in this section that quantization noise may be removed by low pass filter so that accumulation of complementary poles in the filter ought to help in reducing the noise source in the system bandwidth. These poles will also have the effect of attenuating reference spur that will appear in the output spectrum at frequency offset. Frequency offset and input reference reinforce the desire to use the additional pole. Choice of frequency of these poles is fairly arbitrary but the major limitation is parasitic pole

frequency must be a multiplier of ten more than the system bandwidth which will permit adequate pole positioning in the dominant poles of system. These additional poles are easy to implement by using cascading base low-pass filter with one or more RC filters as shown in figure 4.5 by dashed lines. From the above discussion, it is found that loop filter equation modifies with its corresponding additional poles.

4.6.4 Phase Noise Analysis

From equation (4.50), it is obvious that the complete output noise is sum of each spectrum density and power of transfer function of each noise source. Figure 4.6 shows a calculation of individual source noises. In this figure, phase detector noise represents the sum of charge-pump noise and input reference phase noise. In low offset frequencies, the effect of detector noise is dominant that confirms the input reference transfer term mentioned in figure 4.6. Quantization noise in small range of frequency affects the total phase noise because of the use of two parasitic poles in the end of loop filter. In high offset frequencies, the effect of VCO noise is dominant. This observation is confirmed by noting the transfer terms of this noise source at high offset frequencies having more value than input reference and divider noise.

This work describes VCO input voltage at steady state that seems to be a noisy signal. It observes hard random variation around the process. These variations contribute into the output phase noise through the VCO. In other words, small and fast changing on VCO input voltage causes large and fast change of the output frequency of PLL. High VCO gain causes high sensitivity of output frequency to the input voltage i.e. small changing on VCO input voltage converts to large change of output frequency.

Considering above limitations, it is necessary to employ a mechanism for smoothening the variations. For smoothening the variation of input voltage of VCO, there is a need to use new technique that can limit and reduce the phase noise of the system.

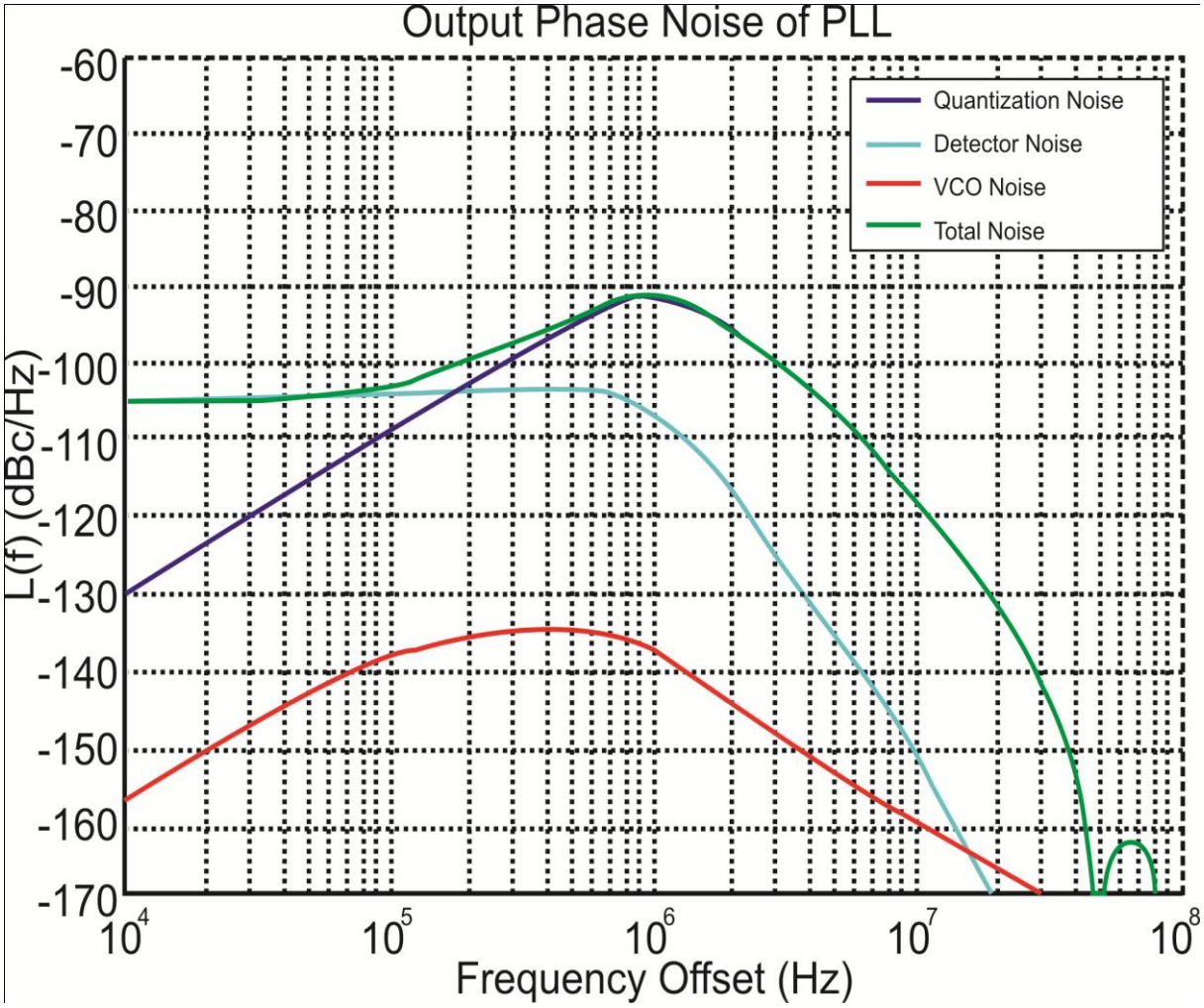

Figure 4.6: Source of noises of conventional system

For that a fractional SDM PLL can be designed to reduce the noise for the better performance of the communication system.

Since these noise sources are not correlated and proposed model is linear, output phase noise PSD is calculated by multiplying input PSD of noise sources with associated square of closed-loop transfer function. The product of the same determines the ability of system to terminate phase noise. If $S_{\varphi-source}(f)$ and $S_{source}(f)$ corresponds to PSD and transfer function of each noise source respectively, then by using superposition theorem, the total output phase noise will be as follows:

$$S_{\varphi-output}(f) = S_{\varphi-ref}(f) \cdot |F_{ref}(f)|^2 + S_{\varphi-fil}(f) \cdot |F_{fil}(f)|^2 + S_{\varphi-vco}(f) \cdot |F_{VCO}(f)|^2 + S_{\varphi-div}(f) \cdot |F_{div}(f)|^2 \quad (4.50)$$

Table 4.2: Sources of noise of conventional system

Frequency(Hz)	Total Noise(dBc/Hz)	VCO Noise(dBc/Hz)	Detector Noise(dBc/Hz)	Quantization/SDM Noise(dBc/Hz)
1 kHz	-105	-155	-105	-130
10 kHz	-103	-138	-104	-91
100 kHz	-93	-137	-108	-95
10 MHz	-119	-158	-150	-119
100 MHz	-156	-167	-166	-151

Noise sources of various components have been calculated using simulation tool. The basic details and their transfer function of each components have already been described in chapter one. The summery of phase noise of the conventional PLL has been presented in table 4.2. How to minimize those noise, a novel architecture of fractional SDM PLL has been presented in the next section.

4.7 ANALYSIS OF FRACTIONAL-N PLL

This work has proposed fractional sigma delta modulator PLL. Sigma delta modulator is the main component in this architecture. It is a device that is used to compensate divider ratio which is at elevated pace as compared to system BW. This overtime is utilized to divide frequency into fractional value. SDM provides wide band width to reduce phase noise and spur. It also improves the phase resolution of system. Phase resolution can be determined by accumulator length of SDM. It can also be utilized to overcome spurious level with the help of quantization noise mapping. Low pass filter is used to carry out quantization noise for synthesizer. This modulator uses third order transfer function and 5 bits output to design the application. High frequency is divided by divide ratio using

SDM for the further uses. Low pass filter is used to filter out required output frequency [142]-[148].

4.7.1 Design approach of PLL

2^{nd} & 3^{rd} order SDMs are basically utilized for fractional-N PLL. 4^{th} or higher order is not generally used due to their complexity. These modulators are not also competent to contain noise at high frequency. 2^{nd} order modulator is restricted for few topologies because divide rate is high as compare to bandwidth but third order modulator is used in all most the topologies; therefore it is being used in proposed architecture.

This architecture includes filter, detector, sigma delta modulator, and composite block, which is shown in figure 4.7.

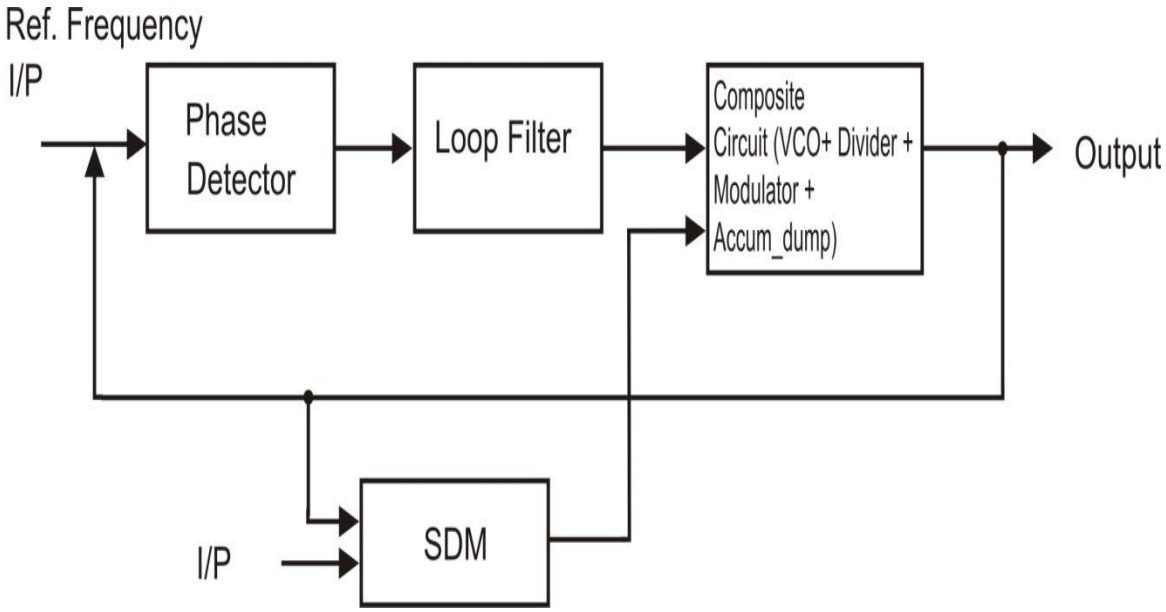

Figure 4.7: Architecture of fractional PLL

The main part of the architecture is composite block. It consists of accum_dump, VCO, divider and gain. Accum_dump has been utilized for decimation of the average output which results in quick simulation response. Composite block returns input with its average value during time of clocking that are shown in figure 4.7 & 4.8. Average value is varied according to the clock apply to it. If clock period is longer, average interval will

be larger. Let us assume that firstly it is in unlocked condition and later it will reach in locked condition. Before locking, period must be short to get into locked condition for which a mechanism is provided to maintain above condition. VCO, SDM, gain, reference input, and clock have been coordinated to each other to achieve smooth output corresponding to reference input. The gain is also adjusted to randomize divider value in closed loop. The main role of divider is to divide out signal by numeric value as per requirement of the system.

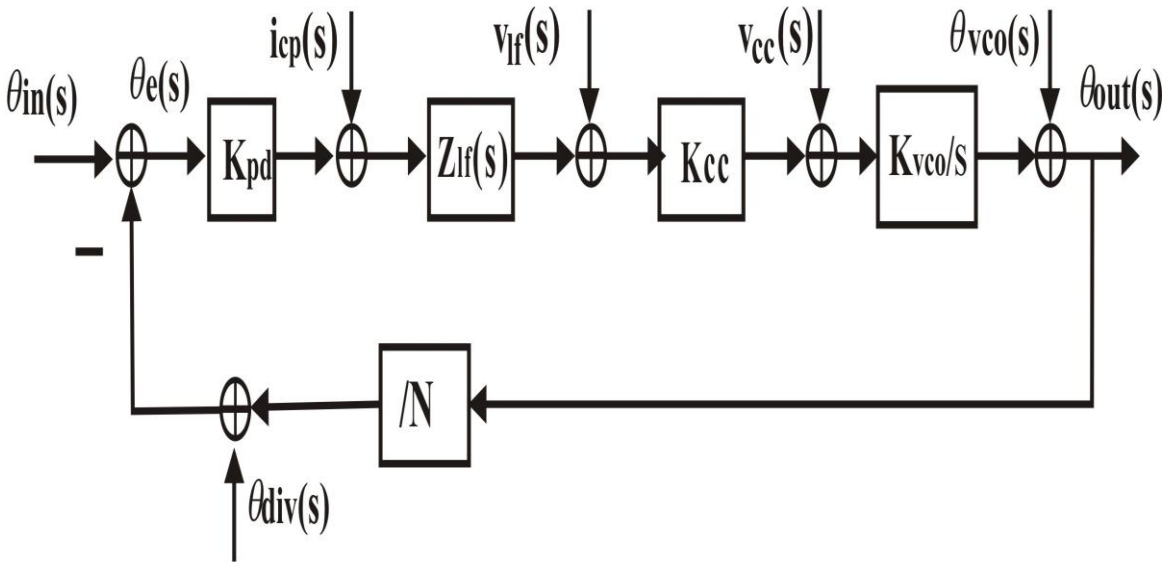

Figure 4.8: Block diagram of fractional PLL

The phase noise output also depends upon order of the SDM, gain, and other additional components which have been used in fractional architecture. Mathematical analysis of figure 4.8 is described here which is incorporated with their simulation results. Various variables and constants have been assumed to find phase, voltage, and noise at output.

Open loop phase noise transfer functions may be expressed as:

$$H_{ol}(s) = \frac{K_{fpd}\, K_{cc}\, K_{vco}\, Z_{lpf}(s)}{N \cdot s} \tag{4.51}$$

where

K_{vco} =VCO Gain

K_{fpd} = Gain of PFD

K_{cc} = Gain of composite circuit

z_{lpf} = Trans-impedance of filter

N = Frequency division ratio

$H_{ol}(s)$ = Open loop transfer function

Closed loop phase noise transfer functions may be calculated as:

$$H_{cl}(s) = \frac{H_{ol}(s)}{1+H_{ol}(s)} \tag{4.52}$$

where

$H_{cl}(s)$ = Closed loop transfer function

Transfer function of input noise is ratio of output and input noise that depends upon reference input and divider output as:

$$\mathrm{H_{IN}}\,(\mathrm{s}) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_{vco}}{s} \cdot \frac{1}{1+H_{ol}(s)} \tag{4.53}$$

where

θ_{in} =Input PN

θ_{out} = Output PN

The phase noise of PFD depends upon gain of detector and value of divider as under:

$$\mathrm{H_{PFDN}}(\mathrm{s}) = \frac{\theta_o(s)}{i_{cp}(s)} = \frac{N}{K_{fpd}} \cdot \frac{H_{ol}(s)}{1+H_{ol}(s)} \tag{4.54}$$

where

$i_{cp}(s)$ = Current noise originated by PFD/CP

The gain of the filter is proportional to overall gain and loop parameters. Transfer function of LF noise is given as:

$$\mathrm{H_{LFN}}(\mathrm{s}) = \frac{\theta_o(s)}{v_{lf}(s)} = \frac{K_{vco}}{s} \cdot \frac{1}{1+H_{ol}(s)} \tag{4.55}$$

where

$v_{lf}(s)$ = VN

Composite block is a circuit that returns input with its average value during time of clocking. This value is varied corresponding to clock, SDM output, divider, and gain apply to it. The gain is also adjusted to randomize divider value in closed loop. Transfer function for the same as under:

$$\mathrm{H_{CCN}(s)} = \frac{\theta_o(s)}{v_{cc}(s)} = A \cdot \frac{H_{ol}(s)}{1+H_{ol}(s)} \quad (4.56)$$

where

$A = \ Gain \ * N * Constant$

A = Gain of accum_dump

The output of composite circuit and VCO provided smoothen variation to the system. High VCO gain causes high sensitivity of output frequency to the input voltage i.e. small changing on VCO input voltage converts to large change of output frequency. Transfer function of VCO noise may be calculated as:

$$\mathrm{H_{VCOnoise}(s)} = \frac{\theta_o(s)}{\theta_{vco}(s)} = H_{cc}(s).\frac{1}{1+H_{ol}(s)} \quad (4.57)$$

where

$\theta_{vco}(s)$= VCO output PN

$\mathrm{H_{CCN}(s)}$ = Transfer function of composite circuit

Divider phase noise depends upon the output of VCO and their component. Transfer function of divider noise is given as:

$$\mathrm{H_{DIVN}(s)} = \frac{\theta_o(s)}{\theta_{div}(s)} = -N \cdot \frac{H_{ol}(s)}{1+H_{ol}(s)} \quad (4.58)$$

where

$\theta_{div}(s)$ = Phase noise by DIV

These derivations have been incorporated with simulation results and which helps to calculate various parameters like phase noise, output voltage, divide ratio etc. Simulation results of this system have been presented in next sub section.

4.7.2 SIMULATION RESULTS AND DISCUSSION

The various parameters of the proposed fractional PLL have been analyzed using CPPSIM simulation tool in this section.

The specifications for output phase noise are as follows:

Dynamic parameters:

- Bandwidth f_0=100 kHz
- Order = 2
- Shape = Butterworth
- Type = 2 with $f_z/f_o = 1/8$

Open loop parameters:

- $k = 3.272\ e + 010$
- $f_p = 2.173\ e + 005\ Hz$
- $f_z = 1.250\ e + 004\ Hz$

Noise parameters:

- Reference Frequency = $26\ MHz$
- Output Frequency = 900 MHz
- Detector = $-\ 95\ dBc/Hz$
- VCO = $-\ 165\ dBc/Hz$
- Frequency offset =$20\ MHz$
- SDM order = 3

Simulation results of synthesizer using a charge pump detector are as follows.

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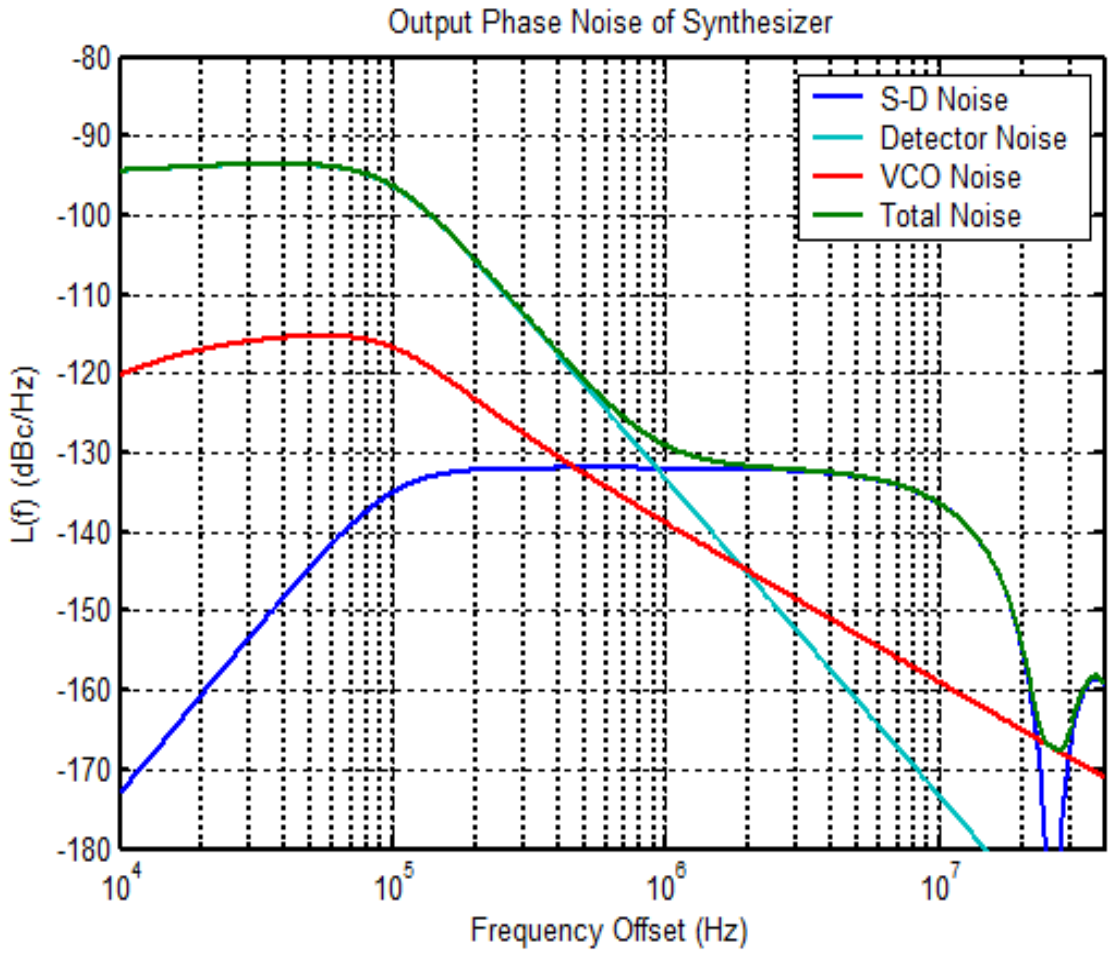

Figure 4.9: Output phase noise at reference frequency 26 MHz & band width 100 kHz

Dynamic parameters:

- Bandwidth f_0=100 kHz
- Order = 2
- Shape = Butterworth
- Type = 2 with $f_z/f_o = 1/8$

Open loop parameters:

- $k = 3.272\ e + 010$

- $f_p = 2.173\ e + 005\ Hz$
- $f_z = 1.250\ e + 004\ Hz$

Noise parameters:

- Reference Frequency = 30 MHz
- Output Frequency = 900 MHz
- Detector = $-95\ dBc/Hz$
- VCO = $-165\ dBc/Hz$
- Frequency offset =20 MHz
- SDM order = 3

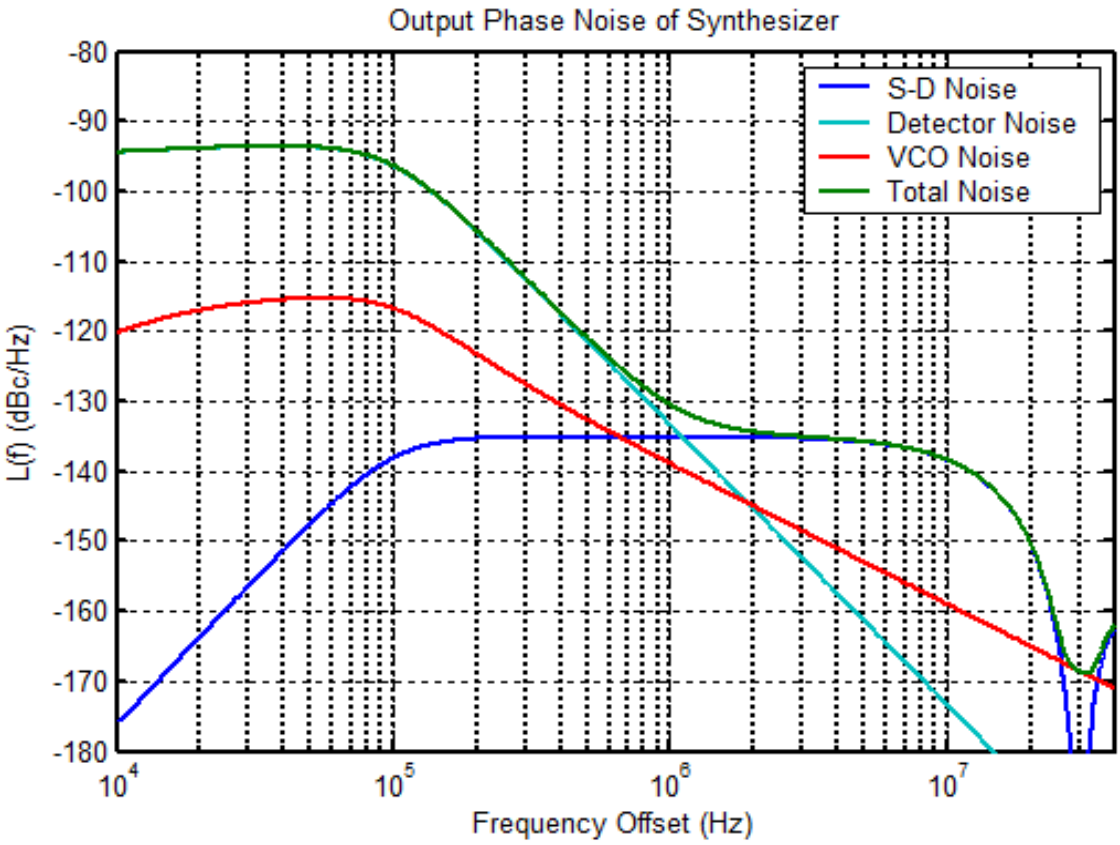

Figure 4.10: Output phase noise at reference frequency 30 MHz & band width 100 kHz

Dynamic parameters:

- Bandwidth f_0=120 kHz
- Order = 2
- Shape = Butterworth
- Type = 2 with $f_z/f_o = 1/8$

Open loop parameters:

- $k = 3.272\ e + 010$
- $f_p = 2.173\ e + 005\ Hz$
- $f_z = 1.250\ e + 004\ Hz$

Noise parameters:

- Reference Frequency = 26 MHz
- Output Frequency = 900 MHz
- Detector = $-95\ dBc/Hz$
- VCO = $-165\ dBc/Hz$
- Frequency offset =20 MHz
- SDM order = 3

From figures 4.9 & 4.10 it has been found that phase noise is varied in accordance with the reference frequency and bandwidth which are used in application. It is also varied with their order of filter and SDM. The PFD, VCO, phase noise of VCO, SDM, and total phase noise have been compared as shown in table 4.3.

Table 4.3: Output phase noise at reference freq. (26 MHz) and bandwidth (100 kHz)

Frequency(Hz)	Total Noise(dBc/Hz)	VCO Noise(dBc/Hz)	Detector Noise(dBc/Hz)	Quantization/SDM Noise(dBc/Hz)
1 kHz	-95	-120	-95	-172
10 kHz	-97	-116	-96	-133
100 kHz	-129	-143	-132	-132
10 MHz	-137	-159	-171	-136
100 MHz	-167	-166	-178	-165

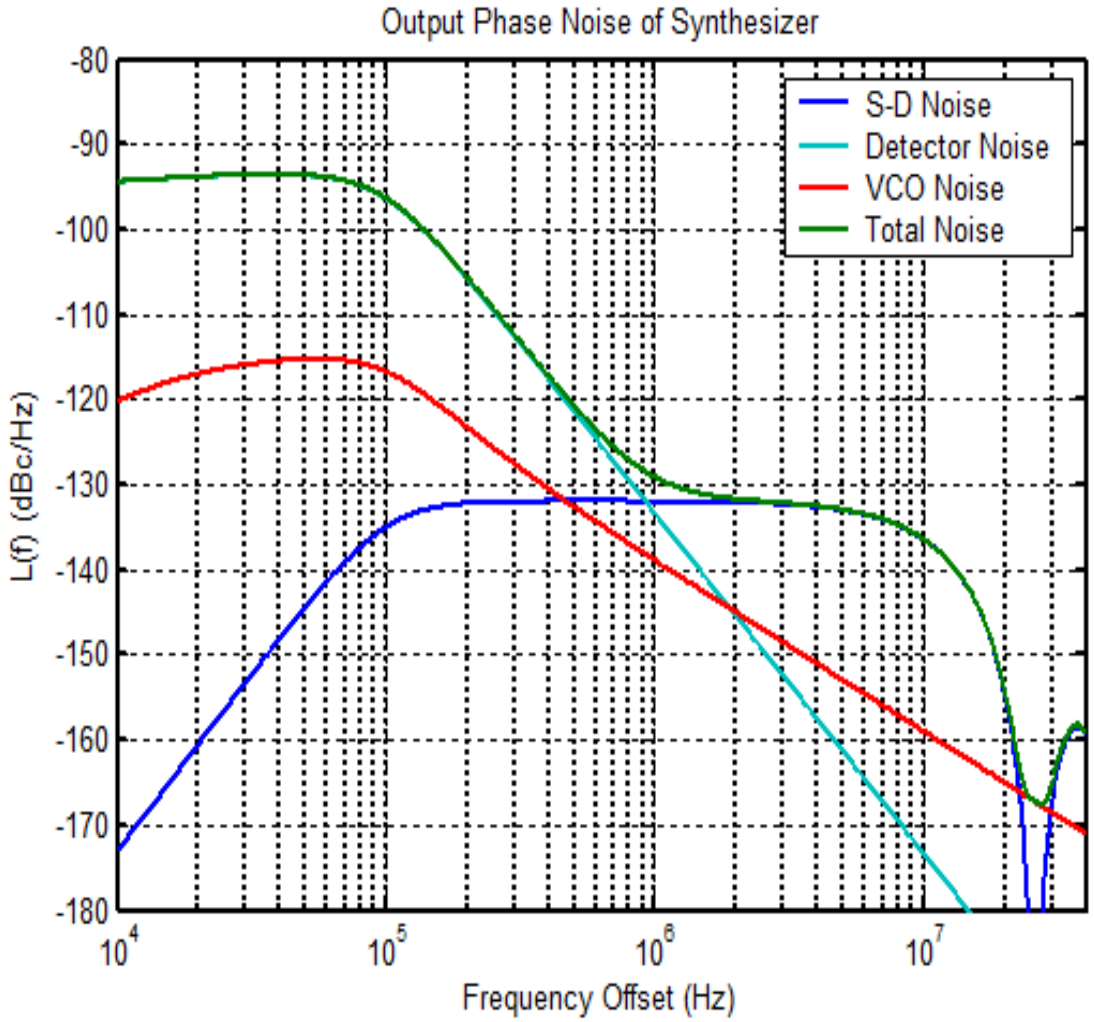

Figure 4.11: Output phase noise at reference frequency 26 MHz & band width 120 kHz

Dynamic parameters:

- Bandwidth f_0=120 MHz
- Order = 2
- Shape = Butterworth
- Type = 2 with $f_z/f_o = 1/8$

Open loop parameters:

- $k = 3.272\ \mathrm{e} + 010$
- $f_p = 2.173\ \mathrm{e} + 005$ Hz
- $f_z = 1.250\ \mathrm{e} + 004$ Hz

Noise parameters:

- Reference Frequency = 30 MHz
- Output Frequency = 900 MHz
- Detector = -95 dBc/Hz
- VCO = -165 dBc/Hz
- Frequency offset = 20 MHz
- SDM order = 3

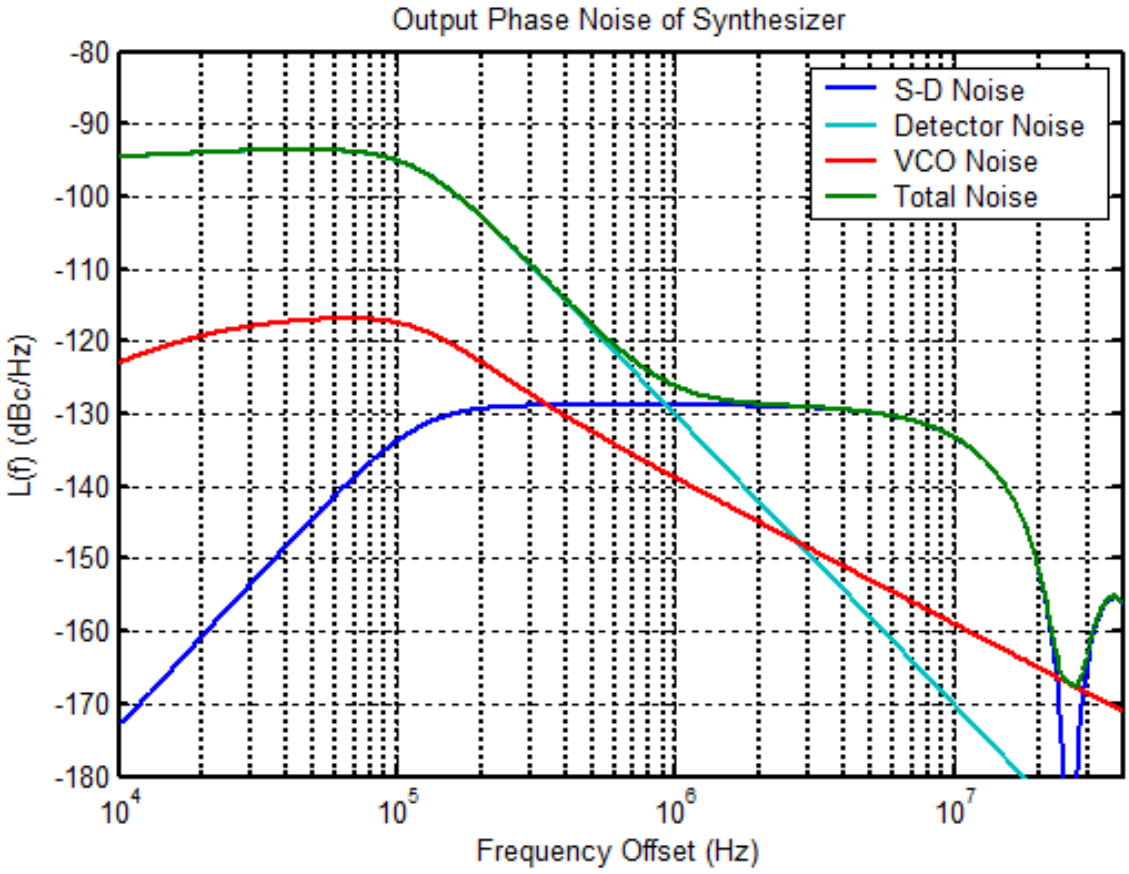

Figure 4.12: Output phase noise at reference frequency 30 MHz & band width 120 kHz

Table 4.4: Total phase noise at various reference frequency and bandwidth

Frequency (Hz)	**Total Phase Noise (dBc/Hz)**			
	Ref. Freq. (26 MHz) & f_0 (100 kHz)	Ref. Freq. (30 MHz) & f_0 (100 kHz)	Ref. Freq. (26 MHz) & f_0 (120 kHz)	Ref. Freq. (30 MHz) & f_0 (120 kHz)
1 kHz	-95	-94	-94	-94
10 kHz	-97	-96	-96	-95
100 kHz	-129	-130	-131	-128
10 MHz	-137	-137	-136	-133
100 MHz	-167	-169	-168	-168

From the table 4.4, it has been found that values of parameters and additional component play important role to minimize phase noise at out of the fractional PLL. The comparison of output phase noise at various reference frequency and bandwidth has been presented in figure 4.11 and figure 4.12.

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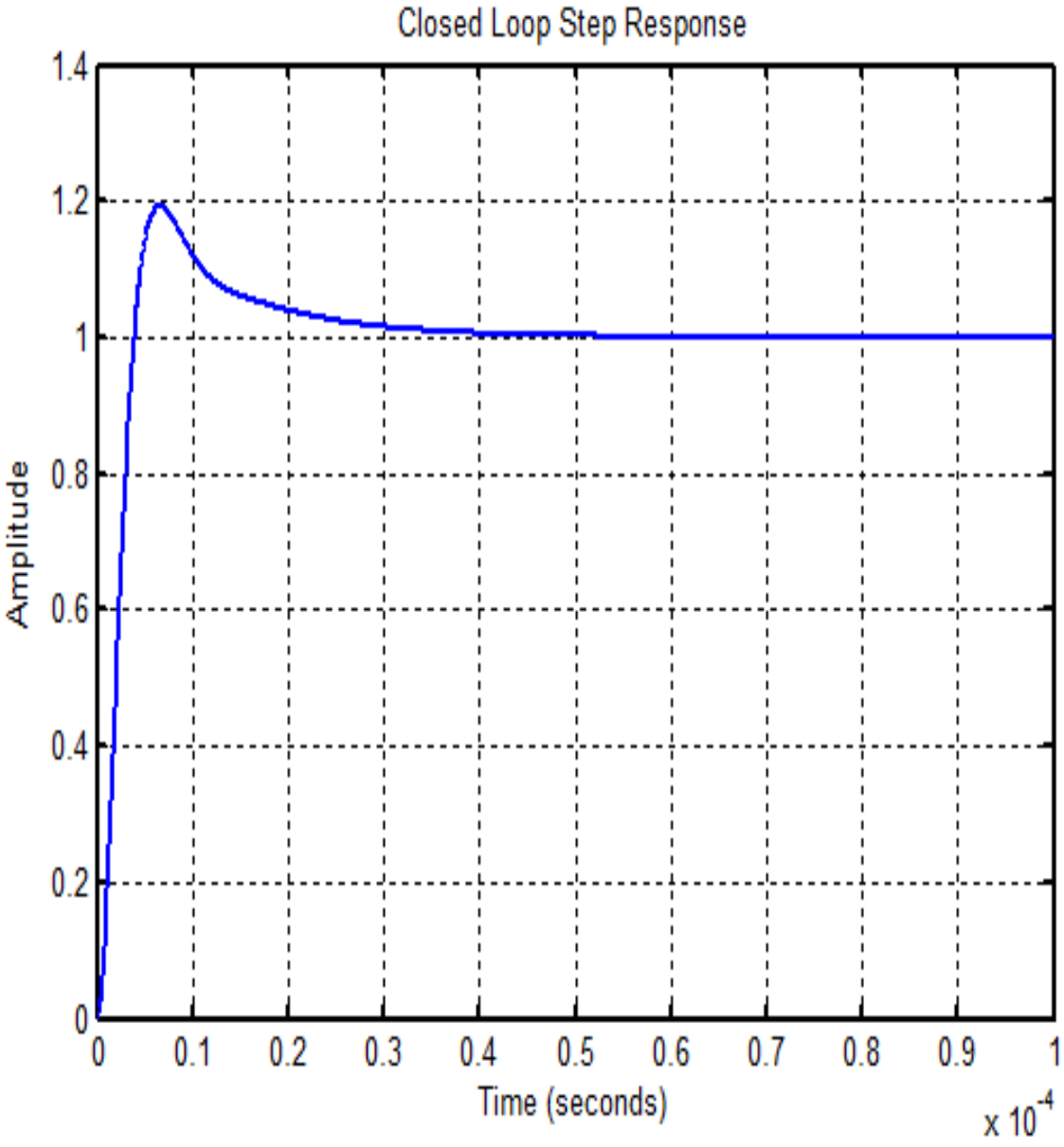

Figure 4.13: Closed loop step response of PLL

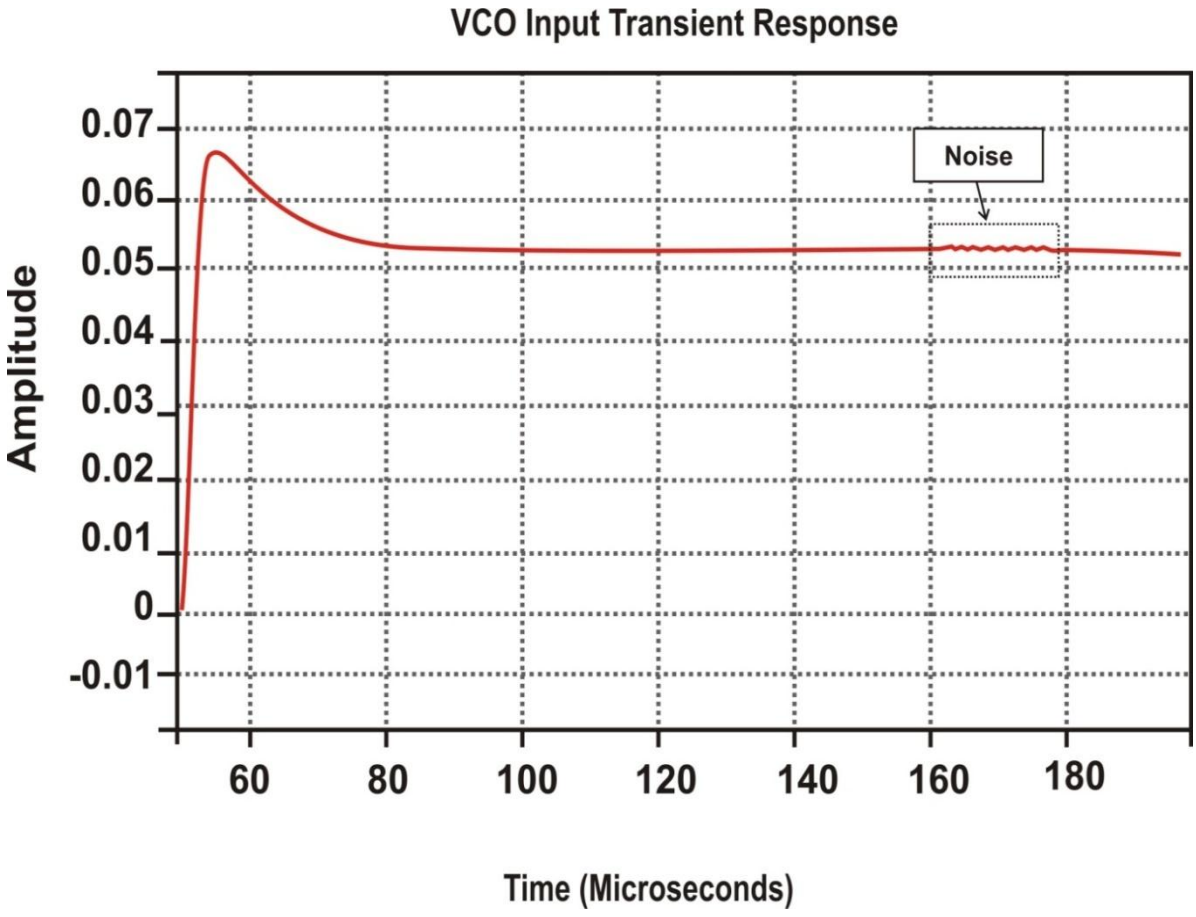

Figure 4.14: Input transient response of VCO

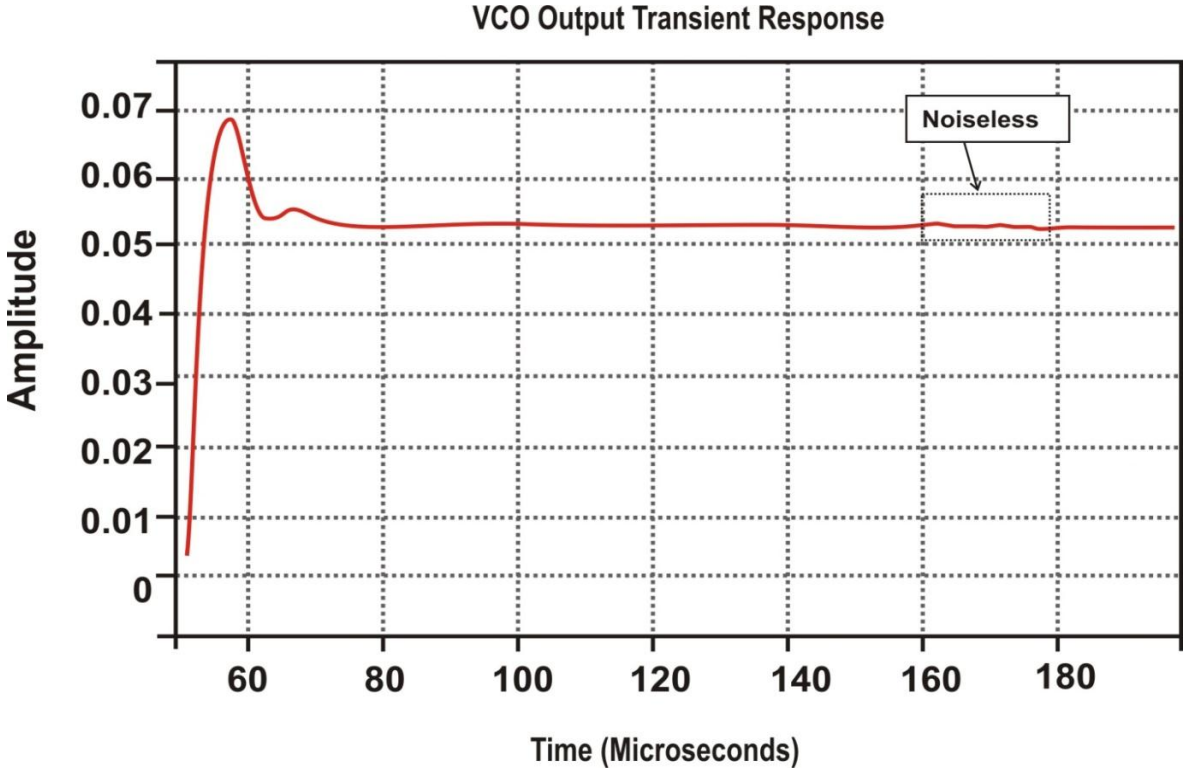

Figure 4.15: Output transient response of VCO

The output of phase noise depends upon order of filter and SDM. Considering previous limitations, a mechanism has already been implemented for smoothening the variations of VCO voltage. Figure 4.13 shows closed loop response of the fractional PLL. Noise region of input VCO voltage has been presented in figure 4.14, which occurs due to hard variation of VCO input. After implementation of proposed mechanism, noiseless transient response has been presented in figure 4.15 which shows that output variation is smooth as compared to conventional architecture.

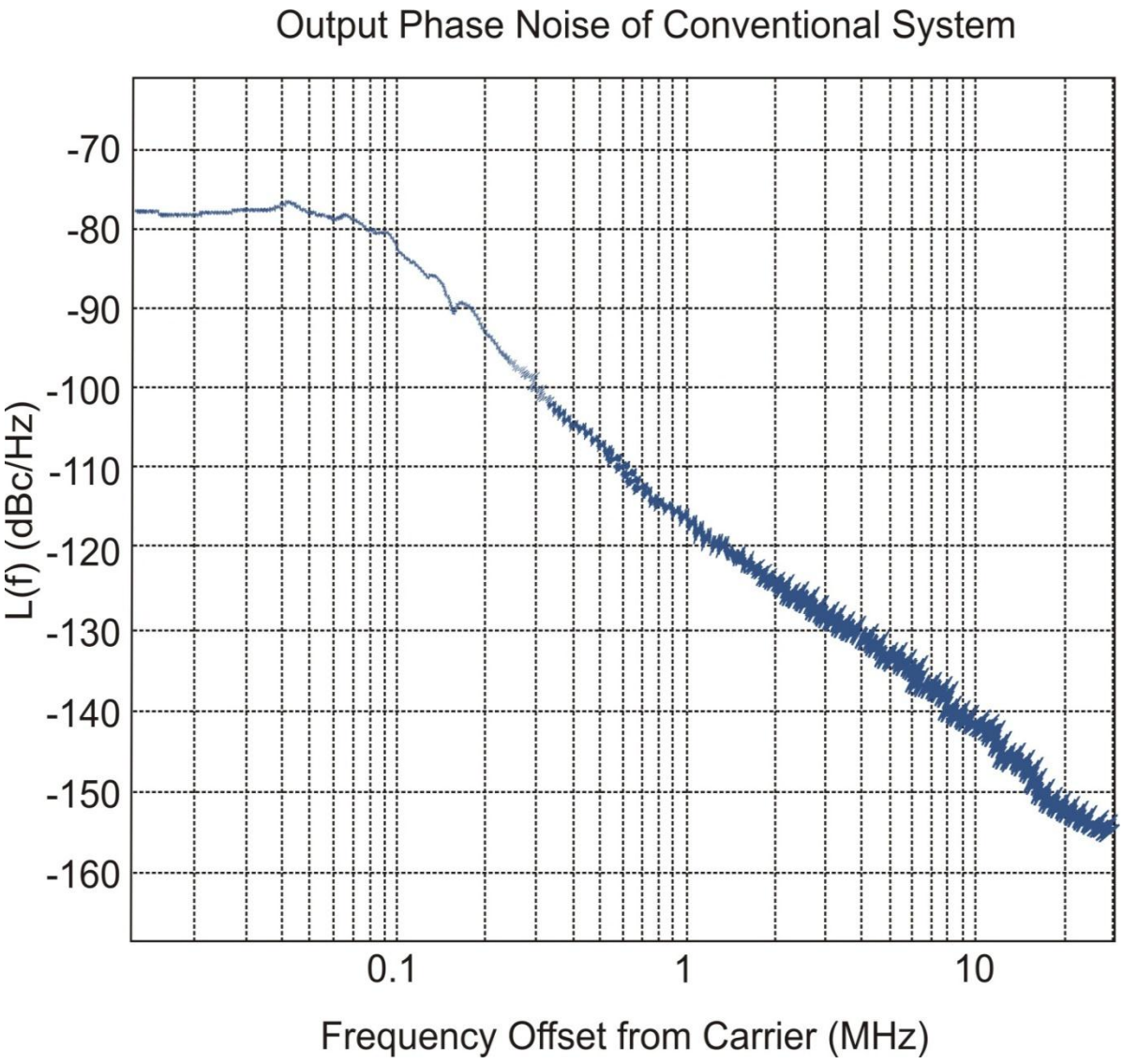

Figure 4.16: Output phase noise of conventional system

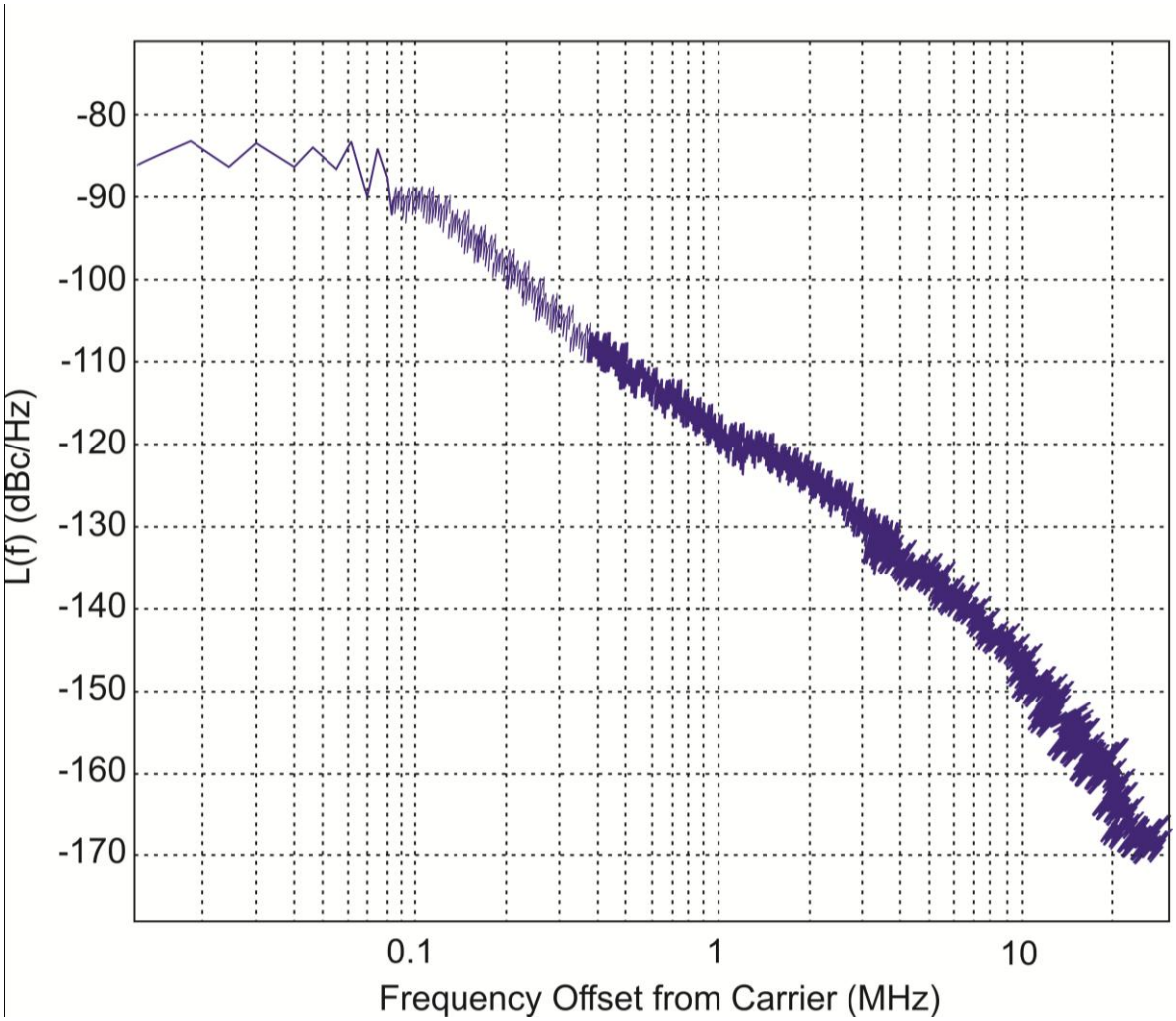

Figure 4.17: Output phase noise of proposed system

Table 4.5: Comparison output phase noise of conventional and proposed architecture

Frequency (Hz)	Phase Noise in Conventional System (dBc/Hz)	Phase Noise in Proposed System (dBc/Hz)
10 kHz	-78	-88
100 kHz	-82	-91
1 MHz	-118	-120
10 MHz	-142	-149
100 MHz	-158	-169

The comparison of phase noise of conventional and proposed architectures have also been calculated in table 4.5. After analyzing output phase noise at various frequencies, it has been found that proposed work improved the performance of fractional PLL in terms of phase noise. Figures 4.16 and 4.17 shows phase noise responses of conventional and proposed system respectively. Finally, after comparison output phase noise has been reduced from -158 dBc/MHz to -169 dBc/MHz at 20 MHz offset. The proposed behavioural simulation results show improvement of around 11 dBc/Hz. The above comparative results show that proposed technique is superior to existing techniques.

4.8 SUMMERY OF THE CHAPTER

This work proposed fractional frequency synthesizer to minimize noise. This work also presents noise contribution of third order modulator. Transfer Function of various phase noise and output phase noise have been derived and calculated. Based on these calculations, a new architecture has been described with a behavioural model for reduction of phase noise using CPPSIM simulator. The proposed results show improvement of around 6.5%. In future, this technique can also be implemented in hybrid PLL. In the next chapter, the conclusion and future scope of the thesis has been presented.

CHAPTER 5

CONCLUDING REMARKS WITH FUTURE SCOPE

5.1 CONCLUDING REMARKS

In this research work, the efficient structures of the frequency synthesizers have been proposed using various techniques. These techniques are used to improve the performance of frequency synthesizers at different frequencies.

A new architecture of the PLL has been proposed to reduce phase noise that finds applications in global system for mobile communication (GSM), modulation, demodulation, clock recovery etc. The transfer functions of individual source noise and output phase noise have been calculated by considering the locked condition of PLL linear model. The phase noise is now reduced to 33.33% at 1 Hz, 7.3% at 100 Hz and 19% at 100 kHz which show improved performance of proposed architecture as compared to existing techniques.

An optimized DDFS utilizing piecewise linear approximation has also been proposed. Proposed technique allows successive read access to memory cells per one clock cycle using time sharing. The output values will be temporarily stored and read at a later time. The reconstructed signal has been obtained from the output of this proposed system which is superior approximation of the preferred signal. As a result, the DDFS only needs to store fewer coefficients and the hardware complexity is significantly reduced by approximately 26.78 %. The emphasis is on designing the ROM compression algorithms along with paradigm equations mandatory to produce the perfect sine wave pattern for given input and output bit size. The work has analyzed the problem related to the most favorable coefficient option & well-organized execution of system with piece-wise polynomial estimation. In this work, a novel ROM elimination technique has been

presented for application in low complex high spectral purity DDFS. Unlike many reported architectures, which used complex circuits to compute sine samples, the proposed technique uses only 32 points from a standard sine LUT with requirement of fewer registers. System complexity has been greatly reduced approximately 16 % by using an efficient phase to amplitude conversion architecture. The technique has been compared with the existing techniques in terms of storage reduction computation and spectral purity. The proposed DDFS has been analyzed using MATLAB. The results obtained show improvement of around 1.43 % in SFDR over existing results.

Moreover, the design technique has been proposed for DDFS system with high spectral purity which has been optimized for speed and phase accuracy using a combination of Lagrange interpolation and quasi-linear methods. Resulting hardware is less complex, primarily because of the use of better parabolic interpolation based on Lagrange's technique and also by using quasi-linear methods. Resulting waveforms further demonstrated accuracy of the design. In continuation of the above work, fractional SDM PLL has been proposed to reduce phase noise that calculates noise contribution of third order modulator. Transfer function of every source of PN and output PN have been derived and calculated. Phase noise is obtained lies in between from -158 dBc/MHz to -169 dBc/MHz at 20 MHz offset by behavioural modeling using CPPSIM simulator. The results obtained show improvement of around 6.5% in phase noise over existing results.

5.2 FUTURE SCOPE

In the aforementioned research work, new architecture of PLL, DDS, and fractional PLL have been proposed and simulated. Lagrange interpolation, quasi linear methods, and other techniques have been presented and implemented which are useful in wireless communication, different standards, and other engineering applications. Complexity in hardware implementation is found to be in trade-off relationship with efficiency of

presented PLL structures. Therefore, the future work includes designing and development of hybrid architecture based low cost, low power, and highly efficient PLLs structures, which can support the high frequency fractional analysis. In future, DDS based PLL hybrid frequency synthesizer can also be designed for high speed communication applications which is the need of current industries.

LIST OF PUBLICATIONS

[1] G. S. Patel and S. Sharma, "Parametric analysis to reduce phase noise of frequency synthesizers for wireless communication system," *Int. J. of Wireless Personal Commun., Springer,* vol. 75, no. 2, pp. 1295-1306, October 2013. (SCI Indexed by Thomson Reuters; Impact Factor = 0.653).

[2] G. S. Patel and S. Sharma, "Parametric analysis of a novel architecture of Phase Locked Loop for communication system," *Int. J. of Wireless Personal Commun., Springer*, vol. 77, no. 2, pp. 1271-1285, December 2013. (SCI Indexed by Thomson Reuters; Impact Factor: 0.653).

[3] G. S. Patel and S. Sharma, "FPGA-Nanotechnology Based DDS Analysis and Implementation," *J. of Computational and Theoretical Nano-Sciences, American Scientific Publishers, USA*, vol. 10, no. 10, pp. 2458-2461, October 2013. (SCI Indexed by Thomson Reuters; Impact Factor = 1.343).

[4] G. S. Patel and S. Sharma, "FPGA-Nanotechnology based Analysis, design and Implementation of ADPLL," *J. of Computational and Theoretical Nano-Sciences, American Scientific Publishers, USA*, vol. 11, no. 7, pp. 1-7, November 2014. (SCI Indexed by Thomson Reuters; Impact Factor = 1.343).

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