

Thesis
On
“Analysis and Design of Comparator for Bio-Medical Applications”

Submitted towards the partial fulfillment of requirement for the award of degree of

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In

VLSI Design

Submitted by

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**ELECTRONICS AND COMMUNICATION ENGINEERING
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DECLARATION

I hereby declare that the project report entitled "Analysis and Design of Comparator for Bio-Medical Applications" is an authentic record of my work carried out as a partial requirement for the award of degree of M.Tech. (VLSI Design) at Thapar University, Patiala, under the supervision of Dr. Alpana Agarwal, Associate Professor, ECED and refers other researcher's work which are duly listed in reference section.

The matter embodied in this thesis has not been submitted for award of any other degree at this or any other university.

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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ABSTRACT

SAR-ADC is best suited for low power applications where power has a trade-off with speed. Comparator is one of the core components of SAR-ADC that introduces error voltage due to mismatch and consumes large power.

This work presents the analysis of various comparators which are there in market and a new comparator has been designed which is optimized to achieve smaller size and less power. All this work is primarily focused for the Bio-Medical Applications and hence the operational parameters are selected accordingly. EDA tool used for design and analysis is Cadence® Virtuoso Analog Design Environment with 180nm technology.

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Recent advances in integrated circuit (IC) technology and innovations in circuit design techniques, have led to systems with processing capabilities that can supplement and can even entirely replace, complex biomedical operations such as hearing aid, pacemaker etc.

The processing capabilities of ICs are virtually unlimited, but energy, in biomedical electronics, is highly limited. This makes the designing for biomedical applications more challenging. A conceptual diagram for a generic biomedical device is shown in Figure 1. The core components of the device are shown, which include data conversion, signal processing, and communication subsystems, and these interface with the biomedical environment through sensors and actuators.

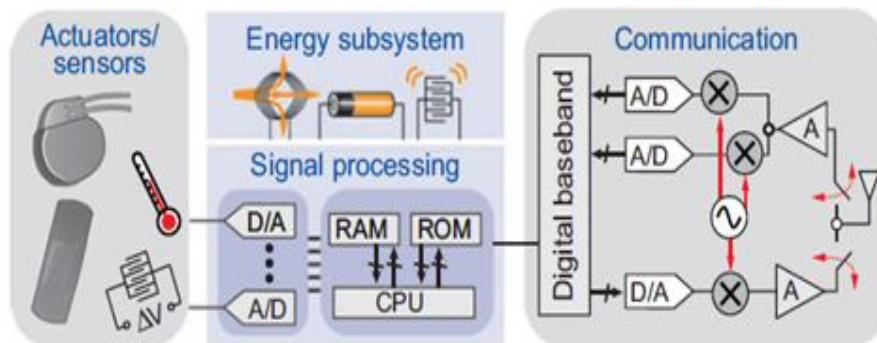


Figure-1 Conceptual Diagram of a Generic Biomedical Device

As seen from the diagram A/D(analog to digital converter) is a important part of all biomedical devices. An analog to digital converter(ADC) is the gateway that provides the link between the analog and the digital world. ADC is a mixed signal device that plays a crucial role in the performance of any system that interfaces with the real world as it converts analog signals, be voltage or current to recognizable digital equivalents that can be analog signal that further worked upon by the digital backend.

Digital computing power has exponentially increased at ever smaller incremental costs over the last few decades. With this powerful abundance, many applications formerly performed with analog are being performed in digital realm whereas the real-world applications are still analog. To bring digital processing to real world applications, the analog signal of interest must be translated into a digital format. This is the function of Analog to Digital converter.

Physical biomedical signals are analog, therefore an ADC is required before they can be processed digitally to take advantage of the sophisticated capabilities of a digital signal processor (DSP). The data being processed by the DSP depends directly on the performance of the ADC. According to performance requirements (resolution, sampling rate) and power consumption, a proper ADC architecture should be carefully chosen and design to meet the performance with the minimum power consumption. Figure 2.1 shows a representation of the functioning of a typical ADC.

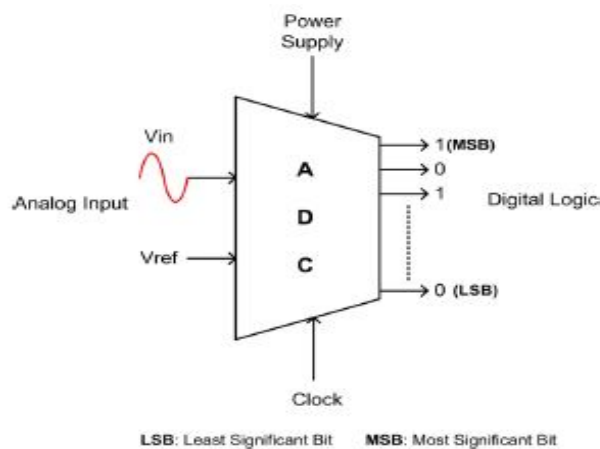


Figure 2.1 Representation of a Typical ADC

An analog signal is applied at the input port of the converter, while a reference signal is applied to the reference port. The output ports of the converter show the digital form of the analog signal that analog signal that has been processed.

To achieve the ultra low power and small size operation of ADC for biomedical devices, the circuitry should be as simple as possible, which means additional circuits such as calibration should not be introduced since it will consume more power; the supply voltage should be as low as possible so that the circuits can operate in sub-threshold region to save power.

In all analog to digital converters it is necessary to first sample the input, the sampled input is then applied to combinations of comparator to determine the digital equivalent of the analog signal.

Various types of ADC are given in literature and they are used according to the intended application. Most popular architectures are:

Flash ADC

Pipelined ADC

Sigma-Delta ADC

Successive Approximation Register ADC

FLASH ADC, is a parallel A/D converter. It uses a series of comparators where each comparator compares input voltage to a different reference voltage. They are the fastest way to convert an analog signal to a digital signal. They are suitable for applications requiring very large bandwidths. However, flash converters consume a lot of power, have relatively low resolution, and can be quite expensive.

PIPELINED ADC divides the conversion task into several consecutive stages. Each of these stages consists of a sample and hold circuit, an m-bit ADC and an m-bit Digital to Analog converter (DAC). First the sample and hold circuit of the first stage acquires the signal. The m-bit flash converter then converts the sampled signal to digital data. The conversion result forms the most significant bit of the digital output. This same digital output is fed into the DAC, and its output is subtracted from the original sampled signal.

The residual analog signal is then amplified and sent on to the next stage in the pipeline to be sampled and converted as it was in the first stage. This process is repeated through as many stages as are necessary to achieve the desired resolution. Pipelined converters achieve higher resolutions than flash converters containing a similar number of comparators.

SIGMA-DELTA ADC consists of an integrator, a comparator, and a single-bit DAC. The output of the DAC is subtracted from the input signal. The resulting signal is then integrated, and the integrator output voltage is converted to a single-bit digital output by the comparator. The resulting bit becomes the input to the DAC, and the DAC's output is subtracted from the ADC input signal, etc. This closed-loop process is carried out at a very high "oversampled" rate. The digital data coming from the ADC is a stream of ones and zeros, and the value of the signal is proportional to the density of digital ones coming from the comparator. Sigma-delta converters offer high resolution, high integration, and low cost.

SAR ADCs most commonly range in resolution from 8 to 16 bits and provide low power consumption. The SAR ADC implements a binary search algorithm. While the internal circuitry may be running at several megahertz (MHz), the ADC sample rate is a fraction of that number due to the successive approximation algorithm. It first sets the MSB, converts MSB to analog using DAC and then compares guess to input, depending upon the comparison result it changes the set bit or keeps it the same and then test the next bit.

Table 1.1 shows a comparison of various types of ADC and their properties.

Low power ADCs with moderate resolution and low sampling frequency is suited for biomedical application. These specifications make SAR ADC the suitable choice. It consumes low power due to its simple structure. Moreover, SAR ADC is scalable with the technology scaling since most parts of the architecture apart from the comparator are digital.

ADC TYPE	RESOLUTION	SAMPLING RATE	CHARACTERISTICS
FLASH	4 to 8	100MHz – 5GHz	High speed High bandwidth High power consumption Large area/die size Matching difficulties
PIPELINE	12 to 16	10MHz-100GMHz	High throughput Moderate bandwidth Low power consumption Moderate area/die size Self calibration techniques
SAR	10 to 16	50KHz to 500KHz	Very high resolution and accuracy Low bandwidth Low power consumption Low sampling rate
SIGMA-DELTA	14 to 20 bits	100 KHz-500MHz	High output resolution Moderate high speed High bandwidth Moderate power consumption
INTEGRATING	16 bits typical	40KHz-100KHz	High resolution Low bandwidth Low power consumption Low sampling rate Good noise immunity

Table 1.1 Comparison Of Different Types Of ADC

In SAR ADCs power dissipation scales with the sample rate. This contrasts with flash or pipelined ADCs which usually have constant power dissipation versus sample rate. This scaled power dissipation is especially useful in low-power applications or applications where the data acquisition is not continuous (for example, PDA digitizers).

In this thesis, first SAR ADC structure is studied in detail followed by study of different structures of comparators; then, various comparator types are designed and implemented in 0.18nm CMOS technology. The main target is to design an improvised comparator with less number of transistors and better performance.

2.1 SUCCESSIVE APPROXIMATION REGISTER ADC

The SAR ADC basically implements a binary search algorithm. The basic architecture of SAR ADC is shown in Figure 2.2. The SAR ADC typically consists of four chief sub-circuits:

1. Sample And Hold Circuit
2. Analog Voltage Comparator
3. Successive Approximation Register
4. Reference DAC

A sample and hold circuit acquires the input voltage V_{in} . A comparator compares V_{in} to the output of the internal DAC and outputs the result of the comparison to the SAR register. The successive approximation register sub-circuit is designed to supply an approximate digital code of V_{in} to the internal DAC. An internal reference DAC supplies the comparator with an analog voltage equal to the digital code output of the SAR. The analog input (V_{in}) is first held by the track/hold circuit. To implement the binary search algorithm, the N-bit register is first set to mid scale, i.e., the MSB is set to 1.

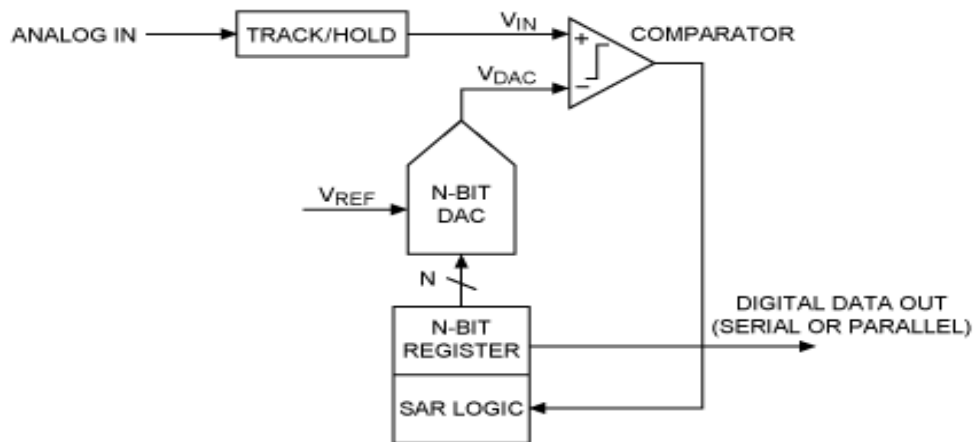


Fig 2.2 SAR ADC architecture

The output from SAR logic is given to DAC whose output is forced to $V_{ref}/2$, where V_{ref} is the reference voltage provided by ADC. A comparison is then performed to determine if V_{in} is less than or greater than V_{dac} . If it is greater the comparator output is logic 1, or else 0. Once the comparator output is high/low, the MSB is set to 1/0, and then the SAR logic moves to the next bit down, forces that bit high, and does another comparison and the process continues down to LSB.

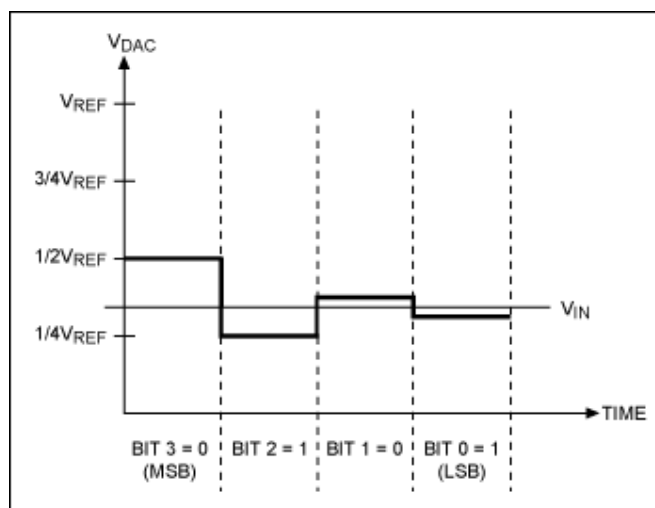


Figure 2.3. SAR operation (4-bit ADC).

Figure 2.3 shows an example of a 4-bit conversion. The y-axis (and the bold line in the figure) represents the DAC output voltage. In the example, the first comparison shows that $V_{IN} < V_{DAC}$. Thus, bit 3 is set to 0. The DAC is then set to 0100_2 and the second comparison is performed. As $V_{IN} > V_{DAC}$, bit 2 remains at 1. The DAC is then set to 0110_2 , and the third comparison is performed. Bit 1 is set to 0, and the DAC is then set to 0101_2 for the final comparison. Finally, bit 0 remains at 1 because $V_{IN} > V_{DAC}$.

An N-bit SAR ADC will require N comparison periods to be ready for the next conversion. Therefore ADCs are power- and space-efficient, yet are rarely seen in speed-and-resolution combinations beyond a few mega-samples per second (MSPS) at 14 to 16 bits.

A SAR ADC's speed is limited by:

1. The DAC
2. The comparator
3. The logic overhead

The settling time of the DAC, this must settle to within the resolution of the overall converter, for example, $\frac{1}{2}$ LSB. The comparator, which must resolve small differences in V_{IN} and V_{DAC} within the specified time and the amount of logic inbuilt decides the speed of the ADC.

2.2 SUB-BLOCKS OF SAR ADC

2.2.1 Sample and Hold

Sample and hold circuit contains a switch and a capacitor. In the tracking mode, when the sampling signal is high and the switch is connected, it tracks the analog input signal. Then, it holds the value when the sampling signal turns to low in the hold mode. In this case, sample and hold provides a constant voltage at the input of the ADC during conversion.

2.2.2 Successive Approximation Register

Successive Approximation Register (SAR) control logic determines each bit successively. The SA register contains N bit for an N-bit ADC. There are 3 possibilities for each bit, it can be set to '1', reset to '0' or keeps its value. In the first step, MSB is set to '1' and other bits are reset to '0', the digital word is converted to the analog value through DAC.

The analog signal at the output of the DAC is inserted to the input of the comparator and is compared to the sampled input. Based on the comparator result, the SAR controller defines the MSB value.

If the input is higher than the output of the DAC, the MSB remains at '1', otherwise it is reset to '0'. The rest of bits are determined in the same manner. In the last cycle, the converted digital word is stored. Therefore, an N-bit SAR ADC takes N+1 clock cycles to perform a conversion.

2.2.3 Comparator

Comparator is the only analog block of a SAR ADC and performs the actual conversion. It compares the analog sampled input to the analog output of the DAC and generates digital output of '0' or '1' which will be used in the SAR logic.

Accuracy and speed of the comparator are two important factors. The comparator need to resolve voltages with small differences. The offset voltage of the comparator employed in SAR ADC is translated to the transfer characteristic of the ADC thus will not affect the linearity of ADC.

The comparators needs to be as accurate as the overall system. In ADC most of the power is consumed by comparator. Moreover the conversion speed of ADC is limited by decision making speed of the comparator which makes it most crucial part of ADC.

In its simplest form, the comparator can be considered as one bit analog to digital converter. The basic symbol of comparator is shown in fig2.4.

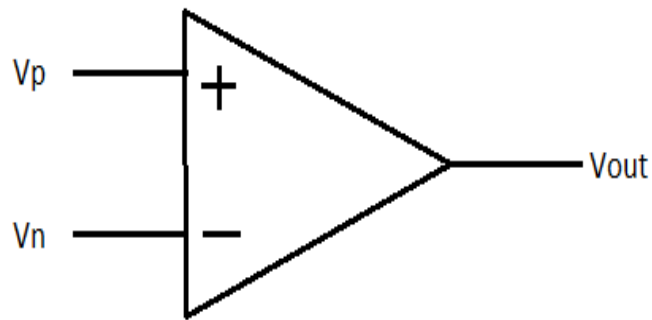


Fig 2.4. Basic Comparator symbol

If $V_p > V_n$ then $V_{out} = \text{logic 1}$

$V_p < V_n$ then $V_{out} = \text{logic 0}$

Apart from ADC, comparators are also can be found in many other applications like

1. Zero-Crossing Detectors
2. Peak Detectors
3. Switching Power Regulators
4. Data Transmission
5. Relaxation Oscillators
6. Level Shifter
7. Window Detector

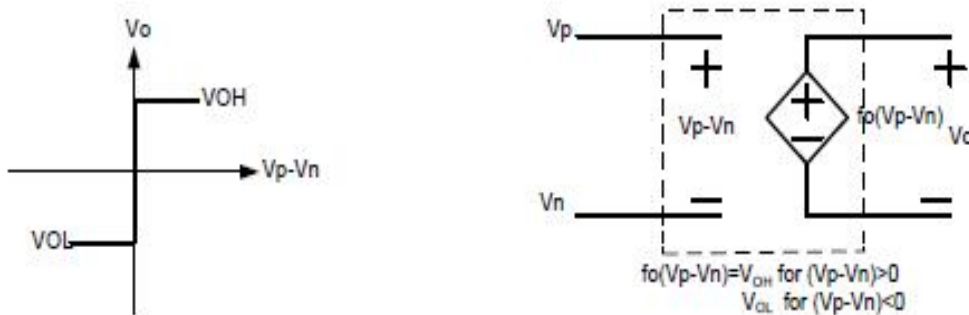
and many other applications especially the one using the digital processing.

3.1. CMOS COMPARATOR CHARACTERIZATION :-

3.1.1 Static Characteristics:-

A comparator is a circuit that has a binary output whose value is based on a comparison of two analog inputs. It is illustrated in Figure-3.1 As shown in this figure. The output of the comparator is high (VOH) when the difference between the non inverting and inverting inputs is positive, and low (VOL) when this difference is negative.

A positive voltage applied at the Vp input will cause the comparator output to go positive, whereas a positive voltage applied at the Vn input will cause the comparator output to go negative. The upper and lower voltage limits of the comparator output are defined as VOH and VOL respectively. It can be modelled with ideal circuit elements as shown in Figure-3.1, it comprises a voltage-controlled voltage source (VCVS) whose characteristics are described the mathematical formulation given on the figure.



In Figure-3.1 the output changes as the input difference crosses zero. If the output did not change until the input difference reached a value $+Vos$, then this difference would be defined as

the offset voltage. This would not be a problem if the offset could be predicted, but it varies randomly from circuit to circuit for a given design. Figure-3.2 illustrates offset in the transfer curve for a comparator, with the circuit model including an offset generator shown in Figure 3.4. The \pm sign of the offset voltage accounts for the fact that V_{os} is unknown in polarity.

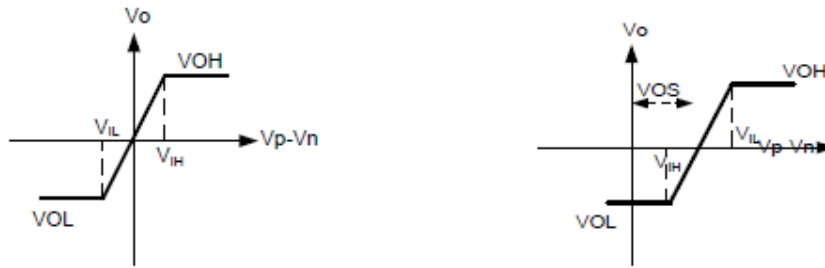


Figure-3.2 a) Transfer curve of comparator with finite gain b) with input offset voltage

In addition to the above characteristics, the comparator can have a differential input resistance and capacitance and an output resistance. In addition, there will also be an input common-mode resistance, R_{icm} . All these aspects can be modelled in the same manner as was done for the op-amp.

Because the input to the comparator is usually differential, the input common-mode range(ICMR) is also important. The ICMR for a comparator would be that range of input common-mode voltage over which the comparator functions normally. This input common-mode range is generally the range where all transistors of the comparator remain in saturation. Even though the comparator is not designed to operate in the transition region between the two binary output states, noise is still important to the comparator.

The noise of a comparator is modelled as if the comparator were biased in the transition region of the voltage-transfer characteristics. The noise will lead to an uncertainty in the transition region as shown in Fig.3.4. The uncertainty in the transition region will lead to jitter or phase noise in the circuits where the comparator is employed.

3.1.2 Dynamic Characteristics:-

The dynamic characteristics of comparator include both small signal and large signal behaviour. The characteristic delay between input excitation and output transition is the time response of the comparator is called the propagation delay of comparator.

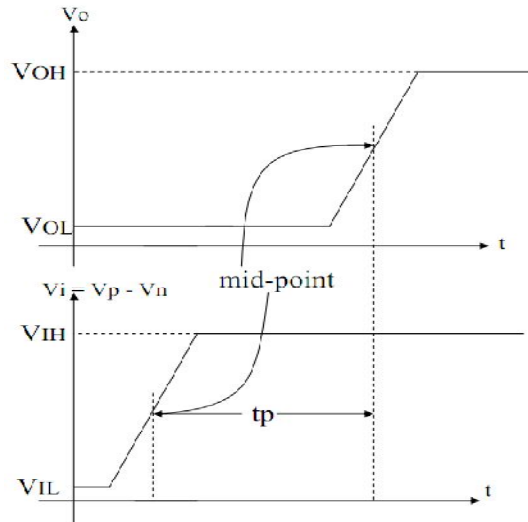


Figure 3.3: Propagation Delay Time of Comparator.

Propagation delay can be defined as at how much speed the amplifier responds with applied input. Simply speaking propagation delay is the delay between output and input. Figure 3.3 shows the propagation time delay characteristics of comparator.

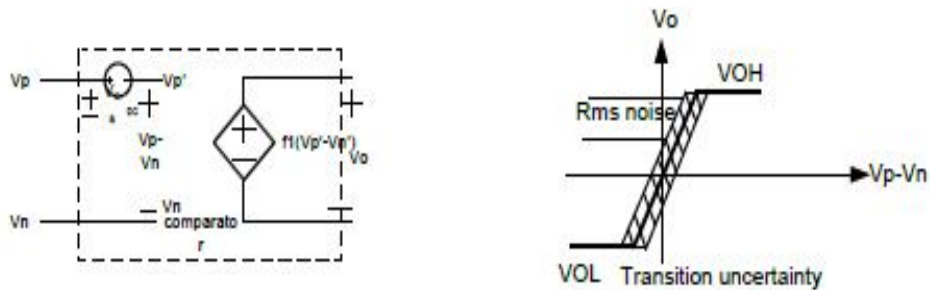


Figure 3.4 Model of comparator including input offset voltage b) influence of noise on a comparator

The propagation delay time in comparators generally varies as a function of the amplitude of the input. A larger input will result in a smaller delay time. There is an upper limit at which a further increase in the input voltage will no longer affect the delay. This mode of operation is called *slewing* or *slew rate*.

Offset Error Voltage And Currents:-

The ideal operational amplifier shown in Fig. 2.9(a) is perfectly balanced, that is, $V_o = 0$ when $V_1 = V_2$. A real operational amplifier exhibits an unbalance caused by a mismatch of the input transistors. This mismatch results in unequal bias currents flowing through the input terminals, and also requires that an input offset voltage be applied between the two input terminals to balance the amplifier output. In this section the DC error voltages and currents that can be measured at the input and output terminals.

Input Bias Current :-The input bias current is one-half the sum of the separate currents entering the two input terminals of a balanced amplifier as shown in Figure 3.5(a) the input bias current is $I_B = (I_{B1} + I_{B2}) / 2$ when $V_o = 0$.

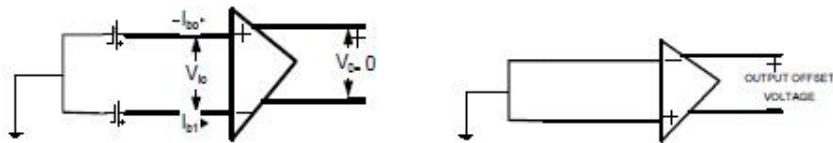


Figure 3.5(a) Input offset voltage 2.9 (b) Output offset voltage.

Input offset current- The input offset current is the difference between the separate currents entering the input terminals of a balanced amplifier. As shown in Figure 3.4(a), we have $I_{io} = I_{B1} - I_{B2}$ when $V_a = 0$.

Input Offset Current Drift :-The input offset current drift is the ratio of the change of input offset current to the change of temperature. T to I

Input Offset Voltage :-The input offset voltage V_{io} is that voltage which must be applied between the input terminals to balance the amplifier, as shown in Figure 3.4(a).

Input Offset Voltage Drift:- The input offset voltage drift is the ratio of the change of input offset voltage to the change in temperature. T/V_i

Output Offset Voltage The output offset voltage is the difference between the dc voltages present at the two output terminals (or at the output terminal and ground for an amplifier with one output) when the two input terminals are grounded (Figure 3.5(b))

Power Supply Rejection Ratio :-The power supply rejection ratio (PSRR) is the ratio of the change in input offset voltage to the corresponding change in one power supply voltage, with all remaining power supply voltages constant.

Slew Rate :-The slew rate is the time rate of change of the closed loop amplifier output voltage under large-signal conditions.

3.2 DESIGN CONSIDERATIONS FOR VOLTAGE COMPARATOR

The basic function of a comparator is to compare an analog signal with another analog signal or reference and output a binary signal based on comparison. Since it is easier to distribute voltages to a large number of comparators than to distribute currents, most converters employ voltage comparison [9]. A voltage comparator can be simply regarded as a 1-bit ADC. The circuit symbol and ideal and practical voltage transfer functions of a comparator are shown in Figure 3.6.

The ideal comparator outputs

V_{OH} (logic high “1” = V_{DD}) if $V_{in+} - V_{in-} > 0$ else

V_{OL} (logic low “0” = 0V (or $-V_{SS}$))

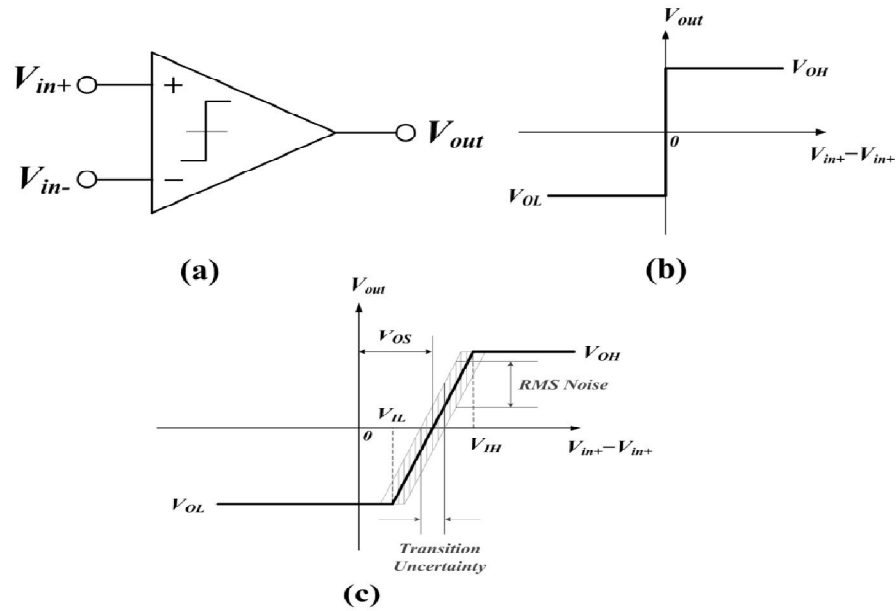


Figure 3.6 Comparator (a) Circuit symbol, (b) Ideal voltage transfer curve, and (c) Practical voltage transfer curve.

The ideal comparator has infinite gain, zero offset voltage and zero RMS noise. However, for a practical comparator shown in Figure 3.6 (c), its output changes because it has a finite gain, non-zero offset voltage and RMS noise (for latched comparators, V_{IL} and V_{IH} are limited by its sampling (or Clk) frequency due to meta-stability. It outputs

V_{OH} if $V_{in+} - V_{in-} > V_{IH} + V_{OS} (+ |V_{noise}|)$ and

V_{OL} if $V_{in+} - V_{in-} < V_{IL} (- |V_{noise}|)$

Therefore, design considerations for voltage comparators are can be summarized as high-speed (maximum clock rate f_s , which is related to small signal bandwidth, slew rate, and settling time), accuracy (high-resolution, which is related to gain, offset voltage [27], [29],[34] RMS and kickback noise [11], [32], [33], overdrive recovery, and linearity of input capacitance), wide input common-mode range, CMR (common-mode rejection), low-power consumption, small-area and so on [35].

Several types of comparator topologies are given in literature. They all can be broadly divided into two category

Open loop comparators

Regenerative comparators

Open loop comparators are basically op-amps without compensation whereas regenerative comparators use positive feedback mechanism to accomplish the comparison of two signals.

3.3 COMPARATOR ARCHITECTURES

3.3.1 Open-Loop Comparators[8],[30],[31]

Open-loop, continuous time comparators, shown in Figure 3.7[8], are an operational amplifier without frequency compensation to obtain the largest possible bandwidth, hence improving its time response. Since the precise gain and linearity are of no interest in comparator design, no-compensation does not pose a problem.

However, due to its limited gain-bandwidth product, open-loop comparators are too slow for many applications. On the other hand, a cascade of open-loop amplifiers usually has a significantly larger gain-bandwidth product than a single-stage amplifier with the same gain. However, since it costs more area and power consumption, cascading does not give practical advantages for many applications.

Many applications use simple open loop op-amp as voltage comparator, but this approach is usually not accurate and fast enough. For a superior sensitivity like the one needed in biomedical application we need high precision, low offset, low input referred noise, high slew rate high speed and low propagation delay. The energy constraints dominate architectural and implementation decisions throughout the design of biomedical systems.

High performance multistage comparators, like the latched comparators, are more suited for biomedical applications which require a good speed and precision.

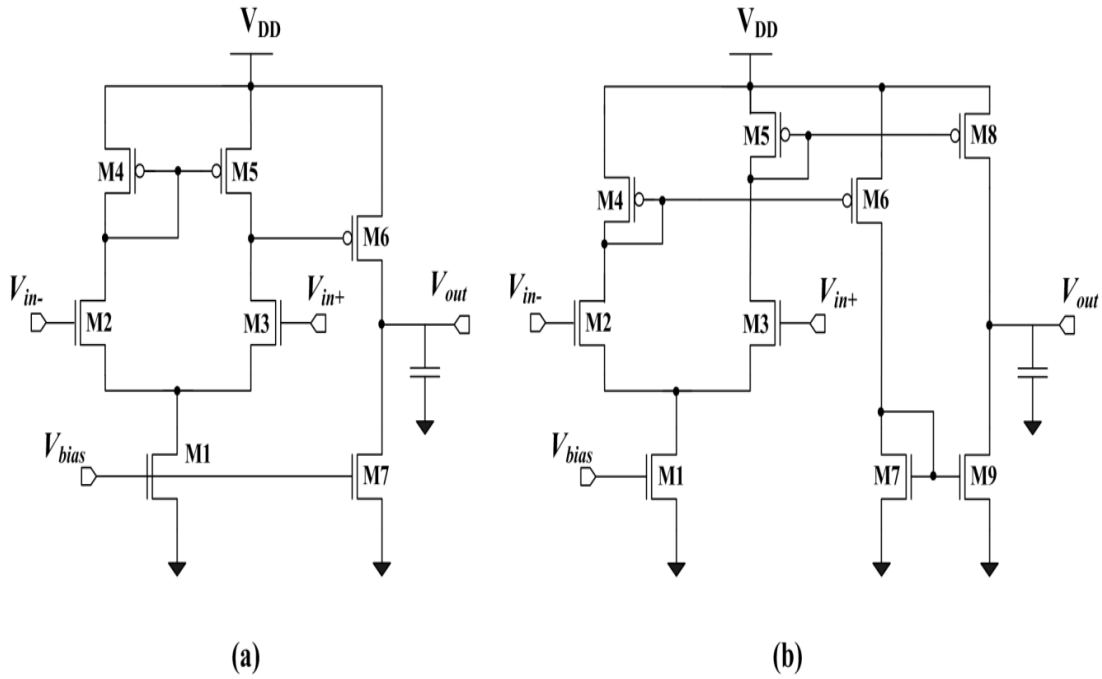


Figure 3.7(a) Two-stage open-loop comparator (b) Push-pull output open-loop comparator

Latched comparators of the following type have been described in literature [11]:

1. Static latched comparator
2. Class AB latched comparator
3. Dynamic latched comparator

In static latched comparator [12], the regeneration is done by two Class-A cross-coupled inverters. This current limited operation leads to a slow regeneration process. The power efficiency is poor, since the consumption is purely static. There is always a differential pair acting as pre-amplifier, whose output current is either mirrored or injected through a cascode transistor in the regeneration nodes.

This isolation between the drains of the differential pair transistors and the regeneration nodes reduces the kickback noise. These latched comparators present low kickback noise, but the static power consumption and slow regeneration process does not make them attractive.

In class AB latched comparators [22] the regeneration is done by two cross-coupled CMOS inverters. Their current increases momentarily, during the regeneration process, to charge the output nodes faster—Class-AB operation. The drains of the input differential pair are directly connected to the regeneration nodes. The circuit reacts quicker to input variations. However, there is an increase in the kickback noise because there are now rail-to-rail signals at nodes capacitively coupled to the inputs.

In dynamic latched comparator [10], the current only flows during the regeneration phase, no current flows during the reset phase. Thus once the regeneration completes the current flow stops making it most power efficient latched comparator. Due to fast-speed, low-power consumption, high-input impedance and full-swing output, CMOS dynamic latched comparators are very attractive for biomedical applications .

Conventionally, as shown in Figure.3.8, a pre-amplifier has been used preceding the regenerative latch stage to reduce the latch offset voltage. It can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage and also it reduces the kickback noise.

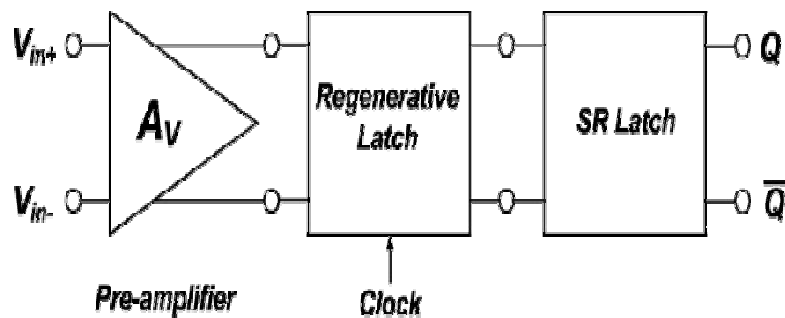


Fig 3.8. Basic Architecture of latched comparator

Latched comparators commonly employ one or two clock signals (Clk and $Clkb$) to determine the modes of operation: *Track Mode (Reset)* : output is reset and input is tracked, *Latch Mode (Evaluation)*:output is toggled by using a positive feedback.

The operation of the circuit shown in Figure 3.9(a) [12-17] is as given, during reset phase ($Clkb=0V$), both complementary output V_{out+} and V_{out-} are reset to 0V by reset (switch) transistor M10 and M11. During evaluation phase ($Clkb=VDD$), as the reset transistors are off, the comparison will be performed by appositve feedback from transistor M7 and M9.

While this comparator present low kickback noise, relatively large static power consumption and slow regeneration due to its limited current operation make it less attractive[11]. Similarly, the operation for the circuit shown in Figure3.9(b) [18-22] ,during reset phase ($Clk=0V$) , PMOS reset transistor M7 will be shorted and make both outputs equal : $V_{out+}=V_{out-}$ while NMOS transistor M8 is off.

During evaluation phase ($Clk=VDD$),as the reset transistor M7 is off and the tail transistor of the latch M8 is on, the comparison will be made by a positive feed-back formed from back-to-back cross coupled inverter pairs (M4/M6 and M5/M7). While this comparator shows faster speed and consumes less power, it generates more kick back noise and during reset phase both outputs (V_{out+}, V_{out-}) are not reset exactly to either VDD or $0V$ [11].

Thus the pre-amplifier based latched comparators, which is a combination of a pre-amplifier and a latch, offer fast speed and low offset while they still consume static power which makes them unsuitable for the biomedical application as the power consumption is one of main design consideration.

3.3.3 Fully Dynamic Latched Comparators

3.3.3.1 Resistor Divider Comparator

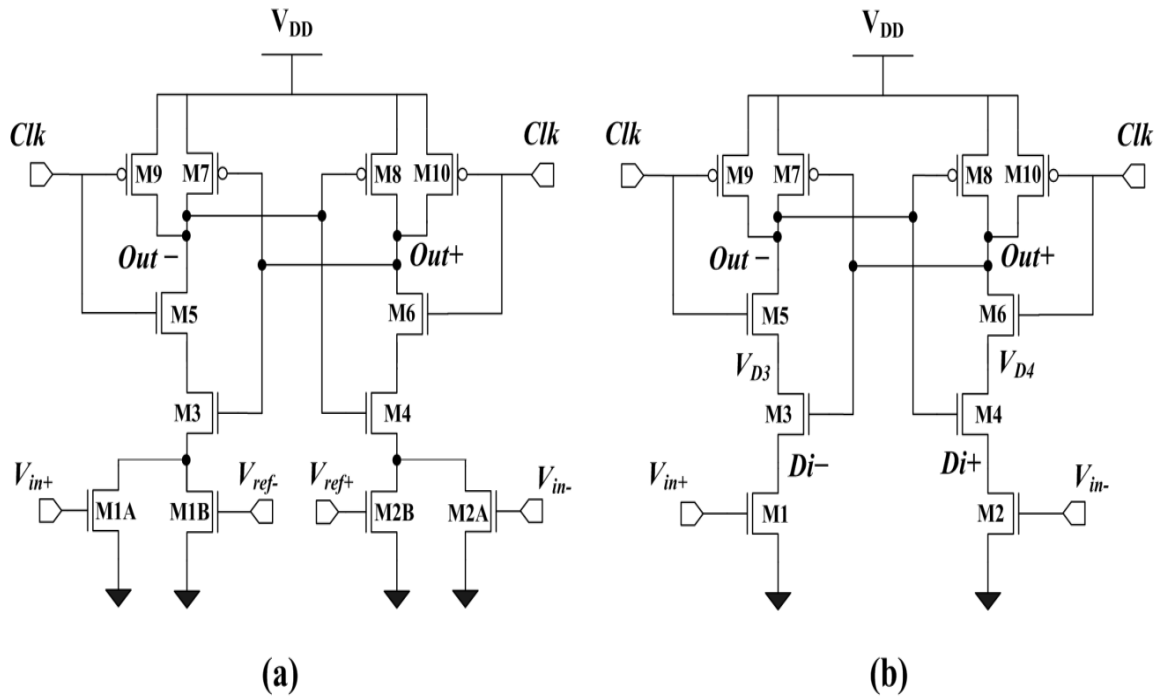


Figure 3.10 (a) Resistor Divider Comparator (b) Simplified form of resistor divider comparator

The comparator shown in Figure 3.10(a) was introduced in [23]. The input transistors $M1A/B$ and $M2A/B$ operate in the triode region and act like voltage controlled resistors, this comparator is called “Resistive Divider Comparator.” The advantage of this comparator is its low power consumption (No DC power consumption) and adjustable threshold voltage.

The threshold voltage (decision level) which is defined as

$$V_{in}(\text{threshold}) = (W_B/W_A)V_{ref} \quad (1)$$

$$\text{where } W_A = W_{1A} = W_{2A} \quad W_B = W_{1B} = W_{2B}$$

$$V_{in} = V_{in+} - V_{in-} \quad V_{ref} = V_{ref+} - V_{ref-}$$

For the comparator shown in Figure 3.10(b), during reset phase ($Clk=0V$), PMOS reset transistor M9 and M10 charge *Out* nodes upto V_{DD} (this makes NMOS transistor M3 and M4 on and the node voltage at $VD_{3,4}$ discharge to ground) and input transistor M1 and M2 discharge *Di* nodes to ground while NMOS transistor M5 and M6 are off.

During Evaluation phase ($Clk=V_{DD}$), as both switch transistor M5 and M6 are on, each node voltage at $Di+$ and $Di-$ instantly rises upto the certain values, and then, each *Out* node voltage starts to discharge from V_{DD} to ground inversely proportional to the applied input voltage such away;

$$V_{in+} \uparrow \rightarrow V_{Di} \downarrow \rightarrow V_{GS3} \uparrow \rightarrow I_{D3} \uparrow \rightarrow V_{out-} \downarrow \rightarrow V_{GS4} \downarrow \rightarrow V_{out+} \uparrow (\rightarrow V_{GS3} \uparrow \dots).$$

With positive feed back operation from the back-to-back cross-coupled inverter pairs (M7/M3 and M8/M4), one *Out* node will discharge to ground and the other *Out* node will charge upto V_{DD} again and this comparator will finish its comparison. Since the input transistor M1 and M2 are operated in the linear region during evaluation phase, the transconductance for those transistors are can be approximately written as

$$g_{m1,2} = \mu_n C_{ox} \left(\frac{W_{1,2}}{L} \right) V_{ds1,2}$$

Also, because transistor M3 and M4 are operated in the saturation region during evaluation phase, the transconductance for those transistors can be written as

$$g_{m3,4} = \mu_n C_{ox} \left(\frac{W_{3,4}}{L} \right) (V_{gs3,4} - V_{tn})$$

The transconductance of transistor M3 and M4 is much larger than that of the input transistor pair; hence the differential voltage gain built between *Di* nodes from the input transistor pair is not big enough to overcome an offset voltage caused from such a small mismatch between transistor M3 and M4 pair.

As a result, those transistors are the most critical mismatch pair in this comparator and needed to be sized big enough to minimize the offset voltage at the cost of the increased power consumption. Besides, the mismatch between transistor M5 and M6 pair (which is switches and operated in the linear region) also causes the considerable input-referred offset voltage.

Furthermore, as the common mode voltage V_{com} of the input transistor pair increases, the relative difference between the voltage controlled resistors ($r_{ds1,2}$) becomes smaller at the same amount of the input voltage difference ΔV_{in} and this in turn increases the offset voltage.

So despite its advantages such as zero-static power consumption and adjustable threshold voltage, because Resistor Divider Comparator shows a high offset voltage and high offset voltage

dependency on a different common mode voltage V_{com} , it is only suitable for low resolution comparison.

3.3.3.2 Differential Pair Comparator/Latch-type Voltage Sense Amplifier

The comparator shown in Figure 3.11 (a) was first proposed in [24-25]. Similar to Resistive Divider Comparator, this comparator also has an adjustable threshold voltage. In Figure 3.11(b) extra switching transistor M10 and M11 are added to improve its characteristics ; since those additional PMOS switch transistors increase the time the input transistor pair M2 and M3 being operated in the saturation region during evaluation phase ($Clk=VDD$), hence the amplification from the differential input pair increases.

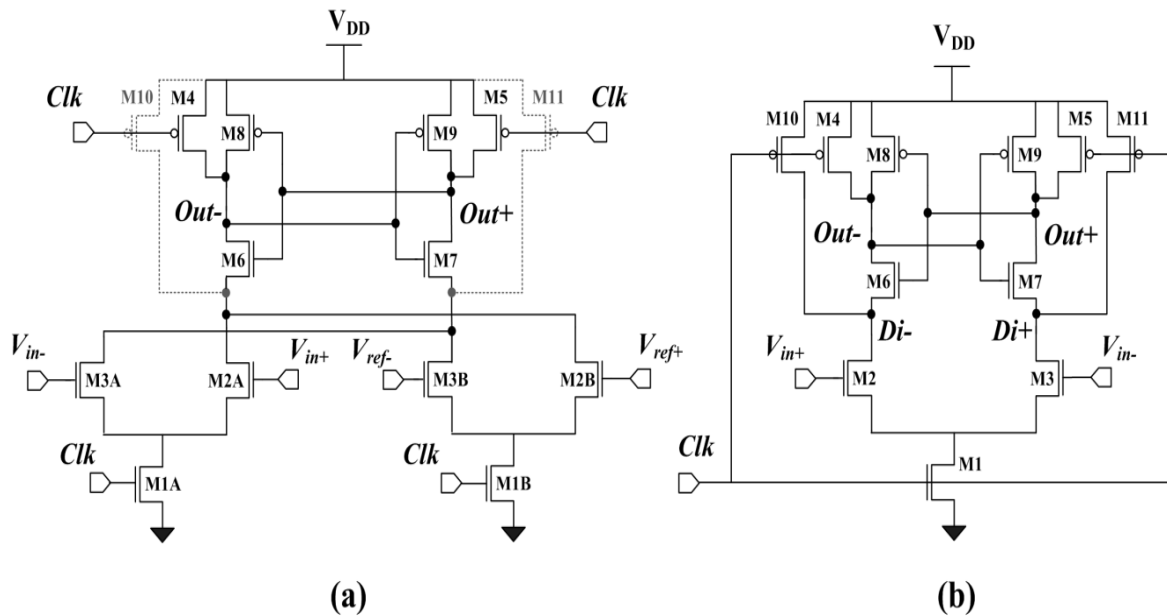


Figure 3.11(a) Differential pair comparator (b) Latch-type voltage sense amplifier

During reset phase ($Clk=0V$), Out nodes of the cross-coupled inverters (M6-M9) are reset to VDD through the reset transistors M4 and M5. During evaluation phase ($Clk=VDD$), the tail transistor

M1 is turned on at the rising Clk edge. The input transistor pair (M2 and M3) starts to discharge each Di node voltage with a different time rate proportional to the each applied input voltage from VDD to $0V$.

Once either of Di node voltages drops around $VDD - V_{tn}$, then the NMOS transistors of the cross-coupled inverters M6 and M7 turn on and this initiates the positive feedback. Once either of Out node voltage reaches around $VDD - |V_{tp}|$, the PMOS transistors of the inverters M2 and M4 also turn on ; further enhancing the positive feedback and enabling the regeneration of a small differential voltage ΔV_{in} to a full swing differential output.

Comparing with Resistor Divider Comparator, this comparator shows faster operation and less overall offset voltage. However, still its structure which consists of a stack of 4 transistors requires large voltage headroom; it is problematic in low-voltage deep-submicron CMOS technologies. Furthermore, in order to increase the drive currents of the latch , it is inevitable to size up the transistor M1 since this comparator has only one tail transistor M1. If the size of transistor M1 is increased, the drain currents of both input transistors M2 and M3 will increase during evaluation phase ($Clk = VDD$)

This , in turn ,means the reduction of the time duration for transistor M2 and M3 being operated in saturation region because Di nodes discharge from VDD to ground in a very short period. Consequently, lower amplification of the input voltage difference will be made and such a small V_{th} variation from mismatch between transistor M6 and M7 can yield high input-referred offset. In addition , since it shows the strong dependency on speed and offset voltage with a different common-mode input voltage V_{com} [2],it is less attractive in applications with wide common-mode ranges such as ADCs [3].

3.3.3.3 Double-Tail Dynamic Latched Comparators

To mitigate the drawbacks (strong dependency on speed and offset with a different common-mode input voltage V_{com} and problem in low power supply voltage operation due to its structure

:a stack of four transistors) from the comparator shown in Figure 3.11(b), a comparator with separated input-gain stage and output-latch stage, shown in Figure 3.12(a), was first introduced in [3].

This separation made this comparator have a lower and more stable offset voltage over wide common-mode voltage (V_{com}) ranges and operate at a lower supply voltage (V_{DD}) as well. It is because by controlling the sizes of the tail transistors (M1 and M12) of the input and output stage such a way that a small tail current for the differential input pair to obtain a long integration time and a better g_m/I_D ratio for a bigger gain (hence, less offset voltage) and a large tail current for the output latch-stage for fast regeneration, one can get fast speed and low offset voltage with less dependence on V_{com} .

During reset phase ($Clk=0V, Clkb=V_{DD}$), PMOS transistor pair M4 and M5 pre-charge Di node capacitances up to V_{DD} (sequentially, the input transistor pair for the output stage M10 and M11 are turned on and Out nodes are reset to 0V) while the both tail transistors (M1 and M12) in the input stage and output latch-stage are off.

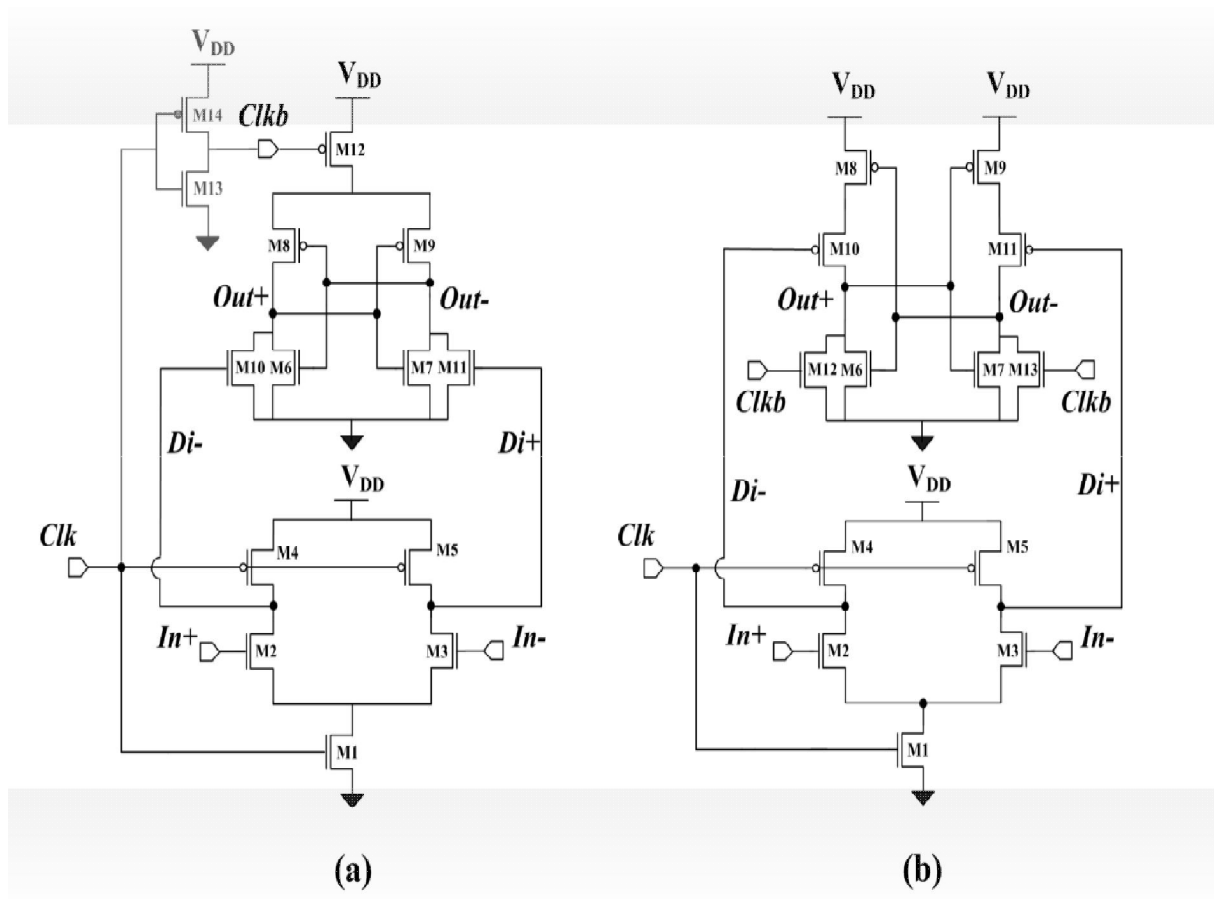


Figure 3.12(a) Double-tail latch-type voltage SA [3] (b) Energy efficient two-stage comparator

[26]

During evaluation phase ($Clk = V_{DD}$, $Clkb = 0V$), once the input-stage tail transistor M1 is turned on, each Di node voltage starts to discharge from V_{DD} to ground with a different time rate proportional to each input voltage. Then, the voltage difference built between Di nodes is passed to Out nodes in the output latch-stage through the input transistor pair (M10 and M11) of the output latch-stage. The cross-coupled inverters start to regenerate the voltage difference formed between Out nodes as soon as the common-mode voltage at the Di nodes is not big enough to clamp Out nodes to ground and the PMOS output tail transistor M12 is on.

Since this comparator requires both Clk and $Clk\ b$ signals for its operation, high accuracy timing between Clk and $Clk\ b$ is required because these condstage has to detect the voltage difference between the differential outputs of the first gain stage at very limited time.

If a simple inverter replaces $Clk\ b$, Clk has to be able to drive an additional large inverter(heavier clock load)in order to drive the largest transistor M12 in a small delay. If $Clk\ b$ is lagging Clk , it results in increased delay and if $Clk\ b$ is leading Clk ,it results in increased power dissipation due to existing the short circuit current path M12 to M10/M11 though M8/M9 and it can even increase the latch off set voltage if the device mismatch between M8 and M9 is significant.

The comparator shown in Figure3.12(b) is a different version of two-stage dynamic latched comparator. The operation is similar to the comparator shown in Figure3.10(a).By modifying the output latch-stage, during reset phase ($Clk=0V,Clkb=VDD$),its Di node capacitances, mostly drain diffusion capacitance so PMOS transistor (M10 and M11)and NMOS transistors (M2 and M3),are reduced, which is much less than the Di node capacitances, mostly gate capacitances of NMOS transistor M10 and M11, in the comparator in[3]; therefore, it can be operated at less power consumption and faster speed.

However, since its till has Clk and $Clk\ b$ for its operation, high accuracy timing between Clk and $Clk\ b$ is required and due to reduced Di node capacitances the relative capacitance mismatch $\Delta CDi/CDi$ and the input referred RMS noise are also increased.

The comparator from [4] without off set calibration technique, shown in Figure3.13, resolved the problem by replacing $Clk\ b$ with Di nodes. As a result, Clk load was lessened and the input-referred off set was reduced because the output latch-stage obtains the gain from the both second-in put transistor pairs (M10/M11andM12/M13).

However, the improved off set has to trade off with the increased delay since the current drivability of the output load was weakened due to the fact that transistor M12 and M13 use Di node voltages as their $Clkb$ signal, which show slow exponential decay shape, and that the maximum drive current of each $Ou\ t$ node was reduced to half of the single output tail current of M12 since it was separated into two transistors M12 and M13.

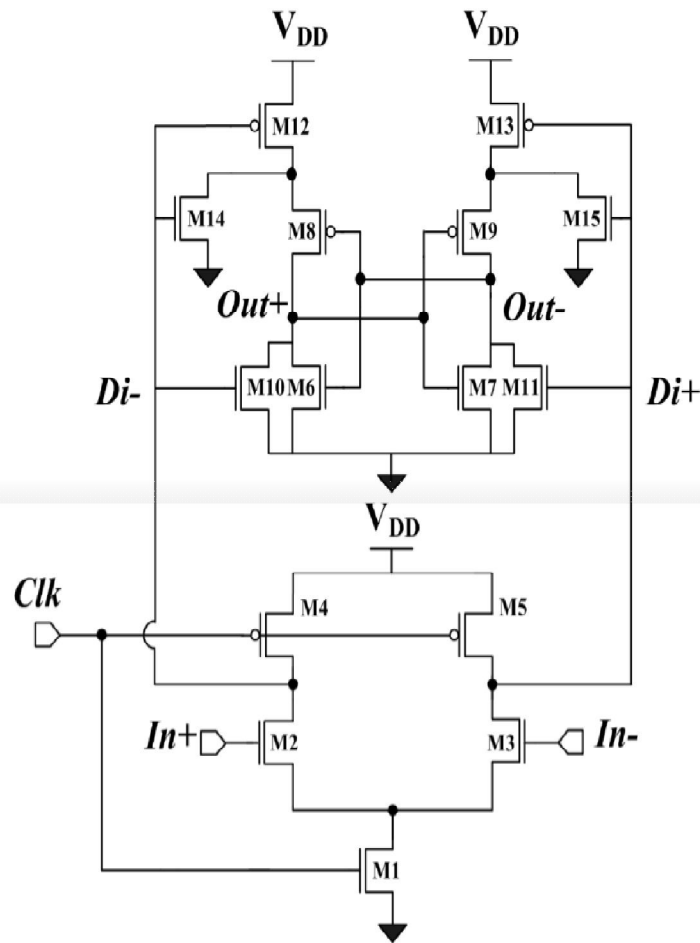


Figure 3.13 Two-stage Dynamic comparator [4]

The voltage difference formed between D_i nodes during the evaluation phase ($Clk = V_{DD}$) is time varying, therefore the speed and offset voltage are affected by the clock skew between Clk and $Clkb$ signals.

If a simple inverter is used to generate $Clkb$, Clk should be able to drive an additional inverter (at the cost of increased clock loading) that drives the largest transistor M_{12} for a small delay.

To overcome the clock skew problem a new comparator was proposed [7]. Fig3.14. The Clk skew problem is resolved by replacing $Clkb$ with D_i nodes. As a result, the performance is not affected by clock skew and the clock load is reduced. In addition, the input-referred offset

voltage and noise are reduced since this comparator has larger D_i nodes capacitance and has double trans-conductance (g_m) at D_i nodes.

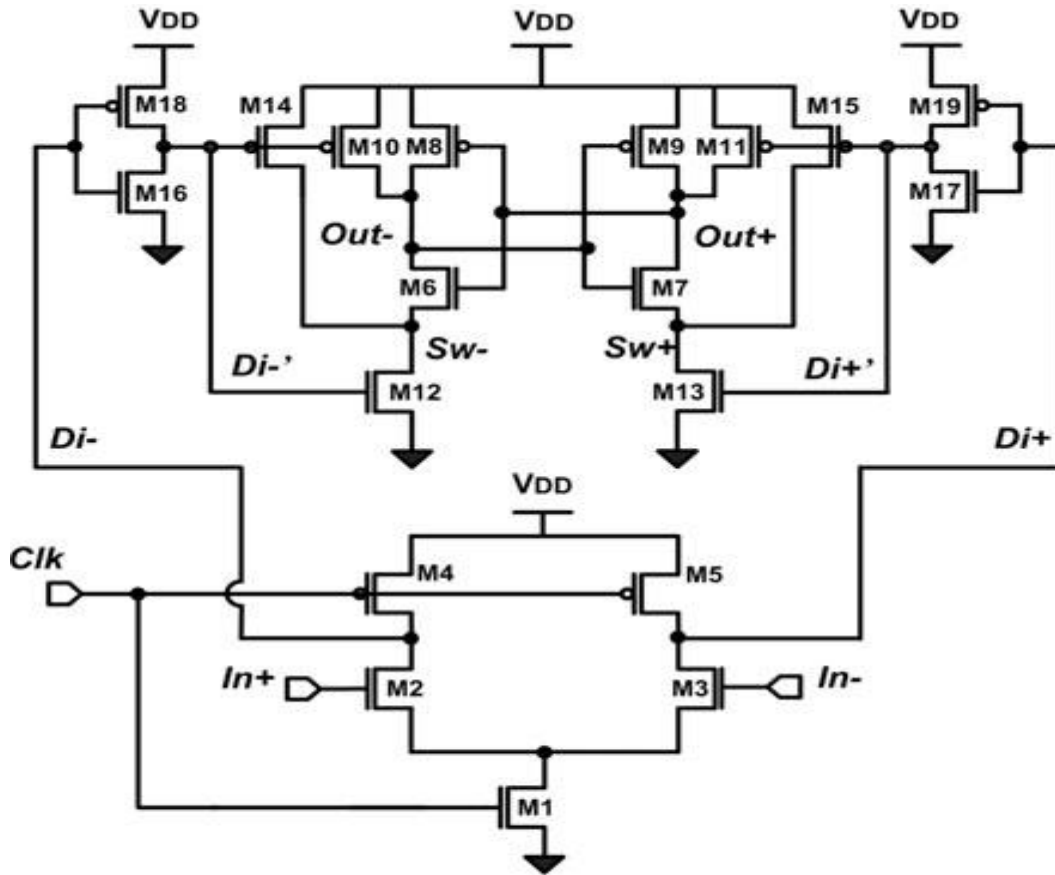


Figure 3.14 Schematic of comparator proposed in [7]

This comparator provides better input offset characteristic and faster operation in addition to the advantage so f those comparators such as less kick back noise, reduced clock load and removal of the timing requirement between Clk and $Clkb$ over a wide common-mode and supply voltage range.

During the pre-charge (or reset) phase ($Clk=0V$) ,both PMOS transistor M4 and M5 are turned on and they charge D_i nodes' capacitance to VDD , which turn both NMOS transistor M16 and M17

of the inverter pair on and Di' nodes discharge to ground. Sequentially ,PMOS transistor M10 ,M11 ,M14 and M15 are turned on and they make Out nodes and Sw nodes to be charged to VDD while both NMOS transistors M12 and M13 are being off.

During the evaluation (decision-making) phase ($Clk=VDD$), each Di node capacitance is discharged from VDD to ground in a different time rate in proportion to the magnitude of each input voltage.

As a result ,an input dependent differential voltage is formed between $Di+$ and $Di-$ node . Once either $Di+$ or $Di-$ node voltage drops down below around $VDD-/V_{tp}$ |, the additional inverter pairs M18/M16 and M19/M17 invert each Di node signal into the regenerated (amplified) Di' node signal.

Then the regenerated and different phased Di' node voltages are amplified again and relayed to the output-latch stage by transistor M10–M13 .As there generated each Di' node voltage is rising from 0V to VDD with a different time interval (or a phase difference ,which increases with the increasing input voltage difference ΔV_{in}) , M12 and M13 turn on one after another and the output-latch stage start store generate the small voltage difference transmitted from Di' nodes into a full-scale digital level:

$$Out+=\text{logichigh}(VDD)\text{if}(Di+'(t)<Di-'(t))$$
$$Out+=\text{low}(0V)\text{otherwise.}$$

Once either of the Out node voltages drops below around $VDD-/V_{tp}$ |,this positive feedback becomes stronger because either PMOS transistor M8 orM9.

However, this comparator has only one tail current transistor M1 which controls the currents flowing through both the differential input pair (M2 and M3) and the latch (M6–M9). Therefore, in order to increase the drive currents of the latch, it is inevitable to size up the transistor M1.

If the size of transistor M1 is increased, the drain currents of the both input transistors M2 and M3 will increase during the evaluation phase ($\text{Clk} = V_{\text{DD}}$). This, in turn, reduces the time duration for which the input transistors operate in the saturation region, because Di nodes discharge from V_{DD} to ground in a very short period.

Consequently, lower amplification of the input voltage difference will be made between Di nodes and a small V_{th} mismatch between transistor M6 and M7 can yield a large input-referred offset voltage. In addition, since it shows large variations of speed and offset voltage with a different input common-mode voltage it is less attractive in applications that need wide input common-mode ranges such as ADCs.

To circumvent these drawbacks, the comparator with separated differential input-gain stage and output-latch stage shown in Fig. 3.15, was introduced in [3]. This stage separation makes this comparator be able to operate at a lower supply voltage (V_{DD}) and have a more stable offset voltage and speed over wide input common-mode voltage (V_{com}) ranges.

However, this comparator requires both Clk and Clkb signals and the highly accurate timing relationship between those clocks is required for its optimal operation. If Clkb is lagging the Clk, it results in increased delay. If Clkb is leading the Clk, it results in increased power dissipation due to the short circuit current path M12 to M10/M11 through M8/M9.

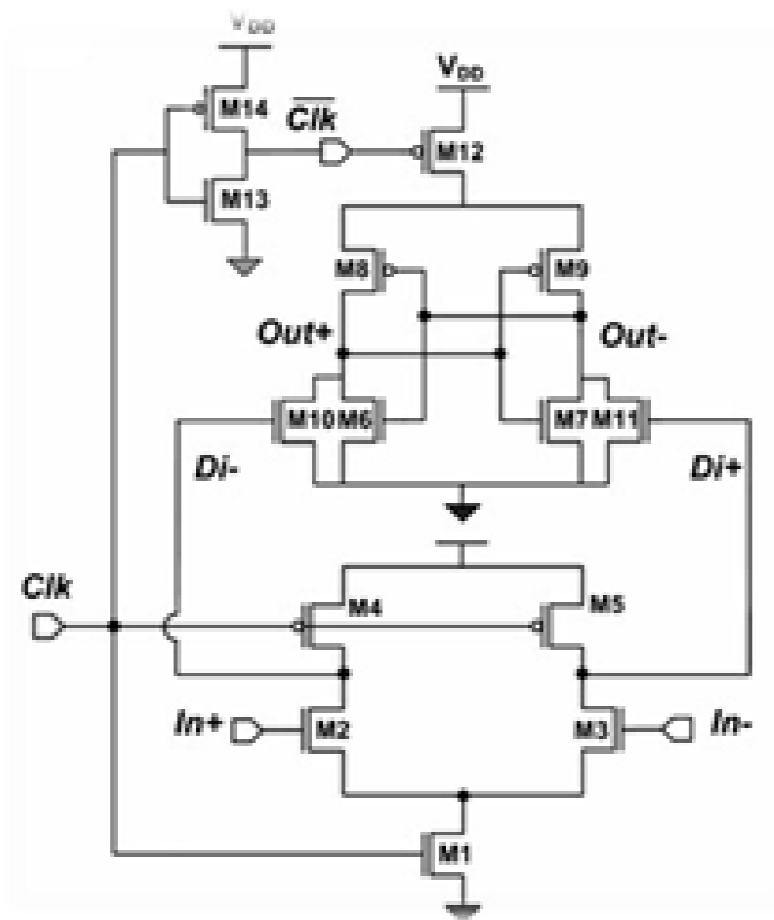


Fig 3.15. Dynamic latched comparator with separate input stage and latch stage

To overcome the clock skew problem a new comparator was proposed. Fig3.16. The Clk skew problem is resolved by replacing Clkb with Di nodes. As a result, the performance is not affected by clock skew and the clock load is reduced. In addition, the input-referred offset voltage and noise are reduced since this comparator has larger Di nodes capacitance and has double trans - conductance (g_m) at Di nodes.

However, these improvements are compromised with the increased delay since the current drivability of the output load is weakened due to the fact that transistor M12 and M13 use Di node voltages instead of Clkb signals, which are slow exponential decaying shape. However, these improvements are compromised with the increased delay since the current drivability of the output load is weakened due to the fact that transistor M12 and M13 use Di node voltages

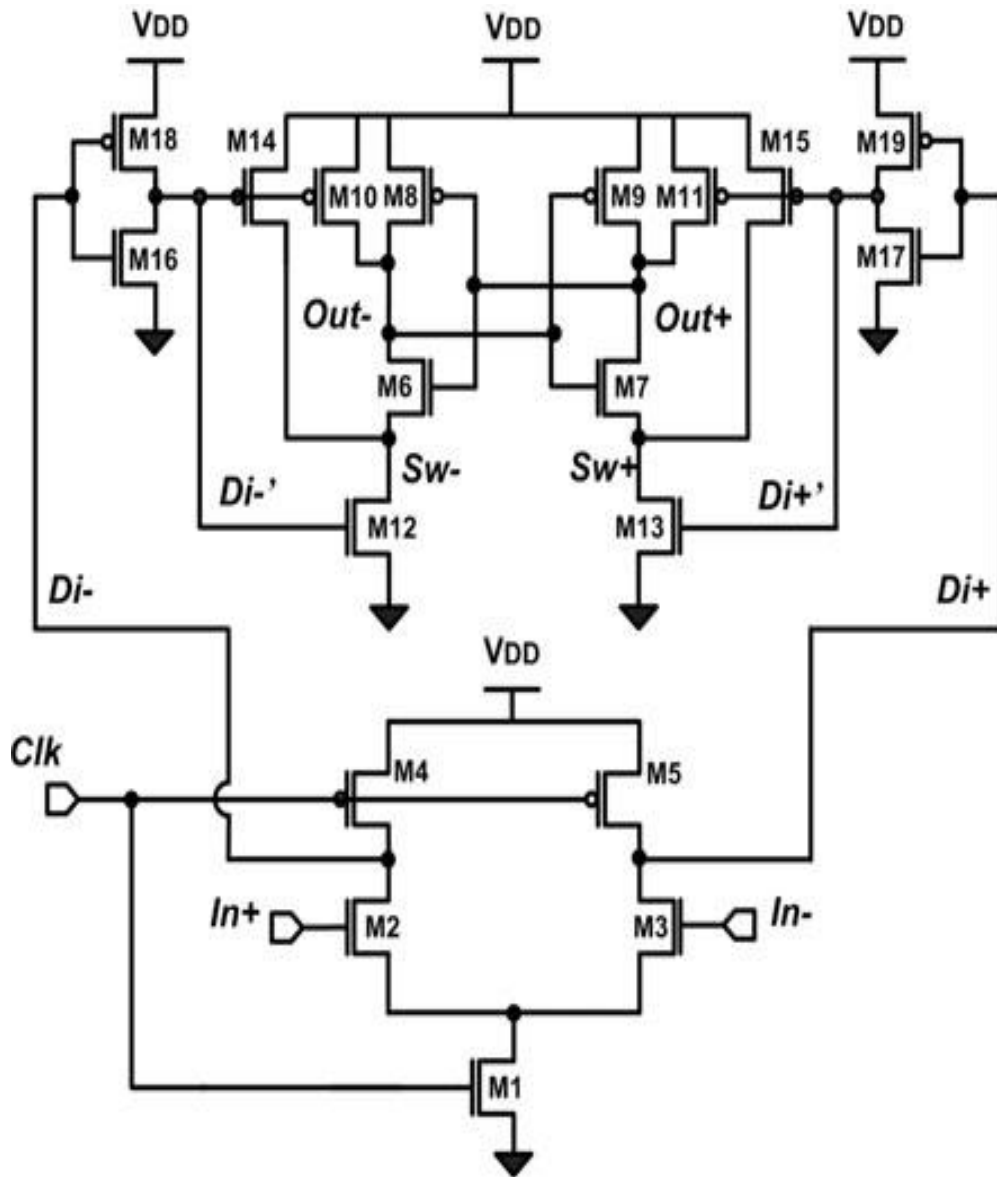


Fig 3.17. Comparator proposed in [1].

During pre-charge (or reset) phase ($Clk = 0\text{ V}$), both PMOS transistors M4 and M5 turn on and Di nodes' capacitances are charged to VDD, which, in turn, make both NMOS transistor M16 and M17 of the inverter pair on and Di0 nodes discharge to ground.

Sequentially, PMOS transistor M10, M11, M14 and M15 turn on and Out nodes and Sw nodes are charged up to VDD while both NMOS transistors M12 and M13 are off. During evaluation (decision-making) phase ($Clk = VDD$), each Di node capacitance is discharged from VDD to ground in a different rate proportional to the magnitude of each input voltage.

As a result, an input dependent differential voltage is formed between Di+ and Di-nodes. Once either Di+ or Di- voltage drops below $VDD - |V_{tp}|$, the inverter pairs (M18/M16 and M19/M17) invert each Di node signal into the regenerated (amplified) Di' node signals. Then the regenerated and different phased Di0 node voltages are relayed to the output-latch stage by M10–M13.

As the regenerated Di0 node voltage is rising from 0V to VDD with a different time interval (or a phase difference which increases with the increasing input voltage difference DV_{in}), M12 and M13 turn on one after another. And the output latch starts regenerating the small voltage difference transmitted from Di0 nodes into a full-scale digital level: Out+ node outputs logic high (VDD) if Di+0 node voltage rises faster than Di-0 node voltage and Out+ Outputs logic low (0 V) otherwise.

Once either of Out node voltages drops below $VDD - |V_{tp}|$, this positive feedback becomes stronger because either PMOS transistor M8 or M9 will turn on. The two additional inverters inserted between Di and Di0 nodes enable the proposed comparator to have less input referred offset voltage in the output latch by amplifying (regenerating) the weakened Di node signals to Di0 node signals.

The output latch stage of the comparator is the complementary version of the latch stage in the conventional design, which made the comparator deliver bigger load currents.

This comparator was used as a base and improvised more for biomedical application. The number of transistors were reduced to optimise the size and better swing at output with less overshoot.

Chapter 4

ANALYSIS AND METHODOLOGY

Each stage of the above comparator was studied in detail. Various types of latches were also studied [8]. In biomedical application small area and small power consumption are of prime importance, thus instead of using CMOS logic style latch a CVSL(cascade voltage switch logic) was thought to be better.

Following observations were made:

1.) Instead of using a cross coupled inverter pair, a pair of cross coupled NMOS or PMOS transistors can also provide a good amount of positive feedback to get rail to rail output.

NMOS cross coupled transistor pair was preferred over the pmos cross coupled transistor pair because the nmos cross coupled pair is faster than the pmos pair because of higher on resistance. The input dependent differential voltage produced between the nodes D_{i+} and D_{i-} is first passed through a inverter pair to amplify the weak signals and also to separate input and output nodes which help to reduce input referred offset voltage as given in the reference comparator architecture [1].

This approach reduced the number of transistors in the latch, which means more optimized design.

2.) Pre-charging consumes a major portion of power in the comparator.

So instead of using pre-charge PMOS transistors as in reference[1], pre-discharge NMOS transistors were used. The pre-discharge NMOS transistors were connected to the output node.

3.) A glitch in the D_{i+} and D_{i-} which is produced due to clock feed-through can also be reduced by using a transistor in between the clocking transistor and the input transistors.

Diode connected transistors were inserted between the clocking transistor and the input transistors. The diode connected load minimizes the output swing from V_{dd} to 0 to $(V_{dd}-V_{ds})$ to 0, thus reducing the dynamic power dissipation .

4.) As the number of transistors which are connected directly to clock increase, the power consumption increases.

So a method was thought where latch is made to work without directly applying clock signal to it.

The basic structure of the proposed comparator stems from the comparators from [1], [3] and [4] by in-corporating the above observations. The comparator has been designed using 0.18 μ m technology. Cadence Virtuoso® Analog Design Environment, Virtuoso® XL Layout Editing Software has been used for analyzing the circuits.

4.1 PROPOSED COMPARATOR

Figure 4.1 shows the proposed comparator. It consists of a input stage which has a diode connected load. When the clock is low the M1 pre-charges the nodes D_{+} and D_{-} to $V_{dd}-V_{gs}$. This voltage drives the two inverters connected to it discharging the OUT_{+} and OUT_{-} to ground potential.

When the clock goes high M6 becomes on and the transistors M4 and M5 starts discharging the nodes D_{+} and D_{-} proportional to the applied input voltage IN_{+} and IN_{-} . when this voltage falls

below V_{th} of M7 and M9 , these transistors start switching on at a rate proportional to the rate at which the input voltage discharges the nodes D_{i+} and D_{i-} .

With the increasing input voltage difference M7 and M9 turn on one after the other and the cross-coupled nmos pair made by M11 and M12 starts regenerating the small voltage difference transmitted from D_i nodes into a full scale digital level. Instead of applying clock directly to the latch, the latches regeneration phase and reset phase were set by the node voltages D_{i+} and D_{i-} .

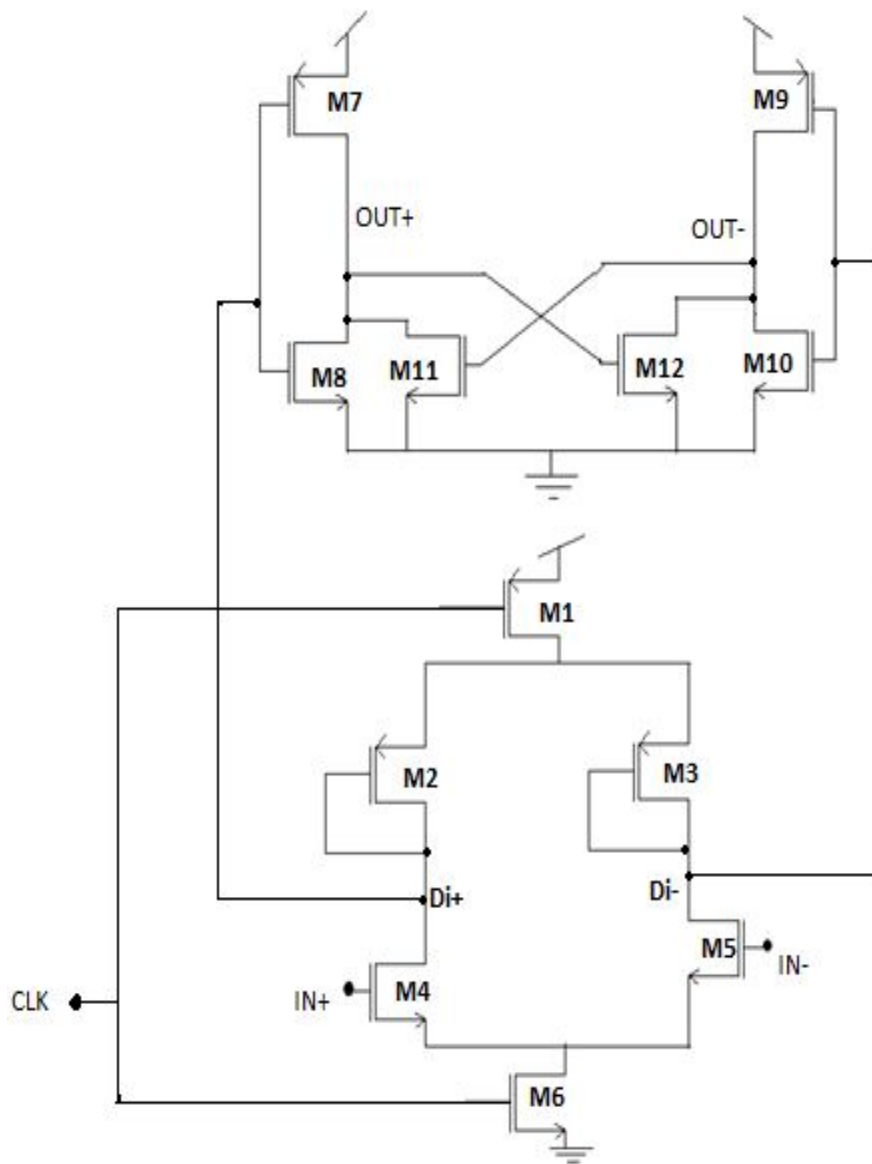


Fig 4.1 Proposed Comparator

Figure 5.1 shows the schematic (designed in Cadence) of the latched comparator circuit.[1]. The supply voltage of this comparator is 1.8 V. PULSE voltage source is used as input voltage source and reference voltage source is a DC voltage source having magnitude 0.9V.

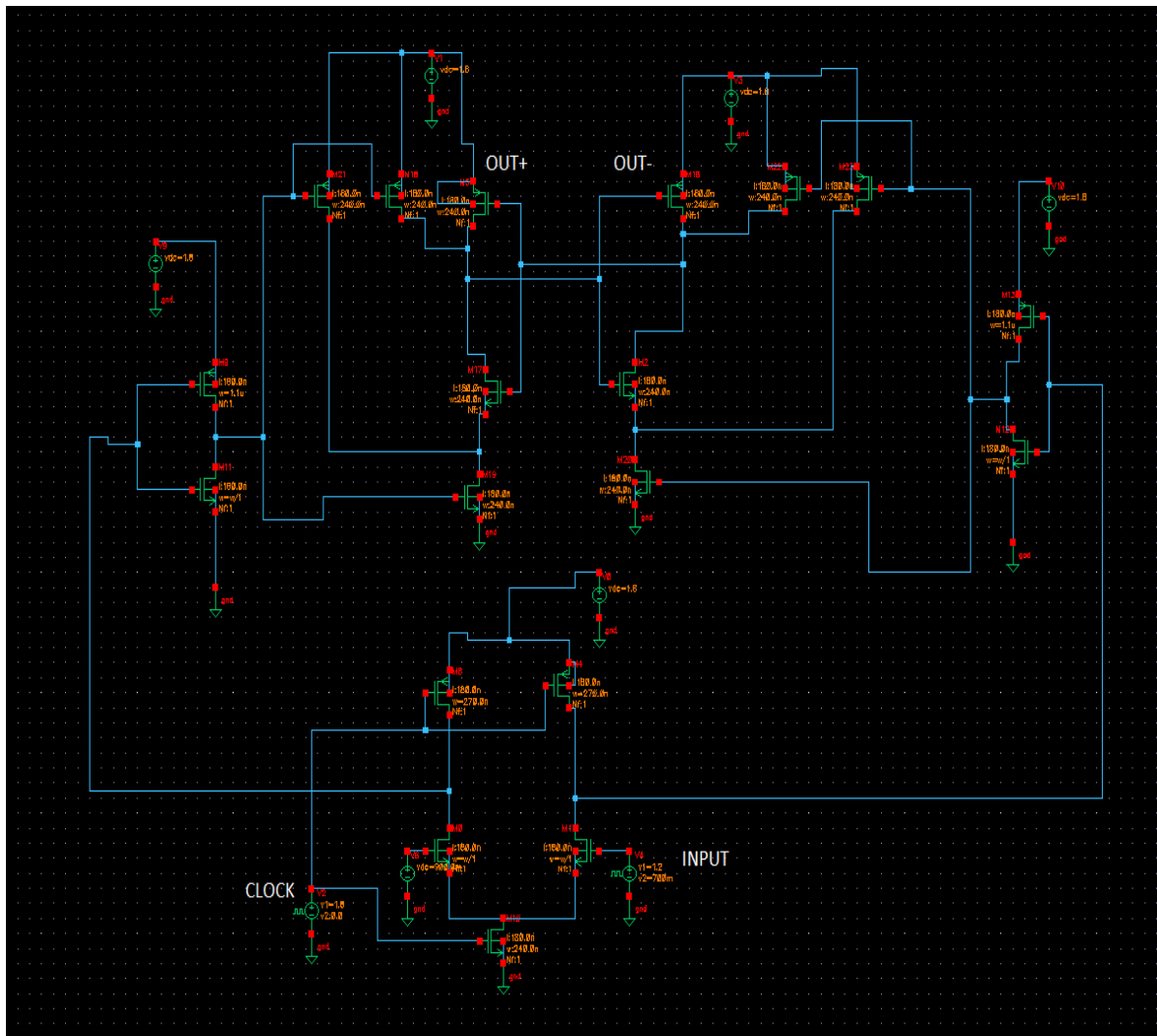


Fig 5.1 Reference comparator [1]

Figure 5.2 shows the Transient response of the above circuit. Whenever the clock goes low (reset phase) both OUT+ and OUT- are charged to Vdd. And when clock goes high OUT+ and OUT- are pulled down on basis of comparison.

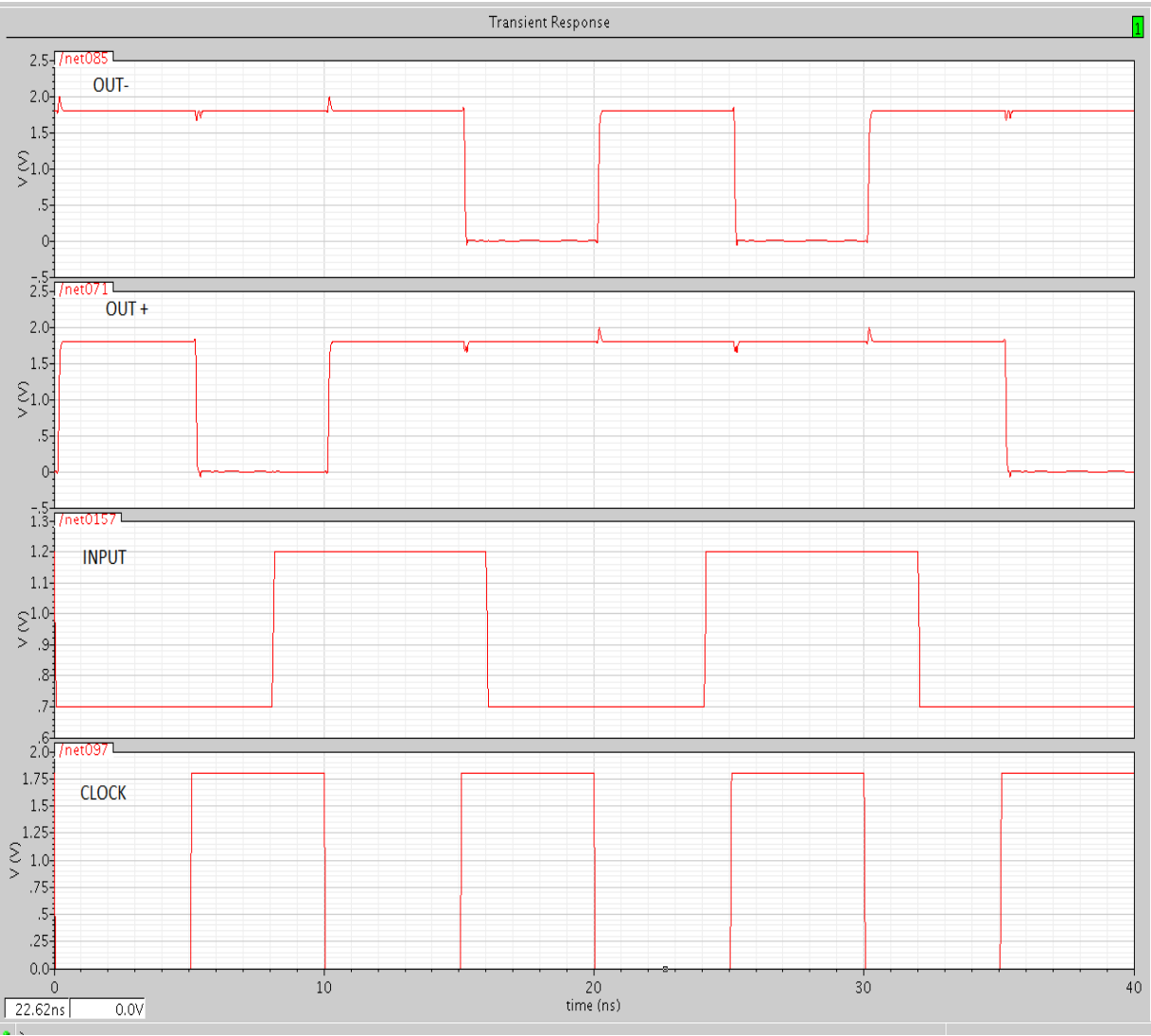


Fig 5.2. Transient response

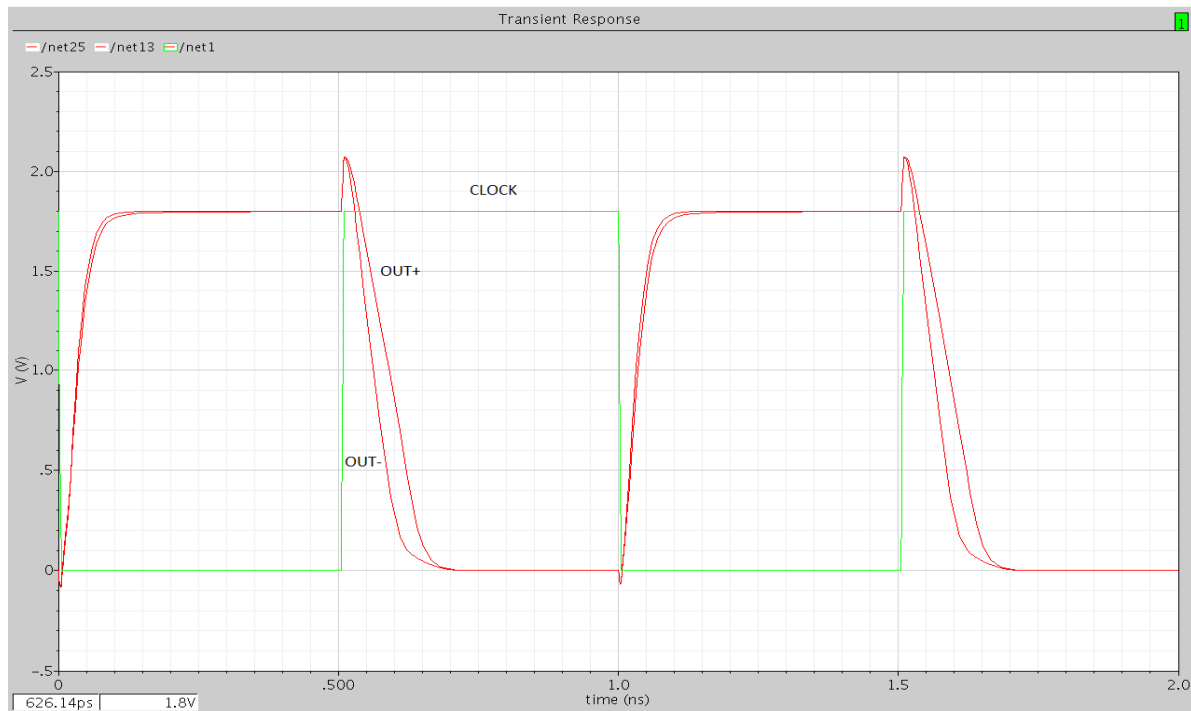


Fig 5.4. Transient response of circuit in figure 11.

Figure 5.5 shows the schematic (designed in Cadence) of the proposed input stage. The supply voltage of this comparator is 1.8 V. PULSE voltage source is used as input voltage source and reference voltage source is a DC voltage source having magnitude 0.9V.

Figure 5.6 shows the Transient response of the above circuit. The maximum swing at the output gets limited because of the diode connected transistor. The glitch height also gets reduced from 0.3v to 0.028v

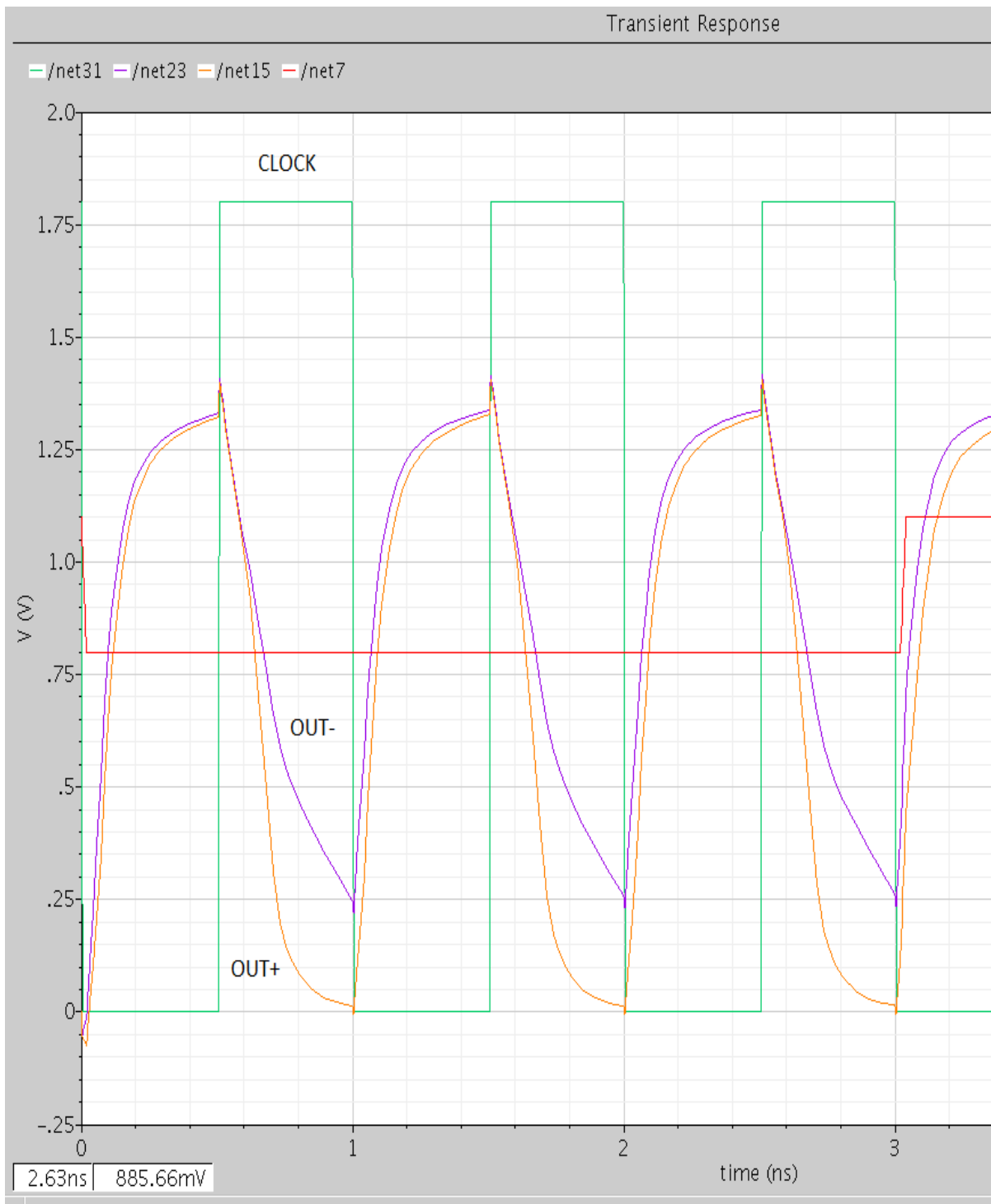


Fig 5.6 Transient response of the input stage.

Figure 5.7 shows the schematic (designed in Cadence) of the proposed latch. The supply voltage of this comparator is 1.8 V. PULSE voltage source is used as input voltage source and reference voltage source is a DC voltage source having magnitude 0.9V.

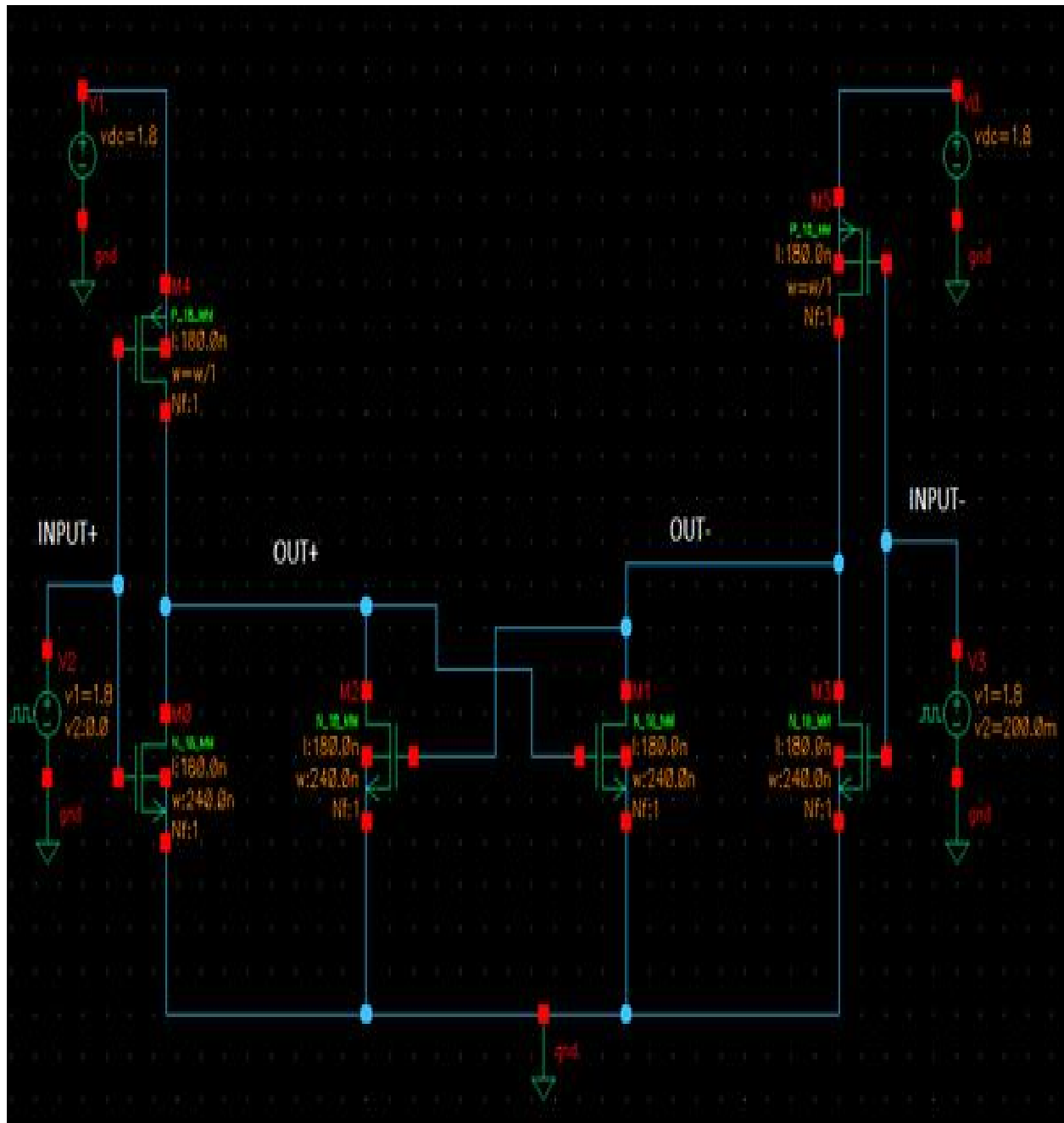


Fig 5.7 Proposed latch

Figure 5.8 shows the transient response of the proposed latch.

Transient Response

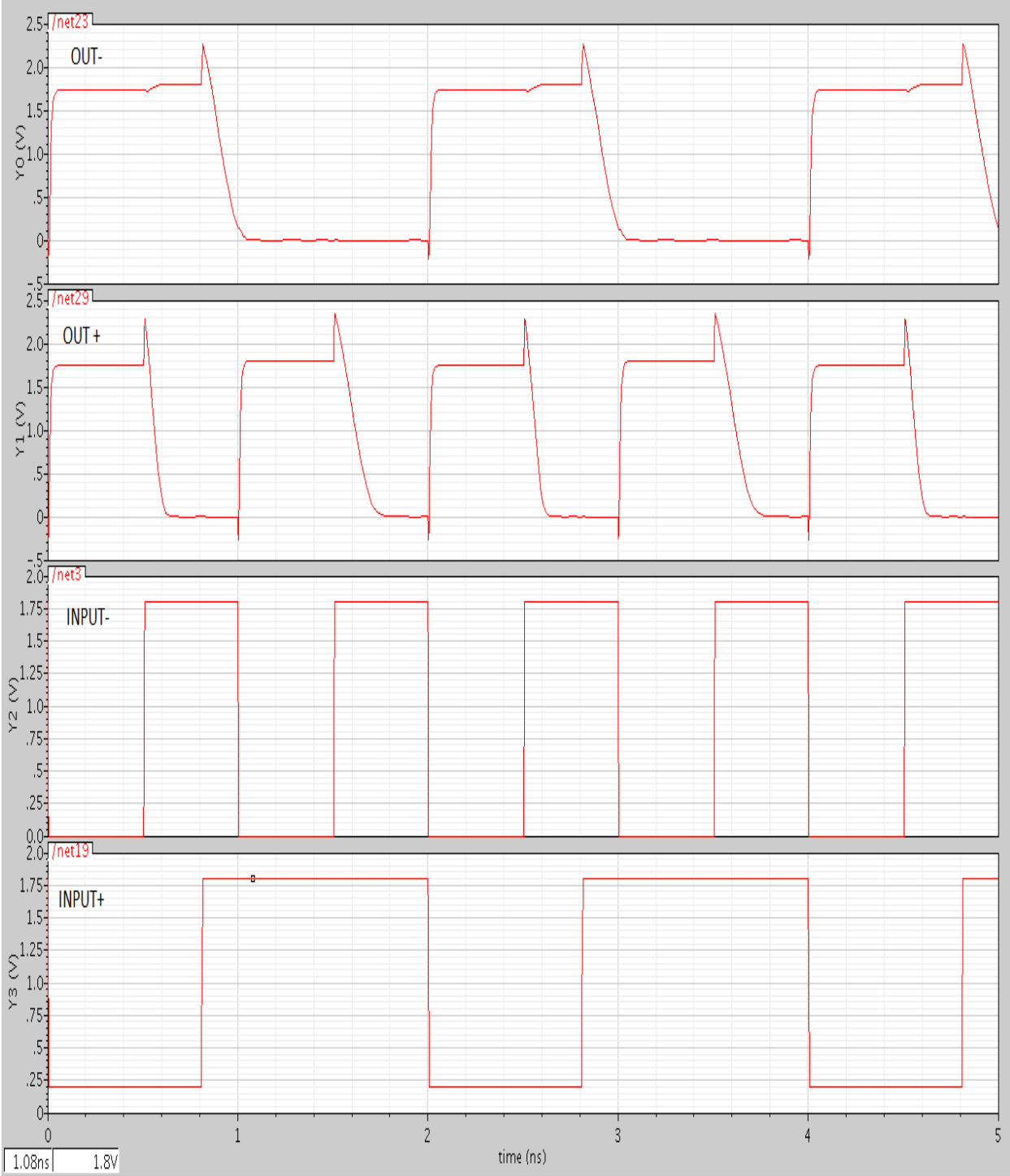


Fig 5.8 transient response of the proposed latch.

Figure 5.9 shows the schematic (designed in Cadence) of the proposed latched comparator circuit. The supply voltage of this comparator is 1.8 V. PULSE voltage source is used as input voltage source and reference voltage source is a DC voltage source having magnitude 0.9V.

Figure 5.10 shows the Transient response of the above circuit with clock frequency in GHz and figure 5.11 shows the transient response with clock frequency in MHz.

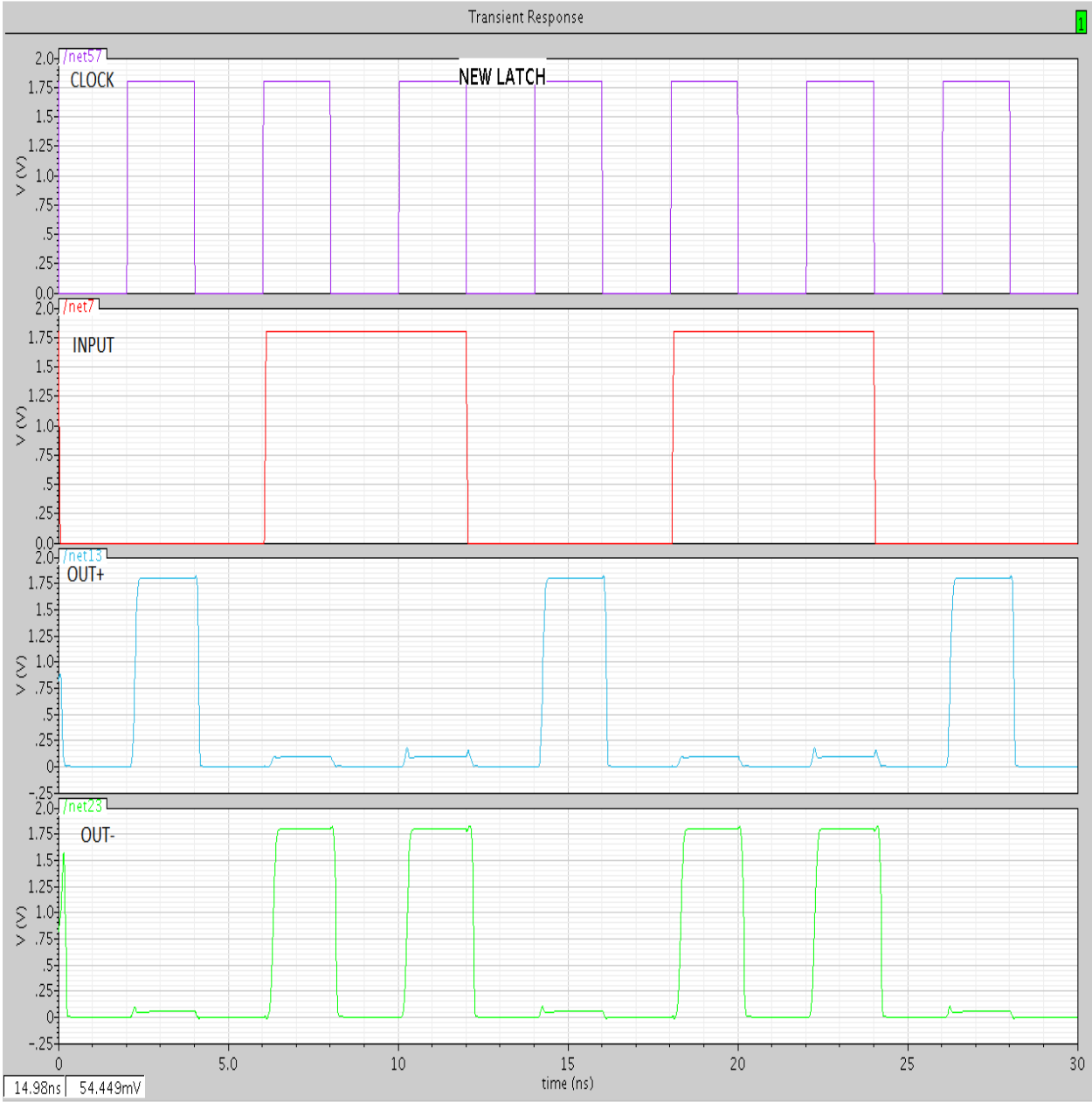


Figure5.10 Transient response of proposed circuit.

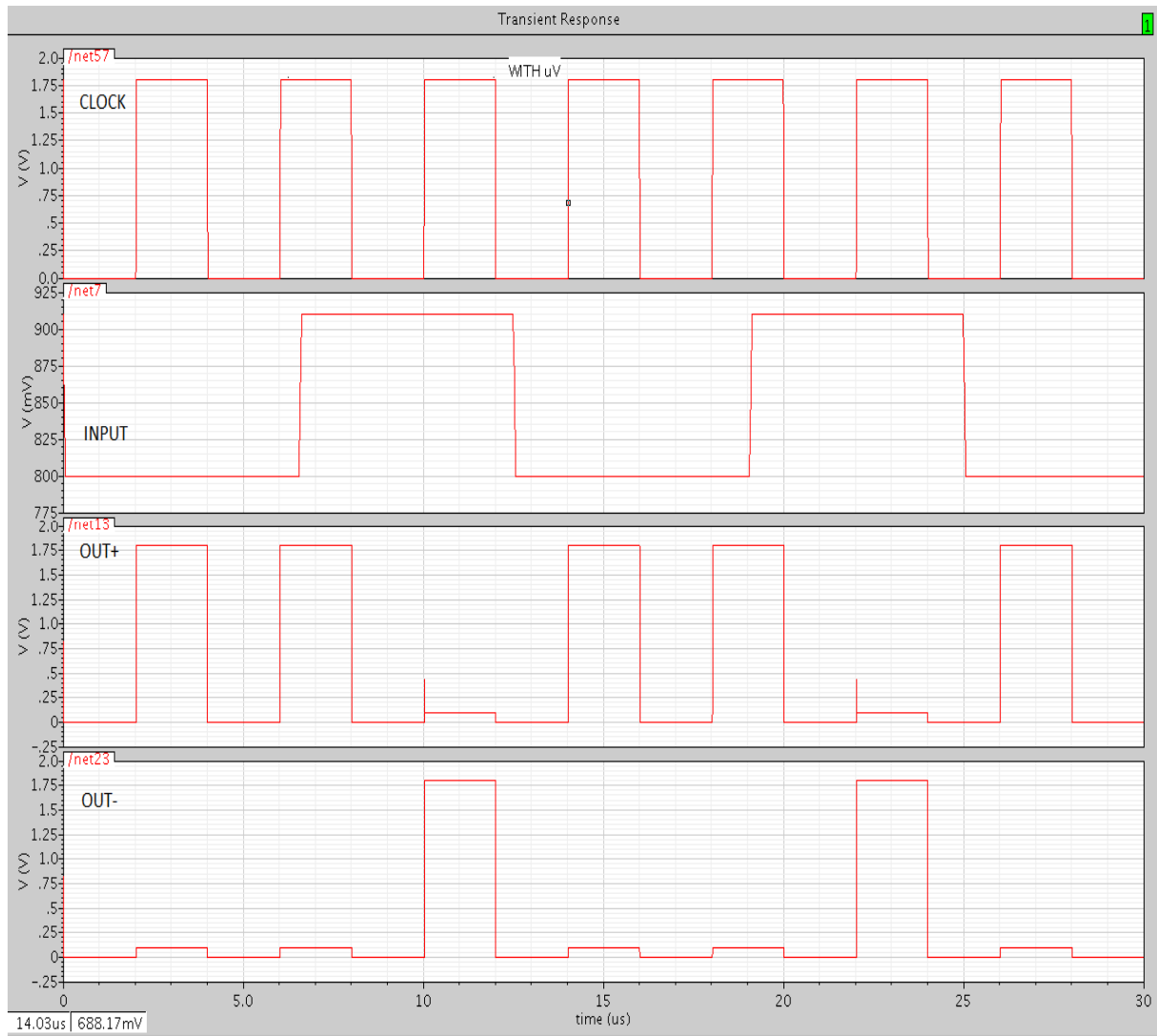


Fig 5.11 Transient Response Of Proposed Latch.

Chapter 6

CONCLUSION AND FUTURE SCOPE

In this thesis first the SAR ADC working was studied followed by a detail study of comparators. Different architecture of comparators were studied and their applicability to biomedical field was analysed as per the power consumed and size of the comparator. Finally few observations were made and a new architecture was designed and optimised for the biomedical application.

The power consumption, offset and delay calculation can be done to prove that the proposed latch is better than the one proposed in the reference[1]. Moreover proper swing is not obtained at the output of the comparator, the high voltage reaches 1.7V whereas the low voltage falls to minimum 0.1V, ways to improve the response can be worked on in future. Noise can be considered which is also one of the important factor. The architecture can further be optimized to achieve noise immunity.

Table 6.1 shows comparison of various architectures reviewed in this thesis and the proposed architecture

	Number of Transistors	Σ Width [μm]	Delay [ps]/ $\log(\Delta V_{in})$	Offset Voltage [mV]	Energy [fJ]/Decision
Comparator 1[19]	10	18.4	~59ps/decade	52mV	40.2fJ
Comparator 2[1]	11	18.4	~61ps/decade	20mV	39.8fJ
Comparator 3[3]	14	18.4	~33ps/decade	20.1mV	57.4fJ
Comparator 4[26]	15	18.4	~32ps/decade	19.1mV	46.7fJ
Comparator 5[4]	15	18.3	~45ps/decade	15.8mV	51.8fJ
Comparator 6[1]	19	18.3	~17ps/decade	16.3mV	52.8fJ
Proposed comparator	12	0.27	~30 ps/decade	20mV	-----

Table 6.1 comparison of various comparators

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