Ground Bounce Minimization in Low Power MTCMOS Circuits

A Dissertation submitted in the partial fulfilment of requirement for the award of degree of

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in

VLSI Design & CAD

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DECLARATION

I hereby declare that the work which is being presented in the dissertation entitled, **"GROUND BOUNCE MINIMIZATION IN LOW POWER MTCMOS CIRCUIS"** in partial fulfillment of the requirement for the award of degree of Master of Technology in VLSI Design & CAD submitted in Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of **Dr. Ravi Kumar,** Assistant Professor, ECED and refers other researcher's work which are duly listed in the reference section.

The matter presented in this dissertation has not been submitted in any other University/Institute for the award of degree.

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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ABSTRACT

Recently, there has been rapid progress in personal communication services (PCS) based on battery drives, including digital cellular phone, personal digital assistants, notebook and computers. In order to promote this development, low power design is essential to achieve the miniaturization and long battery life. Multiple Threshold CMOS (MTCMOS) power gating is one of the most effective techniques in reducing leakage power, which increases exponentially with device scaling. However, this technique suffers a major problem called ground bounce noise during active to sleep mode transition. During mode transition, a sudden current surge flows through parasitic inductance connected to power and ground pins due to packaging which causes voltage fluctuation or ground bounce on the supply line which affect the nearby circuits operating normally.

This dissertation is a comprehensive record of the work done toward minimization of ground bounce noise in the Digital VLSI Circuits. We analyzed this ground-bounce noise and reduced it with novel power-gating structures that utilize holistic integrated device circuit- architecture approaches. The efficiency of the technique has been tested on 16 bit ripple Carry Adder in 180nm CMOS technology. Furthermore performance of Ground bouncing reduction techniques have been compared with the available techniques for reducing ground bounce, not only for the ground bounce but also with respect to other parameter like leakage power, Energy Overhead, the maximum peak of current surge, Wakeup Delay and Area overhead. It is evident from the simulation result that there is approximately 92% of reduction in ground bounce from the proposed technique.

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V_{DD}	Positive supply voltage
I_D	Drain current
VGND	Virtual ground
GNDL	Ground node attached with package pin
VDDL	Voltage node attached with package pin
GBN	Ground bounce noise
ST	Sleep transistor
K_p	PMOS process trans-conductance parameter
K_n	NMOS process trans-conductance parameter
W	Channel width
L	Channel length
μ_n	Mobility of electrons
μ_p	Mobility of holes
C_{OX}	Oxide capacitance
Io	Bias current
V_T	Threshold voltage
V_{tn}	Threshold voltage of NMOS
V_{tp}	Threshold voltage of PMOS
V_{GS}	Gate to source voltage
V_{DS}	Drain to source voltage
U0	Voltage at virtual ground
$V_{D,SAT}$	Saturating Voltage

ABBREVIATIONS

VLSI	Very Large Scale Integration
GBN	Ground bounce noise
IC	Integrated Circuit
GND	Ground
RLC	Resistance, Inductance and Capacitance
ST	Sleep transistor
VGND	Virtual Ground
SPICE	Simulation Program with Integrated Circuit Emphasis
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
NMOS	N-channel Metal Oxide Semiconductor
PMOS	P-channel Metal Oxide Semiconductor
EDA	Electronic Design Automation
SRWS	Slow Rising Wakeup Signal

CHAPTER

1

INTRODUCTION & LITERATURE REVIEW

1.1 Background

High power consumption in portable electronics devices is an issue of serious concern. Shortening of battery life and additional packaging and cooling requirements are associated with high power consumption. Static power dissipation due to standby leakage currents is an important component of total power dissipation. Ubiquitous electronics devices contain different types of component of which many remain idle during a particular operation. Static power dissipation occurring in these idle components and leakage power dissipation in active component account for a huge percentage of total power dissipation in the system. The minimization of this leakage component becomes crucial for effective power management [1]. As a result of continued scaling of MOS devices, a dramatic enhancement in the performance of MOS devices has been achieved. This has led to increase in power dissipation due to leakage currents. Till now, the drain to source sub-threshold current has been the dominant leakage component.

The other driving force behind the low power design phenomenon is a growing class of personal computing devices, such as portable desktops, digital pens, audio and video-based multimedia products, and wireless communications and imaging systems, such as personal digital assistants, personal communicators and smart cards. These devices and systems demand high-speed, high-throughput computations, complex functionalities and often real time processing capabilities. The performance of these devices is limited by the size, weight and lifetime of batteries. Serious reliability problems, increased design costs and battery-operated applications prompted the IC design community to look more aggressively for new approaches and methodologies that produce more power-efficient designs, which means significant reductions in power consumption for the same level of performance [2].

Signal integrity is a crucial problem in VLSI circuits and is becoming increasingly important as the minimum feature size of devices shrinks to 180 nanometers and below. A major component of the circuit noise is the inductive noise. In fact, faster clock speeds and larger number of devices and I/O drivers as dictated by Moore’s Law (and therefore larger value of total circuit current) have resulted in increased amount of this type of noise in the power and ground planes (i.e. the noise, also known as the power/ground bounce). It is a critical and challenging design task to control the amount of inductive noise that is inserted in to the power planes [3].

The above challenges associated with low power Design have served as primary motivation for the present work which primarily deals with the issue of ground bounce in MTCMOS Circuits. The next section gives the available literature on Ground Bounce, its reduction technique and its related topic in MTCMOS circuits.

1.2 Literature Review

Suhwan Kim, et al. [1]: In this paper authors have analyzed the ground-bounce noise and reduced it with novel power-gating structures that utilize holistic integrated device circuit-architecture approaches. They control the amount of charge in the intermediate nodes of the circuit that passes through the sleep transistors during the wake-up transition and stabilize the minimum virtual power supply voltage required for data retention. These techniques have been proven in silicon using 65-nm bulk CMOS technology. They have investigated the ground bounce caused by large charge and discharge currents through a sleep transistor during the mode transition of a power-gating structure. Several novel power-gating structures utilizing holistic integrated device circuit- architecture approaches have been proposed to reduce the magnitude of voltage glitches in the power distribution network, as well as the time required for the network to stabilize. In addition, techniques have been presented to stabilize the minimum virtual power supply voltage required for data retention. The feasibility of their structures has been proved in silicon using very-deep sub micrometer bulk CMOS technology. Experimental results have shown that the ground bounce is reduced by switching power modes in a stepwise or pseudo random manner and that reliable data retention can be achieved by compensating for the effect of changes to the data-retention voltage caused by PVT variations.

Hailong Jiao, et al. [2]: In this paper, the effectiveness of different noise-aware MTCMOS circuit techniques to deal with the ground bouncing noise phenomenon is evaluated. An intermediate relaxation mode is investigated to gradually dump the charge stored on the virtual ground line to the real ground distribution network during the sleep to active mode transitions. In this paper, the ground bouncing phenomenon in MTCMOS circuits is investigated. The peak amplitude of the ground bouncing noise were reduced by up to 69.17% with the noise-aware MTCMOS circuits without sacrificing the savings in leakage power consumption as compared to the standard MTCMOS circuits in a 90nm CMOS technology. A novel tri-transistor controlled power gating structure is introduced to effectively suppress the ground bouncing noise in gated- VDD & ground MTCMOS circuits. A two-step activation scheme with an intermediate relaxation period is investigated with various MTCMOS circuit techniques. The lowest ground bouncing noise is produced by the tri-mode technique among the MTCMOS circuit techniques evaluated in this paper. The noise generation mechanisms during the sleep to active mode transitions are identified. Different noise-aware MTCMOS circuit techniques are characterized and evaluated. The tri-mode technique also suffers from the smallest area overhead among the noise-aware MTCMOS circuit techniques. All the noise aware MTCMOS circuit techniques provide significant leakage savings comparable to the standard MTCMOS circuits.

Payam Heydari, et al. [3]: This paper is concerned with the analysis and optimization of the ground bounce in digital CMOS circuits. In this paper, an analytical method for calculating the ground bounce is presented and the proposed method relies on accurate models of the short-channel MOS device and the chip-package interface parasitic. Thereafter the effect of ground bounce on the propagation delay and the optimum tapering factor of a multistage buffer were discussed and a mathematical relationship for total propagation delay in the presence of the ground bounce is obtained. Effect of an on-chip decoupling capacitor on the ground bounce waveform and circuit speed is analyzed next and a closed form expression for the peak value of the differential- mode component of the ground bounce in terms of the on-chip decoupling capacitor is provided and finally a design methodology for controlling the switching times of the output drivers to minimize the ground bounce is presented. In this paper, authors have proposed a detailed analysis and optimization of the off-chip ground bounce using an accurate and simple chip-package interface circuit model. The effect of ground bounce on the tapered buffer design was studied, and a mathematical analysis was introduced and the effect of the on-chip decoupling capacitor was analytically investigated, and a method to find a closed form expression for the peak value of the differential-mode component of the ground bounce as a function of the decoupling capacitor was proposed. Finally, a new skew control method for ground bounce optimization was proposed. Experimental results confirmed the effectiveness of this method in reducing the ground bounce.

Hailong Jiao, et al, [4]: In this paper, sleep signal slew rate modulation techniques for suppressing mode-transition noise are explored for Power and ground distribution network noise produced during SLEEP to ACTIVE mode transitions. A triple-phase sleep signal slew rate modulation (TPS) technique with a novel digital sleep signal generator is proposed. Reactivation time, mode-transition energy consumption, leakage power consumption, and layout area of different MTCMOS circuits are characterized under an equal-noise constraint. Influences of within-die and die-to-die parameter variations on the reactivation noise, time, and energy consumption of sleep signal slew rate modulated MTCMOS circuits are evaluated with a process imperfections aware robustness metric.

R. Bhanuprakash, et al. [5]: In this paper, a high performance stacking power gating structure is introduced which minimizes the leakage power and provides a way to control the ground bounce noise in transition mode. Stacking power gating technique has been analyzed and the conditions for the important design goals such as minimum ground bounce noise and minimum wakeup latency have been derived. The tradeoff between the ground bounce noise and wakeup latency has been explored for high performance power gating logic circuits. Further, to evaluate the efficacy of the proposed stacking power gating technique, simulation has been done using proposed technique and implemented on basic 2-input NAND gate circuit with 90nm technology. The leakage current is reduced by 81.1% over the conventional power gating technique. Ground bounce noise has also been reduced to 76.28% as comparison to the conventional power gating technique. In this paper a high performance stacking power gating structure has been presented which minimizes the leakage power as well controls the ground bounce noise in transition mode.

Masud H. Chowdhury, et al. [6]: In this paper, an analysis of ground bounce due to power mode transition in power gating structures is presented. An innovative power gating approach is proposed in the paper, which in addition to targeting maximum reduction of major leakage currents will provide a way to control ground bounce during power mode transition. This proposed power gating technique would have an additional intermediate HOLD mode along with conventional CUTOFF and RUN modes. Its stepwise turning on feature will provide higher reduction of the magnitude of peak current and voltage glitches in the power distribution network as well as the minimum time required to stabilize power and ground as compared to other similar techniques. It is imperative that the large magnitude of ground bounce due to power mode transition in power gating scheme must be addressed to ensure signal and power integrity. This paper provides a brief summary of the generation and propagation mechanisms of ground bounce noise in during power gating. In this paper, an innovative power gating technique to simultaneously reduce leakage and ground bounce is proposed and the HOLD mode could be utilized as an intermediate mode to perform a stepwise transition. This proposed power gating structure through its stepwise turning on feature would provide much higher reduction of the magnitude of peak current and voltage glitches in the power distribution network as well as the minimum time required to stabilize power and ground as compared to other similar techniques. Since leakage and ground bounce are the two critical sources of noise in current nanoscale circuits and systems, reduction of leakages and ground bounce would definitely increase the reliability. However, simulation result presented in paper shows that the reduction of voltage level across the logic circuit during data retention mode will drastically reduce the noise tolerance of the circuits during that mode. A related concern is the reduction of logic swing in this mode.

Manisha Pattanaik, et al. [7]: In this paper, low leakage 1bit full adder cells are proposed for mobile applications with low ground bounce noise and a novel technique have introduced with improved staggered phase damping technique for further reduction in the peak of ground bounce noise. As technology scales into the nanometer regime ground bounce noise and noise immunity are becoming important metric of comparable importance to leakage current, active power, delay and area for the analysis and design of complex arithmetic logic circuits. Noise immunity has been carefully considered since the significant threshold current of the low threshold voltage transition becomes more susceptible to noise. They introduced a new transistor resizing approach for 1bit full adder cells to determine the optimal sleep transistor size which reduce the leakage power and ground bounce noise. The simulation results depicts that the proposed design also leads to efficient 1bit full adder cells in terms of standby leakage power, active power, ground bounce noise and noise margin. Noise immunity of proposed full adder cells are comparable to the conventional adder cell (Base case). The proposed novel technique has been introduced with improved staggered phase damping technique for further reduction in the peak of ground bounce noise and overall power mode transition noise**.** They have performed simulations using Cadence Spectre 180nm standard CMOS technology at room temperature with supply voltage of 1.8V.

Liyi Xiao, et al. [8]: In this paper, an analytical model is proposed to calculate the voltage fluctuations during the turn on progress of the power gated circuits, and this model can be used to estimate the maximum and period of the fluctuations. A standard CMOS 90nm process is used to validate the model. The runtime could be greatly reduced. Power gating has been proved to be one of the most effective techniques to reduce the leakage power in the CMOS digital circuits. However, ground bounce effect will be introduced due to the turning on process of the power gating circuits, which could cause severe problems to the entire circuit. In this paper, an analytical model is established, with which the maximum peak value and the period of the voltage fluctuation induced by ground bounce effect could be effectively estimated. Simulation results show that the operation time could be greatly reduced at the average cost of 10.18% and 9.98% accuracy loss for the period and maximum peak value estimation compared with SPICE simulation.

Suhwan Kim, et al. [9]: In this paper, the authors introduced and analyzed the ground bounce due to power mode transition in power gating structures and to reduce the ground bounce. They proposed novel power gating structures in which sleep transistors are turned on in a non-uniform stepwise manner. Their power gating structures reduce the magnitude of peak current and voltage glitches in the power distribution network as well as the minimum time required to stabilize power and ground. Experimental simulation results with Power spice fixture in a package model demonstrate the effectiveness of the proposed power gate switching noise reduction techniques. This paper investigated the ground bounce caused by large discharge current through a sleep transistor during the mode transition of the power gating structure. Two novel power gating structures were proposed to reduce the magnitude of voltage glitches in the power distribution network as well as the time required for the network to stabilize. In Power spice simulation of a 16-bit arithmetic and logic unit (ALU) with a DIP-40 package model, the maximum magnitude of voltage glitches on the VDDL and GNDL rails of the ALUs with their power gating structures were reduced by up to 89.04% and 88.40%, respectively, compared to the ALU with a conventional gating structure.

Hailong Jiao, et al. [10]: In this paper a new forward body bias technique is proposed to minimize the ground bouncing noise with smaller sleep transistors in MTCMOS circuits. The new forward body bias technique lowered the peak ground bouncing noise by up to 15.43% while reducing the size of the additional sleep transistors by up to 52.38% as compared to the previously published noise aware MTCMOS techniques with standard zero-body-biased sleep transistors in a 90nm CMOS technology. The design tradeoffs between the ground bouncing noise and the leakage power consumption in body-biased MTCMOS circuits were evaluated. The proposed forward body bias technique is presented in this paper to lower the ground bouncing noise with smaller sleep transistors in MTCMOS circuits. A novel forward body bias generator is also proposed to dynamically tune the threshold voltage of the Parker for the different modes of operation of a tri-mode MTCMOS circuit.

Rahul Singh, et al.[11]: In this paper, to suppress the ground bounce noise with a minimal wake-up time penalty, a three-step turn-on strategy and its corresponding power-gating structure are proposed. During the circuit’s metastable region of operation, specifically, the amount of current flowing through the sleep transistors is precisely controlled while the virtual or circuit power supply is quickly boosted when the internal nodes of the circuit are stable. In 65 nm CMOS technology, simulation results demonstrated that their technique reduces the peak amplitude of the ground bouncing noise by up to 94% as compared to the conventional abrupt turn-on technique. This paper introduced a novel scheme for implementing the wakeup transition of a power-gating circuit in a controlled three-step manner. Based on the state of the internal nodes, the wake-up mode is divided into three stages: Pre-boosting, Noise-limiting and Post-boosting. A large current is provided to the logic block during the Pre-boosting and the Post-boosting stages while a limited current is supplied in the Noise-limiting stage. In the paper, transition between the stages is controlled by a signal-control FSM which utilizes feedback from the virtual VDD node to force the power gating circuit into one of the three stages.

Hailong Jiao, et al. [12]: In this paper, the effectiveness of different noise-aware combinational MTCMOS circuit techniques to deal with the ground-bouncing-noise phenomenon is evaluated. An intermediate relaxation mode is investigated to gradually dump the charge stored on the virtual lines to the real ground distribution network during the SLEEP to ACTIVE mode transitions. The dependence of ground bouncing noise on the sleep transistor size and temperature is characterized with different power-gating structures. The peak amplitude of ground bouncing noise is reduced by up to 76.62% with the noise-aware techniques without sacrificing the savings in leakage power consumption as compared with standard MTCMOS circuits in a 90-nm CMOS technology. The ground bouncing phenomenon in standard MTCMOS circuits have been investigated in this paper. The noise-generation mechanisms during the SLEEP to ACTIVE mode transitions are identified. Different noise-aware combinational MTCMOS circuit techniques to effectively suppress the ground bouncing noise were presented. A two-step activation scheme with an intermediate relaxation period is investigated with various MTCMOS circuit techniques. The dependence of the ground bouncing noise on the sleep transistor sizes and the die temperature were evaluated. Depending on the sizes of the additional controlling transistors, the lowest ground bouncing noise is produced by either the trimode or the TTL technique among the MTCMOS circuits evaluated in this paper.

1.3 Design Issue

VLSI designs are being a matter of compromise. The following parameter need to be taken care of while implementing a particular ground bounce noise reduction technique. There are some parameters whose optimization is subject to implementation of a particular ground bounce noise reduction technique is a design challenge itself. These parameters are enlisted as follows:-

Wake up delay, Energy overhead, Current Surge, area overhead, leakage power.

Furthermore, the dimension at which ground bounce noise become more prominent are well into the submicron region calling for a new modeling and estimation approach. These challenges have been discussed in the subsequent chapters and section.

1.4 Specific Aspect of this Dissertation

- This dissertation applies four ground bounce reduction technique to a prototype 16 bit ripple carry adder and a comparative analysis of their performance is presented.

- After applying each technique on the prototype circuits, their efficacy with respect to other vital parameter e.g. wakeup delay etc has been assessed.
- Analytical model of ground bounce have been described.
- According to the best of the author’s knowledge, this work on ground bounce minimization is a first of its kind, which taken into account the effect of applying ground bounce noise minimization technique of other parameter of the circuits.

1.5 Outline of the Dissertation

Following the introduction and literature review, the dissertation is organized as follows:

Chapter 2: In this chapter, the introduction of multi threshold CMOS technique for low power consumption for devices is presented. Its drawback in submicron technology such as ground bounce effect, delay and area is presented. The introduction of full adder used for the analysis of ground bounce and its reduction technique is presented.

Chapter 3: In this chapter, the brief introduction of ground bounce in MTCMOS circuits, its cause and its adverse effect on performance of circuits and its effect on different parameter is studied.

Chapter 4: In this chapter, the popular ground bounce reduction technique in MTCMOS circuits is studied. The novel technique for ground bounce reduction technique is presented.

Chapter 5: In this chapter, the simulation result of the different ground bounce noise for MTCMOS technique based 16 bit full adder is studied. The comparative study of the different topology used and the novel power gating technique for suppressing the ground bounce effect on different parameter is analyzed.

Chapter 6: This chapter includes the conclusion of work and the scope for future extension of the work.

CHAPTER

2

GROUND BOUNCING IN MTCMOS CIRCUITS

2.1 Introduction of MTCMOS

With the feature size of the CMOS transistors scaling down, the device density on a chip increases rapidly and power dissipation has become a critical concern in modern IC design methodology. The power factor has always been one of the most important determinants. With the recent trend for high-performance portable SOC for communication and computing, power dissipation has become even more critical design constraint [14].

In most hand-held devices the leakage during intermittent idle periods is the single most dominating component of total power that determines portability and power efficiency. The leakage power is expected to reach more than 50% of total power in the recent technology generation. In current and future designs, whether chips are packaged individually, multiple chips are packaged together, or a complete system is built on a single substrate, power gating technique is expected to become a standard and integral part of performance improvement schemes for handling power and reliability challenges imposed by increasing leakages [11].

In order to reduce the overall power consumption of modern high performance integrated circuits, a well-known technique is to scale supply voltages. However, to maintain performance and the operating speed, devices threshold voltages must scale as well, which cause an exponential increase in sub-threshold leakage currents. However, the leakage current of the CMOS transistor experiences an exponential growth with the threshold voltage reduction.

Multi-Threshold CMOS (MTCMOS), also known as power/ground gating, is the most commonly used circuit technique for leakage power reduction [15]. An integrated circuit is typically divided into multiple autonomous power/ground gating domains for effective reduction of leakage power consumption [16].

Reducing these leakage currents is crucial for burst-mode type circuits, where the system spends the majority of time in an idle standby and a failure to control the leakage currents can greatly reduce the battery life. As a result, leakage power is now playing a major role in the total power of VLSI circuits.

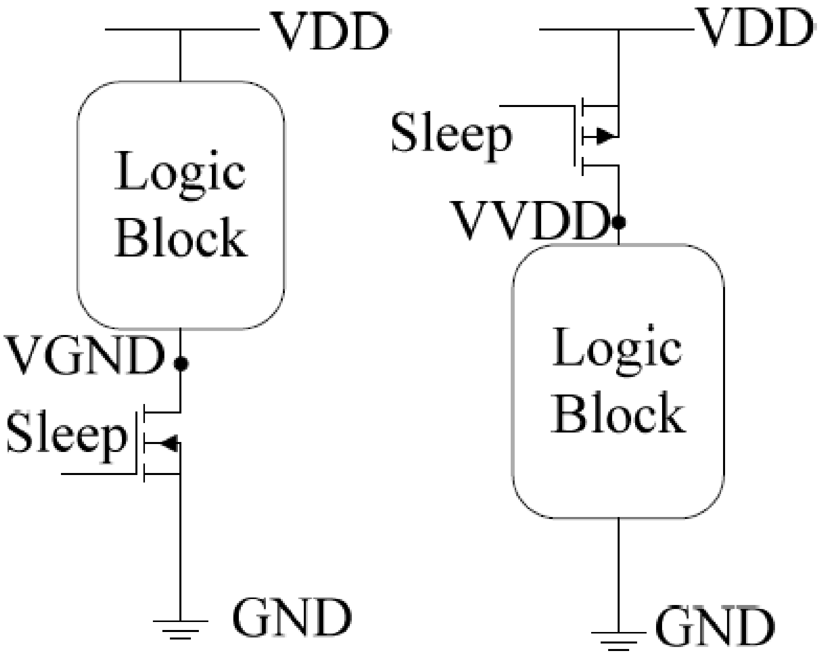

Figure 2.1 The schematic of power gating circuits [8]

The multi-threshold CMOS (MTCMOS) circuit is an effective technique for suppressing the leakage power in standby mode while still permitting high-speed operation in active mode. The power gating switch is typically positioned between the circuit power supply (or circuit ground) and the actual power supply rail (or the actual ground rail) [5]. During the active mode, the sleep transistor is switched ‘on’ ensuring normal operation. During the idle (or sleep) mode however, the sleep transistor is switched ‘off’ to block leakage paths between the power and ground rails which could otherwise steadily draw power even during standby. Usually, the threshold voltage (Vth) of the sleep transistor is higher than the logic, as a result of which, power gating is also called Multi-Threshold CMOS technology.

2.2 Operation of MTCMOS technique:

The power gating circuit could work in three different modes:

1) Active mode, in which the sleep transistor is on and the circuit function normally.

2) Sleep mode, in which the sleep transistor is shut-off and the leakage current of entire circuit is suppressed. The sleep transistor is switched 'off' to block leakage paths between the power and ground rails which could otherwise steadily draw power even during standby.

3) Transition mode, in which the sleep transistor is turned on and the circuit goes from sleep to active [6]. Ground Bounce effect usually occurs in transition mode.

2.2.1 Limitation of Power Gating

However, power gating is not a cost-free technique. The inserted STs introduce area and delay overhead. Besides, the instantaneous current formed during turning on the ST may induce voltage fluctuations on the ground line within the chip through the parasitic parameters of the package, which could prevent the logic blocks nearby from normally functioning. This phenomenon is called ground bounce effect. Ground bounce will increase the turn-on time of power gating circuit and consuming more dynamic power.

If the sleep transistor is turned off during the sleep period the virtual ground (*VGND*) node of the power gating structure is charged up to a steady state value close to *VDD*. Consequently, data is lost from the storage elements, and an extra data recovery process is required leading to degradation of system performance. Besides, the instantaneous discharge current through the sleep transistor operating in its saturation region creates current surges at the sleep/active mode transition, which in turn, causes voltage fluctuations in the on-chip power distribution network due to the bonding wire and on-chip parasitic inductance (Figure 2.2). This voltage fluctuation - also known as ground bounce, which is associated with the switching of I/O buffers and internal digital circuitry, and clock gating [2], [4], is one of the growing concerns for the reliability of power deliver in nanoscale systems.

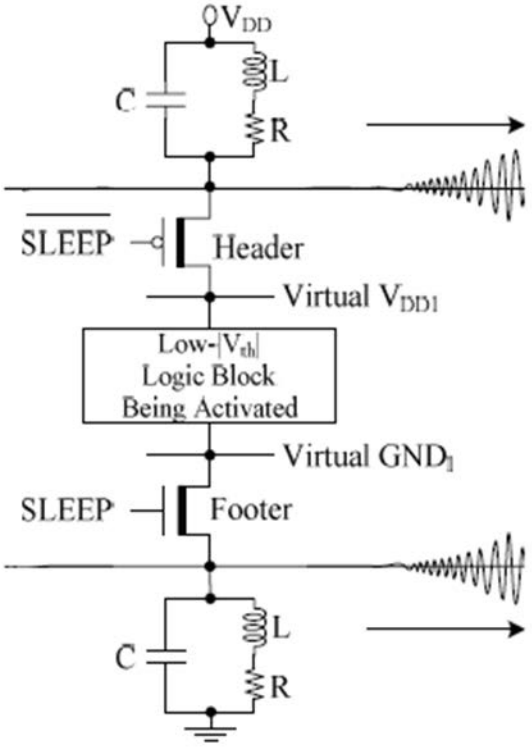

Figure 2.2: Ground bounce due to power gating [10]

Mode transition noise produced by an awakening circuit block propagates to the already active circuit blocks in the neighboring domains through the shared power and ground distribution networks. Logic states of internal nodes in surrounding active circuits are disturbed due to significant noise. With more frequent transitions between the ACTIVE and SLEEP modes of operation to achieve more effective leakage power savings, ground bouncing noise has become an important reliability concern in modern integrated circuits.

The parasitic capacitance of the power and ground rails form multiple resonance circuits with the lead inductances. Until now, ground bounce originating from the power-mode transition of a power gating structure was not seriously considered. However, its effects on the reliability of SOC employing multiple power gating domains to control leakage power can no longer be ignored. Therefore, controlling ground bounce is very crucial for reliability of power deliver and circuit operation in system-on-chip in nanometer regime [6].

Since the ground bounce effect has negative impacts on the performance of the power gating circuits, it is important to estimate the ground bounce effect in the early design time.

2.3 Ground Bounce in Digital VLSI Circuits

Ground Bounce is one of the primary causes of false switching in high speed components and is a major cause of poor signal quality. While ground bounce is easily measured on CMOS components, an accurate measurement is somewhat elusive on bipolar or BiCMOS components [2]. Ground Bounce is a voltage oscillation between the ground pin on a component package and the ground reference level on the component die. Essentially it is caused by a current surge passing through the lead inductance of the package. The effect is most pronounced when all outputs switch simultaneously, (hence the alternate name, Simultaneous Switching Noise). While the inductance is the combined effect of the package lead, the package lead frame, the bond wire and the inductance in the die pad, most of the inductance is caused by the bond wire.

The ground bounce effect originating from the turn-on instantaneous current could result in not only the voltage fluctuations on the GNDL but also electro-migration, which may cause severe problems in the power gating circuit.

Signal integrity is a crucial problem in VLSI circuits and is becoming increasingly important as the minimum feature size of devices shrinks to 180 nanometers and below. A major component of the circuit noise is the inductive noise. In fact, faster clock speeds and larger number of devices and I/O drivers as dictated by Moore’s Law (and therefore larger value of total circuit current) have resulted in increased amount of this type of noise in the power and ground planes (i.e., the noise, also known as the power/ground bounce). It is a critical and challenging design task to control the amount of inductive noise that is inserted in to the power planes [3].

Package pins, bonding wires, and on-chip IC interconnects all have parasitic inductances. When an inductor current experiences time-domain variation, a voltage fluctuation is generated across the inductor. This voltage is proportional to the inductance of the chip-package interface and the rate of change of the current. As a result, when the logic cells in a circuit are switched on and off, the voltage levels at the power distribution lines of the circuit fluctuate. This inductive noise is sometimes referred to as the simultaneous switching noise because it is most pronounced when a large number of I/O drivers switch simultaneously [3].

2.3.1 Modeling the chip-package interface parasitics

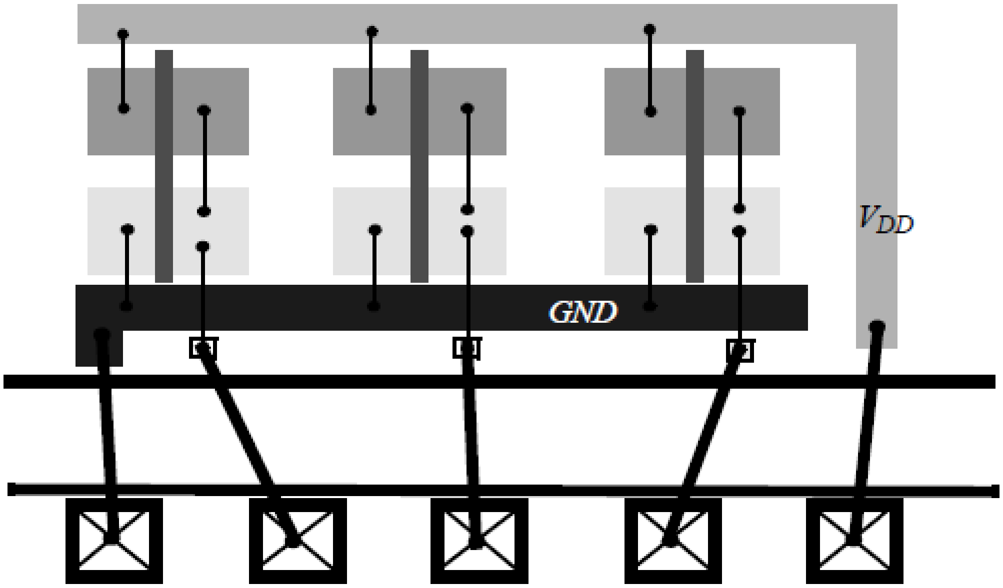

Figure 2.3: layout schematic for the output drivers along with the bonding wires, pads and package pins. [3]

Due to the large slew rates of the currents flowing through the bond wires and package pins, the ground and supply voltage seen by the output drivers experience bouncing due to the parasitic associated with the package and connections to the chip. Fluctuations on the supply and ground rails are further increased when output drivers switch simultaneously.

The P/G bounce noise is the switching noise on the power-supply and ground lines which consists of the resistive *IR* drop due to bond wire and trace resistances, inductive –noise due to the chip-package interface inductance including bond wire self-inductance, trace self inductance, trace-to-trace mutual inductance, and capacitive coupling due to the chip-package interface cross-coupling capacitances. While, due to circuit innovations and device scaling, the speed and accuracy of integrated circuits have steadily increased, the performance of packages, especially for low-cost applications, has not significantly improved. This trend follows from the rather poor scalability of packaging technology and the design environments in which these packages are being employed.

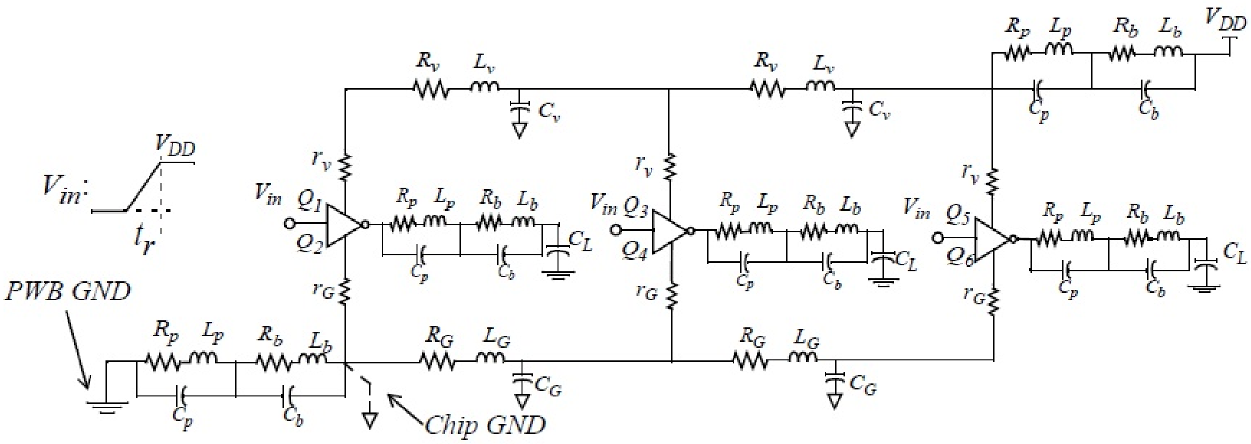

Figure 2.4: The circuit representation of Fig. 2.3 [3]

In general, there are two major inductive components which contribute to the total ground bounce namely the inductive noise due to the on-chip interconnect, and the inductive noise due to the chip package interface consisting of bond wire self-inductance, trace and pin self-inductances, and trace-to-trace mutual inductance.

Shown in Fig. 2.4 is the electrical model of Fig. 2.3 The on-chip power/ground wires are modeled as a single RLC circuit (*RG*,*LG*,*CG*) for the on-chip ground wire and a single RLC circuit (*Rv*,*Lv*,*Cv*) for the on-chip power-supply wire. The off-chip drivers are normally placed in a close proximity to the pads and bond wires.

Power gating is one of the most effective techniques in reducing leakage power, which increases exponentially with device scaling. However, large ground bounces during abrupt changes of power mode may cause unwanted transitions in neighboring circuits, which should still be operating normally**.**

There has been a lot of work on the multi-threshold voltage CMOS (MTCMOS) technique, which uses a MOSFET switch to gate, or cut off, a circuit from its power rail(s) during standby mode. However, without a clear understanding of the technique, the negative effects of power gating and the range of device options may overwhelm the potential benefits. The power-gating switch is typically positioned between the circuit and the power supply rail or between the circuit and the ground rail. During active operation, the power-gating switch remains on, supplying the current that the circuit uses to operate. During standby mode, turning off the power-gating structure reduces the current dissipated through the circuit. Since the switch gates the power when the circuit is in standby, it is also commonly called a sleep transistor.

Many vendors of low-power embedded products now include a power-gating capability in the form of “sleep” modes, which typically operate under software control. When the operating system detects a long idle loop, one of the several processor cores continues to run at its maximum operating frequency, while the other cores are power-gated off .

By turning off the sleep transistor during the sleep period, however, all the internal capacitive nodes of the logic blocks and virtual VDD (VVDD) nodes are discharged to a steady-state value near ground [16]. During a power-mode transition, an instantaneous charge current passes through the sleep transistor, which is operating in its saturation region, and creates current surges elsewhere. Because of the self-inductance of the off-chip bonding wires and the parasitic inductance inherent to the on-chip power rails, these surges result in voltage fluctuations in the power rails. If the magnitude of the voltage surge or drop is greater than the noise margin of a circuit, that circuit may erroneously latch to the wrong value or switch at the wrong time.

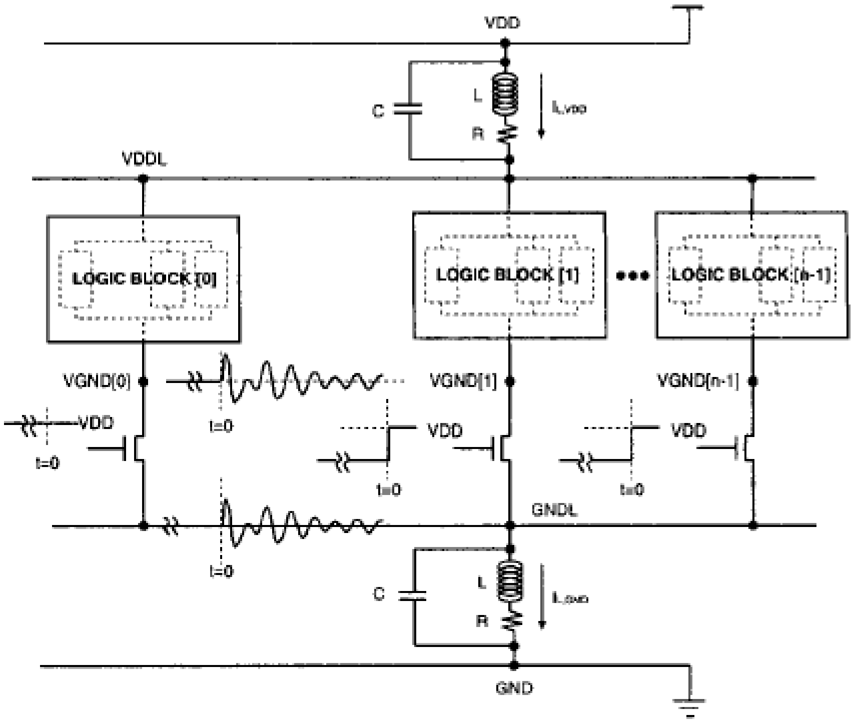

Figure 2.5: Ground bounces in a SOC employing multiple power-gating structures to control leakage power [9]

Inductive noise, also known as simultaneous switching noise, is a phenomenon that has been traditionally associated with input/output buffers and internal circuitry. In the past, inductive noise originating from power-mode transitions between the active and standby modes of a power-gating structure was not considered serious, but it is likely to become an important issue in the design of a system-on-a-chip (SOC) that employs multiple power-gating domains to control leakage power. As shown in Fig.2.5, inductive noise can induce ground bounce in nearby circuits, which should still be operating normally. The noise immunity of a circuit decreases as its supply voltage is reduced. It is therefore essential to consider using a technique such as power gating to address the problem of ground bounce in low-voltage CMOS circuits [9].

2.4 Understanding Ground Bounce

It is important to understand the mechanism for measuring the device ground, which is to monitor an I/O driving out low, commonly referred to as a quiet pin. Since ground pins are connected directly to the board ground, monitoring a ground pin will represent the board ground, not the internal device ground. Problems occur when the amplitude of the ground bounce becomes too large. Signals may be misinterpreted because the relative ground levels are different for the driving device and the receiving device. This discrepancy can cause a logic 0 to be interpreted as a logic 1.

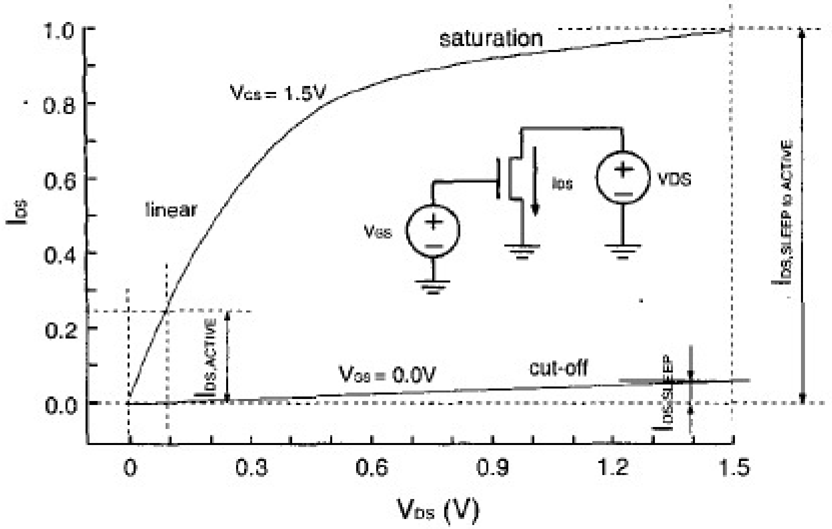

Figure 2.6: I-V characteristics [9]

In active mode, a sleep transistor in a power-gating structure of Figure 2.6 operates in its linear region, in which it may be modeled by a resistor *R*active. This generates a small voltage drop *V*VGND equal to *I*active × *R*active, where *I*active is the total current demand of the logic block operating in active mode. The voltage drop reduces the gate's drive capability from VDD to VDD-*V*VGND and increases the threshold voltage of NMOS pull-down devices due to body effect. Both effects degrade the speed of the circuit, and so, the sleep transistor should not be too small [20].

In standby mode, the sleep transistor operates in the cutoff region of Figure 2.6 and may be modeled by an open switch. During this mode, the leakage current is limited by the sleep transistor, which is reduced by a high threshold and a proportionally smaller width. By turning off the sleep transistor during the sleep period, all internal capacitive loads connected to the VGND node through NMOS pull-down devices are charged up to a steady state value near VDD.

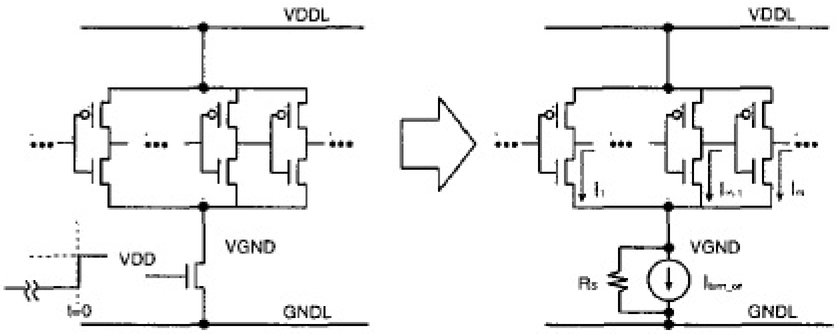

Figure 2.7: Sleep transistor operates as current source. [9]

If the sleep transistor is abruptly turned fully on, all the charge are trapped in the internal capacitive nodes, and the VGND node discharges rapidly through the switched NMOS pull-down paths of the logic blocks and the sleep transistor. Initially, as shown in Figure 2.7 for a time, the sleep transistor operates in its saturation region and may be modeled by a current source. The current that can flow through the sleep transistor in this situation is much larger than the active-mode current *I*active, and this current surge induces voltage fluctuations in the power distribution network

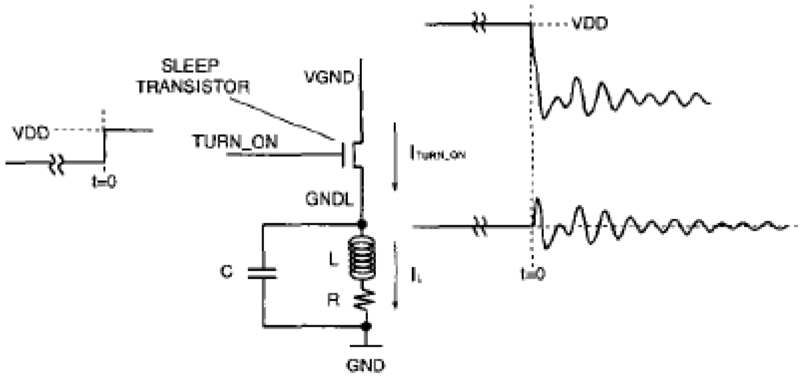

Figure 2.8: Switching noise within a on-chip ground rail. [9]

The amount of instantaneous current that can flow through the sleep transistor at this moment is much larger than the active mode current, ***Iactive.*** As shown in Figure 2.8, the current surge creates inductively induced voltage fluctuations in the power distribution network.

2.5 Factor Affecting the Ground Bounce

There are several factors which affect ground bounce, such as

- Power Supply Voltage
- Magnitude of Current Surge
- Rate of change of current through Sleep Transistor
- Voltage Swing of virtual ground during Wake-up
- The Output and Ground Inductance Value
- Number of Output Switching
- Output Pin Location
- Location and Type of Output Load on the Line
- The Device Technology

2.5.1Power Supply Voltage Effects

The value of VDD also affects the amplitude of the ground bounce. By reducing the VDD level, not only is the output voltage swing reduced, but also the amount of current that the output can deliver. Both of these tend to reduce ground bounce. The results of varying both VDD and load capacitance were taken on a standard test fixture. While the amplitude of the ground bounce changes linearly with voltage, it is not merely the ratio of the voltage levels.

Reducing the VDD by 40% reduces the ground bounce by almost 60%. Since the amplitude of the ground bounce decreases faster than the input threshold, there is a net gain in the noise margin [18].

2.5.2 Magnitude of Current Surge

Ground bounce tends to limit the available AC current in CMOS outputs by reducing the voltage across the output impedance, and therefore, reduces the current that will flow

2.5.3 Rate of change of current through Sleep Transistor

To quantify the magnitude of the inductive noise and its effect on the circuit performance by way of an example, assume that the effective inductance between the ground of the chip and the ground of the Printed-Wiring Board (PWB) plane is 10nH, and the rate of change of the switching current is 5 mA/nsec per I/O pin (Figure 2.9). Assuming that 16 drivers switch at the same time (to provide data for a 16-bit bus), the peak value of the ground bounce is about 0.8V, which is quite large in the context of today's operating voltage levels and can therefore cause harmful effects on the circuit, such as false switching in the logic gates, especially in dynamic logic gates, timing failure, and timing jitter in the on-chip clock generators.

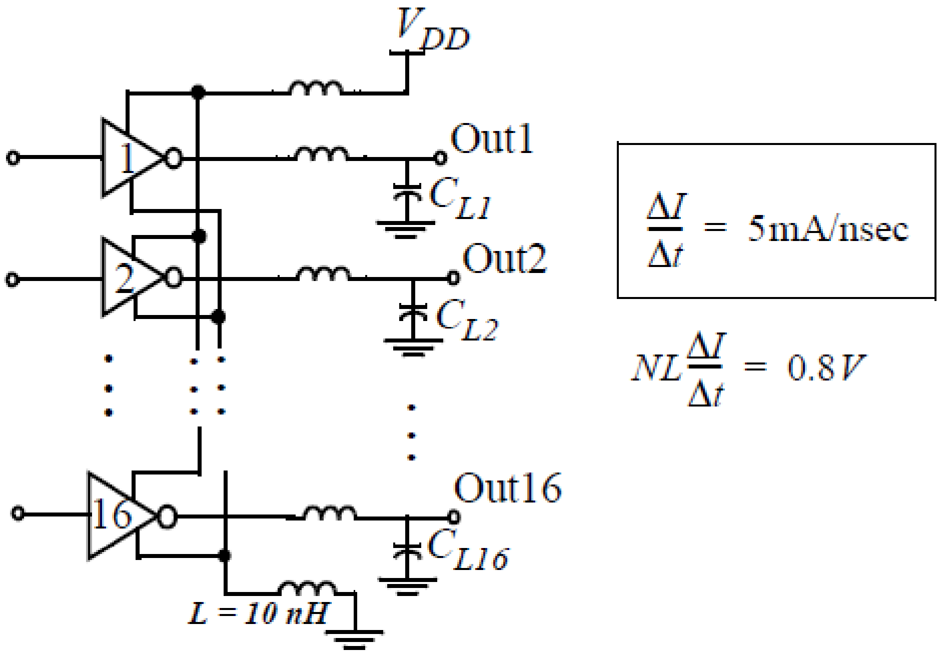

Figure 2.9: simplified circuit schematic of 16 output buffers switching simultaneously [3]

2.5.4 Voltage Swing of virtual ground during Wake-up

As the voltage swing at virtual ground increases, the peak if current surge also increase during wakeup so the peak of ground bounce also increases.

2.5.5 The Output and Ground Inductance Value

The inductance in the ground lead is not the only inductance in the package. All of the output pins have an associated inductance. The inductances in the outputs also contribute to ground bounce, especially any oscillatory effects. While just reducing the ground or VDD does not significantly reduce ground bounce, reducing the inductance in both the power leads and the outputs does reduce ground bounce.

$$V = L\frac{dI}{dt} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.1)$$

Reducing the ground lead inductance is not the solution to ground bounce problems. While a small reduction in ground bounce can be realized, additional problems, like increased crosstalk, may occur. A better solution is to reduce the inductance in all leads. Smaller packages, such as SOIC and LCC/PLCC packages, do reduce ground bounce over both standard and center-VDD/ground-pinned DIP packages.

2.5.6 Number of Outputs Switching

The number of outputs switching simultaneously affects the amplitude of ground bounce. For a simple model, treat the output impedances of each active output as resistors and inductors in parallel. For resistors of equal value in parallel, the formula for the net resistance is R/n, where R is the output impedance of each transistor, and n is the number of resistors. Therefore, as more outputs switch at the same time, the output resistance is reduced and more ground bounce will be generated.

Figure 2.10 illustrates the effect of increasing the number of outputs switching at the same time. We can see that as the number goes up, the amplitude and duration of the ground bounce pulse also increases. Therefore, devices that have fewer outputs will have less ground bounce [18].

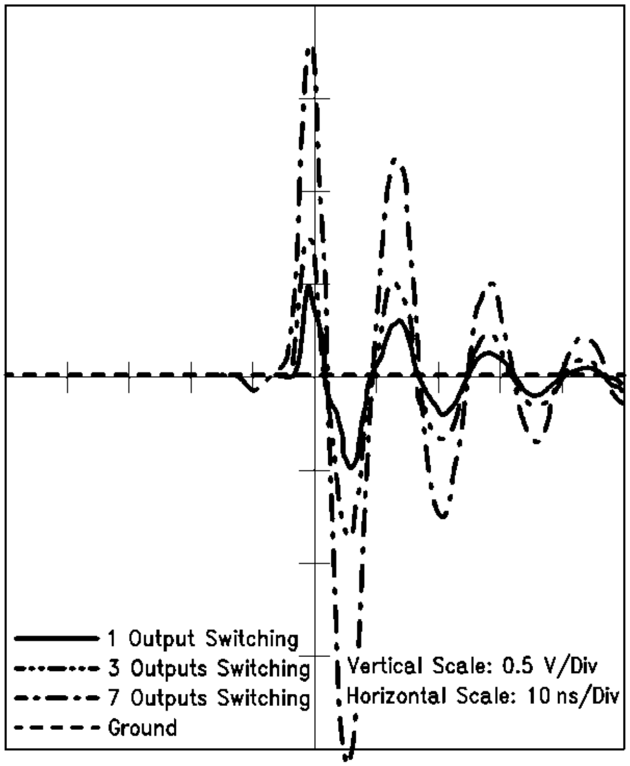

Figure 2.10: Number of Outputs Switching [18]

2.5.7 Output Pin Location

The location of the output pin with respect to the device ground also affects the magnitude of ground bounce. The effects of pin location are portrayed that shows the ground bounce on the worst-case pin, which is the one farthest away from ground and the ground bounce on the best case pin is the one closest to ground. By choosing outputs close to ground, the amount of ground bounce may be reduced by nearly half [18].

2.5.8 Location and Type of Output Load on the Line

The type and value of the output loading is one of the major variables that affect the amplitude of the ground bounce. The amplitude of the ground bounce increased with increased capacitive loading. However, the slope of the curve drops off as the capacitance increases. This is due to the amount of energy that is discharged from the capacitor during the time that the output transistor is turning on [18].

Each of these factors plays a critical role in the generation of ground bounce. Ground bounce tends to limit the available AC current in CMOS outputs by reducing the voltage across the output impedance, and therefore, reduces the current that will flow. When the ground lead inductance is reduced, a corresponding increase in the output edge rate of the device occurs. This is due to the fact that by reducing the inductance in the ground lead we have increased the available AC current. This greater $\Delta I/\Delta t$ tends to reduce any improvement that the reduced ground inductance may have generated.

2.6 Adverse effect by GBN

Because of the self-inductance of the off-chip bonding wires and the parasitic inductance inherent to the on-chip power rails, these current surges manifest as voltage fluctuations in the power rails. If the magnitude of any such voltage droop is greater than the noise margin of the circuit (which is especially low for deep sub-micron designs), it may erroneously latch a wrong value or switch at the wrong time. This inductive noise can therefore cause unexpected logic behavior and signal integrity problems [3].

2.6.1 Effect of ground bouncing

The problems associated with ground bounce occur because the induced voltage across the ground leads creates a voltage differential between the external system ground and the internal device ground. This voltage affects both inputs and outputs, although differently

If the magnitude of a voltage surge/droop due to ground bounce is greater than the noise margin of a circuit, the circuit may erroneously latch the wrong value or switch at the wrong time.

Until now, however, ground bounce originating from the power-mode transition of a power gating structure was not seriously considered, even though it affects the reliability of a system-on-a-chip (SOC) employing multiple power gating domains to control leakage power.

The problems created by ground bounce fall into three related categories, namely false switching, poor signal quality and propagation delay degradation. All of these problems are the result of the die ground moving relative to the external device ground.

2.6.1.1 False Switching

False switching may occur when the die ground or die V_{DD} reference voltage bounces is enough to cause the input toggle point of the die to shift enough to pass through a logic threshold.

2.6.1.2 Poor Signal Quality

The first effect that a designer will see from a component with high ground bounce is poor signal quality. In CMOS components, the output is tied directly to the Die GND through the pull down FET. If the die is bouncing and ringing, this noise will extend directly to the device output and into the signal path. The effect of the Ground Bounce will be enhanced if the transmission line is inductive and the inductive kick extends the peaks and valleys of the noise

2.6.1.3 Propagation Delay Degradation

Propagation delay degradation is a phenomenon familiar to most system designers. As more than one output on a single device is switched, the propagation delay, as measured to the input threshold level, will become longer. Since the rate of voltage change across the load capacitance is directly related to the current available, a decrease in current reduces the rate at which the output voltage changes, i.e., the edge rate slows down. This, in turn, slows down the propagation delay because more time is required for the output to go from one rail to the input threshold.

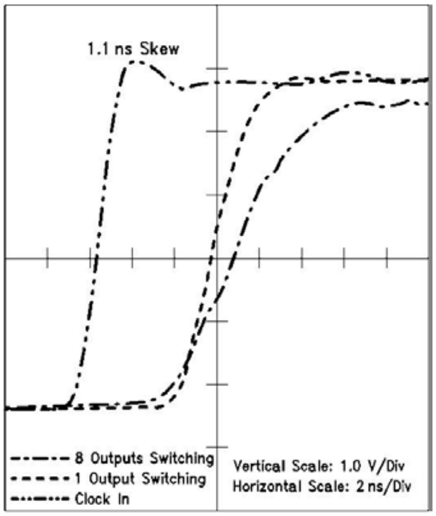

Figure 2.11: Propagation Delay vs. Number of Outputs Switching [18]

2.7 FULL ADDER

Any computational circuit is incomplete without the use of an adder. Addition is one of the primary operations in arithmetic circuits [21]. These adder cells commonly aimed to reduce power consumption and delay. These studies have also investigated different approaches realizing adders using CMOS technology.

Adders are heart of computational circuits and many complex arithmetic circuits are based on the addition [22]. The vast use of this operation in arithmetic functions attracts a lot of researcher’s attention to adder for mobile applications. In recent years, several variants of different logic styles have been proposed to implement 1-bit adder cells. These adder cells commonly aimed to reduce power consumption and increase speed.

The conventional CMOS 28 transistor adder [7], as shown in Figure 2.5, is considered as Base case throughout this paper. All comparisons are done with Base case. Transistor sizes are specified as a ratio of Width/Length (W/L). It is observed in the conventional adder circuit that the transistor ratio of PMOS to NMOS is 2 for an inverter.

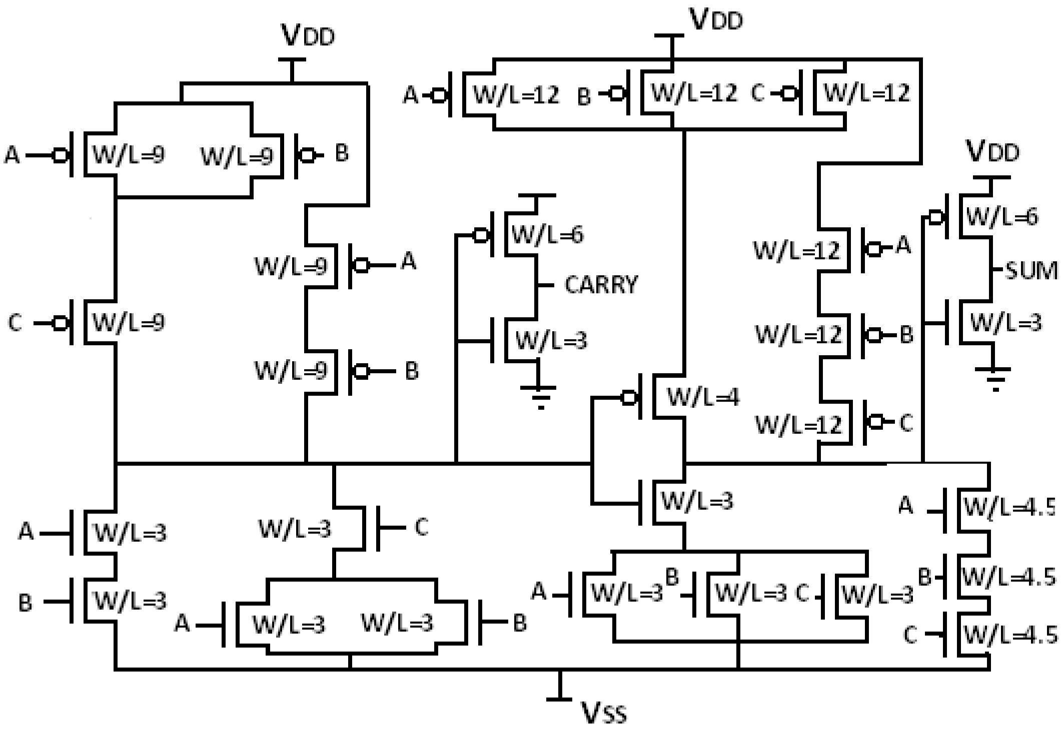

Figure 2.12: Conventional one bit CMOS full adder [7]

The CMOS structure combines PMOS pull up and NMOS pull down networks to produce considered outputs. Transistor sizes are specified as a ratio of Width/Length (W/L).

To see the efficiency of MTCMOS technique, a full adder is designed with conventional high threshold CMOS, low threshold CMOS and MTCMOS technique. The results are shown in the table 2.1 along with the simulation result.

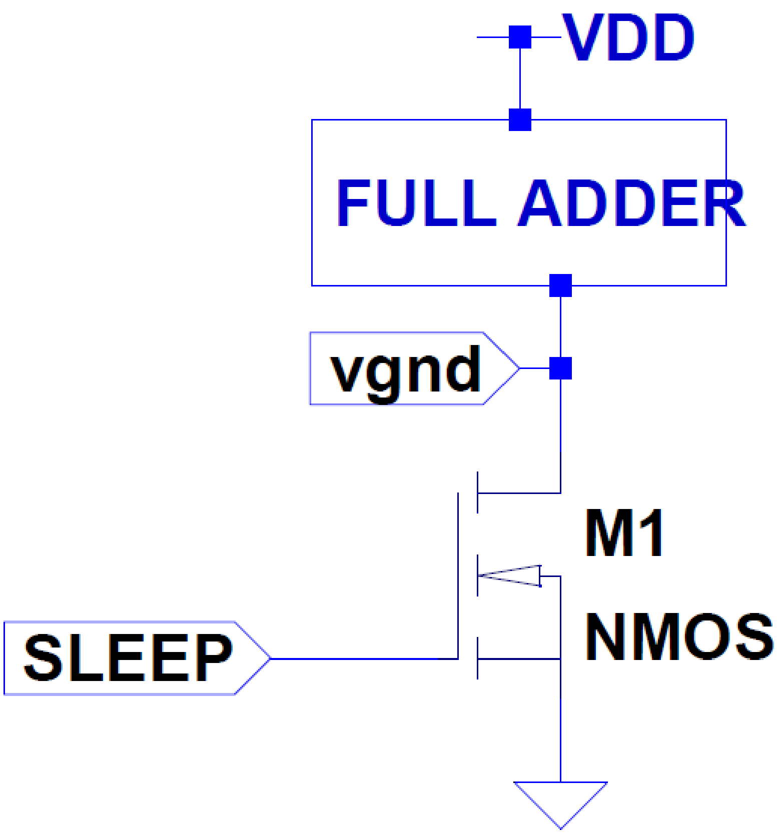

Figure 2.13: Full adder with gated ground MTCMOS

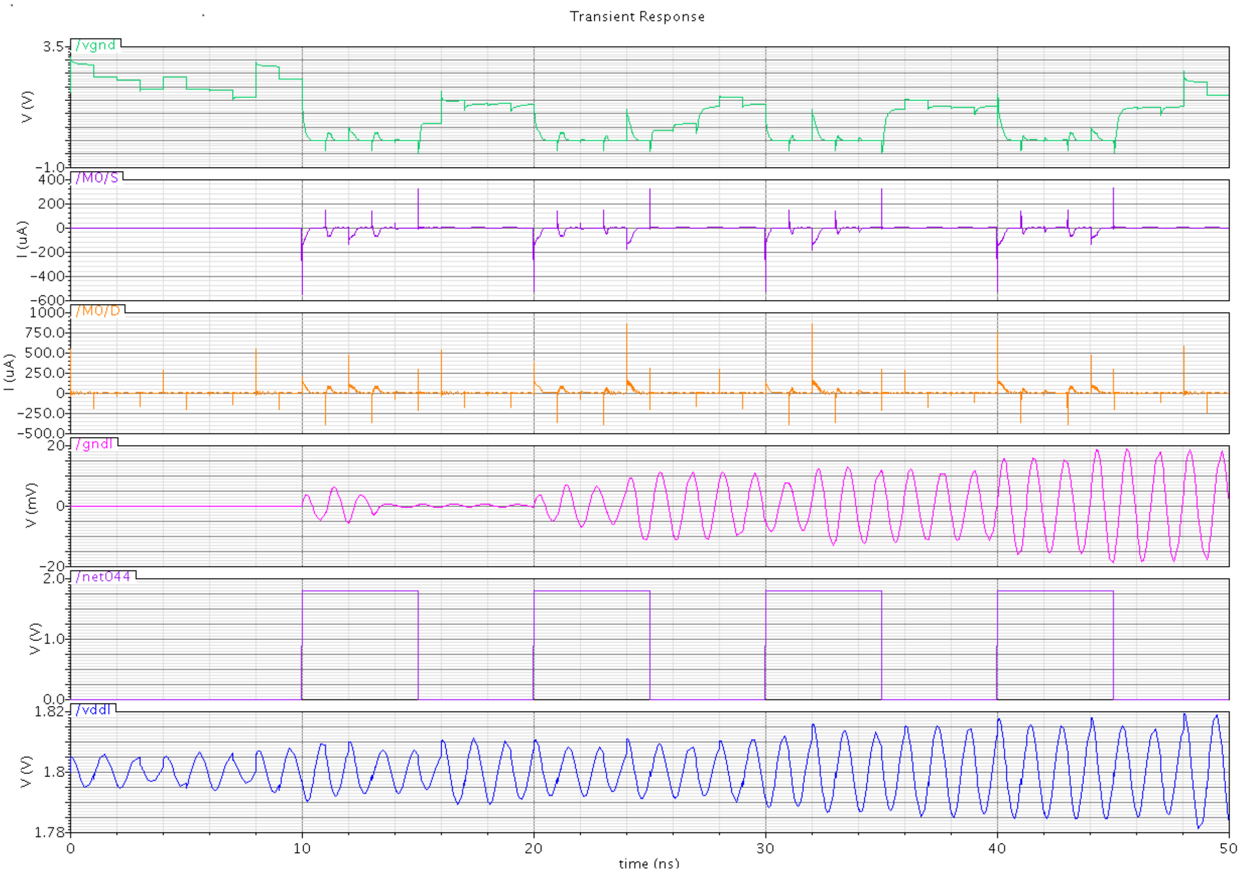

Figure 2.14: output of gated ground MTCMOS full adder

Table 2.1: Comparison of different parameters of one bit full adder.

Parameter	Conventional Full Adder	MTCMOS based Full Adder
Dynamic power	276.4 nW	272.8 nW
Switching power	218 nW	22pW
Delay	477 pS	485 ps

The present chapter dealt with MTCMOS Techniques in general and their efficacy has been demonstrated by taking the example of a one bit full adder. The next chapter is intended to address the problem of ground bounce specially occurring in high speed digital VLSI circuits.

CHAPTER

3

GROUND BOUNCING MINIMIZING TECHNIQUES

3.1 INTRODUCTION

In the previous chapter we have seen the adverse effects of the ground bouncing noise. As the technology is scaling down, the noise margins are also becoming very small. So suppressing the ground bouncing noise to the least possible amplitude is very much essential. The primary factors which affect the amplitude are very much essential. The primary factors which affect the amplitude of the ground bouncing noise are:

- Supply voltage
- Magnitude of current surge
- Rate of change of current through sleep device (di/dt)
- Voltage swing of virtual ground during wakeup
- Inductance value

The peak amplitude of the ground bouncing noise increases with increase in any of the above parameter [12]. Supply voltage and the inductance are fixed for a particular technology and package value noting much we can do at design level. So by manipulating the other three parameter current surge, dI/dt, and voltage swing values are able to minimize the ground bouncing. The two parameter dI/dt and current surge value, we are able to minimize the ground bouncing. The two parameter dI/dt and current surge value depend on the size of the sleep transistor. We can reduce them by decreasing the size of the sleep device but reducing the size of the affects the performance of the circuits. So the ground bouncing minimization techniques are focused on alternative method of reducing the current surge and dI/dt with size fixed and also the control of voltage sing. Wakeup delay is another important parameter which should be taken care of while applying these techniques. The best technique is that one which gives least ground bouncing noise with least wakeup delay. If the wakeup delay is more the circuit may not enter into complete active state by the time it is supposed to enter which may cause problems in the operation of the circuits. The following section describes different techniques used to control the ground bouncing by controlling the different parameter like current surge, dI/dt, voltage swing having its merits and demerits.

3.2 Controlling the Current Surge

Controlling the current surge is an effective way to minimize the ground bouncing as explained in the previous section. The methods explained in this section work on this principle. Following are the two novel power gating structures in which sleep transistor are turned on in a non uniform stepwise manner. Such power gating structure in which sleep transistor are turned on in a non uniform stepwise manner. Such power gating structures reduces the magnitude of voltage fluctuations in the power distribution network as well as the time required to stabilize them. Stepwise switching of the sleep transistor is implemented either by dynamically controlling the gate to source voltage Vgs of a sleep transistor or by turning on only a portion of the sleep transistor at one time.

3.2.1Dynamic Variation of Effective size

In this section, we propose novel power gating structures in which V_{GS} or the effective size of the sleep transistor increases dynamically in a non-uniform stepwise manner. Figure 3.1 shows a power gating structure in which the sleep transistor is implemented with a single transistor or a set of transistors. A sleep transistor implemented by a set of individual transistors wired in parallel is effectively a single transistor because the transistors share both VGND node and GNDL rail and are turned on simultaneously. During the mode transition of these conventional power gating structures, the large instantaneous current flow through the sleep transistor causes large voltage fluctuations in the on-chip power distribution network.

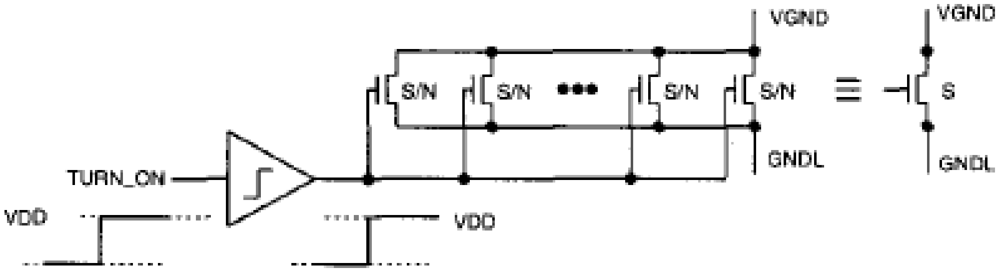

Figure 3.1: A sleep transistor or a set of sleep transistors used in a conventional power gating structure [9]

To solve this problem, a technique is proposed to minimize the instantaneous current flow through the sleep transistor. The first is by dynamically controlling VGS and hence VDS, as shown in figure 3.2

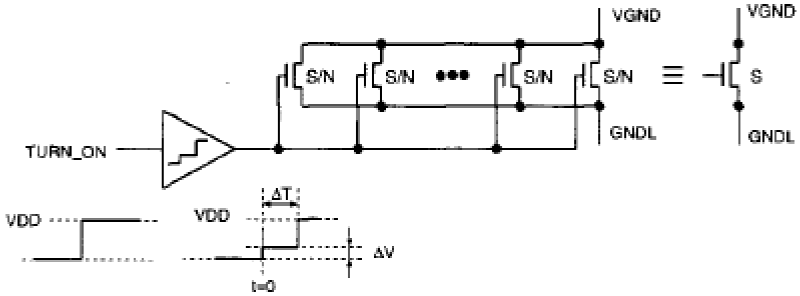

Figure 3.2: A sleep transistor or a set of sleep transistors whose V_{GS} increases in a non-uniform stepwise manner [9]

Stepwise switching of the sleep transistor is implemented by dynamically controlling the gate-to-source voltage, VGS of a sleep transistor. The stepwise switching consists of a relaxation stage followed by a complete turn-on stage. During the relaxation stage, the gate voltage of the sleep transistor is charged to only a small portion of the rail voltage. This stage allows the V_{DS} of the sleep transistor to reduce significantly with only a small peak current. During the complete turn-on stage, V_{GS} is charged up to the complete supply voltage V_{DD}. As shown in figure 4.2, during the relaxation stage, the sleep transistor is weakly turned on with $V_{GS} = V_x$ ($0 < V_x < V_{DD}$), until its V_{DS} is significantly reduced. During the complete turn-on stage, the sleep transistor is completely turned on with $V_{GS} = V_{DD}$. When the V_{DS} of the sleep transistor is small enough, the instantaneous current is less sensitive to variation in the *VGS* of the sleep transistor, thus allowing increasing *VGS* of the sleep transistor in a non-uniform stepwise manner without increasing instantaneous peak current.

3.3 Controlling the Voltage Swing

In the conventional power gating circuits, the virtual ground is charged to Vdd during sleep mode and discharge from V_{dd} to Vgnd during wakeup. Thus there is a voltage swing of approximately vdd while transitioning from sleep to active mode. This causes a high peak value of the ground bouncing noise. This amplitude of this noise is reduced by dividing the voltage sing in to two stage, i.e. from V_{DD} to intermediate voltage Vpark and then from Vpark to Vgnd. The following techniques use this principle for minimizing the noise.

3.3.1 Tri-mode technique [15]:

In this technique, between sleep and active mode an intermediate relaxation mode is created to gradually dump the charge stored on virtual ground line to real ground distribution network during the sleep to active mode transitions. The tri-mode power gating structure used to lower the ground bouncing noise is shown in figure (3.3). High -|Vth| sleep transistor are represented with a thick line in the channel region.

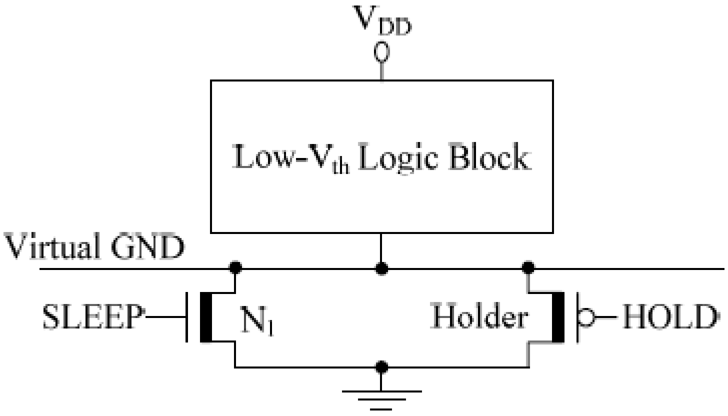

Figure 3.3: Tri-mode power gating structure [15]

A high -|Vth| PMOS data retention transistor (holder) is connected in parallel with the footer transistor (N1) to implement an additional PARK mode (utilized as an intermediate step between the sleep and the active modes) as illustrated in fig.3.3. The Holder is activated while N1 is maintained cut-off during PARK mode. The virtual power is charged to ~V_{DD}.

Both N1 and the Parker are turned off to reduce the subthreshold leakage currents of an idle circuit. The voltage of the virtual ground line is maintained at ~V_{DD} during the SLEEP mode. Prior to the activation of the circuit, the Parker is turned on while N1is maintained cutoff. The circuit transitions to the intermediate PARK mode. The virtual ground line is discharged to the threshold voltage of the Parker high-$|V_{t,p}|$ The first wave of activation noise is produced during the transition from SLEEP mode to PARK mode [15]. N1 is subsequently turned on to complete the activation process. The virtual ground line is discharged to ~V_{GND}. The second wave of activation noise is produced during the transition from PARK mode to ACTIVE mode. The activation noise is reduced due to the lower range of voltage swing on the virtual ground line with a two-step transition from SLEEP mode to ACTIVE mode through PARK mode

Alternatively, the virtual ground line is discharged to the threshold voltage of the Holder (|Vtp |). The ground bouncing noise is suppressed due to lower range of the voltage swing on the virtual ground line with a two step transition from the sleep mode to the active mode through the PARK mode. No complex circuitry is needed for the controlling the operation of the sleep transistor with this technique [15].

3.4 STACKING POWER GATING TECHNIQUE [5]

Stacking sleep transistors are used in stacking power gating technique to reduce the magnitude of peak current and voltage glitches in power rails i.e. ground bounce noise.

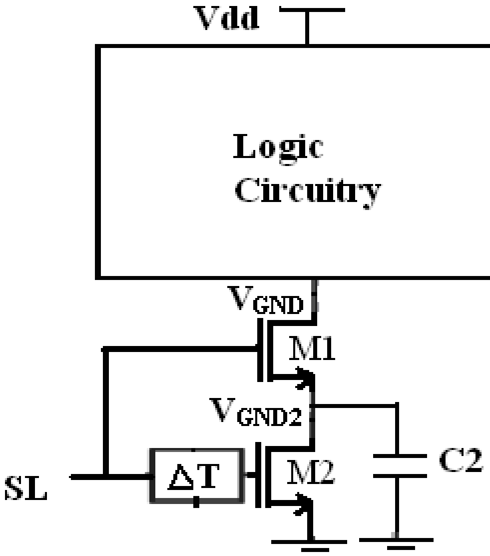

Figure 3.4: Stacking power gating technique [5]

In this technique, the leakage current is reduced by the stacking effect, turning both M1 and M2 sleep transistors OFF. This raises the intermediate node voltage VGND2 to positive values due to small drain current.

Positive potential at the intermediate node has four effects:

1) Gate to source voltage of M1 (Vgs1) becomes negative

2) Negative body-to–source potential (Vbs1) of M1 causes more body effect

3) Drain-to-source potential (Vds1) of M1 decreases, resulting in less drain induced barrier lowering

4) Drain -to -source potential (Vds2) of M2 is less compared to M1, because most of the voltage drops across the M1 in sleep mode. This significantly reduces the drain induced barrier lowering

The expression for the sub threshold leakage current is [13]

$$I_{sub} = Ae^{\frac{q}{nkT}\left(V_{gs} - \mathrm{V}_{\mathrm{th}\,0} + \gamma \mathrm{V}_{\mathrm{ds}} \right)}\left(1 - e^{-\frac{qV_{ds}}{kT}} \right) \tag{3.1}$$

Where A= $\mu_0 C_{ox}(W/L_{eff})$ (kT/q) $2e^{1.8}$, Vgs, Vds, and Vbs are the gate-to source, the drain-to-source, and the bulk-to-source voltages, respectively. The bulk is connected to ground. **Γ** and η are the body effect and DIBL coefficients respectively. Vth0 is the zero-bias threshold voltage. Cox is the gate-oxide capacitance. μ_0 is the zero-bias mobility, and is the sub threshold swing coefficient. From equation (1) it is observed that an increase in the body effect (negative V_{bs}), and reduction in V_{ds} (less DIBL) reduce the sub threshold current exponentially.

Further by using this technique ground bounce noise that occurs during mode transition can be reduced. The strategy to implement this technique is as follows:

1) Isolating the ground for small duration during mode transition.

2) Turning ON the M2 transistor in linear region instead of saturation region to decrease the current surge. During sleep to active mode transition, transistor M1 is turned ON and transistor M2 is turned ON after a small duration of time (ΔT). The logic circuit is isolated from the ground for a short duration as the transistor M2 is turned OFF. During this duration, the ground bounce noise can be greatly reduced by controlling the intermediate node voltage VGND2 and operating the transistor M2 in triode region.

The intermediate node (VGND2) voltage can be controlled by

1) Inserting proper amount of delay, that is less than the discharging time of the M1 transistor.

2) Proper selection of the capacitance C2.

3.5.2 ANALISIS OF STACKING POWER GATING TECHNIQUE

Stacking power gating has three modes of operations

1. Active mode
2. Standby mode
3. Sleep to active mode transition

3.5.2.1 Active mode

In active mode, the sleep signal of the transistor is held at logic ‘1’ and both the sleep transistors M1 and M2 remain ON. The equivalent circuit of sleep transistors M1 and M2 is shown in Figure 3.4. In this case both transistors offer very low resistance and virtual ground (VGND) node potential is pulled down to the ground potential, making the logic difference between the logic circuitry approximately equal to the supply voltage.

3.5.2.2 Standby mode

To reduce the leakage current in this mode, power supply rail and ground rail are isolated by turning OFF the sleep transistors. The sleep signal SL is held at logic ‘0’ to switch OFF the sleep transistors M1 and M2.

3.5.2.3 Sleep to active mode transition

In sleep to active mode transition, initially the transistor M1 is turned ON. After small duration of time (ΔT) transistor M2 is turned ON to reduce the ground bounce noise. The parameters ΔT and the capacitance C2 are decided based on following design objectives.

1. Minimum ground bounce noise.
2. Minimum wakeup latency.
3. Trade off between ground bounce noise and wakeup latency.

CHAPTER

4

SLOW RISING WAKEUP SIGNAL TECHNIQUE

4.1 Controlling dI/dt

Controlling the voltage swing or current surge can reduce the peak amplitude of ground bouncing up to some extent only. Particularly peak amplitude of ground bouncing corresponding to that particular voltage swing and current surge still persists in the ground rails. This magnitude of ground bouncing may still cause problems with scaled noise margins in the present day technologies especially for large circuits like 16 bit full adder which a vast amount of logic. Corresponding to this vast logic the sleep width is also very high and the inductance value is also very high for such a big packages. For such circuits the ground bouncing which is scaled down may still have that much amplitude which can cause trouble. The only way to minimize the ground bouncing to whatever the least magnitude we wanted to achieve is by controlling dI/dt. The rate of change of current is effectively controlled by controlling the slew of wake-up signal. By increasing the slew of the wake up signal we control the rate at which the sleep device is switched on which ultimately decides the rate of change of current that flow through it. By tuning the slew of wakeup we can tune the ground bouncing to the least possible value. But if the slew is too high the time taken for the sleep device to completely switched “on” will be very long that even if the voltage fluctuation are mostly vanished, the sleep transistor V_{GS} will not reach V_{DD}. The following method uses this principle to minimize the ground bouncing. The Wakeup delay problem discussed is also taken care by this method.

4.1.1 Slow Rising Wakeup Sleep Signal

The ground bouncing is controlled by controlling the rate of change of current. This is achieved in this technique by applying a wake signal having long rise time. The set up for the technique is as shown in figure 4.1

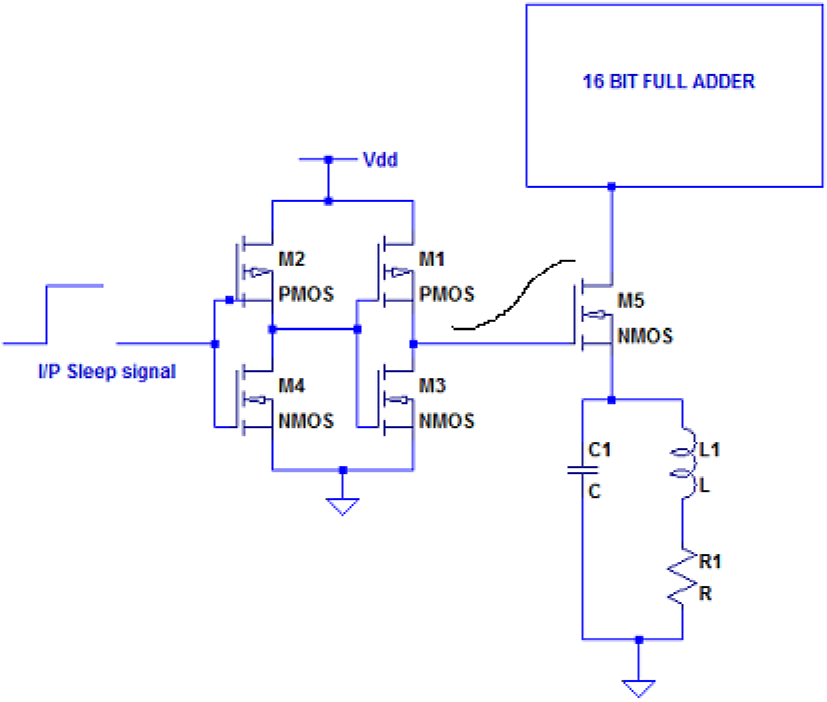

Figure 4.1: Slow rising wakeup signal technique

The wakeup signal is applied to an inverter chain whose output is applied to the sleep device. The sizes of the transistor in the buffer are selected such that the rise time is sufficiently long to achieve the specified level of ground bouncing noise. This rise time is normally high because of the high input capacitance of the sleep device because of its large size. If we increase the length of the pull up transistor of the second inverter or the first inverter that will decrease their current drive which lead to long time for the V_{GS} of sleep transistor to reach V_{DD}. The V_{GS} is starting to raise slowly meanwhile the virtual ground start discharging slowly. Since the V_{GS} is very low the current flowing through the sleep transistor is also very less. So there is no current surge because there is no sudden discharge. So the initial peak of ground bounce is very less. As the V_{GS} is raised further and since the rise time is very long, the rate of change of current that flow through sleep transistor is very low. So the ground bouncing is minimized.

4.2 Operation of the circuits

The noble power gating circuit could work in three different modes:

- Active mode, in which the sleep transistor is on and the circuit function normally.
- Sleep mode, in which the sleep transistor is shut-off and the leakage current of entire circuit is suppressed. The sleep transistor is switched ‘off’ to block leakage paths between the power and ground rails which could otherwise steadily draw power even during standby.
- Transition mode, in which the sleep transistor is turned on and the circuit goes from sleep to active [6]. Ground Bounce effect usually occurs in transition mode.

4.2.1 Active Mode: In this mode of operation, the wakeup signal is on (i.e. V_{DD}), then the NMOS transistor M3 and PMOS transistor M2 is on while PMOS transistor M1 and NMOS transistor M4 is on. The sleep signal as a result of the configuration is reached to V_{DD} level, so Sleep transistor is on and the whole circuits work properly.

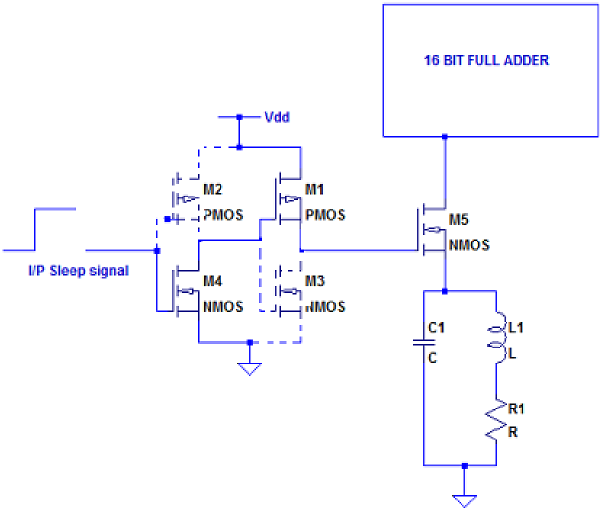

Figure 4.2: SRWS in Active Mode

The sleep transistor works in linear region and the current flow through this transistor is

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{w}{l}\right)(V_{GS} - V_{tn})V_{DS} \qquad V_{DS} \leq V_{DS,sat} \tag{4.1}$$

4.2.2 Sleep Mode: in this mode of operation, the wakeup is off, means no signal is provided by the circuits. The NMOS transistor M3 and PMOS transistor M2 is in cut-off while PMOS transistor M1 and NMOS transistor M4 is on.

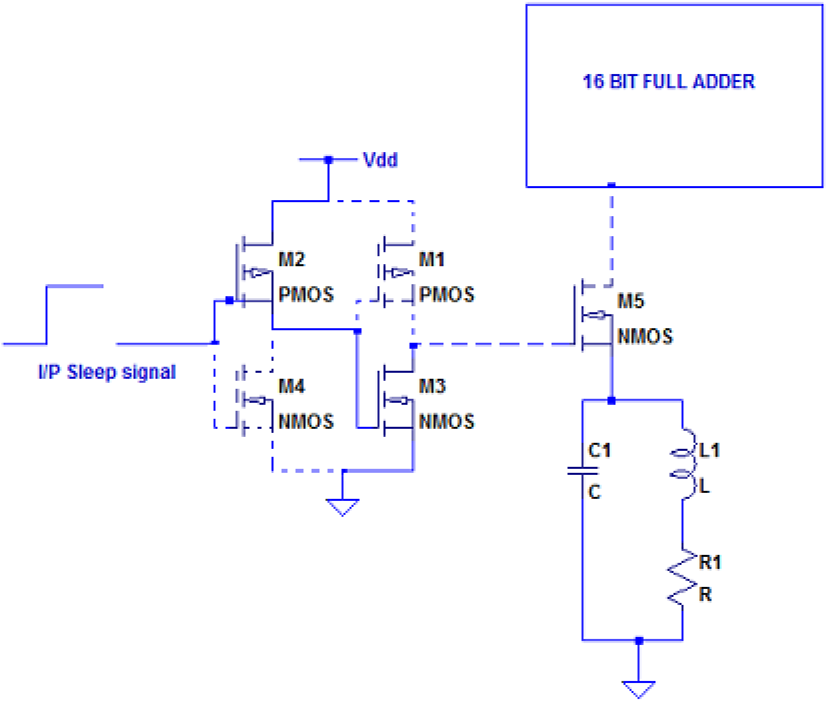

Figure 4.3: SRWS in Sleep Mode

This configuration also leads the sleep transistor M5 to work in cut-off mode. As sleep transistor is shutoff, which leads to the suppression of leakage current of whole circuits.

4.2.3 Transition Mode: In this mode of operation, the wakeup signal for sleep transistor is awaken from 0 to V_{dd}. The NMOS transistor is off so long as $Vgs < Vtn$. During this interval, the NMOS transistor operates in its weak-inversion region. When the transistor is operating in its weak inversion region the amount of drain current flowing through the drain path is very small. The expression for the sub threshold leakage current is [13].

$$I_{sub} = Ae^{\frac{q}{nkT}\left(V_{gs} - \mathrm{V}_{\mathrm{th}\,0} + \gamma \mathrm{V}_{\mathrm{ds}} \right)} \left(1 - e^{-\frac{qV_{ds}}{kT}} \right) \qquad (4.2)$$

As V_{GS} exceeds the threshold voltage V_{th}, the NMOS transistor first enters its saturation region.The transistor stays in saturation region during the entire low-to-high input transition because the off-chip driver drives large capacitive loads, and as a result, the driver output slowly decreases from logic high to a logic low. As the output voltage decreases, so does the drain-source voltage of the NMOS transistor. Eventually at $t = t_s$ ($t_s > tr$) the NMOS transistor makes a transition from saturation region to linear region. The NMOS transistor will stay in the linear region for $t > t_s$ until the next edge transition. The equation of current operating in different region is [24]

$$I_D = \begin{cases} W\vartheta_{sat}\, C_{ox} \left(V_{GS} - V_{tn} - V_{DS,sat} \right) & V_{DS} \geq V_{DS,sat} \\ \mu_n C_{ox} \left(\frac{W}{L} \right) \frac{1}{1 + \frac{V_{DS}}{LE_{sat}}} \left(V_{GS} - V_{tn} - \frac{V_{DS}}{2} \right) V_{DS} & V_{DS} \leq V_{DS,sat} \end{cases} \qquad (4.3)$$

Where $V_{DS,sat} = \frac{LE_{sat}\,(V_{GS} - V_{tn})}{LE_{sat} + V_{GS} - V_{tn}}$

From the aforementioned discussion, the NMOS transistor will enter the linear region when the input voltage is V_{DD} due to the presence of large off-chip capacitive loads. The overdrive voltage is thus constant at $V_{DD} - V_{tn}$. As a result, the nonlinear relationship between the saturated drift velocity, $\vartheta_{d,sat}$ and the drain-source saturation voltage, $V_{DS,sat}$, is evaluated at $V_{GS} = V_{DD}$. This leads to the following simplified transistor equation that holds true for the output drivers:

$$I_D = \begin{cases} \beta_n (V_{GS} - V_{tn}) & V_{DS} \geq V_{DS,sat} \\ \frac{1}{2} \mu_n C_{ox} \left(\frac{w}{l} \right) (V_{GS} - V_{tn}) V_{DS} & V_{DS} \leq V_{DS,sat} \end{cases} \qquad (4.4)$$

Where $\beta_n = \frac{0.5\mu_n C_{ox}\ (W/L)}{\frac{1}{V_{DD} - V_{tn}} + \frac{\gamma}{LE_{sat}}}$

And $V_{DS,sat} = \frac{LE_{sat}\ (V_{GS} - V_{tn})}{LE_{sat} + \gamma (V_{DD} - V_{tn})}$

A similar current-voltage relationship can be derived for the PMOS transistor also. This current is flowing through the NMOS and PMOS transistor in the extra circuit used for wakeup the sleep transistor. Now when the signal having long rise time is given to the gate of sleep transistor, it starts works in different mode as discussed earlier.

4.3 Calculative Model of GBN in Power gating circuits

Most of the charge stored on the capacitive load of output is discharged through sleep transistor during the long rise time of wakeup signal given to the sleep transistor. So peak of current surge is minimized which results in the reduction of amount of ground bounce peak on the transition from sleep to active mode.

The chip-package interface parasitics for ground, supply, and signal lines are modeled by series R,L,C circuits whose values are taken from DIP-40 package value.

Once the sleep signal turns off the sleep transistor (NMOS device), the power gating circuit goes into the sleep mode, and the internal nodes whose initial states are 0 begin to be charged by power supply until their voltage approach VDD. All the capacitances of output nodes can be modeled as a total capacitance Cint shown in Figure 4.4, which can be written as

$$C_{INT} = \sum_{i} C_{i\_0} \tag{4.5}$$

where C_{i_0} is the i_{th} internal node whose initial state is 0. Cp, Lp and Rp are the parasitic capacitance, inductance, and resistance of the package parasitic parameters respectively as shown in figure 4.4. The ultimate voltage of the charged nodes can be denoted as V_{charge}.

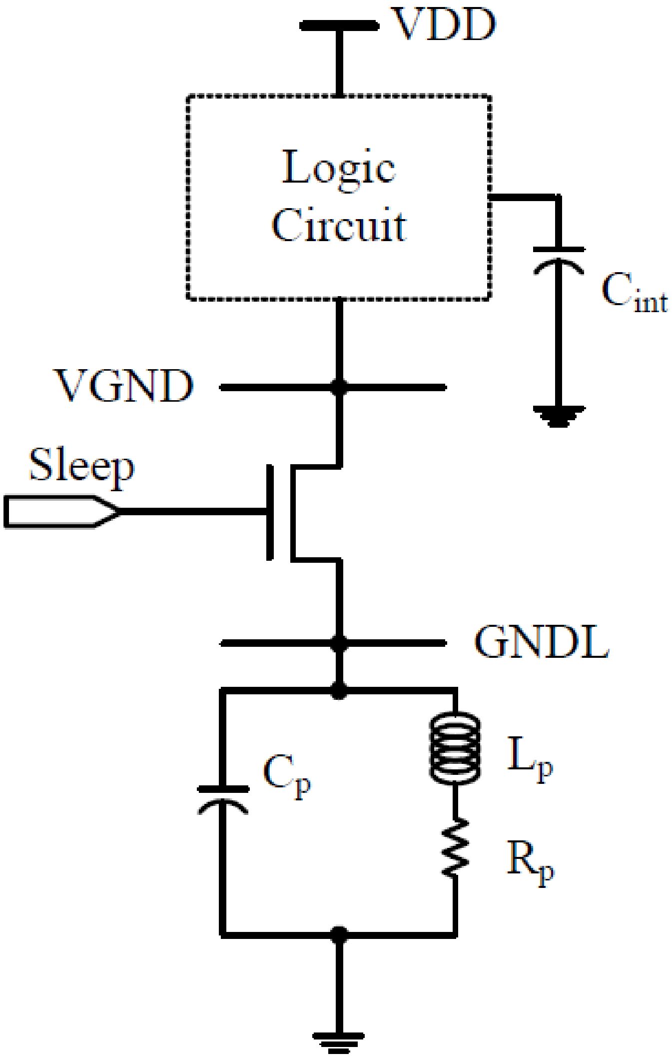

Figure 4.4: The capacitance model of internal nodes in the shut-off power gating circuit [8]

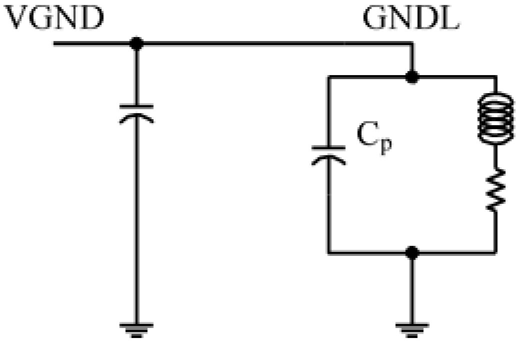

Figure 4.5: Circuit model after the sleep transistor turns on

Figure 4.5 shows the circuit model after the circuit is turned on. The sleep transistor is working in the linear region whose resistance can be negligible because of its large size. The charge accumulated in Cint will be rearranged between Cint and parasitic capacitance Cp, which can be expressed by

$$(C_{INT} + C_P)U_0 = C_{int} V_{charge} \tag{4.6}$$

where U0 is the voltage of V_{GNDL} after charge rearrangement. The entire model of the circuit after turning on could be depicted as the linear system shown in Figure 4.6, in which Ctotal is the total capacitance, and can be expressed by

$$C_{total} = C_{int} + C_p \tag{4.7}$$

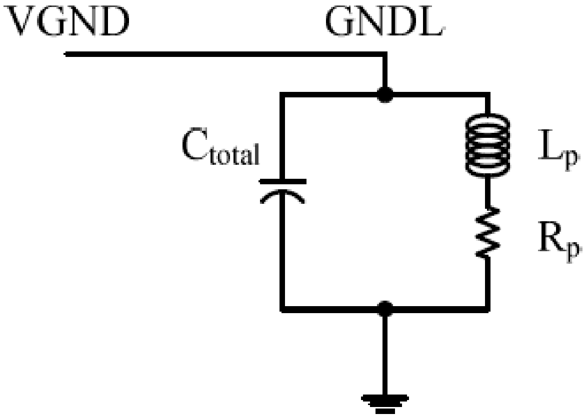

Figure 4.6: Linear circuit model after turning on the circuit

Based on the linear circuit in Figure 4.6, the s-domain equivalent circuit is shown in Figure 4.7, where U0/s is the initial voltage on the capacitance, 1/sCtotal, sLp and Rp are the s-domain equivalent capacitance, inductance and resistance respectively, and UGNDL(s) is the ground line voltage expressed in the s domain.

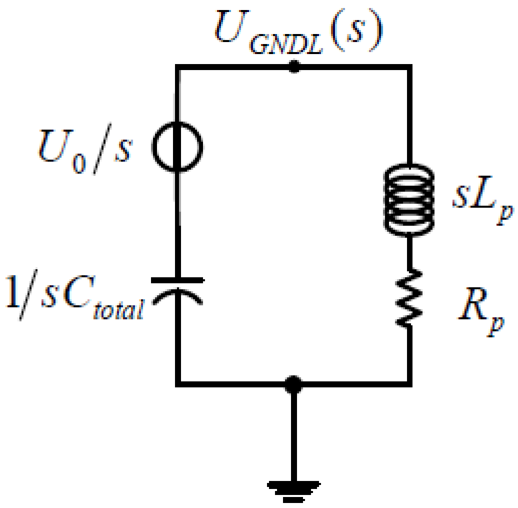

Figure 4.7: S-domain equivalent circuit

According to KVL, the voltage on the ground line can be expressed by

$$U(s) = \frac{U_0(\, R_P + \, sL_P)C_{total}}{s^2LC_{total} \, + \, sR_PC_{total} \, + \, 1} \tag{4.8}$$

Then the s-domain equation of the voltage in EQ(4) can be solved by applying Laplace inverse transform to obtain the time domain equation, which can be expressed by

$$\mathrm{U(t)} = \mathrm{U_0} \exp\left(-\frac{\mathrm{R_P}}{2\mathrm{L_P}}\mathrm{t}\right)\cos\left(\frac{4L_PC_{total} \, - \, R_P^2D_{total}^2}{4L_P^2C_{total}^2}\right)^{1/2} \tag{4.9}$$

According to Equation (4.9), the voltage fluctuation turns out to be a damped oscillation which has maximum amplitude U_0. The maximum amplitude of the voltage fluctuation on the ground line can be written as

$$\mathrm{Max}\ \{\mathrm{U(t)}\} = \mathrm{U_0} \tag{4.10}$$

CHAPTER

5

SIMULATION RESULT AND DISCUSSION

5.1 Circuit Analysis

We carried out both DC and transient analysis for 1 bit ripple carry adder. We calculate maximum peak of the ground bounce noise, wake up delay, leakage power consumption, maximum peak of current surge and area overhead for all technique discussed in chapter 4. We used the **“Cadence Design Environment”** for the design and simulation of all the circuits. Cadence is an Electronic Design Automation (EDA) that allows integrating in a single framework different application and tool (both proprietary and from other vendor), allowing to support all the stage of IC design and verification from a single environment. We used Analog IC Design Flow of Cadence to design and simulate all the circuits.

5.1.1 Tool used

The tool which is used for Design and Simulation of Circuits are briefly described here:

- The schematic of various circuits for simulation were generated using the tool known as “Virtuoso Schematic Composer” in the Cadence design Environment was used.
- To make test benches a symbol view of the circuits schematic must be created. For symbol creation and editing, the “Schematic Composer” was used.
- The circuit simulator in cadence is “Spectre” . The communication with Spectre was performed via “Analog Environment Design” tool. In this tool all setting for successful simulation were made (like assignment of value to design variables, simulation type setup, and selection of signal to be observed). The analog Environment tool generates an ocean script which starts Spectre.

- Two other tools are very necessary for the circuit analysis: “Waveform Viewer” and “Calculator”. The Waveform Viewer was used for displaying selected signal and Calculator was used for various functions like derivation and integration of waveform, FFT etc.

5.1.2 Analysis Performed

We have done two type of analysis for circuit under test i.e. DC Analysis and Transient Analysis:

- **DC Analysis:** The DC Simulation was performed to calculate the steady state condition of the circuits. The DC steady state can be calculated for a sweep over temperature, component parameter and design variable. Using this simulation we have check whether the operating point is met or not.
- **Transient Analysis:** this is time domain simulation. This is suitable to simulate the transient behavior of the circuit. The parameter like standby mode power consumption, energy overheads, maximum peak of ground bounce noise at virtual ground, maximum peak of current surge and wakeup delay were evaluated in this analysis. Special functions of Calculator Tool were used to evaluate the parameter.

5.2 description of Circuits Used

To find out the efficiency of different technique and to minimize the ground bouncing, we carried out simulation on 16 bit ripple carry adder, in which we have taken a conventional full adder as base design.

To show the compatibility of these technique to different environment and different level of logic we have chosen logic 1 bit Ripple Carry Adder in “180 nm” CMOS technology. We have applied these following wakeup techniques for MTCMOS 16 bit ripple Carry Full Adder.

- Conventional one step wakeup technique
- Tri mode technique
- Stacking power gating technique
- Dynamic size variation technique
- Slow rising wakeup signal technique

5.2.1 16 bit ripple carry adder

The block diagram of the 16 bit ripple carry adder is shown in figure 5.1

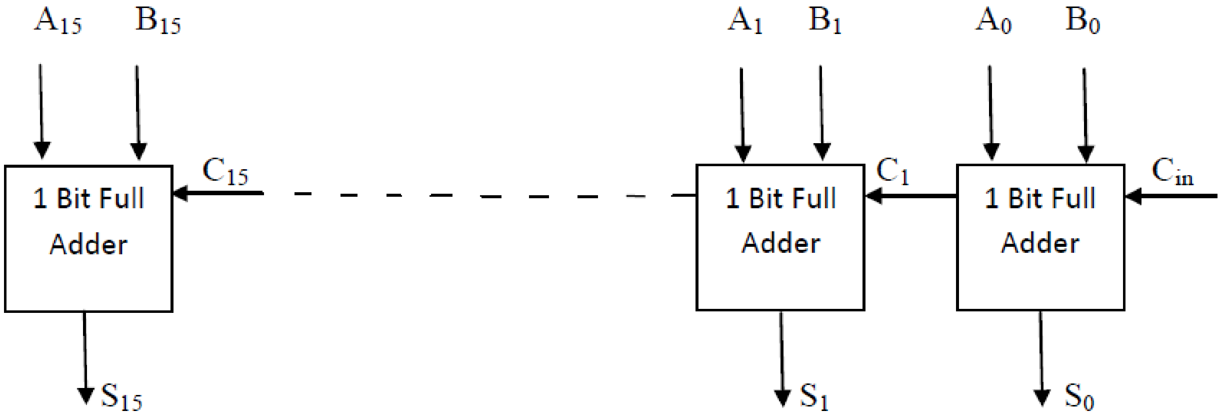

Figure 5.1 16 bit Ripple Carry Full Adder

The circuit use 16 bit Full Adder circuits to add 1 bit inputs. The input string A0 – A15 AND B0 –B15 are added to give 16 bit sum S0-S15 and a carry C_{out} . Carry if each full adder is forwarded to the next full adder and the carry for the first full adder C0 is specially given. This entire circuit is designed with low V_{th} transistor for speed improvement and a sleep device of high V_{th} is used to reduce the leakage as discussed in MTCMOS Technique.

Simulation Setup:

The simulations are carried out in “Cadence Design Environment” using “Spectre” Simulator in “180nm” CMOS Technology. The Ripple Carry Adder is designed with Low Threshold Voltage NMOS and PMOS FETs of 180nm Technology. This is used as low Vth circuit block which is connected in series with high Vth sleep transistor to minimize the leakage in sleep mode as shown in fig 5.2. The parasitic inductance, capacitance and resistance are taken from the dual in line package (DIP-40) package model.

The simulation parameters are:

- NMOS High-V_t Voltage V_{tnhigh} = 0.5V
- NMOS Low-V_t Voltage V_{tnlow} = 0.25V
- PMOS High-V_t Voltage V_{tnhigh} = -0.5V
- PMOS Low-V_t Voltage V_{tnlow} = -0.25V
- Supply voltage V_{DD} = 1.8V
- Sleep device width = 10 µm

5.2.2 DIP-40 package for GBN Model

The ground bounce model used in our simulation is shown in figure 5.2

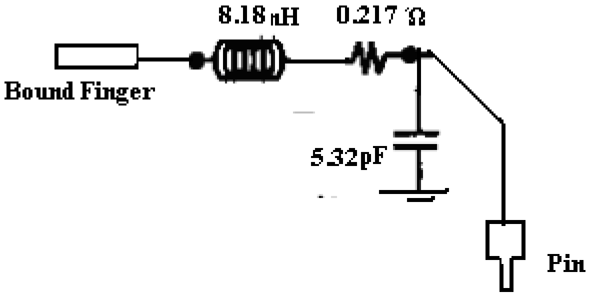

Figure 5.2: DIP -40 package pin ground bounce noise model [18]

- Inductance L = 8.18 nH
- Resistance R = 0.217 Ω
- Capacitance C = 5.32 pF

5.3 Simulation Result

In this section the ground bouncing waveform for 16 bit ripple carry adder are shown for each of the technique used to minimize the ground bouncing.

5.3.1 Conventional one step wakeup MTCMOS Technique

In the schematic shown in figure 5.3, the sleep transistor size is taken as 10 µm. The capacitance, resistance and inductance value are taken from DIP-40 package for pin. The 16 bit ripple carry full adder used in the circuit made from conventional 28 transistors based CMOS one bit full adder.

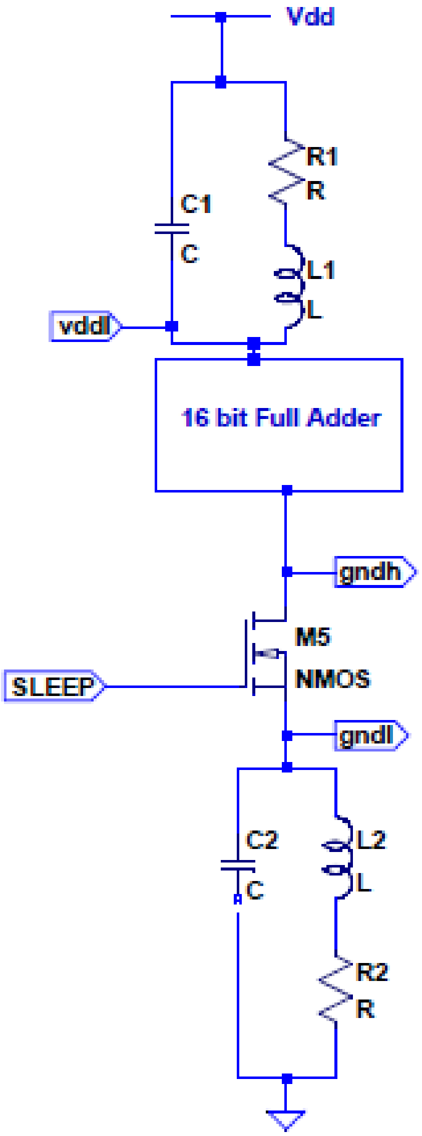

Figure 5.3: Schematic of MTCMOS circuits

The sleep device is switched on instantaneously by applying a step wakeup signal with rise time of 1psec. Due to a high current surge large amount of ground bouncing noise will be take place. Figure 5.3 shows the schematic diagram used for the simulation of 16 bit full adder with one step MTCMOS technology.

5.3.1.1 Simulation result for one step wakeup conventional MTCMOS technique

Figure 5.4 is the simulation result of the schematic from figure 5.3. The result reveals that the maximum peak of the ground bounce noise induced is nearly 356.39 mV and the maximum peak of current surge is 13.69mA

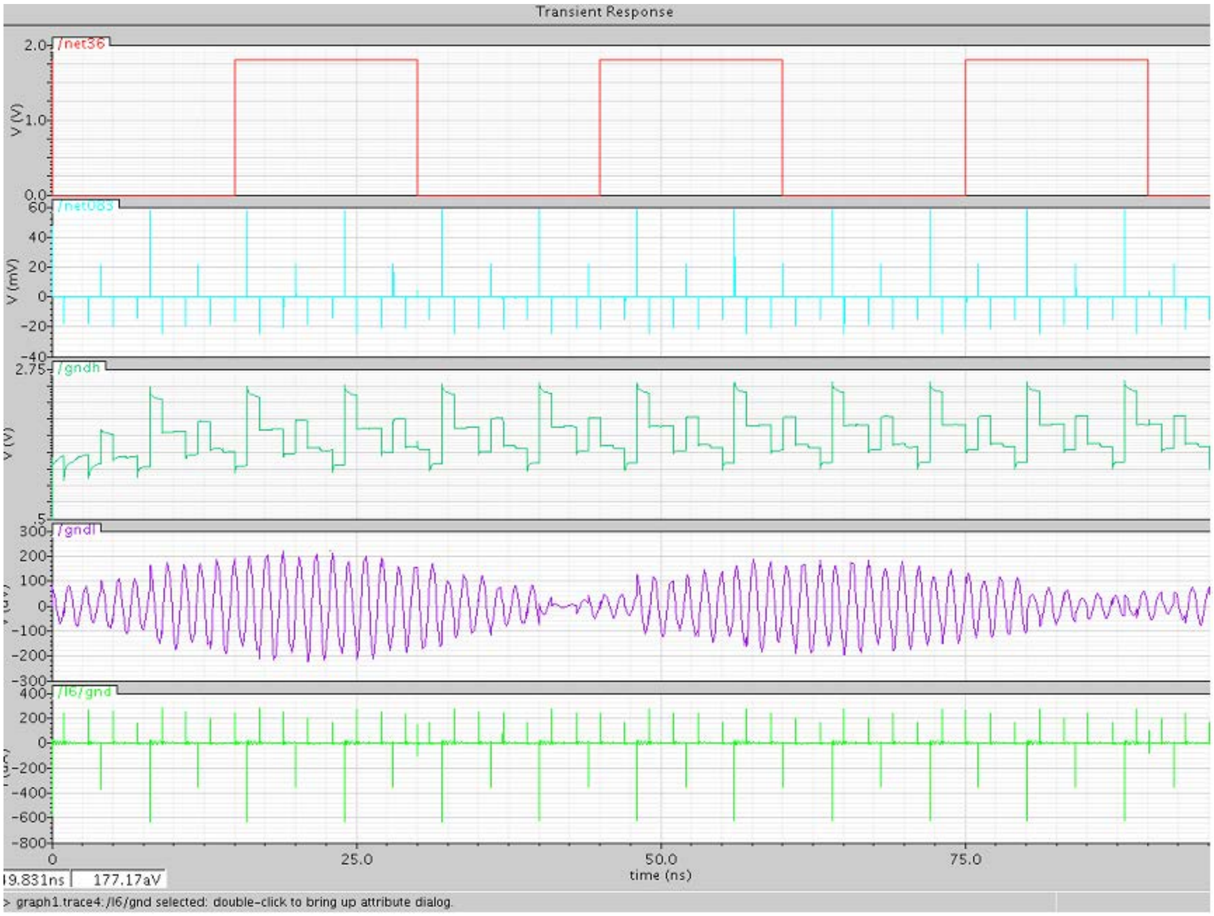

Figure 5.4: Conventional MTCMOS technique simulation result

5.3.2 Tri-Mode Technique

In this technique, between sleep and active mode an intermediate relaxation mode is created to gradually dump the charge stored on virtual ground line to real ground distribution network during the sleep to active mode transitions.

A high -|Vth| PMOS data retention transistor (holder) is connected in parallel with the footer transistor (N1) to implement an additional PARK mode (utilized as an intermediate step between the sleep and the active modes) as illustrated in figure 5.5. The Holder is activated while N1 is maintained cut-off during PARK mode.

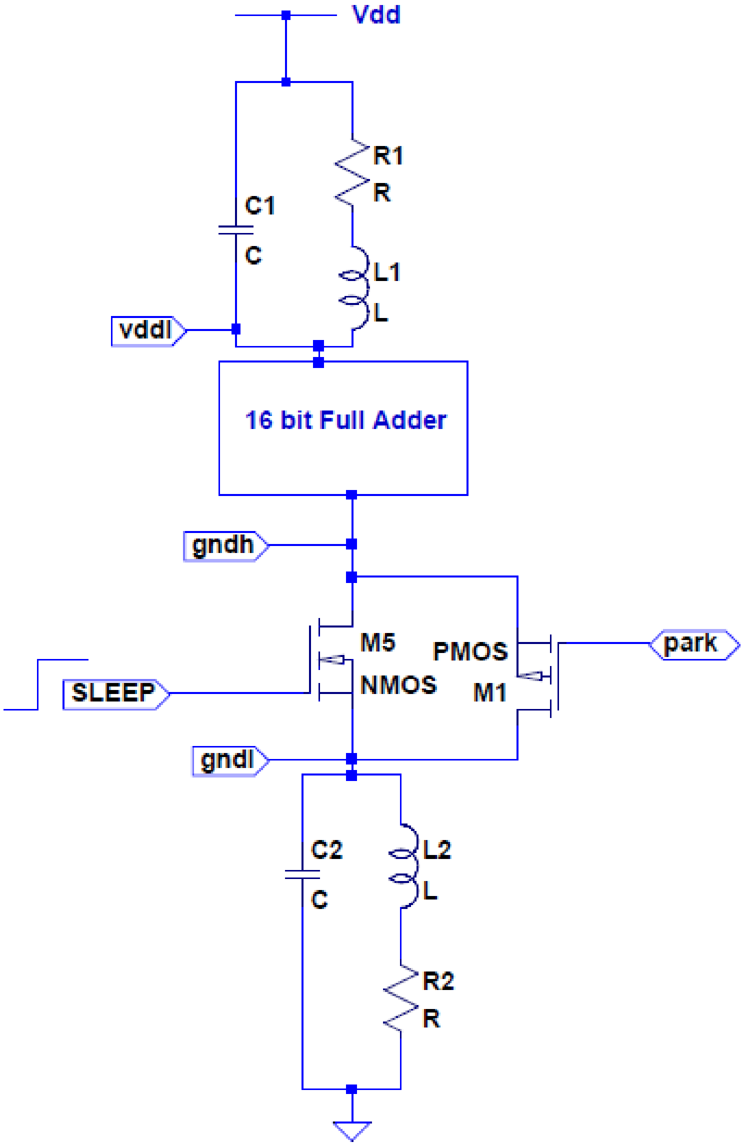

Figure 5.5 Schematic of Tri-mode Technique

5.3.2.1 Simulation result for Tri-Mode technique

Figure 5.6 is the simulation result of the schematic from figure 5.5. The result reveals that the maximum peak of the ground bounce noise induced is nearly 79.13 mV and the maximum peak of current surge is 11.86 mA.

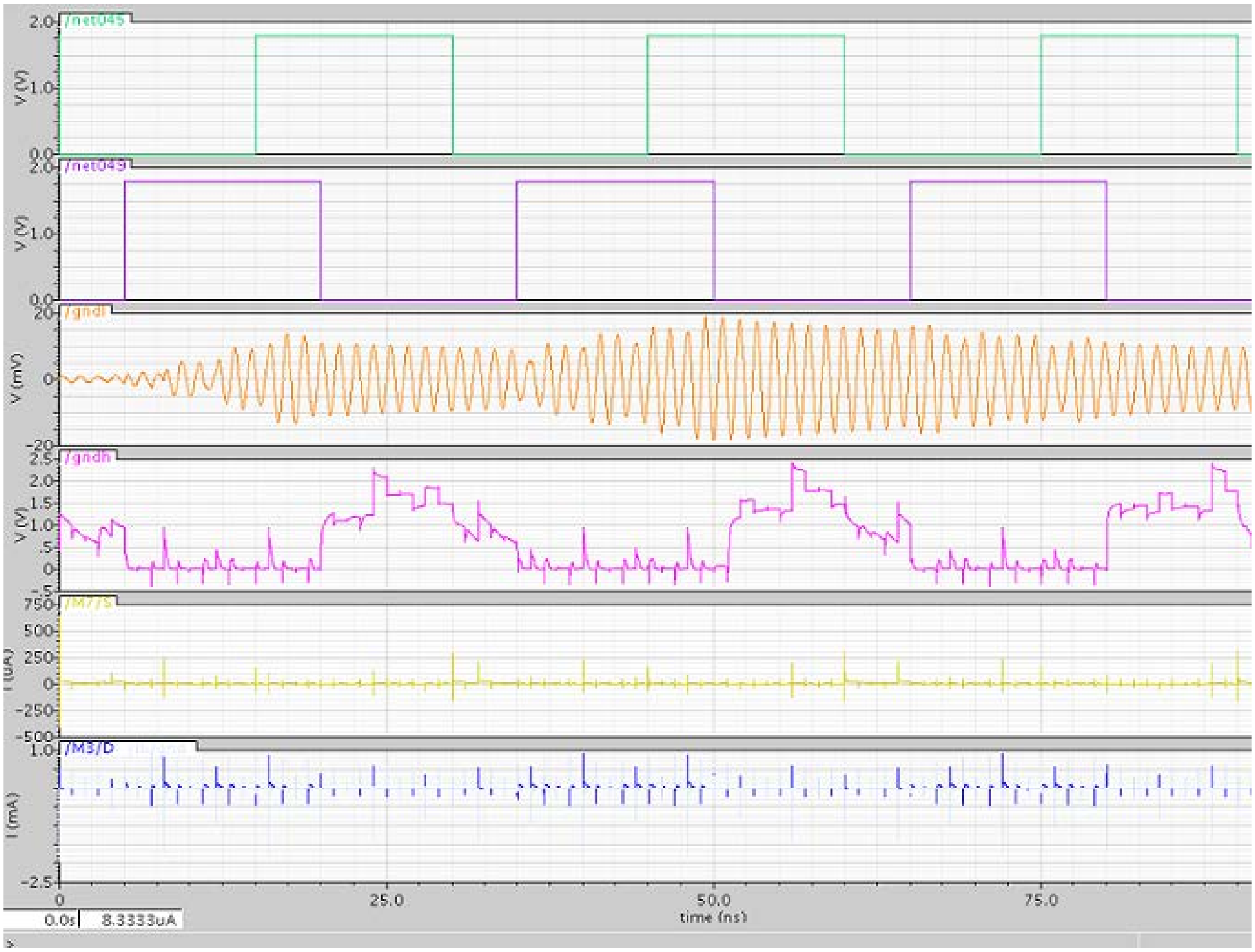

Figure 5.6: Tri-mode Technique simulation result

5.3.2.2 Layout of the circuit used for tri-mode technique

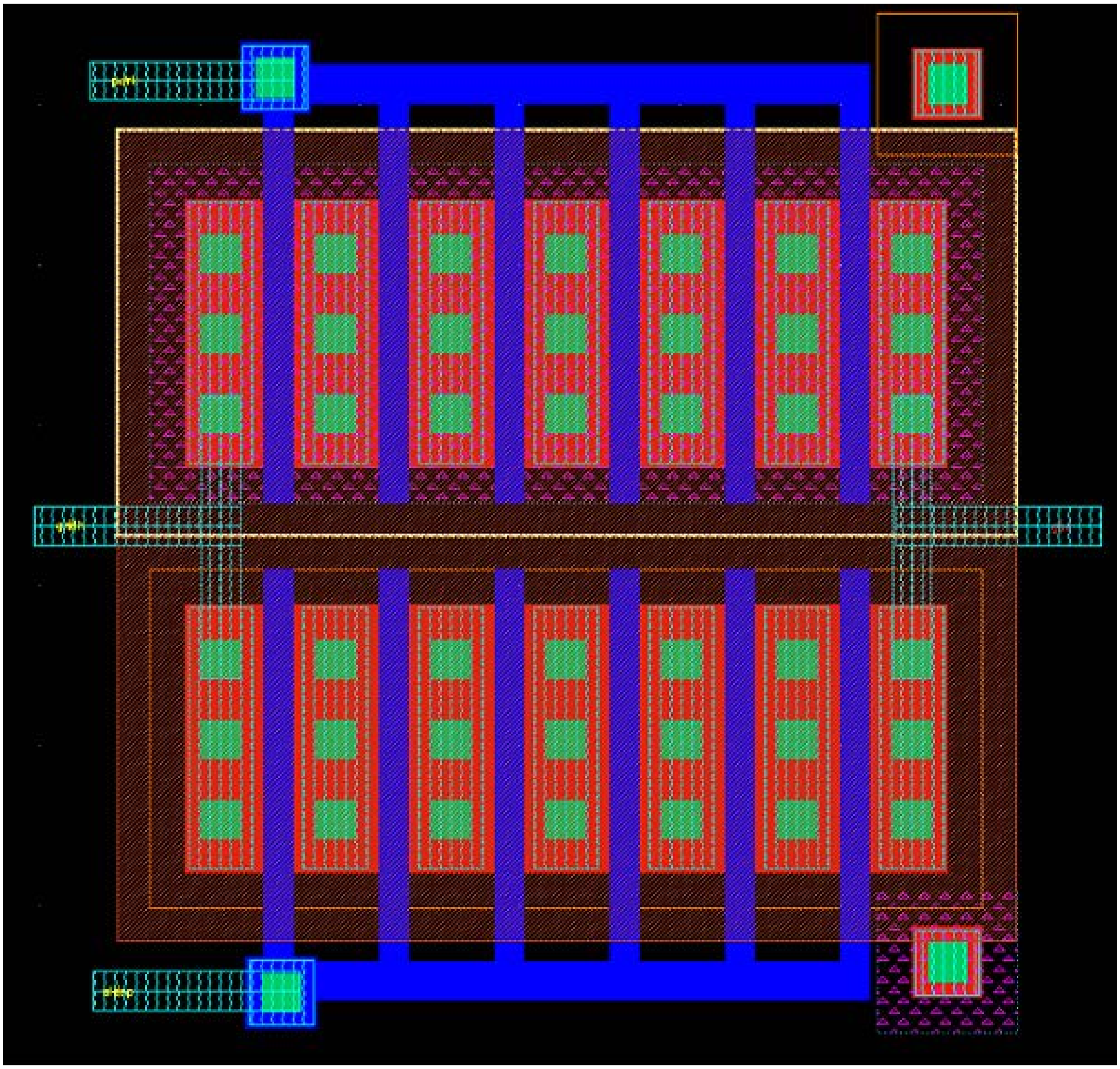

Figure 5.7: Layout of the additional circuit used for tri-mode technique

Figure 5.7 is the Layout of the circuit used for tri-mode technique. It is the layout of the additional circuitry used in the Tri-Mode technique to lower down the ground bounce noise as well as voltage swing on virtual ground node.

5.3.3 Stacking Power Gating Technique

Stacking sleep transistors are used in stacking power gating technique shown in figure 5.8 is to reduce the magnitude of peak current and voltage glitches in power rails i.e. ground bounce noise. The strategy to implement this technique is as follows:

1) Isolating the ground for small duration during mode transition.

2) Turning ON the M2 transistor in linear region instead of saturation region to decrease the current surge. During sleep to active mode transition, transistor M1 is turned ON and transistor M2 is turned ON after a small duration of time (ΔT). The logic circuit is isolated from the ground for a short duration as the transistor M2 is turned OFF. During this duration, the ground bounce noise can be greatly reduced.

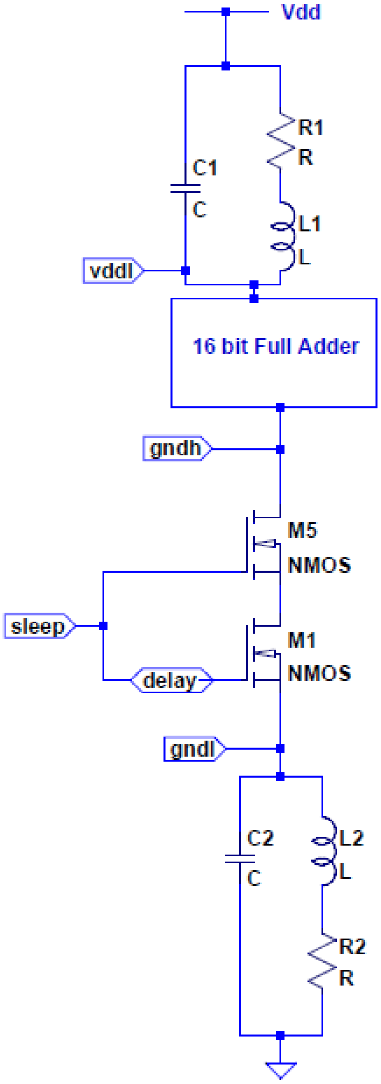

Figure 5.8: Schematic of Stacking power gating technique

5.3.3.1 Simulation result for Stacking power gating technique

Figure 5.9 is the simulation result of the schematic from figure 5.8. The result reveals that the maximum peak of the ground bounce noise induced is nearly 92.66 mV and the maximum peak of current surge is 0.932 mA.

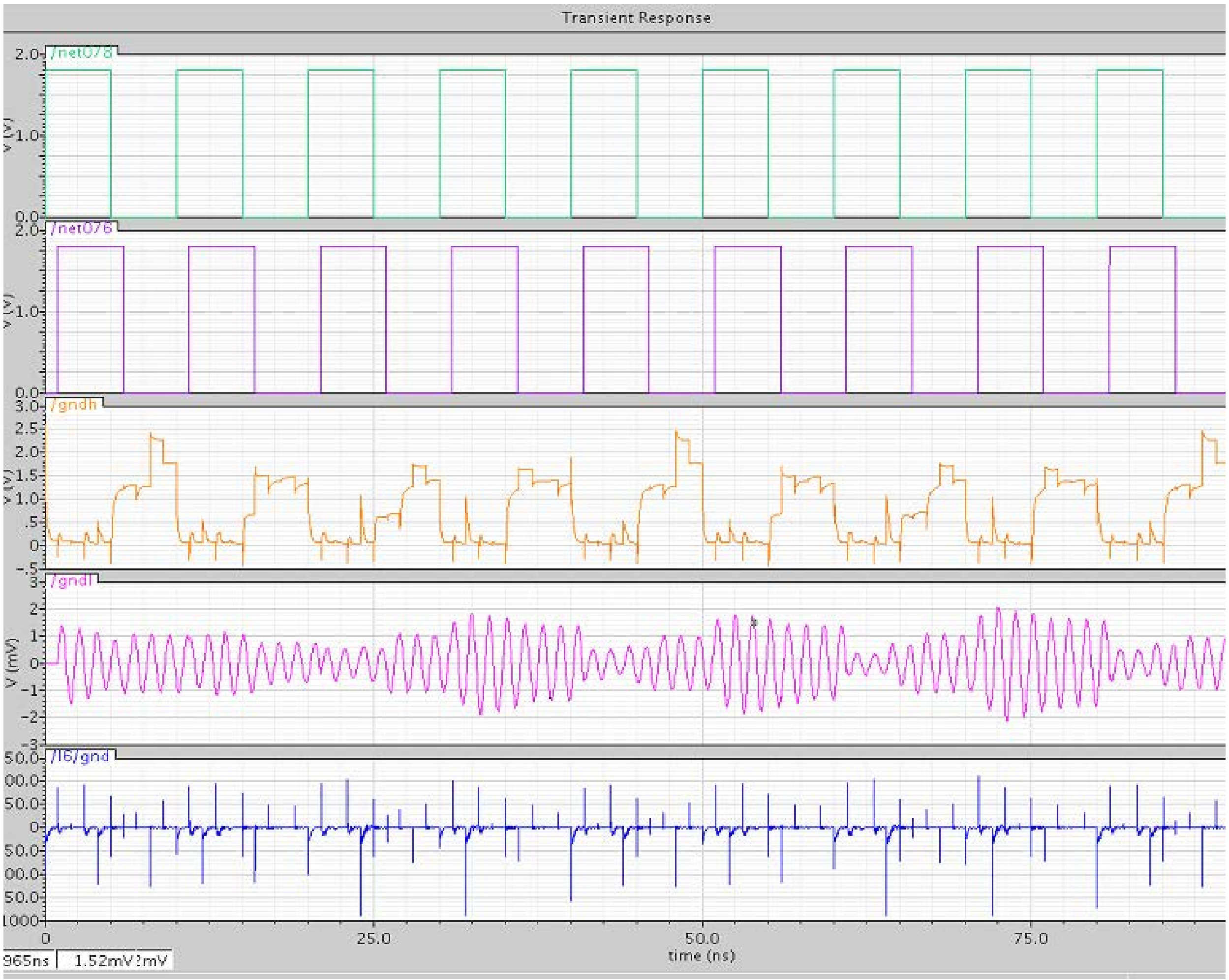

Figure 5.9: Simulation result for stacking power gating technique

5.3.3.2 Layout of the circuit used for stacking power gating technique

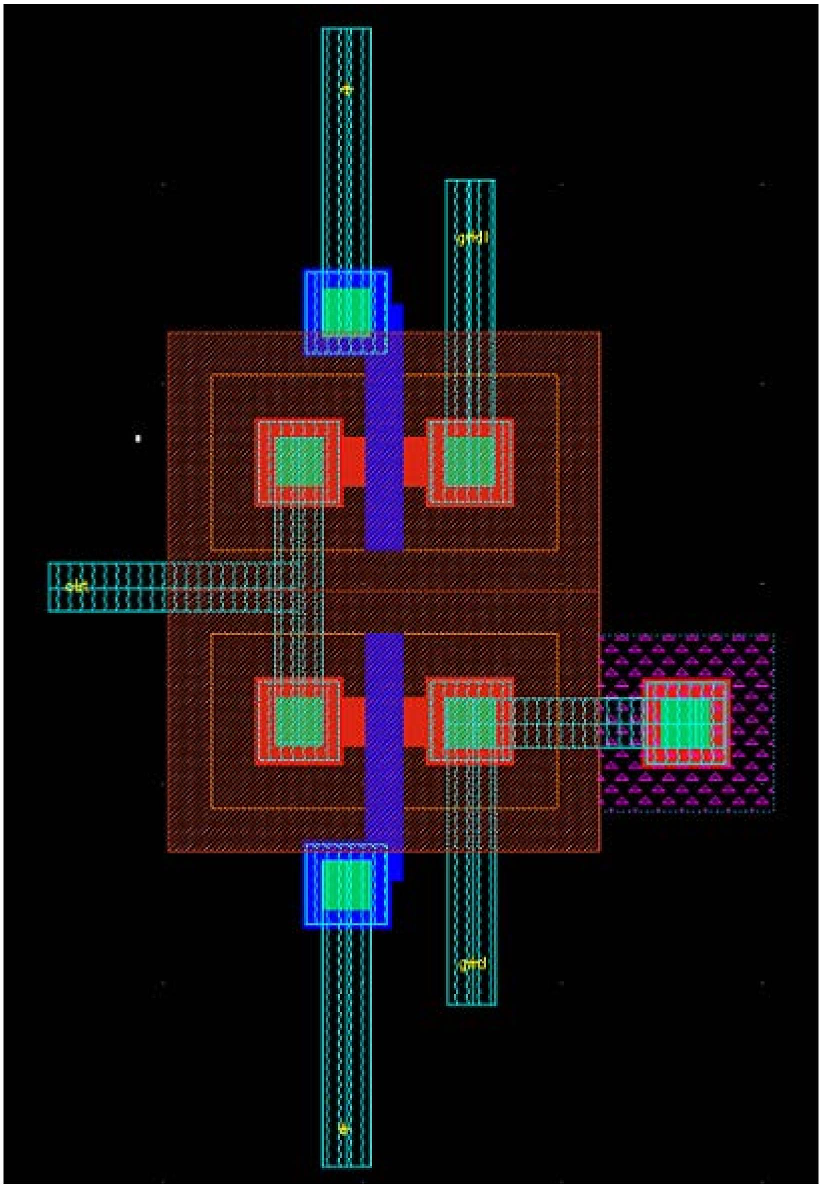

Figure 5.10: Layout of the circuit used for Stacking power gating technique

Figure 5.10 is the Layout of the circuit used for Stacking power gating technique. It is the layout of the additional circuitry used in the Stacking power gating technique to lower down the ground bounce noise as well as current surge.

5.3.4 Slow rising wakeup signal MTCMOS

By applying a slowly rising wakeup signal we can control the rate of change of current passing through the sleep device. So we can reduce the ground bouncing to the desired value by increasing the rise time of the signal. The slow rising wakeup signal can be achieved by a two inverter chain as shown in figure 5.11. By increasing the length of the P2 transistor we can achieve the required signal.

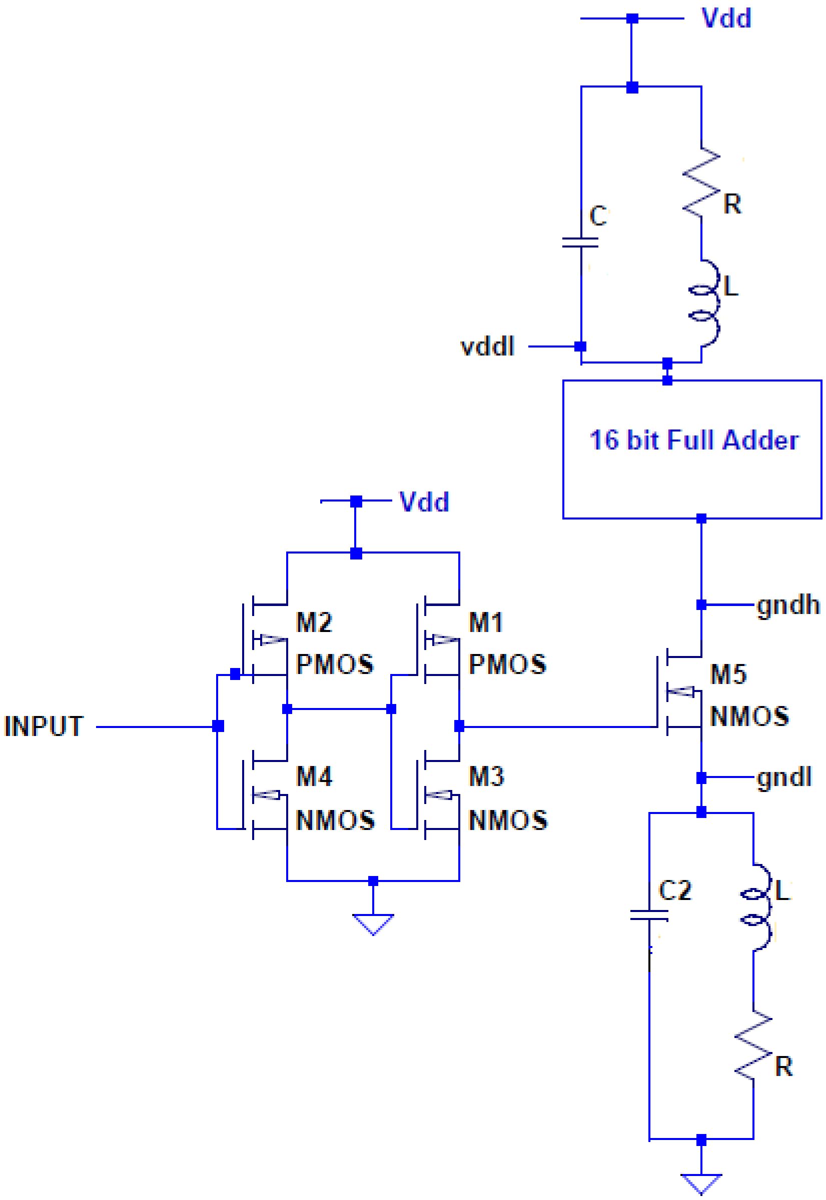

Figure 5.11: Schematic of Slow rising wakeup signal MTCMOS

5.3.4.1 Simulation result for slow rising wakeup signal MTCMOS technique

Figure 5.12 is the simulation result of the schematic from figure 5.11. The result reveals that the maximum peak of the ground bounce noise induced is nearly 28.48 mV and the maximum peak of current surge is 0.63 mA. As we can see from the figure 5.12 that even after the ground bounce is nearly nullified the wakeup signal is still rising to reach V_{DD}. So the time taken for the sleep device to be completely switched on is high, so the wakeup delays are high in this technique.

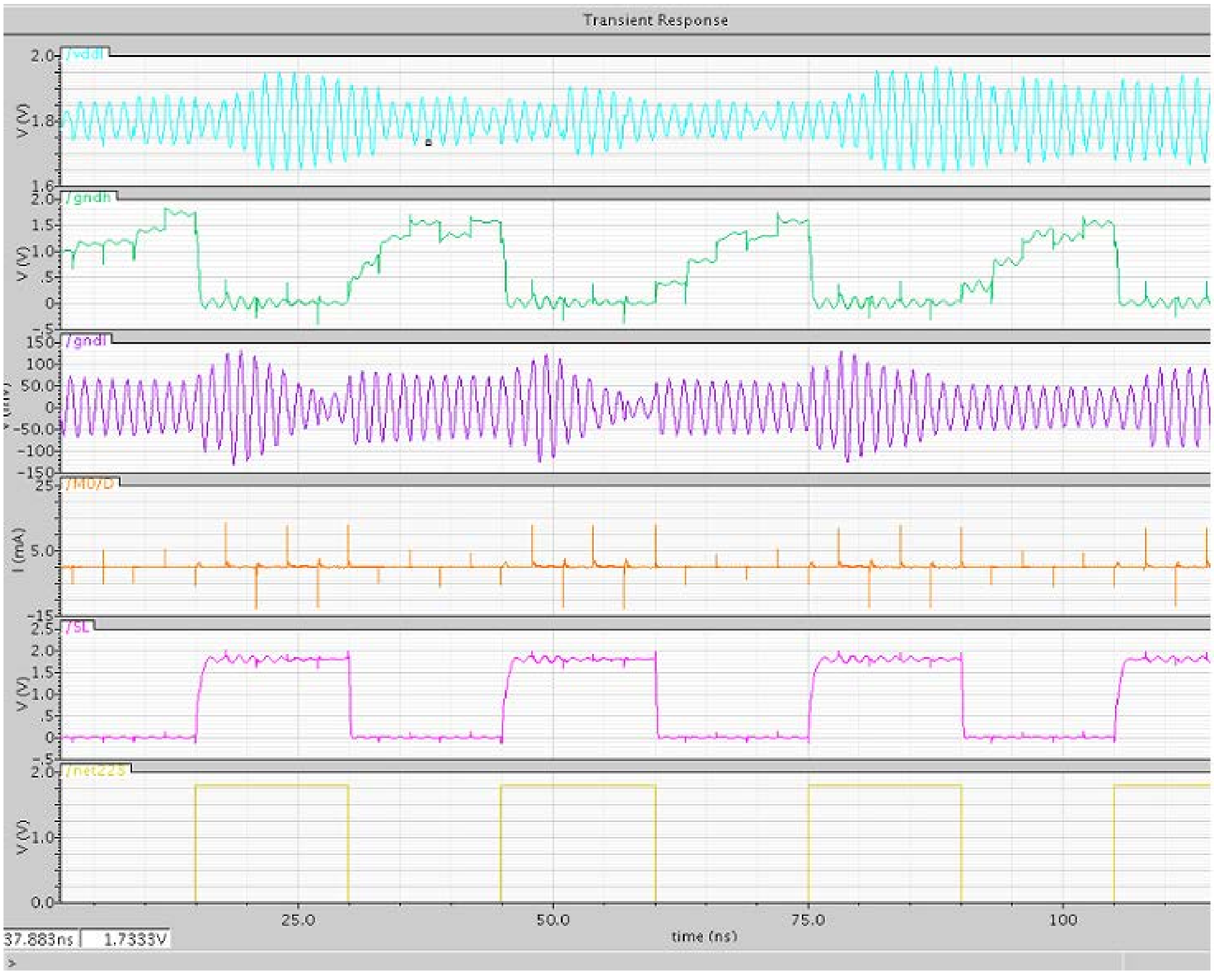

Figure 5.12: Simulation result for slow rising signal technique

5.3.4.2 Layout of slow rising wakeup signal topology

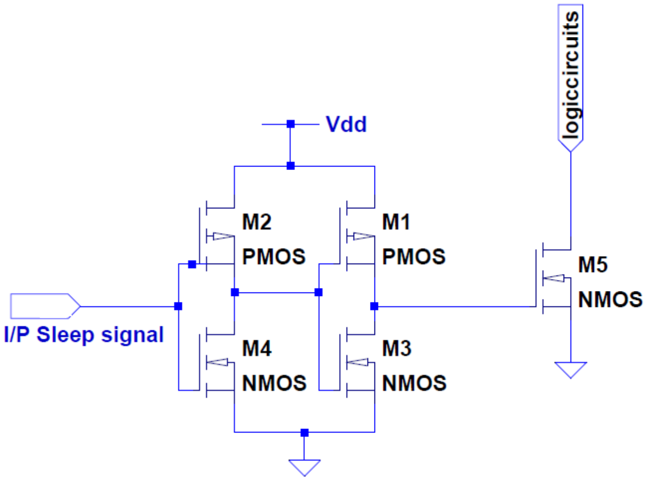

Figure 5.13: Circuit Used in Slow rising wakeup MTCMOS

Figure 5.14 is the Layout of the circuit used (figure 5.13) for the proposed slow rising wakeup MTCMOS technique. It is the layout of the additional circuitry used in the slow rising wakeup MTCMOS technique to lower down the ground bounce noise as well as current surge.

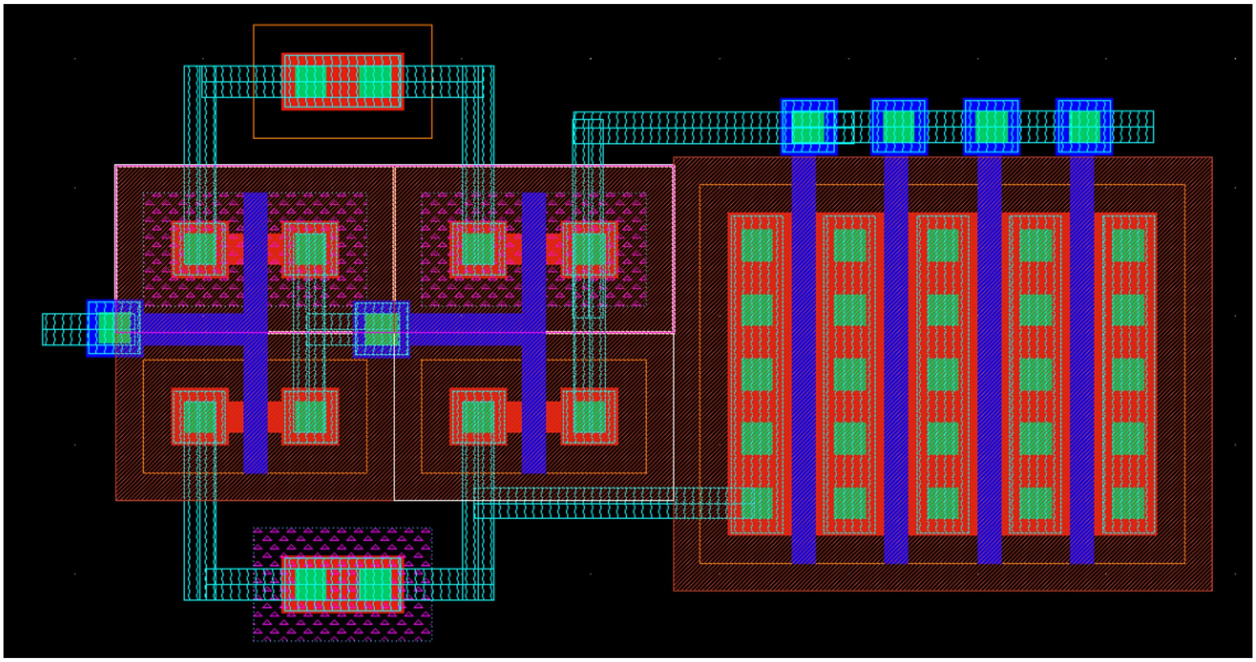

Figure 5.14: Layout of slow rising wakeup signal topology

5.4 Comparison Result of Different Technique

To minimize the ground bouncing, different techniques are proposed. All these technique are successful in minimizing the ground bouncing. In this section we have compared these techniques in terms of the amount of ground bounce minimization, wakeup delay, area overhead caused by the extra circuitry to implement these techniques and the leakage power.

5.4.1 Ground bouncing

The amount of ground bouncing is tabulated in table 5.1 for 16 Bit Full Adder. All the results taken are from cadence tool at 180nm technology.

Table 5.1Comparison of GBN reduction technique for ground bounce

Technique used	Ground bounce peak (mV)	Reduction percentage
MTCMOS Technology	356.39	
Tri-mode	79.13	77.79%
Stacking power gating	92.66	74%
Dynamic Variation of sizes	31.18	91.2%
Slow rising wake up signal	28.48	92 %

From the table 5.1 it is clear that slow rising wakeup signal will minimize the ground bouncing up to 92%. The stacking power technique gives the least minimization among the technique with a reduction of 74%. With the information from table 5.1, the bar graph is plotted for maximum peak of ground bounce for 16 bit full adder shown in figure 5.15.

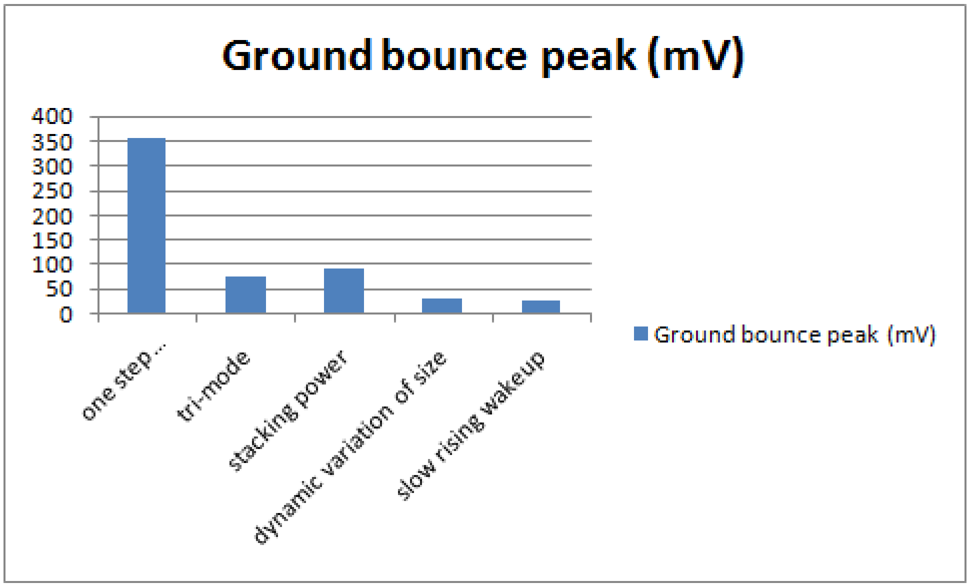

Figure 5.15: Comparison of different power gating technique for GBN

5.4.2 Dynamic power

Dynamic power is calculated in standby mode as well as in active mode. It is also termed as average power which is combination of switching power and static power. The total leakage power is the leakage power through sleep device and the extra circuitry that is designed to apply this technique. Table 5.2 shows the leakage power for 16 bit full adder.

Table 5.2: Comparison of GBN reduction technique for leakage power

Technique used	leakage power	Reduction percentage
Conventional 16bit full adder	360 µW	
MTCMOS Technology	190.6 µW	47%
Tri-mode	178.9344 µW	50.2%
Stacking power gating	201.6 µW	44%
Dynamic Variation of sizes	168 µW	53%
Slow rising wake up signal	145.13 µW	59 %

From the table 5.2, it is observed that the leakage power did not changes much between different technique, because the area overhead caused is very small compared to the size of the sleep device. So the leakage power is majority because of the sleep devices. The extra circuitry causes small leakage compared to leakage of sleep transistor. With the information from table 5.2, the bar graph is plotted for maximum peak of ground bounce for 16 bit full adder shown in figure 5.15.

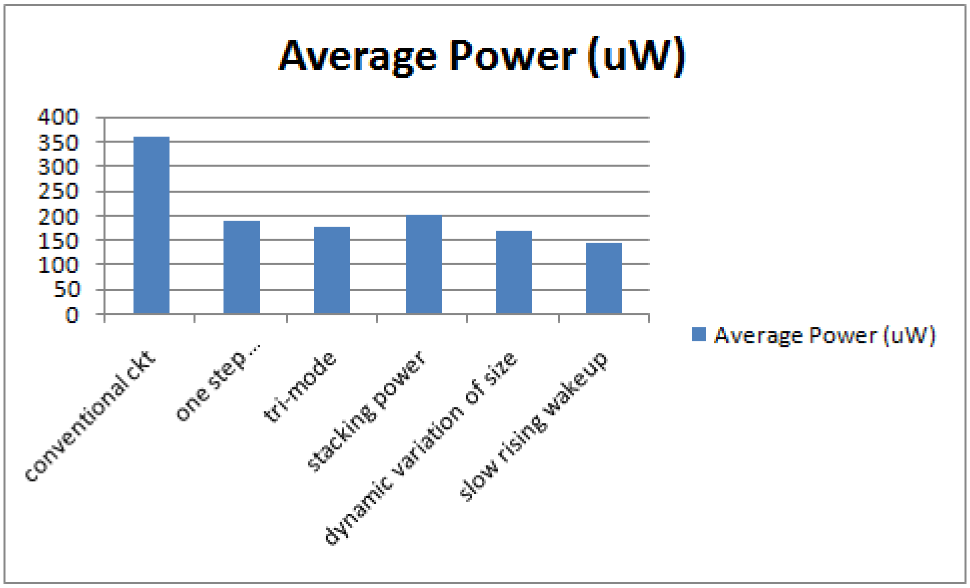

Figure 5.16: Comparison of different power gating technique for average power

5.4.3 Current Surge

The maximum peak of the current surge in the standby mode is measured and tabulated in the table 5.3. The current surge mainly comes in significance when there is mode transition from sleep mode to active mode. This current surge is responsible for the peak of ground bounce noise in the transition mode from sleep to active mode.

Table 5.3: Comparison of GBN reduction technique for current surge

Technique used	Peak current surge, I_{surge} (mA)
MTCMOS Technology	13.64 mA
Tri-mode	11.86 mA
Stacking power gating	0.932 mA
Dynamic Variation of sizes	1.8 mA
Slow rising wake up signal	0.63 mA

From the table 5.3, the slow rising wakeup signal has least current surge in its sleep mode, so that it has least peak of ground bounce also. From the table 5.3, the bar graph is drawn as shown in figure 5.17.

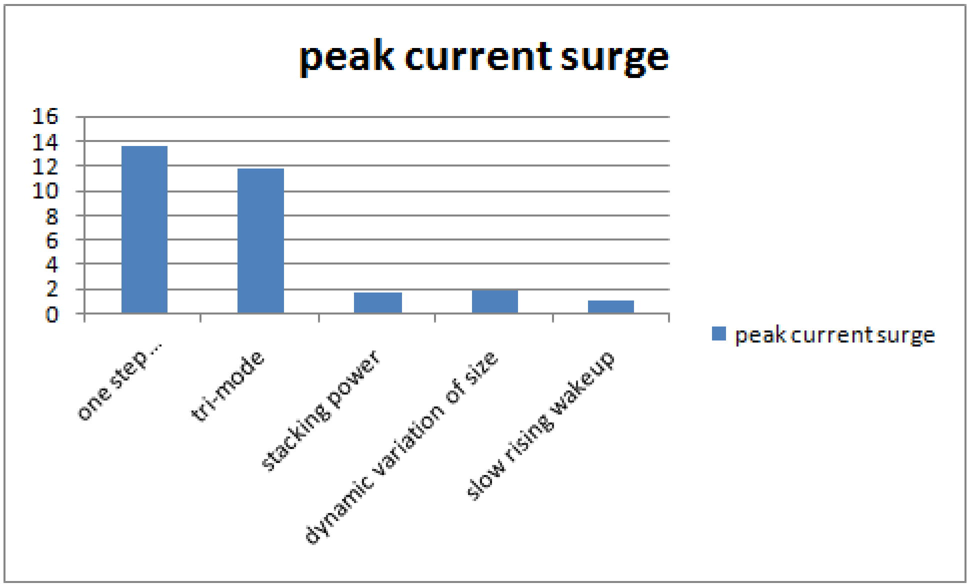

Figure 5.17: Comparison of different power gating technique for peak surge current

5.4.4 Wakeup delay

Wakeup delay is another important parameter to be considered in defining the efficiency of the technique. We have taken the wakeup delay as the time taken for the ground bouncing to reach ±1 mV while the sleep transistor is completely switched on. The wakeup delay is tabulated in table 5.4 which is for different power gating technique used for16 bit full adder circuits

Table 5.4: Comparison of GBN reduction technique for wakeup delay

Technique used	wakeup delay
MTCMOS Technology	138.6 psec
Tri-mode	110.88 psec
Stacking power gating	156.6 psec
Dynamic Variation of sizes	129 psec
Slow rising wake up signal	168 psec

From the table 5.4, it is evident that the stacking power gating has highest wakeup delay and tri-mode technique has least wakeup delay. The least the wakeup delay is reciprocated as best technique. From the table 5.4, bar graph is drawn as shown in figure 5.18.

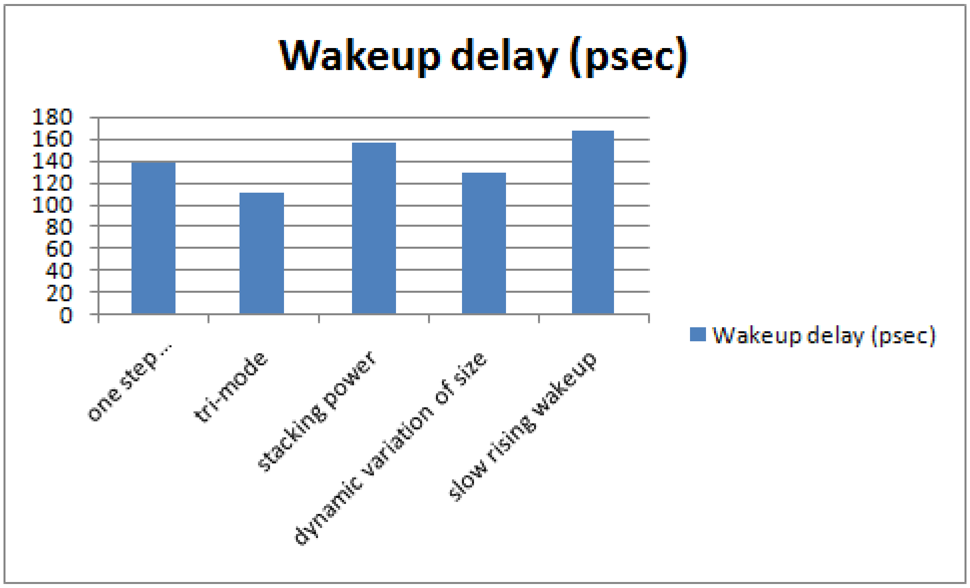

Figure 5.18: Comparison of different power gating technique for wakeup delay

5.4.5 Area overhead

To implement each of the technique some extra circuitry is needed. The area overhead caused by this circuitry is shown in table 5.5 for each technique.

Table 5.5: Comparison of GBN reduction technique for area overhead

Technique used	area overhead (μm^2)
MTCMOS Technology	19.34
Tri-mode	38.6906
Stacking power gating	11.376
Slow rising wake up signal	44.3344

From the table 5.5, it is observed that slow rising wakeup technique has highest area overhead. The bar graph is drawn as shown in figure 5.19 with the help of table 5.5.

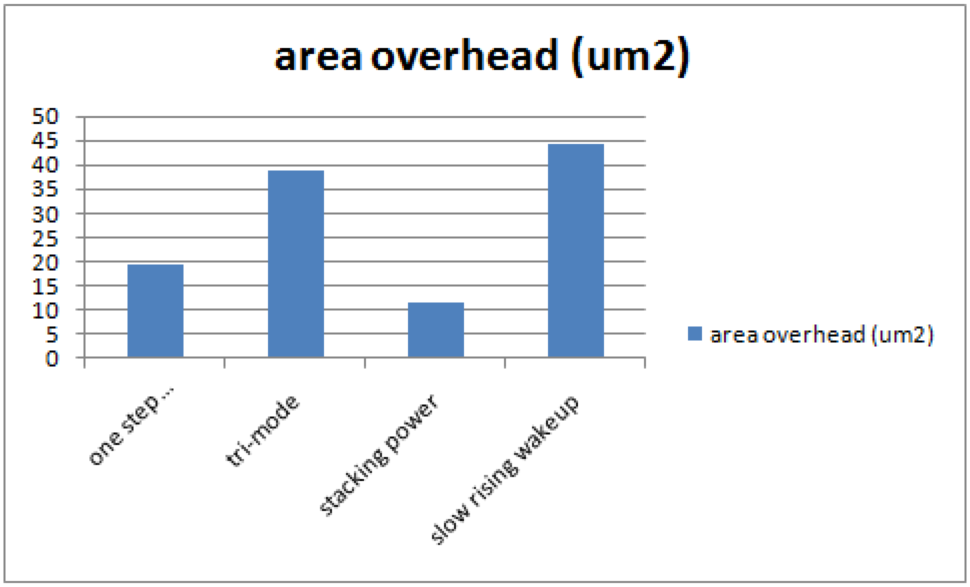

Figure 5.19 Comparison of different power gating technique for Area Overhead

CHAPTER

6

CONCLUSION AND FUTURE SCOPE

MTCMOS Power Gating is a very effective technique for low power VLSI design. But this technique suffers from ground bouncing noise during sleep to active mode transition. To minimize the ground bouncing noise, different techniques are applied on a 16-bit Ripple carry Adder in 180 nm CMOS Technology.

We have investigated the ground bounce caused by large charge and discharge currents through a sleep transistor during the mode transition of a power-gating structure. In the proposed slow rising wakeup technique, the primary motive for the technique is to reduce ground bouncing which is controlled by controlling the rate of change of current. This is achieved in the proposed technique by applying a wake signal having long rise time. The wakeup signal is applied to an inverter chain whose output is applied to the sleep device. By applying slow rising wakeup signal as power gating solution we are able to suppress the ground bouncing amplitude by 92%.

The comparison of the proposed technique with other ground bounce reduction technique like Tri–mode technique, stacking power technique and dynamic variation of size of sleep device have done on different parameter like amount of ground bounce noise reduced, amount of current surge, average power, wakeup delay and area overhead. The slow rising wakeup signal MTCMOS Technique has reduced the amplitude of ground bounce by maximum percentage of 92% in comparison to other techniques.

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