Thesis

On

"DESIGN AND ANALYSIS OF SMART VOLTAGE COMPARATOR"

Submitted In the partial fulfillment for the award of
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In

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DECLARATION

I hereby declare that the thesis entitled **"DESIGN AND ANALYSIS OF SMART VOLTAGE COMPARATOR"** is an authentic record of my work carried out as partial requirement for the award of degree of M.Tech (VLSI Design) at Thapar University, Patiala under the supervision of Dr. Alpana Agarwal, Associate Professor, ECED.

The matter embodied in this thesis has not been submitted for award of any other degree at this or any other university.

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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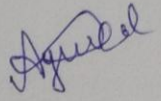

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ABSTRACT

Digital wireless communication, digital signal processing and implanted biomedical devices have emerged as exciting applications of Analog-to-Digital Converters (ADCs). All these applications are energy-constrained and thus demand low-power ADCs. A comparator is a key building block in ADC architecture. Its design affects the various parameters of ADC like power consumption, delay, accuracy etc. An efficient comparator detects the small input voltage difference within short time and amplifies the output to either of the two logic levels i.e. 0 or 1. Though dynamic latched comparators are quite attractive but they suffer from high power consumption and large offset voltage.

This work proposes a novel, digital-in-concept and opamp-less approach to design a fully-differential voltage comparator. Besides low power consumption, it is highly cost-effective as an analog circuit has been designed digitally. Comparators are designed and simulated in Cadence® Virtuoso Analog Design Environment using UMC 180nm CMOS digital process at 1.8V supply with load capacitance of 1pF. Layout of the proposed comparator was designed in Cadence® Virtuoso Layout XL Design Environment. The post-layout and process corner simulations were done for the propagation delay, offset voltage and average power dissipation.

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LIST OF ACRONYMS

IC	Integrated Circuit
CMOS	Complementary Metal-Oxide Semiconductor
NMOS	Negative-Channel Metal-Oxide Semiconductor
SoC	System-on-Chip
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
CM	Common-mode
DP	Differential Pair
ICMR	Input Common Mode Range
ADC	Analog-to-Digital Converter
ADE	Analog Design Environment
UMC	United Microelectronics Corporation
TT	Typical NMOS Typical PMOS
SS	Slow NMOS Slow PMOS
FF	Fast NMOS Fast PMOS
SF	Slow NMOS Fast PMOS
FS	Fast NMOS Slow PMOS
VLSI	Very Large Scale Integration
MOSCAP	Metal-Oxide Semiconductor Capacitor
DC	Direct Current
SAR	Successive Approximation Register
LED	Light Emitting Diode
SC	Switched Capacitor
ICMR	Input Common-Mode Range

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1. INTRODUCTION

1.1 MOTIVATION

With battery operated and easy to carry devices trending, low power has became an important issue in circuit design. Low-power circuits can have a durable battery and minimum area requirements for the battery cells so that the overall device looks handy and light in weight. Usually, power dissipation in analog circuits is reduced by lowering the supply voltage, but reduced supply voltage does not guarantee the best performance for analog circuits. Since, there are various process dependent parameters such as threshold voltage that limit the overall performance of scaled circuit designs. Thus, most of the research, nowadays, is centered at devising new power-efficient methodologies.

Analog ICs haven't derived benefits from CMOS technology improvements. The scaled supply voltages and channel-length have resulted in increased process variations and short-channel which have made the analog IC fabrication very challenging. This has led to more complex circuits and stringent trade-offs. A novel solution to the shortcomings faced in present day analog IC fabrication is to emulate analog functions such that they can be designed by methodologies which are as close as possible to the digital design concepts. This is an appealing approach as it exploits high-performance digital technologies and various verification techniques that are employed in the digital field, to the fullest.

1.2 ANALOG DIFFERENTIAL CIRCUIT

An analog differential circuit is quite a common circuit, which is being used in the first stage of opamp generally. An analog differential circuit can be designed using two identical source-coupled MOSFETs M1 and M2. A constant current source is used to bias both the transistors in the saturation region, as depicted in fig. 1. The output currents i_1

and i_2 flowing through M1 and M2, respectively, are independent of the CM input voltage.

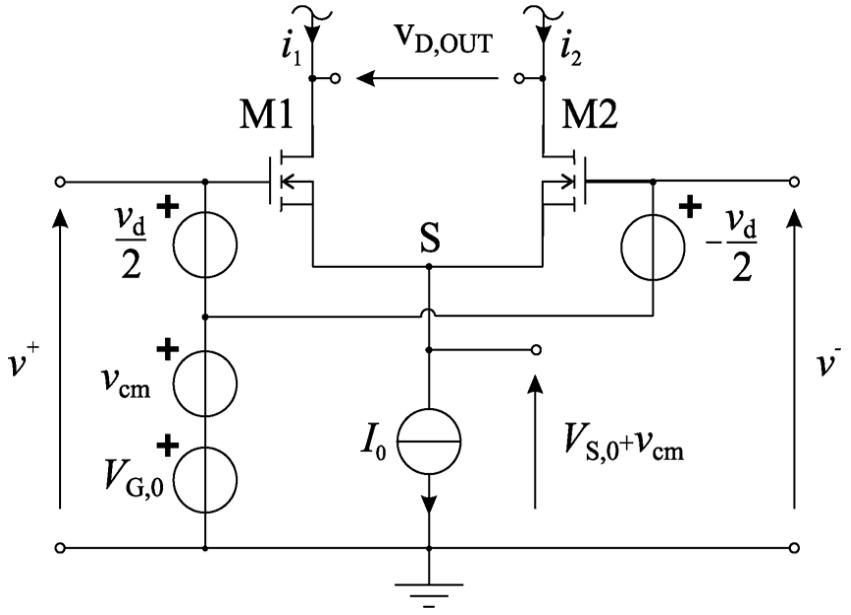


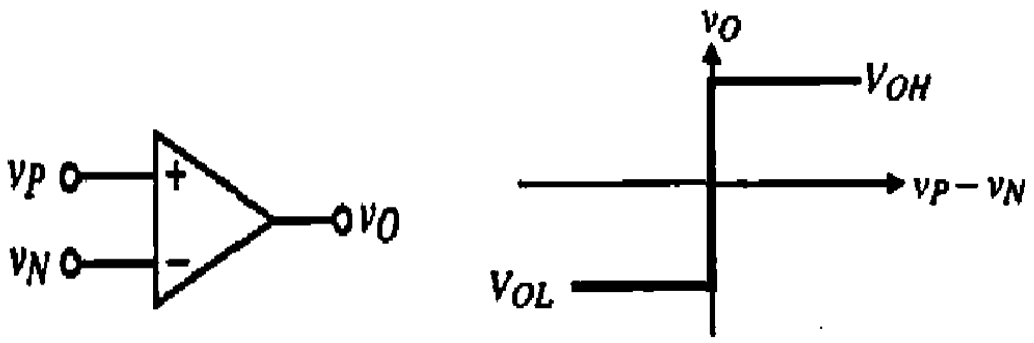
Figure 1. A CMOS differential pair [1]

A CMOS DP, however, suffers from various limitations like ICMR, minimum supply voltage, output voltage swing, power dissipation [2], [3], [4]. Thus, we present here digital-based design of analog comparator [1].

1.3 BASICS OF VOLTAGE COMPARATOR

A comparator provides an output signal that is equal to the difference of two input voltage signals and is independent to the common mode voltage. They are used a lot in various forms of ADCs.

From both the figures 2 (a) and (b), we observe that v_P is the input voltage applied to



(a) (b)

Figure 2. (a) Circuit symbol for a comparator (b) Ideal transfer curve of a comparator [5]

positive input terminal of comparator and v_N is the input voltage applied to negative input terminal of comparator. If v_P is greater than that of v_N, then the output of the comparator is logic high else, it is logic low.

1.3.1 STATIC CHARACTERISTICS

Static characteristics comprises of gain, input offset voltage, resolution and noise. Ideally output changes states for an input change of ΔV, where ΔV approaches zero. The voltage gain of comparator can be written as

$$\text{Gain} = A_v = \lim_{\Delta V \to 0} \frac{V_{OH} - V_{OL}}{\Delta V} \quad (1)$$

Fig. 3 shows the practical dc characteristic curve of a comparator. Thus,

$$A_v = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} \quad (2)$$

where V_{IH} and V_{IL} represent the input voltage difference needed to just saturate the output at its upper and lower limit, respectively.

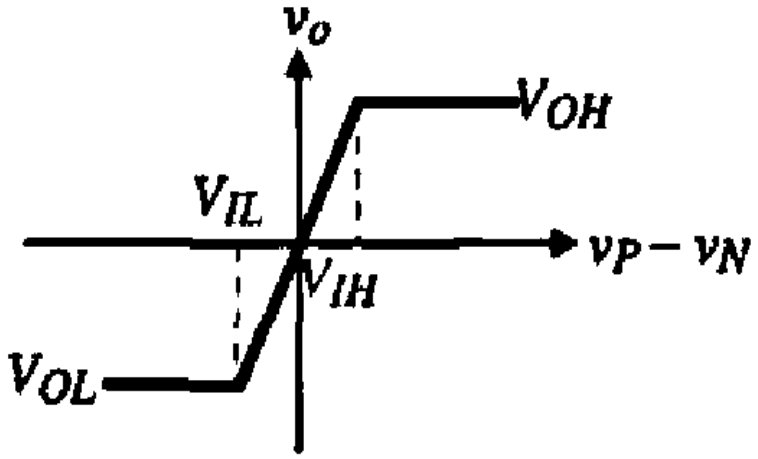


Figure 3. DC characteristic curve of a comparator with finite gain [5]

Gain defines the minimum input change (resolution) necessary to make the output swing between the two binary states.

In fig. 2(b), the output switches from one logic level to another as soon as the inputs' difference becomes zero. If the output doesn't not switch until the inputs' difference reaches a value V_{OS}, then this difference is termed as the offset voltage as shown in fig.4:

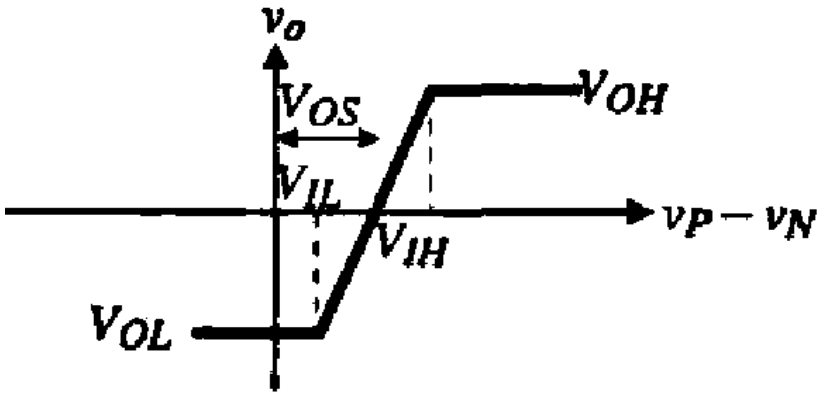


Figure 4. Transfer curve of a comparator including input offset voltage [5]

This offset voltage poses a problem for circuit designers as it varies randomly from circuit to circuit, and is hard to predict.

Besides the above characteristics, ICMR is also an important parameter. The ICMR for a comparator is the range of input common mode voltage over which the comparator functions, perfectly.

1.3.2 DYNAMIC CHARACTERISTICS

These comprise mainly of speed or propagation time delay. Propagation delay (t_p) is determines the conversion speed of an ADC. As shown in fig. 5, t_p can be defined as at how much speed the amplifier responds with applied input.

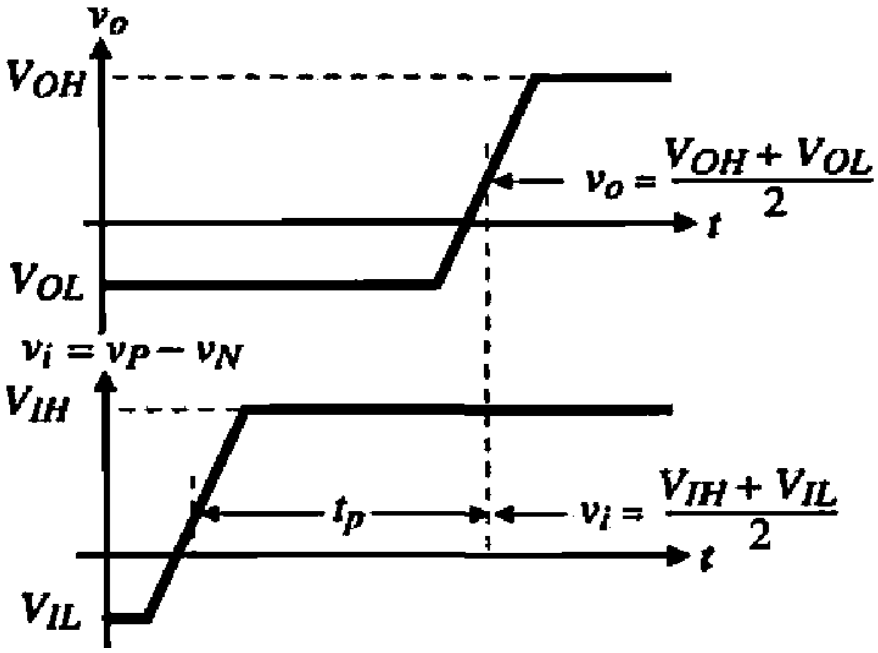


Figure 5. Propagation delay time of a non-inverting comparator [5]

The propagation delay in comparators is dependent on the amplitude of the inputs. A larger input results in a smaller delay time. Delay varies with supply voltage too. It has a tradeoff with power dissipation in the circuit.

1.3.3 POWER DISSIPATION

Power dissipation is a crucial design specification for a comparator. Analog CMOS circuits consume more power as compared to digital CMOS circuits [6].

Total power dissipated in a digital CMOS circuit is given by the sum of dynamic (or

switching) power dissipation (P_{dyn}), short-circuit power dissipation (P_{sh}) and leakage power dissipation (P_{leak}).

$$P_{total}=P_{dyn}+P_{sh}+P_{leak} \quad (3)$$

P_{dyn} is the power dissipated due to switching which occurs when a node capacitance is charged or discharged, P_{sh} is the power dissipated due to the short circuit current (direct path current) that flows from supply voltage to ground and P_{leak} is the power dissipated, even when there is no switching. It plays an important factor in ultra-deep sub-micron technologies. But, it can be easily neglected in the present case of 180 nm technology. Thus, power dissipation, in our case, is mainly due to P_{dyn} and P_{sh}.

1.4 THESIS ORGANIZATION

This thesis work is organized into five chapters as follows:

Chapter1 includes motivation, introduction of analog differential circuit, basics of voltage comparator and organization of the thesis.

Chapter2 provides literature survey of low-power analog circuits, thus emphasizing on the complexity and performance limitations of analog circuits. Further, voltage comparators have been discussed.

Chapter3 provides design of proposed comparators and their simulation results.

Chapter4 provides layout design and post-layout simulation results.

Chapter5 concludes the thesis and provides future scope.

2. LITERATURE SURVEY

Many papers on the recent researches and developments in the field of low-power consumption, improvement of input common mode range, output swing and process variations in operational amplifiers were studied. A succinct review based on the study of these papers is as follows:

J.H.Huijsing, R.Hogervorst, and K.-J. de Langen "Low-power low-voltage VLSI Operational amplifier cells" 1995 [2]

Higher element densities in VLSI circuits affect the fundamental limits in analog circuit design. The bandwidth and gain are restricted by minimum supply currents and voltages. The design of power-efficient rail-to-rail (R-R) class-AB output stages and efficient overall topologies for bandwidth and gain are the problems which must be solved in designing complete new analog circuit architectures that allow supply voltages of down to 1.8 or even 0.9 V. To process signals with the maximum signal voltage at a certain supply voltage, we require R-R input stages. In the two- and three-stage amplifiers, the gate swing of the output transistors was limited by either cascodes or differential pairs, which further constrained the drive capability of the opamp. In this paper, voltage efficient input stages and current-efficient output stages were designed. The aim was to adopt a multipath architecture such that bandwidth gets preserved while adding more stages in cascade. Several circuit examples with a single-stage topology, a two-stage Miller topology, a three stage nested Miller topology, and a four-stage hybrid nested Miller topology were discussed but all of them lead to very complex circuits.

M. Figueiredo, R. Santos-Tavares, E. Santin, J. Ferreira, G. Evans, and J. Goes "A two-stage fully differential inverter-based self-biased CMOS amplifier with high efficiency" 2011 [4]

The power reduction necessity and low supply voltage tendency has driven the ever more challenging design of analog amplifiers to have multiple gain stages and possibly an

output driver stage. In single stage amplifiers, higher dc gain is achieved using cascode devices, but this leads to reduced output swing (*OS*) due to the low supply voltage. Maintaining a high dc gain but now requiring high *OS* would naturally lead to the use of a two-stage amplifier (possibly fully differential, thus doubling the *OS*). In two-stage amplifiers, where compensation is inevitable, though there are numerous techniques for increasing and compensating the gain-bandwidth product, GBW of single and multistage amplifiers, most of them rely on complex multipath and feedforward techniques. In this paper, a two-stage fully differential CMOS amplifier comprising self-biased inverter stages was discussed. A detailed analysis of common-mode feedback, noise, slew rate and input/output range was also presented.

S. S. Rajput and S. S. Jamuar "Low voltage analog circuit design techniques" 2002 [7]

The ultimate goal in design is close to having battery-less systems, because the battery contributes greatly to volume and weight. Solar power, fuel cells, RF power, and so forth, are the most viable alternatives. The voltage of a single solar cell is about 0.5V, which is well below the nominal voltage of dry cells. The design of integrated circuits (ICs) capable of working with solar cells offers a wide range of possibilities. But ICs require much higher voltages for their operation. A possible solution to get higher dc voltage on-chip is voltage multiplication. This technique is noisy and not compatible with sensitive analog circuits. Furthermore, analog designers would have the additional burden of taking care of Power Supply Rejection (PSR) in these circuits. Analog circuits benefit marginally from scaling, as the minimum size transistors cannot be used in analog circuits because of noise and offset voltage constraints. However, scaling results in better performance in digital circuits. In this paper, various low-voltage design techniques like Sub-threshold MOSFETs, Bulk-driven MOSFETs, Self-cascode MOSFETs, Floating gate MOSFETs etc. were presented. For analog circuit design, any one or the proper combination of these techniques can be chosen. Analog circuits can be decomposed into sub-circuits, termed as analog cells. Using any of the low voltage techniques, if these cells can be designed, then the circuits can operate at low voltages.

Pedro M. Figueiredo and João C. Vital ," Kickback Noise Reduction Techniques for CMOS Latched Comparators," 2006 [8]

Latched comparators suffer from a disturbance called kickback noise. In flash ADCs, where a large number of comparators are used, this affects the input and reference voltages of the converter, the location of the code transition voltages may be altered too. Also, in some pipeline architectures, the settling of the amplifiers in each stage may be degraded, due to this phenomenon. This paper reviewed the existing kickback noise reduction techniques. Most common technique is to add a pre-amplifier before the comparator or use source followers. But this leads to static power consumption or increase in offset voltage. It proposed two new effective kickback noise reduction techniques.

Samaneh Babayan-Mashhadi and Reza Lotfi "Analysis and Design of a low-voltage low-power double-tail comparator" 2014 [9]

This paper presented the analysis of dynamic comparator and double-tail dynamic comparator. Clocked regenerative comparators have found wide applications in many high-speed ADCs as they can make fast decisions due to the strong positive feedback in the regenerative latch. However, due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. Also, there is only one current path, via tail transistor and when tail transistor operates in triode region, the tail current depends on input common-mode voltage, which is not favorable for regeneration. In conventional double-tail topology, both the intermediate nodes discharge to the ground during the decision-making phase and each time during the reset phase they should be pulled up back to the V_{DD}. This results in increased power consumption. Also, while designing the proposed double-tail comparator, the effect of mismatch between controlling transistors on the total input-referred offset of the comparator is an important issue. While larger transistors are required for better matching; however, the increased parasitic capacitances are delay bottlenecks. This paper proposed a new dynamic comparator which does not require boosted voltage or stacking of too many transistors. It enhanced the speed by increasing the initial output voltage difference at the beginning of the regeneration and by

enhancing the effective transconductance of the latch. At 1.2V power supply, average power dissipation (at 500 MHz) =329 µW, worst case delay =550ps & offset standard deviation (1-sigma) (σ_{OS}) of 7.8mV were observed.

Mohsen Hassanpourghadi et.al., "A low-power low-offset dynamic comparator for analog to digital converters," 2014 [10]

In comparators, a lower offset comes at the cost of larger transistors hence higher power consumption and reduction in speed. Also, the conventional comparators are complex to design and only few design methodologies control the offset. To reduce the power consumption and the area of comparators, dynamic comparators are proposed. However, they usually suffer from relatively large offset voltage than static counterparts. Thus, a double-phase architecture was proposed, which includes cascading of amplifying stage and a latch stage. This structure cancels the mismatch of inner devices, providing low offset voltage.

Abozeid, K.M. et al., "Different Configurations for Dynamic Latched Comparators used in Ultra Low Power Analog to Digital Converters," 2014 [11]

Meta-stability is an error which occurs in a latched comparator. A meta-stable situation occurs when the latch is not able to switch to a valid logical level "high or low" in the regeneration time constant and reaches an intermediate value. Therefore, an important issue is to compute the probability of this occurrence. Meta-stability can adversely affect the accuracy of the comparator and ADC. Dynamic latched architecture introduces large input referred offset which makes it unappealing for high resolution ADCs. This paper compared different architectures of dynamic comparators on the basis of power consumption and delay under constant offset voltage.

Hamed Aminzadeh, "MOSFET-only pipelined analogue-to-digital converters: non-linearity compensation by digital calibration"2014 [12]

This paper proposed a MOSFET-only pipelined ADC in which it replaced capacitors of the pipeline stages with depletion mode MOSFETs. It discussed about various types of capacitors used in ICs like metal insulator metal (MIM), metal oxide metal (MOM), vertical parallel plate (VPP), poly insulator poly (PIP). These capacitors have been quite costly from fabrication point of view, because of the extra masks required. Instead of these, this paper used MOSCAPs, which are easily available in CMOS technologies and have minimal density and matching issues.

M.B. Guermaz et al., "High-speed low-power CMOS comparator dedicated to 10 bit 20 MHz pipeline ADCs for RF WLAN applications"2008 [13]

This paper proposed a clocked comparator based on switched-capacitors using a two-phase non-overlapping clock, for RF WLAN applications. The clocked comparator circuit includes a pre-amplifier followed by a positive feedback stage. This arrangement uses inverters at the output to lower the gain and increase the bandwidth. But, this comparator suffers from a high offset voltage. To reduce this offset voltage, large transistors have to be added in the pre-amplifier, which in turn, reduce the conversion speed. Hence, a differential comparator configuration was employed to obtain an offset voltage of 77.3 mV, 0.8 mW of power consumption and a delay of 17.3 ns.

I-Chyn Wey et al., "A high-speed, high fan-in dynamic comparator with low transistor count"2014 [14]

This paper approached to enhance the speed by constructing comparator based on dynamic CMOS comparator. This approach resulted in 63.2% saving of transistor count as compared to conventional static circuits. The speed was increased by combating 'weak 0' problem in the PMOS of pull-down network. Instead, an NMOS combined with an inverter was employed. It resulted in low power-delay product (PDP). The proposed 64-bit comparator consumed 0.176 mW power and a delay of 0.38 ns was reported.

Hugues J. Achigui et al., "Low-voltage, high-speed CMOS analog latched voltage comparator using the "flipped voltage follower" as input stage"2011 [15]

The comparator presented in this paper had a differential input stage and had a flipped voltage follower cell that increased the input common-mode range and hence the voltage swing. It also allowed to source large currents, improved slew rate, offered class-AB operation and a high signal-over-noise ratio. It worked on 1V supply and consumed 65 µW power. The core area occupied was 57 µm × 152 µm.

3. DESIGN OF DIGITAL-BASED VOLTAGE COMPARATOR

In literature survey various gaps were found, which are as follows:

- Analog circuits are prone to process & temperature variations.
- Power dissipation in analog circuits is more as compared to digital circuits, because of continuous current flow. While in digital CMOS circuits, there is direct current path from supply voltage to ground at switching instants.
- Full rail-to-rail input and output swings are difficult to achieve, with the trend of scaling, in analog circuits.

Hence, it is required to re-design analog circuits through a novice approach which combat the shortcomings of analog design methodology. Thus, in this chapter, digital-based designs of analog comparator have been presented.

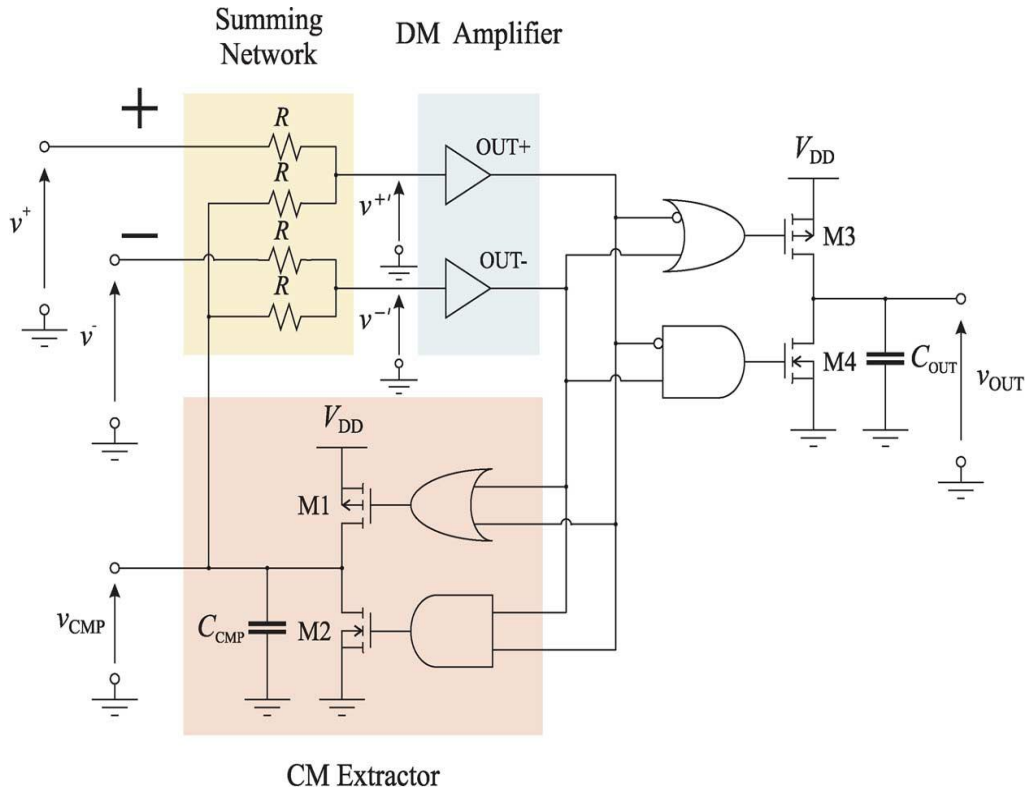


Figure 6. A digital-based differential circuit. [1]

A digital-based differential stage can be designed using two single-ended non-inverting digital buffers [1] as shown in fig. 6. It comprises of CMOS based digital gates and inverters.

This circuit was studied and it was observed that being digital, it takes the full advantage of low-power and ease of circuit design in terms of transistor-sizing, etc. Further changes were brought to it so as to make it more performance-efficient. So, based on this concept, voltage comparator designs have been proposed in this chapter.

3.1 PROPOSED DIGITAL-BASED FULLY DIFFERENTIAL COMPARATOR

Figure 7 shows the design schematic of proposed voltage comparator. It is based on the concept of digital-based differential circuit [1], making use of CMOS-based NAND-NOR and Inverters in the circuit.

3.1.1 SCHEMATIC DESIGN

A buffer provides a logic high output when a signal > V_{sw} is applied at its input & a logic low output when input voltage < V_{sw} is applied. Here, V_{sw} is that input switching/trip voltage at which buffer will change its output voltage. Thus, if we take two buffers and at the input of one buffer, a voltage < V_{sw} is applied and at the input of other buffer, a voltage > V_{sw} is applied, then differential output will be high or low. But, in case the input voltages to both the buffers are > V_{sw} or < V_{sw}, the circuit becomes non-responsive to the differential mode component and hence, the output will be uncertain.

The solution to this deadlock situation is a common mode negative feedback signal (V_{fb}), which is generated with the help of feedback block. V_{fb} gets added up with both the input

voltages V_{p_in} & V_{n_in}, with the help of summer. Summer comprises of four resistors, of equal value. Summer provides the average of the external inputs and the feedback signal (V_{fb}), such that $V_{p\_avg} = \frac{V_{p\_in}+V_{fb}}{2}$ and $V_{n\_avg} = \frac{V_{n\_in}+V_{fb}}{2}$. These voltages are further passed through buffers, to obtain V_p and V_n, which can be regarded as the digital inputs of the circuit. Thus, V_p and V_n are compared and the correct output is obtained, eventually. The feedback block comprises of M5-M6 transistors, loaded by a capacitor, C_{fb}.

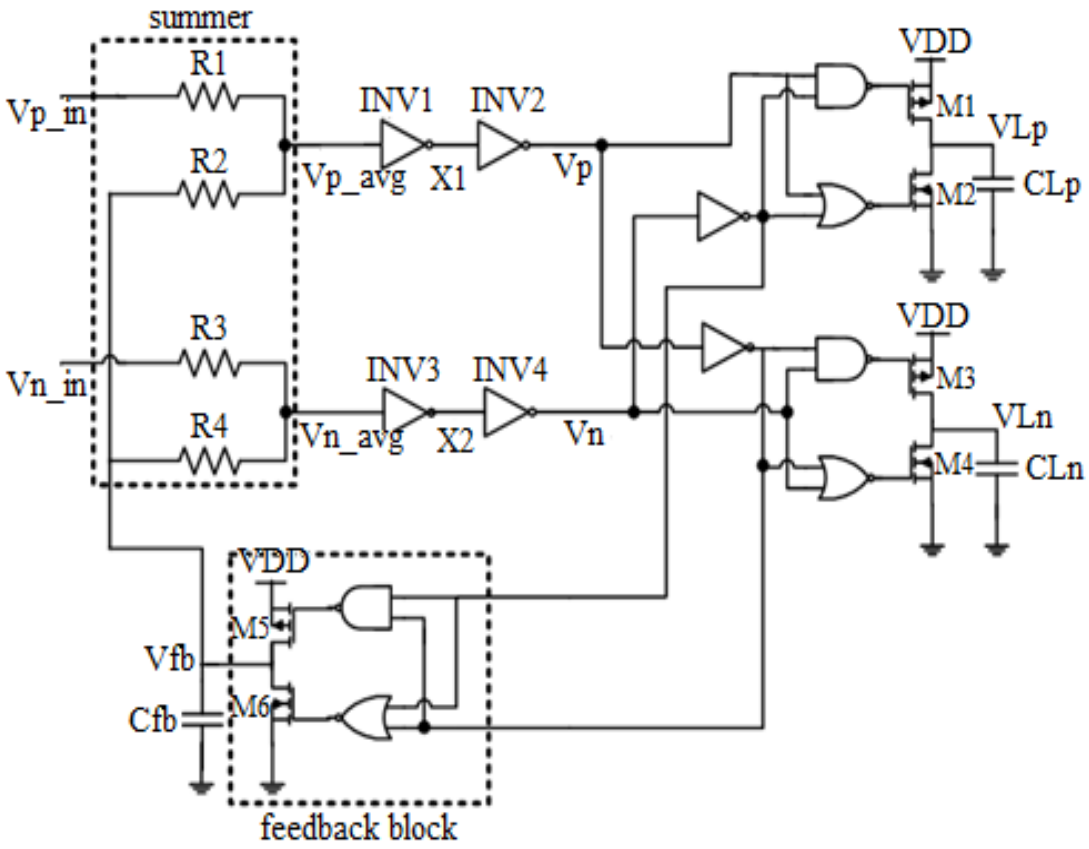


Figure **7**. A proposed digital-based fully differential NAND-NOR based comparator.

Thus, when both the input voltages, V_{p_in} and V_{n_in} are less than V_{sw}, then M5 transistor turns ON to increase V_{fb}. And, when both V_{p_in} and V_{n_in} are greater than V_{sw}, then M6 transistor is turned ON to decrease V_{fb}. This is done to obtain V_{fb} in such a range that after adding up, it leads to distinguishable values of the digital inputs (V_p and V_n) of the circuit. In these two cases, output transistors are OFF, until comparable digital inputs are

obtained through feedback mechanism. And as soon as valid digital inputs are obtained, correct outputs are provided by the output stage. In the case of different input voltages, V_{fb} signal is not required, hence feedback block is OFF and the output-stage transistors (M1-M4) are ON accordingly, to provide correct outputs.

The inverters in fig. 7 have been designed such that their switching threshold voltage (V_{sw})=$\frac{V_{DD}}{2}$. Considering the case of differential inputs, let V_{p_in} be higher than V_{n_in}, once V_{p_avg} and V_{n_avg} cross the V_{sw} of the inverters INV1 and INV3, respectively, V_p rises to logic '1' and V_n decreases to logic '0'. Thus, M1 transistor turns ON and M2 transistor turns OFF. Therefore, VL_p becomes '1' and VL_n becomes '0'. Similarly, when V_{p_in} decreases and V_{n_in} rises, VL_p becomes '0' and VL_n becomes '1'.

As compared to [1], here two output signals VL_p & VL_n have been derived as fully differential circuits have certain benefits over single-ended circuits like, error subtraction, large output swings, rejection of common-mode noise, a high closed-loop speed, etc [16]. But, usually, all this is achieved at the cost of large power requirements [8], [9], which is quite low here. Another advantage of the proposed circuit is the use of universal NAND-NOR gates in the design.

3.1.2 SIMULATION RESULTS

Based on the model presented above, the proposed voltage comparator has been analyzed in this section, through various simulation results. The proposed voltage comparator has been designed and simulated in Cadence® Virtuoso ADE using UMC 180nm CMOS technology.

3.1.2.1 TRANSIENT RESPONSE

To observe the transient response of the comparator, V_{p_in} & V_{n_in} were set at 0.9 V common-mode level (V_{in_cm}) and at an amplitude (ΔV_{in}) of 0.2 V. The various intermediate voltages and final output voltages were observed as shown in fig. 8. Thus, it

is evident from the fig. 8 that in case of differential inputs, V_{fb} remains in the range of V_{sw}.

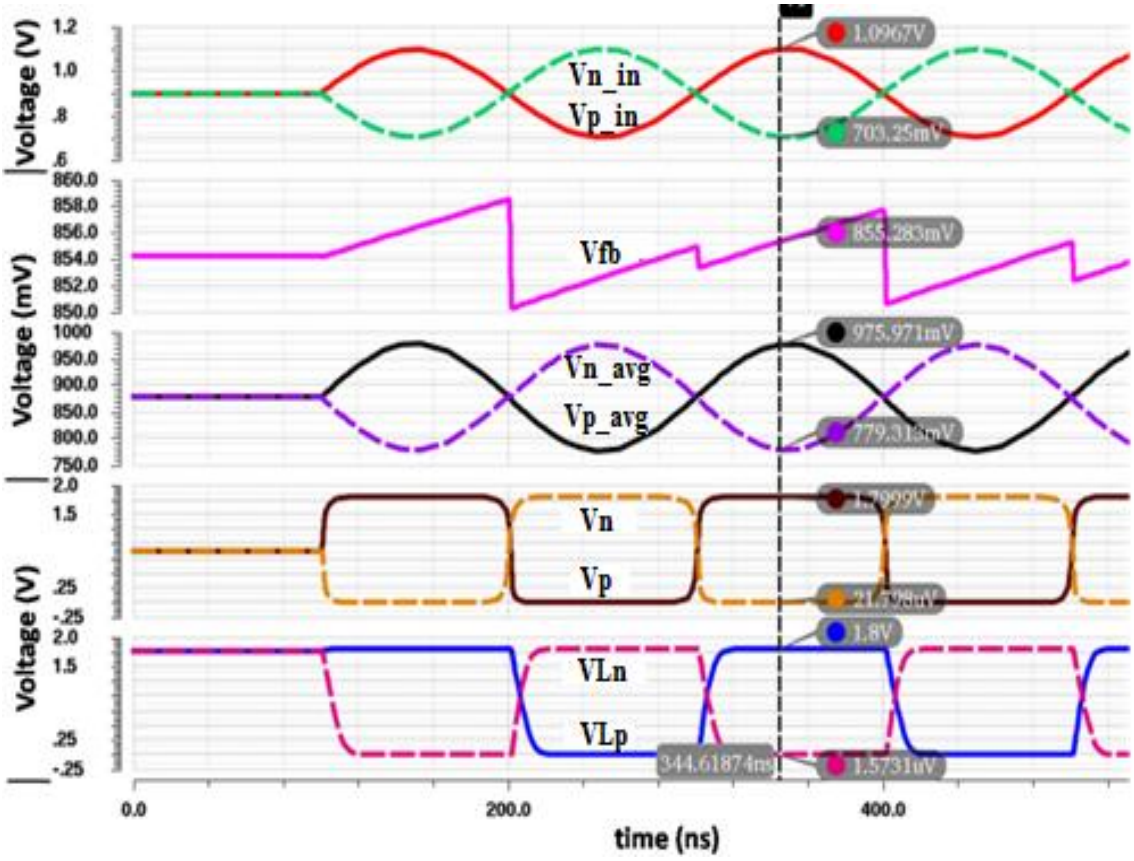


Figure 8. Transient response of digital-based fully differential voltage comparator

The critical (or worst-case delay) path from input to output can be observed in the path from V_{p_in} to VL_n and V_{n_in} to VL_p node. It includes the delay elements as follows:
delay from input V_{p_in} to V_{p_avg} node is due to $(R_1 \| R_2)C_{p\_avg}$ which is equal to 91.5ps where C_{p_avg} is the parasitic capacitance at V_{p_avg} node ,which is mainly due to the input capacitance of inverter INV1. Next, delay from V_{p_avg} to V_p node is 920.9ps, and the delay from V_p node to final output, $VL_n$is 4.4ns. Hence, the total delay from V_{p_in} to VL_n is approximately 5ns. A similar propagation delay analysis can be done for the path from V_{n_in} to VL_p.

Variation in propagation delay [5] of the proposed comparator with change in differential input voltage (ΔV_{in}) can be observed in fig. 9 where V_{in_cm} is at 0.9 V. The delay is

reducing with the increase in input voltage amplitude (ΔV_{in}). The reason is less time consumption, by the feedback block, to bring digital inputs at two different logic levels.

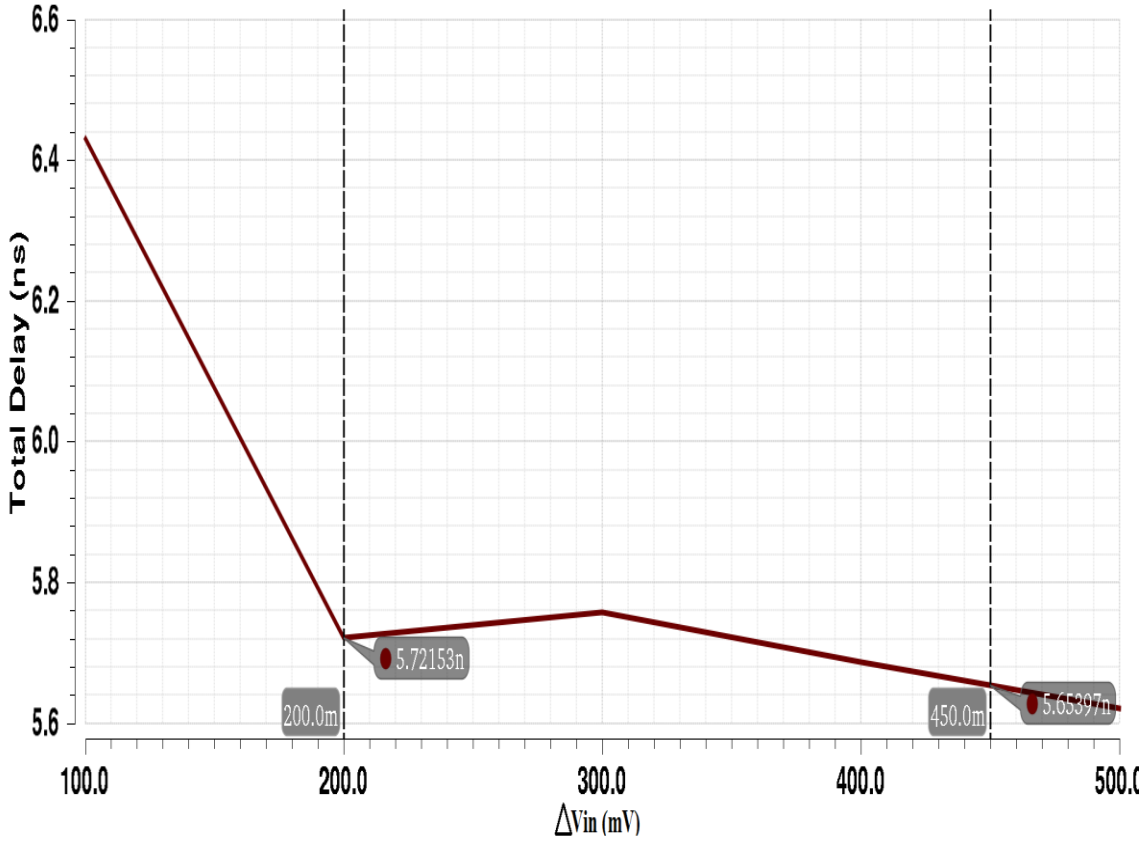


Figure 9. Variation of propagation delay with change in input voltage amplitude

When the input voltage amplitude (ΔV_{in}) is 0.2 V, delay is 5ns approximately.

3.1.2.2 POWER MEASUREMENT

Figure 10 shows the waveforms of voltage and current at various nodes in the proposed comparator. When V_{p_avg} is higher than V_{n_avg}, X1 is lower than X2 and finally V_p and V_n are at different logic levels. Let the currents that flow through INV1 and INV3 inverters be I1 and I3, and the current that flows through rest of the circuit be I2. It can be observed that about 30 µA current flows, all the time, through the inverters INV1 and INV3. While, I2 can be observed only during switching. Thus, most of the circuit's power is consumed by INV1 and INV3. The reason being that the voltage signals V_{p_avg}

and V_{n_avg} are in the range of V_{sw} most of the time. This turns ON both the transistors of INV1 and INV3, which in turn, results in the flow of static current through them. Hence,

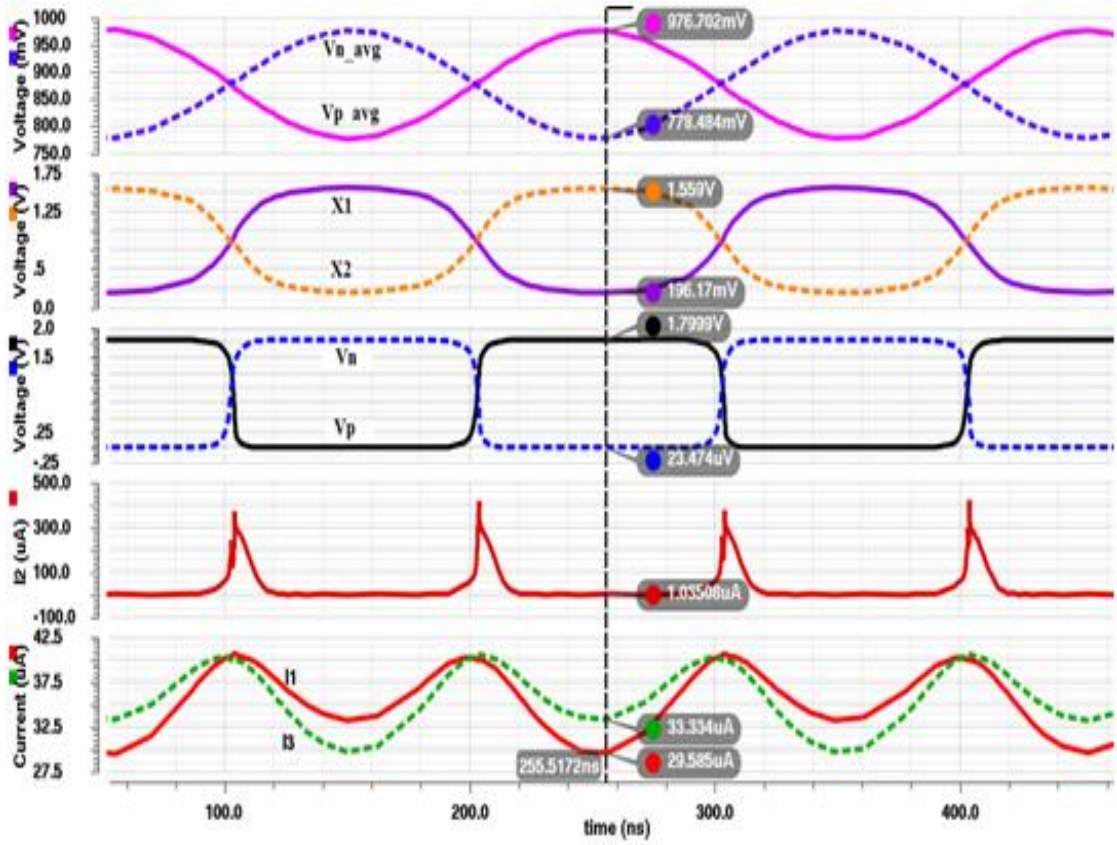


Figure 10. Various voltage and current waveforms

most of the time, the rest of the circuit's current is negligible. This is a very important point from the power consumption point of view. This also proves the fact that very low power is consumed by the digital-based CMOS circuits. Average power dissipated by the proposed comparator was measured to be 180.4 µW.

Variation in average power dissipation with the change in common mode voltage (V_{in_cm}) can be observed in fig. 11. The input voltage amplitude (ΔV_{in}) has been set at 400 mV. This shows that a minima is obtained near V_{in_cm}= 0.9 V and the average power increases whenever we go either side of this minima.

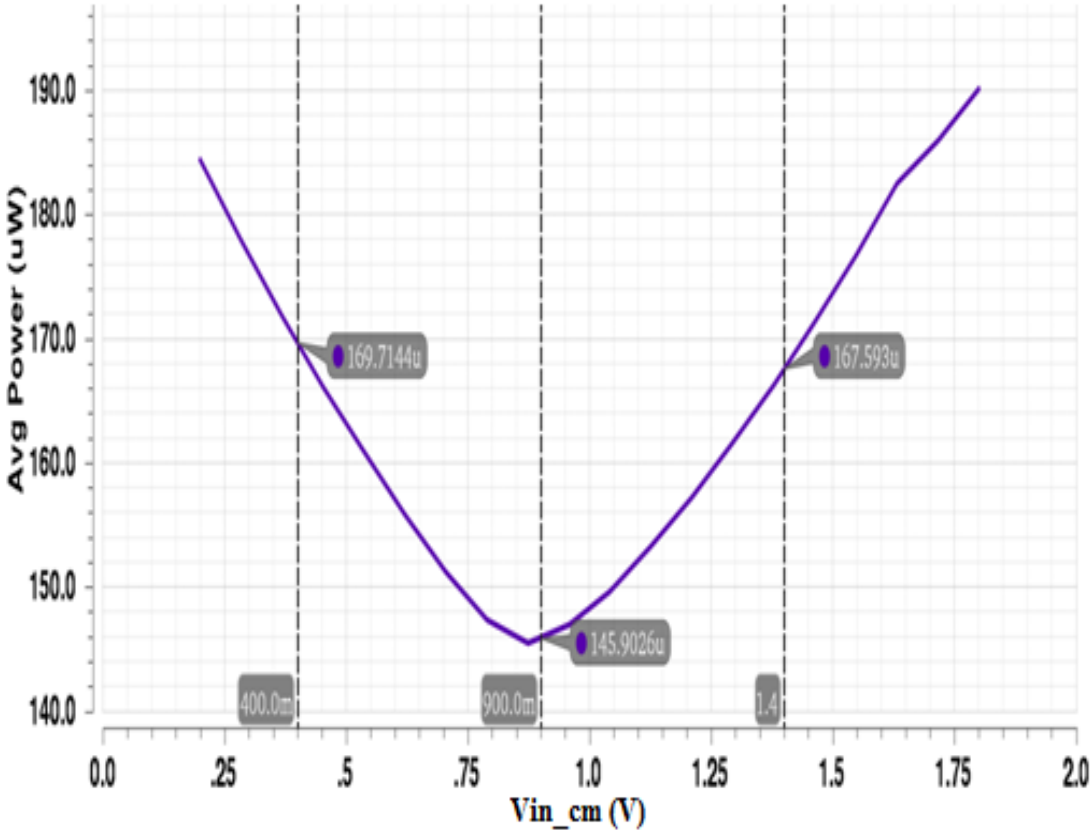


Figure 11. Variation of average power dissipation with input common mode voltage (V_{in_cm})

3.1.2.3 DC ANALYSIS

In DC analysis of the proposed comparator, 5 mV of offset voltage was observed as shown in fig. 12. Though, output voltage is supposed to reach $0.5V_{DD}$ at the dc bias applied at the input. But, the output voltage doesn't reach $0.5V_{DD}$ exactly at the dc bias, this difference is referred to be the offset voltage. Here too, 0.9 V was applied as DC bias to the input. But, instead of switching at this 0.9 V, VL_p switched at 895.09 mV.

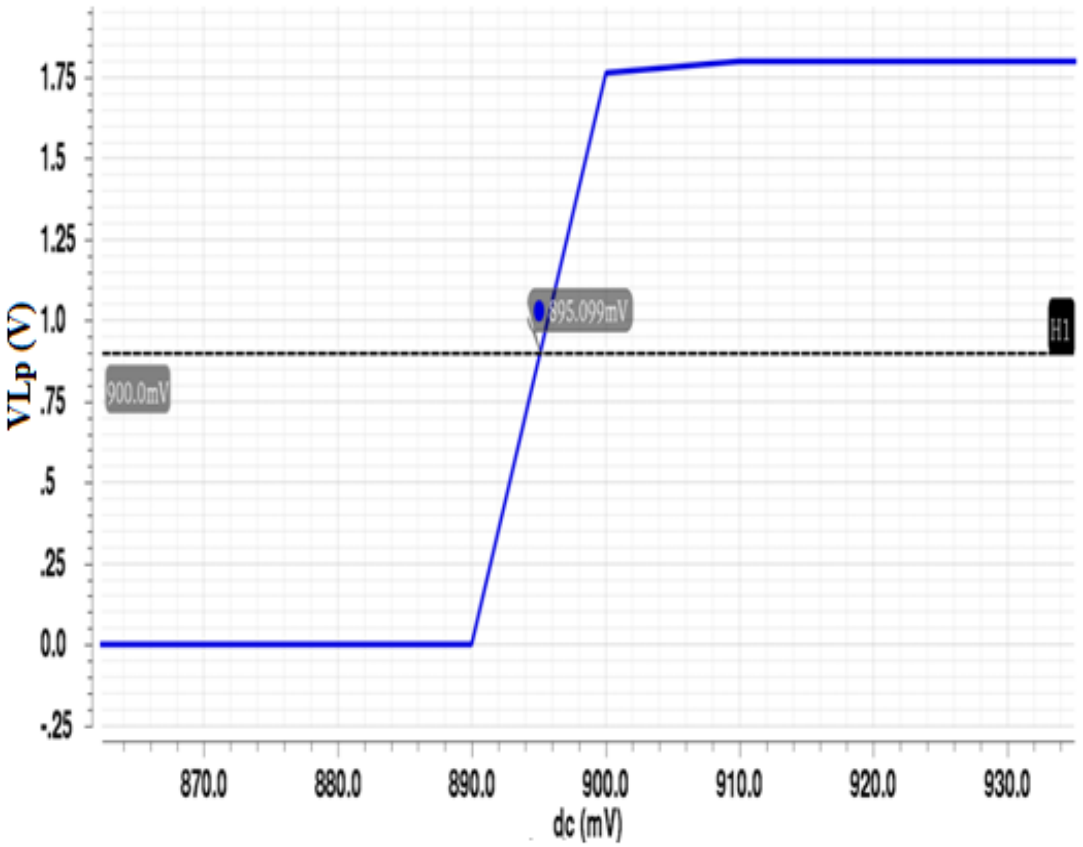


Figure 12: Offset voltage of the proposed comparator

3.1.2.4 PROCESS CORNER VARIATIONS

Corners analysis is a way to measure circuit performance while simulating with sets of parameter values that represent the extreme variations in a manufacturing process. In a real manufacturing scenario, process variables fluctuate randomly around their ideal values. This random variation results in an uncertain yield for the circuit. Corners analysis offers the performance outcomes generated from the most extreme variations expected in the process, temperature and voltage values (the corners). This ensures the largest possible yield of the circuit, in case all parameters produce acceptable results. Therefore, a designer must take into account the effect of process corner variations on the performance of circuit.

In order to observe circuit's performance under extreme conditions, the circuit is observed mainly at four corners: SS (slow NMOS slow PMOS), FF (fast NMOS fast PMOS), SF (slow NMOS fast PMOS) and FS (fast NMOS slow PMOS). Besides, there is one TT (typical NMOS typical PMOS) corner. SS corner is applied with lowest supply voltage (-10% V_{DD}) and highest temperature, thus it provides worst speed. FF corner is applied with highest supply voltage (+10% V_{DD}) and lowest temperature, thus it provides worst power. Table 1 shows the table of corners to obtain simulation results for the proposed comparator:

Table 1: Corners Simulation Table

Corners	V_{DD} (V)	Temperature(◦C)
TT	1.8	27
SS	1.62	125
FF	1.98	0
SF	1.8	27
FS	1.8	27

The various parameters of the circuit were simulated at these corners with temperature and supply voltage as design variables. Table 2 shows the simulated results of various parameters of the proposed comparator of fig. 7 at different process corners.

Table 2: Simulation results with process corner variations

Parameters	**TT**	**SS**	**FF**	**SF**	**FS**
Propagation Delay (ns)	5.7	10.26	4.67	5.5	6.38
Average Power (µW)	180.4	85.9	383.1	173.8	186.8
Offset Voltage (mV)	4.9	2.12	5.46	5	4.8

It is evident from Table 2 that the proposed comparator works at all the corners.

3.2 PROPOSED DIGITAL, MOS-BASED, FULLY DIFFERENTIAL COMPARATOR

In this section, another voltage comparator has been proposed which brings improvements to the proposed comparator of fig. 7.

3.2.1 SCHEMATIC DESIGN

The circuit proposed in fig. 7 had resistors in its summer. In this section, the resistors in the summer have been replaced by four NMOSs, that act as resistors. Moreover, the capacitor (C_{CMP}) in the feedback block has been replaced by MOSCAP (MOSFET capacitor) [12], [17]. MOSCAPs require less area, offer more capacitance per unit area as compared to MIMCAP (metal insulator metal capacitor), MOMCAP (metal oxide metal capacitor),

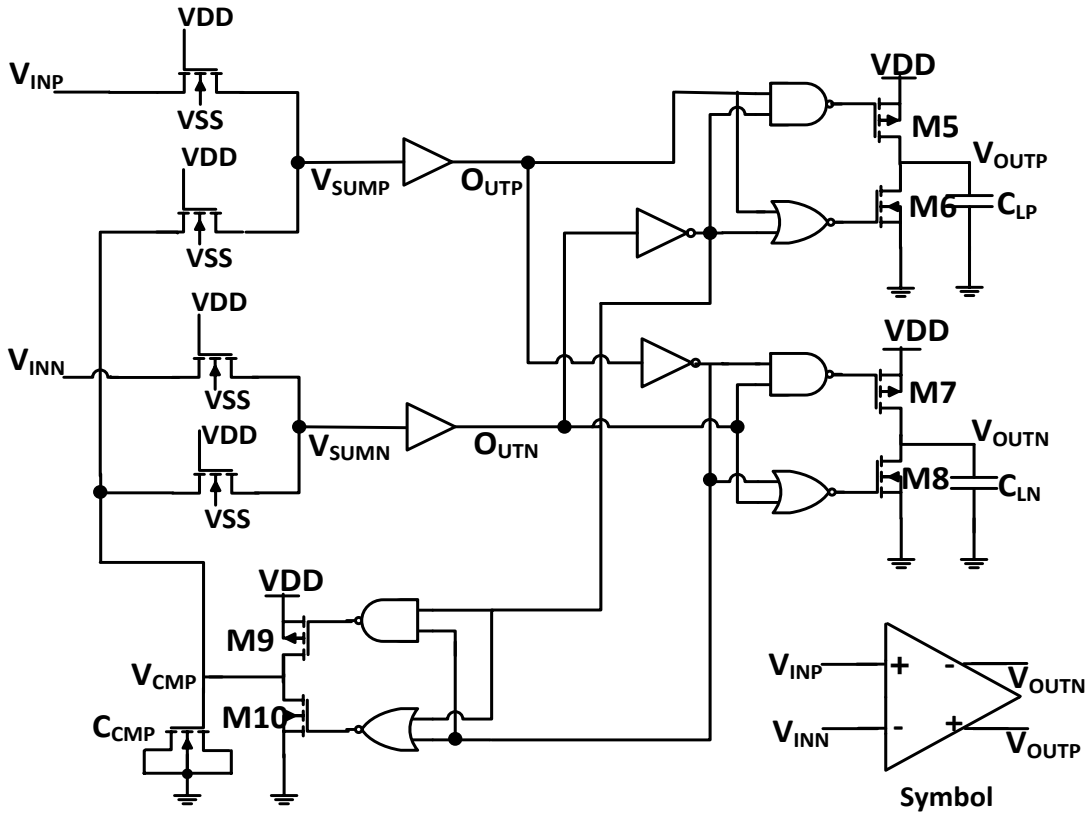


Figure 13. A digital based fully differential voltage comparator circuit

PIPCAP (poly insulator poly capacitor) etc. MOSCAPs are advantageous from digital fabrication point of view.

The circuit diagram of improved comparator is shown in fig. 13. This circuit operates the same as that in fig. 7. Here, V_{INP} and V_{INN} are the external inputs and V_{OUTP} and V_{OUTN} are the final outputs. The feedback block generates V_{CMP} signal which gets added up with the inputs to generate V_{SUMP} and V_{SUMN}. On passing through two buffers, O_{UTP} and O_{UTN} are obtained, which are at two different logic levels. These two voltage signals aid in obtaining final correct outputs.

3.2.2 SIMULATION RESULTS

Based on the model presented above, the proposed voltage comparator has been analyzed in this section, through various simulation results. The proposed voltage comparator was designed and simulated in Cadence® Virtuoso ADE using UMC 180nm CMOS technology.

3.2.2.1 TRANSIENT RESPONSE

To do transient analysis of the comparator in fig. 13, V_{INP} and V_{INN} were set at 900 mV common-mode level (V_{icm}) and at an amplitude (V_p) of 200 mV. Figure 14 shows the transient response of the proposed comparator.

The delay of this comparator was measured to be 8.13 ns. This comparator has an increased delay as compared to that in fig. 7.

Variation in propagation delay [5] of the proposed comparator with change in amplitude of input voltage (V_p) can be observed in fig. 15 where V_{icm} is at 0.9 V. Here too, the delay is reducing with the increase in input voltage amplitude (V_p).

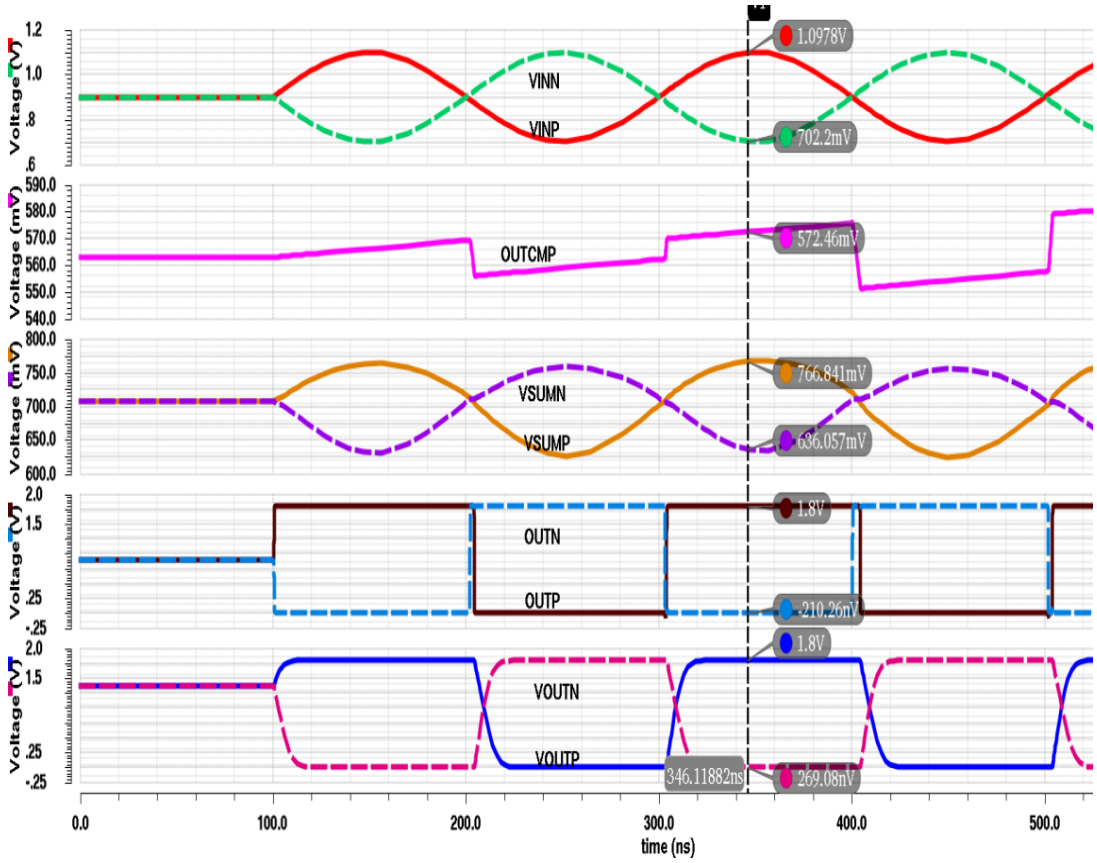


Figure 14. Transient response showing voltages at different nodes in the circuit

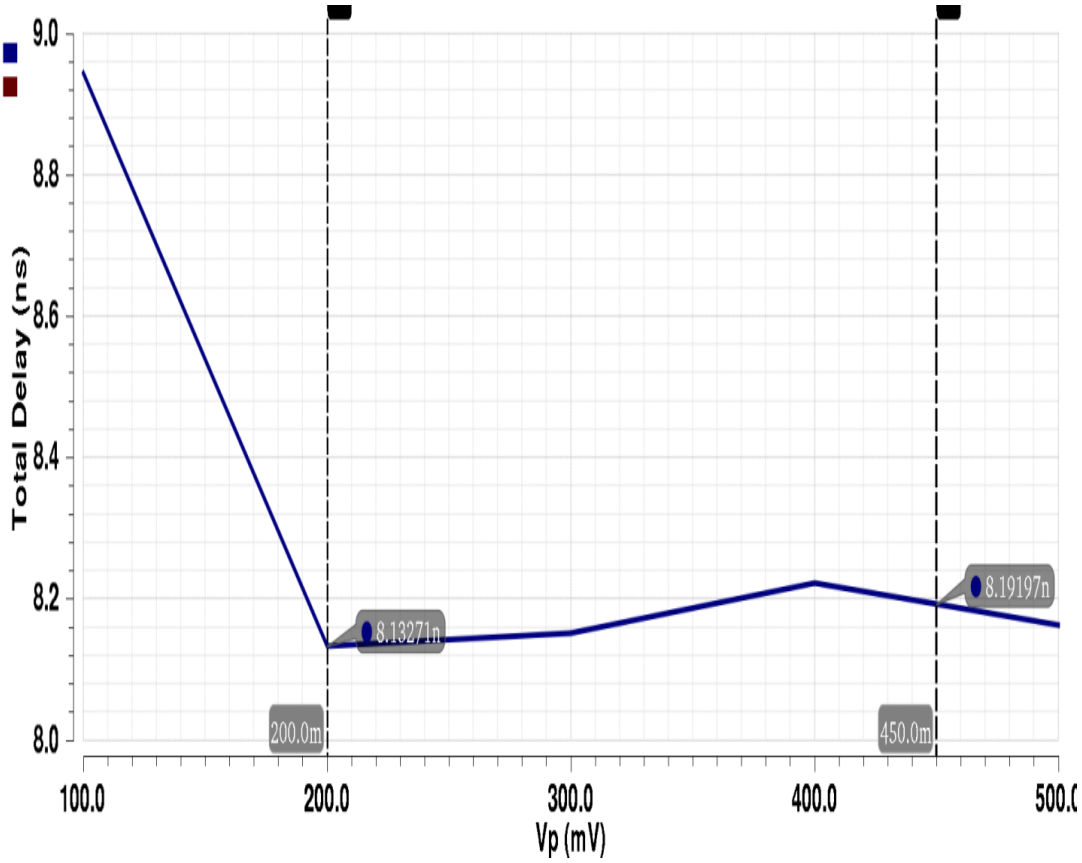


Figure 15. Variation of propagation delay with change in input voltage amplitude(V_p)

3.2.2.2 POWER MEASUREMENT

Average power dissipation of the proposed comparator, shown in fig.13, is 119.5 µW. Figure 16 shows the waveforms of voltage and current signals at various nodes in the proposed comparator. Here too, let the currents that flow through INV1 and INV3 inverters be I1 and I3, and the current that flows through rest of the circuit be I2. At the time instant shown in fig. 16, value of I1 = 18.12 µA and I3 = 16.56 µA. Both these current sum up to be 34.68 µA. Also shown in fig. 16 is the total current of the circuit, I_total, whose value at the same time instant is 36.31 µA. Thus, it has been proved again that most of the circuit's power is consumed by INV1 and INV3. While, the rest of the circuit's current is negligible, most of the time. This circuit consumes less power as compared to that in fig. 7.

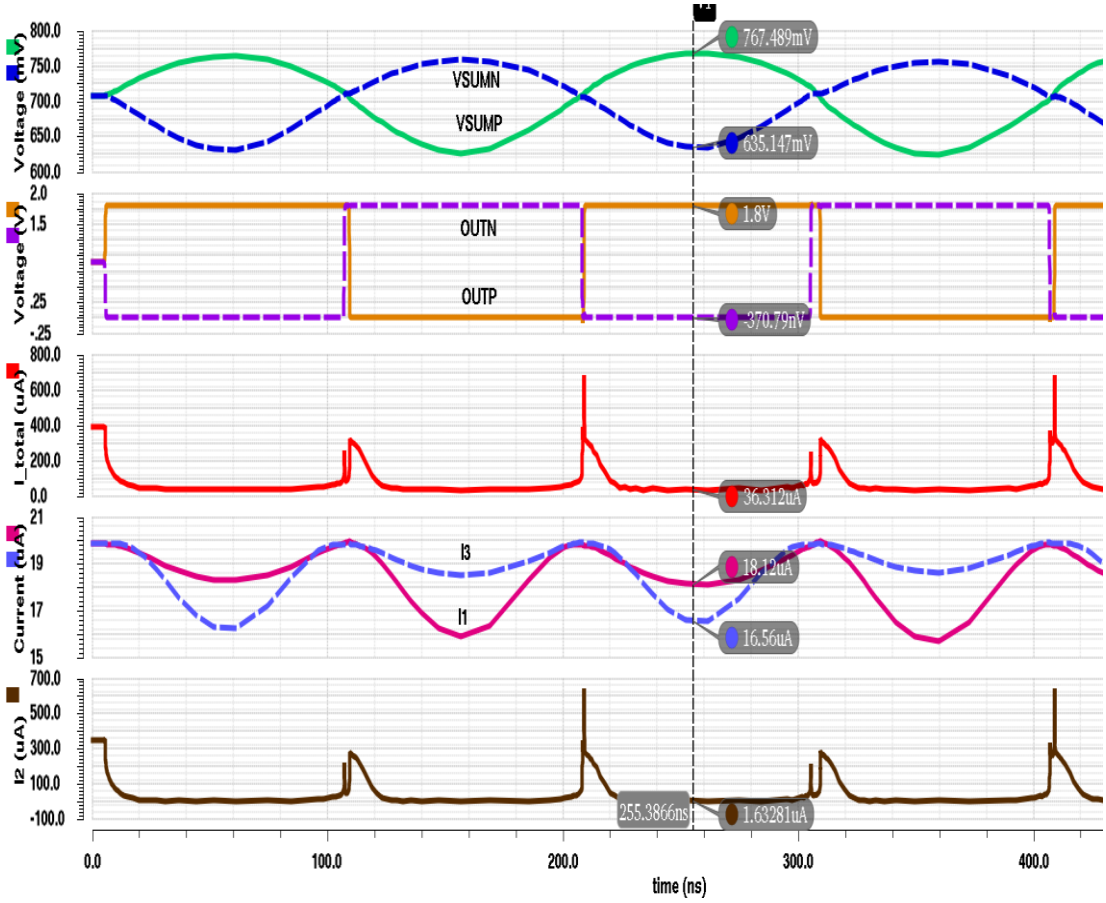


Figure 16. Various voltage and current waveforms

Variation in average power dissipation with the change in common mode voltage (V_{icm}), when input voltage amplitude (V_p) varies from 0.1 V to 0.5 V can be observed in fig. 17. It can be observed that at smaller common-mode voltages, power dissipation is quiet low, but it increases a lot at higher common-mode voltages. This is because of the feedback block which consumes very low power at smaller V_{icm} but its power consumption increases hugely at higher V_{icm}. Also, average power increases with the reduction in V_p as more efforts are required to detect small input difference.

Variation in average power consumed by the comparator as a whole, INV1 inverter and feedback block with the change in V_{icm} can be seen in fig. 18. This too shows that most of the circuit's power dissipation is due to INV1 and INV3 inverters. But, at higher values of V_{icm}, power of feedback block increases rapidly, which affects the average power dissipation of the whole comparator.

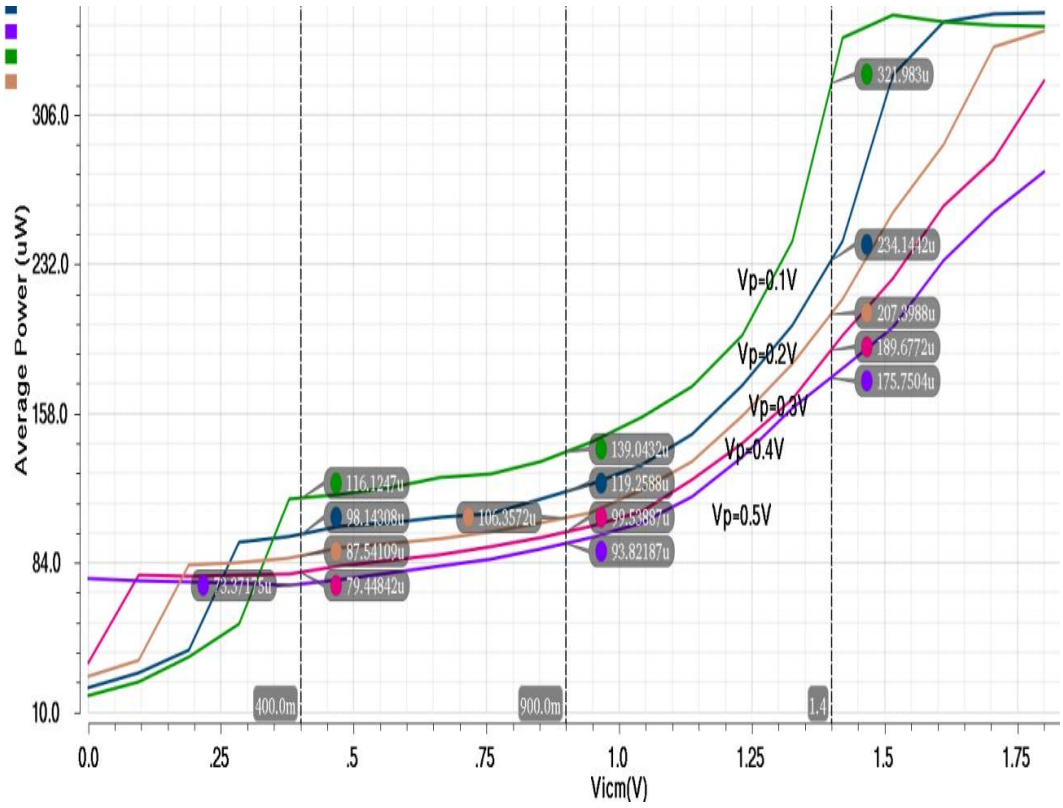


Figure 17. Variation of average power with input common mode voltage (V_{icm})

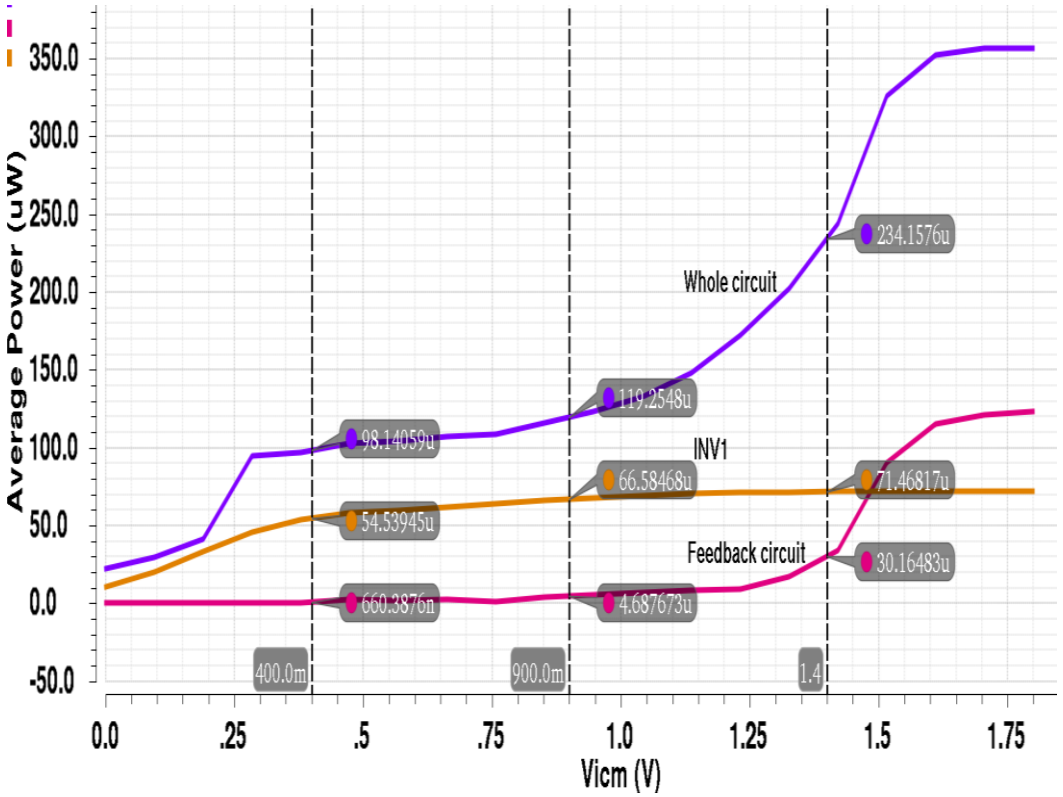


Figure 18. Variation of different power constituents with V_{icm}

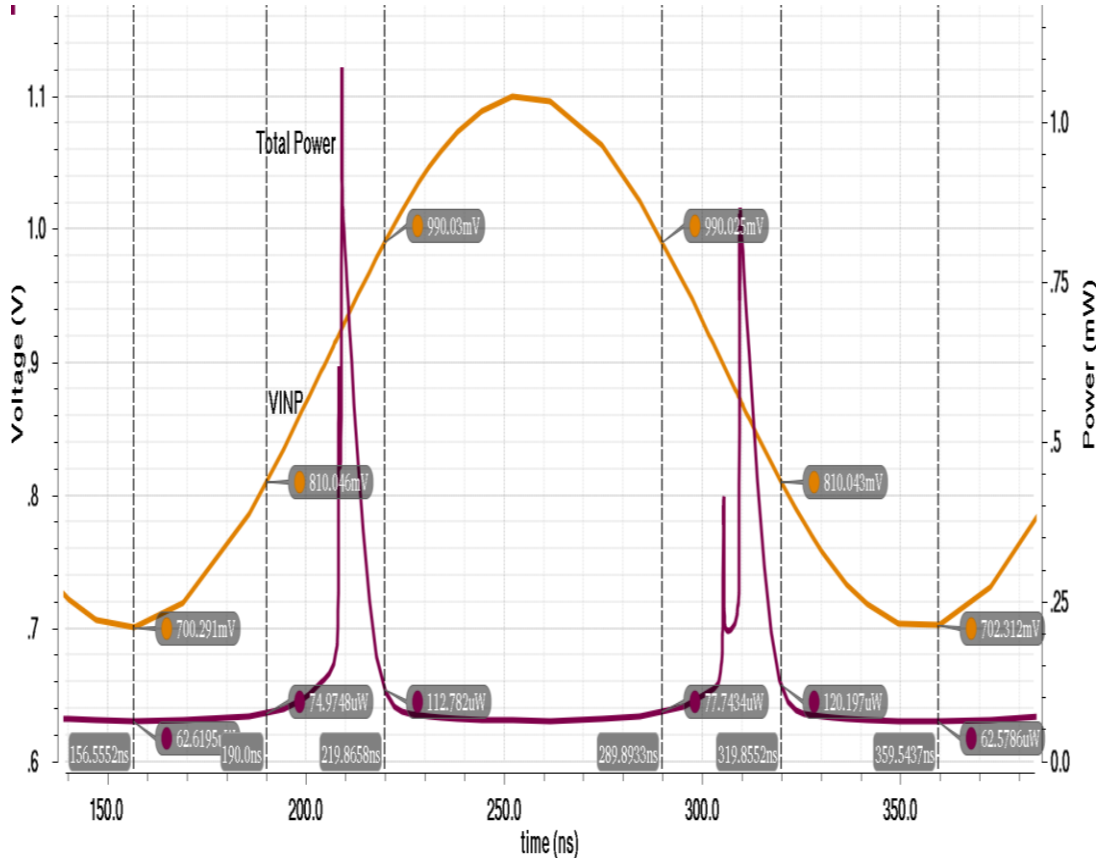


Figure 19. Total power analysis for a cycle of input voltage (V_{INP})

Power dissipation in digital CMOS circuits is mainly due to dynamic component (P_{dyn}), it is apparent from fig. 19. Consider one cycle of input voltage (V_{INP}), where common-mode level (V_{icm}) is 900 mV with V_p having a value of 200 mV, such that V_{INP} lies in the range of 0.7 V to 1.1 V. If V_{INP} is observed for 0.7 V to 0.81 V (i.e. beyond ±10% of V_{icm}) and after 0.99 V too, total power dissipation of the proposed comparator is around 70 µW. This can be termed as static power component as no switching is occurring during these periods. When V_{INP} is in the ±10% of V_{icm} (i.e. 0.81 V to 0.99 V), total power is quite high, which is due to the switching of inputs and intermediate nodes in these periods.

3.2.2.3 DC ANALYSIS

For the DC analysis of the proposed comparator, DC voltage sources were applied at the two inputs, V_{INP} and V_{INN}. A DC sweep was applied at positive input of the comparator,

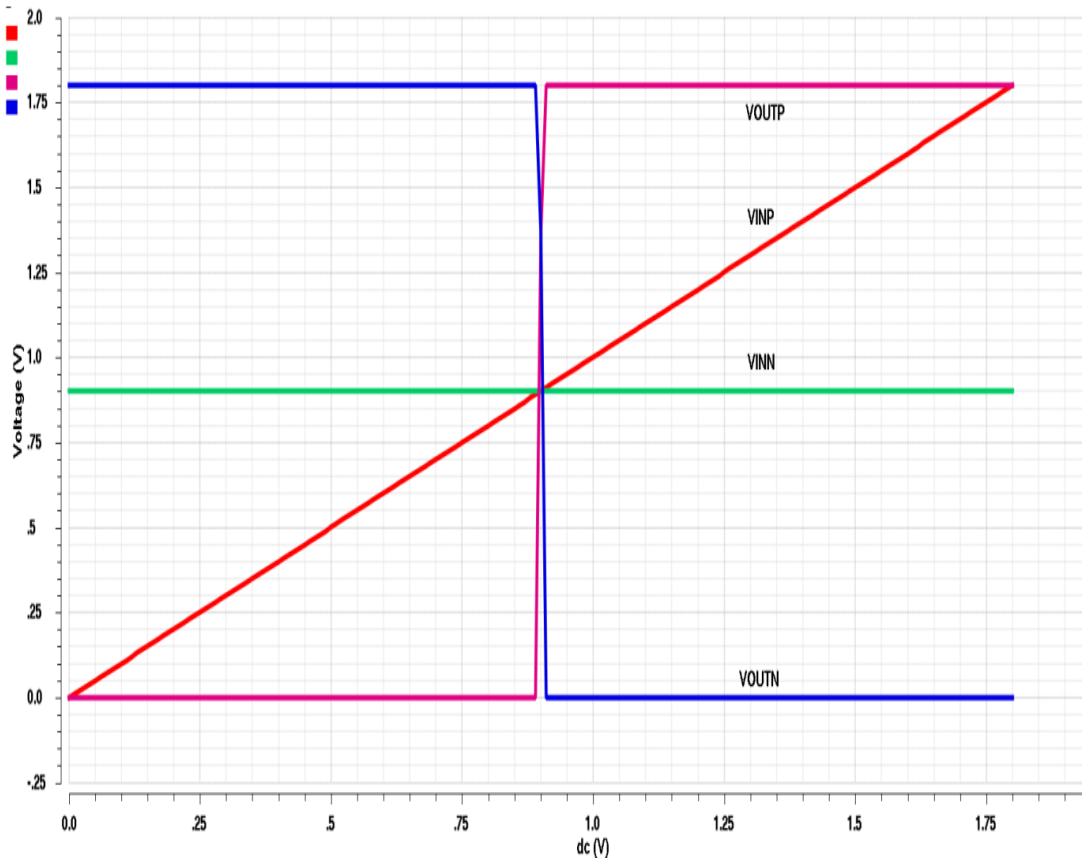


Figure 20. DC analysis plot

and hence a DC transfer curve was obtained as shown in fig. 20. It shows that as V_{INP} rises above V_{INN}, V_{OUTP} reaches to 1.8 V and V_{OUTN} decreases to 0 V.

Here too, 900 mV was applied as DC bias to the input. But, instead of switching at this 900 mV, V_{OUTP} switched at 896.6 mV. This leads to an offset voltage of 3.4 mV. This is shown in fig. 21.

The offset voltage of this comparator is less than that of fig. 7.

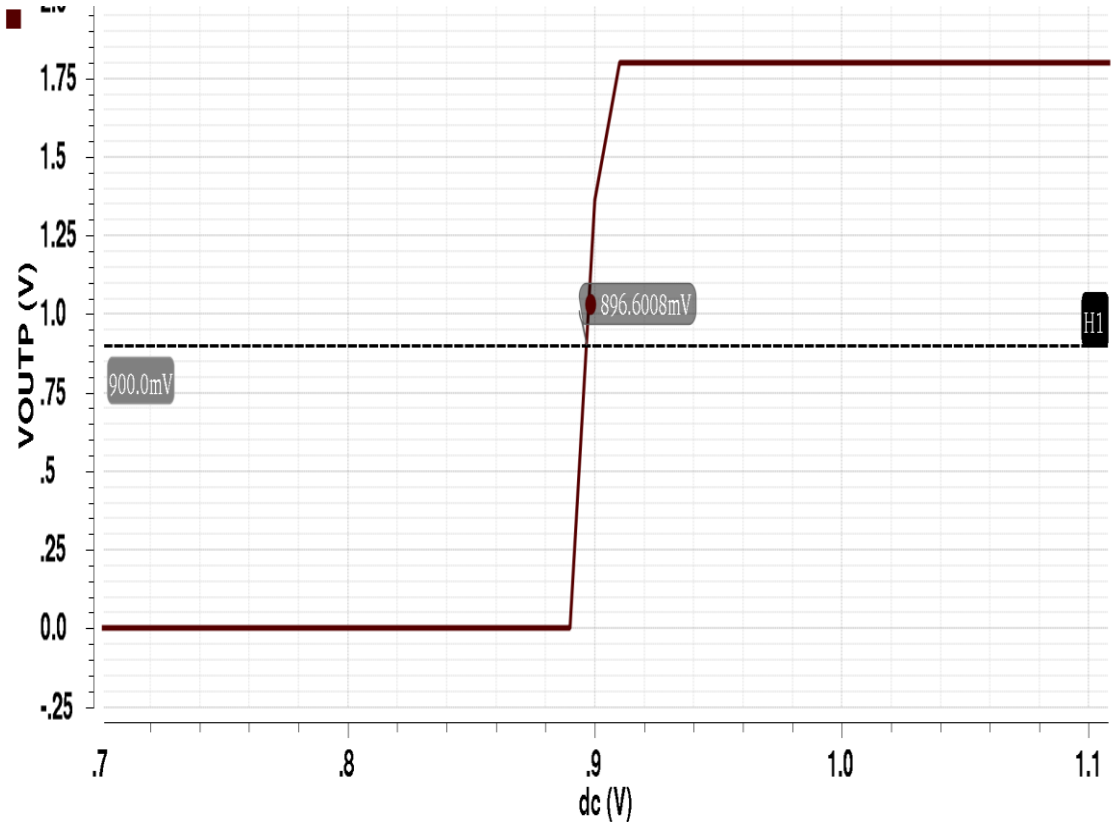


Figure 21. Offset voltage of the proposed comparator

3.2.2.4 PROCESS CORNER VARIATIONS

Corners and design variables have been taken according to the Table 1.

Table 3: Simulation results with process corner variations

Parameters	TT	SS	FF	SF	FS
Propagation Delay (ns)	8.13	11.87	6.46	8.29	8.08
Average Power (µW)	119.5	89.15	162.5	117.4	117.4
Offset Voltage (mV)	3.4	4.93	2.37	4.88	0.629

Thus, the comparator of fig. 13 works at all the corners, as is evident from Table 3. The maximum power at FF corner is more than the typical value, but the variation is not so large as was observed in the case of first proposed comparator. Similar observation holds for minimum power at SS corner and delay values. As far as offset voltage is concerned, it is quite low at FS corner. This is because of the ratioed logic on which output stage is based, wherein PMOS acting slower than NMOS transistor. Thus, in terms of process corner variations, this comparator is better than the one in fig. 7.

3.3 IMPROVED PURELY MOS, DIGITAL-BASED FULLY-DIFFERENTIAL COMPARATOR

The comparator discussed in Section 3.2 had the disadvantage of low ICMR (input common-mode range) i.e. minimum and maximum input CM levels were 0.26 V and 1.5 V. Thus, the comparator couldn't be operated on the full supply range. This caused rapid increase in average power consumption at higher CM levels. Thus, to mitigate that problem, in this section, an improved version of the comparator of fig. 13 has been presented.

In the comparator shown in fig. 13, the summer block has been modified. The pass transistors have been replaced by transmission gates. This comparator was also designed and simulated in Cadence® Virtuoso ADE using UMC 180nm CMOS technology.

The simulation results are as follows:

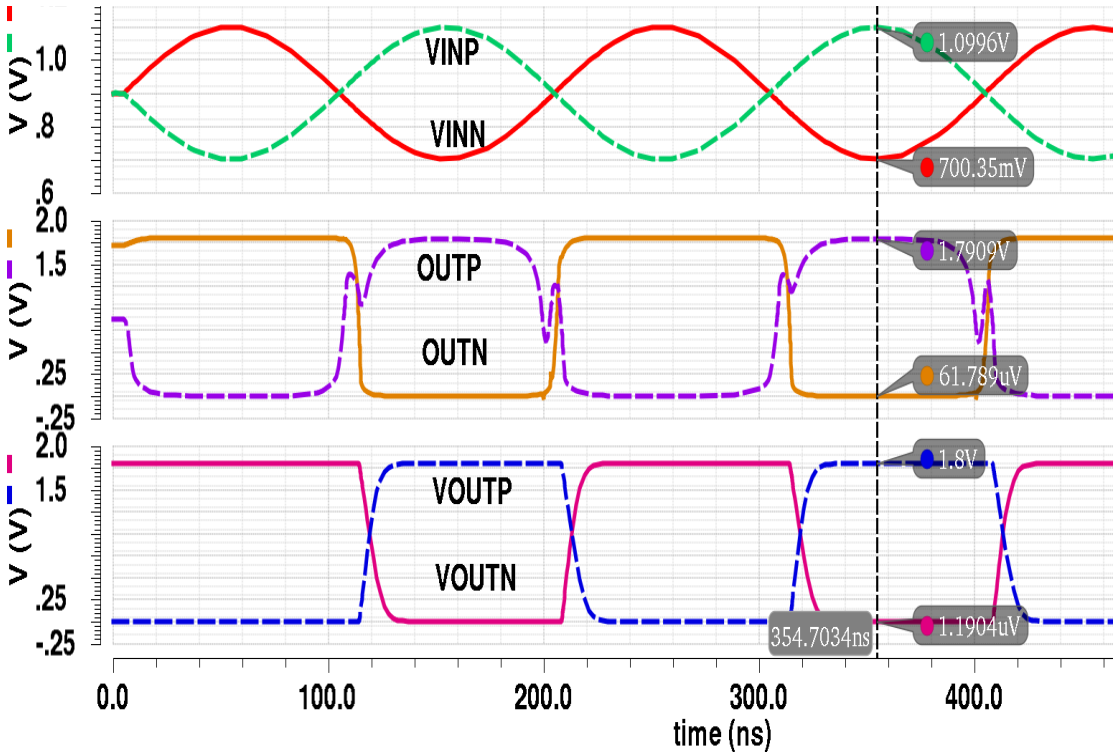


Figure 22. Transient analysis of transmission-gate based comparator

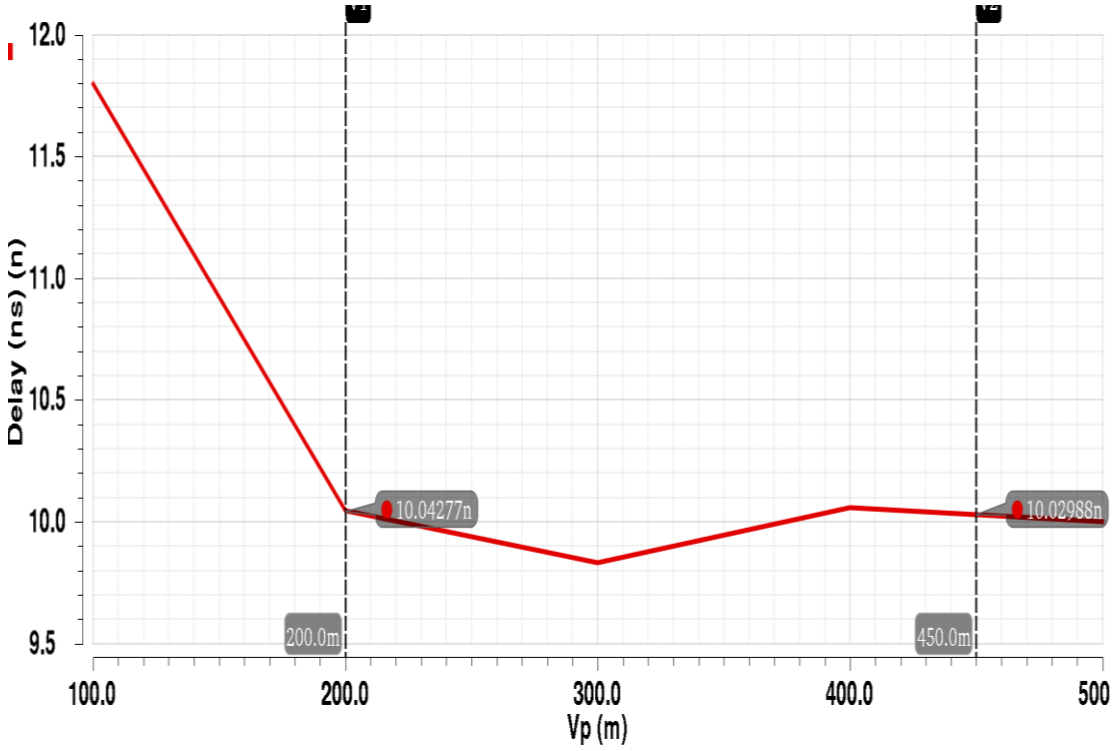


Figure 23. Propagation delay response to change in input amplitude

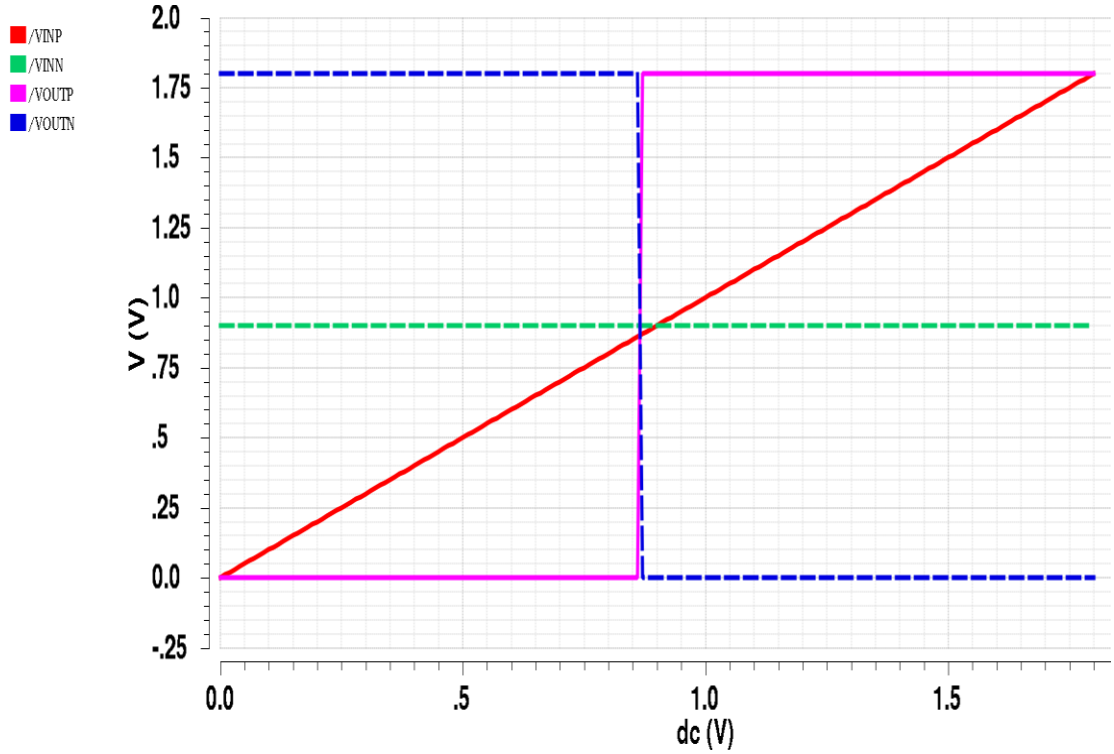


Figure 24. DC analysis of transmission-gate based comparator

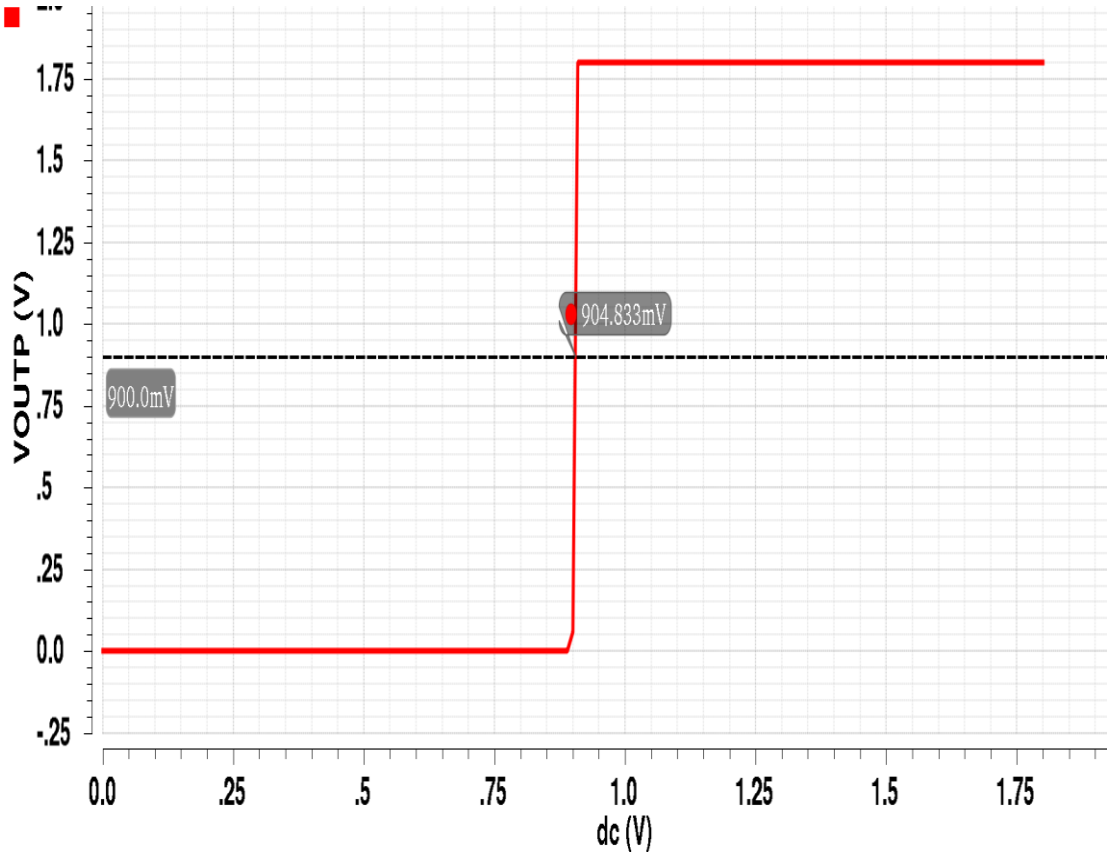


Figure 25. Offset voltage of transmission-gate based comparator

Thus, various parameters of the proposed comparator in this section are:

Offset Voltage : 4.83 mV

Propagation Delay: 10.04 ns

Average Power Dissipation: 126.4 µW

ICMR: Full supply range i.e. upto 1.8 V

4. LAYOUT DESIGN AND POST-LAYOUT SIMULATION RESULTS

In this chapter, layout of the proposed comparator has been presented, whose circuit diagram has been shown in fig. 13 in Chapter 3. The layout was designed at 180 nm technology in Cadence Virtuoso layout editor and DRC/LVS/RCX checks were performed using Cadence Assura.

Once the layout design is over, DRC Run (Design Rule Check) is performed to ensure that the layout design satisfies all the design rules, provided by foundry. Then, LVS Run (Layout versus Schematic) is performed to ensure that all the nets, devices, pins, parameters etc. of layout match properly with the schematic. After LVS, RCX Run (RC Extraction) is performed to obtain RC extracted view of the layout. This view is used to do post-layout simulation.

4.1 LAYOUT DESIGN OF PROPOSED VOLTAGE COMPARATOR

The area occupied by the layout of the proposed comparator is 0.002835 mm^2. The layout comprises of all the digital gates, summer block and the feedback block, loaded by a MOSCAP as shown in fig. 26. Most of the layout's area is consumed by the MOSCAP (40 µm × 36 µm). As all the passive devices like resistors and capacitors have been replaced by MOSFETs, the layout is almost free from mismatches [18]. Another advantage is low chip area coverage because it is known that conventional resistors and capacitors consume a lot of chip area. Besides, the rest of the layout includes digital gates, which means an escape from analog layout. The problems faced in layout design of analog ICs are mismatching and unwanted parasitics.

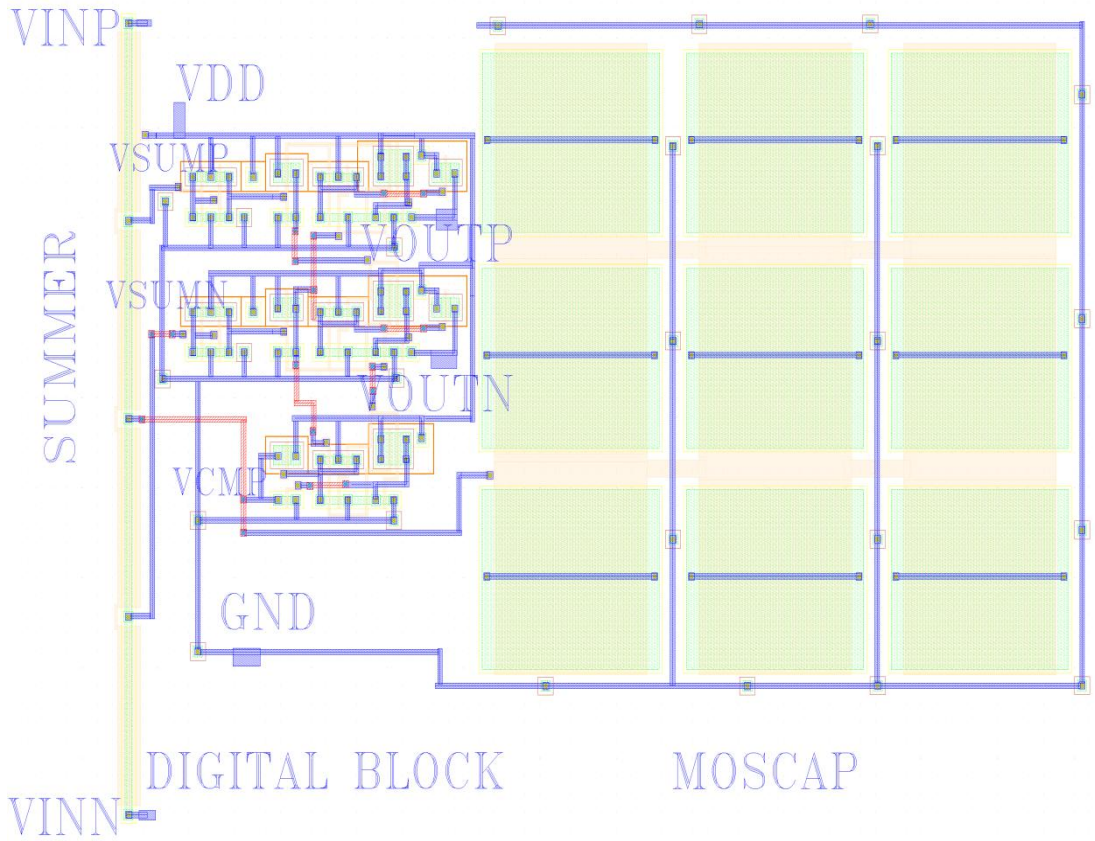


Figure 26. Layout design of proposed voltage comparator

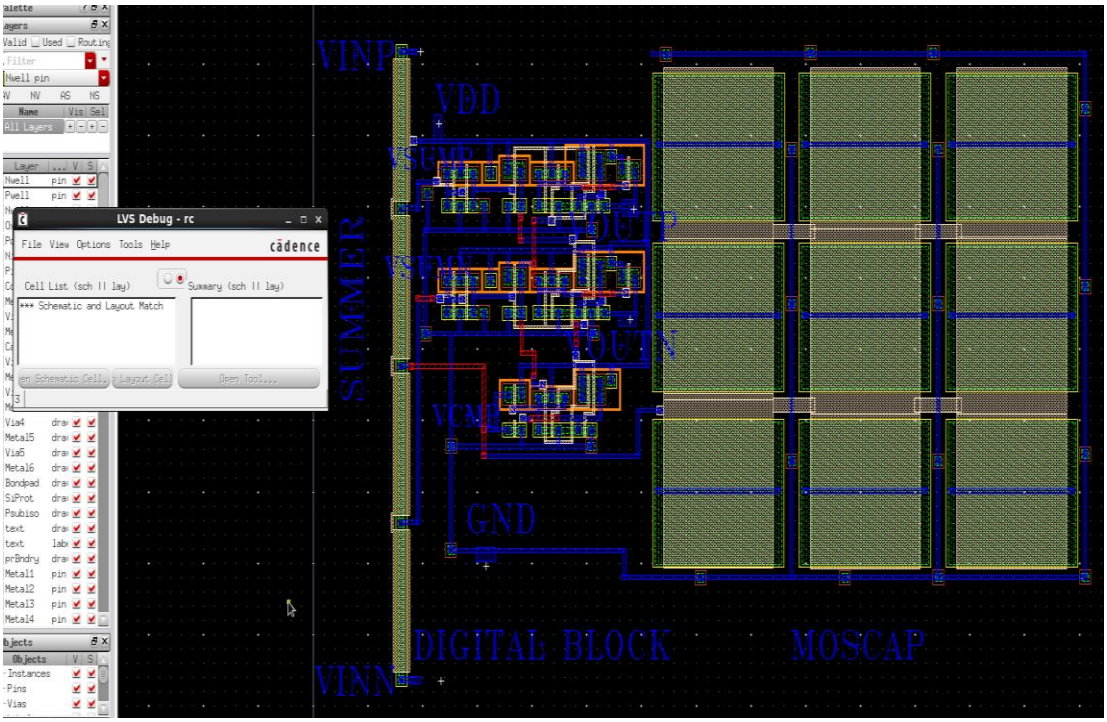


Figure 27. LVS Match

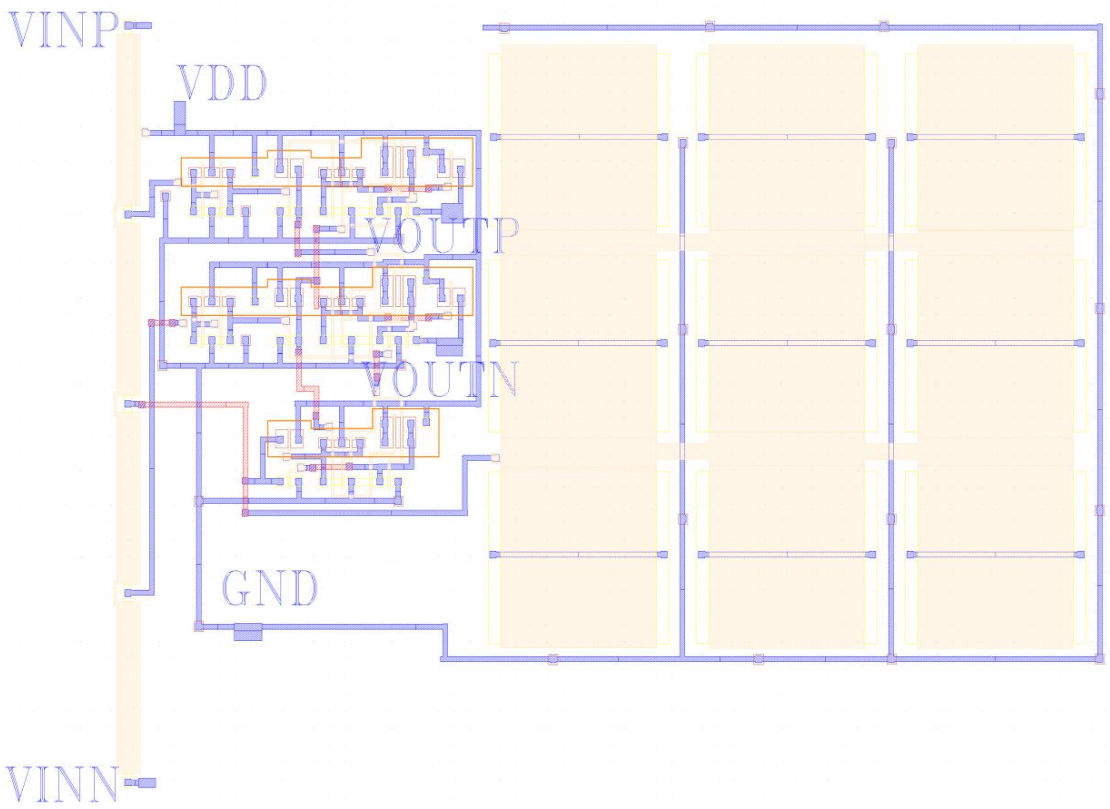


Figure 28. Parasitic Extracted view

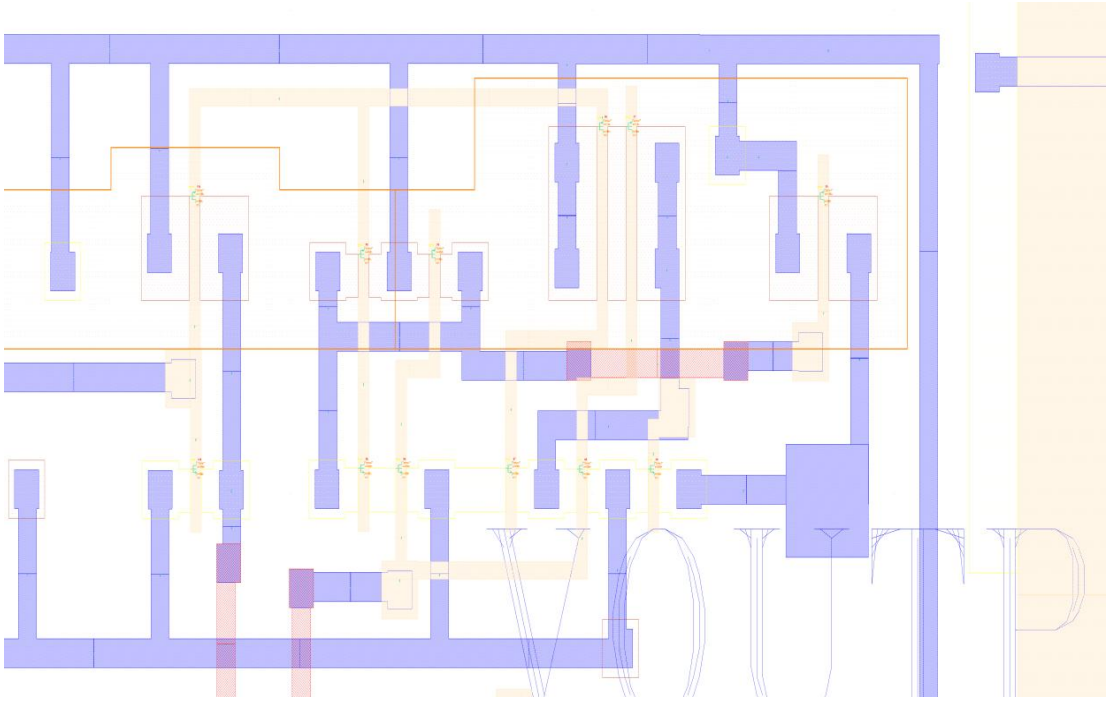


Figure 29. Zoomed view of Parasitic Extracted layout

4.2 POST LAYOUT SIMULATION RESULTS

The simulated results after layout design are shown in fig. 30 and fig. 31. It is clear from fig. 30 that outputs are switching at the middle of the graph at the DC input value of 904.99 mV. Hence, offset obtained is 4.99 mV.

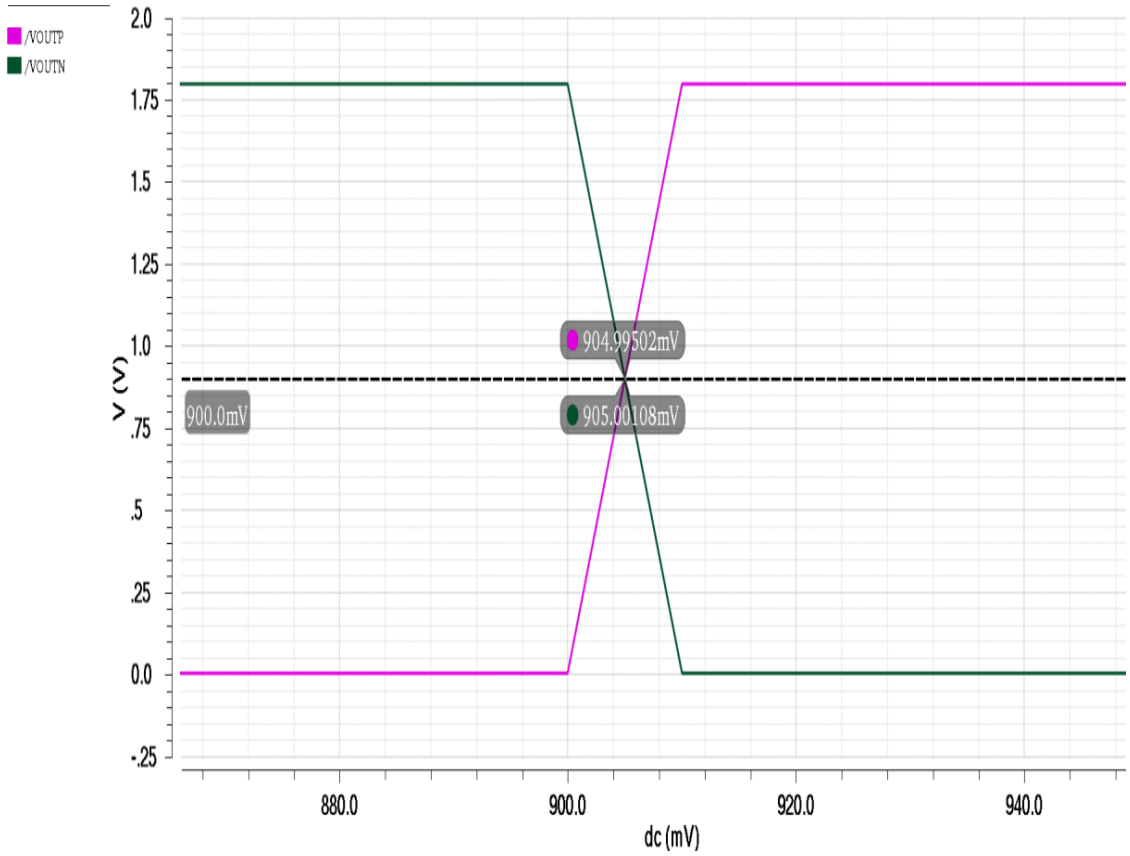


Figure 30. DC analysis plot

Figure 31 shows the transient analysis of the proposed comparator. The output voltages are switching correctly with the switching of input voltages. The spikes can be observed in the waveform nearby switching instants due to the parasitic resistances and capacitances in the layout design.

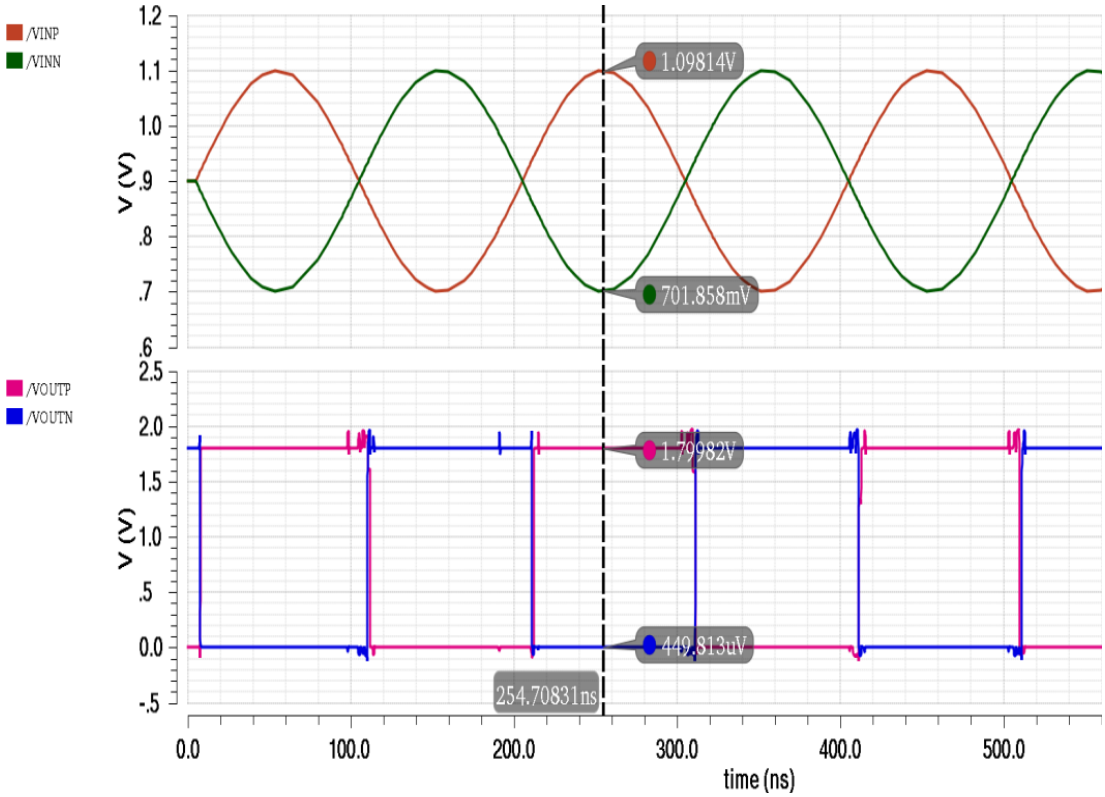


Figure 31. Transient analysis plot

Table 4. Comparison of pre-layout simulation and post-layout simulation of the proposed comparator

Simulation Results	Pre-layout	Post-layout
Average Power (µW)	119.5	174
Propagation Delay (ns)	8.13	8.4
Offset Voltage (mV)	3.4	4.99

5. CONCLUDING REMARKS AND FUTURE SCOPE

An alternative, opamp-less and digital-in-concept implementation technique has been presented to design fully differential voltage comparators. This is highly cost effective as digital-domain design is less tedious and time-consuming as compared to pure analog implementations. The proposed comparators are suitable for SAR ADCs [19], [20], [21], pipeline ADCs [22], low-power ADCs [23], LED driver [24], etc.

Table 5. Comparison of Comparator characteristics

Parameters	**[25]**	**[13]**	**[26]**	**[15]**	**[9]**	**This work 1**	**This work 2**	**This work 3**
CMOS Tech. (µm)	0.5	0.8	0.18	0.18	0.18	0.18	0.18	0.18
Supply vtg (V)	1	5	1.8	1	1.2	1.8	1.8	1.8
Avg. power (µW)		800	158	63.5	329	180.4	119.5	126.4
Offset vtg. (mV)	-	77.3	-	0.0476	7.8	4.9	3.4	4.83
Delay	4µs	17.3ns	0.4ns	26ns	550ps	5.7ns	8.13ns	10.04
Design Meth-od	Analog	Clocked with a SC-network	I-mode second generati-on current conveyor	Analog latched; input stage-flipped voltage follower	Latched double-tail	Digital	Digital	Digital

Table 5 shows that the proposed comparators have comparable values of all the parameters. The comparators were simulated for the load capacitance of 1pF. They provide good trade-off between power dissipation and delay. Being digital based, the proposed comparators can be further designed for low power applications, in scaled CMOS technologies, unlike the analog comparators where supply voltage scaling degrades the performance.

6. REFERENCES

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