PERFORMANCE ANALYSIS OF MULTI WALLED CARBON NANOTUBE (MWCNT) BUNDLE AS VLSI INTERCONNECTS

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In

VLSI Design

Submitted by

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DECLARATION

I hereby declare that the work which is being presented in the thesis entitled, **"Performance Analysis of Multi Wall Carbon Nanotube (MWCNT) bundle as VLSI interconnects"** in partial fulfilment of the requirement for the award of degree of M.Tech. (VLSI Design) at Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Dr. Mayank Kumar Rai, Assistant Professor, ECED.

The matter presented in this thesis has not been submitted in any other University/ Institute for the award of my degree.

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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ABSTRACT

The development of VLSI technology is rapidly advancing into deep submicron domain due to reduction in feature sizes and bringing complexity at the silicon level. As a result, logic components in a microprocessor have shown dramatic performance improvement. On the other hand, on-chip interconnect designing is an increasing gridlock in nanometer-scale VLSI design which is dominating the gate delay. Currently, copper is used as a VLSI interconnects material.

As technology scales down, its performance degrades due to various factors such as electro migration, surface scattering and grain boundary scattering. Carbon nanotubes have been preferred as substitute for the future nodes due to their special physical characteristics. They provide high thermal and mechanical stability and have large current carrying capacity over copper. In this dissertation, temperature dependent performance analysis of MWCNT bundle as VLSI interconnects has been analyzed. The average improvement in delay, power and PDP using thermally aware model of CNT bundle and copper interconnect in comparison with temperature independent model is compared. The temperature dependent circuit parameters and performance analysis in terms of delay, power dissipation and power delay product (PDP) of single walled carbon nanotube (SWCNT) bundle interconnect and multi walled carbon nanotube (MWCNT) bundle interconnect have been analyzed using temperature dependent equivalent circuit model. Results obtained through these analyses at 22nm technology node over a temperature range from 300K to 450K are compared with conventional metal (copper) interconnect. The effects of various parameters such as interconnect length on propagation delay, power and PDP have also been analyzed. The SPICE simulation results reveal that at temperature variation ranging from 300K to 450K, compared to bundle of CNT with copper interconnects, delay in CNT bundle is low at different interconnect lengths ranging from 100um to 1000um whereas reverse is true for power dissipation. Simulated results also reveal that with rise in temperature, MWCNT bundle has less delay as compared with SWCNT bundle for global level (> 700μm) of interconnect lengths and vice versa for local level (≥100μm) of interconnects. However, with rise in temperature, MWCNT bundle dissipates less power than SWCNT bundle for all interconnect lengths. Based on simulation results, the thermally aware model of SWCNT bundle achieved improvement in delay, power and PDP estimation accuracy whereas reverse is true for

MWCNT bundle. Based on these comparative results, the temperature dependent SWCNT bundle is an encouraging alternative to MWCNT bundle and copper interconnect.

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ABBREVIATIONS

AR	Aspect Ratio
AC	Acoustic Phonon
IC	Integrated Circuit
DC	Direct Current
DWCNT	Double Wall Carbon Nanotube
CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nano Tube
EM	Electro-Magnetism
FET	Field Effect Transistor
GHz	Giga Hertz
MFP	Mean Free Path
MWCNT	Multi Wall Carbon Nanotube
OP	Optical Phonon
PDP	Power Delay Product
RC	Resistance-Capacitance
RLC	Resistance-Inductance-Capacitance
SiO_2	Silicon dioxide
SPICE	Simulation Program with Integrated Circuit Emphasis
SWCNT	Single Wall Carbon Nanotube
TCR	Temperature Coefficient of Resistance
VLSI	Very Large Scale Integration

CHAPTER 1

INTRODUCTION

1.1 Introduction

The continuous growth in the enlargement of the technology is due to the scaling in the feature size of device. On the other hand, the length of interconnects is increasing frequently as die size is also expanding. Therefore, their packaging is going to be complicated. On scaling down the technology, the functioning of conventional interconnect i.e. copper is reducing rapidly due to degradation in the properties of copper. Almost 60% of degradation in the VLSI design circuits is due to interconnect performance in terms of delay, power and power delay product (PDP). Therefore, these performances have to be accounted for the designing process of the systems, failing to which causes glitches in digital domain and attenuation in analog circuits, results in failure of the device. Thus it is immensely important to search a potential candidate for VLSI interconnects. This calls for the carbon nanotubes (CNT) as interconnects. At deep submicron level CNT shows the outstanding performance in terms of delay, power as compared to copper. Therefore, it is necessary to study the behaviour of CNT as interconnect.

1.2 Statement of problems

The objectives of proposed work in the thesis are briefly as follows:

1) Development of temperature dependent impedance parameter of Multi Walled Carbon Nanotubes (MWCNT) bundles based interconnects.
2) Study the effect of tube length on delay and power dissipation in MWCNT bundle interconnects at 22nm technology.
3) Study the effect of temperature variation on delay, power and PDP analysis in MWCNT bundle interconnects.
4) Comparison of the results obtained from the above analysis with the results for Single Walled Carbon Nanotube (SWCNT) bundle and Copper interconnects at 22nm technology.
5) Comparison between temperature dependent and independent analysis of performance of SWCNT bundle and MWCNT bundle at 22nm technology.

1.3 Organisation of thesis

In **Chapter 2**, initiating with interconnect, problems with existing material of VLSI interconnect is explained. Further, CNT as VLSI interconnects is described and categorized on different criteria. Broadly CNT are divided in two types: SWCNT bundle and MWCNT bundle which are explained in detail. Literature review of performance analysis of isolated CNT is explained on the basis of tube parameters, delay and power. Moreover temperature dependent crosstalk analysis of SWCNT is also explained in last section of the chapter.

In **Chapter 3**, Influence of length of interconnects on delay, power and power delay product (PDP) of CNT bundle interconnects is mainly focused and analysed. Distributed RLC circuit model is used to model the interconnect circuit. Spice simulation results of CNT bundle are calculated and compared with the copper interconnect.

In **Chapter 4**, Temperature dependent impedance model of SWCNT bundle and copper is formed. Also the performance analysis on the basis of delay, power and PDP is carried out for different interconnect length at different temperature and results are compared with copper interconnect. In the last section of the chapter temperature dependent model of SWCNT bundle is compared with temperature independent model.

In **Chapter 5**, Temperature dependent impedance model of MWCNT bundle is formed. Also the performance analysis of SWCNT bundle and MWCNT bundle is compared at different temperature for different interconnect lengths. Finally temperature dependent model of MWCNT bundle is compared with the temperature independent model of MWCNT bundle.

In **Chapter 6**, Conclusion of the entire dissertation in serial order and future work is explained.

CHAPTER 2

Literature Review

2.1 Introduction

With the emergence of aggressive technology scaling, performance of integrated circuits (ICs) degrades due to the significant downfall of performance of interconnects on the basis of delay, dissipation power and power delay product (PDP). As the feature size of device reduces, it is observed that the temperature of interconnects based on conventional material (copper) increases due to the combined effect of increase in resistivity of metal and current density [1]. So, if CNT bundles are to be enrolled in integrated circuit application it is required to study their electrical characteristics on varying the temperature above room temperature. The equivalent model of various CNTs has been derived by the scientist. Various impedance parameters of different CNTs are calculated for the accurate estimation of propagation delay and power and has been compared with the propagation delay of copper interconnects and each other as well. Dependence of various parameters such as diameter's effect has been studied on propagation delay and power dissipation. Electro-thermal study of metallic SWCNT has been analyzed for the first time. Also, the study of temperature dependent crosstalk analysis in SWCNT bundle interconnects has been done.

2.2 Interconnects

Interconnect is a conducting material that provides physical as well as electrical connection between two subsystems of the circuit formed in the integrated circuits. Interconnection can be used to provide power supply, clock, and ground supply to a device and also to provide the output of one device to another device. As CMOS technology is scaling down, it improves the performance of device by consuming less power and increases density of transistor. Although the on-chip processing is getting faster but interconnects is causing hindrance in circuit behaviour. This is due to the problems arises, with technology scaling, in the conventional material (copper) used as interconnects.[1-4] A disadvantage with copper is that for submicron current

density electro migration, surface scattering and grain boundary effects dominates due to which it degrades the performance of the interconnect. The physical parameters on which reliability of interconnect depends are cross sectional area, pitch, aspect ratio etc dictates that the parameter are distributed to make interconnect an acceptable transmission line. When cross section of copper interconnect reduces, the surface of interconnect becomes rough and it causes increase in resistance resulting in large propagation delay and power dissipation. Thus the performance of copper as interconnect degrades. This calls for the alternative solution for future generation devices. Carbon Nanotubes (CNTs) have inspired a lot of research interest in their applicability as very large scale integration (VLSI) interconnects of the future [2]. CNTs are divided into two parts Single wall CNTs (SWCNT) and Multi wall CNTs (MWCNT). SWCNT is made up of only one thin wall of graphene sheet and MWCNT is made up of multiple concentric SWCNT like graphene tubes.

2.3 Problems with existing materials of VLSI interconnect

There is a trade off between feature size and die size due to which results in large no of increase in length of on chip interconnects as technology scaling pursues. Before copper, frequently used material for interconnects was aluminium because it has good conductivity and adherence on silicon dioxide. Moreover it forms good ohmic contact with silicon. But aluminium has a lot of disadvantage such as at high current densities electro migration and hot carrier effects takes place on a large scale. The formation of electro migration damages the wire and creates voids in the conductor as tolerance power of wire gets degrades. The generation of hot carriers effect in aluminium used as interconnect reduces the lifetime of a system. Thus the performance of aluminium degrades as the current density increases frequently. After aluminium, copper came into picture having better physical and thermal properties than aluminium used as interconnects.

Copper has higher conductivity than aluminium and it can fight with electro migration as it has ten to hundred times' higher resistivity to electro migration failures than aluminium. Due to lower resistivity of copper interconnect, it decreases interconnect RC delay which ultimately increases the integrated circuit speed. Copper has higher thermal stability than aluminium because melting point of copper is higher than aluminium. [5]. Due to these advantages the transition to copper as a interconnect

material is one of the most significant changes for sub-micron and deep sub-micron high performance chips. As the technology is further scaled, the cross-sectional area of copper interconnects decreases appreciably due to which effects like surface roughness and grain boundary scattering become significant leading to increased resistivity. This causes increase in propagation delay, power dissipation and electro migration [2].

Thus, as technology scale, the major issues on which performance of interconnect depend are delay, crosstalk, power, reliability in terms of grain boundary scattering, electro migrations, diffusion barrier width and last but not the least is surface scattering are discussed below:

a) **Delay:** Delay plays a crucial role in the performance of the integrated devices as 60%-70% delay in the system is due to interconnect which deteriorate the results of the circuits. On scaling down the technology, long interconnects are used for connecting IP cores because delay does not scale with gate delay.
b) **Power:** The power of interconnect depends on its capacitance which is needed to be considered carefully for total switching power of device.
c) **Crosstalk:** Crosstalk in interconnects causes logic failure due to some glitches, timing errors and noise in the wire [6]. Both capacitive and inductive crosstalk affects the signal activity which needs to be taken care off.
d) **Reliability:** As technology scales, interconnect reliability due to electro migration, grain boundary scattering, surface scattering and diffusion barrier width is becoming a serious issue [7, 8].

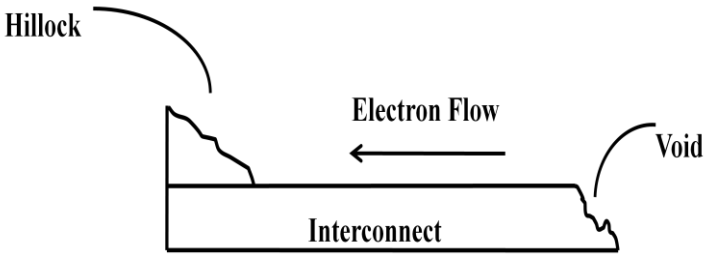

Figure 2.1 Electromigration leads to void.

- **Electro migration** Electro migration is defined as the transport of material in metals under an applied current density and is widely regarded as a major wear-out or failure mechanism of VLSI interconnects as shown in Fig.2.1. When current flows through the interconnect metal, an electronic wind is set up opposite to the direction of current flow. These electrons, upon colliding with the metal ions, impart sufficient

momentum and displace the metal ions from their lattice sites, creating vacancies. These vacancies condense to form voids that result in increase of interconnect resistance or even open-circuit conditions [9, 10].

- **Surface and Grain Boundary Scattering:** Due to reduction in size of interconnects the contribution of surface and grain-boundary scattering to resistivity of interconnect have been subject of research. At deep submicron length of electron mean free path is nearly comparable to the dimension of wire which results in surface scattering due to which mobility of electrons decreases. Grain boundary is defined as interface where crystals of different orientations meet as shown in Fig. 2.2. Copper has a crystalline structure but when they are used as interconnect material they become polycrystalline in nature leading to grain boundaries [11]. Electron scattering caused by grain boundary causes reduction in mobility of electrons. The grain phenomena is inversely proportional to resistance i.e. if grain is smaller resistance will be large which causes obstacle in the flow of electron through interconnect. Thus , it is necessary to tacle both these scattering phenomena.

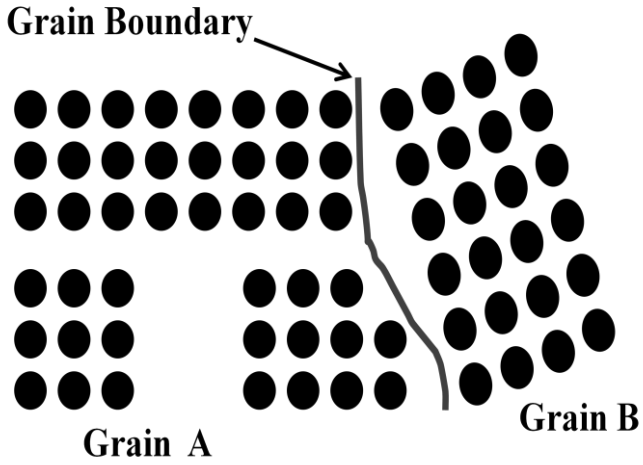

Figure 2.2 Grain Boundary Interfaces

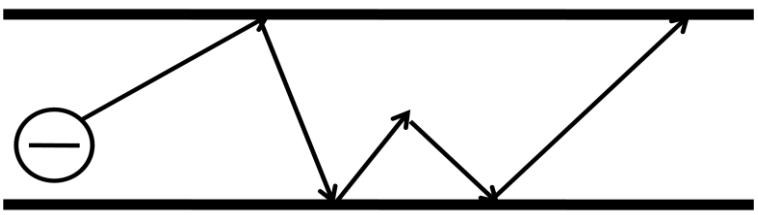

Figure 2.3 Surface Scattering

- **Diffusion Barrier Width:** Due to the mobile nature of SiO_2, copper diffuses into adjacent dielectric silicon. It causes contamination of silicon devices. To alleviate this problem, copper wires are surrounded by a diffusion barrier [12]. Due to the high resistivity of this diffusion barrier, the effective resistivity of the copper wire increases. With the scaling of technology, the cross sectional area of copper wire decreases, but due to reliability constraints the diffusion barrier does not scales as rapidly.

It is observed that with the advent of deep-submicron technology nodes there are several disadvantages in copper as described above. Thus, a potential candidate for interconnect material that is compatible with lower technologies is required. This potential candidate is CNT.

2.4 Carbon Nanotube

There are two crystalline forms in solid carbon i.e. sp^3 hybridized diamond and sp^2 hybridized graphite. Carbon acts as an insulator in its diamond form with a huge energy gap, whereas in graphite form it accumulates into a one-atom thick graphene sheet. These isolated graphene sheets are rolled up in the form of hollow cylinder are called as CNT as shown in Fig. 2.4. Its name is derived from its size because it has a diameter in the range of nanometer. CNT can also be defined as tapered sheets of a million of carbon atoms joined together in the hexagonal pattern as formed in graphite are wrapped in to form tubes having diameter of about 1-2nm.

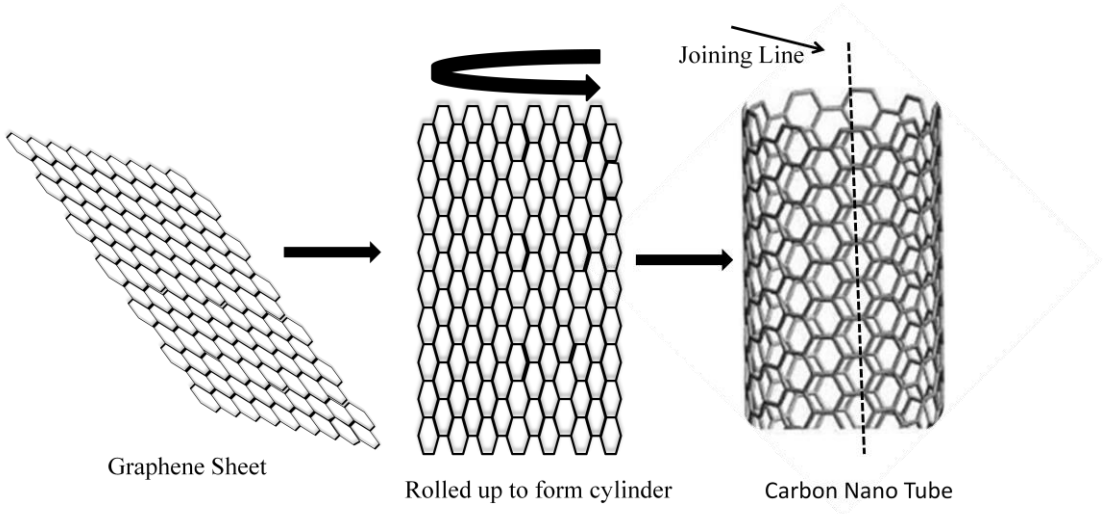

Figure 2.4 Formation of CNT from graphene sheet.

CNT constitute amazing mechanical, structural, electrical and thermal properties that are extracted from the outstanding properties of carbon bonds, their cylindrical symmetry and distinctive quasi 1D nature. All these properties of CNT vary by following different diameter, length and direction of twist of the nanotube. For example, carbon nanotubes are highly conductive both to electricity and heat - they exhibit an electrical conductivity higher than copper and thermal conductivity greater than diamond.

To encapsulate all the properties below in the table 2.1 are a collection of results studied from scientist all over world. All values are for SWCNT unless otherwise stated.

TABLE 2.1 Electrical, Optical and Thermal properties of CNT [13-18]

Equilibrium Structure	
Average Diameter of SWCNT	1.2-1.4nm
Distance from opposite carbon atoms	2.83Aº
Parallel Carbon Bond Separation	2.45Aº
Analogous Carbon Atom Separation	2.456Aº
Carbon Bond Length	1.42Aº
C-C Tight Bonding Overlap Energy	~2.5eV
Lattice Parameter	
Armchair (10,10)	16.78Aº
Chiral (12,6)	16.52Aº
Zigzag (17,0)	16.52Aº
Optical Properties	
Fundamental gap for metallic	0eV
Fundamental gap for semiconducting	~0.5eV
Electrical Transport	
Conductance Quantization	$n(12.9k\Omega)^{-1}$
Resistivity	$10^{-4}\Omega$-cm
Maximum Current Density	$10^{13}A/m^2$
Thermal Properties	
Thermal Conductivity	~2000W/m/K
Phonon Mean Free Path	~100nm
Relaxation Time	$\sim10^{-11}$ s

Due to quantum confinement of electrons in CNT, its structure strongly affects the electrical properties. Around the circumference of the nanotube, periodic boundary conditions come into play. For example, if a zigzag or armchair nanotube has 10 hexagons around its circumference, the 11th hexagon will coincide with the first. Going around the cylinder once introduces a phase difference of 2π.

Because of the quantum confinement, electrons can only propagate along the nanotube axis, and so their wave vectors point in this direction. The resulting number of one-dimensional conduction and valence bands effectively depends on the standing waves that are set up around the circumference of the nanotube. All nanotubes are expected to be very good thermal conductors along the tube, exhibiting a property known as ballistic conduction, but good insulators laterally to the tube axis. Prior to Carbon nanotubes, diamond was the best thermal conductor.

Carbon nanotubes have now been shown to have a thermal conductivity at least twice that of diamond. The high-frequency carbon-carbon bond vibrations provide an intrinsic thermal conductivity higher than even diamond. Unlike bulk diamond, however, whose thermal conductivity is the same in all directions; buckytubes conduct heat far better down the tube axis than sideways from tube to tube.

2.5 Types of CNT

CNTs are mainly classified in two categories: SWCNT and MWCNT whereas they are also divided on the basis of different phenomena like on the basis of chirality they are divided in three categories i.e. armchair, zigzag and chiral; on the basis of conductivity they are divided in two categories i.e. metallic and semiconducting.

- **On the basis of structure**

  There are two types of CNTs: SWCNT and MWCNT as shown in Fig. 2.5. SWCNT is defined as a single sheet of graphene wrapped into tube. They are forms when 2-D graphene sheet of certain size is rolled in a certain direction depending upon chirality. SWCNTs have only single coating of graphene sheet with diameter of 0.7 to 10nm [19]. MWCNT is defined as more than one layer of graphene sheets are rolled up keeping the center of all the sheets same. Each layer in MWCNT is known as shells. The adjacent shells are held each other by vander Waal forces having distance of 3.4A^{o}.

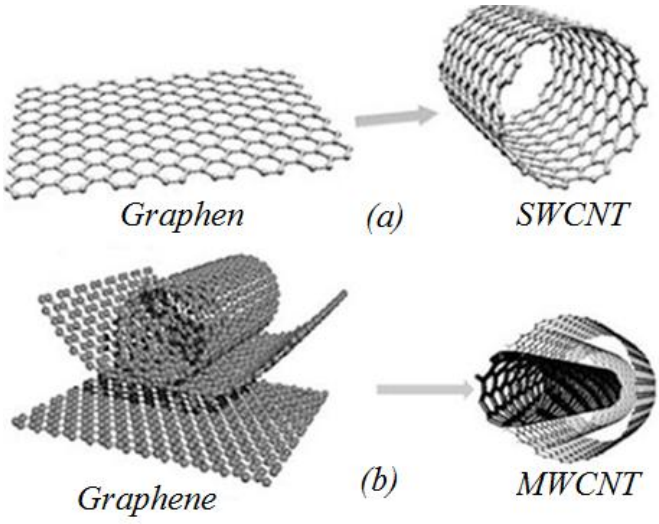

Figure 2.5 Structure of (a) SWCNT (b) MWCNT [19].

- **On the basis of chirality**

The orientation for rolling the graphene sheet to form CNTs is represented by a pair of indices (n, m) called the chiral vector where n and m are number of unit vectors along two directions in the honeycomb crystal lattice of graphene. The vector perpendicular to the nanotube axis is called chiral vector (C_h) and the vector parallel to the axis is called translational vector (T) as shown in Fig. 2.6.

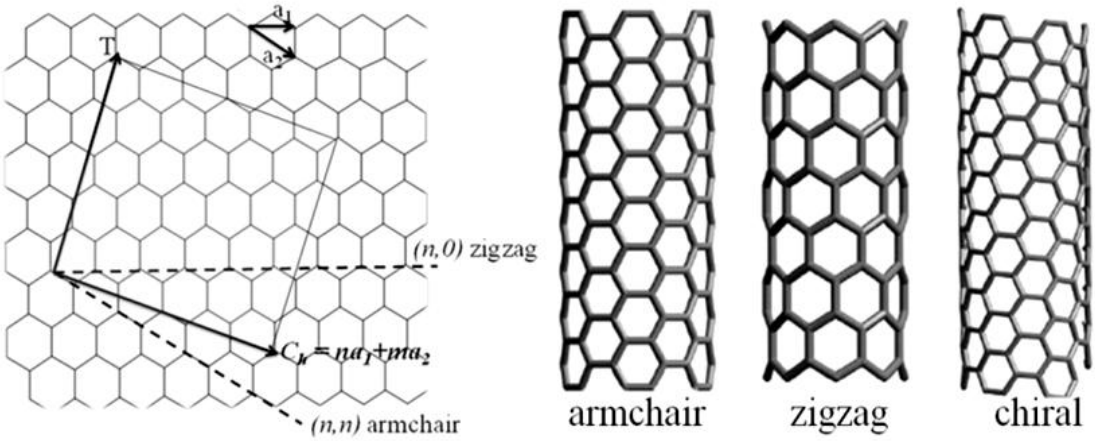

Figure 2.6 Different types of formation of carbon nanotube [20].

For zigzag shape of nanotube m should be zero, for armchair m should be equal to n and for rest of the values of n and m they are chiral [20]. The vector pointing from the first atom towards the other is called the chiral vector and its length is equal to the circumference of the nanotube. The direction of the nanotube axis is

perpendicular to the chiral vector. The schematic of angle (θ), the vector a_1 and a_2 are shown in Fig. 2.6. The chiral vector is given by [20]:

$$\overrightarrow{C_h} = n\overrightarrow{a_1} + m\overrightarrow{a_2},\ where\ 0 \leq m \leq n \quad (2.1)$$

- **On the basis of conductivity**

Depending on the structure of CNT, they are divided in two parts i.e. metallic and semiconducting. For the given (n, m) CNT, if 2n + m = 3q (q is an integer), then the tube is metallic else it is a semiconductor [1.20]. Therefore all armchair CNTs are metallic and rest are semiconducting. Metallic CNTs have a current density more than thousand times greater than conventional metal (copper). A perfect metallic CNT has a ballistic electron transport i.e. an ideal conductor an engineer can dream. If an electron is injected from a contact into a ballistic wire with ideal contacts, the electron will emerge with certainty at the drain contact.

There is no backscattering in the wire, which is the source of intrinsic electric resistance and leads to Ohm's law. Thus, metallic CNTs are attractive interconnect materials because of their high thermal and mechanical stability, thermal conductivity as high as 5800W/mK, ability to carry current in excess of 1014A/m2 current density even at temperatures higher than 200°C and Fermi velocity comparable with that of a metal [21].Moreover, metallic CNT are used as interconnects and semiconducting CNT are used in device applications.

2.6 Multi Wall Carbon Nanotubes

Multiwall carbon nanotubes (MWCNT) is defined as the formation of concentric SWCNT tubes held together within each other by vander Waals forces as shown in Fig. 2.8. The vander Waals distance between the adjacent tubes for two carbon lattices is 3.4Aº. They contain atomic layer planes of carbon, which form a nested series of concentric cylinders, much like the growth rings of on a tree. MWCNTs have several characteristics: wall thickness, number of concentric cylinders, cylinder radius, and cylinder length. Two models are there to describe the structure of MWCNT as shown in Fig. 2.7. In the Russian Doll model, sheets of graphite are arranged in concentric tubes. In the Parchment model, a single sheet of graphite is rolled in around itself as a scroll of newspaper.

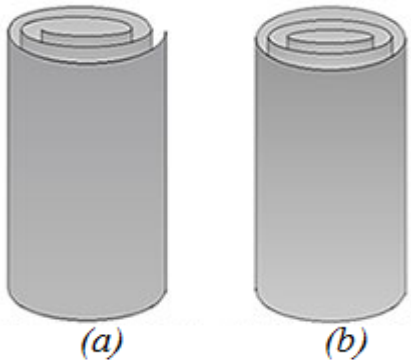

Figure 2.7 (a) Parchment Model (b) Russian Model of MWCNT.

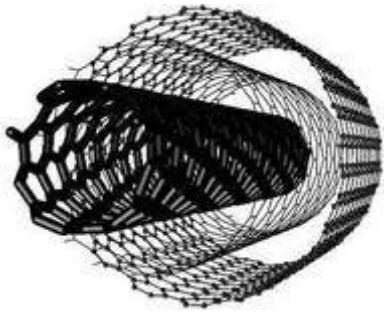

Figure 2.8 Schematic of MWCNT.

On the basis of chirality, MWCNT are always metallic and easier to fabricate whereas SWCNTs can be either metallic or semiconducting. Both SWCNTs and MWCNTs are usually micrometer long and hence can be used very well for components in sub-micron-scale devices and nano composite structure plays a crucial role in emerging technologies. Electrical transport in MWCNTs is ballistic in nature enabling them to carry huge current with no heating effectively. The low resistance of MWCNT makes sure that the dissipated energy in MWCNTs is very less thereby solving the problem of dissipated power density that produces undesirable effects in circuits. However, the high resistance associated with an isolated CNT forced the use of a MWCNT (more number of isolated CNT) and bundle of CNT conducting current in parallel to form an interconnection. Multi-walled CNTs have large diameter of shells due to which the shells are conducting even if they are semiconducting because at room temperature the energy gap between the Fermi level and Conduction band edge (E_c) is smaller than 0.0258 eV. Moreover, due to large density of states in large diameter shells, this energy gap is very small even if it exceeds 0.0258 eV [22]. The electrons in these subbands have reasonable probability (f_i) to appear at E_f following the Fermi-Dirac

distribution function. As the MWCNT have many large diameter shells, they can have large number of conducting channels.

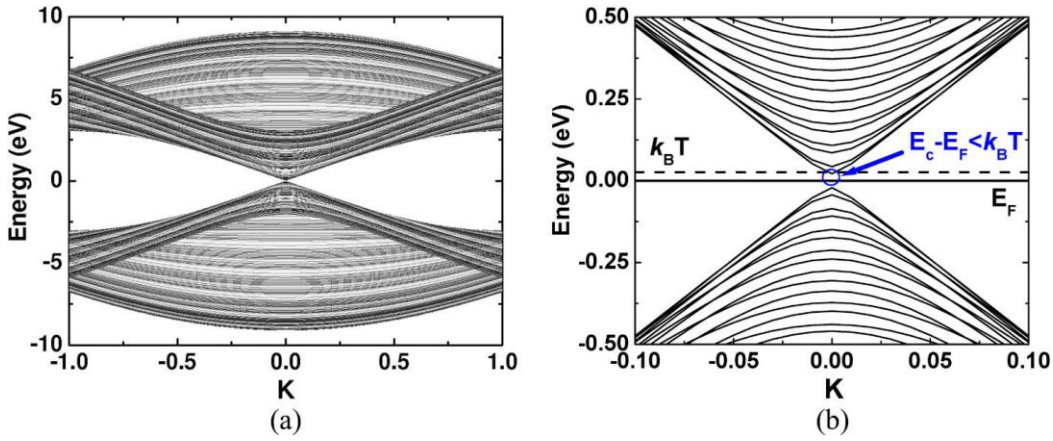

Figure 2.9 Figure 3.23 (a) Band structure of a zigzag (256, 0) carbon nanotube and (b) the band structure after zoom in for clarity. K is the normalized wave vector. Each line denotes a sub-band of CNT shell. In the circular area (around K = 0), the energy difference between the conduction band edge (E_C) and Fermi-level E_F is smaller than kBT [1.22].

2.7 Influence of tube parameters on performance of CNT interconnect

Many researchers [23-26] have studied the performance of CNT interconnect depends on its tube parameter like length, diameter, center to center distance, width, pitch, etc. To study CNT as interconnect material a one-dimensional fluid model for electron transport has been used to develop an equivalent circuit for CNT interconnect [27,28]. Researchers reported that an SWCNT bundle interconnects provides the low resistivity advantage over copper when the bundle length is semi global or global [29, 30]. They also observed that resistivity of copper increases on scaling down the technology node as shown in Fig. 2.10.

They presented that dense and sparse CNT bundle give better performance than the flat arrays of CNT. In Fig.2.11, Flat array and two types of CNT bundle i.e. dense and sparse with different density of metallic CNTs is shown. The performance in terms of delay and power of CNT interconnect is affected by the impedance parameter of CNT. Due to high resistance of CNT, it cannot be used isolated, so they discussed the bundle concept for CNT the formulae to calculate the number of CNT in the bundle for best performance. Then they calculated resistance, capacitance and inductance for CNT bundle. They also compare the performance of the CNT bundle with copper interconnects. They have shown that for local interconnects the resistance of CNT is

higher than Cu if contacts are not perfect. On the other hand, if the contacts are perfect, resistance is much less than Cu interconnects (with maximum densely packed CNT bundles).

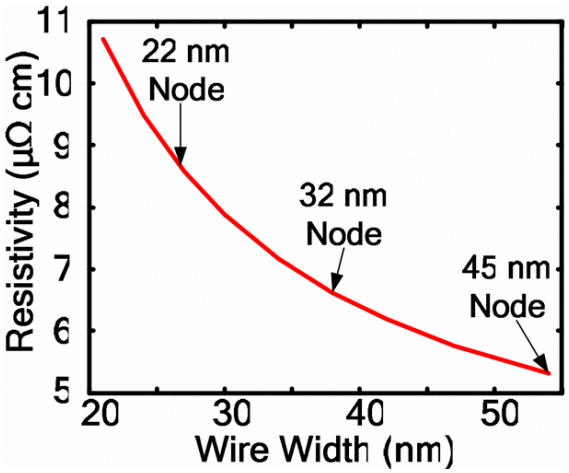

Figure 2.10 Copper interconnects resistivity [30].

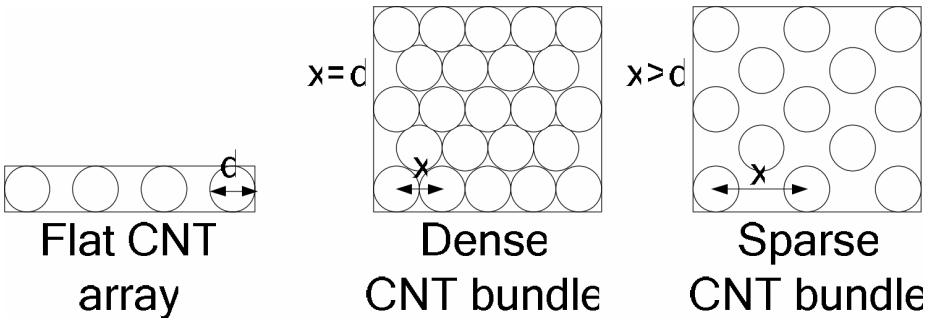

Figure 2.11 CNT bundles with varying density [30].

They have also conducted the experiment to compare the propagation delay of Cu and CNT which shows that for densely packed bundles, propagation delay of local interconnects is higher than that with Cu wires across all technology generations even if contacts are perfect. They have given the reason of higher resistance of minimum sized drivers and capacitance of CNT bundle of local interconnects for this. They observed that the performance of CNT bundles with perfect contacts becomes better than Cu wires if the distance between adjacent metallic CNTs forming a bundle is increased. However, with realistic imperfect contacts the delay is still higher than Cu wires. This interesting result shows that slightly lower metallic CNT density improves local interconnect performance which counters the expectation in previously reported works of them [30]. They have also told there that it is very difficult to achieve the

maximum packing density for CNTs, and these lower densities may be more easily achievable.

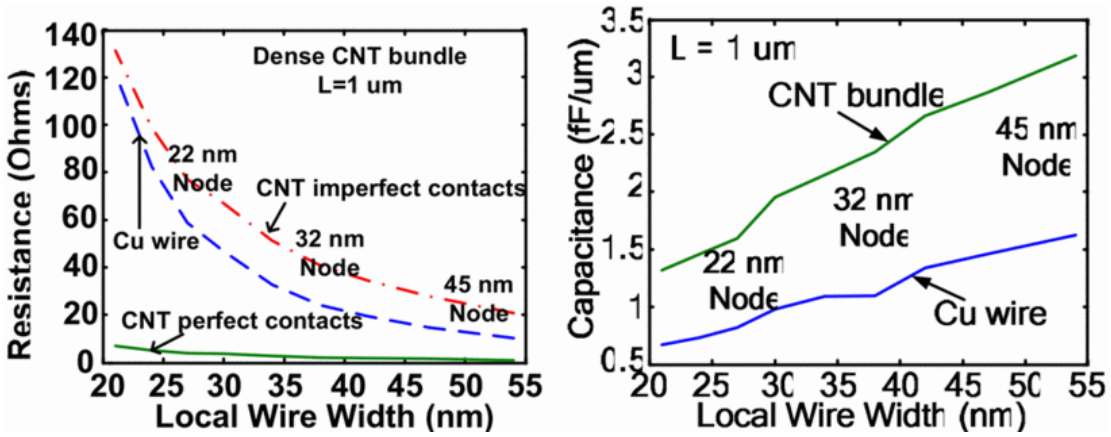

Figure 2.12 Delay of local interconnects [30].

A small decrease in CNT density improves local interconnects performance as it reduces the capacitance of the bundle without increasing resistance too much. They have shown with the help of the experiment that there exists an optimal point where optimum performance can be achieved with the CNT bundle. They also pointed to the fact that, if the imperfect contact resistance is held constant, a reduction in CNT density may not lead to the same improvement in performance as technology scales. They have shown that for intermediate and global interconnects, the performance of CNT- bundle interconnects is better than copper wires and improving with technology scaling even if the contacts are imperfect because at this length Cu resistance becomes very high as shown in Fig.2.12.

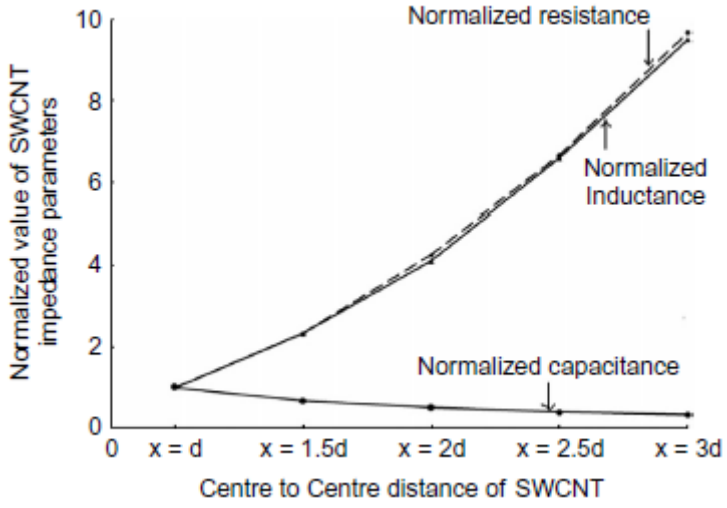

Figure2.13 Normalized impedance parameter as a function of center to center distance of adjacent tube [31].

Khanna et al. [31] and Sarkar et al. [32] analysis the control of tube parameters in terms of diameter, separation between adjacent tubes and lengths, on delay and power dissipation in SWCNT bundle interconnects for VLSI circuit. They observed that on increasing distance between adjacent tubes as well as tube diameter delay is significantly increased whereas reverse is true for power dissipation for different interconnect lengths as shown in Fig. 2.13 and Fig. 2.14.

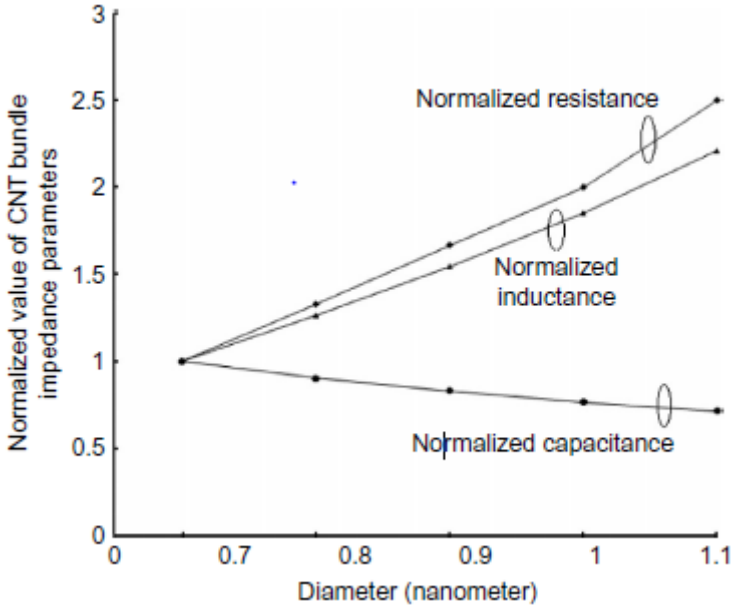

Figure2.14 Normalized impedance parameters as a function of tube diameter [30].

Their results proved that SWCNT bundle interconnects performs better than copper interconnect in terms of delay if the separation between tubes is less than 2nm. Results also indicate that the variation of relative power dissipation with tube separation is observed 10% more on average than of tube diameter. M.K. Rai et al. [33] shows that as the diameter of an isolated tube controls the impedance parameter of a CNT bundle, it is utmost concern to study the effect of isolated tube diameter on delay and power dissipation. Their analysis shows that CNT bundle interconnect composed of tubes of large diameters will have large line resistance. Their analysis also shows that the resistance of CNT interconnect is several times lower than that of copper based interconnects in advanced technology node at global level of interconnects. Their results stated that tube diameter can control SWCNT-interconnect delay and this can also be utilized to improve power dissipation in SWCNT interconnects.

Some studies shows that conductivity of MWCNT shorter than the critical length i.e. 6nm decreases as diameter increases whereas for MWCNT longer than the critical length increasing the diameter results in higher conductivities [34]. This is due to the reason that for long nanotubes, electron mean free path increases linearly with diameter whereas for short nanotubes, quantum resistance and the total number of conduction channels are the key factor as shown in Fig.2.15. Their analysis also shows that for global interconnect lengths MWCNT can have significantly larger conductivity than that of copper or SWCNT bundles.

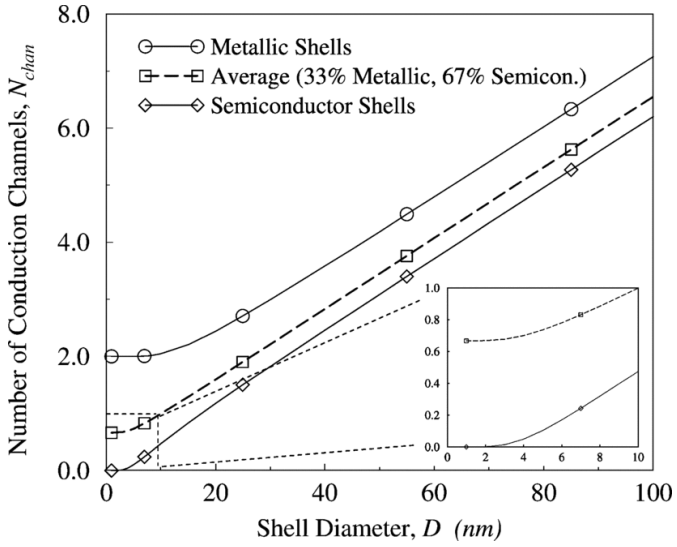

Figure2.15 Number of conducting channels versus shell diameter [35].

Azad Naeemi and James D. Meindl [35,36], presented equivalent circuit models for the resistance of single and multi-wall carbon nanotubes that include various electron–phonon scattering mechanisms as well as changes in the number of conduction channels as a function of temperature. For single and few-wall nanotubes, the temperature coefficient of resistance (TCR) is always positive and increases with length. It reaches 1/ (T − 200 K) for lengths much larger than the electron mean free path. For MWCNs with large diameters (>20 nm), TCR varies from −1/Tto+0.66/ (T − 200 K) as the length varies from zero to very large values.

2.8 Delay Analysis

Yehia Massoud *et al.* [37], developed an equivalent RC circuit model for MWCNT interconnect that captures both DC conductance and high frequency impedance due to capacitive effects and find that MWCNT-based interconnect can have substantially less delay than copper wires in global interconnect applications. Moreover, several

researchers have introduces a diameter-dependent model to analyze the conductance of both SWCNTs and MWCNTs [37]. Their analyses shows that mixed CNT bundles can provide two to five times conductance improvement over copper by selecting suitable parameters such as bundle width, tube density and metallic tube ratio. The work by Massoud et al. [39] demonstrated the relative impact of magnetic and kinetic inductance on SWCNT bundle interconnects. Their results shows that kinetic inductance will not be significant factor in future bundled SWCNT interconnect solutions. Li et al. [40], among the first to study a detailed investigation of MWCNT interconnect performance. In this analysis, a compact equivalent circuit model of MWCNTs is presented and the performance of MWCNT interconnects is evaluated and compared against traditional copper interconnects as well as SWCNT interconnects at different interconnect levels for future technology nodes.

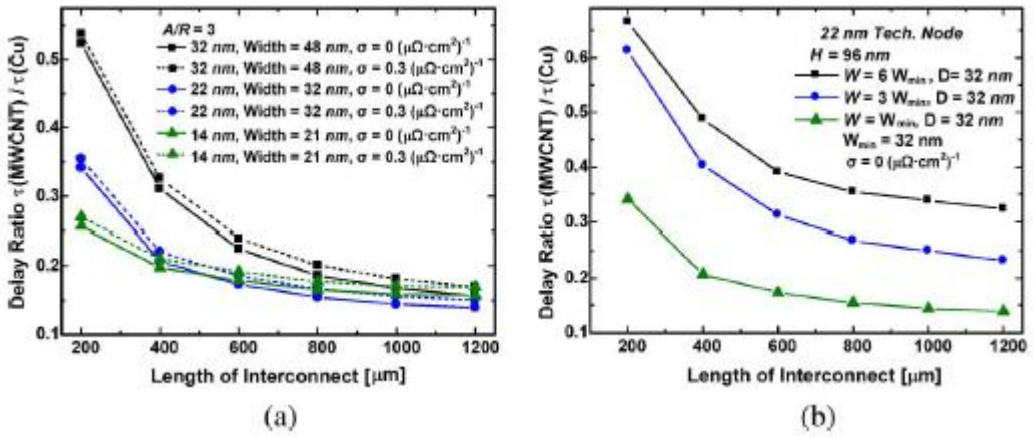

Figure2.16 Delay ratio of MWCNT and copper interconnect at global level for (a) minimum interconnect width (b) different width but same MWCNT diameter.

Their results as shown in Fig.2.16 tells that long (global) interconnects MWCNT interconnects show significant improvement in signal delay as compared to copper wires. They also observed that on increasing contact resistance delay increases. For local length delay increases relatively lower than that of intermediate level of interconnects. However, for short local interconnects the delay of MWCNT interconnects is marginally larger than that of copper as shown in Fig. 2.17. For random chirality, MWCNT interconnects can outperform SWCNT bundles, even at long (global) lengths whereas for metallic chirality, performance of SWCNT bundles is better than MWCNT interconnects as shown in Fig. 2.17.

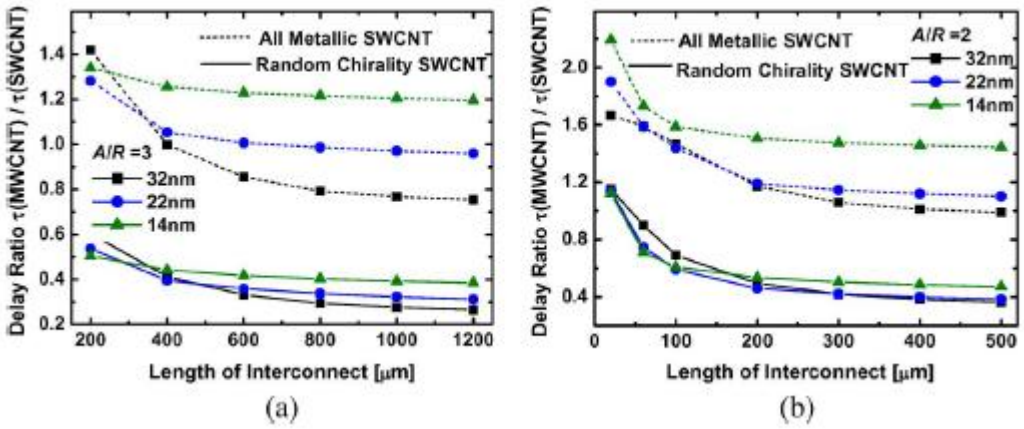

Figure2.17 Delay ratio of MWCNT interconnects with respect to SWCNT interconnects at (a) global and (b) intermediate levels for 32, 22 and 14nm technology nodes respectively.

2.9 Power Analysis

Due to scaling of process technology, effects in the form of power dissipated by wire have become very important. Many researchers have studied the trends of interconnect power consumption based on technology node and current. Youngsoo Shin [41] explained that 20%-30% of power is consumed by interconnect resistance in optimized buffered global interconnect system. Brajesh Kumar Kaushik et al. [42] studied the effect of equal and mismatched signal transition time on power dissipation in global VLSI interconnects. The results obtained represents that the maximum value of dissipated power is 14.1 mW for specified range of rise time. Moreover, dissipated power is quite low for transition from low to high mode whereas reverse of this decreases monotonically with increase in rise time of inputs.

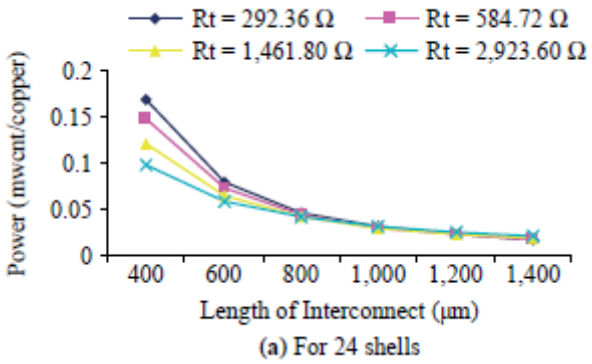

Figure2.18 (a) Power versus length of interconnects for different number of shells.

Yograj Singh Duksh et al. [43] explained the power with variation in driver size and number of shells in MWCNT interconnects. They observed that the ratio of average power consumption of MWCNT versus copper decreases with the variation in driver

size and numbers of shell with respect to the length of interconnect. In Fig2.18 the variation of relative power dissipation of MWCNT to copper interconnect with respect to the length of global interconnect with different driver sizes for different shells is shown.

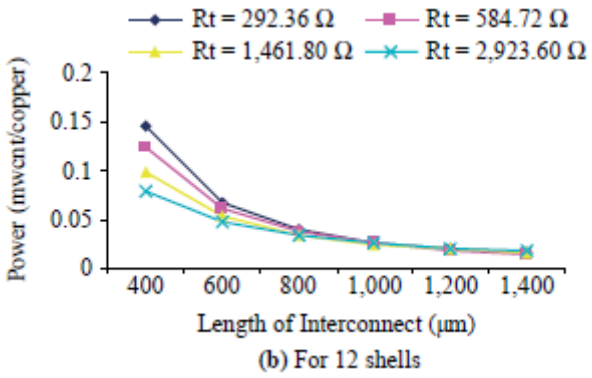

Figure2.18 (b) Power versus length of interconnects for different number of shells.

2.10 Temperature dependent crosstalk analysis

In spite of the fact that high performance ICs have a great discrepancy in temperature ranging from 300 to 450K, only a few prior research have explored the effect of temperature variations on the electrical transport of CNTs. Eric pop et al. [44], among the first to study the electro-thermal behaviour of metallic SWCNTs for interconnect application. It was observed that electron scattering by optical phonon absorption was found to play an important role in altering the low-bias resistance of long SWCNTs, whereas self heating at high bias must be taken into consideration for shorter nanotubes. It was seen as shown in Fig. 2.19 that the temperature dependence of the resistance is obtained through the temperature dependence of the electron scattering mean free paths with acoustic and optical phonons. They also found that the breakdown voltage of SWCNTs in air is linearly proportional to the nanotube length.

Hosseini et al. [45] presented an accurate thermally–aware model for single-walled carbon-nanotube (SWCNT) based interconnects which is a combination of temperature-dependent electrical parasitic model and thermal equivalent circuit that captures both self-heating and heat conduction phenomena as shown in Fig. 2.11. Their results proved that SWCNT-based interconnects offer more than five times reduction in delay at dimensions of 10-20nm for 27-127ºC temperature range.

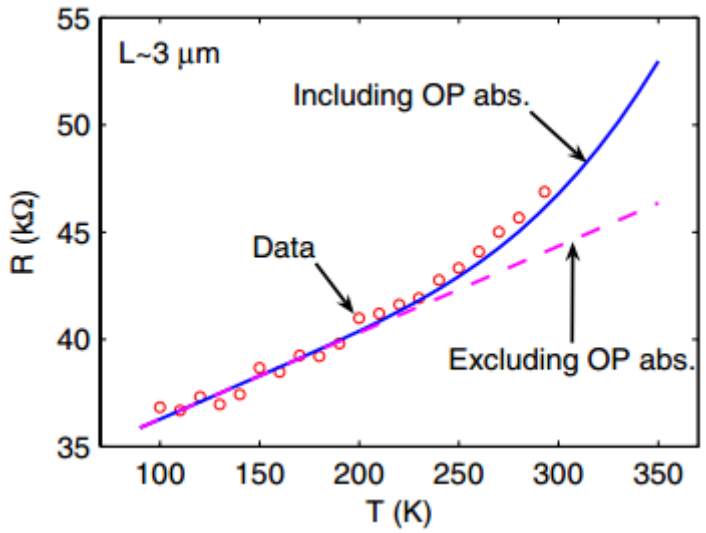

Figure2.19 Variation of the resistance of SWCNT interconnects as a function of temperature for length 3µm [45].

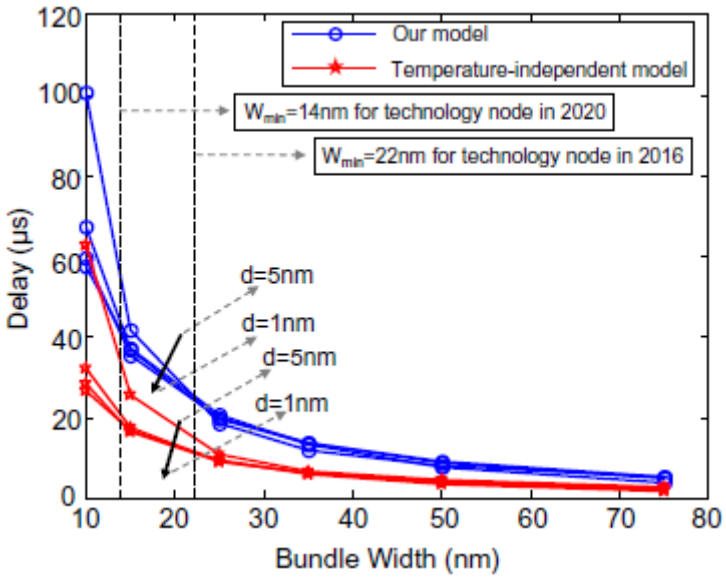

Figure2.20 Propagation delay with respect to SWCNT bundle width [45].

In present day, some of the scientists have studied the consequences of crosstalk in CNT interconnects. Rossi et al. [46] proposed a crosstalk aware CNT bus architecture, formed by double-walled CNTs in parallel and found that this model is less susceptible to crosstalk produced delay and noise voltage peaks. In coupled interconnect, delay, logic failure and noise are the various effects that are caused by crosstalk. Some of the researchers [47] studied that the oxide layer can be damaged due to the crosstalk overshoot and undershoot and observed that the voltage does not vary with scaling ratio of overshoot/undershoot voltages to power supply in all types of interconnect. W. Y. Yin et al. [48] suggested analytical crosstalk models for

SWCNT and DWCNT interconnects to capture crosstalk delay, glitches with upright accuracy. Their analysis includes coupling inductance with coupling capacitance. They have differentiated crosstalk-induced delay in SWCNT and DWCNT bundle interconnects with that of copper interconnects and observed that for semi global and global interconnects CNT, especially DWCNT, crosstalk-induced signal delay is much diminished.

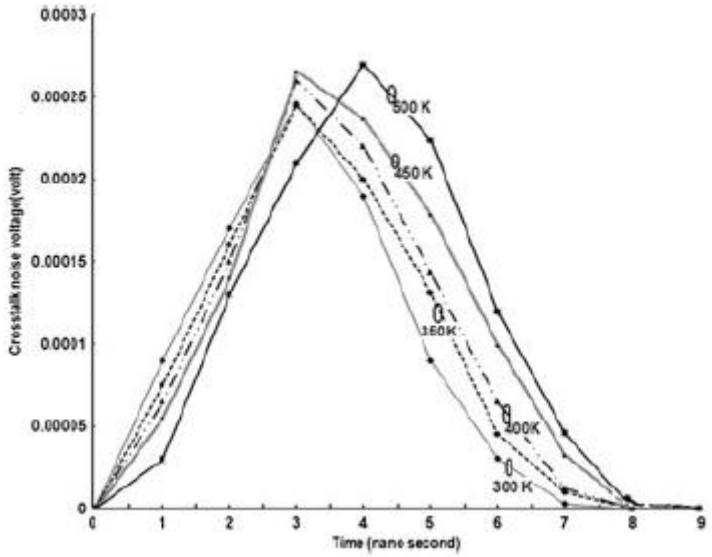

Figure2.21 Crosstalk of coupled interconnects for SWCNT bundle [49].

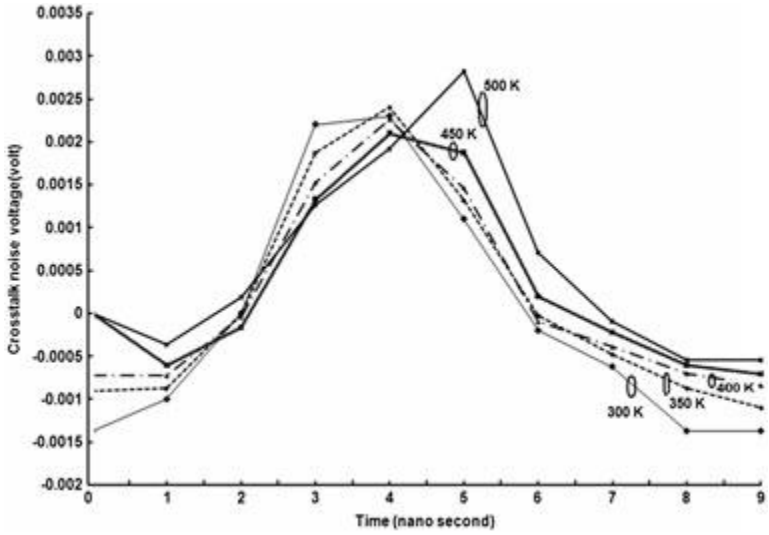

Figure2.22 Crosstalk of coupled interconnects for copper [49].

Rai et al. [49] proposed the temperature dependent equivalent circuit models for SWCNT bundle interconnects and investigated the temperature variation effects on crosstalk-induced voltage noise and their frequency spectrum at the far end of victim

line. Their analysis includes new coupling capacitance model between SWCNT bundles which provides an improved reduction in the crosstalk noise voltage as temperature rises from 300K to 500K. Their results found that on increasing temperature, the effect on the frequency spectrum of victim output waveform reveals that the coupled SWCNT bundle interconnects suppress more frequency component of the noise voltage than the conventional metal (copper) interconnects as shown in Fig. 2.11 and Fig. 2.12.

2.11 Conclusion

In this chapter, it is observed that CNTs are more favourable at deep submicron level because of its distinct properties and have tendency to fight with Electromigration and scattering effects. CNT posses a way more better performance than copper when used as interconnects at nanotechnology. A different type of CNT provides different structures which are used in different applications. However, due to high resistance of isolated CNTs, MWCNT and bundle of CNTs are preferred to reduce the overall resistance of wire which in turn reduce the delay of interconnect and increases the performance. Researchers have worked on different fields related to interconnect. Recent research shows the impact of tube parameters on performance of CNT interconnects. Some of the scientists have explained the performance analysis on the basis of delay and power dissipation of interconnects at deep submicron level. A few researchers have investigated the performance of SWCNTs within integrated circuit from a thermal point of view. As all the integrated circuit works above the room temperature it is necessary to study the effect of temperature on the performance of CNT bundle interconnects.

CHAPTER 3

Influence of length on Delay, Power and PDP of CNT bundle Interconnect

3.1 Introduction

Interconnects are classified in three types, on the basis of their length as global, semi global and local. Global interconnects have large length use to connect between blocks that includes power, ground and clocks. Nodes which are at huge distance are connected by these global interconnects. They are use to connect different devices and different sub circuitry of the circuit. Semi-global interconnects are defined by its name that is intermediate between global and local interconnects. There length lies between global and local interconnects used to connect devices within a block and nodes which are fewer than that of global interconnect. Local interconnects are used to connect nodes of transistors like source, drain, gate in MOSFETs. They are smallest in length.

In this chapter, impedance parameters for CNT bundle i.e. SWCNT bundle and MWCNT bundle; and copper interconnects at different length are calculated and their outcomes on delay, power and PDP (power delay product) is examined and compared. The equivalent distribute circuit model of CNT bundle and copper interconnect is introduced to calculate the equivalent impedance parameters at 22nm technology node at same clock frequency. For scheming the values of impedance parameters such as resistance, capacitance and inductance algorithm have been developed in MATLAB R2013a.

All the SWCNT and MWCNT in the bundles are highly compact and are metallic in nature. All the effects on delay, power and PDP are observed for different interconnect increasing from 100µm to 1000µm with a unit step of 300µm at room temperature i.e. 300K. For SWCNT bundle interconnect, the diameter of the tube is taken as 1nm and for MWCNT bundle interconnect, the diameter of the outermost shell is 32nm for global level. The width and height for interconnect is taken according to the 22nm technology node i.e. 32nm and 96 nm respectively as shown in Table 3.1. All the simulation parameters are given in Table 3.1.

Table 3.1: Simulation parameters at 22 nm technology node [62]

Parameters	**SWCNT**	**MWCNT**	**Copper**
V_{DD}	0.7V	0.7V	0.7V
Global Interconnect:			
Width (w)	32nm	32nm	32nm
Thickness (H)	96nm	96nm	96
Diameter (d) (max)	1nm	32nm	
Mean free path	1µm	1000D	
Aspect ratio	3	3	3
Length (L)	1000µm	1000µm	1000µm
Local and intermediate interconnect :			
Width (w)	22nm	22nm	22nm
Aspect ratio	2	2	2
Thickness (H)	44nm	44nm	44nm
I_{LD} thickness	76.8nm	76.8nm	76.8nm
K_{LD}	2.05	2.05	2.05

3.2 CNT bundle equivalent circuit

3.2.1 SWCNT Bundle

The series combination of resistance, inductance and capacitance of generalized schematic of interconnect is used for isolated SWCNT as shown in Fig. 3.1. The distance between ground plane and SWCNT is denoted as y and the diameter of the SWCNT cylinder is given by d [34].

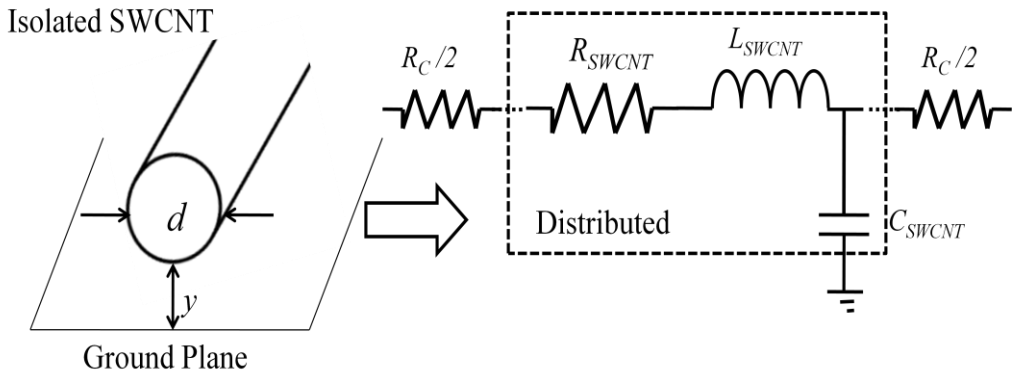

Figure 3.1 SWCNT structure and its distributed circuit.

The numbers of isolated SWCNTs are combined together in parallel combination to generate SWCNT bundle equivalent circuit as shown in Fig. 3.2. The expressions for the resistance, inductance and capacitance are available in the literature [30, 31, 51, 52]. According to Luttinger Liquid Theory, P.J. Burke presented the equivalent circuit model to acquire expressions for resistance, inductance and capacitances of a bundle [30].

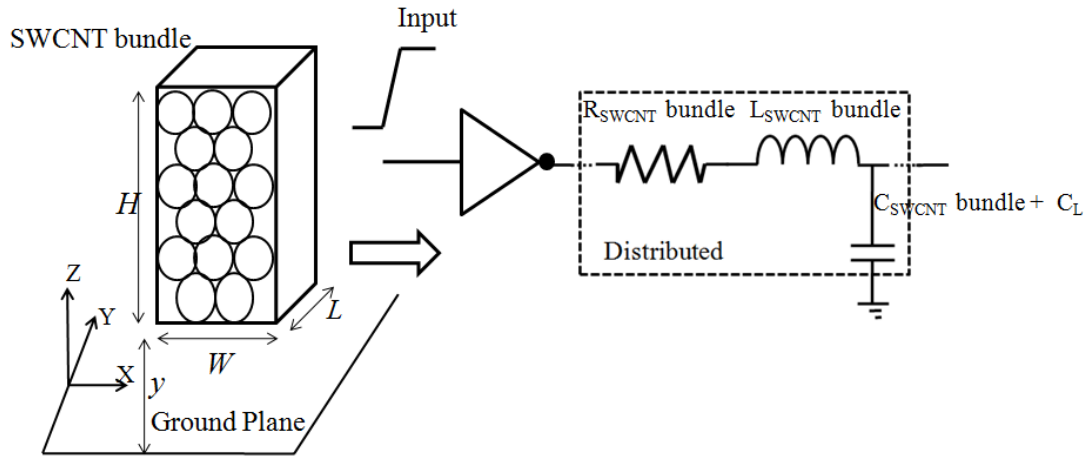

Figure 3.2 Schematic of SWCNT bundle and its equivalent circuit.

The intrinsic impedance per unit length (p.u.l.) of a SWCNT bundle is given by Eq. (2) is given below:

$$Z_{p.u.l} = \left(\frac{h}{2e^2\lambda}\right) + jw\left(\frac{h}{4e^2V_f}\right) \quad (3.1),$$

here V_f is defined as Fermi velocity = 8× 10^5 m/s, h is Planck's constant.

The real part of Eq. 1 is the scattering resistance per unit length (R_s) given by

$$R_s = \left(\frac{h}{2e^2\lambda}\right) \quad (3.2),$$

and the imaginary part is modelled as the kinetic inductance per unit length (L_K) given by

$$L_K = \left(\frac{h}{4e^2V_f}\right) = 8nH/\mu m \quad (3.3).$$

The total sum of the kinetic energy of the right and left going electrons give rise to total kinetic inductance, given in Eq.4, which is denoted for per unit length. The magnetic inductance (L_M) of SWCNT per unit length is given as,

$$L_M = \left(\frac{\mu}{2\pi}\right)\ln\left(\frac{y}{d}\right) \quad (3.4).$$

The magnetic inductance of SWCNT is the inductive component due to electromagnetic (EM) field.

The effective resistance of metallic SWCNT is obtained as a series combination of three components, named as, the contact resistance (R_c), the intrinsic quantum resistance due to ballistic transport ($R_i=h/Ne^2$), and the electron–phonon scattering based ohmic resistance (R_s) is given by Eq. 3, where h is a plank's constant, N is no of conducting channel, e is electron charge. There are 4 conducting channels in SWCNT due to spin and sub lattice degeneracy of electrons. The scattering resistance (R_s) depends on bias voltage and tube parameters viz. length (L), centre to centre distance (x), diameter (d) and width (w). At higher bias where electric field is very high, current saturates and CNT does not show ohmic behaviour. This high bias resistance has much influence on interconnect performance in cases where interconnect length is short ($L \leq \lambda$) [49]. On the other hand, in the low bias regime, the CNT show perfect ohmic behaviour and are compatible with VLSI interconnect applications. For this analysis contact resistance, $R_{c,}$ is assumed to be 24k Ω[45]. Thus, the total Resistance (R_{swcnt}) of SWCNT is written as

$$R_{swcnt} = \left[\frac{h}{4e^2}\right]\left[\frac{L+\lambda}{\lambda}\right] + R_c \text{ , } if\ L > \lambda \tag{3.5}$$

A densely packed SWCNT bundle is taken as shown in Fig. 3.2 where W and H are width and height of SWCNT bundle respectively. The effective resistance of a SWCNT bundle of length L is given by

$$R_{swcnt\ bundle} = \left(\frac{R_{swcnt}}{N_{swcnt}}\right) \tag{3.6}$$

The N_{swcnt} depends upon diameter (d) of CNT tube , thickness (H), width (w) of CNT Bundle interconnect and the separation between the centres of two neighbouring tubes (x) , is defined as [33, 54]:

$$N_{swcnt} = \left\lfloor\frac{w-d}{x}\right\rfloor\left(\left\lfloor\frac{H-d}{\frac{\sqrt{3}}{2}x}\right\rfloor + 1\right) - \frac{1}{2}\left(\left\lfloor\frac{H-d}{\frac{\sqrt{3}}{2}x}\right\rfloor + 1\right) \tag{3.7}$$

if the number of rows in the bundle is even and

$$N_{swcnt} = \left\lfloor\frac{w-d}{x}\right\rfloor\left(\left\lfloor\frac{H-d}{\frac{\sqrt{3}}{2}x}\right\rfloor + 1\right) - \frac{1}{2}\left(\left\lfloor\frac{H-d}{\frac{\sqrt{3}}{2}x}\right\rfloor\right) \tag{3.8}$$

if the number of rows is odd [3.11].

The number of rows is given by

$$n_H = \left(\left\lfloor \frac{H-d}{\frac{\sqrt{3}}{2}x} \right\rfloor + 1 \right) \quad (3.9).$$

The total inductance of the SWCNT bundle is formulated as the parallel combination of the inductances of SWCNT forming the bundle, which is

$$L_{swcnt\ bundle} = \left(\frac{L_M + L_K}{4N_{swcnt}} \right) * L \quad (3.10).$$

In metallic SWCNTs, the magnetic inductance depends on the current axis formed by the bundles due to which it is highly dependent on the geometry of the SWCNT bundle interconnects. When current travels all the combination of parallel SWCNTs encloses same area. Thus, the magnetic inductance remains relatively constant as more SWCNTs are added to the bundle because total area enclosed by current axis remains constant [55]. For length much greater than mean free path of SWCNT the kinetic inductance term is not valid. Thus, L_K is ignored from the calculations in the analysis.

There are two capacitance associated with SWCNT i.e. electrostatic capacitance (C_E) and quantum capacitance (C_Q). The electrostatic capacitance per unit length is defined by the charge stored by the SWCNT-plane system as shown in Fig.3.1 and is given by

$$C_E = 2\pi e \,/\, \ln \frac{y}{d} \quad (3.11)$$

The quantum capacitance occurs due to the quantum electrostatic energy stored in the nanotube when it carries a current and is defined as, for per unit length,

$$C_Q = 2e^2/hV_f \quad (3.12)$$

The effective quantum capacitance is $4C_Q$ because of the four conducting channels in an SWCNT. The total capacitances of a bundle of SWCNTs are given by Eq. (3.13), where $C_E^{Swcnt\ Bundle}$ and $C_Q^{Swcnt\ Bundle}$ are the total electrostatic capacitance and total quantum capacitance of bundle of SWCNT [33] and can be formulated by Eqs. (3.14) and (3.15)

$$C_{swcnt\ bundle} = \left(\frac{C_E^{Swcnt\ Bundle} * C_Q^{Swcnt\ Bundle}}{C_E^{Swcnt\ Bundle} + C_Q^{Swcnt\ Bundle}} \right) * L \quad (3.13),$$

$$C_E^{Swcnt\ Bundle} = 2\left(\frac{2\pi\varepsilon_{ox}}{\ln(s/d)} \right) + \left(\frac{[w-d-2]}{2} \right) \left(\frac{2\pi\varepsilon_{ox}}{\ln(\frac{s+w}{d})} \right) + 3\frac{(n_H-2))}{5} \left(\frac{2\pi\varepsilon_{ox}}{\ln(\frac{s}{d})} \right) \quad (3.14),$$

$$C_Q^{Swcnt\ Bundle} = \left(\frac{2e^2}{hv_f} \right) N_{swcnt} \quad (3.15),$$

where v_f is the Fermi velocity (v_f = 8x10^5 m/s) and s is the separation between adjacent bundles. In this analysis, mSWCNT is considered as interconnect due its

desirable properties and semiconducting SWCNT is ignored [21, 30, 54-57]. The inter-tube tunnelling resistance between the adjacent individual SWCNTs within a bundle is neglected in the bundle. However, constant voltage at every cross-section will also diminish the effect of tunnelling resistance [21, 58]. Therefore, it is safe to collect SWCNTs into bundles which will not affect the performance of individual SWCNTs compared from the single case.

3.2.2 MWCNT Bundle

An isolated MWCNT is made of several concentric rolled up graphene sheets which are known as shells as shown in Fig.3 (a). The distance between the two adjacent shells is equivalent to the vander Waal gap (d)= 0.34nm [40, 59]. D_{max} and D_{min} are the diameters of the outermost and innermost shells as shown in Fig.3.3. The distance between centres of MWCNT to ground plan is denoted as *ht.*

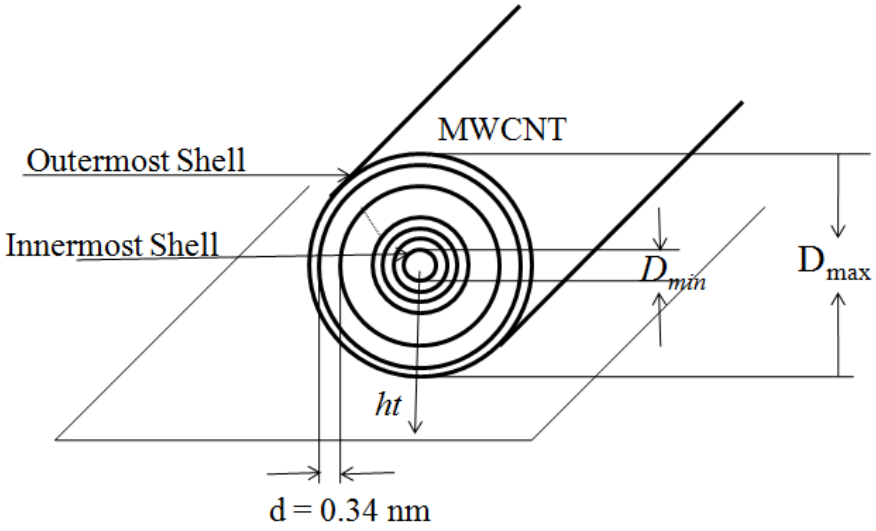

Figure 3.3 Schematic of MWCNT.

A series RLC circuit segment is used to determine the equivalent circuit of an individual shell of isolated MWCNT as shown in Fig.3.4. The number of conducting channels for a particular shell is defined as in [40, 59]

$$N_{shell}\ (D) = \ a * D + b,\ D > 3nm \qquad (3.16),$$

where, D is the diameter of the shells, a = 0.0612 nm^{-1}, and b= 0.425 [40, 45].The ratio of $D_{min}\ /D_{max}$ is assumed to be 0.5, approximately [40, 59]. Thus, the number of shells p of MWCNT is defined as

$$p = 1 + \left\lfloor \frac{(D_{max} - D_{max}\ /2)}{2*d} \right\rfloor \qquad (3.17),$$

Thus, the diameter of the i_{th} shell of MWCNT is obtained by,

$$D_i = D_{max} - 2 * d * (i-1),\ 1 \le i \le p \qquad (3.18).$$

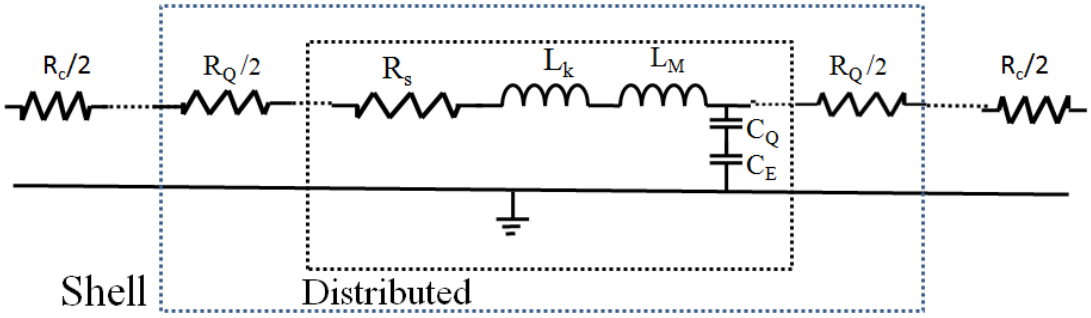

Figure 3.4 Equivalent distribute circuit model of an individual shell.

The effective ($R_{MWCNT/Shell}$) of an isolated shell of MWCNT is obtained by combination of three components, named as

1) Contact resistance (R_c),
2) Intrinsic quantum resistance due to ballistic transport, and
3) Electron–phonon scattering-based ohmic resistance (R_s).

R_s only occur if the length of nanotube (shell) is larger than electron mean free path, where, h is a plank's constant, e is electron charge. The scattering resistance (R_s) depends on bias voltage and tube parameters viz. length (L), centre to centre distance (x), diameter (d) and width (w). The value of intrinsic resistance is given as

$$R_{shell} = R_Q + R_s * L = \frac{h}{N_{shell}(D)*e^2} + \frac{h}{N_{shell}(D)*e^2} * \frac{L}{\lambda_{mwcnt}} \qquad (3.19),$$

Here, L *and* λ_{mwcnt} are the length and mean free path of MWCNT respectively. The value of R_c is assumed to be 1KΩ per shell [45] and $R_Q = h/(N_{shell}(D) * e^2$ whereas, $N_{shell}(D)$ is number of conducting channels for a single shell.

The mean free path of a shell of MWCNT is defined as

$$\lambda_{mwcnt} = 1000 * D_i \qquad (3.20).$$

Here D_i is diameter of the i_{th} shell of the MWCNT.

The inductance of a shell of MWCNT has two components [40]:

1) Magnetic inductance
2) Kinetic inductance

The magnetic and kinetic inductance per unit length of an isolated shell as shown in Fig. 3.4 is given as

$$L_M(p.u.l) = \left(\frac{\mu}{2*\pi}\right) \ln\left(\frac{ht}{D}\right) \qquad (3.21),$$

$$L_{K/channel}\,(p.u.l) = \frac{h}{2*e^2*v_f} * 0.5 \;\approx 8nH/\mu m \quad (3.22),$$

$$L_{K/shell}\,(p.u.l) = \frac{L_{K/channel}\;(p.u.l)}{N_{shell}\,(D)} \quad (3.23),$$

where, ht is the height of the MWCNT bundle from the ground plane, d is the diameter of the shell of MWCNT, v_f is the Fermi velocity. The capacitance of a shell of MWCNT has two components [40], as shown in Fig. 3.4:

1) Quantum Capacitance

2) Electrostatic Capacitance

The quantum and electrostatic capacitance per unit length of an isolated shell as shown in Fig. 3.4 is given as

$$C_{Q/channel} = 2 * \frac{2*e^2}{h*v_f} \approx 193\ aF/\mu m \quad (3.24),$$

$$C_{Q/shell} = C_{Q/channel} * N_{shell}\,(D) \quad (3.25),$$

$$C_E(p.u.l) = \frac{2\pi e}{\ln\,(ht/D_{max}\,)} \quad (3.26),$$

In Mwcnt, different shells have different diameter due to which there is difference in potential at each shell which leads to a shell-to-shell capacitance, is given as [40, 59]

$$C_s = \frac{2\pi e}{\ln\,(D_{out}\,/(D_{out}\,-2d))} \quad (3.27),$$

where, D_{out} is diameter of outer shell and $(D_{out} - 2d)$ is diameter of inner shell, d is the difference between the diameter of two adjacent shells.

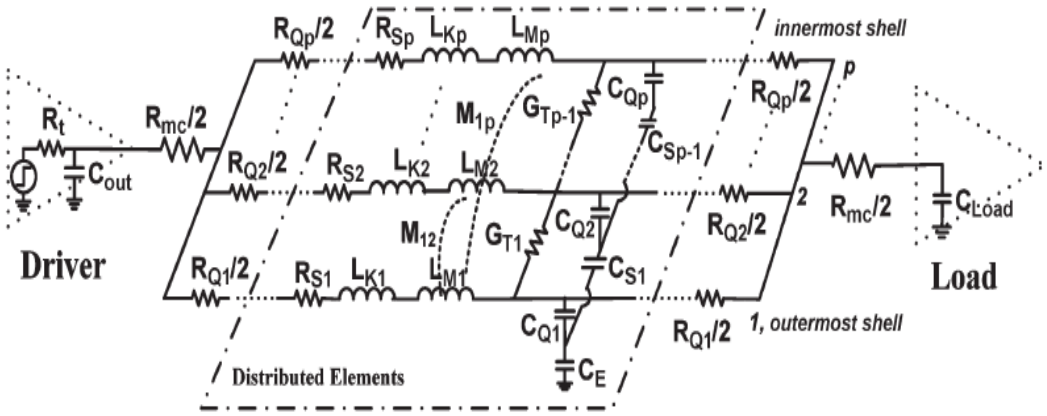

Figure 3.5 Equivalent distributed circuit model of an MWCNT with *P* shells [40].

A large number of shells are combined parallel to form an equivalent circuit of isolated MWCNT as shown in Fig.3.4.

$$\frac{1}{R_{isolated\ \ mwcnt}} = \frac{1}{R_{shell\,(1)}} + \frac{1}{R_{shell\,(2)}} + \ldots\ldots\ldots + \frac{1}{R_{shell\,(P)}} \quad (3.28),$$

where, P is the total number of shells in Mwcnt. A MWCNT bundle consists of parallel combination of a number of MWCNTs. Thus the resistance of a MWCNT bundle of length L is given as

$$R_{mwcnt\ \ (bundle\ )} = \frac{R_{isolated\ \ mwcnt}}{N_{mwcnt}} \quad (3.29),$$

where, N_{mwcnt} is total number of MWCNTs in a bundle is shown as

$$N_{mwcnt} = N_w N_h - \frac{N_h}{2}, \text{ if } N_h \text{ is even} \quad (3.30),$$

$$N_{mwcnt} = N_w N_h - \frac{N_h - 1}{2}, \text{ if } N_h \text{ is odd} \quad (3.31).$$

Here number of MWCNTs along x and z axis are given by N_w and N_h and they are shown as

$$N_w = \frac{(w - D_{\max})}{(D_{max} + d)} \quad (3.32),$$

$$N_h = \frac{2(H - D_{max})}{\sqrt{3}(D_{max} + d)} + 1 \quad (3.33),$$

where, w and h are the width and height of the bundle.

Similarly inductance of the isolated shell of MWCNT is stated as

$$L_{isolated\ \ mwcnt} = \left(\sum \frac{1}{L_{total\ /shell\,(i)}}\right)^{-1}, 1 \le i \le P \quad (3.34),$$

where, $L_{total\ /shell\,(i)}$ is the total inductance of a shell of MWCNT and P is no. of shells in a MWCNT. The total inductance of a shell is given as

$$L_{total\ /shell\,(i)} = L_{K/shell\,(i)} + L_{M(i)} \quad (3.35).$$

Thus, the total inductance of a MWCNT bundle of length L is given by,

$$L_{mwcnt\ \ bundle} = \frac{L_{isolated\ \ mwcnt} * L}{N_{mwcnt}} \quad (3.36).$$

The capacitance of the isolated shell of MWCNT is given as

$$C_{isolated\ \ mwcnt} = \sum C_{total\ /shell(i)}, 1 \le i \le P \quad (3.37),$$

where, $C_{total\ /shell\,(i)}$ is the total capacitance of a shell in MWCNT and P is no. of shells in a MWCNT. The total capacitance of a shell is given as

$$C_{total\ /shell\,(i)} = \left(\frac{C_{Q/shell\,(1)} * C_E}{C_{Q/shell\,(1)} * C_E} + \frac{C_{Q/shell\,(i+1)} * C_s}{C_{Q/shell\,(i+1)} + C_s}\right) * L \quad (3.38),$$

Thus, the total capacitance of a MWCNT bundle of length L is given as

$$C_{mwcnt\ \ bundle} = C_{isolated\ \ mwcnt} * N_{mwcnt} \quad (3.39).$$

The analytical expression used to determine impedance parameters of copper interconnect is summarized as follows [47, 49, 60, 61]:

$$R = \frac{\rho * L}{w * H} \quad (3.40),$$

$$L_s = \frac{\mu_o * L}{2\pi}\left[\ln\left(\frac{2L}{w+H}\right) + 0.5 + 0.22\,\frac{w+H}{L}\right] \quad (3.41),$$

$$C_g = \varepsilon\left[\frac{w}{y} + 2.22\left(\frac{s}{s+0.7y}\right)^{3.19} + 1.17\left(\frac{s}{H+4.53y}\right)^{0.76}\left(\frac{s}{H+4.53y}\right)^{0.12}\right] \quad (3.42).$$

Here, L_s is the self inductance, C_g is the capacitance with respect to ground, Also, L = length, w = width, H= thickness, ρ=resistivity, y = height above ground, s = spacing, ε = dielectric constant and μ_o = permeability.

3.3 Impedance Analysis of CNT

The consequences of change in length of interconnect on the impedance parameters are scrutinized in this section. The outcomes of variation of four different dimensions of interconnect length on the impedance parameters of SWCNT bundle, MWCNT bundle and copper interconnect is shown in Figure 3.5, 3.6 and 3.7. Data given in Table 3.1 are used for all calculations. Delay, power and PDP are affected by the variation in the impedance parameters. It is determined that the values of resistance, inductance and capacitance increase as the interconnect length increases.

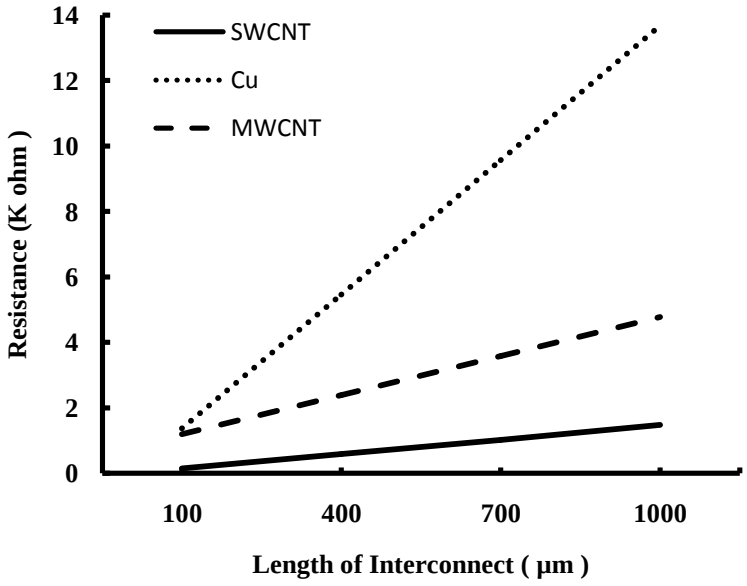

Figure 3.6 Resistance as a function of length of interconnect.

Resistance: Fig 3.6 shows how the resistance varies with the interconnect length increasing from 100µm to 1000 µm at 22nm technology node. The total resistance is due to the net effect of three components of resistance i.e. quantum resistance,

scattering resistance and contact resistance. It is evident using Eqs. (3.2), (3.5), (3.6), (3.19), (3.28), (3.29) and (3.40) that resistance of the interconnect increases with increase in length. The resistance of SWCNT bundle is less than the resistance of both MWCNT bundle and copper interconnect for all values of interconnect length. It is due to the reason that SWCNT bundle has large free mean path of electron than the copper. The free mean path of SWCNT lies in micron meter range where as for copper it lies around nanometer. The resistance of MWCNT bundle lies in between the copper interconnect and SWCNT bundle for all values of interconnect length. For global length (>700 μm) of interconnect the resistance of CNT bundle is significantly less than copper wire due to which CNT bundle interconnect is more suitable candidate for interconnect applications. However, the resistance of MWCNT bundle and copper interconnect at local level (~100 μm) of interconnect have values in similar range whereas SWCNT bundle has lowest resistance at local level (~100 μm) of interconnect which is best suited for connecting interconnections of a system.

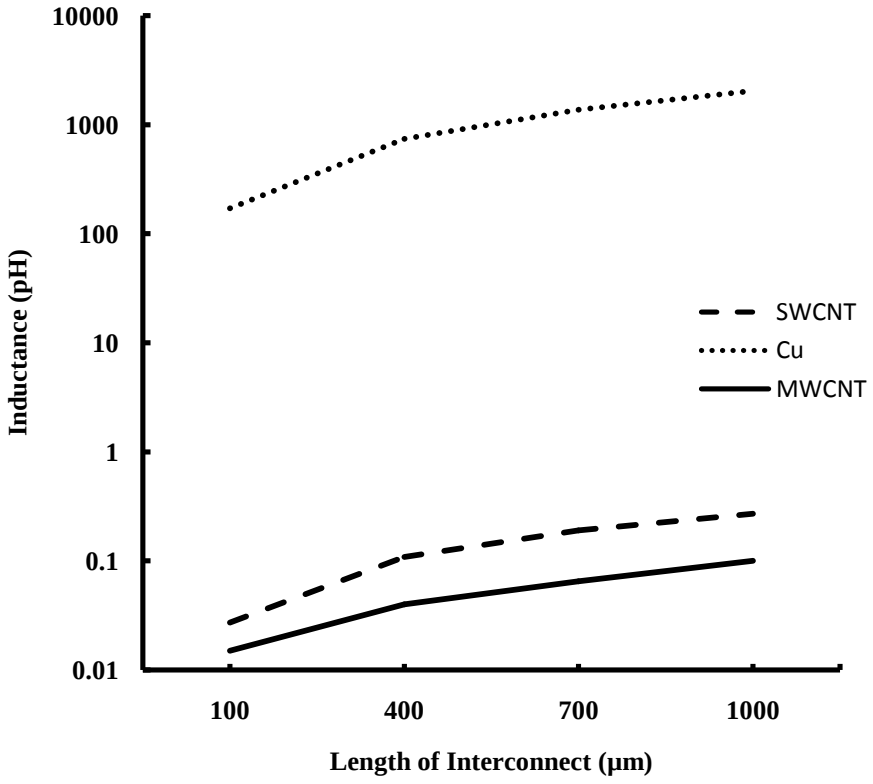

Figure 3.7 Inductance as a function of interconnect length.

Inductance: Figure 3.7 shows the variation of effective inductance as a function of interconnect length for four different dimensions at 22nm technology node. The net inductance of interconnect is due to kinetic inductance and magnetic inductance as

given by Eqs. (3.3), (3.4), (3.10), (3.21)-(3.23) and (3.34)-(3.36) increases as length of interconnect increases from 100μm to 1000 μm. It is observed that copper has significantly very high inductive effect for all values of different interconnect length increasing from 100μm to 1000μm. SWCNT bundle has lower inductance and MWCNT bundle has the lowest inductance for all three interconnect material i.e. copper, SWCNT bundle and MWCNT bundle at different values of interconnect length while the value of inductance element per unit length remains same for respective interconnects.

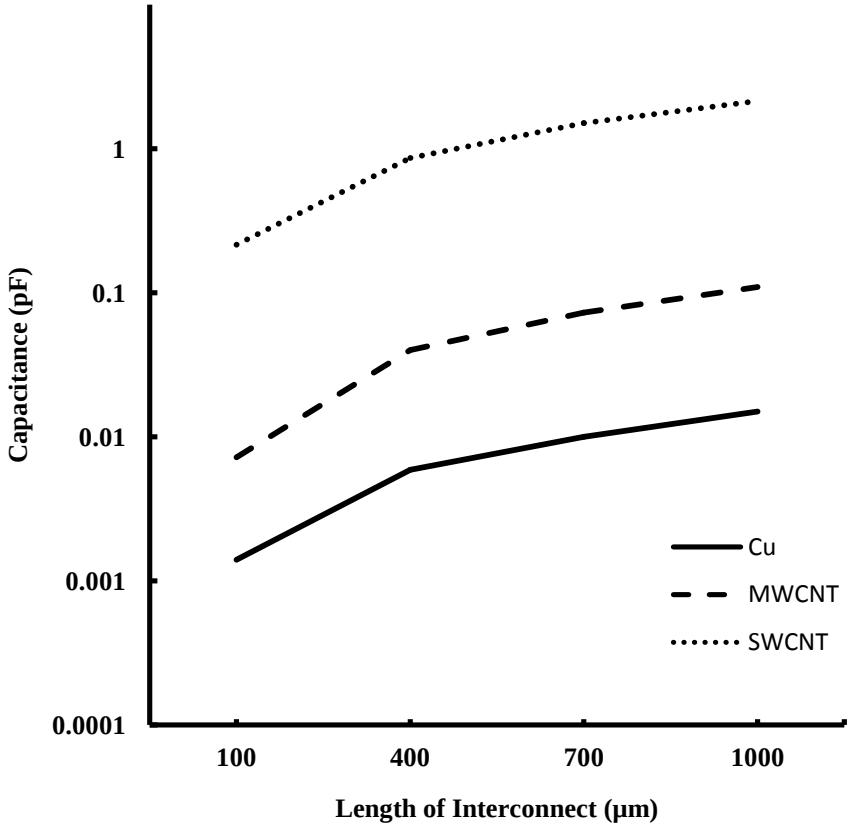

Figure 3.8 Capacitance as a function of interconnect length.

Capacitance: Fig.3.8 shows the variation of capacitance over different interconnect length increasing from 100μm to 1000μm at 22 nm technology node. The effective capacitance is due to the net effect of quantum capacitance, shell to shell capacitance and electrostatic capacitance. It is observed that a bundle of CNT composed of tubes has larger effective capacitance in comparison with all three interconnect material. Due to the cylindrical shape of CNT bundle, its exposed surface area to the surrounding interconnects is larger than the rectangular surface area of copper. Thus, CNT bundle has larger effective capacitance as compared to copper interconnect.

3.4 Performance analysis of CNT

The equivalent distributed circuit of interconnect developed by SWCNT bundle and MWCNT bundle is used to determine the performance in terms of delay, power dissipation and power delay product (PDP) and is compared with the results of copper interconnect for 22nm technology node at different interconnect lengths at room temperature i.e. 300K. For the sake of comparison clock speed of 0.04GHz and load capacitance of 1pF are kept same for all the cases [62, 63]. Optimum number of repeaters has been found out to optimized performance for all three materials i.e. SWCNT bundle, MWCNT bundle and copper. For all calculation and SPICE simulation purposes, the data shown in Table 3.1 are use.

3.4.1 Propagation Delay

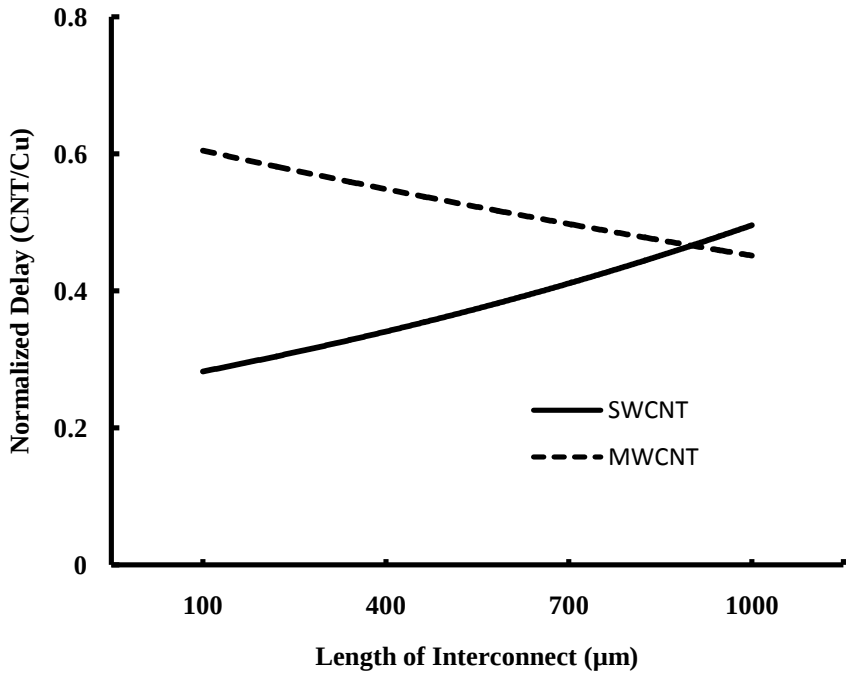

Figure 3.9 Normalized delay of CNT bundle as a function of interconnects length.

The 90% delay has been extracted for all SWCNT bundle, MWCNT bundle and copper interconnects using SPICE simulations results at different interconnect lengths. Fig.3.9 shows the variation in normalized delay of CNT bundle as a function of interconnect length increasing from 100µm to 1000µm. The normalizing factor used is copper interconnect propagation delay for both the CNT bundles. It is observed that the normalized delay of SWCNT bundle increases with increase in length due to the reason that delay of copper increases drastically as length increases whereas reverse is true for SWCNT bundle.

It is also seen that the normalized delay of MWCNT bundle decrease with increase in interconnect length varies from 100µm to 1000µm because of the dominating nature of resistance and inductance in MWCNT bundle as compared to copper interconnect.

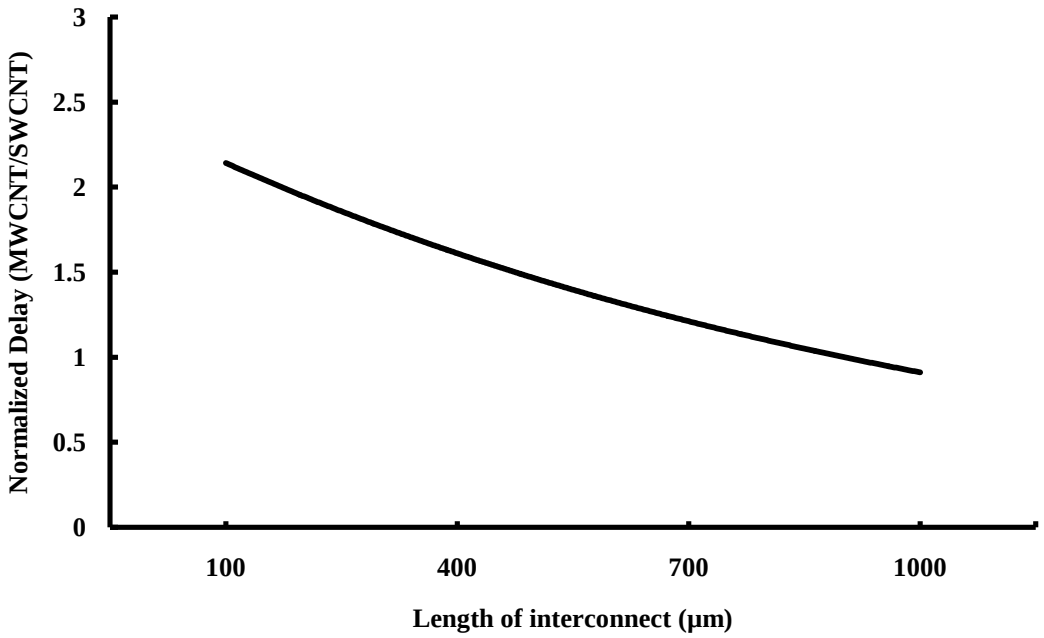

Figure 3.10 Delay ratio of MWCNT bundle versus SWCNT at different interconnect lengths.

In Fig. 3.10, It is seen that ratio of CNT bundle decreases with increase in length of interconnect. It is observed that for interconnect of length 100µm (local level) delay of MWCNT bundle is relatively greater than the delay of SWCNT bundle due to the high resistance of MWCNT bundle in comparison with SWCNT bundle. However, for interconnect of length greater than 700µm, delay of SWCNT bundle and MWCNT bundle is almost similar. As MWCNT bundle are easier to fabricate than SWCNT bundle, these are more appropriate to use than SWCNT bundle at global levels.

3.4.2 Power Dissipation

Fig. 3.11 represents the power dissipation in CNT bundle at different interconnect lengths. It is observed that dissipation power increases with increase in interconnect length increasing from 100µm to 1000µm. It is also observed that SWCNT bundle has less power than copper interconnect at local level (100µm) of interconnect length at room temperature whereas for global level of interconnect SWCNT bundle dissipates more power than copper interconnect. Results also reveals that the MWCNT bundle dissipates more power at all length of interconnect when compared with copper. This

is because as line length increases, the capacitance becomes more dominating in MWCNT bundle.

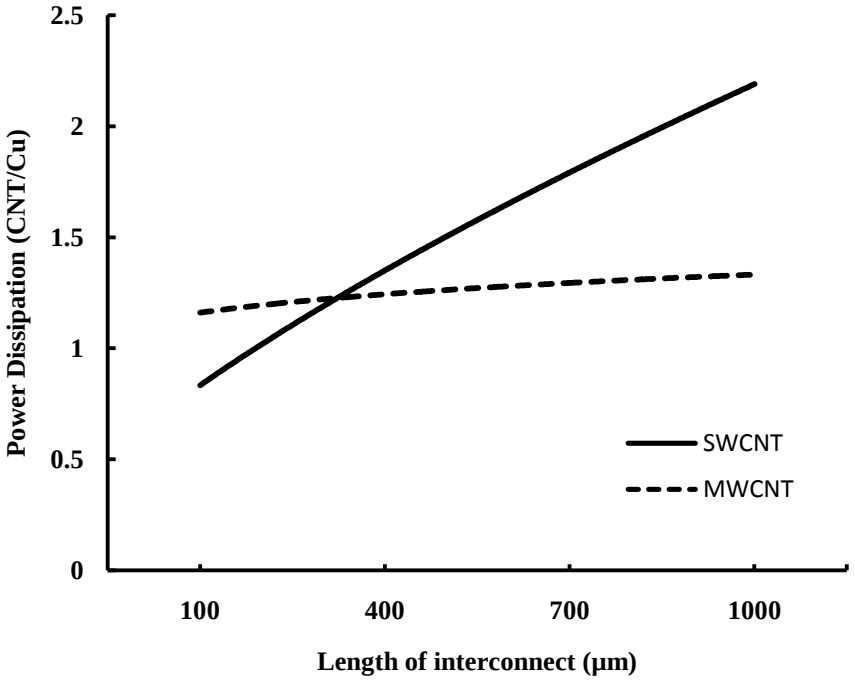

Figure 3.11 Normalized Power dissipation of CNT as a function of interconnect length

However, in Fig. 3.12, it is shown that ratio of power dissipation of MWCNT bundle versus SWCNT bundle decreases as interconnect length increases.

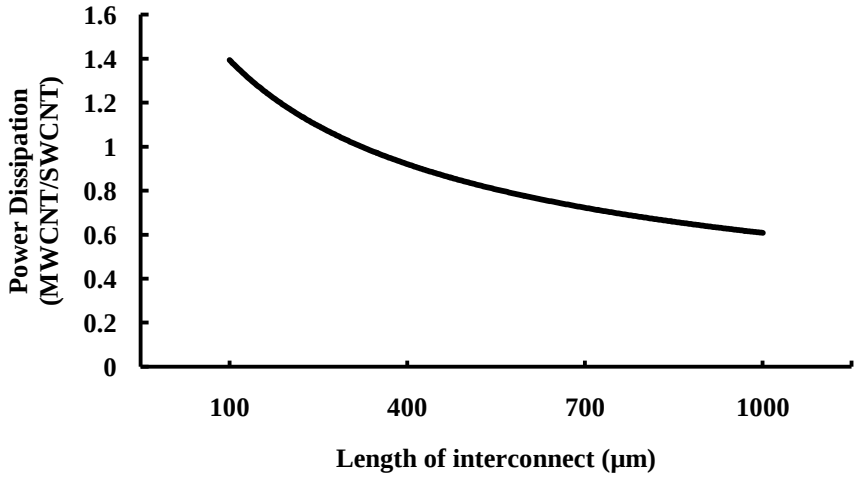

Figure 3.12 Ratio of power dissipation of MWCNT bundle and SWCNT bundle as a function of interconnect length.

For global level of interconnect, MWCNT bundle dissipates less power in comparison with SWCNT bundle due to the dominating nature of capacitance of SWCNT bundle. However, for local level of interconnect, SWCNT bundle dissipates less power at room temperature because resistance of MWCNT bundle is significantly high.

3.4.3 Power Delay Product (PDP)

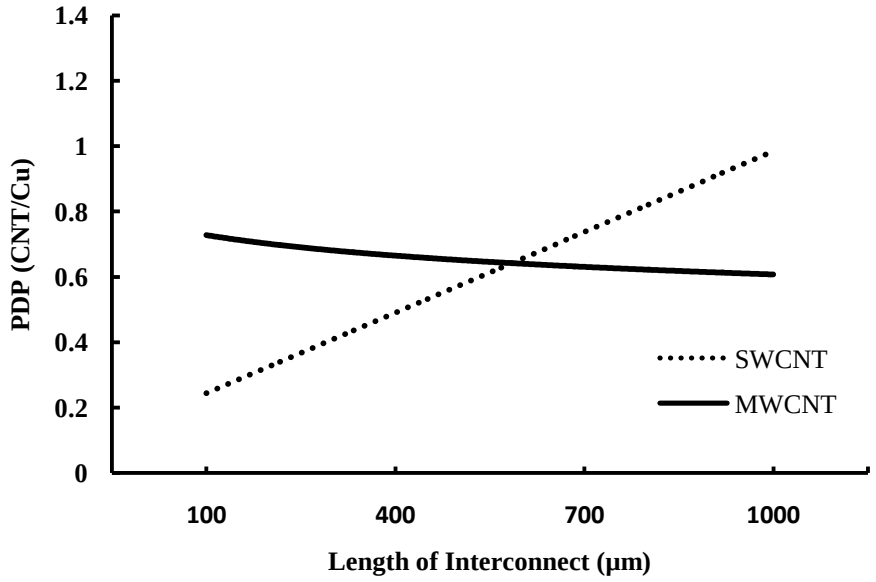

Figure 3.13 PDP of CNT bundle as a function of interconnect length.

Fig. 3.13 shows Power Delay product (PDP) as a function of line length. It is seen that ratio of PDP of SWCNT bundle increases with increase in length of interconnect whereas it decrease for MWCNT bundle with increase in interconnect length. It is shown in Fig. 3.12 that both SWCNT bundle and MWCNT bundle has less PDP than copper interconnect due to the dominating factor of power dissipation.

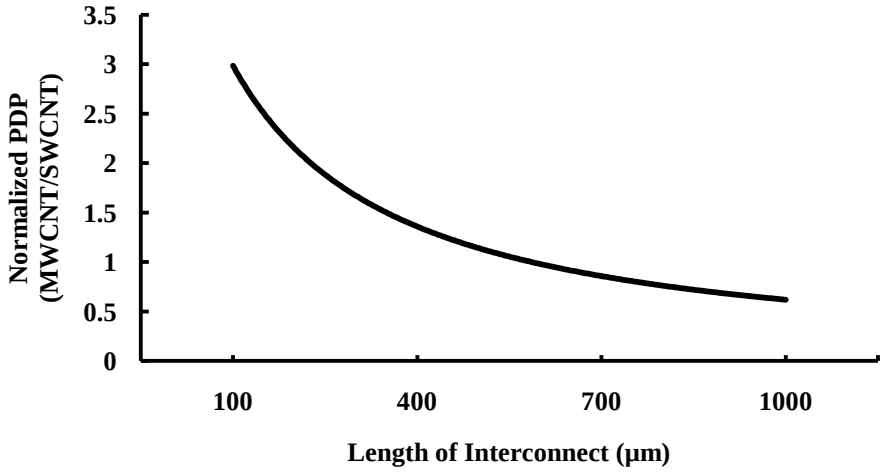

Figure 3.14 Ratio of PDP of MWCNT bundle versus SWCNT bundle.

In Fig. 3.14 It is represented that the ratio of PDP of CNT bundle decreases as increase in length from 100μm to 1000μm at room temperature. It is observed that for interconnect of global length (>700 μm), MWCNT bundle poses lesser PDP than SWCNT bundle whereas for interconnect of local length (100 μm), MWCNT bundle

poses higher PDP than SWCNT bundle. This is due to the reason that SWCNT bundle dissipates more power at higher values of interconnects length.

3.5 Conclusion

The influence of interconnect length on CNT bundle interconnect is examined and SPICE simulation results are used to compare CNT bundle interconnect performance with that of copper interconnect at 22nm technology and with each other i.e. SWCNT bundle and MWCNT bundle. It is concluded that for global lengths of interconnect, performance analysis in terms of propagation delay, power dissipation and PDP at room temperature, MWCNT bundle is more preferred choice of interconnect in comparison with SWCNT bundle and copper interconnect. It is also stated that for local lengths of interconnect performance of SWCNT bundle is best in comparison with MWCNT bundle and copper interconnect at room temperature.

CHAPTER 4

Temperature dependent performance analysis of an SWCNT bundle

4.1 Introduction

Temperature dependent performance analysis in terms of delay, power dissipation and power delay product (PDP), in single walled carbon nanotube (SWCNT) bundle interconnect have been analyzed. Temperature-dependent circuit model for metallic SWCNT bundle is presented. The results are compared with those of currently used copper interconnects at 22nm technology node. It is seen that delay, power dissipation and PDP of SWCNT bundle interconnect increase with rise in temperature from 300K to 450K at different interconnect lengths from 100µm to 1000µm . It is also observed that, with rise in temperature, SWCNT bundle has lower delay than that of copper for all interconnect lengths whereas reverse is true for power dissipation. In addition, with rise in temperature from 300K to 450K, for interconnect lengths at 100µm and 400µm SWCNT bundle has lower PDP compared to copper interconnects where as reverse is true for interconnect lengths at 700µm and 1000µm. Moreover, relative average improvement in delay, power and PDP using thermally aware model in comparison with temperature independent model is estimated.

4.2 Temperature-dependent equivalent circuit parameters of swcnt bundle and copper based interconnect

As the technology scaled down, it is observed that the temperature of interconnects based on conventional material(copper) increases beyond a 45nm node due to the combined effect of increase in resistivity of metal and current density[23].Operating temperature of most of the integrated circuit is much greater than room temperature. Thus, it is very important to understand the temperature dependent electrical characteristics of SWCNTs greater than room temperature.

A series RLC circuit segment is used to determine the equivalent circuits of an isolated SWCNT interconnect as shown in Fig.3.1 in chapter 3 using Luttinger liquid theory [30]. A large number of such circuits are combined parallel to form SWCNT

bundles. The expressions for resistance, capacitance and inductance of SWCNT bundles can be obtained from the literature [31, 18, 54, 64] as explained in chapter 3.

The effective temperature dependent resistance (R_{CNT}) of metallic SWCNT is obtained as a series combination of three components, named as, the contact resistance (R_c), the intrinsic quantum resistance due to ballistic transport($R_i=h/Ne^2$), and the electron–phonon scattering-based ohmic resistance (R_s) where, h is a plank's constant, N is no of conducting channel, e is electron charge. There are 4 conducting channels in SWCNT due to spin and sub lattice degeneracy of electrons. The scattering resistance (R_s) depends on bias voltage, temperature and tube parameters viz. length (L), centre to centre distance (x), diameter (d) and width (w).

At higher bias where electric field is very high, current saturates and CNT does not show ohmic behaviour. This high bias resistance has much influence on interconnect performance in cases where interconnect length is short ($L \leq \lambda_{swcnt}$) [49]. On the other hand, in the low bias regime, the CNT show perfect ohmic behaviour and is compatible with VLSI interconnect applications. The temperature dependence of the resistance of SWCNT is obtained from the temperature dependence of the electron scattering mean free paths (MFPs) with acoustic (AC) and optical (OP) phonons [44].For this analysis contact resistance, R_c is assumed to be 24K Ω[45]. At low bias, resistance of SWCNT increases with temperature due to optical phonon (OP) absorption above 250K. Thus, the total Resistance [44] of SWCNT is written as:

$$R_{SWCNT}(T) = \left[\frac{h}{4e^2}\right]\left[\frac{L+\lambda_{swcnt}(T)}{\lambda_{swcnt}(T)}\right] + R_c \quad if\ L > \lambda_{swcnt} \tag{4.1}$$

where λ_{swcnt} (T) is the net temperature dependent electron MFP. This includes scattering of electrons due to OP emission and absorption [58, 65, 66] and formulated as

$$\lambda_{swcnt}(T) = (\lambda_{AC}^{-1} + \lambda_{Op,ems}^{-1} + \lambda_{Op,abs}^{-1})^{-1} \tag{4.2}$$

The AC scattering and OP absorption and after effect of OP absorption i.e. OP emission length are given respectively as [65, 66]:

$$\lambda_{AC} = \lambda_{AC,300}\left(\frac{300}{T}\right) \tag{4.3}$$

$$\lambda_{OP,abs} = \lambda_{Op,300}\left(\frac{Nop(300)+1}{Nop(T)}\right) \tag{4.4}$$

$$\lambda_{OP,ems} = (1/\lambda_{OP,ems}^{fld} + 1/\lambda_{OP,ems}^{abs})^{-1} \quad (4.5),$$

$$\lambda_{OP,ems}^{fld}(T) = \frac{\hbar op}{e.Vdd} L + \frac{Nop\ (300)+1}{Nop\ (T)+1} \lambda_{OP,300} \quad (4.6),$$

$$\lambda_{OP,ems}^{abs}(T) = \lambda_{OP,abs}(T) + \frac{Nop\ (300)+1}{Nop\ (T)+1} \lambda_{OP,300} \quad (4.7)$$

Here, $\lambda_{AC,300}$ ≈1600nm is the acoustic scattering length at 300 K, $\lambda_{OP,ems}^{abs}$(T) is the OP emission MFP after absorption, $\lambda_{OP,ems}^{fld}$(T) is the former OP emission MFP and $\lambda_{OP,300}$ ≈15 nm is the spontaneous optical emission length at 300 K.

The temperature dependent effective resistance of a SWCNT bundle as shown in Fig.2 ($L > \lambda$), is given by Eqs. (51).This is formulated as:

$$R_{SWCNT}(\text{Bundle}) = \frac{R_{SWCNT}\ (T)}{N_{CNT}} \quad (4.8),$$

where N_{CNT} is total number of SWCNTs in Bundle is presented in chapter 3.

Other temperature independent circuit parameters of SWCNT bundle interconnects such as inductance and capacitance of SWCNT bundle are obtained from the appropriate expressions available in [33, 34, 54] as explained in chapter 3 by Eq. (3.11) and Eq. (3.14) are tabulated in Table4.1 at room temperature i.e. 300K. Furthermore, the performance of copper interconnect under temperature variation can be estimated accurately using the temperature dependent resistance formula available in [23]

$$R(T) = R_o(1+\propto (T - T_o)) \quad (4.9),$$

where, $\propto$ is the temperature coefficient of resistance, measured at room temperature T_0 = 300 K. For copper, $\propto$ = 0.0039K^{-1}. R_o is defined as resistance at room temperature given as $R_o = \rho_o.(L/A)$ where ρ_o is resistivity of copper at room temperature [66].In order to calculate other impedance parameters of copper interconnect like inductance and capacitance, the appropriate expressions are given in chapter 3 by Eq. (3.42) and Eq. (3.43) as they are independent of temperature.

4.3 Analysis of Impedance Parameters

It may be seen from Eqs. (4.1), (4.8) and (4.9) that the effective low bias resistance of SWCNT bundle and copper-based interconnect are function of temperature. The total temperature dependent impedance parameters of SWCNT bundle and copper-based

interconnects is now calculated and the data used for these calculations are given in Table I as shown in chapter 3 for interconnect. The width and thickness of global (~1000 μm long) interconnect are assumed to be 32 and 96 nm, respectively.

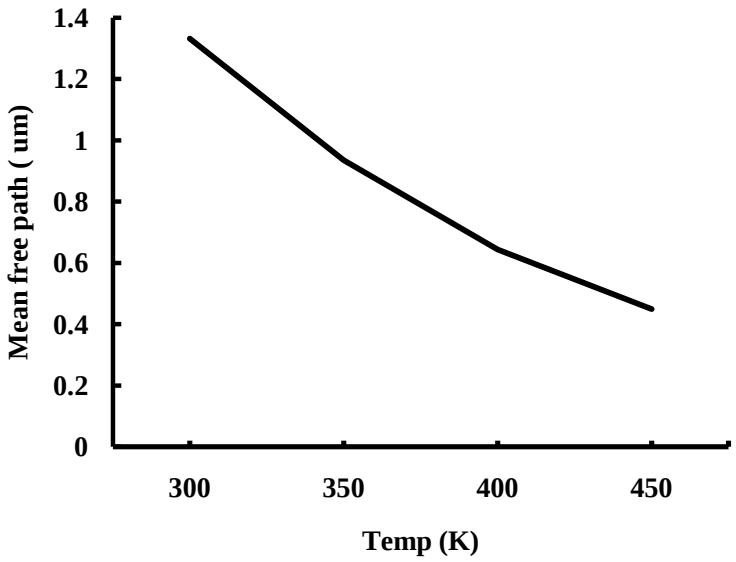

Figure4.1 Mean free path of SWCNT bundle.

As may be seen from Eq. (4.1), the resistance of SWCNT is a function of temperature dependent mean free path of electron. It is seen that the mean free path of SWCNT bundle decreases as temperature increases which states that the low bias resistance of SWCNT bundle increases with a rise in temperature at different interconnect lengths in Fig.4.1. As seen from Eqs. (4.1) - (4.8), the SWCNT bundle resistance is also a function of length. Fig.4.2 shows that in case of the long interconnect, the resistance of SWCNT bundle interconnect, is several times lower than that of copper based interconnect, with rise in temperature. Similar observations were reported by Pop et al. [44] for SWCNT interconnects. This is due to the dominance of OP absorption above room temperature.

TABLE 4.1 Impedance parameters of 1000 μm long interconnect at temperature 300 K, Technology = 22nm

Interconnect Material	Resistance (k Ω)	Capacitance (pF)	Inductance (pH)
Copper	13.67	0.015	2030.3
SWCNT Bundle	1.45	2.15	0.271

It is evident from Fig.4.2 that the resistance of SWCNT bundle, at any specific temperature, in the range 300 to 450 K, is always several times lower than that of copper-based interconnect at different lengths. Further, note from Fig.4.2 that, variation of resistance with temperature indicates the desirable effect on time duration of output pulse [60, 61]. Thus, compared with copper interconnect, SWCNT interconnect is more promising.

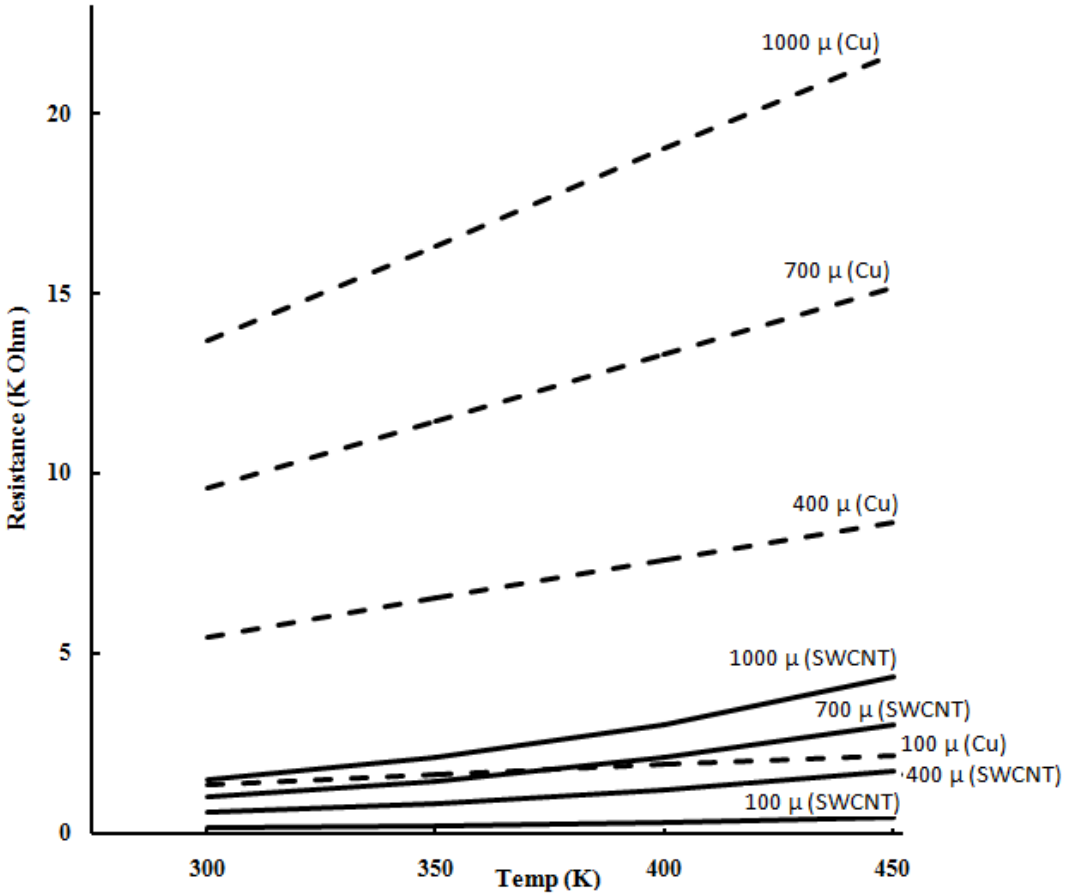

Figure4.2 Resistance of single-walled carbon nanotube bundle and copper interconnects as a function of temperature at different interconnects length.

Calculation using Eq. (3.11) as given in chapter 3, shows that inductance in an SWCNT bundle is negligible in comparison with its inductance of copper (see Table 4.1). It is of the order of a few pH. This notifies that SWCNT bundle has lower inductive effect even in case of high speed applications.

4.4 Analysis of Delay, Power dissipation and PDP

The temperature dependent circuit parameters of interconnect are known to affect its delay, power and PDP [68, 69]. As the temperature dependent MFP of an isolated

tube controls the impedance parameters of a SWCNT bundle, it is of importance to study the effect of MFP on delay, power and PDP. To analyze these effects, a distributed *RLC* circuit of interconnect has been considered as shown in Fig.3.1 (Refer Chapter 3). The signal wire is driven by a CMOS driver at 22-nm technology node [62] with clock speed of 0.04 GHz, Vdd = 0.7 V, and terminated with capacitive load of 1pF [34, 63]. For all calculation and simulation purposes, the data, shown in Table 3.1 (Refer Chapter 3), are used. In this analysis, a densely packed SWCNT bundle with tube diameter of 1 nm has been considered. Similar simulations have been carried out for copper interconnect at same technology and clock speed. In this study, simulations have been performed in the low bias region, where, CNTs depict perfect ohmic behaviour and compatible with interconnect applications.

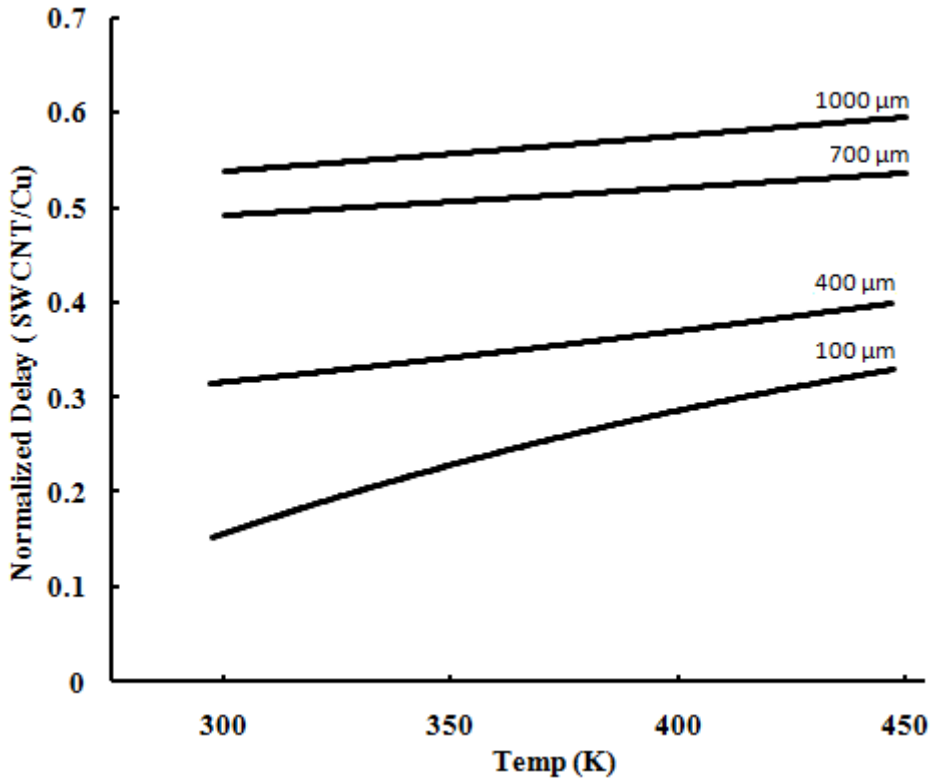

Figure4.3 Temperature dependence of normalized SWCNT bundle interconnect propagation delay at 22nm technology nodes with different interconnect lengths.

4.4.1 Propagation Delay

For both SWCNT bundle and copper interconnects, 90% delay has been extracted from the SPICE simulation results. Predictive technology model [62] has been used for the CMOS-driver. Copper-interconnect propagation delay is used to normalize corresponding SWCNT bundle-interconnect propagation delays. Fig.4.3 shows normalized delay as a function of temperature at different lengths.

TABLE 4.2 Average improvements in accuracy of delay estimation using thermally-aware model in comparison of temperature independent model

Length of interconnects (SWCNT Bundle)	Delay (≠f(T)) (ns)	Delay (=f(T)) (ns)	Improvement in delay (%)
L = 1000 µm	2.29	1.75	30.8
L = 700 µm	1.67	1.32	26.5
L = 400 µm	0.449	0.403	11.4
L= 100 µm	0.293	0.242	21.07

Results obtained through simulation reveal that the normalized delay increases with rise in temperature but these variations are observed more in copper. The variations are simply reflections of the effects of temperature variations on resistance (see Fig.4.2). Another justification due to propagation of wave in high resistance is observed from the Table 4.2 that average delay is improved by 22.44% when thermally dependent model is compared with temperature independent model of SWCNT bundle [33, 40, 49].

4.4.2 Power Dissipation

With the growing trend of portable communication equipments [70, 371], the effect of power dissipation induced by interconnects become a prime concern of VLSI industry. Reduction in scale of process technology causes the excessive increase in power associated with interconnect. The study [71] shows that for optimally buffered global interconnect systems, about 20%-30% power is changed to heat in interconnects. Recent studies in CNT [33, 34, 72] show that the tube parameters viz., center to center distance(x), tube diameter(d),length(L), width(w) etc. control the power dissipation of an SWCNT bundle. It is found that the tube diameter can regulate the power dissipation of SWCNT bundles for high speed applications due to the decrease in capacitance of SWCNT bundle which can be utilized to improve power dissipation in SWCNT bundle interconnect.

A ratio of an SWCNT bundle and copper interconnect power dissipation is illustrated in Fig.4.4 at 22 nm technology nodes. It is observed that SWCNT bundle interconnects dissipates more power than its copper counterpart for global lengths of interconnects (> 700 µm). This is due to higher value of tube capacitance over

resistance of copper [see Table 4.1]. The power dissipation of SWCNT bundle can be lesser when temperature dependent model is used instead of temperature independent model of SWCNT bundle [33, 34, 40]. Table 4.4 shows the significant average improvement of power dissipation of 7.59%.

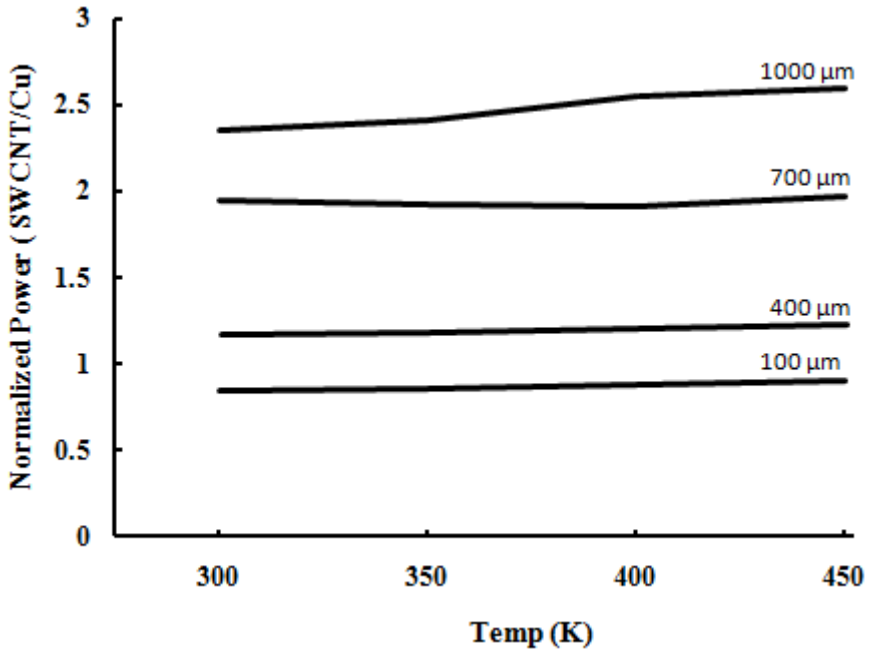

Figure4.4 Temperature dependence of normalized SWCNT bundle interconnect power at 22nm technology nodes with different interconnect lengths.

TABLE 4.3 Average improvement in accuracy of power and PDP estimation using thermally-aware model in comparison of temperature independent model

Length of interconnects (SWCNT Bundle)	**Power (≠f(T)) (µW)**	**Power (=f(T)) (µW)**	**Improvement in power** (%)	**Improvement in pdp**(%)
L = 1000 µm	88	77.2	13.98	49.16
L = 700 µm	68.6	63.6	7.86	36.5
L = 400 µm	26.7	25.05	6.58	18.73
L= 100 µm	31.4	30.8	1.94	23.48

4.4.3 Power Delay Product (PDP)

The normalized PDP as a function of temperature at different interconnect lengths is shown in Fig. 4.5. Results obtained through simulation reveal that the normalized PDP increases with rise in temperature ranging from 300K to 450K at different

interconnect lengths. It is observed that for global level of interconnects, PDP of SWCNT bundle is higher than copper interconnect. However for local level of interconnects, PDP of SWCNT bundle is lesser than copper interconnect for different values of temperature rising from 300K to 450K.

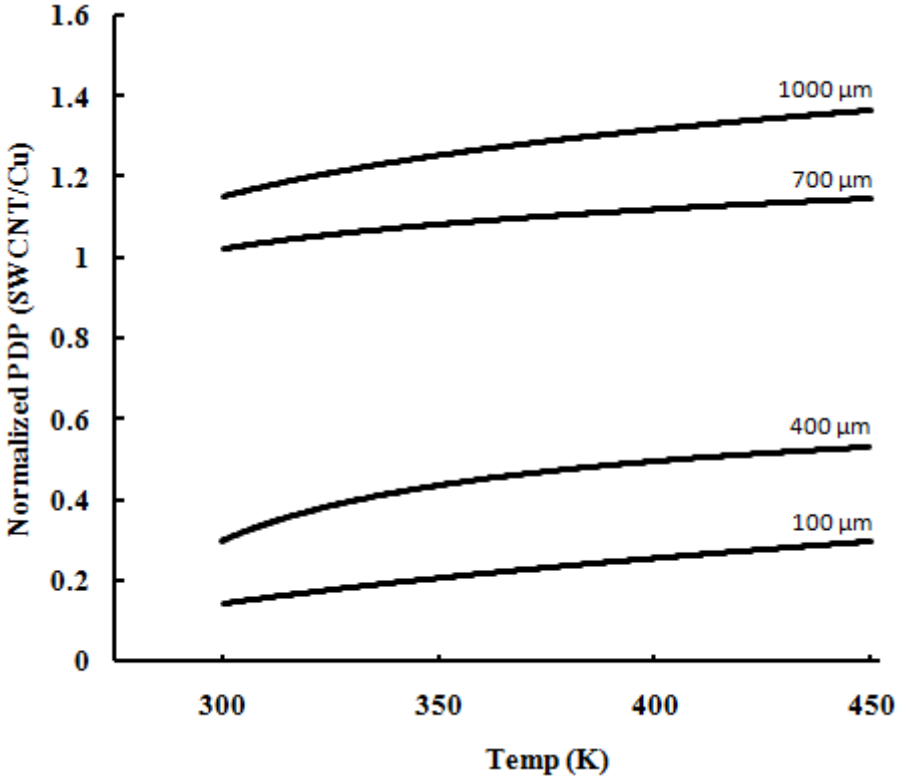

Figure 4.5 Temperature dependence of normalized SWCNT bundle interconnect Power Delay product (PDP) at 22nm technology nodes with different interconnect lengths.

The average relative improvement of 31.96% in accuracy of PDP is estimated by using thermally aware model instead of temperature independent model [33, 34, 40] (See Table 4.4).

TABLE 4.4 Average improvement in accuracy of delay, power and PDP of SWCNT bundle estimation using thermally-aware model in comparison of temperature independent model

Length of interconnects (SWCNT Bundle)	**DELAY** (%)	**POWER** (%)	**PDP (%)**
L = 1000 µm	30.8	13.98	49.16
L = 700 µm	26.5	7.86	36.5
L = 400 µm	11.4	6.58	18.73
L= 100 µm	21.07	1.94	23.48
Average Improvement	22.44	7.59	31.96

4.5 Conclusion

The effect of temperature variations ranging from temperature 300K to 450K on delay, power and PDP of SWCNT bundle interconnect has been examined. SPICE simulation results show that the propagation delay in SWCNT bundle are found to be significantly low compared to copper for all lengths, as temperature rises from 300K to 450K due to low resistance of SWCNT bundle [see Table 4.1] whereas in terms of power dissipation copper dissipates less power compared to SWCNT bundle for global lengths ($\geq$ 700 μm). In addition, PDP in SWCNT bundle are found to be more as compared to copper, for global lengths ($\geq$ 700 μm), as temperature rises from 300K to 450K because of the dominating nature of power dissipation over delay of SWCNT bundle. Our thermally-aware model achieved improvement in the delay, power and PDP estimation accuracy of SWCNT bundle of about 22.4%, 7.59% and 31.96% respectively on average. The result shows that temperature dependent model controls the delay and can be utilized to control the power and PDP of SWCNT bundle interconnect. Thus, temperature dependent circuit modeling of interconnects is the key factor for designing high performance integrated circuits.

CHAPTER 5 Temperature dependent comparison analysis between SWCNT bundle and MWCNT bundle Interconnect

5.1 Introduction

Temperature dependent, delay, power dissipation and power delay product (PDP), in MWCNT bundle interconnect have been analyzed and compared with the independent model. Temperature-dependent distributed circuit model for MWCNT bundle is presented. The results are compared with those of currently used copper interconnects at 22nm technology node. It is seen that irrespective of the type of CNTs, delay, power dissipation and PDP increase with rise in temperature from 300K to 450K at different interconnect lengths from 100µm to 1000µm. It is also observed that, with rise in temperature, CNT bundle have lower delay than that of copper for all interconnect lengths whereas reverse is true for power dissipation. In addition, with rise in temperature from 300K to 450K, for interconnect lengths at 100µm and 400µm single wall CNT (SWCNT) bundle has lowest delay compared to multi wall CNT (MWCNT) bundle and copper interconnects where as MWCNT bundle has lowest delay for interconnect lengths at 700µm and 1000µm. However, with rise in temperature, MWCNT bundle dissipates less power than SWCNT bundle for all interconnect lengths. Moreover, relative average improvement in delay, power and PDP using thermally aware model in comparison with temperature independent model is estimated. Based on simulation results, the thermally aware model of SWCNT bundle achieved improvement in delay, power and PDP estimation accuracy of about 22.44%, 7.59% and 31.96% on average whereas reverse is true for MWCNT bundle giving rise in average delay, power and PDP of about 60.67%, 0.2075% and 59.52% respectively.

5.2 Temperature-dependent equivalent circuit parameters of MWCNT bundle interconnect

An isolated MWCNT is made of several concentric rolled up graphene sheets which are known as shells as shown in Fig.5.1. The distance between the two adjacent shells is equivalent to the vander Waal gap (d)= 0.34nm [40, 45]. D_{max} and D_{min} are the

diameters of the outermost and innermost shells. The distance between centres of MWCNT to ground plan is denoted as *ht.*

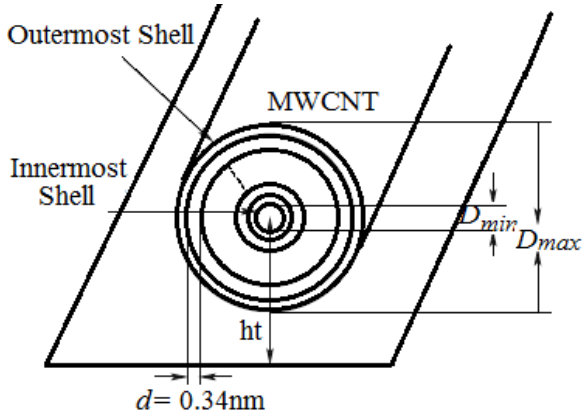

Figure 5.1 Multiwall carbon nanotubes above a ground plane.

A series RLC circuit segment is used to determine the equivalent circuit of an individual shell of isolated MWCNT as shown in Fig.3.4 (Refer Chapter 3). The number of conducting channels for a particular shell ($N_{shell}\ (D)$), number of shells (p) of MWCNT, diameter of the i_{th} shell of MWCNT are explained by Eqns. (3.17) to (3.19) as given in chapter 3. As mentioned in chapter 4 that resistance of SWCNT bundle depends on temperature similarly resistance of MWCNT bundle also depends on temperature. This is because single tube of SWCNT is known as shell in MWCNT.

The value of temperature dependent intrinsic resistance of isolated MWCNT is given as

$$R_{shell}\,(T,D) = R_Q + R_s * L = \frac{h}{N_{shell}\,(D)*e^2} + \frac{h}{N_{shell}\,(D)*e^2} * \frac{L}{\lambda_{mwcnt}\ (T,D)} \qquad (5.1),$$

Here, L *and* λ_{mwcnt} are the length and MFP of MWCNT respectively. The value of R_c is assumed to be 1KΩ per shell [45]. The temperature dependent MFP of each shell will be different because of its dependency on diameter. It can be calculated using the following Eqs. shown in [45] as:

$$\lambda_{mwcnt}\ (T,D) = (\lambda_{AC}^{-1} + \lambda_{Op,ems}^{-1} + \lambda_{Op,abs}^{-1})^{-1} \qquad (5.2).$$

The AC scattering and OP absorption and after effect of OP absorption i.e. OP emission length are given respectively as [65, 66]:

$$\lambda_{AC}(D,T) = \lambda_{AC,300}\left(\frac{300*D}{T*d_0}\right) \quad (5.3),$$

$$\lambda_{OP,abs}(D,T) = \lambda_{Op,300} * D * \left(\frac{Nop(300)+1}{Nop\ (T)*d_0}\right) \quad (5.4),$$

$$\lambda_{OP,ems} = (1/\lambda_{OP,ems}^{fld} + 1/\lambda_{OP,ems}^{abs})^{-1} \quad (5.5),$$

$$\lambda_{OP,ems}^{fld}(D,T) = \frac{\hbar op}{e.Vdd}L + \frac{Nop\ (300)+1}{Nop\ (T)+1}\lambda_{OP,300} * \frac{D}{d_0} \quad (5.6),$$

$$\lambda_{OP,ems}^{abs}(D,T) = \lambda_{OP,abs}(T) + \frac{Nop\ (300)+1}{Nop\ (T)+1}\lambda_{OP,300*}\frac{D}{d_0} \quad (5.7).$$

Here, $\lambda_{AC,300}$ ≈1600nm is the acoustic scattering length at 300 K for diameter $d_0 = 1.8nm$, D is diameter of the shell of Mwcnt bundle. $\lambda_{OP,ems}^{abs}$(T) is the OP emission MFP after absorption, $\lambda_{OP,ems}^{fld}$(T) is the former OP emission MFP event and $\lambda_{OP,300}$ ≈15 nm is the spontaneous optical emission length at 300 K.

A large number of shells are combined parallel to form an equivalent circuit of isolated MWCNT as shown in Fig.4.

$$\frac{1}{R_{isolated\ \ mwcnt\ \ (T)}} = \frac{1}{R_{shell\,(T,1)}} + \frac{1}{R_{shell\,(T,2)}} + \ldots\ldots\ldots + \frac{1}{R_{shell\,(T,P)}} \quad (5.8),$$

where, P is the total number of shells in Mwcnt.

A MWCNT bundle consists of parallel combination of a number of MWCNTs. Thus the resistance of a MWCNT bundle as a function of temperature of length L is given as

$$R_{mwcn\ t\ (bundle\ )}(T) = \frac{R_{isolated\ \ mwcnt\ \ (T)}}{N_{mwcnt}} \quad (5.9),$$

where, N_{mwcnt} is total number of MWCNTs in a bundle is given in chapter 3.

Other impedance parameters of MWCNT bundle such as inductance and capacitance are explained in chapter 3 by Eq. (3.37) and Eq. (3.40) as they are independent of temperature.

5.3 Impedance analysis

It may be seen from Eqs. (4.8), (4.9) and (5.9) that the effective low bias resistance of SWCNT bundle, copper and MWCNT bundle are function of temperature. The total temperature dependent impedance parameters of SWCNT bundle, MWCNT bundle and copper interconnects are now calculated and the data used for these calculations

are given in Table 3.1 (Refer Chapter 3) for interconnect. The width and thickness of global (~1000 µm long) interconnect are assumed to be 32 and 96 nm, respectively.

5.3.1 MWCNT versus Cu Interconnect

As evident from Eq. (5.1), the resistance of shell of isolated Mwcnt is a function of mean free path of electron. Mean free path is proven to be directly dependable on both temperature and diameter which implies that total resistance of MWCNT bundle is dependable on temperature as well as diameter [44, 45, 65]. It is observed that the mean free path of MWCNT bundle decreases as temperature increases from 300K to 450K at different interconnect lengths due to which low bias resistance of MWCNT bundle increases as shown in Fig.5.2.

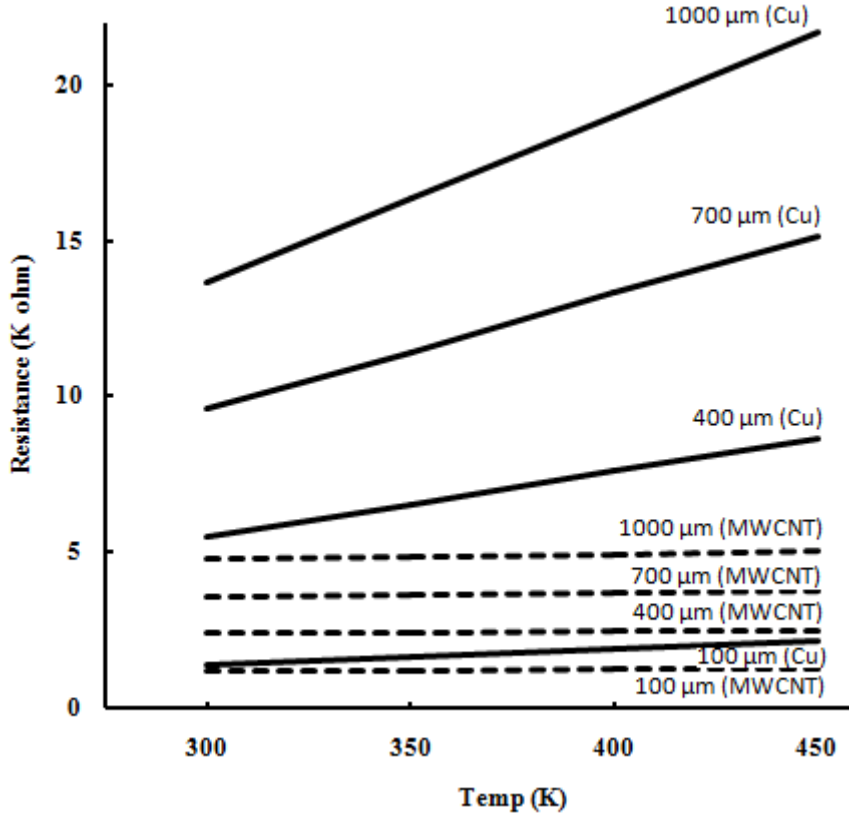

Figure5.2 Resistance of MWCNT bundle and copper interconnects as a function of temperature at different interconnects length.

As seen from Eq (5.1), the MWCNT bundle resistance is also a function of length. Fig. 5.2 shows that, the resistance of MWCNT bundle interconnect is several times lower than that of copper based interconnect, with rise in temperature in case of the global interconnect. Similar observations were stated by Banerjee et al. [40] for MWCNT interconnects. This is due to the large number of sub-bands in large-diameter shells which implies that they have large number of conducting channels

[40]. Moreover due to the dominance of OP absorption above room temperature copper has more resistance than MWCNT [44, 65]. Thus, compared with copper interconnect, MWCNT interconnect turn out to be good electrical conductors.

TABLE 5.1 Impedance parameters of 1000 µm long interconnect at temperature 300 K, Technology = 22nm

Interconnect materials	Resistance (k Ω)	Capacitance (pF)	Inductance (pH)
Copper	13.67	0.015	2030.3
SWCNT Bundle	1.45	2.15	0.271
MWCNT Bundle	4.77	0.11	0.1

Calculation using Eq. (43) shows that inductance in an MWCNT bundle is negligible in comparison with its inductance of copper (see Table 5.1).It is of the order of a very few pH. This states that MWCNT bundle has lower inductive effect even in case of high speed applications.

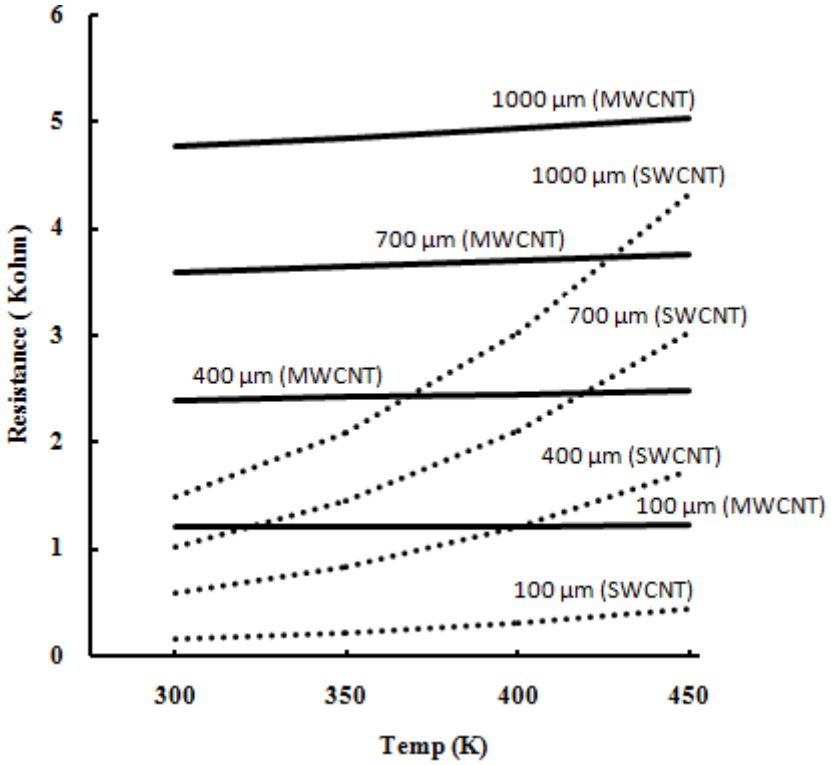

Figure5.3 Resistance of MWCNT and SWCNT bundle as a function of temperature.

5.3.2 MWCNT versus SWCNT Interconnect

From the above results it is seen that both SWCNT bundle and MWCNT bundle are better interconnects than Copper interconnects. Now the comparison is done between SWCNT bundle and MWCNT bundle. It is observed as shown in Fig.5.3 that

resistance of MWCNT bundle is larger than that of the resistance of SWCNT bundle as temperature rises from 300K to 450K for different interconnect lengths. As seen from Eq. (3.16) (Refer Chapter 3) number of conducting channels of shell of MWCNT is a function of diameter due to which different shells have different mean free path as temperature increases. The diameter of shell of MWCNT decreases due to which mean free path of MWCNT also decreases. Thus resistance of MWCNT bundle increases in comparison with SWCNT bundle.

5.4 Performance analysis

The temperature dependent circuit parameters of interconnect are known to affect its delay, power and PDP [67, 68]. As the temperature dependent MFP of an isolated tube controls the impedance parameters of a CNT bundle, it is of importance to study the effect of MFP on delay, power and PDP. To analyze these effects, a distributed *RLC* circuit of interconnect has been considered as explained in chapter 3. The signal wire is driven by a CMOS driver at 22-nm technology node [68] with clock speed of 0.04 GHz, Vdd = 0.7 V, and terminated with capacitive load of 1pF [32, 63].

For all calculation and simulation purposes, the data, shown in Table 3.1 (Refer Chapter 3), are used. In this analysis, a densely packed SWCNT bundle with tube diameter of 1 nm and MWCNT bundle of D_{max} =32nm has been considered. Similar simulations have been carried out for copper interconnect at same technology and clock speed. In this study, simulations have been performed in the low bias region, where, CNTs depict perfect ohmic behaviour and compatible with interconnect applications.

5.4.1 Temperature dependent propagation delay

For SWCNT bundle, MWCNT bundle and copper interconnects, 90% delay has been extracted from the SPICE simulation results. Predictive technology model [62] has been used for the CMOS-driver. Copper-interconnect propagation delay is used to normalize corresponding SWCNT bundle-interconnect as well as MWCNT bundle-interconnect propagation delays. Fig.5.4 shows normalized delay of CNT as a function of temperature at different lengths. Results obtained through simulation reveal that the normalized delay of SWCNT bundle interconnect increases with rise in temperature. It is observed that delay of SWCNT bundle is less than copper interconnect delay [44, 65].

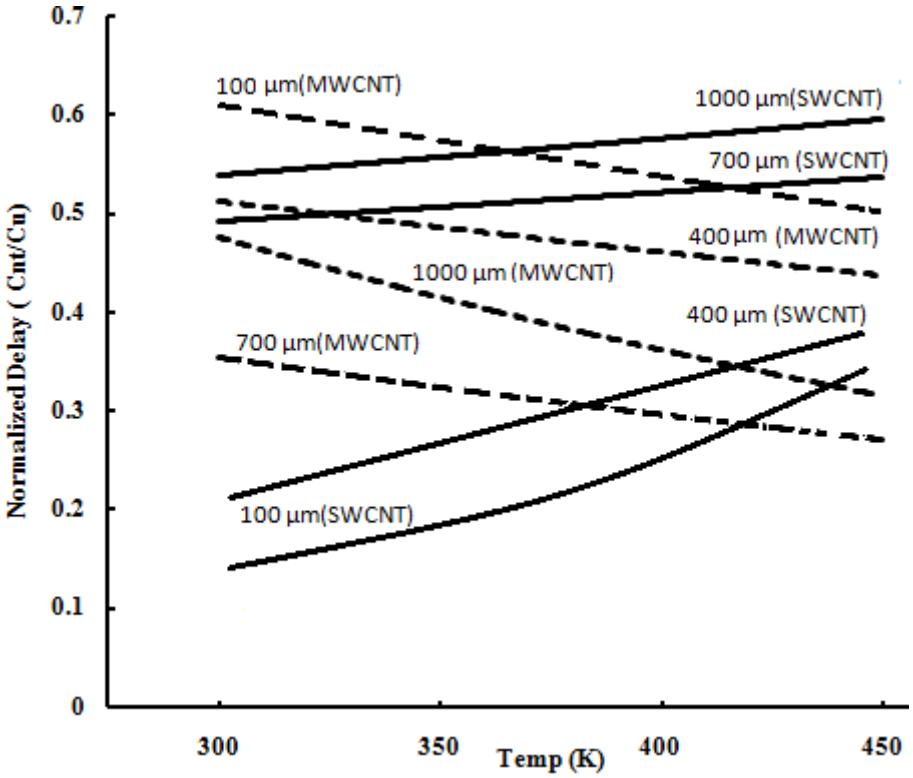

Figure5.4 Temperature dependence of normalized SWCNT bundle and MWCNT bundle interconnect propagation delay at 22nm technology nodes with different interconnect lengths.

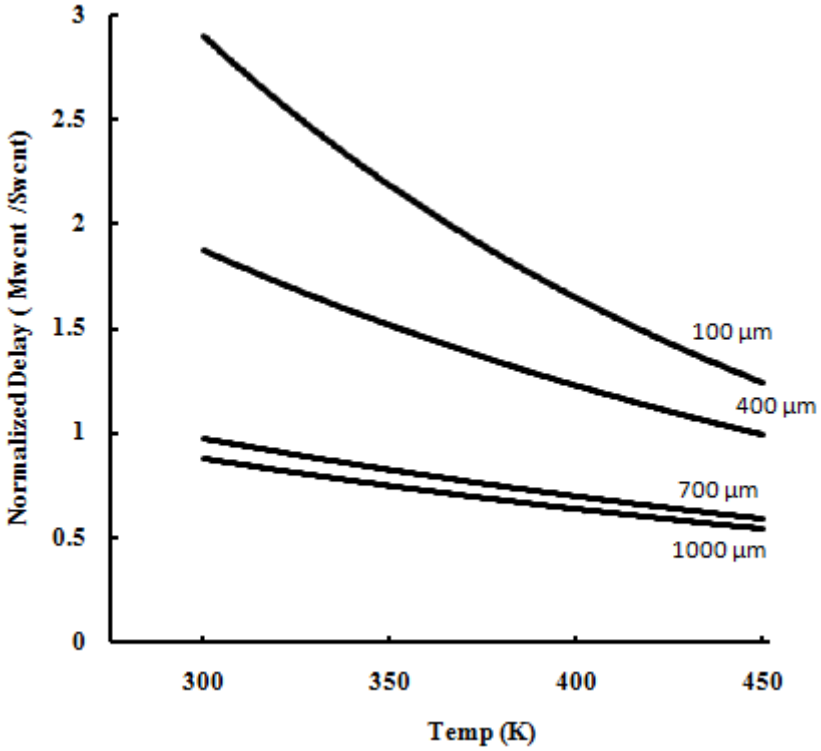

Figure5.5 Temperature dependence of normalized MWCNT bundle interconnect propagation delay at 22nm technology nodes with different interconnect lengths.

Fig 5.4 also shows that normalized delay of MWCNT bundle interconnect decreases with rise in temperature due to the dominance of delay of copper at different

interconnect lengths. The reason behind this is that the delay of copper interconnects increases more rapidly, as temperature rises from 300K to 450K, as compared to the delay of the MWCNT bundle [40, 45].

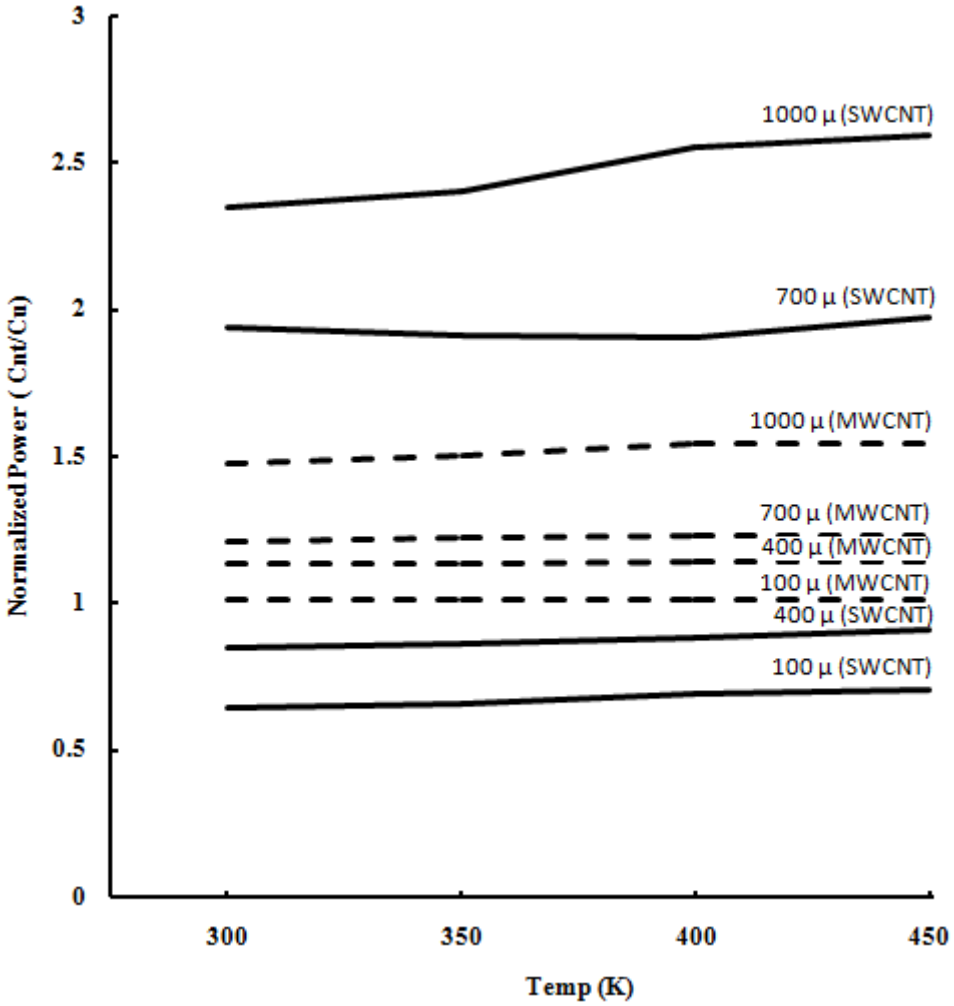

Figure5.6 Temperature dependence of normalized SWCNT bundle and MWCNT bundle interconnect power at 22nm technology nodes with different interconnect lengths.

Fig.5.5 shows the ratio of delay of MWCNT bundle and SWCNT bundle. It is observed that at global level (> 700µm), the delay of MWCNT bundle is less in comparison with SWCNT bundle with rise in temperature from 300K to 450K. It is due to the fact that MWCNT has large diameter at global interconnect level which reduces the number of MWCNT in bundle and causes decrease in resistivity of MWCNT for long lengths. However, at local and intermediate level (>100µm), the delay of SWCNT bundle is less than the MWCNT bundle [40,45].

5.4.2 Temperature dependent power dissipation

With the growing trend of portable communication equipments [70, 71], the effect of power dissipation induced by interconnects become a prime concern of VLSI industry. Reduction in scale of process technology causes the excessive increase in power associated with interconnect. The study [71] shows that for optimally buffered global interconnect systems, about 20%-30% power is changed to heat in interconnects. Recent studies in CNT [33, 34, 72] show that the tube parameters viz., center to center distance(x), tube diameter(d),length(L), width(w) etc. control the power dissipation of a CNT bundle. It is found that the tube diameter can regulate the power dissipation of CNT bundles for high speed applications due to the decrease in capacitance of CNT bundle which can be utilized to improve power dissipation in CNT bundle interconnect.

A ratio of a CNT bundle and copper interconnect power dissipation is illustrated in Fig.5.6 at 22 nm technology nodes. It is observed that SWCNT bundle interconnects dissipates more power than its copper counterpart for global lengths of interconnects (> 700 µm). However MWCNT bundle dissipates more power than copper for all interconnect lengths as shown in Fig.5.6. This is due to higher value of tube capacitance over resistance of copper [see Table 5.1].

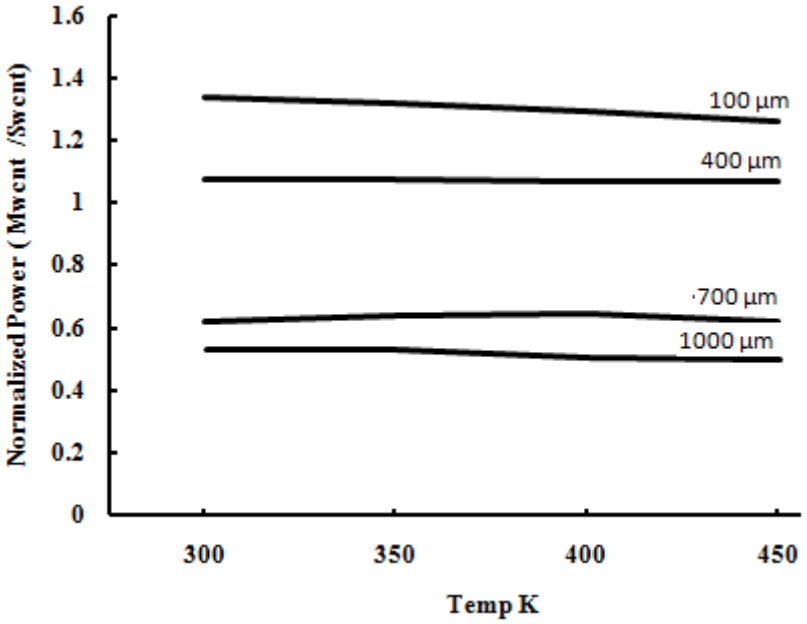

Figure5.7 Temperature dependence of normalized MWCNT bundle interconnect power dissipation at 22nm technology nodes with different interconnect lengths.

It is observed in Fig.5.7 that MWCNT bundle interconnects dissipates less power than SWCNT bundle for global lengths of interconnects where as reverse is true for local length of interconnects.

5.4.3 Temperature dependent power delay product (PDP)

The normalized PDP as a function of temperature at different interconnect lengths is shown in Fig. 5.8 and Fig. 5.9. Results obtained through simulation reveal that the normalized PDP increases with rise in temperature ranging from 300K to 450K at different interconnect lengths. Fig.5.8 shows that for global level of interconnect, PDP of SWCNT bundle is more than copper interconnect whereas for local level of interconnect PDP of SWCNT is less than copper interconnect. It is also observed that for all different lengths of interconnect, PDP of MWCNT bundle is less than the copper interconnect.

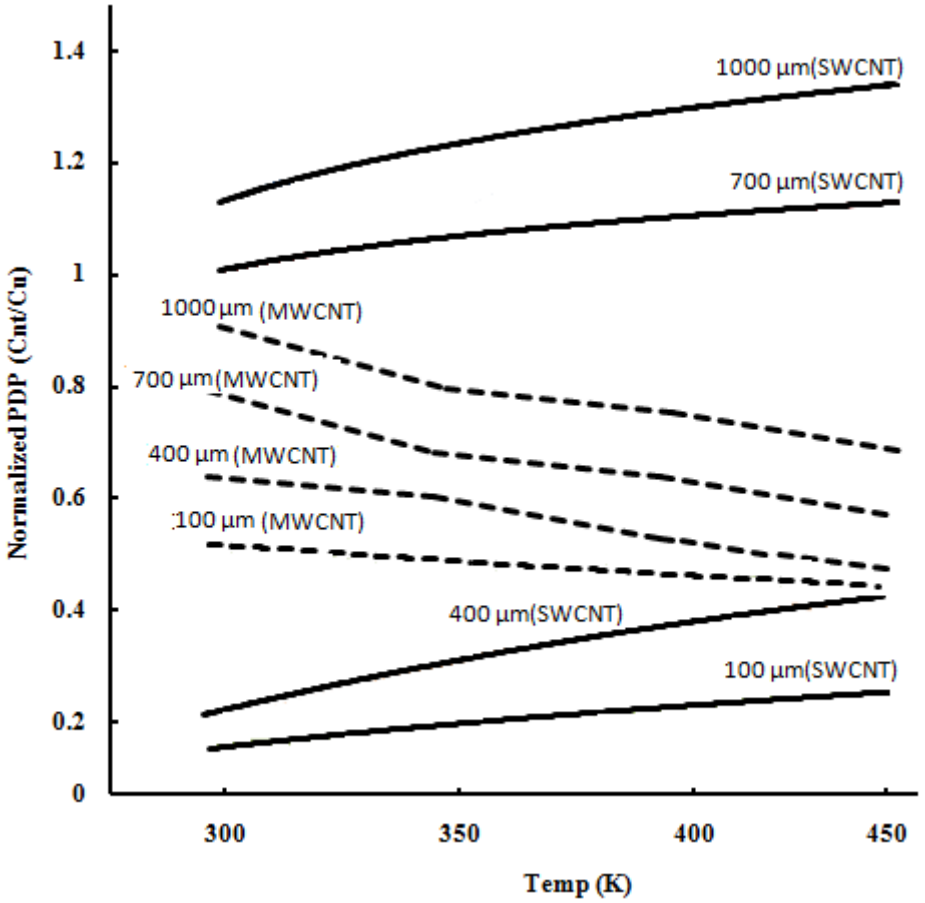

Figure 5.8 Temperature dependence of normalized SWCNT bundle and MWCNT bundle interconnect Power Delay product (PDP) at 22nm technology nodes with different interconnect lengths.

Fig 5.9 shows that PDP of MWCNT bundle is lesser than SWCNT bundle for global length of interconnects whereas for local length of interconnect, PDP of MWCNT bundle is higher than SWCNT bundle. The average relative improvement of 31.96%

in accuracy of PDP is estimated by using thermally aware model instead of temperature independent model [33, 34, 40] (See Table 5.4).

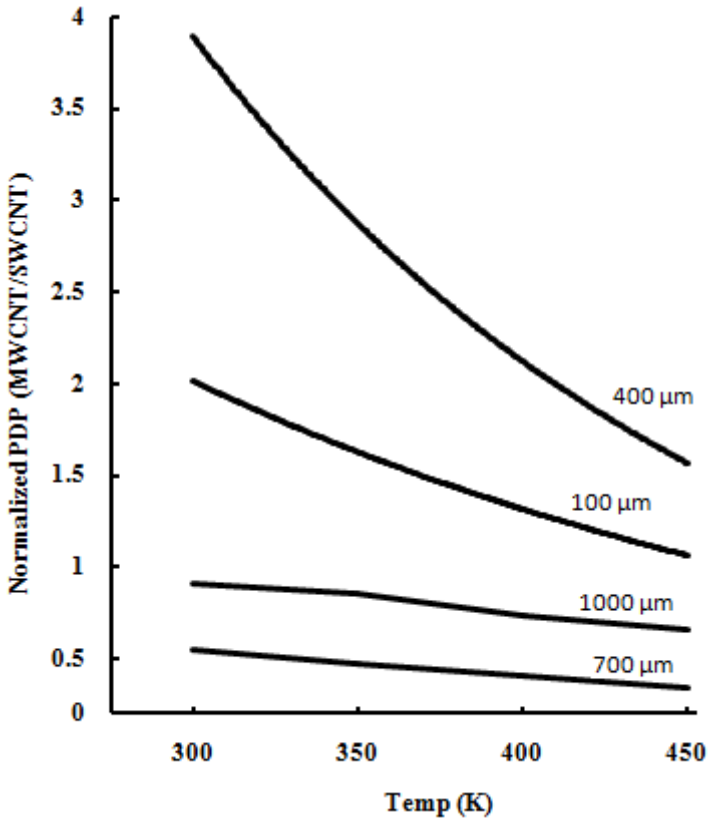

Figure 5.9 Temperature dependence ratio of MWCNT bundle and SWCNT bundle interconnect Power Delay product (PDP) at 22nm technology nodes with different interconnect lengths.

5.5 Comparison between temperature dependent and independent analysis

5.5.1 SWCNT Bundle

The temperature dependent performance analysis of CNT bundle is compared with temperature independent performance analysis. It is represented in Table 5.2 that delay of temperature dependent SWCNT bundle interconnect is less than temperature independent model of SWCNT bundle interconnect for different interconnect length increasing from 100µm to 1000µm. This is due to the reason that on increasing temperature mean free path of temperature dependent SWCNT bundle decreases for every length of interconnect. Therefore resistance of temperature dependent SWCNT bundle interconnect decreases on increasing temperature thereby reducing delay of temperature dependent SWCNT bundle interconnect. It is observed from the Table 5.4 that for SWCNT bundle due to propagation of wave in high resistance that

average delay is improved by 22.44% when thermally dependent model is compared with temperature independent model of SWCNT bundle [33, 40, 49].

TABLE 5.2 Average improvement in accuracy of delay estimation using thermally-aware model in comparison of temperature independent model

Length of interconnects (SWCNT Bundle)	**Delay (≠f(T)) (ns)**	**Delay (=f(T)) (ns)**	**Improvement in delay (%)**
L = 1000 µm	2.29	1.75	30.8
L = 700 µm	1.67	1.32	26.5
L = 400 µm	0.449	0.403	11.4
L= 100 µm	0.293	0.242	21.07

The power dissipation of SWCNT bundle can be lesser when temperature dependent model is used instead of temperature independent model of SWCNT bundle [33, 34, 40]. It is observed from the Table 5.3 that for global level of interconnect, temperature dependent power of SWCNT bundle is significantly less than the temperature independent power of SWCNT bundle whereas for local level of interconnect, the difference in power is comparable to each other.

TABLE 5.3 Average improvement in accuracy of power and PDP estimation using thermally-aware model in comparison of temperature independent model

Length of interconnects (SWCNT Bundle)	**Power (≠f(T))(µW)**	**Power (=f(T))(µW)**	**Improvement in power** (%)	**Improvement in pdp**(%)
L = 1000 µm	88	77.2	13.98	49.16
L = 700 µm	68.6	63.6	7.86	36.5
L = 400 µm	26.7	25.05	6.58	18.73
L= 100 µm	31.4	30.8	1.94	23.48

Table 5.4 shows the significant improvement of average delay, power dissipation of SWCNT bundle of 22.4% and 7.59% respectively. The average relative improvement of 31.96% in accuracy of PDP of SWCNT is estimated by using thermally aware model instead of temperature independent model [33, 34, 40] (See Table 5.4).

TABLE 5.4. Average improvement in accuracy of delay, power and PDP of SWCNT bundle estimation using thermally-aware model in comparison of temperature independent model

Length of interconnects (SWCNT bundle)	**Delay** (%)	**Power** (%)	**PDP (%)**
L = 1000 µm	30.8	13.98	49.16
L = 700 µm	26.5	7.86	36.5
L = 400 µm	11.4	6.58	18.73
L= 100 µm	21.07	1.94	23.48
Average Improvement	22.44	7.59	31.96

5.5.2 MWCNT Bundle

In MWCNT bundle it is seen from Table 5.5 that average delay is increased by 60.67% when thermally dependent model is compared with temperature independent model of MWCNT bundle [33, 40, 49]. This is due to the fact that for independent model mean free path of MWCNT bundle is larger than the temperature dependent mean free path. As mean free path is inversely proportional to resistance of MWCNT bundle the resistance of temperature independent model of MWCNT bundle decreases due to which delay of temperature independent model decreases.

TABLE 5.5 Average increase in accuracy of delay of MWCNT bundle estimation using thermally-aware model in comparison of temperature independent

Length of interconnects (MWCNT Bundle)	**Delay (≠f(T)) (ns)**	**Delay (=f(T)) (ns)**	**Increase in delay (%)**
L = 1000 µm	1.43	1.65	15.38
L = 700 µm	0.786	1.168	48.6
L = 400 µm	0.582	1.1014	89.2
L= 100 µm	0.362	0.405	89.5
Average Increase	0.79	1.081	60.67

In the Table 5.6 the power dissipation of MWCNT bundle is almost equal when temperature dependent model is used instead of temperature independent model of MWCNT bundle [33, 34, 40]. On an average the power dissipation of MWCNT bundle for temperature dependent model is improved by 0.2075% in comparison with

independent model (see Table VII). Results obtained from simulation reveals that PDP of temperature dependent model of MWCNT bundle is larger than the independent model due to the dominance of delay of independent model of MWCNT bundle and the average increase in PDP is 59.52%.

TABLE 5.6 Average improvement in accuracy of power and increase in PDP of MWCNT bundle estimation using thermally-aware model in comparison of temperature independent model

Length of interconnects (MWCNT Bundle)	**Power (≠f(T)) (µW)**	**Power (=f(T)) (µW)**	**Improvement in power** (%)	**Increase in pdp**(%)
L = 1000 µm	48.6	48.4	0.41	15.86
L = 700 µm	39.64	39.58	0.15	48.37
L = 400 µm	33.62	33.57	0.14	89.05
L= 100 µm	33.15	33.08	0.13	84.8
Average improvement	38.75	38.65	0.2075	59.52

5.6CONCLUSION

The effect of temperature variations ranging from temperature 300K to 450K on delay, power and PDP of CNT bundle interconnect has been examined. SPICE simulation results show that the propagation delay in SWCNT bundle are found to be significantly low compared to copper for all lengths, as temperature rises from 300K to 450K due to low resistance of SWCNT bundle [see Table 5.1] whereas in terms of power dissipation copper dissipates less power compared to CNT bundle for lengths (≥ 100 µm). However, it is observed that the propagation delay in MWCNT bundle are found to be low compared to SWCNT bundle for global lengths (≥ 700 µm), as temperature rises from 300K to 450K but reverse is true for local and intermediate interconnect lengths (> 100 µm).

In terms of power dissipation MWCNT bundle dissipates less power compared to SWCNT bundle for all lengths, as temperature increases from 300K to 450K. In addition, PDP in SWCNT bundle are found to be more as compared to copper, for global lengths (≥ 700 µm), as temperature rises from 300K to 450K because of the dominating nature of power dissipation over delay of SWCNT bundle. Moreover,

PDP in MWCNT bundle are found to be less as compared to copper, for all interconnect lengths, as temperature rises from 300K t0 450K. Our thermally-aware model achieved improvement in the delay, power and PDP estimation accuracy of SWCNT bundle of about 22.4%, 7.59% and 31.96% respectively on average.

The result shows that temperature dependent model controls the delay and can be utilized to control the power and PDP of CNT bundle interconnect. For long (global levels) interconnects, MWCNT bundle interconnects show significant improvement in temperature dependent delay as compared to Cu wires and SWCNT bundles. Thus, temperature dependent MWCNT bundle are easier to fabricate with less concern about chirality and they can be attractive for global level interconnects and temperature dependent SWCNT bundle are promising interconnect at local levels.

CHAPTER 6

Conclusion and Future Scope

6.1 Introduction

Due to advancement in technology scaling, the performance of conventional interconnect material (copper) is degraded due to electro migration, scattering phenomena, etc. The mean free path of CNT is larger than the copper due to which it makes more prominent material for future interconnect application. This calls for the detailed analysis of CNTs.

6.2 Carbon Nanotubes as VLSI interconnects

The performance of CNT at deep submicron is more appreciable than the copper due to the unique properties of CNT such as thermal stability, current carrying capacity, mechanical stability, etc. The isolated CNTs posses' high resistance due to which they are combined together to form bundle of CNTs. This reduces the total impedance of the interconnect wire. MWCNT bundles are easier to fabricate and have similar performance than SWCNT bundle. The electro-thermal study of SWCNT revealed that temperature plays an important role in altering the resistance of long SWCNTs.

6.3 Influence of length on performance of CNT bundle interconnect

In chapter 3 it is seen that for global lengths of interconnect MWCNT bundle are more appropriated interconnect at room temperature in comparison with copper as well as SWCNT bundle. The performance in terms of delay, power and PDP of CNT as well as copper increases on increasing length of interconnect. For local length of interconnect, SWCNT bundle shows better performance as compared to MWCNT bundle on increasing length of interconnect.

6.4 Temperature dependent performance analysis of SWCNT bundle

In chapter 4, temperature dependent performance analysis of SWCNT bundle and copper interconnect has been compared with each other as well as with the temperature independent model of SWCNT bundle for different interconnects lengths.

SPICE simulations results are used to compare SWCNT bundle interconnect delay, power and PDP with that of copper interconnects at different temperature rising from 300K to 450K at different length of interconnects. SPICE simulation results bring to light that delay, power and PDP of SWCNT bundle interconnect increases with rise in temperature from 300K to 450K at different interconnect lengths from 100μm to 1000μm due to increase in resistance on increasing temperature. It is revealed that with rise in temperature, SWCNT bundle has lower delay than that of copper for all interconnect lengths whereas reverse is true for power dissipation due to the fact that resistance of copper is significantly higher than SWCNT bundle. It is also seen that temperature dependent model of SWCNT bundle accomplished average improvement in delay, power and PDP of 22.4%, 7.59% and 31.96% respectively compared with temperature independent model of SWCNT bundle.

6.5 Temperature dependent comparison analysis between SWCNT bundle and MWCNT bundle

Thermally aware circuit model for MWCNT bundle is presented in the chapter. It shows that the performance in terms of delay, power and PDP of MWCNT bundle is better than the copper interconnect as temperature rises from 300K to 450K for different interconnect lengths. This is due to the reasons that mean free path of MWCNT bundle is significantly higher than the copper. However it is observed that temperature independent model of MWCNT bundle is better than the thermally aware model of MWCNT because mean free path of temperature independent model is more than the mean free path of temperature dependent model. It is also found that at global level (>700μm) of interconnect lengths, performance of MWCNT bundle is better than SWCNT bundle on rising temperature from 300K to 450K whereas at local level (≥100μm) of interconnect lengths, performance of SWCNT bundle is better than MWCNT bundle.

6.6 Future Scope

The scope of MWCNT bundle as an interconnect material in future design of integrated circuits has been explored. Since MWCNT bundle are easier to fabricate with less worrying about chirality, need to be examined in future. Crosstalk and noise immunity of MWCNT bundles are still to be analysed. Different interconnect material

can be used to made single interconnect material inside the bundle known as mixed CNT interconnect formed by parallel combination of SWCNT and MWCNT bundle. Captivating and high yielding research on these kinds of interconnects on the basis of crosstalk, noise immunity could be taken out.

APPENDIX

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