Temperature Dependent Performance Analysis of Mixed-MWCNT Bundle as VLSI Interconnects

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DOCTOR OF PHILOSOPHY

Submitted by

Pardeep Kumar Jindal

(Registration No. 901506011)

under the supervision of

Dr. Karmjit Singh Sandha

Assistant Professor, ECED

Electronics and Communication Engineering

Thapar Institute of Engineering and Technology

Patiala-147001, India

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Declaration

I hereby declare that the work being presented in this thesis entitled "**TEMPERATURE DEPENDENT PERFORMANCE ANALYSIS OF MIXED-MWCNT BUNDLE AS VLSI INTERCONNECTS**", in partial fulfilment of the requirements for the award of degree of **Doctor of Philosophy** submitted in Department of Electronics and Communication Engineering, Thapar Institute of Engineering and Technology, Patiala, is an authentic record of my own work carried out under the supervision of Dr. Karmjit Singh Sandha, Assistant Professor, Department of Electronics and Communication Engineering, Thapar Institute of Engineering and Technology, Patiala and refers other researcher works which are duly listed in the reference section. The matter presented in this thesis has not been submitted for the award of any other degree of this or any other University.

Date: 17/5/2021

Pardeep Kumar Jindal

Registration No. 901506011

This is to certify that the above statement made by the candidate is correct to the best of my knowledge and belief.

Date: 17/5/21

Dr. Karmjit Singh Sandha (Supervisor)

(Assistant Professor, ECED)

TIET (Deemed to be University)

Patiala-147001, Punjab, India

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PARDEEP KUMAR JINDAL

Abstract

Since 1970, the functionality and performance of integrated circuits (ICs) have been improving year after year at scaled-down technology nodes. The complexity of ICs increase because of increasing the number of functional blocks per chip. The functional blocks per IC increase, which accumulate a large area of a chip because the number of active and passive components is also increased. Thus, the dimensions of components need to be minimized to fabricate a large number of active and passive components on a single-chip. The size of the device gets minimum; however, high speed of operation and less power consumption require for high-performance ICs.

For scaled-down technology nodes, the size of VLSI-IC reduces by minimizing the size of active and passive components and the size of interconnects. Interconnect is a thin conducting line, which provides the path to various parts of the IC such as power supply, ground, input signal and clock pulse. At nanotechnology nodes, the performance of IC dominates by the interconnect length and material is used as VLSI interconnect. The conventional copper (Cu) material is used as interconnect for high-performance VLSI-IC design. However, Cu has few significant issues at scaled-down technology nodes (particularly below 45nm), which is reported in the literature. These issues are low current density, short mean free path (MFP) and high resistivity at deep submicron (DSM) technology nodes. Therefore, replacing the Cu with new material at DSM technology nodes is necessary.

Carbon nanotube (CNT) has been discovered as new conducting material. It may be considered as a good candidate to replace Cu interconnect because CNT has high current density, long MFP and low resistivity at DSM technology nodes. CNT is made-up of a graphene sheet rolling into a cylinder. CNTs are classified as single-walled CNT (SWCNT) and multi-walled CNT (MWCNT). SWCNT is developed by rolling a single sheet of graphene into a cylinder with a diameter of few to several nm. However, MWCNT is made up of rolling two or more graphene sheets into the cylinder, concentrically. The fabricated MWCNT has a diameter ranging from a few to several tens of nm.

In the literature, various CNT bundles are proposed such as Mixed-CNT, MWCNT and SWCNT

bundles, which are considered as interconnect for VLSI-ICs design. Further, bundles of SWCNT have several SWCNT with a fixed diameter, which is difficult to fabricate because there is no control on the growth process as compared to MWCNT. The modeling of MWCNT is complex as compared to SWCNT bundles because MWCNT has a various number of individual shells and each shell has a different diameter. In contrast, SWCNT bundles have only a single shell of fixed diameter.

Further, the Mixed-MWCNT (MMT) bundle is established for VLSI interconnect at DSM technology nodes, which is a mixer of two or more differently-sized MWCNTs. The relative bundle is denser than MWCNT bundle because some MWCNTs of small diameter are inserted into the vacant space at side wall, corner and four adjacent MWCNTs. Thus, the conductivity of MMT increased as compared to MWCNT bundle because MMT has a large number of conducting channels. The performance of MMT as a VLSI interconnect needs to calculate the actual performance for global level interconnects at DSM technology nodes.

This thesis work presents the proposed MMT nanostructure as VLSI interconnect at DSM technology nodes. The proposed MMT has two types of MWCNTs of different diameters such as MWCNT_L (means large diameter MWCNT) and MWCNT_S (denotes small diameter MWCNT), which is considered as global interconnect for DSM technology nodes. The parasitic of MMT is examined by writing the analytical equations in MATLAB tool to develop the equivalent single-conductor (ESC) model. The resistance of MMT nanostructure is obtained for global level interconnect at 32, 22 and 16nm technology nodes. The resistance of MMT increases with increasing length from 400 to 2000μm and also increases for scaled technology nodes. Further, the developed ESC model of MMT nanostructure as global interconnect length is considered to examine the performance in terms of delay, power and PDP at DSM technology nodes. Similarly, the ESC model of Cu interconnect has also been developed to examine the performance of parameters under-consideration for MMT nanostructure at technology nodes such as 32, 22 and 16nm. It reveals that the performance of MMT nanostructure outperforms Cu at DSM technology nodes for global level interconnect.

A variable temperature influences the performance of VLSI interconnect at DSM technology nodes. Therefore, the impact of temperature on the performance of MMT interconnect needs calculation to understand the actual performance under various thermal conditions at DSM technology nodes. Temperature-dependent ESC model of MMT nanostructure as global interconnect length is developed at DSM technology nodes viz. 32, 22 and 16nm for temperature

range (200-450K). The mathematical equations are derived to obtain parasitic of MMT interconnect, which is influenced by a variable temperature range (200-450K).

The parasitic of the MMT interconnect is calculated under various thermally-aware factors for variable environmental conditions at DSM technology nodes. These factors are due to electron-phonon scattering, which results from grain boundary and surface scattering of MMT nanostructure at DSM technology nodes. The MMT interconnect consists of two types of scattering – electron-phonon and electron-electron scattering. The electron-phonon scattering shows a significant impact on their parasitic; however, electron-electron scattering phenomena have a negligible impact on overall scattering phenomena. This temperature-dependent scattering influence the MFP of MMT nanostructure, which further affects the impedance parameters.

Temperature-dependent parasitic of MMT nanostructure is developed and analyzed at DSM technology nodes. Temperature-dependent resistance of MMT interconnect is compared with temperature-independent resistance on a variable temperature range between 200 and 450K at DSM technology nodes. The temperature-dependent impedance parameters are used to calculate the performance such as delay, power and PDP of proposed MMT nanostructure. The calculated performance of MMT for global interconnect length in terms of delay, power and PDP are analyzed and compared at DSM technology nodes on a variable temperature range (200-450K).

Similarly, temperature-dependent ESC models of MWCNTB, SWCNTB and Cu nanostructure as global level interconnect (1000μm) are presented to obtain the performance parameters for MMT nanostructure at DSM technology nodes. Further, the developed ESC models of MWCNTB, SWCNTB and Cu are simulated with the help of the SPICE tool to evaluate the performance at DSM technology nodes. The obtained results for SWCNTB, MWCNTB and Cu are compared with MMT interconnect results at DSM technology nodes on the variable temperature range. The comparative analysis shows that the performance of MMT nanostructure performs better than Cu, SWCNTB and MWCNTB as global level VLSI interconnect at DSM technology nodes (32, 22 and 16nm) for the entire temperature range (200-450K).

It reveals that the performance of MMT nanostructure outperforms Cu, SWCNTB and MWCNTB as global level VLSI interconnect length on a variable temperature range (200-450K) at DSM technology nodes viz. 32, 22 and 16nm. The MMT nanostructure may be used as a global level VLSI interconnect at DSM technology nodes under thermally-aware environmental conditions.

List of Publications

SCI/SCIE INDEXED

1. Pardeep Kumar Jindal and Karmjit Singh Sandha. Thermally-Aware Modeling and Performance Analysis of Mixed-MWCNTB as Very Large Scale Integrated Interconnects Material for Nano-Electronic Integrated Circuits Design. *"Journal of Nanoelectronics and Optoelectronics"*, 14(9): 1255-1266, 2019. (**Impact factor 1.069**).

2. Pardeep Kumar Jindal and Karmjit Singh Sandha. Influence of variable temperature on performance of mixed-MWCNT, MWCNT and SWCNT nanostructures as interconnects for high-performance VLSI-IC design. *"Journal of Materials Science: Materials in Electronics, Springer"*, 31(3): 1828-1838, 2020. (**Impact factor 2.478**).

3. Pardeep Kumar Jindal and Karmjit Singh Sandha. Impact of temperature on the performance of MMT, MWCNTB, SWCNTB and Copper Nano-interconnect. *"Journal of Circuits, Systems, and Computers"*. [Under Revision]

SCOPUS INDEXED

1. Pardeep Kumar Jindal and Karmjit Singh Sandha. Performance of Mixed-MWCNT Structures as VLSI Interconnect for Nanometer Technology Nodes. *"International Journal of Recent Technology and Engineering (IJRTE), ISSN: 2277-3878"*, 8(1), 2708-2713, 2019.

Acronyms and Abbreviations

Abbreviation	Description
CMOS	Complementry Metal Oxide Seniconducor
CNTs	Carbon Nanotubes
DSM	Deep Submicron
EEC	Electrical equivalent circuit
EEMC	Electrical equivalent Multi-conductor
EESC	Electrical equivalent Single-conductor
ESC	Equivalent Single-Conductor
GNR	Graphene Nanoribbon
GSI	Giant Scale integration
ICs	Integrated Circuits
LSI	Large Scale integration
MCTL	Multi-conductor Transmission line
MFP	Mean Free Path
MMT	Mixed-MWCNT Bundle
MSI	Medium Scale integration
MWCNT	Multi-Walled CNT
MWCNTB	MWCNT Bundle
nm	nanometer
PDP	Power Delay Product
SSI	Small Scale integration
SWCNT	Single-Walled CNT
SWCNTB	SWCNT Bundle
ULSI	Ultra Large Scale integration
VLSI	Very Large Scale integration

Glossary of Symbols

Symbol	Description
$C_{q/sh}$	Quantum capacitance of individual shell of MWCNT
C_s	Shell-to-Shell capacitance
C_e	Electrostatic capacitance
C_{ESC}	Total Cacpacitance of MMT
C_{ESC_L}	Total Cacpacitance of Large MWCNTs
C_{ESC_S}	Total Cacpacitance of Small MWCNTs
C_L	Load Capacitance
C_o	Output Capacitance of Driver
C	Interconnect capacitance
D_{max}	Maximum Diameter
D_{min}	Minimum Diameter
D_{max_L}	Maximum Diameter of Large MWCNT
D_{max_S}	Maximum Diameter of Small MWCNT
D_g	Diameter of any gth Shell
D_{g_L}	Diameter of any gth Shell of large MWCNT
D_{g_S}	Diameter of any gth Shell of Small MWCNT
e	electron charge
G_t	Conductance
H	Interconnect Height
h_t	Height from ground plane to center of outermost MWCNT
h	Plank's constant
L_i	Interconnect Length
L	Interconnect Inductance
L_{sh}	Total Inductance of individual shell of MWCNT
L_m	Magnetic Inductance of individual shell of MWCNT
$L_{k/sh}$	Kinetic Inductance of individual shell of MWCNT

L_{ESC}	Total Inductance of MMT
L_{mESC}	Magnetic inductance of MMT
L_{kESC}	Kinetic inductance of MMT
L_{mESC_L}	Magnetic inductance of Large MWCNT
L_{kESC_L}	Kinetic inductance of Large MWCNT
L_{mESC_S}	Magnetic inductance of Small MWCNT
L_{kESC_S}	Kinetic inductance of Small MWCNT
$MWCNT_L$	Large MWCNT
$MWCNT_S$	Small MWCNT
N_{MMT}	Number of MWCNTs in MMT
N_{MWCNT_L}	Number of Large MWCNTs in MMT
N_{MWCNT_S}	Number of Small MWCNTs in MMT
N_{X_L}	Number of large MWCNTs along x-axis in MMT
N_{X_S}	Number of Small MWCNTs along x-axis in MMT
N_{Y_L}	Number of large MWCNTs along y-axis in MMT
N_{Y_S}	Number of Small MWCNTs along y-axis in MMT
N_{sh_L}	Number of shell of Large MWCNT
N_{sh_S}	Number of shell of Small MWCNT
N_{ch/sh_L}	Number of Channel per any gth shell of large MWCNT
N_{ch/sh_S}	Number of Channel per any gth shell of Small MWCNT
N_{ch}^{MMT}	Total Conducting Channels of MMT
$N_{ch}^{MWCNT_L}$	Number of channels of Large MWCNT
$N_{ch}^{MWCNT_S}$	Number of channels of Small MWCNT
R_{sh}	Total reistance of individual shell of MWCNT
R_s	Scattering Reistance of individual shell of MWCNT
R_c	Contact resistance
R_q	Quantum Reistance of individual shell of MWCNT
R_t	Internal resistance of Driver
R	Interconnect resistance
R_{ESC}	Total Resistance of MMT
R_{sESC}	Total Scattering Reistance of MMT
R_{qESC}	Total Quantum Reistance of MMT

R_{sESC_L}	Scattering Reistance of Large MWCNTs
R_{sESC_S}	Scattering Reistance of Small MWCNTs
R_{qESC_L}	Quantum Reistance of Large MWCNTs
R_{qESC_S}	Quantum Reistance of Small MWCNTs
S_f	Scale factor
S	Separation between adjacent interconnect
v_f	Fermi energy
V_{in}	Input Voltage
V_o	Output Voltage
W	Interconnect width
ε	Dielectric Constant
σ	Normalized tunneling Conductnace
δ	Spacing between Shells of MWCNT and adjacent MWCNTs
ρ_0	Resistivity
μ_0	Permeability
λ	Mean Free Path
λ_L	Mean Free Path of Large MWCNT
λ_S	Mean Free Path of Small MWCNT

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Chapter 1

Introduction

1.1 Preamble

The heavy traffic causes road jams and interrupts the regular flow of vehicles in metro cities because the number of vehicles is increasing day-by-day. These problems can be overcome by various technique such as increase the width of roads and/or develop multi-level roads. The multi-level roads are overpass, over-bridges, flyovers and crossroads. To increase the width of roads may impossible due to shortage of land besides the roads between cities. However, the multi-level roads are only possible solution to distribute heavy traffic towards various roads. The multi-level roads can help to maintain regular flow of heavy traffic. The multi-level roads can accumulate large number of vehicles without jams and decrease travel timing. Similarly, the chip designers develop integrated circuits (ICs) with multiple layers of interconnects to provide the connecting paths between active and passive elements. This design technique of ICs not only reduces cost and its size but also increases the chip density because feature size of the device decreases continuously with scaled-down technology nodes. [1–3]

In first half of 20^{th} century, electronic devices were developed with the vacuum tubes. These vacuum tubes have been obsolete because of their large size, high cost, power-hungry and unreliable. Thereafter, transistors were invented to replace the vacuum tubes and transistors transformed the electronics industry in the field of ICs design. Further, various IC-design techniques are used to develop high-performance ICs at various technology nodes. The feature size of device reduces with scaled-down technology nodes, where size of interconnects are also decreasing. Further, the parasitic of interconnect increases because dimensions of interconnect such as length, width and height are reduced with scaled-down technology nodes. These parasitic influence the performance of interconnect and ICs at scaled-down technology nodes. The parasitic of interconnect depends on the properties of conductive material at advance technol-

ogy nodes. Thus, the properties of material plays a significant role in implantation of interconnect. The various materials are considered to design interconnect at various scaled-down technology nodes. [4–6]

1.2 Integrated Circuit

An integrated circuit (IC) consists number of passive and active components, which are fabricated on a silicon wafer. The first developed IC held two transistors along with few passive components. Further, the number of active and passive devices are increasing in an IC with change in technologies. These technologies are small scale integration (SSI), medium scale integration (MSI), large scale integration (LSI), very large scale integration (VLSI), ultra large scale integration (ULSI) and Giant scale integration (GSI). [7–10]

- **Small scale integration (SSI)** – In case of SSI technology, the transistors were build upto one hundred by integrating on a silicon wafer. It has few active and passive components to develop few logic gates on a single chip.

- **Medium scale integration (MSI)** - By improving the technology, the number of transistors for MSI has increased from hundred to thousand to fabricate logic gates upto 100 on a silicon wafer.

- **Large scale integration (LSI)** – Under this technique, the number of transistors has increased upto tens thousands on a chip to manufacture thousands of logic gates.

- **Very large scale integration (VLSI)** – For advancement of technology nodes, the number of transistors is fabricated between tens of thousands to hundreds of thousands onto a single silicon chip to develop complex circuitry with combining billions of logics gates.

- **Ultra large scale integration (ULSI)** - The technology nodes are further to be improved under ULSI, the number of fabricated transistors is embedded in the range of one million to tens of million on a single silicon chip.

- **Giant scale integration (GSI)** - Improvement in technology, the number of transistors are invented more than tens of million on single wafer. [11–14]

1.3 Very large scale integration (VLSI)

VLSI is a technique to fabricate ten thousand to hundred thousand of transistors in a single-chip. In early 1970's, the fabrication of complex ICs had been started under the VLSI technique. These ICs are small in size, high operational speed and high functionality. These are broadly used in various applications of electronics like image and video signal processing, cloud computing, consumer electronics and telecommunication. [15–19]

1.4 Interconnect

The performance of ICs depends on length of interconnect and type of material used to develop interconnects. Interconnect is a thin layer of conducting material, which is used to connect two or more nodes of a device/circuit. It is a set of wires that provides the electrical connection within an IC. Interconnect is use to provide the power supply, ground, clock pulses and input signals. These signals are required for the proper functioning of different blocks of an IC. The schematic diagram of interconnect structure is shown in Figure 1.1. [4, 16, 20, 21]

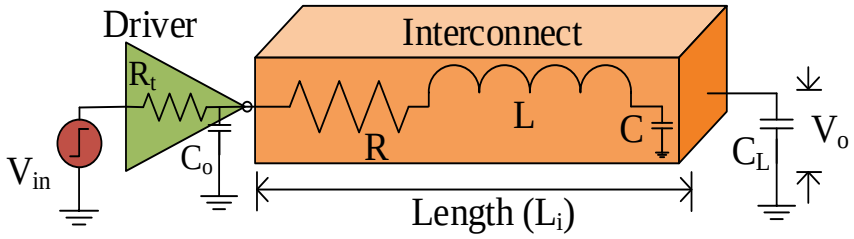


Figure 1.1: Schematic diagram of VLSI interconnects. [16]

An interconnect provides path between input voltage (V_{in}) followed by driver to the output voltage (V_o) across the capacitive load (C_L). The driver has internal resistance (R_t) and output capacitance (C_o), where, L_i is length of interconnect having resistance (R), inductance (L) and capacitance (C). The parasitic is the dominating factor to influence the overall performance of interconnect in terms of propagation delay and power [12, 22, 23]. The parasitic needs to be determined to get actual performance of interconnect.

1.4.1 Types of interconnect

Based on the interconnect length, VLSI interconnects are classified into three categories such as local level (short), intermediate level (semi-global), and global level (long) interconnect as

shown in Figure 1.2 [11, 16].

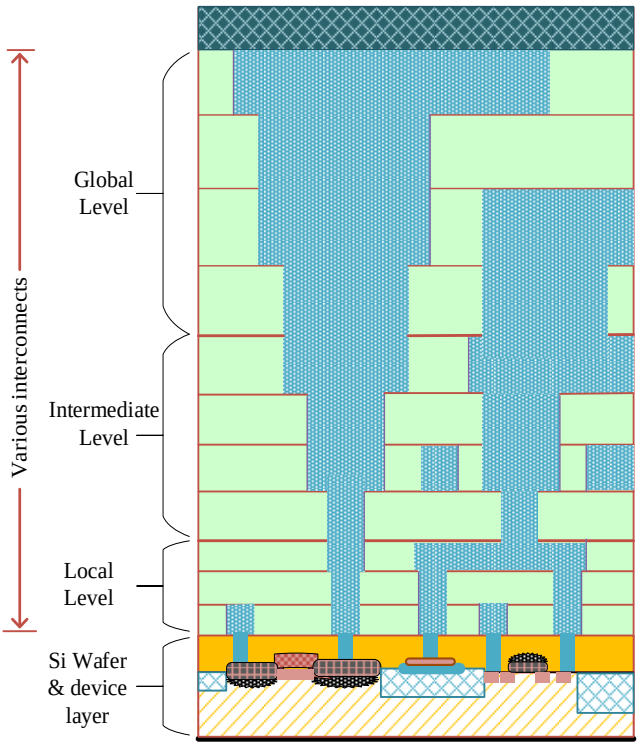


Figure 1.2: Various levels of interconnects in VLSI-IC. [17]

- **Local interconnects**

Local level interconnect consists of very thin connecting lines, which are valid for the length less than 20µm as shown in Figure 1.2. They are used to connect the nearby terminals such as gate, source and drain of transistors within a chip. Local interconnects can be high resistivity due to their short length and they must be capable to sustain at high temperatures [16, 23].

- **Intermediate interconnects**

Intermediate interconnects are longer and wider as compared to local level interconnects, however these are smaller than global level interconnects as shown in Figure 1.2. Intermediate interconnects have length between 20µm and 400µm. Intermediate interconnect is also known as semi-global interconnect because these can be used for short and long interconnect lengths. It can be used to provide path for clock pulse and signal distribution between functional blocks of the device. [16, 24]

- **Global interconnects**

Global interconnect provides the path for clock pulse, signal distribution, input power supply and ground between the various functional blocks of ICs. Global interconnects are valid for the length longer than 400µm [16]. The low resistance material should be used for global

interconnects because they require long length to provide connections between the various parts of an IC. The global level interconnects dominants performance in terms of delay, power and power delay product (PDP) for VLSI-ICs [16,25]. These performance parameters are main factors to understand overall performance of VLSI-ICs.

1.4.2 Design technology for VLSI interconnects

The different design technologies are used for heterogeneous ICs design. In 3-D chip design technique, the problems related to VLSI interconnects can be reduced by utilizing vertical dimensions. By using the heterogeneous design technique, the planar chip is divided into different functional blocks. Each block occupies a different physical level of interconnects and these blocks are connected using short vertical line (also known as via) [26–28]. Due to that, the minimum wire-limited chip area can be achieved and therefore the performance of ICs is improved significantly.

The electronic industry demands multi-functional ICs at cheaper with high operational speed and less power consumption. The operational speed of an IC gets faster by minimizing the delay of device and interconnects. The gate delay of device is reduced with scale-down dimensions of the device. However, the delay of interconnects increases due to rise in parasitic for reduced cross-sectional dimensions and increased length of interconnect. The parasitic is the dominant factor to determine the performance of ICs. The cross-sectional areas and length of interconnects such as local, intermediate and global level are different as shown in Figure 1.2. The dimensions are scaled-down by reducing the feature size of ICs, which influenced the parasitic and overall performance of VLSI-ICs [29–31].

1.5 Importance of Scaling

The feature sizes of the devices and dimensions of connecting wires are continuously reducing with scaled-down technology nodes. The dimensions of interconnect are scaled-down by scaling factor (S_f) at advance technology nodes as shown in Figure 1.3 [32]. Figure 1.3(a), shows that normal dimensions of interconnect such as length (L_i), width (W) and height (H) (means no scaling of interconnect dimensions). The scaling factor is reducing such as S_1 and S_2, which reduces the dimensions of interconnect (L_i, W and H). The dimensions of interconnect

are scaled with scaling factor S_1 and S_2 as shown in Figure 1.3(b) and (c), respectively [24,31].

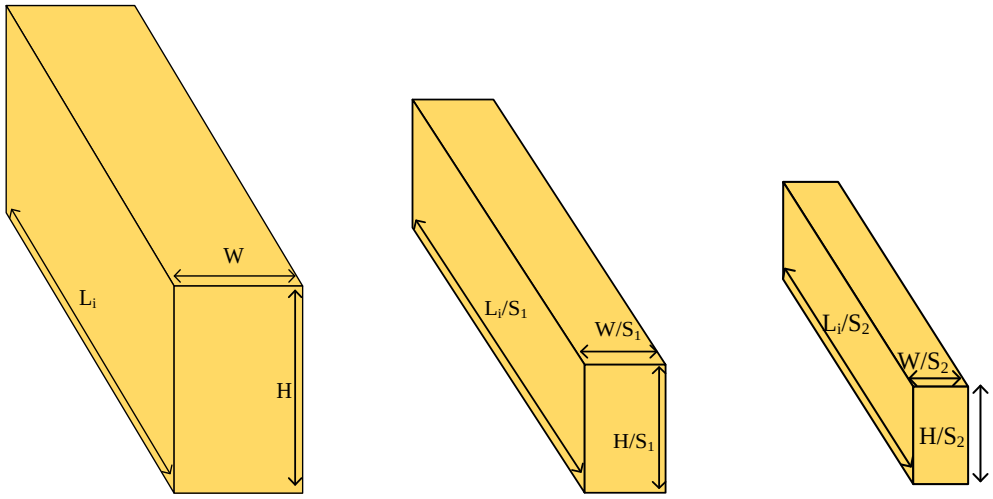
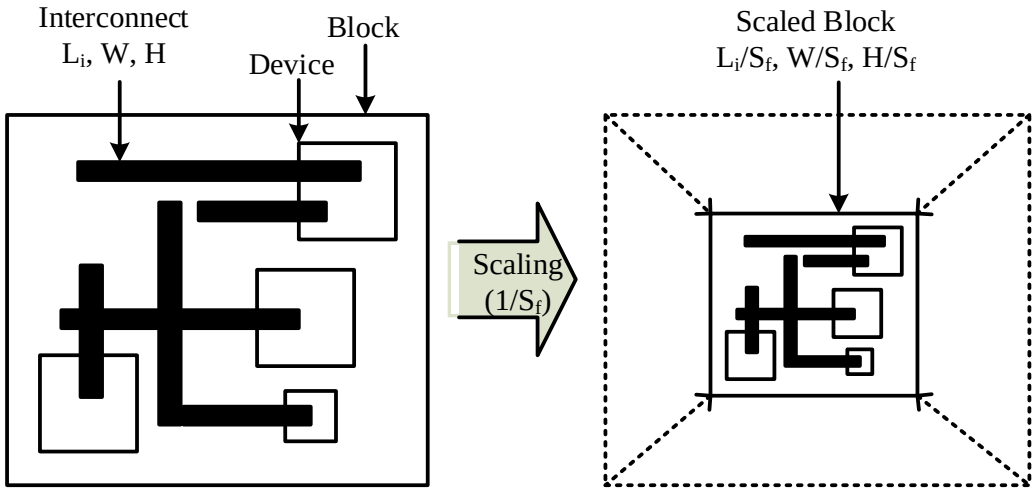
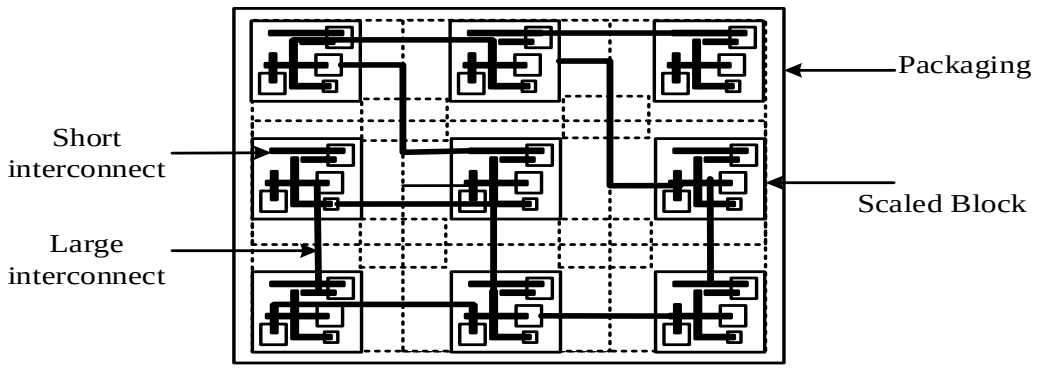


Figure 1.3: Schematic view of interconnect at (a) normal dimensions of interconnect (b) scaled dimensions by scaling factors (S_1) and (c) scaled dimensions by scaling factor (S_2).

The high-performance VLSI-IC design needs a large packing density of transistors/CMOS devices to perform multiple functions. Thus, the requirement of VLSI-IC can be fulfilled by achieving the minimum size of transistors/CMOS devices. The dimensions of CMOS such as length and width of channel are reduced at Deep Sub-Micron (DSM) technology nodes, which reduce the delay of CMOS device [33]. As shown in Figure 1.4(a), the cross-sectional dimensions and length of interconnect are reduced by scaling factor ($1/S_f$) and therefore the packaging density of CMOS increases in an IC as shown in Figure 1.4(b). [32–35]



(a)



(b)

Figure 1.4: (a) The cross-sectional area and length of interconnects reduced by scaling factor (b) scaled-dimensions of interconnect and devices with high pack density within an IC. [23]

The size of interconnects can be reduced at DSM technology nodes for future VLSI-ICs design. The impact of interconnect scaling on the performance needs to evaluate and analyse at various DSM technology nodes. The performance of interconnect depends on its parasitic, which can be calculated based on their length and properties of material. Local level interconnect has less parasitic as compared to semi- and global interconnects because local interconnect has shorter length than semi- and global level interconnects. Further, scaling has negligible impact on the performance of local level interconnect because it has shorter length. However, the impact of scaling has more on the performance of semi-global and global level interconnect because these have large length. [36–39] The scaling reduces the dimensions of interconnect by scaling factor (S_f). The dimensions (L_i, W and H) play a significant role, which increases the propagation delay of interconnect at DSM technology nodes.

1.6 Importance of repeaters insertion

The classification of VLSI interconnects on the basis of their lengths is presented in Section 1.4. The shorter length of wires is used as local level interconnects. These are used to connect the nearby terminals and via of CMOS transistors. The impact of parasitic on performance of the local level interconnect is smaller because parasitic of local interconnects are less than CMOS device. Further, the resistance increases linearly with increasing the interconnect length and is abruptly increases by decreasing dimensions of interconnect at DSM technology nodes [38]. The parasitic of long wire interconnects are larger than CMOS transistors. The parasitic of long interconnect dominates the performance of the devices. The parasitic of interconnect is necessary to calculate for observing the actual performance of device. [21, 40–42]

Thus, the performance of long interconnect can be observed in terms of propagation delay (as RC time constant). The large amount of propagation delay for long interconnect decreases the operational speed of VLSI-IC. The overall delay of long wire interconnects can reduce by inserting the number of repeaters. The reduction of propagation delay can be achieved by splitting long wire into short lines of equal segments (distributed line) and each segment drives by CMOS driver as shown in Figure 1.5. [43–45]

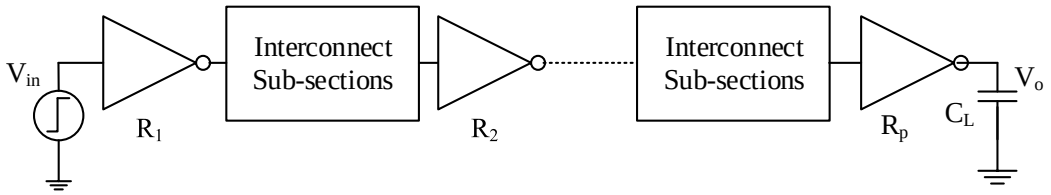


Figure 1.5: The distributed interconnect line with optimum-sized repeater and optimum number of repeaters. [9]

By inserting repeaters, the overall propagation delay decreases and therefore speed of the operation gets faster. The desired performance of the VLSI interconnect can achieve by inserting optimum-sized and optimum number of repeaters.

1.7 Interconnect Models

The electrical equivalent model of a long wire interconnect is known as a lumped model, where, long wire is acting as electrical transmission line. This model is used to examine impedance parameters of interconnect. Further, these parameters are used to determine the performance of interconnect. The developed models may be simple or complex, according to interconnect arrangements. The various aspects can be included to develop an accurate model for interconnect. The RC lumped impedance models for interconnect are classified based on their resistance, capacitance, and inductance arrangements. The RC lumped models such as L-Model, T-Model, and Π-Model are shown in Figure 1.6(a)-(c), respectively. [46–49]

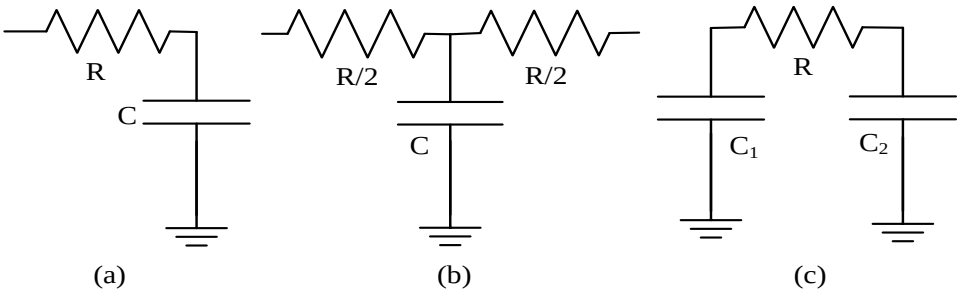


Figure 1.6: Different lumped RC models for interconnect (a) L-model (b) T-model and (c) Π-model. [28,49]

RLC lumped models are more accurate than the RC lumped model because their better performance. The RLC lumped models are shown in Figure 1.7 (a) T-model and (b) Π -Model. [48–50]

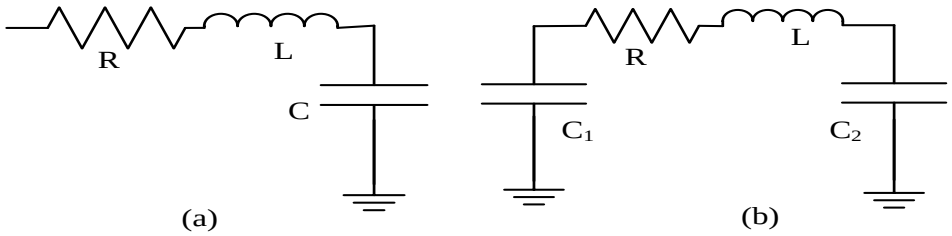


Figure 1.7: RLC lumped models for VLSI interconnect (a) L-model and (b) Π -model. [28,35]

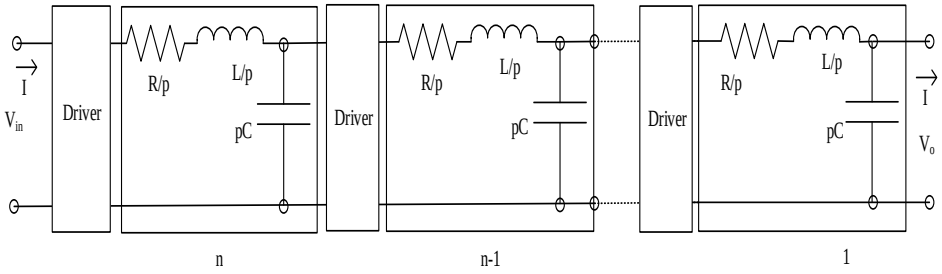


Figure 1.8: Distributed RLC model of a VLSI interconnect having n-segments. [50]

Additionally, the highly accurate performance of interconnect models can be obtained by converting lumped models into distributed models. The distributed models can be obtained by dividing lumped models into number of stages (p) as shown in Figure 1.8. The repeaters are inserted to drive the n-stage of equivalent distributed model for VLSI interconnect. These repeaters increase the driving capacity and reduce overall propagation delay of interconnects [51, 52]. The optimum-sized repeater and optimum number of repeaters are calculated for various technology nodes to simulate the distributed model.

1.8 Aluminium and Copper as interconnects

Firstly, Aluminum (Al) is chosen as interconnect material because it has various advantages as good ohmic contact with silicon, good conductivity and adherence to silicon dioxide [53, 54]. The dimensions of the interconnect decrease with scale down technology nodes to the micron level and therefore increases the current density of interconnects. The electro-migration takes place at high current densities due to that metal conductor can change their shape and leads to break connecting wires [55,56]. The impact of electro-migration increases as the dimensions of interconnect decreases at scaled-down technology nodes. Thus, it was challenging to achieve high current density for micro-scaled technology nodes since it has high resistivity. These

problems can overcome using Copper (Cu) material to replace Al as interconnects at micro-scaled technology nodes [57–60].

Cu shows some advantages over Al such as low resistivity, high current density, and high melting point as shown in Table 1.1. The impact of electro-migration is improved for Cu at high current densities than Al material as VLSI interconnect [61–63]. Thus, Cu become preferable material as VLSI interconnect, especially at micron and submicron technology nodes for high-performance VLSI-ICs [64–66]. The various properties of conducting materials such as Cu, Al, gold and silver are described in Table 1.1.

Table 1.1: Various properties of different conducting materials. [60]

Materials	Properties			
	Resistivity ($\mu\Omega - cm$)	Melting Point (K)	Corrosion in Air	Adhesion to SiO2
Copper (Cu)	1.7	1357	Poor	Poor
Aluminum (Al)	2.7	933	Good	Good
Gold (Au)	235	1264	Excellent	Poor
Silver (Ag)	1.6	1062	Poor	Poor

However, the impedance parameters of Cu interconnect increases at DSM technology nodes (especially below 45nm), which degrades their performance such as delay, power and PDP. The cross-sectional area of VLSI interconnects reduces by scaled-down technology nodes, where it requires high current density and larger electron Mean Free Path (MFP). Cu material has limited current density and a shorter electron MFP. The combined effects of above mention problems are boosting grain boundary, surface scattering and electro-migration. These factors enhance the scattering resistance that influenced the performance such as delay and power of interconnect. ICs have higher delay and large power consumption due to which the speed of operation of the device decreases. [67–71]

Moreover, the rising resistance of Cu interconnects affects the performance of ICs in terms of delay and power at DSM technology nodes. Therefore, it is necessary to investigate new interconnect material at DSM technology nodes to overcome the above mention problems. Thereafter, the carbon-based nanomaterials have been invented to replace Cu as interconnect material for VLSI-ICs design, which can be outperformed at DSM technology nodes. [72–76]

1.9 Carbon Nanotube as VLSI interconnects

In recent research, carbon-based nanostructures like carbon nanotube (CNT) and graphene nanoribbon (GNR) are recommended as global interconnect at DSM technology nodes. CNT is more considerable material than Cu for global interconnect at DSM technology nodes. Numerous research articles are published based on CNT as interconnects for VLSI-IC design at DSM technology nodes. CNT is allotropes of carbon, which can take shape of tubular by rolling up sheet of graphene as single-walled and multi-walled CNT [77].

Table 1.2: Various properties of Cu, graphene, SWCNT and MWCNT. [71]

Properties	Materials			
	Cu	Graphene	SWCNT	MWCNT
Maximum Current density (A/cm^2)	10^6	10^9	10^{10}	10^{10}
Thermal conductivity (*10^3.W/mK)	0.385	3-5	1.75-5.8	3
Mean Free Path (nm)	10	1×10^3	$>10^3$	2.5×10^4
Melting Point (K)	1357	3800 as graphite		
TCR ($10^{-3}/K$)	4	-1.47	<1.1	-1.37
Mechanical Strength	good	Fair	Fair	Fair
Process of Fabrication	easier	Difficult	Difficult	Difficult

It shows that the CNT is superior in field of nanotechnology, electronics, material science, etc. because of mechanical strength, thermal stability and good electrical properties. It can be used as different interconnect levels for various applications. CNT has higher current density, good thermal stability and large electron MFP. Table 1.2 presents the properties of different materials such as Cu, graphene, SWCNT and MWCNT. [78–83]

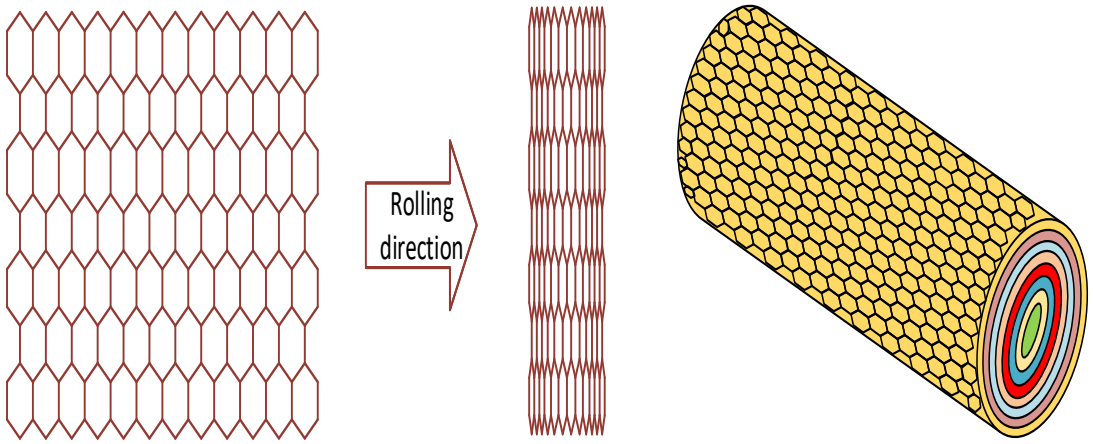
1.9.1 Classification of Carbon nanotube

The CNTs can classify based on their structures, chirality and conductivity.

A. Classification based on their structures

Based on structures, CNTs can classify as single-walled carbon nanotube (SWCNT) and multi-walled carbon nanotube (MWCNT).

SWCNT - SWCNT implemented by rolling a sheet of graphene into tube and has diameter upto few nanometers as shown in Figure 1.9(a) [84]. The SWCNT has only single shell and fixed number of conducting channels. SWCNT bundles (SWCNTB) are fabricated by inserting several SWCNTs of similar diameter, where the number of conducting channels is same for each SWCNT. Number of conducting channels of SWCNTB are also fixed because they have same diameter for each SWCNT in a given bundle. The resistance and inductance of SWCNTB can be calculated by considering all individual SWCNTs to be parallel [85–88]. Thus, the resistance and inductance can be calculated by dividing individual resistance and inductance of SWCNT with number of SWCNTs of a bundle [81]. The capacitance can be calculated by multiplying the individual capacitance of SWCNT to number of SWCNTs of a given bundle. The impedance model of SWCNTB is very simple; however, the fabrication of the fixed diameter SWCNT is complicated due to no control on its growth process [79].



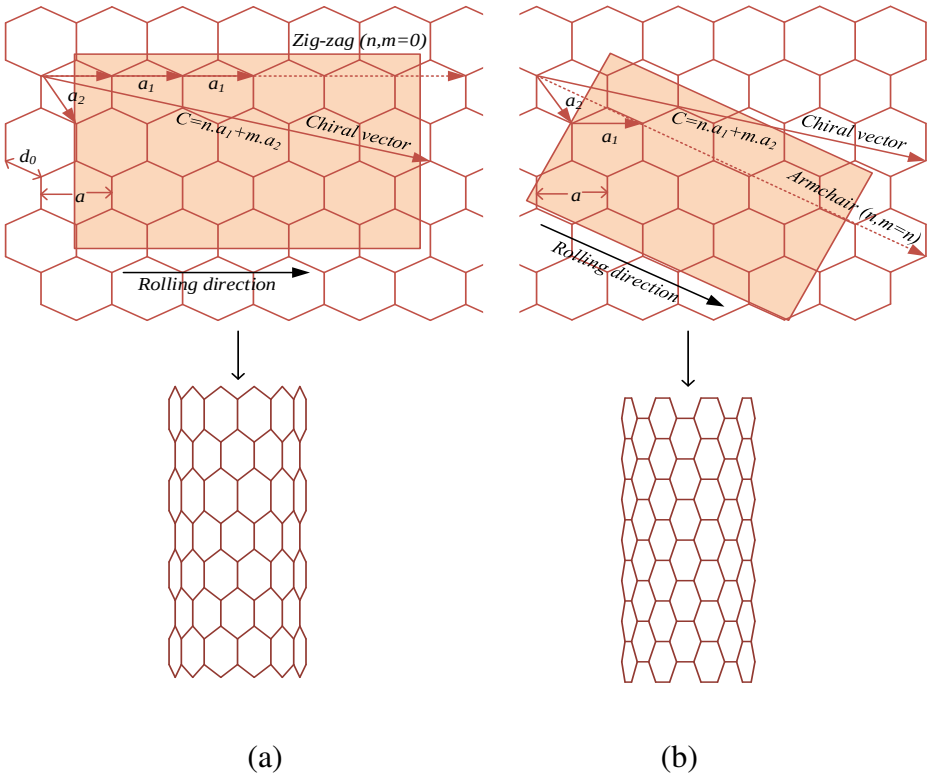
(a) (b)

Figure 1.9: (a) A graphene sheet rolled into the SWCNT, and (b) Structure of MWCNT. [61,69]

MWCNT - MWCNT develops by rolling two or more graphene sheets concentrically in the form of cylinder as shown in Figure 1.9(b). The diameter of MWCNT lies between few nm and several tens of nm. It has various number of shells and each shell of MWCNT has different diameter as well as various numbers of conducting channels [80, 89, 90]. The MWCNT bundle (MWCNTB) has implemented by combining two or more similar MWCNT. The parasitic of individual shell of MWCNT is different because it has various numbers of conducting channels. Therefore, the calculation of impedance parameters of MWCNT is complex and but fabrication is more comfortable as compared to SWCNTB due to better control on the growth process. [86, 91–93]

B. Classification based on chirality and conductivity

The CNTs are classified based on its chiral indices (n, m) - armchair and zigzag. The zigzag structure is developed by rolling a sheet of graphene, if one of chiral indices is equal to zero (n or m = 0) as shown in Figure 1.10(a). However, the armchair structure can be developed by rolling-up a graphene sheet, if chiral indices are equal (n = m) as shown in Fig1.10(b). Further, the direction of rolling up the graphene sheet into CNT (if $n - m = 3i$, where *i* denotes integer) decides its conductivity. Due to that, the implemented CNT can be metallic or semiconducting in nature. The zigzag structures are metallic or semiconducting due to their chiral indices, while the armchair structures are always metallic. Thus, the metallic CNTs can be recommended as long wire interconnects for high-performance VLSI-ICs because of their good electrical and thermal properties. [64, 94, 95]



(a) (b)

Figure 1.10: (a) Zigzag (semiconducting) (b) Armchair (metallic) configuration of CNT. [82]

MWCNT has a greater number of conducting channels and longer MFP because it has large diameter as compared to SWCNT structures. The SWCNTB and MWCNTB have the same current density, however the modeling of SWCNT is easier than the MWCNT bundle [96–98]. The fabrication of MWCNT bundles is quite easier than SWCNT bundle due to better control on its growth processes. Additionally, MWCNT can be recommended as a global interconnect for VLSI-IC design at DSM technology nodes [97–100].

1.9.2 Types of CNT nanostructure as VLSI interconnect

The various CNT nanostructures such as the SWCNTB, MWCNTB, and Mixed-CNT bundle can be recommended as high-performance interconnect for VLSI-ICs design at DSM technology nodes. SWCNTB can be developed by inserting the number of SWCNTs, where each SWCNT has fixed number of conducting channels and same diameter of each SWCNT. The modeling of SWCNTB is easier, however, the fabrication of SWCNTB is difficult to develop similar diameter of each SWCNT because of no control on their growth process [101–105]. Thus, MWCNTB can be implemented with the help of MWCNTs having similar diameters, same number of shells and fixed number of conducting channels of individual MWCNT. The modeling of MWCNTB is complex because it consists various number of shells and each shell has different conducting channels [105–110]. The MWCNTB has left large vacant space, which can be filled with SWCNTs of same diameters as known as the Mixed-CNT bundle. It has both types of CNTs such as SWCNT and MWCNT in a single bundle [111, 112]. Further, the Mixed-MWCNT bundle (MMT) is developed by inserting two or more differently-sized MWCNTs in a bundle. The MMT nanostructure are denser than other CNT bundles because of smaller-sized MWCNTs are inserted into MWCNTB to occupy the vacant space [113, 114].

The CNT nanostructure as VLSI interconnects may have large variations in its performance under thermally aware environmental conditions for various applications such as the automobile industry and space shuttle. It is also important to understand actual performance of high-performance VLSI-ICs design for sensor development and IoT applications at various environmental conditions [115, 116]. The applications such as image processing, which requires high accuracy to real-time detection and cloud computing at variable temperature conditions [117, 118]. The CNT interconnect can be used in low power applications for image processing and applications in high performance biomedical control system [119, 120]. These variations have a significant impact on scattering phenomena such as grain boundary and surface scattering of CNT nanostructure [121–124]. The scattering phenomena has considerable impact on electron MFP, which influences performance of the CNT as global level interconnects [125–128]. The various temperature-dependent impedance (RLC) models are reported for SWCNTB and MWCNTB in the available literature [129–134]. Hence, the impact of temperature on performance of other CNT bundle as VLSI interconnect needs to be determined.

1.10 Motivation

The feature size of devices is reduced day-by-day with scale-down technology nodes. The reduced size of interconnect degrades their performance in terms of delay, power and PDP. The performance of interconnect depends on their parasitic, which are increasing with decrease of cross-sectional area and length of interconnect. The various conducting materials are used to design interconnects for VLSI-ICs. Earlier, the aluminium and copper are considered to implant of interconnects, however, these materials have few limitations at advanced technology nodes.

The researchers introduced carbon based nanostructures (such as GNR and CNT) as new interconnect materials for VLSI-ICs design at DSM technology nodes. As per the literature, these nanostructures are suitable candidate to replace old materials as VLSI interconnects at DSM technology nodes. SWCNTB and MWCNTB nanostructures for VLSI interconnects are performing better than copper interconnects. These nanostructure offers less resistance, which enhances the performance of VLSI interconnects. The fabrication of SWCNTB with similar SWCNTs of fixed-diameter are complex due to chirality and no control on their growth process as compared to MWCNTB nanostructures. However, the MWCNTB has much vacant space around corners, side-walls and adjacent MWCNTs, which decreases their conductivity and degrades the performance.

Further, the closely packed MMT nanostructures are formed by inserting two or more differently-sized MWCNTs, which offers less resistance and high conductivity as VLSI interconnects at DSM technology nodes. The performance for different type of MMT nanostructures in terms of delay, power and PDP have been calculated, which are compared at global interconnect lengths. Still, the impact of temperature on performance of MMT nanostructure has not been concluded. The effect of separation between adjacent shells and MWCNTs, which play a critical role to estimate the conducting channels, parasitic, delay, power and PDP. Literature shows that a little work has been reported and needs to be focus more on the thermally-aware working environment, which can be influenced the performance of MMT as VLSI interconnects. Therefore, the temperature impact can be observed by varying the number of shells and the separation gaps between the walls at various technology nodes.

1.11 Thesis contributions

This thesis presents a temperature-dependent performance analysis of MMT nanostructure as global level interconnect as a function of temperature at DSM technology nodes for VLSI-IC design. The contribution of thesis is given below

- The aim of first objective is to develop the temperature dependent impedance equivalent models for Mixed-MWCNT bundle as VLSI interconnect.

In this objective, temperature-dependent ESC model for proposed Mixed-MWCNT (MMT) nanostructure is developed. The proposed MMT nanostructure as global level VLSI interconnect is implemented by two differently-sized MWCNTs such as $MWCNT_L$ and $MWCNT_S$. The developed MMT nanostructure is denser than MWCNT bundle because it has inserted few $MWCNT_S$ in the MWCNT bundle to fill vacant space at side-walls, corners and adjacent space between four $MWCNT_L$. The number of conducting channels increases because insertion of conductive $MWCNT_S$ in the MWCNT bundle. Thus, the proposed MMT nanostructure offers low resistance and high conductance because of large number of conducting channels. All conducting channels of MMT nanostructure as global interconnect are assumed to be parallel. Further, the mathematical expressions are derived with the help of MATLAB tool to obtain temperature-dependent parasitic in terms of resistance, inductance and capacitance for proposed MMT as global interconnect at various DSM technology nodes.

- The aim of second objective is to analyze the impact of temperature on the impedance parameters of Mixed-MWCNT bundle at deep submicron technology nodes for global interconnect length.

In this objective, temperature-dependent impedance parameters are evaluated for the proposed ESC model of MMT as global level interconnect length for a variable temperature range (200-450K). Temperature-dependent resistance of MMT nanostructure is analyzed at various DSM technology nodes. The resistance of MMT as global interconnect is increased with rising temperature at all three technology nodes. The resistance has been increased due to decrease in mean free path (MFP) of CNT. The number of conducting channels is influenced by MFP, where MFP depends on scattering phenomena. The temperature-dependent MFP is decreased with increasing temperature (200 to 450K) at DSM technology nodes. The calcu-

lated temperature-dependent resistance is compared with temperature-independent resistance of MMT as global interconnect at DSM technology nodes. Further, temperature-dependent parasitic of ESC model is simulated to examine the performance at DSM technology nodes.

- The aim of third objective is to evaluate the temperature dependent performance of Mixed-MWCNT in terms of delay, power dissipation and PDP at different technology nodes.

Temperature-dependent ESC model of MMT nanostructure is developed under the objective 1 and temperature-dependent parasitic are calculated under objective 2. Further, the temperature-dependent ESC model is simulated with the help of SPICE tool to examine the performance in terms of delay, power and PDP under this objective. The performance of MMT nanostructure are calculated in terms of delay, power and PDP for a variable temperature ranging from 200 to 450K at DSM technology nodes (32, 22 and 16nm). The temperature-dependent performance of MMT as global interconnect are analyzed and compared for a variable temperature range at DSM technology nodes.

- The aim of fourth objective is to compare the results obtained from the above analysis with similar analysis for MWCNT, SWCNT and copper interconnects.

The temperature-dependent performance of proposed MMT nanostructure is calculated under objective 3, which is compared with similar analysis of Cu, SWCNTB and MWCNTB interconnect. The comparative performance analysis of MMT with MWCNTB, SWCNTB and Cu interconnect is presented on a variable temperature range between 200 and 450K at 32, 22 and 16nm technology nodes. The results revealed that the MMT outperform all the nanostructures under consideration for global interconnect length as a function of temperature at various DSM technology nodes.

1.12 Thesis organization

Chapter 1 provides the basic information about subsequent chapters to familiarize themselves with these chapters. It provides a brief outline of VLSI interconnect and discusses the disadvantages of Cu as interconnects material at DSM technology nodes. To overcome limitations, the Cu material needs to be replaced with new material for VSLI interconnect. The CNTs are capable of replacing Cu material at DSM technology nodes. The different nanostructures such

as SWCNTB and MWCNTB are used as VLSI interconnect, which has been discussed in this chapter. The feature size of devices and dimensions of interconnects are reducing at advance technology nodes. The parasitic of VLSI interconnects are increased for advance technology nodes. The impedance parameters of interconnect influence with thermally-aware environmental conditions at DSM technology nodes. Further, the impact of thermal variations on the performance of Cu, SWCNTB and MWCNTB interconnect discussed at DSM technology nodes. The performance of interconnect plays a importance role to understand actual performance of device of ICs at DSM technology nodes and thermally-aware environmental conditions.

Chapter 2 presents a detailed study of literature to provide relevant information about the issues to be reflected in this thesis and to highlight the importance of the current work done. It provides the information about various VLSI interconnect materials such as Cu and CNT nanostructure. The detailed study shows that few limitations of Cu interconnect at DSM technology nodes, which can be minimized by using CNT material as VLSI interconnect. It is a promising candidate for intermediate and global level interconnect according to the literature survey. It shows that the SWCNT and MWCNT bundles outperform Cu material as global level interconnect at DSM technology nodes. The impact of temperature on Cu interconnect is highlighted at DSM technology nodes. Temperature-dependent models of SWCNT and MWCNT nanostructures are discussed as global level VLSI interconnect. Further, the Mixed-MWCNTB nanostructure is implemented and work has been presented by very few researchers. The work published related to Mixed-MWCNTB nanostructure is not enough and needs to be more focused on thermally-aware performance at DSM technology nodes, which may be a future of global interconnect.

Finally, some research gaps carried out from the detailed analysis of the literature. The objectives are decided from these research gaps, and the methodology for presented work has also discussed.

Chapter 3 presents the proposed nanostructure of the MMT as global level interconnect for VLSI-ICs design. It is a combination of two differently-sized MWCNTs such as large and small diameter of MWCNTs. The equivalent single conductor (ESC) models of MMT nanostructure developed with the help of mathematical equations for global interconnect at DSM technology nodes. The impedance parameters like inductance, capacitance and resistance are computed by deriving mathematical equations. Further, this model is considered to observe

performance in term of delay, power and PDP by simulating in the SPICE tool at 32, 22 and 16nm technology nodes. Similarly, ESC model of Cu is also presented to evaluate the performance at DSM technology nodes and obtained results from simulation are compared with performance of MMT nanostructure. The comparative analysis is presented and conclusion is drawn in the summary of the chapter.

Chapter 4 explores impact of temperature on performance of MMT nanostructure for global level interconnect at DSM technology nodes. Thermally-aware ESC model of proposed MMT nanostructure is developed to evaluate parasitic at DSM technology nodes. The obtained scattering resistance of MMT nanostructure influenced due to shrinkage of effective MFP with increase in temperature ranging from 200 to 450K. The effective MFP is decreased because the scattering phenomena occur such as electron-phonon and electron-electron scattering at a variable temperature. The electron-electron scattering has a negligible impact, but electron-phonon plays a significant role in the scattering phenomena. The calculated parasitic is considered to examine performance in terms of resistance, delay, power and PDP for a variable temperature range at DSM technology nodes. Thermally-aware ESC model of MMT nanostructure is considered to evaluate the performance at different DSM technology nodes. Further, thermally-aware ESC model is simulated with the help of SPICE tool to observe the performance in term of delay, power and PDP for a temperature range at 32, 22 and 16nm technology nodes. The comparative analysis of MMT is presented at various technology nodes for a variable temperature range 200-450K. Furthermore, the thermally-aware ESC model of Cu is developed to estimate the performance and obtained results are compared with the performance of MMT nanostructure. The results are shown that the delay of both interconnects is increased with increasing temperature ranging from 200 to 450K at 32, 22 and 16nm technology nodes.

Chapter 5 presents the analytical delay model of MMT nanostructure of a variable temperature range 200-450K at various DSM technology nodes. The driver interconnect load (DIL) is used to evaluate parasitic and the performance of MMT interconnect. The analytical model is developed by deriving mathematical equations with the help of MATLAB software. The optimum-sized and optimum number of repeaters are calculated to insert in MMT nanostructure line for converting into distributed model. The analytical model is considered to calculate the analytical delay of MMT nanostructure at DSM technology nodes. The obtained analytical results are compared to the simulated results of MMT interconnect at DSM technology nodes,

which have calculated in the previous chapter 4. Both the results are aligned and raised with increasing temperature from moderate to high at 32, 22 and 16nm technology nodes. Further, the analytical delay is also examined for Cu interconnect and obtained results are compared with simulated results, which are aligned with simulated results.

Chapter 6 describes comparison of temperature-dependent performance of MWCNTB, SWCNTB and Cu interconnect with MMT interconnect at DSM technology nodes for variable temperatures. The performance of MWCNTB, SWCNTB and Cu interconnects are evaluated with the help of ESC models, which are simulated in SPICE tool. Further, the calculated performance of Cu, SWCNTB and MWCNTB interconnect are compared with the performance of MMT obtained in Chapter 4. The comparative analysis of MMT with Cu, SWCNTB and MWCNTB nanostructure as global level VLSI interconnects are presented at DSM technology nodes for temperature ranging from 200 to 450K. The comparative analysis shows that the overall performance of proposed MMT nanostructure for global level interconnect length is better than MWCNTB, SWCNTB and Cu at various DSM technology nodes such as 32, 22, and 16 nm for various temperatures.

Finally, the conclusion will be drawn based on the thesis with the possible future scope of this work is also presented in Chapter 7.

Chapter 2

Literature Review

This chapter gives a thorough review of relevant literature to present necessary information on the issues related to interconnects. These issues are considered in this thesis and highlight the importance of the current study. This chapter gives information about various nanostructures and different delay models as VLSI interconnects in the literature. Also, discuss the limitations of Copper (Cu) as VLSI interconnect and the necessity of inventing new material as VLSI interconnect to replace Cu at DSM technology nodes. The carbon-based nanostructures such as SWCNTB, MWCNT, MWCNTB and Mixed-MWCNT (MMT) presented for VLSI interconnects at DSM technology nodes. Further, various temperature-dependent models are presented for Cu, SWCNTB, MWCNT and MWCNTB as VLSI interconnects at advanced technology nodes.

2.1 Introduction

The performance of VLSI interconnects influences with scaling from micron-scale to nano-scale technology nodes for VLSI-IC design. The die-size increases, which increases the density of chip and long interconnects require to connect device terminals within the chip. The feature size of the devices is reducing to nano-scale technology nodes, where the dimensions of interconnects also need to be reduced. The various delay models are present in the literature to study accurate performance of VLSI interconnects. The effect of parasitic can be minimized by inserting a number of repeaters with fix-sized repeaters, which has been proposed in the literature. The minimized parasitic helps to reduce the delay of long interconnects for VLSI-IC design. The characteristics of used material for interconnect play a significant role at nano-scaled technology nodes. The performance of Cu material used as VLSI interconnects gets degraded below 45nm technology nodes.

Further, carbon-based nanostructures as VLSI interconnects have been proposed to replace Cu at DSM technology nodes. Numerous relevant research articles have been published to know the performance of carbon-based nanostructures. The various properties of CNTs make them preferable material for intermediate and global interconnects. The performance of various CNT nanostructures (SWCNTB, MWCNT and MWCNTB) has been compared to Cu interconnect for various interconnect lengths at DSM technology nodes. It needs to be examined the actual performance of VLSI interconnects under the variable temperature conditions at DSM technology nodes. In the literature, different thermally-aware impedance models have been presented for Cu, SWCNTB, MWCNT and MWCNTB. These impedance models have been used to calculate the performance for VLSI interconnect in terms of delay, power and PDP. The presented literature is related to the performance of MWCNTB, MWCNT, SWCNTB and Cu as VLSI interconnects. Also, literature shows the impact of a variable temperature range on performance of MWCNTB, MWCNT, SWCNTB and Cu interconnect at different technology nodes.

2.2 Delay models for VLSI Interconnects

The transmission line models are used to determine performance in terms of power and delay of interconnects. These models have been used to analyze the overall performance of systems at DSM technology nodes for VLSI-IC design. The number of delay models presented in the published work, which considered to develop mathematical expressions and used to evaluate the delay and shapes of output waveforms for VLSI interconnects.

H. B. Bakoglu *et al.* [8] presented the delay of VLSI interconnects in terms of delay. The delay has been raised rapidly due to dimensions of the chip have been scaled-down, which has increased the RC time constant of interconnect lines. The performance of MOS circuits has better than bipolar and GaAs-based circuits because the output impedance of MOS transistors has low. It plays a essential role in capacitive load as compared to RC load, whereas load resistance has higher than the output resistance of transistor. The propagation delay of multilayer interconnects has been improved impressively. The dimensions of interconnects can reduce at scaled-down technology nodes that have been increased the delay. The repeaters have been inserted to eliminate the internal resistance and capacitance to stabilize the overall delay and power consumption of ICs. The minimum interconnects delay has been achieved by inserting an optimum number of repeaters and minimum driver size.

Andrew B. Kahng *et al.* [26] introduced a new distributed RC and RLC model for interconnects load of the CMOS gate. The impedance model for interconnect has been proposed based on the parasitic as inductance, capacitance and resistance. The various models have been used to observe the rise time and gate delay, which has examined as 25% of SPICE simulation values. This model has been recommended to reduce the complexity of formula for the total capacitive load in modeling. The proposed line model has been expanded to consider effect of various capacitances such as interconnect and discrete/load capacitance, separately.

Yehea I. Ismail *et al.* [36] presented the finite delay expression based on alpha power law in the distributed RLC line of CMOS gate. It has been computed as 7% of SPICE simulation at DSM technology nodes. The delay error for on-chip interconnect considered as pure RC distributed line has been observed over 30%. The effect of inductance on the propagation delay has been increased for the RC interconnect line, which can be a significant impact on design methods. The problem of inserting repeaters into the RLC line has been influenced the finite delay model. The proposed finite solutions for insertion of repeater have been massively accurate to numerical solutions. The error has been increased between RC and RLC delay models up to 30% because the inductance effect has been neglected in the design process of inserting repeaters. It concluded that the effect of inductance has played a important role in design process for high-performance ICs.

Raguraman Venkatesan *et al.* [49] presented the novel analytical models for VLSI interconnect distributed RLC to calculate propagation delay, insertion of repeaters and crosstalk delay with capacitive load. The error has been observed as compared to HSPICE simulations for propagation delay, insertion of a repeater and crosstalk delay as 2% for the delay, 2% for insertion of a repeater and 10% for crosstalk delay, respectively. The normalized delay has been observed minimum for 8-10 repeaters for proposed model and compared with already presented models in the literature. The reduction in crosstalk delay and cross-sectional area of line with insertion of the intelligent repeater for proposed model has been calculated as 51% and 83%.

Kevin T. Tang *et al.* [50] investigated impact of on-chip inductance on the delay and short circuit power of a CMOS for high-speed ICs design. The significant impact on the output voltage and short circuit power has been determined by analytical expression for fast input ramp signals. It concluded that the short circuit current has been increased due to large load inductance and fast switching time of input signals. It concluded that the accuracy of analytical

expressions has been examined as 10% with compared to the SPICE simulation results.

Magdy A. El-Moursy *et al.* [44] studied the insertion of repeaters to achieve minimum propagation delay for high impedance parameters of interconnect lines. The highly inductive lines have influenced the nature of signal, optimum-size and number of repeaters to drive an interconnect line. The long interconnect lines have been driven by an optimum number of repeaters with fixed-sized repeaters to reduce propagation delay to a minimum level and less power dissipation. The minimum PDP has been achieved by optimizing the width of the interconnect line that may fulfil the requirement of electron velocity, the least power consumption for VLSI-ICs design. It concluded that the insertion of repeaters reduced power and delay by up to 65% and 97%, respectively. The efficient technique of Power-Delay-Area-Product (PDAP) has been presented to size of interconnect line in a repeater insertion system.

Rajeevan Chandel *et al.* [35] determined the performance of on-chip VLSI interconnect based on transmission line in terms of delay and power. The delay has been increased because of decreasing chip area (scaling dimensions) and arising several active devices on-chip. The different techniques had been represented in published articles to insertion of buffer in global interconnect lines. This article has been investigated the delay and power reduction by using repeater insertion for global interconnect length at low power conditions. It has also been considered the impact of voltage-scaling on the insertion of repeaters for long wire lines. It has been shown that the fixed-size and optimum number of repeaters play a vital role in minimizing propagation delay. The power has been reduced due to voltage-scaling and insertion of repeaters for long VLSI interconnect.

Rajeevan Chandel *et al.* [37] presented impact of voltage scaling on repeaters for delay of interconnect that has been minimized with insertion of repeaters. The proposed analytical models have been used to determine the number of optimum repeaters for scaling of supply voltage. The comparative analysis of results has been obtained from analytical model and SPICE simulation model, which have been calculated for resistive and inductive interconnects. It revealed that power dissipation had been reduced by voltage scaling and delay of interconnect has been reduced by insertion of an optimum number of repeaters. The delay has been improved by voltage scaling and repeater-insertion in the interconnect line.

Morteza Gholipour *et al.* [110] examined characteristics of MWCNTs as VLSI interconnect

for VLSI-ICs design. The performance of MWCNTs and Cu nanostructures has been simulated and obtained results have been compared at global, semi-global and local interconnect lengths. The semi-analytical model has been presented to estimate delay and technique of repeater insertion in MWCNT as interconnects have been studied. The results have been compared for both the simulated and proposed analytical models. It revealed that the proposed model has accurate and efficient. This work demonstrated that number of insertion repeaters for MWCNT can be required less than Cu interconnect.

Maria Sabrina Sarto *et al.* [135] presented ESC model for MWCNT as VLSI interconnect. The multi-conductor transmission line concept has been used to develop an ESC model. The closed-form expressions of equivalent kinetic inductance and quantum capacitance have been determined per unit length. The approximate accurate expression has been proposed for quantum capacitance in terms of per unit length. It revealed that the new analytical equations have been suitable for most structures of MWCNT interconnect. The model presented in this article has been considered for both domains (frequency and time).

Sourajeet Roy *et al.* [48] proposed the crosstalk noise and propagation delay models for integrated resistance-inductance-capacitance (RLC) of interconnect. The introduced algorithm has been improved version of Lie formula. This algorithm has been considered for variable coupled RLC lines and various topologies. It could be used to develop an equivalent model for non-identical and identical multi-conductor transmission lines for various loads. It concluded that the delay error and crosstalk noise for results of proposed model and SPICE simulation had been calculated as 50% and 0.75%, respectively.

Saeid Taji *et al.* [47] examined performance of CNT interconnect in terms of power and delay. The proposed model has been established based on parasitic such as capacitance and resistance of CNT interconnects. The propagation power and delay for the integrated circuit have been determined through an expression of dynamic power and delay. The performance of CNT and Cu NoC has been analyzed and compared with each other. It concluded that the PDP had been obtained less between 10 to 20% for CNT as compared to Cu NoC.

Wen-Sheng Zhao *et al.* [41] calculated optimum number of repeater insertion for Cu and CNT interconnects to minimize the power and delay. The impact of contact resistance and inductance of CNT have been considered and appropriately managed. The impedance parameters of

Cu and CNT as VLSI interconnects have been calculated with the help of mathematical equations for various technology nodes. The number of repeaters insertion and minimum-sized repeater of Cu and the CNT as VLSI interconnect have been obtained by using particle swarm optimization (PSO) method. The obtained results have been validated by the results of analytical and genetic algorithms. The machine learning neural network can be implemented to simplify the design of CAD.

2.3 Carbon nanotube as VLSI interconnects

The conventional Cu used as VLSI interconnect and more preferable for over 50nm technology nodes for VLSI-IC design. The dimensions of interconnects and overall chip area have been reduced for scaled-down technology nodes, especially below 45nm. The conventional Cu material can be replaced with new proposed material as CNTs to resolve the problems related to Cu interconnect. After a detailed investigation, CNT material has been considered as a good alternative material for VLSI interconnect. It has a good alternate because it has incredible mechanical, electrical and thermal properties than Cu material at DSM technology nodes. In the literature, the numerous relevant articles have been reported to discuss the capability of CNT material as VLSI interconnects.

Werner Steinhogl *et al.* [19] observed the resistivity of nanowire for scaled lateral dimension to corresponding bulk material of Cu. The adequate size of Cu wire has been observed upto a particular range of lateral dimensions at scaled-down technology nodes for width ranging from 40 to 800nm, which prepared within the SiO_2 matrix. The resistivity of wire has been increased with decrease in width of interconnect and it has 2.6 times greater for narrowest wire as compared to bulk material of Cu as 1.75 μΩ-cm. The resistance has been calculated at a variable temperature ranging from 77 to 573K. It revealed that the electron scattering has occurred in the nanowire from surface and grain boundaries due to the length of a nanowire shorter than its MFP. The presented model has been considered to observe the impact of electron scattering and it has higher for shorter nanowires.

Azad Naeemi *et al.* [78] discussed the capability of CNTs as VLSI interconnect with the help of physical models. The performance of CNTs has been compared to nanowire of Cu as VLSI interconnect at various technology nodes. The obtained results have provided essential infor-

mation about the nature of CNT at various technology nodes. This information has helped to improve the performance of developed CNT as VLSI interconnect at nano-scaled technology nodes. The CNT bundle may be recommended as VLSI interconnect over single CNT. It concluded that the improvement in the performance of CNT bundles has been observed as 80% at 22nm technology nodes and has been examined negligible at 45nm technology nodes.

Navin Srivastava *et al.* [73] proposed a new delay model for CNTs for global VLSI interconnects at nanotechnology nodes. The performance of CNT bundles has been improved for global interconnect length, but the power dissipation has been increased with negligible value because of the higher metallic density of CNT bundles. The impact of large current density has been increased with increase in temperature of interconnect and has been proposed back-end thermal management in the article. It concluded that Cu interconnects and CNT bundles vias had been integrated and that can enhance the life of Cu interconnect as double and observed 30% reduction in global interconnect delay.

Kaustav Banerjee *et al.* [76] examined the various advantages and challenges of nano-scaled technology nodes for Cu and CNTs. The dimensions of interconnect and chip size of VLSI-IC design have been reduced with scaled-down technology nodes and the active devices per chip have been increased. The resistivity of Cu interconnect has been increased and current density decreases at various DSM technology nodes. However, interconnect has been required high current density to drive number of output stages. CNT has been introduced as new material that can replace Cu material and has increased the lifetime of interconnects.

Hong Li *et al.* [63] presented the current status of research for carbon nanomaterials like CNT and GNR. The carbon-based nanomaterials have been recommended as a next-generation interconnect material for VLSI-ICs because of their properties such as electrical, thermal and mechanical. The electrical and thermal models have been presented for different CNT and GNR structures as VLSI interconnects. These models have been considered to examine the performance and obtained results have been compared to conventional Cu interconnects. The performance of SWCNT, DWCNT and MWCNT have been performed better than conventional Cu as VLSI interconnects. It revealed that GNR interconnect had been needed interlayer doping and edge-specularity to perform better than Cu and CNTs interconnects. The CNT used as long via has been played a vital role in 3-D ICs applications. The carbon nanomaterials have been considered as on-chip interconnects for future VLSI-ICs design at nano-scaled technol-

ogy nodes. The fabrication of on-chip capacitance and inductance have been influenced the form factor and skin effect reduction in the CNT interconnects, respectively.

Chris Rutherglen *et al.* [85] presented the electromagnetic properties of CNT bundles as VLSI interconnects and as a nano-antennas. The properties of CNT as antennas have been presented for a very new topic for making many predictions. In the literature, the predictions have been made for a dipole using various techniques. Nevertheless, the properties of Maxwell's equations have been understood by solving with antenna geometries. The observations have been few and partly because of their fabrication and measurement are challenging.

Navin Srivastava *et al.* [86] examined the capability of SWCNT as VLSI interconnects at different nano-scaled technology nodes for VLSI-IC design. The resistance of SWCNTB as VLSI interconnects has been analyzed on various physical parameters. The 3-D capacitance of SWCNTB has been simulated for realistic dimensions of VLSI interconnect. The significant effect of inductance has been examined for SWCNTB as VLSI interconnects. The CNT has been used as vertical interconnect (as via) that has been addressed first time in the article. The propagation delay of CNT interconnect has been improved as 30%-40% for the global interconnect length. It revealed that the functionality of CNT monolayers has been limited for local level interconnect length, which had mentioned in earlier literature. The power dissipation of dense-CNT bundle as global interconnect has been reduced four times than Cu at 22nm technology nodes. Further, the propagation delay has been examined same as compared to Cu interconnect for the insertion of a similar number of repeaters at 22nm technology nodes. The power dissipation has been decreased to 8-times at 14nm technology nodes.

Daniel Josell *et al.* [136] presented the impact of cross-sectional dimensions on electrical conductance of Cu nanowire as VLSI interconnect at room temperature. The resistivity of nanowire has been influenced dramatically and has increased with the increase in temperature between a few kelvins to hundreds of kelvins. The size-dependent resistivity of Cu has been increased because electron scattering as surface and grain boundary scattering at nano-scale technology nodes. Describing the factors of inventions have been modified in the case of theoretical and experimental results, facilitated or advanced understanding.

Naushad Alam *et al.* [87] investigated the performance of CNT bundles as various interconnects for future VLSI-ICs design at DSM technology nodes. The resistance of CNT bundle

has smaller as compared to Cu as intermediate and global interconnects at DSM technology nodes. However, the resistance of CNT bundles as local level interconnect length has been much higher than Cu. The resistance has been reduced by changing the diameter of CNT and bundle density. The performance of CNT interconnect has been examined without including the effect of high inductance because inductive impedance has been much smaller than resistive effect at nano-scaled technology nodes. However, the capacitance has been smaller for CNT bundles than Cu as various interconnect lengths. It concluded that the CNT bundles had been performed better as compared to Cu as semi-global and global interconnects.

Mayank Kumar Rai *et al.* [130] examined the impact of varying diameters of SWCNTB as VLSI interconnects. The SPICE simulation tool has been considered to obtain the performance of SWCNTB as interconnects in terms of power and delay at 22 and 32nm technology nodes. Further, the obtained results have been compared to similar analyses of Cu as VLSI interconnect. It revealed that the diameter of SWCNTs in bundle affects power and delay. Large diameters of SWCNTs in bundle have been chosen for low power consumption VLSI-IC applications. However, the optimum (if available) diameters of SWCNTs can be considered to increase operational speed of interconnects and the overall performance of high-performance ICs.

Feng Liang *et al.* [137] investigated the number of optimal repeaters and expressions of closed-form for conventional Cu as VLSI interconnects. The modified expressions have been considered to minimize delay of MWCNT as VLSI interconnects. The expressions have been useful by simulation of numerical FDTD circuit for intermediate and global level interconnects. The number of optimal repeaters in the MWCNT as interconnects has been provided significant delay reduction as 50%. The performance of conventional Cu has been compared with similar analysis of MWCNT interconnect. Further, to achieve the minimum interconnect delay has been required one-third number of repeaters insertion in MWCNT as interconnect.

Sandeep Sharma *et al.* [74] examined the performance of various nanostructures such as SWCNTs, SWCNTB, MWCNTs and conventional Cu. The contact resistance occurs due to imperfect contact between CNT and metal, which has been considered to evaluate performance of VLSI interconnect. The performance of conventional Cu as VLSI interconnect has been influenced because of grain boundary and surface scattering. Further, impact of densely packed SWCNTB has been calculated and analyzed. It concluded that the MWCNT had been per-

formed better than SWCNTB and Cu nanostructures for various interconnect lengths at 45nm technology nodes. It concluded that MWCNT interconnect can recommend as local, intermediate and global interconnect for future VLSI-IC applications.

Ahmet Ceyhan *et al.* [64] investigate the problems for long length interconnect, which degrade their performance with scaled-down technology nodes. The resistivity of small length interconnect has been increased drastically at DSM technology nodes. The SWCNTB as VLSI interconnect has been proposed, which has been provided discernible improvement in delay and energy for high-performance circuit at the end of roadmap. Finally, the performance in terms of delay, power and PDP have been evaluated for various types of SWCNTB design as compared to Cu as VLSI interconnect for different technology nodes.

Manodipan Sahoo *et al.* [82] presented the comprehensive performance analysis of Cu and CNT-based nanostructures such as SWCNT, DWCNT and MWCNT for various interconnect levels at technology nodes (45, 32, 22 and 16nm). The highly accurate models for DWCNTs and MWCNTs as interconnects have been established as similar to equivalent ESC model for SWCNT. The closed-form analytical delay formulae for SWCNT, DWCNT and MWCNT as VLSI interconnects have been determined to evaluate the performance at various technology nodes. The improvement in performance of SWCNTB interconnect has been observed by nearly 50% than Cu for local level interconnect at 16nm technology nodes. However, the performance has been improved for DWCNT and MWCNTB than Cu as local level interconnect at 16nm technology nodes as 35% and 50%, respectively. For intermediate interconnects, the performance of densely packed SWCNT, dense DWCNT and MWCNTB has been examined as 85%, 75% and 80% at 16nm technology nodes, respectively. For global interconnects, the improvement in the performance of dense SWCNT, dense DWCNT and MWCNT has been calculated as 85%, 75% and 85% at 16nm technology nodes. It concluded that the improvement in the performance of carbon-based nanostructures had been influenced by the scaling of interconnect levels at various technology nodes. It concluded that the ratio of delay for CNT to Cu interconnects has been calculated and observations have agreed with the published work.

Prakhar Litoria *et al.* [138] presented the model to examine the impact of inter-shell tunneling conductance on the performance of MWCNTs as VLSI interconnect at different technology nodes as 32, 22 and 16nm. It indicated that the increase in length of interconnect has been enhanced the effect of inter-shell tunneling conductance and also increased with the scaled-

down the technology node from 32 to 16nm. According to the results, the effect of the tunneling conductance cannot be ignored for the local level interconnects at DSM technology node.

2.4 MWCNT and Mixed-MWCNT bundles as interconnect

MWCNT has number of concentric shells with various diameters and its outermost shell has large diameter. The MWCNT has a large number of conducting channels and large MFP as compared to SWCNT. The equivalent resistance of MWCNT has smaller as compared to SWCNT, but current carrying capacity is same for both. However, the fabrication process of MWCNT is easier than SWCNT because their growth process can control easily. The MWCNTB as VLSI interconnects has performed better than SWCNTB. Further, the nanostructure of MWCNTB has much vacant space between four adjacent MWCNTs, corners and side-walls, which is responsible for decreasing the conductivity of the MWCNTB as interconnect. Few researchers have proposed various nanostructures to overcome this problem by inserting the various types of MWCNTs in a bundle and developed bundle is known as Mixed-MWCNT (MMT) bundle. These bundles are considered as VLSI interconnect at DSM technology nodes and evaluate the performance for various interconnect lengths at DSM technology nodes.

H. J. Li *et al.* [107] investigated the electrical transport of vertical MWCNT at room temperature in scanning electron microscope (SEM) chamber. It has been observed that MWCNT was carried large current as 7.27mA (maximum). The obtained resistance and conductance have been lowest (nearly $\sim 34.4\Omega$) and high (about 460-490$\mho$), respectively. The results revealed that a multichannel quasi-ballistic conduction in large diameter MWCNTs has been attributed to involvement of several walls in electric transport and large diameter-MWCNTs.

Azad Naeemi *et al.* [139] developed the electrical models to observe the conductivity of MWCNTB as VLSI interconnects. The conductance of MWCNT for short interconnect length has been decreased with increase in diameter. However, the conductance of MWCNT has been examined high for long interconnect length at large diameters of MWCNT. The conductivity of MWCNTs as long interconnect lengths have been observed to be several times greater than Cu and SWCNTB. It has been shown that the SWCNTB can be used for short interconnect lengths because it offers high conductance almost two times MWCNTs.

Azad Naeemi *et al.* [134] utilized a physics-based circuit model approach to contrast the per-

formance of both single and multiwall carbon nanotube (CNT) as VLSI interconnect materials with Cu at a 100°Ctemperature. The comparison of resistivity of various CNT bundles and Cu has been presented according to decreasing technology nodes year per year. The dependency of quantum capacitance along temperature and CNT diameter has been captured by the circuit models for different scattering phenomena. The performance of Cu and CNT interconnects has been affected with variation in temperature and has been investigated at a practical temperature range. Finally, the authors have been established a hybrid system of Cu, SWCNT and MWCNT interconnects to achieve the better performance.

Hong Li *et al.* [140] presented the frequency-dependent electrical impedance models for SWCNT and MWCNTB as interconnect. The high kinetic inductance has been occurred in the CNT because of considerable momentum relaxation time and it has been reduced the skin effect than conventional metal conductors. Due to that, CNTs have been promising and more suitable material for high-frequency applications. The performance of MWCNTs has been observed better than SWCNTs because of low dc resistivity and less skin effect of MWCNTs. The MWCNTs have been preferred at high-frequency for CNTs-based on-chip inductors. The Q-factor of these types of inductors has been obtained much higher than Cu without using any improvement technique or any magnetic materials. The fabrication of metallic-SWCNTs and highly dense bundles have been remained a challenge. The MWCNTB can be used as future high-frequency VLSI interconnect applications.

Hong Li *et al.* [16] discussed the metallic CNTs based MWCNTB as VLSI interconnects. The equivalent circuit model has been presented to observe the performance and described the analysis of MWCNT as VLSI interconnects. The observed results were compared with Cu and SWCNT as interconnects (like local, intermediate and global interconnects) at various technology nodes. The MWCNT interconnect has been observed less delay as compared to Cu interconnect for intermediate and global interconnects. The delay for intermediate and global interconnect was improved as 15% of the Cu interconnects, whereas it can be a noticeable change with scaling down the technology nodes. It revealed that the SWCNTB interconnects has been outperformed MWCNT interconnects, however, the fabrication of MWCNTs can be easier than SWCNTs because MWCNTs has better control on their growing process.

Yograj Singh Duksh *et al.* [94] presented an electrical model of MWCNT as VLSI interconnects to evaluate the delay and power for different number of shells and driver-size at 22nm

technology nodes. The results obtained from the MWCNT have been compared with Cu interconnect and it observed that MWCNT has less delay than Cu. Further, it has been noticed that the delay ratio becomes smaller if the number of shells and driver size increases. The power ratio has been reduced by increase in the driver size and decrease in number of shells. Finally, it concluded that MWCNT as VLSI interconnects have a less delay at the global level interconnects as compare to Cu interconnects for specific driver size.

Ashok Srivastava *et al.* [141] presented the fluid model of 1-D application in electron transport modeling of CNTs. The equivalent impedance model has been developed to evaluate performance of VLSI interconnect and results have been compared to Cu interconnects. The electron transport of CNTs has been considered a quasi 1-D fluid with strong electrons interaction. The simulation technique as Verilog-AMS in Cadence/Spectre has been used to analyze the results. The SWCNT, MWCNT and other bundles of CNTs as interconnects (local and global level) have been regarded for ballistic conduction region. A complementary pair of CNT-FET inverter has been used for simulating the analytical model and computer-aided technique. The performance of CNTs as VLSI interconnect has been improved by increase in number of metallic CNTs in a bundle.

Anil Kumar *et al.* [99] analyze the signal noise and crosstalk delay for different types of interconnect materials like Cu, SWCNTB and MWCNT. The ESC models for the different types of interconnects such as MWCNT, SWCNTB and Cu. The research revealed that overall crosstalk delay has been reduced for MWCNTs than SWCNTB and Cu. The results has shown that MWCNTs outperformed SWCNTB and Cu at DSM technology nodes (32, 22 and 16nm). The MWCNT has more suitable materials as the global VLSI interconnects.

Iman Madadi *et al.* [106] investigated the limitations of traditional Cu as VLSI interconnects at DSM technology nodes for future VLSI-ICs design. These problems have been overcome to replace Cu with CNT-based nanostructure as SWCNT and MWCNT. The dc resistance of MWCNT as VLSI interconnect has been calculated in two different levels of bias voltage as low and high for various geometric structures. The resistance of MWCNTB of various numbers of shells and Cu has been calculated. The analytical equation has been developed to observe the total resistance of MWCNT. The performance of MWCNTs interconnect in terms of power and delay has been performed better than Cu interconnect.

Min Tang *et al.* [142] established electrical ESC model with detailed analysis of the MWCNT interconnect. ESC model has been recommended to examine the impact of inter-shell tunneling conductance. Tunneling conductance and imperfect contact resistance have been considered to analyze their accuracy and efficiency. The analytical results of single MWCNT and coupled MWCNT have been investigated as VLSI interconnects. The accuracy of ESC model has been influenced due to high imperfect contact resistance.

M. Kaur *et al.* [96] discussed capability of CNT material to replace Cu material as on-chip interconnects for high-performance VLSI-ICs. The MWCNTs are highly dense and better control on chirality as well as growth process of SWCNTs for global level interconnects. The impact of geometrical parameters has been calculated and analyzed on impedance parameters such as RLC for global level VLSI interconnects. The number of conducting channels has been increased in MWCNT due to increase in number of shells that have been decreased its resistance and inductance, however the inter-shell capacitance of MWCNT has been increased. For shorter interconnect length ($<$100μm), no improvement in performance has been observed because their high resistance, while, there is a significant impact on the resistance of intermediate ($<$500μm) and global ($>$500μm) interconnects lengths. The performance of MWCNTs such as delay, power and PDP has been influenced by changing the aspect ratio of MWCNTs bundles. The obtained results have been compared with SWCNTB and Cu at various technology nodes (32, 22 and 16nm) for global interconnect.

Manoj Kumar Majumder *et al.* [114] presented a model to analyze the performance of MMT for various diameter and number of shells of each MWCNT. The results have been observed for different arrangement:- firstly, Mixed bundle (MB) with the same number shells and diameter for MWCNTs, other bundle has number of shells and diameter of MWCNTs are different (MMB). The results and experimental observations have been shown that MMB superior to MB. The propagation delay and crosstalk in the case of MMB have been reduced than MB 15.33% and 29.59%, respectively.

Pankaj Kumar Das *et al.* [143] developed the analytical models for the different arrangement of MWCNT bundles. The ESC model has been developed based on multi conductor transmission line (MTL) theory for MMB arrangements. The fabrication process of MMB (MWCNTs of different diameters within bundle) has been more comfortable than MB (MWCNTs of same diameter in bundle) because it has too hard to control the growing process of MWCNTs with

the same diameter. The crosstalk delay of MMB and MB for different transition time and inter bundle space is 5 to 30nm. The results revealed that overall crosstalk delay of MMB has been reduced by 47.26% as compared to MB.

Karmjit Singh Sandha *et al.* [113] presented the overall performance and analysis of various MB and MMB as a global interconnect level for future VLSI-IC design. The MMB and MB nanostructure have been developed using various MWCNTs of the different number of shells and identical MWCNTs, respectively. The electrical ESC models have been proposed for all types of structures considered in this paper to examine the performance as delay, power and PDP. The ESC models have been developed with the help of multi-conductor transmission line models for all structures at interconnect length ranging from 500 to 2000μm on various DSM technology nodes. The calculated results of various MB have been compared with the results of various MMB nanostructures. The comparative analysis revealed that the performance of MMB nanostructures has been outperformed MB nanostructures in terms of delay, power and PDP for various global interconnect lengths. Further, the MMB can be preferred as future global level interconnect material than MB nanostructures for VLSI-IC design at DSM technology.

2.5 Impact of temperature on the performance of MWCNTB, SWCNTB and Cu interconnect

The performance of high-performance VLSI interconnects has highly influenced by a variable temperature range. It plays a important role in enhancement of scattering such as surface and grain boundary scattering in SWCNT, MWCNT and Cu interconnects at DSM technology nodes. The impedance parameters of VLSI interconnects are enhanced because of the electron scattering. The temperature-dependent impedance parameters of VLSI interconnects considered to examine the performance in terms of delay, power and PDP. The impact of variable temperatures on the performance of various interconnect materials needs to investigate at DSM technology nodes. The literature shows that few researchers are proposed various models, which include the effect of variable temperature.

Eric Pop *et al.* [128] presented the extracting technique for thermal conductivity of individual metallic-SWCNTs from their I-V characteristics of a temperature ranging from 300 to 800K.

The thermal conductivity and conductance for SWCNT having length as 2.6μm with diameter as 1.7nm have been observed as 3500W/mK and 2.4nW/K, respectively. The observed slope of thermal conductivity has been decreased for higher temperature range and it ascribed for 2-order 3-phonon scattering from 2-acoustic to 1-optical mode. In this article, the simple analytical model for thermal conductivity of SWCNT has been proposed on length and temperature dependent.

Eric Pop *et al.* [101] studied the electro-thermal conductance of metallic-SWCNTs interconnects. For short interconnect length applications ($<$1μm), the self-heating has been played a significant role, which has been analyzed by using accurate model and experimental data. Impact of optical phonon absorption of micro-scaled SWCNT has been observed over the temperature range of 250K. The electrical breakdown of SWCNTs has been investigated for variable length in the atmosphere's air. If the power densities of SWCNT interconnects have been limited upto 5μW/μm, then the self-heating can be ignored.

Andrea G. Chiariello *et al.* [125] calculated the impact of variable temperature and size of interconnect on the performance and current density. The resistance models have been presented as a function of temperature for CNTs and Cu materials as VLSI interconnects at 22nm technology nodes. The proposed thermally-aware and size-dependent resistance model for CNT as VLSI interconnect has been very simple and more accurate.

Amir Hosseini *et al.* [127] investigated the performance of traditional Cu material and temperature-dependent SWCNTB as VLSI interconnects at DSM technology nodes. The limitations of Cu over nanotechnology nodes have also been described as compared to SWCNTB. CNTs have the potential to replace the Cu material as high-performance VLSI interconnect applications. The thermally-aware impedance model has been proposed with high accuracy for SWCNT interconnects to examine the effect of temperature-dependent performance (approximation) of SWCNTB interconnects over variable temperature conditions. The accuracy of proposed electro-thermal model has been improved up-to 51% (average) in case of propagation delay. It is concluded that the reduction in delay for simulation results of SWCNTB interconnects have been provided five times more as a function of temperature range between 27 and 127°C.

Pierre Gautreau *et al.* [144] studied the hot phonon that has a significant impact on the scattering of electron-phonon. The joule heating used Ensemble Monte Carlo (EMC), which has

been simulated with stepwise updating of total phonon consider to generate hot phonon. The role of hot phonon in the joule heating appeared as a function of electric field at room temperature. It revealed that joule heating by hot phonon influenced significantly high at room temperature, however it declined for high temperature. The EMC simulation results have been recommended for an extremely high temperature of about 1800K and more than that the joule heating effect may be reduced for SWCNTs by non-equilibrium phonon.

Karmjit Singh *et al.* [66] investigated the performance of MWCNTB as VLSI interconnect for variable temperature range at technology nodes (32, 22 and 16nm). A comparative analysis has been done for the performance of MWCNTB interconnect with similar analysis for Cu interconnect. The comparative analysis revealed that delay and PDP have been increased for increasing temperature ranging from 200 to 450K. It concluded that the MWCNTB has been outperformed Cu interconnect at different technologies for global interconnects in term of power, PDP and delay.

Karmjit Singh *et al.* [97] presented the impact of variable temperature on performance of MWCNT, SWCNT and Cu interconnect at various DSM technology nodes. Thermally-aware ESC model for MWCNTB as VLSI interconnects has been established at various DSM technology nodes. Temperature-dependent electron-phonon scattering phenomena has been examined for the MWCNTB interconnect as a function of temperature. The performance of the MWCNTB has been observed for a variable temperature range (from 200 to 500K) at DSM technology nodes (32, 22 and 16nm). The obtained results from the MWCNTB have been compared with a similar analysis of SWCNTB and Cu interconnects at various technology nodes. It concluded that the MWCNTB has been performed better than SWCNTB and Cu interconnect for a variable temperature range at nanotechnology nodes.

Karmjit Singh *et al.* [131] studied effect of temperature of SWCNTB interconnect at various technology nodes. The power and delay of SWCNTB have been compared with similar results of Cu interconnect at various technology nodes like 32, 22 and 16nm. Moreover, simulation results proved that the densely packed SWCNTB can be easily replaced Cu as global interconnects for advanced technology nodes.

Mayank Kumar Rai *et al.* [145] investigated the performance of temperature-dependent and temperature-independent for SWCNTB as VLSI interconnects in terms of delay, power and

crosstalk noise. The results of SWCNTB interconnects have been compared to the results of Cu, which reported in the literature at 22nm technology node. It revealed that delay of SWCNTB has been lower than Cu as interconnects with increased temperature ranging 300-500K at various interconnect lengths (from 100 to 1000μm). However, this trend reversed in the case of power dissipation. The performance parameters (temperature-dependent to temperature-independent) has been improvement as nearly 22.44% for the delay, 7.59% for power and 31.96% for PDP at variable interconnect lengths (from 100 to 1000μm). It revealed that the performance has also been improved delay as 16.6%, power as 5.6% and PDP as 19.72% for a variable diameter of CNT shells.

2.6 Research Gaps in present Study

Carbon Nanotube as VLSI interconnects is an alternative material for the forthcoming IC design. The related reported work shows that the CNT outperforms as compared to Cu, which make capable of replacing Cu in the field of interconnects. As the technology nodes reduced to DSM, CNT became preferable for VLSI interconnects as compared to Cu, especially below 45nm technology nodes. The resistance of Cu increases suddenly as the feature size becomes closer to the MFP of Cu (below 45nm technology nodes), which reduces the performance of interconnect. Therefore, CNT used as VLSI interconnects has capable to overcome the problems of Cu interconnect. It can be good alternative material as future of VLSI interconnects for high-performance IC design.

MWCNTs have less power consumption for intermediate and global interconnects. It performs better for intermediate and global level VLSI interconnect. MWCNTs have relatively low sensitive and smaller variations in resistance. The effect of separation of adjacent shells in the MWCNT plays a critical role to estimate propagation delay and power dissipation. The resistance and inductance of MWCNT increases, however capacitance decreases with decreasing number of shells in MWCNTs because these are inversely proportional and directly proportional, respectively. So, number of shells in MWCNTs affects the performance of MWCNTs as interconnects. The modeling of MWCNT is complex because it has various number of shells as compared to SWCNT (only single shell). However, the fabrication of MWCNT is easier than SWCNT bundle with fixed diameter of each SWCNT in a SWCNT bundle because SWCNT has no control on their growth process.

It reveals from the literature that different nanostructures of MMT can be used as VLSI interconnect at DSM technology nodes. Further, it concluded from previous studies available in the literature that the MWCNTB and MMT can outperform because of their low resistance and less delay as compared to various CNTs arrangements as VLSI interconnect. The fabrication of MMT can be easier than MWCNT and SWCNT bundle because MMT nanostructure has no issues related to chirality and density controls. The performance of MMT influences under thermal variable environmental conditions, which impact the scattering, delay, power and PDP. Literature shows that little work has been reported and needs to be focused more on the thermally-aware working environment, which can be affected the performance parameters of the MMT nanostructures as VLSI interconnects. Therefore, the temperature impact can be observed by varying the number of shells and the separation gaps between the walls at various technology nodes.

2.7 Objectives of Proposed Research Work

The following objectives have included based on the literature review, as reported in this chapter and according to initial studies.

1. To develop the temperature dependent impedance equivalent models for Mixed-MWCNT bundle as VLSI interconnect.
2. To analyze the impact of temperature on the impedance parameters of Mixed-MWCNT bundle at deep submicron technology nodes for global interconnect length.
3. To evaluate the temperature dependent performance of Mixed-MWCNT in terms of delay, power dissipation and PDP at different technology nodes.
4. To compare the results obtained from the above analysis with similar analysis for MWCNT, SWCNT and copper interconnects.

2.8 Research Methodology

The methodology for research work to be done for proposed Ph.D. proposal will have the following constituent components.

The Mixed-MWCNT (MMT) nanostructure is to be designed by inserting two differently-sized MWCNTs such as $MWCNT_L$ (large diameter MWCNTs) and $MWCNT_S$ (small diameter MWCNTs). The designed MMT nanostructure will be much denser than MWCNT bundle and highly conductive because of inserted metallic $MWCNT_S$ to fill vacant space created adjacent four MWCNTs. The developed MMT nanostructure is to be used to develop equivalent single-conductor (ESC) model as VLSI interconnect at DSM technology nodes. Further, to evaluate parasitic of the developed ESC model of MMT nanostructure as global interconnect at room temperature. ESC model is to be simulated with the help of SPICE tool to calculate actual performance in terms of delay, power and PDP for global interconnect at DSM technology nodes. The obtained results of MMT interconnect (temperature-independent) compare with similar results of copper interconnect at various technology nodes.

Furthermore, to develop a temperature-dependent ESC model for MMT nanostructure as VLSI interconnect at DSM technology nodes. The temperature-dependent parasitic of MMT nanostructure will be compared with temperature-independent at various technology nodes for various temperatures. Temperature-dependent performance of MMT nanostructure will be simulated with the help of SPICE tool to examine in terms of delay, power and PDP. The obtained results compare with temperature-dependent performance of Cu, SWCNTB and MWCNTB as global interconnect at DSM technology nodes. Finally, the comparative performance analysis to be done and conclusion will be drawn.

Chapter 3

Performance and Analysis of MMT nanostructure

In this chapter, the nanostructure of the Mixed-MWCNT bundle (MMT) is proposed as a suitable candidate for interconnect to design high-performance VLSI circuits. The proposed MMT nanostructure as VLSI interconnect is implemented by two differently-sized MWCNTs into a single bundle. The electrical Equivalent Single-Conductor (ESC) model is developed for proposed MMT nanostructure with the help of derived mathematical expressions for various Deep Sub-Micron (DSM) technology nodes. The parasitic of MMT interconnect is calculated for various interconnect lengths at DSM technology nodes. The calculated parasitic of MMT is simulated to evaluate the performance in terms of delay, power and power delay product (PDP) for an interconnect length ranging from 400 to 2000μm at DSM technology nodes viz. 32, 22 and 16nm. Further, the ESC models of Cu interconnect at DSM technology are determined to calculate the parasitic for various interconnect lengths. The performance of proposed MMT nanostructure is analyzed and compared with results of Cu interconnect at DSM technology nodes for various interconnect lengths.

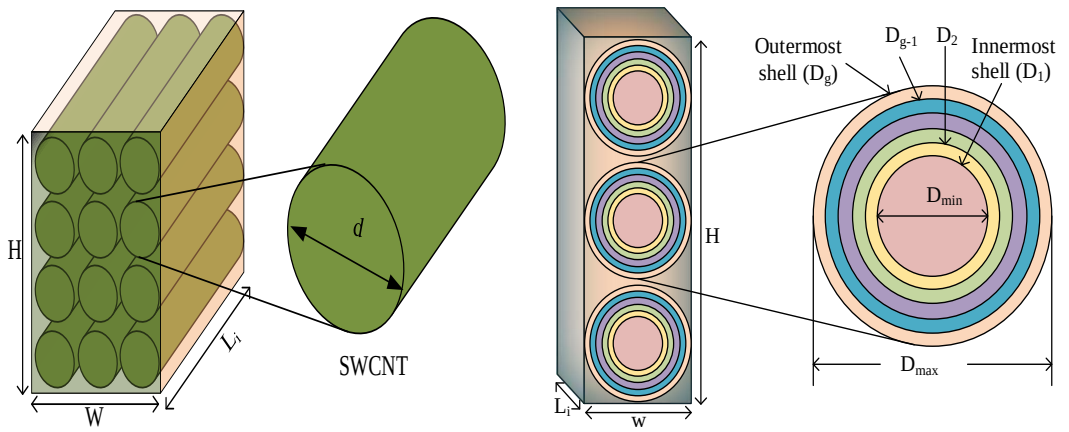
3.1 Introduction

The electronic industry requires fast operational speed for ICs at DSM technology nodes. The operational speed of ICs depend on the parasitic of VLSI interconnect at micro-scaled and nano-scaled technology nodes, where the parasitic of interconnect are influenced by different factors such as current density, thermal conductivity and electron MFP. The performance of VLSI interconnect degrades due to a significant variation in their parasitic that increases the delay of VLSI-ICs. [12, 24, 63]

Conventional Cu is used as VLSI interconnect material for high-performance IC design [58–60]. However, below 45nm technology nodes, Cu material has some limitations such as surface and grain boundary scattering. The increase in scattering results to shrinkage of MFP because

the cross-sectional dimensions of interconnects are reduced at scaled-down technology nodes. Due to that, a sudden increase in resistance of Cu interconnects, which degrade its performance at DSM technology nodes. Further, the electro-migration occurs at high current because Cu has low current density and small MFP ($\approx 40nm$) [146–149]. Therefore, it is necessary to address the above mentioned problems to obtain the desire performance of VLSI interconnect at DSM technology nodes. Thus, the literature proposed carbon nano-materials (CNT and GNR) are proposed as new material to replace Cu for VLSI interconnects at DSM technology nodes. [64–67, 150]

Literature shows that CNT has low resistance, high current density, high thermal stability and large electron MFP as compared to Cu. The CNT is a promising candidate to replace the conventional Cu as interconnect for future VLSI-IC design at DSM technology nodes. The CNT is formed by rolling up the graphene sheet into the shape of cylinder and can be classified into two types:- SWCNT and MWCNT. CNT may be metallic or semiconducting that depends on the chirality (rolling direction of graphene sheet) [72–75]. SWCNT is developed by rolling a single sheet of graphene into tubular shape and has only single shell of diameter ranging from few to several nm [16, 150, 151]. The SWCNT bundle (SWCNTB) is developed using similar types of SWCNTs having same diameter (d) as shown in Figure 3.1(a) [152]. SWCNTB is difficult to fabricate with same diameter of each SWCNT because it has no control on their growth process [133, 134].



(a) (b)

Figure 3.1: Nanostructures used as VLSI interconnects (a) SWCNTB and (b) MWCNTB. [97]

MWCNT is formed by rolling two or more sheets of graphene in tubular shape, concentrically inserted [90–93]. MWCNT has number of individual shells and each shell of MWCNT have different diameter. The diameter of outermost shell varies from few to several tens of nm. The

MWCNTB is formed using MWCNTs of similar number of shells and same diameters of inner and outermost shells as shown in Figure 3.1(b) [94–96]. The fabrication of MWCNTB is easier because there is better control on its growth process. Moreover, the modeling of MWCNTB is complex as compared to SWCNTB [97–99]. However, the large space around the side-walls and corners lefts vacant in MWCNTB as shown in Figure 3.2(a). It is proposed in literature that the vacant space can be filled with the similar-sized SWCNTs, which is known as Mixed-CNT bundle and it is shown in Figure 3.2(b) [111, 112]. Such type of Mixed-CNT bundles are difficult to fabricate as similar-sized SWCNTs have no control on their growing process.

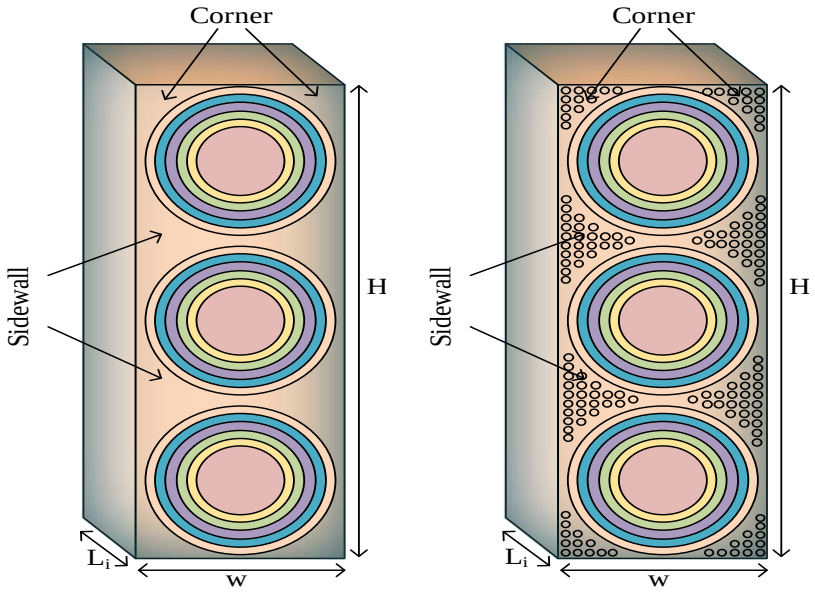
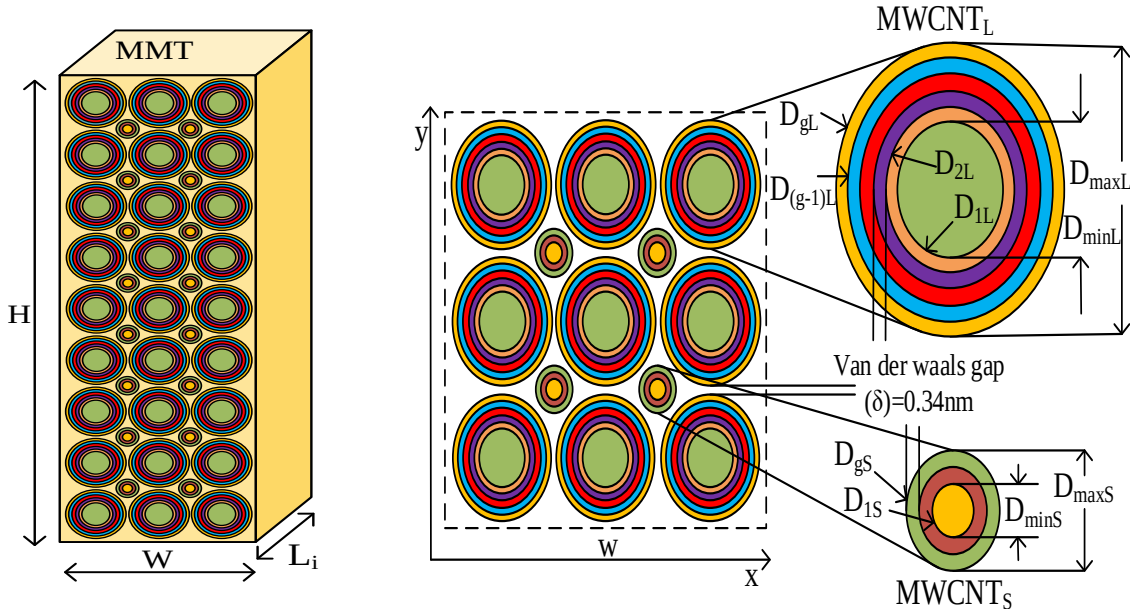


Figure 3.2: (a) the vacant space around side-walls and corners in MWCNTB [109] (b) Mixed-CNT bundle.

In this chapter, the proposed MMT nanostructure for interconnect is different from available structures given in reported literature. The proposed MMT nanostructure is a mixer of two differently-sized MWCNTs as shown in Figure 3.3(a). These two differently-sized MWCNTs are representing as $MWCNT_L$ (MWCNT with large diameter) and $MWCNT_S$ (MWCNT with small diameter). The partially enlarged view of proposed nanostructure is shown in Figure 3.3(b). MMT is denser because $MWCNT_S$ is inserted to occupy vacant space among four adjacent $MWCNT_L$ as shown Figure 3.3. Due to the insertion of multiple conductive $MWCNT_S$, the overall conductivity of the bundle increases, which improves the performance of proposed MMT interconnect in terms delay, power and PDP. The proposed MMT nanostructure is considered to analyze the performance of various interconnects at DSM technology nodes.



(a) (b)

Figure 3.3: (a) Proposed MMT nanostructure (b) A partially enlarged view of MMT with an individual structure of MWCNTs ($MWCNT_L$ and $MWCNT_S$)

In the previous studies, various impedance models have been presented for the SWCNTB, MWCNTB and Cu at different DSM technology nodes. This chapter proposed an electrical ESC model for MMT nanostructure as VLSI interconnect at various technology nodes (32, 22 and 16nm). The proposed model is used to calculate parasitic of MMT for various interconnect lengths (400 to 2000μm). Similarly, the ESC model for Cu interconnect is developed to compute the parasitic for variable interconnect lengths at DSM technology nodes. The obtained results of proposed MMT are compared with the results of Cu interconnect.

Further, the impedance parameters are considered to evaluate the performance of MMT and Cu nanostructures at DSM technology nodes for various interconnect length. The evaluated performance of proposed MMT nanostructure is analyzed and compared with performance of Cu as VLSI interconnect in terms of delay, power and PDP at DSM technology nodes.

3.2 Impedance model of MMT interconnects

The MMT nanostructure as VLSI interconnect are proposed by combining two differently-sized MWCNTs such as $MWCNT_L$ and $MWCNT_S$ as shown in Figure 3.3. The proposed MMT nanostructure is denser because of its arrangement, number of $MWCNT_S$ bundles is inserted to occupy the space between four adjacent $MWCNT_L$ bundles. The overall resistance of proposed MMT bundle decreases due to inserting the number of conductive $MWCNT_S$

bundles. The cross-sectional view of $MWCNT_L$ and $MWCNT_S$ is different as shown in Figure 3.3(b). The diameters of the innermost and outermost shell of MWCNTs are denoted as D_{min} and D_{max}, respectively. The ratio of D_{min} to D_{max} is known as diameter ratio and this varied from 0.8 to 0.35 [16]. The diameter ratio is considered as 0.5 for this work. The separation between individual adjacent shells of a MWCNT and different MWCNTs is known as Van Der Waals gap and this is considered 0.34nm [16] as shown in Figure 3.3(b).

3.2.1 Total Number of MWCNTs in the MMT nanostructure

The number of MWCNTs (N_{MMT}) in a MMT nanostructure as VLSI interconnect can be calculated by using following equation

$$N_{MMT} = N_{MWCNT_L} + N_{MWCNT_S} \tag{3.1}$$

where, N_{MWCNT_L} and N_{MWCNT_S} are the number of $MWCNT_L$ and $MWCNT_S$ available in the MMT nanostructure, which can be calculated by the following equations

$$N_{MWCNT_L} = N_{X_L} N_{Y_L} \tag{3.2}$$

$$N_{MWCNT_S} = N_{X_S} N_{Y_S} \tag{3.3}$$

N_{X_L} and N_{Y_L} are used to calculate the number of available $MWCNT_L$ in direction of x-axis and y-axis in the MMT nanostructure. Similarly, N_{X_S} and N_{Y_S} are used to obtain the number of available $MWCNT_S$ in direction of x-axis and y-axis in the MMT nanostructure. N_{X_L}, N_{Y_L}, N_{X_S} and N_{Y_S} can be calculated by the following equations

$$N_{X_L} = \frac{W}{D_{max_L} + \delta} \tag{3.4}$$

$$N_{Y_L} = \frac{H}{D_{max_L} + \delta} \tag{3.5}$$

$$N_{X_S} = round(N_{X_L}) - 1 \tag{3.6}$$

$$N_{Y_S} = round(N_{Y_L}) - 1 \tag{3.7}$$

W, H, δ and D_{max_L} are width, height of interconnect, spacing between two adjacent MWCNTs (as 0.34nm) and diameter of outermost shell of $MWCNT_L$, respectively. round () represents only closest integer.

3.2.2 Number of shells and conducting channels per shell in MWCNT

The number of shells for differently-sized MWCNTs such as $MWCNT_L$ and $MWCNT_S$ are determined by varying the diameters of individual shell of a MWCNT. The number of shells in a MWCNT can be counted from outer- to inner-most shell as 1, 2,. . . , g,. . . ., N_{sh} [129] as shown in Figure 3.3(b). The number of shells for $MWCNT_L$ and $MWCNT_S$ can be calculated by

$$N_{sh_L} = 1 + round\left(\frac{D_{min_L}}{2\delta}\right) \tag{3.8}$$

$$N_{sh_S} = 1 + round\left(\frac{D_{min_S}}{2\delta}\right) \tag{3.9}$$

where, D_{min_L} and D_{min_S} are the diameters of innermost shells of $MWCNT_L$ and $MWCNT_S$ for MMT nanostructure.

The diameters of any individual g^{th} shell of $MWCNT_L$ and $MWCNT_S$ are denoted as D_{g_L} and D_{g_S}, respectively. These can be calculated by [121]

$$D_{g_L} = D_{max_L} - 2\delta(g_L - 1) \qquad for \quad 1 \leq g_L \leq N_{sh_L} \tag{3.10}$$

$$D_{g_S} = D_{max_S} - 2\delta(g_S - 1) \qquad for \quad 1 \leq g_S \leq N_{sh_S} \tag{3.11}$$

The number of conducting channels of any g^{th} shell of $MWCNT_L$ and $MWCNT_S$ can be obtained as [7]

$$N_{ch/sh} \approx 2/3 \qquad \text{for diameter of any } g^{th} < 3\text{nm} \tag{3.12}$$

$$N_{ch/sh_L} \approx aD_{g_L} + b \qquad \text{for diameter of any } g^{th} > 3\text{nm} \tag{3.13}$$

$$N_{ch/sh_S} \approx aD_{g_S} + b \qquad \text{for diameter of any } g^{th} > 3\text{nm} \tag{3.14}$$

where, a=1.836x10^{-1}/nm, b=1.275 [127].

Now, the number of conducting channels of the MMT nanostructure (N_{ch}^{MMT}) can be calculated by adding all the conducting channels of individual shells of $MWCNT_L$ ($N_{ch}^{MWCNT_L}$) and $MWCNT_S$ ($N_{ch}^{MWCNT_S}$), which is given by following equations

$$N_{ch}^{MMT} = N_{MWCNT_L} * N_{ch}^{MWCNT_L} + N_{MWCNT_S} * N_{ch}^{MWCNT_S} \tag{3.15}$$

$$N_{ch}^{MWCNT_L} = \sum_{g=1}^{N_{sh_L}} N_{ch/sh_L} \tag{3.16}$$

$$N_{ch}^{MWCNT_S} = \sum_{g=1}^{N_{sh_S}} N_{ch/sh_S} \tag{3.17}$$

where, N_{sh_L} and N_{sh_S} are the number of shells of $MWCNT_L$ and $MWCNT_S$ in MMT nanostructure.

3.2.3 Impedance parameters of MMT nanostructure

The performance of VLSI interconnect depends on the impedance parameters such as inductance, resistance and capacitance. The electrical equivalent circuit (EEC) model of an individual shell of the MWCNT is shown in Figure 3.4.

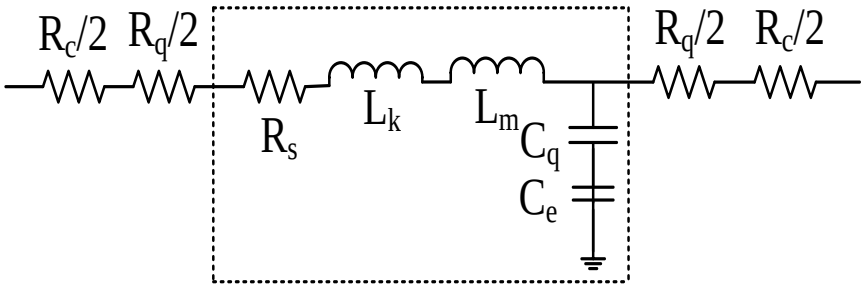


Figure 3.4: EEC model of an individual shell of the MWCNT [16].

A. Resistance of the MMT nanostructure

The resistance (R_{sh}) of an individual MWCNT shell consists of scattering resistance (R_s), quantum resistance (R_q) and contact resistance (R_c). The resistance (R_{sh}) of each MWCNT shell can be calculated as [111]

$$R_{sh} = R_c + R_q + R_s * L_i \tag{3.18}$$

where, L_i is the length of individual MWCNT shell.

The quantum resistance (R_q) exists due to quantum confinement of electrons in nano-wire and can be calculated by [111]

$$R_q = \frac{h}{2e^2}\frac{1}{N_{ch/sh}} \tag{3.19}$$

where, $\frac{h}{2e^2}$ is the quantum intrinsic resistance ($12.9k\Omega$). h and e are the plank's constant and electron charge, respectively.

The scattering resistance (R_s) occurs because the length of CNT as VLSI interconnect is large than its MFP and given by the following equation [123]

$$R_s = \frac{h}{2e^2}\frac{1}{N_{ch/sh}\lambda} \tag{3.20}$$

where, λ is MFP of individual shell of MWCNT and calculated for constant thermal environmental condition at room temperature using the equation given below [16]

$$\lambda = 1000D_g \tag{3.21}$$

D_g is diameter of the g^{th} shell of MWCNT.

The contact resistance (R_c) occurs due to imperfect contact between the metal and shells of CNTs, which is measured from hundred to hundreds of kilo Ω. It can be minimized by making perfect contact between the metal and shells of MWCNT through the fabrication process and considered as $2k\Omega$ in this research work [106].

Now, the resistance (R_{ESC}) of MMT interconnect can be calculated assuming all the shells of MWCNTs to be parallel and can be determined as [113, 114]

$$R_{ESC} = R_c + R_{qESC} + R_{sESC} * L_i \tag{3.22}$$

where, R_{qESC} and R_{sESC} are the combining resistance of all the quantum resistance and scattering resistance of individual shells of $MWCNT_L$ and $MWCNT_S$ considering in parallel combination. R_{qESC} and R_{sESC} can be calculated as

$$R_{qESC} = (R^{-1}_{qESC_L} + R^{-1}_{qESC_S})^{-1} \tag{3.23}$$

$$R_{sESC} = (R^{-1}_{sESC_L} + R^{-1}_{sESC_S})^{-1} \tag{3.24}$$

R_{qESC_L} and R_{qESC_S} are the quantum resistance of all $MWCNT_L$ and $MWCNT_S$ in the MMT nanostructure, respectively. Similarly, R_{sESC_L} and R_{sESC_S} are the scattering resistance of all

$MWCNT_L$ and $MWCNT_S$, respectively. These can be calculated by the equations

$$R_{qESC_L} = \frac{h}{2e^2}\frac{1}{N_{MWCNT_L}N_{ch}^{MWCNT_L}} \tag{3.25}$$

$$R_{qESC_S} = \frac{h}{2e^2}\frac{1}{N_{MWCNT_S}N_{ch}^{MWCNT_S}} \tag{3.26}$$

$$R_{sESC_L} = \frac{h}{2e^2}\frac{1}{N_{MWCNT_L}\sum_{g=1}^{N_{sh_L}} N_{ch/sh_L}\lambda_L} \tag{3.27}$$

$$R_{sESC_S} = \frac{h}{2e^2}\frac{1}{N_{MWCNT_S}\sum_{g=1}^{N_{sh_S}} N_{ch/sh_S}\lambda_S} \tag{3.28}$$

$N_{ch}^{MWCNT_L}$ and $N_{ch}^{MWCNT_S}$ are calculated by the Eqs. 3.16 and Eqs. 3.17, respectively. λ_L and λ_S can be calculated by the following equations

$$\lambda_L = 1000 D_{g_L} \tag{3.29}$$

$$\lambda_S = 1000 D_{g_S} \tag{3.30}$$

D_{g_L} and D_{g_S} are the diameter of any g^{th} shell of individual $MWCNT_L$ and $MWCNT_S$, respectively.

The separation between adjacent shells ($\approx 0.34nm$) is reported as optimum in the literature to ignore the tunneling effect in this work. The tunneling conductance (G_t) happens due to flow of electron between two adjacent shells of MWCNT along its length and can be determined by

$$G_t = \sigma \pi D_g \tag{3.31}$$

where, σ and D_g are normalized tunneling conductivity at $0.34nm$ and diameter of any g^{th} for MWCNT, respectively. The impact of tunneling is ignored for this research work because separation between shells are considered as $0.34nm$, which is optimum [16].

B. Inductance of MMT nanostructure

The inductance (L_{sh}) of an individual shell of MWCNT can be obtained as

$$L_{sh} = L_m + L_{k/sh} * L_i \tag{3.32}$$

where, L_m and $L_{k/sh}$ are the magnetic and kinetic inductance of an individual shell of MWCNTs and can be calculated by

$$L_m = \frac{\mu}{2\pi} \cosh^{-1}\left(1 + \frac{2h_t}{D_g}\right) \tag{3.33}$$

$$L_{k/sh} = \frac{h}{2e^2} \frac{1}{\upsilon_f N_{ch/sh}} \tag{3.34}$$

where, h_t, μ and υ_f are the height from ground plane to the MWCNT placed above the ground, mobility of electrons and Fermi-velocity of electron ($8 \times *10^5 m/s$), respectively. $\cosh^{-1}()$ denotes the inverse hyperbolic cosine function [133].

Now, the inductance (L_{ESC}) of MMT nanostructure as VLSI interconnect and calculated by the sum of total kinetic inductance (L_{kESC}) and magnetic inductance (L_{mESC}). It can be obtained by the following equation

$$L_{ESC} = L_{mESC} + L_{kESC} \tag{3.35}$$

where, L_{kESC} and L_{mESC} are the kinetic inductance and magnetic inductance of all $MWCNT_L$ and $MWCNT_S$, which can be examined by the equations

$$L_{kESC} = (L_{kESC_L}^{-1} + L_{kESC_S}^{-1})^{-1} * L_i \tag{3.36}$$

$$L_{kESC_L} = \frac{h}{2e^2} \frac{1}{\upsilon_f N_{MWCNT_L} N_{ch}^{MWCNT_L}} \tag{3.37}$$

$$L_{kESC_S} = \frac{h}{2e^2} \frac{1}{\upsilon_f N_{MWCNT_S} N_{ch}^{MWCNT_S}} \tag{3.38}$$

$$L_{mESC} = (L_{mESC_L}^{-1} + L_{mESC_S}^{-1})^{-1} \tag{3.39}$$

$$L_{mESC_L} = \frac{\mu}{2\pi} \cosh^{-1}\left(1 + \frac{2h_t}{D_{g_L}}\right) \tag{3.40}$$

$$L_{mESC_S} = \frac{\mu}{2\pi} \cosh^{-1}\left(1 + \frac{2h_t}{D_{g_S}}\right) \tag{3.41}$$

The calculated magnetic inductance of the MMT (L_{mESC}) is negligible small as compared to kinetic inductance L_{kESC}, which can be neglected due to $L_{mESC} \ll L_{kESC}$.

C. Capacitance of MMT nanostructure

The MMT nanostrcuture has three types of capacitance such as electrostatic (C_e), shell-shell (C_s) and quantum (C_q) capacitance. C_q occurs due to the quantum energy stored in each shell of MWCNTs at the time of current flows through it. C_s happens between two adjacent shells of MWCNT, when each shell has different potential. C_e exists because of energy stored in outermost shell of MWCNT, which is placed above the ground plane at distance h_t. All the types of capacitance of individual MWCNTs can be calculated as

$$C_{q/sh} = \frac{2e^2}{h}\frac{2N_{ch/sh}}{\upsilon_f} \tag{3.42}$$

$$C_s = \frac{2\pi\varepsilon}{\ln\left(\frac{D_{g+1}}{D_g}\right)} \tag{3.43}$$

$$C_e = \frac{2\pi\varepsilon}{\cosh^{-1}\left(1+\frac{h_t}{D_{min}}\right)} \tag{3.44}$$

where, D_g, D_{g+1} and ε are the inner diameter, outer diameter of adjacent shells of MWCNT and permittivity.

The capacitance of MMT (C_{ESC}) examined using all the capacitance of $MWCNT_L$ (C_{ESC_L}) and $MWCNT_S$ (C_{ESC_S}) given by the following equation

$$C_{ESC} = (C_{ESC_L}N_{X_L} + C_{ESC_S}N_{X_S}) * L_i \tag{3.45}$$

where, C_{ESC_L} is the capacitance of $MWCNT_L$ for MMT nanostructure calculated by combining quantum (C_{q_L}), electrostatic (C_{e_L}) and shell-shell (C_{S_L}) capacitance of individual shells of $MWCNT_L$ as shown in Figure 3.5.

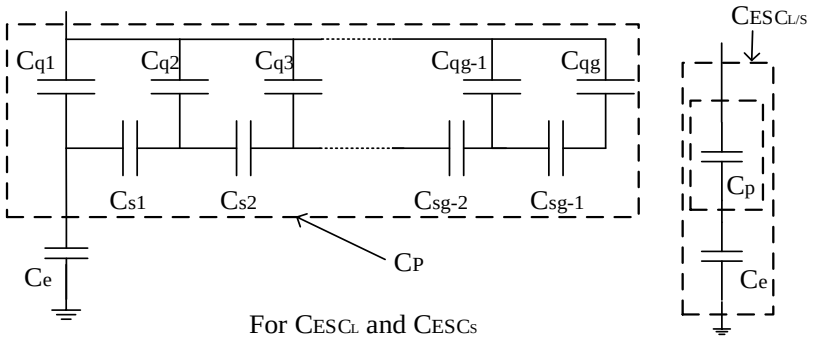


Figure 3.5: Capacitance equivalent circuit of individual MWCNT. [138]

Similarly, C_{ESC_S} is the capacitance of $MWCNT_S$ for MMT nanostructure calculated by combining quantum (C_{q_S}), electrostatic (C_{e_S}) and shell-shell (C_{S_S}) capacitance of individual shells of $MWCNT_S$. All the above mentioned capacitance can be calculated by the following equations

$$C_{ESC_L} = (\underbrace{[(C_{q(g_L)}^{-1} + C_{s(g_L-1)}^{-1})^{-1} + C_{q(g_L-1)}]}_{C_{P_L}}^{-1} + C_{e_L}^{-1})^{-1} \tag{3.46}$$

$$C_{ESC_S} = (\underbrace{[(C_{q(g_S)}^{-1} + C_{s(g_S-1)}^{-1})^{-1} + C_{q(g_S-1)}]}_{C_{P_S}}^{-1} + C_{e_S}^{-1})^{-1} \tag{3.47}$$

$$C_{q(g_L)} = \frac{2e^2}{h}\frac{2N_{ch/sh_L}}{\upsilon_f} \tag{3.48}$$

$$C_{e_L} = \frac{2\pi\varepsilon}{\cosh^{-1}\left(1 + \frac{h_t}{D_{min_L}}\right)} \tag{3.49}$$

$$C_{s(g_L)} = \frac{2\pi\varepsilon}{\ln\left(\frac{D_{g_L+1}}{D_{g_L}}\right)} \tag{3.50}$$

$$C_{q(g_S)} = \frac{2e^2}{h}\frac{2N_{ch/sh_S}}{\upsilon_f} \tag{3.51}$$

$$C_{e_S} = \frac{2\pi\varepsilon}{\cosh^{-1}\left(1 + \frac{h_t}{D_{min_S}}\right)} \tag{3.52}$$

$$C_{s(g_S)} = \frac{2\pi\varepsilon}{\ln\left(\frac{D_{g_S+1}}{D_{g_S}}\right)} \tag{3.53}$$

where, $D_{g_L}(D_{g_S})$ and $D_{g_L+1}(D_{g_S+1})$ are inner- and outer-most diameters of adjacent shells of $MWCNT_L$ ($MWCNT_S$), respectively [138].

3.2.4 Electrical ESC model of MMT as interconnect

The parasitic such as inductance, resistance and capacitance are examined through the Multi-Conductor Transmission Line (MCTL) model of MMT nanostructure as an interconnect. This model is proposed for individual shells of all $MWCNT_L$ and $MWCNT_S$ as shown in Figure 3.6. All the shells are taken parallel and assumed all shells participate in conduction. The MCTL model indicates the multi-conductor transmission line for each shell of individual $MWCNT_L$ and $MWCNT_S$.

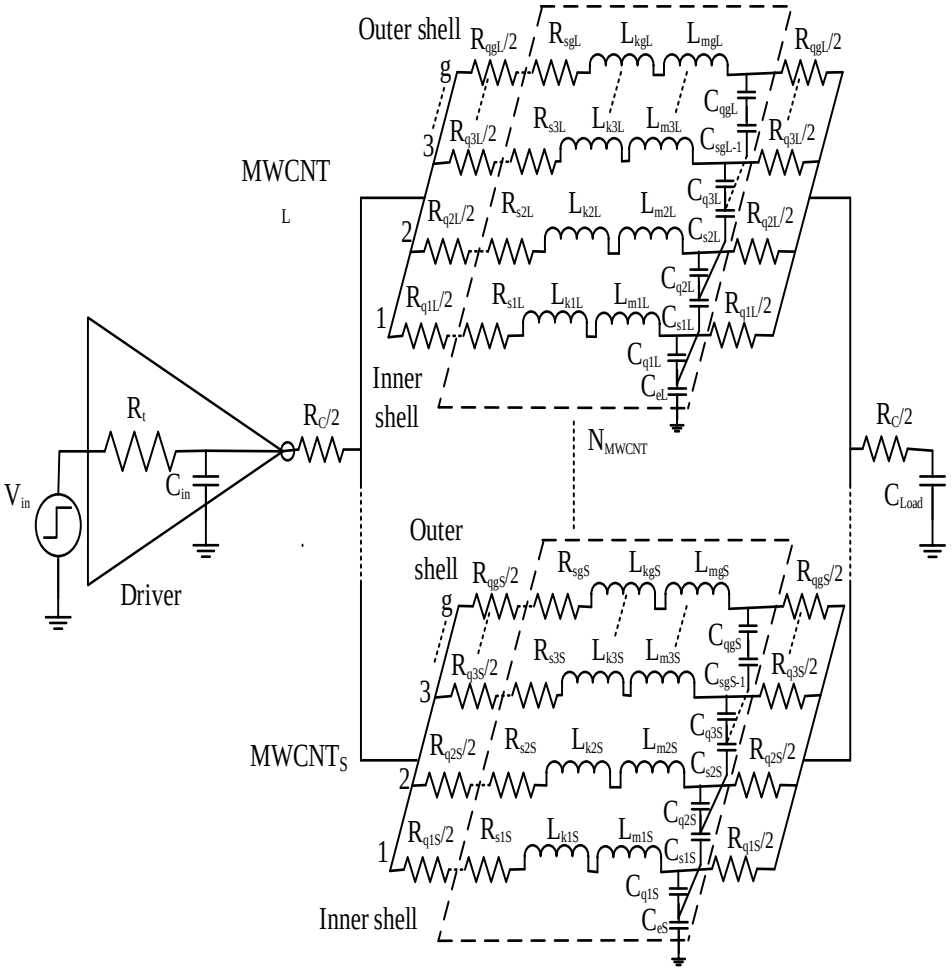


Figure 3.6: MCTL model for $MWCNT_L$ and $MWCNT_S$ of MMT interconnect.

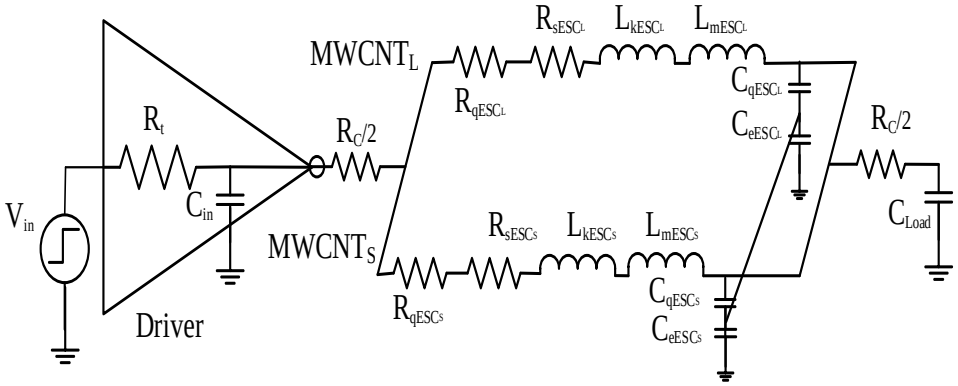


Figure 3.7: EEMC model of MMT interconnect.

Further, the MCTL model is considered to develop electrical equivalent multi-conductor (EEMC) model of MMT nanostructure for $MWCNT_L$ and $MWCNT_S$ as shown in Figure 3.7. The EEMC model is developed by combining the multi-conductor model of all individual $MWCNT_L$ ($MWCNT_S$) into a single-conductor parasitic such as R_{qESC_L} (R_{qESC_S}), R_{sESC_L} (R_{sESC_S}), L_{kESC_L} (L_{kESC_S}), L_{mESC_L} (L_{mESC_S}), C_{qESC_L} (C_{qESC_S}) and C_{eESC_L} (C_{eESC_S}) as presented in Figure 3.7.

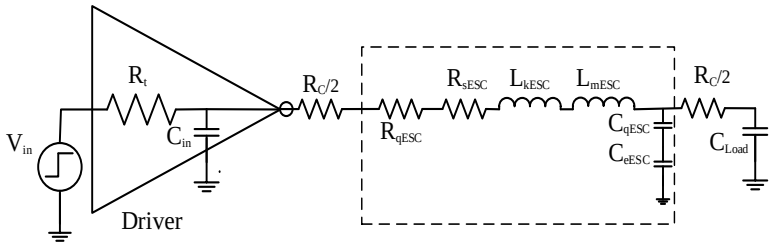


Figure 3.8: EESC model of MMT interconnect.

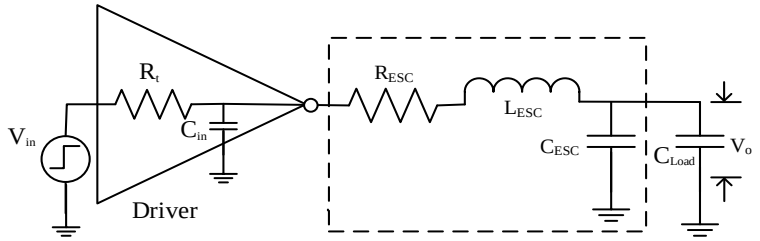


Figure 3.9: ESC model of MMT interconnect.

The EEMC model is represented into a simplified electrical equivalent single-conductor (EESC) model of MMT nanostructure as shown in Figure 3.8, where single-conductor parasitic of all $MWCNT_L$ and $MWCNT_S$ converted into a parasitic of EESC model as R_{qESC}, R_{sESC}, L_{kESC}, L_{mESC}, C_{qESC} and C_{eESC}. The EESC model is further be simplified into ESC model, which have a single-conductor parasitic values of MMT nanostructure (as R_{ESC}, L_{ESC} and C_{ESC}) shown in Figure 3.9. The ESC model is developed by using the Eq. 3.22, Eq. 3.35 and Eq. 3.45 for ESC resistance (R_{ESC}), inductance (L_{ESC}) and capacitance (C_{ESC}), respectively.

3.3 Impedance parameters of Cu interconnect

In this section, parasitic of Cu interconnect is calculated to develop an ESC model. The dimensions of Cu interconnect are height (H), width (W) and length (L_i) as shown in Figure 3.10.

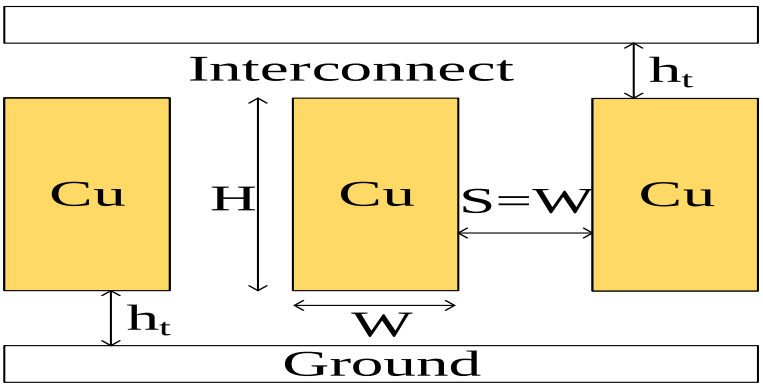


Figure 3.10: Cu structure of an interconnect. [154]

Table 3.1: Parameters of interconnects as per ITRS-2013. [153]

Interconnect Parameters	Technology Node		
	32nm	22nm	16nm
Width (W) in nm	40	28	18
Height (H) in nm	120	84	54
Oxide thickness t_{ox} (nm)	93.6	65.5	40
Aspect Ratio (A/R)	3	3	3
Dielectric constant (ε)	2.77	2.59	2.31
Resistivity of Cu (ρ_0) ($\mu\Omega - cm$)	3.66	4.2	5.69

The separation between two neighbour interconnect same as their width ($S = W$) and the distance from ground plane to outermost shell of MWCNT is denoted as h_t. The interconnect parameters are considered according to ITRS-2013 and shown in Table 3.1 [153, 154]. By using these parameters developed, the ESC model for Cu interconnect for various interconnect lengths at DSM technology nodes. This model is used to evaluate the performance in terms of delay, power and PDP at technology nodes viz. 32, 22 and 16nm.

3.3.1 Resistance of Cu interconnects

The resistance of Cu (R_{cu}) depends on cross-section dimensions of interconnect and its resistivity. The resistance of Cu can be calculated by following equation [131]

$$R_{cu} = \rho_0 \frac{L_i}{WH} \tag{3.54}$$

where, W, L_i, H and ρ_0 are width, length, height of Cu interconnect and the technology-dependent resistivity of Cu material.

3.3.2 Inductance of Cu interconnects

The inductance (L_{cu}) of Cu interconnect can be calculated as [131]

$$L_{cu} = \frac{\mu_0 L_i}{2\pi} \left[ln\left(\frac{2L_i}{W+H}\right) + \frac{1}{2} + \frac{0.22(W+H)}{L_i} \right] \tag{3.55}$$

where, μ_0 is the permeability ($= 4\pi \times 10^{-7} Hm^{-1}$).

3.3.3 Capacitance of Cu interconnects

The capacitance (C_{cu}) of Cu interconnect occurs because of ground capacitance (C_g) and coupling capacitance (C_c). The ground capacitance (C_g) can be obtained, when interconnect placed over the ground and generated fringing flux. The coupling capacitance (C_c) exists due to coupling between nearby interconnects. C_{cu}, C_g and C_c can be determined by using the following equations [131, 153]

$$C_{cu} = 2(C_g + C_e) * L_i \tag{3.56}$$

$$C_g = \varepsilon \left[\frac{W}{h_t} + 2.22 \left(\frac{S}{S + 0.7h_t} \right)^{3.19} + 1.17 \left(\frac{S}{S + 1.51h_t} \right)^{0.76} \left(\frac{H}{H + 4.53h_t} \right)^{0.12} \right] \tag{3.57}$$

$$\begin{aligned} C_c = {} & \varepsilon \left[1.14 \left(\frac{H}{S} \right) \left(\frac{h_t}{h_t + 2.06S} \right)^{0.09} + 0.74 \left(\frac{W}{W + 1.59S} \right)^{1.14} \right] \\ & + \varepsilon \left[1.17 \left(\frac{W}{W + 1.87S} \right)^{0.16} \left(\frac{h_t}{h_t + 9.8S} \right)^{1.18} \right] \end{aligned} \tag{3.58}$$

where, h_t, S and ε are height of interconnect from ground plane, separation between two adjacent interconnect and dielectric constant, respectively.

3.4 Performance analysis of proposed MMT nanostructure and Cu as VLSI interconnects

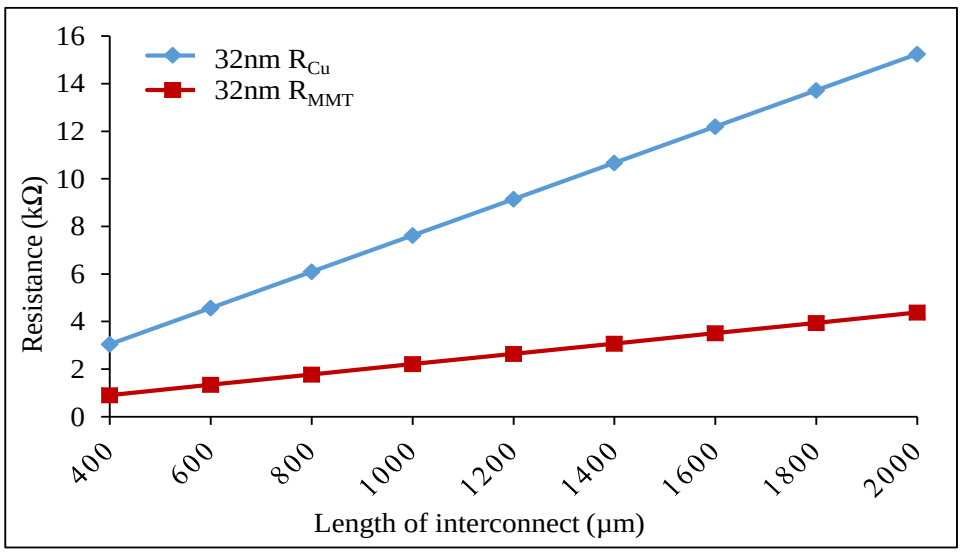
The ESC models of proposed MMT and Cu interconnect are calculated with the help of MATLAB tool and cross-sectional dimensions for various VLSI interconnect at DSM technology nodes are considered according to ITRS-2013 as shown in Table 3.1. Further, the MMT and Cu models are used to evaluate the performance in terms of resistance, delay, power and PDP at DSM technology nodes (32, 22 and 16nm) for a variable interconnect length ranging from 400 to 2000µm. The resistance of MMT nanostructure as VLSI interconnects are calculated using Eqs. 3.22 to 3.28 and the ESC model (as shown in Figure 3.9) is developed by assuming all shells of MMT nanostructure to be parallel and each shell participates in conduction. The number of MWCNTs ($MWCNT_L$ and $MWCNT_S$) and total number of conducting channels of MMT nanostructure determined by using the Eqs. 3.1 to 3.17. The inductance and capacitance of MMT interconnect are calculated by equations from Eqs. 3.32 to 3.53. The resistance, inductance and capacitance of Cu interconnect are determined using Eq. 3.54, Eq. 3.55 and

Eqs. 3.56 to 3.58, respectively. The resistance of MMT and Cu nanostructure are calculated for various interconnect lengths from 400 to 2000μm at DSM technology nodes viz. 32, 22 and 16nm as shown in Table 3.2.

Table 3.2: Resistance of Cu and MMT interconnect in kΩ.

		Interconnect length (μm)								
Technology	Materials	400	600	800	1000	1200	1400	1600	1800	2000
32nm	R_{Cu}	3.1	4.6	6.1	7.6	9.2	10.7	12.2	13.7	15.3
	R_{MMT}	0.9	1.3	1.8	2.2	2.6	3.1	3.5	3.9	4.4
22nm	R_{Cu}	7.1	10.7	14.3	17.9	21.4	25.0	28.6	32.1	35.7
	R_{MMT}	1.8	2.7	3.6	4.5	5.4	6.3	7.2	8.1	8.9
16nm	R_{Cu}	23.4	35.1	46.8	58.5	70.3	82.0	93.7	105.4	117.1
	R_{MMT}	4.5	6.6	8.7	10.9	13.0	15.2	17.3	19.5	21.6

The comparison of resistance of the MMT and Cu for interconnect lengths for 400 to 2000μm at DSM technology nodes viz. 32, 22 and 16nm are shown in Figure 3.11(a)-(c), respectively. It shows that the resistance of the MMT nanostructure is smaller than Cu for various VLSI interconnect lengths at all the three DSM technology nodes. It reveals from the comparative analysis, the resistance of MMT and Cu interconnects are increased with rising length from 400 to 2000μm. Figure 3.11 (d), presented the Comparison of resistance for MMT and Cu on a variable interconnect length ranging from 400 to 2000μm at DSM technology nodes at room temperature.



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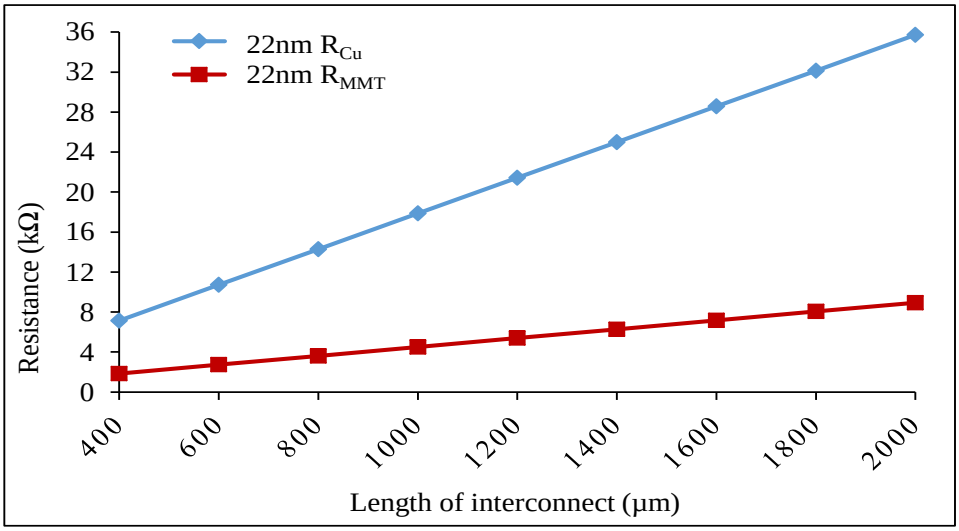

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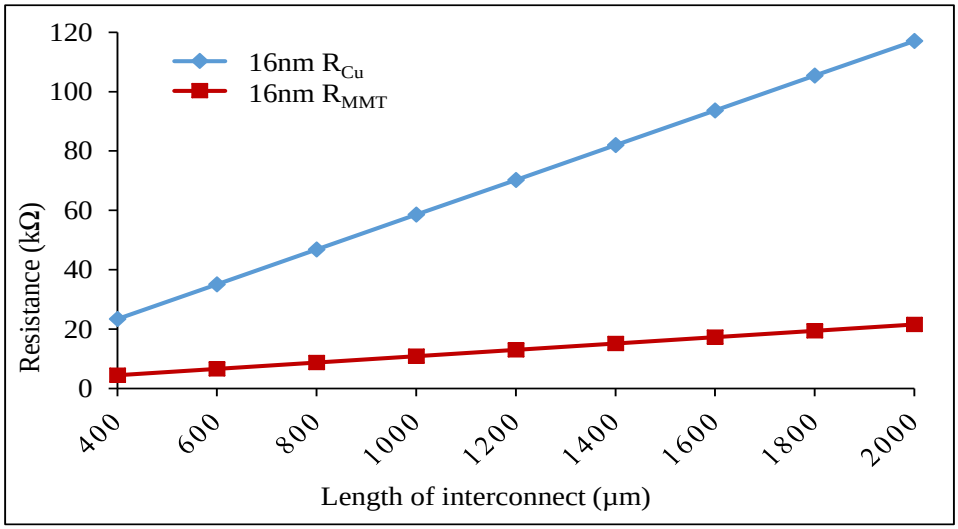

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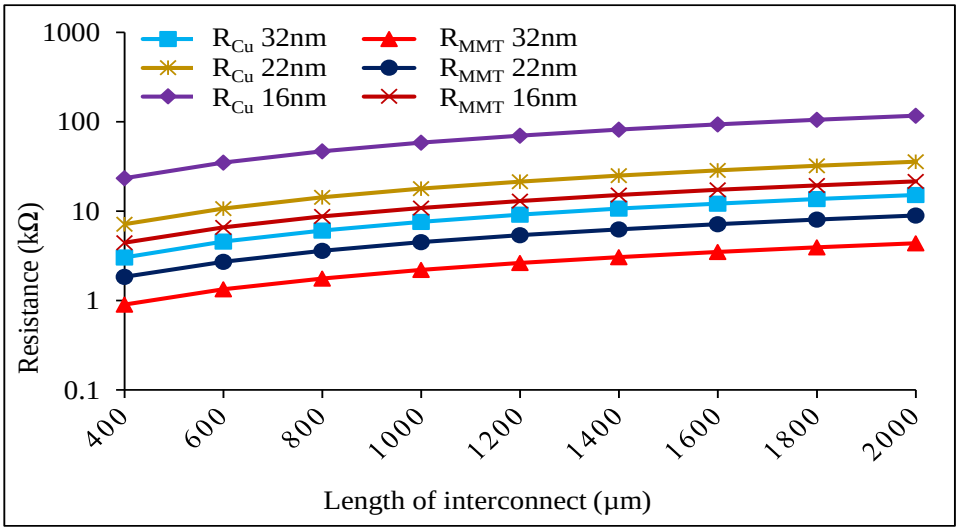


(d)

Figure 3.11: Resistance of MMT and Cu interconnect at (a) 32, (b) 22 and (c) 16nm technology nodes. (d)comparison of resistance for MMT and Cu interconnect on logarithmic scale.

Further, the approximated reduction in resistance of Cu to MMT observed for interconnect as 71%, 75% and 81% at 32, 22 and 16nm technology nodes, respectively. It is revealed that the approximated reduction in resistance of Cu to MMT nanostructure is improved from 71% to 81% for scale-down technology node from 32 to 16nm. It concludes that the MMT nanostructure can be used for interconnect because it has less resistance than Cu interconnects at DSM technology nodes.

3.5 Performance analysis of MMT and Cu interconnect

Further, parasitic of MMT and Cu interconnect are simulated using Tanner tool to estimate the performance in terms of delay, power and PDP at various DSM technology nodes. The simulated setup has number of CMOS driver to drive the load, which have need to achieve minimum delay and less power consumption at various DSM technology nodes. The parasitic of CMOS is minimized at DSM technology nodes and parasitic of interconnect is dominating part in overall delay of IC [155]. The simulation setup requires optimum-sized and optimum number of repeaters to minimize power consumption and delay of line. The number of repeaters (R_{opm}=8) and optimum-sized repeater (A/R=30) are evaluated by observing the minimum delay and less power consumption in the interconnect line [97]. Figure 3.12, shows the simulation setup, the interconnect consists of resistance, inductance and capacitance, that provides the path between the input signal (V_o) and output across load capacitance (C_L) through the driver having internal resistance (R_t) and input capacitance (C_{in}).

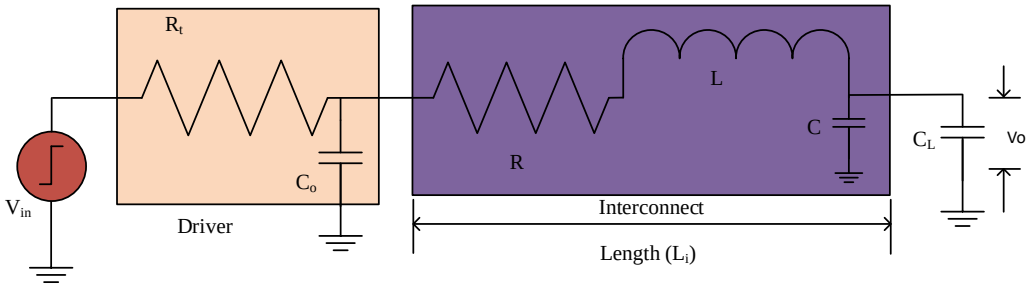


Figure 3.12: Single stage of simulation setup used for MMT interconnect. [119]

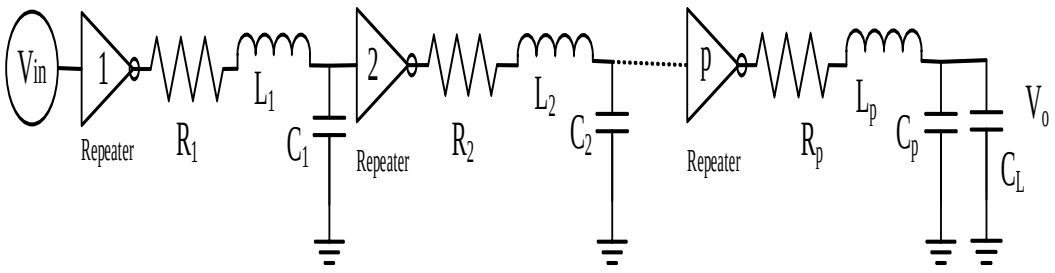


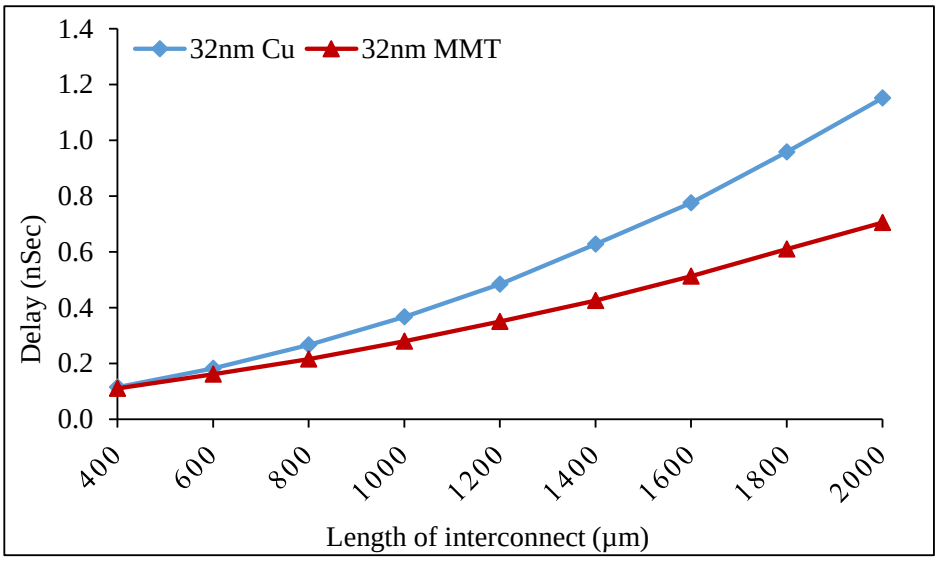
Figure 3.13: Simulation setup used for MMT interconnect of p-stages. [133]

The developed simulation setup of the MMT interconnect as distributed RLC model (for p-stages) at various DSM technology nodes as shown in Figure 3.13. The simulation parameters are considered to evaluate the performance of MMT nanostructure as VLSI interconnects as shown in Table 3.3 [111, 156, 157]. Similarly, the performance of Cu interconnect is also calculated with the same simulated setup in terms of delay, power and PDP. The obtained results are compared with MMT interconnect at DSM technology nodes viz. 32, 22 and 16nm.

Table 3.3: Simulation Parameters of interconnects.

Parameters	Technology Node		
	32nm	22nm	16nm
V_{dd} (volts)	0.9	0.8	0.7
C_L (fF)	0.1	0.1	0.1
No. of Repeaters (R_{opm})	8	8	8
Size of Repeater (A/R)	30	30	30
Model file (PTM)	54	54	54

The delay comparison of MMT and Cu is presented for a variable interconnect lengths from 400 to 2000µm as shown in Figure 3.14(a)-(c) for 32, 22 and 16nm technology nodes, respectively. The evaluated delay of MMT interconnects is smaller as compared to Cu for variable interconnect lengths at DSM technology nodes. The delay of MMT and Cu increases with raising interconnect lengths for all three DSM technology nodes.



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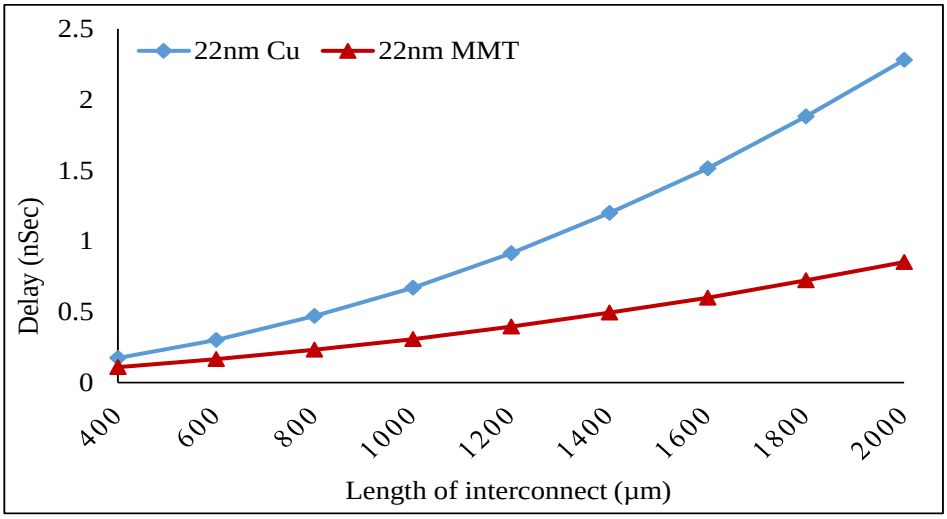

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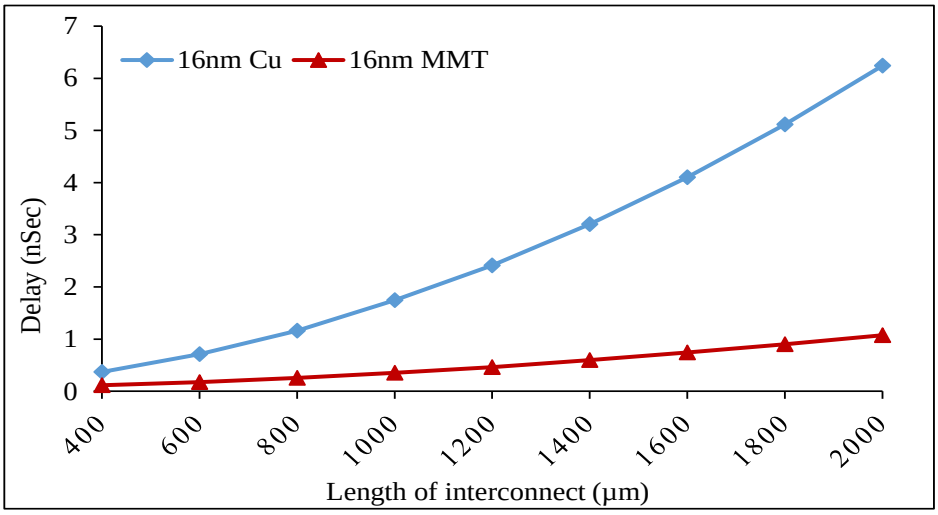

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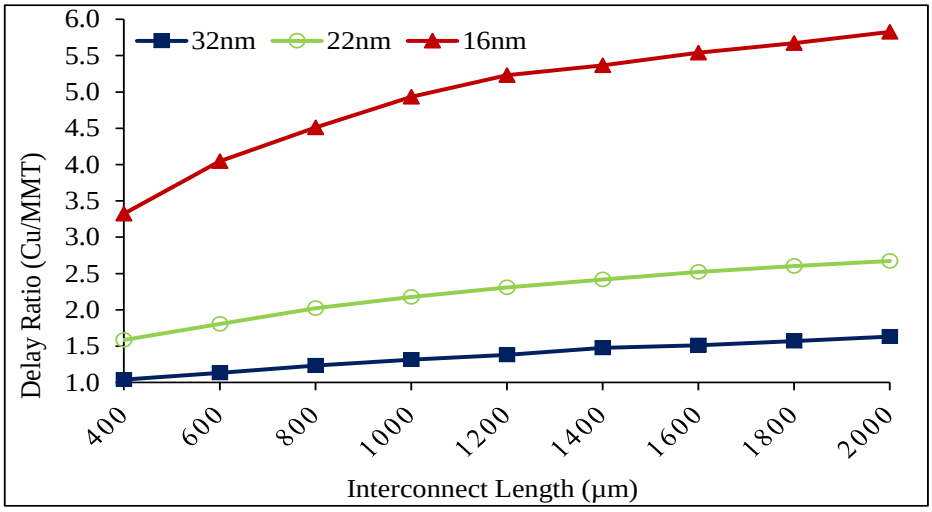


(d)

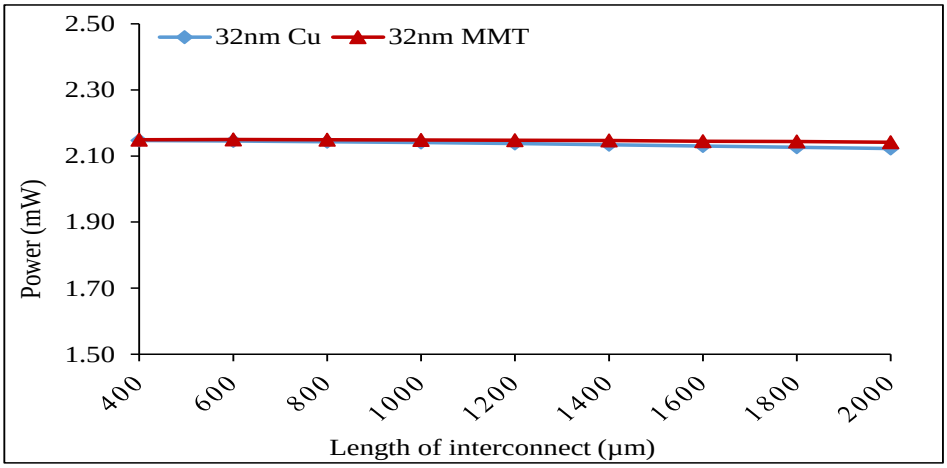
Figure 3.14: Delay of MMT and Cu interconnect at (a) 32, (b) 22 and (c) 16nm technologies. (d) Delay ratio (Cu/MMT) at 32, 22 and 16nm technology nodes.

The delay ratio (Cu/MMT) for interconnect length at DSM technology nodes viz. 32, 22 and 16nm is shown in Figure 3.14(d). It is observed that the delay ratio is greater than unity and increased for interconnect lengths at DSM technology nodes. It means that the delay of Cu interconnect is large than the MMT nanostructure. The delay ratio is increased for interconnect length from 400 to 2000μm at scaled-down technology nodes from 32 to 16nm. It reveals that the delay slop of Cu is higher than the MMT interconnect. It shows that the MMT can perform better than Cu for interconnect length beyond 400μm at DSM technology nodes.

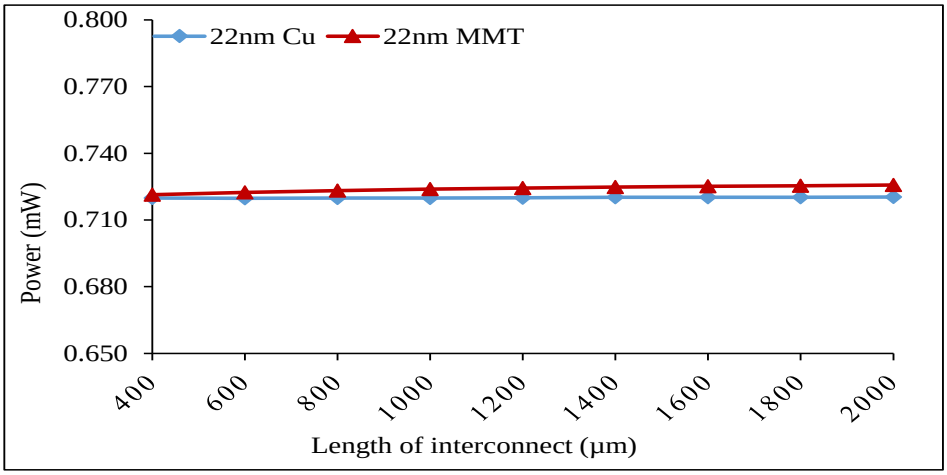
Further, the approximated delay reduction (Cu to MMT) in % for interconnect length 400 to 2000μm is calculated as 3.9 to 38.7%, 36.9 to 62.6% and 69.9 to 82.8% at 32, 22 and 16nm technology nodes, respectively. The % of delay reduction for decreasing technology nodes from 32 to 16nm is improved as 3.9 to 69.9% and 38.7 to 82.8% for interconnect length 400 and 2000μm, respectively. It reveals that the performance of MMT nanostructure in terms of delay reduction is improving with increased length as well as decreased technology nodes. It concludes that the MMT can be used as a future interconnect because it performs better than Cu at DSM technology nodes for high-performance VLSI-ICs design.

The power of MMT and Cu for different interconnect lengths at 32, 22 and 16nm technology nodes are shown in Figure 3.15(a), (b) and (c), respectively. The power of MMT interconnect is examined, which is more as compared to Cu interconnect at DSM technology nodes. The power dissipation of CNT interconnect depends on the capacitance, which is dominating factor as compared to other impedance parameters of the CNT interconnect. The capacitance of CNTs are large due to high tube capacitance as compared to copper as shown in literature. The capacitance of CNT bundle depends upon the number of shells of the bundle and the overall capacitance is the product of the number of shells of the bundle and capacitance of an individual shell. Therefore, overall capacitance of MMT nanostructure is also large at 32 and 22 nm technology nodes as compared to the copper. The capacitance of MMT is determined high due to large number of MWCNT bundles (as $MWCNT_L$ and $MWCNT_S$) as well as large number of shells, which increases the overall capacitance and cause to increase the power dissipation of MMT interconnect at 32, 22nm technology nodes as compared to copper for global interconnect length. The power is decreasing with increase in interconnect lengths at 32nm technology nodes; however, the trend is opposite in case of 22 and 16nm technology nodes for a variable interconnect lengths.

The ratio of power (Cu/MMT) at 32 and 22nm technology nodes are observed less than unity, however, it is examined greater than unity at 16nm technology nodes for different interconnect lengths between 400 and 2000μm in Figure 3.15(d). It illustrates that the power of MMT and Cu as VLSI interconnect is decreasing with scaled-down technology nodes from 32 to 16nm.



(a)



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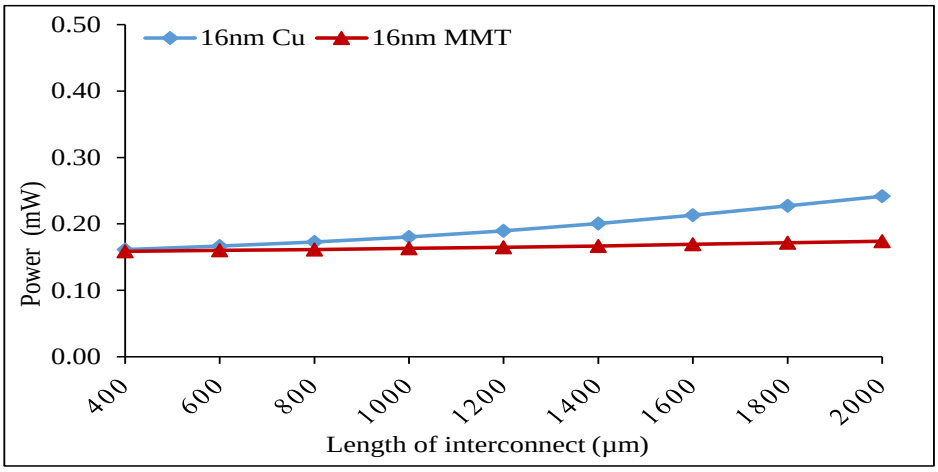

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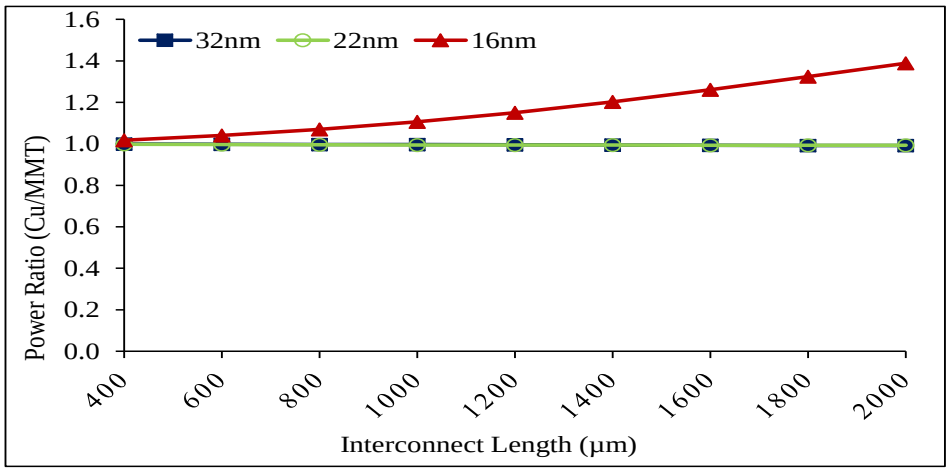
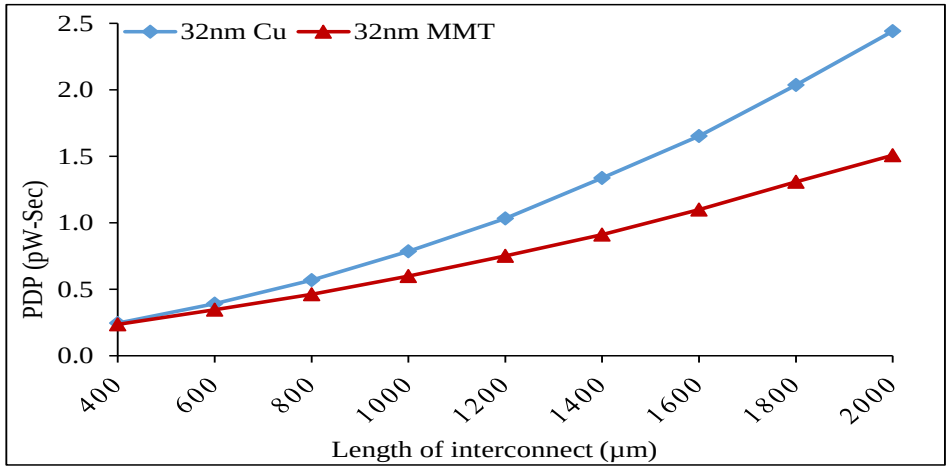


(d)

Figure 3.15: Power dissipation of MMT and Cu for variable interconnect length at DSM technology nodes as (a) 32, (b) 22 and (c) 16nm. (d) Power ratio of Cu/MMT at DSM technology nodes for various interconnect lengths.

The PDP of MMT and Cu is presented for interconnect lengths from 400 to 2000µm at DSM technology nodes viz. 32, 22 and 16nm as shown in Figure 3.16(a), (b) and (c), respectively.



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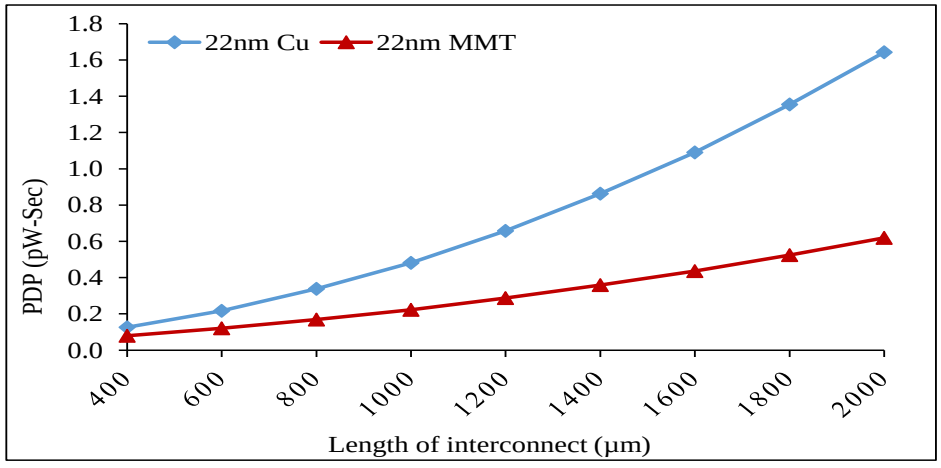

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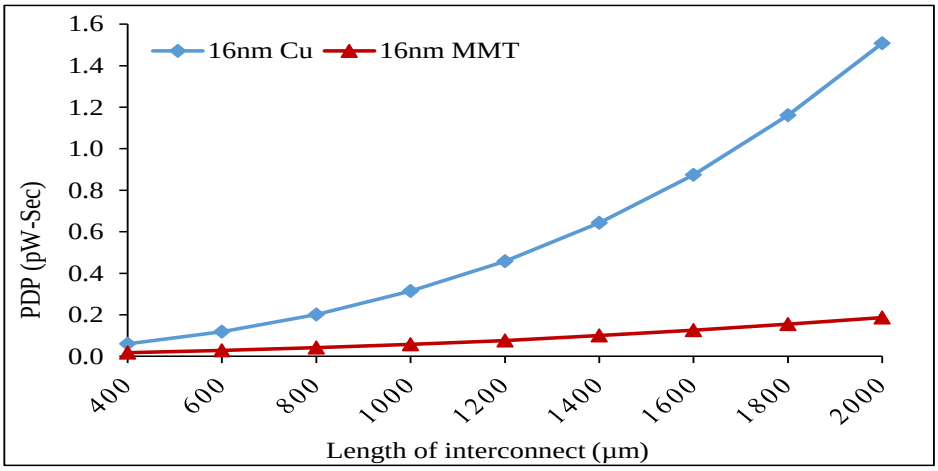

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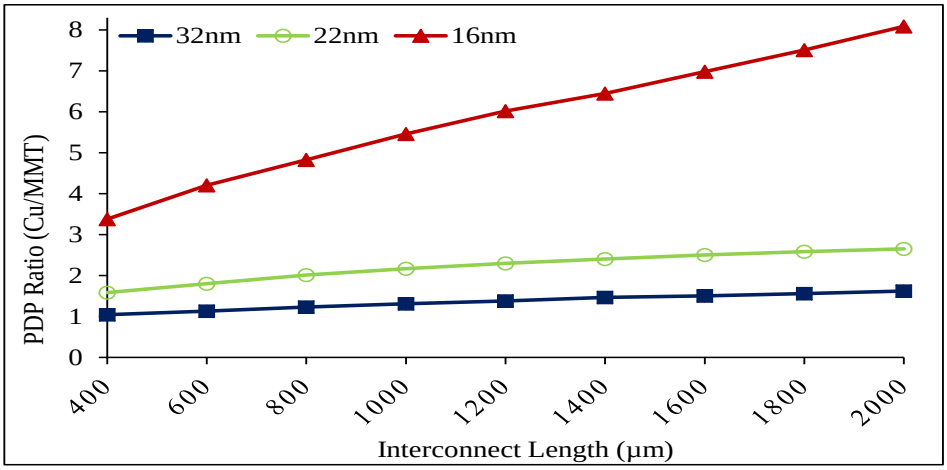

(d)

Figure 3.16: The PDP of MMT and Cu for different interconnect lengths at DSM technology nodes as (a) 32, (b) 22 and (c) 16nm. (d) The ratio of PDP (Cu/MMT) for VLSI interconnect lengths at DSM technology nodes.

PDP of MMT is evaluated less than Cu for different interconnect lengths and DSM technology nodes. PDP of both types of nanostructures (MMT and Cu) is increased with increasing interconnect length between 400 and 2000µm at 32, 22 and 16nm technology nodes.

The ratio of PDP (Cu/MMT) is calculated for various interconnect lengths as shown in Figure 3.16(d), which is always greater than unity at all three technology nodes. The MMT nanostructure shows better results for global than intermediate interconnect. The approximation reduction in PDP (%) for variable interconnect length is examined as 3.8 to 38.2%, 36.8 to 62.3% and 70.4 to 87.7% at 32, 22 and 16nm technology nodes, respectively. The PDP reduction (%) is also improving for scaled-down technology nodes from 32 to 16nm as 3.8 to 70.4% for 400µm and 38.2 to 82.7% for 2000µm interconnect length. It reveals that the performance

of MMT is better than Cu in terms of PDP for various interconnect lengths at DSM technology nodes. It is concluded that the MMT nanostructure can be used as a future of VLSI interconnect material at DSM technology nodes for variable interconnect lengths.

Chapter Summary

In this chapter, MMT nanostructure is proposed as VLSI interconnects for VLSI-IC design at DSM technology nodes. The MMT nanostructure is developed using two differently-sized MWCNTs are inserted into a bundle, that bundle is denser then MWCNTB. The proposed MMT nanostructure is different from available nanostructures in literature. MMT nanostructure considered as various VLSI interconnect lengths (400 to 2000μm) at DSM technology nodes (32, 22 and 16nm). The performance depends on the parasitic of VLSI interconnect such as capacitance, resistance and inductance. These parameters are calculated for all individual shells for the MWCNTs, which are considered to be parallel. Further, the ESC model is developed with the help of mathematical equations written in the MATLAB tool. The ESC model has considered to calculate the parasitic of MMT interconnect at 32, 22 and 16nm technology nodes for variable interconnect lengths ranging from 400 to 2000μm.

Similarly, the parasitic of Cu is also computed for the parameters under consideration for MMT interconnect at 32, 22 and 16nm technology nodes. Then, the study of comparative analysis of MMT and Cu interconnect is presented for various interconnect lengths at DSM technology nodes. It shows that the resistance of MMT observed less than Cu interconnect for the entire range of interconnect lengths at 32, 22 and 16nm technology nodes. The performance of MMT interconnect is calculated to compare with the performance of Cu interconnect for interconnect lengths (400 to 2000μm) at DSM technology nodes (32, 22 and 16nm). The improvement in delay reduction (%) for VLSI interconnect length from 400 to 2000μm is examined as 3.9 to 38.7%, 36.9 to 62.6% and 69.9 to 82.8% at 32, 22 and 16nm technology nodes, respectively. For decreasing technology nodes from 32 to 16nm, the improvement delay reduction (%) is also examined as 3.9 to 69.9% for 400μm and 38.7 to 82.8% for 2000μm interconnect length. The performance of MMT in terms of delay, power and PDP outperforms Cu for interconnect lengths at DSM technology nodes. The MMT nanostructure can be used as a future interconnect material at advanced technology nodes for VLSI-ICs design.

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Chapter 4

Temperature Dependent Performance analysis of MMT

This chapter presents the impact of temperature on the performance of proposed Mixed-MWCNT (MMT) nanostructure as VLSI interconnects in terms of delay, power and PDP at various DSM technology nodes. The temperature-dependent mathematical equations are proposed to derive temperature-dependent ESC model of MMT nanostructure as VLSI interconnect at DSM technology nodes for a variable temperature range. The impedance parameters of the proposed nanostructure influenced by rising temperature from moderate to high (300 to 450K). By using the developed ESC models, the performance of MMT interconnect is evaluated with SPICE simulation tool in terms of delay, power and PDP at DSM technology nodes viz. 32, 22 and 16nm. The obtained performance parameters of MMT is analyzed and compared at different DSM technology nodes for a variable temperature ranging from 200 to 450K. Further, the temperature-dependent performance of MMT is compared with the similar analysis of Cu as global interconnect at DSM technology nodes. The temperature-dependent ESC model has been developed to calculate the parasitic of Cu interconnect for global length at DSM technology nodes. The obtained parasitic of Cu interconnect are simulated and results are compared with MMT nanostructure as VLSI interconnect.

4.1 Introduction

VLSI interconnects require fast switching and less power consumption at DSM technology nodes. Conventional Cu is used as VLSI interconnects and have some severe problems at DSM technology nodes (especially below 45nm technology nodes) [145, 157]. Cu has a small electron MFP and low current density, which increase the impact of scattering phenomena and electro-migration at DSM technology nodes [149]. The grain boundary and surface scattering phenomena occur because the cross-sectional dimensions of VLSI interconnect scaled-down at DSM technology nodes [131, 133, 158]. These parameters have influenced the performance of global level interconnect and reduced the overall speed of operation. Therefore, the impact

of variable temperatures needs to include for understanding the actual performance of interconnect in thermally-aware environmental conditions at DSM technology nodes. Temperature-dependent impedance models for SWCNTB and MWCNTB have already been published in the available literature [97, 121, 124–127].

In this chapter, temperature-dependent ESC model of the MMT interconnect is presented and it is used to evaluate the impedance parameters in terms of resistance, capacitance and inductance. This model is presented for semi-global and global level interconnect length at 32, 22 and 16nm technology nodes for high-performance VLSI-IC design. This model is used to examine the performance of a variable temperature range (200 to 450K) for global level VLSI interconnect. The thermal variations influenced the impedance parameters of VLSI interconnects at DSM technology nodes.

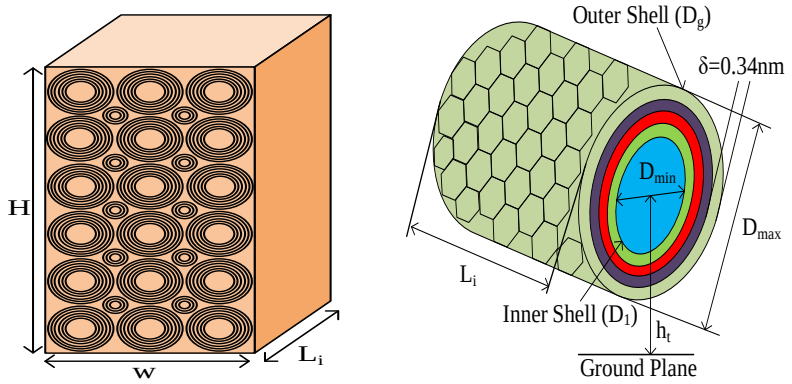
The parasitic of the MMT interconnect calculated under various thermally-aware factors under variable temperatures at DSM technology nodes as 32, 22 and 16nm. Thermally-aware factors are grain boundary and surface scattering in MMT nanostructure at DSM technology nodes. The MMT interconnect consists of two types of scattering – electron-phonon and electron-electron scattering. The electron-phonon and electron-electron scattering show a significant impact on their parasitic of CNTs. The temperature-dependent scattering phenomena decreases the electron MFP and increases the resistance of MMT nanostructure because electron MFP is inversely propositional to resistance [114, 121, 122, 159].

The thermally-aware parasitic of MMT is determined by mathematical expressions driven with the help of MATLAB tool for global interconnect (1000µm) at DSM technology nodes on variable temperature range between 200 and 450K. The calculated temperature-dependent resistance of MMT is analysed and compared to temperature-independent resistance at 32, 22 and 16nm technology nodes. The temperature-dependent parasitic is considered to evaluate the temperature-dependent performance of MMT in terms of delay, power and PDP at DSM technology nodes viz. 32, 22 and 16nm.

4.2 Temperature-dependent ESC model of MMT

The MMT nanostructure as VLSI interconnect consists of two differently-sized MWCNTs such as $MWCNT_L$ (large diameter MWCNT) and $MWCNT_S$ (small diameter MWCNT) as shown

in Figure 4.1(a). These look-alike, but their physical dimensions and electrical properties are dissimilar because $MWCNT_L$ and $MWCNT_S$ have different inner- and outer-most diameters. Accordingly, the number of shells are also different for $MWCNT_L$ and $MWCNT_S$. The $MWCNT_L$ has a higher number of shells as compared to $MWCNT_S$ because $MWCNT_L$ has large outer diameters. The diameters of inner- and outer-most shells of MWCNTs are denoted as D_{min} and D_{max}, respectively.



(a) (b)

Figure 4.1: (a)Proposed MMT nanostructure as VLSI interconnect. (b) Cross-sectional view of MWCNT on the ground plane. [16]

The distance of ground plane to the outer MWCNT defines as h_t in Figure 4.1(b). The separation between concentric shells of MWCNT and adjacent MWCNTs is called Van Der Waals gap. It can be considered ranging from 0.30 to 0.40nm for inter-shell spacing and adjacent MWCNT bundles as shown in literature. The optimum inter-shell spacing and adjacent bundles spacing are considered as 0.34nm for this thesis work. The decrease in the separation between the shells will increase the inter-shell capacitance and introduce the tunnelling impact which increase the power dissipation and crosstalk impact for VLSI interconnect. However, large spacing between shells increases the resistance of interconnect as the number of shells will decrease, which increase the propagation delay of MMT as VLSI interconnect. To get the optimum overall performance of MMT interconnect, the optimum spacing is considered as 0.34nm for the adjacent shells and the adjacent MWCNT bundles. The tunnelling impact is also negligible at this spacing. [16].

4.2.1 Temperature-dependent conducting channels and parasitic of MMT

The number of MWCNTs (N_{MMT}), number of shells (N_{sh}) and diameter of each shell (D_g) for individual MWCNTs are given by Eqs. 3.1 to 3.11 mentioned in Chapter 3. Further, total number of conducting channels (N_{total}^{MMT}) in a MMT nanostructure as VLSI interconnect are

calculated using Eqs. 3.15 to 3.17 as per Chapter 3. Temperature-dependent conducting channels ($N_{ch/sh}^{T_K}$) for $MWCNT_L$ and $MWCNT_S$ can be calculated using the following equations

$$N_{ch/sh_L}^{T_K} \approx aD_{g_L}T_K + b, for > 3nm \tag{4.1}$$

$$N_{ch/sh_S}^{T_K} \approx aD_{g_S}T_K + b, for > 3nm \tag{4.2}$$

where, $a = 6.12 \times 10^{-4}/nmK, b = 1.275$. T_K is a variable temperature ranging from 200 to 450K and D_g is diameter of any g^{th} shell of MWCNT [127].

The MMT nanostructure has two differently-sized MWCNTs such as $MWCNT_L$ and $MWCNT_S$ having different number of shells for both MWCNTs. The performance of the VLSI interconnect depends on the parasitic such as capacitance, resistance and inductance. All shells of individual MWCNTs are assumed to be parallel and considered to develop an equivalent multiconductor transmission line (MCTL) model.

4.2.2 Temperature-dependent Resistance of the MMT nanostructure

The resistance of an individual shell (R_{sh}) consists of quantum resistance (R_q), contact resistance (R_c) and scattering resistance (R_s). R_c occurs because of imperfect contact between shells and metal that considered as $2k\Omega$ for this work. R_q arises due to quantum confinement of electrons in a nanowire and can be calculated according to Eq. 3.19 in Chapter 3. The scattering resistance (R_s) depends on length (L_i) of MWCNT shell, when it is large than the MFP of CNT, due to this the scattering phenomena occurs as electron-phonon and electron-electron scattering. The electron-electron scattering has a negligible impact, but electron-phonon plays an significant role in scattering phenomena. The temperature-dependent scattering resistance of an individual shell is calculated by the following equation [121, 133, 145, 157]

$$R_s = \frac{h}{2e^2}\frac{1}{N_{ch/sh}^{T_K}\lambda_{eff}^{T_K}} \tag{4.3}$$

where, $\lambda_{eff}^{T_K}$ is MFP of individual shell of MWCNT.

Further, temperature-dependent resistance (R_{ESC}) of the MMT interconnect consists of contact resistance (R_c), scattering resistance (R_{sESC}) and quantum resistance (R_{qESC}). Temperature-dependent scattering resistance (R_{sESC}) can be calculated by using number of conducting chan-

nels per individual shell of MWCNTs. The resistance of MMT (R_{ESC}) can be calculated by following equations

$$R_{ESC} = R_c + R_{qESC} + R_{sESC} * L_i \tag{4.4}$$

where, quantum resistance (R_{qESC}) and scattering resistance (R_{sESC}) of MMT interconnect can be calculated as

$$R_{qESC} = \left[\left(\frac{h}{2e^2} \frac{1}{N_{MWCNT_L} N_{ch}^{MWCNT_L}} \right)^{-1} + \left(\frac{h}{2e^2} \frac{1}{N_{MWCNT_L} N_{ch}^{MWCNT_S}} \right)^{-1} \right]^{-1} \tag{4.5}$$

$$R_{sESC} = \left[(R_{sESC_L})^{-1} + (R_{sESC_S})^{-1} \right]^{-1} \tag{4.6}$$

$$R_{sESC_L} = \frac{h}{2e^2} \frac{1}{N_{MWCNT_L} \sum_{g=1}^{N_{sh_L}} N_{ch/sh_L}^{T_K} \lambda_{eff}^{T_K}} \tag{4.7}$$

$$R_{sESC_S} = \frac{h}{2e^2} \frac{1}{N_{MWCNT_S} \sum_{g=1}^{N_{sh_S}} N_{ch/sh_S}^{T_K} \lambda_{eff}^{T_K}} \tag{4.8}$$

The effective MFP ($\lambda_{eff}^{T_K}$) are calculated by the expression explain in the next subsection.

4.2.3 Effective MFP of an MMT nanostructure

The scattering resistance (R_{sESC}) is influenced by temperature-dependent effective MFP ($\lambda_{eff}^{T_K}$), which decreases with increase in temperature ranging from 200 to 450K. It affects the performance in terms of power and delay for MMT nanostructure at DSM technology nodes viz.32, 22 and 16nm. Temperature-dependent scattering phenomena depends on two type of scattering namely - electron-phonon and electron-electron scattering. The electron-electron scattering has negligible impact, however electron-phonon scattering has main dominating part of scattering phenomena to effective MFP of MMT nanostructure. The temperature-dependent effective MFP ($\lambda_{eff}^{T_K}$) happens due to acoustic and optical-zone boundary scattering phenomena in metallic shell of CNT [121–124]. It can be determined by following equation

$$\lambda_{eff}^{T_K} = (\lambda_{ac}^{-1} + \lambda_{ozb}^{-1})^{-1} \tag{4.9}$$

where, the λ_{ac} and λ_{ozb} are acoustic MFP and optical-zone boundary MFP, respectively. The λ_{ac} occurs because acoustic scattering phenomena in MMT nanostructure. For temperature less than 300K, λ_{ac} plays a important role to influence effective MFP. The resistance of MMT

nanostructure is directly depending on λ_{ac}, which increases with decrease in λ_{ac}. The λ_{ac} is reduced with rise in temperature and effective MFP is also decreased. The λ_{ac} depends on diameter (D_g) of any g^{th} shell and variable temperature (T_K) as calculated by the following equation

$$\lambda_{ac} = 266667\frac{D_g}{T_K} \tag{4.10}$$

For temperature more than 300K, the λ_{ozb} plays a essential role to influence effective MFP of MMT nanostructure. It occurs due to optical-zone boundary scattering such as electron-phonon emission and absorption. In case of high bias conditions, electrons get accelerated due to generated electric field along CNT and increase their kinetic energy [123]. When electron energy reaches optical phonon energy level, a phonon will be emitted with energy $h\omega$ ($\approx$0.16eV for zone-boundary phonon and $\approx$0.2eV for optical phonon). The optical or zone boundary scattering can take place when and electron acquires required energy by absorbing another optical or zone boundary phonon. The λ_{ozb} can be calculated by the following equation

$$\lambda_{ozb} = [(\lambda_{ozb}^{fld})^{-1} + (\lambda_{ozb}^{abs})^{-1}]^{-1} \tag{4.11}$$

where, λ_{ozb}^{fld} is based on electric-field acceleration scattering and can be examined by the following equation

$$\lambda_{ozb}^{fld} = \frac{(hw - k_B T_K)}{eV} L_i + \frac{\lambda_{ozb300} D_g}{D_0} \frac{N_{ozb}^{300} + 1}{N_{ozb}^{T_K} + 1} \tag{4.12}$$

k_B and T_K are Boltzmann's constant and variable temperature, respectively. First term represents the distance travels by electron to achieve phonon emission threshold energy. Second term correspond to the distance travels by electron after getting energy and before releasing a phonon. The spontaneous effective emission length is measured as $\lambda_{ozb300} \approx 15nm$ for diameter (D_0) at 300K. MWCNTs of large diameters have their sub-bands extended to Fermi level that plays important role for its conductance by creating the conducting channels for the flow of electron.

λ_{ozb}^{abs} is scattering due to absorption of optical or zone boundary phonon and can be calculated by the following equation

$$\lambda_{ozb}^{abs} = \frac{\lambda_{ozb300} D_g}{D_0} \frac{N_{ozb}^{300} + 1}{N_{ozb}^{T_K}} \tag{4.13}$$

where, the occupied states of optical-zone boundary phonon (N_{ozb}) are known as density of states for final electron state after scattering of an phonon, which can be given below [124–127]

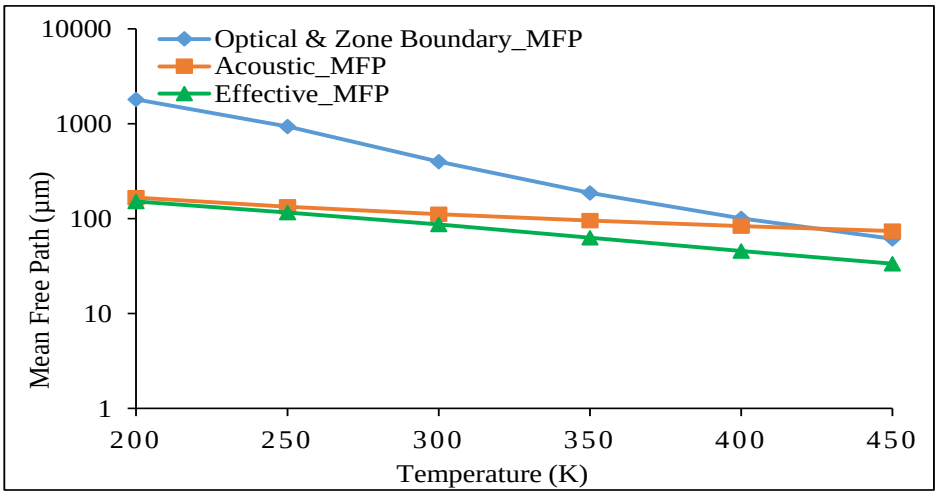
$$N_{ozb}^{T_K} = \left[exp\left(\frac{hw}{k_B T_K}\right) - 1 \right]^{-1} \tag{4.14}$$

The above mentioned equations (Eqs. 4.9 to 4.14) are used to calculate the $\lambda_{eff}^{T_K}$ of the MMT nanostructures for variable temperature having range 200-450K. The effective MFP depends on the acoustics and optical-zone boundary MFPs for a variable temperature range. The $\lambda_{eff}^{T_K}$, λ_{ac} and λ_{ozb} are calculated as shown in Table 4.1. The λ_{ozb} is much higher than λ_{ac} for low to moderate temperature range. The combined impact of λ_{ozb} and λ_{ac} is slightly less on $\lambda_{eff}^{T_K}$ for temperature less than 300K as compared to higher temperatures. The comparison of $\lambda_{eff}^{T_K}$, λ_{ac} and λ_{ozb} is presented in Figure 4.2(a)-(c) at 32, 22 and 16nm technology nodes, respectively.

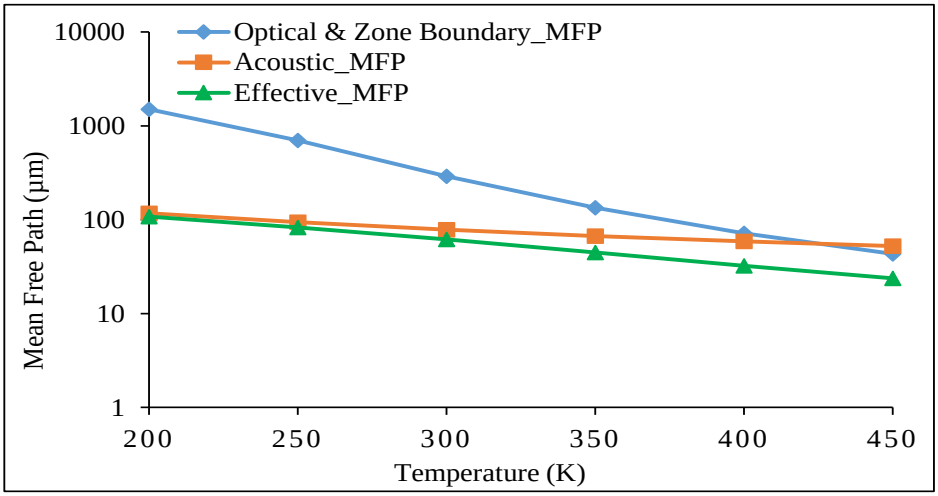
Table 4.1: λ_{ozb}, λ_{ac} and $\lambda_{eff}^{T_K}$ of MMT interconnect.

Temperature (K)	Technology Nodes (nm)								
	32			22			16		
	λ_{ozb}	λ_{ac}	$\lambda_{eff}^{T_K}$	λ_{ozb}	λ_{ac}	$\lambda_{eff}^{T_K}$	λ_{ozb}	λ_{ac}	$\lambda_{eff}^{T_K}$
200	1800	166.4	151.3	1500	117.3	107.9	1100	76.42	71.21
250	932.8	133.1	116.1	701.9	93.90	82.64	500.3	61.14	54.38
300	398.8	110.9	86.72	289.8	78.25	61.58	196.1	50.95	40.42
350	186.9	95.08	63.01	133.8	67.07	44.67	88.76	43.67	29.26
400	100.7	83.2	45.57	71.69	58.69	32.27	47.15	38.21	21.10
450	61.15	73.95	33.47	43.36	52.17	23.68	28.41	33.96	15.47

The comparative analysis shows that the λ_{ozb} and λ_{ac} are decreased with increased temperature ranging from 200 to 450K at DSM technology nodes. The large variation is observed between λ_{ozb} and λ_{ac} at lower temperatures. Therefore, the combined impact of λ_{ozb} and λ_{ac} is computed, which is observed minimum at temperature below 300K. It observes that the λ_{ozb} is sharply decreased for increasing temperature ranging from 200 to 450K. The $\lambda_{eff}^{T_K}$ is calculated by combining the λ_{ac} and λ_{ozb}, which is large variation at higher temperature ranging from 300 to 450K. However, the effective MFP is decreased for rising temperature ranging between 300 and 450K.



(a)



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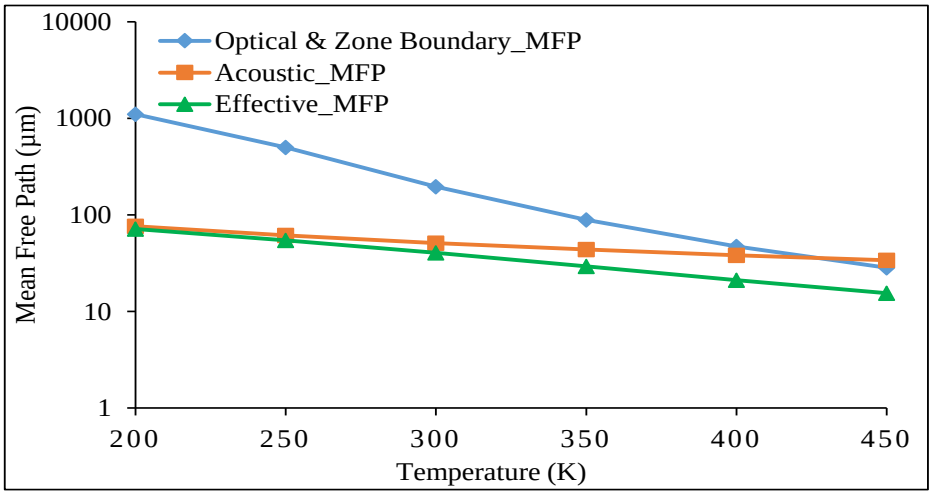


(c)

Figure 4.2: Temperature-dependent acoustic, optical-zone boundary and effective MFPs at DSM technology nodes as (a) 32, (b) 22 and (c) 16nm.

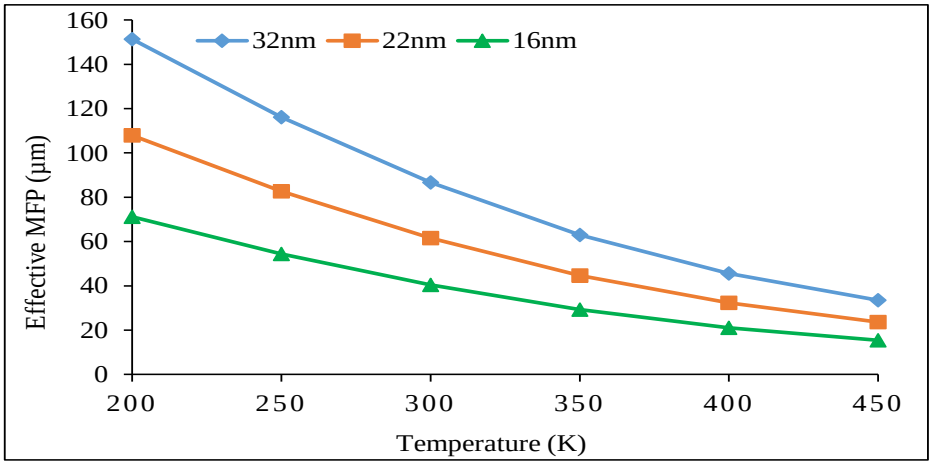


Figure 4.3: Temperature-dependent effective MFPs at 32, 22 and 16nm technology nodes.

The effective MFPs of MMT nanostructure are evaluated for global interconnect length (1000µm) at DSM technology nodes (32, 22 and 16nm) of a variable temperature ranging from 200 to 450K as shown in Figure 4.3. It shows that effective MFP is decreasing for increasing temperature for DSM technology nodes and effective MFP is decreasing for scaled-down technology nodes from 32 to 16nm.

4.2.4 Inductance and capacitance of MMT nanostructures

Inductance (L_{ESC}) of the MMT interconnect involves the kinetic (L_{kESC}) and magnetic (L_{mESC}) inductance of an individual MWCNTs for MMT. L_{kESC} can be calculated by the sum of the individual inductance of $MWCNT_L$ (L_{kESC_L}) and $MWCNT_S$ (L_{kESC_S}). Similarly, L_{mESC} is obtained using the individual inductance of $MWCNT_L$ (L_{mESC_L}) and $MWCNT_S$ (L_{mESC_S}). The calculated values of L_{mESC} can be neglected because its value is much smaller than L_{kESC}. L_{ESC} of MMT is calculated by the Eqs. 3.35 to 3.41 in Chapter 3.

The capacitance (C_{ESC}) of MMT interconnect is obtained by considering all capacitance in the combination of series and parallel, according to the literature and discussed in Chapter 3. C_{ESC} can be determined using all the capacitance of $MWCNT_L$ (C_{ESC_L}) and $MWCNT_S$ (C_{ESC_S}). Further, the C_{ESC_L} (C_{ESC_S}) can be calculated with the help of electrostatic C_{e_L} (C_{e_S}), quantum C_{q_L} (C_{q_S}) and shell-to-shell C_{s_L} (C_{s_S}) capacitance of an individual shell of $MWCNT_L$ ($MWCNT_S$) for MMT nanostructure. These can be calculated by Eqs. 3.45 to 3.53 in Chapter 3.

The individual shells of MWCNTs are assumed to be parallel and considered to calculate temperature-dependent parasitic. Further, these parasitic are used to develop equivalent MCTL model as shown in Figure 4.4.

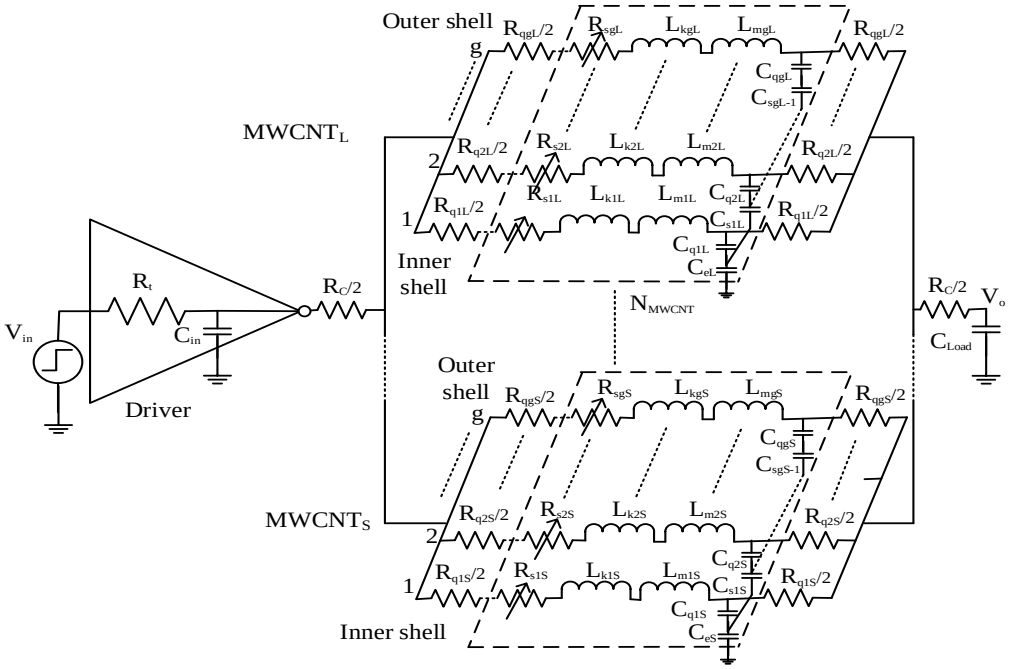
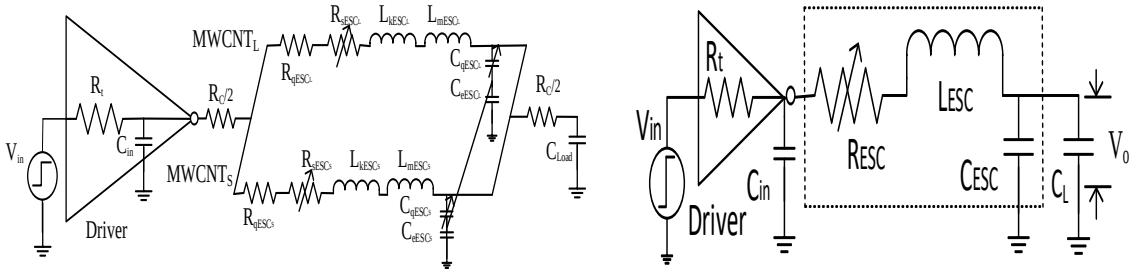


Figure 4.4: Temperature-dependent MCTL model of an individual MWCNT.

The calculated thermally-aware parasitic are considered to develop a thermally-aware equivalent multi-conductor (EMC) model for all $MWCNT_L$ and $MWCNT_S$, as shown in Figure 4.5(a). Then, the thermally-aware EMC model is considered to propose thermally-aware ESC model of MMT as global level VLSI interconnect as shown in Figure 4.5(b). The detail procedure for develop EMC and ESC has been discussed in Chapter 3.



(a) (b)

Figure 4.5: (a)EMC model of all the $MWCNT_L$ and $MWCNT_S$ for MMT interconnect. (b) ESC model of the MMT interconnect.

The resistance of MMT nanostructure as global level interconnect length (1000µm) is calculated for a variable temperature range (200 to 450K) at 32, 22 and 16nm technology nodes as shown in Figure 4.6. Temperature-dependent resistance of MMT is increasing with increase in temperature ranging from 200 to 450K at DSM technology nodes. It reveals that the resistance of MMT nanostructure is increased quickly for temperature more than 300K at 16nm technology nodes.

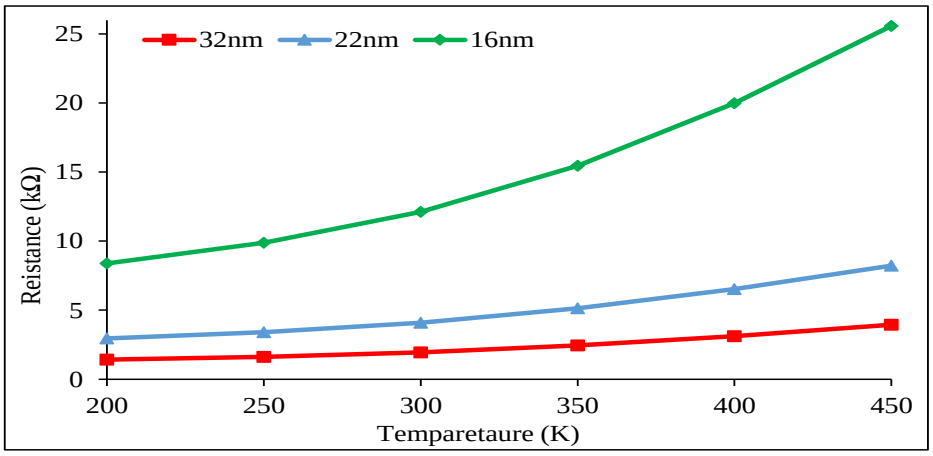
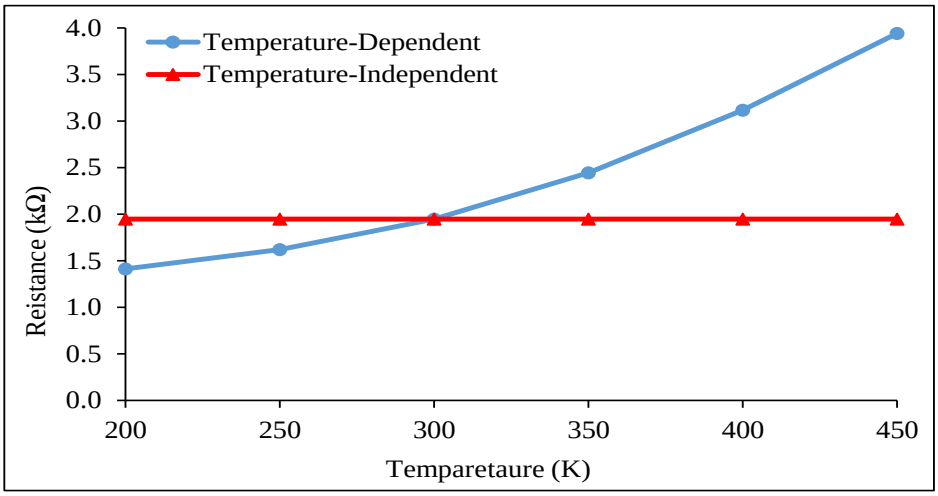


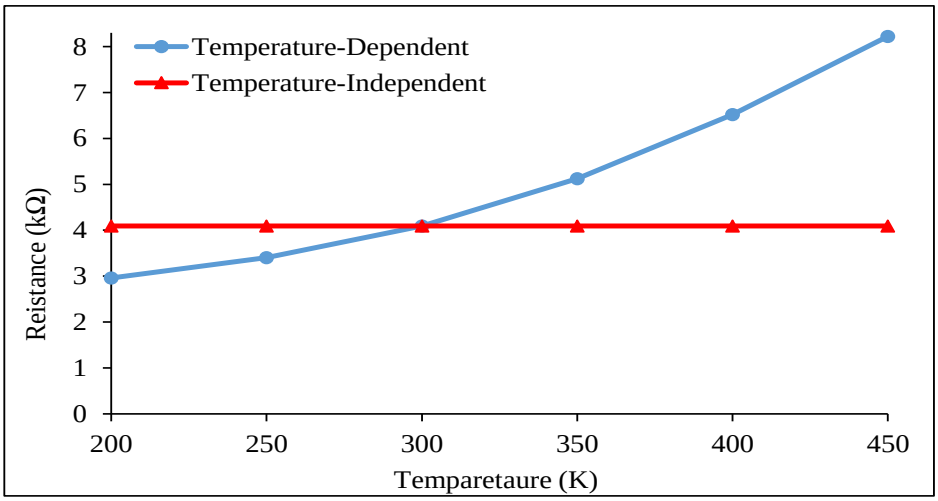
Figure 4.6: Temperature-dependent resistance of the MMT for global interconnect length (1000µm) at DSM technology nodes (32, 22 and 16nm).

The resistance of CNT based nanostructures is increasing sharply for the temperature more than 300K at 16nm technology nodes. The scattering resistance is dominating factor in the overall resistance of MMT nanostructure that influence by effective MFP of CNTs. The effective MFP, which decreases sharply for 16nm technology nodes at temperature more than 300K. The effective MFP happens due to acoustic and optical-zone boundary scattering. The impact of optical-zone boundary scattering is negligible at temperature less than room temperature (300K) but play a non-negligible role for temperature more than 300K. Due this the effective MFP decreases sharply for higher temperature range (¿300K) and it increases the resistance sharply DSM technology nodes particularly at 16nm technology nodes. So, the resistance of MMT interconnect is sharply increased for 16nm technology nodes as compared to 22 and 32 nm for temperature more than 300K. However, the resistance are increased consistently for temperature range 300 - 450K at 32 and 22nm technology nodes. The resistance of MMT nanostructure are increased because the effective MFP is inversely proportional to resistance and MFP is decreased with increasing temperature for all three technology nodes.

The comparison of temperature-dependent and temperature-independent resistance is presented in Figure 4.7 (a), (b) and (c) at DSM technology nodes viz. 32, 22 and 16nm, respectively. It shows that it has a considerable impact of temperature on the resistance of MMT nanostructure at DSM technology nodes. The resistance of MMT increased with a rise in temperature ranging from 200 to 450K at DSM technology nodes. The temperature-dependent resistance is sharply increased because effective MFP of MMT decreased for temperature range between 300 and 450K. It reveals that the influence of temperature on resistance is considered to analyze the actual performance of MMT interconnect under thermally-aware environmental conditions.



(a)



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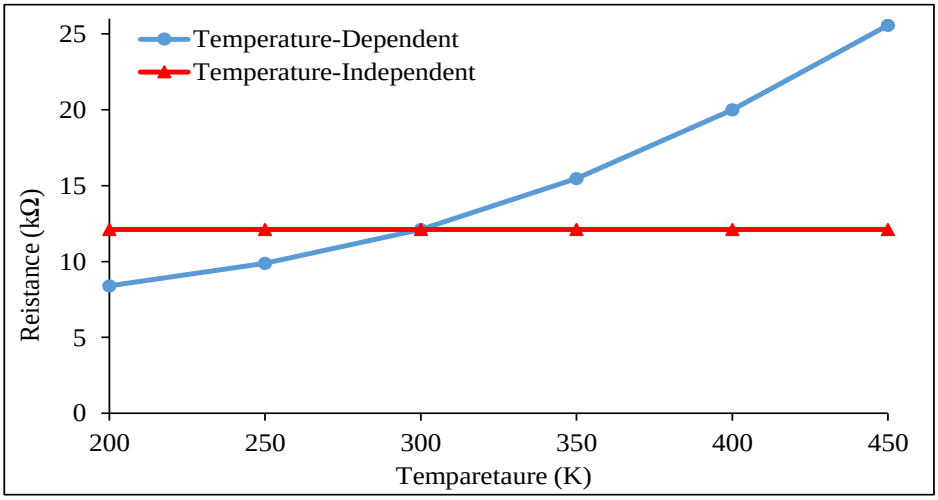


(c)

Figure 4.7: Comparison of temperature-dependent and temperature-independent resistance of MMT interconnect length (1000µm) at DSM technology nodes as (a) 32, (b) 22 and (c) 16nm).

Further, the performance of proposed thermally-aware ESC model of MMT interconnect is examined using SPICE simulation tool in upcoming section.

4.3 Thermally-aware performance of MMT interconnect

The performance of MMT nanostructure is evaluated in terms of delay, power and PDP for global interconnect length as 1000μm on a variable temperature range at DSM technology nodes viz. 32, 22 and 16nm. The performance is evaluated for ESC model of MMT interconnect with the help of simulation SPICE tool for all three technology nodes. The simulation setup is required optimum-sized and optimum number of repeaters to minimize the power dissipation and propagation delay of the MMT interconnect. The optimum-sized and optimum number of repeaters calculated as 30 and 8, respectively [137, 156]. The actual simulation setup is used to evaluate the performance of MMT nanostructure with the help of SPICE tool and shown in Figure 4.8.

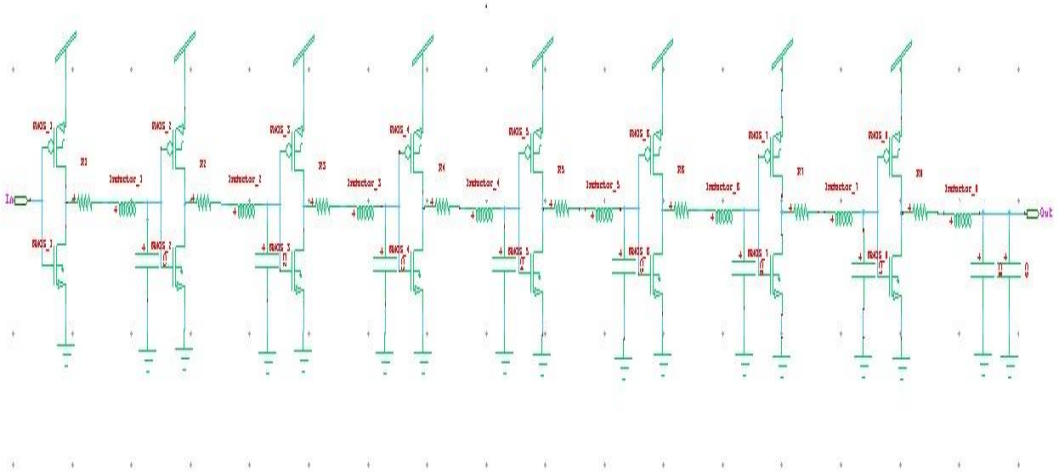
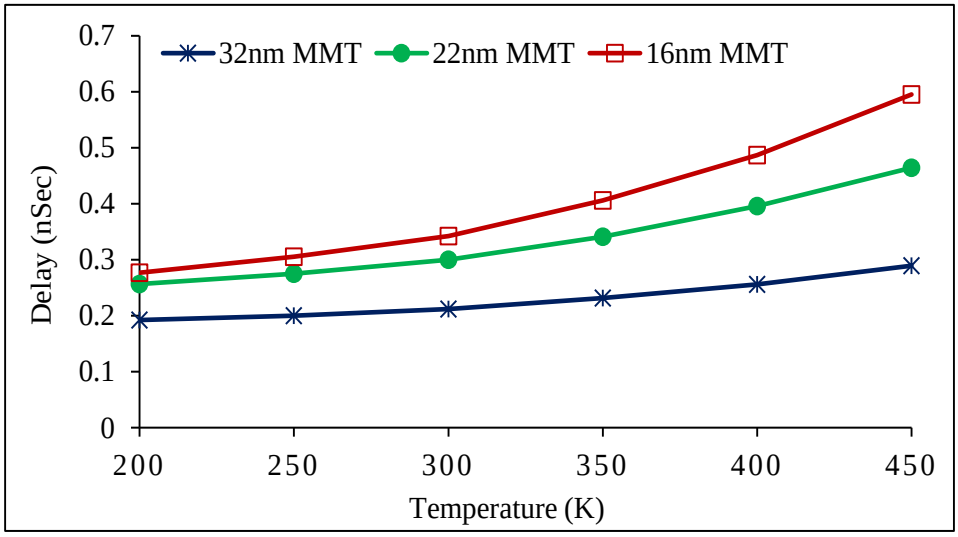


Figure 4.8: Simulation Setup with optimum-sized and optimum number of repeaters.

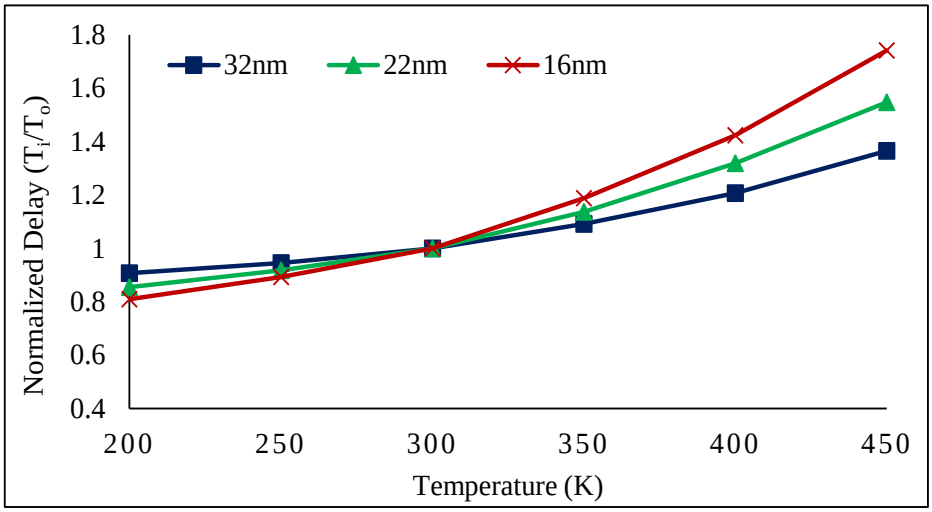
The simulation setup has used eight repeaters with fixed aspect ratio (A/R=30) and individual repeaters can be derived each segment of MMT interconnect (distributed RLC segment). The proposed simulation setup derived by input driver and output is given across load capacitor [139, 159]. The proposed simulation setup is used to evaluate the performance MMT interconnect for variable temperature at various DSM technology nodes and the obtained results of MMT nanostructure are shown in Figure 4.9, 4.10 and 4.11.

Temperature-dependent performance of MMT nanostructure as VLSI interconnect for global interconnect length (1000μm) in terms of delay is shown in Figure 4.9(a) for 32, 22 and 16nm

technology nodes. The results reveal that delay is increased with increasing temperature ranging from 200 to 450K for DSM technology nodes under consideration. The delay of the MMT is observed less for 32nm technology node than 22 and 16nm technology nodes. Therefore, the delay of MMT nanostructure is increased for scaled-down technology nodes from 32 to 16nm.



(a)



(b)

Figure 4.9: (a)Temperature-dependent performance in terms of delay and (b) Normalized delay ratio of MMT interconnect at 32, 22 and 16nm DSM technology nodes.

Further, the normalized delay ratio (T_i/T_0) of MMT nanostructure as VLSI interconnect is shown in Figure 4.9(b). The normalized delay ratio of MMT nanostructure as VLSI interconnect is significantly large for temperature greater than 300 to 450K for DSM technology nodes as 32, 22 and 16nm as shown in Table 4.2. The normalized delay ratio for temperature 200K is observed as 0.90 at 32, 0.85 at 22 and 0.81 at 16nm technology nodes. The normalized

delay ratio of MMT nanostructure for temperature ranging from 300 to 450K is observed as 1.09 to 1.36, 1.13 to 1.54 and 1.18 to 1.74 for 32, 22 and 16nm technology nodes, respectively. For 450K temperature, the normalized delay ratio is observed for technology node 32 as 1.36, 22 as 1.54 and 16nm as 1.74. The impact of temperature above 300K on the performance of MMT nanostructure is increasing with decreased technology nodes from 32 to 16nm. For scaled-down technology nodes from 32 to 16nm, the normalized delay ratio is examined on temperature 350K as 1.09 to 1.18, 400K as 1.2 to 1.42 and 450K as 1.36 to 1.74. It reveals that the performance of MMT nanostructure in terms of delay is worst with increase in temperature as well as decreasing technology nodes. Therefore, it is necessary to include the impact of temperature on the performance of high-performance VLSI-ICs design for real-time applications.

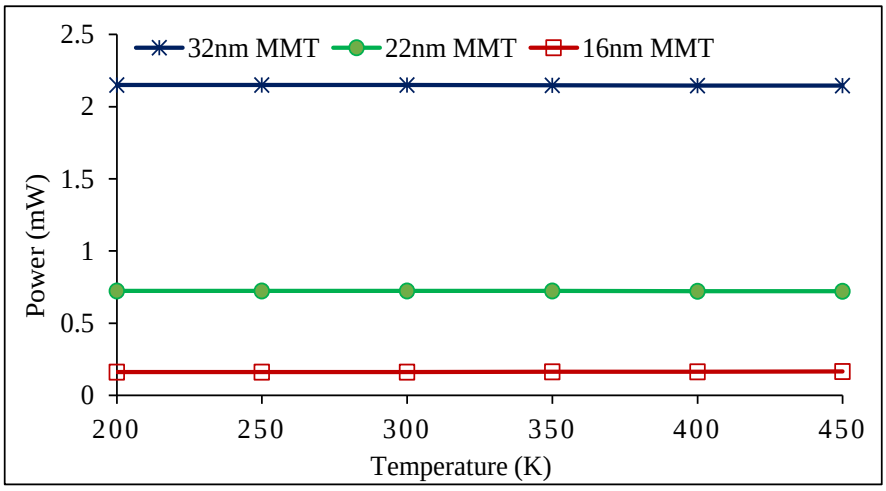
Table 4.2: Normalized delay ratio (T_i/T_0) of MMT interconnect

Technology	Temperature (K)					
nodes	200	250	300	350	400	450
32nm	0.906791	0.944688	1	1.091557	1.206333	1.365142
22nm	0.854251	0.917072	1	1.136479	1.31854	1.546816
16nm	0.809096	0.892951	1	1.187657	1.423896	1.740831

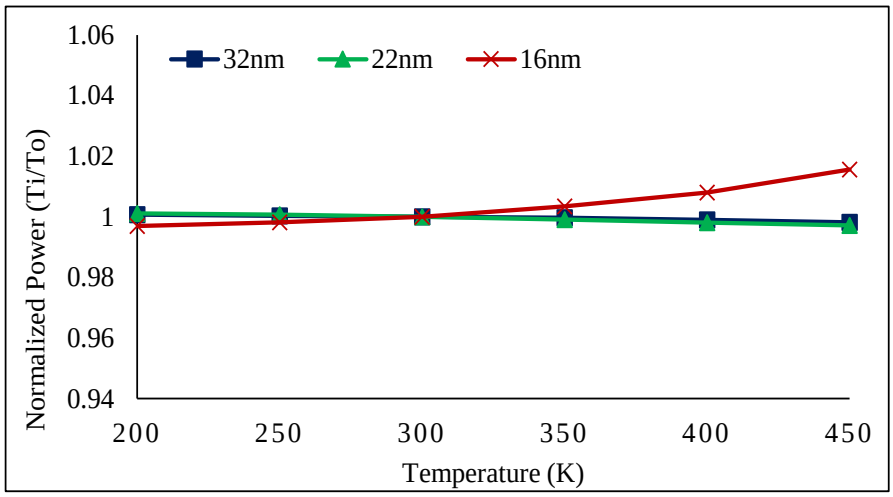
The performance of MMT nanostructure in terms of power is shown in Figure 4.10(a) for temperature range (200-450K) at DSM technology nodes. The power of MMT nanostructure is decreased for scaled-down technology nodes from 32 to 16nm. The power consumption of MMT interconnect is observed less for 16nm as compare to 22 and 32nm technology nodes. Further, normalized power ratio (T_i/T_0) has been evaluated for variable temperature range 200-450K at DSM technology nodes (32, 22 and 16nm) as presented in Table 4.3. The normalized power ratio is almost constant for 32 and 22nm technology nodes, however, it is increased for temperature ranging from 200 to 450K at 16nm technology nodes as shown in Figure 4.10(b).

Table 4.3: Normalized power ratio (T_i/T_0) of MMT interconnect

Technology	Temperature (K)					
nodes	200	250	300	350	400	450
32nm	1.000679	1.000363	1	0.99967	0.998948	0.998165
22nm	1.001131	1.000704	1	0.999091	0.998043	0.997171
16nm	0.996977	0.998218	1	1.003463	1.00799	1.015589

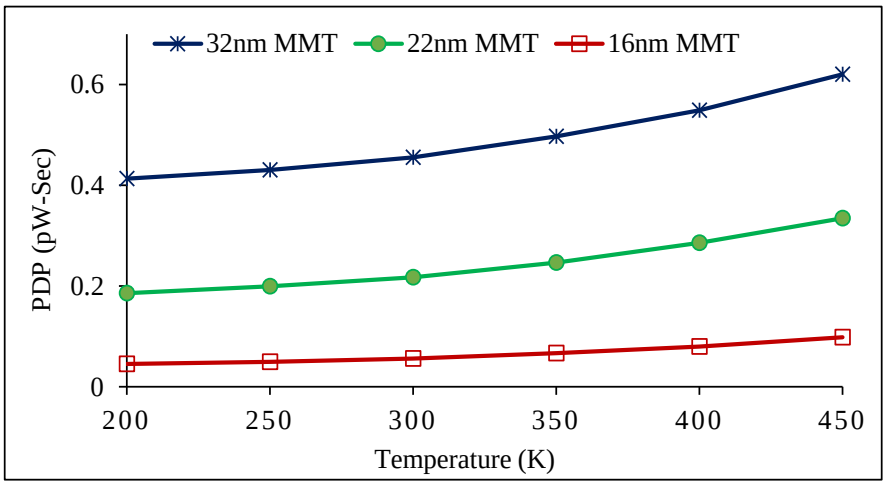


(a)

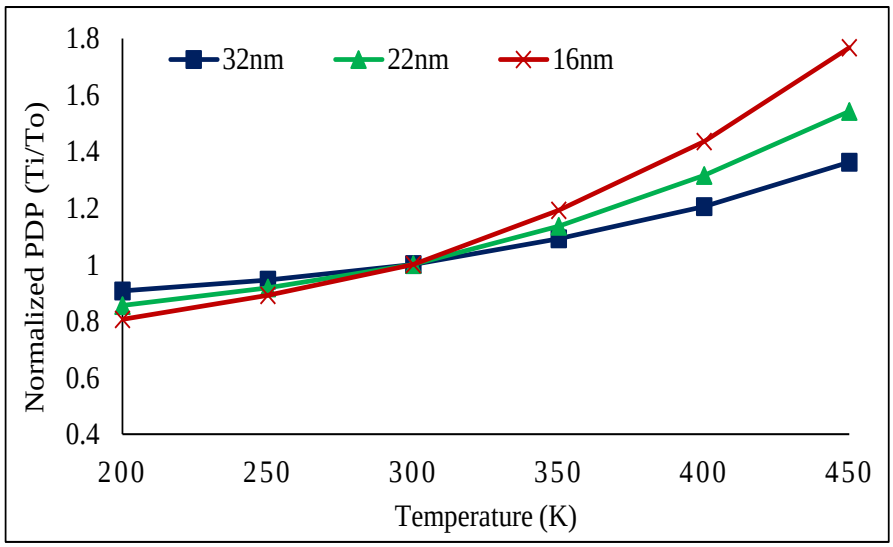


(b)

Figure 4.10: (a)Temperature-dependent performance in terms of power and (b) Normalized power ratio of MMT interconnect at 32, 22 and 16nm DSM technology nodes.



(a)



(b)

Figure 4.11: (a)Temperature-dependent PDP and (b) Normalized PDP ratio of the MMT interconnect at 32, 22 and 16nm technology nodes.

Table 4.4: Normalized PDP ratio of MMT interconnect

Technology	Temperature (K)					
nodes	200	250	300	350	400	450
32nm	0.907407	0.945031	1	1.091196	1.205064	1.362638
22nm	0.855217	0.917718	1	1.135446	1.315959	1.542439
16nm	0.80665	0.89136	1	1.19177	1.435274	1.767968

The performance of MMT nanostructure in terms of PDP is shown in Figure 4.11(a). The PDP of MMT interconnect is increased with increasing temperature ranging from 200 to 450K for DSM technology nodes viz. 32, 22 and 16nm. The PDP is decreased with scaled-down technology nodes from 32 to 16nm technology nodes. The normalized PDP ratio of MMT nanostructure as VLSI interconnect is calculated as given in Table 4.4.

The normalized PDP ratio of MMT interconnect is sharply increased for temperature greater than 300K at all three technology nodes under consideration as shown in Figure 4.11(b). The normalized PDP ratio of MMT is examined large for 16nm as compared to 22 and 32nm technology nodes. The normalized PDP ratio is estimated for a temperature range 200 to 450K as 0.90 to 1.36, 0.85 to 15.4 and 0.80 to 1.76 at 32, 22 and 16nm technology nodes, respectively. At scaled-down technology nodes from 32 to 16nm, the normalized PDP ratio is also examined for temperature 350K as 1.09 to 1.19, 400K as 1.2 to 1.43 and 450K as 1.36 to 1.76.

4.4 Temperature-dependent ESC model of Cu interconnects

This section presents the temperature-dependent parasitic of Cu to develop ESC model for global interconnect (length 1000μm) at DSM technology nodes viz. 32, 22 and 16nm. Then, this ESC model is considered to evaluate performance in terms of delay, power and PDP for a variable temperature ranging from 200 to 450K. The parasitic of Cu depend upon a cross-sectional area and length of interconnect as well as its resistivity, which is considered as per ITRS-2013. The structure of Cu interconnect is presented with various dimensions such as height (H), width (W) and length (L_i) of interconnect at the ground plane as shown in Figure 6.1. The temperature-dependent resistance of Cu as global level VLSI interconnect can be

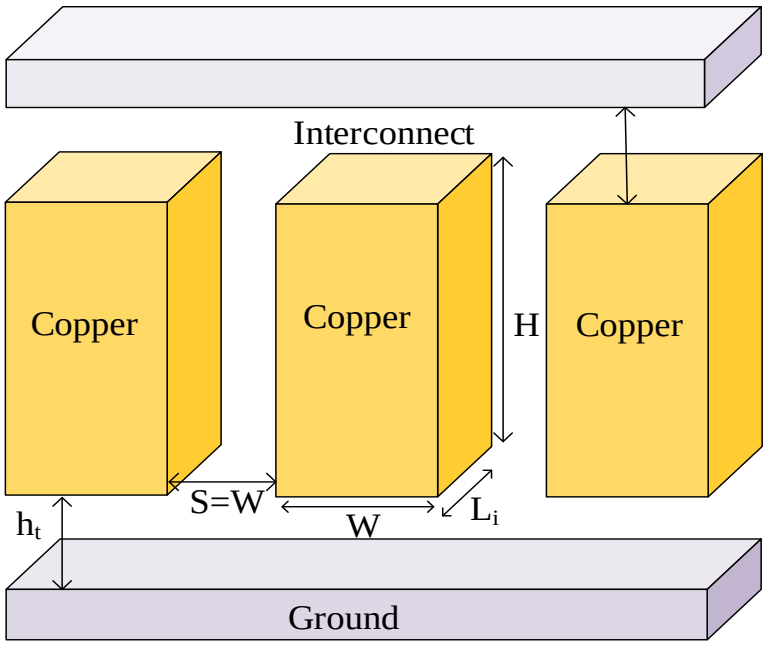


Figure 4.12: Structure of Cu as VLSI interconnects at the ground plane.

calculated by the following equation

$$R_{Cu} = \rho_T \frac{L_i}{HW} \tag{4.15}$$

where, ρ_T, L_i, H and W are temperature-dependent resistivity of Cu, length, height and width of interconnect, respectively. Temperature-dependent resistivity (ρ_T) can be given by

$$\rho_T = \rho_0[1 + 0.004(T_K - T_0)] \tag{4.16}$$

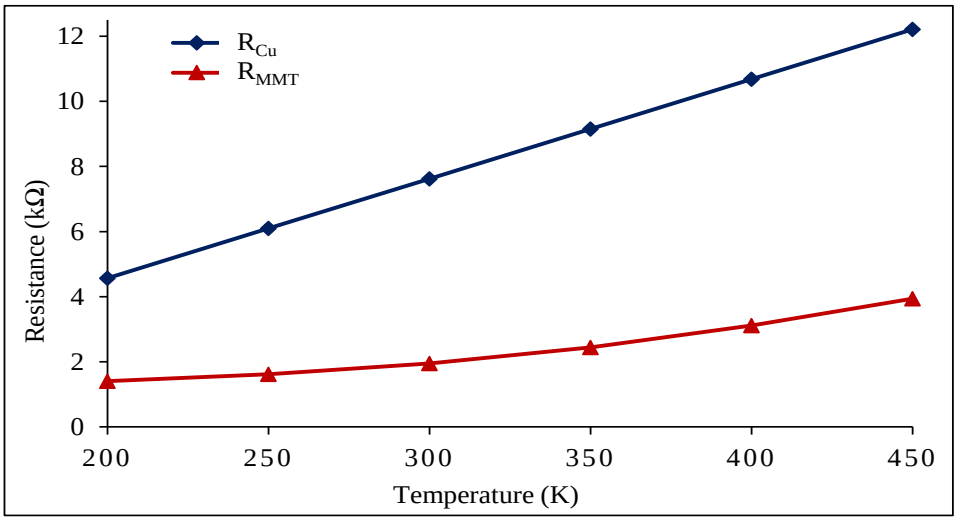
ρ_0, T_K and T_0 are technology dependent resistivity of Cu at 300K, a variable temperature range 200-450K and room temperature as 300K, respectively.

The inductance (L_{Cu}) and capacitance (C_{Cu}) of Cu material used as VLSI interconnect can be calculated by Eqs. 3.55 to 3.58 given in Chapter 3 [97, 153, 154].

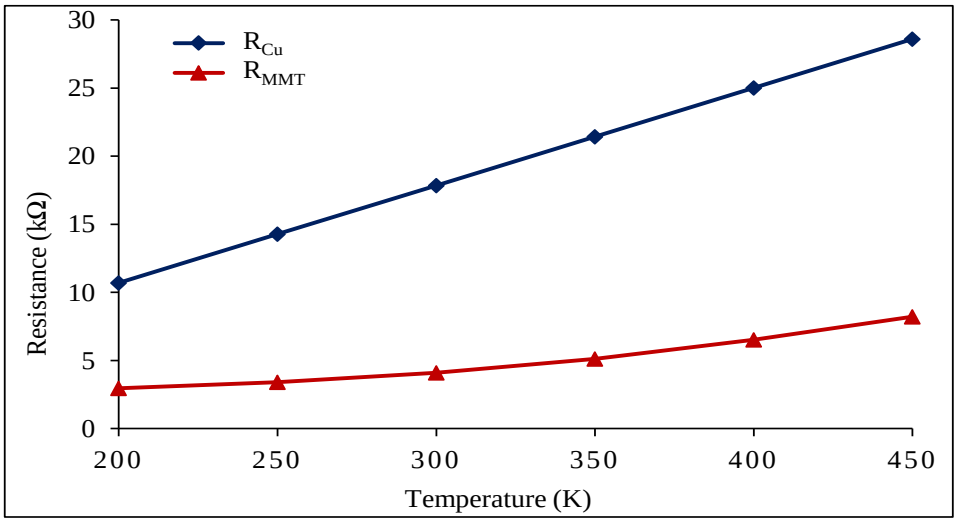
4.5 Temperature-dependent resistance of Cu and MMT interconnect

The comparison of temperature-dependent resistance of MMT nanostructure and Cu material as global level VLSI interconnect. The cross-sectional dimensions of VLSI interconnect for DSM technology nodes are considered as predicted by ITRS-2013 as shown in Table 3.1. The calculated resistance of proposed MMT nanostructure and Cu material as VLSI interconnect is present in Figure 4.13. The results are calculated for a global interconnect length (1000μm) at technology nodes, i.e., 32, 22 and 16nm for variable temperature ranging from 200 to 450K. The comparison of resistance shows that the resistance of Cu and MMT is increasing with increase in temperature from 200 to 450K.

The parasitic of Cu interconnect increases at DSM technology nodes (especially below 45nm) as the MFP of Cu is approximately 45nm, which degrades their performance. The cross-sectional area of VLSI interconnect reduces by scaled-down technology nodes, where it requires high current density and larger electron MFP. But Cu material has limited current density and small electron MFP. The combined effects of above mention problems are boosting the surface and grain boundary scattering as well as electro-migration. These factors enhance the scattering resistance, which increases the overall resistance of Cu interconnect.
On the other hand, CNT has large electron MFP and high current density even at DSM technology nodes. Due to these advantages, the CNT is the promising candidate at DSM technology nodes particularly below 45nm technology nodes. Therefore, the resistance of MMT nanostructure at DSM technology nodes is observed less as compared to copper as VLSI interconnect. The resistance of Cu and MMT has increased because of decreasing MFP with increase in temperature-dependent scattering phenomena. The impact of resistance for Cu has observed more as compared to MMT nanostructure as VLSI interconnect.



(a)



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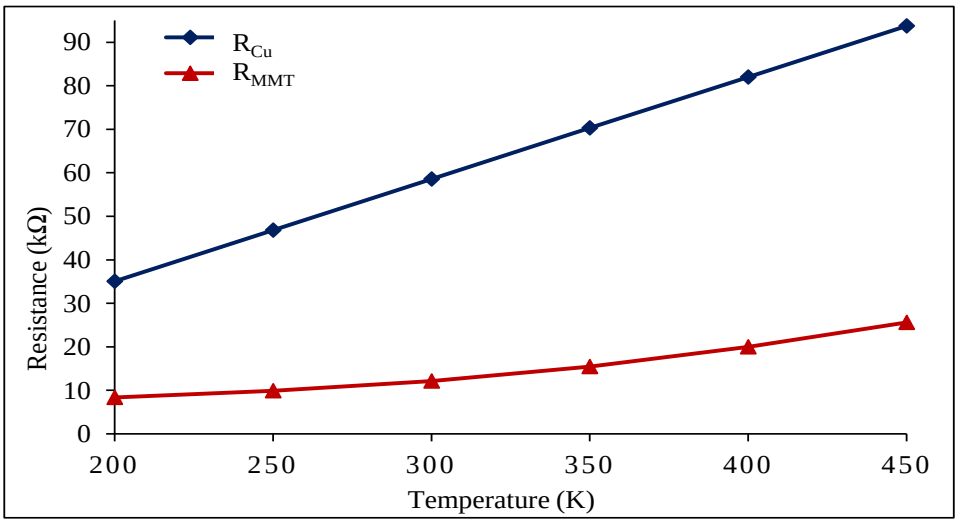


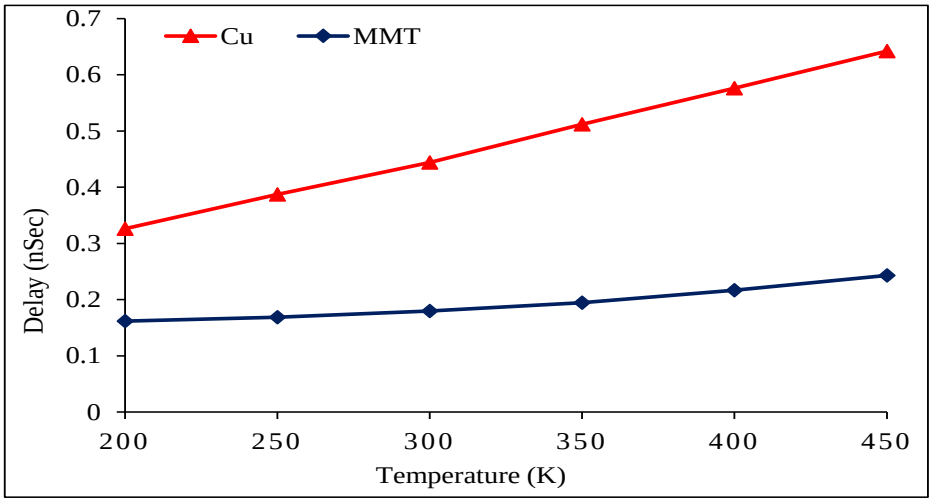
(c)

Figure 4.13: Temperature-dependent resistance of MMT and Cu as global level VLSI interconnect at DSM technology nodes as (a) 32, (b) 22 and (c) 16nm.

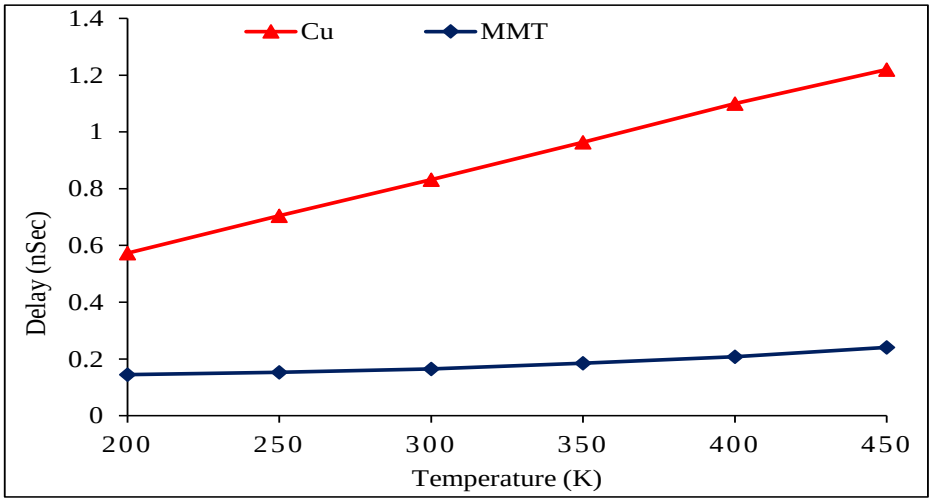
The gap between resistance of Cu and MMT nanostructure has been increased from temperature ranging from 200 to 450K. It reveals that the performance of MMT is better than Cu at DSM technology nodes for global interconnect length under thermally-aware environmental conditions.

4.6 Temperature-dependent performance analysis of MMT and Cu interconnects

The estimated performance of MMT nanostructure in terms of delay, power and PDP are compared with Cu interconnect on a variable temperature (200-450K) at DSM technology nodes. The temperature-dependent ESC models for MMT nanostructure and Cu interconnects are presented for DSM technology nodes.



(a)



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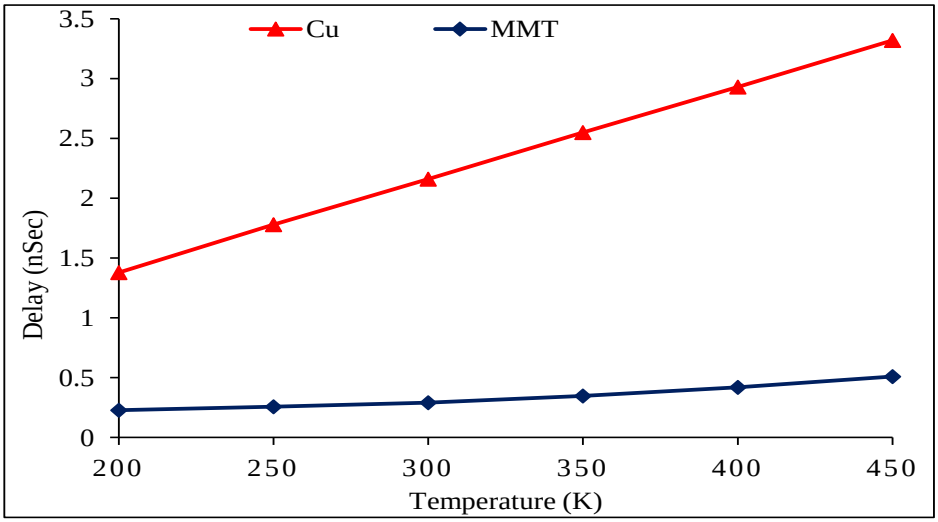


(c)

Figure 4.14: Comparison of delay for MMT and Cu for 1000μm interconnect length at DSM technology nodes as (a) 32, (b) 22 and (c) 16nm.

Further, the obtained parasitic of MMT nanostructure and Cu interconnect using ESC models are simulated with the help of SPICE tool to examine the performance i.e. power and delay. Temperature-dependent delay of MMT nanostructure and Cu as VLSI interconnects are compared on a variable temperature range (200-450K) at DSM technology nodes viz. 32, 22 and 16nm as shown in Figure 4.14 (a)-(c), respectively. It revealed that the delay of MMT and Cu interconnects are increased with rising temperature from 200-450K because of decrease in the MFPs of MMT.

However, the delay of MMT is smaller than Cu for global interconnect for DSM technology nodes. The performance of MMT has significantly improved in terms of delay as compared to Cu interconnect for rising temperature range 200-450K at 32, 22 and 16nm technology nodes.

Chapter Summary

In this chapter, impact of temperature on the performance of proposed MMT interconnect under thermally-aware environmental conditions is presented at DSM technology nodes. The performance of MMT nanostructure is calculated for global interconnect length (1000μm) as a function of temperature ranging from 200 to 450K at various DSM technology nodes (32, 22 and 16nm). The influence of variable temperature on scattering phenomena of CNTs are observed in this Chapter. The scattering phenomena influenced the MFP of each shell of individual MWCNTs of MMT nanostructure and it is obtained using the mathematical calculations

presented in this chapter. The MFP based on electron-phonon and electron-electron scattering mechanism. Further, effect of temperature observed directly on the parasitic of MMT nanostructure as a global level interconnects at DSM technology nodes. The temperature-dependent RLC model is developed for each shell of individual MWCNT and considered to develop a temperature-dependent ESC model of MMT nanostructure.

Furthermore, the performance of the MMT interconnect is evaluated form the developed ESC model in terms of delay, power and PDP at DSM technology nodes for a variable temperature range. The performance in terms of delay of the MMT nanostructure is increased with rising temperature moderate to high at all three technology nodes considered for this work. For temperature 450K, the normalized delay ratio of MMT interconnect is observed as 1.36, 1.54 and 1.74 for 32, 22 and 16nm technology nodes, respectively. For temperature range 200 to 450K, the normalized PDP ratio is also calculated at technology nodes 32nm as 0.90 to 1.36, 22nm as 0.85 to 15.4 and 16nm as 0.80 to 1.76. It reveals that the performance of MMT is influenced with increase in temperature and with deceasing technology nodes. Then, the temperature-dependent ESC model of Cu interconnect is developed to examine the performance in terms of delay at DSM technology nodes. It shows that the performance of MMT nanostructure as VLSI interconnect outperforms Cu in terms of delay. It can be used as future interconnect material at DSM technology nodes for high-performance VLSI-ICs design.

Pardeep Kumar Jindal and Karmjit Singh Sandha. Thermally-Aware Modeling and Performance Analysis of Mixed-MWCNTB as Very Large Scale Integrated Interconnects Material for Nano-Electronic Integrated Circuits Design. *"Journal of Nanoelectronics and Optoelectronics"*, 14(9): 1255-1266, 2019. (**Impact factor 1.069**).

Chapter 5

Analytical Delay Model For MMT Interconnects

This chapter presents the temperature-dependent analytical delay model of the MMT nanostructure as VLSI interconnects at DSM technology nodes. The results obtained from the analytical model are compared with simulated results of MMT nanostructure obtained from Chapter 4. It reveals that the delay of analytical and simulated models increased with rising temperature ranging from 200 to 450K at various technology nodes as 32, 22 and 16nm. Further, the temperature-dependent analytical delay of Cu interconnect is also calculated at DSM technology nodes. The analytical results of Cu and MMT nanostructure are compared with simulated results of Cu and MMT, which are increasing with rise in temperature ranging from 200 to 450K at various technology nodes as 32, 22 and 16nm. The calculated analytical results for proposed model are aligned with the simulated results for all three technology nodes viz. 32, 22 and 16nm.

5.1 Introduction

For DSM technology nodes, the reduced chip size of VLSI-ICs decreases the device size and interconnect dimensions. The overall delay of device increases, the delay consists of the gate delay and interconnect delay. Earlier gate delay was dominant part to influence total interconnect delay. It predicts by assuming the entire interconnect tree at output of gate and a lumped RLC model is shown in Figure 5.1. Now for DSM technology nodes, the delay of interconnects is a dominating part of the total delay of the device because the parasitic of interconnect are larger than device [4, 5, 9].

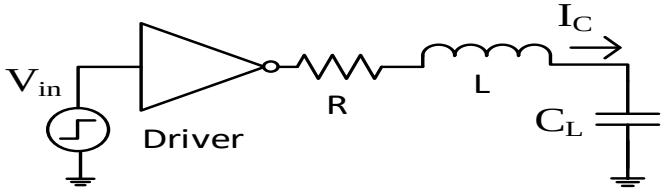


Figure 5.1: RLC lumped model followed by inverter. [119]

Further, the dimensions of interconnect is decreasing due to scaled-down technology nodes and impedance parameters become larger [34, 66, 67]. The lumped model is not much accurate to estimate performance for large impedance parameters because it introduces an error to obtain approximation capacitance and rise time for the interconnect line. The accuracy of predicting gate delay and rise time depend on impedance parameters. VLSI Interconnects are considered as transmission lines having impedance parameters such as resistance, capacitance and inductance. The highly accurate RLC distributed model requires to evaluate accurate delay of interconnects for VSLI-ICs at DSM technology nodes as shown in Figure 5.2. Elmore delay model is a simple RC model, which is considered to estimate performance of interconnect in terms of delay. The results of Elmore model is inaccurate for an input signal of high frequency because the inductive effect is not included, which is increasing at DSM technology nodes [44, 48–52].

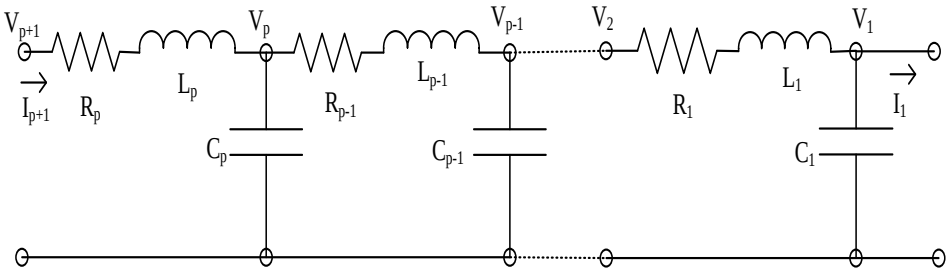


Figure 5.2: RLC Distributed model. [25]

The Al and Cu material were used as VLSI interconnect at micro-scaled technology nodes and the ESC models are developed to calculate parasitic [56, 57]. Many researchers have presented the numerous RC and RLC lumped models and considered to estimating the delay of interconnects. These lumped models are used as distributed models by inserting number of optimum-sized repeater in interconnect line as shown in Figure 5.3.

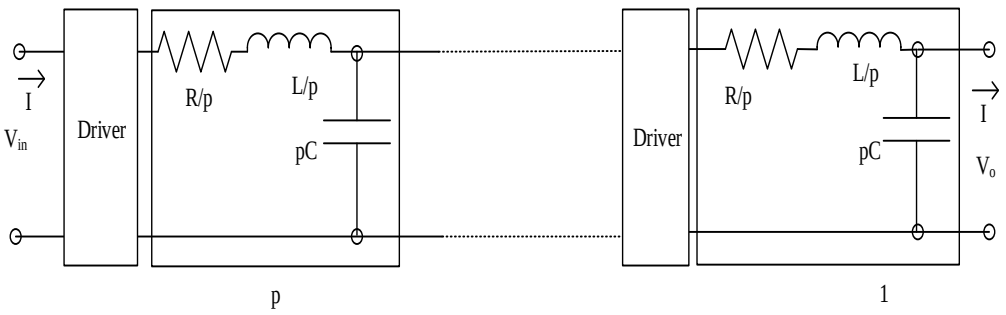


Figure 5.3: Distributed RLC model of a VLSI interconnect having p-segments. [50]

Further, the RC delay models are used to calculate delay for resistive-capacitance loads only, where the inductive effect is not included. Nevertheless, few research articles have also been

published, which includes the impact of inductance. The RLC delay models are provided highly accurate results of delay as compared to RC delay models [28, 36, 38, 41].

The Cu has some limitations at DSM technology nodes like electro-migration and scattering phenomena. To overcome these issues, the CNT can use as an alternative material for interconnects [64, 67, 78, 83]. The parasitic of CNTs are different for complex circuitry of VLSI-ICs, the available models in the literature are not accurate enough to estimate the delay.

The ESC models are developed by considering interconnects as transmission lines and developed models are used to estimating performance in terms of delay. After that, number of delay models of the SWCNT and MWCNT interconnects have been proposed by various researchers as discussed in the literature [16, 66, 83, 97, 134]. In MWCNTB, the few delay models have developed based on assumption that only a few shells are involved in conduction of signal due to imperfect contact between shells of CNT and metal. A few number of models of MWCNT have developed assuming all shells can be contributed in conduction [73–76, 92–96].

The perfect contact has established between the metal and all shells of MWCNTB by using the end contact technique. These models can be considered to examine the performance as VLSI interconnects. The ESC models of MWCNTB and SWCNTB interconnect have already been proposed in the literature. Further, the MWCNTB are outperformed as global and semi-global interconnect lengths. The distributed RLC models considered to observe performance in terms of minimum delay and less power consumption. [110, 147, 148, 156]

The closed-form mathematical equations have established to examine the delay, the optimum-sized repeater and the optimum number of repeaters in the line for the proposed MMT bundle as global interconnect [137, 156]. The performance of MMT nanostructure in terms of delay is calculated by mathematical model at DSM technology nodes for a variable temperature range (200-450K). The obtained results from analytical model are compared with simulated results.

5.2 ESC model for MMT nanostructure as VLSI interconnect

The MMT has proposed by combining two differently-sized MWCNTs such as $MWCNT_L$ and $MWCNT_S$ for VLSI interconnect. The overall conductivity of the MMT is increased due to insertion of multiple conductive $MWCNT_S$ to occupy the vacant space in densely packed MWCNTB. The developed MMT nanostructure has a large number of conducting channels as

compared to MWCNTB as global interconnect. All the shells of $MWCNT_L$ and $MWCNT_S$ in MMT nanostructure as VLSI interconnect are considered to be parallel. The ESC model of MMT nanostructure as VLSI interconnect at DSM technology nodes on a variable temperature range as shown in Figure 5.4.

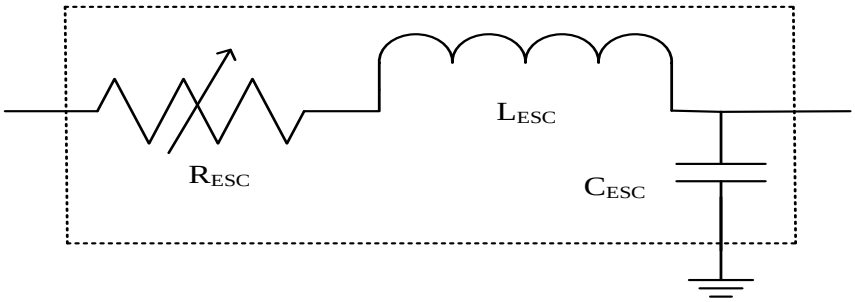


Figure 5.4: The ESC model for MMT nanostructure as VLSI interconnects.

The MMT has two differently-sized MWCNTs ($MWCNT_L$ and $MWCNT_S$) with various number of shells (N_{sh}) as obtained by the Eqs. 3.8 - 3.9 in Chapter 3. These shells are counted from outer- to inner-most as 1, 2, 3,....., g,....., N_{sh}. Each shell of $MWCNT_L$ and $MWCNT_S$ have different diameter and various number of conducting channels obtained by Eqs. 3.10 - 3.11 and Eqs. 4.1 - 4.2, respectively.

The temperature-dependent performance of MMT as global level VLSI interconnect is analyzed and presented in this thesis. The temperature-dependent resistance of each shell of MWCNT depends on quantum resistance (R_q), scattering resistance (R_S) and contact resistance (R_C). The temperature-dependent scattering resistance (R_S) occurs due to length of CNT greater than its MFP. The quantum resistance (R_q) happens because of quantum confinement of nano-wires. The contact resistance (R_C) depends on imperfect contact between metal and shells of MWCNT. The value of R_C measures from few to hundreds of kΩ and can be reduced by making perfect contact between metal and shells. Its value is considered as 2 kΩ for the work presented in this thesis [97, 106, 121]. The temperature-dependent resistance of an shell is obtained by

$$R_{sh} = \underbrace{2k\Omega}_{R_c} + \underbrace{\frac{h}{2e^2}\frac{1}{N_{ch/sh}^{T_K}}}_{R_q} + \underbrace{\frac{h}{2e^2}\frac{L_i}{N_{ch/sh}^{T_K}\lambda_{eff}^{T_K}}}_{R_s} \tag{5.1}$$

where, $\frac{h}{2e^2}$ is the quantum intrinsic resistance (12.9kΩ) for a single conducting channel of each shell of individual MWCNT and temperature-dependent MFP denotes as $\lambda_{eff}^{T_K}$ [125].

Now, the resistance of MMT interconnect (R_{MMT}) can calculate by assuming all shells of MWCNTs to be parallel, where each shell is participating in the conduction. It can be calculated by

$$R_{MMT} = R_C + R_L^{MMT} + R_S^{MMT} * L_i \tag{5.2}$$

where, lumped resistance (R_L^{MMT}) and scattered resistance (R_S^{MMT}) for both $MWCNT_L$ as well as $MWCNT_S$, which can be given by

$$R_L^{MMT} = \left[\left(R_L^{MMT_L} \right)^{-1} + \left(R_L^{MMT_S} \right)^{-1} \right]^{-1} \tag{5.3}$$

$$R_S^{MMT} = \left[\left(R_S^{MMT_L} \right)^{-1} + \left(R_S^{MMT_S} \right)^{-1} \right]^{-1} \tag{5.4}$$

$$R_L^{MMT_L} = \frac{R_q}{N_{MWCNT_L} \sum_{g=1}^{N_{sh_L}} N_{ch/sh_L}^{T_K}} \tag{5.5}$$

$$R_L^{MMT_S} = \frac{R_q}{N_{MWCNT_S} \sum_{g=1}^{N_{sh_S}} N_{ch/sh_S}^{T_K}} \tag{5.6}$$

$$R_S^{MMT_L} = \frac{R_q}{N_{MWCNT_L} \sum_{g=1}^{N_{sh_L}} N_{ch/sh_L}^{T_K} \lambda_{eff_L}^{T_K}} \tag{5.7}$$

$$R_S^{MMT_S} = \frac{R_q}{N_{MWCNT_S} \sum_{g=1}^{N_{sh_S}} N_{ch/sh_S}^{T_K} \lambda_{eff_S}^{T_K}} \tag{5.8}$$

$\lambda_{eff}^{T_K}$ are temperature dependent electron MFP of g^{th} shell of MWCNT.

The electron-phonon and electron-electron scattering influence $\lambda_{eff}^{T_K}$. The electron-phonon scattering can calculate by combining acoustic, optical-zone boundary scattering phenomena of metallic CNT shell and can be calculated by the following equations

$$\lambda_{eff}^{T_K} = \left[\underbrace{\left(266667 \frac{D_g}{T_K} \right)^{-1}}_{\lambda_{ac}} + \underbrace{(\lambda_{ozb}^{fld})^{-1} + (\lambda_{ozb}^{abs})^{-1}}_{\lambda_{ozb}} \right]^{-1} \tag{5.9}$$

The acoustic MFP (λ_{ac}) presents due to acoustic scattering and it has a negligible impact on $\lambda_{eff}^{T_K}$ for temperature less than 300K. It depends on the diameter (D_g) of MWCNT shells and a variable temperature range (T_K). The optical-zone boundary MFP (λ_{ozb}) occurs because of emission and absorption of electron-phonon. The electric field generated along CNT, where electron accelerates to get kinetic energy upto phonon energy level. After getting sufficient

energy, electron starts emitting a phonon with energy $h\omega$ ($h\omega$ are 0.16eV and 0.2eV for optical phonon and zone-boundary, respectively). The optical or zone-boundary scattering happens due to electron acquires required energy by absorbing another optical or zone boundary phonon.

λ_{ozb}^{fld} is optical or zone-boundary scattering based on electric-field acceleration MFP and can examine by the following equation.

$$\lambda_{ozb}^{fld} = \frac{h\omega - k_B T_K}{eV} * L_i + \frac{\lambda_{ozb300} D_g}{D_0} \frac{N_{ozb}^{300} + 1}{N_{ozb}^{T_K} + 1} \tag{5.10}$$

where, k_B and $k_B T$ are the Boltzmann's constant and thermal energy, respectively. First term represents distance travels by electron to achieve phonon emission threshold energy. Second term correspond to the distance travels by electron after getting energy and before releasing a phonon. The spontaneous effective emission length is measured as $\lambda_{ozb300} \approx 15nm$ for diameter (D_0) at 300K. MWCNTs of large diameters have their sub-bands extended to Fermi level that plays important role for its conductance by creating the conducting channels for the flow of electron.

λ_{ozb}^{abs} is the scattering due to absorption of optical or zone boundary phonon and can be calculated by the following equation

$$\lambda_{ozb}^{abs} = \frac{\lambda_{ozb}^{300} D_g}{D_0} \frac{N_{ozb}^{300} + 1}{N_{ozb}^{T_K}} \tag{5.11}$$

where, the occupied states of optical-zone boundary phonon (N_{ozb}) are known as density of states for final electron state after scattering of an phonon, which can be given below [123–126]

$$N_{ozb}^{T_K} = \left[exp\left(\frac{h\omega}{k_B T_K} \right) - 1 \right]^{-1} \tag{5.12}$$

The inductance (L_{MMT}) of an individual shell of MWCNT have magnetic (L_m) and kinetic (L_{kESC}) inductance (per unit length). L_m is very small as compared to L_{kESC}, which can be neglected [16, 133]. These inductance can be obtained by the following equations

$$L_{MMT} = L_{mESC} + L_{kESC} \tag{5.13}$$

$$L_{mESC} = \left[\left(L_{mESC}^{g_L, g_L+1} \right)^{-1} + \left(L_{mESC}^{g_S, g_S+1} \right)^{-1} \right]^{-1} \tag{5.14}$$

$$L_{mESC}^{g_L,g_L+1} = \frac{\mu_0}{2\pi} \ln\left(\frac{D_{g_L+1}}{D_{g_L}}\right) \tag{5.15}$$

$$L_{mESC}^{g_S,g_S+1} = \frac{\mu_0}{2\pi} \ln\left(\frac{D_{g_S+1}}{D_{g_S}}\right) \tag{5.16}$$

$$L_{kESC} = \left[(L_{kESC_L})^{-1} + (L_{kESC_S})^{-1}\right]^{-1} \tag{5.17}$$

$$L_{kESC_L} = \frac{L_k}{N_{MWCNT_L} \sum_{g=1}^{N_{sh_L}} N_{ch/sh_L}^{T_K} \lambda_{eff_L}^{T_K}} \tag{5.18}$$

$$L_{kESC_S} = \frac{L_k}{N_{MWCNT_S} \sum_{g=1}^{N_{sh_S}} N_{ch/sh_S}^{T_K} \lambda_{eff_S}^{T_K}} \tag{5.19}$$

$$L_k = \frac{h}{2e^2 v_f} \approx 16.2mH/m \tag{5.20}$$

The capacitance of MWCNT (C_{MMT}) is electrostatic capacitance (C_e), quantum capacitance (C_q) and shell-to-shell capacitance (C_s). All capacitance of individual MWCNTs have taken per unit length. [16, 138]. Moreover, total capacitance of MMT (C_{MMT}) is examined using all the capacitance of $MWCNT_L$ (C_{ESC_L}) and $MWCNT_S$ (C_{ESC_S}) as shown in Figure 3.5. These capacitance can be obtained by

$$C_{MMT} = (C_{ESC_L} N_{X_L} + C_{ESC_S} N_{X_S}) * L_i \tag{5.21}$$

$$C_{ESC_L} = \left(\left[\left(C_{q_{L(g)}}^{-1} + C_{s_{L(g-1)}}^{-1}\right)^{-1} + C_{q_L(g-1)}\right]^{-1} + C_{e_L}^{-1}\right)^{-1} \tag{5.22}$$

$$C_{ESC_S} = \left(\left[\left(C_{q_{S(g)}}^{-1} + C_{s_{S(g-1)}}^{-1}\right)^{-1} + C_{q_S(g-1)}\right]^{-1} + C_{e_S}^{-1}\right)^{-1} \tag{5.23}$$

where, the capacitance (C_{ESC}) of MMT consists of quantum (C_q), electrostatic (C_e) and shell to shell (C_s) of individual shell of $MWCNT_L$ and $MWCNT_S$. These can be calculated by

$$C_{q(g)} = \frac{2e^2}{h} \frac{2N_g}{v_f} \tag{5.24}$$

$$C_e = \frac{2\pi\varepsilon}{cosh^{-1}(1 + h_t/D_{min_L})} \tag{5.25}$$

$$C_s = \frac{2\pi\varepsilon}{\ln(D_{g+1}/D_g)} \tag{5.26}$$

D_{g+1} and D_g are outer- and inner-most diameters of adjacent shells of MWCNT, respectively.

The Eqs. 5.1 to 5.26 can be used to develop ESC model of MMT bundle. The delay for ESC model of MMT is estimated by using Driver Interconnect Load (DIL) as shown in Figure 5.1, where input CMOS as driver and a load at output terminal. The estimated delay can be calculated for proposed MMT by using the expression as given below [156, 160]

$$T_d^{MMT} = \frac{2T_2^{MMT}}{\sqrt{4T_2^{MMT} - (T_1^{MMT})^2} - T_1^{MMT}} \ln \left[\frac{0.2\sqrt{4T_2^{MMT} - (T_1^{MMT})^2}}{T_1^{MMT} + \sqrt{4T_2^{MMT} - (T_1^{MMT})^2}} \right] \quad (5.27)$$

where, the T_1^{MMT} and T_2^{MMT} are calculated as following

$$\begin{aligned} T_1^{MMT} = & \left[\frac{R_S^{MMT} C_{MMT}(nx)^2}{2} + R_{d0}C_{d0} + C_{MMT}(nx)(R_a + R_{d0}) \right] \\ & + C_L[2R_a + R_{d0} + R_S^{MMT}(nx)] \end{aligned} \quad (5.28)$$

$$\begin{aligned} T_2^{MMT} = & \left(\frac{L_{MMT}C_{MMT}(nx)^2}{2} + \frac{(R_S^{MMT})^2 C_{MMT}^2 (nx)^4}{4!} \right) \\ & + \left(\frac{R_S^{MMT} C_{MMT}(nx)^2 R_{d0}C_{d0}}{2} + \frac{R_S^{MMT} C_{MMT}^2 (nx)^3 (R_a + R_{d0})}{3!} \right) \\ & + R_a R_{d0} C_{d0} C_{MMT}(nx) + C_L \left(\frac{R_S^{MMT} C_{MMT}(nx)^2}{2} (2R_a + R_{d0}) \right) \\ & + C_L \left(2R_a R_{d0} C_{d0} + \frac{(R_S^{MMT})^2 C_{MMT}(nx)^3}{3!}) + L_{MMT}(nx) \right) \\ & + C_L \left(R_a^2 C_{MMT}(nx) + R_S^{MMT} R_{d0} C_{d0}(nx) + R_a R_{d0} C_{MMT}(nx) \right) \end{aligned} \quad (5.29)$$

$$R_a = R_C + R_L^{MMT} \quad (5.30)$$

R_S^{MMT}, C_{MMT} and L_{MMT} are the scattering resistance, capacitance and inductance of ESC model for MMT nanostructure as VLSI interconnect, respectively. C_L, R_{d0} and C_{d0} are load capacitance, output resistance and capacitance of CMOS driver, respectively. R_C and $R_{L^{MMT}}$ are contact resistance and quantum resistance of MMT as VLSI interconnect. n is the number segments, which equals to the number of optimum repeaters (R_{opm}) inserted to convert lumped model in distributed model. x is the length of each segment and it calculated by dividing the total interconnect length (L_i) with calculated number of optimum repeaters (R_{opm}). [110, 137, 160] The number of optimum repeaters (R_{opm}) is inserted to convert lumped model into distributed model to achieve minimum delay and power dissipation that enhance the overall performance on interconnect line. The number of optimum repeaters (R_{opm}) can be calculated as given in upcoming section.

5.3 Repeater Insertion

The lumped model is used to estimate delay of MMT nanostructure as global level interconnect length. This thesis has presented the performance of MMT nanostructure for global interconnect at DSM technology nodes. To calculate the accurate performance of MMT, the lumped model needs to change into distributed model. The lumped model of MMT is divided into segments to develop distributed model as shown in Figure 5.5. Each segment is followed by

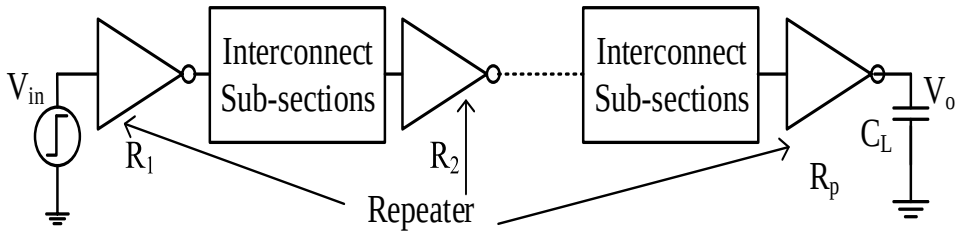


Figure 5.5: Distributed network model of MMT for p-segments. [11]

CMOS driver as shown in Figure 5.6 and each segment has fixed-size repeater. The distributed model has used number of repeater to drive each segment in this model [137, 156].

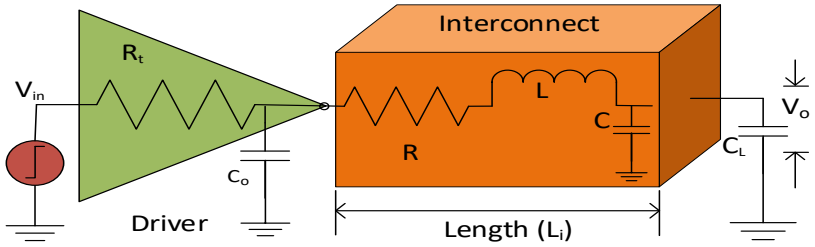


Figure 5.6: Schematic diagram for distributed network model of any p-segment.

Distributed delay model requires optimum number of repeaters and optimum-sized repeater to get desire performance such as delay and power. The number of optimum repeaters (R_{opm}) and optimum-sized repeater (S_{opt}) are given by [137]

$$S_{opt} = \sqrt{\frac{R_{d0}C_{MMT}}{C_{d0}R_{MMT}}[1 + 0.18(T_{L/R})^3]^{-0.26}} \tag{5.31}$$

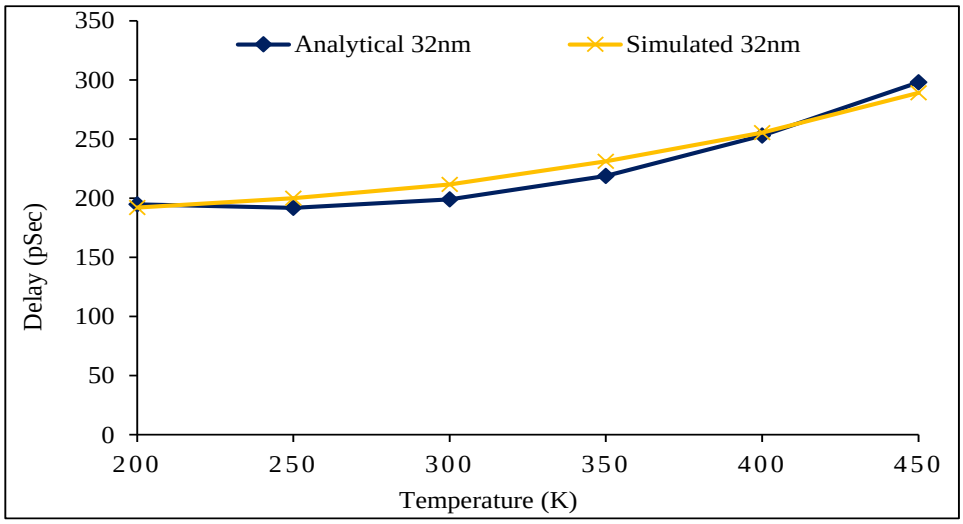
$$R_{opm} = int\left[\sqrt{\frac{R_{MMT}C_{MMT}}{2R_{d0}C_{d0}}[1 + \beta(T_{L/R})^3]^{-0.28}}\right] - 1 \tag{5.32}$$

$$T_{L/R} = \sqrt{\frac{L_{MMT}}{R_{MMT}R_{d0}C_{d0}}} \tag{5.33}$$

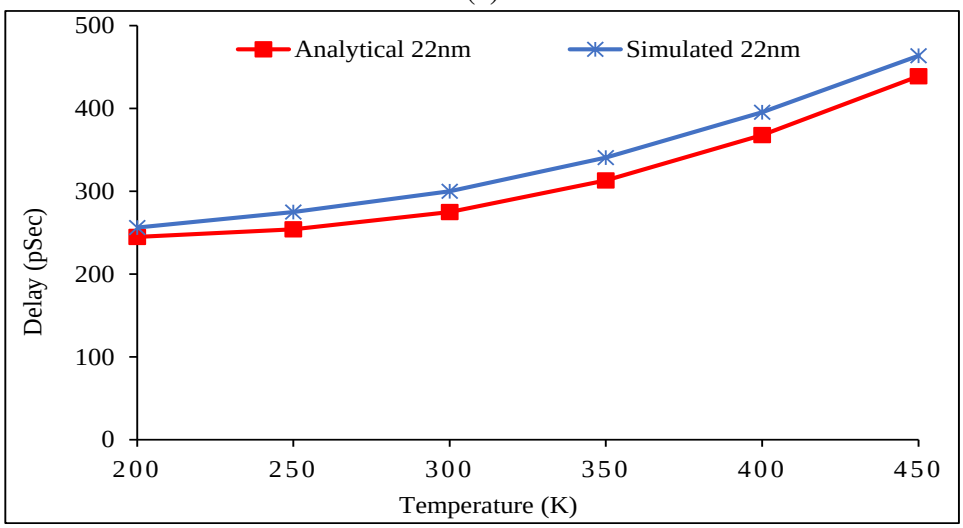
where, β is the fitting co-efficient and taken as ranging from 0.21 to 0.28 for Cu and MWCNTB interconnect [137].

5.4 Analytical delay of MMT as global interconnect

The analytical model are proposed by using the above equations, the delay of MMT nanostructure is observed for global level interconnect at 32, 22 and 16nm technology nodes on variable temperature ranging from 200 to 450K. The ESC model is developed using the Eqs. 5.1 to 5.26 to estimate the impedance parameters at DSM technology nodes as 32, 22 and 16nm. The simulated parameters are considered as per ITRS-2013 to calculate the parasitic of MMT nanostructure as shown in Table 3.3. The optimum number of repeaters and optimum-sized repeaters are calculated using Eqs. 5.31 to 5.32. Therefore, the optimum delay has been obtained by writing Eqs. 5.27 to 5.30 in MATLAB. The obtained analytical delay results from mathematical calculations are compared with simulated delay results determined in Chapter 4 as shown in Figure 5.7.



(a)



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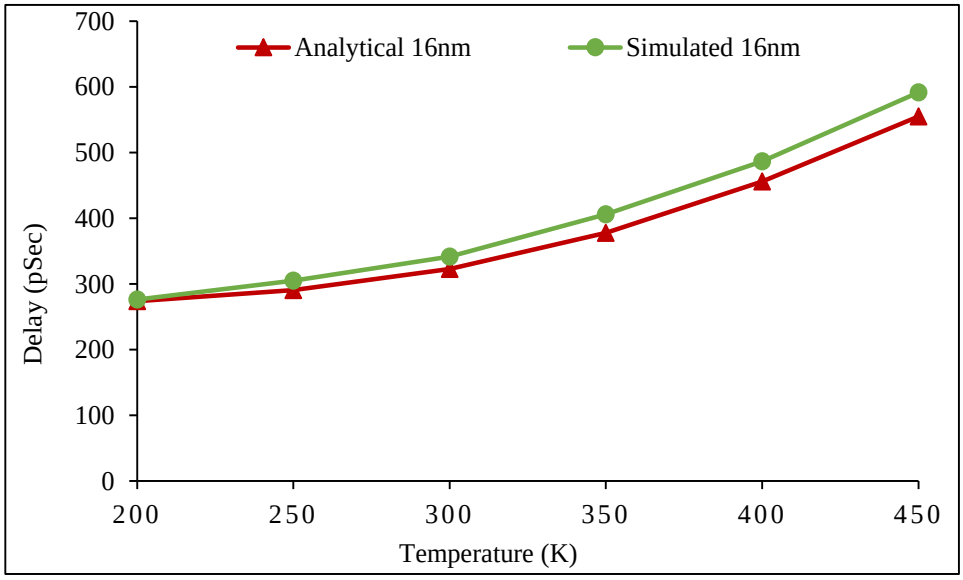
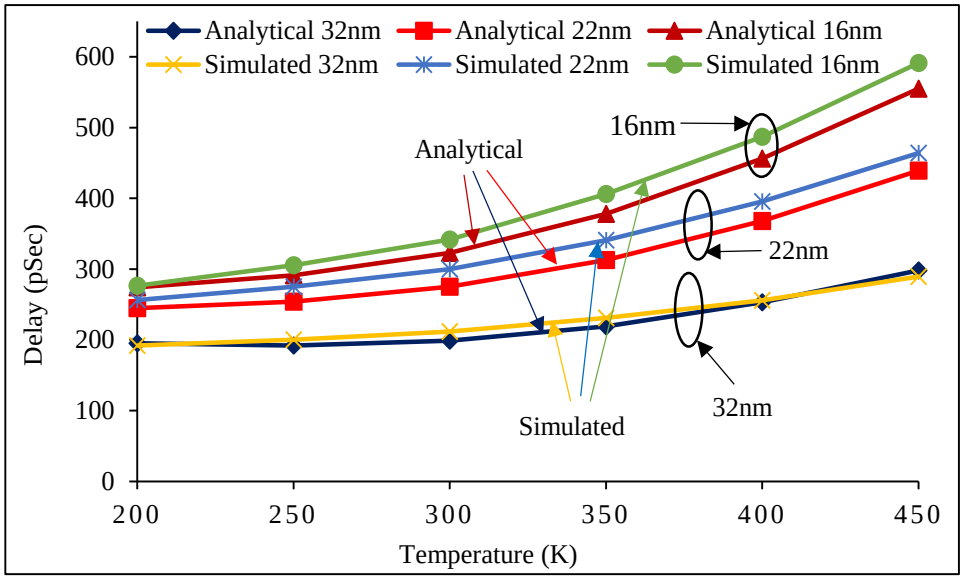


(c)



(d)

Figure 5.7: Comparison of analytical and simulated delay of MMT nanostructure for global interconnect as a function of temperature at DSM technology nodes as (a) 32, (b) 22 and (c) 16nm. (d) Combined comparison of analytical and simulated delay of MMT interconnect at DSM technology nodes.

The comparative analysis of analytical and simulated delay of MMT nanostructure is shown in Figure 5.7 for global interconnect length (1000μm) as a function of temperature (200-450K) at DSM technology nodes as (a) 32, (b) 22 and (c) 16nm. The analytical delay are increased with rising temperature ranging from 200 to 450K at all three DSM technology nodes. The comparison of analytical and simulated results show that both the results are aligned and increased with increasing temperature ranging from 200 to 450K at DSM technology nodes under consideration this work.

5.5 Analytical delay of Cu interconnect

Similarly, the analytical delay of Cu interconnect is calculated for global interconnect length at DSM technology nodes on a variable temperature ranging from 200 to 450K. The optimum number of repeaters having optimum-sized of each repeater are used for Cu interconnect as similar for MMT nanostructure. The analytical delay is calculated for Cu interconnect by using the following equation [160]

$$T_d^{Cu} = \frac{2T_2^{Cu}}{\sqrt{4T_2^{Cu} - (T_1^{Cu})^2} - T_1^{Cu}} \ln\left[\frac{0.2\sqrt{4T_2^{Cu} - (T_1^{Cu})^2}}{T_1^{Cu} + \sqrt{4T_2^{Cu} - (T_1^{Cu})^2}}\right] \tag{5.34}$$

where, the T_1^{Cu} and T_2^{Cu} are calculated as following

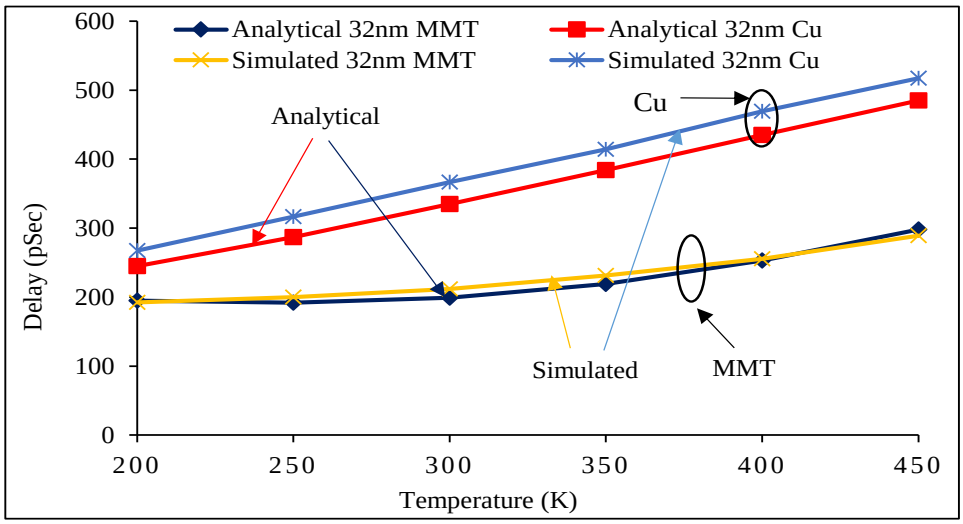
$$T_1^{Cu} = \left[\frac{R_{Cu}C_{Cu}(nx)^2}{2} + R_{d0}C_{d0} + C_{Cu}(nx)(R_{d0})\right] + C_L[R_{d0} + R_{Cu}(nx)] \tag{5.35}$$

$$\begin{aligned} T_2^{Cu} = &\left(\frac{L_{Cu}C_{Cu}(nx)^2}{2} + \frac{R_{Cu}^2C_{Cu}^2(nx)^4}{4!} + \frac{R_{Cu}C_{Cu}(nx)^2R_{d0}C_{d0}}{2}\right) \\ &+ \left(\frac{R_{Cu}C_{Cu}^2(nx)^3(R_{d0})}{3!}\right) + C_L\left(\frac{R_{Cu}C_{Cu}(nx)^2}{2}(R_{d0})\right) \\ &+ C_L\left(\frac{R_{Cu}^2C_{Cu}(nx)^3}{3!} + L_{Cu}(nx) + R_{Cu}R_{d0}C_{d0}(nx)\right) \end{aligned} \tag{5.36}$$

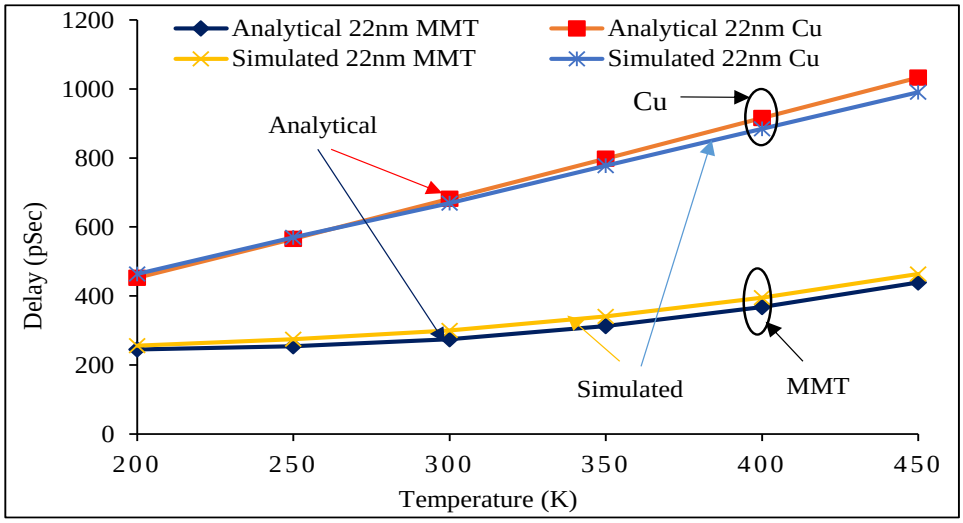
where, R_{Cu}, C_{Cu} and L_{Cu} are the temperature resistance, capacitance and inductance of ESC model for Cu as VLSI interconnect, respectively. The calculated analytical delay of Cu as global level interconnect length (1000μm) for temperature ranging from 200 to 450K at DSM technology nodes viz. 32, 22 and 16nm. The analytical delay results of Cu interconnect are aligned with simulated delay results for entire temperature range at DSM technology nodes under consideration for this work. The analytical and simulated delay results are increasing with increase in temperature ranging from 200 to 450K at 32, 22 and 16nm technology nodes.

5.6 Delay comparison of MMT and Cu interconnect

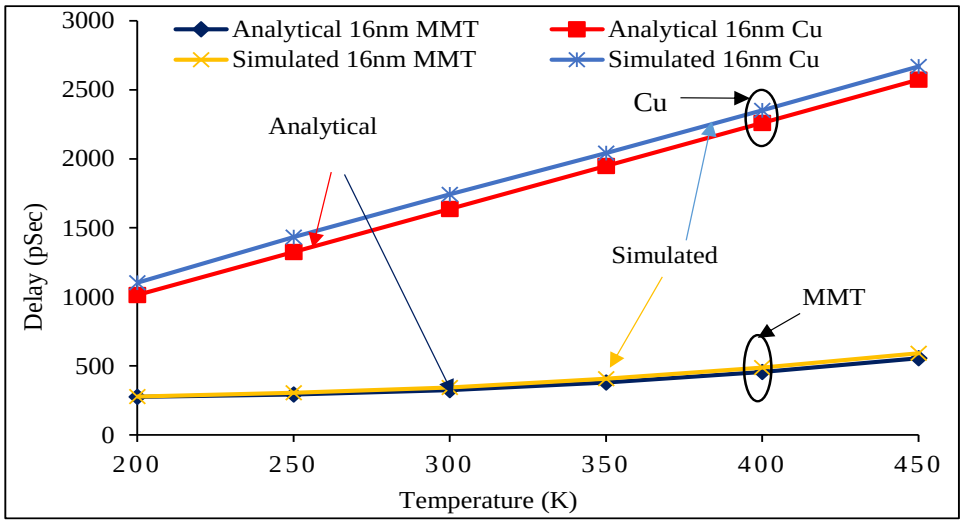
The calculated analytical delay of Cu and MMT interconnect is increased with increasing temperature ranging from 200 to 450K at DSM technology nodes viz. 32, 22 and 16nm. The comparison of analytical and simulated delay results of Cu and MMT nanostructure for global interconnect as a function of temperature at various DSM technology nodes as shown in Figure 5.8 (a) 32, (b) 22 and (c) 16nm.



(a)



(b)



(c)

Figure 5.8: Comparison of analytical and simulated delay of Cu and MMT interconnect on temperature range (200-450K) at DSM technology nodes as (a) 32, (b) 22 and (c) 16nm.

The comparison of analytical and simulated delay of Cu and MMT nanostructure as global level VLSI interconnect for variable temperature range at DSM technology nodes. It shows that the calculated delays are increased with increasing temperature ranging from 200 to 450K. The analytical delay are aligned with the simulated delay for both nanostructure used as global interconnect for various DSM technology nodes viz. 32, 22 and 16nm.

Chapter Summary

In this chapter, the temperature-dependent analytical delay model is presented for proposed MMT nanostructure and Cu as global level VLSI interconnect at DSM technology nodes. The obtained results from the analytical delay model is compared with simulated results calculated in Chapter 4. The mathematical equations are expressed to developed ESC model of MMT nanostructure for global interconnect length at DSM technology nodes. The developed ESC model is considered to examine the analytical delay of MMT nanostrcuture and Cu interconnect at various DSM technology nodes. The lumped model is divided into p-segment to develop distributed model, where each segment of distributed model is operated with optimum-sized repeater. The optimum-sized repeater and number of repeaters are calculated with the help of derived mathematical expressions in this Chapter.

Further, the analytical delay model of MMT and Cu is considered to estimate delay for global interconnect length (1000μm) as a function of temperature ranging from 200 to 450K at various DSM technology nodes (32, 22 and 16nm). The analytical delay of MMT and Cu nanostructure are compared with the simulated results at DSM technology nodes. The results of both analytical and simulated are increased with increase in temperature ranging from 200 to 450K at 32, 22 and 16nm technology nodes. The comparative analysis of analytical and simulated delay presented in the Chapter are aligned for a variable temperature range at DSM technology nodes under consideration for this work.

Chapter 6

Temperature Dependent Performance Analysis of MMT, Cu, SWCNTB and MWCNTB Interconnects

In this chapter, comparative analysis of temperature-dependent performance of Mixed-MWCNT (MMT) nanostructure with MWCNTB, SWCNTB and Cu interconnects are presented in terms of resistance, delay, power and PDP at 32, 22 and 16nm technology nodes. Temperature-dependent performance of MMT nanostructure is calculated and analysed for 32, 22 and 16nm technology nodes in Chapter 4. The temperature-dependent equivalent single conductor (ESC) models of MWCNTB, SWCNTB and Cu nanostructure are also presented for DSM technology nodes at global interconnect length (1000μm). These models are considered to calculate the temperature-dependent parasitic for global interconnect length at various technology nodes.

The obtained impedance parameters in terms of resistance for MWCNTB, SWCNTB and Cu are compared with the calculated resistance of MMT as given in Chapter 4. Further, the parasitic of MWCNTB, SWCNTB and Cu interconnects are simulated with the help of SPICE tool to examine the performance in terms of delay, power and PDP. The calculated temperature-dependent performance of MMT nanostructure as given in Chapter 4 are compared with obtained performance of MWCNTB, SWCNTB and Cu in this chapter. The comparative analysis are presented for variable temperature ranging from 200 to 450K at DSM technology nodes i.e. 32, 22 and 16nm.

6.1 Temperature-dependent ESC models of Cu, SWCNTB and MWCNTB

Temperature-dependent ESC models are developed for Cu, SWCNTB and MWCNTB nanostructures as VLSI interconnects in this section. In the literature, various thermally-aware impedance models for MWCNTB, SWCNTB and Cu are available as VLSI interconnect [66,

97, 121, 126, 145]. Temperature-dependent ESC models for MWCNTB, SWCNTB and Cu as global interconnect are developed with the help of literature as a function of temperature range between 200 and 450K at 32, 22 and 16nm technology nodes. Further, these models are considered to examine performance of VLSI interconnect at DSM technology nodes. The obtained results from these models are compared with MMT nanostructure.

6.1.1 Temperature-dependent ESC model of Cu interconnects

This section presents temperature-dependent parasitic of Cu to develop ESC model for global interconnect (1000µm) at DSM technology nodes viz. 32, 22 and 16nm. Then, this ESC model is considered to evaluate performance in terms of delay, power and PDP for a variable temperature ranging from 200 to 450K. The parasitic of Cu depend upon a cross-sectional area, length of interconnect and its resistivity and all these parameters are taken as per ITRS-2013. The structure of Cu interconnect is presented with various dimensions as height (H), width (W) and length (L_i) of interconnect at the ground plane as shown in Figure 6.1.

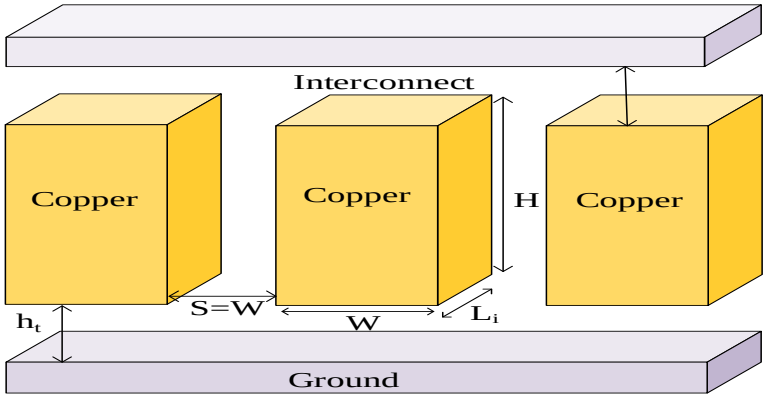


Figure 6.1: Structure of Cu as VLSI interconnects at the ground plane.

The temperature-dependent resistance of Cu as global level VLSI interconnect can be calculated by the following equation

$$R_{Cu} = \rho_T \frac{L_i}{HW} \tag{6.1}$$

where, ρ_T, L_i, H and W are temperature-dependent resistivity, length, height and width of Cu interconnect, respectively.

The temperature-dependent resistivity (ρ_T) for Cu interconnect can be calculated as

$$\rho_T = \rho_0[1 + 0.004(T_K - T_0)] \tag{6.2}$$

where, ρ_0, T_0 and T_K are technology dependent resistivity of Cu material at room temperature, room temperature as 300K and variable temperature ranging from 200 to 450K, respectively.

The inductance (L_{Cu}) and capacitance (C_{Cu}) of Cu material used as VLSI interconnect can be calculated by Eqs. 3.55 to 3.58 as discussed in Chapter 3. [97, 153, 154]

6.1.2 Temperature-dependent ESC model of SWCNTB

The SWCNTB is made up with number of SWCNTs having equal diameter for each SWCNT, which has diameters ranging from 1 to 10nm. The structure of SWCNTB at ground plane is shown in Figure 6.2, which considered as global VLSI interconnect with technology dependent dimensions as width(W), height (H) and length (L_i).

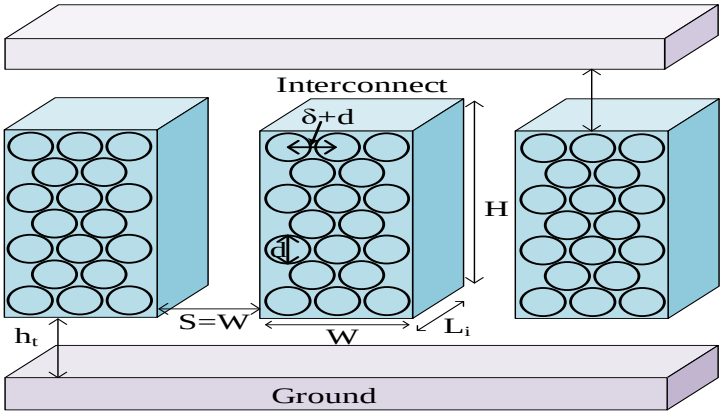


Figure 6.2: SWCNTB used as VLSI interconnects at the ground plane.

The electrical equivalent circuit (EEC) model is developed for individual SWCNT of the SWCNTB as global interconnect length as shown in Figure 6.3. EEC model is used to develop ESC model for SWCNTB by considering each SWCNT to be parallel and assuming each SWCNT is participated in conduction. The ESC model of the SWCNTB are used to calculate temperature-dependent parasitic as inductance, resistance and capacitance. Temperature-dependent ESC model of SWCNTB for global level interconnect length (1000μm) is used to evaluate the performance in terms of delay, power and PDP for DSM technology nodes viz. 32, 22 and 16nm.

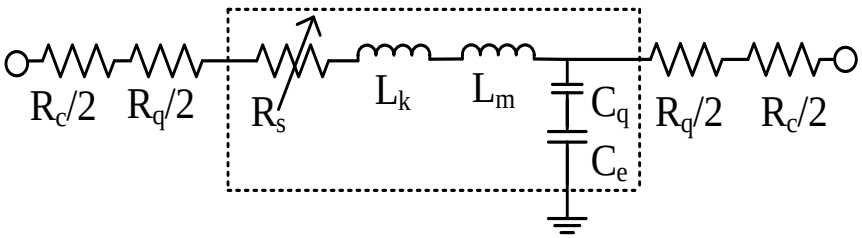


Figure 6.3: EEC model of an individual SWCNT of the SWCNTB.

The number of SWCNTs (N_{SWCNT}) in a bundle is calculated by computing the number of SWCNTs in rows (N_X) and columns (N_Y). The gap between adjacent SWCNTs is taken as 0.34nm and the distance between center of two SWCNTs denotes as $\delta + d$. The number of SWCNTs are calculated differently for even and an odd number of rows of the bundle. These can be calculated using the following equations [134]

$$N_{SWCNT} = N_X N_Y - 0.5(N_Y) \qquad \text{for even number of rows} \tag{6.3}$$

$$N_{SWCNT} = N_X N_Y - 0.5(N_Y - 1) \qquad \text{for an odd number of rows} \tag{6.4}$$

where, N_X and N_Y can be examined with the help of following equations

$$N_X = \frac{W - d}{\delta + d} \tag{6.5}$$

$$N_Y = \frac{H - d}{0.866(\delta + d)} + 1 \tag{6.6}$$

The resistance of SWCNT (R_{SWCNT}) consists of quantum resistance (R_q), scattering resistance (R_S) and contact resistance (R_c). R_c occurs due to imperfect contact between the metal and SWCNT shells of the SWCNTB, which is considered as $2k\Omega$ for this research work. R_q occurs due to quantum confinement of electron in nanowire and estimated as $6.45k\Omega$ for individual SWCNT. R_S is length dependent scattering resistance and arises when length of SWCNT is longer than its MFP. Further, the parasitic like resistance (R_{ESC}^{SWCNT}), inductance (L_{ESC}^{SWCNT}) and capacitance (C_{ESC}^{SWCNT}) of SWCNTB can be calculated by following equation [134]

$$R_{ESC}^{SWCNTB} = \frac{R_c + \frac{h}{2e^2}\frac{1}{N_{ch/sh}^{T_K}}(1 + \frac{L_i}{\lambda_{eff}^{T_K}})}{N_{SWCNT}} \tag{6.7}$$

where, h, e $N_{ch/sh}^{T_K}$ and $\lambda_{eff}^{T_K}$ are plank's constant, electron charge, number of channel per SWCNT and effective MFP (obtained by Eqs. 4.9 - 4.14 as mentioned in Chapter 4), respectively.

The inductance (L_{ESC}^{SWCNTB}) of SWCNTB nanostructure has magnetic (L_M) and kinetic (L_k) inductance. L_{ESC}^{SWCNTB} can be calculated by following equation

$$L_{ESC}^{SWCNTB} = \frac{L_M + L_k}{4N_{SWCNT}} \tag{6.8}$$

where, L_M, L_k and N_SWCNT can be calculated according to published article [132].

The capacitance (C_{ESC}^{SWCNTB}) of SWCNTB nanostructure as VLSI interconnect comprises as quantum capacitance (C_Q) and electrostatic Capacitance (C_E), which can be obtained as

$$C_{ESC}^{SWCNTB} = \frac{C_E C_Q}{C_E + C_Q} \tag{6.9}$$

where, C_Q and C_E can be calculated as

$$C_Q = 2\left(\frac{2\pi\varepsilon_{ox}\varepsilon_0}{lnS/d}\right) \tag{6.10}$$

$$C_E = 2\left(\frac{2e^2}{hv_f}\right) N_{SWCNT} \tag{6.11}$$

v_f, S and h are the fermi velocity, separation gap between the adjacent SWCNTB interconnect and plank's constant, respectively [127, 131, 134].

6.1.3 Temperature-dependent ESC Model of MWCNTB

The nanostructure of the MWCNTB is used as a global interconnect as shown in Figure 6.4. The parasitic are considered to develop ESC model of MWCNTB interconnect length (1000μm) under a variable temperature (200 to 450K) at DSM technology nodes. Further, it is used to observe performance in terms of delay, power and PDP.

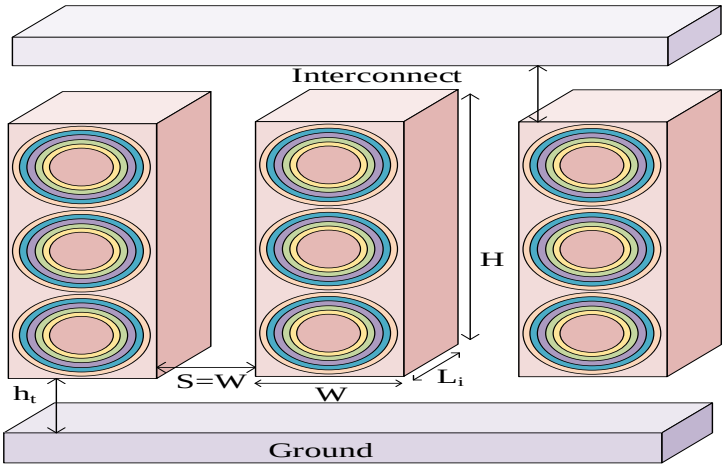


Figure 6.4: The nanostructure of MWCNTB as global level interconnect.

Number of MWCNTs (N_{MWCNT}) in MWCNTB can be calculated [97]. Number of shells (N_{sh}) of an individual MWCNT and total conducting channels in MWCNTB ($N_{total-ch}^{MWCNTB}$)

can be calculated by following equations [126]

$$N_{sh} = 1 + round\left(\frac{D_{min}}{2\delta}\right) \tag{6.12}$$

$$N_{total-ch}^{MWCNTB} = N_{MWCNT}\sum_{i=1}^{N_{sh}} N_{ch/sh}^{T_K} \tag{6.13}$$

Temperature-dependent parasitic of an MWCNTB interconnect are examined as resistance (R_{ESC}^{MWCNTB}), inductance (L_{ESC}^{MWCNTB}) and capacitance (C_{ESC}^{MWCNTB}), which can be calculated by the following equations [129]

$$R_{ESC}^{MWCNTB} = R_c + R_q^{MWCNTB} + R_S^{MWCNTB}L_i \tag{6.14}$$

$$R_q^{MWCNTB} = \frac{h}{2e^2}\frac{1}{N_{total-ch}^{MWCNTB}} \tag{6.15}$$

$$R_S^{MWCNTB} = \frac{h}{2e^2}\frac{1}{N_{MWCNTB}\sum_{i=1}^{N_{sh}} N_{ch/sh}^{T_K}\lambda_{eff}^{T_K}} \tag{6.16}$$

$$L_{ESC}^{MWCNTB} = (\frac{h}{2e^2}\frac{1}{2v_f N_{total-ch}^{MWCNTB}})L_i \tag{6.17}$$

$$C_{ESC}^{MWCNTB} = (C_{ESC}N_X)L_i \tag{6.18}$$

where, effective MFP ($\lambda_{eff}^{T_K}$) of an individual shell of MWCNT is given by the equations (Eqs. 4.9 to 4.14) [126, 127, 129, 133].

6.2 Comparison of temperature-dependent resistance of MMT with Cu, SWCNTB and MWCNTB nanostructures

Temperature-dependent resistance of MMT nanostructure as VLSI interconnect length 1000μm are calculated at DSM technology nodes viz. 32, 22 and 16nm for a variable temperature range 200-450K in Chapter 4. Similarly, the temperature-dependent resistance are obtained for Cu, SWCNTB and MWCNTB interconnects for the same parameters under consideration of the MMT nanostructure. The obtained results of Cu, SWCNTB and MWCNTB are compared to results of MMT nanostructure. Comparative analysis of performance in terms of resistance is presented at DSM technology nodes for a variable temperature conditions in the upcoming sub-sections.

6.2.1 Temperature-dependent resistance of the MMT and Cu interconnect

The comparison of temperature-dependent resistance of MMT and Cu as global level VLSI interconnect. The cross-sectional dimensions of VLSI interconnect for DSM technology nodes are considered as predicted by International Technology Roadmap for Semiconductors (ITRS version 2013) as shown in Table 3.1. The resistance of proposed MMT nanostructure and Cu as VLSI interconnect is calculated using Eqs 4.4 to 4.8 and Eqs 6.1 to 6.2, respectively. The resistance is calculated for a global interconnect length (1000μm) for temperature ranging from 200 to 450K at different technology nodes, i.e., 32, 22 and 16nm.

The temperature-dependent resistance of the MMT nanostructure depends on the MFPs of the individual shells of MWCNT. Effective MFP of an individual shell is calculated using the Eqs. 4.10 to 4.14. The MFP is declined with increased temperature range (from 200-450K). All individual shells of MMT nanostructure are assumed to be parallel to form MCTL as shown in Figure 4.4 in Chapter 4. The number of shells in MMT and their conducting channels are determined by using the Eqs. 3.1 to 3.11 in Chapter 3. The capacitance and inductance of MMT are calculated by the Eqs. 3.32 to 3.53 as presented in Chapter 3. From the MCTL, a temperature-dependent EMC model of the MMT nanostructure as a global interconnect is developed as presented in Figure 4.5(a). Finally, the ESC model is established for MMT nanostructure as global level interconnect as shown in Figure 4.5(b).

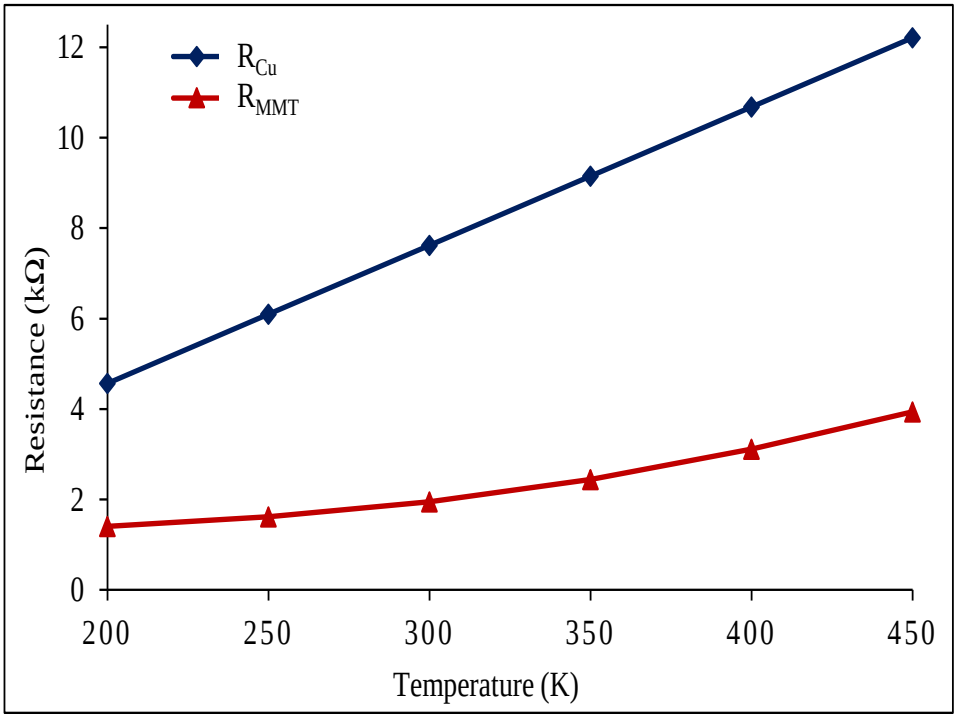
The temperature-dependent resistance of Cu and MMT interconnect, and their difference ($R_{Cu}-R_{MMT}$) are shown in Table 6.1 for DSM technology nodes. Temperature-dependent resistance of MMT and Cu as global VLSI interconnect is presented at DSM technology nodes 32, 22 and 16nm as shown in Figure 6.5 (a), (b) and (c), respectively. The combined comparison of resistance at various DSM technology nodes as shown in Figure 6.5(d) on a logarithmic scale.

The resistance of Cu and MMT interconnect is increasing with increased temperature range (200-450K) for DSM technology nodes. The resistance of Cu and MMT nanostructure is increasing due to increase in scattering phenomena. The impact of scattering phenomena is increased with increase in temperature that decreases the MFP. The MFP of Cu interconnect is smaller as 40nm for DSM technology nodes below 45nm as compared to MMT. The resistance is inversely proportional to MFP, which is decreasing with increase in temperature. The difference ($R_{Cu} - R_{MMT}$) of resistance is higher for a temperature 450K than 200K at

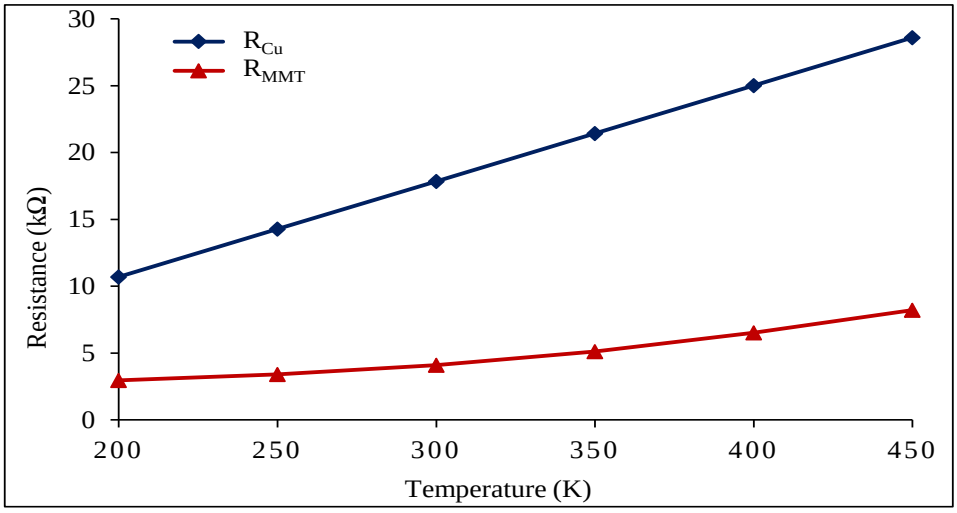
DSM technology nodes. The resistance of both nanostructure is increasing with decreased in technology nodes from 32 to 16nm.

Table 6.1: Resistance of Cu, MMT interconnect and their difference in kΩ.

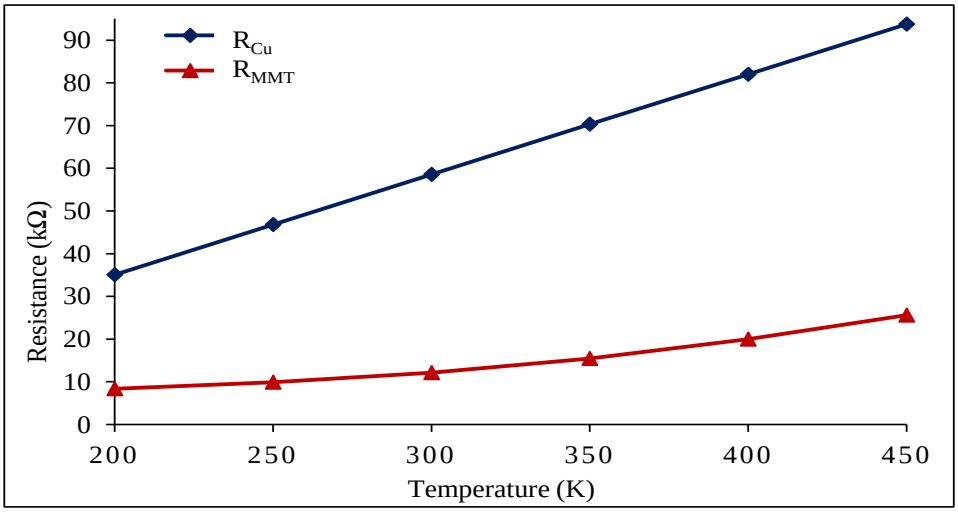
Technology nodes	Material	Temperature (K)					
		200	250	300	350	400	450
32nm	R_{Cu}	4.57	6.10	7.63	9.15	10.68	12.21
	R_{MMT}	1.41	1.62	1.95	2.44	3.12	3.94
	$R_{Cu} - R_{MMT}$	3.16	4.48	5.68	6.71	7.57	8.27
22nm	R_{Cu}	10.70	14.28	17.86	21.44	25.02	28.60
	R_{MMT}	2.96	3.40	4.09	5.13	6.52	8.22
	$R_{Cu} - R_{MMT}$	7.74	10.87	13.76	16.31	18.50	20.38
16nm	R_{Cu}	35.07	46.80	58.54	70.28	82.01	93.75
	R_{MMT}	8.39	9.88	12.12	15.46	19.99	25.57
	$R_{Cu} - R_{MMT}$	26.68	36.93	46.42	54.82	62.02	68.18



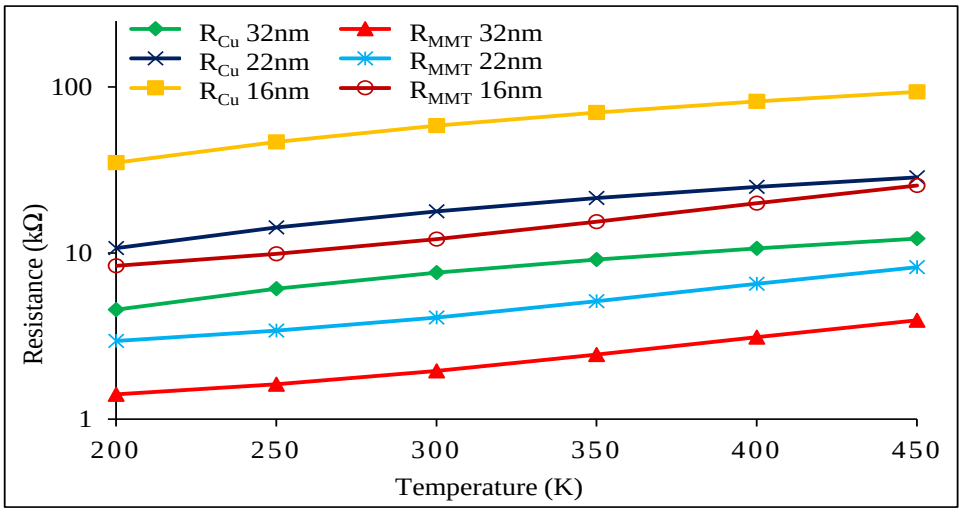
(a)



(b)



(c)



(d)

Figure 6.5: Temperature-dependent resistance of MMT and Cu interconnect at DSM technology nodes as (a) 32, (b) 22 and (c) 16nm on a linear scale. (d) The combined comparison of resistance at DSM technology nodes on a logarithmic scale.

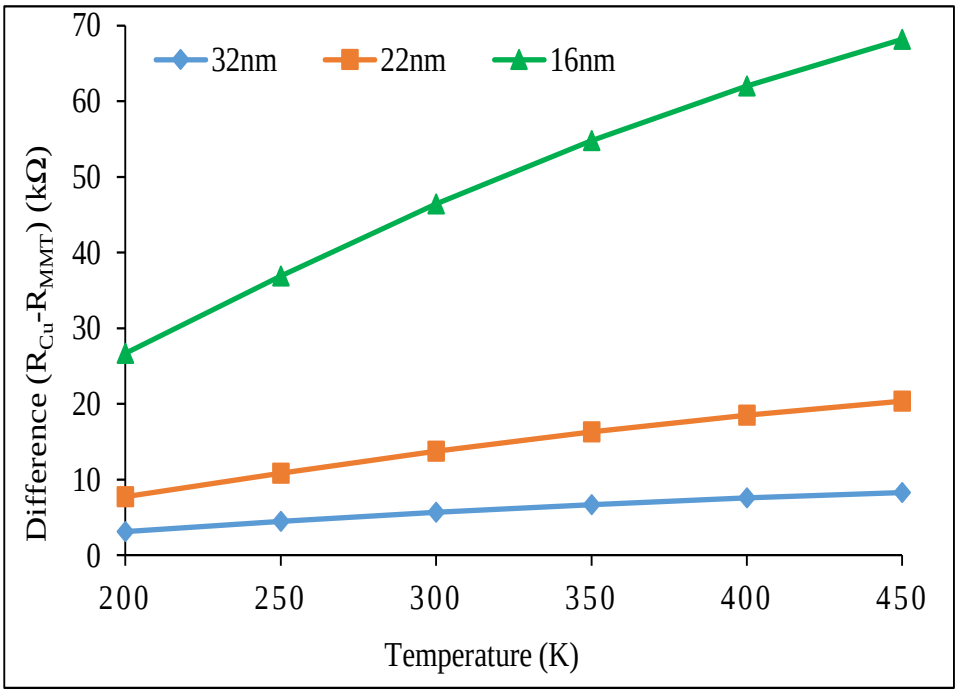


Figure 6.6: The difference of resistance ($R_{Cu} - R_{MMT}$) at DSM technology nodes.

The difference of resistance between Cu and MMT global level VLSI interconnect at DSM technology nodes as a function of temperature is shown in Figure 6.6. The difference of resistance ($R_{Cu} - R_{MMT}$) is increasing with rise in temperature ranging from 200 to 450K at DSM technology nodes as 32, 22 and 16nm as presented in Table 6.1. It reveals that temperature variations have exert a more significant impact on the resistance of Cu as compared to the MMT nanostructure, particularly at the higher temperatures and scaled-down technology nodes. The results shows that the MMT nanostructure performs better than Cu for global level VLSI interconnect in terms of resistance at DSM technology nodes viz. 32, 22 and 16nm.

6.2.2 Temperature-dependent resistance of MMT and SWCNTB

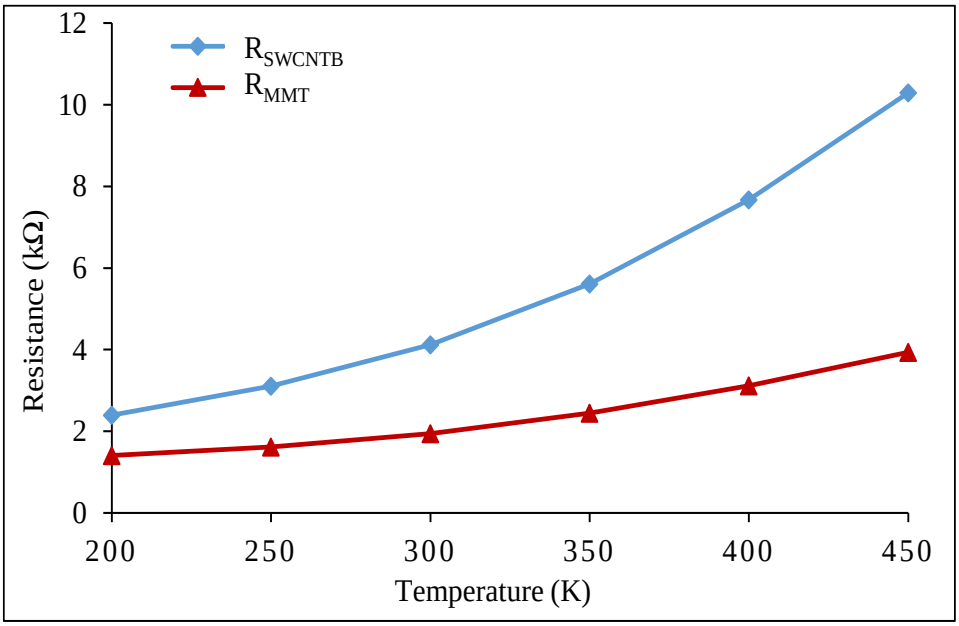
The resistance are calculated according to developed ESC model of SWCNTB interconnect as presented in previous section. The resistance of SWCNTB for VLSI interconnect is increasing with rise in temperature ranging from 200 to 450K at 32, 22 and 16nm technology nodes. The resistance of SWCNTB and MMT interconnect along with the difference ($R_{SWCNTB} - R_{MMT}$) are given in the Table 6.2.

The comparison of SWCNTB and MMT resistance is presented at DSM technology nodes as 32, 22 and 16nm as shown in Figure 6.7(a), (b) and (c), respectively. The resistance of

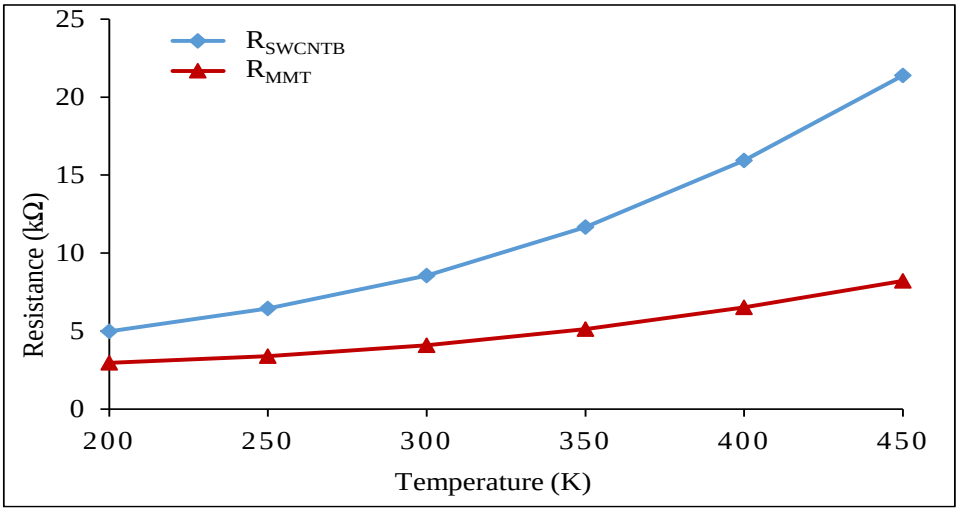
SWCNTB and MMT is increasing with increase in temperature range 200-450K, however, the resistance of SWCNTB is increasing slightly as compared to MMT for temperature above 300K at DSM technology nodes as 32, 22 and 16nm. The resistance of SWCNTB and MMT is increasing with decrease in temperature-dependent MFP due to rising scattering phenomena for a variable temperature range at DSM technology nodes. The combined resistance of SWCNTB and MMT is presented for global interconnect at various DSM technology nodes as shown in Figure 6.7(d).

Table 6.2: Resistance of SWCNTB, MMT interconnect and their differences in kΩ.

Technology nodes	Material	Temperature (K)					
		200	250	300	350	400	450
32nm	R_{SWCNTB}	2.40	3.10	4.12	5.62	7.67	10.29
	R_{MMT}	1.41	1.62	1.95	2.44	3.12	3.94
	$R_{SWCNTB} - R_{MMT}$	0.99	1.48	2.17	3.17	4.55	6.35
22nm	R_{SWCNTB}	4.99	6.45	8.57	11.67	15.94	21.39
	R_{MMT}	2.96	3.40	4.09	5.13	6.52	8.22
	$R_{SWCNTB} - R_{MMT}$	2.03	3.05	4.47	6.54	9.42	13.17
16nm	R_{SWCNTB}	12.49	16.16	21.46	29.23	39.92	53.57
	R_{MMT}	8.39	9.88	12.12	15.46	19.99	25.57
	$R_{SWCNTB} - R_{MMT}$	4.10	6.28	9.34	13.76	19.93	28.00



(a)



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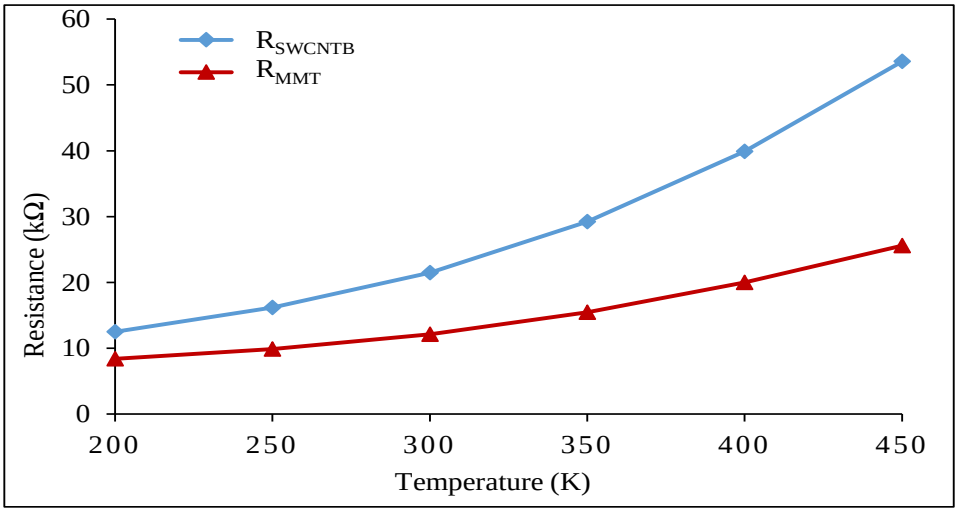

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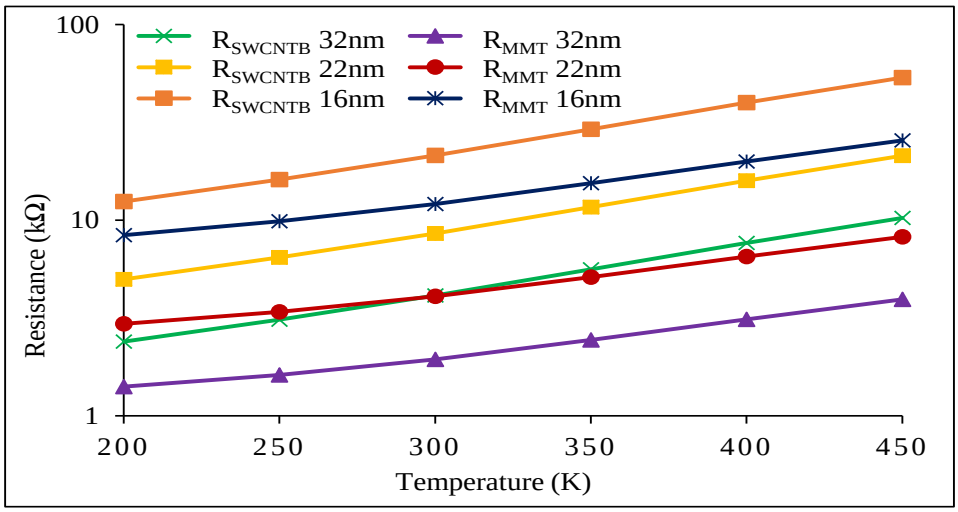


(d)

Figure 6.7: The comparison of resistance of SWCNTB and MMT at DSM technology nodes as (a) 32, (b) 22 and (c) 16nm on a linear scale. (d) Comparison of combined resistance for 32, 22 and 16nm on a logarithmic scale.

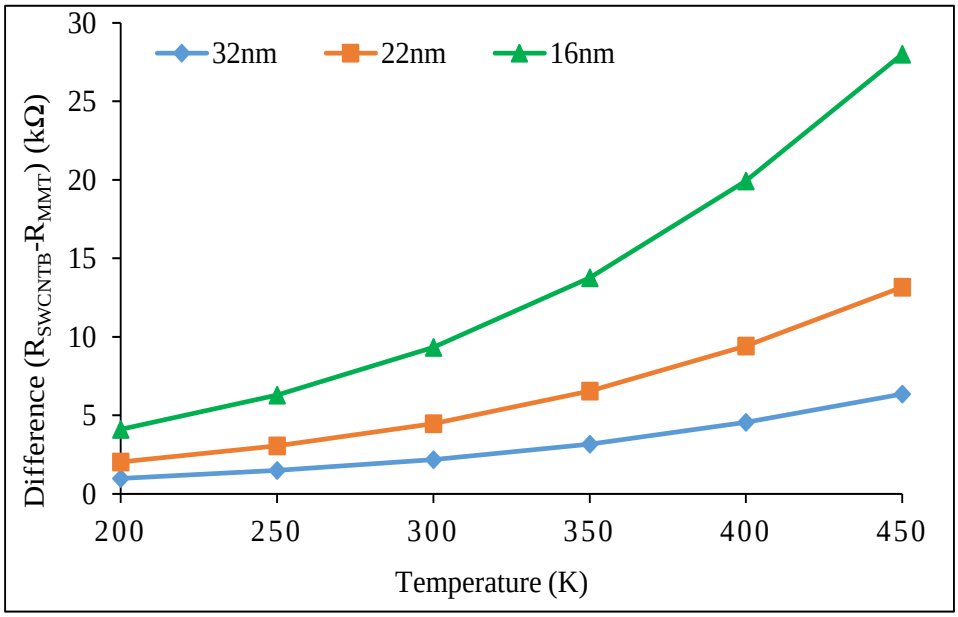


Figure 6.8: The difference of resistance ($R_{SWCNTB} - R_{MMT}$) at DSM technology nodes.

Further, the difference between the resistance of SWCNTB and MMT are also examined as shown in Figure 6.8 at 32, 22 and 16nm technology nodes. The difference ($R_{SWCNTB} - R_{MMT}$) of resistance is increasing with increased temperature ranging from 200 to 450K at all three technology nodes. The difference between the resistance of SWCNTB and MMT interconnect increased sharply for temperature greater than 300K. The impact of temperature is higher on the SWCNTB as compared to MMT at temperature 450K. It reveals that the impact of temperature on the resistance of SWCNTB is greater than MMT nanostructure at 32, 22 and 16nm technology nodes. It shows that the temperature-dependent resistance of SWCNTB are affected more as compared to the MMT nanostructure at a higher temperature range (300-450K). It concludes that the MMT nanostructure is better candidate than SWCNTB as VLSI interconnect at DSM technology nodes for a variable temperature range.

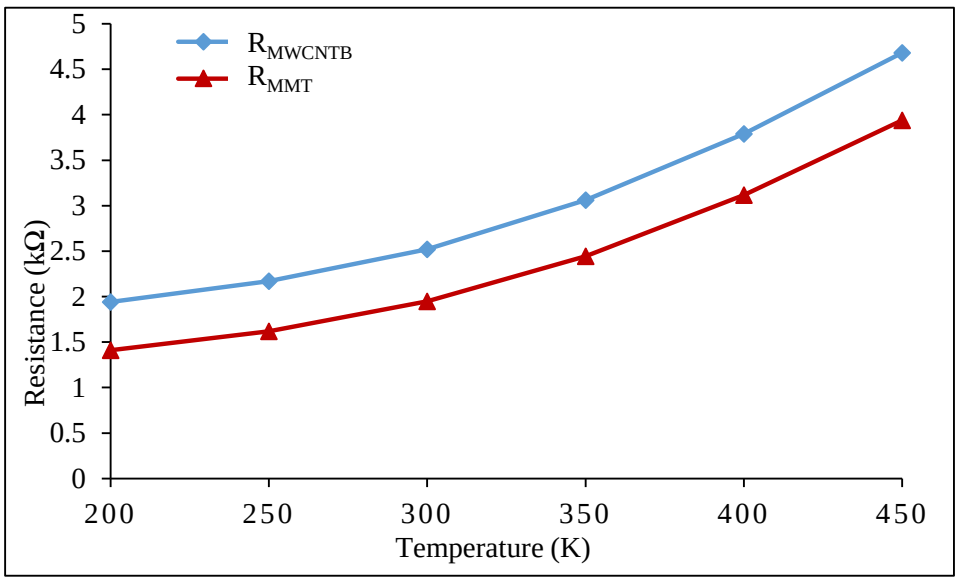
6.2.3 Temperature-dependent resistance of MMT and MWCNTB nanostrcuture

The resistance of MWCNTB and MMT as a function of temperature are obtained for global interconnect length (1000μm) at DSM technology nodes. The resistance of MWCNTB increases with rising temperature from 200 to 450K and increases with scale-down technology nodes from 32 to 16nm. The resistance are calculated using developed ESC model of MWCNTB interconnect at DSM technology nodes for a variable temperature range as given in Table 6.3.

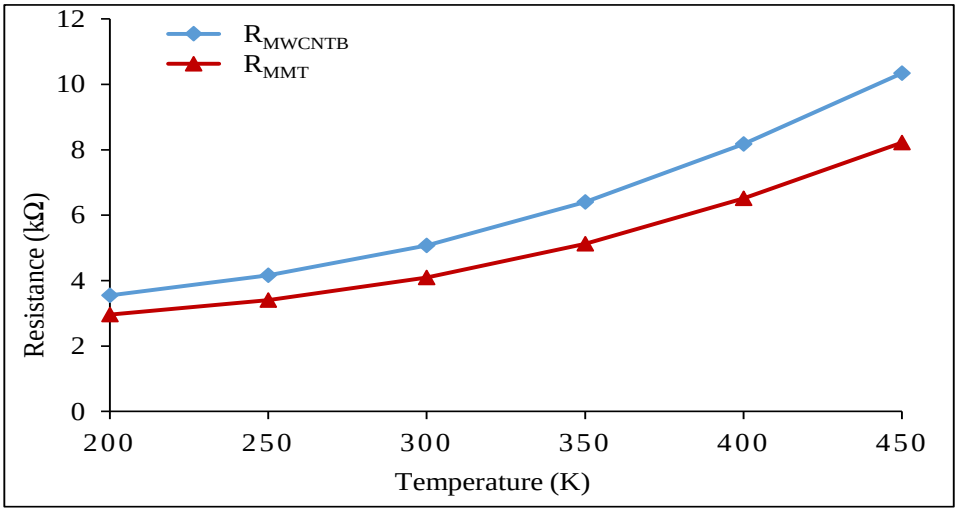
Table 6.3: Resistance of MWCNTB, MMT and their differences in kΩ.

Technology nodes	Material	Temperature (K)					
		200	250	300	350	400	450
32nm	R_{MWCNTB}	1.94	2.17	2.52	3.06	3.79	4.68
	R_{MMT}	1.41	1.62	1.95	2.44	3.12	3.94
	$R_{MWCNTB} - R_{MMT}$	0.53	0.55	0.57	0.62	0.67	0.74
22nm	R_{MWCNTB}	3.55	4.16	5.07	6.40	8.18	10.34
	R_{MMT}	2.96	3.40	4.09	5.13	6.52	8.22
	$R_{MWCNTB} - R_{MMT}$	0.59	0.76	0.98	1.27	1.66	2.12
16nm	R_{MWCNTB}	9.16	10.87	13.35	16.98	21.84	27.84
	R_{MMT}	8.39	9.88	12.12	15.46	19.99	25.57
	$R_{MWCNTB} - R_{MMT}$	0.77	0.99	1.23	1.52	1.85	2.27

The resistance of MWCNTB interconnect is increasing with increase in temperature ranging from 200 to 450K at DSM technology nodes. The resistance of MWCNTB and MMT nanostructure depends on the MFP, which is inversely proportional to the resistance. The MFP of MWCNTB and MMT nanostructure decreases because scattering of electron and phonon is increasing with rising temperature range 200-450K at DSM technology nodes. The The comparison of resistance of MWCNTB and MMT nanostructure at DSM technology nodes are shown in Figure 6.9 (a) 32, (b) 22 and (c) 16nm.



(a)



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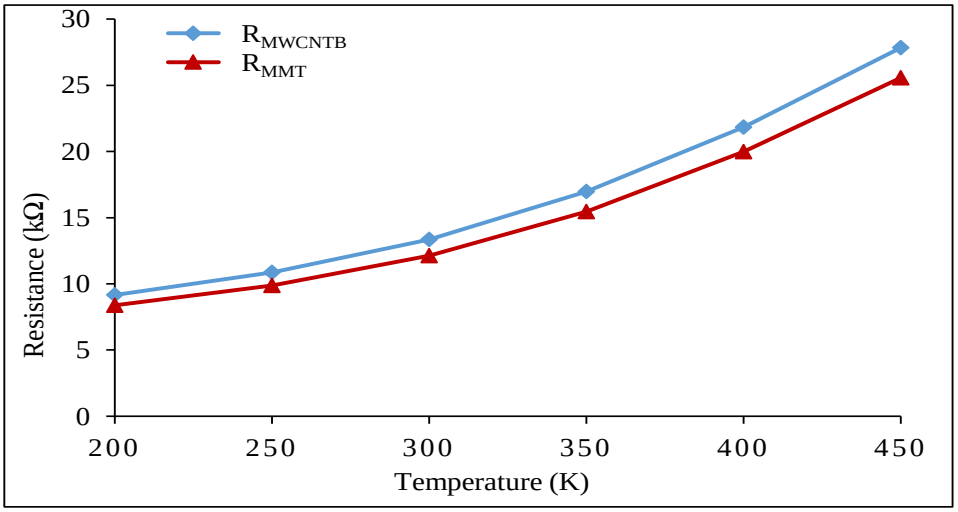
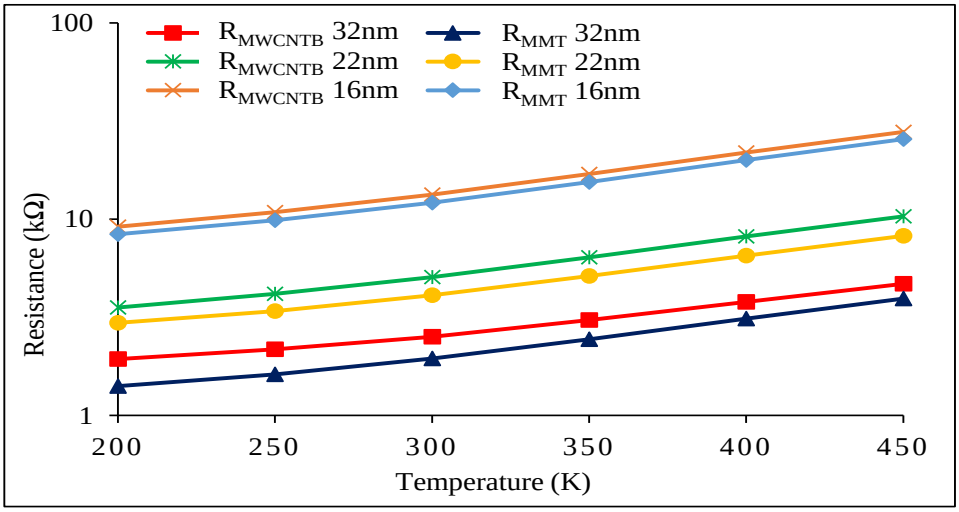


(c)



(d)

Figure 6.9: Temperature-dependent resistance of MWCNTB and MMT at DSM technology nodes as (a) 32, (b) 22 and (c) 16nm on a linear scale. (d) The combined resistance of MWCNTB and MMT at 32, 22 and 16nm technology nodes on a logarithmic scale.

The resistance of MWCNTB is higher as compared to MMT nanostructure for a variable temperature ranging from 200 to 450K at DSM technology nodes. The combined comparison of resistance for MWCNTB and MMT at DSM technology nodes is shown in Figure 6.9(d). The impact of temperature on resistance of MWCNTB and MMT interconnect is increasing with decreased technology nodes from 32 to 16nm.

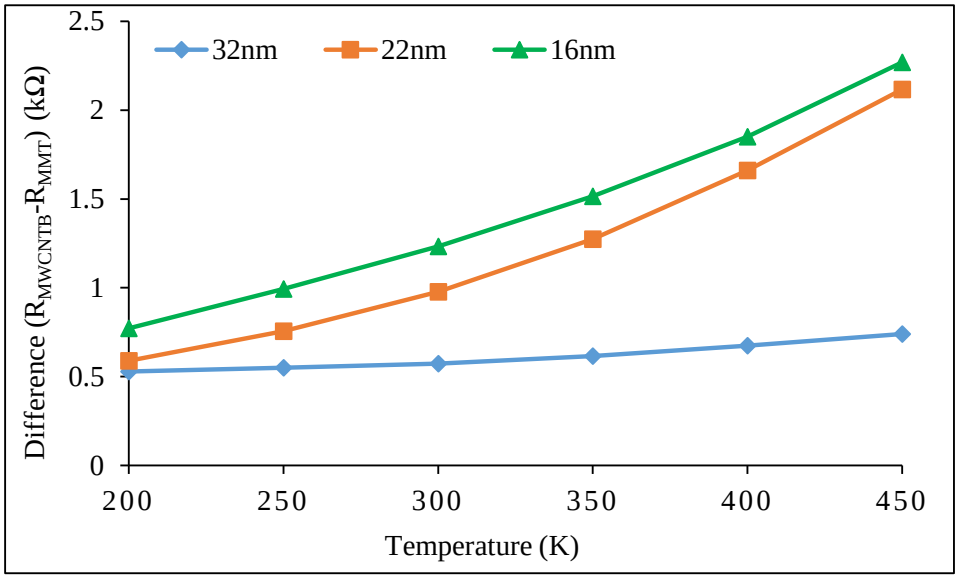


Figure 6.10: The difference of resistance ($R_{MWCNTB} - R_{MMT}$) at DSM technology nodes.

The difference of resistance ($R_{MWCNTB} - R_{MMT}$) is increasing with rise in temperature at technology nodes 22 and 16nm; however, it is very less for 32nm technology nodes as shown in Figure 6.10. Impact of temperature on resistance of MWCNTB and MMT nanostructure is more for 16nm technology nodes. The resistance of MWCNTB of increased more as compared to MMT for 22nm technology nodes as shown in Figure 6.10. It is concluded that MMT nanostrcture outperforms MWCNTB as VLSI interconnect in terms of resistance for DSM technology nodes as a function of temperature.

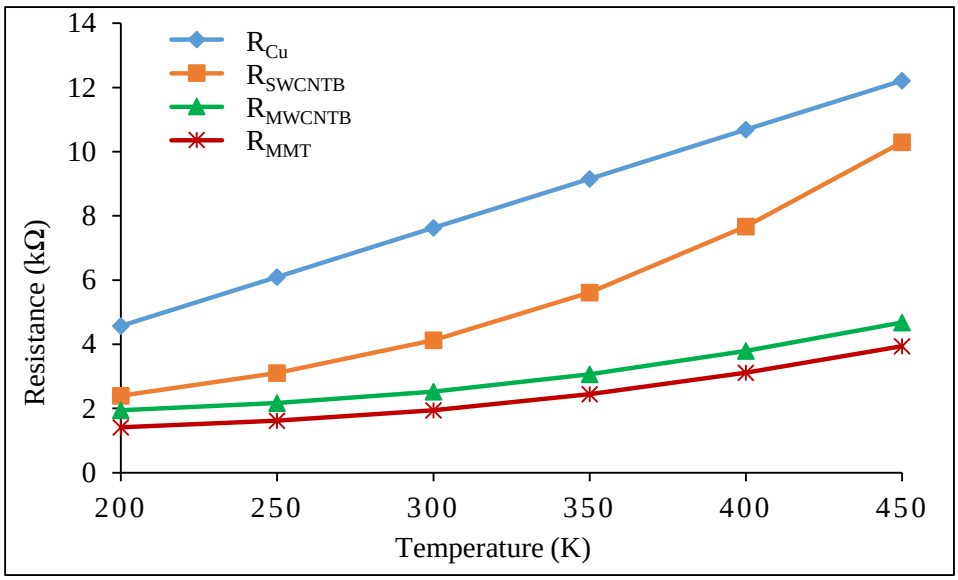
6.2.4 Comparison of temperature-dependent resistance of MMT, MWCNTB, SWCNTB and Cu interconnects

The resistance of MMT is compared to all nanostructures such as Cu, SWCNTB and MWCNTB for a variable temperature range 200-450K at DSM technology nodes viz. 32, 22 and 16nm as shown in Figure 6.11 (a), (b) and (c), respectively. Thermally-aware resistance of the MMT, MWCNTB, SWCNTB and Cu nanostructures are compared for the global interconnect length (1000µm) for DSM technology nodes as shown in Table 6.4. The resistance

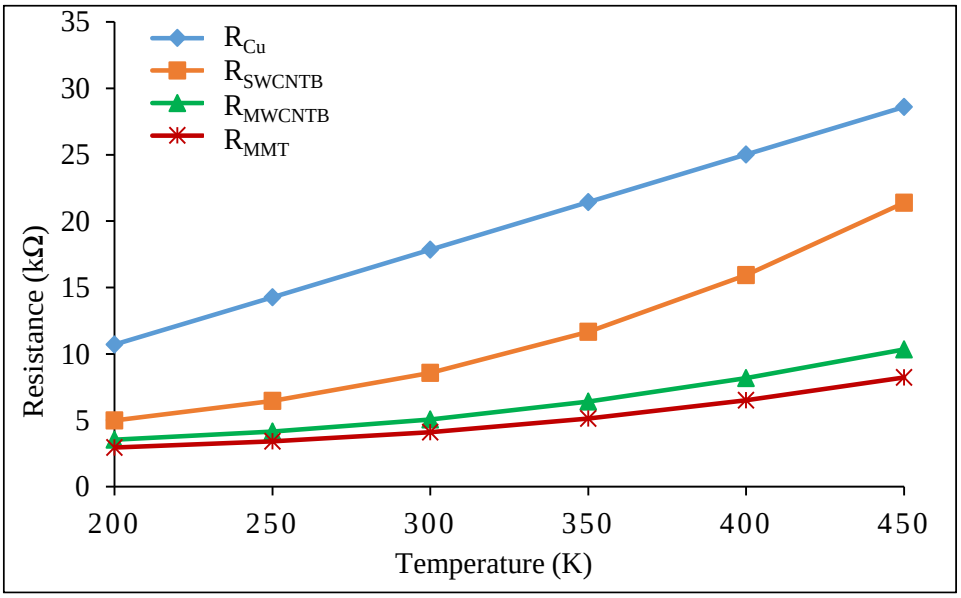
of MMT nanostructure is less as compared to Cu, SWCNTB and MWCNTB for entire temperature range 200-450K at 32, 22 and 16nm technology nodes. It is revealed that the MMT interconnect performs better than Cu, SWCNTB and MWCNTB at DSM technology nodes for VLSI interconnect.

Table 6.4: Resistance of Cu, SWCNTB, MWCNTB and MMT interconnect in kΩ.

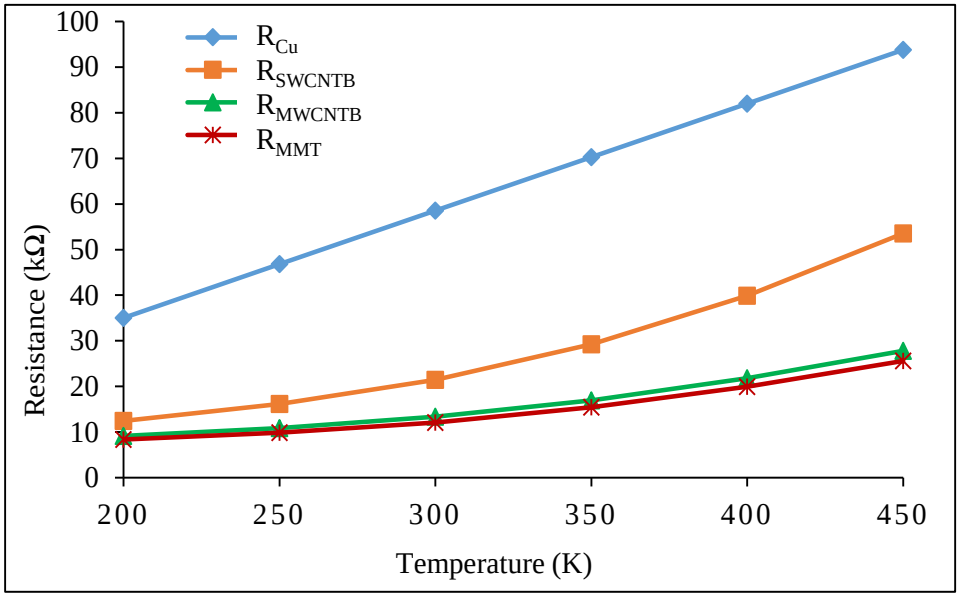
Technology nodes	Material	Temperature (K)					
		200	250	300	350	400	450
32nm	R_{Cu}	4.5674	6.096	7.625	9.154	10.683	12.211
	R_{SWCNTB}	2.3987	3.1036	4.1217	5.615	7.668	10.292
	R_{MWCNTB}	1.94	2.17	2.52	3.06	3.79	4.68
	R_{MMT}	1.4107	1.6199	1.9473	2.4438	3.1159	3.9405
22nm	R_{Cu}	10.696	14.277	17.857	21.437	25.018	28.598
	R_{SWCNTB}	4.9855	6.4506	8.5667	11.67	15.938	21.391
	R_{MWCNTB}	3.55	4.16	5.07	6.40	8.18	10.34
	R_{MMT}	2.9601	3.4049	4.0927	5.1263	6.5185	8.2224
16nm	R_{Cu}	35.065	46.802	58.54	70.28	82.01	93.75
	R_{SWCNTB}	12.486	16.155	21.455	29.228	39.916	53.572
	R_{MWCNTB}	9.16	10.87	13.35	16.98	21.84	27.84
	R_{MMT}	8.3884	9.8759	12.117	15.464	19.99	25.571



(a)



(b)



(c)

Figure 6.11: Comparison of temperature-dependent resistance of MMT, MWCNTB, SWCNTB and Cu at DSM technology nodes as (a) 32, (b) 22 and (c) 16nm.

The values of resistance get increasing with rise in temperature range for DSM technology nodes under consideration in this work. The values of resistance for the MMT nanostructures always have lower than MWCNTB, SWCNTB and Cu nanostructures. Therefore, the performance of MMT nanostructure outperforms MWCNTB, SWCNTB and Cu nanostructures as a global VLSI interconnect in terms of resistance. Accordingly, it concludes that the MMT nanostructure overtakes MWCNTB, SWCNTB and Cu as a global level VLSI interconnect length of thermally-aware environmental conditions at DSM technology nodes.

6.3 Temperature-dependent performance analysis of MMT nanostructure, Cu, SWCNTB and MWCNTB interconnects

The temperature-dependent performance of MMT nanostructure is calculated for global interconnect length at DSM technology nodes in Chapter 4. Similarly, thermally-aware ESC models of Cu, SWCNTB and MWCNTB interconnect are simulated to examine the actual performance with the help of SPICE tool at DSM technology nodes. The parasitic of ESC models are obtained with the help of MATLAB software as presented in Section 6.1. The performance of all nanostructures as VLSI interconnect is evaluated by using simulation setup, which is shown in Figure 6.12 (only single-stage). The signal is applied at input (V_{in}) and output (V_o) is taken across capacitive load (C_L). Further, the performance i.e. delay and power for distributed RLC interconnect are simulated with setup having p-segments (each segment like Figure 6.12) as shown in Figure 6.13.

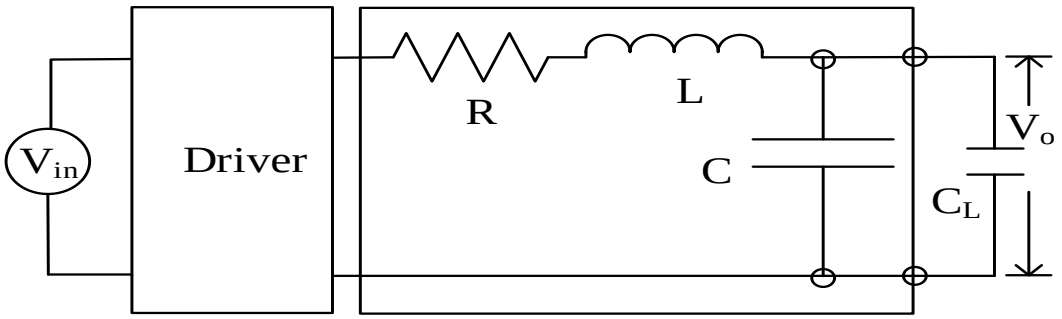


Figure 6.12: Schematic diagram of VLSI interconnect of any p-segment (only one-stage). [113]

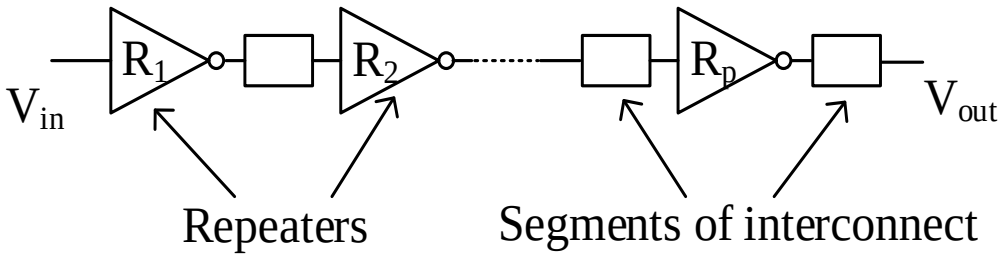


Figure 6.13: Distributed RLC interconnect model with 'p' number of repeaters. [113]

The repeaters are inserted to reduce delay and increase driving capacity [137]. The simulation parameters are considered for various DSM technology nodes as per ITRS-2013. The optimum number of repeaters, optimum size of each repeater, input signal frequency and capacitive load for various technology nodes are taken as given in Table 6.5.

Table 6.5: Simulation parameters for various technology nodes.

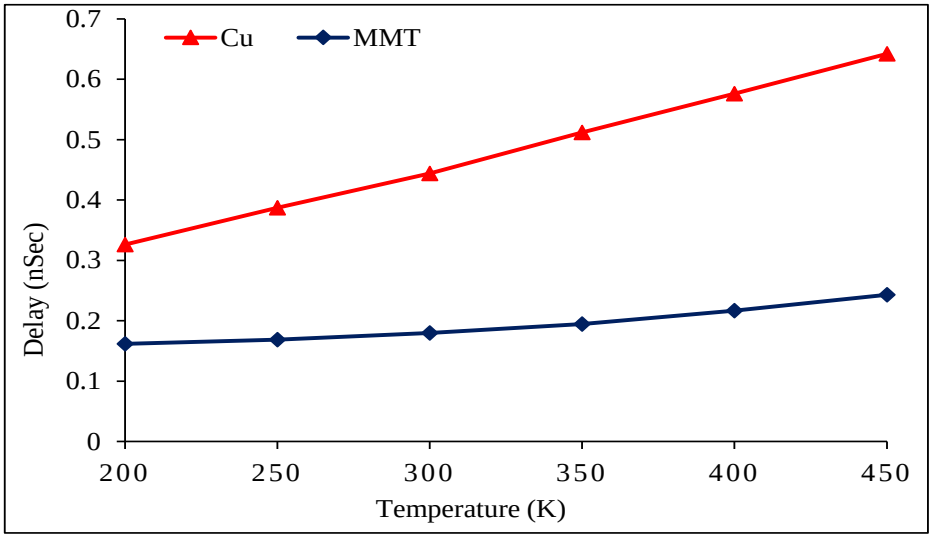
Parameters	Technology Node		
	32nm	22nm	16nm
Frequency (GHz)	0.1	0.1	0.1
Repeater size (W/L)	30	30	30
No. of repeaters	8	8	8
Capacitive Load (fF)	1	1	1

The comparative performance analysis of MMT nanostructure presents with Cu, SWCNTB, MWCNTB for global interconnect length (1000μm) at 32, 22 and 16nm technology nodes on a variable temperature range (200-450K) in upcoming sub-section.

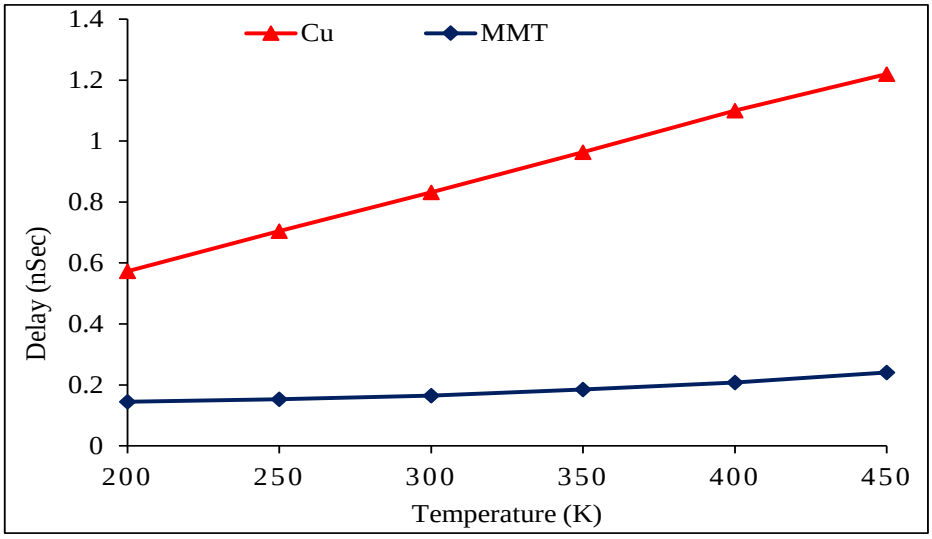
6.3.1 Temperature-dependent performance analysis of MMT and Cu interconnects

The estimated performance of MMT nanostructure in terms of delay, power and PDP are compared with Cu interconnect on a variable temperature (200-450K) at DSM technology nodes. The temperature-dependent ESC models for MMT nanostructure and Cu interconnects are presented for DSM technology nodes. Further, the obtained parasitic of MMT nanostructure and Cu interconnect using ESC models are simulated with the help of SPICE tool to examine the performance i.e. delay and power for distributed RLC model as shown in Figure 6.13.

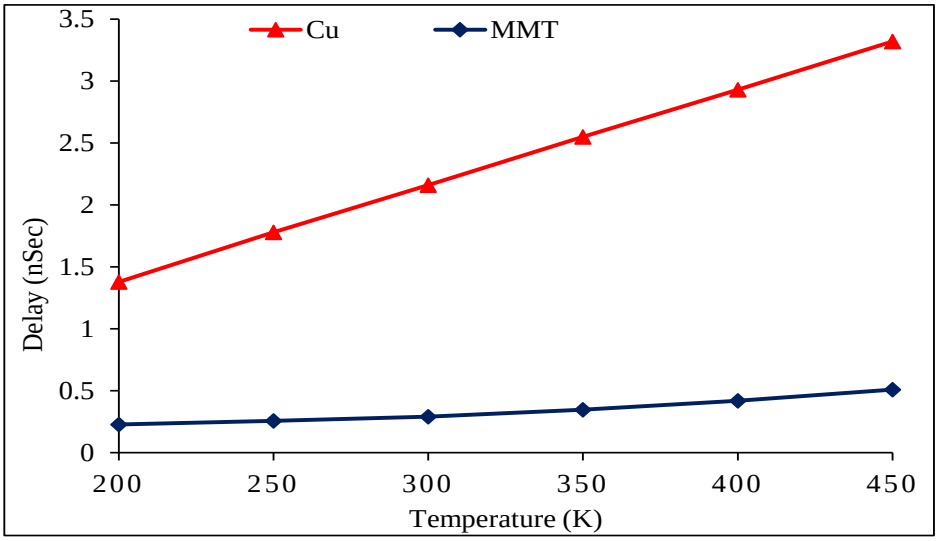
Temperature-dependent delay of MMT nanostructure and Cu interconnects are compared for 1000μm interconnect length at DSM technology nodes viz. 32, 22 and 16nm as shown in Figure 6.14. The comparison of delay for MMT and Cu as global interconnect on a variable temperature range (200-450K) is shown in Figure 6.14 (a) 32, (b) 22 and (c) 16nm technology nodes. It revealed that the delay of MMT and Cu interconnects are increased with rising temperature from 200-450K because of decrease in the MFPs of MMT. However, the delay of MMT is smaller than Cu for global interconnect length for DSM technology nodes. The performance of MMT has significantly improved in terms of delay for global interconnect as compared to Cu for rising temperature range 200-450K at 32, 22 and 16nm technology nodes.


Cu
MMT
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
Delay (nSec)
200
250
300
350
400
450
Temperature (K)

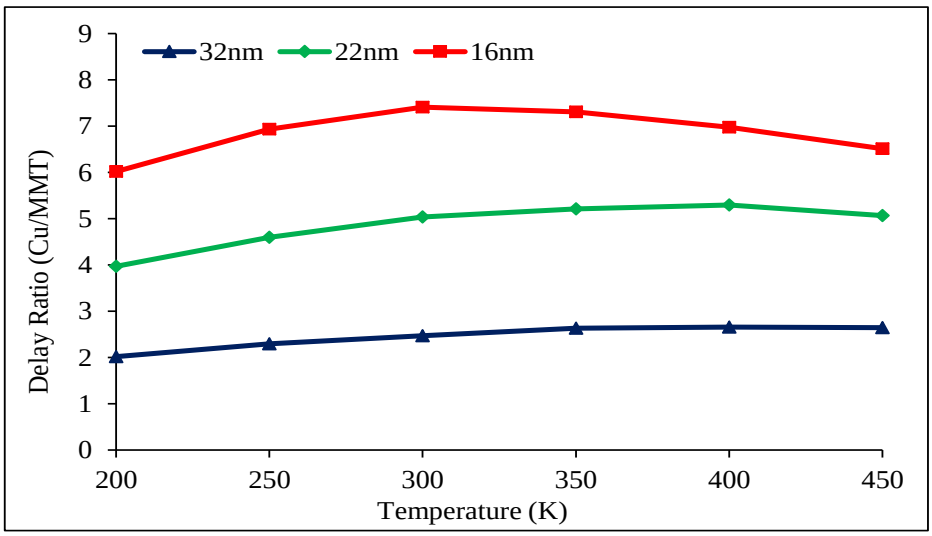
(a)


Cu
MMT
1.4
1.2
1
0.8
0.6
0.4
0.2
0
Delay (nSec)
200
250
300
350
400
450
Temperature (K)

(b)


Cu
MMT
3.5
3
2.5
2
1.5
1
0.5
0
Delay (nSec)
200
250
300
350
400
450
Temperature (K)

(c)



(d)

Figure 6.14: Delay comparison of MMT and Cu interconnect at DSM technology nodes as (a) 32, (b) 22 and (c) 16nm. (d) The delay ratio (Cu/MMT) at 32, 22 and 16nm technology nodes.

The delay ratio (Cu/MMT) for global level interconnect length (1000μm) on a various temperature range (200-450K) at DSM technology nodes i.e. 32, 22 and 16nm is shown in Figure 6.14(d). It is seen that the delay ratio (Cu/MMT) is more than unity for entire temperature range 200-450K at DSM technology nodes. The delay ratio (Cu/MMT) is calculated for temperature range 200-450K as 2.01-2.64 at 32nm, 3.97-5.06 at 22nm and 6.02-6.51 at 16nm technology nodes. It means that the delay of MMT is less as compared to Cu interconnects at all three DSM technology nodes. For scaled-down technology nodes from 32 to 16nm, the delay ratio is increased as 2.01 to 6.02 and 2.64 to 6.51 at 200 and 450K temperatures, respectively.

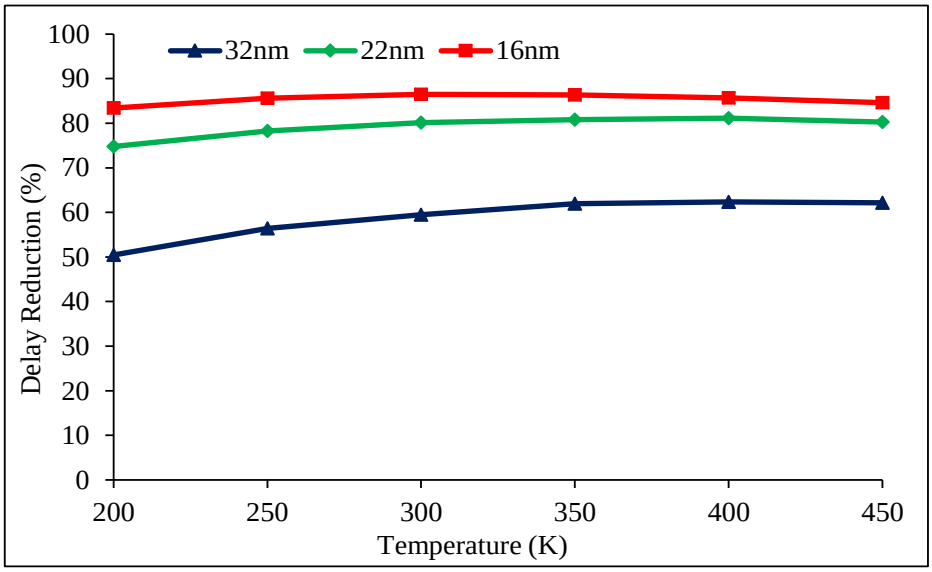
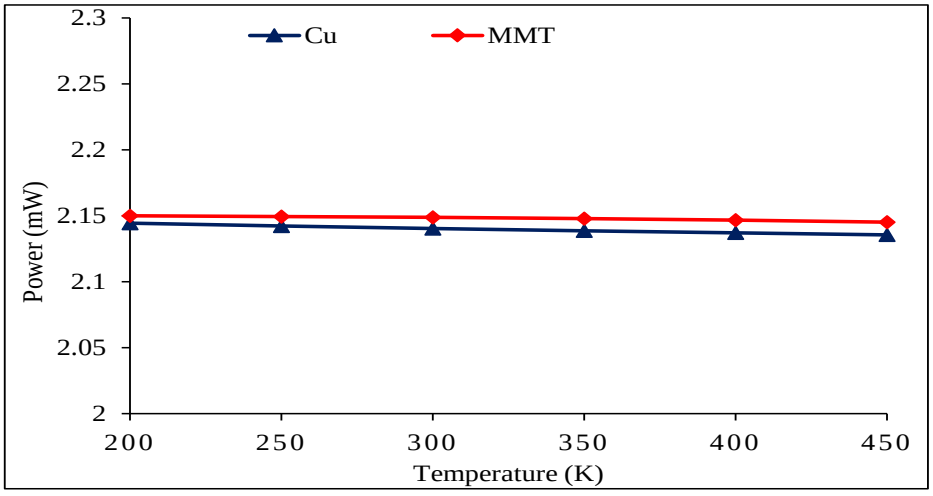


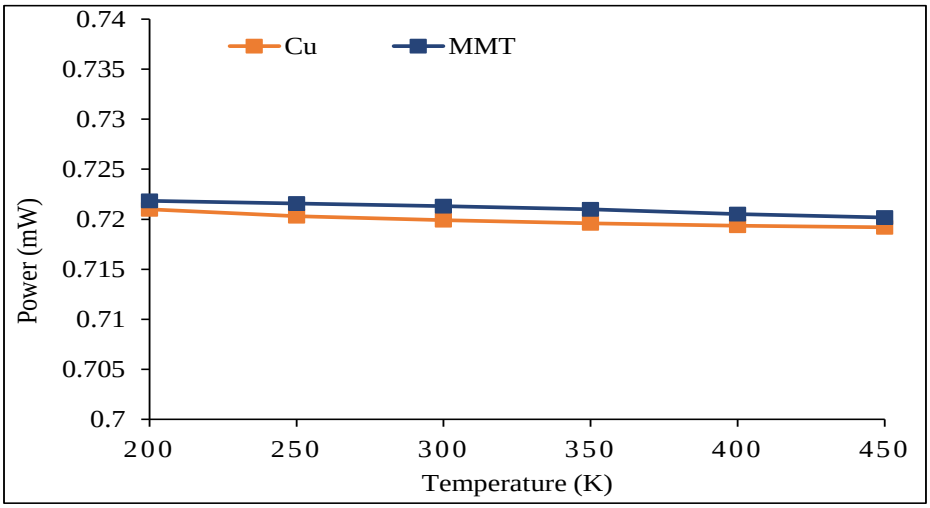
Figure 6.15: Delay reduction in % (Cu to MMT) at 32, 22 and 16nm technology nodes.

The delay reduction in % ($\frac{Cu-MMT}{Cu} * 100$) is observed for DSM technology nodes (32, 22 and 16nm) as shown in Figure 6.15. The delay reduction (%) for temperature ranging from 200 to 450K is calculated as 50.4 to 62.1%, 74.8 to 80.2% and 83.3 to 84.6% at technology nodes as 32, 22 and 16nm, respectively. It reveals that the delay reduction (%) has significantly improved for temperature ranging from 200 to 450K at DSM technology nodes (32, 22 and 16nm). The % of delay reduction is increased for scaled-down technology nodes from 32 to 16nm as 50.43 to 83.39% for 200K and 62.15 to 84.64% for 450K temperature. It means that performance of MMT nanostructure is better than Cu interconnect for DSM technology nodes. It is supporting to MMT nanostructure, which can be considered as global interconnect material at DSM technology nodes. It concludes that performance in terms of the delay for MMT nanostructure is better as compared to Cu for global interconnect length at DSM technology nodes (32, 22 and 16nm) on a variable temperature range (200-450K).

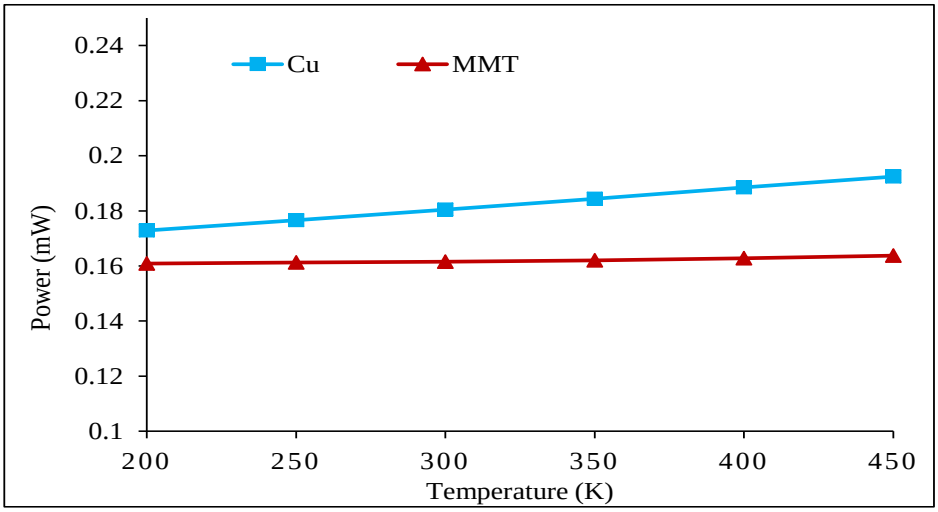
The temperature-dependent performance in terms of power for MMT and Cu as VLSI interconnect is shown in Figure 6.16 (a) 32, (b) 22 and (c) 16nm technology nodes. The results show that the power of MMT nanostructure is more as compared to Cu interconnect due to high tube capacitance of MMT nanostructure. The power of MMT and Cu interconnect are decreased with scaled-down technology nodes from 32 to 16nm. It increases with increase in temperature ranging from 200 to 450K at 16nm technology nodes. However, the power is decreased in case of 32 and 22nm technology nodes for increase in temperature ranging from 200 to 450K. The power ratio of Cu/MMT nanostructure is presented in Figure 6.16(d), where the power ratios are constant and nearly or equal to unity for 32 and 22nm technology nodes. The power ratio increases with increasing temperature ranging from 200 to 450K at 16nm technology node.



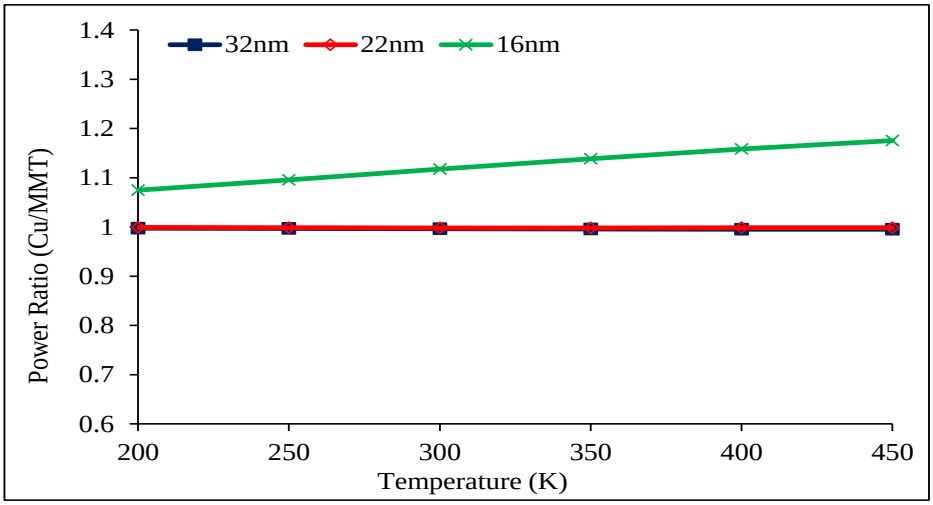
(a)



(b)

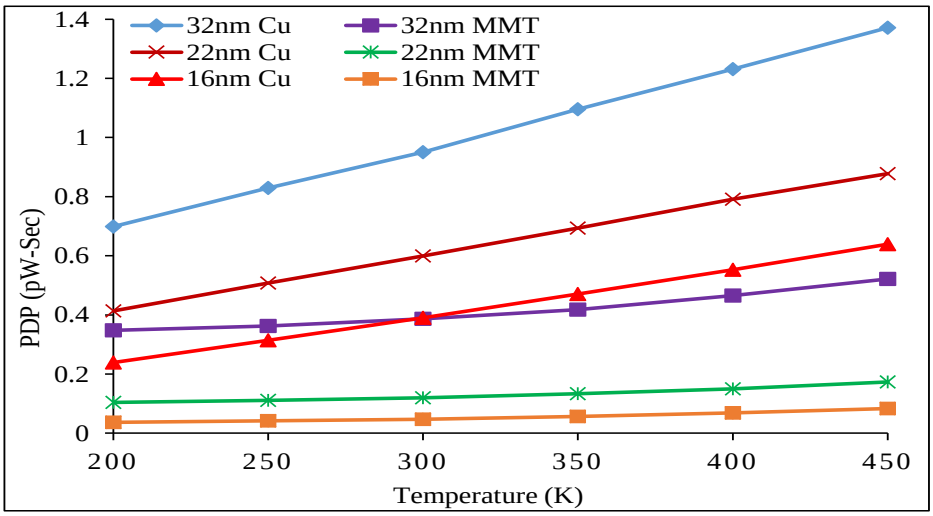


(c)

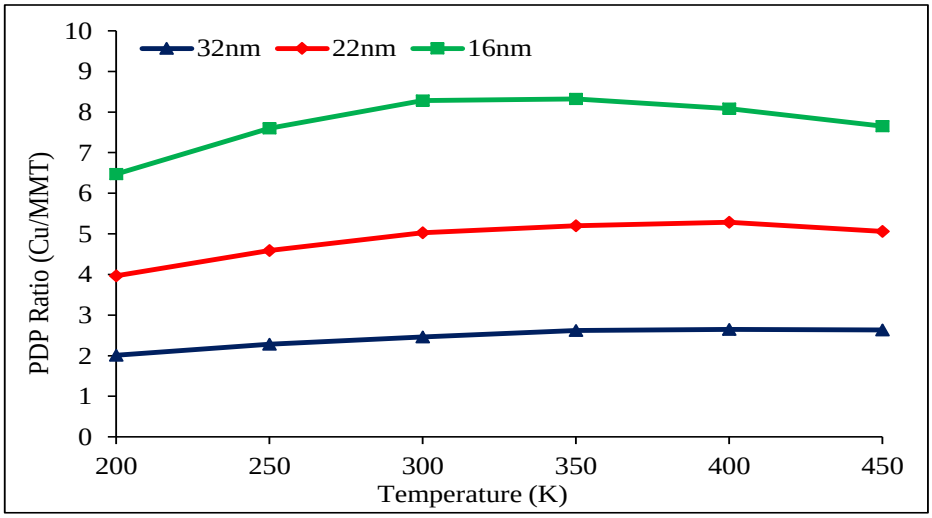


(d)

Figure 6.16: Power comparison of MMT and Cu interconnect at DSM technology nodes as (a) 32, (b) 22 and (c) 16nm. (d) The power ratio (Cu/MMT) at 32, 22 and 16nm technology nodes.



(a)



(b)

Figure 6.17: (a) Comparison of PDP for MMT and Cu as global interconnect at DSM technology nodes as 32, 22 and 16nm. (b) The PDP ratio (Cu/MMT) at DSM technology nodes.

The comparative analysis of temperature-dependent PDP for MMT nanostructure and Cu as global level interconnect is shown in Figure 6.17 (a) at DSM technology nodes viz. 32, 22 and 16nm. It reveals that performance in terms of PDP for both the interconnect materials such as MMT and Cu are influenced with rising temperature range (200-450K) at DSM technology nodes. The comparison of PDP ratio (Cu/MMT) is observed more than unity at all three technology nodes (32, 22 and 16nm) as shown in Figure 6.17 (b) as a function of temperature. For temperature range 200 to 450K, the PDP ratio is determined as 2.01 to 2.63, 3.96 to 5.05 and 6.47 to 7.65 for 32, 22 and 16nm technology nodes, respectively. The PDP ratio is increased with scaled-down technology nodes from 32 to 16nm. It shows that the MMT is better candidate than Cu interconnect at DSM technology nodes.

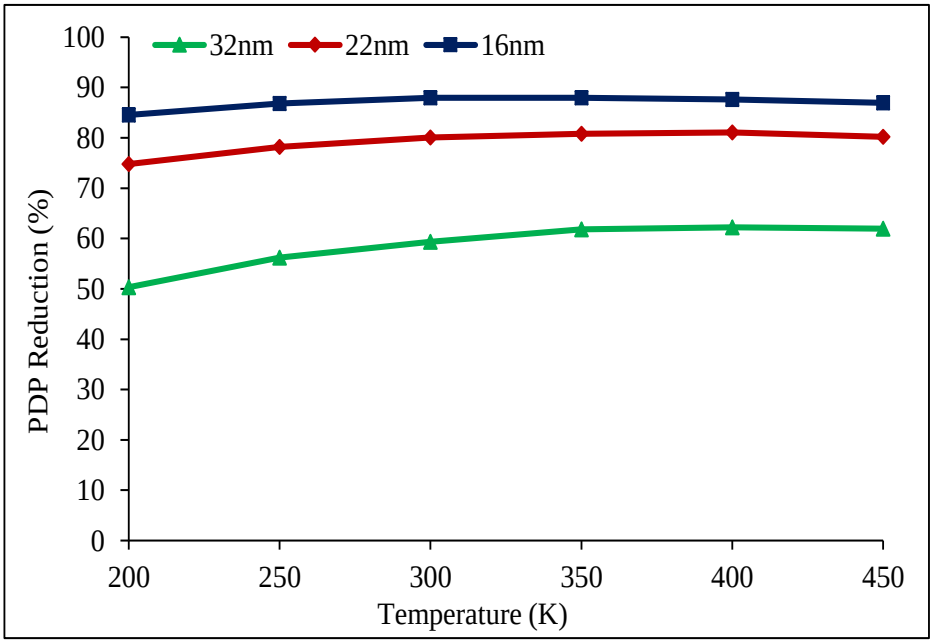


Figure 6.18: PDP reduction in % (Cu to MMT) at 32, 22 and 16nm technology nodes.

The PDP reduction ($\frac{Cu-MMT}{Cu} * 100$) in % is calculated for technology nodes (32, 22 and 16nm) as shown in Figure 6.18. At temperature ranging from 200 to 450K, the PDP reduction (%) is examined as 50.30 to 61.98%, 74.77 to 80.23% and 84.54 to 86.93% at technology nodes as 32, 22 and 16nm, respectively. It reveals that the PDP reduction (%) is small variation for temperature range above 300K at DSM technology nodes (32, 22 and 16nm). The PDP reduction (%) is increased for scaled-down technology nodes from 32 to 16nm. It means that the MMT nanostructure is performed better than Cu interconnect for DSM technology nodes. It is concluded that performance of MMT nanostructure is outperformed Cu interconnect in terms of PDP for global interconnect on a variable temperature range at DSM technology nodes.

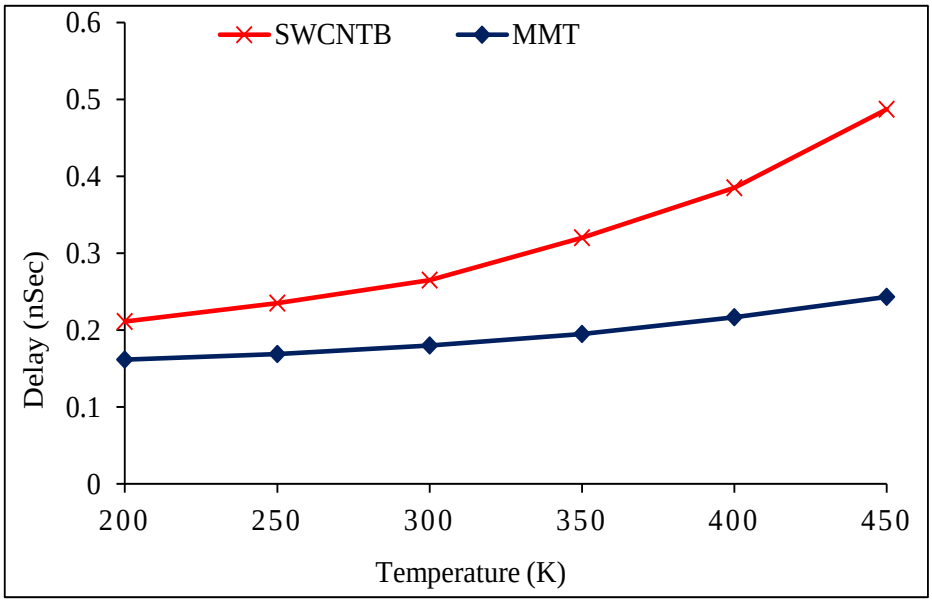
6.3.2 Temperature-dependent performance analysis for MMT and SWCNTB interconnects

This sub-section presents the temperature-dependent performance analysis of MMT nanostructure and SWCNTB as VLSI interconnect. The impact of temperature on performance for MMT and SWCNTB as global interconnect length is examined at DSM technology nodes i.e. 32, 22 and 16nm on a variable temperature ranging from 200 to 450K. In case of CNTs, the MFP plays a significant role which is described in chapter 4. The MFP of CNTs is influenced by scattering such as electron-phonon and electron-electron scattering at various temperatures. MFP

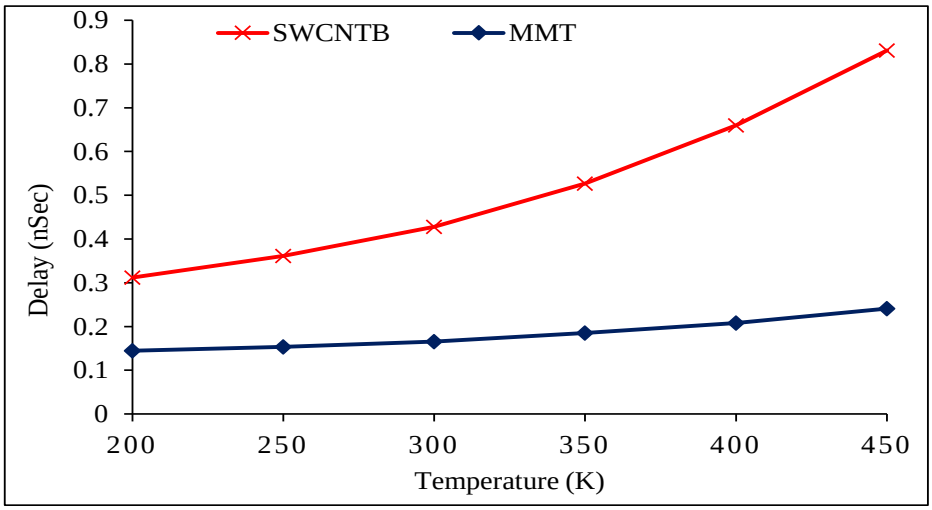
decreases with increasing temperature ranging from 200 to 450K, which affect the impedance parameter in terms of resistance for both the MMT and SWCNTB interconnects. The resistance of MMT and SWCNTB interconnect increases with decrease in MFP. The resistance of CNTs depends on MFP but the capacitance and inductance are independent of it.

Further, these parameters affect the performance in terms of delay, power and PDP for MMT and SWCNTB interconnect. The temperature-dependent parasitic of SWCNTB are calculated for global interconnect at DSM technology nodes in Chapter 6. The simulation parameters are considered to evaluate the performance as per ITRS-2013. The temperature-dependent performance of MMT and SWCNTB in terms of delay for interconnect length 1000μm on temperature ranging between 200 and 450K is shown in Figure 6.19 (a) 32, (b) 22 and (c) 16nm technology nodes.

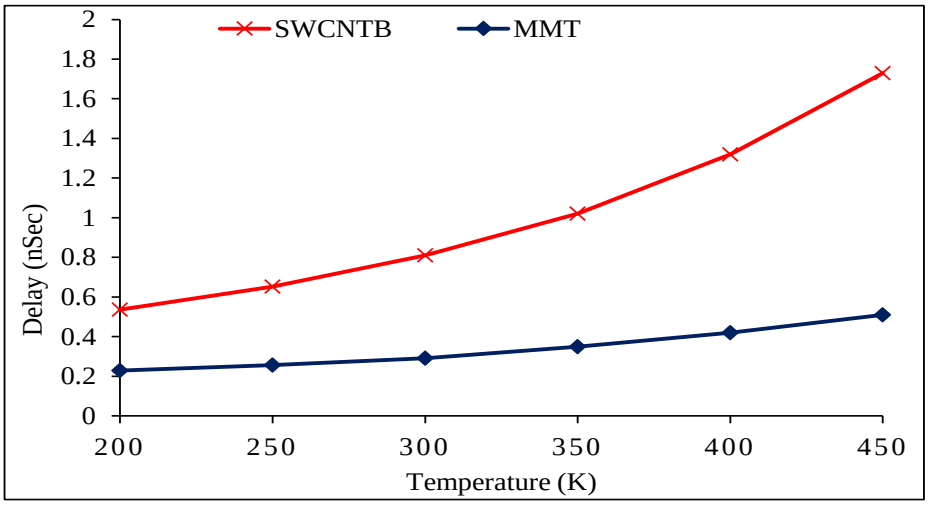
It reveals that the the delay of MMT and SWCNTB are increased with rise in temperature ranging from 200 to 450K at DSM technology nodes under consideration. The delay is increased because the resistance of MMT and SWCNTB increases with decrease in MFPs (MFP is inversely proportional to resistance). The MFPs of CNTs are reduced with increase in temperature moderate to high at DSM technology nodes. Further, the delay of MMT nanostructure is smaller as compared to SWCNTB for global interconnect at DSM technology nodes. The performance of MMT interconnect in terms of delay is improved than SWCNTB interconnect with increase in temperature.



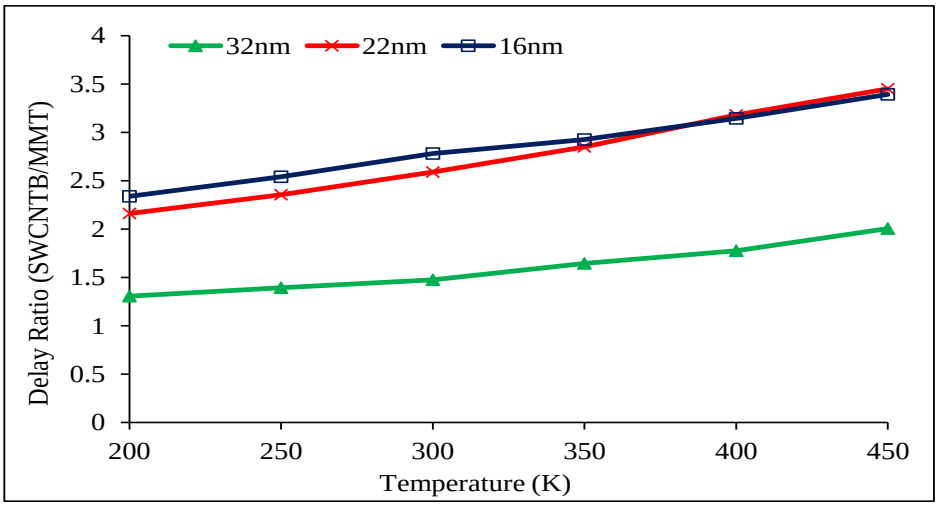
(a)



(b)



(c)



(d)

Figure 6.19: Delay comparison of MMT and SWCNTB interconnect at technology nodes viz. (a) 32, (b) 22 and (c) 16nm. (d) The delay ratio (SWCNTB/MMT) at DSM technology nodes.

The delay ratio (SWCNTB/MMT) is presented in Figure 6.19(d) at different technology nodes for variable temperature ranging from 200 to 450K. The delay ratio (SWCNTB/MMT) is examined more than unity for all three technology nodes. It means that MMT nanostructure offers less delay as compared to SWCNTB interconnect for entire temperature range under consideration. The delay ratio (SWCNTB/MMT) is calculated for technology nodes 32nm as 1.30 to 2.0, 22nm as 2.16 to 3.45 and 16nm as 2.33 to 3.39 at a variable temperature ranging from 200 to 450K. It is revealed from the results, the performance of MMT nanostructure in terms of delay is better than SWCNTB for a variable temperature ranging from 200 to 450K. The delay ratio is also examined for scaled-down technology nodes from 32 to 16nm as 1.30 to 2.33 and 2.0 to 3.39 at temperature 200 and 450K, respectively. The performance of MMT is also better as compared to SWCNTB at scaled-down technology nodes viz. 32 to 16nm.

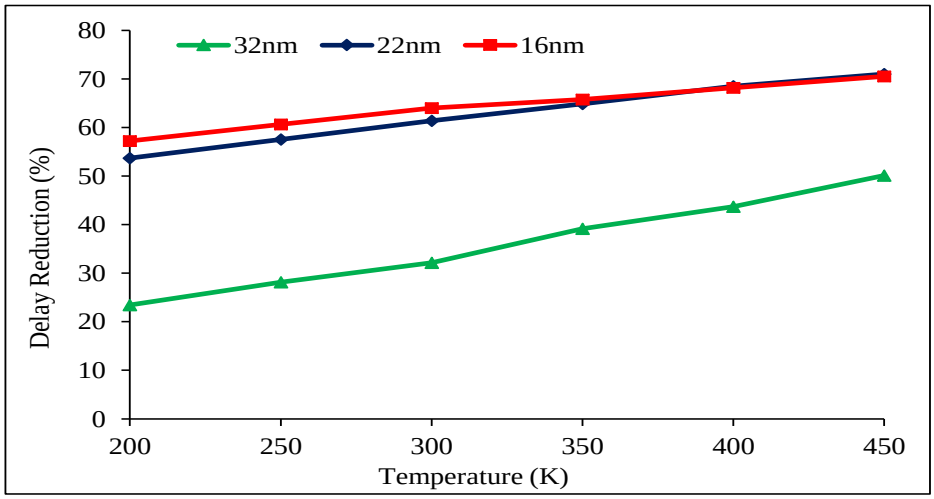
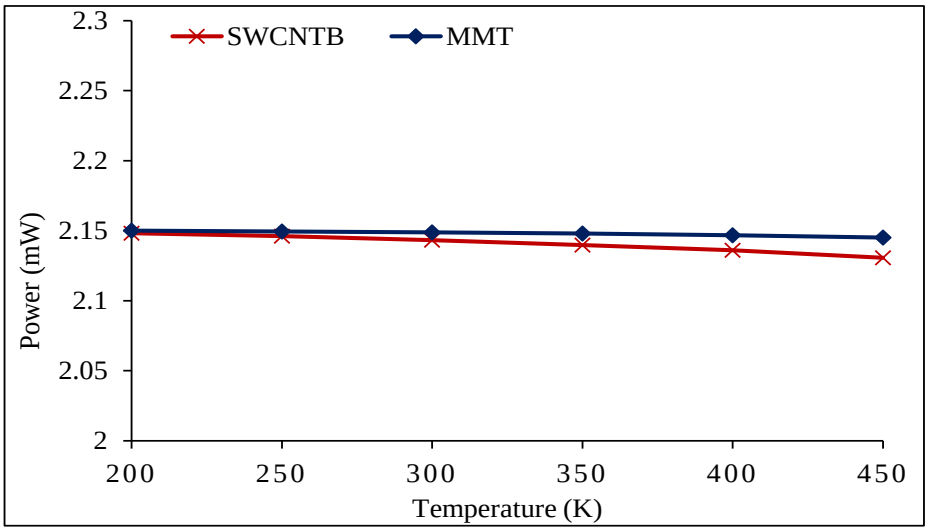
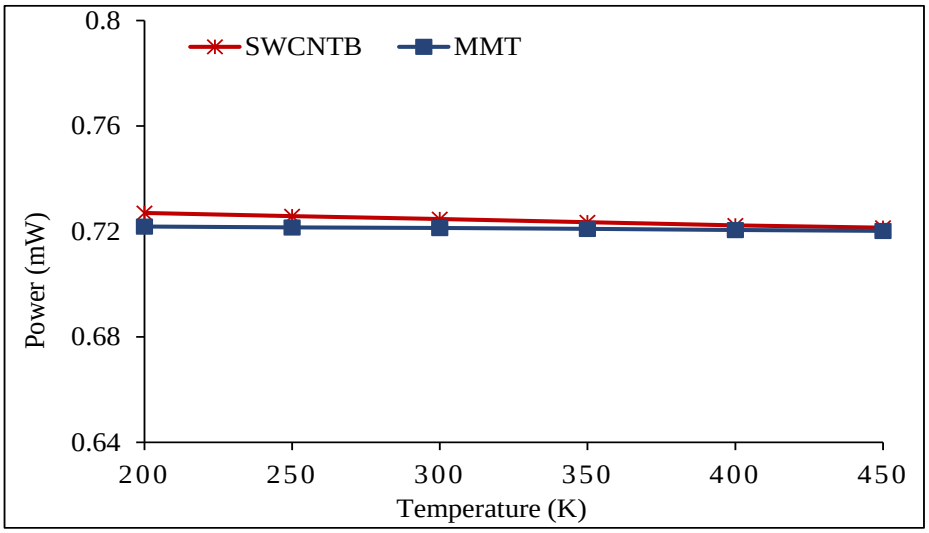


Figure 6.20: Delay reduction in % (SWCNTB to MMT) at DSM technology nodes.

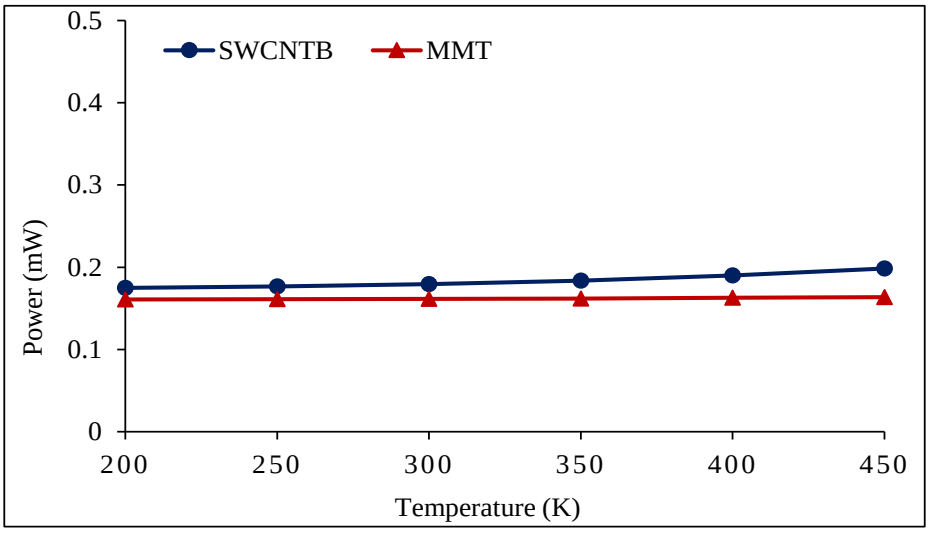
The delay reduction ($\frac{SWCNTB-MMT}{SWCNTB} * 100$) in % is determined for DSM technology nodes (32, 22 and 16nm) as shown in Figure 6.20. For temperature ranging from 200 to 450K, the delay reduction (%) is calculated as 23.42 to 50.10% at 32nm, 53.72 to 71.01% at 22nm and 57.24 to 70.52% at 16nm technology nodes. It reveals that the delay reduction (%) is observed less variation for temperature above 300K at DSM technology nodes as 22 and 16nm as compared to 32nm. The delay reduction (%) for scaled-down technology nodes from 32 to 16nm is also calculated as 23.42 to 57.24% and 50.10 to 70.52% at 200 and 450K temperatures, respectively. It means that the performance of MMT nanostructure is better than SWCNTB interconnect for DSM technology nodes. It is concluded that performance of MMT in terms of delay is outperformed SWCNTB as VLSI interconnect at DSM technology nodes for moderate to high temperatures.


SWCNTB
MMT
2.3
2.25
2.2
2.15
2.1
2.05
2
Power (mW)
200
250
300
350
400
450
Temperature (K)

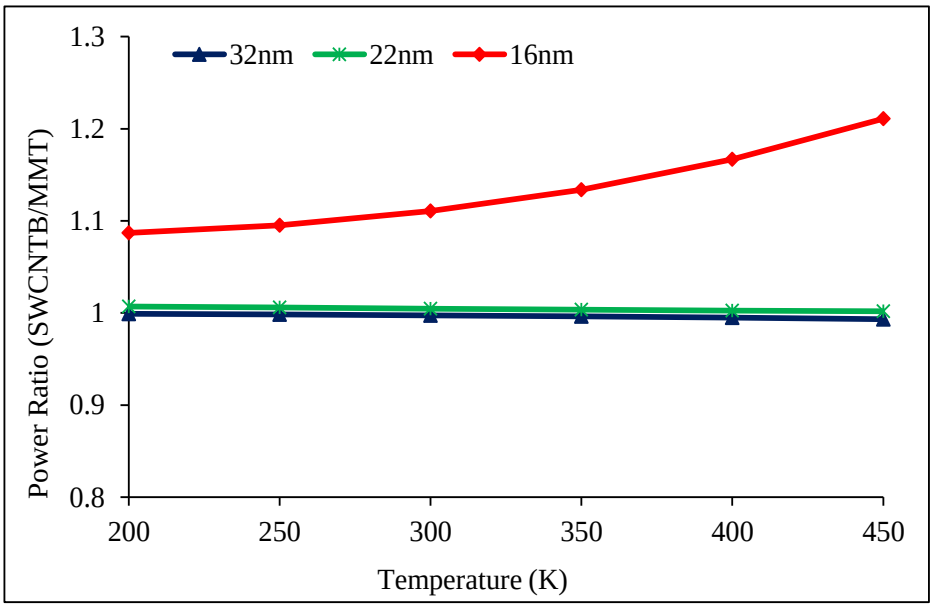
(a)


SWCNTB
MMT
0.8
0.76
0.72
0.68
0.64
Power (mW)
200
250
300
350
400
450
Temperature (K)

(b)


SWCNTB
MMT
0.5
0.4
0.3
0.2
0.1
0
Power (mW)
200
250
300
350
400
450
Temperature (K)

(c)

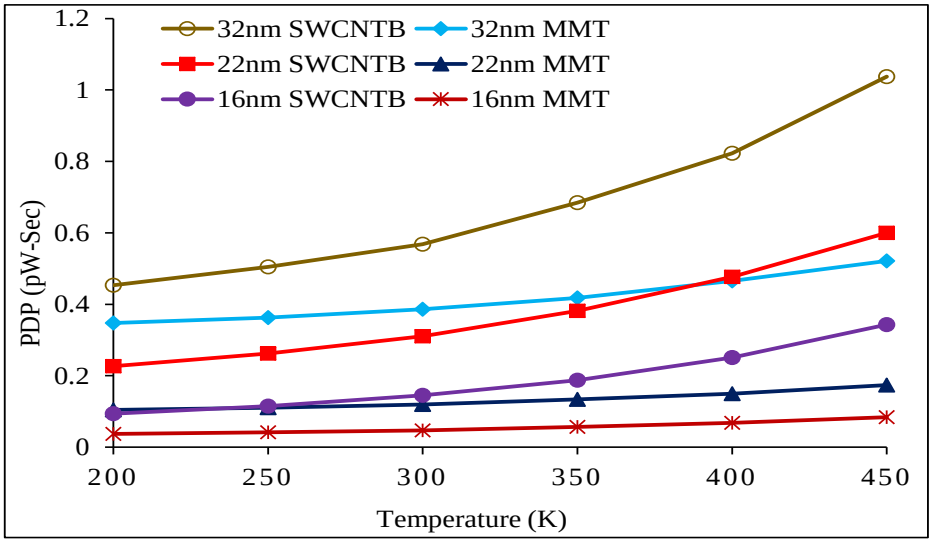


(d)

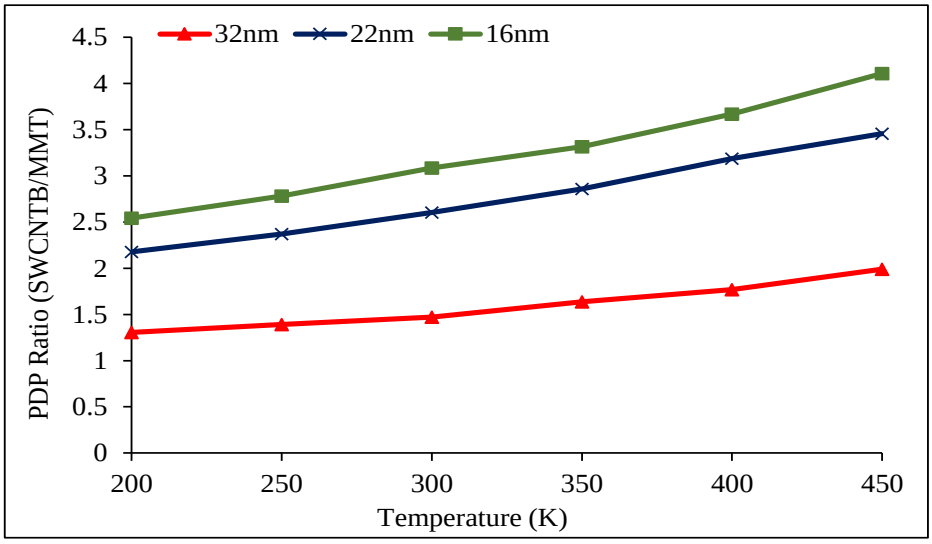
Figure 6.21: Power comparison of MMT and SWCNTB interconnect at DSM technology nodes (a) 32, (b) 22 and (c) 16nm. (d) The power ratio (SWCNTB/MMT) at DSM technology nodes.

Temperature-dependent performance in terms of power for MMT and SWCNTB is shown in Figure 6.21. The comparison of power dissipation of MMT and SWCNTB as VLSI interconnect length (1000μm) for temperature range between 200 and 450K at DSM technology nodes viz. 32, 22 and 16nm are shown in Figure 6.21 (a), (b) and (c), respectively. It reveals that power consumption is high in case of MMT nanostructure due to large tube capacitance as compared to SWCNTB. Figure 6.21 (d) is presented power ratio (SWCNTB/MMT) for global interconnect at DSM technology nodes viz. 32, 22 and 16nm. The power ratio is constant at 32 and 22nm technology nodes for temperature (200-450K) as compared to 16nm, which is increased with increasing temperature ranging from 200 to 450K. It shows that the power is increased for reduce in technology nodes from 32 to 16nm on a variable temperature range.

The performance of MMT and SWCNTB as global interconnect in terms of PDP are compared at DSM technology nodes viz. 32, 22 and 16nm on various temperatures is shown in Figure 6.22 (a). The comparison of PDP for MMT and SWCNTB as global interconnect are increased with rising temperature range (200 to 450K) at DSM technology nodes. It reveals that the PDP of MMT nanostructure is examined lower than SWCNTB at all three technology nodes under consideration. However, the PDP decreased for scaled-down technology nodes from 32 to 16nm. It is concluded that MMT nanostructure may be considered as global interconnects at DSM technology nodes for variable temperature conditions.



(a)



(b)

Figure 6.22: (a) Comparison of PDP for MMT and SWCNTB interconnect at various DSM technology nodes. (b) PDP ratio (SWCNTB/MMT) at DSM technology nodes.

Figure 6.22(b) shows that the comparison of PDP ratio (SWCNTB/MMT) for various temperatures from 200 to 450K at DSM technology nodes. The ratio of PDP is increased with increase in temperature ranging from 200 to 450K for technology nodes viz. 32, 22 and 16nm. It is always more than unity for entire temperature range and all three technology nodes under considered for this work. It is examined for temperature 200 to 450K as 1.30 to 1.99, 2.17 to 3.45 and 2.54 to 4.10 at 32, 22 and 16nm technology nodes, respectively. It reveals that the MMT nanostructure as VLSI interconnect offers less PDP than SWCNTB interconnects for DSM technology nodes. The PDP ratio is increased with scaled-down technology nodes from 32 to 16nm. The PDP of MMT is improved than SWCNTB as global interconnect

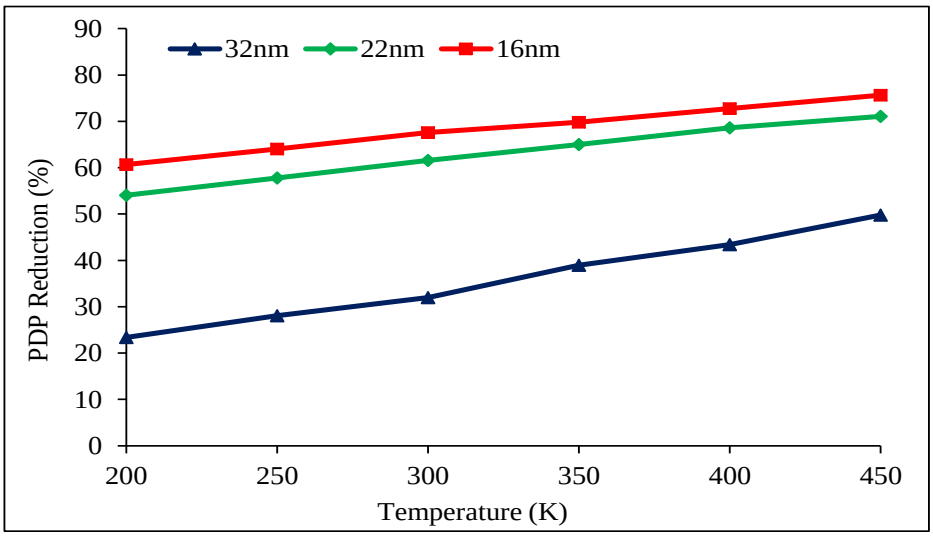
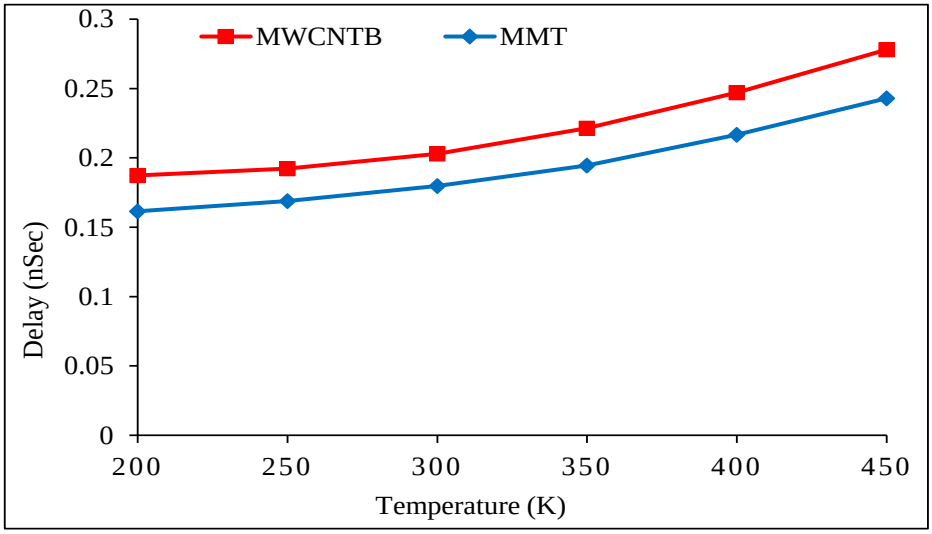


Figure 6.23: PDP reduction in % (SWCNTB to MMT) at 32, 22 and 16nm technology nodes.

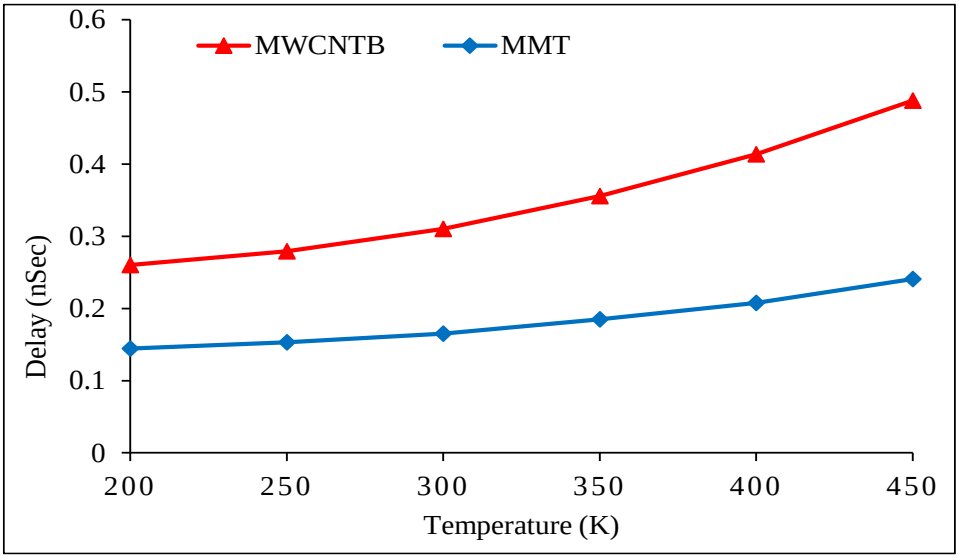
The PDP reduction in % ($\frac{SWCNTB-MMT}{SWCNTB} * 100$) is calculated as shown in Figure 6.23, which is increased with increase in temperature ranging from 200 to 450K. The PDP reduction (%) is increased with decrease in technology nodes from 32 to 16nm. It is observed that the PDP reduction (%) is calculated as 23.36 to 49.77%, 54.05 to 71.06% and 60.66 to 75.66% for technology nodes viz. 32, 22 and 16nm, respectively. It concludes that MMT nanostructure performs better than SWCNTB as VLSI interconnect at DSM technology nodes for thermally-aware environmental conditions. The MMT may be considered as global interconnect for a variable temperature range at DSM technology nodes.

6.3.3 Temperature-dependent performance analysis of MMT and MWCNTB interconnects

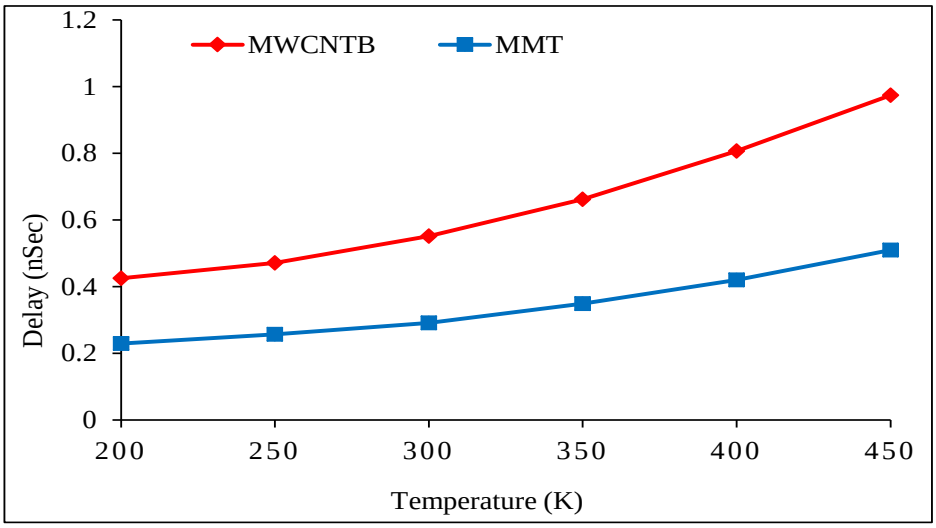
This sub-section presents the performance analysis of MMT nanostructure and MWCNTB as global level interconnect for variable temperature range at DSM technology nodes. The calculated parasitic of MWCNTB in Subsection 6.2.3 and these parasitic are simulated by using the SPICE tool for DSM technology nodes viz. 32, 22 and 16nm. The temperature-dependent performance in terms of delay of MMT and MWCNTB is compared for global interconnect length at all three technology nodes under consideration as shown in Figure 6.24. The temperature-dependent delay of MMT and MWCNTB as VLSI interconnect length 1000μm for 32, 22 and 16nm technology nodes is shown in Figure 6.24 (a), (b) and (c), respectively. It is revealed that the delay of MMT and MWCNTB increases with rising temperature between 200 and 450K for DSM technology nodes.


MWCNTB
MMT
Delay (nSec)
0.3
0.25
0.2
0.15
0.1
0.05
0
200
250
300
350
400
450
Temperature (K)

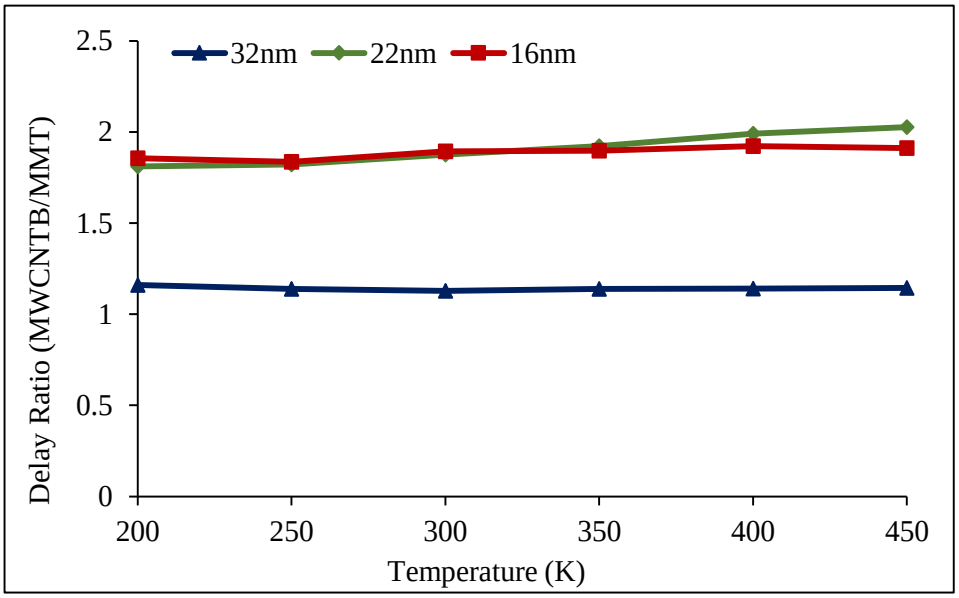
(a)


MWCNTB
MMT
Delay (nSec)
0.6
0.5
0.4
0.3
0.2
0.1
0
200
250
300
350
400
450
Temperature (K)

(b)


MWCNTB
MMT
Delay (nSec)
1.2
1
0.8
0.6
0.4
0.2
0
200
250
300
350
400
450
Temperature (K)

(c)



(d)

Figure 6.24: Delay comparison of MMT and MWCNTB interconnect at DSM technology nodes as (a) 32, (b) 22 and (c) 16nm. (d) The delay ratio (MWCNTB/MMT) at DSM technology nodes.

The delay of MMT and MWCNTB is increasing for a variable temperature range at DSM technology nodes under consideration. However, the delay of MMT nanostructure offers less than MWCNTB for temperature range (200-450K) at DSM technology nodes (32, 22 and 16nm). Figure 6.24(d) indicates the delay ratio (MWCNTB/MMT) as VLSI interconnect on a various temperature range at 32, 22 and 16nm technology nodes. The delay ratio is examined more than unity for all three technology nodes considered for this work for entire temperature range. The delay ratio (MWCNTB/MMT) for temperature 200 to 450K is calculated as 1.16 to 1.14 at 32nm, 1.81 to 2.06 at 22nm and 1.85 to 1.91 at 16nm technology nodes. The delay ratio (MWCNTB/MMT) for scaled-down technology nodes from 32 to 16nm is also examined for 200 and 450K as 1.16 to 1.85 and 1.14 to 1.91, respectively.

The delay reduction ($\frac{MWCNTB-MMT}{MWCNTB} * 100$) in % is examined for DSM technology nodes (32, 22 and 16nm) as shown in Figure 6.25. At temperature ranging from 200 to 450K, the delay reduction (%) is calculated for technology nodes 32nm as 13.79 to 12.63%, 22nm as 44.78 to 50.84% and 16nm as 46.09 to 47.68%. The delay reduction (%) is increased for scaled-down technology nodes from 32 to 16nm. It is calculated as 13.79 to 46.09% and 12.63 to 47.68% for temperature 200 and 450K at scaled-down technology nodes, respectively. It revealed that performance of MMT is better than MWCNTB interconnect for DSM technology nodes as a function of temperature.

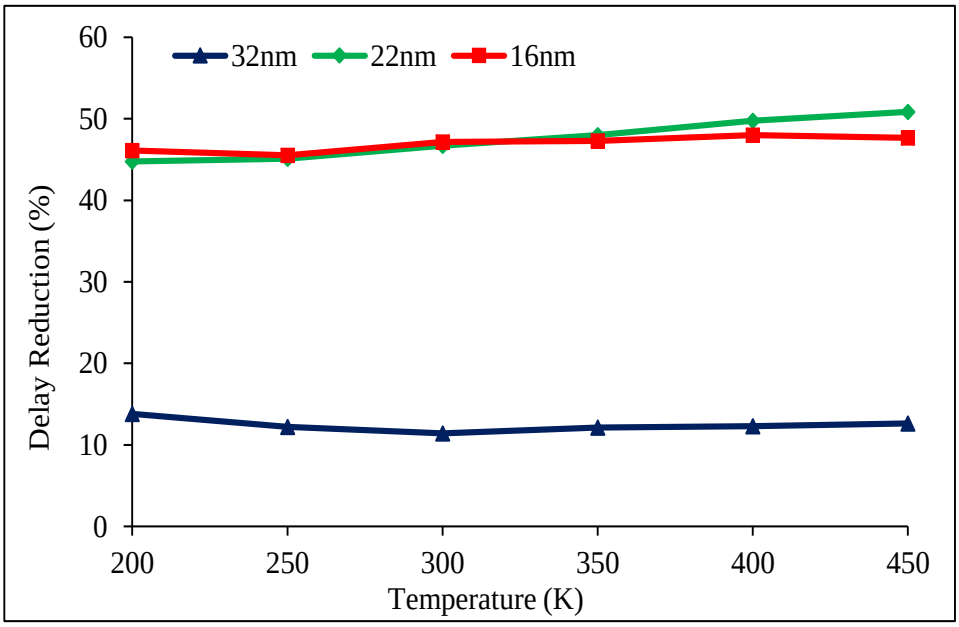
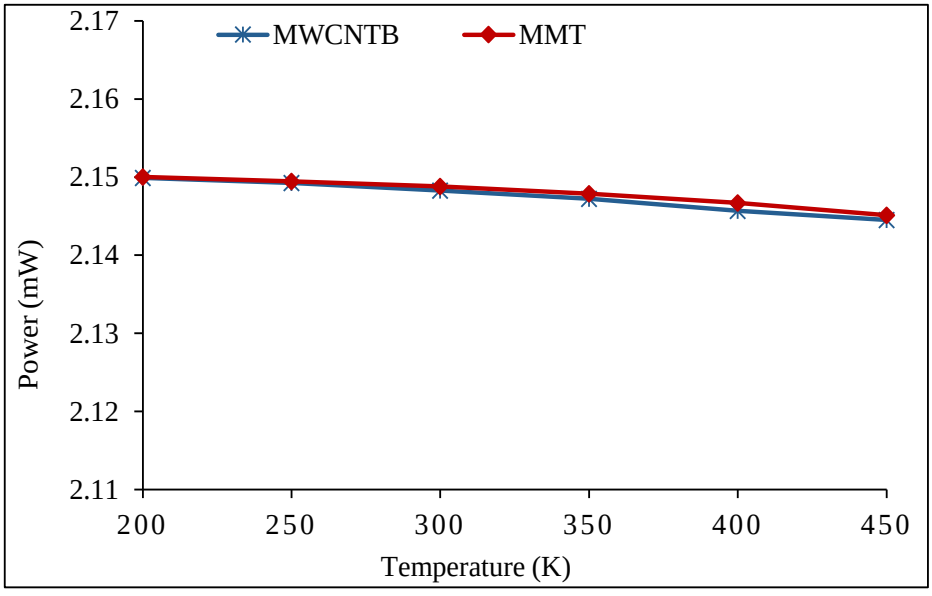
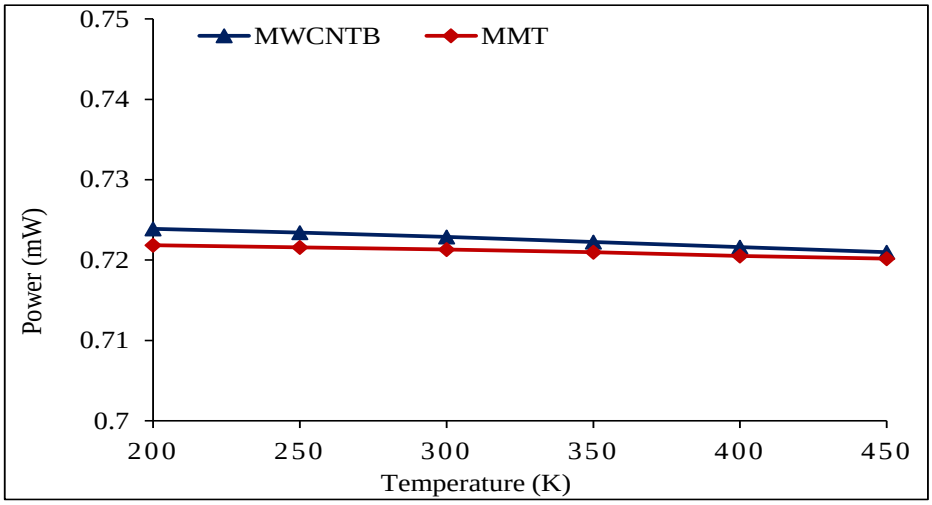


Figure 6.25: Delay reduction in % (MWCNTB to MMT) at DSM technology nodes.

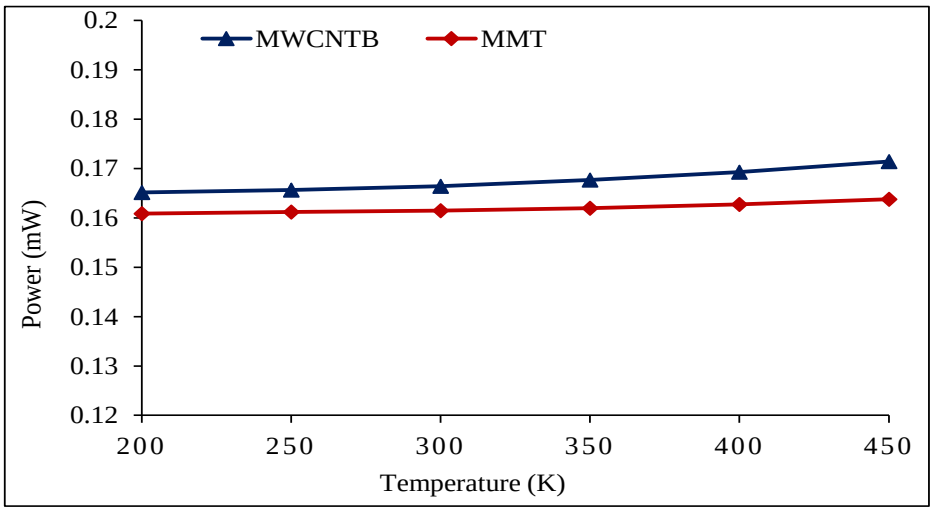
Temperature-dependent performance in terms of power for MMT and MWCNTB interconnect is presented in Figure 6.26 (a) 32, (b) 22 and (c) 16nm technology nodes. The power dissipation of MMT and MWCNTB are almost same for temperature ranging from 200 to 450K at DSM technology nodes viz. 32, 22 and 16nm. It is revealed that the power of MMT nanostructure is slightly higher than MWCNTB for variable temperature at 32nm technology nodes. However, performance in terms of power is improved for technology nodes as 22 and 16nm. It is supporting the MMT nanostructure is better candidate at DSM technology nodes viz. 22 and 16nm for higher temperatures.



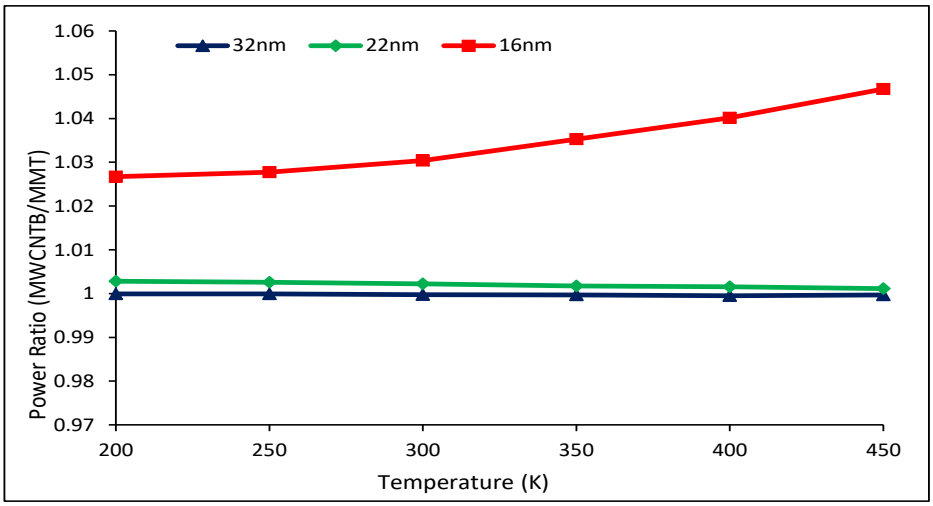
(a)



(b)

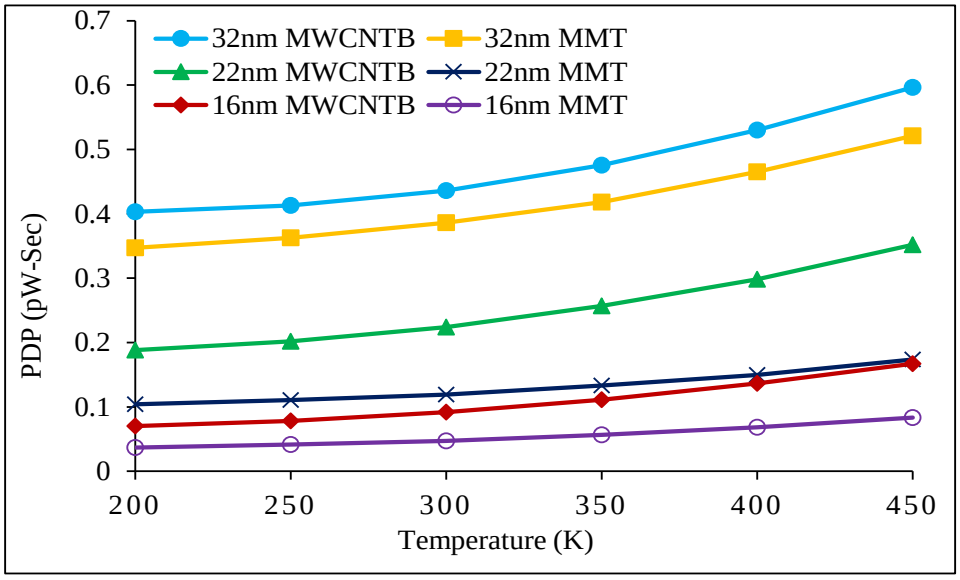


(c)

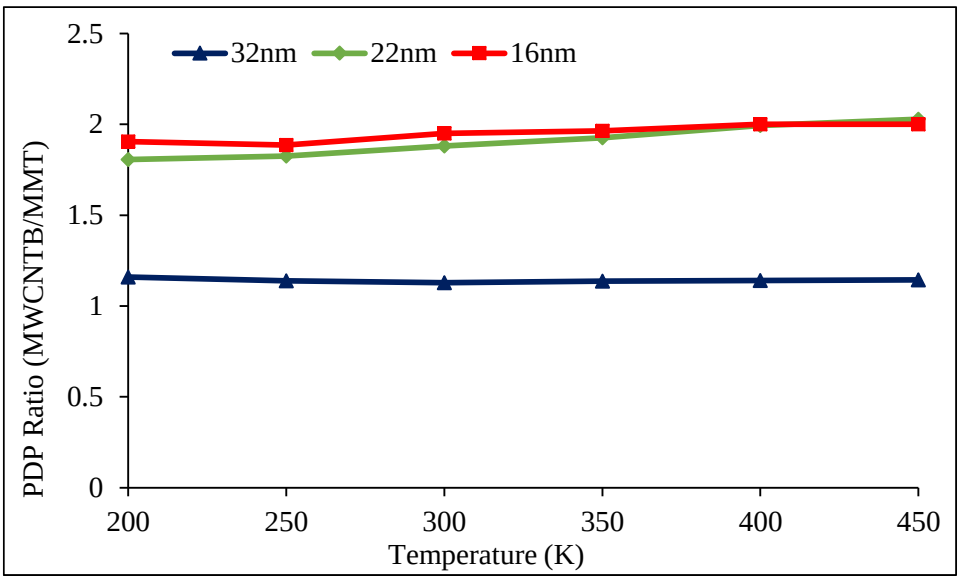


(d)

Figure 6.26: Power comparison of MMT and MWCNTB interconnect at (a) 32, (b) 22 and (c) 16nm technology nodes. (d) The power ratio (MWCNTB/MMT) at DSM technology nodes.



(a)



(b)

Figure 6.27: Comparison of PDP for MWCNTB and MMT at DSM technology nodes. (b) PDP ratio (MWCNTB/MMT) at DSM technology nodes.

The performance of MMT and MWCNTB interconnect in terms of PDP is shown in Figure 6.27 (a) for various technology nodes on a variable temperature range. The PDP of MMT and MWCNTB are increased with rising temperature for DSM technology nodes viz. 32, 22 and 16nm. The PDP of MMT and MWCNTB are increased with scaled-down technology nodes from 32 to 16nm. The performance of MMT in terms of PDP is significantly improved for moderate to high temperature at DSM technology nodes as 22 and 16nm. It reveals that performance of MMT nanostructure in terms of PDP perform better than MWCNTB for moderate to higher temperature at DSM technology nodes.

The comparison of PDP ratio (MWCNTB/MMT) is presented in Figure 6.27 (b) and it is calculated more than unity for a variable temperature range 200 to 450K at DSM technology nodes. The PDP ratio for temperature ranging from 200 to 450K is examined at technology nodes 32nm as 1.16 to 1.14, 22nm as 1.80 to 2.0 and 16nm as 1.90 to 2.0. The PDP ratio is increased with rise in temperature from 200 to 450K at 22 and 16nm technology nodes. The performance in terms of PDP is improved for MMT nanostructure as compared to MWCNTB interconnect for 22nm and 16nm technology nodes as a function of temperature.

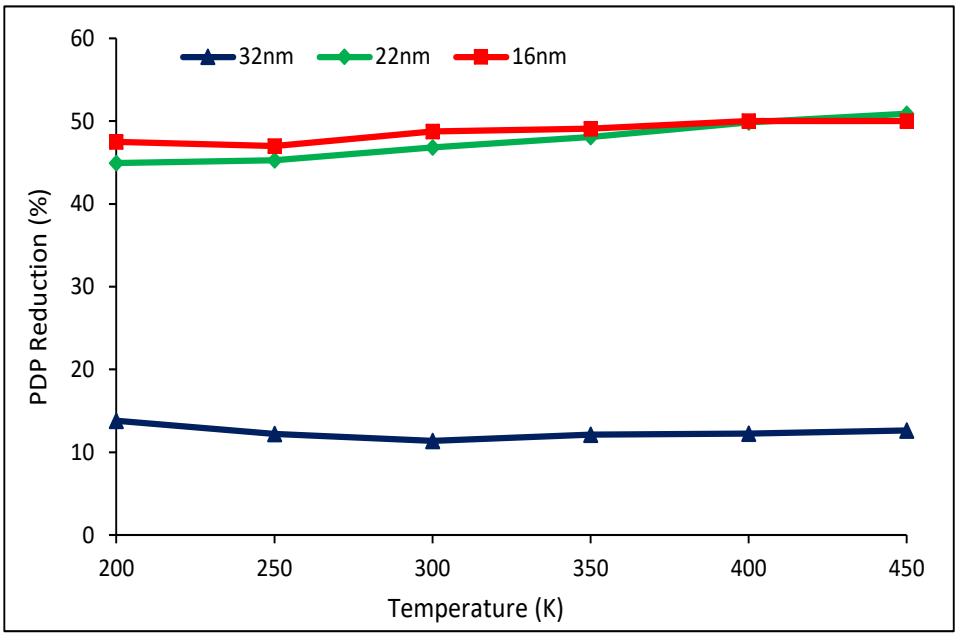


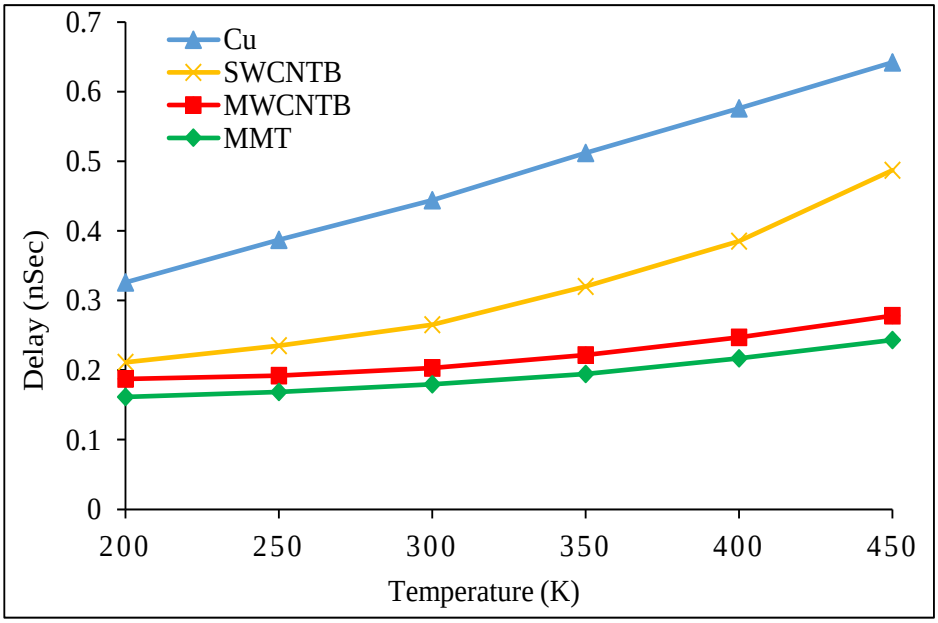
Figure 6.28: PDP reduction in % (MWCNTB to MMT) at DSM technology nodes.

The PDP reduction ($\frac{MWCNTB-MMT}{MWCNTB} * 100$) in % is examined for DSM technology nodes (32, 22 and 16nm) as shown in Figure 6.28. The PDP reduction (%) for temperature ranging from 200 to 450K is calculated as 13.79 to 12.60%, 44.94 to 50.89% and 47.49 to 50.01% at technology nodes as 32, 22 and 16nm, respectively. It concludes that the performance of MMT nanostructure outperform MWCNTB as global level VLSI interconnect at DSM technology nodes for a variable temperature conditions.

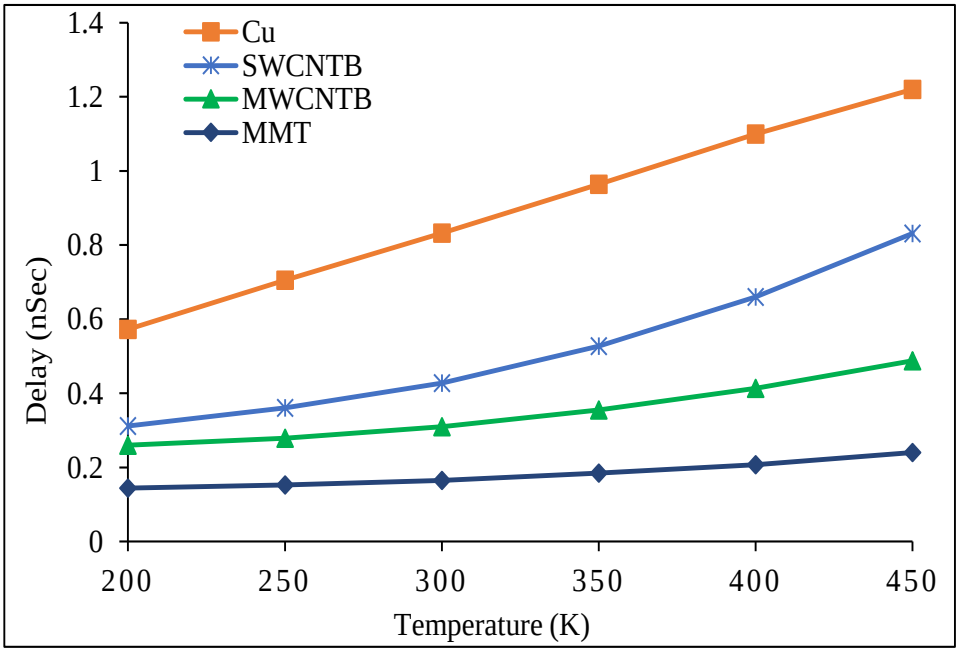
6.3.4 Temperature-dependent performance analysis of MMT, MWCNTB, SWCNTB and Cu interconnects

This sub-section presents temperature-dependent performance of MMT nanostructure, MWCNTB, SWCNTB and Cu for global interconnect length in terms of delay, power and PDP at

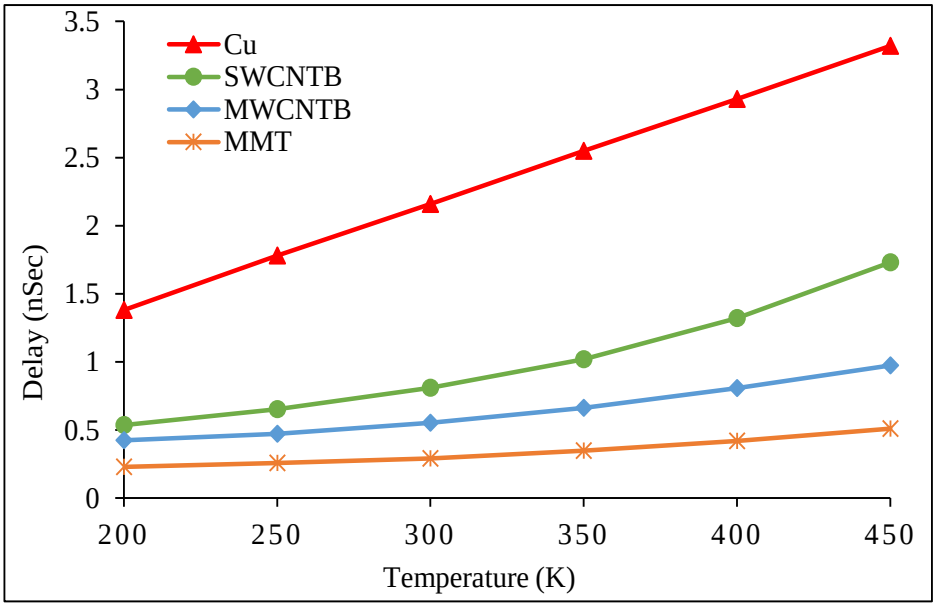
various technology nodes viz. 32, 22 and 16nm. The temperature-dependent impedance parameters of MMT, MWCNTB, SWCNTB and Cu interconnect are calculated by using Eqs. 4.1 to 4.14 as described in Chapter 4, Eqs. 6.12 to 6.18, Eqs. 6.3 to 6.11 and Eqs. 6.1 to 6.4 in Chapter 6, respectively. The temperature-dependent impedance parameters are simulated to examine the performance with the help of SPICE tool, where simulated parameters are considered based on ITRS-2013 for global interconnect length at various DSM technology nodes as 32, 22 and 16nm.



(a)



(b)

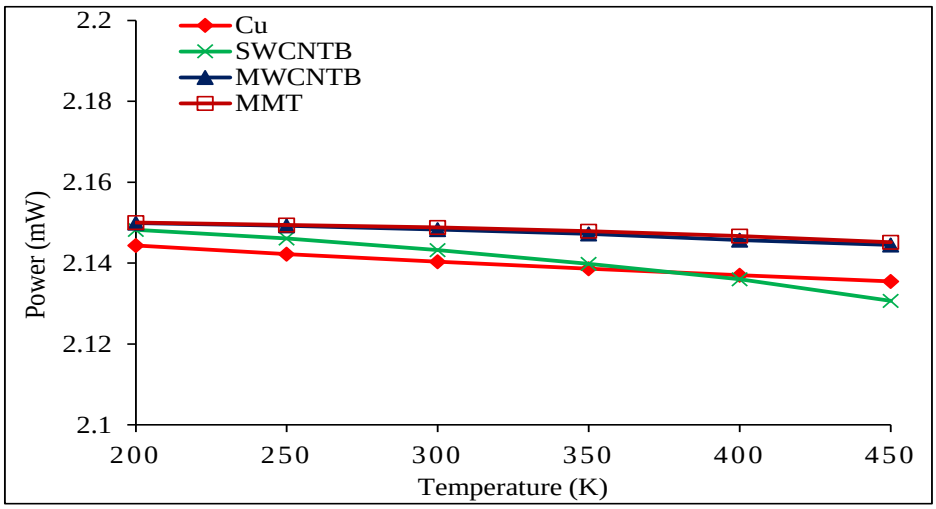


(c)

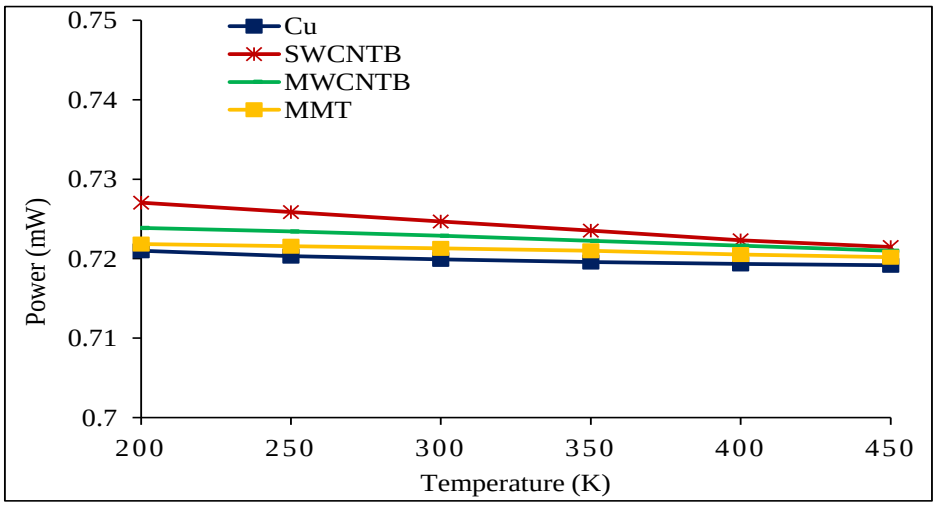
Figure 6.29: Delay comparison of MMT, MWCNTB, SWCNTB and Cu as VLSI interconnect at DSM technology nodes as (a) 32, (b) 22 and (c) 16nm, respectively.

The comparative analysis of the performance in terms of delay for MMT nanostructure, MWCNTB, SWCNTB and Cu as global interconnect length is presented for temperature ranging from 200 to 450K as shown in Figure 6.29 (a) 32, (b) 22 and (c) 16nm technology nodes. It is shown that the delay for MMT, MWCNTB, SWCNTB and Cu interconnect increases with increasing temperature ranging from 200 to 450K at DSM technology nodes viz. 32, 22 and 16nm. It is also revealed that the delay of MMT nanostructure offers less as compared to MWCNTB, SWCNTB and Cu interconnects for all three technology nodes. It indicates that the delay results has significant improvement for increasing temperature at DSM technology nodes. It concludes that the performance of MMT nanostructure is outperformed than MWCNTB, SWCNTB and Cu interconnect for a variable temperature range (200-450K) at 32, 22 and 16nm technology nodes.

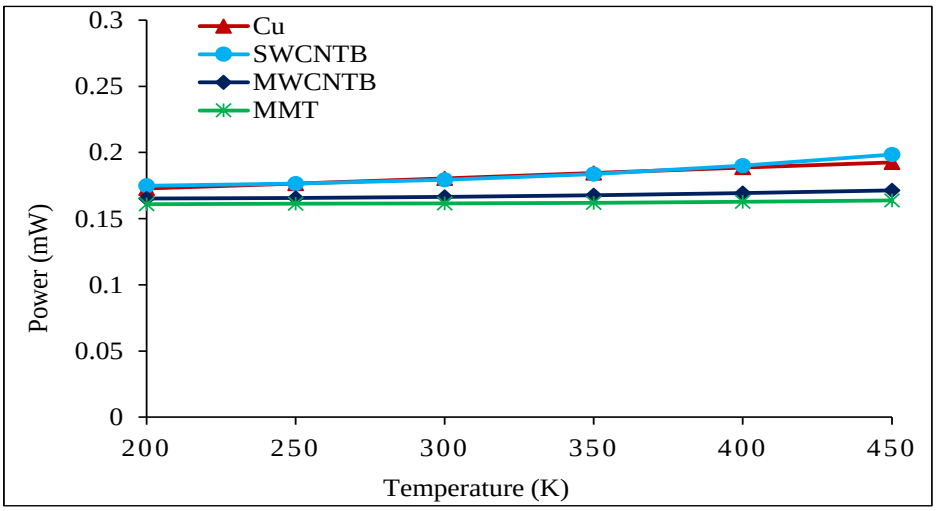
The comparison of power dissipation for MMT nanostructure, MWCNTB, SWCNTB and Cu interconnects is presented for a variable temperature range (200-450K) at 32, 22 and 16nm technology nodes as shown in Figure 6.30. It shows that performance in terms of power for MMT is higher as compared to MWCNT, SWCNTB and Cu interconnect at 32nm technology nodes as shown in Figure 6.30(a). The power consumption is more because of large tube capacitance of CNTs. It is examined that the power dissipation is decreased for scaled-down technology nodes from 32 to 16nm.



(a)

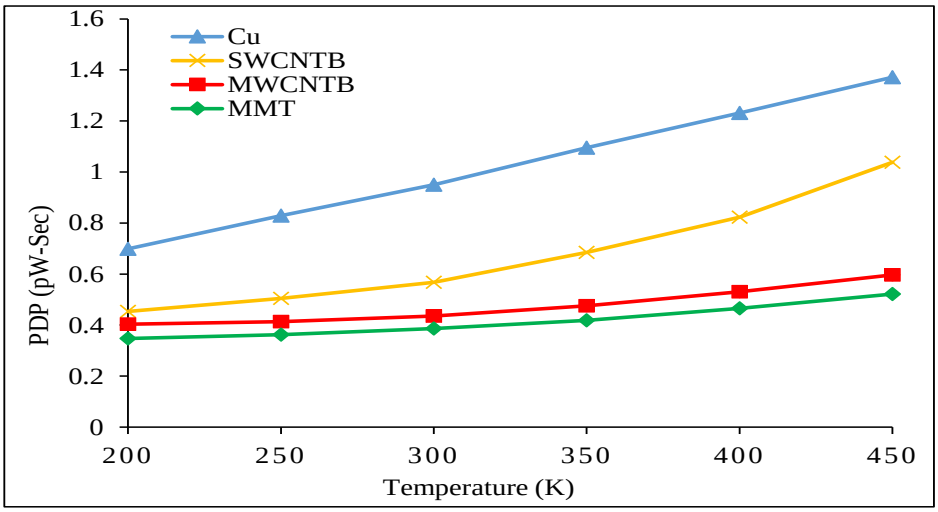


(b)

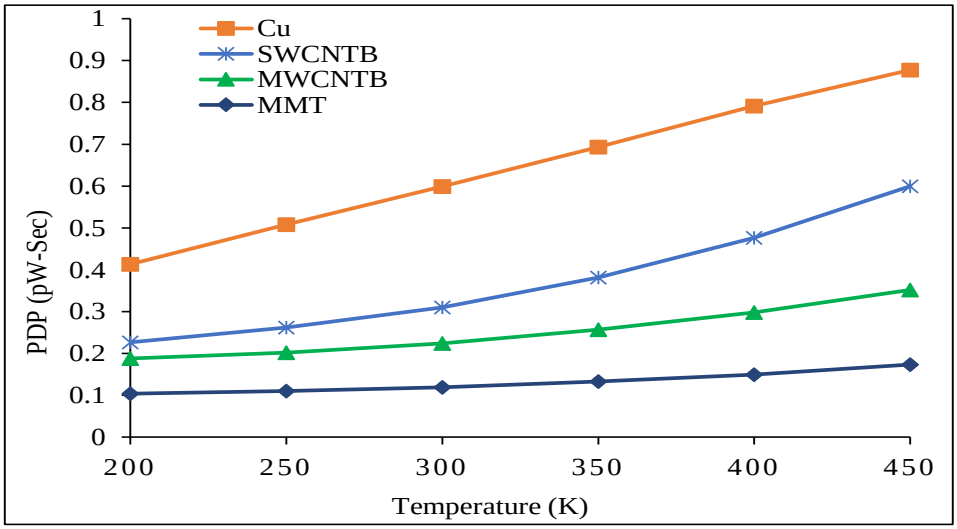


(c)

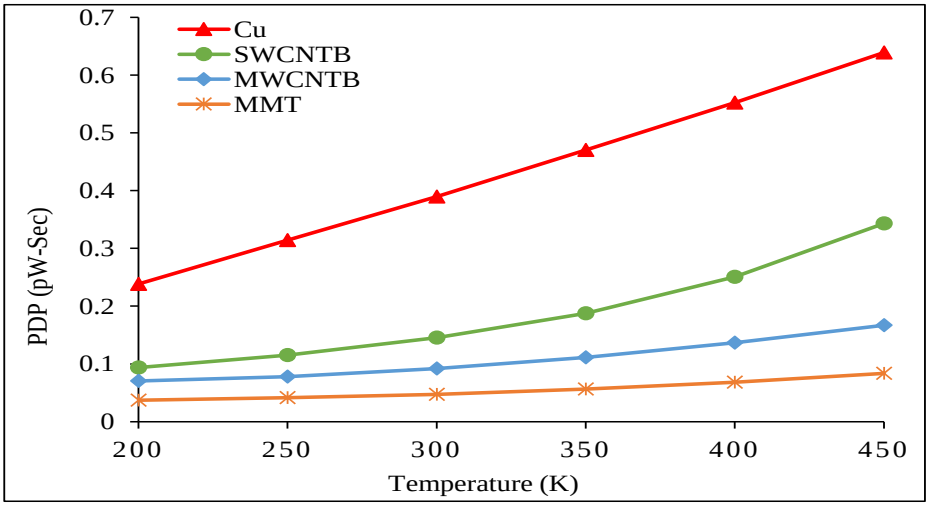
Figure 6.30: Power comparison of MMT, MWCNTB, SWCNTB and Cu interconnects for technology nodes as (a) 32, (b) 22 and (c) 16nm.



(a)



(b)



(c)

Figure 6.31: PDP comparison of MMT nanostructure, MWCNTB, SWCNTB and Cu interconnects at DSM technology nodes as (a) 32, (b) 22 and (c) 16nm.

Figure 6.31 shows the comparison of PDP for MMT, MWCNTB, SWCNTB and Cu interconnects on a variable temperature range at DSM technology nodes. It is examined that the PDP of MMT nanostructure is increased with rising temperature from 200 to 450K, which is shown in Figure 6.31 (a) 32, (b) 22 and (c) 16nm technology nodes. The performance in terms of PDP is significantly improved in favour of MMT nanostructure than MWCNTB, SWCNTB and Cu interconnects at DSM technology nodes. The PDP of MMT nanostructure is decreased with scaled-down technology nodes from 32 to 16nm. It concludes that the performance of MMT in terms of PDP is better than MWCNTB, SWCNTB and Cu interconnects.

Chapter Summary

This chapter presented comparative performance analysis of MMT nanostructure in terms of resistance, delay, power and PDP with the MWCNTB, SWCNTB and Cu interconnect. Temperature-dependent ESC models for MWCNTB, SWCNTB and Cu for global interconnect are presented to calculate impedance parameters at technology nodes viz. 32, 22 and 16nm. The comparative analysis of resistance for MMT is presented with Cu, SWCNTB and MWCNTB at DSM technology nodes on a variable temperature range. The lumped impedance model is converted into a distributed model by inserting number of optimum repeaters with optimum-sized repeater in simulation setup. The repeaters are used to decrease the delay and increasing the driving capacity.

Further, the temperature-dependent parasitic are simulated with the help of simulation setup in SPICE tool to observe the performance of MMT, Cu, SWCNTB and MWCNTB interconnect. The calculated performance in terms of delay, power and PDP for MMT nanostructure is compared with the similar analysis of Cu in Sub-section 6.3.1. It reveals that the performance of MMT performs better than Cu in terms of delay and PDP. Similarly the MMT results are compared with SWCNTB and MWCNTB interconnect in section 6.3.2 and 6.3.3, respectively. It shows that the performance of MMT is better than SWCNTB and MWCNTB interconnect.

For temperature from 200 to 450K, the delay ratio (Cu/MMT) is calculated as 2.01 to 2.64 at 32nm, 3.97 to 5.06 at 22nm and 6.02 to 6.51 at 16nm technology nodes. At scaled-down technology nodes from 32 to 16nm, it is also examined as 2.01 to 6.02 for 200K and 2.64 to 6.51 for 450K temperature. The delay reduction (%) for a variable temperature range 200 to 450K is calculated as 50.4 to 62.1%, 74.8 to 80.2% and 83.3 to 84.6% at technology nodes as 32, 22 and 16nm, respectively. It is also determined for scaled-down technology nodes from

32 to 16nm as 50.43 to 83.39% for 200K and 62.15 to 84.64% for 450K temperature. For temperature ranging from 200 to 450K, the PDP reduction (%) is examined as 50.30 to 61.98% at 32nm, 74.77 to 80.23% at 22nm and 84.54 to 86.93% at 16nm technology nodes.

The delay ratio (SWCNTB/MMT) for temperature ranging from 200 to 450K is calculated for technology nodes 32nm as 1.30 to 2.0, 22nm as 2.16 to 3.45 and 16nm as 2.33 to 3.39. It is also examined for scaled-down technology nodes from 32 to 16nm as 1.30 to 2.33 at 200K and 2.0 to 3.39 at 450K temperature. The delay reduction (%) for temperature range 200 to 450K is determined at technology nodes 32nm as 23.42 to 50.10%, 22nm as 53.72 to 71.01% and 16nm as 57.24 to 70.52%. At scaled-down technology nodes from 32 to 16nm, it is calculated as 23.42 to 57.24% for 200K and 50.10 to 70.52% for 450K temperature. The PDP reduction (%) is calculated as 23.36 to 49.77%, 54.05 to 71.06% and 60.66 to 75.66% for technology nodes viz. 32, 22 and 16nm, respectively.

For MWCNTB and MMT, the delay ratio (MWCNTB/MMT) for temperature 200 to 450K is calculated as 1.16 to 1.14 at 32nm, 1.81 to 2.06 at 22nm and 1.85 to 1.91 at 16nm technology nodes. It is also examined for temperature 200K as 1.16 to 1.85 and 450K as 1.14 to 1.91 at scaled-down technology nodes from 32 to 16nm. For temperature ranging from 200 to 450K, the delay reduction (%) is calculated as 13.79 to 12.63%, 44.78 to 50.84% and 46.09 to 47.68% at 32, 22 and 16nm technology nodes, respectively. It is calculated at scaled-down technology nodes from 32 to 16nm as 13.79 to 46.09% for 200K and 12.63 to 47.68% for 450K temperature. The PDP reduction (%) at temperature ranging from 200 to 450K is calculated as 13.79 to 12.60% for 32nm, 44.94 to 50.89% for 22nm and 47.49 to 50.01% for 16nm technology nodes.

Further, it concludes that the performance of MMT nanostructure as global interconnect length in terms of delay, power and PDP outperforms MWCNTB, SWCNTB and Cu interconnects at all three DSM technology nodes on a variable temperature under consideration. The MMT nanostructure is good replacement of Cu, SWCNTB and MWCNTB for global level VLSI interconnects on a variable temperature range at DSM technology nodes.

Pardeep Kumar Jindal and Karmjit Singh Sandha. Thermally-Aware Modeling and Performance Analysis of Mixed-MWCNTB as Very Large Scale Integrated Interconnects Material for Nano-Electronic Integrated Circuits Design. *"Journal of Nanoelectronics and Optoelectronics"*, 14(9): 1255-1266, 2019. (**Impact factor 1.069**).

Pardeep Kumar Jindal and Karmjit Singh Sandha. Influence of variable temperature on performance of mixed-MWCNT, MWCNT and SWCNT nanostructures as interconnects for high-performance VLSI-IC design. *"Journal of Materials Science: Materials in Electronics, Springer"*, 31(3): 1828-1838, 2020. (**Impact factor 2.478**).

Chapter 7

Conclusion and Future Scope

In this thesis, the proposed analytical and simulation models of MMT nanostructure are used to study performance in terms of delay, power and PDP. A comparative analysis of the obtained results of the proposed MMT nanostructure is performed and summarized with Cu, SWCNTB and MWCNTB as VLSI interconnect material for future interconnect design. This chapter presents the conclusion and future scope of this thesis work in upcoming sections.

7.1 Conclusion

In the thesis, the work is presented to estimate impact of variable temperature on performance of MMT nanostructure as global VLSI interconnect at various DSM technology nodes viz. 32, 22 and 16nm. Initially, a comprehensive study of Cu and various nanostructures of CNT bundle as VLSI interconnect are carried out and presented in the literature. The limitations of Cu and advantages of various CNT bundles as VLSI interconnect at DSM technology nodes on a variable temperature range are discussed and highlighted in the literature review. The impact of variable temperature on performance is deeply studied as presented in the literature for Cu, MWCNTB and SWCNTB interconnect. Several temperature-dependent models are presented for Cu, MWCNTB and SWCNTB as VLSI interconnect at various DSM technology nodes.

The densely packed MWCNTB has created much space vacant at the sidewalls, corners and four adjacent MWCNTs. The MMT nanostructure as VLSI interconnect is proposed by inserting $MWCNT_S$ (small diameter MWCNT) to fill the vacant space among the four $MWCNT_L$ (large MWCNT). Temperature-dependent ESC model is proposed for MMT as global level interconnect, which includes the temperature-dependent scattering phenomena. The effect of temperature on the MFP of MMT nanostructure is included to understand the actual performance using the mathematical expressions written in MATLAB. Temperature-dependent MFPs

are used to calculate impedance parameters and these parasitic are considered to propose RLC model of individual shells of MWCNT. Then, the equivalent single-conductor (ESC) model for MMT nanostructure is established with the help of RLC model of individual shells of MWCNT. All shells of MWCNT are considered to be parallel. The parasitic of MMT nanostructure as global interconnect length is calculated for a variable temperature range (200-450K) at 32, 22 and 16nm technology nodes. The interconnect parameters are considered for DSM technology nodes as per ITRS-2013. It reveals that the resistance of MMT is increased with a decrease in MFP of the individual shell of MWCNT. The MFP decreases due to increase in the collision rate with rising in temperature from 200 to 450K. Therefore, the resistance has significant impact on performance in terms of power and delay on a variable temperature range at DSM technology nodes.

The impact of temperature on performance in terms of delay, power and PDP is analyzed for MMT as global interconnect length (1000μm) at DSM technology nodes viz. 32, 22 and 16nm. The obtained impedance parameters of MMT nanostructure are simulated to examine the performance with the help of simulation SPICE tool. Firstly, the lumped ESC model is converted into a distributed model by splitting it into small sub-sections. The optimum number of repeaters and optimum-sized repeaters are obtained to minimize the delay and power dissipation for all three technology nodes. The simulated parameters and model files are considered ITRS-2013 and Predictive Technology Model (PTM), respectively. The simulation results are analyzed for variable temperature at DSM technology nodes viz. 32, 22 and 16nm.

The simulation results reveal that the performance in terms of delay, power and PDP are increased for MMT nanostructure because of reducing the MFPs on rising temperature from 200-450K at DSM technology nodes viz. 32, 22 and 16nm. The impact of temperature is examined for moderate to higher temperature range (above 300K), and the normalized delay ratio is increased from 1.09 to 1.36, 1.13 to 1.54 and 1.18 to 1.74 for 32, 22 and 16nm technology nodes, respectively. The analysis shows that the performance in terms of delay is influenced more by higher temperature for scaled-down technology nodes from 32 to 16nm. The normalized delay ratio increases significantly for temperatures more than 300K. It concludes that the temperature has a considerable impact on the performance of MMT nanostructure as VLSI interconnect.

The PDP of MMT nanostructure has also been examined for global interconnect length at DSM

technology nodes viz., 32, 22 and 16nm. The PDP of MMT as VLSI interconnect is increasing with increase in temperature ranging from 200 to 450K at 32, 22 and 16nm technology nodes. However, the PDP is decreased with scale-down technology nodes from 32 to 16nm. The normalized PDP ratios are estimated for a variable temperature range 200-450K as 0.90 to 1.36, 0.85 to 15.4 and 0.80 to 1.76 at 32, 22 and 16nm technology nodes, respectively.

The temperature-dependent analytical delay model for MMT and Cu interconnects is presented for variable temperature at DSM technology nodes viz. 32, 22 and 16nm. The obtained results from analytical model are compared with simulation results. It reveals that analytical and simulated results are aligned, and both the results have the same trend at DSM technology nodes on a variable temperature range. The delay of MMT and Cu calculated by analytical and simulation is increased with increasing temperature (200-450K) at 32, 22 and 16nm technology nodes. It is shown that the thermally-aware conditions have a considerable impact on the performance of high-performance VLSI-IC, which needs to be included to get accurate performance.

Further, the comparative analysis has been done for MMT with various structures such as Cu, SWCNTB and MWCNTB interconnect as a function of temperature at DSM technology nodes. The temperature-dependent impedance parameters are calculated from the ESC model of Cu, SWCNTB and MWCNTB for similar parameters as considered for MMT interconnect. Further, these parasitic are simulated with the SPICE tool to examine the performance of Cu, SWCNTB and MWCNTB in terms of delay, power and PDP. The comparison of delay, power and PDP of MMT with similar results of Cu, SWCNTB and MWCNTB are presented at various technology nodes viz. 32, 22 and 16nm.

For Cu and MMT, the improvement in delay reduction (%) for temperature ranging from 200 to 450K is calculated as 50.4 to 62.1%, 74.8 to 80.2% and 83.3 to 84.6% at technology nodes as 32, 22 and 16nm, respectively. The PDP reduction (%) is improved as 50.30 to 61.98% for 32, 74.77 to 80.23% for 22 and 84.54 to 86.93% for 16nm technology nodes at temperature ranging from 200 to 450K. For SWCNTB and MMT, the delay reduction (%) is improved for temperature ranging from 200 to 450K at technology nodes 32nm as 23.42 to 50.10%, 22nm as 53.72 to 71.01% and 16nm as 57.24 to 70.52%. The improvement in PDP reduction (%) is examined as 23.36 to 49.77% at 32nm, 54.05 to 71.06% at 22nm and 60.66 to 75.66% at 16nm technology nodes. For MWCNTB and MMT, the delay reduction (%) is obtained, which is improved for technology nodes 32nm as 13.79 to 12.63%, 22nm as 44.78 to 50.84% and

16nm as 46.09 to 47.68% at temperature ranging from 200 to 450K. The improvement in PDP reduction (%) is calculated as 13.79 to 12.60% for 32nm, 44.94 to 50.89% for 22nm and 47.49 to 50.01% for 16nm technology nodes on a variable temperature ranging from 200 to 450K.

The delay and PDP (ratio and reduction) of MMT to Cu, SWCNTB and MWCNTB interconnect are examined, which shows that the ratio of Cu to MMT is highest, SWCNTB to MMT is medium and MWCNTB to MMT interconnect is least. It reveals that the performance of MMT is better than MWCNTB, MWCNTB outperforms SWCNTB and SWCNTB performs better than Cu interconnect. The same trend is indicated in the literature review. The results indicate that the performance of MMT nanostructure is better as compared to Cu, SWCNTB, and MWCNTB interconnect for entire temperature range at DSM technology nodes (32, 22 and 16nm).

Summary

MMT nanostructure is performed better than Cu, SWCNTB and MWCNTB for intermediate (semi-global) and global interconnects lengths. It may be considered as the future of interconnect to design high-performance VLSI-ICs at DSM technology nodes. It is necessary to include impact of temperature to get the accurate performance of MMT interconnects for thermally-aware environmental conditions.

7.2 Future Scope of Work

This thesis presents the limitations of Cu, SWCNTB and MWCNTB interconnect at DSM technology nodes on variable temperatures for global interconnect. To overcome these drawbacks, the MMT nanostructure as VLSI interconnects is proposed as the future of VLSI interconnects for high-performance IC design. The impact of temperature is also included to present ESC model for MMT nanostructure at 32, 22 and 16nm technology nodes. The comparative analysis has been performed for MMT with Cu, SWCNTB and MWCNTB interconnect. It concludes that the performance of MMT nanostructure is better than Cu, SWCNTB, and MWCNTB as global interconnect length at 32, 22 and 16nm technology nodes for a variable temperature ranging from 200 to 450K in the design of high-performance VLSI-ICs. Therefore, the performance of VLSI-ICs could further be improved by exploring the other parameters of the proposed area. The following ideas are explored in the future

1. For DSM technology nodes, interconnects are highly denser, which causes to increase the coupling between nearby interconnect lines. Thus, the influence of temperature on crosstalk for MMT nanostructure needs to examine for global interconnect length.

2. Impact of tunneling conductance on the performance of MMT nanostructure as VLSI in terms of delay and power dissipation at advanced technology nodes.

3. The impact of shell diameters for MWCNTs on the performance of VLSI interconnect at DSM technology nodes.

4. The manufacturing of CNT based interconnects are the major challenge due to their growth process and needs to be taken care of in future work.

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