COMMON-MODE VOLTAGE STATUS IN THREE - LEVEL FIVE - PHASE INVERTER

A Dissertation submitted in fulfillment of the requirements for the Degree of

MASTER OF ENGINEERING
in
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Submitted by

JOSHIKA RANI
802042011

Under the Guidance of
Dr. YOGESH TATTE
Assistant Professor, EIED

THAPAR INSTITUTE
OF ENGINEERING & TECHNOLOGY
(Deemed to be University)

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Electrical and Instrumentation Engineering Department
Thapar Institute of Engineering & Technology, Patiala
(Declared as Deemed-to-be-University u/s 3 of the UGC Act., 1956)
Post Bag No. 32, Patiala – 147004
Punjab (India)

DECLARATION

I hereby certify that the work which is presented in dissertation entitled, **Common-Mode Voltage Status in Three-Level Five-Phase Inverter**, in partial fulfillment of the requirements for the award of the degree of Master of Engineering in Power Systems, submitted to Electrical & Instrumentation Engineering Department of Thapar Institute of Engineering & Technology (Deemed to be University) is as authentic record of my own work carried under the supervision of **Dr. Yogesh Tatte**. It refers others researcher's work which are duly listed in the reference section. The matter contained in this dissertation has not been submitted, neither in part nor in full to any other degree to any other university or institute except as reported in text and references.

Place: Patiala **JOSHIKA RANI**
Date: 31-08-2022 **Roll No.: 802042011**

It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

(Dr. Yogesh Tatte)
Assistant Professor, EIED

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Joshika Rani

Joshika Rani
802042011

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LIST OF ABBREVATIONS

ANPC	-	ACTIVE NEUTRAL POINT CLAMPED
CHB	-	CASCADED HYBRID BRIDGE
CMV	-	COMMON MODE VOLTAGE
DC	-	DIRECT CURRENT
DTC	-	DIRECT TORQUE CONTROL
EMI	-	ELECTROMAGNETIC INTERFERENCE
IGBT	-	INSULATED-GATE BIPOLAR TRANSISTOR
ML1	-	MULTILEVEL INVERTER
MMC	-	MODULAR MULTILEVEL CONVERTER
NPC	-	NEUTRAL POINT CLAMPED
SPWM	-	SINUSODIAL PULSE WIDTH MODULATION
SVPWM	-	SPACE VECTOR PULSE WIDTH MODULATION
THD	-	TOTAL HARMONIC DISTORTION
VAR	-	VOLT-AMPS REACTIVE
VSI	-	VOLTAGE SOURCE INVERTER

ABSTRACT

The common-mode voltage (CMV) is one of the main reasons for the flow of bearing currents in induction motors (IM). This mainly leads to the bearing failure and causes severe problems. The CMV is one of the major issues in NPC inverters. It causes rise of bearing current in motor, which leads to damage and shortens the lifetime of the motor. In addition, the CMV can also be the cause for increases in electromagnetic interference issues. In this work three-level five-phase inverter (TL-FPI) is used for the study of CMV elimination because TL-FPI offers more voltage vectors than its two-level counterpart. The space vector pulse width modulation (SVPWM) technique is developed for the elimination of CMV, only those switching states are selected which give zero CMV. The selection of TL-FPI is based on availability of those voltage vectors which eliminate the CMV. There are two types of voltage vectors available in TL-FPI, via vertex and non-vertex voltage vectors. These vertex voltage vectors do not eliminate CMV, whereas non-vertex voltage vectors eliminate CMV. There are forty non-vertex voltage vectors along with one zero voltage vector available to eliminate the CMV. In this work two different methods are presented. In first method large and zero voltage vectors are selected to get CMV elimination and maximum DC link. In second method large, medium and zero voltage vectors are selected to get elimination of CMV and *x*-*y* stator plane. Both the simulation and experimental results are given to validate the methods.

CHAPTER 1
INTRODUCTION

1.1 OVERVIEW

An inverter plays a very important role in the field of variable speed drives and industrial applications. Multilevel inverter topologies are being used due to their advantages such as reduced CMV, minimized output harmonics in voltage and current, lower switching losses, reduced EMI problems and reduced voltage stresses across the switches. The multiphase system plays an important role in various applications such as marine propulsion, hybrid electric vehicles and electric traction due to its reduced torque ripple, improved fault tolerance and higher torque density. Multi-level inverters are used for multipurpose uses such as active filter, static VAR compensator and large motor drives. When the number of levels is increased, this leads to a huge increase in switching devices, making the inverter more complex and expensive. Among the various multilevel inverter topologies, the NPC three-level inverter has multiple advantages such as voltage stress reduction, a single DC source effectively shared by three phases and capacitor voltage balancing. Major research work on multilevel inverters focuses on pulse width modulation methods used to improve the performance of the inverter circuit.

CMV is one of the main problems in a NPC inverters. It causes increase of bearing current in the motor, which leads to damage the motor bearing and shortens the life of the motor. Furthermore, CMV can also be the cause of the increase in electromagnetic interference problems. Therefore, it is very important to reduce the CMV level in NPC inverters. Numerous solutions have been presented to address the minimization of the CMV level such as the use of filter circuits, multi-carrier SPWM, space vector modulation, SPWM with interleaved carriers and phase shift method. Generally, pulse width modulation (PWM) is implemented to control the power switches located in the drive topology. Among them, SVPWM techniques and carrier-based modulation techniques mainly preferred PWM techniques.

SVPWM is a widely used method among various multilevel inverter modulation techniques, which improves inverter performance and better utilization of DC link voltage. Although the SVPWM implementation is complicated in terms of computing the switching time and identifying the reference vector in a complex spatial region. The SVPWM control strategy is implemented to minimize the DC current balance and CMV level in the inverters with parallel current source in steady state and transient state conditions. SVPWM was developed for multilevel converters to improve various factors such as computation time, voltage distortion, DC link current balance and neutral current elimination.

1.2 BACKGROUND

1.2.1 DEVELOPMENT OF MLI TOPOLOGIES

A thorough study of MLI evolution has been discussed in this section. CHB was first developed by Baker and Bannister in the 1970s, which possessed the capability of generating multilevel voltage using different DC source voltage. The next advancement in MLI topology was the NPC inverter, first evolved by Nabae et al. in the 1980s. In the 1990s, Maynard and Foch and Lavieville et al. developed the FC type of MLI. These three classical types of MLI-based topologies were regarded as the foundation of most MLI inverters presented in the modern era. The next invention was the modular multilevel converter (MMC), primarily applied in industrialization. In 2000, a generalized MLI named P2 was introduced. Many other new MLI configurations with application-based approaches have been proposed and conferred in the recent past. Authors have also focused on developing a new reduced switch count topology of MLI.

MLI can be categorized as (i) symmetric type based on the use of equal DC sources; (ii) asymmetric type based on the use of unequal DC sources; (iii) having inherent negative level (iv) without inherent negative level; (v) use of capacitors links with single sources; (vi) regenerative configuration for operation as both an inverter and a rectifier and (vii) hybrid approach of NPC, FC and CHB

1.2.2 CLASSICAL AND NEW REDUCED SWITCH COUNT MLI TOPOLOGIES

The concept of MLIs was first introduced in 1975 and then pursued by combative work to develop numerous topologies based on modifying the configuration regarding arrangements of power electronic semiconductor switches and DC sources. Research was also conducted to achieve greater power by the series combination of switches using DC sources with a small voltage range to convert power and synthesize voltage. The most frequently used voltage sources which could be configured in single and multiple units are RER, batteries and capacitors. The broad categorization of MLI on several DC sources used and their structure is given in Fig. 1.1. In addition, a comprehensive survey of the literature yields various classifications of MLI based on different strategies as suggested by many researchers.

- **Single DC Source**

  This type of topology is extensively endorsed in the industrial field, considering its simple structure, high efficiency, and power rendering.

- **Neutral Point Clamped Multilevel Inverter (NPC-MLI)**

  Nabae, Takashi, and Akagi in 1981 proposed the diode clamped multilevel inverter (DC-MLI), also termed NPC-MLI. These inverters have been broadly adopted on account of their immense proficiency in high-power and medium-voltage operations with comparatively high efficiency. It is a three-level structure with two diodes that clamp the switching voltage to half the supply voltage magnitude. Further, it guarantees equal sharing of the supply voltage among the two halves of the switches being held at these points consisting of a neutral point between them. The middle voltage level is termed the neutral point. This topology employs multiple capacitor banks in series for providing multiple DC voltage levels. NPC inverters are a family of multilevel power converters that are characterized by the use of clamping diodes for guaranteeing the proper voltage sharing across the power switches. NPC inverters offer superior waveform quality compared to two-level inverters, leading to reduced filtering requirements. They are often present in medium voltage applications, where their superior blocking voltage capability is also an essential requirement. However, the industrial use of NPC-type inverters is mostly limited to three-level topologies, due to the complex mechanical arrangement of the power devices with a higher number of levels [1-7].

The main advantages of NPC topology are:

(i) The need for the converter capacity is reduced as all sections share a standard DC bus.

(ii) Improved ability to reduce THD.

(iii) Provides high efficiency.

(iv) A number of switches, clamping diodes and capacitors can be upgraded to achieve higher power levels.

However, this topology faces some problems such as:

(i) Start-up costs may be increased as additional reactors are required to reduce the high levels of electricity and current THD as this topology uses a basic frequency switch.
(ii) Although the voltage level can be increased by improving the number of capacitors and clamping diodes. Increases the complexity of the whole configuration.

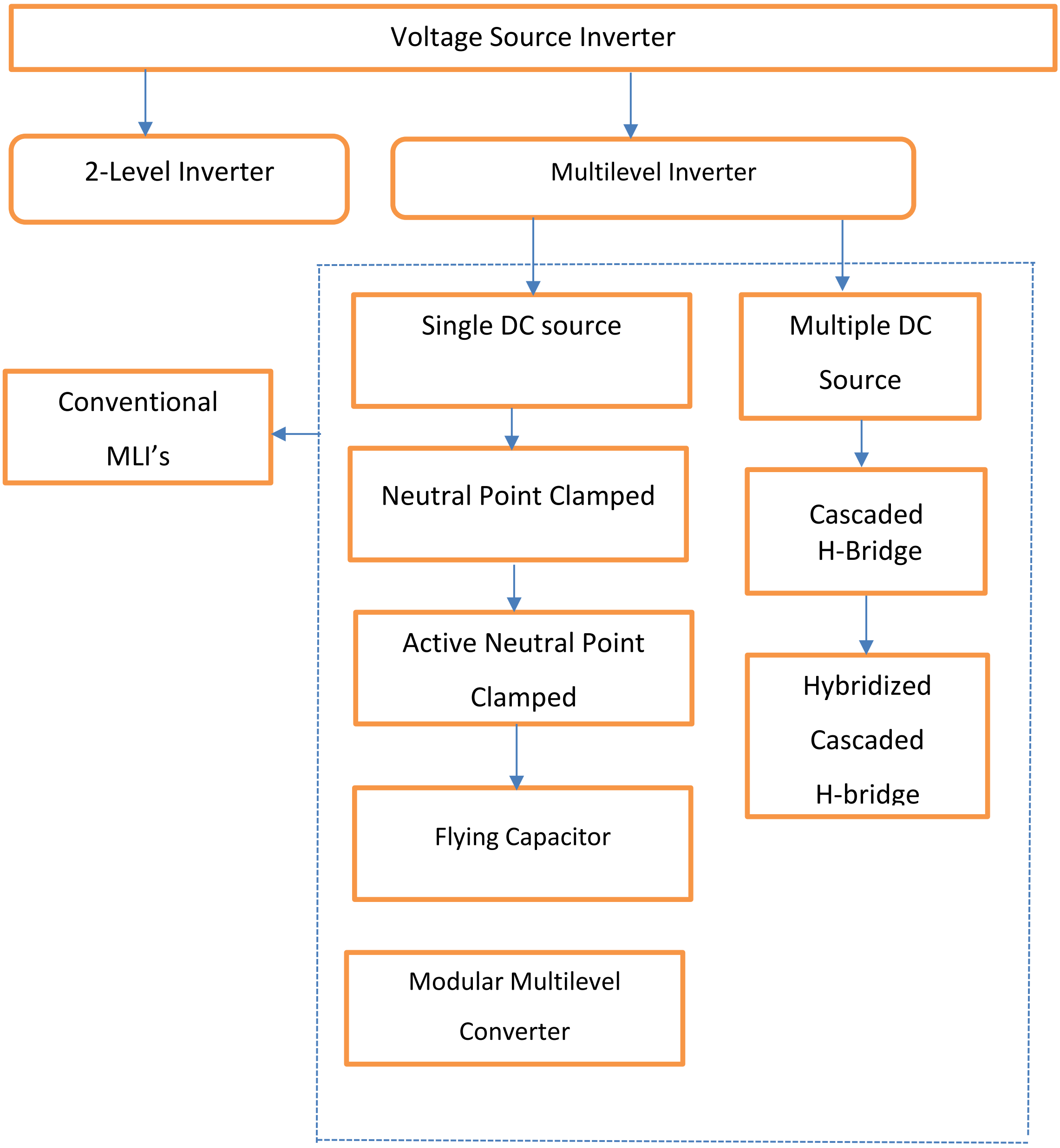

Fig. 1.1 Overall classification of MLI

1.3 MODULATION TOPOLOGIES

The basic structure of a multilevel power converter is formed by small discrete DC-voltage sources. The modulation strategies can be divided into two parts: Fundamental switching frequency and high switching frequency PWM. The latter part is the main focus in this chapter, because this is the part that is relevant for high voltage conversion. There are several different PWM methods.

Here, some of the most common modulation topologies are discussed. Type of modulation is selected based on following requirements:

- Minimization of harmonics of load current and switching frequency.
- Provide uniform switching frequency for all switching devices and balanced DC capacitor voltage.

Different PWM schemes - approaches have the same goal: To reduce the THD of the current. Increase in switching frequency reduces the lower-harmonics, which contributes to a lower THD, achieving the goal of a voltage output waveform with the requested RMS values and frequency and a sinusoidal waveform resemblance. Turning the switches ON and OFF creates pulses with the same amplitude but with different width. These pulses are generated in the output to replace the sinusoidal waveform. The easiest way of creating this is by using a intersection method, comparison with a sawtooth/triangle waveform (carrier wave). When the reference wave (sinus) is larger than the triangular waveform, the PWM signal is switched ON (value: 1) and when it is smaller it is switched OFF (value: 0).

The most common method is called the SPWM. Although it is commonly used, it has a big disadvantage – it has low output voltage. There are however other methods that can meet these demands in a better way, using similar carrier-based systems with different forms as shown in Fig. 1.2.

- **Trapezoidal modulation**:
  Differentiation of a triangular wave and a modulating trapezoidal wave.

- **Staircase modulation**:
  The modulation signal is formed as a scale and the levels are calculated to eliminate some harmonics. Not recommended for cycles with less than 15 pulses.

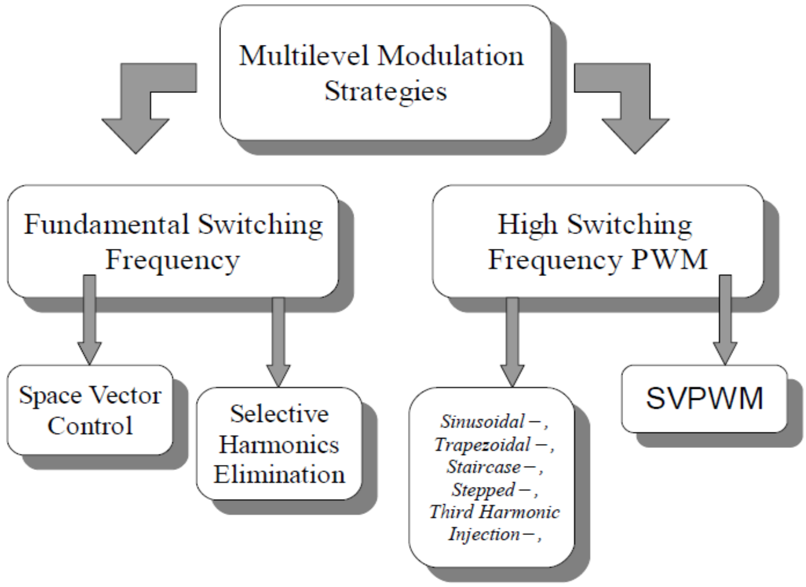

Fig. 1.2 Overview of different modulation strategies

- **Stepped modulation**:

  Each step is a certain portion of time (in degrees) that individually controls amplitude and is used to eliminate harmonics. Provides low distortion, but high amplitude.

- **Third harmonic injected PWM**:

  Implementation in the same way as for the SPWM, but the references signal is not a sinusoidal wave. It consists of a 1) fundamental component 2) Third harmonic component. This method gives higher amplitude and a better utilization of the DC-source.

- **Space vector pulse width Modulation:**

  SVPWM generates the appropriate gate drive waveform for each PWM cycle. The inverter is treated as one single unit and can combine different switching states (number of switching states depends on levels). The SVPWM provides unique switching time calculations for each of these states. This technique can easily be changed to higher levels and works with all kinds of multilevel inverters (cascaded, capacitor clamped, diode clamped). The three vectors that form one triangle will provide duty cycle time for each, giving the desired voltage vector (V_{ref}). SVPWM also have good utilization of the DC link voltage, low current ripple and relative easy hardware implementation. Compared to the SPWM, the SVPWM has a 15% higher utilization ratio of the voltage. This feature makes it suitable for high voltage high power applications such as renewable power generation. As the number of level increase the redundant switching states increases and also the complexity of selection of the switching states. So, deciding which level is right for a certain application it is important to find a balance between losses and specification of the positioning of the reference vector.

1.4 LITERATURE SURVEY

In 2015, Saifullah Payami et al. proposed the elimination of CMV that are generated due to pulse width modulation (PWM). In this technique the CMV is eliminated in three-level inverter using some non-vertex vectors [8].

In 2016, B.Sakthisudhursun, Jay K. Pandit and M.V. Aware proposed the simplified space vector pulse width modulation (SVPWM) for a three-level five-phase inverter. The proposed method generates the duty cycle of the three-level inverter switches based on dwell times of the two-level inverter and carrier index [9].

In 2017, Quoc Anh Le and Dong-Choon Lee proposed reduction of common-mode voltages for five-level active NPC inverters by the space vector modulation technique which decreases the peak value of the CMV to one-twelfth of the DC-link voltage [10].

In 2018, Namina Soulahi et al proposed comparison between a two-Level and three-level inverter fed induction motor including losses and efficiency. In this paper, losses, efficiency and THD depending on the switching frequency are investigated and induction motor is used as a load [11].

In 2018, E. Levi, R. Bojoi, F. Profumo, H. Toliyat, and S. Williamson, proposed multiphase induction motor drives and also technology status review which advise about working of multiphase induction drive [12].

In 2018, L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo and M. A. M. Prats, proposed the age of multilevel converters arrives which discussed the different level of converter [13].

In 2018, L. B. Zheng, J. E. Fletcher, B. W. Williams and X. He, proposed dual-plane vector control for a five-phase induction machine for an improved flux which discuses about the different parameter to control the flux [14].

In 2018, C.M. Hutson, G.K. Venayagamoorthy and K.A.Corzine discussed about the optimal SVM switching for a multilevel multiphase machine using modified discrete PSO [15].

In 2019, Arpan Hota et al. proposed an improved three-phase five-level inverter topology with reduced number of switching power devices and the topology also benefits with reduced switching and conduction loss. An algorithm is also devised to generate the switching pulses for the bus and the 3-LI, using a carrier-based space vector modulation technique [16].

In 2019, O. Lopez, J. Alvarez, J. Doval-Gandoy and F. D. Freijedo discussed about multilevel multiphase space vector PWM algorithm with switching state redundancy. It tells about the algorithm of SVPWM and how to implement in three level inverter topology [17].

In 2019, M. M. Renge and H. M. Suryawanshi discussed about the three-dimensional space-vector modulation to reduce common-mode voltage for multilevel inverter. In this paper, an approach to reduce common-mode voltage (CMV) at the output of multilevel inverter using three dimensional space-vector modulation (SVM) is proposed [18].

In 2019, Palanisamy Ramasamy and Vijayakumar Krishnasamy proposed the minimization of common mode voltage for five-phase three-level inverter using SVPWM strategy in which 116 switching states are used to minimize the CMV level and to obtain the desired output voltage levels. The CMV is reduced up to $\frac{V_{dc}}{6}$ [19].

In 2020, Bheemaiah Chikondra et al. proposed the performance comparison of three-level five-Phase NPC with two-Level five-Phase VSI and examine various aspects like CMV, voltage and current THD, switching losses, conduction losses, and efficiency under the steady-state and dynamic loading conditions over a wide range of the modulation index action of the feeding power converters [20].

In 2022, Bheemaiah Chikondra, Utkal Ranjan Muduli and Ranjan Kumar Behera proposed improved DTC technique for THL-NPC VSI Fed five-phase induction motor drive based on VVs assessment over a wide speed range in which DTC utilizes the appropriate non-vertex voltage vectors to form VVs that neutralize the average volt-second in the *x-y* plane, maintain DC-link capacitor voltage balancing and limits the switching voltage stress [21].

1.5 RESEARCH GAP

- The two-level five-phase inverter has only 32 vectors which could not eliminate the common mode voltage.
- The CMV translates into common mode currents (CMC) which through the capacitance between the different parts of the induction motor drives and the ground flow to ground. This can cause motor bearing failure, unexpected operation of earth current protection relays, and electromagnetic disturbances which can lead to tripping of complete induction motors. Due to these drawbacks, the five-phase induction motor drive may lose its reliability.
- The three-level five-phase inverter has 243 voltage vectors which has different CMV status from $\frac{V_{dc}}{2}$ to $0\ V_{dc}$.

1.6 STATEMENT OF PROBLEMS

- The vertex voltage vectors in three-level five-phase inverters generate the CMV.
- The two-level five-phase generate more CMV because of the availability of only vertex voltage vectors.
- CMV may cause non reliable operation of three-level five-phase inverter.

1.7 OBJECTIVES

- To study the three-level five-phase inverter.
- To study the three-level five-phase induction motor drives.
- To implement hardware prototype of three-level five-phase inverter.
- To eliminate the common-mode voltage in five-phase system.

CHAPTER 2
THREE-LEVEL FIVE-PHASE INVERTER

2.1 OVERVIEW

In a balanced five-phase system, the five stator phase groups are distributed with a spacing of 72^0. The cage rotor is similar to that used in a three-phase motor. The stator coils when excited by balanced five-phase sinusoidal supply produce a rotating magneto motive force (MMF) of constant amplitude. The revolving field causes rotor reaction and produces useful torque. It is not easy, however, to obtain pure sinusoidal voltages from static inverters. The inverter output voltage contains time harmonic components which inject harmonic currents into the machine stator windings. The five-phase connection eliminates the fifth and other quintuple-order harmonics. The successive harmonic components in the machine phase voltage of a five-phase induction motor fed from a five-phase square wave inverter are of order (10n + 1), (10n + 3), (10n + 7), (10n + 9) (where n = 0, 1, 2, 3, -). Their amplitude will be inversely proportional to their harmonic order. When the space sequence of the machine winding is connected to a, b, c, d & e the fundamental (with sequence a b c d e) and other (10n + 1) order harmonics produce rotor reaction and positive torque, 2) the (10n + 9) order harmonics produce rotor reaction but negative torque and 3) the (10n + 3) and (10n + 7) order harmonics produce no rotor reaction. Accordingly, the lower order harmonics which produce rotor reactions are the ninth, eleventh, nineteenth, and twenty-first while the harmonics that do not produce rotor reaction are the third, seventh, thirteenth, and seventeenth. Among these, the third harmonic is the strongest, and it will not get sufficiently filtered by the leakage inductance of the motor. As a consequence of these harmonics, the phase current of the five-phase machine will be very much distorted compared to the sinusoidal shape. The torque pulsations in the five-phase drive are produced by the interaction of rotor flux produced by the (10n + 1) and (10n + 9) order harmonics with the fundamental revolving air gap flux. The rotor MMF's due to (10n + 1) order harmonics revolve in the forward sequence, and those due to (10n + 9) order harmonics revolve in the backward sequence. In both cases, the torque ripples produced will have a frequency of order 10n. Because of the reduced amplitude of the ninth- and eleventh-order harmonics and the increased frequency of torque pulsations, the torque ripple behavior of five-phase drive is inherently superior to that of a three-phase drive.

Low voltage switches can be used in multi-level inverters. These are faster, smaller and cheaper than high voltage switches used in 2-level inverters. When switches are in series, they withstand higher voltages. Multilevel inverters offer better sinusoidal voltage waveform than 2-level inverters due the fact that output voltage can be formed using more than two voltage levels. This causes the THD to be lower. Switching losses are reduced because switching frequency can be lower than in 2- level inverter and also the switching speed is faster with low voltage switches than with high voltage switches that are usually needed in 2-level inverters. Conduction losses are also lower because of low forward-voltage drop. When several voltage levels are used, the *dv/dt* of the output voltage is smaller thus the stress in cables and motor is smaller. In two-level five-phase inverter, which consists of 5 phases (5 legs) and each phase contains 2 switches. Each leg can be operated in 2 switching states like $+\frac{V_{dc}}{2}$ and $-\frac{V_{dc}}{2}$ as shown in Fig. 2.1.

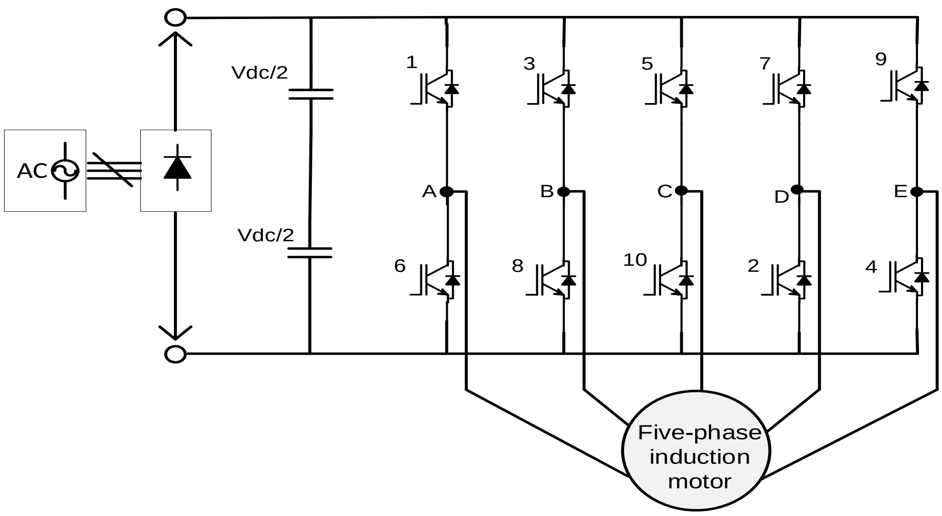

Fig. 2.1 Two-level five-phase inverter

The three-level NPC type of MLI is widely used in the application of motor drive. The multilevel inverter scheme combined the very small step of staircase output voltage from numerous levels of the DC capacitor voltage variations. A k level NPC-MLI inverter contains (k-1) capacitors on DC bus link, 2 (k-1) power switching vector devices per phase and 2 (k-2) variable clamping diodes per phase as shown in Fig.2.2. The capacitors used in 3-level inverter are C1 and C2, which divides the DC bus voltage split into 3-level. Each capacitor divides voltage as $\frac{V_{dc}}{2}$ volts and voltage pressure will be inadequate to one capacitor level throughout clamping diodes. In this proposed system, which consists of 5 phases (5 legs) and each phase contains 4 switches. Each leg can be operated in 3 switching states like $+\frac{V_{dc}}{2}$, $0\ V_{dc}$ & $-\frac{V_{dc}}{2}$ shown in Table 2.1. This inverter has the advantages which are as follows:

- The concentrated peak value and improved switching frequency.
- The system with enhanced power density.
- The total harmonic distortion is less.
- The power divisions between the inverter legs are enhanced.
- Current harmonics and capacitor balancing also reduced.

The switching states of NPC inverters depends on n^m, where n- no. of levels and m- no. of phases. In three-level five-phase NPC inverters, this contains totally 3^5 = 243 switching states are available. It has two dc link capacitors connected in the inverter switches.

Table 2.1 Switching states of three-level inverter

States	**Switching States**				**Terminal Voltage**
	Sa1	**Sa2**	**Sa3**	**Sa4**	
2	ON	ON	OFF	OFF	$+\frac{V_{dc}}{2}$
0	OFF	OFF	ON	ON	$-\frac{V_{dc}}{2}$
1	OFF	ON	ON	OFF	$0\ V_{dc}$

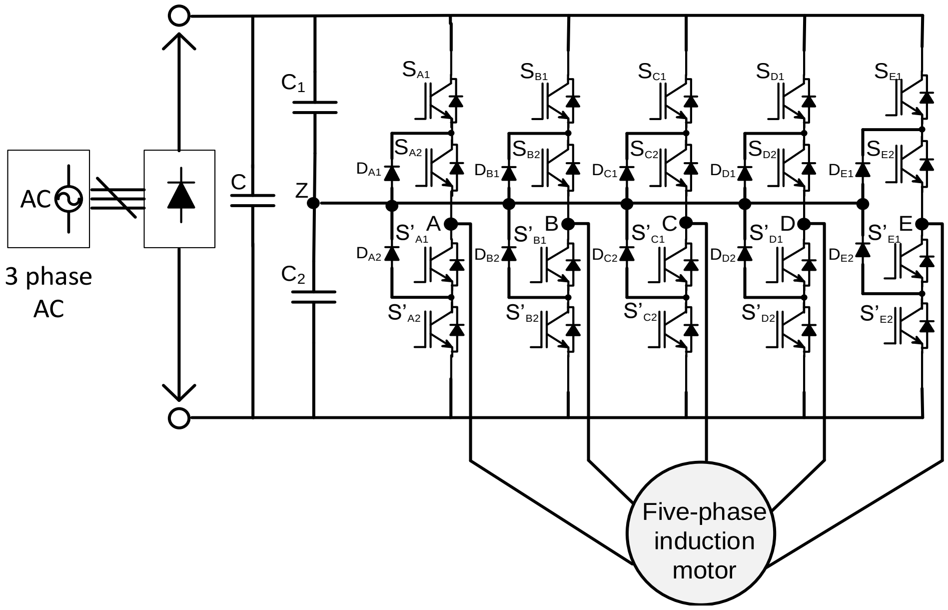

Fig. 2.2 Three-level five-phase inverter with load

The three-level NPC inverter offers the following features:

- There is no any dynamic voltage sharing problem. Each of the switches in the NPC inverter withstands only half of the total dc voltage during interchange.
- The static voltage equalization without using extra components. The static voltage equalization can be attained when the leakage current of the top and bottom switches in an inverter leg is selected to be lower than that of the inner switches.
- The less THD and *dv*/*dt*. The waveform of the line-to-line voltages is composed or five voltage levels, which leads to less THD and *dv*/*dt* in comparison to two-level inverter operating at the same voltage rating and device switching frequency.

Advantages and disadvantages of three-level Inverter:

Advantages:

- The multilevel inverters produce common mode voltage reducing the stress and don’t damage the motor.
- The multilevel inverter can draw input current with minimum distortion.
- The selective harmonic elimination technique along with the multilevel topology results the THD becomes the lower in the output waveform without using filter circuit.
- The flow of reactive power can be controlled.
- Common dc bus shared by all the phases.

Disadvantages:

- There is need of high voltage rating diodes to block the reverse voltages.
- Increment of circuit with the increment in the number of output voltage levels.

2.2 COMPARISON BETWEEN TWO-LEVEL AND THREE-LEVEL INVERTER

Compared to three-level five-phase inverter two level inverter has 32 voltage vectors. The conventional two-level inverters fail to operate in the medium voltage range due to the semiconductor’s blockage voltage limitation. However, three level inverter play a key role in medium-voltage and high-power operations. Further, for the same power ratings, three level inverter has merit over a two-level inverter in terms of reduced harmonic contents of line-to-line voltage that are fed to load with respect to its level of switching frequencies. The cost and power losses were compared in two-level and three-level converters. It was discovered that the two-level configuration is 27% cheaper than the three-level configuration, but the power losses are 44 % higher in a two-level converter than in a three-level converter. The most suitable three-level topology for wind power application is diode clamped inverter because it can use only one DC-bus from where the different voltage levels are produced by capacitors in series. In high-power and high-voltage applications these two-level inverters however have some limitations in operating at high frequency mainly due to switching losses and constraints of device rating. This is where multilevel inverters are advantageous. Increasing the number of voltage levels in the inverter without requiring higher rating on individual devices can increase power rating. The unique structure of multilevel voltage source inverters' allows them to reach high voltages with low harmonics without the use of transformers or series-connected synchronized-switching devices. The harmonic content of the output voltage waveform decreases significantly. The primary reasons behind the three level inverter serving as a vital revolution in the era of industrialization for potent performance are as follows:

(i) Compatible in design.
(ii) Capability of operating at higher current and voltage due to its modular structure.
(iii) Lesser voltage derivatives on power electronic switches as the voltage stress gets divided across the switches at various levels.
(iv) Easy interface with RER and motor drives where the load sharing is brought about by DC link.
(v) Enhanced power quality performance with low harmonic content and better electromagnetic compatibility.
(vi) It produces lower common-mode voltage.
(vii) Ability of transformer-less operation.
(viii) Enhanced efficiency level due to switching at fundamental frequency thus decreasing losses due to conduction and switching.
(ix) It draws input current with fewer distortions.
(x) It uses various control approaches and reduced switching states for achieving fault-tolerant operation.

Table 2.2 Primary differences between a traditional two-level inverter and the three-level inverter

Properties	**Two- level Inverter**	**Three- level Inverter**
Structure	Complicated	Modular
Operation at high voltage and current	Can operate (for parallelized structures)	Can operate
Stress on power electronic Switches	More	less
Application	Low voltage	High Voltage
Performance of power quality	Low	High
Harmonic content	Low	High
EMI Immunity/Susceptibility	Less	More
Production of CMV	Higher	Lower
Ability of transformer-less operation	No	Yes
Efficiency	Low	High
Switching losses	High	Low
Operation at the fundamental frequency	Fails	Operate
Input current distortions	High	Low
Fault tolerant operation	Impossible	Possible
Rate of change of voltage	High	Low
Ability to operate at low/high/fundamental frequency	More	less
Production of multiple voltage level	Not possible	Possible
EMI generation	High	Low

2.3 SPACE VECTOR PULSE WIDTH MODULATION

Space vector modulation (SVM) is one of the preferred real-time modulation techniques and is widely used for digital control of voltage source inverters. This treats the sinusoidal voltage as a constant amplitude vector rotating at constant frequency. The main feature of the SVM scheme is fast dynamic response. SVPWM is a technique used in the final step of field oriented control to determine the pulse-width modulated signals for the inverter switches. It is improved technique for generating a fundamental sine wave that provides a higher voltage to the motor; lower total harmonic distortion, and controls the number of short pulses in the PWM waveform. It provides a constant switching frequency and therefore the switching frequency can be adjusted easily. Although SVPWM is more complicated than sinusoidal PWM and hysteresis band current control, it may be implemented easily with modern DSP based control Systems.

Comparison between SPWM & SVPWM is given as follows:

Device switching frequency: The number of switchings of each power electronic device in one cycle of the inverter output voltage is equal to the frequency modulation index for both the SPWM & SVPWM techniques. Thus, there is no difference between the two techniques as far as device switching frequency is concerned.

Frequency spectrum: Comparison shows that the SPWM gives a much cleaner frequency spectrum as compared to SVM, even though the THD is greater. This is because the output line voltage in case of SVM is inherently half-wave asymmetric, as a result of which even-order harmonics are also present in the output voltage. However, the harmonics can be eliminated by making some changes in the switching sequence design.

Ease of implementation: SPWM is much easier to implement as compared to SVM as the concept behind it is pretty simple. However, it must be noted that the sinusoidal modulating waves and the carrier wave cannot be generated using digital processors; instead look-up tables have to be used in digital processor. The accuracy of the generated waves depends on the number of data points in the look-up tables. Also, if carrier-based PWM schemes are used for multilevel inverters, the number of such look-up tables goes on increasing. No such look-up tables are required for SVM implementation. In fact, it is possible to have algorithm based all-digital SVM implementation even for multilevel inverters using techniques such as the g-h coordinate transformation technique.

Design flexibility: There is no flexibility in design afforded by the SPWM technique. However, this flexibility is available in case of SVM wherein it is possible to design the switching sequence as per the requirements. There is the option to use which switching states to use, how many segments to have in one sampling period, Ts, etc. The design options increase significantly in case of multilevel inverters. As such, SVM has been, and continues to be, a favourite for researchers.

Sinusoidal Pulse-Width Modulation is conceptually simpler to understand as well as implement as compared to Space Vector Modulation for DC to AC converters. However, the advantages offered by SVM are significant as compared to SPWM. Even though SVM requires some effort to master it, its advantages in the long run over SPWM make it worthwhile to do so. To an engineer, the design flexibility offered by SVM is also very encouraging and interesting [22-23]. Table 2.3 shows the comparison between the SPWM & SVPWM technique for three level inverter on the basis of performance.

Table 2.3 Performance comparison between SPWM and SVPWM technique

Performance Parameters	**Three-Level Converters**	
	Control Technique Used	
	SPWM	**SVPWM**
Switching frequency & power loss	High, but less than 2-level Converter	Low
Efficiency	Less than SVPWM	Greater than SPWM
Switching Stresses	Less	Very less
dv/dt	Less	Very less
Voltage Stress	Less, very less for high level converter	Less, very less for high level converter
Voltage & power level	Medium	Medium
Line current THD	Very less	Very less
EMI interference	less	less
Input power factor	Unity	Unity

Algorithm of SVPWM:

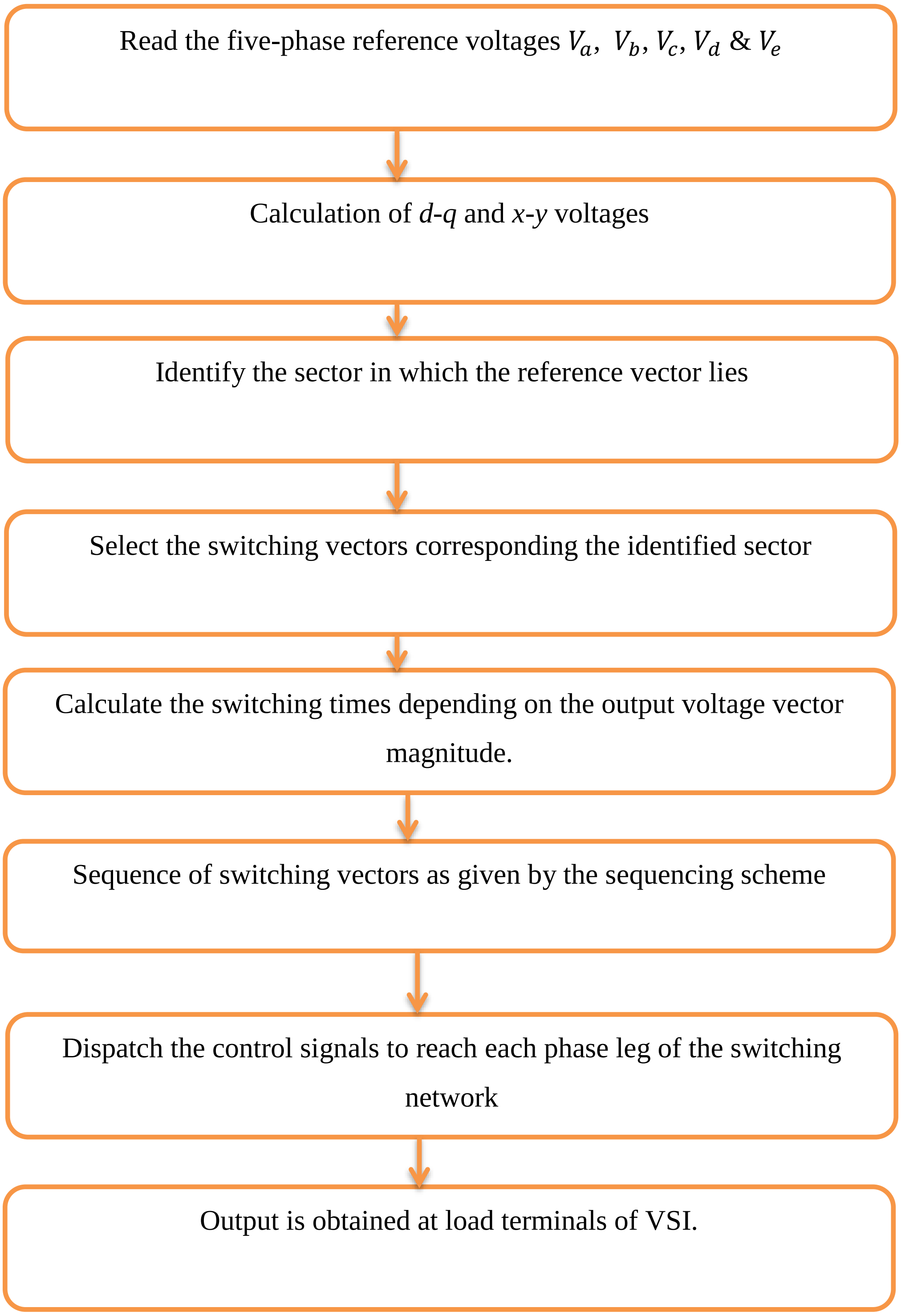

Fig. 2.3 Flowchart of SVPWM

The algorithm of SVPWM step-wise is given below:

1. Apply five phase voltages with the phase difference of 72^0.

2. Calculation of *d-q* and *x-y* voltages using given matrix,

$$\begin{bmatrix} v_d \\ v_q \\ v_x \\ v_y \\ v_z \end{bmatrix} = \frac{2}{5} \begin{bmatrix} 1 & \cos\theta & \cos 2\theta & \cos 3\theta & \cos 4\theta \\ 0 & \sin\theta & \sin 2\theta & \sin 3\theta & \sin 4\theta \\ 1 & \cos 2\theta & \cos 4\theta & \cos\theta & \cos 3\theta \\ 0 & \sin 2\theta & \sin 4\theta & \sin\theta & \sin 3\theta \\ 1/2 & 1/2 & 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \\ V_{DN} \\ V_{EN} \end{bmatrix}$$

$$V_{d-q} = \frac{2}{5}(V_{AN} + \alpha V_{BN} + \alpha^2 V_{CN} + \alpha^3 V_{DN} + \alpha^4 V_{EN}) \quad (2.1)$$

$$V_{x-y} = \frac{2}{5}(V_{AN} + \alpha V_{CN} + \alpha^3 V_{EN} + \alpha^3 V_{BN} + \alpha^4 V_{DN}) \quad (2.2)$$

$$\alpha = e^{j2\pi/3}$$

4. Identification of sector in method-1 -18^0 to $+18^0$ and method-2 0^0 to $+36^0$.

5. Identification of the sector in which vectors lie, total ten sector present in which voltage vectors lie.

6. Selection of switching vectors corresponding to the identified sector.

7. Calculation of the switching times depending on the magnitude of the output voltage,

$$V_{dref} = V_{ref}\cos(\theta) \quad (2.3)$$

$$V_{qref} = V_{ref}\sin(\theta) \quad (2.4)$$

$$V_{xref} = 0 \quad (2.5)$$

$$V_{yref} = 0 \quad (2.6)$$

$$T_1 = \left|\frac{V_{ref}}{V_1}\right| T_s \quad T_2 = \left|\frac{V_{ref}}{V_2}\right| T_s \quad (2.7)$$

$$T_0 = T_s - (T_1 + T_2) \quad (2.8)$$

T_0 , T_1 & T_2 are specified time for given voltage vectors.

8. Sequence of the switching vectors as given by the sequencing scheme in proposed methods.

9. Give the control signals to each phase leg of the switching network.

10. At the load terminals of VSI output is obtained.

The five-phase three-level inverter has two planes which are orthogonal to each other. The d-q plane lie at $10n \pm 1$ & *x-y* at $10n \pm 3$. The fundamental supply component plus supply harmonics of the order $10n \pm 1$ ($n = 0, 1, 2, 3, \ldots$) map into the *d-q* space plane and the supply harmonics of the order $10n \pm 3$ ($n = 0, 1, 2, 3, \ldots$) map in the *x-y* space plane.The *x-y* vector space is similar to the *d−q* vector space domain but with the *d−q ABCDE* phase order replaced by a *x-y ACEBD* phase order system. Hence, the *x-y* vector space voltage represents a distortion voltage that generates a *x-y* component in combination with the *d−q* component generated by the *d-q* vector space. It is generally desired to eliminate the *x-y* voltage distortion by making the *x-y* voltage vector null, resulting in sinusoidal voltages hence a sinusoidal air-gap flux pattern in the induction machine. There are two types of voltage vectors available in *d-q* and *x-y* planes. These are vertex and non-vertex voltage vectors as shown in Figs. 2.4 & 2.5. The vertex voltage vectors are positioned 18^0 displaced from non-vertex vectors as shown in Fig. 2.4.

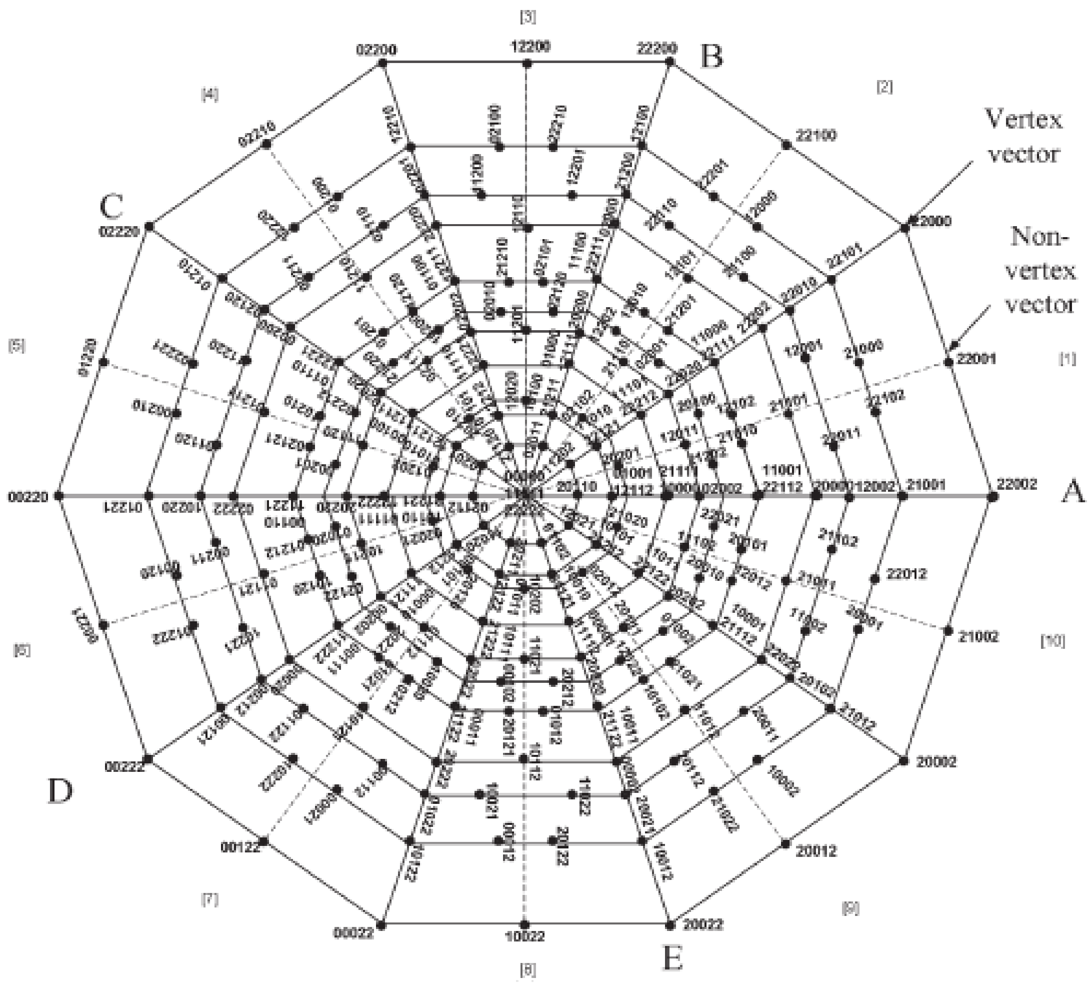

Fig. 2.4 Two-hundred forty-three inverter states mapped in *d-q* vector space

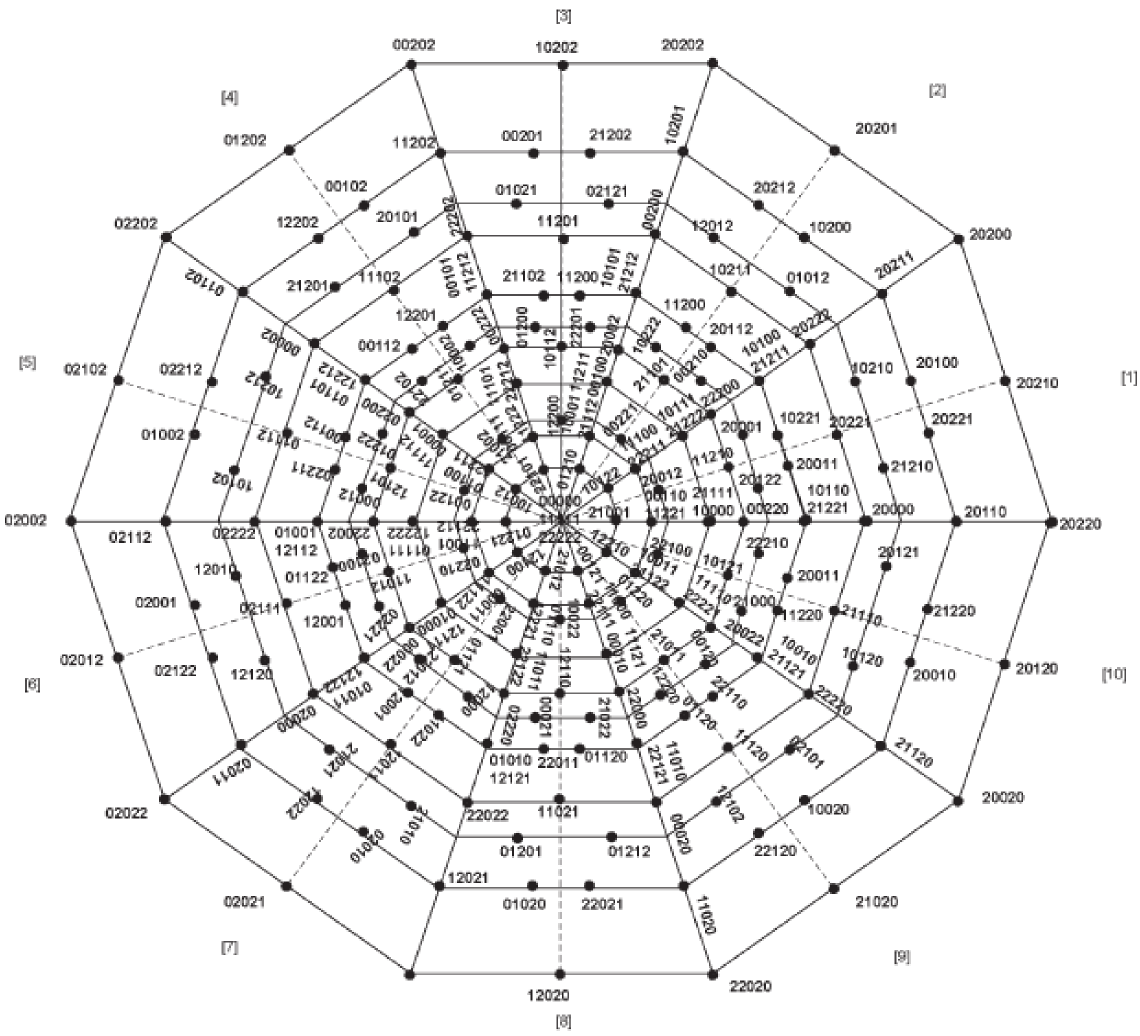

Fig. 2.5 Two-hundred forty-three inverter states mapped in *x*-*y* vector space

In *d*-*q* plane as shown in Fig. 2.6, voltage vectors lie in same line facing towards right side however in *x*-*y* plane the same voltage vectors lie opposite to each other. For e.g. the voltage vector with switching state 22001 and 21101 lie on same side in *d*-*q* plane, whereas the switching states lie opposite to each other in *x*-*y* plane as shown in Fig. 2.7. This helps in eliminating *x*-*y* stator plane.

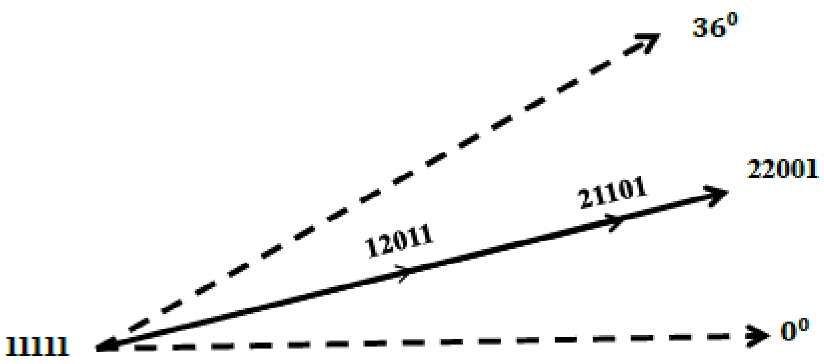

Fig. 2.6 *d*-*q* plane non-vertex vectors for sector-1

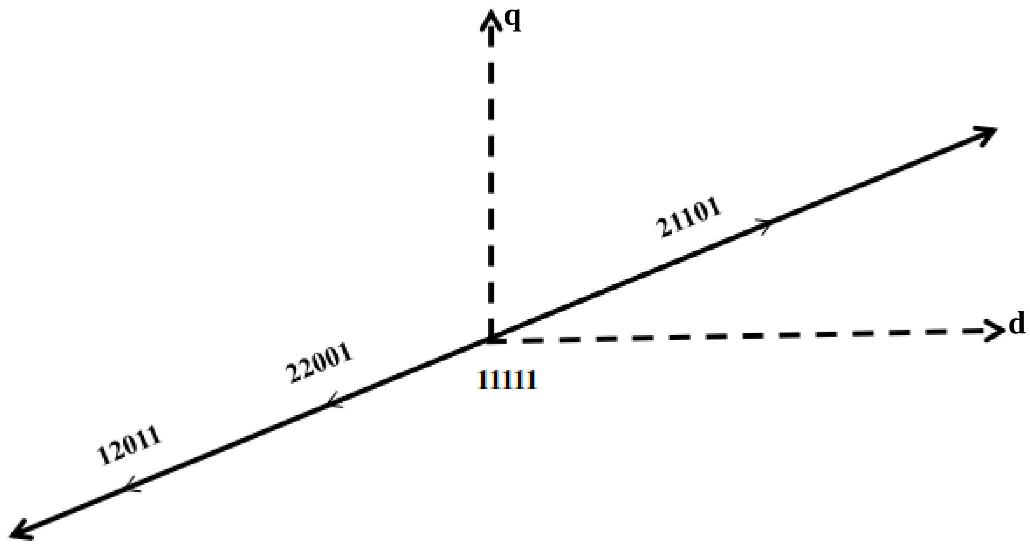

Fig. 2.7 *x-y* plane non-vertex vectors for sector-1

2.4 NON-VERTEX VECTORS

Out of 243 vectors 31 voltage vectors will be selected for practical proposed model. By using these vectors CMV will be coming out as $0\,V_{dc}$. In proposed method, there are 31 voltage vectors selected for CMV elimination as shown in Fig. 2.8.

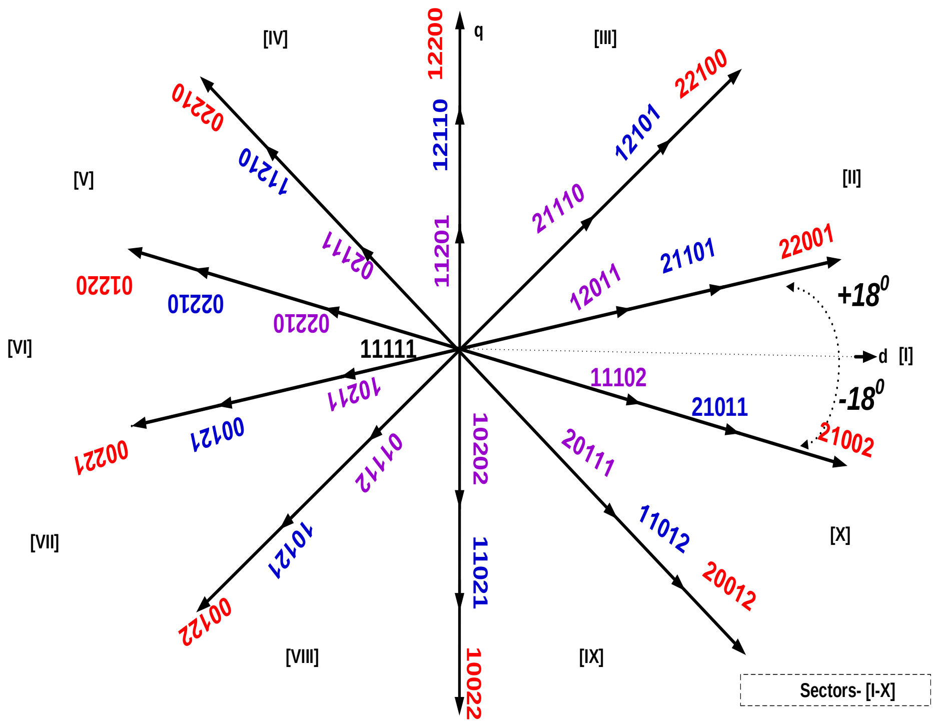

Fig. 2.8 Non-vertex voltage vectors space mapping

$$CMV = \frac{V_{AN}+V_{BN}+V_{CN}+V_{DN}+V_{EN}}{5} \tag{2.9}$$

Consider switching state 22001, A phase pole voltage is $+\frac{V_{dc}}{2}$, for B phase pole voltage is $+\frac{V_{dc}}{2}$, for C, D, E phase pole voltages are $-\frac{V_{dc}}{2}$, $-\frac{V_{dc}}{2}$ and $0\ V_{dc}$. Therefore the CMV is $0\ V_{dc}$ as given by formula (2.11).

The CMV for remaining non-vertex vectors of sector-1 is given in Table 2.4.

Table 2.4 CMV of non -vertex vectors of sector-1

CMV of non-vertex vector of sector-1	
22001	$0\ V_{dc}$
21101	$0\ V_{dc}$
12011	$0\ V_{dc}$
11111	$0\ V_{dc}$

2.5 VERTEX VECTORS

Out of 243 vectors these 32 vectors will be selected for classical model. By using these vectors CMV will be coming out as $\frac{V_{dc}}{2}$. Vertex vectors along with two zero voltage vectors cannot eliminate the CMV, because their switching states generate CMV. The CMV generation related to voltage vectors is given in Fig. 2.9.

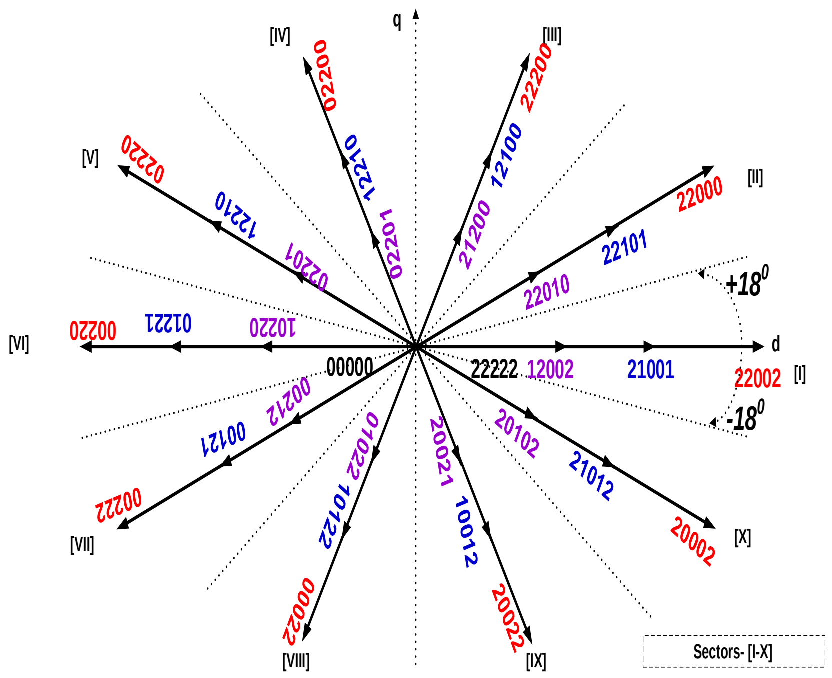

Fig. 2.9 Vertex voltage vectors space mapping

Consider switching state 22002, A phase pole voltage is $+\frac{V_{dc}}{2}$, B phase pole voltage is $+\frac{V_{dc}}{2}$, for C, D, E phase pole voltages are $-\frac{V_{dc}}{2}$, $-\frac{V_{dc}}{2}$ and $+\frac{V_{dc}}{2}$. Therefore the CMV is $+\frac{V_{dc}}{10}$ as given by formula (2.11). The CMV for remaining vertex vectors of sector-1 is given in Table 2.5.

Table 2.5 CMV of vertex vectors of sector-1

CMV of vertex vectors of sector-I	
22222	$+\frac{V_{dc}}{2}$
21001	$-\frac{V_{dc}}{10}$
22002	$+\frac{V_{dc}}{10}$
00000	$-\frac{V_{dc}}{2}$

CHAPTER 3
COMMON-MODE VOLTAGE STATUS

3.1 OVERVIEW

Inverter topologies are used with different PWM methods for the control of the torque, speed and current of the machine. In PWM inverter-fed drives the CMV is generated because of their switching actions. Because of the CM voltage, bearing current and shaft voltage are generated which are main reasons for the bearing failure. As the CM voltage is the one of the main reasons for the bearing current, if not eliminated, can lead to the bearing failures. Many researchers have worked either for elimination or reduction of CMV. For the mitigation of CM voltage, one approach is to use CM filters. But, using filters increases the cost and size of inverters. So, another approach is the modification in the modulation strategy of the inverters.

The common mode voltage is one of the major issues in a neutral point clamped inverter. It causes an increase in the rise of bearing current in motor, which leads to damage of the bearing of the motor and shortens the lifetime of the motor (Das and Jana 2017; Kumar and Gupta 2017). In addition to this, CMV can also be the cause for increases in electromagnetic interference issues. Hence, it is very important to reduce the CMV level in NPC inverters. A number of solutions have been proposed to address the minimization of CMV level like using filter circuits, multicarrier SPWM, space vector modulation, SPWM with interleaved carriers and phase shifting method (Palanisamy and Vijayakumar 2018). The effects of common mode voltage include faults in motors, premature failure of bearings, unwanted tripping of switchgears, and glitches in the control equipment.

The multilevel inverters generate a lower common mode voltage compared to two-level or three-level inverters. Therefore, increasing the output voltage levels by using multilevel inverters is one technique that can be employed for reducing the common-mode voltage in an electrical system with inverters. In three-phase inverters, modifying the topology by adding a fourth leg is suitable for reducing the common mode voltage. The utilizing dual bridge inverter is also a reduction method used for common mode voltage in conventional inverters. In 2-level and multilevel inverter, CMV generates within the motor windings which may result in problems in motor and drive applications.

The CMV enables the motor shaft voltage to build up through electrostatic couplings between the rotor and stator windings and the frame and the rotor, which results in excessive bearing currents when the shaft voltage exceeds the dielectric capability of the bearing grease. It has been found that bearing currents may cause premature motor bearings failures. At the same time, CMV will cause a much larger common mode leakage current to flow into the ground via electrostatic coupling between the stator windings and the grounded frame. Since this current will flow back to the input terminals through the ground conductor and the power mains, it will cause common mode EMI emission.

In addition, the leakage current may cause false tripping of ground current relays installed for protection. Three level inverter will not generate CMV when the inverter output voltages are limited within the certain of the available switching states. At the medium voltage levels, such controlled multilevel inverters will still provide reduced device voltage ratings and improved harmonic characteristics over 2-level inverter, whereas at low voltage levels, 3-level inverters could be considered mainly for the purpose of the cancellation of CMV [24-25].

3.2 EFFECT OF CMV

CMV results in common mode currents (CMC) which through capacitance between the different parts of the induction motor drives and the ground flows to the ground. This may cause motor bearing failure, unexpected operation of ground current protection relays and electromagnetic interference noise that may lead to tripping of complete induction motor drives. Due to these drawbacks, the induction motor drive may lose its reliability.

3.3 COMMON MODE VOLTAGE

CMV is defined as the voltage difference between the neutral point of load (N) and DC-link neutral point. Generally, the CMV of five-phase system is written as follows:

$$\text{CMV}= \frac{V_a+V_b+V_c+V_d+V_e}{5} \tag{3.1}$$

Where V_a, V_b, V_c, V_d & V_e are the pole voltages of the inverter. Pole voltage is voltage between the phase and DC-link neutral point.

Where $V_i = (S_{i1} - S_{i4})\frac{V_{dc}}{2}$ (i = {a, b, c, d, e})

The simplified form of CMV is expressed as

$$V_{cmv} = \frac{\sum(S_{i1} - S_{i4})\ \frac{V_{dc}}{2}}{5} \tag{3.2}$$

Where $S_{i1} - S_{i4}$ denotes the switches used in the various phases of the NPC inverter and each phase is operated in three different switching modes. It based on that, the output voltages + $\frac{V_{dc}}{2}, 0, -\frac{V_{dc}}{2}$ are obtained.

For e.g. 22001, A phase $+\frac{V_{dc}}{2}$, B phase $+\frac{V_{dc}}{2}$ and for C, D, E phase is $-\frac{V_{dc}}{2}, -\frac{V_{dc}}{2}$ & $0\ V_{dc}$.

This five-phase three level NPC inverter has 243 switching modes of operation, every mode has a separate CMV level-based position of power switches, which includes various switching state vectors like small, large, medium and zero (or) null vectors. In this proposed five-phase inverter system, the CMV level is varied from $\pm\frac{V_{dc}}{2}$ to $0\ V_{dc}$ times of input voltage, which is located among various switching state vectors. Hence, based on the proper selection of switching states the CMV level can be eliminated. The large and small vertex vectors are having minimized CMV level; hence, these vectors are mostly preferred for minimization of CMV level. The non –vertex voltage vectors, which are large, medium and small vectors, have zero CMV output. Along with these vectors zero vector also has zero CMV output. The CMV range calculations for sample switching vectors are shown as follows: (by using (3.1))

$$22001 = \frac{\frac{V_{dc}}{2}+\frac{V_{dc}}{2}-\frac{V_{dc}}{2}-\frac{V_{dc}}{2}+0}{5} = 0\ V_{dc} \tag{3.3}$$

$$22011 = \frac{\frac{V_{dc}}{2}+\frac{V_{dc}}{2}-\frac{V_{dc}}{2}-0+0}{5} = +\frac{V_{dc}}{10} \tag{3.4}$$

Consider switching state 22001, A phase pole voltage is $+\frac{V_{dc}}{2}$, for B phase pole voltage is $+\frac{V_{dc}}{2}$, for C, D, E phase pole voltages are $-\frac{V_{dc}}{2}$, $-\frac{V_{dc}}{2}$ and $0\ V_{dc}$ Therefore the CMV is $0\ V_{dc}$ as given by formula (3.1).

The CMV for remaining vertex and non-vertex vectors is given in Table 3.1.

Table 3.1 Classification of voltage vectors

Types	**Voltage vectors**	**CMV**	**Switching states**
Vertex vectors	Large vectors	$\pm\frac{V_{dc}}{10}$	22002, 22000, 22200, 02200, 02220, 00220, 00222, 00022, 20022, 20002
	Medium vectors	$\pm\frac{V_{dc}}{10}$	21001, 22101, 12100, 12210, 01210, 01221, 00121, 10122, 10012, 21012
	Small vectors	$\pm\frac{V_{dc}}{10}$	20110, 11202, 02011, 21120, 10201, 02112, 11020, 20211, 01102, 12021
	Zero vectors	$+\frac{V_{dc}}{2}$	22222, 00000
Non-vertex vectors	Large vectors	$0\,V_{dc}$	22001, 22100, 12200, 02210, 01220, 00221, 00122, 10022, 20012, 20012
	Medium vectors	$0\,V_{dc}$	21101, 12101, 12110, 11210, 01211, 01121, 10121, 10112, 11012, 21011
	Small vectors	$0\,V_{dc}$	20201, 02102, 12020, 20210, 01202, 02021, 20120, 10202, 02012, 21020
	Zero vector	$0\,V_{dc}$	11111

Table 3.2 DC length of voltage vectors

Methods	**Voltage vectors**	**DC length**
Proposed method-I	Large Vectors	$0.6156V_{dc}$
Proposed method-II	Large Vectors	$0.6156V_{dc}$
	Medium Vectors-1	$0.3804V_{dc}$
	Medium Vectors-2	$0.2764V_{dc}$

In this work two different methods are presented. In first method, non-vertex large and zero voltage vectors are selected to get CMV elimination and maximum DC link. In second method large, medium and zero voltage vectors are selected to get CMV elimination and *x*-*y* stator pane elimination.

Method 1:

In this method sector is considered from -18^0 to 18^0. Only large and zero vectors are selected for CMV elimination as shown in Fig. 3.1.

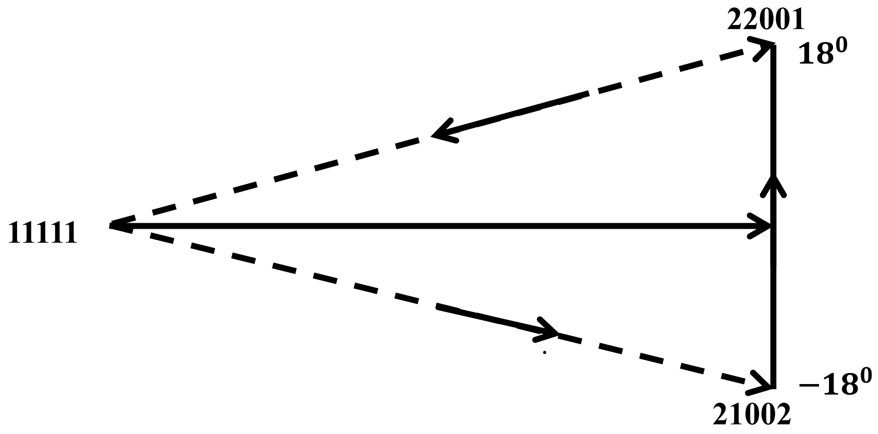

Fig. 3.1 Non-vertex voltage vectors of sector-1 in method-1

The CMV of the voltage vectors considered in method-I is shown in Table 3.3.

Table 3.3 CMV of non-vertex voltage vectors in method-I

Method-1		
Sectors	**Voltage Vectors**	**CMV**
1	11111, 21002, 22001	0 V_{dc}
2	11111, 22001, 22100	0 V_{dc}
3	11111, 22100,12200	0 V_{dc}
4	11111, 12200, 02210	0 V_{dc}
5	11111, 02210, 01220	0 V_{dc}
6	11111, 01220, 00122	0 V_{dc}
7	11111, 00122, 00122	0 V_{dc}
8	11111, 00122, 10022	0 V_{dc}
9	11111, 10022, 20012	0 V_{dc}
10	11111, 20012, 21002	0 V_{dc}

Dwell Time Calculation:

Voltage second balance equation:

$$V_0T_0 + V_1T_1 + V_2T_2 = V_{ref}T_s \tag{3.5}$$

$$T_0 = T_s - 1.618T_sM\cos\theta \tag{3.6}$$

$$T_1 = 0.309T_sM\cos\theta - 0.951T_s\sin\theta \tag{3.7}$$

$$T_2 = 0.309T_sM\cos\theta + 0.951T_s\sin\theta \tag{3.8}$$

Method II:

In this method sector is considered from 0^0 to 36^0. Only large, medium and zero vectors are selected for CMV elimination as shown in Fig. 3.2.

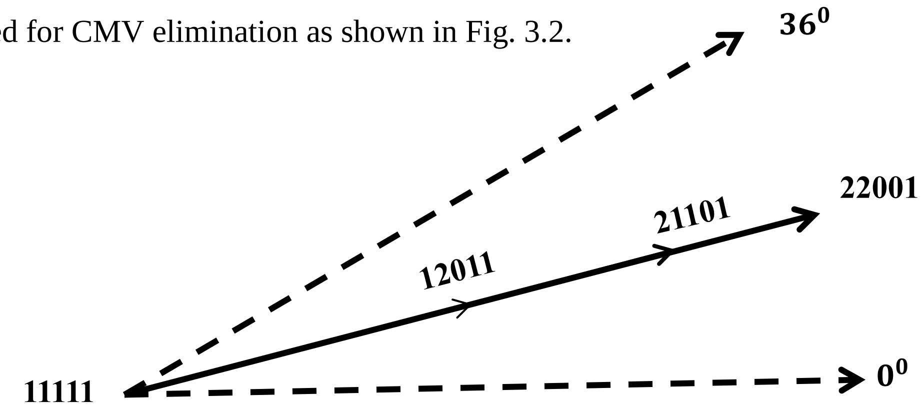

Fig. 3.2 Non-vertex voltage vectors of sector-1 in method-II

The CMV of all the voltage vectors considered in method-I is shown in Table 3.4.

Table 3.4 CMV of non-vertex voltage vectors in method-II

Method-II		
Sectors	**Voltage Vectors**	**CMV**
1	11111, 12011, 21101, 22001	0 V_{dc}
2	11111, 21110, 12101, 22100	0 V_{dc}
3	11111, 11201, 12110, 12200	0 V_{dc}
4	11111, 02111, 11210, 02210	0 V_{dc}
5	11111, 11120, 01211, 01220	0 V_{dc}
6	11111, 10211, 01121, 00221	0 V_{dc}
7	11111, 01112, 10121, 00122	0 V_{dc}
8	11111, 11021, 10112, 10022	0 V_{dc}
9	11111, 20111, 11012, 20012	0 V_{dc}
10	11111, 11102, 21011, 21002	0 V_{dc}

Dwell Time Calculation:

Voltage second balance equation:

$$V_0T_0 + V_1T_1 + V_2T_2 + V_3T_3 = V_{ref}T_s \tag{3.9}$$

$$T_0 = T_s - 0.382M\cos\theta \tag{3.10}$$

$$T_1 = 0.382T_sM\cos\theta - 0.612T_s\sin\theta \tag{3.11}$$

$$T_2 = 0.5T_sM\cos\theta - 0.612T_s\sin\theta \tag{3.12}$$

$$T_3 = 0.382T_sM\cos\theta + 0.612T_s\sin\theta \tag{3.13}$$

Advantages:

Method-I

- It helps in CMV elimination.
- It gives maximum DC link.

Method-II

- It helps in CMV elimination
- It helps in reducing torque ripple by implementing higher level torque comparator in direct torque control technique for multiphase machine applications.
- It gives *x*-*y* stator plane elimination for obtaining sinusoidal phase current.

CHAPTER 4

SIMULATION

4.1 OVERVIEW

The simulation is carried out in MATLAB-Simulink software using sim-power system blockset. The DC link voltage is kept at 400V, capacitors are rated 4700 µF and R-L load of 25 Ω and 100 mH per phase are taken. The simulation results corresponding to modulation index 0.9 and 0.7 are taken. The sampling frequency is taken as 5 kHz.

Table 4.1 Specifications

Parameter	**Value**
DC link Voltage	400V
DC Link Capacitor	4700 μF
Sampling frequency	5 kHz
Resistance	25 Ω
Inductance	100mH

4.2 SIMULATION RESULTS

Figs. 4.1 & 4.2 represent the results of CMV and load current of method–I, taken as modulation index of 0.9, in which CMV is eliminated but current is not sinusoidal because *x-y* stator plane is not eliminated. Figs. 4.3 & 4.4 represent the result of method–II taken at modulation index of 0.9, in which CMV is eliminated and also current is sinusoidal due to elimination of *x-y* stator plane. Figs. 4.5 & 4.6 represent the result of classical method in which vertex voltage vectors are considered at modulation index of 0.9, which give CMV $\frac{V_{dc}}{2}$ and current with third harmonics because x-y stator plane is not eliminated. Figs. 4.7 & 4.8 represent the results of CMV and load current of method–I taken at modulation index of 0.7, in which CMV is eliminated and current is not sinusoidal but magnitude is slightly increases due to decrease in the modulation index. Figs. 4.9 & 4.10 represent the result of method–II, taken at modulation index of 0.7, in which CMV is eliminated and also current is sinusoidal due to elimination of *x-y* stator plane. Figs. 4.11 & 4.12 represent the result of classical method in which vertex voltage vectors considered modulation index of 0.7, which give CMV more than $\frac{V_{dc}}{2}$ and current with third harmonics because *x-y* stator plane is not eliminated.

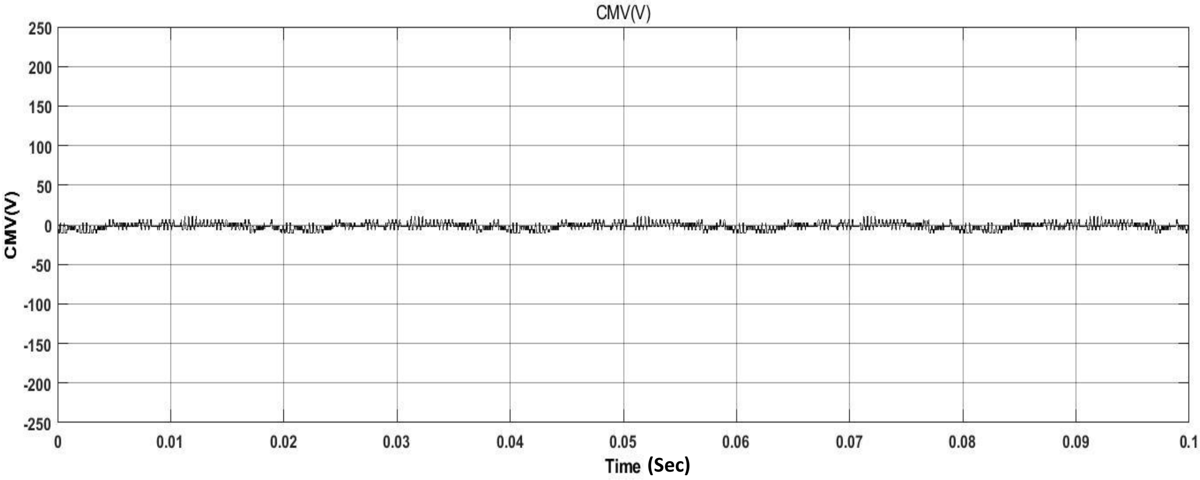

Fig. 4.1 CMV of method-I [M=0.9]

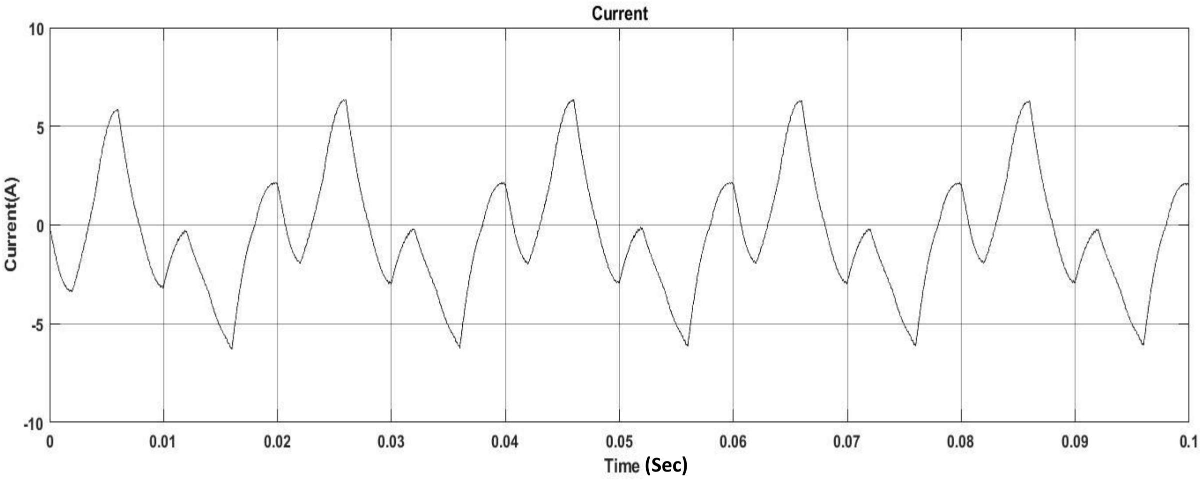

Fig. 4.2 Load current of method-I [0.9]

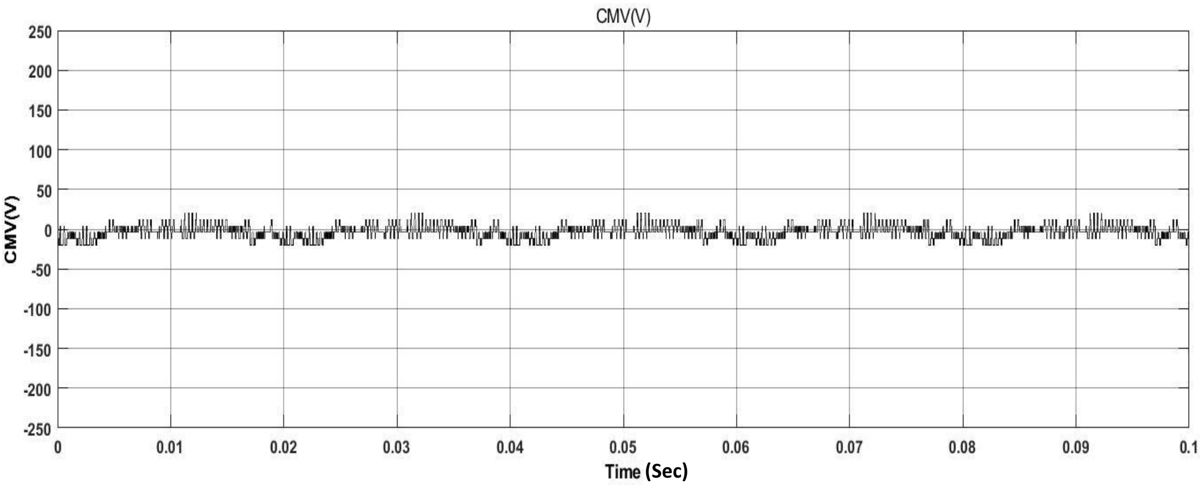

Fig. 4.3 CMV of method-II [M=0.9]

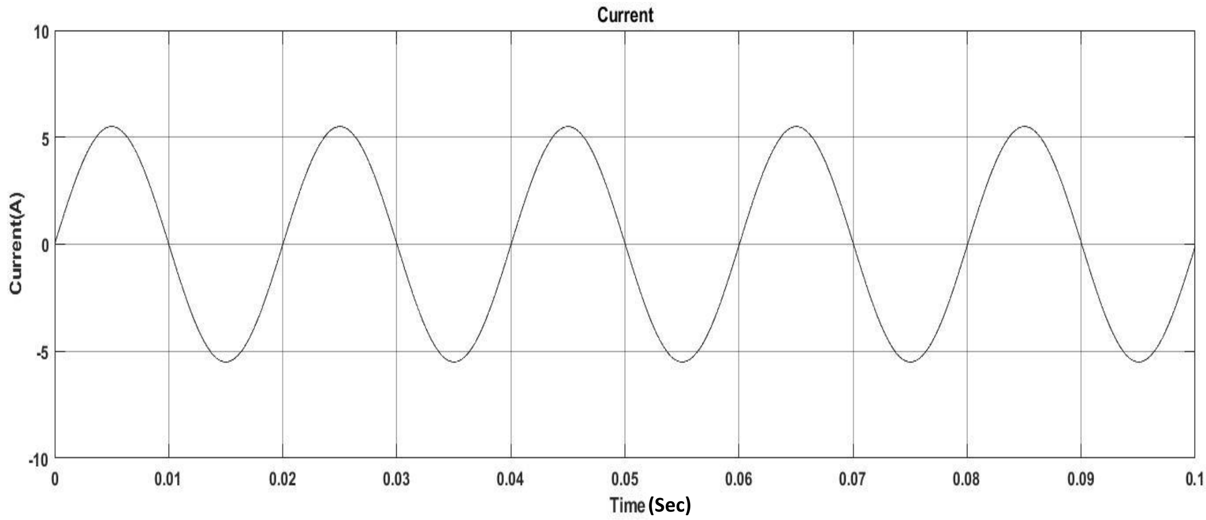

Fig. 4.4 Load current of method-II [M=0.9]

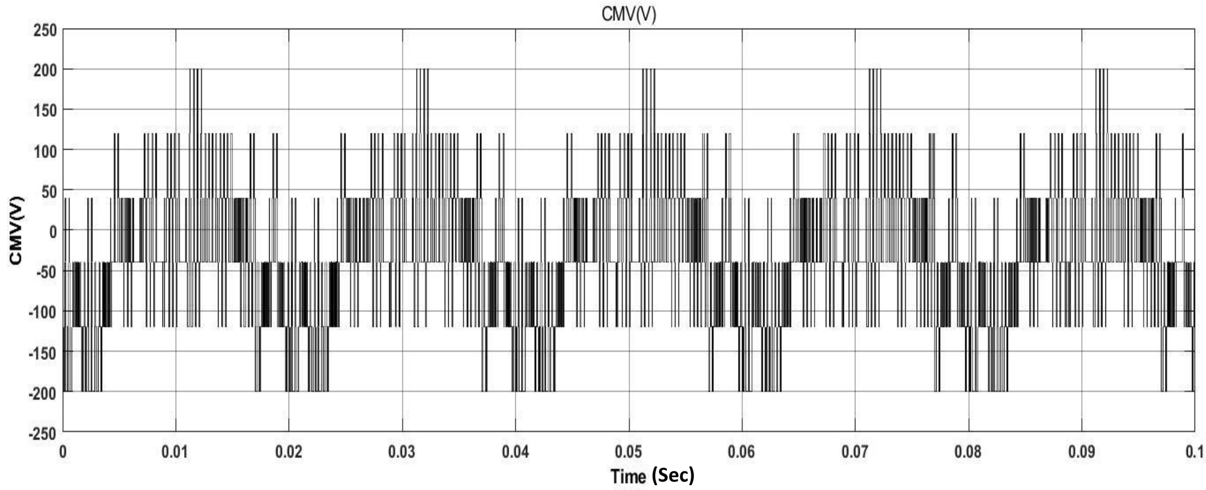

Fig. 4.5 CMV of vertex vector (Classical method) [M=0.9]

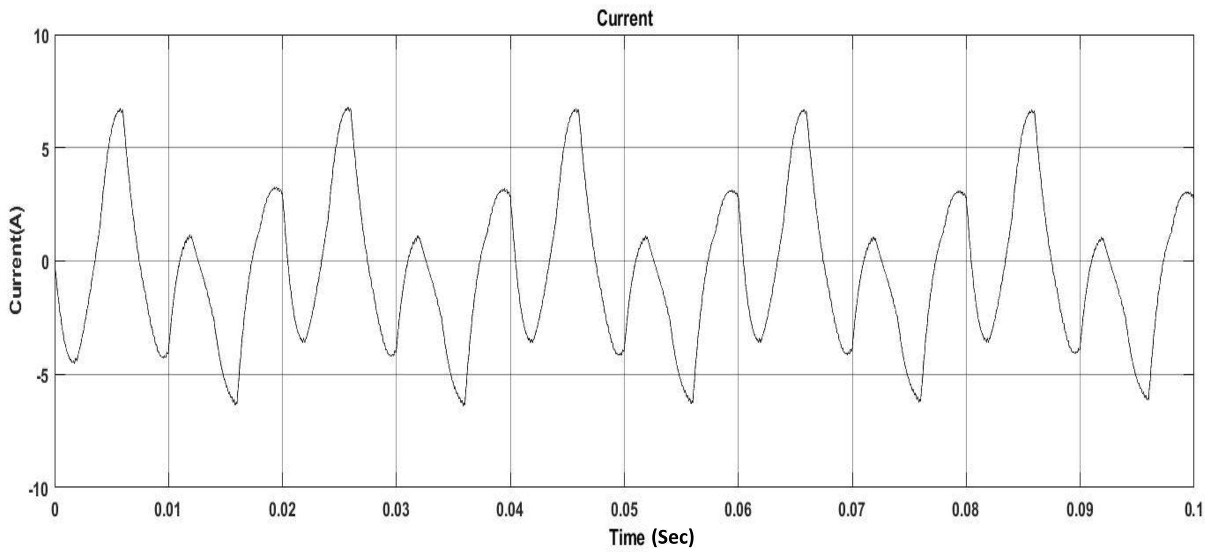

Fig. 4.6 Load current (Classical method) [M=0.9]

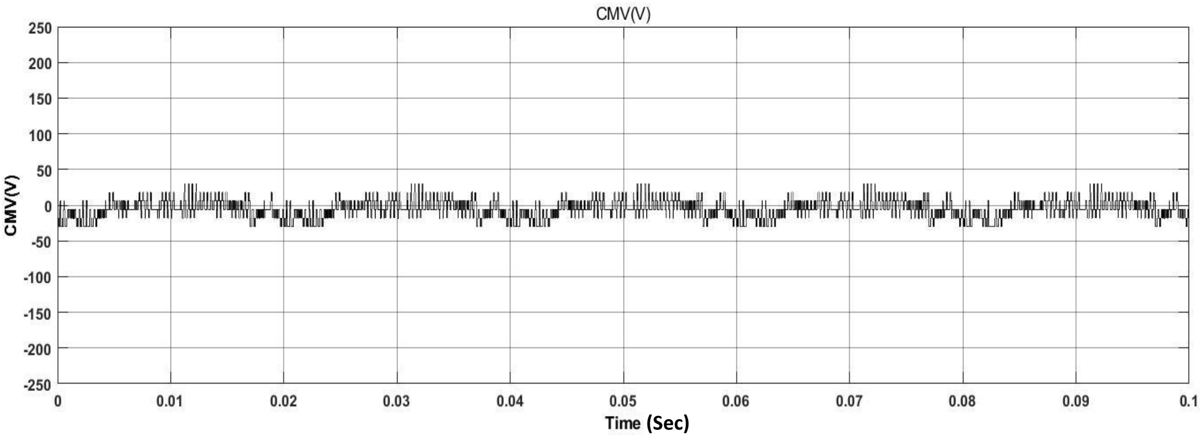

Fig. 4.7 CMV of method-I [M=0.7]

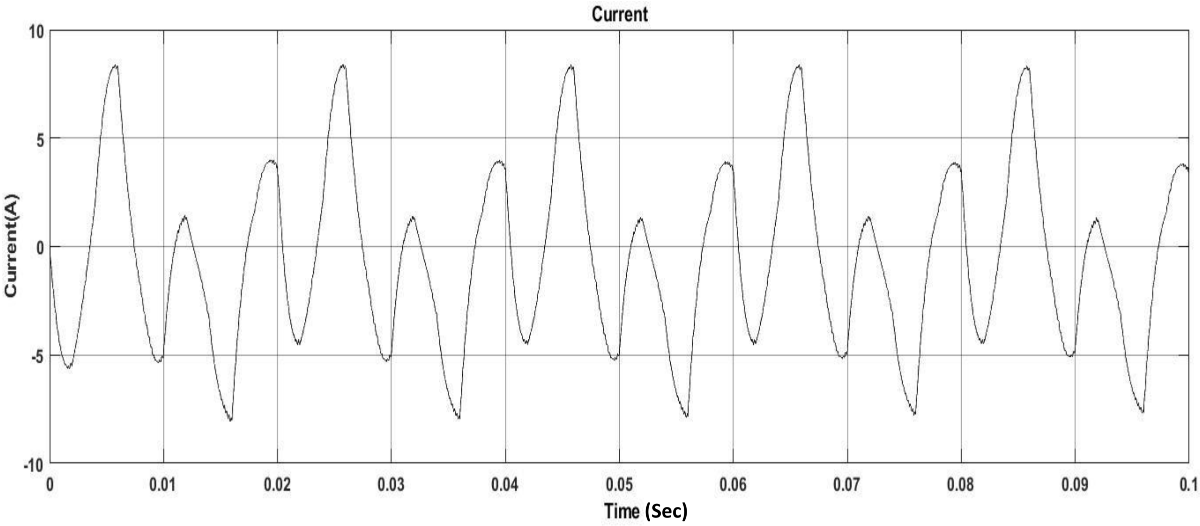

Fig. 4.8 Load current of method-I [0.7]

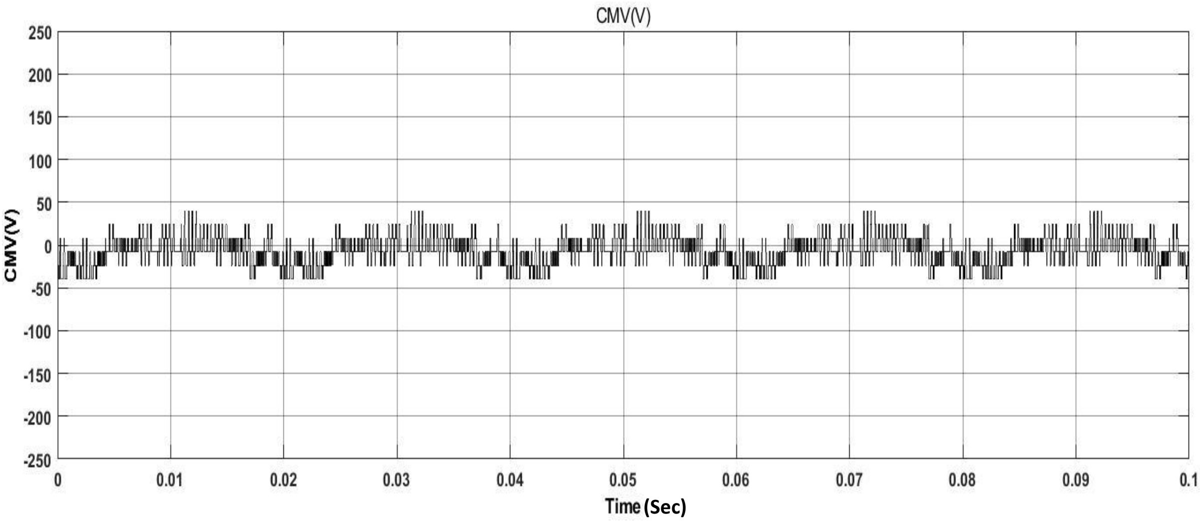

Fig. 4.9 CMV of method-II [M=0.7]

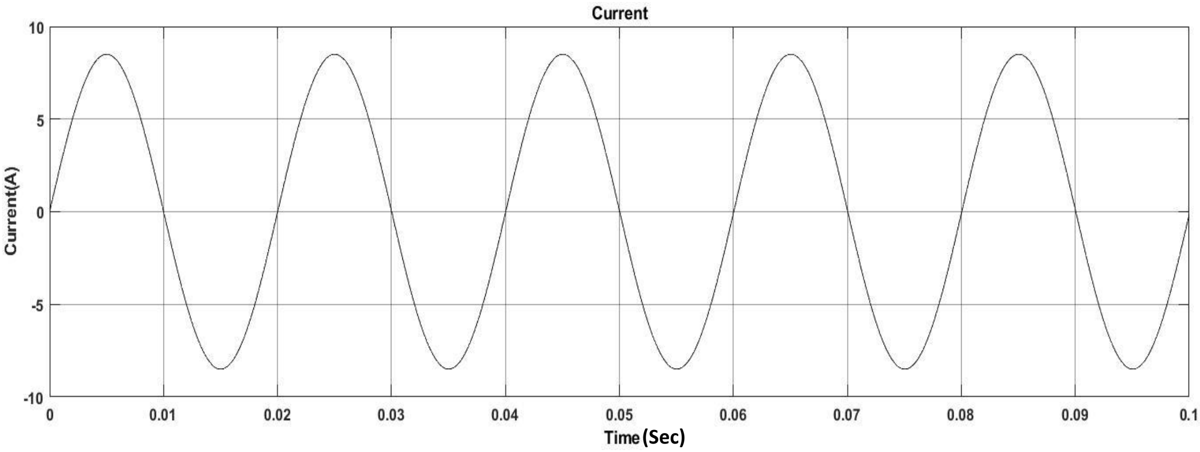

Fig. 4.10 Load current of method-II [M=0.7]

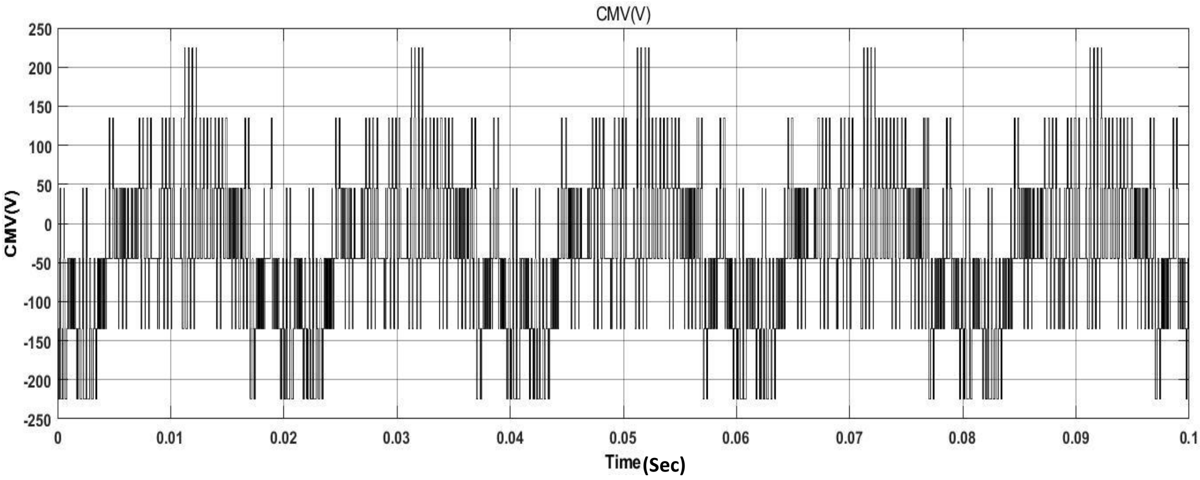

Fig. 4.11 CMV of vertex vector (Classical method) [M=0.7]

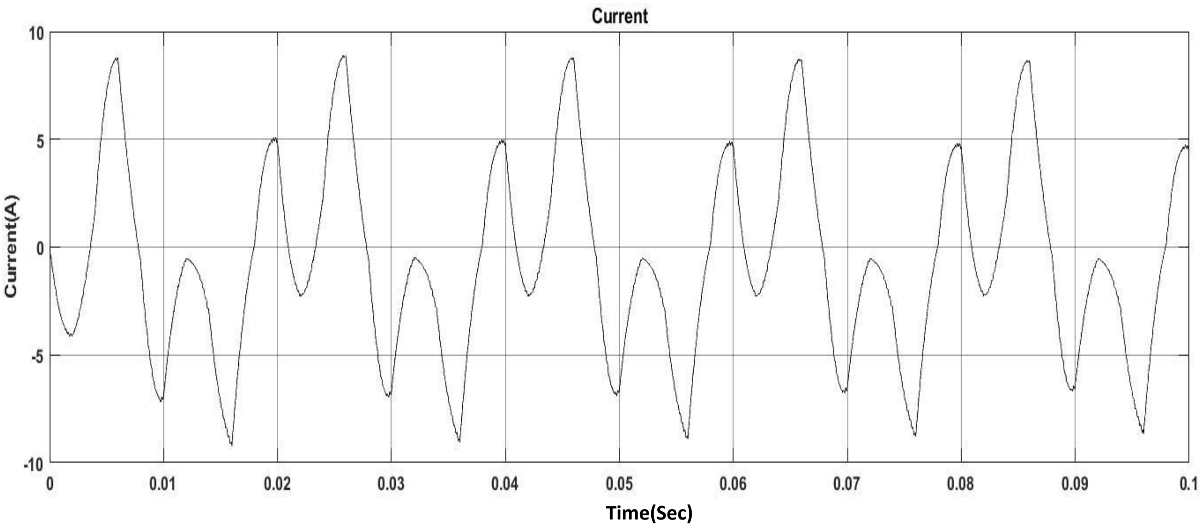

Fig. 4.12 Load current (Classical method) [M=0.7]

CHAPTER 5
EXPERIMENTATION

5.1 THEE-LEVEL INVERTER

The three level inverter is fabricated with DC Input connected across terminals marked as '+VE' & '–VE' as shown in Fig. 5.1. The AC output terminals are marked as A, B, C. Each leg of the three level inverter has 1 No of SKM150MLI066T AT Module. The gate driver Skyper 32Pro (2 Nos) drives each Leg of the 3-Level Inverter. Each of the driver drives two IGBT Switches. The IGBT switches T1 & T4 are driven by one Skyper 32Pro & IGBT switches T2 & T3 are driven by the other Skyper 32Pro.The terminal marked +15V & 0V are power supply terminals for the IGBT gate drivers. The regulated power supply of 15V DC to be used. 'Vin1' corresponds to input signal for IGBT switch 'T1', 'Vin2' for 'T2', 'Vin3' for 'T3' & 'Vin4' for 'T4'. 'ER1' corresponds to error signal output/input for IGBT switches. 'T1' & 'T4' & 'ER2' corresponds to error signal output/input for IGBT switches 'T2'& 'T3'. The driver which drives T1 and T4 is provided interlock/dead time to protect from shoot through fault (dead short of +VE DC and –VE DC). Also the driver (driving T1 and T4) is protected with dynamic short circuit protection. The driver which drives T2 and T3 is provided with zero dead time.

Allowed states:

- All IGBTs are in off state; the converter is switched off.
- Either T2 or T3 may be switched on solely.
- Each state where two adjacent IGBT's are switched on(T1/ T2,T2/ T3,T3/ T4)

Potentially harmful states:

- Either T1 or T4 is switched on solely or together.
- Two not adjacent IGBTs are switched on (T1/ T3 or T2/ T4)

The consequences depend on the switching pattern applied to the module of the other phase legs.

Destructive states:

- Three adjacent IGBTs are switched on (T1/ T2/ T3-shorting upper half of DC link; T2/ T3/ T4-shorting lower half of DC-link)

- ➢ Three not adjacent IGBTs are switched on (T1/ T2/ T4- full DC link voltage applies to T3 ; T1/ T3/ T4-full DC link voltage applies to T2)
- ➢ Four IGBTs switched on - DC+, DC- and N shorted.

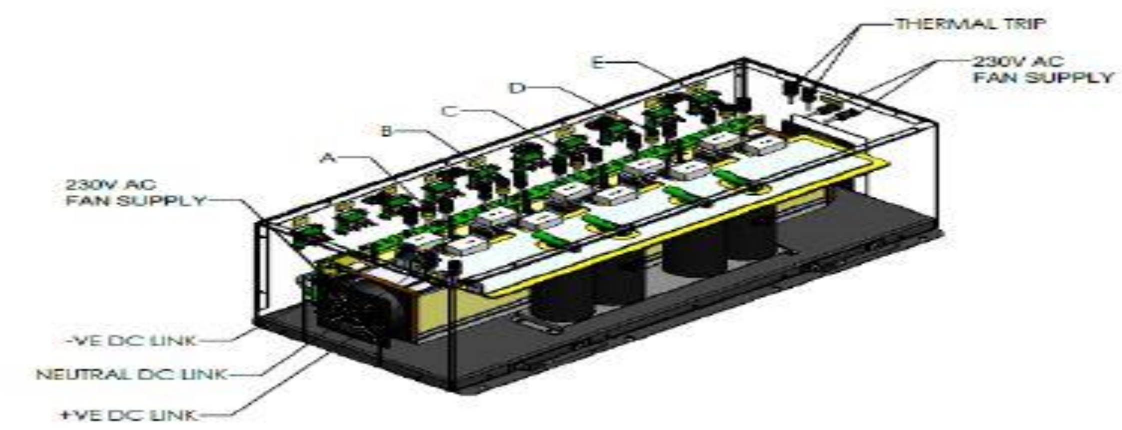

Fig. 5.1 Hardware of three-level inverter

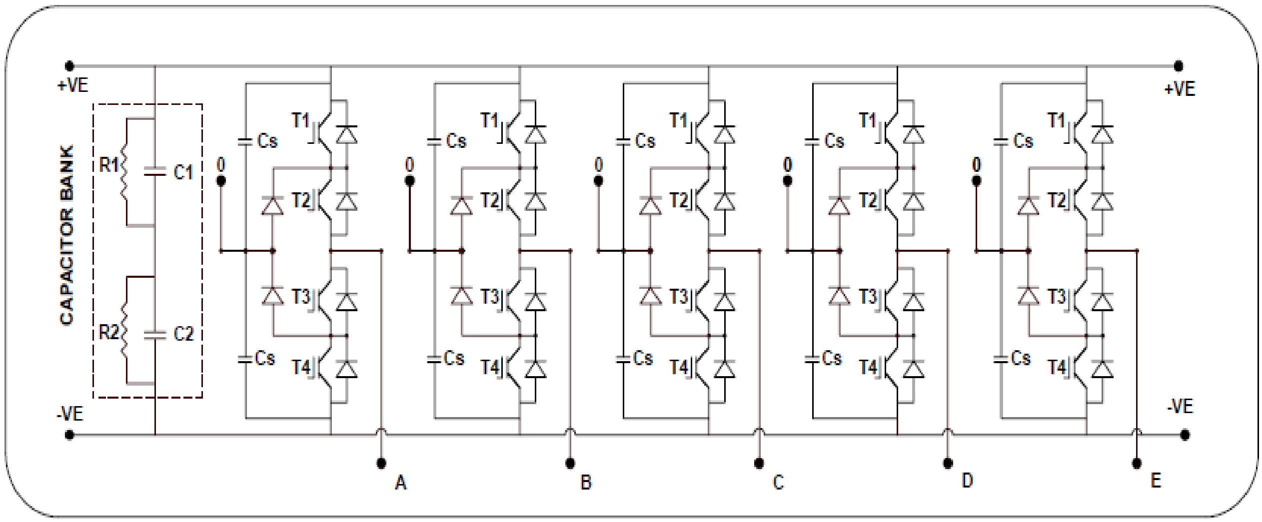

Fig. 5.2 Schematic of hardware prototype of three- level inverter

5.2 COMPONENTS OF THREE-LEVEL INVERTER

5.2.1 GATE DRIVER: SKYPER 32 PRO

The gate driver is an interface between IGBT and controller. It isolates the primary circuit (controller) from the secondary (IGBT) which is directly connected to high power. It also controls the IGBT's dynamic behaviour and provides various protection features such as short pulse suppression, power supply under-voltage monitoring, short circuit protection & soft turn OFF. It amplifies the logic signal ON/OFF and delivers high peak current for switching ON/OFF the gate.

5.2.2 DC CAPACITOR BANK AND SNUBBER CAPACITORS

The rectified DC input is given to electrolytic filtering capacitors. Also recommended the slow charging of the DC to avoid damage to the Electrolytic capacitors. Each of the capacitor is rated at 4700 μF /450 V and the two capacitors are rated at 4700μF/450Vconnected in parallel across + Ve DC to 'O', similarly two capacitors are connected in parallel across 'O' to -Ve DC. The resistors 27 kΩ/20 W are connected across each capacitor for voltage balancing/sharing and also provides discharging path when DC Supply is removed from the system. Avoid to touch DC terminal till five minutes after removal of DC power. The snubber capacitors of 0.22 μF/1500 V_{DC} are connected across the +Ve DC and 'O' and across 'O' to –Ve DC link for voltage overshoot protection. The snubbers limit the over-voltages during commutations and as a consequence reduce the losses. They are kept very close to the device to reduce the inductance between the switches and the capacitors.

5.2.3 HEATSINK AND FAN

The three level inverter stack assembly is provided with forced air cooling. The IGBT and diode modules are mounted on 700mm heat sink (extruded type).The two number of Hi cool fans connected to heat sink to dissipate the heat generated by the IGBT's & diodes. The flow of air is measured to be around 3 to 4m/s. The input to the fan is single phase 230V Supply.

5.2.4 TEMPERATURE PROTECTION

The normally closed thermal contact switch is used for protection against thermal runaway. These are potential free contacts. The terminals of the switch are electrically short, when its temperature is below the threshold temperature (60^0 C) & get electrically open above 60^0 C. After cooling down, it again retains it normally closed position. The thermal switch is placed at the warmest point on the heat sink. It is recommended to take the feedback of the thermal trip output to the controller.

5.3 GENERAL PURPOSE INPUT AND OUTPUT (GPIO)

The GPIO pin are generic pins whose value consists of two voltage setting (0 or 1) and whose behaviour can be programmed through software.

The F28379D launch pad pin out and pin mux options – J1, J2, J3, J4 , J5, J6, J7, J8 in which total 40 pin available. According to requirement choose 20 GPIO pins. Selected GPIO are GPIO 0,GPIO 1, GPIO 2, GPIO 3, GPIO 4, GPIO 5, GPIO 6, GPIO7, GPIO8, GPIO9, GPIO10, GPIO11, GPIO22, GPIO 24 ,GPIO26, GPIO27, GPIO44, GPIO56, GPIO 65, GPIO94.
The states given to GPIO according to these vectors:

1. Non vertex vector of sector-1:
   Method-I: 21002, 22001, 11111
   Method-II: 22001, 21101, 12011, 11111
2. Vertex vector of sector-1: 22002, 21001, 12002, 00000

Table 5.1 Division of GPIO

Ist leg	**2nd leg**	**3rd leg**	**4th leg**	**5th leg**
GPIO 0	GPIO 4	GPIO 8	GPIO 22	GPIO 44
GPIO 1	GPIO 5	GPIO 9	GPIO 24	GPIO 56
GPIO 2	GPIO 6	GPIO 10	GPIO 26	GPIO 65
GPIO 3	GPIO 7	GPIO 11	GPIO 27	GPIO 94

For e.g if 22110 vector is representing the legs condition as shown in Table 5.2.

Table 5.2 Working of Sates

States	**Leg Switches**
2	Ist leg Switches
1	2nd leg Switches
0	3rd leg Switches
0	4th leg Switches
2	5th leg Switches

For non- vertex vectors switching states of method-1 & method-II, the legs condition are shown in Tables 5.3 & 5.4.

Table 5.3 Working of non-vertex vectors of method-1

GPIO	21002	22001	11111
0	ON	ON	
1	ON	ON	ON
2			ON
3			
4		ON	
5	ON	ON	ON
6	ON		ON
7			
8			
9			ON
10	ON	ON	ON
11	ON	ON	
22			
24			ON
26	ON	ON	ON
27	ON	ON	
44	ON		
56	ON	ON	ON
65		ON	ON
94			

Table 5.4 Working of non-vertex vectors of method-II

GPIO	21001	21101	12011	11111
0	ON	ON		
1	ON	ON	ON	ON
2			ON	ON
3				
4			ON	

5	ON	ON	ON	ON
6	ON	ON		ON
7				
8				
9		ON		ON
10	ON	ON		ON
11	ON			
22				
24				ON
26	ON	ON	ON	ON
27	ON	ON	ON	
44				
56	ON	ON	ON	ON
65	ON	ON	ON	ON
94				

For vertex vectors switching states the legs condition are shown in Table 5.5.

Table 5.5 Working of vertex vectors

GPIO	**22002**	**21001**	**12002**	**00000**
0	ON	ON		
1	ON	ON	ON	
2			ON	ON
3				ON
4	ON		ON	
5	ON	ON	ON	
6		ON		ON
7				ON
8				
9				
10	ON	ON	ON	ON
11	ON	ON	ON	ON

22				
24				
26	ON	ON	ON	ON
27	ON	ON	ON	ON
44	ON		ON	
56	ON	ON	ON	
65		ON		ON
94				ON

5.4 EXPERIMENTAL SET-UP

In the experimental set-up, the twenty pins of GPIO of DSP are connected to twenty switches of three-level five-phase inverter. Input voltage given to the inverter is 100V. The programs for method 1 & 2 are built in computer programming. Multimeters are used to measure the current and the voltage. The experimental set-up consisting of inverter, digital storage oscilloscope, DC supply & induction motor acting as load as shown in Fig. 5.3.

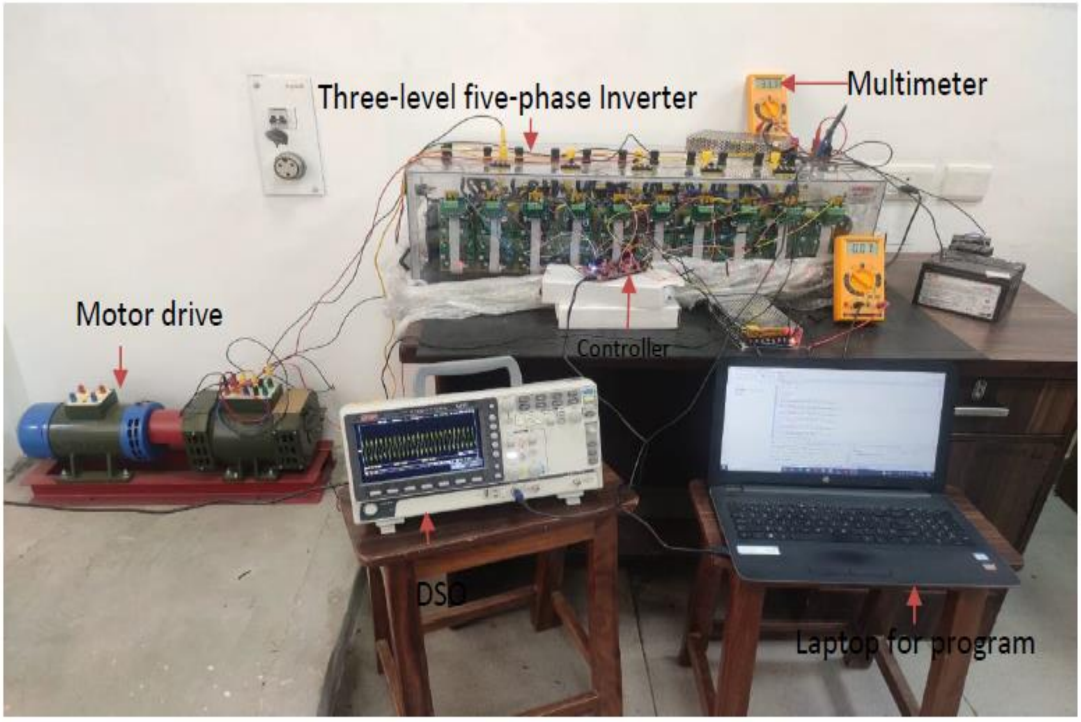

Fig. 5.3 Experimental set-up

5.5 EXPERIMENTAL RESULTS

The experiment results of the proposed method are taken & shown in this section. The control signals are given through TMSF28379D at frequency of 5KHz. Fig. 5.4 shows the results of method-1 of CMV elimination in which by giving 100V supply, CMV is coming out as 2V at modulation index of 0.9. Fig. 5.5 shows the result of method-II of CMV elimination in which by giving 100V supply, CMV will be coming out as 2V at modulation index of 0.9. In Fig. 5.6 classical method gives the CMV more than, method-I & method-II which is approx. 50V $\left(\frac{V_{dc}}{2}\right)$.

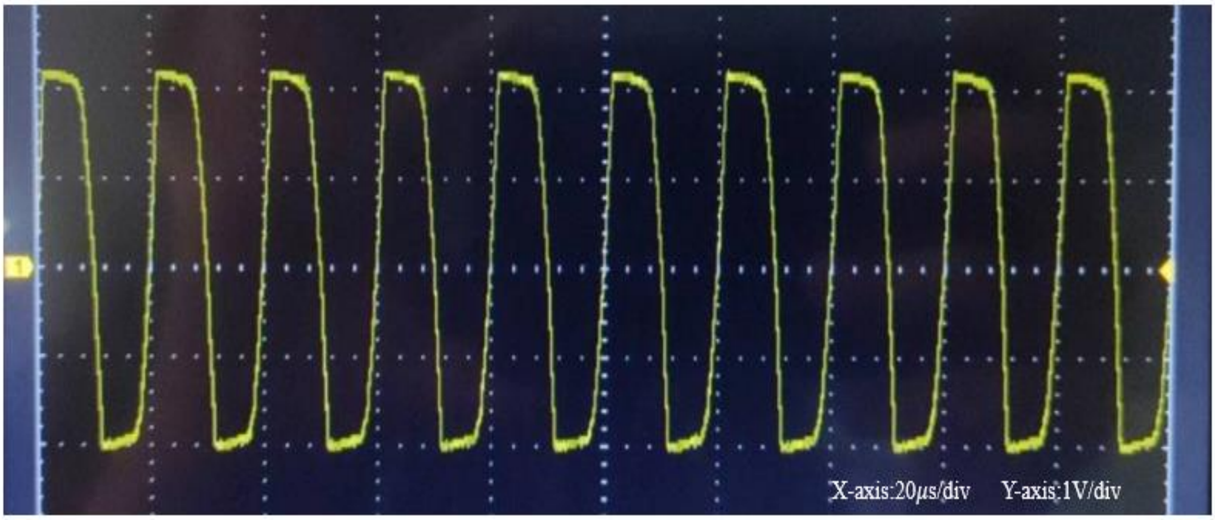

Fig. 5.4 CMV of method-I [M=0.9]

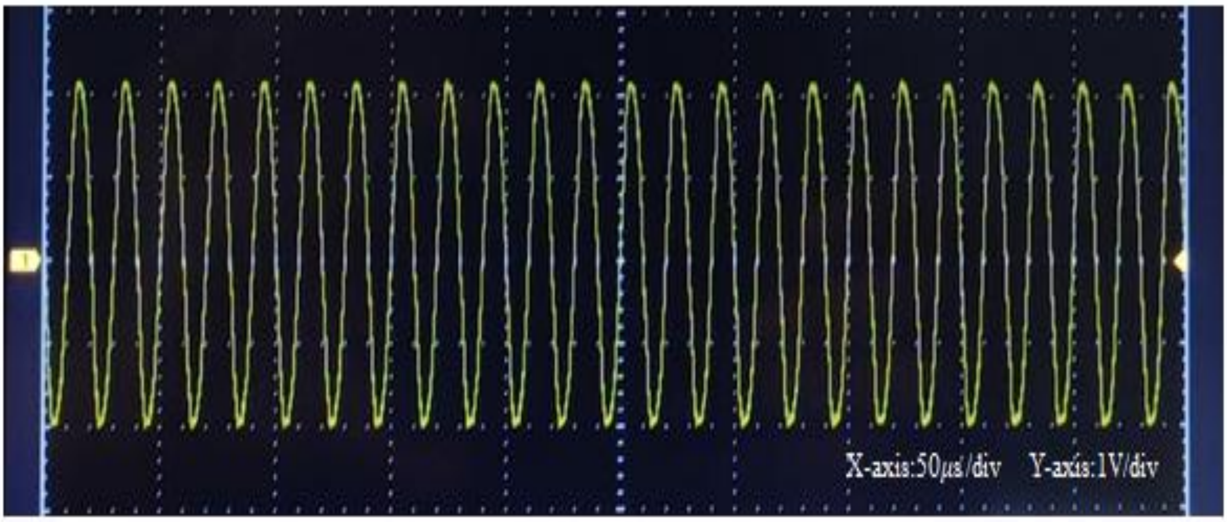

Fig. 5.5 CMV of method-II [M=0.9]

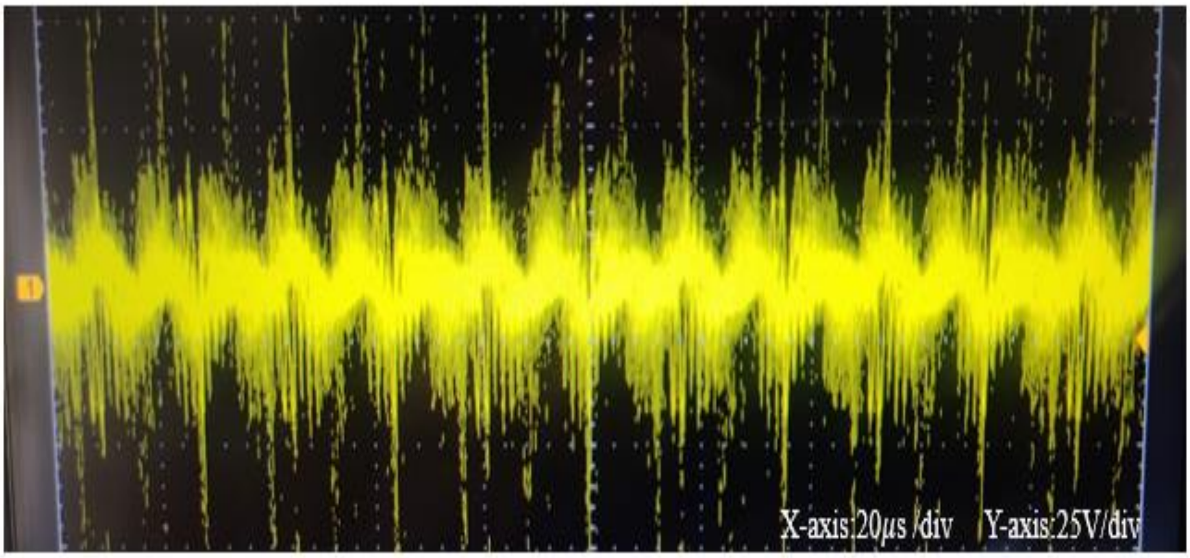

Fig. 5.6 CMV of classical method [M=0.9]

CHAPTER 6
CONCLUSION AND FUTURE SCOPE

CONCLUSION

The CMV is one of the main reasons for the bearing failures in motor. SVPWM is developed to eliminate the CMV for three-level five-phase inverter. In this technique, only those switching states that give CMV zero are considered. Hence, the proposed SVPWM technique for five-phase powered three-level VSI has eliminated the CMV. Two different methods are presented in this project. In the first method, large and zero voltage vectors are selected to achieve CMV elimination and maximum DC link. In the second method, large, medium and zero voltage vectors are selected to achieve CMV elimination and *x-y* stator plane elimination. Simulation and experimental results confirm the validity of the techniques.

FUTURE SCOPE

In future, this SVPWM technique can be applied for other multiphase machines. The proposed methods can be extended to multilevel inverters for CMV elimination. The proposed methods can be extended to the control strategies where CMV elimination is required.

ANNEXURE

FOR PROPOSED SYSTEM

```
#include "F28X_Project.h"
int i=0;
void main(void)
{
InitSysCtrl();
InitGpio();
GPIO_SetupPinMux(27,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(31, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(0,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(34, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(22,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(22, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(56,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(52, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(65,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(67, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(94,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(94, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(1,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(1, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(2,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(2, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(3,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(3, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(4,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(4, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(5,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(5, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(6,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(6, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(7,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(7, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(8,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(8, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(9,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(9, GPIO_OUTPUT, GPIO_PUSHPULL);
```

```
GPIO_SetupPinMux(10,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(10, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(11,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(11, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(24,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(24, GPIO_OUTPUT,  );
GPIO_SetupPinMux(25,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(25, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(26,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(26, GPIO_OUTPUT, GPIO_PUSHPULL);
    while(1)
    {
        for(i=1; i<4; i++)
        {
               if (i==1)
                            {
                                GpioDataRegs.GPASET.bit.GPIO0= 1;
                                GpioDataRegs.GPASET.bit.GPIO1= 1;
                                GpioDataRegs.GPACLEAR.bit.GPIO2= 1;
                                GpioDataRegs.GPACLEAR.bit.GPIO3= 1;
                                GpioDataRegs.GPACLEAR.bit.GPIO4= 1;
                                GpioDataRegs.GPASET.bit.GPIO5 = 1;
                                GpioDataRegs.GPASET.bit.GPIO6 = 1;
                                GpioDataRegs.GPACLEAR.bit.GPIO7 = 1;
                                GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;
                                GpioDataRegs.GPACLEAR.bit.GPIO9= 1;
                                GpioDataRegs.GPASET.bit.GPIO10= 1;
                                GpioDataRegs.GPASET.bit.GPIO11 = 1;
                                GpioDataRegs.GPACLEAR.bit.GPIO22 = 1;
                                GpioDataRegs.GPACLEAR.bit.GPIO24 = 1;
                                GpioDataRegs.GPASET.bit.GPIO26 = 1;
                                GpioDataRegs.GPASET.bit.GPIO27 = 1;
                                GpioDataRegs.GPBSET.bit.GPIO44 = 1;
                                GpioDataRegs.GPBSET.bit.GPIO56 = 1;
                                GpioDataRegs.GPCCLEAR.bit.GPIO65 = 1;
                                 GpioDataRegs.GPCCLEAR.bit.GPIO94 = 1;

                            }
```

```
if (i==2)
            {
                GpioDataRegs.GPASET.bit.GPIO0= 1;
                GpioDataRegs.GPASET.bit.GPIO1= 1;
                GpioDataRegs.GPACLEAR.bit.GPIO2= 1;
                GpioDataRegs.GPACLEAR.bit.GPIO3= 1;
                GpioDataRegs.GPASET.bit.GPIO4= 1;
                GpioDataRegs.GPASET.bit.GPIO5 = 1;
                GpioDataRegs.GPACLEAR.bit.GPIO6 = 1;
                GpioDataRegs.GPACLEAR.bit.GPIO7 = 1;
                GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;
                GpioDataRegs.GPACLEAR.bit.GPIO9= 1;
                GpioDataRegs.GPASET.bit.GPIO10= 1;
                GpioDataRegs.GPASET.bit.GPIO11 = 1;
                GpioDataRegs.GPACLEAR.bit.GPIO22 = 1;
                GpioDataRegs.GPACLEAR.bit.GPIO24 = 1;
                GpioDataRegs.GPASET.bit.GPIO26 = 1;
                GpioDataRegs.GPASET.bit.GPIO27 = 1;
                GpioDataRegs.GPBCLEAR.bit.GPIO44 = 1;
                GpioDataRegs.GPBSET.bit.GPIO56 = 1;
                GpioDataRegs.GPCSET.bit.GPIO65 = 1;
                 GpioDataRegs.GPCCLEAR.bit.GPIO94 = 1;
            }
if (i==3)
            {
                GpioDataRegs.GPACLEAR.bit.GPIO0= 1;
                GpioDataRegs.GPASET.bit.GPIO1= 1;
                GpioDataRegs.GPASET.bit.GPIO2= 1;
                GpioDataRegs.GPACLEAR.bit.GPIO3= 1;
                GpioDataRegs.GPACLEAR.bit.GPIO4= 1;
                GpioDataRegs.GPASET.bit.GPIO5 = 1;
                GpioDataRegs.GPASET.bit.GPIO6 = 1;
                GpioDataRegs.GPACLEAR.bit.GPIO7 = 1;
                GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;
                GpioDataRegs.GPASET.bit.GPIO9= 1;
                GpioDataRegs.GPASET.bit.GPIO10= 1;
                GpioDataRegs.GPACLEAR.bit.GPIO11 = 1;
                GpioDataRegs.GPACLEAR.bit.GPIO22 = 1;
                GpioDataRegs.GPASET.bit.GPIO24 = 1;
```

```
                                    GpioDataRegs.GPASET.bit.GPIO26 = 1;
                                    GpioDataRegs.GPACLEAR.bit.GPIO27 = 1;
                                    GpioDataRegs.GPBCLEAR.bit.GPIO44 = 1;
                                    GpioDataRegs.GPBSET.bit.GPIO56 = 1;
                                    GpioDataRegs.GPCSET.bit.GPIO65 = 1;
                                     GpioDataRegs.GPCCLEAR.bit.GPIO94 = 1;
                                    }
                             DELAY_US(1000); // micro seconds 5khz = 10000 micro seconds
                }
            }
        }
```

FOR CLASSICAL SYSTEM

```
//classical //
#include "F28X_Project.h"
int i=0;
void main(void)
{
InitSysCtrl();
InitGpio();
GPIO_SetupPinMux(27,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(31, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(0,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(34, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(22,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(22, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(56,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(52, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(65,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(67, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(94,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(94, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(1,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(1, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(2,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(2, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(3,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(3, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(4,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(4, GPIO_OUTPUT, GPIO_PUSHPULL);
```

```
GPIO_SetupPinMux(5,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(5, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(6,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(6, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(7,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(7, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(8,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(8, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(9,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(9, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(10,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(10, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(11,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(11, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(24,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(24, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(25,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(25, GPIO_OUTPUT, GPIO_PUSHPULL);
GPIO_SetupPinMux(26,GPIO_MUX_CPU1, 0);
GPIO_SetupPinOptions(26, GPIO_OUTPUT, GPIO_PUSHPULL);
    while(1)
    {
        for(i=1; i<5; i++)
        {
            if (i==1)
                                {
                                    GpioDataRegs.GPASET.bit.GPIO0= 1;
                                    GpioDataRegs.GPASET.bit.GPIO1= 1;
                                    GpioDataRegs.GPACLEAR.bit.GPIO2= 1;
                                    GpioDataRegs.GPACLEAR.bit.GPIO3= 1;
                                    GpioDataRegs.GPASET.bit.GPIO4= 1;
                                    GpioDataRegs.GPASET.bit.GPIO5 = 1;
                                    GpioDataRegs.GPACLEAR.bit.GPIO6 = 1;
                                    GpioDataRegs.GPACLEAR.bit.GPIO7 = 1;
                                    GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;
                                    GpioDataRegs.GPACLEAR.bit.GPIO9= 1;
                                    GpioDataRegs.GPASET.bit.GPIO10= 1;
                                    GpioDataRegs.GPASET.bit.GPIO11 = 1;
                                    GpioDataRegs.GPACLEAR.bit.GPIO22 = 1;
```

```
                GpioDataRegs.GPACLEAR.bit.GPIO24 = 1;
                GpioDataRegs.GPASET.bit.GPIO26 = 1;
                GpioDataRegs.GPASET.bit.GPIO27 = 1;
                GpioDataRegs.GPBSET.bit.GPIO44 = 1;
                GpioDataRegs.GPBSET.bit.GPIO56 = 1;
                GpioDataRegs.GPCCLEAR.bit.GPIO65 = 1;
                 GpioDataRegs.GPCCLEAR.bit.GPIO94 = 1;
            }

    if (i==2)
            {
                GpioDataRegs.GPASET.bit.GPIO0= 1;
                GpioDataRegs.GPASET.bit.GPIO1= 1;
                GpioDataRegs.GPACLEAR.bit.GPIO2= 1;
                GpioDataRegs.GPACLEAR.bit.GPIO3= 1;
                GpioDataRegs.GPACLEAR.bit.GPIO4= 1;
                GpioDataRegs.GPASET.bit.GPIO5 = 1;
                GpioDataRegs.GPASET.bit.GPIO6 = 1;
                GpioDataRegs.GPACLEAR.bit.GPIO7 = 1;
                GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;
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                GpioDataRegs.GPASET.bit.GPIO11 = 1;
                GpioDataRegs.GPACLEAR.bit.GPIO22 = 1;
                GpioDataRegs.GPACLEAR.bit.GPIO24 = 1;
                GpioDataRegs.GPASET.bit.GPIO26 = 1;
                GpioDataRegs.GPASET.bit.GPIO27 = 1;
                GpioDataRegs.GPBLEAR.bit.GPIO44 = 1;
                GpioDataRegs.GPBSET.bit.GPIO56 = 1;
                GpioDataRegs.GPCSET.bit.GPIO65 = 1;
                 GpioDataRegs.GPCCLEAR.bit.GPIO94 = 1;
            }

     if (i==3)
            {
                GpioDataRegs.GPACLEAR.bit.GPIO0= 1;
                GpioDataRegs.GPASET.bit.GPIO1= 1;
                GpioDataRegs.GPASET.bit.GPIO2= 1;
                GpioDataRegs.GPACLEAR.bit.GPIO3= 1;
                GpioDataRegs.GPASET.bit.GPIO4= 1;
```

```
                  GpioDataRegs.GPASET.bit.GPIO5 = 1;
                  GpioDataRegs.GPACLEAR.bit.GPIO6 = 1;
                  GpioDataRegs.GPACLEAR.bit.GPIO7 = 1;
                  GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;
                  GpioDataRegs.GPACLEAR.bit.GPIO9= 1;
                  GpioDataRegs.GPASET.bit.GPIO10= 1;
                  GpioDataRegs.GPASET.bit.GPIO11 = 1;
                  GpioDataRegs.GPACLEAR.bit.GPIO22 = 1;
                  GpioDataRegs.GPACLEAR.bit.GPIO24 = 1;
                  GpioDataRegs.GPASET.bit.GPIO26 = 1;
                  GpioDataRegs.GPASET.bit.GPIO27 = 1;
                  GpioDataRegs.GPBSET.bit.GPIO44 = 1;
                  GpioDataRegs.GPBSET.bit.GPIO56 = 1;
                  GpioDataRegs.GPCCLEAR.bit.GPIO65 = 1;
                   GpioDataRegs.GPCCLEAR.bit.GPIO94 = 1;
                  }
if (i==4)
             {
                  GpioDataRegs.GPACLEAR.bit.GPIO0= 1;
                  GpioDataRegs.GPACLEAR.bit.GPIO1= 1;
                  GpioDataRegs.GPASET.bit.GPIO2= 1;
                  GpioDataRegs.GPASET.bit.GPIO3= 1;
                  GpioDataRegs.GPACLEAR.bit.GPIO4= 1;
                  GpioDataRegs.GPACLEAR.bit.GPIO5 = 1;
                  GpioDataRegs.GPASET.bit.GPIO6 = 1;
                  GpioDataRegs.GPASET.bit.GPIO7 = 1;
                  GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;
                  GpioDataRegs.GPACLEAR.bit.GPIO9= 1;
                  GpioDataRegs.GPASET.bit.GPIO10= 1;
                  GpioDataRegs.GPASET.bit.GPIO11 = 1;
                  GpioDataRegs.GPACLEAR.bit.GPIO22 = 1;
                  GpioDataRegs.GPACLEAR.bit.GPIO24 = 1;
                  GpioDataRegs.GPASET.bit.GPIO26 = 1;
                  GpioDataRegs.GPASET.bit.GPIO27 = 1;
                  GpioDataRegs.GPBCLEAR.bit.GPIO44 = 1;
                  GpioDataRegs.GPBCLEAR.bit.GPIO56 = 1;
                  GpioDataRegs.GPCSET.bit.GPIO65 = 1;
                   GpioDataRegs.GPCSET.bit.GPIO94 = 1;
  }
```

```
 DELAY_US(1000); // micro seconds 5khz = 1000 micro seconds
        }


    }
}
```

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