DESIGN OF LOW POWER OPERATIONAL AMPLIFIER

Thesis submitted towards the partial fulfillment of the requirements for the award of the degree of

Master of Technology (VLSI Design & CAD)

Submitted by

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A person who never made a mistake never tried anything new.

-Albert Einstein

CERTIFICATE

I hereby certify that the work which is presented in the thesis entitled **"DESIGN OF LOW POWER OPERATIONAL AMPLIFIER"**, in partial fulfillment of the requirements for the award of degree of **Master of Technology in VLSI Design & CAD at Thapar University, Patiala** is an authentic record of my own work carried out under the supervision of **Ms. Alpana Agarwal**, Assistant Professor, Department of Electronic and Communication Engineering and refers other researcher's work which are duly listed in the reference section.

The matter embedded in this thesis has not been submitted for the award of any other degree of this or any other university.

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ABSTRACT

The main objective of this thesis is to decrease power dissipation. A low power CMOS operational amplifier using weak inversion region of MOSFET for biomedical instrumentation operating with a 1.8V supply is described. The opamp is designed in UMC .18μm CMOS technology using tool cadence. Two types of compensation techniques (a) RC compensation (b) Current buffer are used. With RC compensation technique, the open loop gain is 76.97 db, the gain bandwidth product (GBW) is 489.9 kHz, CMRR obtained is 79.11 db, with large range of ICMR 0V to 1.689V and phase margin is 56.09 degree with 10pF load. The power consumption is 1.516 μW. With Current buffer compensation technique, the open loop gain is 76.21db, the gain bandwidth product (GBW) is 743.2 kHz, CMRR obtained is 157.1db, with large range of ICMR 0.119V to 1.54V and phase margin is 62.77 degree with 10pF load. The power consumption is 3.69μW. Current buffer compensation technique provide high CMRR, high gain bandwidth product and high phase margin as compared to RC compensation technique. Also, area requirement for current buffer compensation technique is very less as compared to RC compensation technique. In this thesis work PVT variations are also given. Process variations management techniques are also discussed.

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CHAPTER

INTRODUCTION

The world is an analog place and the use of analog processing allows electronic circuits to interact with the physical world. Digital techniques also have importance but there are many analog building blocks such as operational amplifiers, transistor amplifiers, comparators, A/D and D/A converters, phase-locked loops and voltage references etc. that are still used and will be used in the future.

1.1 MOTIVATION [1]

The era of low power microelectronics began with the invention of transistor in the late 1940's and came of age with the invention of the integrated circuit in the late 1950's. Historically, the most demanding applications of low power microelectronics have been battery operated products such as wrist watches, hearing aids, implantable cardiac pacemakers, pocket calculators, pagers, cellular telephones and prospectively, the hand held multi-media terminal. However, in early 1990's low power microelectronics rapidly evolved as a mainstream of microelectronics. The principal reasons for this transformation were the increasing packaging density of the transistor and increasing clock frequencies of CMOS microchips pushing heat removal and power distribution to the forefront of the problems confronting the advance of microelectronics.

Historically, the motivation for the low power electronics has stemmed from three reasonably distinct classes of need: (1) the earliest and the most demanding of these is the portable battery operated equipment that is sufficiently small in size and weight and long in operating life to satisfy user; (2) the most recent need is for ever increasing packing density in order to further enhance the speed of high performance systems which imposes severe restrictions on power dissipation density; and (3) the broadest need is for conservation of power in desktop and desk side systems where a competitive life cycle cost-to-performance ratio demands low power operation to reduce power supply and cooling cost.

So, the power consumed by a integrated circuit must be reduced to reduce heat dissipation and to save energy in battery-operated instruments. Yet, some reduction in performance must be accepted to achieve micropower operation

1.2 APPLICATION OF LOW POWER OPAMP [2, 3, 4]

Low power circuits required in battery operated devices. Low power opamp can be used as bio-potential amplifier. The essential purpose of a bio-potential amplifier is to amplify and filter the extremely weak bio-potential signals. However, the design of this amplifier is not straight forward. Bio-potential amplifiers must cope with various challenges in order to extract the bio-potential signals. Meanwhile, the power dissipation of the amplifier must be minimized for long-term power autonomy. The challenges of designing a bio-potential amplifier for portable bio-potential acquisition systems can be summarized as follows:

- High CMRR.
- Low-noise for high signal quality.
- Ultra-low power dissipation for long-term power autonomy. The bio-potential amplifier should minimize its power dissipation to improve the power autonomy
- Configurable gain and filter characteristics that suit the needs of different bio-potential signals and different applications.

In biomedical field low power opamp is useful as bio-potential amplifier require small bandwidth. For example, one of the most important electrophysiological measurements in medical diagnosis and patient care is that of the electrocardiogram (ECG or EKG). The amplitude and wave shape of the ECG depends on where the measuring electrode pair is located on the skin surface. It consists of QRS spike, P wave and T wave, the ECG QRS spike can range from a 500 μV to 5 mV peak. Its amplitude depends on the recording site and the patient's body type.

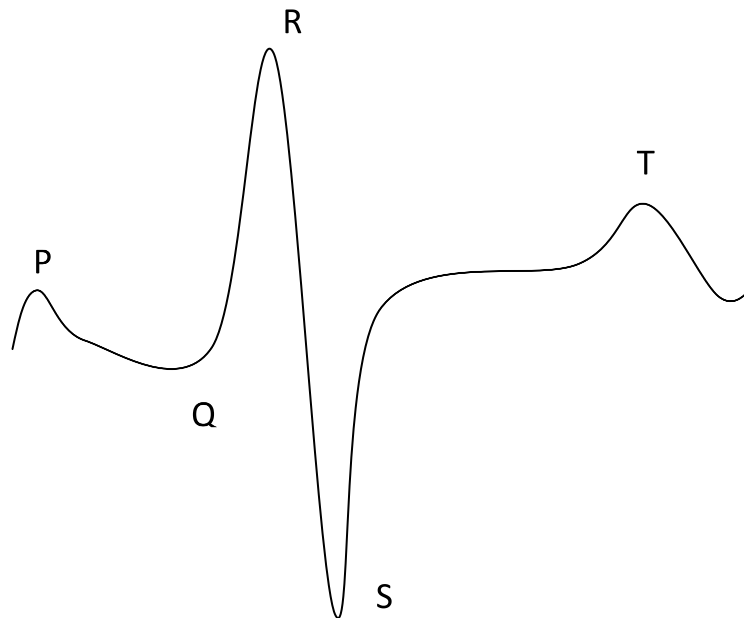

Figure 1.1 ECG signal

ECG amplifiers are reactively coupled with standardized -3-dB corner frequencies at 0.05 and 100 Hz. Signals such as ECG and EEG require approximately 0.1 to 100 Hz. The fundamental frequency for the QRS complex at the body surface is 10 Hz, and most of the diagnostic information is contained below 100 Hz in adults, although low amplitude, high-frequency components as high as 500 Hz have been detected and studied. The QRS of infants often contains important components as high as 250 Hz. The fundamental frequency of T waves is approximately 1 to 2 Hz. RR interval gives the indication of heart rate.

Heart Rate = Beats/Minute=60(RR intervals in seconds)

The common-mode rejection specified by the AAMI (Association for the Advancement of Medical Instrumentation) is 90 dB minimum for standard ECG and 60 dB minimum for ambulatory recorders.

According to AAMI worst case ECG pulse has a slew rate of 0.28V/s. AAMI defined highest slew rate for ECG equipment can be estimated by dividing the maximum peak amplitude with in AAMI range 0.5 to 5mV and dividing it by minimum rise time of QR interval within the AAMI range of 17.5 to 52.5ms. This gives a maximum slew rate of 5mV /17.5ms = 0.28V/s for a worst case ECG pulse [3].

1.3 THESIS ORGANIZATION

CHAPTER1: INTRODUCTION. This chapter introduces motivation, application of low power operational amplifier and organization of thesis work.

CHAPTER2: LOW POWER TECHNIQUES. This chapter discuss low power techniques for analog designing and specifications for designing is also decided in this chapter

CHAPTER3: PARAMETER EXTRACTION OF MOS IN SUBTHRESSHOLD REGION. In this chapter MOS subthresshold parameters like n, $I_{o,}$ coefficient of channel length modulation are calculated experimentally.

CHAPTER4: DESIGN OF TWO STAGE OPAMP USING GM/I_D METHODLOGY. In this chapter two stage opamp is designed with RC compensated techniques using $g_m/I_{D.}$Also process corner simulation is done.

CHAPTER5: DESIGN OF TWO STAGE OPAMP WITH CURRENT BUFFER COMPENSATION TECHNIQUE. Two stage opamp is designed using current buffer technique and it is compared with RC compensated opamp designed in previous chapter and also simulated on all PVT variations.

CHAPTER6: LAYOUT DESIGN AND POST LAYOUT SIMULATION. In this chapter, layout design and post layout simulation is done over all PVT variations.

CHAPTER 7: CONCLUSIONS AND FUTURE RESEARCH. This chapter summarizes the major accomplishments of this thesis and presents the scope for future and further research.

CHAPTER

LOW POWER TECHNIQUES

2.1 LOW POWER TECHNIQUES

Preamplifier is an important block of biomedical sensor architecture and designing an ultra low power preamplifier has become an important research area. In order to achieve ultra low power consumption requirement, preamplifier can be implemented using bulk input MOS transistor, FGCMOS technique, current driven bulk technique (CDB technique; this is basically low voltage technique. In this technique threshold voltage of transistor is reduced for low voltage applications) and weak inversion MOS transistor technique, in this technique bias current is minimized. However, very low bias current reduces performance of amplifier. Low power preamplifier can be used to reduce heat dissipation and to save energy in battery-operated instruments. Portable health monitoring devices usually contain various types of sensors such as heart rate sensor, ECG sensor, hearing aids etc. Small size and to sustain long battery life these sensor must consume very small current. These reasons are making it necessary to develop circuit techniques and building blocks operating with low power consumption. In this chapter, above mentioned low power techniques for analog designing are discussed.

2.1.1 BULK – DRIVEN MOSFETS

BULK DRIVEN PRINCIPLE [5]

An important factor concerning analog circuits is that the threshold voltages of future standard CMOS technologies are not expected to decrease much below what is available today. To overcome the threshold voltage a bulk-driven MOST has been used, it is well known that a reverse bias on the well-source junction will cause the threshold voltage to increase. Similarly, a forward bias on this junction will cause the threshold voltage to decrease.

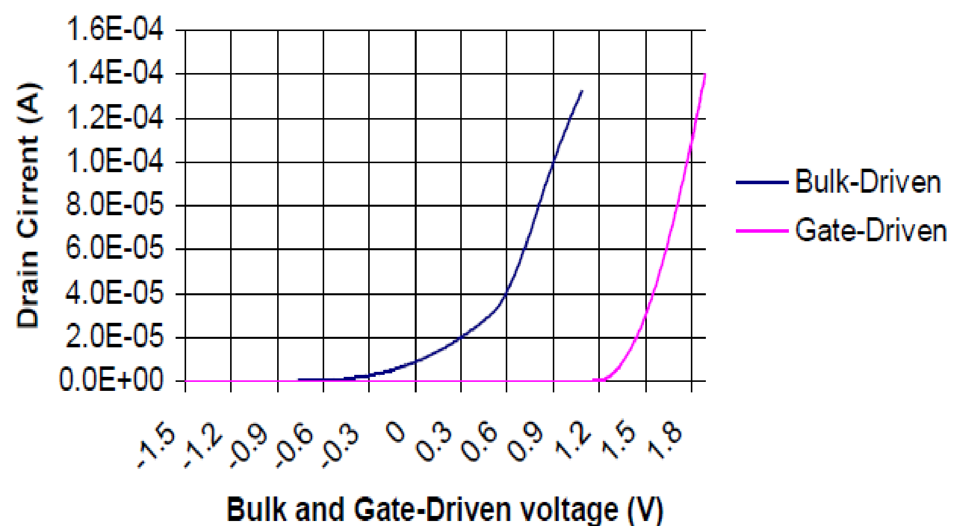

Figure 2.1 Drain current versus Bulk and Gate-Driven voltage

The bulk-driven transistor is a good solution to overcome the threshold voltage Limitation. It can work under negative, zero, or even slightly positive biasing condition as depicted on Figure 2.1.

To enable bulk driving, one must first bias the gate to form a conduction channel inversion layer by connecting the gate terminal to a fixed voltage that is sufficient to form an inversion layer (e.g., $V_{GS} > V_T$ for the NMOS)

The operation of the bulk-driven MOSFET is of depletion type. The gate-source voltage is set to a value sufficient to turn on the transistor. Input voltage is then applied to the

bulk-termina1 (i.e. well) of the transistor to modulate the current flow through the transistor. The advantage of a bulk-driven device over a gate-driven device is that the threshold voltage limitation disappears and both positive and negative bias voltages are possible.

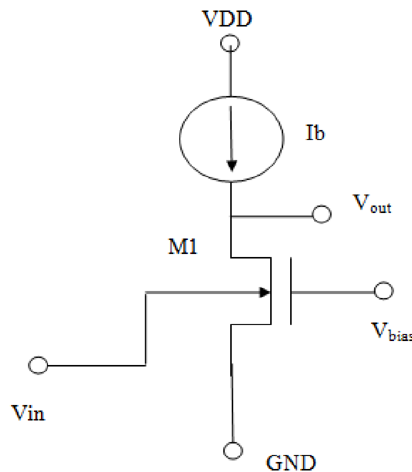

Figure 2.2 Bulk-driven MOS transistor

This is especially important in analog low voltage circuits where the dynamic range of the signal should be maximized with respect to the supply voltage in order to maximize the performance of the circuit. There are also some drawbacks of bulk-driven devices compared to gate-driven devices, such as smaller transconductance (g_{mb} instead of g_m) because of smaller control capacitance of the depletion layer, larger parasitic capacitance to the substrate, which results in lower f_T, and higher input referred noise, because of smaller transconductance. Also, it has to be noted that there is only one type of bulk-driven devices available (PMOS in n-well or NMOS in p-well) depending on the process used. By applying the input signal to the bulk-terminals instead of gate-terminals of the input transistors, the threshold voltage limitation disappears and a large input CMR of the opamp is achievable.

2.1.2 FLOATING GATE TECHNIQUE [6]

In floating gate transistor the charge on the gate of MOSFET is controlled by two or more inputs through poly-poly capacitor between each input and the floating gate (figure 2.3(a)).

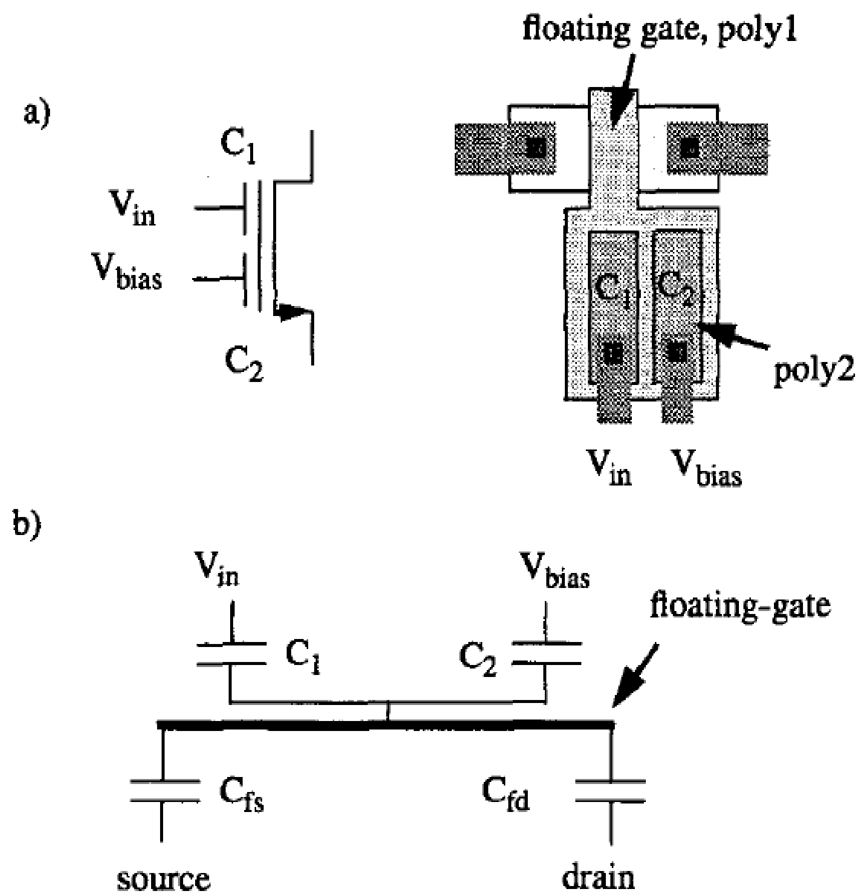

Figure 2.3 floating gate MOSFET: (a) ideal device (b) practical device

By using one input for the signal and one for bias voltage, the floating gate potential can be partly set by the bias voltage, (figure 2.3(a)) the floating gate potential V_{FGB} is,

$$V_{FGB} = (C_1 V_{in} + C_2 V_{bias}) / (C_1 + C_2) \tag{2.1}$$

The potential of the floating-gate is controlled also by source and drain voltages through capacitances C_{fs}, C_{fd} respectively (Figure 2.3(b)) and by any possible parasitic capacitances to other nodes.

The potential of the floating gate is also determined by a random charge component (Q_{fg}). During processing a random amount of charge accumulates on the floating-gate causing a change in its potential and in the case of a differential pair an offset since the amount of charge on the two floating-gates may be different. This charge can be removed by grounding the inputs and exposing the poly-poly capacitor edges to shortwave UV-light.

2.1.3 CURRENT DRIVEN BULK (CDB) TECHNIQUE [7]

Current driven bulk (CDB) technique can be used to achieve low power and low voltage design. The CDB technique was introduced as a method for low voltage design by reducing threshold voltage. Current Driven Bulk (CDB) as a technique to reduce the threshold voltage of MOS transistor in standard CMOS technology. CDB technique, which is used as a method for compensating body effect, as means of reducing the threshold voltage in some transistors.

The relationship between threshold-voltage and V_{BS}, which is called bulk bias voltage, is given as:

$$V_{th} = V_{th0} + \gamma\left(\sqrt{\left|2\phi_F - V_{BS}\right|} - \sqrt{2\phi_F}\right) \tag{2.2}$$

Where V_{th0}: zero bias threshold voltage

γ: bulk effect factor

φ_F: Fermi potential

The relationship between threshold voltage and acceptor concentration (N_A) in NMOS can be expressed using the following equations:

$$V_{th0} = \phi_{ms} + 2\phi_F - \frac{Q_{Bo}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_i}{C_{ox}} \tag{2.3}$$

$$QBo = \sqrt{2qN_A\varepsilon_{si}\left|-2\phi_F\right|} \tag{2.4}$$

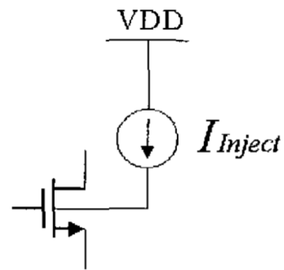

Figure 2.4 NMOS CDB transistor

Injecting a current into the bulk in NMOS would change the acceptor concentration (NA), which in turn, causes a decrease in the threshold voltage of NMOS. Same understanding is valid for PMOS and donor concentration by extracting an electron from hulk. In semiconductor physics, the V_{th} of an NMOS is usually defined as the gate voltage for which the interface is “as much n-type as the substrate is p-type.

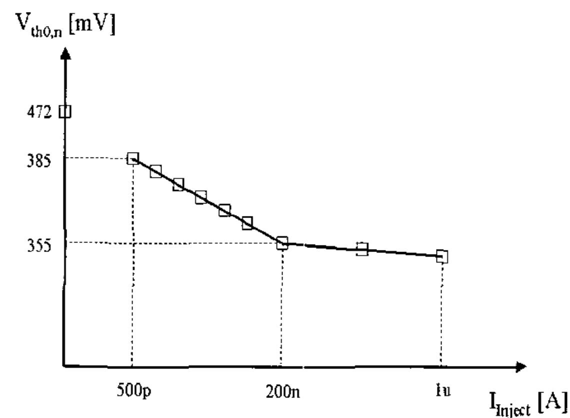

Figure 2.5 Effect of injection current on threshold voltage

Effect of injection current on thresshold voltage is shown in figure2.5. One can observe reduction in threshold voltage

2.1.4 WEAK INVERSION TECHNIQUE [8]

A simple model for weak inversion is given as

$$i_D = \frac{W}{L} I_{Do} \exp\left(\frac{v_{GS}}{n(KT/q)}\right) \tag{2.5}$$

Where

n is the subthresshold slope factor and its value of n is greater than 1 and less than 3 and I_{Do} is process dependent parameter. It also depends on v_{SB} and V_T .

The point at which transistor enters the weak inversion region can be approximated as

$$v_{gs} < V_T + n\frac{KT}{q} \tag{2.6}$$

Operation of the MOS device in subthresshold region is very important when low power circuits are desired.

From above equation, the transconductance can be derived as

$$g_m = \frac{I_D}{nKT/q} \tag{2.7}$$

There is linear relationship between transconductance and current. Also transconductance is independent of device geometry. But in strong inversion relationship between transconductance and current is square law and also function of device geometry.

2.2 SPECIFICATIONS

Specifications are decided according to previous research on low power opamp using above mentioned techniques bulk input technique, FGCMOS technique and from biomedical application discussed in 1.2. In table2.1 previous research work and target specification are shown.

TABLE 2.1

PREVIOUS RESEARCH WORK RESULTS

AND TARGET SPECIFICATIONS

YEAR	**UNITS**	**2005 [9]**	**2000 [10]**	**2000 [11]**	**2008 [12]**	**TARGET SPECFICATION**
TECHNIQUE			bulk input	floating gate input		weak inversion
SUPPLY	V	3	1	1.2		1.8
AO	db	55.56	70	65	65	>70
UGB	kHz		190	230		>250
-3DB	Hz	170			127	>100
PHASE MARGIN	Degree		60	62		60
POWER DISSIPATION	μ W	66	5	5.16	104	<5
SR+	kV/s	50	150	180	41	>200
SR-	kV/s					>200
CMRR	db	100			110	>85
PSRR	db				80	>90
ICMR(MAX)	V	2				1.3
ICMR(MIN)	V	0.3				0.2
C_L	pF		7	9	10	10
C_C	pF		4	2	150	

In table 2.2 previous research work on low power opamp is shown. All research work shown below are taken from low power opamp for biomedical application.

TABLE 2.2

PREVIOUS RESEARCH WORK RESULTS [13]

YEAR	**UNITS**	**2002**	**2004**	**2005**	**2007**	**2009**
CMOS TECHNOLOGY		.7 μ	1.5 μ	.35 μ	.18 μ	.18 μ
SUPPLY	V	5	3V	3	1	1.8
AO	db	60.6	39.3	56	14	60
UGB	kHz	5.5	2.7	130	2.7	2820
-3DB	Hz					
PHASE MARGIN	Degree					63.5
POWER DISSIPATION	μ W	11000	114.8	72.6	3.15	37.8
SR+	kV/s		6400	50	10	3450
SR-	kV/s		6400	50	10	1670
CMRR	db	137		100		85
PSRR	db		50		56	100

CHAPTER 3

PARAMETER EXTRACTIONS OF MOS IN SUBTHRESSHOLD REGION

Procedure for extracting parameters of MOS [14] in subthresshold regions is mentioned here. I_D for weak inversion is given as

$$I_D = I_o \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{nU_T}} \left(1 - e^{-\frac{V_{DS}}{nU_T}}\right)$$

(3.1)

Where

$$I_o = 2.n.\mu.C_{ox} U_T^2 e \frac{V_{THo}}{nU_T} e \frac{(n-1)V_{BS}}{nU_T}$$

(3.2)

U_T is thermal voltage which is 25.9mV,

V_{TH} is threshold voltage and

n is subthresshold parameter

3.1 SUBTHRESSHOLD PARAMETER EXTRACTION

Subthresshold parameters of MOS in weak inversion can be calculated experimentally using I_D and V_{GS} curve in weak inversion region. Subthresshold parameter 'n' is normally measured from the slope of linear region $\ln(I_D)$ and V_{GS} curve in weak inversion region. Parameter extraction (I_o and n) for nmos in subthresshold region is given here.

3.1.1 SUBTHRESSHOLD SLOPE FACTOR 'n' EXTRACTION

Subthresshold parameter 'n' is normally measured from the slope of linear region $\ln(I_D)$ and V_{GS} curve in weak inversion region. From this curve we can measure the slope of the $\ln(I_{DS})$ vs V_{GS} curve shown in figure 3.1.This slope is also derived by differentiating the drain current in subthresshold region with respect to V_{GS} i.e. slope is obtained by differentiating equation (3.1) and is given as

$$slope = \frac{1}{nU_T} \tag{3.3}$$

Where U_T is thermal voltage which is 25.9mV.

From equation (3.3), Subthresshold parameter 'n' can be calculated as

n= 1.172

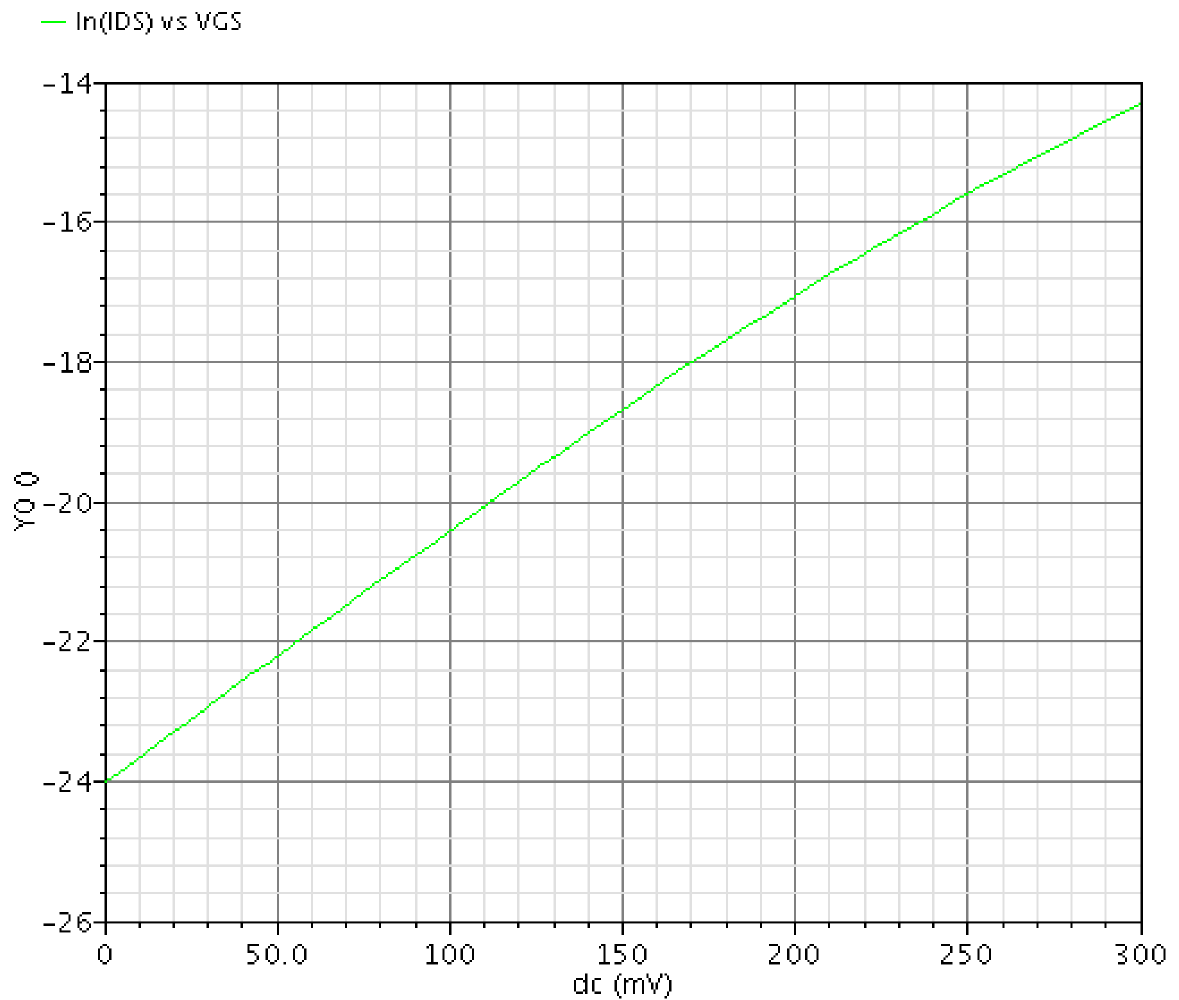

Figure 3.1 ln(I_D) and V_{GS} curve in weak inversion region

3.1.2 I_O EXTRACTION

I_o is calculated from I_D and V_{GS} curve in weak inversion region. I_D and V_{GS} curve in weak inversion region is given below in figure 3.2

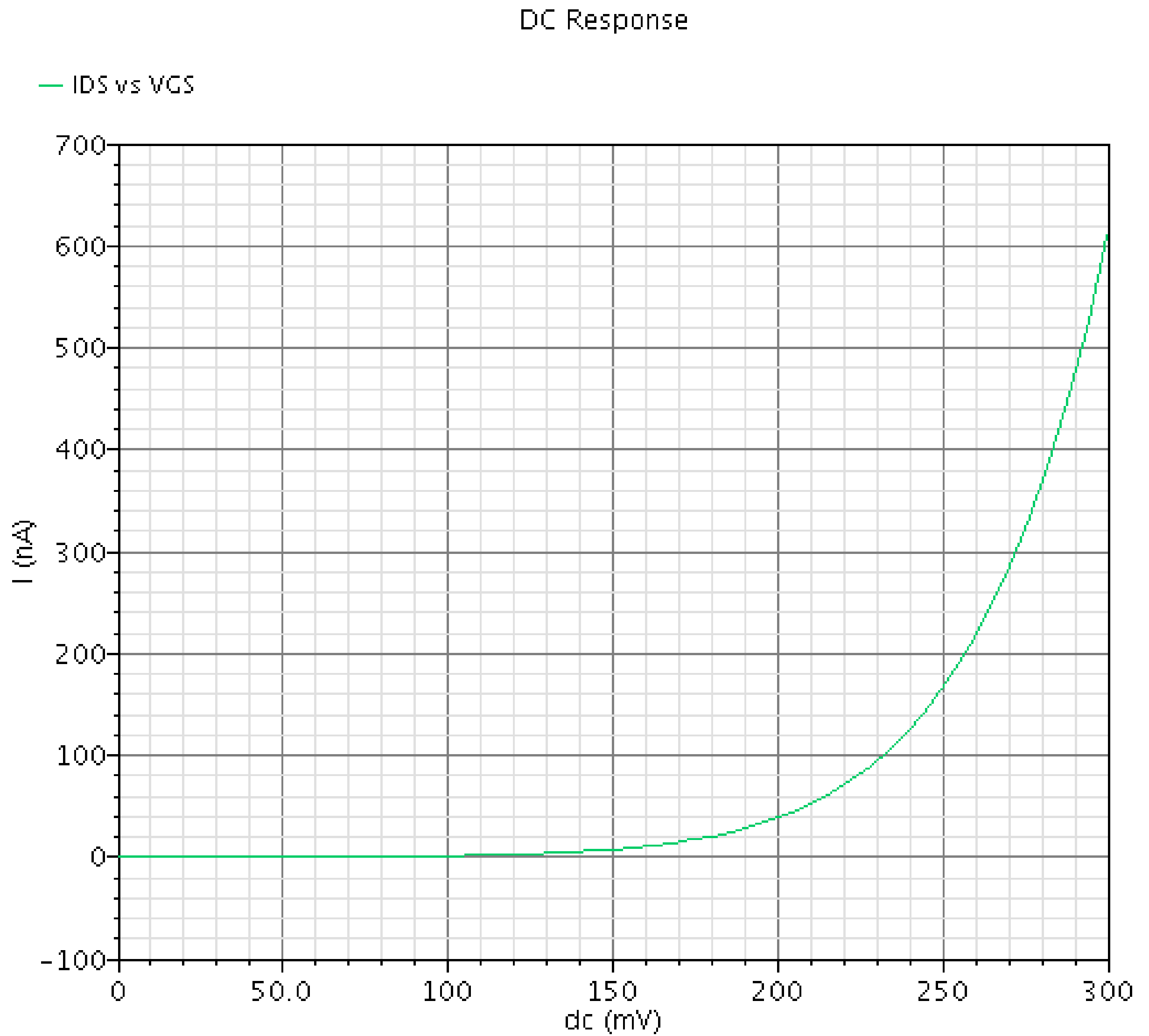

Figure 3.2 I_D and V_{GS} curve in weak inversion region

PROCEDURE FOR CALCULATING I_O:

Select four to five set of values of V_{GS} and corresponding values of I_D. And then calculate value of I_o using equation (3.1) for each set of values. And then averaging all values to get final value of I_o . I_D and V_{GS} curve in weak inversion region is given below in figure 3.2

TABLE 3.1

VALUES OF CURRENT AND VOLTAGES FROM

GRAPH IN FIGURE 3.2

V_{GS} (V)	I_{DS} (nA)	I_o (nA)
0.1	1.283	273.14
0.15	6.9832	281.24
0.2	34.64	276.70
0.25	145.07	224.45

Average value of I_o = 263.5nA

3.1.3 CALCULATION CHANNEL LENGTH MODULATION COEFFICIENT (LAMBDA, λ)

Channel length modulation coefficient can be calculated from curve I_{DS} vs V_{DS} given in figure 3.3.Channel length modulation coefficient can be calculated experimentally by using following formula:

$$\frac{I_{DS1}}{I_{DS2}} = \frac{1+\lambda V_{DS1}}{1+\lambda V_{DS2}} \tag{3.4}$$

For 2um length

$\lambda_{n,sub}$ = 0.28, for NMOS transistor in subthresshold region , λ_n = 0.13 for strong inversion and λ_p = 0.0215, for PMOS transistor

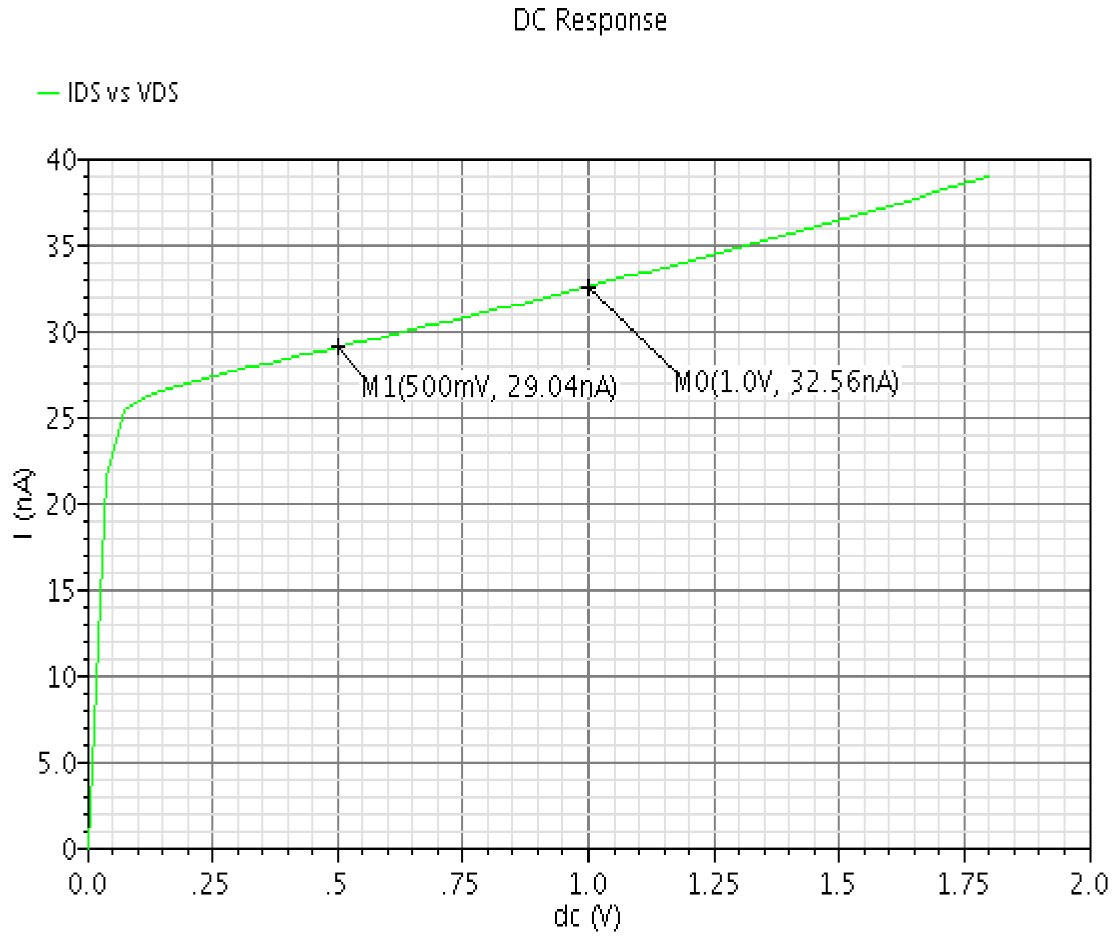

Figure 3.3 Plot between I_D vs V_{DS} for NMOS in subthresshold

CHAPTER

4

DESIGN OF TWO STAGE OPAMP USING GM/ID METHODOLOGY

The two stage operational amplifier is widely used analog building block. Schematic for two stage opamp with compensation block is shown in figure 4.1. Where CB is compensation block. The design procedure is based on the following main parameters: phase margin, gain bandwidth product, load capacitance, slew rate, input common mode range.

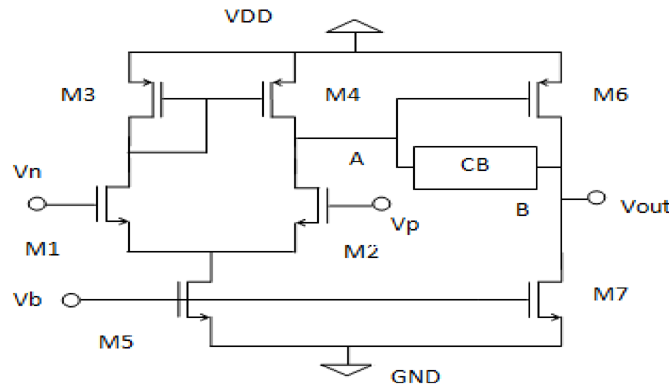

Figure 4.1 Circuit diagram of two stage opamp

Important parameters such as CMRR and PSRR, will not be used during design steps. Such parameters greatly depend on the amplifier topology and can be predicted by simulation using accurate transistor models. In this chapter designing of two stage opamp with RC compensation using gm/I_D methodology is given.

4.1 DESIGNING USING GM/I_D METHODOLOGY

gm/I_D characteristic of MOSFET tells about the region of the transistor operation and helps in calculating the dimensions of transistor. The main advantage of this method is that this curve is unique for given technology. This curve is called as current density plot. This curve gives the knowledge of inversion level i.e. whether the transistor is operating in weak inversion or in moderated inversion or in strong inversion. Knowledge of inversion level allows proper evaluation of design tradeoffs among gain, bandwidth etc. basically weak inversion favours gain and strong inversion favours bandwidth. This method minimizes the time spent on design stage and achieves major accuracy in results. The gm/I_D value is maximum in weak inversion and the maximum value is equal to 1/nU_T . The gm/I_D ratio decreases as the operating point moves toward the strong inversion when I_D or V_G are increased. The normalized current is independent of the transistor size. So, this current density plot is independent of size of transistor [15, 16].

The design flow for gm/I_D methodology is as follows:

1. Determine the gm from the given specification such as gain and bandwidth.

2. Determine the current from the given specifications such as power dissipation.

3. Decide L for the design depending on the specification requirement.

4. Get gm/I_D ratio.

5. Determine Bias voltage for current source bias for desired gm/$I_{D.}$

The relationship between g_m/I_D and the normalized current is a unique characteristic for all transistor of the same type (NMOS or PMOS).

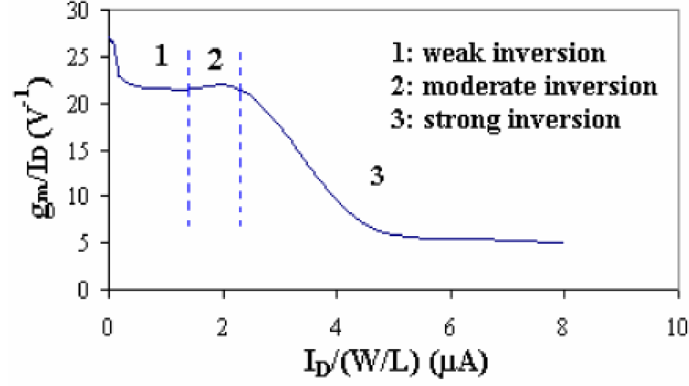

Figure 4.2 g_m/I_D Vs $I_D/(W/L)$ curve for NMOS

In present work, all NMOS transistors are put in subthresshold region and PMOS transistors are put in saturation region. This technique is used to calculate sizes of transistors using values of gm/I_D and I_D/W. these values are calculated from specifications. For example, First we fix the length L=2um. Current is calculated from power dissipation. Power dissipation is given as :

$$PD = V_{DD}I \tag{4.1}$$

From power dissipation we calculate current, I_{D1} = 200nA, I_{D5} = 400nA and $I_{D6,7}$ = 800nA

From gain and bandwidth we calculate gm/I_D for NMOS and PMOS transistors and from this corresponding normalized current we calculate W of each transistor.

Gain and bandwidth for two stage opamp is given as:

$$A = \frac{g_{m1}}{I_{D1}}\frac{g_{m6}}{I_{D6}}\frac{1}{(\lambda_n + \lambda_p)^2} \tag{4.2}$$

$$UGB = \frac{g_{m1}}{2\Pi C_C} \tag{4.3}$$

For UGB 250kHz , $\frac{g_{m1}}{I_{D1}} \geq 17.2$ and from $g_{m1} = \frac{I_{D1}}{nU_T}$, $\frac{g_{m1}}{I_{D1}} = 32.82$

From equation (4.2) and above value of $\frac{g_{m1}}{I_{D1}} = 32.82$, $\frac{g_{m6}}{I_{D6}}$ is calculated.

For NMOS transistors in subthresshold $V_{GS} < V_{TH.}$ Biasing voltage $V_b < V_{TH}$ for putting NMOS tail transistor in subthreshold region.

For 60° phase margin, $C_C = 0.22C_L$ (4.4)

$$C_C = 2.2pF \text{ where } C_L = 10pF$$

In RC compensated opamp [8], this resistor R allows independent control over the placement of the zero. In order to remove the right hand plane zero, R $= \frac{1}{g_{m6}}$. Another way is to move RHP zero to the LHP and place it on the top of p_2(2nd pole), for this value of R is given as

$$R = \frac{1}{g_{m6}}\left(\frac{C_C + C_L}{C_C}\right) \tag{4.5}$$

In present work, R is implemented using PMOS transistor in linear region as shown in figure 4.3

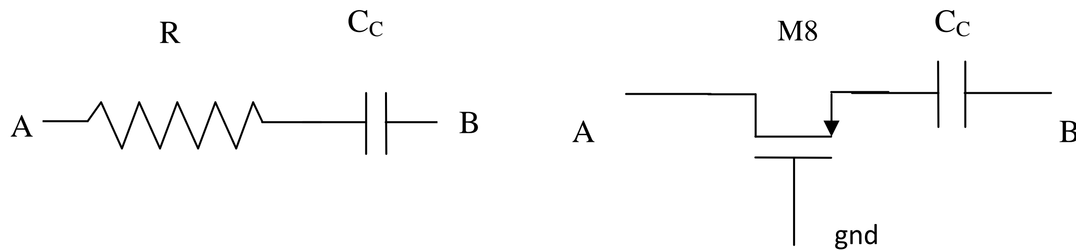

Figure 4.3 RC compensation block

Figure 4.1 and figure 4.2 shows the gm/I_D plot for NMOS and PMOS transistor respectively in .18um technology.

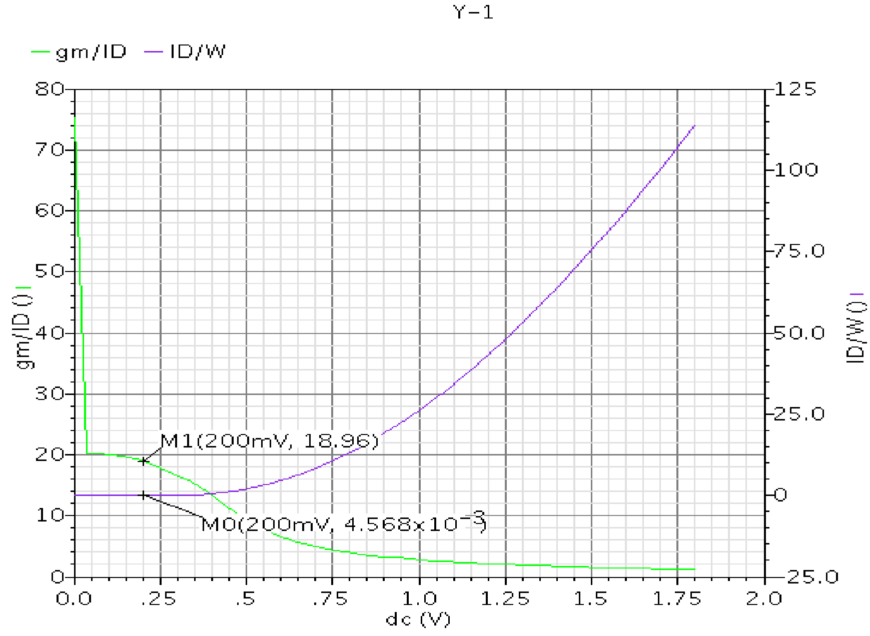

Figure 4.4 gm/I_D vs I_D/W plot for NMOS in .18 μ m technology

For V_{GS} = 0.2V less than threshold voltage, from gm/I_D vs I_D/W plot for NMOS in .18 μ m technology,

$$\frac{g_{m1}}{I_{D1}} = 18.96 \quad \text{and} \quad \frac{I_{D1}}{W} = 4.568 \times 10^{-3}$$

From power dissipation we calculate current, I_{D1} = 200nA, I_{D5} = 400nA and $I_{D6,7}$ = 800nA

$$\left(\frac{W}{L}\right)_{1,2} = \frac{43.782\mu m}{2\mu m} \tag{4.6}$$

$$\left(\frac{W}{L}\right)_{5} = \frac{87.56\mu m}{2\mu m} \tag{4.7}$$

$$\left(\frac{W}{L}\right)_{7} = \frac{175.13\mu m}{2\mu m} \tag{4.8}$$

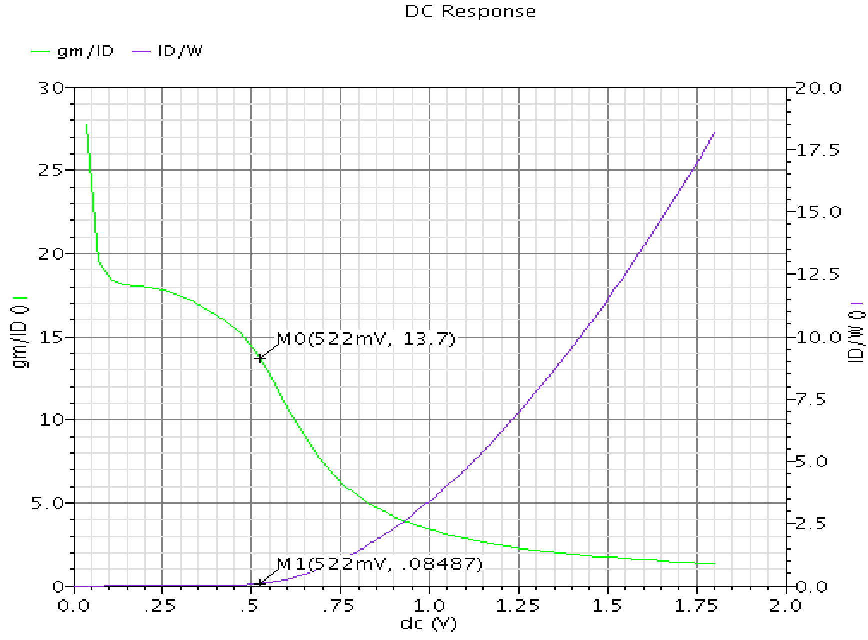

Figure 4.5 gm/I_D vs I_D/W plot for PMOS in .18 μ m technology

From gm/I_D vs I_D/W plot for PMOS in .18 μ m technology,

$$\frac{g_{m6}}{I_{D6}} = 13.7 \qquad \text{and} \qquad \frac{I_{D6}}{W} = 0.08487$$

$$\left(\frac{W}{L}\right)_6 = \frac{9.426\mu m}{2\mu m} \tag{4.9}$$

$$\left(\frac{W}{L}\right)_{3,4} = \frac{2.36\mu m}{2\mu m} \tag{4.10}$$

In RC compensated opamp, R is implemented using PMOS transistor in linear region and value of R is given as

$$R = \frac{1}{g_{m6}}\left(\frac{C_C + C_L}{C_C}\right) \tag{4.11}$$

$$g_{m6} = 10.96 \times 10^{-6} \mu A/V \tag{4.12}$$

$$R = \frac{1}{10.96 \times 10^{-6}}\left(\frac{2.2pF + 10pF}{2.2pF}\right) \tag{4.13}$$

$$R = 505.97k\Omega \tag{4.14}$$

$$\left(\frac{W}{L}\right)_8 = \frac{0.310\mu m}{10\mu m} \tag{4.15}$$

Using gm/I_D methodology one can calculate sizes of transistors as given in Table 4.1

TABLE 4.1

SIZES AND OPERATING REGION OF TRANSISTORS

TRANSISTOR	**SIZE**	**TYPE**	**REGION**
M1,2	43.78/2	NMOS	SUBTHRESSHOLD
M5	87.57/2	NMOS	SUBTHRESSHOLD
M7	167/2	NMOS	SUBTHRESSHOLD
M3,4	2.36/2	PMOS	SATURATION
M6	9.34/2	PMOS	SATURATION
M8	0.310/10	PMOS	LINEAR
C_C	2.2pF	COMPENSATION CAPACITOR	
C_L	10pF	LOAD CAPACITOR	

4.2 SIMULATION RESULTS

Simulation methods and simulation results for gain, bandwidth, phase margin, ICMR, CMRR, PSRR, transient response etc at tt corner are shown in this section.

4.2.1 AC ANALYSIS

The AC analysis of operational amplifier is done by following circuit setup as shown in figure 4.6 and simulation results for AC analysis for gain and phase plot vs frequency is shown in figure 4.7

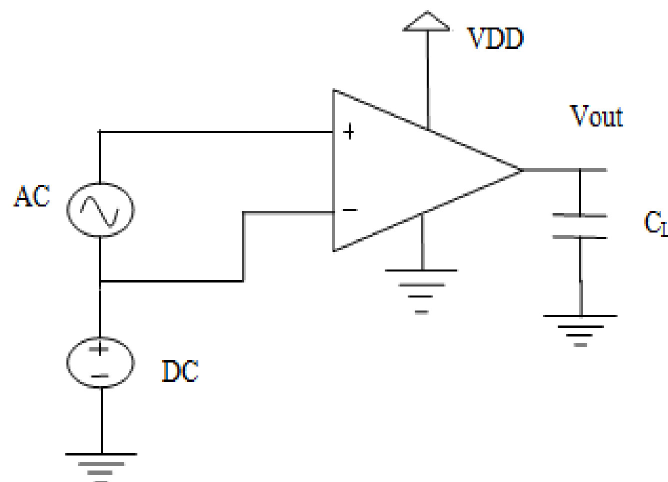

Figure 4.6 Setup for AC analysis

With C_C = 2.2pF, -3db is 43.23Hz and phase margin is 69.47deg. So, C_C reduces to .9pF by trying number of iterations. It also compensate pole and zero, previously which is not compensated. From figure 4.7, designed opamp has DC gain is 76.97db, UGB is 489.9 kHz, -3db is 102.8Hz and Phase margin is 56.09 degree.

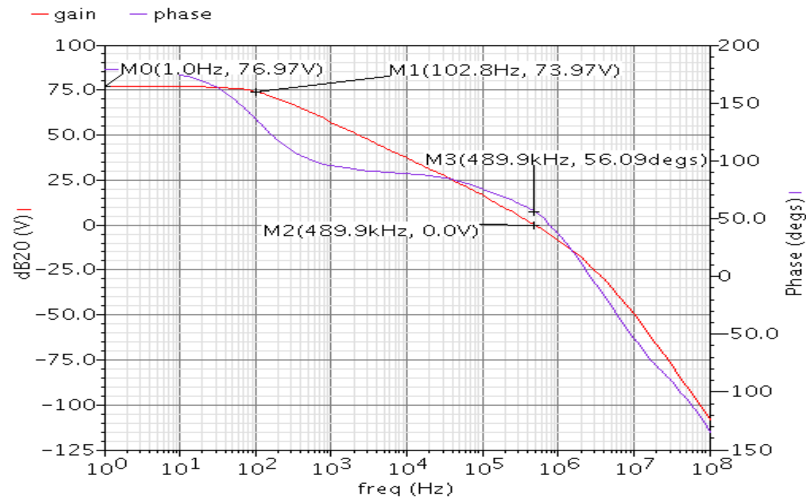

Figure 4.7 Gain and phase plot at tt corner

4.2.2 CMRR MEASUREMENT

The circuit setup for CMRR analysis is shown in figure 4.8 and response is shown in figure 4.9 and the measure CMRR is 79.11db as shown in figure 4.9.

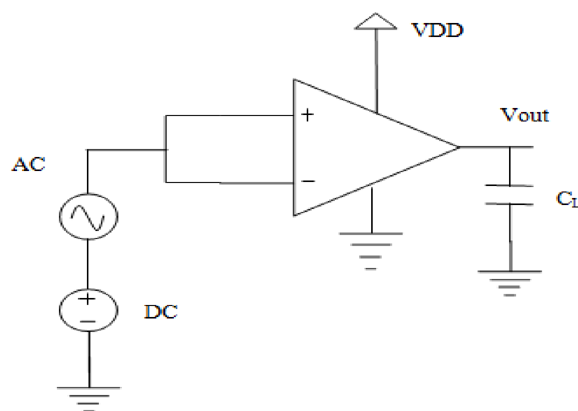

Figure 4.8 Setup for CMRR measurement

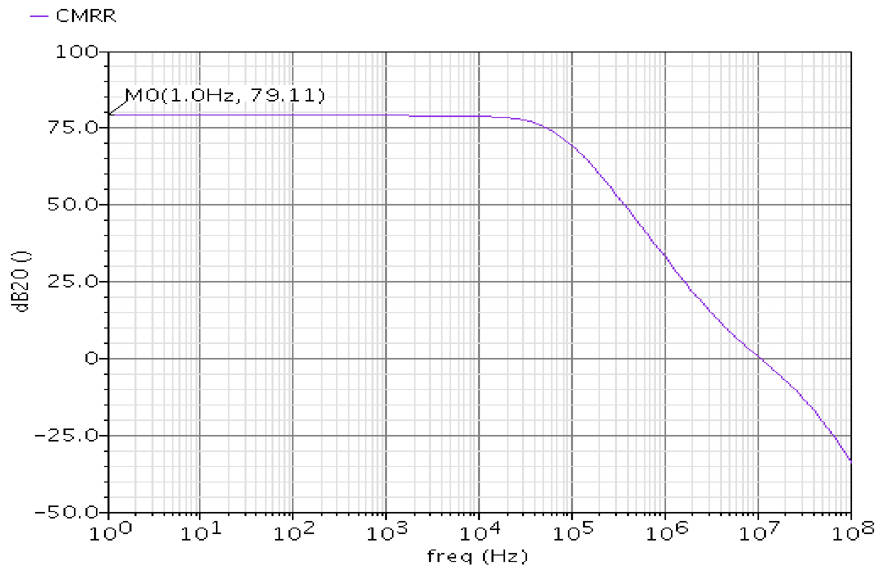

Figure 4.9 Common mode rejection ratio (CMRR)

4.2.3 PSRR MEASUREMENT

For the measurement of PSRR, opamp is connected in unity gain feedback, a DC bias is connected to input and AC signal at VDD terminal for PSRR measurement. Setup for PSRR measurement is shown in figure 4.10 and PSRR response in figure 4.11.

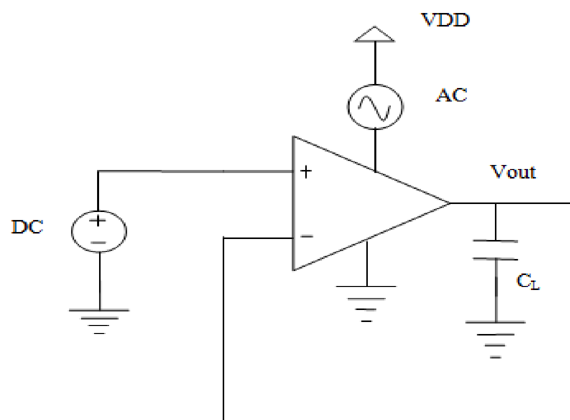

Figure 4.10 Setup for PSRR measurement

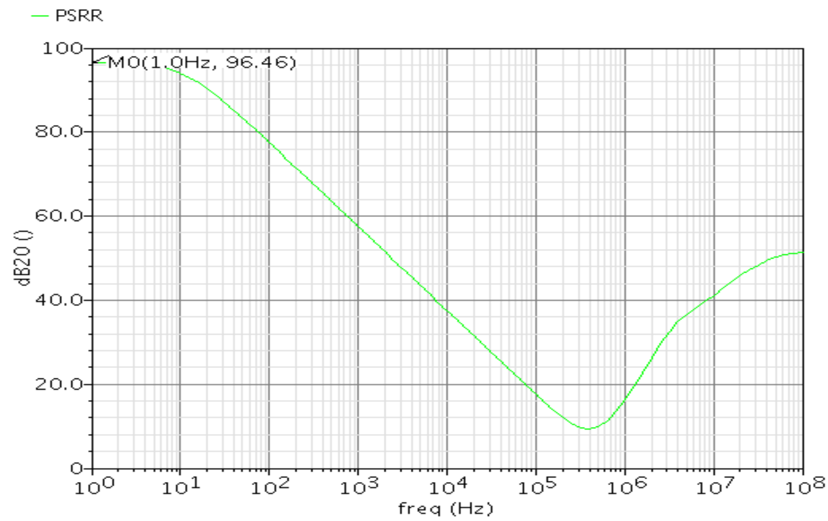

Figure 4.11 power supply rejection ratio (PSRR)

The above PSRR response shown in figure 4.11 is 96.46db.

4.2.4 ICMR MEASUREMENT

For ICMR measurement apply variable DC voltage at input of opamp in unity gain configuration as shown in figure 4.12 and its response is shown in figure 4.13.

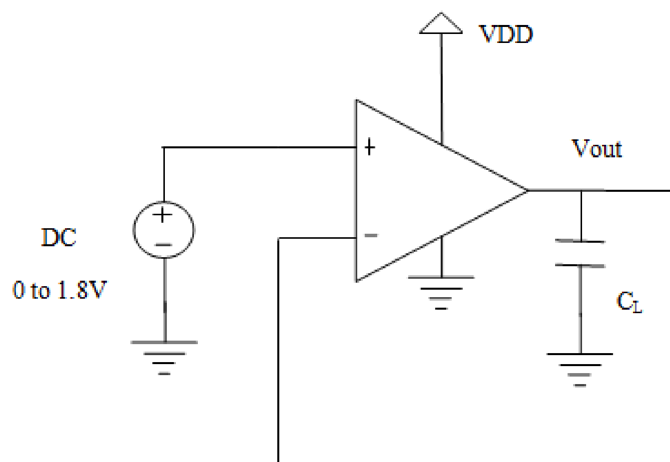

Figure 4.12 Setup for ICMR measurement

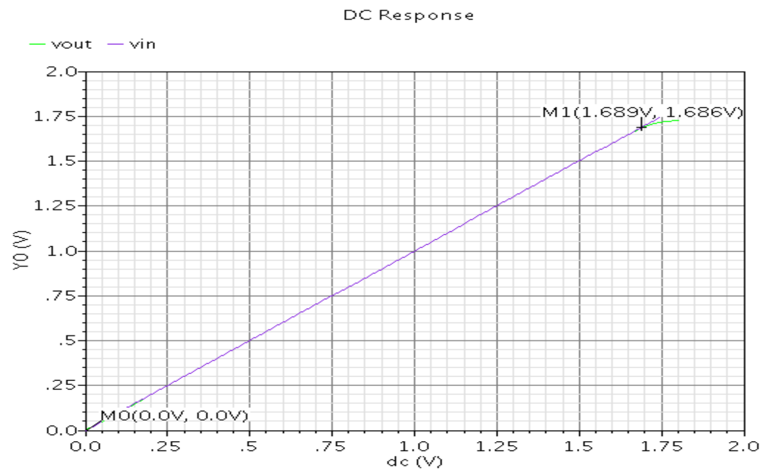

Figure 4.13 Input common mode range (ICMR)

From above plot shown in figure 4.13 ICMR(max) is 1.689 and ICMR(min) is 0V.

4.2.5 SLEW RATE MEASUREMENT

The following figure 4.14 shows the setup for slew rate measurement.

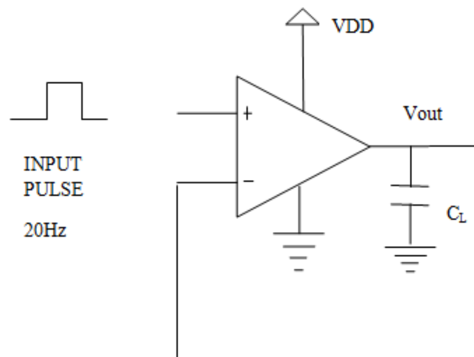

Figure 4.14 Setup for slew rate measurement

From above circuit setup for slew rate measurement, positive slew rate is measured as 338.941kV/s and negative slew rate is measured as 50.07kV/s.

4.2.6 TRANSIENT ANALYSIS

Setup for transient analysis is shown in figure 4.15 and output transient response shown in figure 4.16. A sin wave is applied with 240 μ V peak to peak is applied as input.

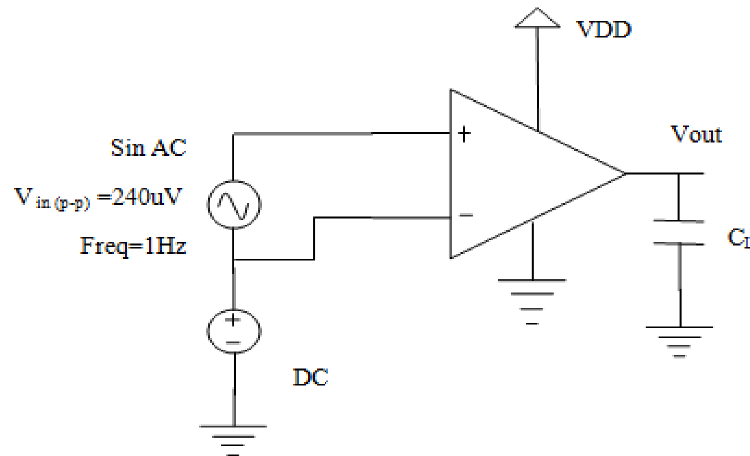

Figure 4.15 Setup for transient analysis

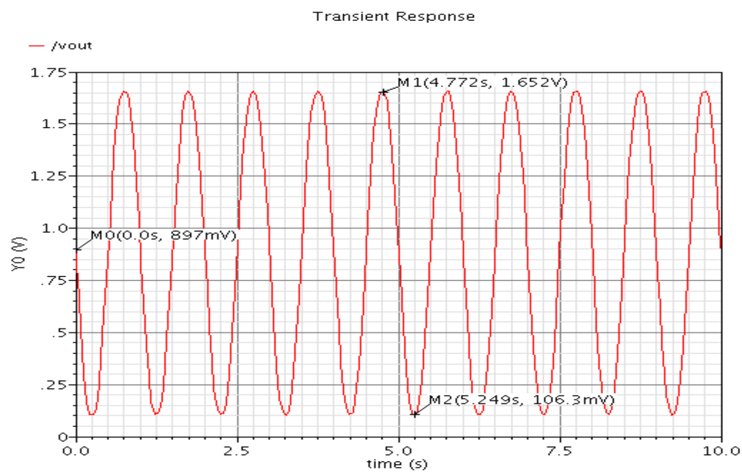

Figure 4.16 Output transient Response

In above figure 4.16, $V_{out(p-p)}$ = 1.5457 and $V_{in(p-p)}$ = 240 μ V, thus

$$Gain = \frac{1.5457}{240\mu} = 6440.41667 = 76.178db$$

Following table 4.2 is showing comparison between target specifications and obtained simulated results.

TABLE 4.2

COMPARISON BETWEEN OBTAINED RESULTS

AND

TARGET SPECIFICATIONS

PARAMETER	**UNITS**	**TARGET SPECIFICATIONS**	**OBTAINED RESULTS**
A_O	db	>70	76.97
-3DB	Hz	>100	102.8
UGB	kHz	>250	489.9
PHASE MARGIN	Degree	60	56.09
POWER DISSIPATION	μW	<5	1.516
CMRR	db	>85	79.11
PSRR	db	>90	96.46
ICMR(MAX)	V	>1.3	1.689
ICMR(MIN)	V	<0.2	0
SR+	kV/s	>200	338.941
SR-	kV/s	>200	50.076

In above comparison it can be seen that obtained CMRR and negative slew rate is not meeting to target specifications.

4.2.7 EFFECT OF PROCESS CORNERS

In table 4.3 effect of process corners SS, FF, SF, FS are shown and compared with TT corner are shown.

TABLE 4.3

EFFECT OF PROCESS CORNERS

PARAMETER	UNITS	TT	SS	FF	SF	FS
A_O	db	76.97	77.88	75.63	77.56	76.18
-3DB	Hz	102.8	40.43	258.1	63.7	163.5
UGB	kHz	489.9	155.2	1181	228	835.8
PHASE MARGIN	Degree	56.09	45.41	46.11	44.85	48.49
POWER DISSIPATION	μW	1.516	.646	3.42	.956	2.32
CMRR	db	79.11	80.16	77.65	79.73	78.35
PSRR	db	96.46	97.46	95.01	96.41	96.4
ICMR(MAX)	V	1.689	1.71	1.675	1.725	1.676
ICMR(MIN)	V	0	0	0	0	0

There are some parameters which are not according to target specifications. Also during process corner analysis design is fails to obtain target specifications. During process corner simulation when NMOS is slow, -3db frequency UGB degrades with large amount. So, there is need to increase bandwidth and need to change compensation technique.

In this two stage opamp the results like -3db frequency, UGB, phase margin does not meet required target specifications during process corner simulation.

When NMOS is slow or during SS and SF process corner simulation -3db and UGB decrEeses. This is because all NMOS transistors in subthresshold region, M5 and M7 current sources are in subthresshold. So, current is affect a lot during process corner simulation. So, when NMOS is slow current in circuit decreases. Now UGB is given as:

$UGB = \frac{g_{m1}}{2\Pi C_C}$ and $g_{m1} = \frac{I_{D1}}{nU_T}$, as current decreases , transconductance decreases and hence UGB decreases . In case of weak inversion current depends exponentially on threshold voltage, so, small change in V_{TH} produce large change in current. So, during process corners SS and SF current change is large as NMOS are in weak inversion.

Now gain depends upon $\frac{g_{m1}}{I_{D1}}$ and $\frac{g_{m6}}{I_{D6}}$.

$$\frac{g_{m1}}{I_{D1}} = \frac{1}{nU_T} \tag{4.16}$$

This is constant. So, it does not affect the gain. Now, M6 in saturation. So, $g_{m6} \propto \sqrt{I_{D6}}$

Now current in M7 decreases with large amount as it is in subthresshold. So, Say current in M6 become half during process corner SS

$$I_{D6}^{'} = \frac{I_{D6}}{2} \tag{4.17}$$

$$\sqrt{I_{D6}^{'}} = \sqrt{\frac{I_{D6}}{2}} \tag{4.18}$$

$$g_{m6}^{'} = \frac{g_{m6}}{\sqrt{2}} \tag{4.19}$$

Dividing above transconductance equation by current equation, we get

$$\frac{g_{m6}^{'}}{I_{D6}^{'}} = \frac{\frac{g_{m6}}{\sqrt{2}}}{\frac{I_{D6}}{2}} \tag{4.20}$$

$$\frac{g'_{m6}}{I'_{D6}} = \sqrt{2}\frac{g_{m6}}{I_{D6}} \tag{4.21}$$

So, $\frac{g_{m6}}{I_{D6}}$ increases so gain increases during ss corner.

-3db depends on r_{o2}, r_{o4}, r_{o6} and r_{o7}

$$r_o = \frac{1}{\lambda I_D} \tag{4.22}$$

So, I_D is decreasing and hence r_o increasing and hence -3db is decreasing

In subthresshold region , current follow exponential law i.e.

$$I_D \propto e^{\frac{V_{GS}-V_{TH}}{nU_T}} \tag{4.23}$$

For slow NMOS V_{TH} is large as compared to TT corner, so the term $e^{\frac{V_{GS}-V_{TH}}{nU_T}}$ decreases, so the I_D decreases exponentially. So, in subthresshold region, current decreases exponentially ie there is large change in current as compared to mosfet in saturation region(in saturation region current is follow square law) . So, during process corner simulation if transistors are in subthresshold region there is large change in current which affect power dissipation, UGB and -3db frequency.

Effect of threshold voltage when NMOS is slow:

When NMOS is slow, threshold voltage of NMOS is taken as 0.3222V but for typical value of threshold voltage is 0.3075V.For V_{GS}=0.2V, one can calculate relative change in current as compared to typical NMOS. Current in M1,2,3 become 61.7% when NMOS is slow i.e. 123.4nA as compared to current when NMOS is typical. So, UGB should be 61.7% of calculated for typical NMOS. So, UGB become 293.11 kHz when NMOS is slow, so, UGB decreases. Now experimentally observed value of UGB during SS and SF corner is 155.2 kHz and 228 kHz respectively. Here only effect of threshold voltage is shown.

CHAPTER 5

DESIGN OF OPAMP USING CURRENT BUFFER COMPENSATION TECHNIQUE

5.1 INTRODUCTION

In previous chapter two stage opamp is designed with RC compensation technique. In that opamp during process corner analysis, when NMOS is slow bandwidth degrades with large extent so it is required to increase bandwidth. So, here for overcoming the drawbacks of RC compensation opamp current buffer compensation technique is used. Current buffer compensation technique has higher bandwidth and it is area efficient as compared to RC compensated technique. Another modification is that only input stage differential pair nmos transistors are put in subthresshold region not all NMOS transistor as in RC compensated opamp and other current source nmos transistors M5 and M7 are not put in subthresshold region. This is because current in subthresshold follows exponential law so during process variation whenever NMOS is slow current decreases with large amount when NMOS in subthresshold region than as compared to NMOS in saturation region as it follows square law. So process variations affect mosfet in subthresshold region as compared to mosfet in saturation because in subthresshold region current follows exponential law so small changes affect a lot as compared to mosfet in saturation as it follows square law.

5.2 DESIGN TWO STAGE OPAMP USING CURRENT BUFFER COMPENSATION TECHNIQUE

This current buffer compensation technique [17] is based on removing the feed forward path from the output of first stage to the output of opamp. Schematic for two stage opamp with compensation block is shown in figure 4.1. Where, CB is compensation block. In this technique Compensation block is current buffer as shown in figure 5.1

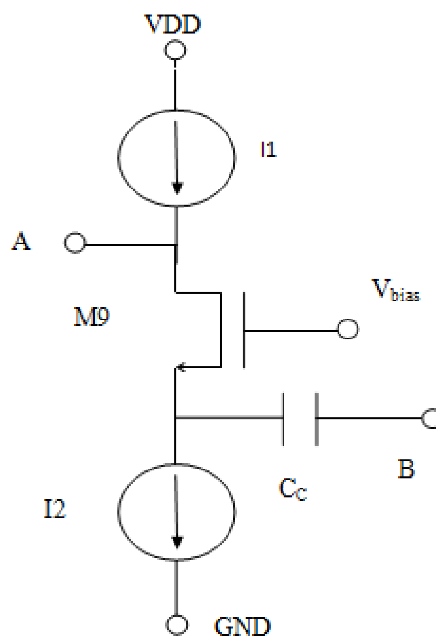

Figure 5.1 Current buffer compensation block

Frequency response of two stage opamp with common gate current buffer compensation technique as shown in figure 5.2 is given as

$$A(s) = \frac{g_{m1} R_1 g_{m6} R_2 \left(1 + \frac{C_C}{g_{m9}} s\right)}{\left(1 + C_C R_1 g_{m6} R_2\right)\left[1 + \left(\frac{C_{o1}}{g_{m6}} + \frac{C_{o1} C_L}{C_C g_{m6}}\right) s + \frac{C_{o1} C_L}{g_{m1} g_{m6}} s^2\right]} \tag{5.1}$$

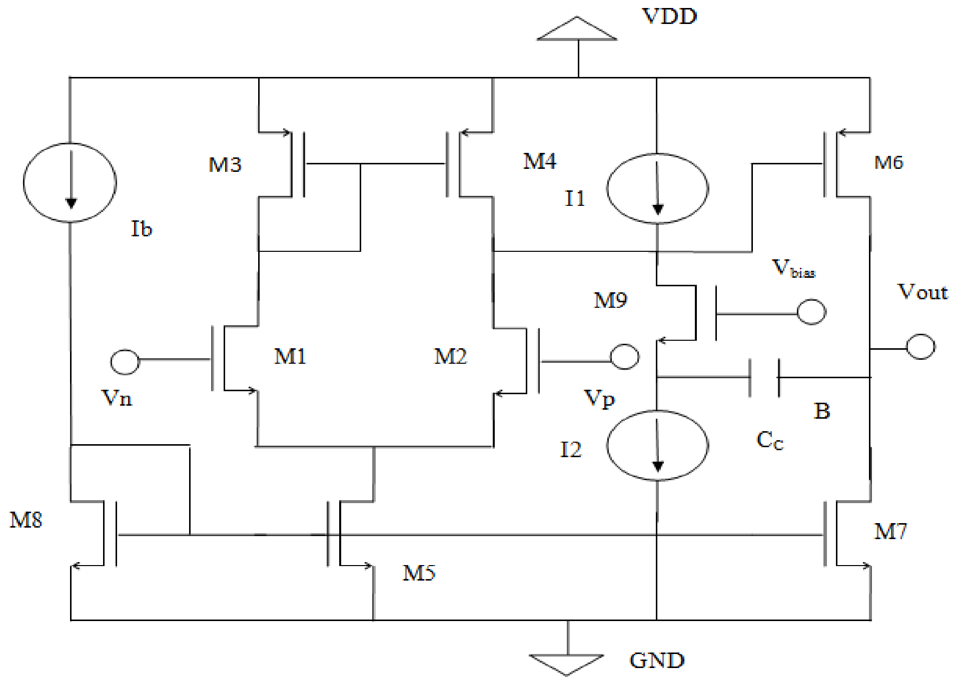

Figure 5.2 Schematic of two stage opamp with common gate current buffer compensation technique

Two poles and zero of this opamp is given as

$$P_1 = \frac{1}{g_{m6} R_2 C_C R_1} \tag{5.2}$$

$$P_2 = \frac{g_{m6} C_C}{C_{o1}(C_C + C_L)} \tag{5.3}$$

$$Z = \frac{g_{m9}}{C_C} \tag{5.4}$$

Unity gain bandwidth is given by

$$UGB = \frac{g_{m1}}{C_C} \tag{5.5}$$

Dividing equation (5.3) and (5.5), we get

$$\frac{P_2}{UGB} = \frac{g_{m6}}{g_{m1}} \frac{C_C}{C_{o1}} \frac{C_C}{(C_C + C_L)} \tag{5.6}$$

$\frac{C_C}{C_{o1}}$ is called as improvement factor, greater is this ratio greater is phase margin. C_{o1} can be reduced by careful layout and design of first stage.

Current can be calculated from power dissipation.Power dissipation is given as

$$PD = V_{DD} I \tag{5.7}$$

Only input transistors are biased in subthresshold region this is explained above. Current equation of MOSFET in subthreeshold region [14] is given as

$$I_D = I_o \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{nU_T}} \left(1 - e^{-\frac{V_{DS}}{nU_T}}\right) \tag{5.8}$$

Where $I_o = 2.n.\mu.C_{ox} U_T^2 e \frac{V_{THo}}{nU_T} e \frac{(n-1)V_{BS}}{nU_T}$ (5.9)

U_T is thermal voltage which is 25.9mV,

V_{TH} is threshold voltage and

n is subthresshold parameter

For MOSFET to be in saturation region when it is in subthresshold, V_{DS}>3U_T. it reduces subthresshold current equation to

$$I_D = I_o \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{nU_T}} \tag{5.10}$$

Procedure for extracting parameters of MOS in subthresshold regions is given in chapter 3 and these are n=1.172, I_o=263.5nA, $\lambda_{n,sub}$ = 0.28, for NMOS transistor in subthresshold region , λ_n =0.13 for strong inversion and λ_p = 0.0215, for PMOS transistor

Gain bandwidth optimization [18] can be achieved by setting

$$g_{m9} = 2g_{m1,2} \tag{5.11}$$

and

$$C_C = \sqrt{\frac{g_{m1,2}}{g_{m6}}\left(\frac{2K-1}{2+K}+\frac{1}{2}\right)C_L C_{01}} \tag{5.12}$$

Where

$K = \tan\phi$ (ϕ is phase margin) and

C_{o1} = 48.1fF is the Capacitance at the output of first stage. It is given as

$$C_{o1} = C_{gd2} + C_{bd2} + C_{gd4} + C_{bd4} + C_{gd9} + C_{bd9} + C_{gd13} + C_{bd13} + C_{gs6} + C_{gd6} \tag{5.13}$$

Capacitances [8] given as:

In subthresshold region,

$$\left.\begin{aligned} C_{gb} &= C_{ox}.W.L + CGBO.W \\ C_{gs} &= CGSO.W \\ C_{gd} &= CGDO.W \end{aligned}\right\} \tag{5.14}$$

In saturation region,

$$\left.\begin{aligned} C_{gb} &= CGBO.W \\ C_{gs} &= CGSO.W + \left(2/3\right)C_{ox}.W.L \\ C_{gd} &= CGDO.W \end{aligned}\right\} \tag{5.15}$$

C_{bd} is given as:

$$C_{bd} = \frac{CJ.AD}{\left[1-\left(\frac{V_{bd}}{PB}\right)\right]^{MJ}} + \frac{CJSW.PD}{\left[1-\left(\frac{V_{bd}}{PB}\right)\right]^{MJSW}} \tag{5.16}$$

Where AD area of source/drain and PD perimeter of drain contact.

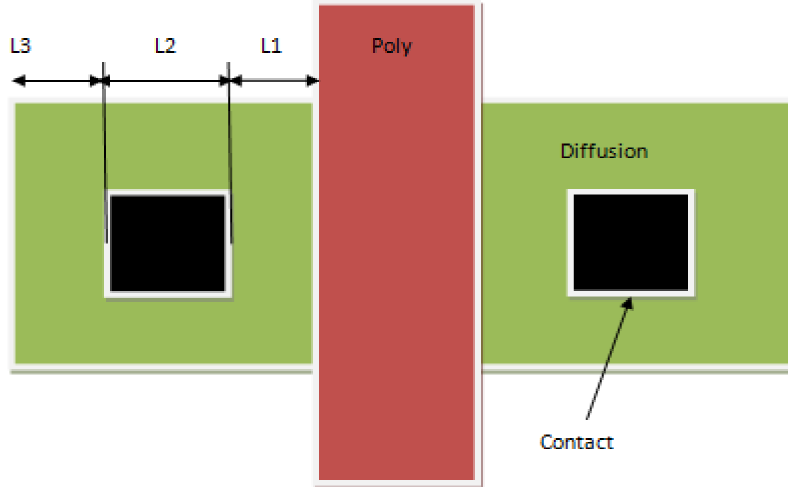

Figure 5.3 For MOS transistor area and perimeter calculation

Where S = L1 + L2 + L3, AD(source/drain area)=S×W, PD(perimeter of source/drain)=2 ×(S+W) and W is the width of transistor.

ICMR is used to calculate the size of M3 and M4. From ICMR $V_{gs3,4}$ can be calculated also from g_{m6}, V_{gs6} can be calculated.

$$ICMR(\max) = V_{DD} - V_{SG3} + V_{TH1} \tag{5.17}$$

As M1,2 in subthresshold and M5 in saturation,

$$ICMR(\min) = V_{dsat5} \tag{5.18}$$

For equal positive and negative slew rate I1 =I2 [19] as shown in figure 5.1. Also I2 > I_{D1} i.e. current following in current buffer must be greater than current in input transistors.

$$SR = \frac{I_{D5}}{C_C} \tag{5.19}$$

In order to improve CMRR, accurate matching must be guranted by both a proper layout design and symmetrical bias conditions. This means the same drain-source voltages.

$$V_{GS3} = V_{DS4} = V_{GS6} \tag{5.20}$$

From above design procedure sizes of transistors can be calculated as given in table 5.1. These values of transistors are calculated for gain = 80db, UGB = 500 kHz, PD<5 μW, phase margin is 65° for achieving required target specifications

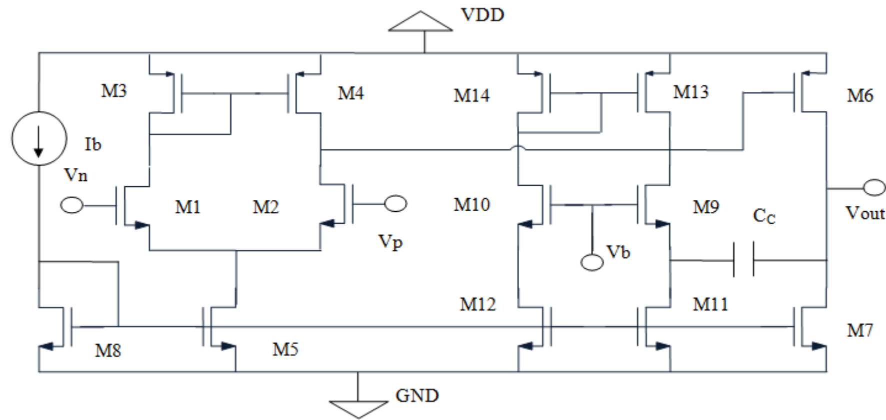

Figure 5.4 Schematic of two stage opamp with current buffer compensation technique

TABLE 5.1

SIZES AND REGIONS OF TRANSISTORS FOR FIGURE 5.4

TRANSISTOR	SIZE	TYPE	REGION
M1,2	18.2/2	NMOS	SUBTHRESSHOLD
M5,8	.336/2	NMOS	SATURATION
M7	1.68/2	NMOS	SATURATION
M9,10	.388/2	NMOS	SATURATION
M11,12	.674/2	NMOS	SATURATION
M3,4	.252/2	PMOS	SATURATION
M6	2.526/2	PMOS	SATURATION
M13,14	1/2	PMOS	SATURATION
C_C	0.390pF	COMPENSATION CAPACITOR	
C_L	10pF	LOAD CAPACITOR	

5.3 SIMULATION RESULTS

Simulation methods and simulation results for gain, bandwidth, phase margin, ICMR, CMRR, PSRR, transient response etc at TT corner are shown in this section.

5.3.1 AC ANALYSIS

The AC analysis of operational amplifier is done by following circuit setup as shown in figure 4.6 and simulation results for AC analysis for gain and phase plot vs frequency is shown in figure 5.5

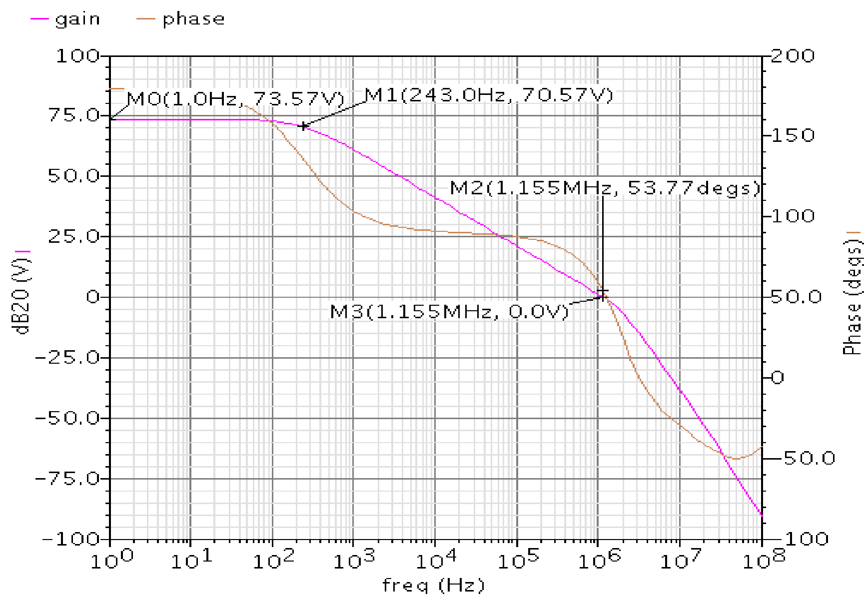

Figure 5.5 Gain and phase plot with C_C =0 .390pF

From figure 5.5, designed opamp has gain = 73.57db, UGB = 1.155MHz, phase margin is 53.77̊. But with this compensation capacitor phase margin is low so it is requires to adjust

compensation capacitor because $\frac{C_C}{C_{o1}}$ is improvement factor and as $\frac{C_C}{C_{o1}}$ increases phase margin increases. So, after iteration value of capacitor is given as 0.490 pF for 65° degree for which calculation is to be done. AC response with 0.490pF compensation capacitor is shown in figure5.6. This shows improvement in phase margin but little degradation in bandwidth.

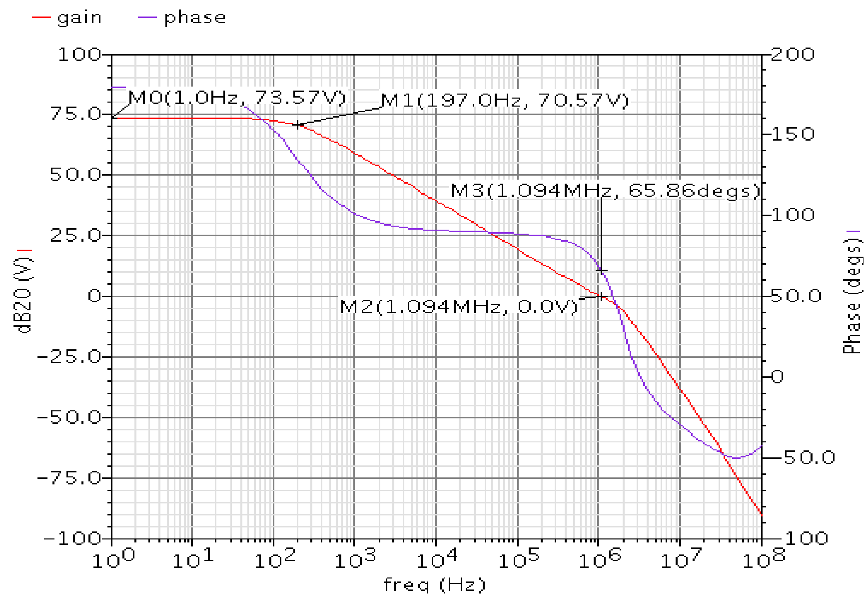

Figure 5.6 Gain and phase plot with C_C = 0.490pF

Now from figure 5.6, designed opamp has Gain = 73.57db, -3db = 197Hz, UGB = 1.094MHz and Phase margin = 65.86°

5.3.2 CMRR MEASUREMENT

The circuit setup for CMRR analysis is shown in figure 4.8 and response is shown in figure 5.7 and the measure CMRR is 147.9db as shown in figure 5.7.

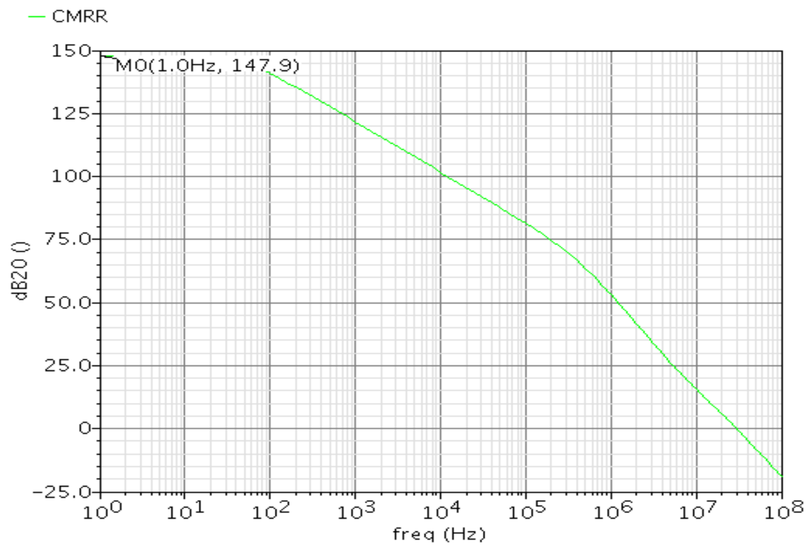

Figure 5.7 Common mode rejection ratio(CMRR)

5.3.3 PSRR MEASUREMENT

For the measurement of PSRR, opamp is connected in unity gain feedback, a DC bias is connected to input and AC signal at VDD terminal for PSRR measurement. Setup for PSRR measurement is shown in figure 4.10 and PSRR response in figure 5.8

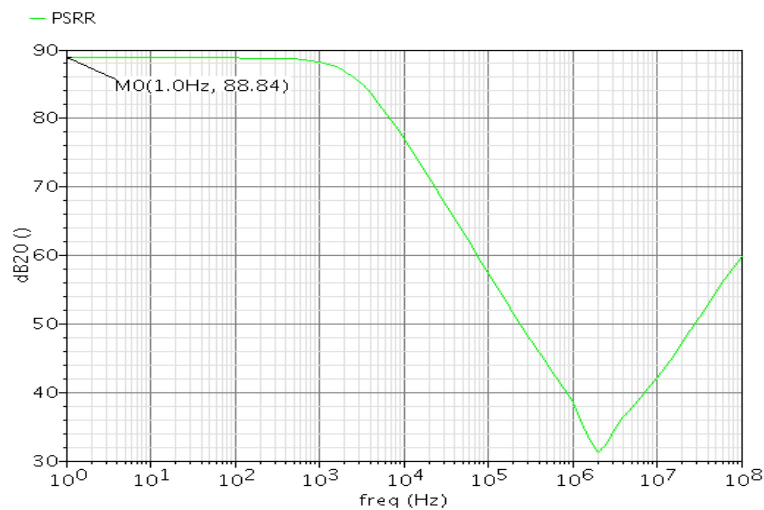

Figure 5.8 Power supply rejection ratio (PSRR)

Above figure 5.8 shows PSRR = 88.84db

5.3.4 ICMR MEASUREMENT

For ICMR measurement apply variable DC voltage at input of opamp in unity gain configuration as shown in figure 4.12 and its response is shown in figure 5.9.

From ICMR plot shown in figure 5.9, ICMR(max) is 1.495 and ICMR(min) is 0.142V.

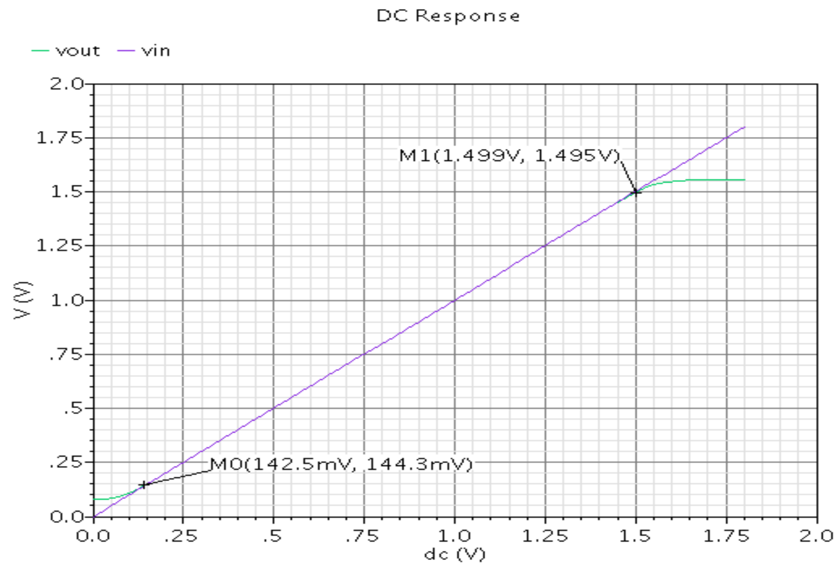

Figure 5.9 Input common mode range (ICMR)

5.3.5 TRANSIENT ANALYSIS

Setup for transient analysis is shown in figure 4.15 and output transient response shown in figure 5.10. A sin wave is applied with 240 μ V peak to peak is applied as input.

In figure 5.10, $V_{out(p-p)}$ = 1.1803 and $V_{in(p-p)}$ = 240 μ V, thus

$$Gain = \frac{1.1803}{240\mu} = 4917.9166 = 73.83db$$

Ac analysis in figure 5.6 shows that gain =73.57db which is approximately equal to gain calculated by transient analysis which is 73.83db.

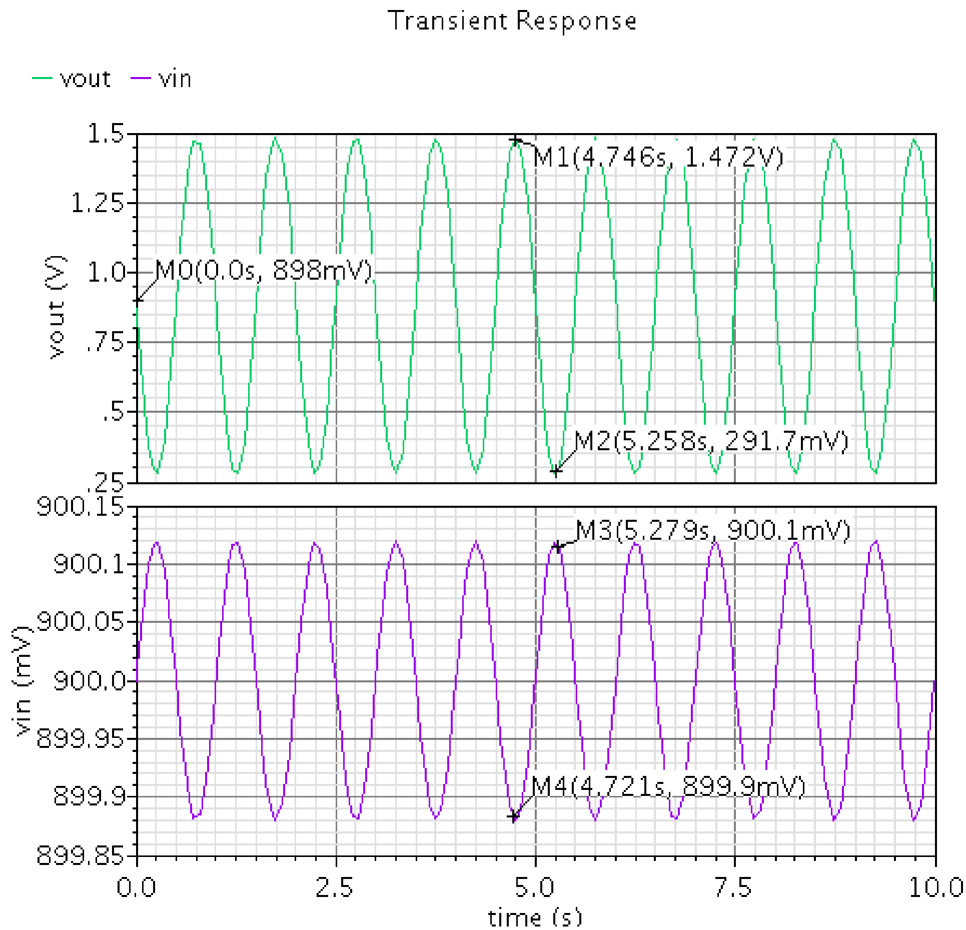

Figure 5.10 Input and Output transient Response

5.3.6 SLEW RATE MEASUREMENT

From the circuit setup for slew rate measurement shown in figure 4.14, positive slew rate is measured as 399.2kV/s and negative slew rate is measured as 107.342kV/s.

5.3.7 COMPARISON

In following table 5.2, comparison between target specifications and obtained results is shown. In this designed opamp in figure 5.4.

TABLE 5.2

COMPARISON BETWEEN OBTAINED RESULTS

AND TARGET SPECIFICATION

PARAMETER	UNITS	TARGET SPECIFICATIONS	SIMULATED RESULTS
A_O	db	70	73.57
-3DB	Hz	100	197
UGB	kHz	250	1094
PHASE MARGIN	Degree	60	65.86
POWER DISSIPATION	μW	5	4.35
CMRR	db	85	147.9
PSRR	db	90	88.84
ICMR(MAX)	V	0.2	1.49
ICMR(MIN)	V	1.3	0.142
SR+	kV/s	200	399.2
SR-	kV/s	200	107.342

All specifications are achieved except PSRR which is little lesser than target specification and negative slew rate is less.

In table 5.3, there is comparison between RC compensated opamp shown in figure 4.1 and current buffer compensated opamp shown in figure 5.4.

TABLE 5.3

COMPARISON BETWEEN CURRENT BUFFER COMPENSATED OPAMP AND RC COMPENSATED OPAMP

PARAMETER	**UNITS**	**CURRENT BUFFER COMPENSATED OPAMP**	**RC COMPENSATED OPAMP**
A_O	db	73.57	76.97
-3DB	Hz	197	102.8
UGB	kHz	1094	489.9
PHASE MARGIN	Degree	65.86	56.09
POWER DISSIPATION	μW	4.35	1.516
CMRR	db	147.9	79.11
PSRR	db	88.84	96.46
ICMR(MAX)	V	1.49	1.689
ICMR(MIN)	V	0.142	0
SR+	kV/s	399.2	338.941
SR-	kV/s	107.342	50.076

Current buffer compensated opamp there is improvement of gain, bandwidth, phase margin CMRR, slew rate but power dissipation increases and PSRR decreases.

5.4 EFFECT OF PROCESS CORNERS

In table 5.4 effect of process corners SS, FF, SF, FS are shown and compared with TT corner are shown.

TABLE 5.4

EFFECT OF PROCESS CORNER

PARAMETER	**UNITS**	**TT**	**SS**	**FF**	**SF**	**FS**
A_O	db	73.57	70.65	72.16	45.86	44.47
-3DB	Hz	197	260.4	223.5	4.354K	5.024K
UGB	kHz	1094	1047	1093	985.3	907.2K
PHASE MARGIN	Degree	65.86	72.87	63.75	71.76	63.06
POWER DISSIPATION	μW	4.35	5.64	3.5	4.48	4
CMRR	db	147.9	85.1	89.75	87.9	88.93
PSRR	db	88.84	85.51	91.5	85.74	95.92
ICMR(MAX)	V	1.49	1.42	1.54	1.51	1.48
ICMR(MIN)	V	.142	.165	.108	.144	.142

Some parameter specially gain decreases during SF and FS process corner analysis. One can observe large improvement in CMRR phase margin bandwidth as compared to RC compensated opamp shown in figure 4.1. But still does not fulfill all requirements during all process corners. So, it needs some improvement.

5.5 MANAGEING PROCESS VARIATIONS

Moore's law driven technology scaling has improved VLSI performance by five orders of magnitude in the last four decades. As the advanced technologies continue the pursuit of Moor's law, a variety of challenges will need to overcome. One of these challenges is management of process variation. In recent years process variation emerges as new challenge associated with advanced CMOS technologies, process variation has been a continuing theme throughout the history of semiconductor process engineering. [20]

5.5.1 CRITICAL SOURCES OF PROCESS VARIATIONS

Critical sources of variation are random dopant fluctuation, line edge roughness, line width roughness, oxide thichness, fixed charge, defects, traps etc.

RANDOM DOPANT FLUCTUATION (RDF)

In sub-micron CMOS technologies, MOS threshold voltage variation due to random fluctuations in the number and location of dopant atoms is an increasingly significant effect.

As the number of dopant atoms in the channel decreases with scaled dimensions,the impact of variation associated with the atom increases. Figure 5.11 shows the decreasing average number of dopant atoms in the channel as a function of technology node.

RDF is assumed to be major contributor to device mismatch of identical adjacent devices and is represented by stolk's formulation given below in equation (5.20).

$$\sigma V_{Tran} = \left(\frac{\sqrt[4]{4q^3\varepsilon_{si}\phi_B}}{2}\right).\frac{T_{ox}}{\varepsilon_{ox}}.\left(\frac{\sqrt[4]{N}}{\sqrt{W_{eff}.L_{eff}}}\right) = \frac{1}{\sqrt{2}}\left(\frac{C_2}{\sqrt{W_{eff}.L_{eff}}}\right) \tag{5.21}$$

From equation (5.20), matching improves with decrease in

(i) Channel doping (N),

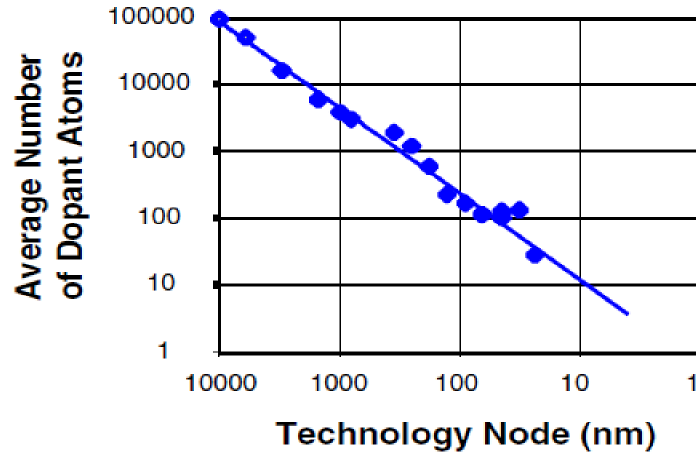

Figure 5.11 Average number of dopant atom in the channel as a function of technology node

(ii) Gate oxide thickness (T_{ox}) and

(iii) With increase in device area. With increase of area variation decreases shown in figure 5.12.

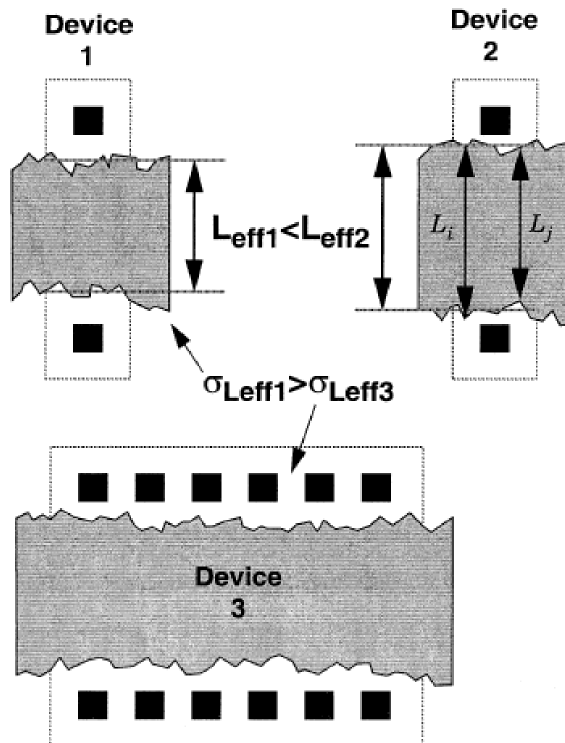

Figure 5.12 Comparison of variation between devices with different dimensions

LINE WIDTH AND LINE EDGE ROUGHNESS (LER AND LWR)

The primary concern with LER/LWR is variations in poly-gate patterning. For poly-gate patterning, LER and LWR are associated with increase in subthresshold current as well as degradation in threshold voltage.

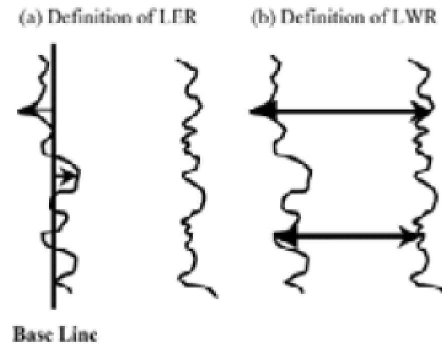

Figure 5.13 LER/LWR definitions

Other effects like gate oxide thickness, fixed charge, defects and traps affect threshold voltage (i.e. fluctuation in threshold voltage). Fixed charge, defects and traps also affect the mobility i.e. degradation in mobility. In addition to fundamental variation mechanism of random dopant fluctuation , there are number of variation sources associated with the physical implant and anneal process. The implant tool conditions are a significant source of transistor variations

5.5.2 PROCESS, DESIGN AND LAYOUT TECHNIQUES TO MITIGATE THE IMPACT OF PROCESS VARIATIONS

There are many techniques to mitigate the impact of process variation. These techniques can be characterized as a pure process techniques (i.e. techniques transparent to design), combination process and design techniques (i.e. techniques that exercise tight cooperation between process and design) and pure design technique (i.e. transparent to process). RDF is major contributor to random variation and it is represented by equation (5.20). It shows that matching improves with decrease in channel doping (N) and gate oxide thickness

(T_{ox}) and degrades with decrease in device area. This comes under process migration technique. As with scalling gate oxide thickness reduces suggests a continued improvement in the random variation coefficient (C_2). In combined process-design migration technique, “wide” design topology rather than “tall” design topology. As the wide design improves CD (critical dimension) control and variation by aligning the poly in single direction, eliminating diffusion corners, and relaxing some patterning constraints on other critical layers. In design migration technique variations are minimized through the use of good layout techniques for example, multi finger layout technique.

In this current buffer compensated opamp shown in figure 5.4, process corner simulation is shown in table 5.4. During SF and FS simulation it is observed that gain is decreasing. Now gain depends on g_m/I_D of M6 and experimentally it is also observed that dc biasing voltage of output node of first stage of opamp shown in figure 5.4 is varying during process corner so the g_m/I_D of M6. Hence, the gain is varying. So, this dc bias of output node of first stage must be stable or variation of voltage at this node should be decrease so to achieve results during process variation. So, there are some sensitive nodes in circuits and voltage at these sensitive nodes should be stable during process variations.

Now process variation depends upon length and width or area of device as shown in equation (5.20). this equation shows that with increase of device area variation decreases. So, area of devices connected to output node of first stage or affecting dc bias of this node should increase but keeping same W/L ratio so as to decrease variations. But here capacitance at this output node of first stage affect the performance of opamp as it is connected to the improvement factor of opamp i.e. it will affect $\frac{C_C}{C_{o1}}$ improvement factor as it will increase output capacitane of first stage i.e. C_{o1}. It will degrade UGB, -3db and also phase margin. So, area of devices should increase but keeping target specification in mind.Here, transistors M3, M4, M13, M14, M9, M10 are connected to this node, so there areas are to be increase but keeping same W/L and keeping target specification in mind. So, sizes of transitors modified are given below. For 60 degree phase margin, C_C is also modified to 0.580pF.

$$\left(\frac{W}{L}\right)_{3,4} = \frac{1.25}{10}, \left(\frac{W}{L}\right)_{13,14} = \frac{2.22}{10}, \left(\frac{W}{L}\right)_{9,10} = \frac{0.98}{5} \text{ and } \left(\frac{W}{L}\right)_{11,12} = \frac{3.33}{10}$$

5.6 SIMULATION RESULTS OVER TT CORNER OF OPTIMIZED OPAMP FOR TOLERATING PROCESS VARIATIONS

In this section, simulation results of improved opamp for gain, bandwidth, phase margin, ICMR, CMRR, PSRR etc at TT corner are shown.

5.6.1 AC ANALYSIS

The AC analysis of operational amplifier is done by following circuit setup as shown in figure 4.6 and simulation results for AC analysis for gain and phase plot vs frequency is shown in figure 5.14

From figure 5.14, designed opamp has DC gain is 75.69db, UGB is 756.6 kHz, -3db is 128.9Hz and Phase margin is 60.24 degree.

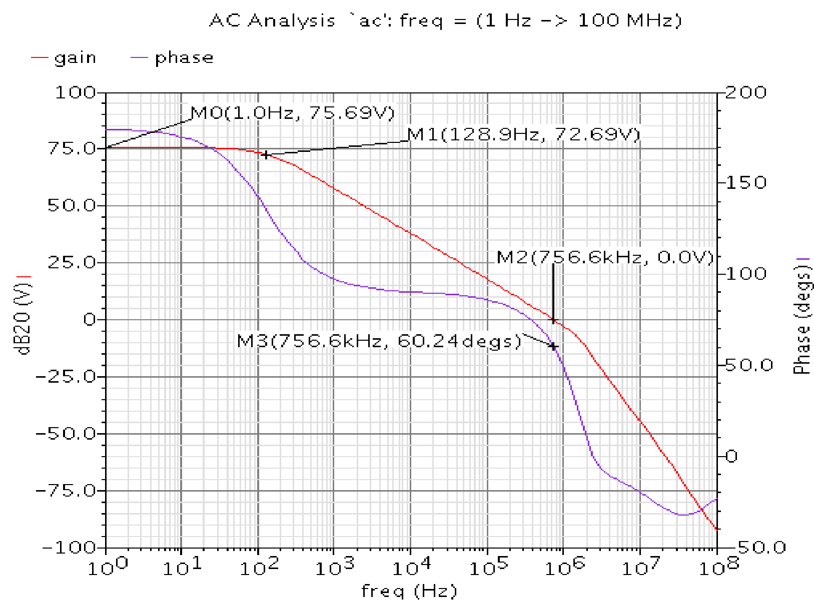

Figure 5.14 Gain and phase plot

5.6.2 CMRR MEASUREMENT

The circuit setup for CMRR analysis is shown in figure 4.8 and response is shown in figure 5.15

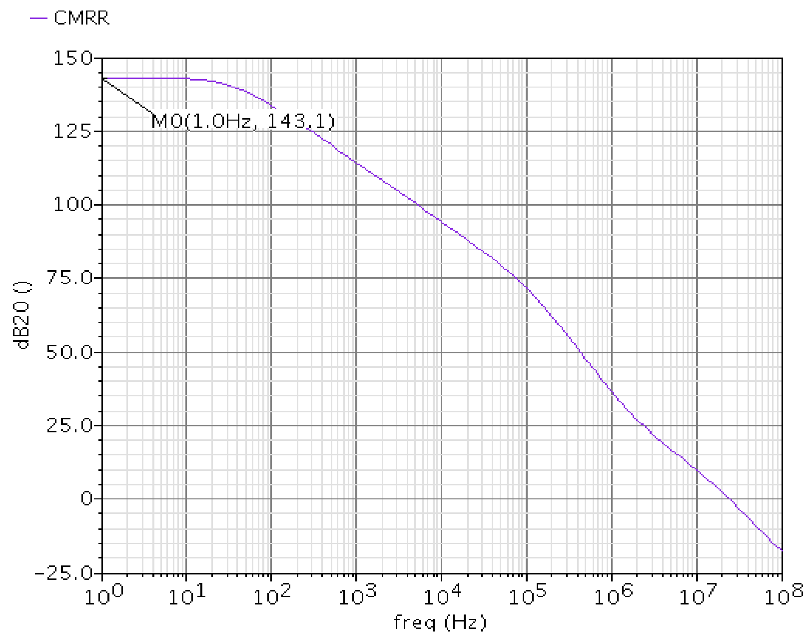

Figure 5.15 Common mode rejection ratio (CMRR)

The measure CMRR is 143.1db as shown in figure 5.15

5.6.3 PSRR MEASUREMENT

For the measurement of PSRR, opamp is connected in unity gain feedback, a DC bias is connected to input and AC signal at VDD terminal for PSRR measurement. Setup for PSRR measurement is shown in figure 4.10 and PSRR response in figure 5.16 and PSRR is 92.29db.

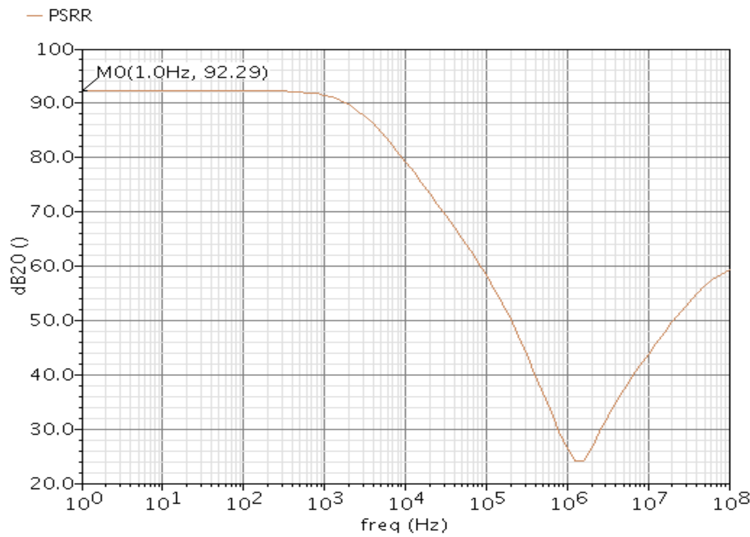

Figure 5.16 Power supply rejection ratio (PSRR)

5.6.4 ICMR MEASUREMENT

For ICMR measurement apply variable DC voltage at input of opamp in unity gain configuration as shown in figure 4.12 and its response is shown in figure 5.17. From this plot shown in figure 5.17 ICMR (max) is 1.51 and ICMR (min) is 0.143V.

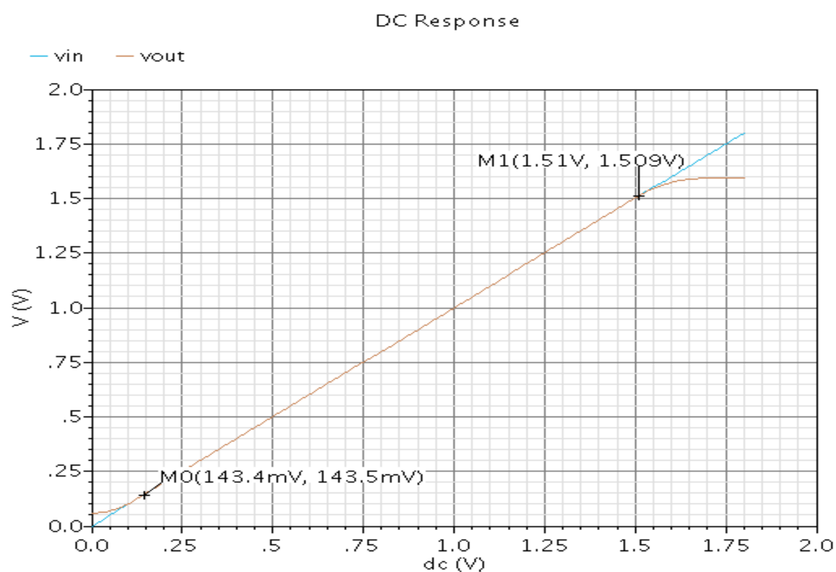

Figure 5.17 Input common mode range (ICMR)

5.6.5 TRANSIENT ANALYSIS

Setup for transient analysis is shown in figure 4.15 and output transient response shown in figure 5.18. A sin wave is applied with 240 μ V peak to peak is applied as input.

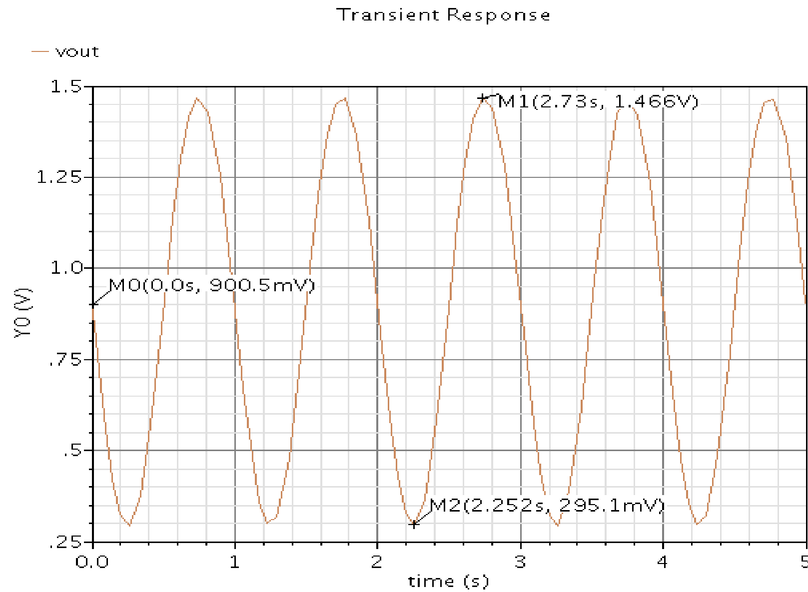

Figure 5.18 Transient Analysis TT corner

In above figure 4.16, $V_{out(p-p)}$ = 1.5457 and $V_{in(p-p)}$ = 240 μ V, thus

$$Gain = \frac{1.1709}{240\mu} = 4878.75 = 73.76db$$

Table 5.5 showing simulated result of optimized opamp for process variations and also comparison with target specifications. From table 5.5 one can observe that all parameters or target specifications are achieved except negative slew rate. Because of optimization for process variation some of parameters degrades because of increase in C_{o1} (output capacitance of first stage) as $\frac{C_C}{C_{o1}}$ (improvement factor) degrades. Basically, UGB, -3db and phase margin degrades but still target specifications are achieved. UGB become 756.6 kHz previously it was 1.094MHz, -3db degrades to 128.9Hz previously it was 197Hz and phase margin degrades to 60.24 degree previously it was 65.86 degree

TABLE 5.5

COMPARISON BETWEEN OBTAINED RESULTS

AND

TARGET SPECIFICATION

PARAMETER	**UNITS**	**TARGET SPECIFICATIONS**	**RESULTS**
A_O	db	70	75.69
UGB	kHz	100	756.6
-3DB	Hz	250	128.9
PHASE MARGIN	Degree	60	60.24
POWER DISSIPATION	μW	5	3.51
CMRR	db	85	143.1
PSRR	db	90	92.29
ICMR(MAX)	V	0.2	1.51
ICMR(MIN)	V	1.3	.143
SR+	kV/s	200	338.962
SR-	kV/s	200	79.459

5.7 EFFECT OF PVT VARIATIONS

In this section effect of Process, supply voltage and temperature variations are shown.

Supply voltage variation is taken 10% i.e. minimum supply voltage is 1.62V and maximum supply voltage is 1.98V.

Temperature variation is taken from -20℃ to 80℃.

And also with these supply and temperature variations five process corner variations are also considered.

TABLE 5.6

PVT VARIATION CHART

SUPPLY VARIATION(V)	**TEMPERATURE VARIATION (℃)**	**PROCESS CORNERS**				
1.8	27	TT	SS	FF	SF	FS
1.8	-20	TT	SS	FF	SF	FS
1.8	80	TT	SS	FF	SF	FS
1.62	27	TT	SS	FF	SF	FS
1.98	27	TT	SS	FF	SF	FS

5.7.1 EFFECT OF PROCESS CORNER

In table 5.7 effect of process corners SS, FF, SF, FS are shown and compared with TT corner are shown. All specifications are achieved except negative slew rate.

TABLE 5.7

EFFECT OF PROCESS CORNER

PARAMETERS	UNITS	TT	SS	FF	SF	FS
AO	db	75.69	75.61	75.69	75.9	75.39
UGB	kHz	756.6	745.9	768.3	755.2	757.9
-3DB	Hz	128.9	128.6	130.2	125.9	133.5
PHASE MARGIN	Degree	60.24	59.71	60.77	59.9	60.49
POWER DISSIPATION	μW	3.51	3.65	3.39	3.54	3.49
SR+	kV/s	338.962	338.464	344.750	344.696	339.839
SR-	kV/s	79.459	79.528	78.816	79.986	78.717
CMRR	db	143.1	111.8	117.8	104.1	104.8
PSRR	db	92.29	92.77	91.99	92.13	92.62
ICMR(MAX)	V	1.51	1.51	1.548	1.56	1.51
ICMR(MIN)	V	0.143	0.147	0.090	0.123	0.102

5.7.2 EFFECT OF TEMPERATURE AND PROCESS CORNER VARIATIONS

Effect of process variation with temperature of -20 deg. and 80deg. is shown in table 5.8 and table 5.9 respectively.

TABLE 5.8

EFFECT OF PROCESS CORNER

AND

TEMPERATURE (TEMP = -20 DEGREE)

PARAMETERS	UNITS	TT	SS	FF	SF	FS
A_O	db	75.93	75.97	75.79	76.07	75.7
UGB	kHz	698.7	690.8	707.6	697.8	699.3
-3DB	Hz	112.5	110.9	115.4	110.4	115.9
PHASE MARGIN	Degree	61.92	61.29	62.55	61.73	62.14
POWER DISSIPATION	μ W	3.55	3.67	3.44	3.58	3.52
SR+	kV/s	333.096	325.853	340.238	341.098	340.136
SR-	kV/s	83.736	84.470	83.002	84.083	82.826
CMRR	db	99.2	96.57	98.04	93.84	104
PSRR	db	93.29	91.59	91.07	91.2	91.44
ICMR(MAX)	V	1.51	1.51	1.51	1.54	1.47
ICMR(MIN)	V	0.072	0.092	0.054	0.098	0.072

During these variations temperature (-20 deg. and 80deg.) with all five process corner variations all target results are achieved except negative slew rate as shown in above table 5.8 and table 5.9.

TABLE 5.9

EFFECT OF PROCESS CORNER

AND

TEMPERATURE (TEMP = 80 DEGREE)

PARAMETERS	**UNITS**	**TT**	**SS**	**FF**	**SF**	**FS**
A_O	db	75.14	74.89	75.26	75.41	74.75
UGB	kHz	802.4	789.6	816	800.2	804.3
-3DB	Hz	148.6	151.1	148.4	143.6	156.5
PHASE MARGIN	Degree	59.35	58.97	59.67	59.11	59.6
POWER DISSIPATION	μ W	3.48	3.63	3.35	3.51	3.45
SR+	kV/s	346.861	341.956	349.973	348.580	341.025
SR-	kV/s	74.338	75.33	73.490	74.911	73.673
CMRR	db	97.85	101.9	97.89	105.7	95.76
PSRR	db	91.32	93.77	92.95	92.97	93.87
ICMR(MAX)	V	1.53	1.54	1.56	1.55	1.51
ICMR(MIN)	V	0.165	0.183	0.142	0.180	0.156

5.7.3 EFFECT OF SUPPLY VOLTAGE AND PROCESS CORNER VARIATIONS

Effect of process variation with supply voltage of 1.62V and 1.98V with $\pm 10\%$ variation is shown in table 5.10 and table 5.11 respectively.

TABLE 5.10

EFFECT OF PROCESS CORNER

AND

SUPPLY (VDD = 1.62V)

PARAMETERS	UNITS	TT	SS	FF	SF	FS
A_O	db	75.44	75.23	75.49	75.69	75.07
UGB	kHz	752.8	741.5k	764.8	751.5	753.8
-3DB	Hz	132.1	133.7	132.7	128.4	137.8
PHASE MARGIN	Degree	59.87	59.29	60.44	59.62	60.11
POWER DISSIPATION	μW	3.16	3.288	3.05	3.19	3.14
SR+	kV/s	338.241	334.991	342.555	342.610	332.722
SR-	kV/s	78.215	78.978	72.213	78.601	77.447
CMRR	db	105.5	100.5	110.4	99.56	119.6
PSRR	db	89.92	90.76	89.4	89.71	90.74
ICMR(MAX)	V	1.33	1.31	1.35	1.35	1.30
ICMR(MIN)	V	0.114	0.131	0.090	0.143	0.108

TABLE 5.11

EFFECT OF PROCESS CORNER

AND

SUPPLY (VDD = 1.98V)

PARAMETERS	**UNITS**	**TT**	**SS**	**FF**	**SF**	**FS**
A_O	db	75.85	75.82	75.81	76.04	75.59
UGB	kHz	759.4	748.8	770.8	757.9	760.7
-3DB	Hz	127	126.1	128.9	123.9	130.7
PHASE MARGIN	Degree	60.54	60.06	61.04	60.31	60.79
POWER DISSIPATION	μW	3.86	4.01452	3.73	3.9	3.83
SR+	kV/s	351.848	350.402	350.439	352.339	351.735
SR-	kV/s	79.462	80.259	78.742	79.991	78.697
CMRR	db	119.8	116.8	113.7	105.2	103.2
PSRR	db	93.67	93.93	93.32	93.45	93.95
ICMR(MAX)	V	1.71	1.73	1.76	1.77	1.70
ICMR(MIN)	V	0.108	0.145	0.095	0.133	0.110

During these variations supply voltage (1.62V and 1.98V) with all five process corner variations all target results are achieved except negative slew rate as shown in above table 5.10 and table 5.11

5.8 EFFECT OF FINGERS ON CMRR

Here CMRR is calculated for different number of fingers. As number of fingers increases matching increases between transistors so CMRR should increase with increase in number of fingers. CMRR depends upon matching between M3 and M4 transistor and matching between them increase as number of fingers increases. So, CMRR should increase with increase in number of fingers. This is shown in figure 5.19 and table 5.12.

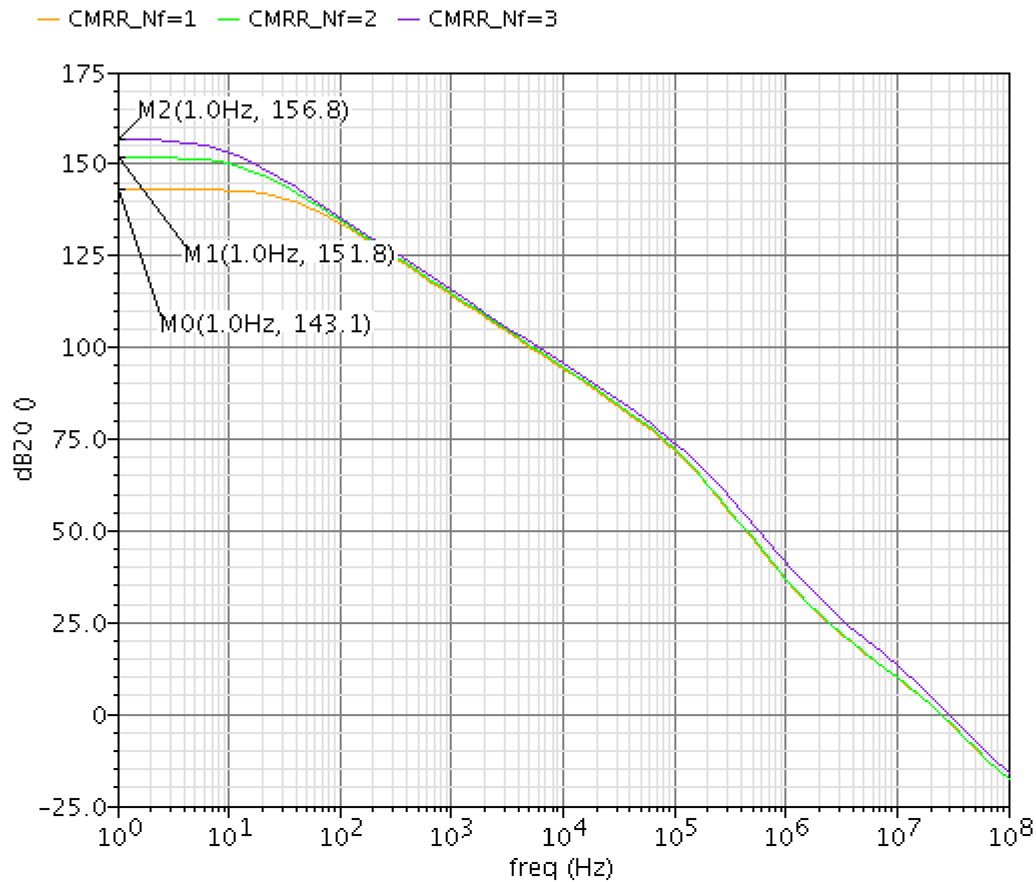

Figure 5.19 Effect of fingers on CMRR

TABLE 5.12

EFFECT OF FINGERS ON CMRR

NUMBER OF FINGERS(NF)	CMRR(db)
1	143.1
2	151.8
3	156.8

5.9 ACHIEVING HIGH CMRR

One can observe from figure 5.7 and figure 5.15 (i.e. from analysis of CMRR), for current buffer compensated opamp CMRR is very high. This is possible i.e. high CMRR is possible by symmetrical bias condition i.e. matching.

In order to improve CMRR, accurate matching must be guranted by both a proper layout design and symmetrical bias conditions. This means the same drain-source voltages.

$$V_{GS3} = V_{DS4} = V_{GS6} \tag{5.22}$$

This matching can be achieved by transistors M13 and M14.

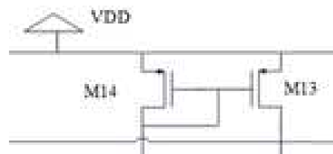

Figure 5.20 M13, 14 used for high CMRR

These two transistors helps in achieving high CMRR. By properly sizing these transistors one can achieve high CMRR.

5.10 PARAMETER EXTRACTION USING BSIM MODEL EQUATION [21]

EFFECTIVE CHANNEL WIDTH AND LENGTH

W_{eff} and L_{eff} in above equation are effective channel width and length and given as, $W_{eff} = W_{drawn} - 2dW$ and $L_{eff} = L_{drawn} - 2dL$. Where dL and dW is given as,

$$dL = L_{INT} + \frac{L_L}{L_{LLN}} + \frac{L_W}{W_{LWN}} + \frac{L_{WL}}{L_{WLN}W_{WWN}} \quad (5.23)$$

$$dW = W_{INT} + \frac{W_L}{W_{WLN}} + \frac{W_W}{W_{WWN}} + \frac{W_{WL}}{L_{WLN}W_{WWN}} \quad (5.23)$$

For NMOS dL= 15.8nm, dW = 10.22nm and for PMOS dL= -10.4nm, dW = -152.5nm

I_O EXTRACTION

In subthresshold region current equation is given as,

$$I_{ds} = I_O \frac{W_{ef} f}{L_{eff}}\left[1 - \exp\left(-\frac{V_{ds}}{nU_T}\right)\right]\exp\left[\frac{V_{gs} - V_{TH} - VOFF}{nU_T}\right] \quad (5.25)$$

Where $I_o = \mu\sqrt{\frac{q\varepsilon_{si}N_{CH}}{4\phi_B}}U_T^2$ and $\phi_S = 2U_T \ln\left(\frac{N_{CH}}{n_i}\right) = 2\phi_B$,

l=44.5nm, X_{dep}=.055um, I_o = 41.8nA, l_t= 26.09nm, C_{dep}=1883.48uF/m^2

Where N_{CH} is average doping concentration in channel, n is slope factor and U_T is thermal voltage and its value is 25.9mV, X_{dep} is depletion width, l_t is characteristic length, VOFF is offset voltage and its value for NMOS is -.1208. The theoretical subthresshold voltage is given by $V_{th,sub} = V_{th} + VOFF$. The difference between threshold voltage of strong inversion and threshold of subthresshold region is several U_T and to account this fact VOFF is introduced.

I_o is calculated as 41.8nA

SUBTHRESSHOLD SLOPE FACTOR (n)

Subthresshold slope factor (n) is given as

$$n = 1 + NFACTOR\frac{C_{dep}}{C_{ox}} + \frac{C_{IT}}{C_{ox}} + \frac{(CDSC + CDSCD..V_{ds} + cdscb.V_{bs})\left(\exp\left(-DVT1\frac{L_{eff}}{2l_t}\right) + \exp\left(-DVT1\frac{L_{eff}}{l_t}\right)\right)}{C_{ox}} \quad (5.26)$$

Where NFACTOR is introduced to cover for any uncertainty in the calculation of depletion capacitance and C_{IT} is interface charge capacitance.

Value of n=1.053 for NMOS.

COEFFICIENT OF CHANNEL LENGTH MODULATION

V_A is early voltage given as

$$V_A = V_{Asat} + \left[1 + \frac{PVAG.V_{gs}}{E_{sat}L_{eff}}\right]\left[\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBL}}\right]^{-1} \quad (5.27)$$

Where V_{ACLM} early voltage due to channel length modulation, V_{ADIBL} is early voltage due to drain induced barrier lowering and V_{Asat} is early voltage at saturation point.

Channel length modulation is inverse of early voltage $\lambda = \frac{1}{V_A}$.

$\lambda_{n1,2}$ =0 .068 for M1 amd M2, $\lambda_n = 0.048$, $\lambda_p = 0.025$

Following table 5.13 shows the calculated sized of transistors of current compensated two stage opam using above parameters calculated using equations (5.21) to (5.25)

TABLE 5.13

SIZES OF TRANSISTORS

TRANSISTOR	SIZE	TYPE	REGION
M1,2	7.5/2	NMOS	SUBTHRESSHOLD
M5,8	0.360/2	NMOS	SATURATION
M7	1.67/2	NMOS	SATURATION
M9,10	0.39/2	NMOS	SATURATION
M11,12	0.68/2	NMOS	SATURATION
M3,4	0.470/2	PMOS	SATURATION
M6	1.945/2	PMOS	SATURATION
M13,14	0.960/2	PMOS	SATURATION
C_C	0.420PF	COMPENSATION CAPACITOR	
C_L	10PF	LOAD CAPACITOR	

TABLE 5.14

COMPARISON BETWEEN OBTAINED RESULTS

AND

TARGET SPECIFICATION

PARAMETER	**UNITS**	**TARGET SPECIFICATIONS**	**SIMULATED RESULTS**
A_O	db	70	75.07
-3DB	Hz	100	167
UGB	kHz	250	950.4
PHASE MARGIN	Degree	60	60.5
POWER DISSIPATION	μW	5	2.87
CMRR	db	85	123.6
PSRR	db	90	90.24
ICMR(MAX)	V	0.2	1.57
ICMR(MIN)	V	1.3	0.180
SR+	kV/s	200	465.999
SR-	kV/s	200	58.180

Table 5.14 shows the comparison between target specification and simulated obtained results. One can observe that negative slew rate is very less than required target specification. All other specifications are obtained

CHAPTER 6

LAYOUT DESIGN AND POST LAYOUT SIMULATION

6.1 INTRODUCTION

In amplifiers it is assumed that the circuits are perfectly symmetric i.e. two sides exhibit identical properties and bias currents. But in reality identical devices suffers from a finite mismatch due to uncertainties in each step of the manufacturing process. Let us take an example, as shown in figure 6.1 shown below, the gate dimensions of MOSFET suffer from random, microscopic variations and hence mismatches between equivalent lengths and widths of two transistors that are identically laid out [20].

Also, MOS devices exhibits threshold voltage mismatch because V_{TH} is a function of doping levels in the channel and the gate, and these levels vary randomly from one device to another.

$$V_{TH} = \Phi_{MS} + \Phi_F + \frac{Q_{dep}}{C_{ox}} \quad (6.1)$$

Where Φ_{MS} is the difference between the work functions of poly gate and the silicon substrate, $\Phi_F = (KT/q)ln(N_{sub}/n_i)$, q is electron charge, N_{sub} is the doping concentration of substrate , Q_{dep} is the charge in depletion region, and C_{ox} is the gate capacitance per unit area. So, to minimize effect of mismatch effective layout technique is needed.

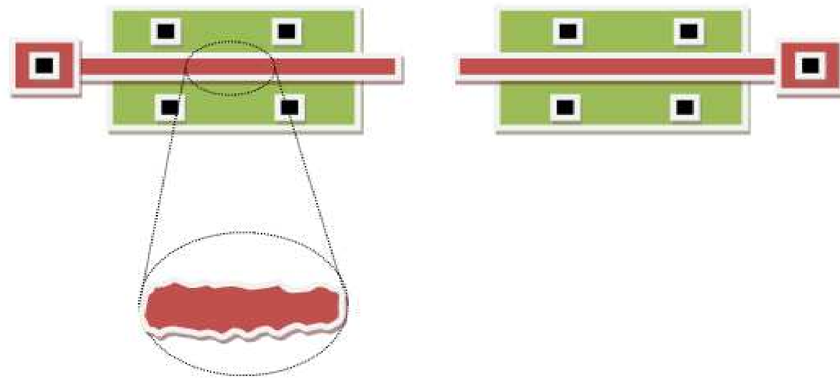

Figure 6.1 Random mismatch due to microscopic variations in device dimensions

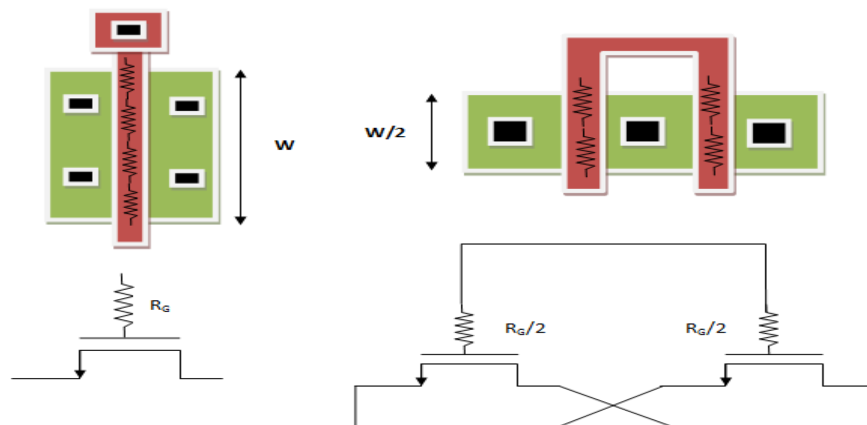

Figure 6.2 Reduction of gate resistance by multi-finger layout design style or by folding

Analog systems demand many layout precautions so as to minimize mismatch and parasitic. Multi-finger transistors use to reduce mismatch S/D junction area and the gate resistance. Thumb rule for fingering is "the width of each finger is chosen such that the resistance of the finger is less than the inverse transconductance associated with the finger". While the gate resistance can be reduced by decomposing the transistor into more parallel fingers but the capacitance associated with the perimeter of the S/D areas increases. For example, as shown in figure 6.2. Multi-finger layout or folding reduces the gate resistance by a factor of four.

6.2 LAYOUT OF OPAMP

In figure 6.3 layout of current buffer compensated opamp is shown. Schematic of this opamp is shown in figure 5.4. Optimized sizes of transistors and compensation capacitor for process variation shown in section 5.5.2.

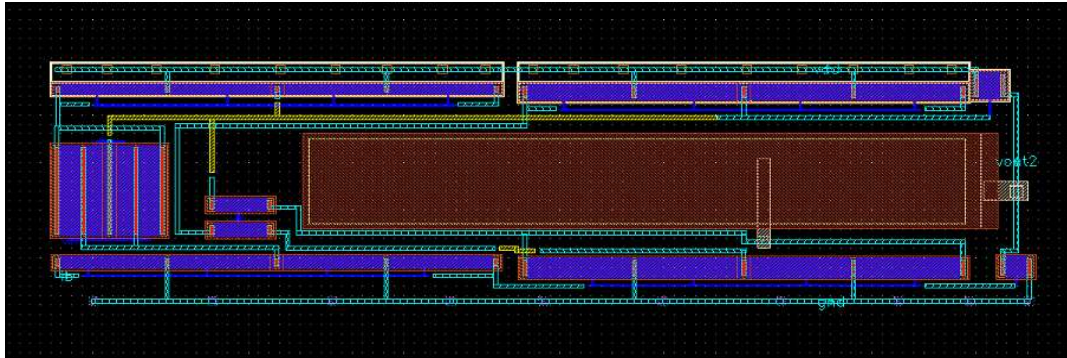

Figure 6.3 Layout of two stage opamp with current buffer compensation with C_C=0.580pF

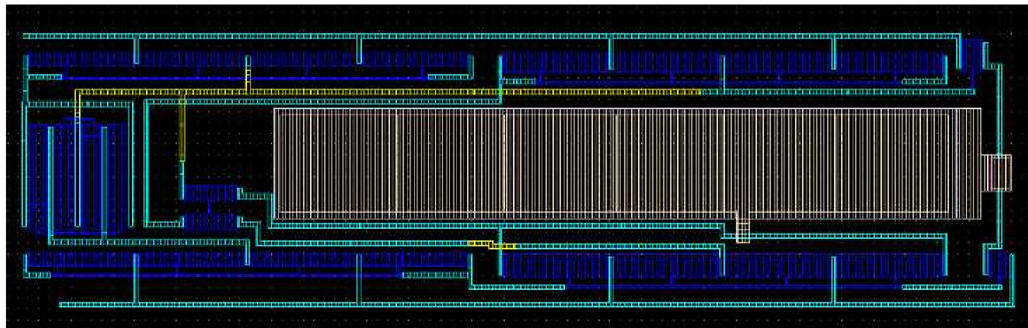

Figure 6.4 Extracted view of layout of two stage opamp in figure 6.3

In figure 6.4 extracted view of layout shown in figure 6.3 is shown. With extracted view parasitic are attached like parasitic capacitance and parasitic resistors. This view is used for post layout simulation.

RCX is use to extract parasitic from layout and for post layout simulation this extracted view is simulated i.e. parasitic are attached to schematic.

Parasitic like parasitic capacitance and parasitic resistors attached with extracted view are shown in figure 6.5. Figure 6.5 is enlarged or zoomed picture of extracted view.

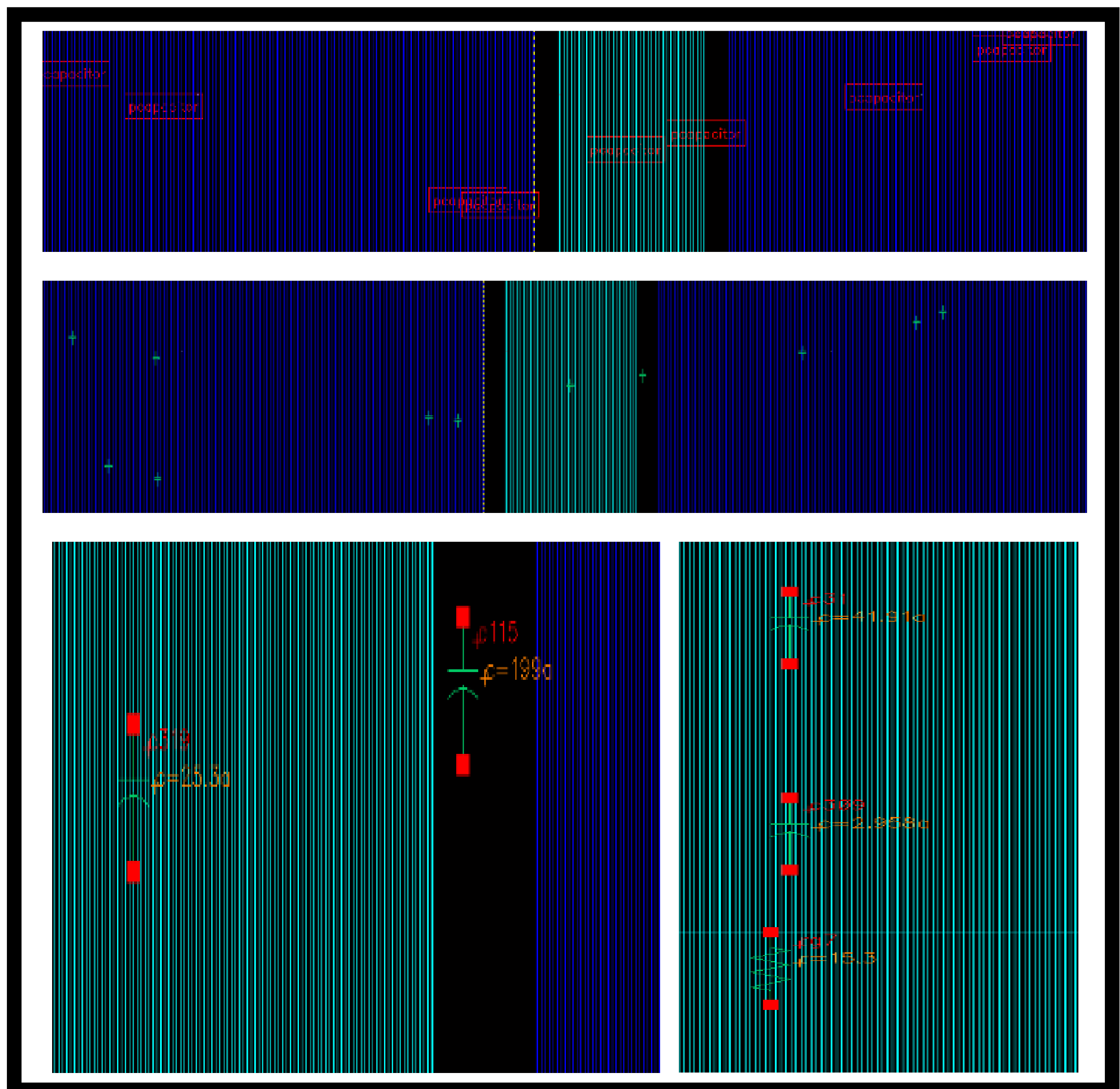

Figure 6.5 Zoomed extracted view of layout showing parasitic

6.3 FREQUENCY RESPONSE

In figure 6.6 the AC analysis of layout is shown. This figure 6.6 shows post layout simulation.

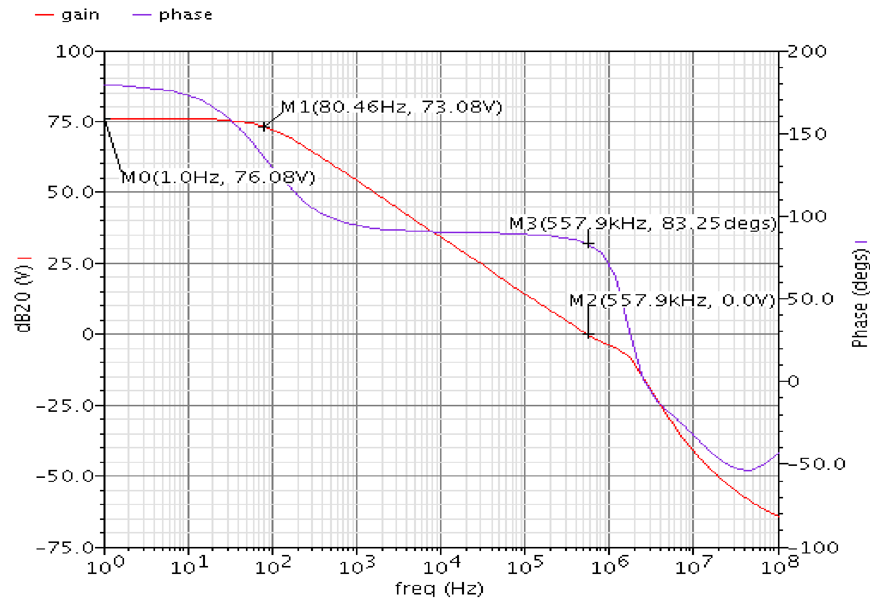

Figure 6.6 Post layout simulation

In above figure 6.6 Gain, phase vs frequency plot with C_C=0.580pF is shown. One can observe that result in this case after post layout simulation degrades or changes this is due to parasitic UGB and -3db degrades to 557.9kHz and 80.46Hz and phase margin become 83.42 degree. It means that C_C should be decrease so as to decrease phase margin and increase or improve bandwidth. Results shows that parasitic are added in C_C i.e. parasitic are increasing compensation capacitor. So, one has to decrease value of compensation capacitor for compensating parasitic so that to achieve same result as we are getting with schematic. So C_C value is taken as 0.380pF.

In figure 6.7, the optimized layout of opamp with C_C=0.380pF is shown.

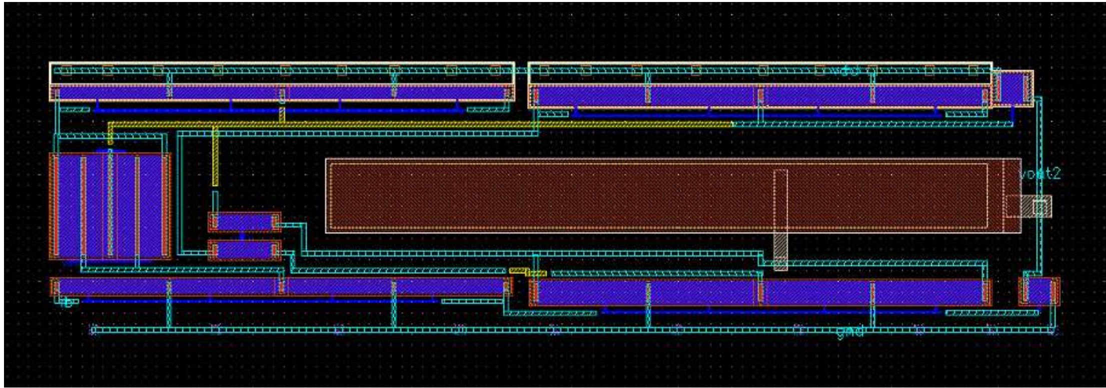

Figure 6.7 Optimized layout of two stage opamp with C_C=0.380pF

6.4 POST LAYOUT SIMULATION OF OPTIMIZED LAYOUT

Simulation results for gain, bandwidth, phase margin, ICMR, CMRR, PSRR, transient response etc at tt corner are shown in this section.

6.4.1 AC ANALYSIS

The AC analysis of operational amplifier is done by following circuit setup as shown in figure 4.6 and simulation results for AC analysis for gain and phase plot vs frequency is shown in figure 6.8. Now from figure 6.8, designed opamp has

Gain = 76.21db

-3db = 119.4Hz

UGB = 743.2 KHz

Phase margin = 62.77°

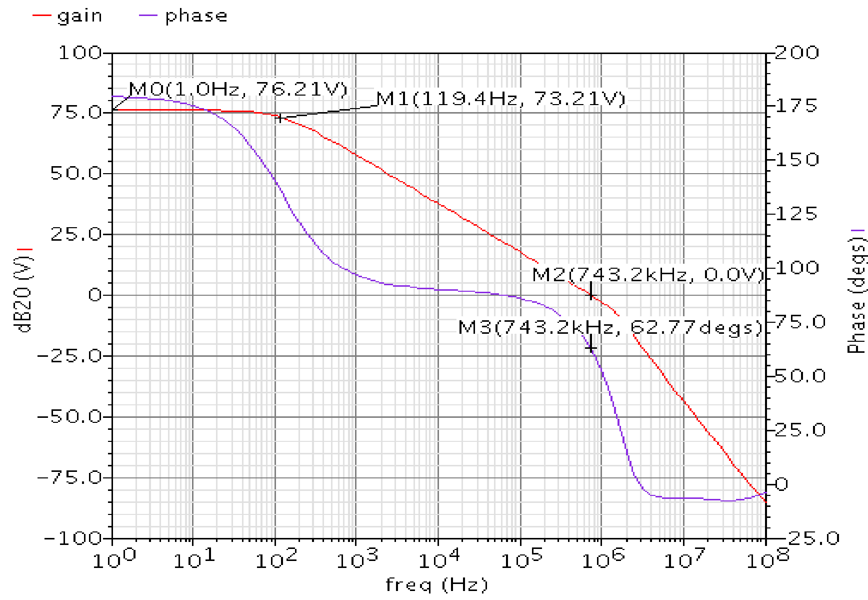

Figure 6.8 Gain and phase plot

6.4.2 CMRR MEASUREMENT

The circuit setup for CMRR analysis is shown in figure 4.8 and response is shown in figure 6.9 and the measure CMRR is 157.1db as shown in figure 6.9.

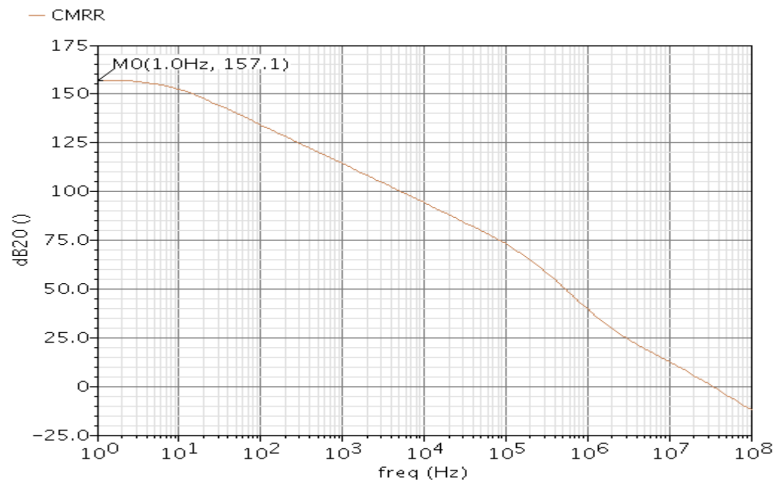

Figure 6.9 Common mode rejection ratio (CMRR)

In layout CMRR increases to 157.1db as compared to schematic where CMRR is 143.1 shown in figure 5.15.

6.4.3 PSRR MEASUREMENT

For the measurement of PSRR, opamp is connected in unity gain feedback, a DC bias is connected to input and AC signal at VDD terminal for PSRR measurement. Setup for PSRR measurement is shown in figure 4.10 and PSRR response in figure 6.10. Above figure 6.10 shows PSRR = 92.85db

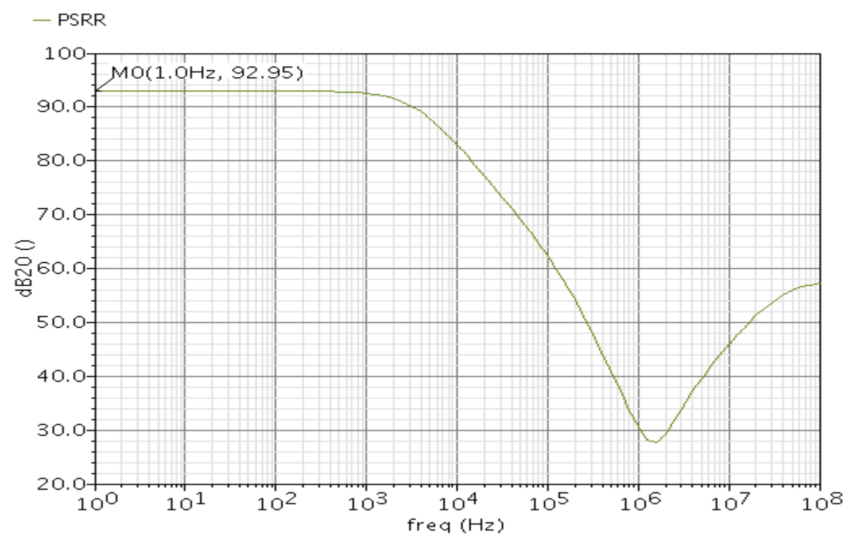

Figure 6.10 Power supply rejection ratio (PSRR)

6.4.4 ICMR MEASUREMENT

For ICMR measurement apply variable DC voltage at input of opamp in unity gain configuration as shown in figure 4.12 and its response is shown in figure 6.11.

From ICMR plot shown in figure 6.11, ICMR (max) is 1.54 and ICMR (min) is 0.119V.

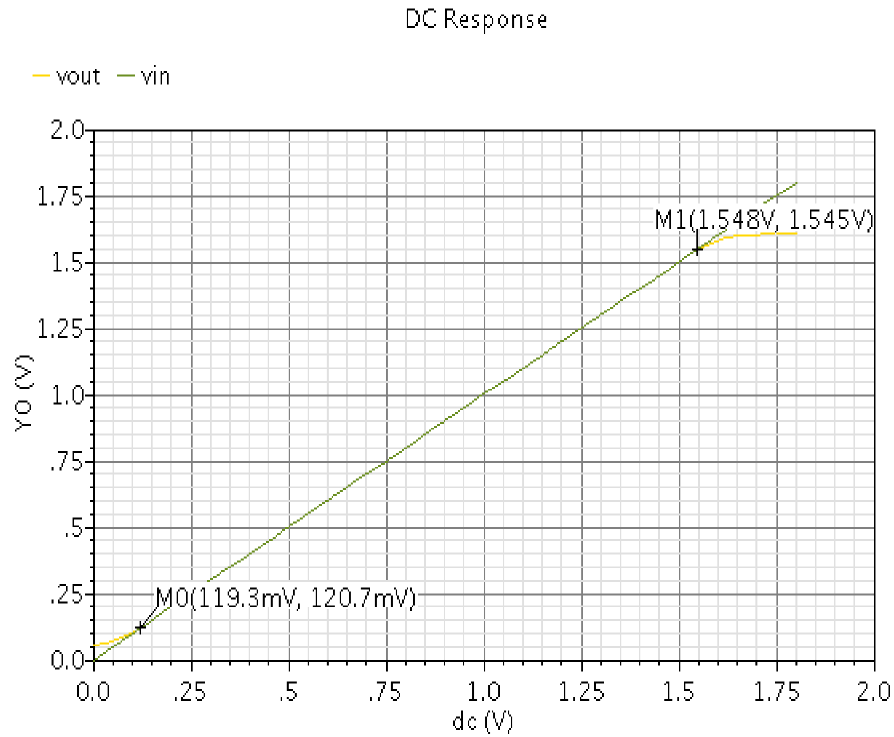

Figure 6.11 Input common mode range (ICMR)

6.4.5 TRANSIENT ANALYSIS

Setup for transient analysis is shown in figure 4.15 and output transient response shown in figure 6.14. A sin wave is applied with 240μV peak to peak is applied as input.

In figure 6.14, $V_{out(p\text{-}p)} = 1.1928$ and $V_{in(p\text{-}p)} = 240\mu V$, thus

$$Gain = \frac{1.1928}{240\mu} = 4970 = 73.92db$$

AC analysis in figure 6.8 shows that gain = 76.21db and gain calculated by transient analysis is 73.92db.

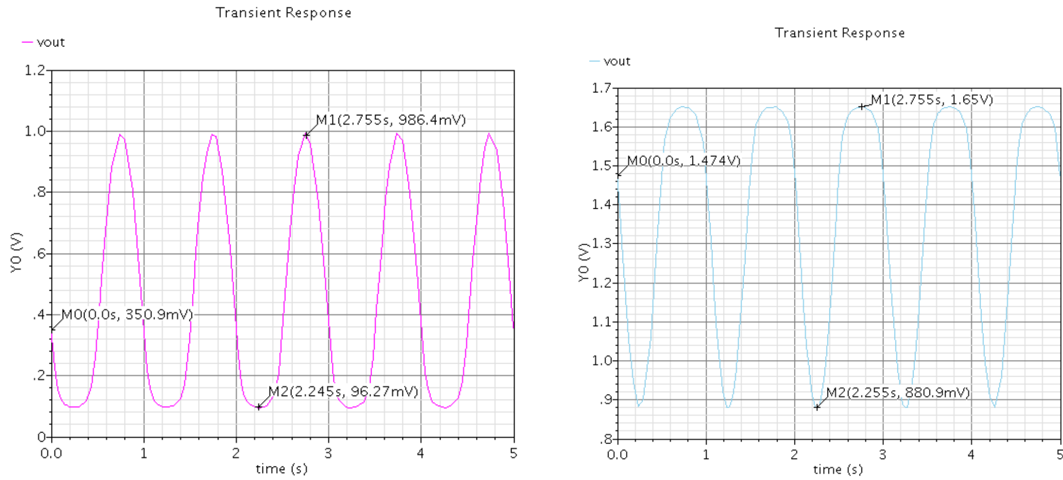

Figure 6.12 Transient analyses during SF and FS corners

During process corner simulation SF and FS corner simulation transient analysis are shown in figures shown above. One can observe that transient analysis fails during SF and FS process corner simulation. For removing this problem, one has to remove process variations, now process variation can be minimized by using fingers. As fingers are used process variation effect decreases. When fingers of M6 is taken as 4 and M7 taken as 2, transient analysis is optimized to large extent. Basically, it is observed during process corner analysis that Ron6 and Ron7 differ with large amount that is why during SF and FS Vcm_out varies with large amount. Ron6 and Ron7 is 1Mohm during TT corner but during SF Ron6 become 1.4Mohm and Ron7 is 300kohm and during FS Ron6 become 300kohm and Ron7 is 1.4Mohm. Fingering of M6 and M7 is shown in layout shown below in layout. All results shown in this chapter taken using final layout shown in figure 6.13

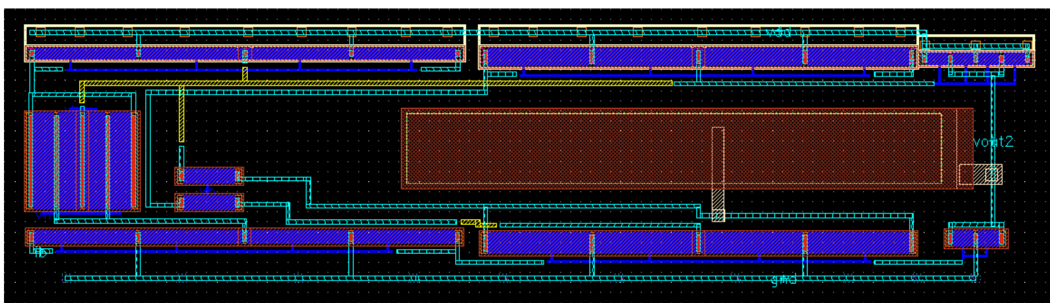

Figure 6.13 Final layout of opamp

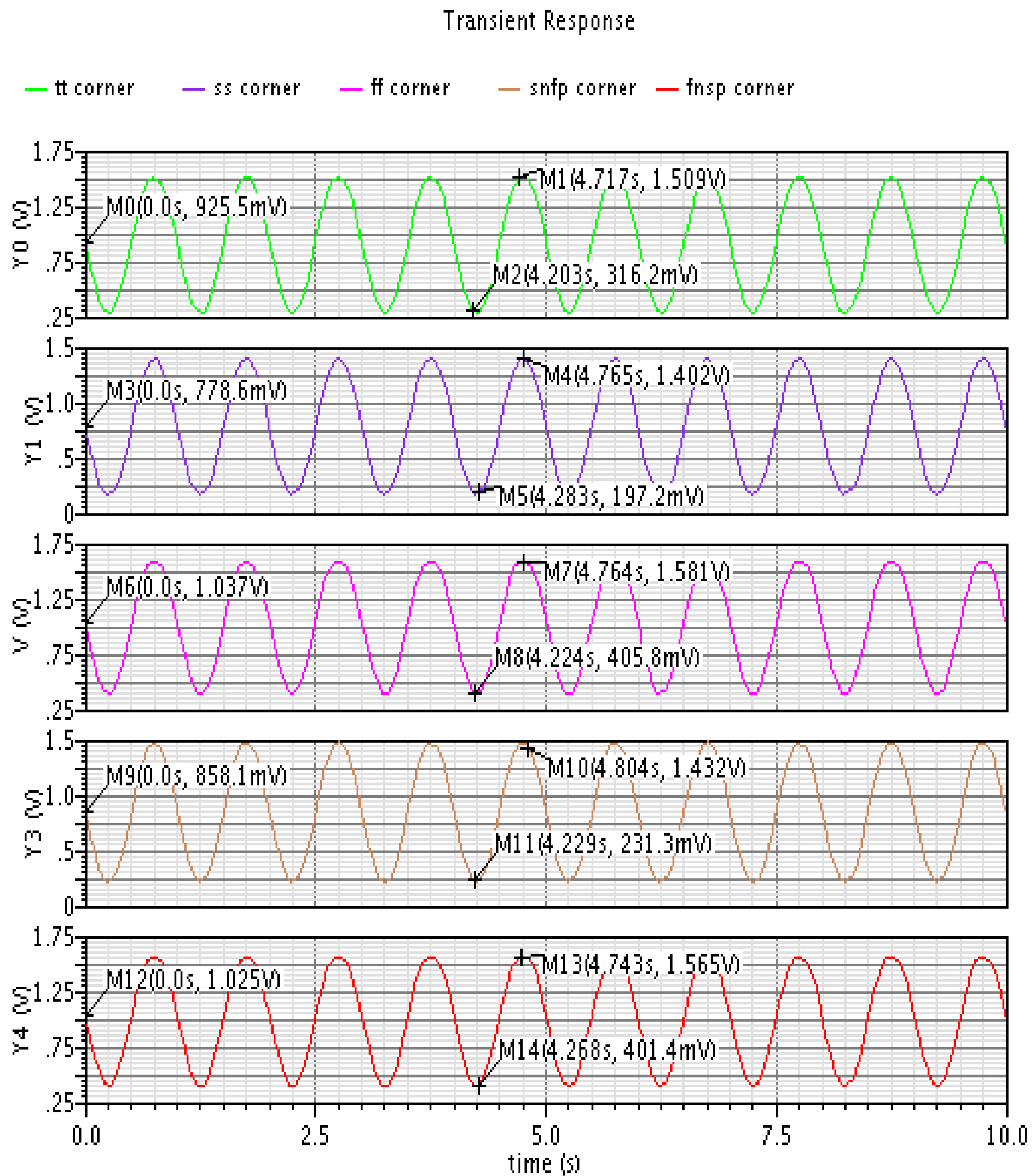

Figure 6.14 Transient analysis at all five process corners

6.5. EFFECT OF PVT VARIATION

PVT variation chart is shown in table 5.6. In this section 6.5.1 effect of process corners is given.

6.5.1 EFFECT OF PROCESS CORNERS

In table 6.1 effect of process corners SS, FF, SF, FS are shown and compared with TT corner are shown. All specifications are achieved except negative slew rate.

TABLE 6.1

EFFECT OF PROCESS

PARAMETERS	UNITS	TT	SS	FF	SF	FS
A_O	db	76.21	76.01	76.21	75.73	73.85
-3DB	Hz	119.4	120	119.4	125.1	156.2
UGB	kHz	743.2	726	739.9	728.6	735.2
PHASE MARGIN	Degree	62.77	63.76	61.01	62.5	62.04
POWER DISSIPATION	μW	3.69	3.84	3.19	3.54	3.43
SR+	kV/s	334.124	330.276	339.497	338.655	329.121
SR-	kV/s	74.309	83.489	67.013	78.624	70.149
CMRR	db	157.1	103.39	103	104.3	99.66
PSRR	db	92.45	91.99	92.81	91.48	94.43
ICMR(MAX)	V	1.54	1.52	1.54	1.56	1.54
ICMR(MIN)	V	0.119	0.123	0.081	0.112	0.093

6.5.2 EFFECT OF TEMPERATURE AND PROCESS CORNER VARIATIONS

Effect of process variation with temperature of -20 deg. and 80deg. is shown in table 6.2 and table 6.3 respectively.

TABLE 6.2

EFFECT OF PROCESS CORNER

AND

TEMPERATURE (TEMP= -20 DEGREE)

PARAMETERS	UNITS	TT	SS	FF	SF	FS
A_O	db	75.64	75.49	75.79	75.69	72.68
-3DB	Hz	136.9	137.6	136	135.6	193.6
UGB	kHz	777.6	764.3	786.1	772.6	780.6
PHASE MARGIN	Degree	61.32	62.8	59.9	61.39	60.98
POWER DISSIPATION	μW	3.47	3.86	3.15	3.53	3.42
SR+	kV/s	339.107	334.653	342.950	340.729	334.529
SR-	kV/s	70.997	80.914	63.267	75.635	66.558
CMRR	db	98.43	105.5	95.63	110.6	95.91
PSRR	db	92.98	92.41	93.41	91.64	95.34
ICMR(MAX)	V	1.54	1.53	1.58	1.58	1.54
ICMR(MIN)	V	0.160	0.184	0.125	0.165	0.144

TABLE 6.3

EFFECT OF PROCESS CORNER

AND

TEMPERATURE (TEMP= 80 DEGREE)

PARAMETERS	**UNITS**	**TT**	**SS**	**FF**	**SF**	**FS**
A_O	db	76.34	76.28	76.34	75.57	74.11
-3DB	Hz	105.1	105	105.8	114.2	135.9
UGB	kHz	676.6	671.4	682.3	673.3	678.5
PHASE MARGIN	Degree	64.15	65.46	62.91	64.39	63.76
POWER DISSIPATION	μW	3.49	3.83	3.22	3.55	3.45
SR+	kV/s	329.170	319.653	336.047	334.324	320.902
SR-	kV/s	76.901	85.394	69.958	80.947	72.745
CMRR	db	102.8	97.62	107.93	96.44	113.3
PSRR	db	91.76	91.35	92.04	90.7	93.56
ICMR(MAX)	V	1.51	1.50	1.53	1.52	1.51
ICMR(MIN)	V	0.056	0.084	0.054	0.077	0.043

During these variations temperature (-20 deg. and 80deg.) with all five process corner variations all target results are achieved except negative slew rate as shown in above table 6.2 and table 6.3.

6.5.3 EFFECT OF SUPPLY VOLTAGE AND PROCESS CORNER VARIATIONS

Effect of process variation with supply voltage of 1.62V and 1.98V with ± 10% variation is shown in table 6.4 and table 6.5 respectively.

TABLE 6.4

EFFECT OF PROCESS CORNER

AND SUPPLY (VDD = 1.62V)

PARAMETERS	UNITS	TT	SS	FF	Sf	fs
A_O	db	75.88	75.74	75.99	75.42	75.63
-3DB	Hz	122.8	123.8	122.4	129.2	128
UGB	kHz	730.4	723.6	737.7	726.7	741.9
PHASE MARGIN	Degree	62.22	63.61	60.89	62.4	62.06
POWER DISSIPATION	μW	3.13	3.46	2.87	3.19	3.23
SR+	kV/s	333.318	328.849	337.748	335.516	328.209
SR-	kV/s	70.035	82.091	65.824	73.37	68.947
CMRR	db	118.8	100.9	108.3	101.5	100.8
PSRR	db	90	89.27	90.51	88.23	94.89
ICMR(MAX)	V	1.33	1.32	1.36	1.36	1.34
ICMR(MIN)	V	0.108	0.137	0.081	0.113	0.108

TABLE 6.5

EFFECT OF PROCESS CORNER

AND SUPPLY (VDD = 1.98V)

PARAMETERS	**UNITS**	**TT**	**SS**	**FF**	**SF**	**FS**
A_O	db	76.28	76.18	76.35	75.93	75.23
-3DB	Hz	117.4	117.8	117.6	122.2	133
UGB	kHz	734.2	728.2	741.5	730	737.9
PHASE MARGIN	Degree	62.44	63.82	61.09	62.57	62.28
POWER DISSIPATION	μW	3.82	4.22	3.51	3.89	3.78
SR+	kV/s	343.841	324.342	346.236	343.924	322.664
SR-	kV/s	74.324	83.434	67.085	79.405	70.180
CMRR	db	108	114.4	102.3	105.6	98.84
PSRR	db	93.82	93.38	94.08	92.83	95.17
ICMR(MAX)	V	1.74	1.71	1.76	1.75	1.72
ICMR(MIN)	V	0.108	0.132	0.072	0.128	0.092

During these variations supply voltage (1.62V and 1.98V) with all five process corner variations all target results are achieved except negative slew rate as shown in above table 6.4 and table 6.5

CHAPTER

CONCLUSION AND FUTURE RESEARCH

7.1 CONCLUSION

In present work two compensation techniques are compared. In table 5.3, there is comparison between RC compensated opamp shown in figure 4.1 and current buffer compensated opamp shown in figure 5.4.

RC compensated opamp design method presented in this present work, one can observe that C_C is 0.9pF which is less than minimum accepted value i.e. 2.2Pf (C_C=0.22 C_L where C_L=10pF). So, advantage of this technique is that compensation capacitor value decreases.

Current buffer compensated opamp there is improvement of gain, bandwidth, phase margin CMRR, slew rate but power dissipation increases and PSRR decreases. Also, area requirement for current buffer compensation technique is very less as compared to RC compensation technique.

Compensation capacitor is less for current buffer compensated opamp as compared to RC compensated opamp.

In this present work, technique to achieve high CMRR is given as shown in section 5.9. One of the main advantages of current buffer compensated opamp is that it has high CMRR and high bandwidth. On can use it where high CMRR is required. One can observe that typical value of CMRR obtained in this current buffer compensated opamp is 157.1db after post layout simulation.

During transient analysis improvement, it is observed that a MOS can be represented as resistor and during process variations its value should not be vary so as to pass process corners. So, any analog circuit can be represented by RC network.

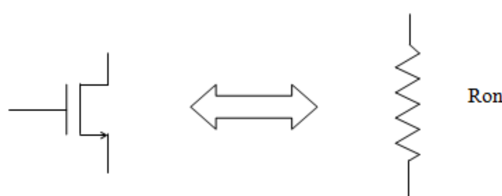

Figure 7.1 MOS and resistor equivalence

In section 5.5 it is shown that how to manage process variations. And tried to implement process variation mitigate techniques like increasing area of some MOS devices, design should be “wide” for proper aligning of poly or aligning poly in same direction and multi-finger technique.

One main thing for managing process variation is that current sources should be in saturation as it affect current less as compared to current source in subthresshold region. As in saturation current follows square law and in subthresshold region current follow exponential law.

Also, there may one or more sensitive nodes voltages on such nodes should be stable for stability during process variations, from this concept of sensitive nodes emerges like in current buffer compensated opamp output of first stage is sensitive node.

All simulation results are shown in form of best case, worst case, and typical case compared with target specifications of current compensated opamp. These results are shown in table 7.1 given below.

TABLE 7.1

SPECIFICATION COMPARISON IN TERMS OF TYPICAL, BEST AND WORST CASE

PARAMET-ERS	**UNITS**	**TARGET SPECIFICA-TIONS**	**TYPICAL**	**BEST CASE**	**WORST CASE**
A_O	db	>70	76.21	76.35	72.68
-3db	Hz	>100	119.4	193.6	105
UGB	kHz	>250	743.2	786.1	671.4
PHASE MARGIN	Degree	60	62.77	65.46	59.9
POWER DISSIPATION	μW	<5	3.69	2.87	4.22
SR+	kV/s	>200	334.124	346.236	320.902
SR-	kV/s	>200	74.309	85.394	63.267
CMRR	db	>85	157.1	157.1	95.63
PSRR	db	>90	92.45	95.34	88.23
ICMR(MAX)	V	1.3	1.54	1.76	1.32
ICMR(MIN)	V	0.2	0.119	0.043	0.184

7.2 FUTURE RESEARCH

In this work, one can observe that negative slew rate is not equal to positive slew rate and negative slew rate is 4 to 5 times smaller than positive slew rate. Condition for negative slew rate is that I1=I2 (see figure 5.1) even after applying this condition negative slew rate is not equal to positive slew rate. Thus, this is one main problem or area of improvement.

Hence, above low power opamp can be used as preamplifier for biomedical applications as it is stable and achieves almost all target specifications for biomedical applications like ECG. So, it can be used to make low power biomedical systems like ECG system.

APPENDIX

IMPROVEMENT FOR PROCESS VARIATION

In this section improvement in results during process corner simulation is done. In table 5.4 process corner analysis is given during SF and FS one can observe that simulation fails. A way is to use fingers for M6 and M7 when 8 fingers for M6 and 4 fingers for M7 is taken (NMOS has taken just half the fingers of PMOS, also taken in section 6.4.5 for improvement in transient

TABLE A.1

EFFECT OF PROCESS CORNER

PARAMETER	UNITS	TT	SS	FF	SF	FS
A_O	db	73.55	73.04	73.537	73.5	73.429
-3DB	Hz	194	202	194.27	194.3	194.3
UGB	kHz	1055	989.1	1127	1033	1072
PHASE MARGIN	Degree	64.88	66.459	63.42	66.17	63.737
POWER DISSIPATION	μW	3.79	4.34	3.42	4.08	3.55
CMRR	db	110.87	85.68	89.157	88.61	88.339

analysis it shows good results or one can say best case when fingers of PMOS is twice the NMOS). Results are shown in table A.1

One can observe from table A.1 effect of process variation minimizes. One can compare with results shown in table 5.4 where gain, bandwidth are not stable during process corner simulation.

APPENDIX

B

SMALL SIGNAL ANALYSIS

In this section small signal analysis of current buffer compensated opamp is given.

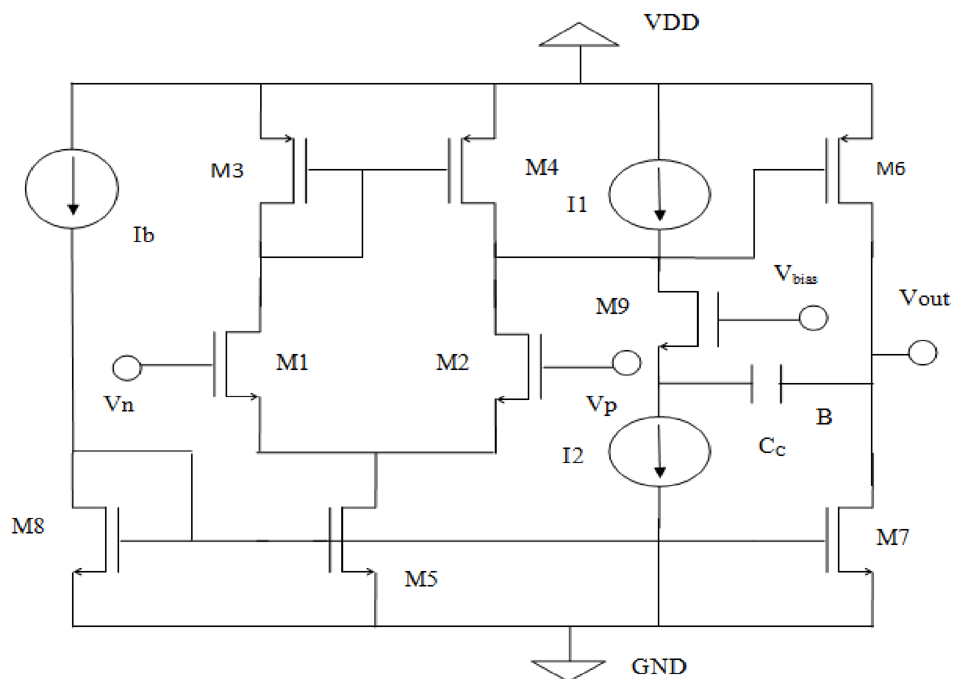

Figure B.1 Schematic of current buffer compensated opamp

Small signal circuit of figureB.1 is shown in figure B.2 and its simplified circuit is shown in figure B.3

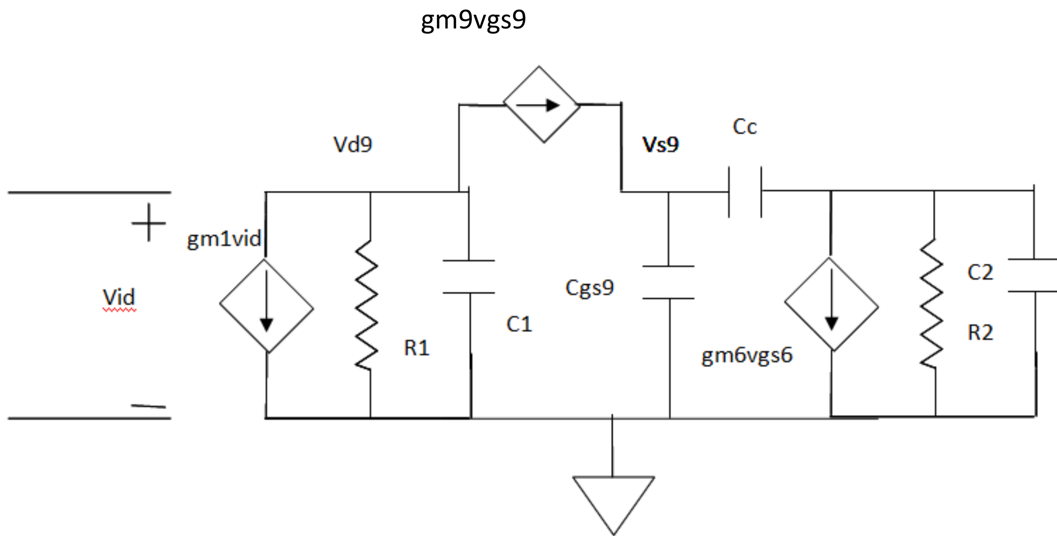

Figure B.2 Small signal circuit of current buffer compensated opamp

Source rearrangement method is used to simplify circuit [8]. Figure B.2 is simplified to Figure B.3 as shown below.

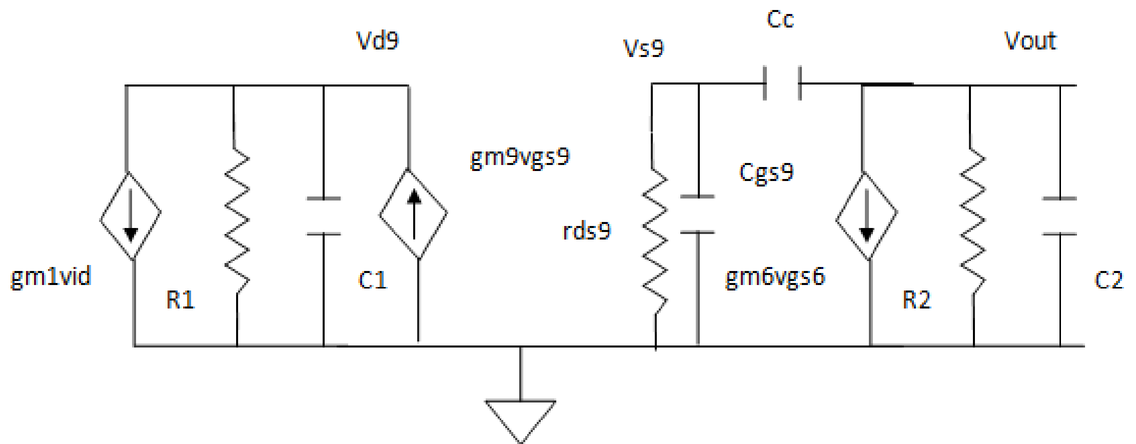

Figure B.3 Simplified Small signal circuit

One can divide circuit in three parts given below:

PART 1

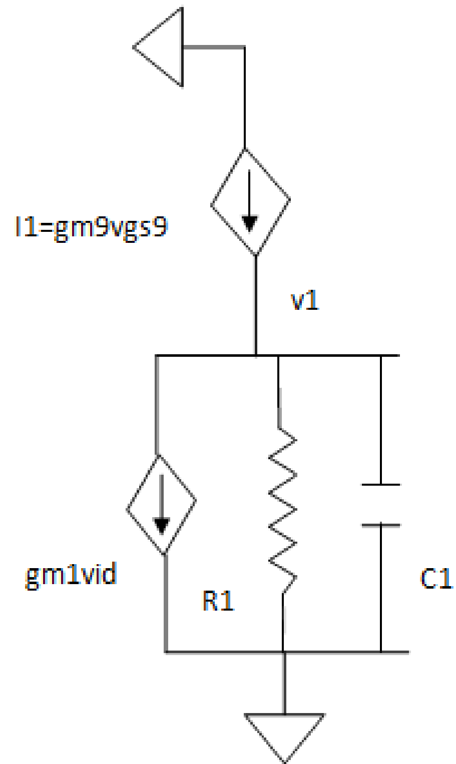

Figure B.4 Part1 of simplified Small signal circuit

$$i1 = gm9vgs9 \tag{B.1}$$

$$(vout - vs9)sCc = i1 \tag{B.2}$$

$$(vout - vs9)sCc = gm9vs9 \tag{B.3}$$

$$\frac{voutsCc}{gm9 + sCc} = vs9 \tag{B.4}$$

$$i1 = gm1vid + \frac{v1}{R1} + v1sC1 \tag{B.5}$$

PART2

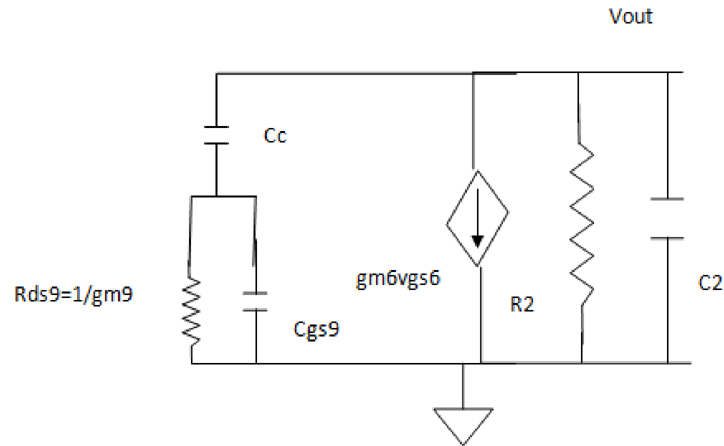

Figure B.5 Part2 of simplified Small signal circuit

$$\frac{vout}{\frac{1}{scgs9+gm9}+\frac{1}{sCc}}+gm6v1+\frac{vout}{R2}+voutsC2=0 \tag{B.6}$$

PART3

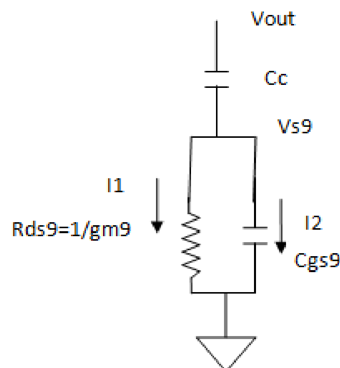

Figure B.6 Part3 of simplified Small signal circuit

$$\frac{vout-0}{\dfrac{1}{gm9+sCgs9}+\dfrac{1}{sCc}}=i1+i2=\frac{vs9}{1/gm9}+vs9sCgs9 \tag{B.7}$$

$$(gm9+sCgs9)vs9=\frac{vout}{(sCc+gm9+sCgs9)}sCc(gm9+sCgs9) \tag{B.8}$$

$$vs9=\frac{voutsCc}{s(Cc+Cgs9)+gm9} \tag{B.9}$$

From equation (B.1) and (B.5) we get,

$$gm9vs9=gm1vid+\frac{v1}{R1}+v1sC1=0 \tag{B.10}$$

Putting value of vs9 from (B.9) into (B.10), we get

$$gm9\frac{voutsCc}{s(Cc+Cgs9)+gm9}=gm1vid+\frac{v1}{R1}+v1sC1=0 \tag{B.11}$$

$$\frac{gm9sCcvout}{s(Cc+Cgs9)+gm9}=gm1vid+v1\left[\frac{1}{R1}+sC1\right] \tag{B.12}$$

From equation (B.6), we get,

$$gm6v1=-\frac{voutsCc(sCgs9+gm9)}{sCc+gm9+sCgs9}-\frac{vout}{R2}-svoutC2 \tag{B.13}$$

Putting value of v1 from (B.13) into (B.12), we get,

$$\frac{gm9sCcvout}{s(Cc+Cgs9)+gm9}gm6=gm1vidgm6-\left[\frac{voutsCc(gm9+sCgs9)}{s(Cgs9+Cc)+gm9}+\frac{vout}{R2}+voutsC2\right]\left[\frac{1}{R1}+sC1\right] \tag{B.14}$$

$$\left[\frac{gm6gm9sCc}{s(Cc+Cgs9)+gm9}+\left(\frac{sCc(gm9+sCgs9}{s(Cc+Cgs9)+gm9}+\frac{1}{R2}+sC2\right)\left(\frac{1}{R1}+sC1\right)\right]vout=gm1gm6vid$$

(B.15)

$$\frac{gm6gm9sCc}{s(Cc+Cgs9)+gm9}+\frac{sCc(gm9+sCgs9)}{s(Cc+Cgs9)+gm9}\left(\frac{1}{R1}+sC1\right)+\left(\frac{1}{R2}+sC2\right)\left(\frac{1}{R1}+sC1\right)=gm1gm6\frac{vid}{vout}$$

(B.16)

$$gm6gm9sCc+sCc(gm9+sCgs9)\left(\frac{1}{R1}+sC1\right)+\left(s(Cc+Cgs9)+gm9\right)\left(\frac{1}{R1}+sC1\right)\left(\frac{1}{R2}+sC2\right)$$
$$=gm1gm6\frac{vid}{vout}\left[s\left(Cc+Cgs9\right)+gm9\right]$$

(B.17)

Solving left hand side of equation (B.17):

$$\Rightarrow gm6gm9sCc+sCc(gm9+sCgs9)\left(\frac{1}{R1}+sC1\right)+(s(Cc+Cgs9)+gm9)\left(\frac{1}{R2}+sC2\right)\left(\frac{1}{R1}+sC1\right)$$

Taking gm9 common and take it to right hand side, we get left hand side as,

$$\Rightarrow sgm6Cc+sCc\left(1+\frac{sCgs9}{gm9}\right)\left(\frac{1}{R1}+sC1\right)+\left(\frac{s(Cc+Cgs9)}{gm9}+1\right)\left(\frac{1}{R1}+sC1\right)\left(\frac{1}{R2}+sC2\right)$$

Taking R1R2 as L.C.M. at L.H.S. And take R1R2 in numerator to R.H.S., we get L.H.S. as,

$$\Rightarrow sgm6R1R2Cc+sCc\left(1+\frac{sCgs9}{gm9}\right)(1+sR1C1)R2+\left(\frac{s(Cc+Cgs9)}{gm9}+1\right)(1+sR1C1)(1+sR2C2)$$

$$\Rightarrow sgm6R1R2Cc+sCc\left(1+\frac{sCgs9}{gm9}\right)\left(1+sR1C1\right)R2+\left(1+\frac{s(Cc+Cgs9)}{gm9}\right)(1+sR1C1)(1+sR2C2)$$

$$\Rightarrow sgm6R1R2Cc + sCR2 + s^3 \frac{CcCgs9}{gm9} C1R1R2 + s^2 \left[\frac{R2CcCgs9}{gm9} + CcC1R1R2 \right]$$

$$+ \left[1 + s^3 \left(\frac{Cc + Cgs9}{gm9} R1C1R2C2 \right) \right] + s^2 \left[\frac{Cc + Cgs9}{gm9} C1R1 + R1C1R2C2 + \frac{Cc + Cgs9}{gm9} R2C2 \right]$$

$$+ s \left[\frac{Cc + Cgs9}{gm9} + R1C1 + R2C2 \right]$$

$$\Rightarrow s^3 \left[\frac{Cgs9CcC1R1R2}{gm9} + \frac{Cc + Cgs9}{gm9} R1C1R2C2 \right]$$

$$+ s^2 \left[\frac{Cc + Cgs9}{gm9} R1C1 + R1C1R2C2 + \frac{Cc + Cgs9}{gm9} R2C2 + \frac{CcCgs9}{gm9} R2 + R1R2C1Cc \right]$$

$$+ s \left[gm6R1R2Cc + CcR2 + \frac{Cc + Cgs9}{gm9} + R1C1 + R2C2 \right] + 1$$

(B.18)

Small signal frequency response of current buffer compensated opamp is given as,

$$A(s) = \frac{vout}{vid} = \frac{gm1gm6R1R2 \left[1 + \frac{s(Cc + Cgs9)}{gm9} \right]}{1 + as + bs^2 + cs^3} \qquad \text{(B.19)}$$

Equation (B.18) is the denominator of equation (B.19)

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