EFFECT OF DRIVER SIZE AND OPTIMUM REPEATERS ON PROPAGATION DELAY AND POWER DISSIPATION IN MWCNT INTERCONNECTS

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CERTIFICATE

I, Arun Verma, hereby certify that the work which is being presented in this dissertation entitled **"Effect of Driver Size and optimum Repeaters on propagation delay and power dissipation in MWCNT Interconnects"** by me in partial fulfillment of the requirements for the award of degree of Master of Engineering in Electronics and Communication Engineering from Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of **Karmjit Singh Sandha** and refers other researcher's work which are duly listed in the reference section.

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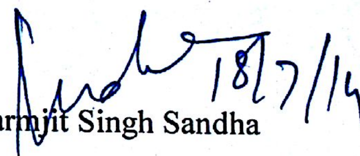

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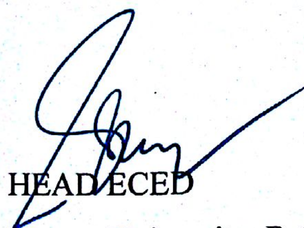

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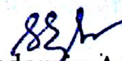

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ABSTRACT

At such a high pace advancements in the technologies today and their ubiquitous use, speed and size, has been the important aspects in VLSI interconnect. Most importantly interconnects play a big role in defining the size, power consumption and clock frequency in digital system. This thesis covers the various aspects of Carbon Nanotube (CNT) based VLSI interconnects. CNT interconnects presents a promising option for replacing the existing Copper interconnects. The two basic types of CNT are the Single wall and Multi wall CNT (i.e. SWCNT and MWCNT). The MWCNT's equivalent electrical model has been briefly studied. It has been seen how the individual shell structure of the MWCNT behaves like the equivalent circuit of the passive elements i.e. RLC, which results us to easily study the MWCNT. The comparative study between MWCNT and Copper interconnects are shown with respect to RLC values, Delay and Average power consumed. The value of driver size, where the propagation delay is minimum and power is not too high is the optimum value, because the value of power is increasing with the driver size as propagation delay decreases for some values. The lumped circuit for the RLC interconnects results in an increased propagation delay, so a distributed circuit is found as a panache giving a decreased in the propagation delay. Our motive is to reduce the propagation delay and to achieve this we place a number of Repeaters in a long interconnect wire and also uses the driver-interconnect-load (DIL) employing CMOS driver. There is an occurrence of tradeoff between propagation delay and power consumed, because propagation delay value decreases but power consumption gets increased, so, an optimum value of repeaters is taken. The repeaters used in the distributed circuit are the CMOS devices, these distributed circuit also provides a good analysis of the RLC interconnect.

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LIST OF SYMBOLS

N	Number of shells in MWCNT
D_i	Diameter of ith shell
D	Separation between two adjacent shells
N_i	Number of conducting channels in i^{th} shell
Λ	Electron mean free path
L	Length of interconnect
H	Planck's constant
E	Electron charge
H	Separation between ground plane and center of MWCNT
μ	Permeability
ε	Permittivity
W	Width of interconnect
ρ	Resistivity of copper
T	Thickness of interconnect
t_{ox}	ILD thickness (height of interconnect from ground plane)
s	Separation between interconnects
μ_n	Mobility of electron
C_{ox}	Oxide capacitance
V_{DD}	Positive supply voltage
L	Channel length
W	Channel width

ABBREVIATIONS

VLSI	Very Large Scale Integration
CNT	Carbon Nanotube
IC	Integrated Circuit
SWCNT	Single Wall Carbon Nanotube
MWCNT	Multi Wall Carbon Nanotube
CMOS	Complementary Metal Oxide Semiconductor
RLC	Resistance, Inductance and Capacitance
DIL	Driver Interconnect Load
MFP	Mean Free Path
SPICE	Simulation Program with Integrated Circuit Emphasis
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
ITRS	International Technology Road map for Semiconductors
Cu	Copper
PDP	Product of Delay and Power

CHAPTER

1

INTRODUCTION TO VLSI INTERCONNECTS

1.1 Introduction

Interconnects are a conducting material which provides electric connection between components on a VLSI chip and to connect these chips, so basically interconnects are wires. At present, interconnection plays most significant role in determining the size, power consumption and clock frequency of digital system. A VLSI interconnect plays an important role in deep submicron technology because in deep submicron technology interconnect can no longer be act as a simple resistor.

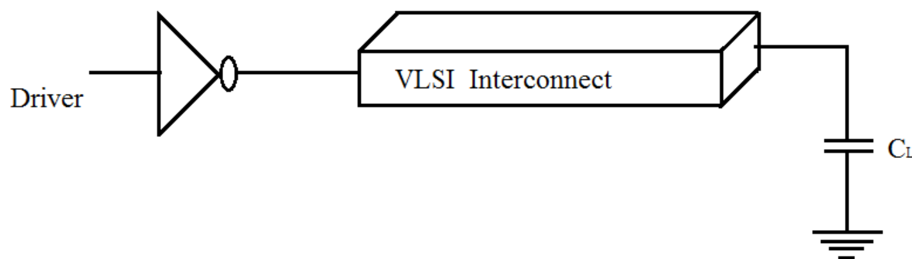

Fig. 1.1: VLSI Interconnect

The associated parasitic such as inductance and capacitance are also need to be considered in deep submicron technologies. These parasitic introduces delay in a propagating signal through interconnects. As the chip size growth increase due to increase in complexity and functionality, the capacitance and resistance of interconnect wires quickly increases. With the advancement in technology node, the feature size of ICs has been shrinking to improve the propagation delay, power consumption, silicon area and cost characteristics. The effect of technology scaling in VLSI interconnect is in the form of increased density. This increased density results in the increasing of the coupling effect. Interconnect plays a very important role in the performance of a high-speed chip and also used to connect the different macro cells within a VLSI chip [1].

1.2 Types Of Interconnects

1.2.1 Copper Interconnects

Copper based chips are semiconductor integrated circuits, usually micro-processors, which use copper for interconnections. Since copper is a better conductor than aluminum, chips using this technology can have smaller metal components, and use less energy to pass electricity through them. Together, these effects lead to higher-performance processors [2].

1.2.2 Optical interconnects

Optical interconnect is a way of communication by optical cables. Optical wires are capable of high bandwidth. Optical interconnects have negligible frequency dependent loss, low cross talk and high band width. Optical interconnects are not much used commercially since optical interconnects technology is incompatible with manufacturing processes and assembly methods that are currently used in the semiconductor industry [3].

1.2.3 Carbon Nanotube Interconnects

Carbon nanotubes are the allotropes of carbon with cylindrical nanostructure. Nanotubes have been constructed with length-to-diameter ratio of up to 132,000,000:1. They have extraordinary thermal conductivity and mechanical and electrical properties. Nanotubes are the member of the fullerene family. Nanotubes are categorized as single-walled nanotubes (SWCNTs) and multi-walled nanotubes (MWCNTs). On the basis of Chirality CNT are classified as armchair, zigzag and chiral [4].

1.3 Carbon Nanotube

CNTs are known as allotropes of carbon and made by rolling up a sheet of graphene into a cylinder. Graphene is a monolayer sheet of graphite in which carbon atoms are arranged in a honeycomb lattice structure. Graphene is stronger than diamond which makes graphene the strongest material. CNTs have not only unique atomic arrangement but also interesting physical properties; including current carrying capability, long ballistic transport length, high thermal conductivity, and mechanical strength. These remarkable properties make CNTs one of the most promising research materials for future VLSI technology [1].

1.4 Classification of Carbon Nanotubes (CNT)

CNT can be classified in three categories as follow

1.4.1 Based on layers

1.4.1.1 Single-walled carbon nanotube (SWCNT)

Single Wall carbon nanotubes are madeby rolling up a sheet of graphene into a cylinder, as shown in Fig. 1.2.

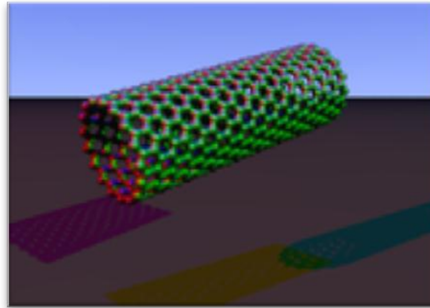

Fig. 1.2: Single-wall Carbon nanotube [4]

1.4.1.2 Multi-walled carbon nanotube (MWCNT)

Multiwall CNT are made by rolling up two or more concentric graphene sheets, as shown in Fig. 1.3.

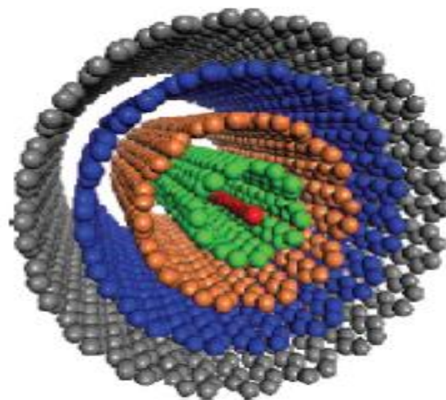

Fig. 1.3: Multi-walled Carbon nanotube [4]

1.4.1.3 Difference between MWCNT and SWCNT

The main difference between SWCNT and MWCNT arises from number of concentrically rolled up graphene sheets. For SWCNTs, only one rolled up grapheme sheet is there whereas for two or more concentrically rolled up graphene sheets, CNTs

are known as MWCNT. SWCNT bundle is formed by packing together a large number of SWCNTs in a bundle form. The parasitic elements of SWCNT bundle and MWCNTs depend on number of metallic SWCNTs in the bundle and number of shells in the MWCNTs. It is very difficult to achieve ballistic transport for MWCNTs for a long length whereas SWCNTs have mean free path of the order of a micron due to its diameter in nano range [1]. SWCNTs has only one shell with diameter ranging from 0.33nm to 5.0nm and lengths from 2nm to 10nm, whereas MWCNTs has several concentric shells with diameter ranging from several nanometers to tens of nanometers and length of several microns [6].

1.4.2 Based on chirality

Structure of CNTs depends on chiral indices i.e., the rolling up direction of a grapheme sheet. Depending on the chiral indices (n, m), CNTs can get their unique armchair or zigzag structures.

1.4.2.1 Zigzag CNT

For zigzag CNTs, it is n or m = 0 as shown in Fig. 1.4. These are either metallic or semiconducting in nature depending on their chiral indices.

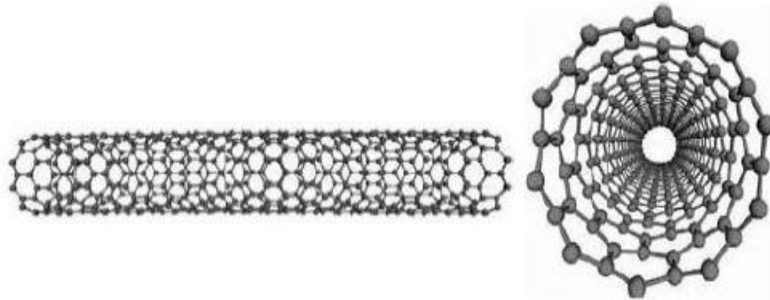

Fig. 1.4: Zigzag (n,0) CNT [47]

1.4.2.2 Armchair CNT

For armchair CNTs, the chiral indices is defined by n = m as shown in Fig. 1.5. The armchair CNTs are always metallic.

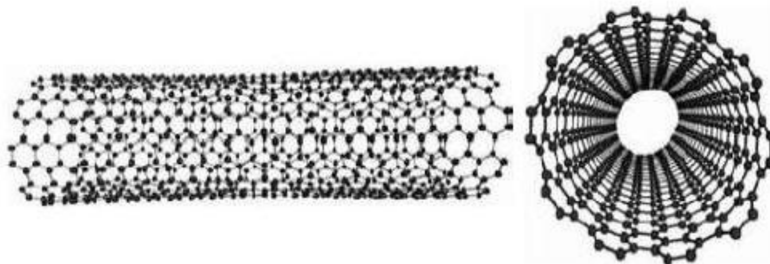

Fig. 1.5: Armchair (n,n) CNT [47]

1.4.2.3 Chiral CNT

For other values of n and m, CNTs are known as chiral as in Fig. 1.6.

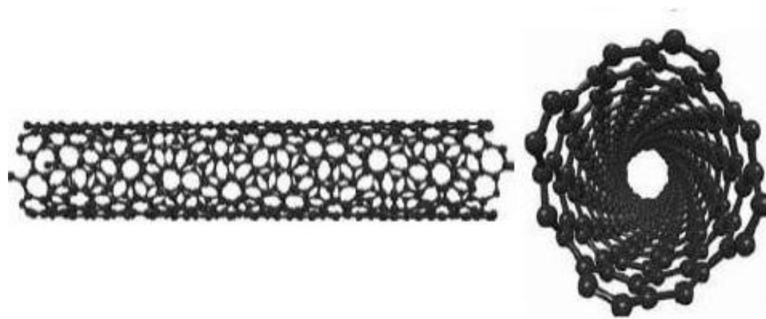

Fig. 1.6: Chiral (n,m) CNT [47]

1.4.3 Based on conductivity:

Depending upon their different structures, CNTs can exhibit both metallic and semiconducting properties. By satisfying the condition n – m =3i (where i is an integer), the armchair CNTs are always metallic and zigzag CNTs are either metallic or semiconducting in nature depending on their chiral indices. Statistically, a natural mix of CNTs will have 1/3rd of metallic and 2/3rd of their semiconducting chirality. These unique structures of CNTs basically depend on the rolling up directions of graphene sheet. Each shell of MWCNT can have different chiralities depending on the direction they are rolled up, which implies that the shells in MWCNT are metallic or semiconducting [7].

1.5 Repeaters in VLSI

Due to the domination of interconnect delay on gate delay in the deep sub micrometer VLSI circuits there is an increase in the delay. Repeaters are often used to minimize the delay to propagate a signal through the interconnect lines. The continuous scaling of technology and increased die area, the interconnect delay continues to increase. In order to properly design complex circuits, more accurate interconnect models and signal propagation characterization are required. To conquer this difficulty the repeaters are used in which the interconnect lines are best modeled as an RC impedance.

Interconnect has been modeled as a single lumped capacitance in the analysis of the performance of on-chip interconnects. The cross-sectional area of wires has been scaled down while interconnect length has increased due to the scaling of technology and increased chip sizes. The resistance of interconnect has increased in significance,

requiring the use of more accurate RC delay models. Many design techniques have therefore been developed to minimize the propagation delay of global interconnect.

Currently, inductance is becoming more important with faster on-chip rise times and longer wire lengths. Wide wires are frequently encountered in clock distribution networks and in upper metal layers. These wires are low resistive wires that can exhibit significant inductive effects. Furthermore, increasing performance requirements are pushing the introduction of new materials for low resistance interconnects. In the limiting case, high temperature superconductors may become commercially available. With these trends it is becoming more important to include inductance when modeling on-chip interconnects. We also want to provide an accurate estimation of the propagation delay of nonlinear CMOS gates driving distributed RLC lines as well as to develop design expressions for optimum repeater insertion to minimize the propagation delay of a distributed RLC line. The work also aims to highlight the relative effect of increasing inductance on design techniques traditionally used to optimize the propagation delay of on-chip interconnect [8].

A driver-interconnect-load (DIL) system shown in Fig. 1.7, employing CMOS driver is used to calculate the delay.

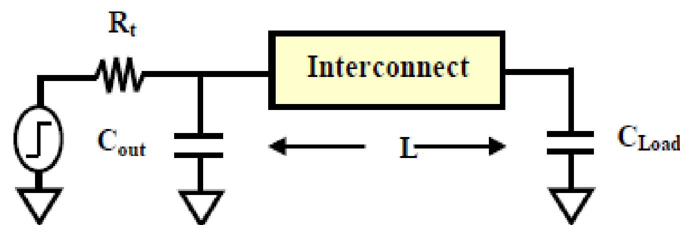

Fig. 1.7: Schematic of Driver-interconnect-load (DIL) circuit [7].

Here R_t and C_{out} are the equivalent output resistance and capacitance of the gate driver respectively and C_{load} is the input capacitance of the load gate. For accurate estimation of delay, CMOS inverter is used instead of a simple resistive driver. The reason behind is that a transistor in a CMOS gate operates partially in linear region and partially in saturation region during switching. But, a transistor can be accurately approximated by a resistor only in the linear region. In the saturation region, the transistor is more accurately modeled as current source with a parallel high resistance. The insertion of repeaters is used to minimize the interconnect response time by mitigating the effect of resistance and capacitance [9].

1.6 Applications

- **Bulk nanotube:** Current use and application of nanotubes has mostly been limited to the use of bulk nanotubes, which is a mass of rather unorganized fragments of nanotubes. Bulk nanotube materials may never achieve a tensile strength similar to that of individual tubes, but such composites may, nevertheless, yield strengths sufficient for many applications.

  Bulk carbon nanotubes have already been used as:

  - Composite fibers: These are used in polymers to improve the mechanical, thermal and electrical properties of the bulk product.
  - Tissue engineering: carbon nanotubes can act as scaffolding for bone growth [4].

- **For small circuit delays:** For applications requiring small circuit delays, MWCNT interconnects should be used due to smaller capacitances.

- **Replacement for Copper:** Applications requiring large transmission efficiency and low reflection losses, CNT bundles should be used for interconnects since the numbers of conducting channels per shell are more in SWCNTs bundle than the number of conducting channels per shell in MWCNT of the same size. This suggests that MWCNT and SWCNT bundle can replace Copper as interconnection wires in next generation of VLSI integrated circuits [5].

- **Other versatile applications:** In the area of nanoelectronics, CNTs show their prospects as energy storage devices (such as super capacitors), energy conversion devices (including thermoelectric and photovoltaic devices), field emission displays and radiation sources, nanometer semiconductor transistors, nanoelectromechanical systems (NEMS), electrostatic discharge (ESD) protection , as well as interconnects and passives[1].

The extraordinary physical properties of CNTs make them exciting prospects for a variety of applications in microelectronics/nanoelectronics, spintronics, optics, material science, mechanical and biological fields.

CHAPTER 2

LITERATURE REVIEW

Manoj Kumar Majumder *et al.* [1] proposed a comprehensive analysis of propagation delay for both MWCNT and SWCNT bundles at different interconnect lengths and shows a comparison of equivalent number of SWCNTs in bundle and shells in MWCNTs for specified propagation delays and lengths. In their paper, models for MWCNT and SWCNT bundle interconnects are reviewed on the basis of one-dimensional fluid theory. These models are compared at 32 nm technology nodes in terms of propagation delay. It has been observed that irrespective of the type of CNTs, propagation delay increases with interconnect lengths. For same propagation delay performance, the number of SWCNTs required in a bundle are found to be more than number of shells in MWCNT for a given interconnect length.

Hong Li *et al*. [6] presented for the first time, a detailed investigation of MWCNT based interconnect performance. He also explored the applicability of MWCNTs as an interconnect candidate in future design of integrated circuits. With large diameter, each shell in MWCNT has long MFP and contributes to the conductance, even if the shell is of semiconducting chirality. A compact equivalent circuit model of MWCNTs is presented for the first time, and the performance of MWCNT interconnects is evaluated and compared against traditional Copper interconnects, as well as Single-Walled CNT (SWCNT) based interconnects, at different interconnect levels for future technology nodes. It is shown in their paper, that at the intermediate and global levels, MWCNT interconnects can achieve smaller signal delay than that of Copper interconnects and the improvements become more significant with technology scaling and increasing wire lengths. On the other hand, since MWCNTs are easier to fabricate with less concern about the chirality and density control. The applicability of MWCNTs as an interconnect candidate in future design of integrated circuits has been explored theoretically in this paper. With large diameter, each shell in MWCNT has long MFP and contributes to the conductance, even if the shell is of semiconductor chirality. A comprehensive equivalent

distributed circuit model has been presented, based on which the performance of MWCNT interconnect has been evaluated and compared with that of Copper interconnects as well as SWCNT interconnects.

Ashok Srivastava *et al*. [5] presents models for CNT interconnects, which include SWCNT, MWCNT and SWCNT bundle are discussed based on one-dimensional fluid theory. The one-dimensional fluid model can be applied to CNT interconnects using low resistance contacts in current low-voltage nanometer CMOS technologies. MWCNT and SWCNT bundle interconnects exhibit higher transmission efficiency and lower reflection losses, smaller delays and less power dissipations. This is mainly due to larger conductivity of MWCNT and SWCNT bundle, proportional to the number of conducting shells in MWCNT and conducting SWCNTs, respectively. With no special separation techniques, the metallic nanotubes are distributed with probability $\beta = 1/3$. The delays in MWCNT and SWCNT bundle interconnects can be further decreased with increase in β and approaching to 1. It is also noticed that with the increase in interconnection length, the delay of Copper interconnect increases faster than that of MWCNT and SWCNT bundle interconnects. For application requiring small circuit delays MWCNT interconnects should be used due to smaller capacitance. Application requiring large transmission efficiency and low reflection losses, CNT bundles should be used for interconnects since the numbers of conducting channels per shell are more in SWCNTs bundle than the number of channels per shell in MWCNT of the same size. These finding suggest MWCNT and SWCNT bundle can replace Copper as interconnection wires in next generation of VLSI integrated circuits.

Yograj Singh Duksh *et al.* [7] proposed the effect of driver size and number of shell on propagation delay for MWCNT interconnect at 22nm technology node. An equivalent circuit model of MWCNT was used for estimation and analysis of propagation delay. The delay through MWCNT and Copper interconnects are compared for various driver sizes and number of MWCNT shells. The MWCNT interconnect has lower propagation delay than Copper interconnects. Furthermore it is also observed that as the size of driver or number of shells in MWCNT increases the propagation delay through it reduces. To elaborate it can be said that in all the cases, the propagation delay of MWCNT interconnect is less than the Copper interconnect at global level for a particular driver size.

Yehea Ismail *et al.* [8] proposed a closed form expression for the propagation delay of a CMOS gate driving a distributed RLC line is introduced that is for a wide range of RLC loads. This expression is based on the alpha power law for deep sub micrometer technologies. It is shown that the error in the propagation delay if inductance is neglected and interconnects is treated as a distributed RC line can be over 30% for present on-chip interconnects. The closed form CMOS delay model is applied to the problem of repeater insertion in RLC interconnect. Closed form solutions are presented for inserting repeaters into RLC lines that are highly accurate with respect to numerical solutions. It is shown that large errors in the repeater design process are encountered if inductance is neglected. The error between the RC and RLC models increases as the gate parasitic impedances decrease. Thus, the importance of inductance in high performance VLSI design methodologies will increase as technologies scale.

Pankaj Kumar Das *et al.* [9] proposed a modeling approach for different bundled CNT structures. Based on the arrangements of single and multi-walled CNTs in bundle, two different structures of mixed CNT bundles (MCBs) are proposed. Performance in terms of propagation delay is compared between different bundled CNT structures by using driver-interconnect-load (DIL) system. They observed that the overall reduction in delay is in the range of 22.33% to 56.87% for bundled MWCNT with respect to other CNT structures at global interconnect lengths. They also observed that the propagation delay primarily depends on interconnect parasitic that can be determined using bundle geometry. On an average, the propagation delay is improved by 63.89% for bundle MWCNT with respect to MCB-I structure containing equal halves of horizontally located SWCNTs and MWCNTs.

Hui Li *et al.* [12] studied the electric transport properties of an individual vertical mult-wall carbon nanotube at room temperature in a scanning electron microscope chamber. They found that the single MWCNT has a large current carrying capacity, and the maximum current can reach 7.27mA. At the same time, a very low resistance of about 34.4Ω and high conductance of about 460-490G were obtained. The experimental observation imply a multichannel quasi ballistic conducting behavior occurring in the MWCNTs with large diameter, which can be attributed to the participation of the multiple walls in electric transport and the large diameter of the MWCNTs.

Nisarg D. Pandya *et al.* [19] proposed a new modeling approach for mixed carbon nanotube (CNT) bundle (MCB) interconnects. An accurate modeling hierarchy has been proposed for MCB structures. Bundled single-walled CNTs (SWCNTs) and multi-walled CNTs (MWCNTs) have been modeled as equivalent single conductor (ESC) transmission lines and then combined to form a MCB interconnect. This MCB interconnect is basically a multiple single conductor model. By considering different arrangements of SWCNT and MWCNT in mixed CNT bundle, performance is analyzed for two different MCB structures in terms of propagation delay, crosstalk delay and power dissipation.

Luigi Egiziano *et al.* [20] proposed the performances of the SWCNT bundles have been analyzed in order to consider their possible use for the future next generation interconnects on intermediate and global level. First, they have shown that the unknown distribution of metallic CNT in the densely-packed arrays may affect the high-frequency behavior of the interconnects. Accounting for realistic terminations, CNT bundles have shown performances better than those obtained for ideally scaled Copper interconnects. The presence of repeaters rise the maximum frequency allowed for the input signals. The effect of high parasitic contact resistance between CNT bundle and lumped circuit elements might constitute a bottleneck for the effectiveness of repeaters insertion.

Azad Naeemi *et al.* [21] presented compact physical models derived for the number of conduction channels in MWCNTs and SWCNT bundles as well as their conductivities. For MWCNTs with diameters larger than 6nm, there was a critical length at which conductivity becomes independent of diameter. For nanotubes shorter than the critical length, increasing the diameter lowers the conductivity, whereas for nanotubes longer than that, increasing the diameter increased conductivity. This is because for long nanotubes, electron MFP, which increases linearly with diameter, is important, whereas for short nanotubes, quantum resistance and the total number of conduction channels per unit area are the key parameters. For long lengths, MWCNTs can have conductivities several times larger than that of Copper or SWCNT bundles. For short lengths (< 10 μm), however, dense SWCNT bundles offered more than two times higher conductivities compared to MWCNTs.

Kyung-Hu Koo *et al.*[22] found that for local interconnects, the CNT bundle shows lower latency than Copper. Moreover, CNT bundle's performance advantage can be further amplified by leveraging its superior EM properties and reducing the wire AR

(aspect ratio). This reduces wire capacitance, which dominates delay instead of wire resistance. They quantified these advantages by plotting the optimum latency as well as the optimum AR for all technologies. For global wires, they used proper inductance, resistance, and capacitance modeling as well as optical link optimizations to compare latency, power density/energy efficiency, and bandwidth density of Copper, CNTs, and optical wires. They found optical wires to be superior, particularly for longer links. For shorter semi global links, they yield comparable latency to CNT, particularly at 22nm node.

Yograj Singh Duksh *et al.*[23] analyze the effect of driver size and number of shells on propagation delay and power for multi-walled carbon nanotubes (MWCNT) interconnect at 22nm technology node. The SPICE simulation results show that the MWCNT interconnect has lower propagation delay than Copper interconnects. The delay ratio of MWCNT to Copper decreases with increase in length for different driver size and number of MWCNT shells. However, the delay ratio increases with reduction in number of MWCNT shells. The ratio of average power consumption (MWCNT/Copper) also decreases with the variation in driver size and numbers of shells with respect to the length of interconnect. The theoretical study proves CNTs to be better alternatives against Copper on the ground of performance parameters.

Manoj Kumar Majumder *et al* [24] proposed that Multi-walled carbon nanotubes with higher number of shells have potentially provided attractive solution in propagation delay and power dissipation. Their research paper presents an equivalent single conductor model of MWCNT interconnects that is well accurate with any number of shells and distance from ground plane. Using the equivalent single conductor model, HSPICE circuit simulations have been performed for different number of shells in MWCNTs. Based on the simulation results, approximate number of shells have been calculated for optimized delay and power performance at global interconnect lengths. It has been observed that the overall delay is improved by 64.33% for higher number of shells as compared to the lower one. Therefore, MWCNTs with higher number of shells can be predicted as more appropriate candidate for future global VLSI interconnects.

Manoj Kumar Majumder *et al* [26] proposed that Multi-walled carbon nanotubes have provided potentially attractive solution over single-wall carbon nanotube bundle at current very large scale integration (VLSI) technologies. Their paper presents a

comprehensive analysis of propagation delay for both MWCNT and SWCNT bundle at different interconnect lengths (global) and shows a comparison of equivalent number of SWCNTs in bundle and shells in MWCNTs for specified propagation delays and lengths. They observed that irrespective of the type of CNTs, propagation delay increases with increases with interconnect lengths. For some propagation delay performance, the number of SWCNTs required in a bundle are found to be more than number of shells in MWCNT for a given interconnect length. Also MWCNTs are more promising candidate than SWCNT bundle in terms of area for certain specified propagation delay and interconnect length in modern VLSI technology.

H. B. Bakoglu *et al* [27] proposed that the propagation delay of interconnection line is a major factor in determining the performance of VLSI circuits because the RC time delay of these lines increases rapidly as chip size is increased and cross-sectional interconnection dimensions are reduced. They developed a model for interconnection time delay that includes the effects of scaling transistor, interconnection and chip dimensions. The delays of aluminum and poly silicon line are compared and propagation delays in future VLSI circuits are projected. Properly scaled multilevel conductors, repeaters, cascaded drivers and cascaded driver/repeater combinations are investigated as potential methods for reducing propagation delay. Their model yields optimal cross-sectional interconnection dimensions and driver/repeater configurations that can lower propagation delays by more than an order of magnitude in MOSFET circuits.

Brajesh Kumar Kaushik *et al* [28] deals in crosstalk analysis of a CMOS-gate-Driven capacitively and inductively coupled interconnect. Alpha power-law model of MOS transistor is used to represent a CMOS driver. This is combined with a transmission-line-based couple interconnect model to develop a composite driver-interconnect-load model for analytical purposes. On this basis, a transient analysis of crosstalk noise is carried out. Comparison of the analytical results with SPICE extracted results shows that the average error involved in estimating noise peak and their time of occurrence is less than 7%.

CHAPTER

MWCNT AND COPPER STRUCTURE AND EQUIVALENT ELECTRICAL MODEL

3.1 Introduction

Recently, some researchers have addressed the issue for implementation of MWCNT based interconnects considering their complexity in both structure and characterization [6, 10]. Interestingly, it has been found that multiple shells in an MWCNT can contribute to conductance if proper end contacts can be made. In [11, 12] properly contacted MWCNTs have been implemented to achieve low resistance with the contribution of inner shells [7].

An isolated MWCNT on an infinite ground plane is shown in Fig. 3.1 [6]. The separation between the ground plane and the multi-walled center is H. D_{max} and D_{min} are the outermost and innermost shell's diameter respectively as shown in Fig. 3.1. The separation between two adjacent shells is d ≈ 0.34 nm, which is the vander Waals gap.

3.2 Number of Shells for MWCNT

The number of shells are counted from outer to inner as 1,2…i… n. The ratio (D_{min}/D_{max}) is equal to 1/2 [12]. Thus, the number of shells n of the MWCNT is

$$n = 1 + \mathrm{int}\left[\frac{D_{max} - \frac{D_{max}}{2}}{2d}\right] \tag{3.1}$$

where "int [.]" indicates that only the integer part is taken into account. The diameter of the i_{th} shell is given by [6]

$$D_i = D_{max} - 2d.(i-1), \qquad \text{for } 1 \le i \ge n \tag{3.2}$$

The innermost diameter is in Fig. 3.1 [7]

$$D_{min} = D_{max} - 2d.(n-1) \tag{3.3}$$

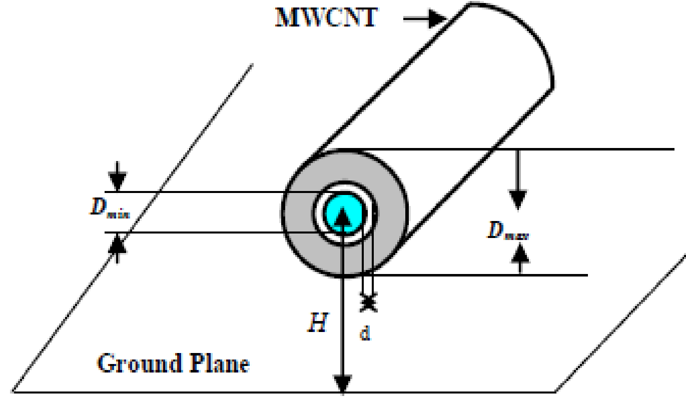

Fig. 3.1: MWCNT structure on a ground plane [7]

Note that the ratio of D_{min}/D_{max} is assumed to be ½, D_{min} may be large than $D_{max}/2$ because D_{max} may not be an integer multiple of d.

3.3 Number of channels for MWCNT

The number of conducting channels for each shell [6] is

$$N_{chan/shell} = \sum_{subbands} \frac{1}{\exp(|E_i - E_F|/K_B T) + 1} \tag{3.4}$$

where E_i, is the highest (or lowest) value for the sub-bands below (or above) the Fermi level E_F. K_B and T are the Boltzmann constant and absolute temperature respectively. The number of channels per shell [21] can be approximated to

$$N_{chan/shell}(D) \approx a.D + b \tag{3.5}$$

where D is the shell diameter, a= $0.0612 nm^{-1}$, and b=0.425. The error obtained by approximated form of (3.4), due to different chiralities, is less than 15% for all values of D. The number of conducting channels of the ith shell is given by [6]

$$N_i = a.D_i + b \tag{3.6}$$

Hence, the total number of conducting channels is given by the sum of the conducting channels (N_i) of all the shells. It is note that equations (3.4) and (3.5) are applicable for small voltages, which is valid for interconnect applications [6].

3.4 Individual shell model

The equivalent circuit model for an individual shell of an MWCNT can be obtained on the basis of the model of SWCNT [6], which is shown in Fig. 3.2.

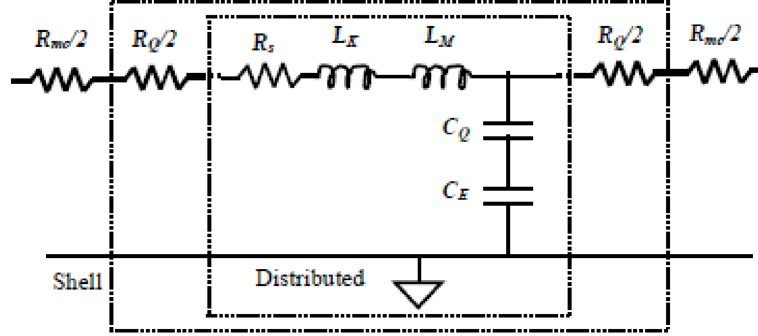

Fig. 3.2: Equivalent circuit model of an individual shell [7]

3.4.1 Resistance

The shell resistance of an MWCNT consists of three parts: quantum contact resistance R_Q, scattering induced resistance R_S and imperfect contact resistance R_{mc}. Scattering induced resistance occurs only when the length of nanotube (shell) is larger than the electron mean free path (MFP). R_Q and R_S are intrinsic and R_{mc} is due to fabrication process. The total shell resistance [6] is given by

$$R_{shell} = R_Q + R_S.L = \frac{h}{2e^2N} + \frac{h}{2e^2N}\frac{L}{\lambda} \quad (3.7)$$

where $h/2e^2 = 12.9k\Omega$, and L, λ and N ($N = a.D + b$) are the length, MFP and number of conducting channels of the shell respectively. The imperfect contact resistance R_{mc} can range from zero to hundreds of kilo-ohms for different growth process. Recently, it has been observed that R_{mc} in MWCNT could be very small compared to the total resistance [11, 12]. It can be observed from equation (3.7) that the value of MFP plays an important role in determining the resistance of the nanotube. It has been proven that the MFP of metallic nanotube is directly proportional to the shell diameter (D). The MFP for metallic MWCNT [12, 14] at room temperature is

$$\lambda = 1000.D \quad (3.8)$$

3.4.2 Inductance

There are the two types of inductances for MWCNT i.e. the magnetic and kinetic inductances per unit length [13] of a shell are given by

$$L_{magnetic} = (\mu/2\pi).\cosh^{-1}(2H/D) \quad (3.9)$$

$$L_{K/channel} = h/2 \times 2e^2 v_F \approx 8nH/\mu m \quad (3.10)$$

$$L_{K/shell} = L_{K/channel}/N \quad (3.11)$$

The total kinetic inductance ($L_{K/shell}$) may decrease from 13 to 1 nH/µm for 3nm<D<100nm and the magnetic inductance ranges from 0.2 to 1.2 pH/µm for 1< H/D<100, which is much smaller than the kinetic inductance. Therefore, the magnetic inductance has been neglected in this.

3.4.3 Capacitance

The capacitance of the MWCNT consists of two parts: quantum capacitance C_Q and electrostatic capacitance C_E. The quantum capacitance per unit length of a shell is given by [13]

$$C_{Q/channel} = 2 \times 2e^2/hv_F \approx 193aF/\mu m \quad (3.12)$$

$$C_{Q/shell} = C_{Q/channel}.N \quad (3.13)$$

The electrostatic capacitance between a MWCNT and a ground plane is given by [13].

$$C_E = \frac{2\pi\mathcal{E}}{\ln\left(\frac{H}{D}\right)} \quad (3.14)$$

The circuit parameters of different shells vary in MWCNT and the potentials of different shells cannot be assumed to be equal as in the case of SWCNT bundles, which induces shell-to-shell capacitive coupling. This coupling capacitance is similar to electrostatic capacitance and will be very large due to the small separation between two adjacent shells. The shell-to-shell capacitance per unit length (C_S) [6] can be obtained by using coaxial capacitance formula.

$$C_S = \frac{2\pi\varepsilon}{\ln(D_{out}/D_{in})} = \frac{2\pi\varepsilon}{\ln[D_{out}/D_{out}-2d]} \quad (3.15)$$

where D_{out} and D_{in} are the outer and inner diameters of adjacent coaxial shells respectively and d = 0.34nm. The intershell tunneling conductance per unit length [6, 15] is

$$G_T = \sigma\,\pi\,D \quad (3.16)$$

where σ is normalized tunneling conductivity at d = 0.34 nm. The tunneling conductance is proportional to the shell diameter because there are more atoms in a larger diameter shell and thus tunneling is more likely to take place.

The magnetic coupling between the shells in an MWCNT is another effect. Each shell of MWCNT can be treated as an ideal sheet cylinder with zero thickness due to its large diameter and small thickness. The mutual inductance per unit length between different shells can be written from the equations in [6] as

$$M_{shells} = \frac{\mu}{2\pi}\left(\ln\frac{4l}{D_{out}} - 1 + \frac{D_{out}+D_{in}}{\pi L}\right) \quad (3.17)$$

The mutual inductance between shells can be determined from (3.17), which is around 2pH/μm and is therefore much smaller than the kinetic inductance of each shell (of the order of nH/μm). Hence, mutual inductance is neglected.

Based on the aforementioned parameters, an equivalent distributed circuit model for MWCNT interconnect is shown in Fig. 3.3 [6]. The quantum capacitance C_Q is in series with electrostatic capacitance (including shell-to-shell capacitance C_S and ground capacitance C_E) [6, 13]. Note that only one total ground capacitance C_E is shown in Fig. 3.3. For shell to-shell capacitance and tunneling, only neighboring shells are involved. Therefore, for n shells, there is only 'n-1' number of C_S and G_T (intershell tunneling conductance per unit length). The equivalent model in Fig. 3.3 can be employed for circuit simulation using SPICE.

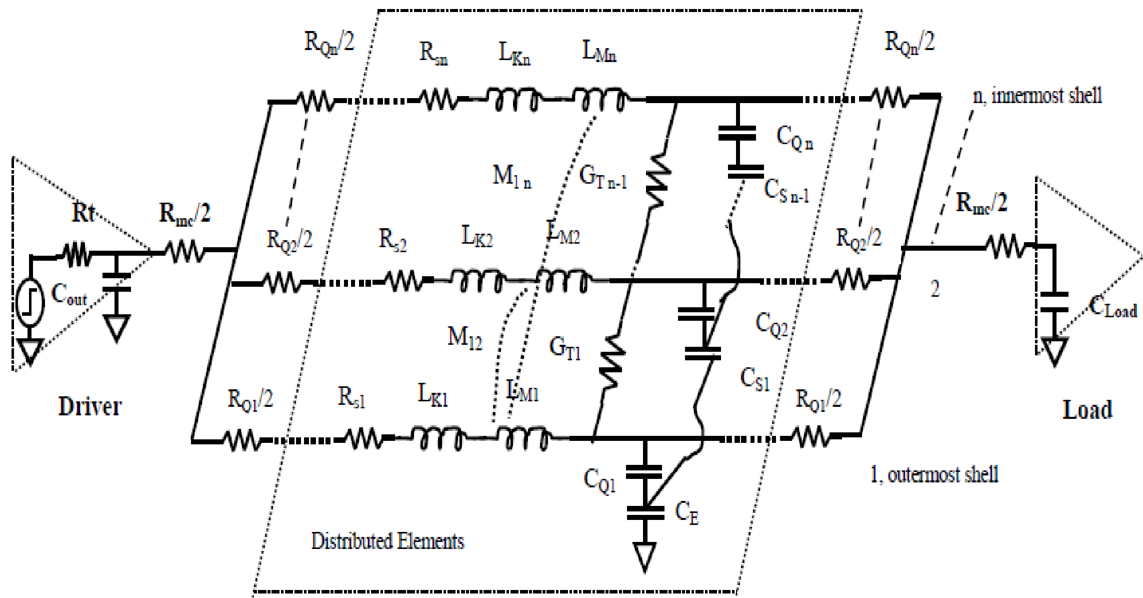

Fig. 3.3: Equivalent distributed circuit model of an MWCNT with n shells [7]

3.5 Equivalent circuit model of Copper

Equivalent circuit model of Copper interconnect is shown in Fig. 3.4. Where Req is equivalent resistance of Copper interconnect, Leq is equivalent inductance of Copper interconnect and Ceq is equivalent capacitance of Copper interconnect.

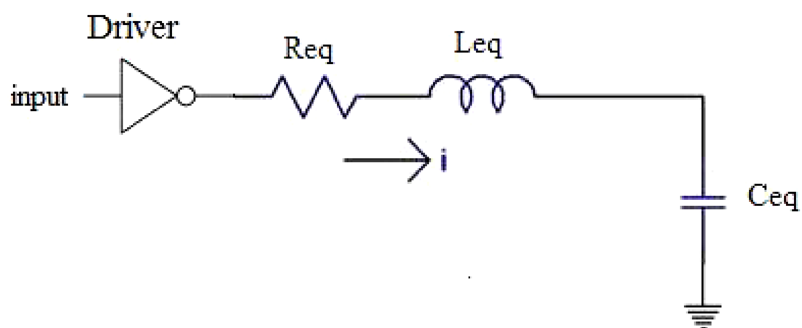

Fig. 3.4: Equivalent circuit model of Copper interconnect

According to the model, the thickness of interconnect is t, the width of interconnect is w, t_{ox} is the height of interconnect above the ground plane and s is the separation between interconnects as shown in Fig. 3.5. All interconnect parameters used in simulation are obtained from ITRS 2008[16].

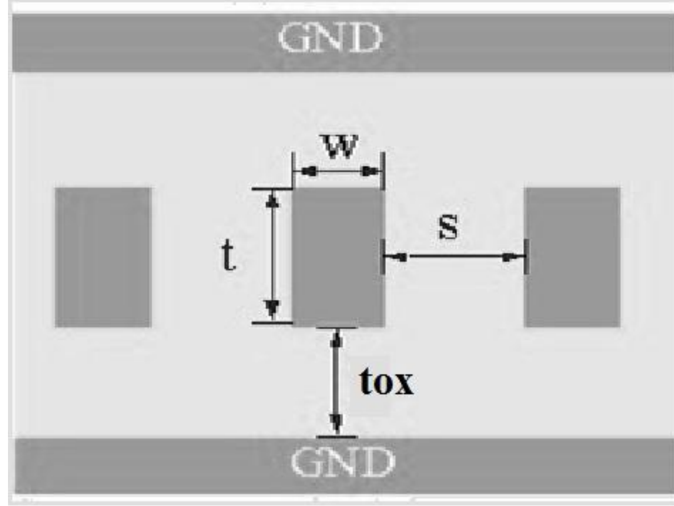

Fig. 3.5: Schematic diagram of Copper interconnects

3.5.1 Equivalent Resistance

Based on this model, the resistance of Copper interconnects of length l is given by following equation:

$$R_{eq} = \frac{\rho l}{wt} \quad (3.18)$$

where ρ is the resistivity of copper, w is the width and t is the thickness.

3.5.2 Equivalent Capacitance

The equivalent capacitance is given by

$$C_{eq} = 2C_g + 2C_c \quad (3.19)$$

where C_g is ground capacitance and C_C is coupling capacitance as shown in Fig. 3.6. Now mathematical representation of ground capacitance is as

$$C_g = \mathcal{E}\left[\frac{w}{t_{ox}} + 2.04\left(\frac{s}{s+0.54\,t_{ox}}\right)^{1.77}\left(\frac{t}{t+4.53\,t_{ox}}\right)^{0.07}\right] \quad (3.20)$$

where t_{ox} is the height of interconnect from ground plane and s is the separation between two interconnects.

And coupling capacitance is represented mathematically as

$$C_C = \mathcal{E}\left[\,1.41\frac{t}{s}e^{\left(-\frac{4s}{s+8.01\,t_{ox}}\right)} + 2.37\left(\frac{w}{w+0.31s}\right)^{0.28}\left(\frac{t_{ox}}{t_{ox}+8.96s}\right)^{0.76}e^{\left(-\frac{2s}{s+6\,t_{ox}}\right)}\right] \quad (3.21)$$

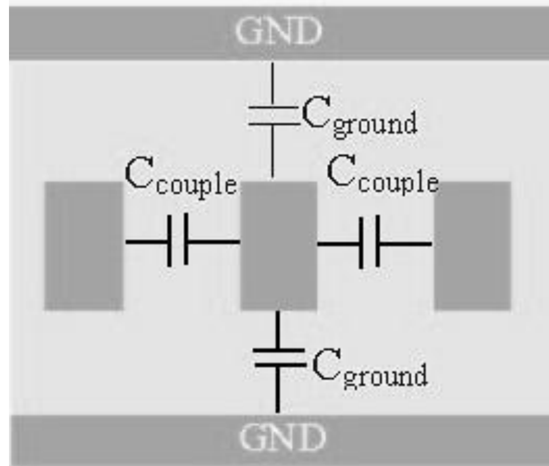

Fig. 3.6: The different capacitance with copper interconnects

where ε is dielectric permittivity which is equal to $\varepsilon_0 \times \varepsilon_r$, where ε_r is relative permittivity and ε_0 is vacuum permittivity which is equal to 8.854×10^{-12} F/m.

3.5.3. Equivalent Inductance

The equivalent inductance is given by

$$L_{eq} = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{(w+t)}\right) + \frac{1}{2} + \frac{0.22(w+t)}{l}\right] \tag{3.22}$$

where μ_0 is permeability of free space and $\mu_0 = 4\pi \times 10^{-7}$ H/m.

CHAPTER 4

VARIATION OF RLC IN MWCNT AND COPPER INTERCONNECTS

In the last chapter the equivalent circuit of an interconnect in MWCNT and Copper was studied. Any type of interconnect can be studied by representing its equivalent circuit (the value of RLC is known from this circuit) and the delay can be calculated. This chapter encompasses the calculation of resistance, capacitance and inductance in MWCNT and Copper interconnects shown in the tables and their variation is also studied from the graphs.

4.1 Resistance

The value of resistance is calculated in kΩ for MWCNT interconnects using equations (3.6), (3.7), (3.8) and for Copper interconnects using equation (3.18). Table 4.1 shows the values of resistance for MWCNT and Copper interconnect for different length varying from 100um to 1000um and for different technology nodes i.e. 16nm, 22nm and 32nm.

Table 4.1: Resistance comparison of MWCNT and Cu interconnect for different length and for different Technology nodes i.e. 16nm, 22nm and 32nm

Resistance in kΩ						
Length (μm)	**For 16nm**		**For 22nm**		**For 32nm**	
	MWCNT	**Cu**	**MWCNT**	**Cu**	**MWCNT**	**Cu**
100	5.0403	14.3359	1.8135	6.2087	0.7331	2.3584
200	9.5228	28.6719	3.3504	12.4174	1.3192	4.7168
300	14.0046	43.0078	4.8868	18.6260	1.9050	7.0752
400	18.4862	57.3438	6.4232	24.8347	2.4907	9.4336
500	22.9677	71.6797	7.9595	31.0434	3.0764	11.7920
600	27.4492	86.0156	9.4958	37.2521	3.6620	14.1504
700	31.9307	100.3516	11.0321	43.4607	4.2477	16.5088
800	36.4121	114.6875	12.5684	49.6694	4.8334	18.8672
900	40.8935	129.0234	14.1046	55.8781	5.4190	21.2256
1000	45.3749	143.3594	15.6409	62.0868	6.0047	23.5840

Fig. 4.1(a) shows the comparison of MWCNT and Copper resistance for 16nm technology node similarly Fig. 4.1(b) for 22nm technology node and Fig. 4.1(c) for 32nm technology node. From the Fig. 4.1(a), Fig. 4.1(b) and Fig. 4.1(c) it is clear that resistance of Copper is increasing much rapidly than that of MWCNT.

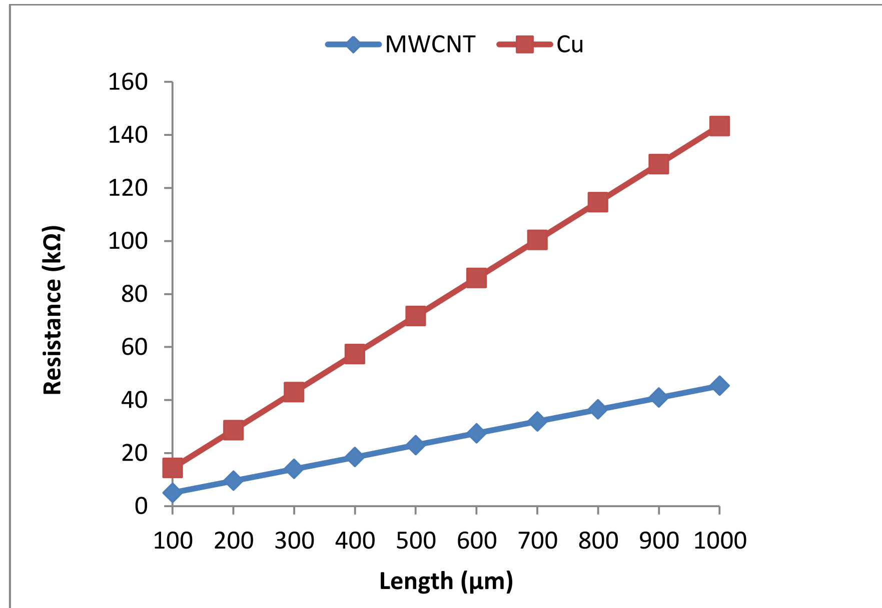

Fig. 4.1(a): Resistance comparison of MWCNT and Cu interconnect for 16nm Technology node

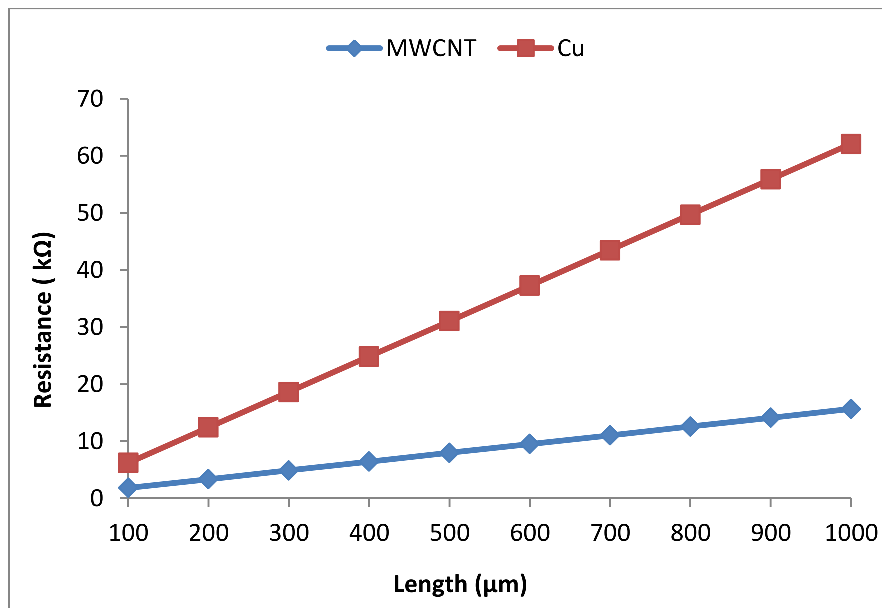

Fig. 4.1(b): Resistance comparison of MWCNT and Cu interconnect for 22nm Technology node

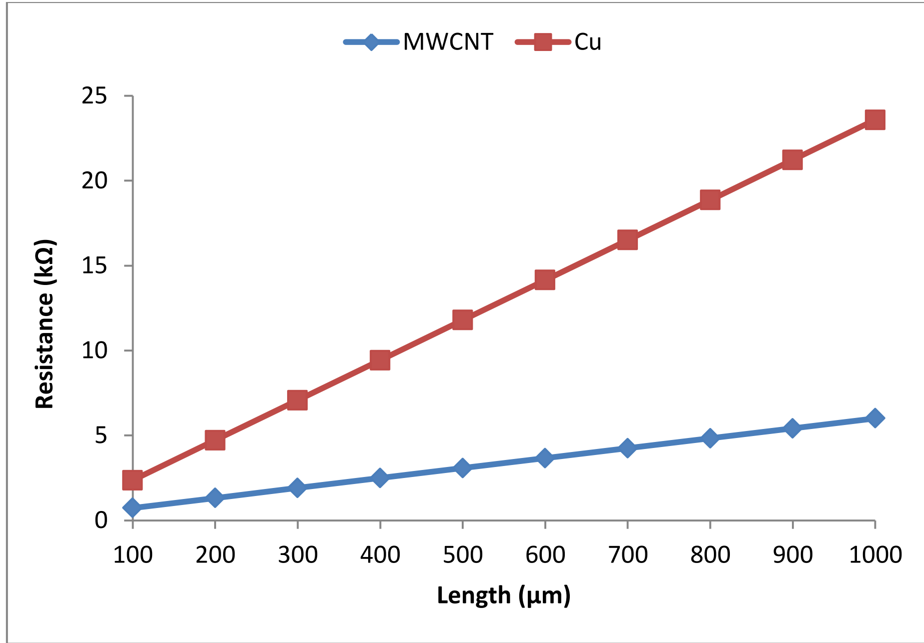

Fig. 4.1(c): Resistance comparison of MWCNT and Cu interconnect for 32nm Technology node

4.2 Capacitance

The value of capacitance is calculated in pF. By using equations (3.12), (3.13), (3.14) and (3.15) the value of capacitance for MWCNT interconnects is calculated and for Copper interconnects equations used are (3.19), (3.20) and (3.21) for different length and different technology nodes.

Table 4.2: Capacitance comparison of MWCNT and Cu interconnect for different length and for different Technology nodes i.e. 16nm, 22nm and 32nm

Capacitance in pF						
Length (μ)	**For 16nm**		**For 22nm**		**For 32nm**	
	MWCNT	**Cu**	**MWCNT**	**Cu**	**MWCNT**	**Cu**
100	0.0142	0.0117	0.0163	0.0136	0.0181	0.0150
200	0.0284	0.0234	0.0326	0.0273	0.0362	0.0300
300	0.0426	0.0352	0.0489	0.0409	0.0543	0.0450
400	0.0569	0.0469	0.0652	0.0545	0.0725	0.0600
500	0.0711	0.0586	0.0815	0.0682	0.0906	0.0750
600	0.0853	0.0703	0.0978	0.0818	0.1087	0.0900
700	0.0995	0.0820	0.1141	0.954	0.1268	0.1050
800	0.1137	0.0938	0.1305	0.1091	0.1449	0.1200
900	0.1279	0.1055	0.1468	0.1227	0.1630	0.1350
1000	0.1422	0.1172	0.1631	0.1363	0.1811	0.1500

Table 4.2 shows the value of capacitance for MWCNT and Copper interconnect for different length varying from 100um to 1000um for different technology nodes i.e. 16nm,

22nm and 32nm. Fig. 4.2(a) shows the comparison of Capacitance between MWCNT and Copper interconnects for different length and for 16nm technology node similarly Fig. 4.2(b) for 22nm and Fig. 4.2(c) for 32nm technology node. From these figures: Fig. 4.2(a), Fig. 4.2(b) and Fig. 4.2(c) it is clear that the change in capacitance almost similar in MWCNT and Copper interconnects.

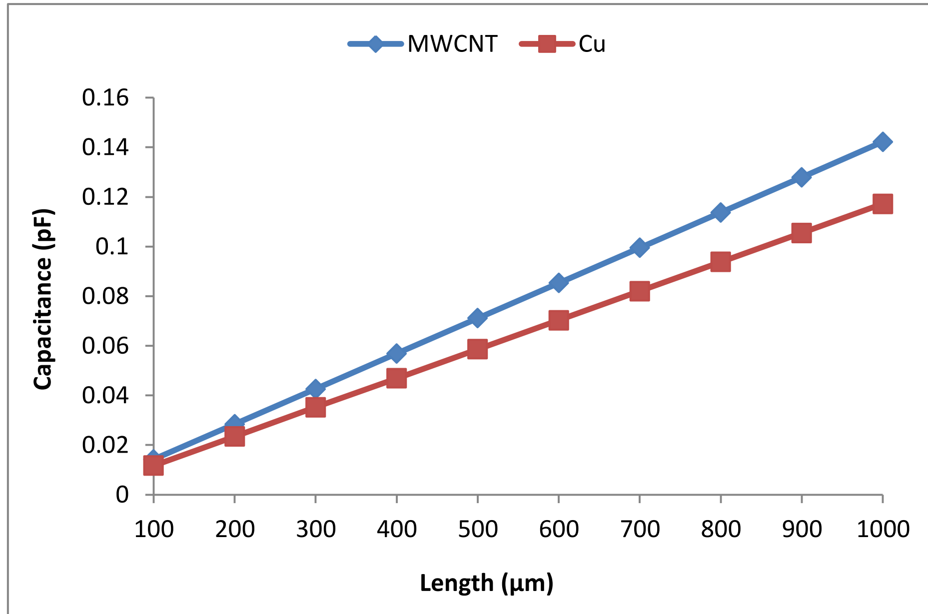

Fig. 4.2(a): Capacitance comparison of MWCNT and Cu interconnect for 16nm Technology node

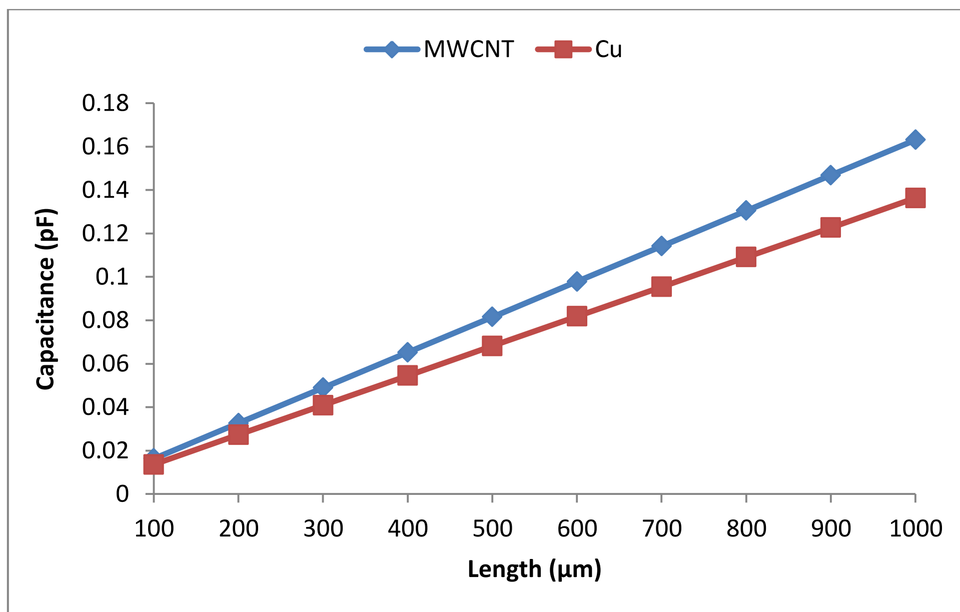

Fig. 4.2(b): Capacitance comparison of MWCNT and Cu interconnect for 22nm Technology node

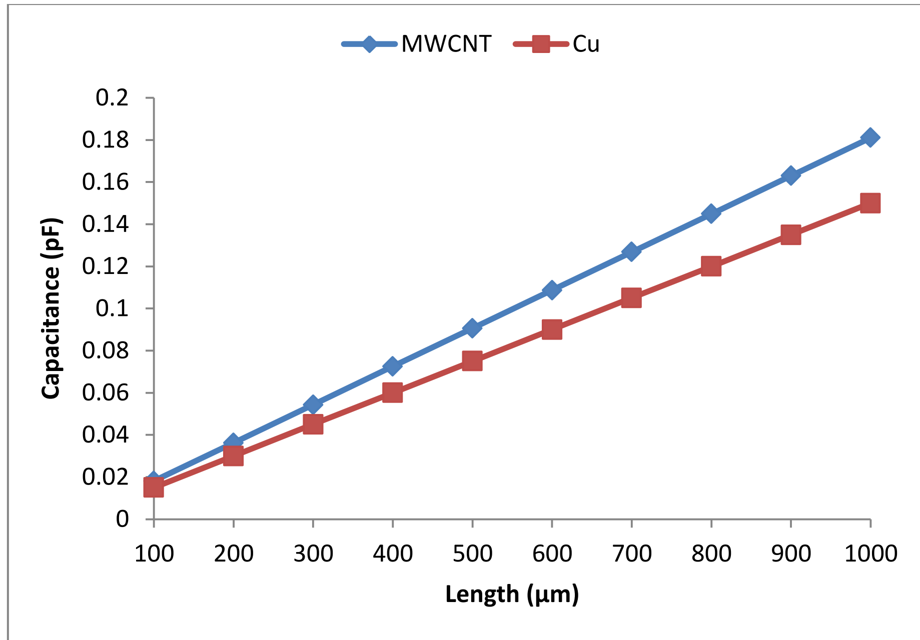

Fig. 4.2(c): Capacitance comparison of MWCNT and Cu interconnect for 32nm Technology node

4.3 Inductance

Inductance is calculated in nH for different length for MWCNT interconnects using equations (3.9), (3.10) and (3.11). For Copper interconnect using equation (3.22), values are listed below in Table 4.3 for different lengths and for different technology nodes.

Table 4.3: Inductance comparison of MWCNT and Cu interconnect for different length and for different Technology nodes i.e. 16nm, 22nm and 32nm

Inductance in nH						
Length (µm)	**For 16nm**		**For 22nm**		**For 32nm**	
	MWCNT	**Cu**	**MWCNT**	**Cu**	**MWCNT**	**Cu**
100	33.6124	0.1767	16.8068	0.1703	8.9638	0.1628
200	67.2249	0.3811	33.6136	0.3684	17.9277	0.3534
300	100.8373	0.5960	50.4204	0.5769	26.8915	0.5544
400	134.4498	0.8177	67.2272	0.7922	35.8553	0.7622
500	168.0622	1.0444	84.0340	1.0126	44.8191	0.9751
600	201.6746	1.2752	100.8408	1.2370	53.7830	1.1920
700	235.2871	1.5093	117.6476	1.4647	62.7468	1.4123
800	268.8995	1.7463	134.4544	1.6953	71.7106	1.6354
900	302.5120	1.9858	151.2612	1.9285	80.6745	1.8610
1000	336.1244	2.2275	168.0680	2.1638	89.6383	2.0889

From Fig. 4.3(a), it is observed that the increase in the inductance of MWCNT is high as compared to the inductance of Copper (the inductance is very low) for 16nm technology

node similarly from Fig. 4.3(b) and Fig. 4.3(c) which is for 22nm and 32nm technology node respectively.

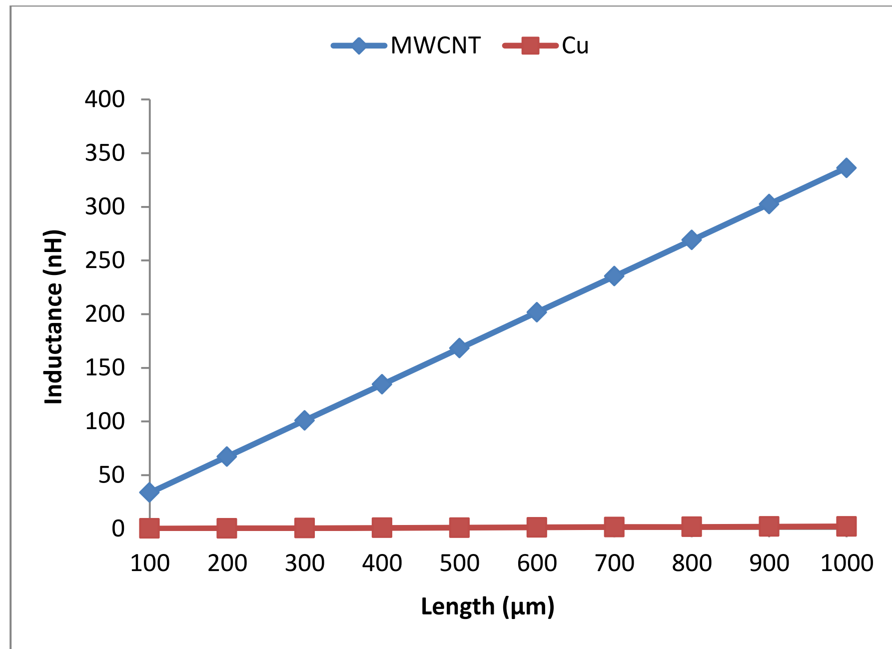

Fig. 4.3(a): Inductance comparison of MWCNT and Cu interconnect for 16nm Technology node

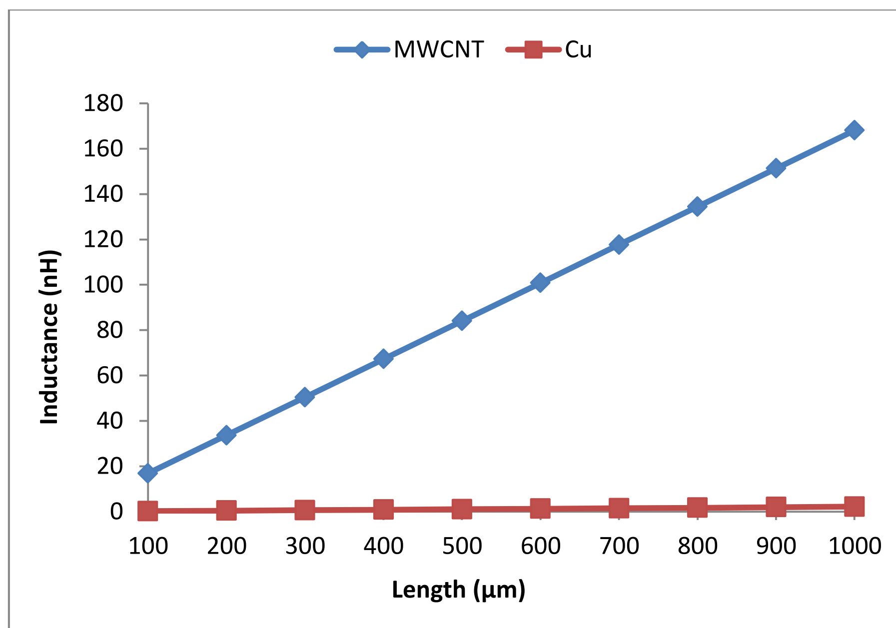

Fig. 4.3(b): Inductance comparison of MWCNT and Cu interconnect for 22nm Technology node

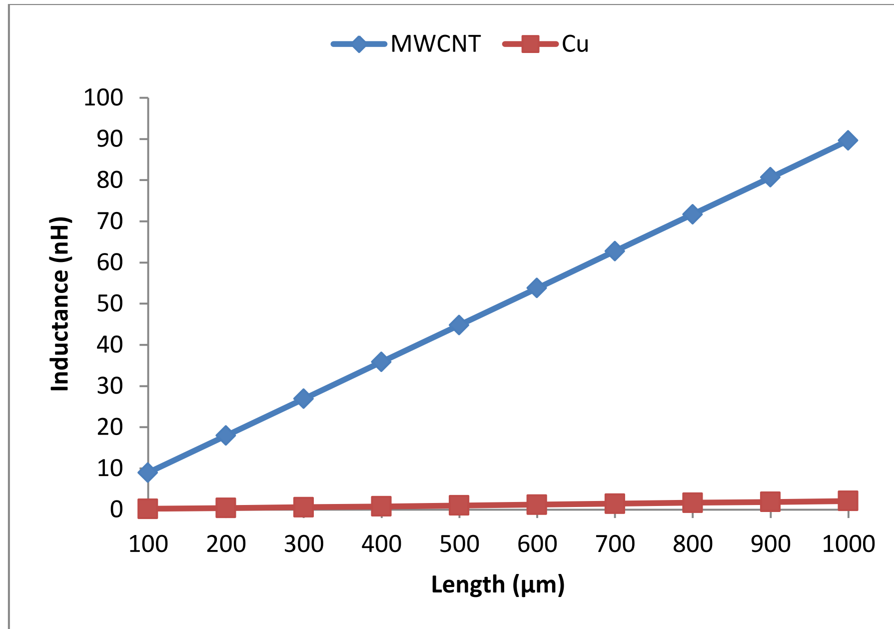

Fig. 4.3(c): Inductance comparison of MWCNT and Cu interconnects for 32nm Technology node

4.4 Observation made

- Resistance: There is seen a rapid increase in the value of resistance for Copper as the length increases from 100um to 1000um for different Technology node. The increase is said to be rapid as it's comparison is seen with the resistance value of MWCNT.
- Capacitance: Now, if the value of capacitance is observed with the same variation of length, the capacitance value of Copper does increase with increase in length but all the values are lower than the value of capacitance of MWCNT.
- Inductance: Finally the value of inductance for Copper and MWCNT is observed for the same variation of length, for Copper the value of inductance is very less than that of MWCNT and the increase is very less.

Now these calculated values of RLC are used to measure the delay, which is done with the help of Tanner Tool. We are required to have minimum delay, which has been discussed in Chapter 5.

CHAPTER 5

DELAY AND POWER ANALYSIS

The value of resistance, capacitance and inductance stand already calculated in Chapter 4. These values are the requirement for the calculation of delay and power. Motive of this thesis is to reduce the propagation delay and to achieve this number of Repeaters are placed in a long interconnect wire and also uses the driver-interconnect-load (DIL) employing CMOS driver. Also optimum value of driver size and number of repeaters are analyzed to reduce the propagation delay.

Tool used for delay calculation is Tanner Tool. This tool comprises of the following:

- S_Edit: Schematic Editor, the circuit is drawn using the precise components as per requirement. Schematic diagram of driver, interconnect and load is shown in Fig. 5.1. Here, CMOS is used as driver and interconnect is replaced by its equivalent RLC circuit. For load C_{Load} is used.

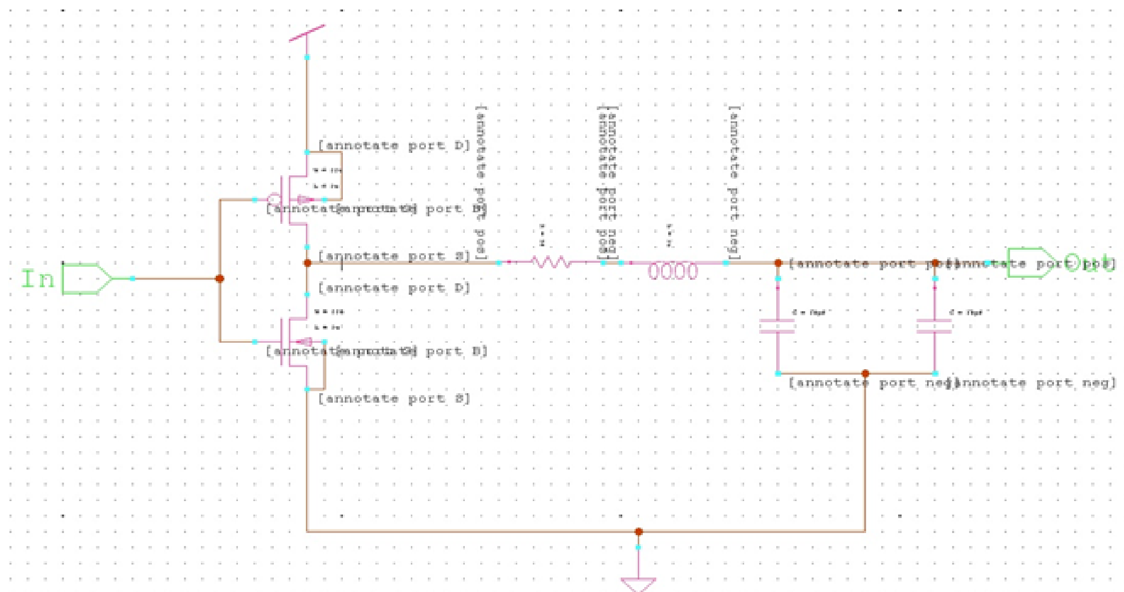

Fig. 5.1: Schematic diagram of Driver-Interconnect-Load

- T_Spice: This is circuit simulator. To simulate the circuit drawn in the S_Edit as shown in Fig. 5.1, this circuit is opened in T_Spice and a model file is added

which is shown in Appendix. The codes are written and the file is run for simulation.

- W_Edit: This is waveform editor used as waveform viewer. After the circuit is simulated the final or the output waveform are seen in W_Edit as shown in Fig. 5.2. From these waveforms delay is easily calculated. In the Fig. 5.2 given below the input waveform is of blue color and output is of pink color.

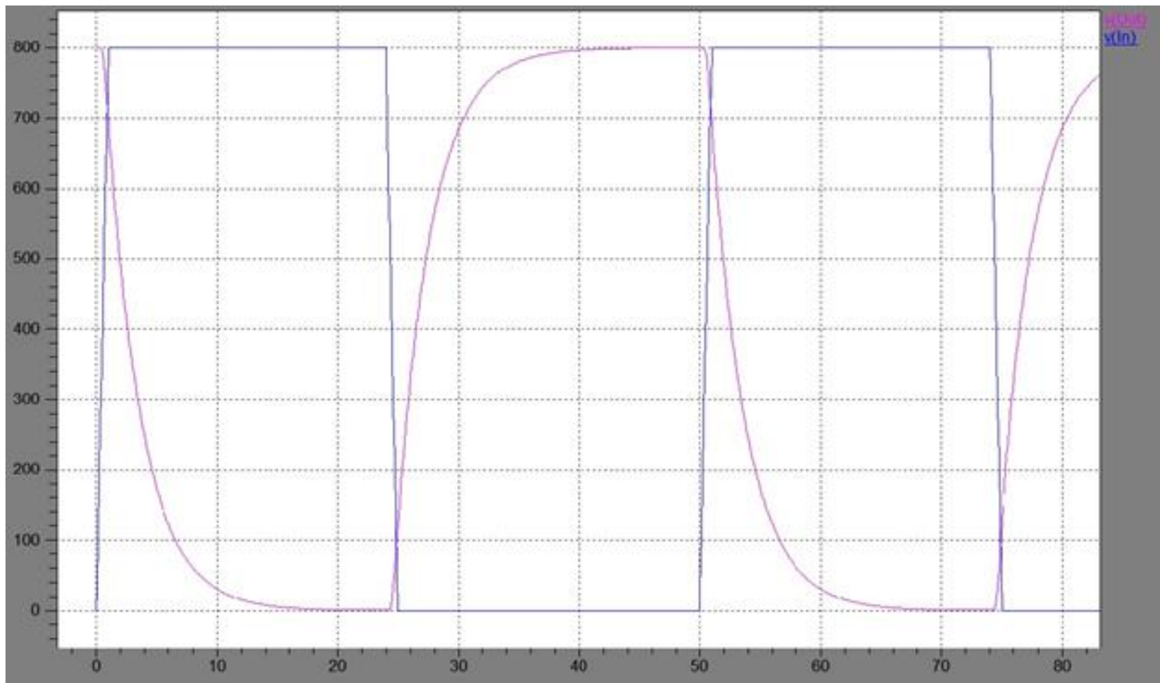

Fig. 5.2: waveform representation of Input and Output in W_Edit

In section 5.1 and 5.2 the effect on propagation delay and average power consumption of interconnects for lumped circuit is studied, but there is no use of the repeaters in these sections. The effect of number of repeaters on propagation delay and average power consumption is seen in the last section of this chapter 5.3 which is for distributed circuit.

5.1 Delay

The Tanner Tool helps to get the precise value of delay. Propagation delay for both MWCNT and Copper are calculated using SPICE simulation tool. The length of interconnect is varied from 400 to 1000µm which lies in intermediate interconnect range. The variation on the delay ratio of MWCNT and Copper interconnects are studied for different driver resistance, on particular technology nodes; viz 32nm, 22nm and 16nm. This analysis is seen in the Fig. 5.3(a), Fig. 5.3(b) and Fig. 5.3(c). The driver resistance is R_t which is inversely proportional to the driver size of driver [27].

Mathematical value of driver resistance is given:

$$R_t = \frac{\frac{L}{W}}{\mu_n \, C_{ox} V_{DD}} \tag{5.1}$$

where W/L is driver size, μ_n is mobility of electron, C_{ox} is oxide capacitance and V_{DD} is supplied voltage in circuit. From equation (5.1) the inverse proportionality of driver resistance and driver size is seen.

Following are the graphs to study the delay:

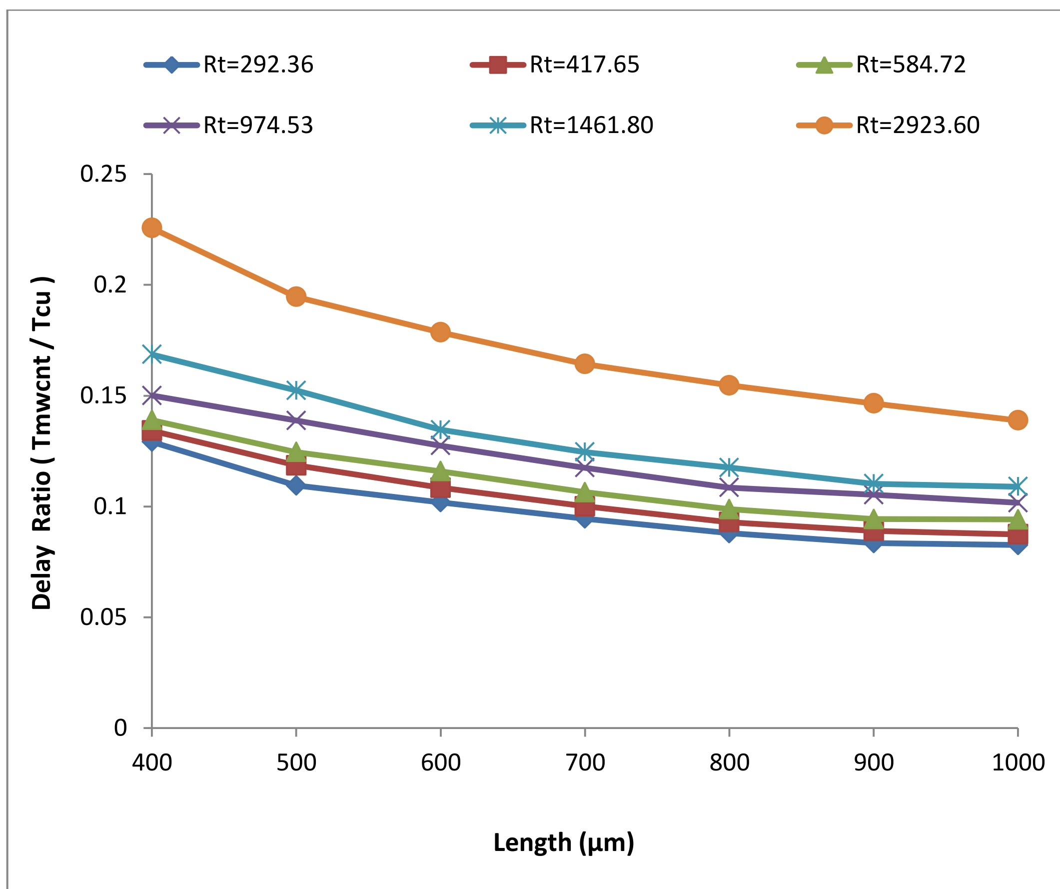

Fig. 5.3(a): Delay ratio between MWCNT and Cu interconnect (T_{MWCNT}/T_{Cu}) for different values of Driver resistance (R_t in ohm) for 32nm Technology node

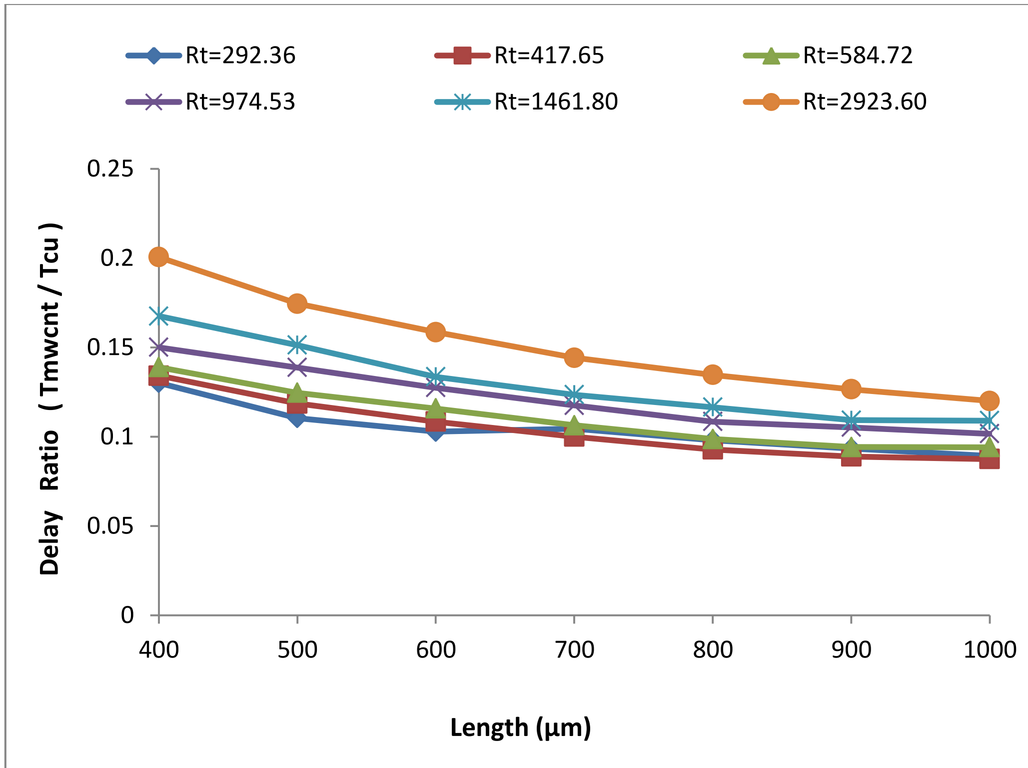

Fig. 5.3(b): Delay ratio between MWCNT and Cu interconnect (T_{MWCNT}/T_{Cu}) for different values of Driver resistance (R_t in ohm) for 22nm Technology node

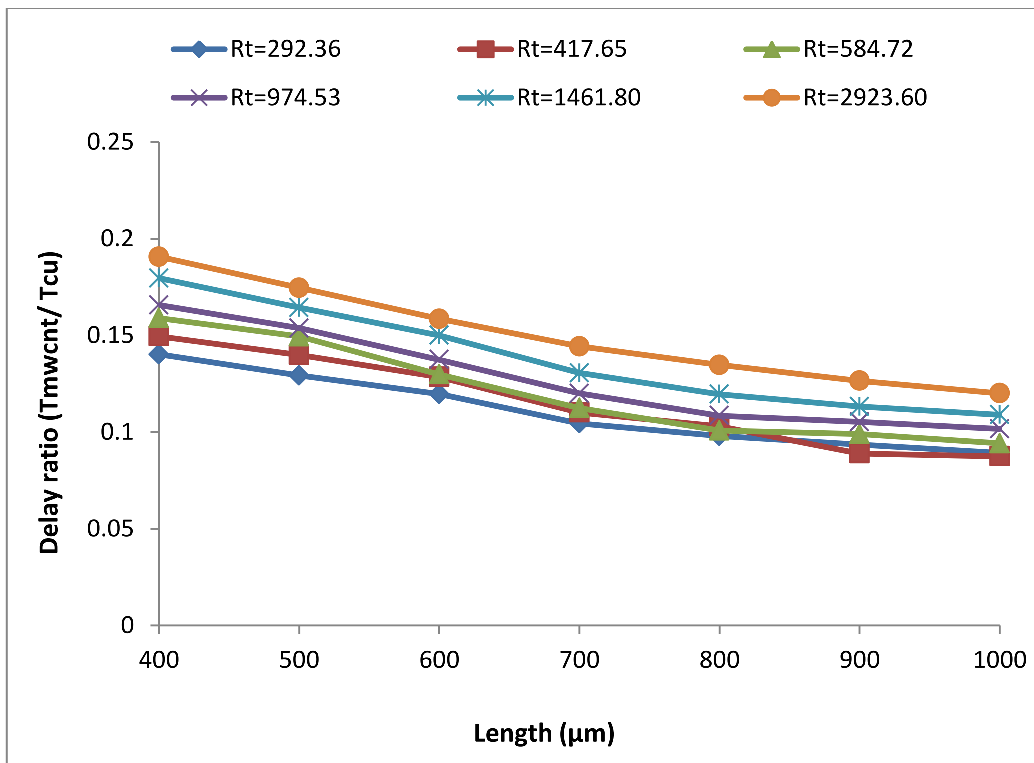

Fig. 5.3(c): Delay ratio between MWCNT and Cu interconnect (T_{MWCNT}/T_{Cu}) for different values of Driver resistance (R_t in ohm) for 16nm Technology node

Entire three graphs show gradual decrease in the delay with increase in driver size. The value of delay ratio that is above 0.2 and below 0.15 in Fig. 5.3(a) for driver resistance value of 2923.60Ω gets narrowed down between 0.2 and 0.10. Same result is seen for the different values of driver resistance for different technology node. Conclusively, there is decrease in the delay ratio for every technology node with the decrease in the driver resistance, but on the contrary there is also narrowness in the values of delay ratio in individual technology node.

5.2 Power Consumption

Power consumption has a very important role in VLSI chip, and interconnects play most significant role in determining the power consumption of digital system. Interconnect having less power consumption with the variation of driver size and length is the best suited interconnect. Power consumption of MWCNT and Copper are analyzed. Fig.5.4(a) shows the ratio of average power consumed by MWCNT to Copper for 32nm technology node, similarly Fig. 5.4(b) for 22nm and Fig. 5.4(c) for 16nm technology node. From all these figures: i.e. Fig. 5.4(a), Fig. 5.4(b) and Fig. 5.4(c), it is clear that average power consumed by MWCNT is less than the power consumed by Copper for various driver sizes. Overall average power consumption decreases with decreasing the technology node and with increase in length of interconnect for fixed driver size.

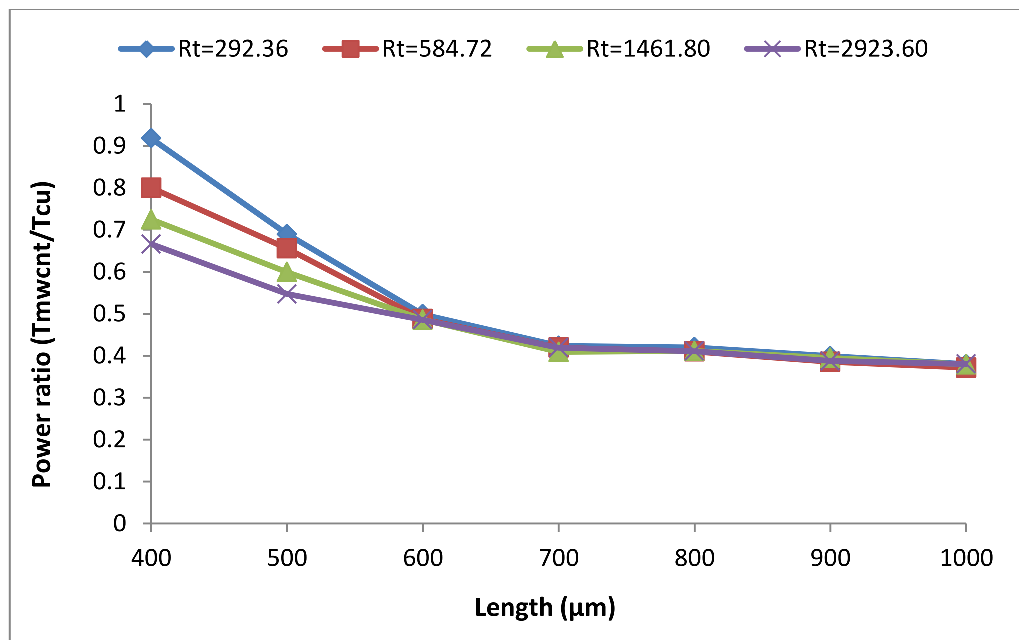

Fig. 5.4(a): Power ratio between MWCNT and Cu interconnect (T_{MWCNT}/T_{Cu}) for different values of Driver resistance (R_t in ohm) for 32nm Technology

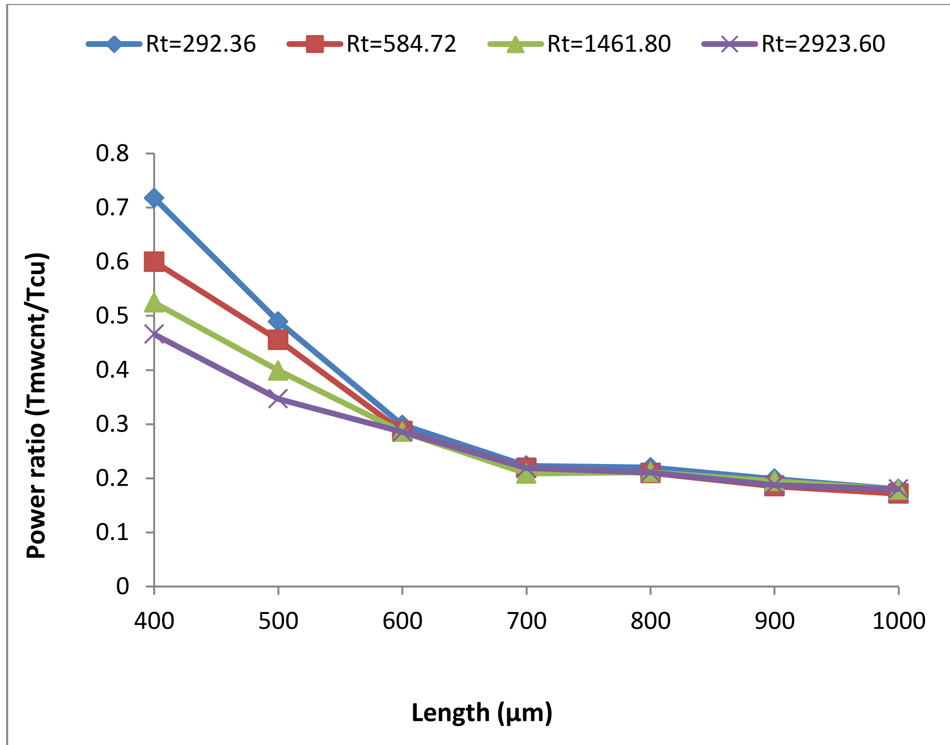

Fig. 5.4(b): Power ratio between MWCNT and Cu interconnect (T_{MWCNT}/T_{Cu}) for different values of Driver resistance (R_t in ohm) for 22nm Technology node

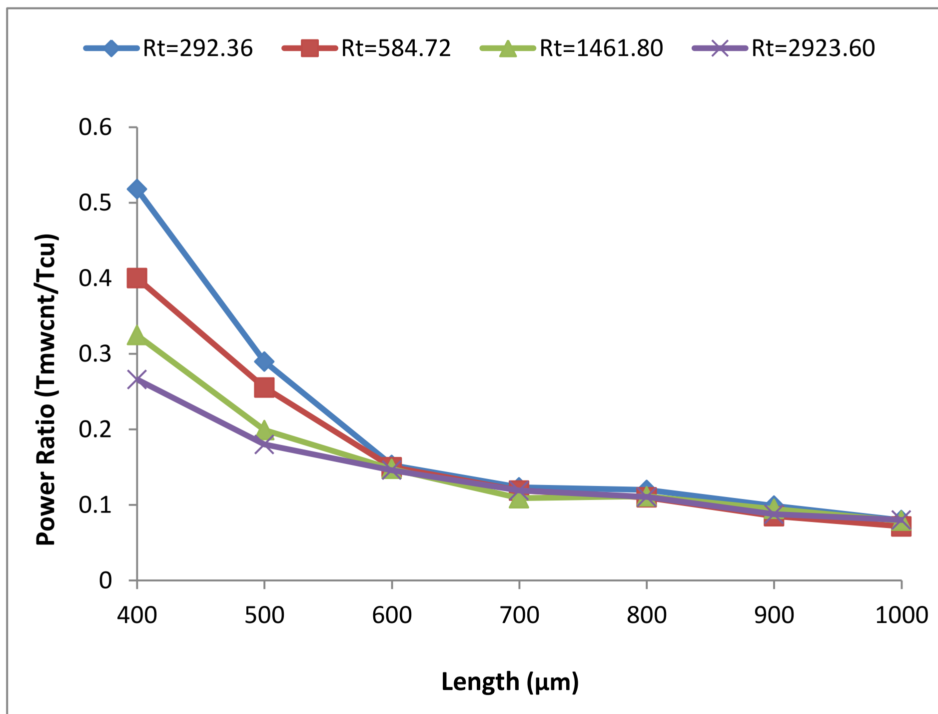

Fig. 5.4(c): Power ratio between MWCNT and Cu interconnect (T_{MWCNT}/T_{Cu}) for different values of Driver resistance (R_t in ohm) for 16nm Technology node

From all the result shown in Fig. 5.4(a), Fig. 5.4(b) and Fig. 5.4(c) it is inferred that there is a decrease in the value of power ratio. In the beginning the decrease is sharp for some values and then the curve decreases gradually.

5.3 Effect of Repeaters in MWCNT interconnects for 22nm at 1000um length

In section 5.1 and 5.2 the variation of delay and power consumption were seen for the lumped circuit or without use of repeaters. Here in section 5.3 the distributed circuit will be studied, with the help of repeaters. Fig. 5.5 shows a distributed circuit. There are three repeaters used and the circuit has been segmented into four parts. The Fig. 5.5 exemplifies how distributed circuit can be made with the use of repeaters. If number of repeaters are taken N, then the circuit get segmented into N+1 part.

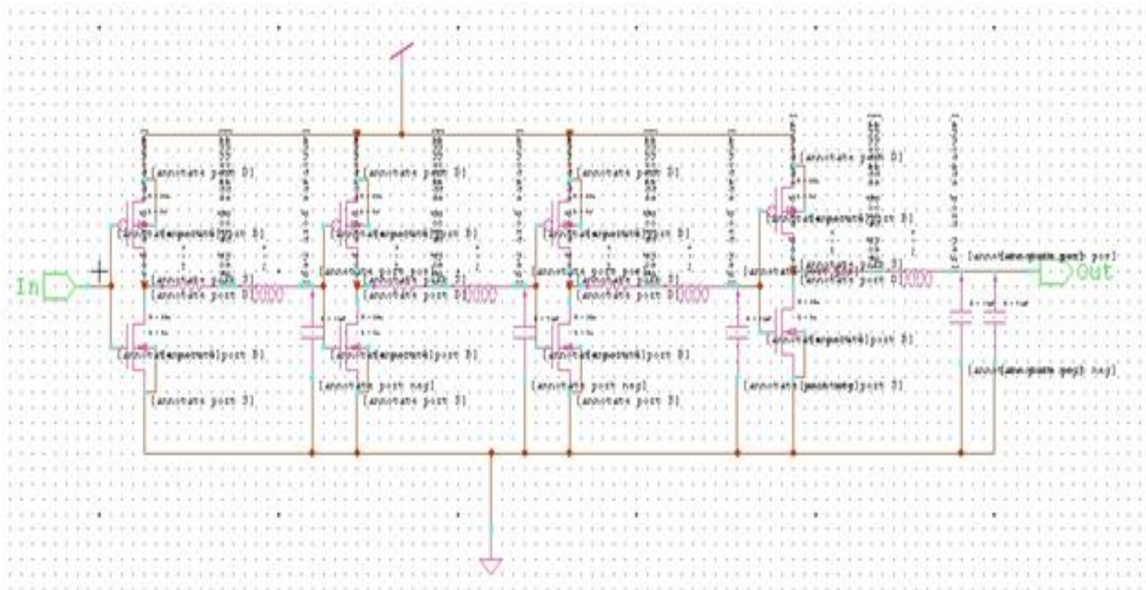

Fig. 5.5: Driver-Interconnect-Load circuit with three repeaters

The foremost requirement of having minimum delay is also achieved with the use of repeaters. So, in this section we will be studying the effect of adding repeaters on the delay and power consumption. The optimum value of driver size is calculated for MWCNT interconnect because with increase in the driver size average power consumption is also increasing. As given in Table 5.1 there is value of delay, average power consumption and also product of delay and power (PDP) is given for 22nm technology node and for 1000um interconnect length, where T_r and T_f are rise and fall time respectively.

Table 5.1: Variation of delay, average power consumed and product of delay and power of MWCNT interconnect for 22nm Technology node at 1000um length with different Driver size

Driver Size (W/L)	R_t(kΩ)	Delay			Avg. Power(P)	PDP
		T_r(ns)	T_f(ns)	T(ns)		
10	1911.308	6.29n	6.09	6.19	2.4223E-006	1.50E-05
20	955.654	6.09	5.94	6.015	2.6180E-006	1.57E-05
30	637.103	6.00	5.89	5.945	2.8172E-006	1.67E-05
40	477.827	5.95	5.85	5.90	3.0171E-006	1.78E-05
50	382.262	5.89	5.81	5.85	3.2176E-006	1.90E-05
60	318.551	5.95	5.85	5.90	3.4180E-006	2.02E-05
70	273.044	5.90	5.83	5.865	3.6183E-006	2.12E-05
80	238.913	5.91	5.80	5.855	3.8185E-006	2.24E-05
90	212.367	5.90	5.80	5.85	4.0185E-006	2.35E-05
100	191.131	5.94	5.84	5.89	4.2183E-006	2.47E-05

For the Table 5.1, values calculated are for Technology node 22nm at length 1000um. From studying the Table 5.1 it is inferred that driver resistance 382.262Ω is the optimum value. For this value of driver resistance the delay is minimum that is 5.85ns, average power is 3.2176E-006w and PDP (product of delay and power) is 1.90E-05. All these results give the driver size value of 50 and driver resistance of 382.262Ω.

So, this driver resistance is used for the further calculation. Now for driver resistance 382.262Ω, optimum value of repeaters is calculated for same technology at 1000um, which is shown in Table 5.2.

Table 5.2: Variation of delay and power consumed of MWCNT interconnect for 22nm Technology node at 1000um length with different number of Repeaters

R_t = 382.262Ω					
No. of Rep.	T_r (ps)	T_f (ps)	T (ps)	P(Watt)	PDP
1	1.83(ns)	1.88(ns)	1.855(ns)	5.029E-06	9.329E-03
2	994.42	927.57	960.995	4.775E-06	4.589E-03
3	619.27	598.71	608.99	4.665E-06	2.841E-06
4	443.45	391.98	417.715	4.548E-06	1.900E-03
5	397.79	370.06	383.925	4.604E-06	1.768E-03

6	306.50	256.00	281.25	4.829E-06	1.358E-03
7	205.92	186.90	196.41	4.812E-06	9.451E-04
8	189.32	133.84	161.58	5.087E-06	8.220E-04
9	170.50	102.93	136.715	5.251E-06	7.179E-04
10	161.94	77.98	119.96	5.554E-06	6.662E-04
11	128.88	72.87	100.875	5.739E-06	5.789E-04
12	115.37	55.27	85.32	6.119E-06	5.221E-04
13	103.00	60.17	81.585	6.305E-06	5.144E-04
14	100.32	51.22	75.77	6.771E-06	5.130E-04
15	96.85	50.40	73.625	6.897E-06	5.078E-04
16	97.31	45.97	71.64	7.337E-06	5.256E-04
17	92.41	51.24	71.825	7.473E-06	5.367E-04
18	92.08	45.92	69.00	7.944E-06	5.481E-04
19	87.84	46.31	67.075	8.058E-06	5.405E-04
20	90.40	42.96	66.68	8.506E-06	5.672E-04

where T_r and T_f are the rise and fall time respectively and T is mean of both. P is the average power consumed by the circuit. The conclusive result from the above table is as following:

- Form above table it is inferred that with increase in number of repeaters the value of delay is reducing, which is a positive result.
- At the same time value of average power consumed by the circuit is increasing with increase in number of repeaters, this increase is required not to be very high.
- Above two factors in the tradeoff between delay and average power consumed.
- So, an optimum value has to be selected for which there is a less delay and the power consumption is not very high.
- Keeping in mind these factors and the above calculated values of power and delay a graph is drawn in Fig. 5.6, so that the optimum value can be easily calculated.

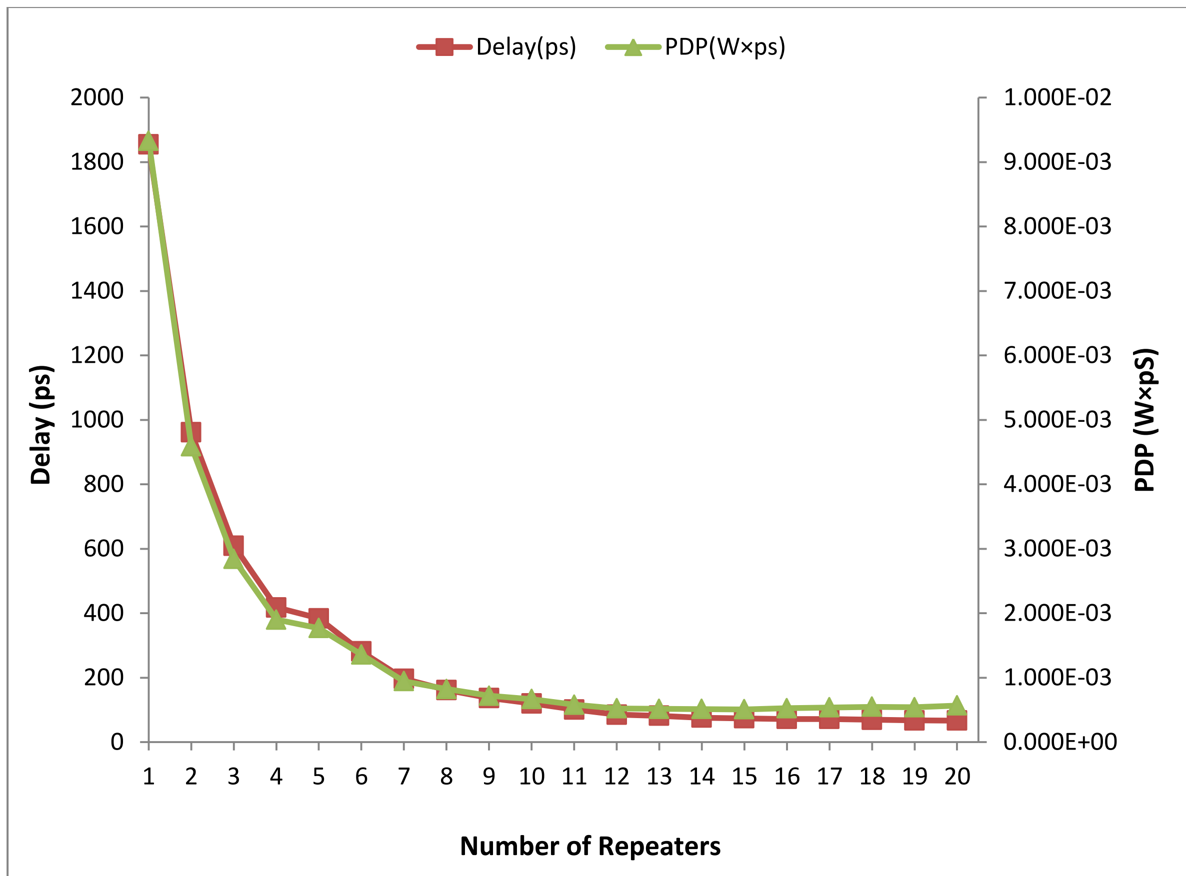

Fig. 5.6: Variation of delay and average power consumption of MWCNT interconnect for 22nm Technology node at 1000um length with different number of repeaters

CHAPTER 6 CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

The work done in this thesis analyzed the effect of driver size on propagation delay from Fig. 5.3 and average power consumption Fig. 5.4 for different Technology Nodes viz 32nm, 22nm and 16nm and different interconnects length. The following points are concluded on observing the simulated results: MWCNT has lower propagation delay and average power consumption than Copper interconnects. As the size of driver increases the propagation delay is reduces and average power consumption also reduces as compared to Copper. So it can be said that in all the cases, the propagation delay and power of MWCNT interconnect is less than Copper interconnect at intermediate level for a particular driver size.

It is inferred from the results in Table 5.1 that the delay is reducing with the decrease in driver resistance till driver resistance reaches 382.262Ω and almost remains constant henceforth. So, optimum value of driver resistance is taken 382.262Ω in this case.

By the use of repeater the delay is reduced as the number of repeater are increased. In case of power, the value starts increasing as shown in Table 5.2. So an optimum value of repeaters is chosen for which average power consumption is low and the delay remains minimum.

It is observed that delay for lumped element model is more in comparison to distributed element model. To conquer this problem, repeaters are used to convert the lumped element model into distributed element model. So, by increasing the number of repeaters value of delay starts decreasing. But, the number of repeaters cannot be increased above an optimum value because repeaters consume power and therefore average power consumption of model becomes high which is not desirable. Hence, optimum number of repeaters is chosen.

6.2 Future Scope

Carbon nanotubes have aroused research interest for their applicability as very-large-scale-integration (VLSI) interconnects because of their high thermal stability, high thermal conductivity and large current carrying capacity. A CNT can carry current densities in excess of 1000MA/sq-cm without damage even at an elevated temperature of 250 ℃ , eliminating electro migration reliability concerns that plague Copper interconnects.

As delay is very important parameter to obtain the best performance of CNT so further analysis in change in driver size for optimum value of repeaters, also analyze the effect of different technology node and different length of interconnect.

LIST OF PUBLICATIONS

[1] Arun Verma and Karmjit Singh Sandha, "Effect of Driver Size on Multiwall Carbon Nanotubes as VLSI Interconnects for Local and Intermediate Length," *communicated to IEEE conference on Contemporary Computing.*

[2] Arun Verma and Karmjit Singh Sandha, "Effect of Driver Size and number of repeaters on Multiwall Carbon Nanotubes as VLSI Interconnects for Local and Intermediate Length," *communicated to International Journal of Electronics Circuits and Systems (IJECS).*

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APPENDIX

A.1 PTM level 54 model

This model is used for simulation of equivalent circuit model of CNT.

.model nmosnmos level = 54

```
+version = 4.0        binunit = 1          paramchk= 1
mobmod  = 0
+capmod = 2           igcmod  = 1          igbmod  = 1
geomod  = 1
+diomod  = 1          rdsmod  = 0          rbodymod= 1
rgatemod= 1
+permod  = 1          acnqsmod= 0          trnqsmod= 0
+tnom    = 27         toxe    = 1.15e-009  toxp    = 9e-010
toxm    = 1.15e-009
+dtox    = 2.5e-010   epsrox  = 3.9        wint    = 5e-009
lint    = 2.7e-009
+ll      = 0          wl      = 0          lln     = 1
wln     = 1
+lw      = 0          ww      = 0          lwn     = 1
wwn     = 1
+lwl     = 0          wwl     = 0          xpart   = 0
toxref  = 1.15e-009
+xl          = -14e-9
+vth0    = 0.49396    k1      = 0.4        k2      = 0
k3      = 0
+k3b     = 0          w0      = 2.5e-006   dvt0    = 1
dvt1    = 2
+dvt2    = 0          dvt0w   = 0          dvt1w   = 0
dvt2w   = 0
+dsub    = 0.1        minv    = 0.05       voffl   = 0
dvtp0   = 1e-011
+dvtp1   = 0.1        lpe0    = 0          lpeb    = 0
xj      = 1e-008
+ngate   = 1e+023     ndep    = 4.12e+018  nsd     = 2e+020
phin    = 0
+cdsc    = 0          cdscb   = 0          cdscd   = 0
cit     = 0
+voff    = -0.13      nfactor = 2.508      eta0    = 0.0048
etab    = 0
+vfb     = -0.55      u0      = 0.05       ua      = 6e-010
ub      = 1.2e-018
+uc      = 0          vsat    = 210000     a0      = 1
ags     = 0
+a1      = 0          a2      = 1          b0      = 0
b1      = 0
+keta    = 0.04       dwg     = 0          dwb     = 0
pclm    = 0.02
```

```
+pdiblc1 = 0.001         pdiblc2 = 0.001          pdiblcb = -0.005
drout   = 0.5
+pvag    = 1e-020        delta   = 0.01           pscbe1  = 8.14e+008
pscbe2  = 1e-007
+fprout  = 0.2           pdits   = 0.01           pditsd  = 0.23
pditsl  = 2300000
+rsh     = 5             rdsw    = 150            rsw     = 75
rdw     = 75
+rdswmin = 0             rdwmin  = 0              rswmin  = 0
prwg    = 0
+prwb    = 0             wr      = 1              alpha0  = 0.074
alpha1  = 0.005
+beta0   = 30            agidl   = 0.0002         bgidl   = 2.1e+009
cgidl   = 0.0002
+egidl   = 0.8           aigbacc = 0.012          bigbacc = 0.0028
cigbacc = 0.002
+nigbacc = 1             aigbinv = 0.014          bigbinv = 0.004
cigbinv = 0.004
+eigbinv = 1.1           nigbinv = 3              aigc    = 0.020014
bigc    = 0.0027432
+cigc    = 0.002         aigsd   = 0.020014       bigsd   = 0.0027432
cigsd   = 0.002
+nigc    = 1             poxedge = 1              pigcd   = 1
ntox    = 1
+xrcrg1  = 12            xrcrg2  = 5
+cgso    = 8.5e-011      cgdo    = 8.5e-011       cgbo    = 2.56e-011
cgdl    = 2.653e-010
+cgsl    = 2.653e-010    ckappas = 0.03           ckappad = 0.03
acde    = 1
+moin    = 15            noff    = 0.9            voffcv  = 0.02
+kt1     = -0.11         kt1l    = 0              kt2     = 0.022
ute     = -1.5
+ua1     = 4.31e-009     ub1     = 7.61e-018      uc1     = -5.6e-011
prt     = 0
+at      = 33000
+fnoimod = 1             tnoimod = 0
+jss     = 0.0001        jsws    = 1e-011         jswgs   = 1e-010
njs     = 1
+ijthsfwd= 0.01          ijthsrev= 0.001          bvs     = 10
xjbvs   = 1
+jsd     = 0.0001        jswd    = 1e-011         jswgd   = 1e-010
njd     = 1
+ijthdfwd= 0.01          ijthdrev= 0.001          bvd     = 10
xjbvd   = 1
+pbs     = 1             cjs     = 0.0005         mjs     = 0.5
pbsws   = 1
+cjsws   = 5e-010        mjsws   = 0.33           pbswgs  = 1
cjswgs  = 3e-010
+mjswgs  = 0.33          pbd     = 1              cjd     = 0.0005
mjd     = 0.5
```

```
+pbswd   = 1          cjswd   = 5e-010       mjswd   = 0.33
pbswgd  = 1
+cjswgd  = 5e-010     mjswgd  = 0.33         tpb     = 0.005
tcj     = 0.001
+tpbsw   = 0.005      tcjsw   = 0.001        tpbswg  = 0.005
tcjswg  = 0.001
+xtis    = 3          xtid    = 3
+dmcg    = 0          dmci    = 0            dmdg    = 0
dmcgt   = 0
+dwj     = 0          xgw     = 0            xgl     = 0
+rshg    = 0.4        gbmin   = 1e-010       rbpb    = 5
rbpd    = 15
+rbps    = 15         rbdb    = 15           rbsb    = 15
ngcon   = 1
```

.model pmos pmos level = 54

```
+version = 4.0        binunit = 1            paramchk= 1
mobmod  = 0
+capmod = 2           igcmod  = 1            igbmod  = 1
geomod  = 1
+diomod  = 1          rdsmod  = 0            rbodymod= 1
rgatemod= 1
+permod  = 1          acnqsmod= 0            trnqsmod= 0
+tnom    = 27         toxe    = 1.2e-009     toxp    = 9e-010
toxm    = 1.2e-009
+dtox    = 3e-010     epsrox  = 3.9          wint    = 5e-009
lint    = 2.7e-009
+ll      = 0          wl      = 0            lln     = 1
wln     = 1
wwn     = 1
+lwl     = 0          wwl     = 0            xpart   = 0
toxref  = 1.2e-009
+xl          = -14e-9
+vth0    = -0.49396   k1      = 0.4          k2      = -0.01
k3      = 0
+k3b     = 0          w0      = 2.5e-006     dvt0    = 1
dvt1    = 2
+dvt2    = -0.032     dvt0w   = 0            dvt1w   = 0
dvt2w   = 0
+dsub    = 0.1        minv    = 0.05         voffl   = 0
dvtp0   = 1e-011
+dvtp1   = 0.05       lpe0    = 0            lpeb    = 0
xj      = 1e-008
+ngate   = 1e+023     ndep    = 3.07e+018    nsd     = 2e+020
phin    = 0
+cdsc    = 0          cdscb   = 0            cdscd   = 0
cit     = 0
+voff    = -0.13      nfactor = 2.1          eta0    = 0.0048
etab    = 0
```

```
+vfb     = -0.55          u0      = 0.05           ua      = 2e-009
ub      = 5e-019
+uc      = 0              vsat    = 180000         a0      = 1
ags     = 1e-020
+a1      = 0              a2      = 1              b0      = 0
b1      = 0
+keta    = 0.047          dwg     = 0              dwb     = 0
pclm    = 0.12
+pdiblc1 = 0.001          pdiblc2 = 0.001          pdiblcb = 3.4e-008
drout   = 0.56
+pvag    = 1e-020         delta   = 0.01           pscbe1  = 8.14e+008
pscbe2  = 9.58e-007
+fprout  = 0.2            pdits   = 0.08           pditsd  = 0.23
pditsl  = 2300000
+rsh     = 5              rdsw    = 150            rsw     = 75
rdw     = 75
+rdswmin = 0              rdwmin  = 0              rswmin  = 0
prwg    = 0
+prwb    = 0              wr      = 1              alpha0  = 0.074
alpha1  = 0.005
+beta0   = 30             agidl   = 0.0002         bgidl   = 2.1e+009
cgidl   = 0.0002
+egidl   = 0.8            aigbacc = 0.012          bigbacc = 0.0028
cigbacc = 0.002
+nigbacc = 1              aigbinv = 0.014          bigbinv = 0.004
cigbinv = 0.004
+eigbinv = 1.1            nigbinv = 3              aigc    = 0.020014
bigc    = 0.0027432
+cigc    = 0.002          aigsd   = 0.020014       bigsd   = 0.0027432
cigsd   = 0.002
+nigc    = 1              poxedge = 1              pigcd   = 1
ntox    = 1
+xrcrg1  = 12             xrcrg2  = 5
+cgso    = 8.5e-011       cgdo    = 8.5e-011       cgbo    = 2.56e-011

cgdl    = 2.653e-010
+cgsl    = 2.653e-010     ckappas = 0.03           ckappad = 0.03
acde    = 1
+moin    = 15             noff    = 0.9            voffcv  = 0.02
+kt1     = -0.11          kt1l    = 0              kt2     = 0.022
ute     = -1.5
+ua1     = 4.31e-009      ub1     = 7.61e-018      uc1     = -5.6e-011
prt     = 0
+at      = 33000
+fnoimod = 1              tnoimod = 0
+jss     = 0.0001         jsws    = 1e-011         jswgs   = 1e-010
njs     = 1
+ijthsfwd= 0.01           ijthsrev= 0.001          bvs     = 10
xjbvs   = 1
+jsd     = 0.0001         jswd    = 1e-011         jswgd   = 1e-010
```

```
njd     = 1
+ijthdfwd= 0.01        ijthdrev= 0.001        bvd     = 10
xjbvd   = 1
+pbs     = 1           cjs     = 0.0005       mjs     = 0.5
pbsws   = 1
+cjsws   = 5e-010      mjsws   = 0.33         pbswgs  = 1
cjswgs  = 3e-010
+mjswgs  = 0.33        pbd     = 1            cjd     = 0.0005
mjd     = 0.5
+pbswd   = 1           cjswd   = 5e-010       mjswd   = 0.33
pbswgd  = 1
+cjswgd  = 5e-010      mjswgd  = 0.33         tpb     = 0.005
tcj     = 0.001
+tpbsw   = 0.005       tcjsw   = 0.001        tpbswg  = 0.005
tcjswg  = 0.001
+xtis    = 3           xtid    = 3
+dmcg    = 0           dmci    = 0            dmdg    = 0
dmcgt   = 0
+dwj     = 0           xgw     = 0            xgl     = 0
+rshg    = 0.4         gbmin   = 1e-010       rbpb    = 5
rbpd    = 15
+rbps    = 15          rbdb    = 15           rbsb    = 15
ngcon   = 1
```