EFFECT OF CHANGE OF DIAMETER RATIO ON PERFORMANCE OF MWCNTS AS VLSI INTERCONNECTS

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Submitted by

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DECLARATION

I, Shweta Maheshwari, hereby certify that the work which is being presented in this thesis entitled "Effect of Change of Diameter Ratio on Performance of MWCNTS as VLSI Interconnects" by me in partial fulfilment of the requirements for the award of degree of Master of Technology in VLSI Design from Thapar University (Deemed University), Patiala, is an authentic record of my own work carried out under the supervision of Mr. Karamjit Singh Sandha.

The matter presented in this thesis has not been submitted in any other University / Institute for the award of any other degree.

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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Shweta Maheshwari

ABSTRACT

According to the Moore's law, the number of transistors and densities on integrated circuits doubles approximately every two years. Hence as per Moore's law, the dimensions and performance of devices are scaling down over the last 40 years. Due to scaling, performance of on-chip intermediate length copper interconnect faces many challenges such as using copper as interconnect the speed of device getting slower, power consumption increasing and the requirement of bandwidth does not fulfilled. As technology scales down the problems associated with copper as interconnects are low mean free path, electro migration and high resistivity due to rough surface and grain boundary scattering. The most promising solution of copper problem is Carbon Nanotubes (CNT) for future integrated circuits. As CNTs have good electrical properties, high thermal and mechanical strength. CNTs have long mean free paths (MFPs) on the order of several micro meters as compared to Copper at room temperature, which provide low resistivity and possible ballistic transport in intermediate-length interconnects. An isolated CNT can carry current densities in excess of 10^{10} A/cm^2 without any signs of damage, thereby eliminating electromigration reliability concerns that plague nanoscale Copper interconnects.

CNTs are classified as SWCNT (Single-walled Carbon Nanotube) and MWCNT (Multi-walled Carbon Nanotube). SWCNT consists of single shell of graphene sheet, it can have diameters varying from few nanometers to 4nm. MWCNTs is consists of multiple concentric shells of graphene sheets.

In this thesis work, the performance of MWCNTs and Copper has been compared at 32nm, 22nm and 16nm technology node at intermediate level of interconnect. The model of MWCNT and Copper as interconnect used for delay calculation has been estimated.

Changing the diameter ratio leads to change in number of shell. As the diameter ratio increases this means the number of shell decreases. As the number of shells increases then the number of conducting channels increases. This leads to increase in conductivity of MWCNT, hence decrease in resistivity of MWCNT. The diameter ratio of MWCNT has been varied for all of three technologies to compare performance parameter i.e. delay, power consumption and power delay product(PDP) with respect to copper as interconnect at intermediate level. It is shown that MWCNT gives better result than copper interconnects at

intermediate level. Even that the worst case of MWCNT as interconnect provides better performance than copper.

LIST OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ABBREVIATIONS

IC	Integrated Circuits
RLC	Resistance, Inductance, Capacitance
MFP	Mean Free Path
CNT	Carbon Nanotubes
SWCNT	Single-Walled Carbon Nanotubes
MWCNT	Multi-Walled Carbon Nanotubes
VLSI	Very Large Scale Integration
OCC	Onho Continuous Casting
CVD	Chemical Vapour Deposition
EM	Electromigration
ITRS	International Technology Roadmap for Semiconductors
CMOS	Complementary Metal-Oxide Semiconductors
EDA	Electronic Design Automation
SPICE	Simulation Program with Integrated Circuit Emphasis
PDP	Power Delay Product

CHAPTER - 1

INTRODUCTION

1.1. INTRODUCTION

Interconnects are acts as the highways and streets of the integrated circuit (IC), i.e. connecting devices of the IC to the outside world and into a functioning whole. Interconnect levels vary in numbers depending on the complexity of the device and are interconnected by vias. The main function of interconnect is to provide clock signal and other useful signal within the same functional block(local interconnects) or within the different functional blocks (global interconnects)[1]. They also used to distribute the power and ground signal throughout the integrated circuits. Interconnects are also used to provide communication signals among the modules.

There are three types of interconnects:

Local Interconnects- are short interconnects and used to connect the gate and transistors within the same functional block.

Intermediate Interconnects- are wider and taller than local interconnects and used to provide clock and other signal within a functional block.

Global Interconnects- are long interconnects and used to provide power/ground and clock signal within the different functional blocks.

For higher technology, interconnects does not plays a very important role because in higher technology the gate delay is higher than interconnect delay hence the interconnect delay is not dominating factor in slowing the speed of device. But as the technology scales down i.e. technology below the deep-submicron (45nm and below), the interconnect delay plays a major role in slowing the speed of device as interconnect delay becomes comparable to gate delay. Interconnects in deep-submicron does not acts as simple linear resistor in fact the parasitic capacitance and inductance associated with it also comes into picture.

The main reason for growth of semiconductor industries is scaling of device which leads to reduction of feature size. With the scaling, the packing density, complexity and circuit chip

size is continuously increasing [2]. To achieve this, the requirement of size of transistors is as small as possible. As the gate dielectric thickness, gate length and packing density scaled down this leads to improve performance and density by integrating more and more devices on same chip which increases chip area. According to theory of scaling [2], for smaller circuits, the speed of circuit enhances. But this theory is not valid for larger circuits. In larger circuits, the interconnect delay plays an important role in determining the performance of circuits. Due to scaling, the feature size reduces which leads to reduction of interconnection area. But due to scaling as the density increases the chip area increases because of higher integration level in larger circuits allows the length of interconnection to increase which may increases the chip area. Hence the effect of scaling of interconnects is shown in interconnect RLC delay. Therefore for larger circuits the interconnect delay is appreciable portion of total delay. Hence for larger circuits the total time delay of circuit is not only decided by device performance.

For scaling, there is a technique used for scaling called constant field scaling. In this technique, the threshold voltage and power supply has to be scaled down to maintain the electric field constant. As the power supply is scaled down, so it is necessary to scaled down the interconnect dimension to make feature size small. In doing this complexity of interconnection will increases, hence chip cross-sectional area increases. As chip area this leads to increase in interconnect resistance and capacitance to increase. As operating frequency increases this leads to increase the effect of inductance of scaled interconnect. Hence the effects of scaled interconnect are increase in RLC delay, crosstalk delay, current density and power consideration. These effects will rapidly increases in deep-submicron technology.

1.2. INTERCONNECT PARASITICS

Due to scaling, today's interconnection wiring of integrated circuits forms a complex geometry that introduces three parasitic- resistance, capacitance and inductance. All of three together have effect on performance of circuit.

1. An increase in propagation delay.
2. An impact on power distribution and energy dissipation.

3. Introduces extra noise sources, which indirectly affects reliability of circuit.

Each wire in a bus network connects transmitters to a set of receivers. Assume that all segments are implemented on a single interconnect layer and are isolated from each other and from silicon substrate by a layer of dielectric material as shown in fig. 1.1. This is representation of interconnect wire having length L, width W and height (or thickness) H.

1.2.1. RESISTANCE

The parasitic resistance of a wire has a significant influence on signal propagation delay. The resistance of wire depends on material used, number and location of contacts and the dimension of wire.

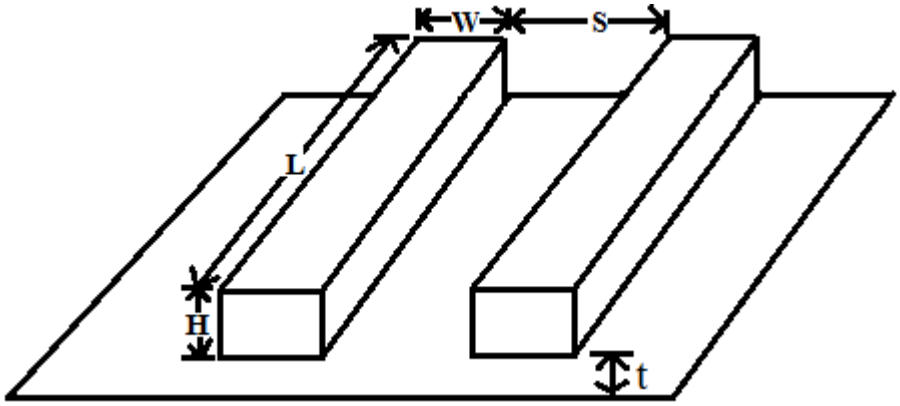

Fig.1.1. Interconnection Dimensions[3]

The resistance of wire is inversely proportion to cross-sectional area A and directly proportional to length L. The resistance of a rectangular conductor as shown in fig 1.1. can be expressed as

$$\boldsymbol{R = \frac{\rho L}{A} = \frac{\rho L}{tW}} \tag{1.1}$$

where ρ is the resistivity of the material (Ω-m).

Eq. 1.1 can be written as follows

$$\boldsymbol{R = \frac{R_s L}{W}} \tag{1.2}$$

where

$$\boldsymbol{R_s = \frac{\rho}{t}} \tag{1.3}$$

R_s is the sheet resistance of the material.

Transitions between routing layers add extra resistance to a wire called contact resistance[5]. It is preferred to avoid excess contacts by keeping wires in a single layer whenever possible to reduce contact resistance. Contact resistance is dependent on size of the contact and contacted material. By making contact larger, contact resistance can be reduced.

At high frequencies, the resistance becomes frequency dependent this effect is called skin effect[5]. The high frequency current flows through the surface of conductor with the current density falling off exponentially with depth into the conductor. The skin depth δ is defined as the depth where the current falls off to a value of e^{-1} of its nominal value.

$$\boldsymbol{\delta = \sqrt{\frac{\rho}{\pi f \mu}}} \tag{1.4}$$

where *f* is the frequency of the signal and μ is the permeability of the dielectric (permeability of free space is $4\boldsymbol{\pi} \times 10^{-7}$ H/m) .

At higher frequency increased resistance may cause distortion and attenuation of the signal being transmitted over the wire. Since clock tend to carry high frequency signal and are enough wide to limit resistance hence the skin effect shows its effects on these line first.

1.2.2. INDUCTANCE

At high switching frequency, inductance plays an important role. Disadvantages of on- chip inductance are reflection of signal due to mismatch, overshoot effects, switching noise due to Ldi/dt voltage drops and inductive coupling between lines.

The inductance of circuit can be expressed with the help of its definition i.e. a change in current passing through inductor generates a voltage drop ΔV.

$$\boldsymbol{\Delta V = L\frac{di}{dt}} \tag{1.5}$$

There are many ways to compute inductance of a wire but the simpler approach relies on the fact the capacitance c and inductance l are related to each other with the following formula[5].

$$\boldsymbol{cl = \varepsilon\mu} \tag{1.6}$$

where Ɛ is the permittivity and μ is the permeability of the dielectric.

The product of the permittivity and permeability defines the speed *v* at which an electromagnetic wave can propagate through medium. The propagation speed in vacuum is two times faster than SiO_2.

$$v = \sqrt{\frac{1}{lc}} = \frac{1}{\sqrt{\varepsilon\mu}} = \frac{c_o}{\sqrt{\varepsilon_r \mu_r}} \quad (1.7)$$

where c_o is speed of light i.e. 30cm/nsec in a vacuum.

1.2.3. CAPACITANCE

The capacitance of wire is a function of its environment, distance from substrate, its shape and the distance from the surrounding wires. Each interconnect wire is surrounded by the other wires on the same layer or on other layers.

The wire has two types of capacitance-

1. Parallel plate capacitance over the ground plane.
2. Fringing capacitance due to fringing fields arises at the edges of conductor having finite thickness.
3. In addition to above capacitances, there is an another type of capacitance i.e. a wire adjacent to another wire on same layer also exhibit capacitance to the neighbouring wire.

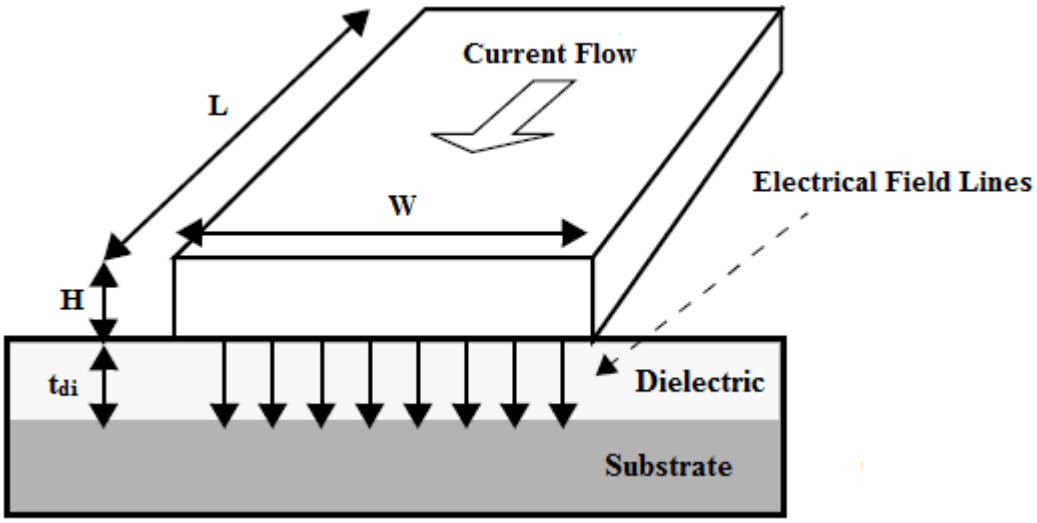

Fig.1.2. Parallel Plate Capacitance model of Interconnect wire[5]

Parallel- Plate Capacitance

An isolated wire over the substrate can be modelled as conductor over the ground plane as shown in fig. 1.2. If the thickness of dielectric is smaller than the width of conductor then electrical field lines are orthogonal to the plates as shown in fig.1.2. The formula of parallel-plate capacitance[5] is

$$C_{pp} = \frac{\varepsilon_{di}}{t_{di}} WL \quad (1.8)$$

where ε_{di} and t_{di} are the permittivity and thickness of the dielectric, respectively. W and L are the width and length of the conductor, respectively. ε is product of permittivity of free space (ε_o) and the relative permittivity of insulating material (ε_r). Value of permittivity of free space (ε_o) is 8.854×10^{-12} F/m. Hence from equ. 1.8., it is possible to say that capacitance is inversely proportional to the separation between the conductors and directly proportional to the overlap between them.

Fringing Capacitance

If the distance over the ground plane becomes comparable to thickness of conductor H then fringing field increases the parasitic capacitance and that capacitance is called fringing capacitance. This capacitance lies between the substrate and side-walls of conductors as shown in fig. 1.3.

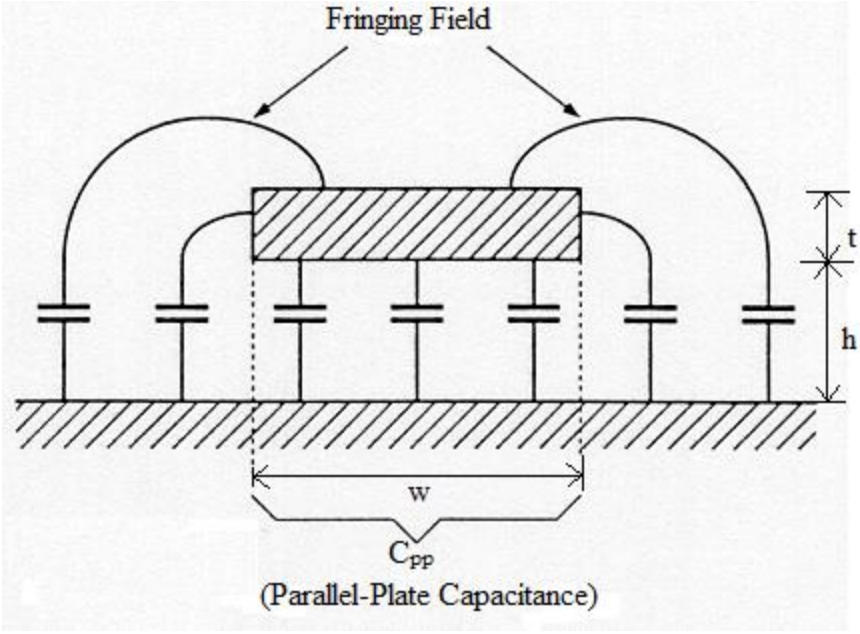

Fig.1.3. Effect of fringing field on capacitance[1]

A set of formulas are used to calculate the interconnect capacitance under the influence of fringing field. There are two different formulas depending on different range of width of conductor[1].

$$C = \varepsilon\left[\frac{w - t/2}{h} + \frac{2\pi}{ln\left(1 + \frac{2h}{t} + \sqrt{\frac{2h}{t}\left(\frac{2h}{t} + 2\right)}\right)}\right] \quad \text{for } w \geq \frac{t}{2} \qquad (1.9)$$

$$C = \varepsilon\left[\frac{w}{h} + \frac{\pi\left(1 - 0.0543.\frac{t}{2h}\right)}{ln\left(1 + \frac{2h}{t} + \sqrt{\frac{2h}{t}\left(\frac{2h}{t} + 2\right)}\right)} + 1.47\right] \quad \text{for } w < \frac{t}{2} \qquad (1.10)$$

These formulas provide accurate approximation within 10% error.

Above capacitance does not include capacitance of neighbouring wires on same layer or different layer. Consider the model which considering capacitance of neighbouring wires on same layer or different layer as show in fig1.4. The total capacitance is now the sum of capacitances between two conductor on same layer, to above layer and to below layer. Consider above and below planes as ground planes.

$$C_{gnd} = C_{top} + C_{bot} \qquad (1.11)$$

$$C_{tot} = C_{gnd} + 2C_{adj} \qquad (1.12)$$

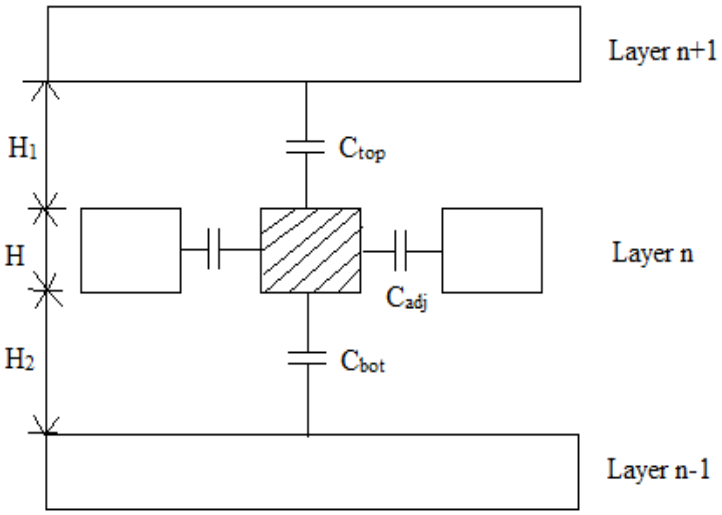

Fig.1.4. Multilayer capacitance Model[4]

1.3. INTERCONNECT DELAY

Earlier interconnect delay does not plays an important role and was ignored. But now due to scaling as feature size reduces due to which interconnection layer increases hence chip size increases. Due to increase in chip area interconnect delay for short interconnect increases. Hence interconnect delay is used to estimate the performance of device.

Interconnections contribute to the delay time by capacitive loading and by distributed-RC delay. Currently, there are basically two delay domains – transmission line delay domain and RC delay domain depending upon circuit parameters.

For RC delay[6],

$$t_d(0\sim50\%) = 0.69\tau \quad (1.13)$$

$$t_r(10\%\sim90\%) = 2.2\tau \quad (1.14)$$

with τ is the RC time constant.

Unfortunately, these formulas gives the rough approximation of transient behaviour of interconnect line.

1.4. METHODS TO REDUCE INTERCONNECT DELAY

In large chip area, due to long resistance interconnect the propagation delay limit the performance of devices. Because length of interconnect is going to increase with increase in size of CMOS integrated circuit. As the length increase, linear increase in both interconnect resistance and capacitance leads to increase the interconnect delay quadratically[7]. Hence it is required to reduce the interconnect propagation delay to make performance of circuit better.

Repeater Insertion

Repeater insertion technique is a technique used for reducing the time delay of long resistive interconnects in integrated circuits. This technique involves dividing the long wire into two or more short wires and inserting a repeater between each pair of short wires as shown in fig.1.5. The propagation delay becomes linear with length by dividing the interconnection into smaller subsection with the use of repeater. It is possible to achieve the shortest total delay, by making the delay of segment connected by the repeaters should be equal to delay of a repeater. By increasing the size of the repeaters the propagation delay can be further improved as the current-driving capability of the inverter is directly proportional to the *W/L* ratio[8].

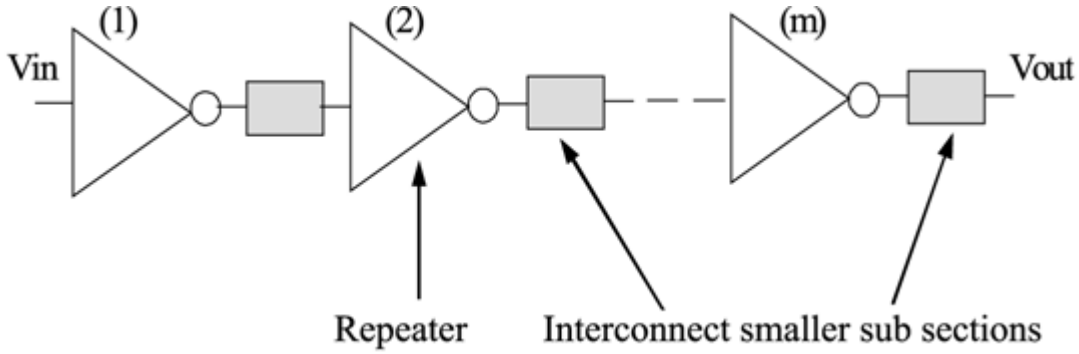

Fig.1.5. Uniform repeater system driving a distributed RLC interconnect[9]

Multilayer Interconnection

It is difficult to connect all the transistors with a single interconnect level. Multilayers interconnections improve propagation delay[8]. The long-distance interconnection uses the upper levels with thicker and wider lines that lead to smaller propagation delays. This can be done by dividing logic master chip into cells[10]. Each cell contains a functional element and it allows the wire to pass through it. In this way multilayers occupy less chip area, which reduces interconnection length and reduces propagation delay because the average interconnection length is inversely proportional to the number of levels [11].

Cascading Drivers

For driving large capacitive loads, cascaded drivers technique is used to reduce the propagation delay[8]. Let the resistance and capacitance of interconnect are R_{int} and C_{int}. As the total propagation delay is proportional to product of resistance and capacitance, therefore it can be written as follows

$$\boldsymbol{T \approx (R_{int} + R_{tr})C_{int}} \qquad (1.15)$$

where R_{tr} is the output resistance of minimal transistor. As we know that propagation delay increases quadratically with length of interconnect. But the R_{tr} is also dominating term. Hence by reducing R_{tr}, the propagation delay can be reduced and this can be done by introducing the larger driver in a wire. The first transistor is the minimal transistor and it drives another driver that is bigger by a factor α, etc. This procedure will continue until a driver that is large enough to drive the whole wire in a sufficient short delay time. The optimal arrangement is the well-known exponential sequence of drivers[12].

The total delay is expressed as

$$\boldsymbol{T = 2.3eR_{tr}C_{tr}ln\left(\frac{C_{int}}{C_{tr}}\right) + R_{int}C_{int}} \qquad (1.16)$$

where C_{tr} is input capacitance of minimum size transistor and e is the base of natural logarithm. Hence, cascaded driver technique reduces the $R_{tr}C_{int}$ term in (1.14), but the $R_{int}C_{int}$ term does not changes. As a result, this method is good when R_{int} is small and C_{int} and R_{tr} are dominating[8].

1.5. COPPER INTERCONNECTS

In earlier times, due to increased packing density and chip area, it leads to increase in resistance of metal due to reduction in line width and there is increase in capacitance which leads to increase in RC delay. Hence copper was used as VLSI interconnects due to its lower sheet resistance. Copper wires conduct electricity more than the aluminium wires due to its less resistance than aluminium wires, which results in high speed than aluminium wires. Copper wires also significantly more reliable over time and more durable, and can be shrunk to smaller sizes than aluminium. Aluminium has a lower melting point (933K) than copper (1357K).

1.6. PROBLEMS OF COPPER INTERCONNECT IN DEEP SUB-MICRON

As copper interconnect replaced an aluminium wires due to its low resistance but as technology scales down to deep sub-micron technology the resistivity of copper increases due to its low mean free path. This increase in resistivity is due to grain boundary and electron surface scattering. The requirement of higher bandwidth is major concern when copper is used as interconnect for higher clock frequency.

1.6.1. GRAIN BOUNDARY SCATTERING

The main feature of polycrystalline materials is grain boundaries. A grain boundary is the interface between two crystallites in a polycrystalline material. Grain boundaries are defects in the crystal structure and tend to decrease the thermal and electrical conductivity of the material. Grain boundaries in polycrystalline films may act like partially reflecting planes located perpendicular to the electric field [13], have an adverse effect on signal attenuation and distortion. Grain boundaries causes electron scattering which leads to reduce the mobility of electron. Smaller the grain boundary, higher the resistivity and slower the speed of electron. With the increase in number of grain boundaries, the resistivity increases. When the number of grain boundary is small, then the resistivity rapidly increases till the certain amount of number of grain boundary after which the increase in resistivity becomes slow.

The mathematical formula for the resistivity of copper under the effect of grain boundary as follows[14]

$$\frac{\rho_g}{\rho_o} = 3\left[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 ln\left(1 + \frac{1}{\alpha}\right)\right] \qquad (1.17)$$

where

$$\alpha = \frac{\lambda}{d}\left(\frac{R}{1-R}\right) \quad (1.18)$$

where ρ_o is the bulk resistivity at 300K, R is resistivity coefficient, λ is the electron mean free path and d is the distance between grain boundaries.

1.6.2. ELECTRON SURFACE SCATTERING

As the width scales down, the mean free path of electron of copper becomes comparable to the width of interconnect. Hence an electron will suffer more reflection at the surfaces. So the collisions with the surfaces will become a significant fraction of the total number of collisions. Electrons scatter when they emit or absorb phonons, encounter impurities in metal alloys and metal or reach the line surface[15].

Various model has been modelled describing the electron surface scattering effect on resistivity. Electron surface scattering effect depends on the copper–barrier interface quality and on the interconnect operation temperature. The surface scattering effect will be less at high temperature. However, the bulk resistivity would be higher. Increase in resistivity is described by determining the extent of elastic collisions suffered by electrons at the interface.

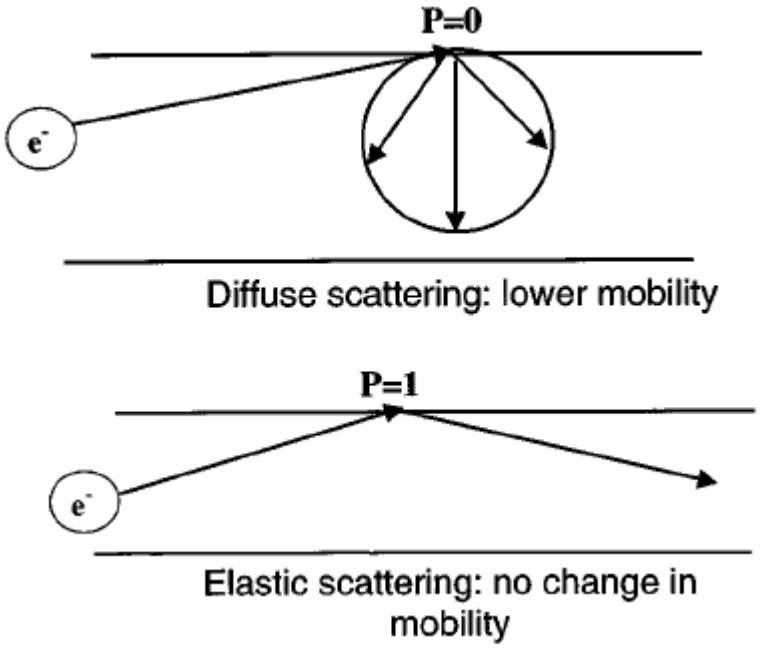

Fig.1.6. Electron Surface Scattering[16]

The fraction of electrons, which suffer elastic collisions at the interface resulting in specular scattering, is modelled by an empirical parameter, whose values lies between 0 and 1[16].

An electron that scatters completely loses the additional momentum that it has gained from

the electric field and leaves the surface in a random direction (P=1). An electron that is specularly scattered does not change its momentum in the directions parallel to the surface (P=0) as shown in fig.1.6.Thus, specular scattering does not contribute in increasing resistivity.

The mathematical formula for the resistivity of copper under the effect of grain boundary as follows[17]

$$\frac{\rho_s}{\rho_o} = 1 + \frac{3}{4}(1 - P)\frac{\lambda}{w} \qquad (1.19)$$

where P is specular scatted coefficient, λ is electron mean free path and w is the width of wire.

1.7. CARBON NANOTUBES AS INTERCONNECT

The most promising solution of copper problem is Carbon Nanotubes (CNT) for future integrated circuits. As CNTs have good electrical properties, high thermal and mechanical strength. CNTs have long mean free paths (MFPs) on the order of several micro meters as compared to Copper at room temperature, which provide low resistivity and possible ballistic transport in intermediate-length interconnects. An isolated CNT can carry current densities in excess of 10^{10} A/cm^2 without any signs of damage, thereby eliminating electromigration reliability concerns that plague nanoscale Cu interconnects.

CNTs are classified as SWCNT (Single-walled Carbon Nanotube) and MWCNT (Multi-walled Carbon Nanotube). SWCNT consists of single shell of graphene sheet, it can have diameters varying with few nanometers to 4nm. MWCNTs is consists of multiple concentric shells of graphene sheets held within by vander waal forces. The distance between two sheets is vander waal distance i.e. 0.34nm. The diameter of MWCNT can vary few nanometers to hundred nanometers depending on technology.

CHAPTER - 2

LITERATURE REVIEW

Farrokh Mahommadi et al.[2]

This paper proposed the effect of scaling on VLSI interconnects. This paper shows that with increase in chip size and other dimensions then interconnect delay time plays a significant role in demonstrating the total circuit delay time. Due to scaling, the feature size reduces which leads to reduction of interconnection area. But due to scaling as the density increases the chip area increases because of higher integration level in larger circuits allows the length of interconnection to increase which may increases the chip area. Hence the effect of scaling of interconnects is shown in interconnect RLC delay. Therefore for larger circuits the interconnect delay is appreciable portion of total delay. Hence for larger circuits the total time delay of circuit is not only decided by device performance.

This paper shows that due to scaling of local interconnect line the response time and the voltage drop of local interconnect line stays the same; but the current density of line increases which leads to device-performance problems, such as electromigration.

This paper also concluded that the voltage drop of long interconnect will increase with scaling. Because the long interconnect response time rises drastically due to scaling, hence a substantial amount of delay and energy is consumed during communication through the interconnection and therefore, the performance of the circuits can suffer from the technological advancement.

Fen Chen et al.[13]

This paper shows that as dimensions of interconnect scaled to the deep-submicrometer level, then width of interconnect lines becomes comparable to MFP of electrons, hence it increases the resistivity of a Cu. The resistance of Copperincreased non-linearly as width of interconnect line decreased. This enhancement occurs due to the increased surface and grain boundary scattering. As almost 50% of the electrons is elastically scatter during the transport of electron from one side to other side wire with width of line below 0.5μm.

In this paper, resistivity in Copperdue to specular reflection at external surfaces is generally modeled according to Fuchs' size-effect theory. This paper shows that it will be important to develop interconnections with smooth surface on all sides to maximize elastic scattering of electrons.

Krishna C. Saraswat et al.[16]

This paper proposed that an increase in resistivity in deep sub-micron technology is due to grain boundary and surface scattering effects and copper barrier oxide layer. This paper proposed that as width scales down to increase the chip density as per industry requirement this leads to increase in length of interconnection due to which the chip area increases. But due to scaling of width of copper interconnects; the mean free path of copper becomes comparable to width due to which rate of electron collisions increases. But depending on type of collision it leads to whether the resistivity of copper increases or not. If the collision is elastic collision then the electron moves in random direction after the change of momentum then it increases resistivity. If the collision is specular collision then there is no change in momentum hence the electron movies in the direction of the electric field. Hence there is no increase in resistivity. This paper proposed the model of copper showing the effect of surface scattering in resistivity of copper.

This paper also proposed the model showing the effect of copper barrier oxide layer on the effective resistivity of copper. This paper shows that as the area of barrier oxide layer increases then this leads to increase in resistivity of copper. That means the resistivity of copper is proportional to thickness of barrier layer. It was also concluded that increase in resistivity of aluminium is slower than increase in resistivity of copper.

Yan Wen et al.[18]

This paper proposed that effect of grain boundary on resistivity of copper. This paper had used the concept of Onho Continuous Casting (OCC) method to maintain the long and thin single crystal copper wire. As in single crystal copper wire there is no grain boundary. Due to availability of grain boundaries, it leads to attenuation and distortion of signal passing through copper. This paper proposed that as annealing temperature increase, the number of grain boundary decreases. With increase in number of grain boundary, the resistivity

increases up to some critical number of grain boundary, after which rate of increase of resistivity becomes slow and comparable to the resistivity of aluminium wire.

This paper also shows that effect of grain boundary on resistivity is not linear unlike the effect of dislocation and lattice vacant sites. As the number of grain boundary is small the change in resistivity is determinable but when the number of grain boundary is higher, the change in resistivity is ignorable. This effect is not linear.

Navin Srivastava et al. [19]

This paper proposed that due to scaling, the resistivity of copper increases due to surface and grain boundary scattering and the presence of highly diffusive barrier oxide layer. Copper interconnect faces many challenges like as temperature rises, it will degrade the interconnect electromigration lifetime, which will limit the current carrying capacity of copper. Due to high increase in resistance of copper interconnect, it will lead in increase in interconnect RC delay not as global interconnect but also as local interconnect. Hence this paper shows that the challenges faced by copper can be overcome by using Carbon Nanotubes as interconnect.

CNT becomes the promising solution of challenges occurred under deep sub-micron technology. Metallic CNT can be used for interconnect application due to its excellent electrical and thermal properties, mechanical stability and high current carrying capacity. A carbon nanotube is thick graphene sheet which is rolled into seamless cylinder having diameter of nanometer range.

Morinobu Endo et al. [20]

This paper proposed that due to unusual chemical and electrical properties of CNTs, they are being used in the fabrication of nanocomposites, nano-electronic sensors and devices. Many efforts have been done to produce cost effective CNT at a large scale. Hence the catalytic CVD method has been used to produce CNT at low cost. This technique is used for the production of both MWCNT and SWCNT using a rotating reactant technique. This can be done by feeding nanoscale catalytic particle and hydrocarbon simultaneously in reaction chamber in their gas phase, in this way CNT can be synthesized in large scale. In production of CNT, the main thing to be remembered is to obtain the purity of CNT because the remained metallic impurities may cause to their toxic properties.

Kaustav Banerjee et al.[21]

This paper proposed a performance of MWCNT based interconnect. Each shell in MWCNTs has different parameters and also there are couplings between neighbouring shells (Inter shell coupling and tunnelling effects). The delay of an MWCNT interconnect is estimated and compared with the traditional copper interconnect. For global and intermediate interconnects level, the resistivity of MWCNTs is much lower than copper wire and becomes increasingly comparable to that of SWCNT bundles. Hence, the delay of MWCNT interconnects is smaller than Copper interconnects and that the improvement in delay performance in the case of MWCNT interconnects increases for longer lengths. For local interconnects the resistivity of MWCNTs is much larger than that of copper wires for lengths around 1 μm. Hence, the delay of MWCNT interconnects at the local level is marginally larger than that of copper.

Hong Li et al. [22]

This paper presented the effect of high frequency on the performance of CNT due to presence of high on- chip inductance. This paper shows that CNT has low skin effect as compared to copper, hence CNT can also be used for high frequency application. This paper also shows that as the frequency increases, the resistance of copper increases. But the resistance and inductance of CNT increases and decreases respectively by small amount and become saturate at high frequency, hence this shows that skin effect get reduced in CNT at high frequency. In CNT, the skin effect gets reduced due to presence of high kinetic inductance at high frequency. The *Q* factor of CNT-based inductors is as high as 3.3 times compared to Copper based inductors without using any magnetic materials. As compared with SWCNT, MWCNT gives better result at high frequency as reduced skin effect in MWCNT compared with SWCNT. Hence large-diameter MWCNT interconnects can be used for future high-frequency interconnects applications including inductor design.

Kaustav Banerjee et al. [23]

This paper proposed the performance, power dissipation and reliability of carbon nanotube bundle interconnects in VLSI. This paper shows that CNT bundles can improve the performance of long global interconnects and minimizing the additional power consumption. For local interconnects, CNT bundle have larger delay than Copper due to large resistance of CNT. CNT bundle interconnects has lower intermediate and global interconnect delay due to

its smaller resistance. Hence, CNT bundles can significantly improve the performance of long global interconnects with minimum additional power dissipation. Repeater insertion methodology can be applied to CNT bundle interconnects (just as with Cu) to minimize power with a small increase in delay. Due to lower resistance of CNT bundle than Cu, vias made up of CNT bundles can very effectively be used as thermal vias to reduce interconnect temperatures.

Taisuke Iwai et al. [24]

This paper proposed that the resistance of multi-walled carbon nanotube (MWCNT) vias, can be lowered by using parallel channel conduction of each tube's inner shells. The contact made at each side is about of good ohmic contact even with the inner shells of MWCNTs by tunnelling. The current increased linearly proportional to the voltage, and this shows the good ohmic contact between the MWCNT bundles and Copper wire. Although the density of MWCNT bundles must be increased by one order of magnitude to obtain resistance as low as that of Copper wire, Hence, it is possible to fabricate CNT interconnects with low resistance and a high tolerance to migration.

Iman Madadi et al. [25]

This paper proposed that the most important parts in carbon nanotube interconnect is its impedance. The delay and power of interconnect is affected by the resistance. In low bias regime, we apply low bias signals (Vb<0.1) thus, no R_{HB} in circuit model of MWCNT. With increase in length, the resistivity decreases. That's why, MWCNT interconnect can be used instead of Copper interconnect at global and intermediate interconnect level. MWCNT interconnect with large number of shells has smaller resistivity as compared to Copper interconnect. In high bias regime, R_{HB} plays an important role in resistance as well as in frequency response. At high bias (0.1V), the dc resistance starts increasing with the increase in the bias voltage.

Brajesh Kumar Kaushik et al. [26]

This paper proposed the effect of driver size and number of shells on propagation delay for MWCNT interconnects at 22nm technology node. This paper also compares the delay through MWCNT and Copper interconnects for various driver sizes and number of MWCNT

shells. The delay ratio (T_{MWCNT}/T_{Cu}) decreases with increase in length of interconnect for various driver sizes and number of MWCNT shells. The propagation delay in MWCNT decreases as compared with Copper with increase in interconnects length irrespective of number of MWCNT shells. It is also observed that as the number of shells are increased the overall propagation delay through interconnect is also reduced.

Feng Liang et al. [27]

This paper proposed that the repeaters insertion into long MWCNT interconnects can effectively reduce the total propagation delay of the MWCNT interconnects. This paper has presented the formula used for the calculation of optimal number of repeaters to minimize the total time delay of MWCNT interconnects line with a driver and a load. Using the same size of repeaters, the minimum time delay of the MWCNT interconnects is apparently smaller than that of its Cu. The optimum number of repeaters of the MWCNT interconnect (is about one third of that in the Cu) is less than that of its Cu. The time delay in the MWCNT interconnects decreases at first to the minimum value, and then nearly linearly increases as the number of repeaters increases.

B. K. Kaushik et al.[28]

This paper presented an analysis of propagation delay for both MWCNT and SWCNT bundles for different interconnect lengths (global) and it also shows the comparison between number of SWCNTs in bundle and shells in MWCNTs for a particular propagation delays and lengths. The parasitic elements of SWCNT bundle and MWCNTs depend on number of metallic SWCNTs in the bundle and number of shells in the MWCNTs, respectively. For both MWCNT and bundled SWCNT, propagation delay increases with increase in interconnect lengths. However, the delay decreases with the increase in number of shells of MWCNT and also with increase in number of SWCNTs in a bundle. For particular interconnect lengths (global), number of SWCNT's in a bundle is more than number of shells in MWCNTs for same propagation delay. Therefore, the area occupied by SWCNT bundles is more than the area occupied by MWCNTs with equivalent number of shells. MWCNTs are more promising candidate than SWCNT bundle in terms of area for certain specified propagation delay and interconnect length in modern VLSI technology.

Nisarg D. Pandya et al. [29]

This paper proposed that MWCNT and bundled SWCNT interconnect has been potentially attractive solution in current deep submicrometer and Nanoscale technology. A comparative analysis has been done between the MWCNT and the bundled SWCNT at different global interconnect lengths in terms of time delay and area. The crosstalk effect in the bundled-SWCNT and MWCNT interconnects is important to analyse because it depends on several factors, such as mutual capacitances etc. It may cause undesired voltage glitch on a bus line due to the transition in one or more adjacent bus lines. The same crosstalk-induced time delay is achieved for fewer numbers of shells using MWCNTs as compared with the number of SWCNTs in a bundle that results in the reduction of the area using MWCNT interconnects. The improvement in the crosstalk induced time delay significantly increases with increasing interconnects lengths, and this improvement is more for the MWCNT as compared with equivalent bundled-SWCNT interconnects. Therefore, MWCNTs can be predicted as more appropriate candidate for future global very large scale integration interconnects.

Naushad Alam et al.[30]

This paper investigated the effect of variations on the resistance and capacitance of CNT bundle and also compare it with the Copper interconnects at the 32nm technology node. The resistance of Copper are higher than CNT bundle and the resistance of Copper increases significantly with reducing interconnect width at global and intermediate interconnects level. The CNT bundle has smaller propagation delay and dissipates less power for Intermediate and global interconnects. The resistance of CNT bundle reduces when the bundle width increases because the number of CNT in the bundle increases with increase in the width and the resistance of bundle is determined as $R_{Bundle} = R_{CNT} / N_{CNT}$. For Local interconnects, the resistance of CNT bundle is higher because smaller number of CNT of smaller diameter is accommodated in the bundle. Moreover, the resistance of CNT bundle Local interconnect remains independent of length. For Local interconnects, Copper wire outperforms CNT bundle.

CHAPTER - 3

EQUIVALENT CIRCUIT MODEL OF COPPER AND MULTI-WALLED CARBON NANOTUBE AS INTERCONNECT

3.1. INTRODUCTION

As the VLSI technology advances, it leads to the development of high speed integrated circuits, in the nanoscale and deep sub-micron technology. Interconnect plays an important role in determining the circuit performance with the increase in clock frequency and shrinking of feature size. As resistance of copper interconnects having cross-sectional dimensions of the order of mean free path of electron (~40nm in Copper at room temperature) at current technology, is increasing exponentially with the combined effect of grain boundary and surface scattering and the presence of diffusion barrier layer[25]. Due to this high resistance, the copper interconnects creates some serious challenges for interconnect delay. In order to overcome these challenges, the bundles of the CNTs can be used as interconnects instead of on-chip Copper interconnects. Due to their great thermal and electrical properties, high mechanical stability and current carrying capacity which typically have current density of order of 10^5 A/cm^2, CNTs are the most promising material to replace copper as interconnects. Due to their covalent bonded structure[30], CNTs can alleviate the significant electromigration (EM) reliability concerns at high temperature as happens in Copper interconnects. Besides these, CNTs have longer mean free path (MFPs) of electron of the order of micrometers, due to which it provide low resistance and hence provides ballistic transport in short-length interconnects.

3.2. COPPER USED AS INTERCONNECTS

In earlier times, due to increased packing density and chip area, it leads to increase in resistance of metal due to reduction in line width and there is increase in capacitance which leads to increase in RC delay[31]. Hence copper was used as VLSI interconnects due to its lower sheet resistance. Copper wires conduct electricity more than the aluminium wires due

to its less resistance than aluminium wires, which results in high speed than aluminium wires. Copper wires also significantly more reliable over time and more durable, and can be shrunk to smaller sizes than aluminium. Aluminium has a lower melting point (933K) than copper (1357K). A model is developed to calculate equivalent circuit parameters for a copper based on interconnect geometry as shown in fig. 3.1.

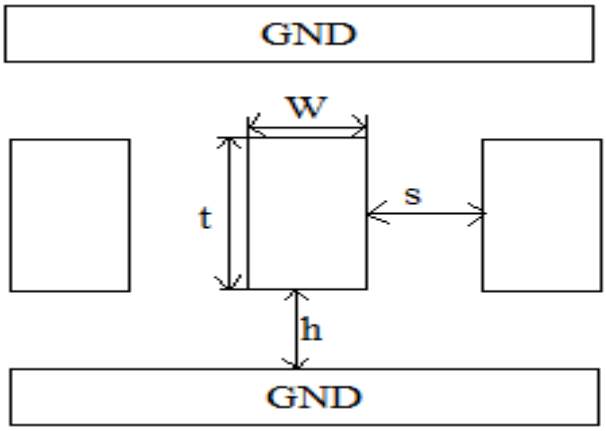

Fig.3.1. Interconnect geometry for Copper[32]

3.2.1. MODELLING PARAMETERS OF COPPER

Resistance

The resistance per unit length of copper interconnect[31] with rectangular cross-sections were calculated using expression-

$$\boldsymbol{r = \frac{\rho L}{Wt} = \frac{\rho_s + \rho_g}{Wt} L} \qquad (3.1)$$

where the resistivity ρ takes into account the effects due to surface scattering and grain boundary scattering.

Inductance

The inductance of copper wire with a rectangular cross section area can be expressed[31] as

$$\boldsymbol{L_s = \frac{\mu_0 L}{2\pi}\left[ln\left(\frac{2L}{W+t}\right) + \frac{1}{2} + \frac{0.22(W+t)}{t}\right]} \qquad (3.2)$$

Where μ_0 is the permeability and given as $\mu_0 = 4\pi \times 10^{-7}$.

Capacitance

The total effective capacitance of the copper interconnect is given by[32]

$$\boldsymbol{C_t = 2C_g + 2C_c} \qquad (3.3)$$

Where C_g is capacitance of area and fringe flux to the underlying plane and expressed as

$$C_g = \varepsilon\left[\frac{W}{h} + 2.04\left(\frac{s}{s+0.54h}\right)^{1.77}.\left(\frac{t}{t+4.53h}\right)^{0.07}\right] \quad (3.4)$$

C_c is coupling capacitor and expressed as

$$C_c = \varepsilon\left[1.41\frac{t}{s}e^{-\frac{4s}{s+8.01h}} + 2.37\left(\frac{W}{W+0.31s}\right)^{0.28}.\left(\frac{h}{h+8.96s}\right)^{0.76}.e^{-\frac{2s}{s+6h}}\right] \quad (3.5)$$

3.3. CARBON NANOTUBES

CNTs are basically one-atom thick sheet of graphite which rolled up as seamless hollow cylinder of diameters of order of nanometers. CNTs can demonstrate any metallic or semiconducting properties, depending on the direction in which they are rolled.

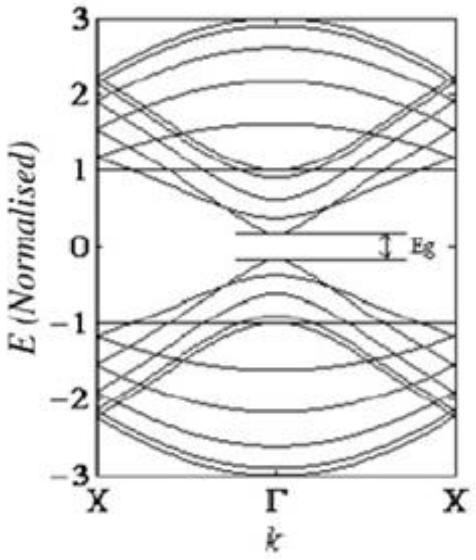

Fig. 3.2(a). Band Structure of Semiconducting CNTs

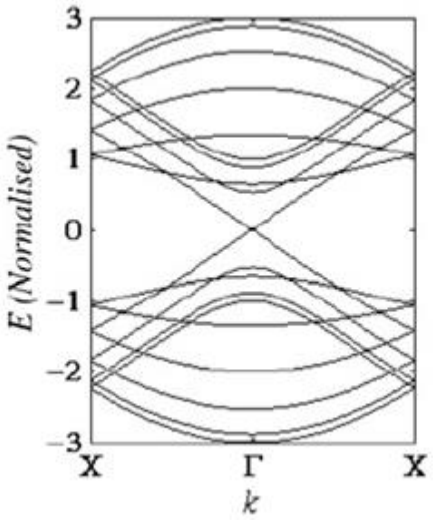

Fig. 3.2(b). Band Structure of Metallic CNTs[33]

The semiconducting CNTs have distinct band gap in their band structure diagram, whereas there is not any band gap for metallic CNTs, as shown in Fig. 3.2[33]. As there is lack of control on chirality, any bundle of CNTs consist of metallic or semiconducting CNTs. But semiconducting nanotubes does not make its contribution in current conduction in interconnects. Changing the direction of rolling of CNTs leads to different chiralities which is determined by chirality index (m, n). When either m or n is zero then it is zigzag chirality as shown in fig.3.3. When m and n both are equal then it is armchair chirality, otherwise for all other cases they are called chiral.

3.4. SYNTHESIS OF CNT

Synthesis of CNT is the method of production used to create carbon nanotubes. They are essentially constructed of a lattice work sheet of graphite that is rolled into a cylindrical shape. The most common methods of used in modern science include

1. Arc discharge method
2. Chemical vapour deposition
3. Laser ablation (vaporization).

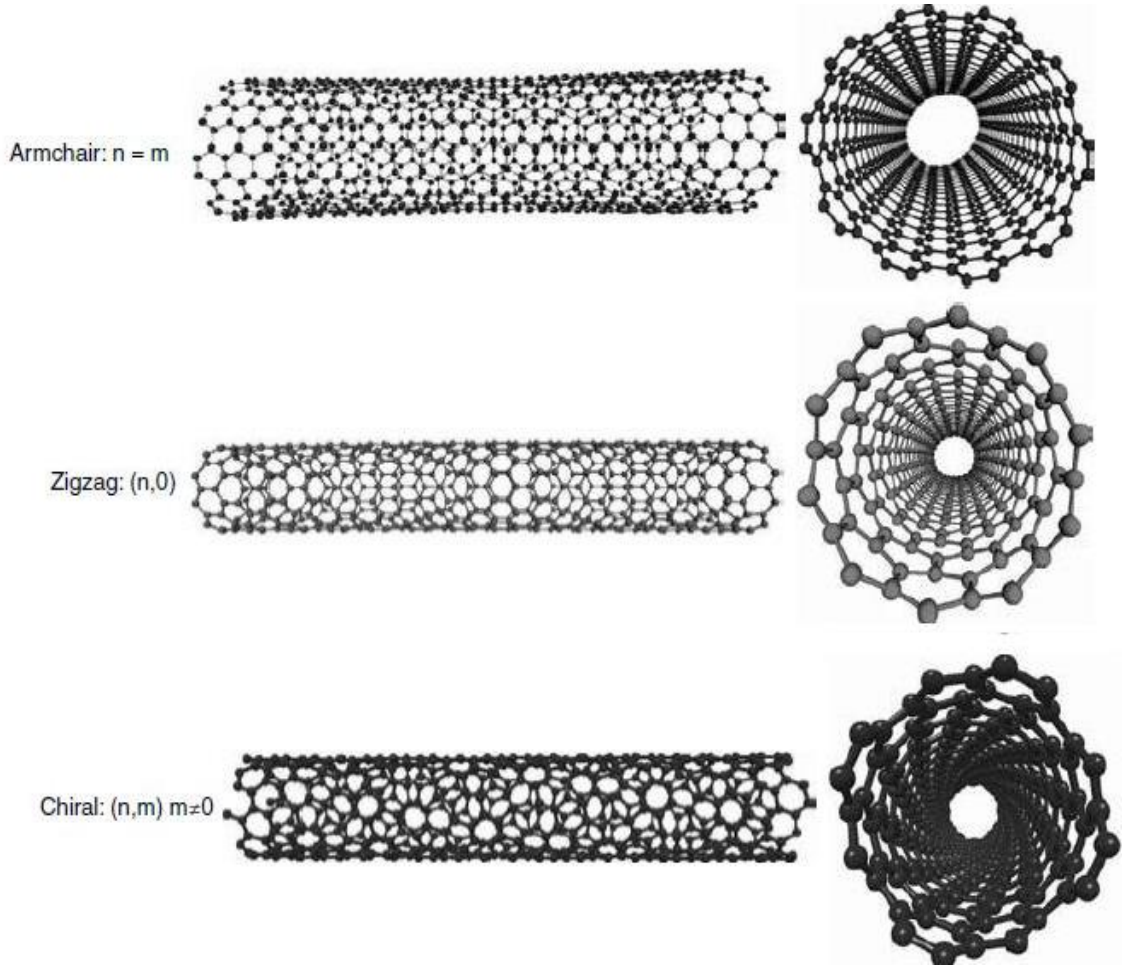

Fig.3.3. Different configuration of CNTs depending on the direction in which they are rolled[36].

3.5. ELECTRONICS PROPERTIES OF CNTs

Electronic band structure is the most exciting property of nanotube. Nanotubes can be metallic or semiconducting, depending on their helicity and diameter. The armchair tubes are always metallic, whereas the zigzag and chiral tubes can be either metallic or semiconducting.

The electronic conduction process in nanotubes is quantum limited because in the radial direction, the electrons are restricted in the singular plane of the graphene sheet. The conduction occurs in metallic armchair tubes through gapless modes [36] because the conduction and valence bands always cross each other at Fermi energy for a certain special wave vector. In most of the chiral tubes, the one-dimensional band structure shows an opening of the gap at Fermi energy and hence, has semiconducting properties.

However, zigzag and chiral tubes also become conducting when one of the sub-bands crosses the *K* point. When the diameter of the tubes increases, the band gap (which varies inversely proportional to the tube diameter) tends to zero, yields a zero-gap semiconductor i.e. equivalent to the planar graphene sheet. Hence, in a MWCNT, the electronic structure of the smallest inner tubes is superimposed by several outer, larger planar graphene like tubes.

3.6. MECHANICAL PROPERTIES OF CNTS

Apart from electronic properties, the mechanical behaviour of nanotubes is also important. MWCNTs are one of the stiffest materials ever made.

As carbon-carbon covalent bonds are one of the strongest in nature, a structure based on a perfect arrangement of these bonds oriented along the axis of nanotubes produces a strong material. SWCNTs have Young's modulus as high as 1-5 TPa[35]. It have been predicted that the softening of CNT increases with increasing tube radius. For MWCNTs, the actual strength is affected by the sliding of individual graphene cylinders with respect to each other. Fracture can occur in a nanotube via collapse of the hollow. This provides extra absorption of energy and increased toughness in a composite. The high Young's modulus suggests that the nanotubes have high bending moments. Bending in nanotubes depends on various parameters such as the nanotube wall thickness, size of the hollow interior and tube size. Nanotubes can sustain extreme strains (40%) in tension without showing signs of plastic deformation, bond rupture or brittle behaviour.

3.7. BALLISTIC FLOW IN CNTs

Ideally any perfect metal tube is always a ballistic conductor. In the ballistic conductor, the resistance of conductor is length independent of the conductor. In other words, all electrons that are injected from one end of the tube should have to reach the other end without a single electron loss. The ballistic electronic transport occurs when the length of the conductor is

smaller than the electronic mean free path. On the other hand, the conductors should have to follow ohm's law and thus dependent of length of the conductor.

In the band structure of metallic carbon nanotubes, there are two distinct linear bands. One band is formed by bonding of molecular orbitals and another one is formed by anti-bonding of molecular orbitals, and the electrons move in opposite directions w.r.t the direction of electron in these two bands. This keeps them moving in a single direction, and that means no scattering and, hence they are ballistic in nature.

The basic electrical properties of semiconducting carbon nanotubes changes when they are placed inside a magnetic field. The band gap of semiconducting nanotubes got narrowed down steadily in the presence of a strong magnetic force. It is demonstrated that in the presence of very high magnetic fields, the band gap get disappear completely and the semiconducting nanotubes becomes a metal.

3.8. TYPES OF CNTs

There are two types of CNTs follows as

3.8.1. SINGLE-WALLED CARBON NANOTUBES (SWCNTs)

SWCNTS consists of one graphene shell and diameter ranging from .4nm to 4nm. It has electron mean free path of the order of a micron and achieve ballistic transport over long lengths.

SWCNTs can be metallic or semiconducting. SWCNTs can be metallic when the difference between the chiral indexes is an integer multiple of 3 i.e. m-n=3i. For other cases, they are semiconductor. Armchair SWCNTs are always metallic. Due to the high resistance of an isolated SWCNT, so it requires the use of a bundle of SWCNTs to form a low-resistance interconnect. The minimum inter tube spacing observed in SWCNT bundles is 0.32 nm, i.e. van der gap. All SWCNTs of such a bundle are not metallic.

3.8.2. MULTI-WALLED CARBON NANOTUBES (MWCNTs)

If several SWCNTs of different diameter are nested concentrically inside one another, the resulting structure is called a multi-walled carbon nanotube (MWCNT). MWCNTs are always metallic. MWCNTs consist of several coaxial CNT shells as shown in Fig. 3.4. and each shell in an MWCNT can have different chirality depending on the direction they are rolled up, which implies that the shells in MWCNT may be metallic or semiconducting.

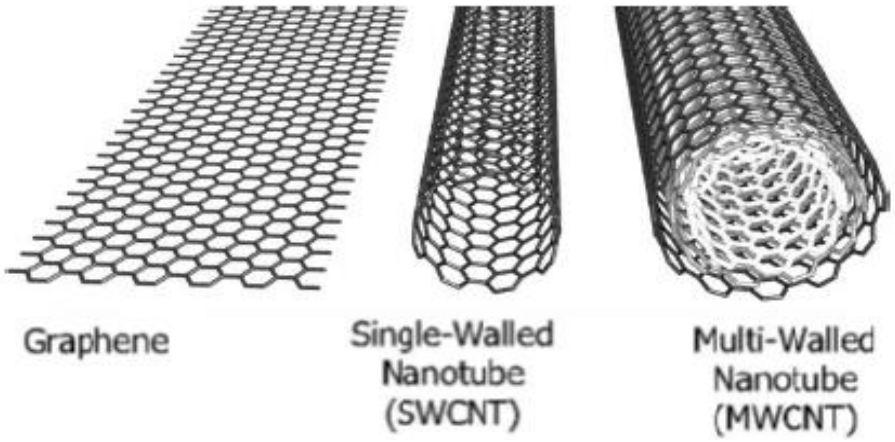

Fig.3.4. Schematic of a 2-D grapheme sheet, single-walled and multi-walled carbon nanotubes[33]

3.9. MWCNTS VERSUS SWCNTS

- As interconnect material, MWCNT having lower conductivity and is less preferable to the relatively higher conductivity SWCNTs[34].
- Longer mean free path (about 1μm) of SWCNT as compared to that of MWCNT (a few nm).
- MWCNTs are always metallic whereas SWCNTs can be either metallic or semiconducting depending on their chirality.
- Moreover, metallic SWCNTs have similar current carrying capacity as MWCNTs but are difficult to fabricate than MWCNTs, due to easier control of the growth process of MWCNTs.
- Due to its simple structure, SWCNTs can be modelled more easily than MWCNTs. In fact, while most CNT interconnect fabrication efforts have targeted MWCNTs, nearly all modelling efforts are focused on the analysis of isolated SWCNTs or SWCNT bundles.
- For an SWCNT bundle, since all nanotubes in the bundle are assumed to have identical diameter, they can be easily transformed into a simple circuit model: The effective resistance per tube and kinetic inductance per tube are divided by the number of SWCNTs, and the quantum capacitance per tube is multiplied by the number of SWCNTs. In MWCNT, different shells have different diameters, which further have different number of channels and different MFPs, resulting in different circuit parameters. Hence, the parameters of each shell cannot be combined in a simple way as in the case of SWCNT bundles[35].

3.10. MWCNT AS INTERCONNECTS

If several SWCNTs of different diameter are nested concentrically inside one another, the resulting structure is called a multi-walled carbon nanotube (MWCNT). The diameter of the innermost and outermost shells is D_{min} and D_{max}, respectively. The distance between nanotube centre and the ground plane is *H*. The spacing between shells corresponds to the van der Waals distance between graphene layers in graphite, which is $d \approx 0.34$nm(as shown in fig.3.5). Because of its large diameter, the shells of an MWCNT would be conductive even if they are of semiconducting chirality.

It is a semiconducting structure and has an energy gap, as shown in Fig. 3.6[37]. At room temperature (T = 300 K), the thermal energy, denoted by k_BT is equal to 0.0258 eV approximately, where k_B is the Boltzmann constant.

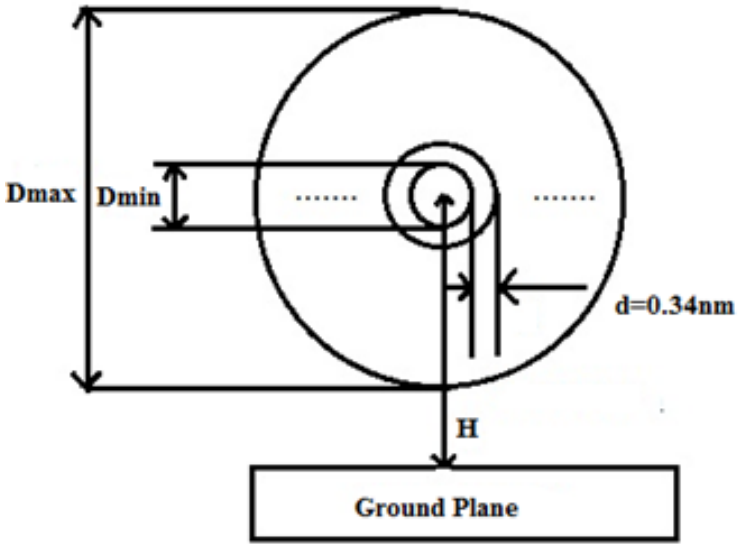

Fig.3.5. Cross-section view of MWCNT[38]

From Fig.3.6, it has been observed that for MWCNT, the energy difference between the conduction band edge (*EC*) and the Fermi level E_F is smaller than 0.0258 eV, which indicates that when the diameter of MWCNT is around 20 nm or larger, these energy differences will be smeared by the environment temperature.

In addition, even if the energy difference between the sub bands and E_F is larger than k_BT, this energy difference is relatively small due to the large density of states in large diameter shells.

The probability (f_i) of finding electrons in those sub bands to appear at E_F follows the Fermi–Dirac distribution function:

$$f_i = \frac{1}{e^{\frac{|E_i - E_f|}{k_B T}} + 1} \tag{3.6}$$

Where, E_i is the lowest (or highest) value for the sub bands above (or below) the Fermi level E_f.

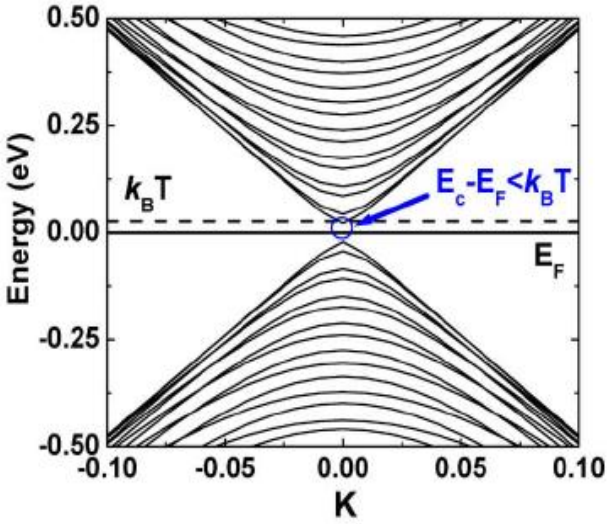

Fig.3.6. Band structure of a zigzag (256, 0) carbon nanotube[37]

As there are large number of sub bands in large-diameter shells, their effect on the probability could be large, hence there can be large number of conducting channels. Thus, since MWCNTs have many large-diameter shells, they could turn out to be good electrical conductors and would be very attractive as possible interconnect materials.

3.10.1. NUMBER OF CHANNELS FOR MWCNT

The number of conducting channels for each shell is

$$N_{chan/shell} = \Sigma_{subbands} \frac{1}{e^{\frac{|E_i - E_f|}{k_B T}} + 1} \tag{3.7}$$

where E_i, is the highest (or lowest) value for the sub-band below (or above) the Fermi level E_F[37]. k_B and *T* are the Boltzmann constant and absolute temperature respectively.

The number of channels per shell can be approximated to

$$\frac{N_{chan}}{shell}(D) = aD + b, for\ D > 3nm \tag{3.8}$$

where, D is the shell diameter, a=0.1836 nm^{-1}, and b=1.275[39]. The number of shells are counted from outer to inner as 1, 2,…, *n*. Assuming an average value of diameter ratio

D_{min}/D_{max} to be 0.5[37]. Hence the number of shells *n* of the MWCNT is

$$\boldsymbol{n = 1 + int\left[\frac{D_{max} - D_{min}}{2d}\right]} \quad (3.9)$$

where, "int [.]" indicates that only the integer part is taken into account.

The diameter of the i^{th} shell is given by[37]

$$\boldsymbol{D_i = D_{max} - 2d(i-1), for\ 1 \leq i \geq n} \quad (3.10)$$

The diameter of innermost shell (as shown in Fig.3.5.) is given as

$$\boldsymbol{D_i = D_{max} - 2d(n-1)} \quad (3.11)$$

The number of conducting channels of the i^{th} shell is given by

$$\boldsymbol{N_i = aD_i + b} \quad (3.12)$$

Hence, the total number of conducting channels is given by the sum of the conducting channels (N_i) of all the shells.

3.11. MWCNT EQUIVALENT CIRCUIT MODEL

The equivalent circuit model for an individual shell of an MWCNT can be obtained on the basis of the model of SWCNT, which is shown in Fig.3.7[37].

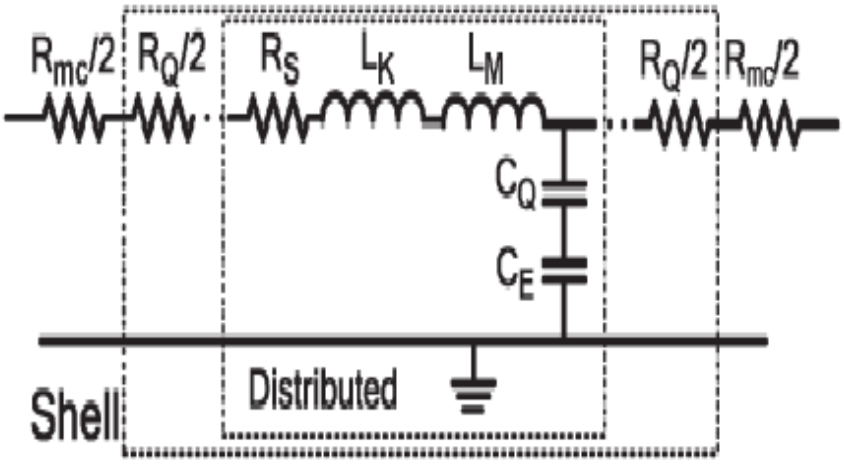

Fig.3.7.Equivalent circuit model of an individual shell[38]

3.11.1. RESISTANCE OF SHELL

The resistance of shell of an MWCNT consists of three parts: quantum resistance R_Q , scattering induced resistance R_S, and imperfect contact resistance R_{mc}.

Scattering induced resistance occurs only when the length of nanotube is larger than the mean free path of electron (MFP). R_Q and R_S are intrinsic and R_{mc} presents due to imperfect metal-nanotube contact.

R_Q is the fundamental quantum resistance associated with MWCNT shell of length less than electron MFP. For this type of length, electron transport in the nanotube is always be ballistic and hence resistance is independent of length.

The total shell resistance is given by[30]

$$\boldsymbol{R_{shell} = R_Q + R_S L = \frac{h}{2e^2 N}\left(1 + \frac{L}{\lambda}\right)} \quad (3.13)$$

Where, $h/2e^2$ = 12.9kΩ, and L is length of nanotube, λ is the MFP of shell and N is the number of conducting channels presents in the shell.

The value of imperfect contact resistance R_{mc} varies from zero to hundreds of kilo-ohms depending on different growth process. Now, it has been observed that R_{mc} in MWCNT could be very small compared to the total resistance. It has been observed that the value of MFP plays an important role in determining the resistance of the nanotube. It has been proven that the MFP of metallic nanotube is directly proportional to the shell diameter (D). The MFP for metallic MWCNT at room temperature is λ = 1000.D

3.11.2. INDUCTANCE OF SHELL

The inductance of any conductor determines the energy stored due to motion of electron carrying current through it.

There are the two types of inductances for MWCNT-

Magnetic Inductance

The energy stored due to motion of electron generates the current I in the presence of magnetic field is $(1/2)L_{magnetic}I^2$, where $L_{magnetic}$ is magnetic inductance.

The magnetic per unit length of a shell is given by[37]

$$\boldsymbol{L_{magnetic} = \frac{\mu}{2\pi} cosh^{-1}\left(\frac{2H}{D}\right)} \quad (3.14)$$

Kinetic Inductance

For a net current to flow through a conductor, there are an excess number of electrons moving in the direction opposite to current flow. In a 1-D conductor, there is low density of states at the Fermi energy level (E_F), and then these excess electrons can only be added at available quantum energy states above E_F, only if they have a higher kinetic energy. This

additional kinetic energy, stored in the moving electrons responsible for current flow in a 1-D conductor, is determines as (1/2) $L_K I^2$, where L_K is kinetic inductance.

The kinetic inductances per unit length of a shell is given by[37]

$$\boldsymbol{L_{K/channel} = h/2 \times 2e^2 v_F \cong 8nH/\mu m} \quad (3.15)$$

$$\boldsymbol{L_{K/shell} = L_{K/channel}/N} \quad (3.16)$$

The magnetic inductance is to be neglected compared with the kinetic inductance.

3.11.3. CAPACITANCE OF SHELL

Whenever an external voltage is applied to conductor, it will affect its electrochemical potential energy in two ways.

Electrostatic Capacitance

The change in electrostatic potential energy whenever a charge δQ is added to conductor and is given as $(\delta Q)^2/(2C_E)$, where C_E is the electrostatic capacitance.

The electrostatic capacitance between a MWCNT and a ground plane is given by[37]

$$\boldsymbol{C_E = (2\pi\varepsilon)/\ln\left(\frac{H}{D}\right)} \quad (3.17)$$

Quantum Capacitance

Due to the low density of states at the E_F, the charge δQ has to occupy available quantum energy states above the E_F. Hence, the additional quantum energy is to be required to add charge δQ to these higher energy states can be determined as $(\delta Q)^2/(2C_Q)$, where C_Q is its quantum capacitance**.**

The quantum capacitance per unit length of a shell is given by[37]

$$\boldsymbol{C_{Q/channel} = 2 \times 2e^2/hv_F \cong 193aF/\mu m} \quad (3.18)$$

$$\boldsymbol{C_{Q/shell} = C_{Q/channel}/N} \quad (3.19)$$

Shell to shell Capacitance

The potentials of different shells of MWCNT cannot be assumed to be equal as in the case of SWCNT bundles and the circuit parameters of different shells vary in MWCNT. Hence it induces shell to shell capacitive coupling. This coupling capacitance is almost similar to electrostatic capacitance and is very large due to the small separation between two adjacent

shells. The shell to shell capacitance per unit length (Cs) can be obtained by using coaxial capacitance formula.

$$C_S = \frac{2\pi\varepsilon}{ln\left(\frac{D_{out}}{D_{in}}\right)} = \frac{2\pi\varepsilon}{ln\left(\frac{D_{out}}{D_{out}-2d}\right)} \quad (3.20)$$

where D_{out} and D_{in} are the outer and inner diameters of adjacent coaxial shells respectively and d is vander waals gap(=0.34nm) .

3.11.4. EFFECTS IN MWCNTs

An important physical effect in MWCNTs is the **tunnelling effect** occurs between two adjacent shells[40]. However, the tunnelling effect would be exponentially dependent on gap between two adjacent shells. Since this gap between shells (shell interval) of MWCNT can be assumed to be 0.34 nm, a parameter is introduced i.e. normalized tunnelling conductivity (σ) that includes shell interval dependence.

The inter shell tunnelling conductance per unit length can be derived as

$$G_T = \sigma\pi D \quad (3.21)$$

where, σ is normalized tunnelling conductivity at d = 0.34 nm and D is the shell diameter. The tunnelling conductance is proportional to the diameter. This is because there are more atoms in a larger diameter shell and tunnelling is more likely to take place.

Another effect is the **magnetic coupling between the shells** in an MWCNT. Due to the large diameter and small thickness of shell, hence each shell can be treated as an ideal sheet cylinder with zero thickness.

The mutual inductance per unit length between different shells can be derived as

$$M_{shell} = \frac{\mu}{2\pi}\left(ln\frac{4L}{D_{out}} - 1 + \frac{D_{out}+D_{in}}{\pi L}\right) \quad (3.22)$$

Where, L is the length, and D_{out} and D_{in} are the diameters of the outer and inner shells of of MWCNT, respectively.

From (3.22)[40], the mutual inductance between shells can be assumes to very small in the order of pH/μm, which is much smaller than the kinetic inductance of each shell (of the order of nH per μm). Hence, the mutual inductance is ignored.

3.12. EQUIVALENT DISTRIBUTED CIRCUIT MODEL FOR MWCNT INTERCONNECT

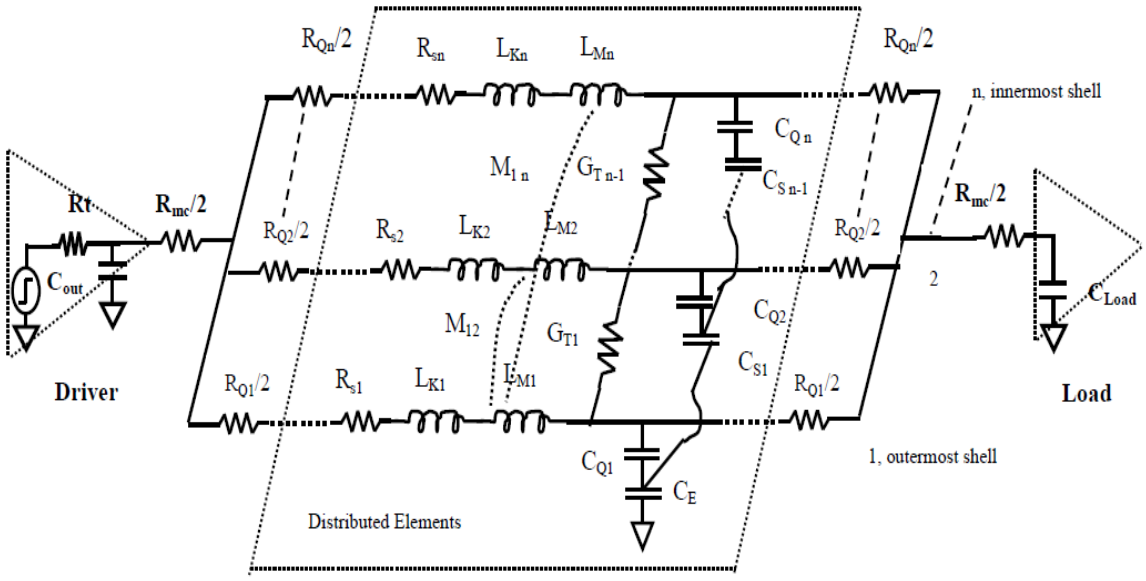

Fig.3.8 Equivalent distributed circuit model of an MWCNT with n shells[37]

An equivalent distributed circuit model for MWCNT interconnect is proposed, as shown in fig.3.8[37]. The values of resistances, capacitance and inductances have been calculated using the formulas from (3.13) to (3.22) as explained in section 3.11. The quantum capacitance C_Q is in series with electrostatic capacitance (including shell-to-shell capacitance C_S and ground capacitance C_E). Note that there is only one total ground capacitance C_E in the model shown in Fig.3.8. This is because only the outermost shell has the electrostatic interaction with the ground, whereas the inner shells are shielded. For shell to shell capacitance and tunnelling, only neighbouring shells are involved. Therefore, for n shells, there is only $n - 1$ number of C_S and G_T.

CHAPTER - 4

EFFECT OF CHANGE OF DIAMETER RATIO ON PARASITIC ELEMENTS OF MWCNT

4.1. INTRODUCTION

In last chapter, the equ. (3.13) to (3.22) is used for the calculation of resistance, inductance and capacitance by assuming D_{min}/D_{max} equal to 0.5. In this chapter the effect of variation of diameter ratio from 0.4 to 0.8 will be observed on the equivalent R, L and C for 32nm, 22nm and 16nm technology nodes. With increase in diameter ratio (D_{min}/D_{max}), the number of shell decreases hence the number of overall conducting channel decreases. Each shell has different diameter so each shell has different number of conducting channels. From the equ. (3.12), it has been observed that the shell having larger diameter will have higher number of conducting channels. The variation of number of conducting channels for each shell versus shell diameter is plotted in fig.4.1. for metallic inner shells[42].

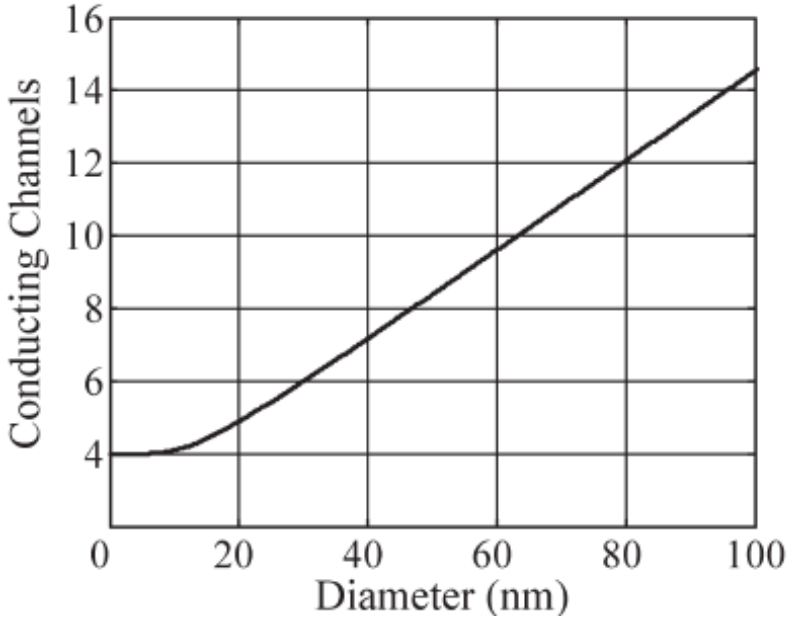

Fig.4.1. Number of conducting channels for shells of different diameters[42]

The variation of number of conducting channel has its effect on equivalent resistance, inductance and capacitance.

4.2. INTERCONNECT PARAMETERS USED FOR CALCULATION

As discussed earlier, that interconnect equivalent model contains three parasitic elements- resistance, capacitance and inductance. The value of these parasitic elements for MWCNT as interconnects for different technology nodes i.e. 32nm, 22nm, 16nm has been calculated according to the formula discussed above by using MATLAB. The outermost diameter of MWCNT is set equal to minimum width of interconnects at each technology node. The length of interconnect has been varied from 100μm to 1000μm at intermediate level. The other different parameters used for calculation for intermediate level of interconnects for 32nm, 22nm and 16nm technologies have been obtained from ITRS 2006 as summarized in table 4.1[43].

Table 4.1. ITRS 2006 based simulation parameters for intermediate level[43]

Technology Nodes	32nm	22nm	16nm
Width(nm)	32	22	16
A/R(Aspect Ratio)	2	2	2
Thickness,H(nm)	64	44	32
Diameter of Outermost Shell(nm)	32	22	16
ILD Thickness, t_{ox}(nm)	54.4	39.6	25.2
ε_{ox}, Relative Permittivity	2.25	2.05	1.75

4.3. CALCULATION OF PARASITIC ELEMENTS

4.3.1. CALCULATION OF RESISTANCE

As the diameter ratio decreases, the number of shell increases. In MWCNT each shell contains different number of conducting channel depending on its shell diameter. With increase in number of shell, the total number of overall conducting channel of MWCNT increases, therefore the conductance increases and resistance decreases. As per equ. (3.13.), the resistance is inversely proportional to conducting channel.

Fig.4.2. to fig 4.4. shows the effect of variation of diameter ratio and length of interconnect on resistance at 32nm, 22nm and 16nm technology, respectively.

From fig.4.2 to 4.4, it is observed that as technology node decreases from 32nm to 16nm, the value of resistance increases because for higher technology, the diameter of each shell of MWCNT is higher, hence the number of conducting channels increases It has been observed that as diameter ratio decreases, the value of resistance decreases for a particular technology. As the length of interconnect increases, the resistance of MWCNT increases for all three of technologies and for all diameter ratio because the resistance of MWCNT is proportional to length of interconnect.

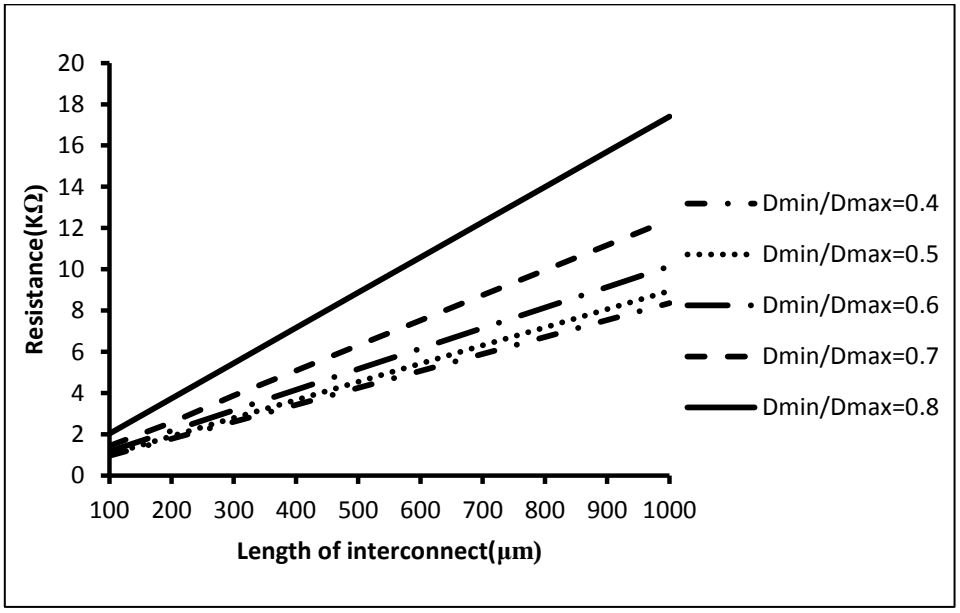

Fig. 4.2. Resistance v/s Length for different diameter ratio at 32nm technology

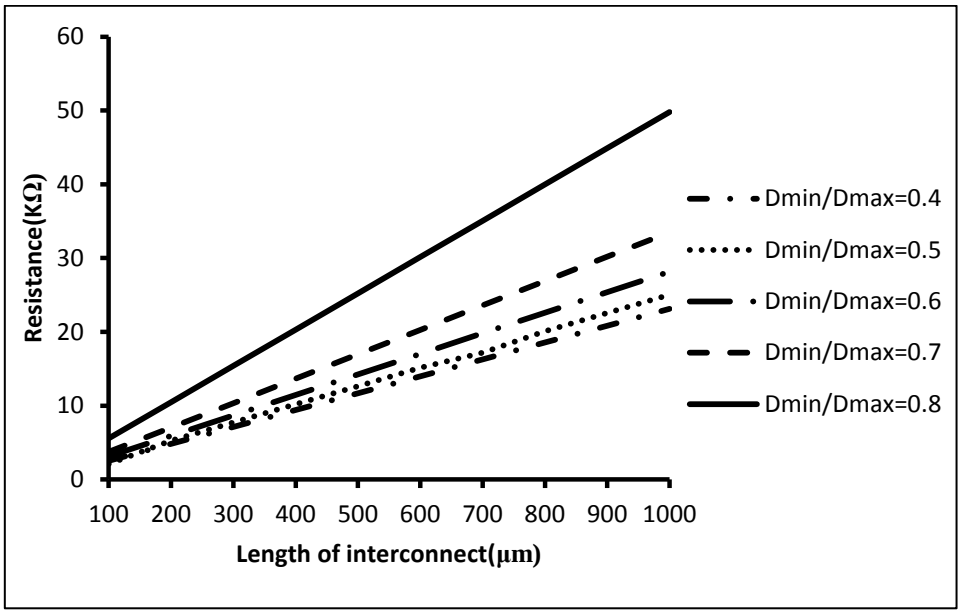

Fig .4.3. Resistance v/s Length for different diameter ratio at 22nm technology

4.3.2 CALCULATION OF INDUCTANCE

As the diameter ratio decreases, the number of shell increases. In MWCNT each shell contains different number of conducting channel depending on its shell diameter. With increase in number of shell, the total number of overall conducting channel of MWCNT increases As per equ. (3.16), kinetic inductance is inversely proportional to number of overall conducting channel. Hence with increase in number of shells, inductance decreases.

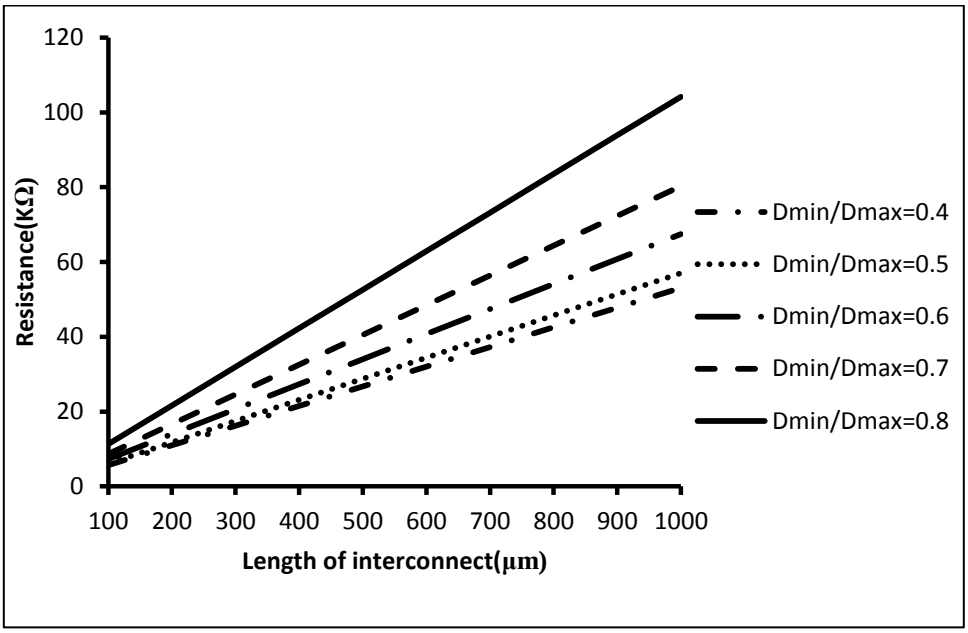

Fig.4.4. Resistance v/s Length for different diameter ratio at 16nm technology

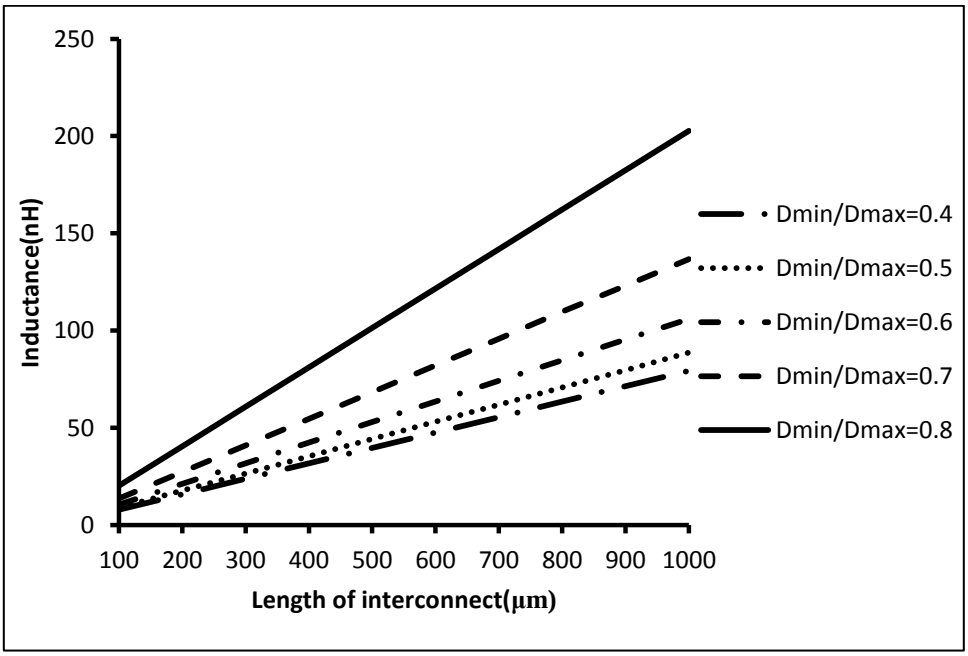

Fig.4.5. Inductance v/s Length for different diameter ratio at 32nm technology

Fig.4.5. to fig 4.7. shows the effect of variation of diameter ratio and length of interconnect on inductance at 32nm, 22nm and 16nm technology, respectively. It is observed that as technology node decreases from 32nm to 16nm, the value of inductance increases because for higher technology, the diameter of each shell of MWCNT is higher, hence the number of conducting channels increases.

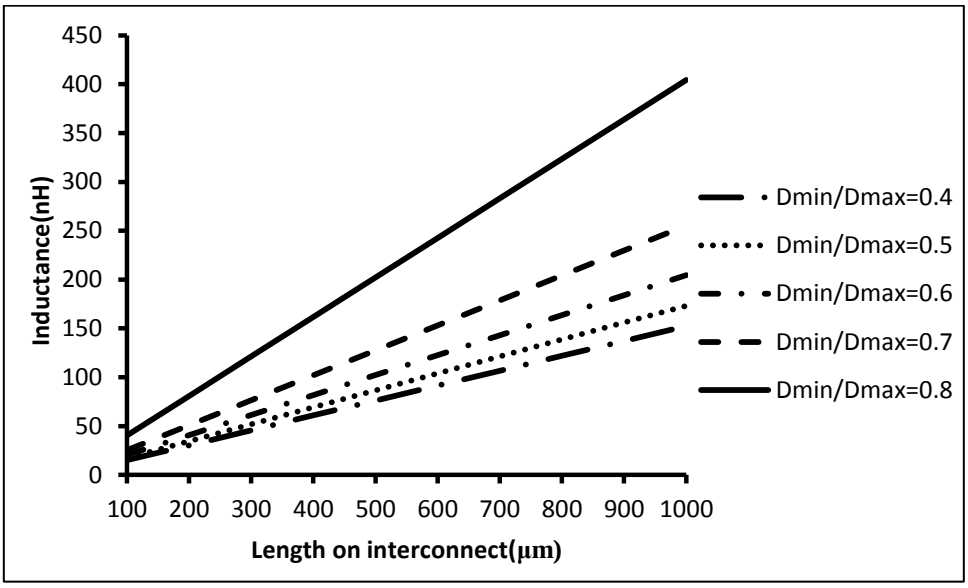

Fig.4.6. Inductance v/s Length for different diameter ratio at 22nm technology

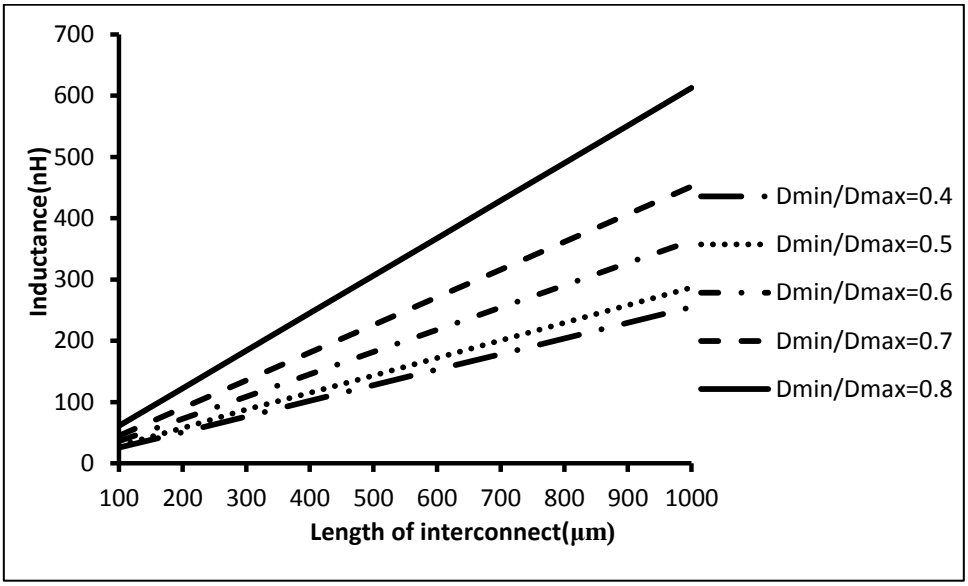

Fig.4.7. Inductance v/s Length for different diameter ratio at 16nm technology

It has been observed that as diameter ratio decreases, the value of inductance decreases for a particular technology. As the length of interconnect increases, the inductance of MWCNT

increases for all three of technologies and for all diameter ratio because the inductance of MWCNT is proportional to length of interconnect.

4.3.3. CALCULATION OF CAPACITANCE

As the diameter ratio decreases, the number of shell increases. In MWCNT each shell contains different number of conducting channel depending on its shell diameter. With the increase in number of shell, the total number of overall conducting channel of MWCNT increases. With increase in number of conducting channel, the distance between the adjacent conducting channels reduces, as the capacitance is inversely proportional to distance between two conductors, hence the capacitance increases. Also with increase in number of conducting channels, crosstalk capacitance also increases. Hence with increase in number of shells, the equivalent capacitance increases.

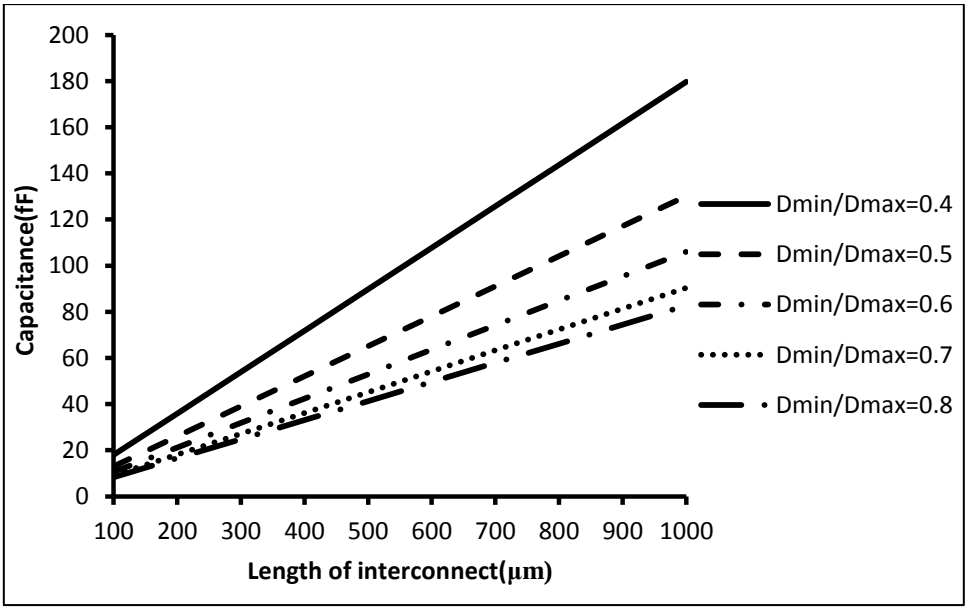

Fig.4.8. Capacitance v/s Length for different diameter ratio at 32nm technology

From fig.4.8. to fig.4.10. shows the effect of variation of diameter ratio and length of interconnect on capacitance at 32nm, 22nm and 16nm technology, respectively. It has been observed that as technology node decreases from 32nm to 16nm, the value of capacitance decreases because for higher technology, the diameter of each shell of MWCNT is higher, hence the number of conducting channels increases, hence capacitance increases. It has been observed that as diameter ratio decreases, the value of capacitance increases for a particular technology. As the length of interconnect increases, the capacitance of MWCNT increases

for all three of technologies and for all diameter ratio because the capacitance of MWCNT is proportional to length of interconnect.

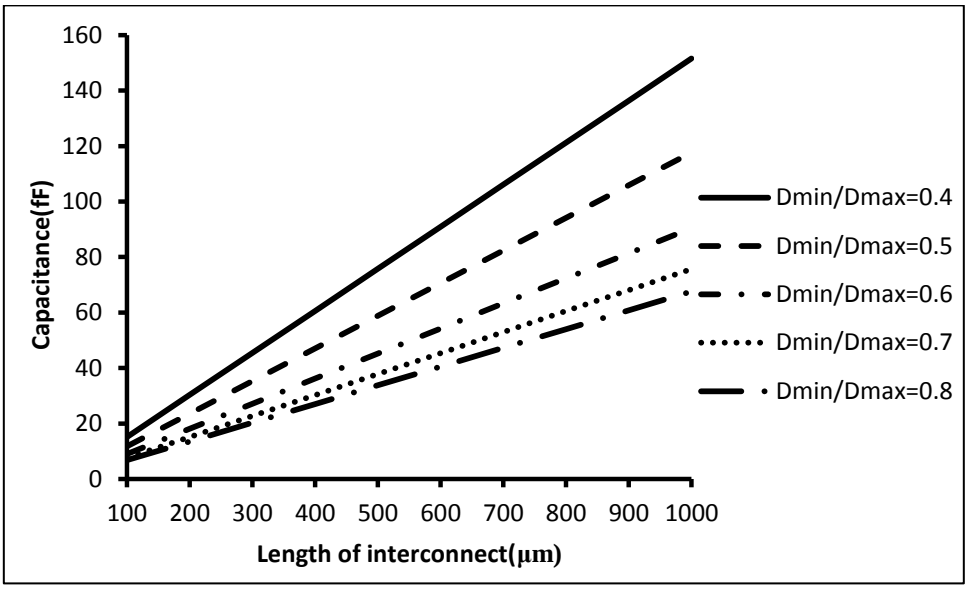

Fig.4.9. Capacitance v/s Length for different diameter ratio at 22nm technology.

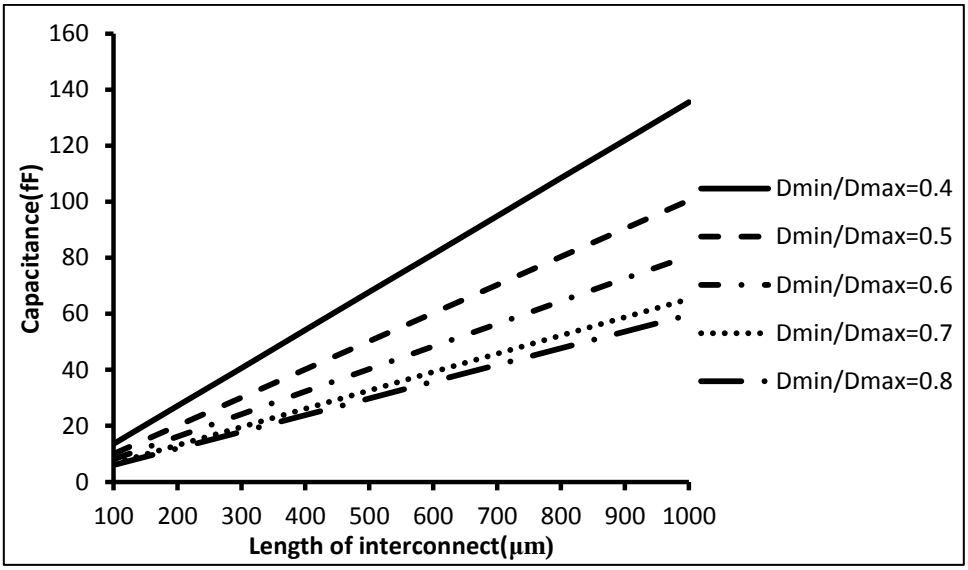

Fig. 4.10. Capacitance v/s Length for different diameter ratio at 6nm technology

CHAPTER - 5

RESULTS AND DISCUSSION

5.1. INTRODUCTION

On the basis of earlier calculated value of equivalent R,L and C of MWCNT and Copper, interconnect delay is determined by using these parasitic as a load to CMOS inverter as shown in fig. 5.1. With the help of Tanner EDA tool, these parasitic are used as a load to CMOS inverter. By performing transient analysis using Tanner EDA tool at 32nm, 22nm and 16nm technology at frequency of 1GHz, delay is determined for MWCNT and copper interconnect.

5.2. INTERCONNECT DELAY MODEL

To study the parasitic effects described above requires the introduction of electrical models that estimate and approximate the real behaviour of the wire as a function of its parameters. These models vary from very simple to very complex depending upon the effects that are being studied and the required accuracy. The delay of interconnects has been simulated using T-SPICE 12.5.

5.2.1. LUMPED RLC MODEL

The circuit parasitic of a wire are distributed along its length and are not lumped into a single position. For observation of the effects of parasitic or when looking at only one aspect of the circuit behaviour, it is often to lump the different fractions into a single circuit element.

Schematic diagram of lumped RLC model as shown in fig.5.1. is used to obtain to optimum aspect ratio(ratio of width of NMOS transistor to length of NMOS transistor) of driver at which delay is minimum or Power delay product is minimum using width of PMOS transistor equal to thrice of width of NMOS transistor, keeping length of both transistor equal. Here the switching frequency of 0.1GHz is used in input for all technology nodes.

The delay of interconnect for different aspect ratio for all technology nodes can be calculated using the waveform viewer as shown in fig.5.2. From Fig.5.2 fall time has been calculated by considering that fall time is equal to time at which

$V_{90\%}$ of input signal has been attained minus time at which $V_{10\%}$ of output signal has been attained.

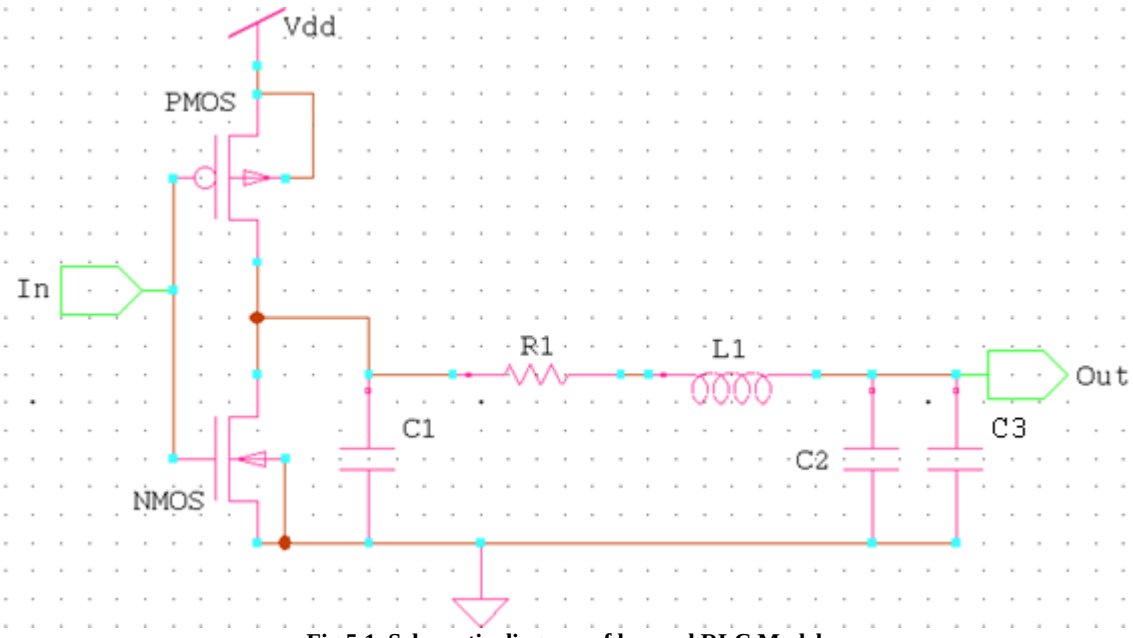

Fig.5.1. Schematic diagram of lumped RLC Model

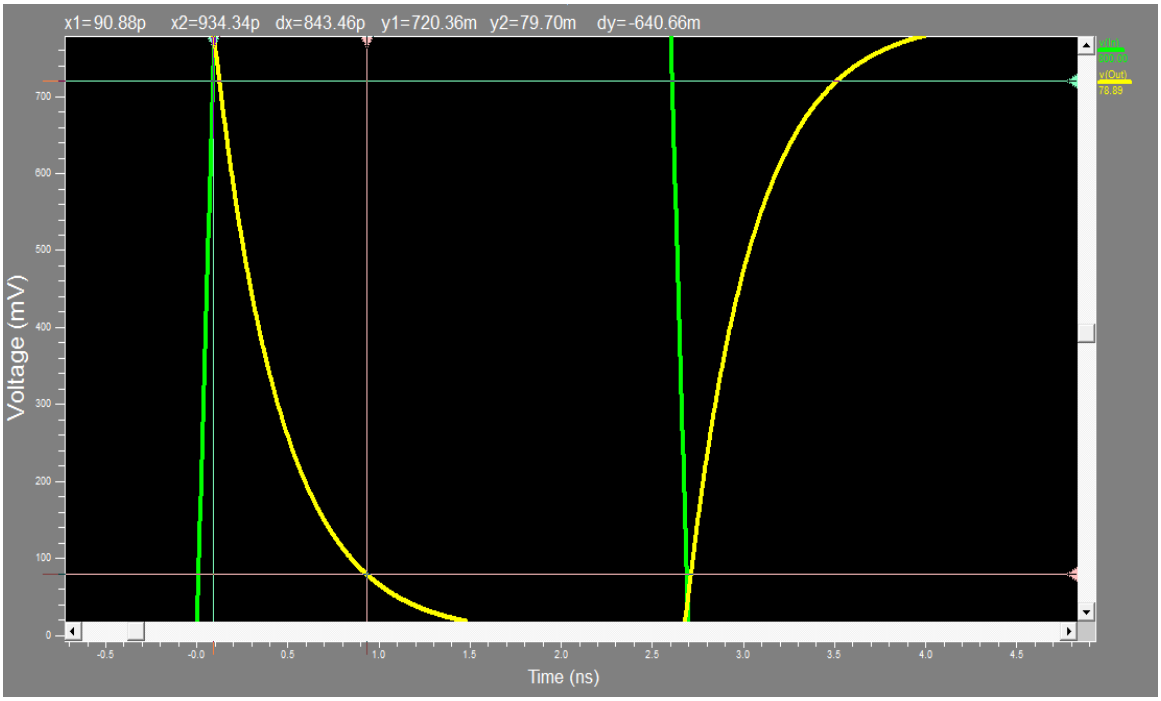

Fig. 5.2. Output Window after the simulation has been performed

Similarly, rise time can be calculated considering that rise time is equal to time at which $V_{10\%}$ of input signal minus time at which $V_{90\%}$ of output signal has been attained. Delay is equal to average of rise time and fall time.

5.2.2. DISTRIBUTED RLC MODEL

The lumped model is a highly inaccurate model, as it has more delay and for resistive-capacitive-inductive wire a distributed RLC model is appropriate. The distributed RLC line can be approximated by a lumped multi-stage RLC ladder network. By insertion of repeaters, lumped RLC line can be converted into distributed RLC line

Role and Insertion of Repeaters

Since the time delay is proportional to square of the interconnect length as the inductance effect is considered. Equispaced repeaters are usually inserted into the MWCNT interconnects to reduce the total time delay. After repeater insertion, the time delay becomes proportional to length of interconnect instead of square of the length of interconnect. The repeaters are assumed to be implemented as CMOS inverters.

Repeater insertion is a method to reduce the propagation delay of long wires by inserting repeaters, as shown in fig.5.3. Inserting n - 1 repeaters with a fixed delay denoted by t_{rep}, will divide the line into n segments having equal lengths of L/n.

Defining elements value

$$\boldsymbol{R_n = \frac{R}{n}, C_n = \frac{C}{n}\ and\ L_n = \frac{L}{n}} \qquad (5.1)$$

Therefore the total propagation delay of the repeater inserted line is the sum of the delay of n segments of length L/n, and the delay of n - 1 repeaters.

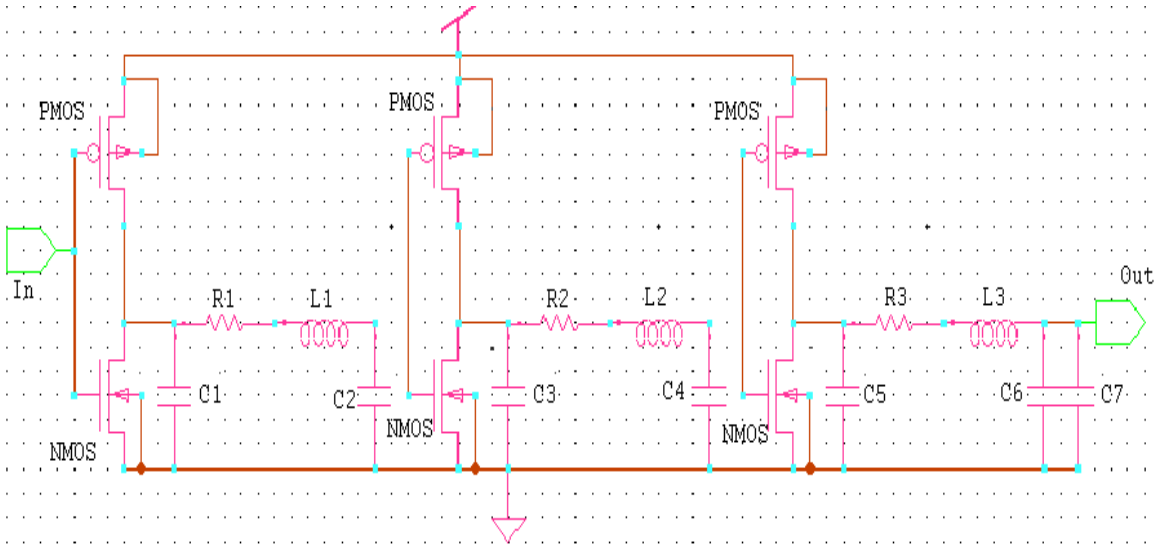

Fig. 5.3. Schematic diagram of repeater insertion with 3 repeaters

Schematic diagram as shown in fig.5.3 shows that lumped RLC get divided into number of segments after the repeater insertion. Fig.5.3. is used to get optimum number of repeaters for which delay of network or power delay product is minimum with switching frequency of 0.1GHz. Simulation of this schematic is also done in the same way as discussed above.

Once optimum no. of repeaters is known then delay of interconnects has been analysed by varying their switching from 0.1GHz to 1GHz because as a very promising future interconnect material, besides their circuit performance in terms of delay, it is also important to investigate their high-frequency behaviour. This is desirable not only for future high-frequency circuit design but also due to the fact that the significant frequencies of digital signals in VLSI[21] are expected to increase further with technology scaling.

5.3. SPICE SIMULATION RESULTS

In this section, the performance of an MWCNT interconnect is estimated and compared with its different diameter ratio. In this section, the length of interconnects has been considered from 100μm to 1000μm at the intermediate level. The parameters used for simulation has been summarized in table 5.1.

Table 5.1. Parameters used for simulation for intermediate level

Technology Nodes	32nm	22nm	16nm
Vdd	0.9	0.8	0.7
Driver and repeater size	80	80	80
Number of repeaters	7	4	3
C_{Load}(fF)	1	1	1

A typical interconnect structure shown in Fig.5.4. is used for the simulation [38]. Here R_t and C_{out} are the equivalent output resistance and capacitance of the gate driver, respectively, and C_{load} is the input capacitance of the load gate. The input excitation is assumed to be pulse signal. We consider a typical interconnect structure shown in Fig. 5.4. In the simulations, coupling capacitance between two MWCNT bundles (C_c) are also calculated using the "W" model[44] as shown in Fig.5.5.

We consider all capacitances that exist between two MWCNT bundles. In this section the effect of variation of diameter ratio of MWCNT and the length of interconnect of MWCNT for different technology has been compared.

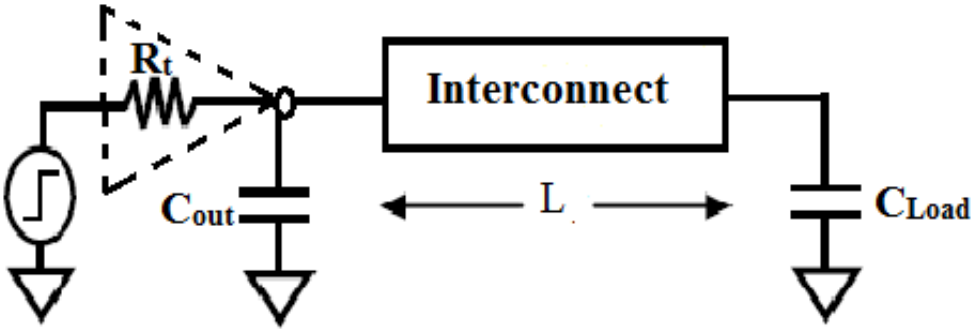

Fig.5.4. Schematic of circuit used for evaluation[38].

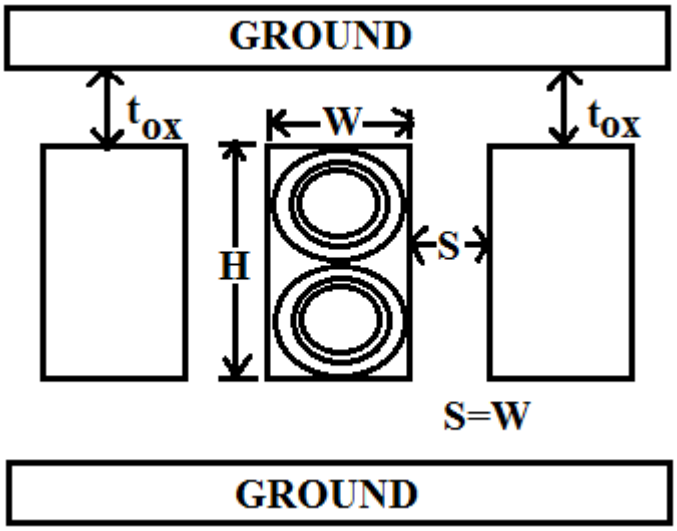

Fig.5.5. Cross section of a typical interconnect configuration[38]

5.3.1. COMPARISON OF PROPAGATION DELAY

Using the schematic as shown in fig.5.2. the propagation delay of MWCNT and copper has been calculated. The comparison of delays between copper and MWCNT interconnect has benn done by taking ratio of their delays. From fig.5.6. to fig.5.8 shows the effect of varying the diameter ratio and length of interconnect on delay ratio (MWCNT/Cu) at 32nm , 22nm and 16nm technology node, respectively.

From fig.5.6 to fig.5.8, it may be shown that MWCNT has lower propagation delay than copper interconnect for different technologies, different diameter ratio and for different length of interconnect. It is observed that for a particular length of interconnect, as the

diameter ratio decreases, the number of shells increases. With the increase in number of shells, propagation delay ratio decreases for a particular technology node. It also shows that for a particular diameter ratio as technology changes from 32nm to 16nm, propagation delay ratio increases. It also noted that for a particular diameter ratio, as the length of interconnect increases, the propagation delay ratio decreases for a particular technology.

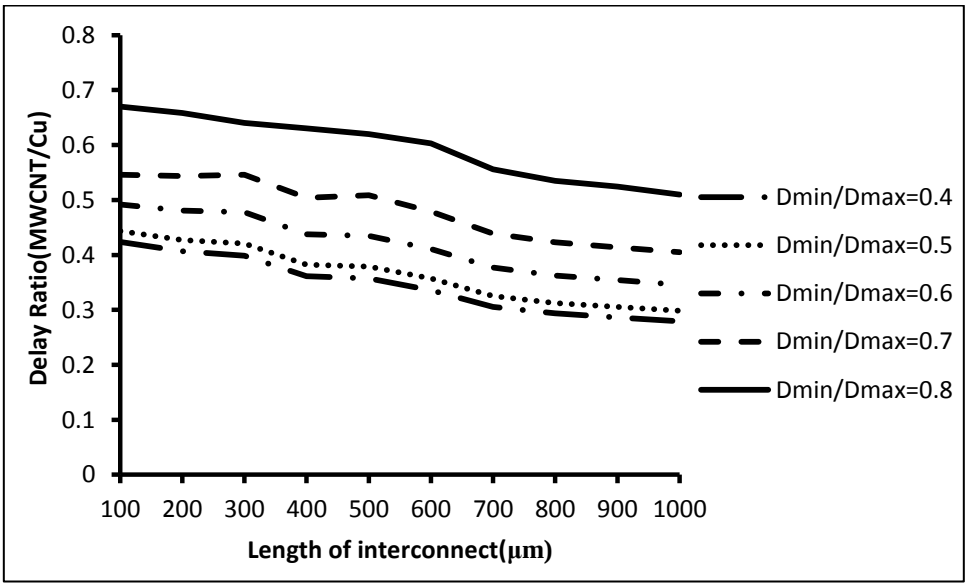

Fig.5.6. Delay Ratio v/s Length for different diameter ratio at 32nm technology

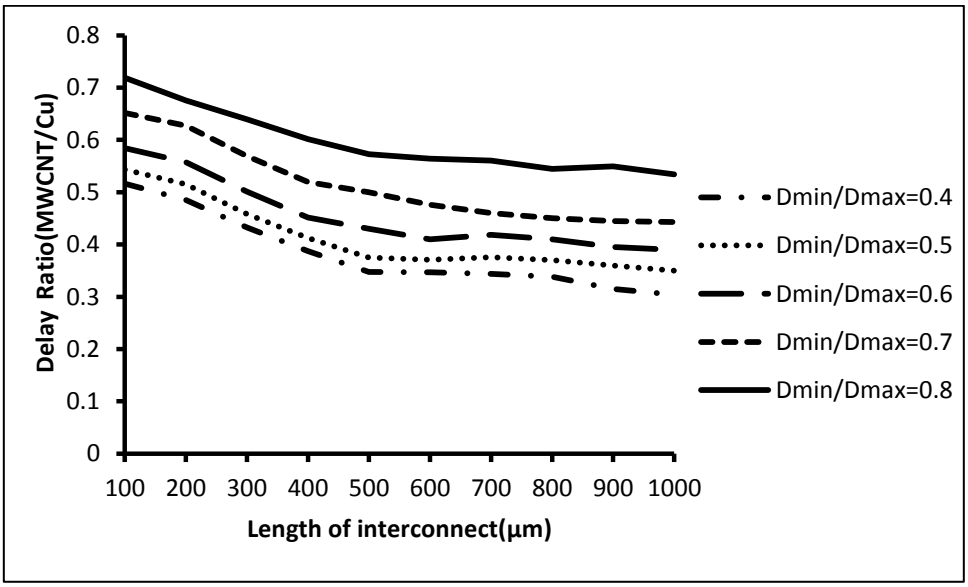

Fig.5.7. Delay Ratio v/s Length for different diameter ratio at 22nm technology

5.3.2. COMPARISON OF POWER DISSIPATION

Using the SPICE simulation, the power dissipation of MWCNT and copper has been calculated. The comparison of power dissipation between copper and MWCNT interconnect has been done by taking ratio of their powers. From fig. 5.9. to fig. 5.11. shows the effect of variation of diameter ratio and length of interconnect on power ratio(MWCNT/Cu) for different technologies i.e. 32nm, 22nm and 16nm.

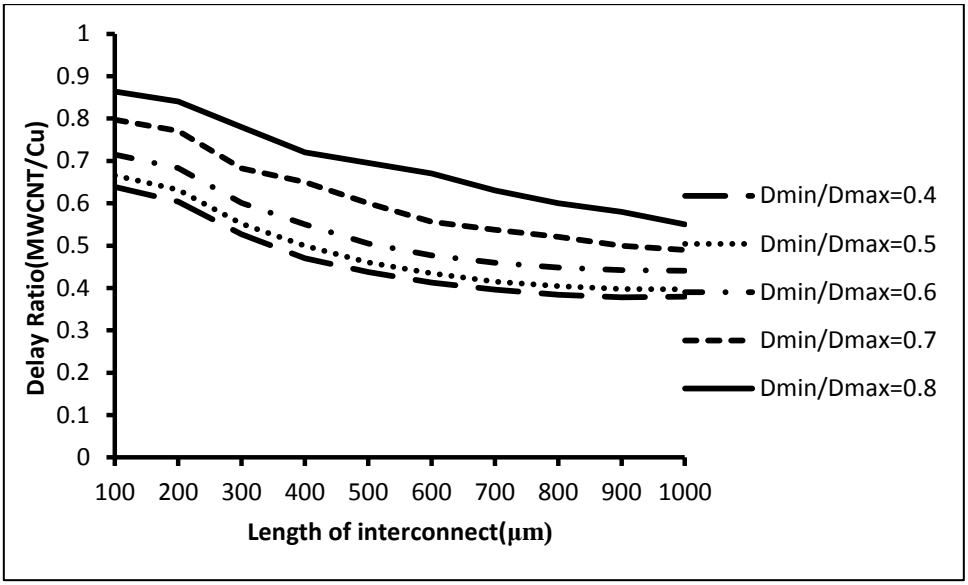

Fig.5.8. Delay Ratio v/s Length for different diameter ratio at 16nm technology

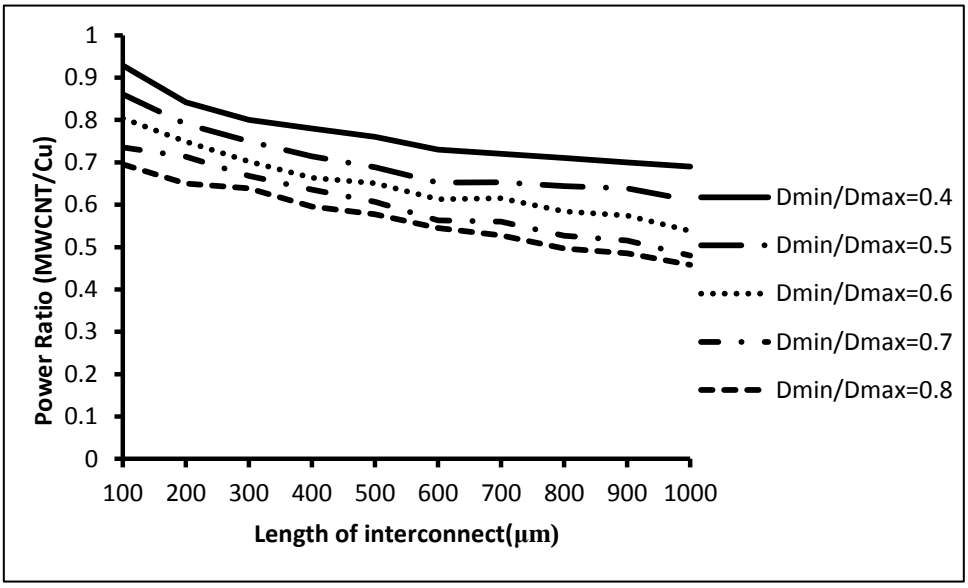

Fig.5.9. Power Ratio v/s Length for different diameter ratio at 32nm technology

From fig.5.9 to fig.5.11, it is observed that MWCNT has lower power consumption than Copper interconnect for different technologies, different diameter ratio and for different length of interconnect. It may also shows that for a particular length of interconnect, as diameter ratio increases from 0.4 to 0.8, the number of shells decreases, hence power ratio decreases for a particular technology node. It shows that for a particular diameter ratio as technology changes from 16nm to 32nm, power ratio increases. It also noted that for a particular diameter ratio and for a particular technology, as the length of interconnect increases, the power ratio decreases.

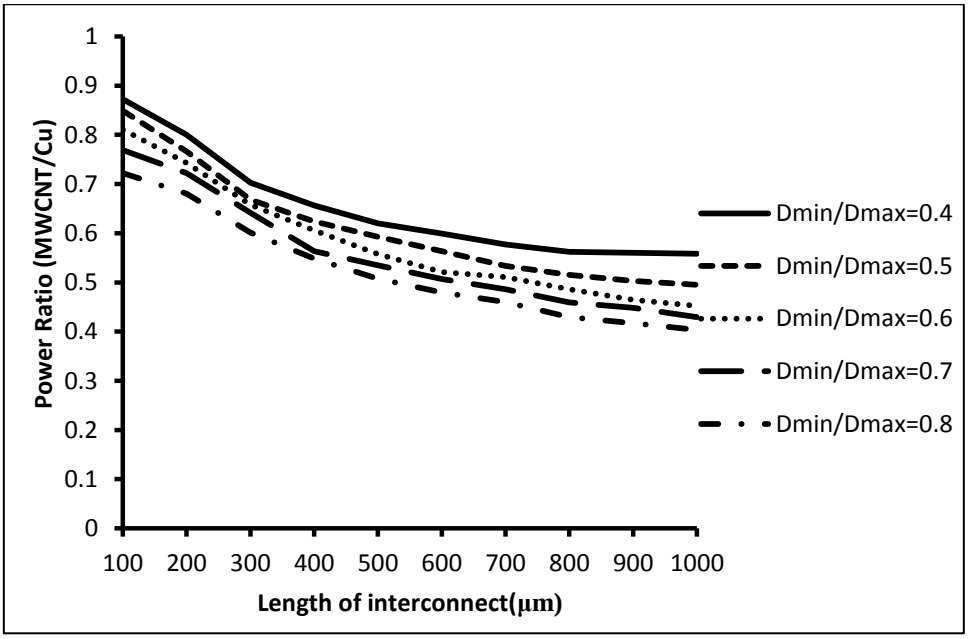

Fig.5.10. Power Ratio v/s Length for different diameter ratio at 22nm technology

5.3.3. COMPARISON OF POWER DELAY PRODUCT (PDP)

Using the SPICE simulation, the PDP of MWCNT and copper has been calculated. The comparison of PDP between copper and MWCNT interconnect has been done by taking ratio of their PDP. From fig.5.12 to fig.5.14 shows the effect of varying the diameter ratio and length of interconnect on power delay product ratio (MWCNT/Cu) at 32nm , 22nm and 16nm technology node, respectively.

From fig.5.12 to fig.5.14, it is shown that MWCNT has lower PDP than Copper interconnect for different technologies, different diameter ratio and for different length of interconnect. It may also be noted that for a particular length of interconnect, with increases in diameter ratio, PDP ratio increases for a particular technology node.

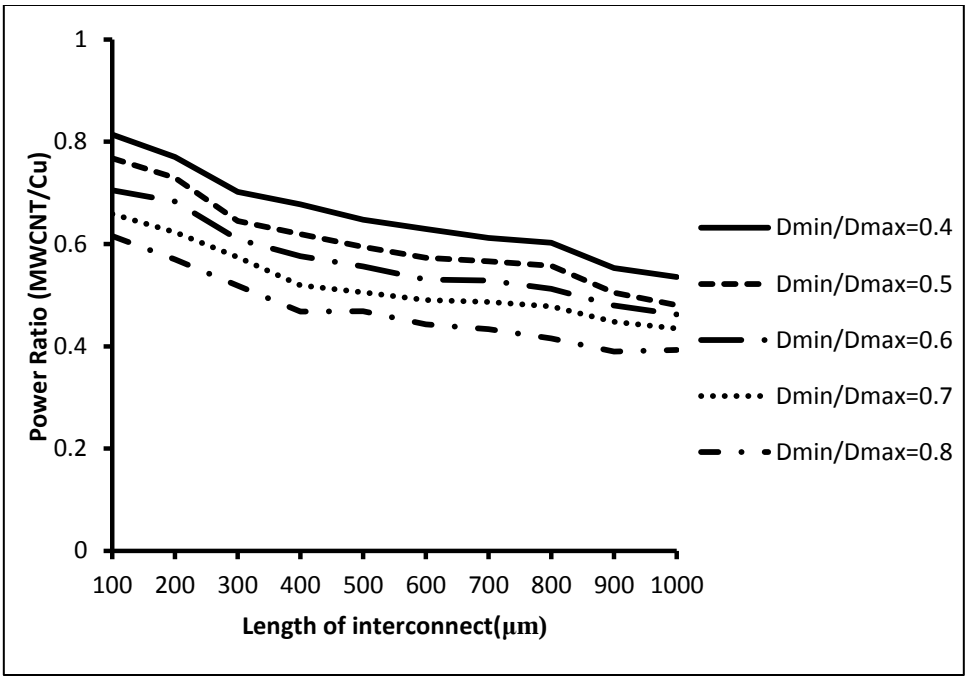

Fig.5.11. Power Ratio v/s Length for different diameter ratio at 16nm technology

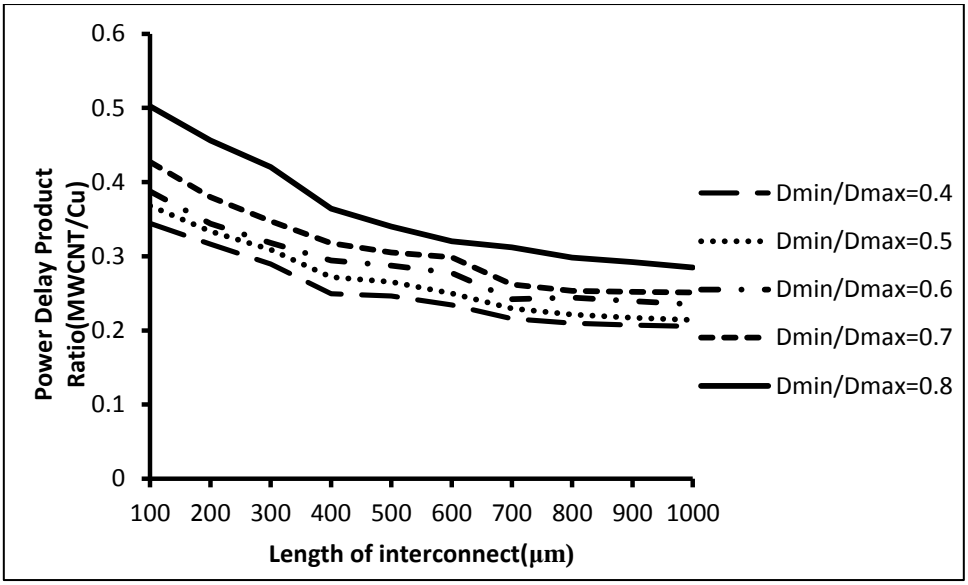

Fig.5.12. PDP Ratio v/s Length for different diameter ratio at 32nm technology

It shown that as technology node changes from 16nm to 32nm, power delay product (PDP) ratio decreases for a particular diameter ratio. It also noted that for a particular diameter ratio and for a particular technology, as the length of interconnect increases, the power delay product ratio decreases.

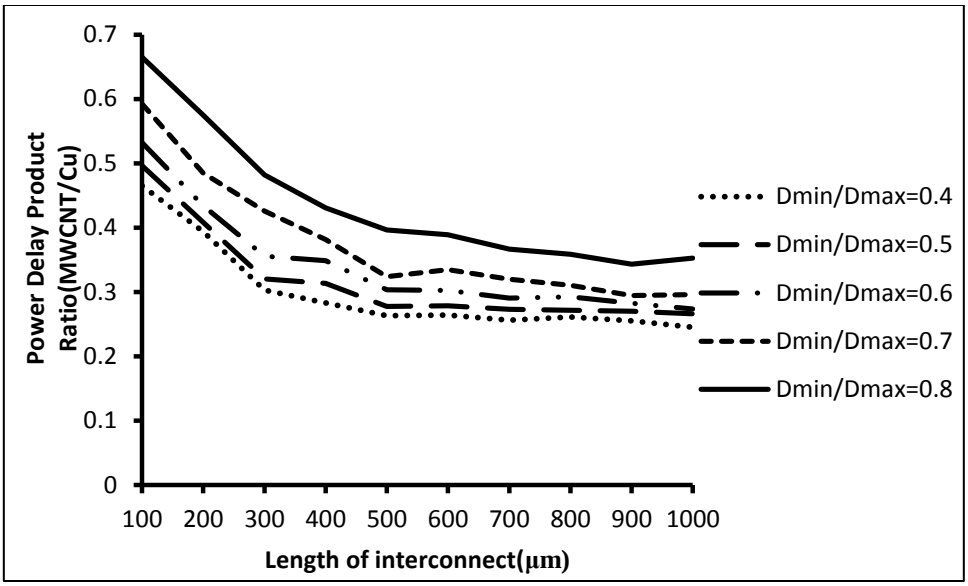

Fig.5.13. PDP Ratio v/s Length for different diameter ratio at 22nm technology

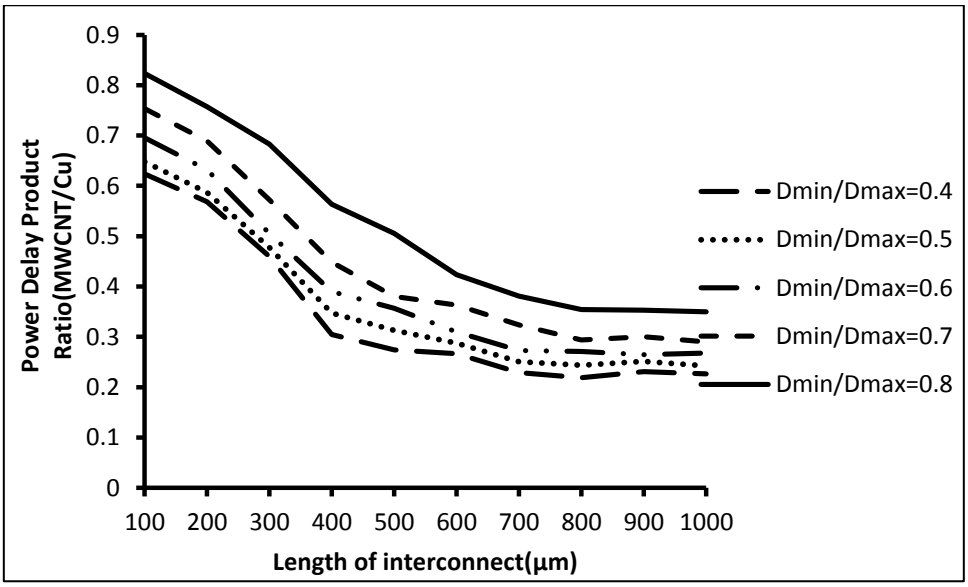

Fig.5.14. PDP Ratio v/s Length for different diameter ratio at 16nm technology

CHAPTER - 6

CONCLUSION

This work analyzed the effect of variation of diameter ratio and length of interconnect on the value of parasitic elements. As diameter ratio increases, then the number of shells decreases, due to which total number of conducting channels decreases. With increase in diameter ratio, resistance and inductance increases but the capacitance decreases. As length of interconnect increases, all of the three parasitic elements increases. In this work, SPICE simulation is used to compare the performance of copper interconnects with MWCNT interconnects for 16nm, 22nm and 32nm technology. This work also concluded the effect of variation of diameter ratio and length of interconnect on propagation delay, power consumption and PDP for MWCNT interconnect and its result has been compared with Copper interconnects at 16nm, 22nm and 32nm technology node. An equivalent circuit model of MWCNT and Copper was used for estimation and analysis of propagation delay. The work shows that MWCNT has smaller delay, power consumption and PDP than Copper interconnect. The work also shows that for a particular length of interconnect as diameter ratio increases then delay ratio, power delay product (PDP) ratio increases but power ratio decreases for a particular technology node. This work shows that as technology nodes increases from 16nm to 32nm then delay ratio, power delay product ratio and power ratio decreases for a particular diameter ratio. It also noted that for a particular diameter ratio and for a particular technology node, as length of interconnect increases, then delay ratio, power ratio and PDP ratio decreases. It has been concluded that the worst case of MWCNT also provides better performance than Copper interconnect. Hence MWCNT is considered to be potential alternative to copper interconnects in future.

LIST OF PUBLICATIONS

[1]. Shweta Maheshwari, Karamjit Singh Sandha, "Performance and Analysis of Multi-Walled Carbon Nanotubes as Interconnects at Intermediate Level" at International Conference on Electronics, Communication and Information Technology on Oct 04-05, 2013.

[2]. Shweta Maheshwari, Karamjit Singh Sandha, " Effects of change of diameter ratio on propagation delay and power consumption of MWCNT as interconnects" , International Journal of VLSI and Embedded Systems-IJVES, May 2014.

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APPENDIX A

A.1. PTM LEVEL 54 MODEL FOR 32nm TECHNOLOGY

.model nmos nmos level = 54

+version = 4.0	binunit = 1	Paramchk = 1	mobmod = 0
capmod = 2	+igcmod = 1	igbmod = 1	geomod = 1
+diomod = 1	rdsmod = 0	rbodymod= 1	rgatemod= 1
+permod = 1	acnqsmod= 0	trnqsmod= 0	
+tnom = 27	toxe = 1.15e-009	toxp = 9e-010	toxm = 1.15e-009
+dtox = 2.5e-010	epsrox = 3.9	wint = 5e-009	lint = 2.7e-009
+ll = 0	wl = 0	lln = 1	wln = 1
+lw = 0	ww = 0	lwn = 1	www = 1
+lwl = 0	wwl = 0	xpart = 0	toxref = 1.15e-009
+xl = -14e-9			
+vth0 = 0.49396	k1 = 0.4	k2 = 0	k3 = 0
+k3b = 0	w0 = 2.5e-006	dvt0 = 1	dvt1 = 2
+dvt2 = 0	dvt0w = 0	dvt1w = 0	dvt2w = 0
+dsub = 0.1	minv = 0.05	voffl = 0	dvtp0 = 1e-011
+dvtp1 = 0.1	lpe0 = 0	lpeb = 0	xj = 1e-008
+ngate = 1e+023	ndep = 4.12e+018	nsd = 2e+020	phin = 0
+cdsc = 0	cdscb = 0	cdscd = 0	cit = 0
+voff = -0.13	nfactor = 2.508	eta0 = 0.0048	etab = 0
+vfb = -0.55	u0 = 0.05	ua = 6e-010	ub = 1.2e-018
+uc = 0	vsat = 210000	a0 = 1	ags = 0
+a1 = 0	a2 = 1	b0 = 0	b1 = 0
+keta = 0.04	dwg = 0	dwb = 0	pclm = 0.02
+pdiblc1 = 0.001	pdiblc2 = 0.001	pdiblcb = -0.005	drout = 0.5
+pvag = 1e-020	delta = 0.01	pscbe1 = 8.14e+008	pscbe2 = 1e-007
+fprout = 0.2	pdits = 0.01	pditsd = 0.23	pditsl = 2300000
+rsh = 5	rdsw = 150	rsw = 75	rdw = 75

+rdswmin = 0	rdwmin = 0	rswmin = 0	prwg = 0
+prwb = 0	wr = 1	alpha0 = 0.074	alpha1 = 0.005
+beta0 = 30	agidl = 0.0002	bgidl = 2.1e+009	cgidl = 0.0002
+egidl = 0.8	aigbacc = 0.012	bigbacc = 0.0028	cigbacc = 0.002
+nigbacc = 1	aigbinv = 0.014	bigbinv = 0.004	cigbinv = 0.004
+eigbinv = 1.1	nigbinv = 3	aigc = 0.020014	bigc = 0.0027432
+cigc = 0.002	aigsd = 0.020014	bigsd = 0.0027432	cigsd = 0.002
+nigc = 1	poxedge = 1	pigcd = 1	ntox = 1
+xrcrg1 = 12	xrcrg2 = 5		
+cgso = 8.5e-011	cgdo = 8.5e-011	cgbo = 2.56e-011	cgdl = 2.653e-010
+cgsl = 2.653e-010	ckappas = 0.03	ckappad = 0.03	acde = 1
+moin = 15	noff = 0.9	voffcv = 0.02	
+kt1 = -0.11	kt1l = 0	kt2 = 0.022	ute = -1.5
+ua1= 4.31e-009	ub1 = 7.61e-018	uc1 = -5.6e-011	prt = 0
+at = 33000			
+fnoimod = 1	tnoimod = 0		
+jss = 0.0001	jsws = 1e-011	jswgs = 1e-010	njs = 1
+ijthsfwd = 0.01	ijthsrev = 0.001	bvs = 10	xjbvs = 1
+jsd = 0.0001	jswd = 1e-011	jswgd = 1e-010	njd = 1
+ijthdfwd = 0.01	ijthdrev = 0.001	bvd = 10	xjbvd = 1
+pbs = 1	cjs = 0.0005	mjs = 0.5	pbsws = 1
+cjsws = 5e-010	mjsws = 0.33	pbswgs = 1	cjswgs = 3e-010
+mjswgs = 0.33	pbd = 1	cjd = 0.0005	mjd = 0.5
+pbswd = 1	cjswd = 5e-010	mjswd = 0.33	pbswgd = 1
+cjswgd = 5e-010	mjswgd = 0.33	tpb = 0.005	tcj = 0.001
+tpbsw = 0.005	tcjsw = 0.001	tpbswg = 0.005	tcjswg = 0.001
+xtis = 3	xtid = 3		
+dmcg = 0	dmci = 0	dmdg = 0	dmcgt = 0
+dwj = 0	xgw = 0	xgl = 0	
+rshg = 0.4	gbmin = 1e-010	rbpb = 5	rbpd = 15
+rbps = 15	rbdb = 15	rbsb = 15	ngcon = 1

.model pmos pmos level = 54

+version = 4.0	binunit = 1	Paramchk = 1	mobmod = 0
capmod = 2	+igcmod = 1	igbmod = 1	geomod = 1
+diomod = 1	rdsmod = 0	rbodymod= 1	rgatemod= 1
+permod = 1	acnqsmod= 0	trnqsmod= 0	
+tnom = 27	toxe = 1.2e-009	toxp = 9e-010	toxm = 1.2e-009
+dtox = 3e-010	epsrox = 3.9	wint = 5e-009	lint = 2.7e-009
+ll = 0	wl = 0	lln = 1	wln = 1
+lw = 0	ww = 0	lwn = 1	www = 1
+lwl = 0	wwl = 0	xpart = 0	toxref = 1.2e-009
+xl = -14e-9			
+vth0 = -0.49115	k1 = 0.4	k2 = -0.01	k3 = 0
+k3b = 0	w0 = 2.5e-006	dvt0 = 1	dvt1 = 2
+dvt2 = -0.032	dvt0w = 0	dvt1w = 0	dvt2w = 0
+dsub = 0.1	minv = 0.05	voffl = 0	dvtp0 = 1e-011
+dvtp1 = 0.1	lpe0 = 0	lpeb = 0	xj = 1e-008
+ngate = 1e+023	ndep = 3.07e+018	nsd = 2e+020	phin = 0
+cdsc = 0	cdscb = 0	cdscd = 0	cit = 0
+voff = -0.126	nfactor = 2.1	eta0 = 0.0048	etab = 0
+vfb = 0.55	u0 = 0.014	ua = 2e-09	ub = 5e-019
+uc = 0	vsat = 180000	a0 = 1	ags = 1e-20
+a1 = 0	a2 = 1	b0 = 0	b1 = 0
+keta = -0.047	dwg = 0	dwb = 0	pclm = 0.12
+pdiblc1 = 0.001	pdiblc2 = 0.001	pdiblcb = 3.4e-008	drout = 0.56
+pvag = 1e-020	delta = 0.01	pscbe1 = 8.14e+008	pscbe2 = 9.58e-007
+fprout = 0.2	pdits = 0.08	pditsd = 0.23	pditsl = 2300000
+rsh = 5	rdsw = 150	rsw = 75	rdw = 75
+rdswmin = 0	rdwmin = 0	rswmin = 0	prwg = 0
+prwb = 0	wr = 1	alpha0 = 0.074	alpha1 = 0.005
+beta0 = 30	agidl = 0.0002	bgidl = 2.1e+009	cgidl = 0.0002

+egidl = 0.8	aigbacc = 0.012	bigbacc = 0.0028	cigbacc = 0.002
+nigbacc = 1	aigbinv = 0.014	bigbinv = 0.004	cigbinv = 0.004
+eigbinv = 1.1	nigbinv = 3	aigc = 0.020014	bigc = 0.0027432
+cigc = 0.002	aigsd = 0.020014	bigsd = 0.0027432	cigsd = 0.002
+nigc = 1	poxedge = 1	pigcd = 1	ntox = 1
+xrcrg1 = 12	xrcrg2 = 5		
+cgso = 8.5e-011	cgdo = 8.5e-011	cgbo = 2.56e-011	cgdl = 2.653e-010
+cgsl = 2.653e-010	ckappas = 0.03	ckappad = 0.03	acde = 1
+moin = 15	noff = 0.9	voffcv = 0.02	
+kt1 = -0.11	kt1l = 0	kt2 = 0.022	ute = -1.5
+ua1= 4.31e-009	ub1 = 7.61e-018	uc1 = -5.6e-011	prt = 0
+at = 33000			
+fnoimod = 1	tnoimod = 0		
+jss = 0.0001	jsws = 1e-011	jswgs = 1e-010	njs = 1
+ijthsfwd = 0.01	ijthsrev = 0.001	bvs = 10	xjbvs = 1
+jsd = 0.0001	jswd = 1e-011	jswgd = 1e-010	njd = 1
+ijthdfwd = 0.01	ijthdrev = 0.001	bvd = 10	xjbvd = 1
+pbs = 1	cjs = 0.0005	mjs = 0.5	pbsws = 1
+cjsws = 5e-010	mjsws = 0.33	pbswgs = 1	cjswgs = 3e-010
+mjswgs = 0.33	pbd = 1	cjd = 0.0005	mjd = 0.5
+pbswd = 1	cjswd = 5e-010	mjswd = 0.33	pbswgd = 1
+cjswgd = 5e-010	mjswgd = 0.33	tpb = 0.005	tcj = 0.001
+tpbsw = 0.005	tcjsw = 0.001	tpbswg = 0.005	tcjswg = 0.001
+xtis = 3	xtid = 3		
+dmcg = 0	dmci = 0	dmdg = 0	dmcgt = 0
+dwj = 0	xgw = 0	xgl = 0	
+rshg = 0.4	gbmin = 1e-010	rbpb = 5	rbpd = 15
+rbps = 15	rbdb = 15	rbsb = 15	ngcon = 1

A.2. PTM LEVEL 54 MODEL FOR 22nm TECHNOLOGY

.model nmos nmos level = 54

+version = 4.0	binunit = 1	Paramchk = 1	mobmod = 0
capmod = 2	+igcmod = 1	igbmod = 1	geomod = 1
+diomod = 1	rdsmod = 0	rbodymod= 1	rgatemod= 1
+permod = 1	acnqsmod= 0	trnqsmod= 0	
+tnom = 27	toxe = 1.05e-009	toxp = 8.0e-010	toxm = 1.05e-009
+dtox = 2.5e-010	epsrox = 3.9	wint = 5e-009	lint = 2e-009
+ll = 0	wl = 0	lln = 1	wln = 1
+lw = 0	ww = 0	lwn = 1	www = 1
+lwl = 0	wwl = 0	xpart = 0	toxref = 1.05e-009
+xl = -9e-9			
+vth0 = 0.50308	k1 = 0.4	k2 = 0	k3 = 0
+k3b = 0	w0 = 2.5e-006	dvt0 = 1	dvt1 = 2
+dvt2 = 0	dvt0w = 0	dvt1w = 0	dvt2w = 0
+dsub = 0.1	minv = 0.05	voffl = 0	dvtp0 = 1e-011
+dvtp1 = 0.1	lpe0 = 0	lpeb = 0	xj = 7.2e-009
+ngate = 1e+023	ndep = 5.5e+018	nsd = 2e+020	phin = 0
+cdsc = 0	cdscb = 0	cdscd = 0	cit = 0
+voff = -0.13	nfactor = 2.3	eta0 = 0.004	etab = 0
+vfb = -0.55	u0 = 0.04	ua = 6e-010	ub = 1.2e-018
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+a1 = 0	a2 = 1	b0 = 0	b1 = 0
+keta = 0.04	dwg = 0	dwb = 0	pclm = 0.02
+pdiblc1 = 0.001	pdiblc2 = 0.001	pdiblcb = -0.005	drout = 0.5
+pvag = 1e-020	delta = 0.01	pscbe1 = 8.14e+008	pscbe2 = 1e-007
+fprout = 0.2	pdits = 0.01	pditsd = 0.23	pditsl = 2300000
+rsh = 5	rdsw = 145	rsw = 75	rdw = 75
+rdswmin = 0	rdwmin = 0	rswmin = 0	prwg = 0
+prwb = 0	wr = 1	alpha0 = 0.074	alpha1 = 0.005
+beta0 = 30	agidl = 0.0002	bgidl = 2.1e+009	cgidl = 0.0002

+egidl = 0.8	aigbacc = 0.012	bigbacc = 0.0028	cigbacc = 0.002
+nigbacc = 1	aigbinv = 0.014	bigbinv = 0.004	cigbinv = 0.004
+eigbinv = 1.1	nigbinv = 3	aigc = 0.0213	bigc = 0.0025889
+cigc = 0.002	aigsd = 0.0213	bigsd = 0.0025889	cigsd = 0.002
+nigc = 1	poxedge = 1	pigcd = 1	ntox = 1
+xrcrg1 = 12	xrcrg2 = 5		
+cgso = 6.5e-011	cgdo = 6.5e-011	cgbo = 2.56e-011	cgdl = 2.653e-010
+cgsl = 2.653e-010	ckappas = 0.03	ckappad = 0.03	acde = 1
+moin = 15	noff = 0.9	voffcv = 0.02	
+kt1 = -0.11	kt1l = 0	kt2 = 0.022	ute = -1.5
+ua1= 4.31e-009	ub1 = 7.61e-018	uc1 = -5.6e-011	prt = 0
+at = 33000			
+fnoimod = 1	tnoimod = 0		
+jss = 0.0001	jsws = 1e-011	jswgs = 1e-010	njs = 1
+ijthsfwd = 0.01	ijthsrev = 0.001	bvs = 10	xjbvs = 1
+jsd = 0.0001	jswd = 1e-011	jswgd = 1e-010	njd = 1
+ijthdfwd = 0.01	ijthdrev = 0.001	bvd = 10	xjbvd = 1
+pbs = 1	cjs = 0.0005	mjs = 0.5	pbsws = 1
+cjsws = 5e-010	mjsws = 0.33	pbswgs = 1	cjswgs = 3e-010
+mjswgs = 0.33	pbd = 1	cjd = 0.0005	mjd = 0.5
+pbswd = 1	cjswd = 5e-010	mjswd = 0.33	pbswgd = 1
+cjswgd = 5e-010	mjswgd = 0.33	tpb = 0.005	tcj = 0.001
+tpbsw = 0.005	tcjsw = 0.001	tpbswg = 0.005	tcjswg = 0.001
+xtis = 3	xtid = 3		
+dmcg = 0	dmci = 0	dmdg = 0	dmcgt = 0
+dwj = 0	xgw = 0	xgl = 0	
+rshg = 0.4	gbmin = 1e-010	rbpb = 5	rbpd = 15
+rbps = 15	rbdb = 15	rbsb = 15	ngcon = 1

.model pmos pmos level = 54

+version = 4.0	binunit = 1	Paramchk = 1	mobmod = 0

capmod = 2	+igcmod = 1	igbmod = 1	geomod = 1
+diomod = 1	rdsmod = 0	rbodymod= 1	rgatemod= 1
+permod = 1	acnqsmod= 0	trnqsmod= 0	
+tnom = 27	toxe = 1.1e-009	toxp = 8e-010	toxm = 1.1e-009
+dtox = 3e-010	epsrox = 3.9	wint = 5e-009	lint = 2e-009
+ll = 0	wl = 0	lln = 1	wln = 1
+lw = 0	ww = 0	lwn = 1	www = 1
+lwl = 0	wwl = 0	xpart = 0	toxref = 1.1e-009
+xl = -9e-9			
+vth0 = -0.4606	k1 = 0.4	k2 = -0.01	k3 = 0
+k3b = 0	w0 = 2.5e-006	dvt0 = 1	dvt1 = 2
+dvt2 = -0.032	dvt0w = 0	dvt1w = 0	dvt2w = 0
+dsub = 0.1	minv = 0.05	voffl = 0	dvtp0 = 1e-011
+dvtp1 = 0.05	lpe0 = 0	lpeb = 0	xj = 7.2e-009
+ngate = 1e+023	ndep = 4.4e+018	nsd = 2e+020	phin = 0
+cdsc = 0	cdscb = 0	cdscd = 0	cit = 0
+voff = -0.126	nfactor = 2.1	eta0 = 0.0038	etab = 0
+vfb = 0.55	u0 = 0.095	ua = 2e-09	ub = 5e-019
+uc = 0	vsat = 210000	a0 = 1	ags = 1e-20
+a1 = 0	a2 = 1	b0 = 0	b1 = 0
+keta = -0.047	dwg = 0	dwb = 0	pclm = 0.12
+pdiblc1 = 0.001	pdiblc2 = 0.001	pdiblcb = 3.4e-008	drout = 0.56
+pvag = 1e-020	delta = 0.01	pscbe1 = 8.14e+008	pscbe2 = 9.58e-007
+fprout = 0.2	pdits = 0.08	pditsd = 0.23	pditsl = 2300000
+rsh = 5	rdsw = 145	rsw = 75	rdw = 75
+rdswmin = 0	rdwmin = 0	rswmin = 0	prwg = 0
+prwb = 0	wr = 1	alpha0 = 0.074	alpha1 = 0.005
+beta0 = 30	agidl = 0.0002	bgidl = 2.1e+009	cgidl = 0.0002
+egidl = 0.8	aigbacc = 0.012	bigbacc = 0.0028	cigbacc = 0.002
+nigbacc = 1	aigbinv = 0.014	bigbinv = 0.004	cigbinv = 0.004

+eigbinv = 1.1	nigbinv = 3	aigc = 0.0213	bigc = 0.0025889
+cigc = 0.002	aigsd = 0.0213	bigsd = 0.0025889	cigsd = 0.002
+nigc = 1	poxedge = 1	pigcd = 1	ntox = 1
+xrcrg1 = 12	xrcrg2 = 5		
+cgso = 6.5e-011	cgdo = 6.5e-011	cgbo = 2.56e-011	cgdl = 2.653e-010
+cgsl = 2.653e-010	ckappas = 0.03	ckappad = 0.03	acde = 1
+moin = 15	noff = 0.9	voffcv = 0.02	
+kt1 = -0.11	kt1l = 0	kt2 = 0.022	ute = -1.5
+ua1= 4.31e-009	ub1 = 7.61e-018	uc1 = -5.6e-011	prt = 0
+at = 33000			
+fnoimod = 1	tnoimod = 0		
+jss = 0.0001	jsws = 1e-011	jswgs = 1e-010	njs = 1
+ijthsfwd = 0.01	ijthsrev = 0.001	bvs = 10	xjbvs = 1
+jsd = 0.0001	jswd = 1e-011	jswgd = 1e-010	njd = 1
+ijthdfwd = 0.01	ijthdrev = 0.001	bvd = 10	xjbvd = 1
+pbs = 1	cjs = 0.0005	mjs = 0.5	pbsws = 1
+cjsws = 5e-010	mjsws = 0.33	pbswgs = 1	cjswgs = 3e-010
+mjswgs = 0.33	pbd = 1	cjd = 0.0005	mjd = 0.5
+pbswd = 1	cjswd = 5e-010	mjswd = 0.33	pbswgd = 1
+cjswgd = 5e-010	mjswgd = 0.33	tpb = 0.005	tcj = 0.001
+tpbsw = 0.005	tcjsw = 0.001	tpbswg = 0.005	tcjswg = 0.001
+xtis = 3	xtid = 3		
+dmcg = 0	dmci = 0	dmdg = 0	dmcgt = 0
+dwj = 0	xgw = 0	xgl = 0	
+rshg = 0.4	gbmin = 1e-010	rbpb = 5	rbpd = 15
+rbps = 15	rbdb = 15	rbsb = 15	ngcon = 1

A.3. PTM LEVEL 54 MODEL FOR 16nm TECHNOLOGY

.model nmos nmos level = 54

+version = 4.0	binunit = 1	Paramchk = 1	mobmod = 0
capmod = 2	+igcmod = 1	igbmod = 1	geomod = 1

+diomod = 1	rdsmod = 0	rbodymod= 1	rgatemod= 1
+permod = 1	acnqsmod= 0	trnqsmod= 0	
+tnom = 27	toxe = 9.5e-010	toxp = 7e-010	toxm = 9.5e-0010
+dtox = 2.5e-010	epsrox = 3.9	wint = 5e-009	lint = 1.45e-009
+ll = 0	wl = 0	lln = 1	wln = 1
+lw = 0	ww = 0	lwn = 1	www = 1
+lwl = 0	wwl = 0	xpart = 0	toxref = 9.5e-010
+xl = -6.5e-9			
+vth0 = 0.47965	k1 = 0.4	k2 = 0	k3 = 0
+k3b = 0	w0 = 2.5e-006	dvt0 = 1	dvt1 = 2
+dvt2 = 0	dvt0w = 0	dvt1w = 0	dvt2w = 0
+dsub = 0.1	minv = 0.05	voffl = 0	dvtp0 = 1e-011
+dvtp1 = 0.1	lpe0 = 0	lpeb = 0	xj = 5e-009
+ngate = 1e+023	ndep = 7e+018	nsd = 2e+020	phin = 0
+cdsc = 0	cdscb = 0	cdscd = 0	cit = 0
+voff = -0.13	nfactor = 2.3	eta0 = 0.0032	etab = 0
+vfb = -0.55	u0 = 0.03	ua = 6e-010	ub = 1.2e-018
+uc = 0	vsat = 290000	a0 = 1	ags = 0
+a1 = 0	a2 = 1	b0 = 0	b1 = 0
+keta = 0.04	dwg = 0	dwb = 0	pclm = 0.02
+pdiblc1 = 0.001	pdiblc2 = 0.001	pdiblcb = -0.005	drout = 0.5
+pvag = 1e-020	delta = 0.01	pscbe1 = 8.14e+008	pscbe2 = 1e-007
+fprout = 0.2	pdits = 0.01	pditsd = 0.23	pditsl = 2300000
+rsh = 5	rdsw = 140	rsw = 75	rdw = 75
+rdswmin = 0	rdwmin = 0	rswmin = 0	prwg = 0
+prwb = 0	wr = 1	alpha0 = 0.074	alpha1 = 0.005
+beta0 = 30	agidl = 0.0002	bgidl = 2.1e+009	cgidl = 0.0002
+egidl = 0.8	aigbacc = 0.012	bigbacc = 0.0028	cigbacc = 0.002
+nigbacc = 1	aigbinv = 0.014	bigbinv = 0.004	cigbinv = 0.004
+eigbinv = 1.1	nigbinv = 3	aigc = 0.0213	bigc = 0.0025889
+cigc = 0.002	aigsd = 0.0213	bigsd = 0.0025889	cigsd = 0.002

+nigc = 1	poxedge = 1	pigcd = 1	ntox = 1
+xrcrg1 = 12	xrcrg2 = 5		
+cgso = 5e-011	cgdo = 5e-011	cgbo = 2.56e-011	cgdl = 2.653e-010
+cgsl = 2.653e-010	ckappas = 0.03	ckappad = 0.03	acde = 1
+moin = 15	noff = 0.9	voffcv = 0.02	
+kt1 = -0.11	kt1l = 0	kt2 = 0.022	ute = -1.5
+ua1= 4.31e-009	ub1 = 7.61e-018	uc1 = -5.6e-011	prt = 0
+at = 33000			
+fnoimod = 1	tnoimod = 0		
+jss = 0.0001	jsws = 1e-011	jswgs = 1e-010	njs = 1
+ijthsfwd = 0.01	ijthsrev = 0.001	bvs = 10	xjbvs = 1
+jsd = 0.0001	jswd = 1e-011	jswgd = 1e-010	njd = 1
+ijthdfwd = 0.01	ijthdrev = 0.001	bvd = 10	xjbvd = 1
+pbs = 1	cjs = 0.0005	mjs = 0.5	pbsws = 1
+cjsws = 5e-010	mjsws = 0.33	pbswgs = 1	cjswgs = 3e-010
+mjswgs = 0.33	pbd = 1	cjd = 0.0005	mjd = 0.5
+pbswd = 1	cjswd = 5e-010	mjswd = 0.33	pbswgd = 1
+cjswgd = 5e-010	mjswgd = 0.33	tpb = 0.005	tcj = 0.001
+tpbsw = 0.005	tcjsw = 0.001	tpbswg = 0.005	tcjswg = 0.001
+xtis = 3	xtid = 3		
+dmcg = 0	dmci = 0	dmdg = 0	dmcgt = 0
+dwj = 0	xgw = 0	xgl = 0	
+rshg = 0.4	gbmin = 1e-010	rbpb = 5	rbpd = 15
+rbps = 15	rbdb = 15	rbsb = 15	ngcon = 1

.model pmos pmos level = 54

+version = 4.0	binunit = 1	Paramchk = 1	mobmod = 0
capmod = 2	+igcmod = 1	igbmod = 1	geomod = 1
+diomod = 1	rdsmod = 0	rbodymod= 1	rgatemod= 1
+permod = 1	acnqsmod= 0	trnqsmod= 0	
+tnom = 27	toxe = 1e-009	toxp = 7e-010	toxm = 1e-009

+dtox = 3e-010	epsrox = 3.9	wint = 5e-009	lint = 1.45e-009
+ll = 0	wl = 0	lln = 1	wln = 1
+lw = 0	ww = 0	lwn = 1	www = 1
+lwl = 0	wwl = 0	xpart = 0	toxref = 1e-009
+xl = -6.5e-9			
+vth0 = -0.43121	k1 = 0.4	k2 = -0.01	k3 = 0
+k3b = 0	w0 = 2.5e-006	dvt0 = 1	dvt1 = 2
+dvt2 = -0.032	dvt0w = 0	dvt1w = 0	dvt2w = 0
+dsub = 0.1	minv = 0.05	voffl = 0	dvtp0 = 1e-011
+dvtp1 = 0.1	lpe0 = 0	lpeb = 0	xj = 5e-009
+ngate = 1e+023	ndep = 5.5e+018	nsd = 2e+020	phin = 0
+cdsc = 0	cdscb = 0	cdscd = 0	cit = 0
+voff = -0.126	nfactor = 2.1	eta0 = 0.0032	etab = 0
+vfb = 0.55	u0 = 0.006	ua = 2e-09	ub = 5e-019
+uc = 0	vsat = 250000	a0 = 1	ags = 1e-20
+a1 = 0	a2 = 1	b0 = 0	b1 = 0
+keta = -0.047	dwg = 0	dwb = 0	pclm = 0.12
+pdiblc1 = 0.001	pdiblc2 = 0.001	pdiblcb = 3.4e-008	drout = 0.56
+pvag = 1e-020	delta = 0.01	pscbe1 = 1.2e+009	pscbe2 = 8.0472e -7
+fprout = 0.2	pdits = 0.08	pditsd = 0.23	pditsl = 2300000
+rsh = 5	rdsw = 140	rsw = 75	rdw = 75
+rdswmin = 0	rdwmin = 0	rswmin = 0	prwg = 0
+prwb = 0	wr = 1	alpha0 = 0.074	alpha1 = 0.005
+beta0 = 30	agidl = 0.0002	bgidl = 2.1e+009	cgidl = 0.0002
+egidl = 0.8	aigbacc = 0.012	bigbacc = 0.0028	cigbacc = 0.002
+nigbacc = 1	aigbinv = 0.014	bigbinv = 0.004	cigbinv = 0.004
+eigbinv = 1.1	nigbinv = 3	aigc = 0.0213	bigc = 0.0025889
+cigc = 0.002	aigsd = 0.0213	bigsd = 0.0025889	cigsd = 0.002
+nigc = 1	poxedge = 1	pigcd = 1	ntox = 1
+xrcrg1 = 12	xrcrg2 = 5		
+cgso = 5e-011	cgdo = 5e-011	cgbo = 2.56e-011	cgdl = 2.653e-010

+cgsl = 2.653e-010	ckappas = 0.03	ckappad = 0.03	acde = 1
+moin = 15	noff = 0.9	voffcv = 0.02	
+kt1 = -0.11	kt1l = 0	kt2 = 0.022	ute = -1.5
+ua1= 4.31e-009	ub1 = 7.61e-018	uc1 = -5.6e-011	prt = 0
+at = 33000			
+fnoimod = 1	tnoimod = 0		
+jss = 0.0001	jsws = 1e-011	jswgs = 1e-010	njs = 1
+ijthsfwd = 0.01	ijthsrev = 0.001	bvs = 10	xjbvs = 1
+jsd = 0.0001	jswd = 1e-011	jswgd = 1e-010	njd = 1
+ijthdfwd = 0.01	ijthdrev = 0.001	bvd = 10	xjbvd = 1
+pbs = 1	cjs = 0.0005	mjs = 0.5	pbsws = 1
+cjsws = 5e-010	mjsws = 0.33	pbswgs = 1	cjswgs = 3e-010
+mjswgs = 0.33	pbd = 1	cjd = 0.0005	mjd = 0.5
+pbswd = 1	cjswd = 5e-010	mjswd = 0.33	pbswgd = 1
+cjswgd = 5e-010	mjswgd = 0.33	tpb = 0.005	tcj = 0.001
+tpbsw = 0.005	tcjsw = 0.001	tpbswg = 0.005	tcjswg = 0.001
+xtis = 3	xtid = 3		
+dmcg = 0	dmci = 0	dmdg = 0	dmcgt = 0
+dwj = 0	xgw = 0	xgl = 0	
+rshg = 0.4	gbmin = 1e-010	rbpb = 5	rbpd = 15
+rbps = 15	rbdb = 15	rbsb = 15	ngcon = 1