"STUDY THE TEMPERATURE-DEPENDENT ANALYTICAL TIME DOMAIN DELAY MODEL FOR PERFORMANCE OPTIMIZATION OF SINGLE-WALLED CARBON NANOTUBE (SWCNT) BUNDLE BASED VLSI INTERCONNECTS"

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In

VLSI Design

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CERTIFICATE

I hereby declare that the work which is being presented in the thesis entitled "**Study the Temperature-Dependent Analytical Time Domain Delay Model for Performance Optimization of Single-Walled Carbon Nanotube (SWCNT) Bundle based VLSI Interconnects**" in partial fulfillment of the requirement for the award of degree of M.Tech. (VLSI Design) at Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of **Dr. Mayank Kumar Rai**, Assistant Professor, ECED.

The matter presented in this thesis has not been submitted in any other University/Institute for the award of my degree.

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(Anu Gupta)

ABSTRACT

As the technology is advancing, the device and interconnect dimensions are scaling down from submicron to deep submicron (DSM) regime. This leads to increase in the density of integrated circuits and hence increase in length of the interconnect. Smaller widths and longer lengths cause decay in the conductive properties of copper interconnects and give rise to reliability issues. Additionally, progressive scaling leads to increase in operating temperature of the integrated circuit and thus the thermal issues are also a major concern. Carbon nanotubes (CNTs) due to their extraordinary mechanical strength and thermal stability have spurred a lot of interest in the research of their use as the next generation VLSI interconnects.

This thesis presents a temperature-dependent analytical model to extract the transient response of the far end of the Single-walled carbon nanotube (SWCNT) bundle interconnects. The overall logic stage delay of a CMOS driven SWCNT bundle interconnect is estimated. The driving transistor is represented by alpha power law model and all the operating regions of transistor are taken into account. The gate delay is obtained by modeling the driving point admittance at the gate output using an effective capacitance. The effective capacitance model takes into consideration the resistance shielding effect and is also compatible with the empirically derived equations. The gate delay obtained analytically for both slow and fast input ramp is in good agreement with the SPICE results. The interconnect delay is estimated by the numerical convolution of gate output and two-pole approximated transfer function of distributed interconnect line. The overall logic delay from analytical model is within 7.9% of the SPICE computed delay. The voltage waveforms at both near end and far end of the interconnect are compared with SPICE simulations. It is observed that the results match quite closely.

A comparative analysis in terms of delay performance between SWCNT bundle interconnects with resistance obtained using temperature independent model and thermally aware model is carried out. The simulations are done at 22nm technology node at 300K temperature for lengths varying from 200μm to 1000μm. An average improvement of 18.18% is observed in delay estimated using thermally aware model

over temperature dependent model of resistance. A similar analysis is performed to compare the delay of SWCNT bundle interconnect with that of copper interconnect, at 22 nm technology node, with temperatures varying from 300K to 500K and lengths varying from 200μm to 1000μm. The simulation results reveal that the delay of copper interconnects is larger than that of SWCNT bundle interconnects for the entire range of length and temperature. This is due to the dominance of line resistance over capacitance and inductance that determines the propagation delay of interconnect, and copper has higher line resistance as compared to SWCNT bundle.

TABLE OF CONTENTS

LIST OF ACRONYMS

CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nanotube
GNR	Graphene Nano-Ribbon
IC	Integrated Circuit
ILD	Inter Layer Dielectric
ITRS	International Technology Roadmap for Semiconductor
MFP	Mean Free Path
MWCNT	Multi Walled Carbon Nanotube
RC	Resistance Capacitance
RLC	Resistance Inductance Capacitance
SPICE	Simulation Program with Integrated Circuit Emphasis
SWCNT	Single Walled Carbon Nanotube
VLSI	Very Large Scale Integration
1D	One Dimensional

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS

C	Capacitance
C_E	Electrostatic capacitance
C_Q	Quantum Capacitance
h	Height
l	Length of interconnect
L	Inductance
L_K	Kinetic inductance
L_M	Magnetic inductance
R	Resistance
R_C	Contact resistance
R_Q	Quantum resistance
R_S	Scattering resistance
s	Separation between adjacent bundles
w	Width
y	ILD Thickness

Chapter 1 Introduction and Statement of the Problems

1.1 Interconnect

A thin film of conducting material which is used for providing electrical connections among various nodes of the circuit made on the silicon chip is called interconnect. As they connect elements within the chip into a functional unit, they can be called as the streets and highways of the integrated circuit (IC). Interconnects are used for providing power and ground, and for distributing clocks and signals in the integrated circuits. Interconnects can have many layers or levels whose number depend on the complexity of the device. The various levels of interconnect are connected to each other using vias.

1.1.1 Importance of Interconnects

Earlier, the laying of interconnections of transistors was a routinely task and was paid significant attention only for some special cases. With the advent of deep submicron technologies, the device dimensions are decreasing and the die sizes are increasing. This leads to increase in the length of interconnect and thus substantial increase in the parasitic effects associated with it. The unwanted effects introduced due to interconnects are increase in propagation delay and power dissipation. Thus it becomes essential to analyse the behaviour of interconnects and their effect on system performance.

1.1.2 Classification of Interconnects

On the basis of their length, interconnects are classified as [1]:

- Local interconnects are very thin lines which connect interconnection among gates and transistors of a functional block. They occupy the lower most metal layers i.e. first and second metal layer.
- Intermediate interconnects are lines with length of 3-4 mm. They are used for distributing clocks and signals within a functional block. They are made to be more wide and thick than local interconnects so that they offer lower resistance.

- Global interconnects are interconnects which occupy the top most layers. They are used for providing clock and signal distribution between the functional blocks and provide power and ground connections. They have length more than 4 mm. Due to its large length, it becomes necessary to employ interconnects with low resistivity so that propagation delay introduced by them is not significant. Large propagation delay can seriously affect the performance of the circuit.

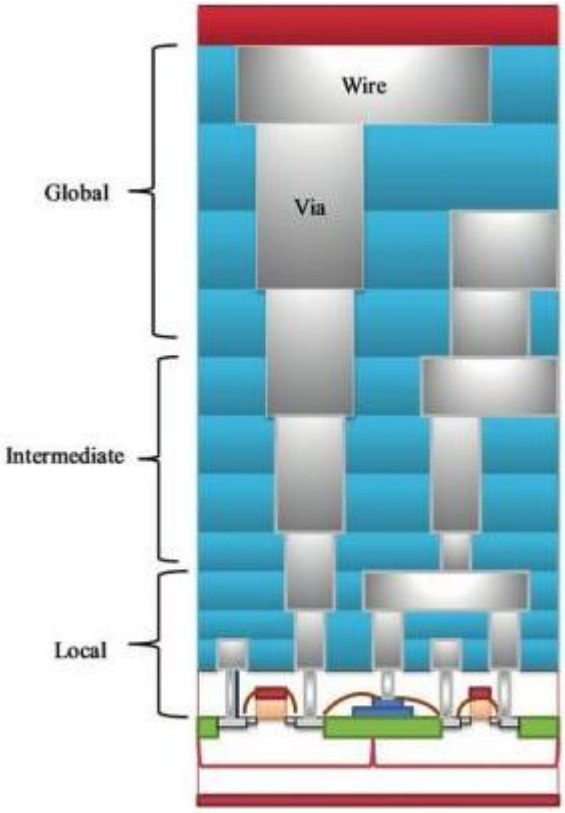

Fig.1.1. Cross-section of stacked interconnects [2].

Fig.1.1 shows the levels of interconnects.The bottom two layers are of local interconnects, the upper two layers are of global interconnects and the layers between them are that of intermediate interconnects.The wires are connected to each other using metal fillings called Vias. The dielectrics are used to isolate the interconnects.The level to level separation between wires is provided by interlayer dielectrics(ILD) and the isolation within the same layer is provided by inter-metal dielectrics (IMD).

1.2 EVOLUTION OF INTERCONNECTS

Continuous advancement in technology has led to decrease in dimensions of device and increase in complexity. The demand for VLSI circuits with higher speed and component density is also increasing continuously. During recent past, various IC designers employed only metallic interconnections (such as Al or Cu). But due to their persistent limitations researchers are forced to look for several other possibility of using carbon based interconnections in near future.

1.2.1 Aluminium Interconnects

Aluminium, because of its good conductivity, used to be the most widely used material for interconnects. It has strong adherence to silicon dioxide and the ohmic contact it forms with silicon is quite good. However, with the advancement of technology, the device dimensions decreased and the interconnect density increased, leading to increase in the current density. At high current densities, electromigration takes place and thus an alternate material had to be used as interconnect.

1.2.2 Copper Interconnects

Copper has higher conductivity than aluminium. It is reliable in carrying five times higher density of current than aluminium and thus is more resistant to electromigration. So copper was preferred as an interconnect material over aluminium. However as the technology further scaled, copper interconnect faced with many limitations. Due to surface roughness and grain boundary scattering, the resistivity of copper increases which leads to higher propagation delay and electromigration.

1.2.3 Carbon Nanotube Interconnects

To overcome the problems in existing VLSI interconnects, there is an urgent need to replace copper with a more promising material. Carbon based interconnects have provided one such alternative. Both carbon nanotubes (CNT) and graphene nanoribbons (GNR) are made up of graphene. Due to the high mechanical strength and excellent thermal and electrical properties of graphene, carbon based interconnects are seen as the future interconnects.

Advantages of carbon nanotubes:

- High thermal conductivity: The thermal conductivity of an isolated carbon nanotube, at room temperature, is as high as 6600W/mK [3]. It is as good as that of diamond, which is considered to be one of the best thermal conductors. This high value of thermal conductivity of carbon nanotubes can be attributed to large mean free path of phonons, which leads to low phonon scattering.
- High current density: Graphene has sp^2 bonding which is stronger than sp^3 bonding in diamond. This strong covalent bonding makes graphene the strongest material ever measured [4]. Due to this high mechanical strength, carbon nanotubes offer high stability against electromigration. They can carry high current densities of $10^9 – 10^{10}$ A/cm^2 without any considerable change in resistance even at high temperatures [5].
- High electrical conductivity: One-dimensional structure of carbon nanotubes leads to reduction in the phase space for scattering by acoustic phonons [6]. Thus the mean free path of carbon nanotubes is approximately 1μm, which is much larger in comparison to that of copper, whose mean free path is in order of tens of nanometers. Hence the carbon nanotubes have higher conductivity than copper.

1.3 DELAY MODELING OF INTERCONNECTS

The propagation delay of a circuit highly influences the performance of a VLSI circuit. The overall delay of the logic stage comprises of two components - gate delay and interconnect delay**.** There are two well accepted methods for estimating the overall delay:

- Empirically derived expressions- The delay is expressed as a function of load capacitance and input-signal transition time (k-factor equations).
- Switch resistor model- This model comprises of a linear resistor and a voltage source. The value of linear resistor is obtained using empirical fitting.

1.4 Statement of the problems

Recent studies in the area of CNT addressed the performance analysis using temperature independent circuit model. Integrated circuits mostly used at temperatures which are much greater than the room temperature. Therefore, if SWCNTs are to be used in integrated circuits applications, it is important to study the variation in their electrical characteristics at temperatures which are greater than the room temperature.

Thus, there is a dire need to develop a temperature dependent model for delay and power dissipation in CNT interconnects to extract transient response.

The objectives of proposed work are briefly as follows:

- Development of temperature-dependent impedance parameters of SWCNT bundle based interconnects.
- Development of analytical time model to extract the transient response at the far end of the SWCNT interconnect bundle.
- A comparative analysis of analytically extracted transient response and simulated response of the far end output for both SWCNT bundle and copper interconnects at 22nm technology node.

1.5 Organization of thesis

Chapter 2 presents the literature review of the work done by researchers on computing the propagation delay. Various models for gate delay, interconnect delay and overall logic delay, are discussed in brief, along with their methodologies, advantages/disadvantages.

Chapter 3 introduces carbon nanotubes and parameters associated with the carbon nanotube interconnects. The modelling of temperature dependent impedance parameters of SWCNT bundle as well as copper is presented.

Chapter 4 proposes temperature dependent delay model for carbon nanotubes based interconnect. The method for estimating the overall logic delay is presented. The analytically obtained results are compared with the simulated results.

Chapter 5 presents comparative analysis between interconnects of SWCNT bundle and copper. The delay of SWCNT bundle and copper is evaluated and compared with variations in length and temperature.

Chapter 6 concludes the thesis and presents the future scope.

Chapter 2 A Review of Delay Models

2.1 Introduction

With scaling down of technology, the performance of conventionally used copper based interconnects is on a decline, thus posing a serious concern over their use as VLSI interconnects. Researchers are looking for an alternative and carbon nanotubes are being considered to provide promising solution. In recent years a lot of work has been done on modeling and performance analysis of SWCNT bundle. To estimate the delay, the interconnect has been modeled by a total capacitance, RC circuit or an RLC circuit. The interconnect line has also been approximated by effective capacitance models and Π-models. All these delay models are described in brief in section 2.2. Section 2.3 discusses the modeling of circuit parameters of SWCNT bundle interconnects and also includes the work related to temperature dependent models.

2.2 Delay Models of Interconnects

W.C. Elmore (1948) **[**7] presented Elmore delay model. He showed that when a unit step input is applied to a linear network and its transient response consists of a monotonic rise to a final constant value, then the delay time and the rise time can be obtained very easily from the Laplace transform representation of the system function of the network.

If $e(t)$ is the step response of a system and $e'(t)$, the derivative of $e(t)$ is the impulse response, then the delay time is defined to be from time t=0 to the centroid of area of $e'(t)$.

$$T_D = \int_0^\infty te'(t)dt \tag{2.1}$$

which means that delay time is the first moment of the impulse response of the system.

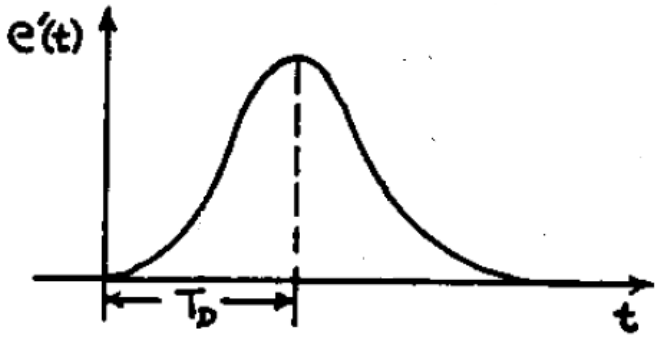

Fig. 2.1. Curve depicting definition of delay time [7].

The relation between transfer function and impulse response is given as:

$$G(s) = \int_0^\infty e'(t)e^{-st}dt \tag{2.2}$$

Expanding e^{-st} in terms of st gives,

$$G(s) = 1 - s\int_0^\infty te'(t)dt + \frac{s^2}{2!}\int_0^\infty t^2e'(t)dt - .... \tag{2.3}$$

From equations (2.1) and (2.3), it is seen that, when the transfer function is expanded in the ascending powers of 's', delay time is equal to the negative of coefficient of 's' in the transfer function of the system.

Thus if transfer function of a system is

$$\mathrm{G(s)} = \frac{1+ \mathrm{a_1s}+\mathrm{a_2s^2}+\mathrm{a_3s^3}+...}{1+ \mathrm{b_1s}+\mathrm{b_2s^2}+\mathrm{b_3s^3}+...}, \tag{2.4}$$

then delay will be $T_D = b_1 - a_1$.

Elmore delay is widely used to calculate interconnect delays in very-large-scale integration (VLSI) routing topologies. It is extremely easy to compute. Delay calculated using Elmore Delay matches very closely with the results obtained from the spice simulation. Disadvantage of Elmore delay is that it cannot be used to calculate delay for RLC interconnect loads because Elmore delay does not take into consideration the inductance of the RLC interconnect. Also, it does not take into account the transition time of the input signal.

A.B. Kahng *et al.* (1996) [8] presented a delay model for interconnects which is applicable for ramp inputs with finite transition time. It also takes the inductive effects

into account. The analysis is done for both one pole and two pole estimation of transfer function of the Interconnect. The finite ramp inputs are expressed as combination of infinite ramp inputs. For each infinite ramp, output expression is obtained by convolution with the system transfer function. The output voltage is achieved by summing up all these components corresponding to infinite ramp. This method is applicable to both rising ramps and falling ramps.

The gate delay can be obtained by approximating the Interconnect load at output of the gate with just a lumped capacitance i.e. the total capacitance seen by the gate. The gate is replaced by an equivalent resistance. Thus, the delay estimation is reduced to deducing Elmore delay of the RC network, where Resistance is that of gate and Capacitance is that of the Interconnect.

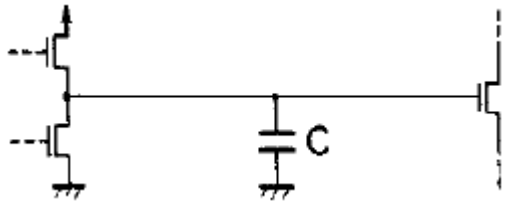

Fig. 2.2. Lumped capacitance model to approximate the interconnect [9].

With the decrease in feature size, the density of chips is increasing. So the width of interconnect is decreasing whereas its length is increasing. Thus the interconnect resistance increases and becomes comparable to the gate resistance. The capacitance seen by the gate is shielded by the interconnect resistance and therefore if the gate delay is now estimated with total capacitance as load, the delay estimated will be more than the actual value. So the interconnect is represented by both resistance and capacitance.

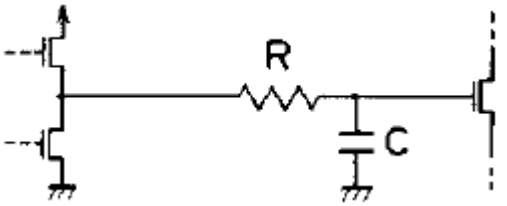

Fig. 2.3. Lumped RC model to approximate the interconnect [9].

In Distributed RC model, resistance and inductance is distributed along the entire length of the Interconnect. The total resistance and total capacitance of a wire can be written as

$R = r \times l$

$C = c \times l$, where l is the length of the interconnect, r is the resistance per unit length, c is the capacitance per unit length

COMPARISON BETWEEN DISTRIBUTED AND LUMPED RC MODEL

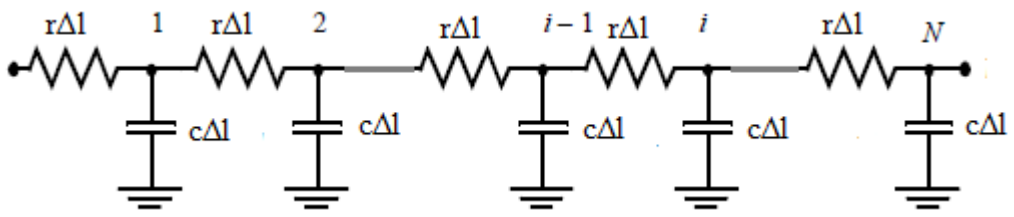

Fig. 2.4. Distributed RC model to approximate the interconnect [10].

For a distributed RC model,

n is the number of segments and Δl is the length of a segment.

$$\text{Elmore Delay} = (r\Delta l)(c\Delta l)\frac{n(n+1)}{2} = rc(\Delta l)^2\frac{n(n+1)}{2} \quad (2.5)$$

For large n, $n.(\Delta l) \rightarrow l$, giving

$$\text{Elmore Delay} = \frac{rcl^2}{2} \quad (2.6)$$

For a lumped RC model(See Fig.2.3)

$$\text{Elmore Delay} = RC = (rl)(cl) = rcl^2 \quad (2.7)$$

From equations (2.6) and (2.7), it can be seen that the delay estimated by lumped RC model is twice that of delay estimated by distributed RC model. So the distributed RC model is preferred over lumped RC model to represent the Interconnect.

If the circuit simulator does not support distributed *RC* model then one of the approximations of distributed RC into lumped RC given in Fig.2.5 can be used. **T. Sakurai** (1983) [9] investigated the approximation of distributed RC network into lumped RC by using Π and T ladder circuits. The results show that the error is quite less for Π and T ladder circuits as compared to L ladder circuits.

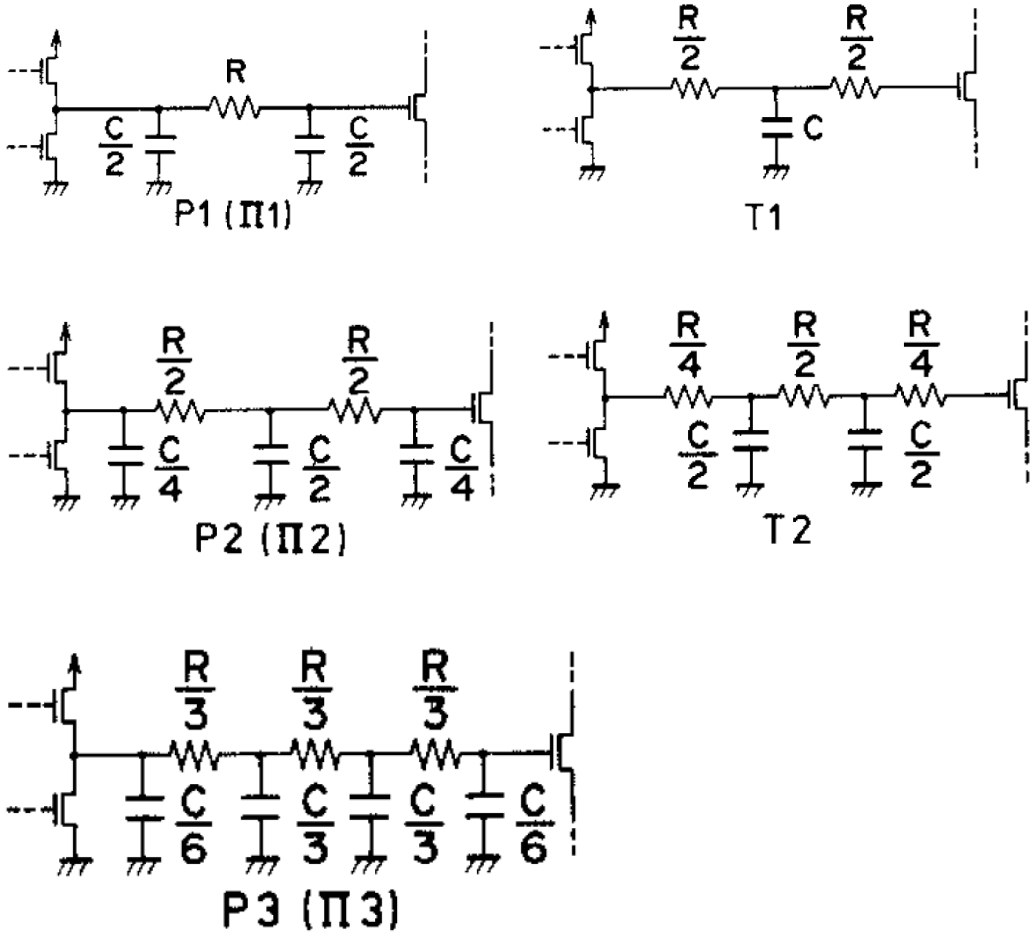

Fig. 2.5. Lumped Π and T circuits used to approximate distributed circuit [9].

With advancement of technology, the clock frequency is increasing and input rise times are becoming faster. Thus the wire inductance starts to play a significant role on the chip. So RC model is no longer being adequate and RLC model is proposed.

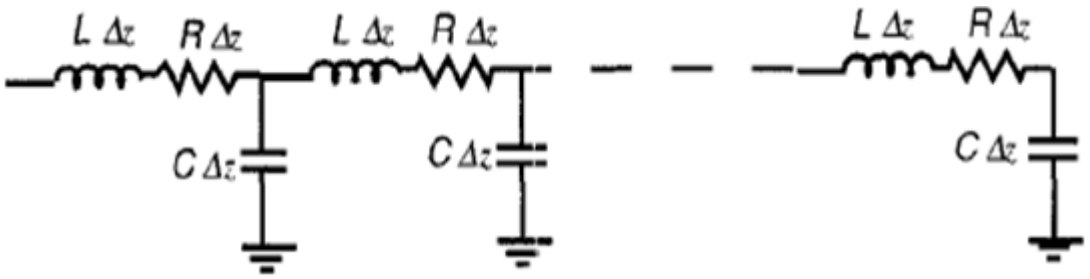

Fig. 2.6. Distributed RLC model of Interconnect [11].

Y. I. Ismail *et al.* (1998) [11] presented two figures of merit which help to determine whether the Interconnect is to be modelled using RLC circuit or RC circuit.

The first figure of merit is the damping factor ξ which is given as

$$\xi = \frac{Rl}{2}\sqrt{\frac{C}{L}}, \tag{2.8}$$

where R, L, C are resistance per unit length, inductance per unit length, capacitance per unit length respectively and l is the length of the Interconnect. ξ represents the attenuation faced by the signal as it propagates through the interconnect line. For ξ < 1, the poles are real and the effect of inductance is negligible. However for ξ > 1, the poles are complex and oscillations take place. In this case, the inclusion of inductance becomes important.

The second figure of merit is the ratio of input signal transition time t_r and the time of flight. Time of flight T_0 is defined as the time taken by the signal to travel the entire length of the Interconnect.

For $t_r < 2T_0$, where $T_0 = l\sqrt{LC}$,

the inductive effects are significant. Otherwise the inductance can be neglected.

Combining both the figure of merits, a range of length is achieved for which inductive effects are significant and thus cannot be neglected. This range of length is:

$$\frac{t_r}{2\sqrt{LC}} < l < \frac{2}{R}\sqrt{\frac{L}{C}} \tag{2.9}$$

Outside this range, there is no need for taking inductance into consideration and RC model can be used to represent the interconnect. This range will exist only if $t_r < \frac{4L}{R}$.

If $t_r > \frac{4L}{R}$, then the inductive effects are insignificant for all values of interconnect length.

O'Brien and Savarino (1989) [12] presented a model to approximate the driving point admittance at the gate output. The approximation is done to determine the influence of interconnect driven by gate on the gate delay. A reduced order lumped approximation of distributed RC interconnect is presented.

The driving point admittance of distributed RC Interconnect is:

$$Y(s) = \sqrt{\frac{sC_{LOAD}}{R_{LOAD}}} \tanh\left(\sqrt{sC_{LOAD}R_{LOAD}}\right), \tag{2.10}$$

where C_{LOAD} is the total capacitance and $R_{LOAD}$is the total resistance.

The third order (Π-segment) approximation proposed is:

$$C_1 = \frac{5}{6}C_{LOAD} \tag{2.11}$$

$$C_2 = \frac{5}{6}C_{LOAD} \tag{2.12}$$

$$R = \frac{12}{25}R_{LOAD} \tag{2.13}$$

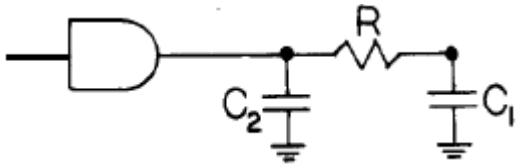

Fig. 2.7 .Π-model to approximate driving point admittance at gate output for an RC interconnect [12].

A.B. Kahng *et al.* (1996) [13] presented a Π-model to approximate driving point admittance at gate output for both RC and RLC interconnects. Previously proposed Π-model did not take into consider the inductive effects of the interconnect line. Also, it computed the first three moments of driving point admittance recursively. The new Π-model presented depends only on the interconnect parameters (resistance, inductance and capacitance).

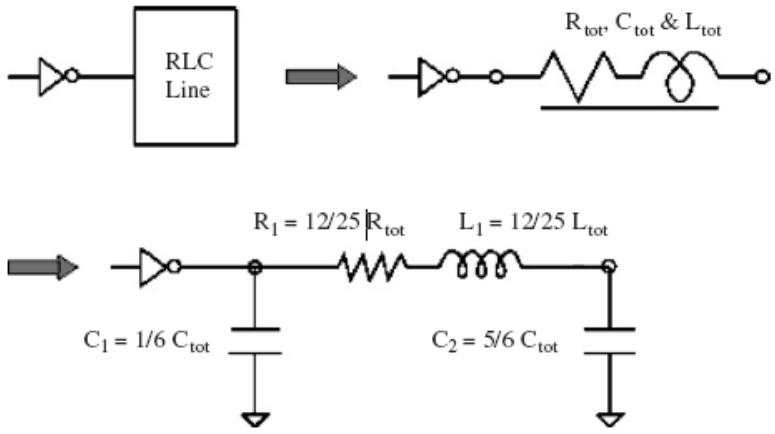

Fig.2.8. Π-model to approximate driving point admittance at gate output for an RLC interconnect [13].

The parameters of the Π-model obtained are:

$$C_1 = \frac{5}{6}C_{LOAD},\ C_2 = \frac{5}{6}C_{LOAD},\ R_1 = \frac{12}{25}R_{LOAD},\ L_1 = \frac{12}{25}L_{LOAD} \qquad (2.14)$$

J. Qian, S. Pullela, L. Pillage (1994) [14] presented a complete scheme for modeling the delay of CMOS logic gates when the resistance of the interconnect significantly shields some of the load capacitance. The Π-model proposed by [13] models the resistance shielding effectively but it is incompatible with the k-factor equations. Empirically derived k-factor equations are used to express the delay of gate with capacitive load as a function of total capacitance and input transition time. For Π-model, the fitting of k-factor equations would require a 4D look up table which is quite impractical. The effective capacitance model presented models the resistance shielding effect as well as is compatible with the empirical equations. In this model, Π-model is replaced by an effective capacitance which will offer the same gate delay as Π-model. This is done by equating the currents through both Π-load and capacitive load till 50% point delay.

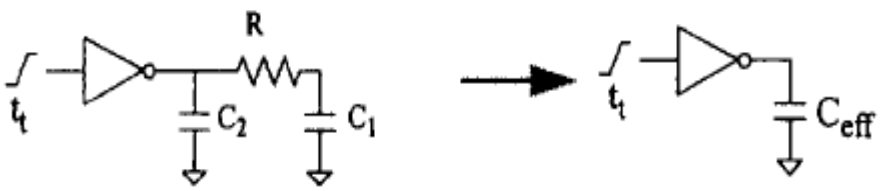

Fig.2.9. An effective capacitance model that replaces Π-model [14].

Initially the total capacitance is assumed to be the load capacitance and subsequently after a number of iterations the suitable effective capacitance is achieved. The delay estimated by this model is quite close to the actual delay.

The Π-model [13] presented a second order load and the effective capacitance model [14] replaced it with a single capacitance. However, some applications may require higher order load models. **F. Dartu *et al.*** (1996) [15] proposed an effective capacitance model that approximates driving point admittance by nth order load. This model does not depend on the threshold points of the input voltage. The CMOS inverter is modeled using a linear resistor and a Thevenin voltage. The values of resistor and voltage are such that the gate output waveform and gate delay achieved is same as that achieved by actual CMOS inverter.

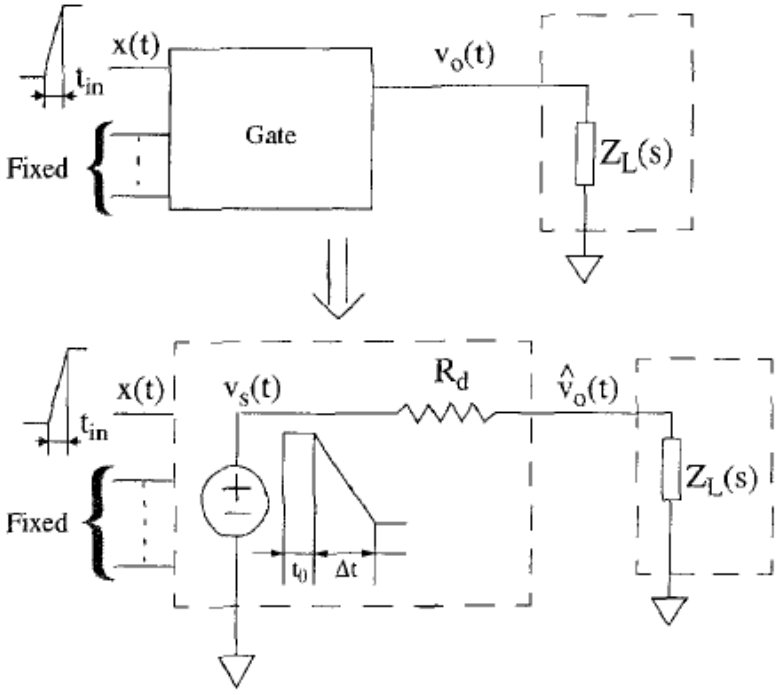

Fig. 2.10. Thevenin equivalent model for a CMOS gate [15].

After obtaining the resistance and voltage source values, the load is modelled using an appropriate effective capacitance by equating the average currents through loads.

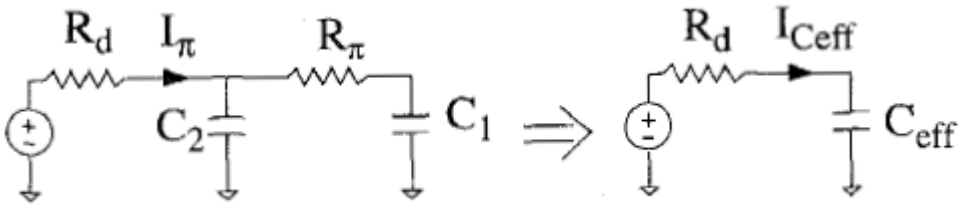

Fig. 2.11. Averaging the load currents to obtain effective capacitance [15].

The method of obtaining effective capacitance is presented for a second order model and it can be extended up to nth order model.

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T. Sakurai, A. Richard Newton (1990) [16] introduced the **α-power law MOS model**, a simple model for MOSFET, to consider the short-channel effects, which become pronounced in submicron technology. The Shockley MOSFET model is not able to predict the drain saturation voltage and drain saturation current for short channel MOSFETs due to velocity saturation effects. The proposed model suggests an improvement in Shockley's square law model mainly in the saturation region by introducing index alpha (α).

The model is given as:

$$I_D = \begin{cases} 0, & V_{GS} \leq V_{TH} : \text{Cutoff Region} \\ \left(\frac{I'_{D0}}{V'_{D0}}\right) V_{DS}, & V_{DS} < V'_{D0} : \text{Linear Region} \\ I'_{D0}, & V_{DS} \geq V'_{D0} : \text{Saturation Region} \end{cases} \quad (2.15)$$

where

$$I'_{D0} = I_{D0}\left(\frac{V_{GS} - V_{TH}}{V_{DD} - V_{TH}}\right)^{\alpha},$$

$$V'_{D0} = V_{D0}\left(\frac{V_{GS} - V_{TH}}{V_{DD} - V_{TH}}\right)^{\alpha/2},$$

V_{DD} is the supply voltage, V_{th} is the threshold voltage, α is the velocity saturation effect, V_{D0} is the drain saturation voltage at $V_{GS}= V_{DD}$, I_{D0} is the drain current at $V_{GS}=V_{DS}=V_{DD}$.

Because of its simplicity, it can be employed for analytically studying MOSFET circuits and understanding the behaviour of the in the sub-micrometer region**.**

B.K. Kaushik *et al.* (2007) [17] analysed the performance of RLC interconnect load driven by CMOS inverter. The MOSFET is modeled by using an Alpha-Power (α) law model [16] and the RLC interconnect is modeled by Π-model [13]. The output waveform and the propagation delay of the inverter are calculated by analytical computation. The analytical calculations are done for four different regions of operation of NMOS and PMOS transistors. By solving the differential equations for each of the four regions, the waveform of the output voltage at the far end of the Interconnect is achieved. Comparison is made with the SPICE simulations. The results of the SPICE simulations and analytically obtained results for the output voltage waveform and propagation delay are quite similar.

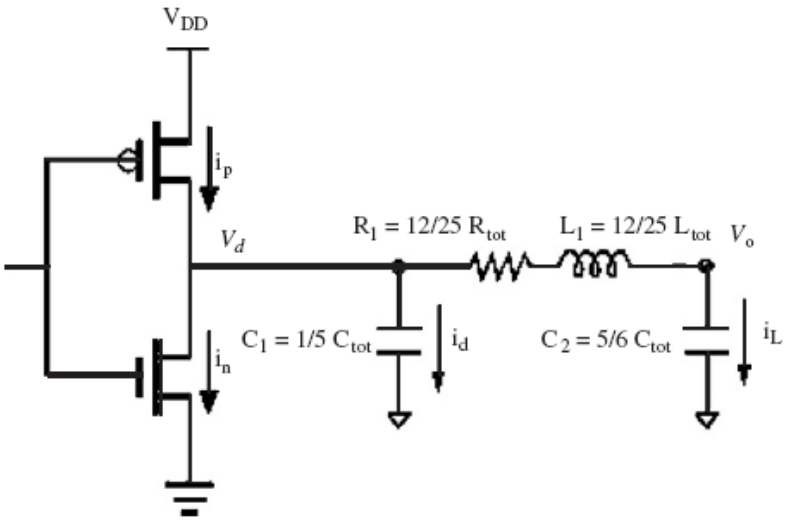

Fig. 2.12.CMOS inverter driving Π-load of an RLC interconnect [17].

2.3 Circuit modeling of carbon nanotubes

P.J. Burke [18] (2002) modeled spinless 1D quantum wire by resistance, capacitance and inductance. The inductance is modeled by magnetic inductance as well as kinetic inductance. The capacitance is modeled by quantum capacitance and electrostatic capacitance. He then presented the circuit model considering four conducting channels for SWCNT.

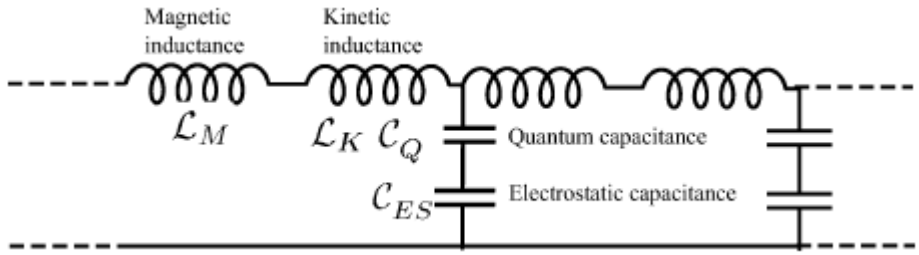

Fig. 2.13. Circuit modeling of SWCNT interconnect [18].

N. Srivastava and K. Banerjee [19] (2005) investigated performance of carbon nanotubes as a VLSI interconnect. They presented equivalent circuit model for SWCNT bundle interconnect. Using these model parameters, they compared the performance of SWCNT bundle with that of copper interconnects. The results show that SWCNT bundle can surpass copper interconnects at all levels (local, intermediate and global) of interconnects.

E. Pop *et al.* [20] (2005) presented the first account of temperature dependent model for SWCNT interconnects. They stated that at high temperatures (greater than 250k), for calculation of low bias resistance, in addition to the acoustic phonon scattering, the previously neglected optical phonon absorption is also to be taken into account.

M.K. Rai *et al.* [21**]** (2016) analyses the delay performance of SWCNT bundle interconnect using temperature dependent and temperature independent models. The improvement in delay estimated by temperature dependent model over temperature independent model is 22.44%. They also compared the delay performace of copper interconnects and SWCNT bundle interconnects for temperatures varying from 300K to 500K and length varying from 100 to 1000μm.

2.4 Conclusion

Various models were presented in this chapter to compute the delay. The gate delay is estimated by approximating the driving point admittance at the gate output by total capacitance, Π-load or an effective capacitance. The total capacitance load does not take into consideration the resistive shielding and hence delay estimated is more than the actual delay. The Π-load model although includes the resistive shielding effect, but

it is incompatible with the k-factor equations. The effective capacitance models presented require a number of iterations to obtain value of effective capacitance. They model the transistor incorrectly as a linear resistor. The transistor operates in cutoff, saturation and linear regions during its operation and thus cannot be modeled using a linear resistor.

Chapter 3 Temperature- dependent circuit modeling of SWCNT bundle interconnect

3.1 Introduction

With scaling of technologies to deep submicron regime, copper interconnects are facing many problems and their replacement is being considered. Carbon nanotubes with their extraordinary properties are being considered as an alternative. The modelling of circuit parameters for SWCNT interconnects is presented in this chapter to assist the performance analysis of interconnects. As the thermal issues are on a rise due to increase in operating temperature, the circuit modelling presented is temperature-dependent.

3.2 Carbon Nanotubes

Carbon, due to different arrangements of its atoms, can form many different structures called allotropes. One of these structures is Carbon Nanotube. It was discovered in 1991 by Sumio Iijima [22]. Carbon Nanotubes are formed by rolling up of graphene sheets in the form of cylinder, the diameter being in the range of a few nano meters. Graphene is single atomic layer of graphite. As can be seen in Fig.3.1, graphite is a stack of graphene held together by weak van der Waal's forces. Graphene has a two-dimensional structure in which the carbon atoms are arranged in a honeycomb lattice.

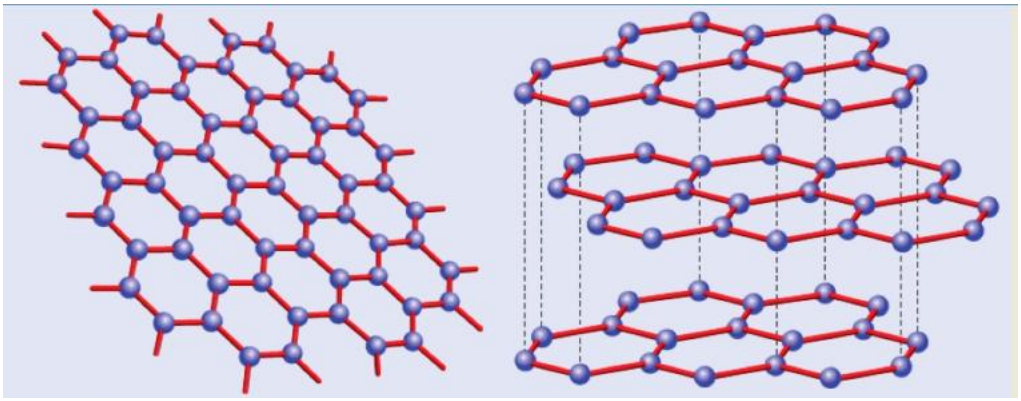

Fig.3.1. Graphene sheet (on the left), Structure of graphite (on the right) [23].

Depending upon the chirality i.e. direction in which the graphene sheets are rolled up, carbon nanotubes can be metallic or semiconducting in nature. This direction is represented by using a two-dimensional lattice vector $R = nR_1 + mR_2$ [24]. Here n and m are chiral indices. Along the direction of (n, m), the sheet is rolled up. As shown in Fig.3.2, when both the indexes are same (n= m), the edge of circumference is in the shape of armchair, therefore it is called armchair carbon nanotube [25]. For (n, 0), the edge of circumference is in zigzag form, therefore it is called zigzag carbon nanotube. These two types of CNTs are achiral. For all other directions, the carbon nanotube is chiral.

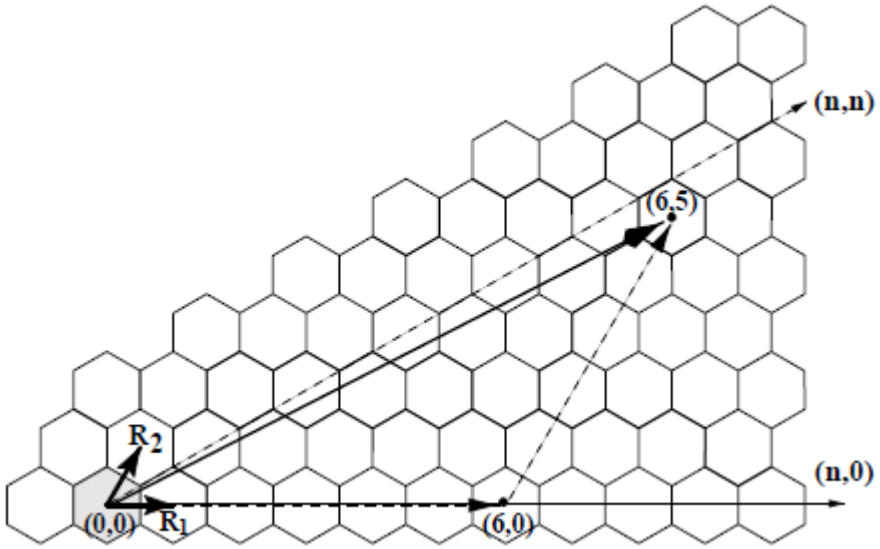

Fig. 3.2. Two dimensional graphene lattice structure [24].

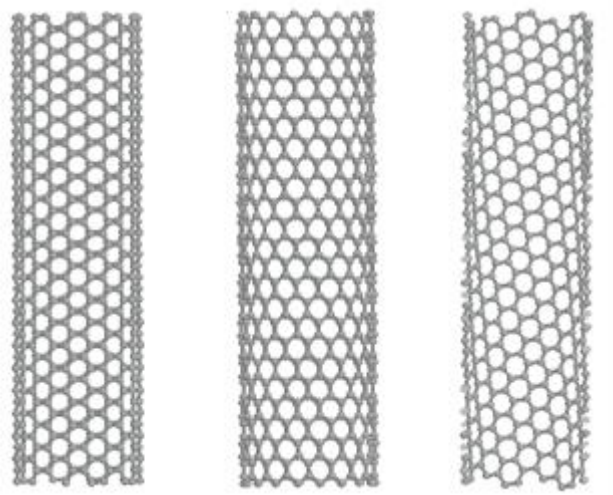

Fig. 3.3. Armchair, zigzag and chiral carbon nanotubes [26].

Armchair Carbon Nanotubes are always metallic, while zigzag carbon nanotubes can be metallic or semiconducting in nature. Semiconducting CNTs are expected to replace silicon transistors in future by becoming a potential material used for channel formation. The metallic CNTs are potential candidates for use as VLSI interconnects.

On the basis of structure, carbon nanotubes can be classified into SWCNT (Single-walled carbon nanotube) and MWCNT (Multi-walled carbon nanotube) as shown in Fig. 3.4 and Fig. 3.5. When a single graphene sheet is rolled into a seamless cylinder, then it is called SWCNT. Whereas when a number of graphene sheets with different diameters are arranged in concentric cylinders, then the resulting structure is called MWCNT. MWCNTs are diffusive conductors and are incapable of ballistic transport [27]. Whereas SWCNTs are ballistic conductors and thus are suitable for use as VLSI interconnects.

Fig. 3.4. Single walled carbon nanotube [28].

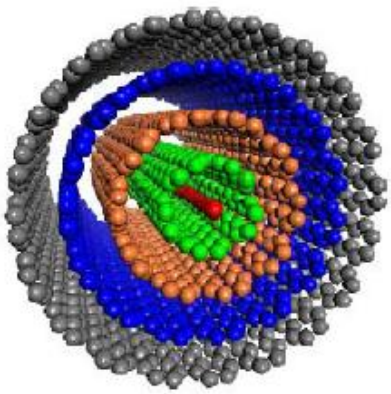

Fig. 3.5. Multi walled carbon nanotube [28].

3.3 Temperature-dependent modelling of impedance parameters of isolated SWCNT

Equivalent circuit model for an SWCNT as shown in Fig.3.6 comprises of resistance, inductance and capacitance. The equations used for calculating these parameters are presented in this section.

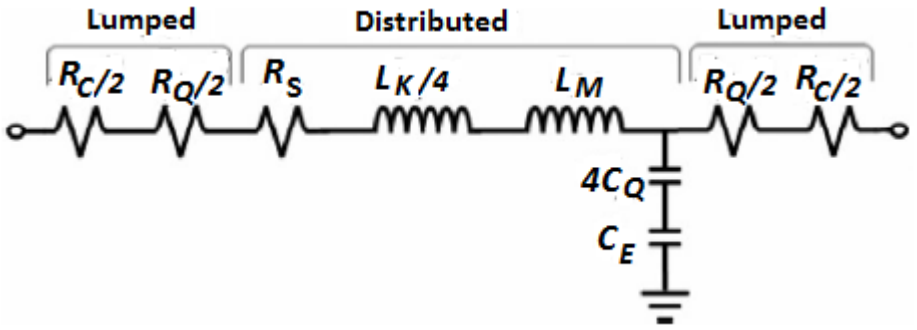

Fig. 3.6. Equivalent circuit model for an isolated SWCNT [29].

3.3.1 Calculation of Resistance of SWCNT interconnect

According to the two-terminal Landauer-Buttiker formula ,the conductance(G) of 1D system is given as $G = \frac{Ne^2T}{h}$, where N is the number of conducting channels, T is the transmission coefficient for electrons through the sample and h is the Planck's constant. As an isolated SWCNT has four conducting channels, therefore its conductance (taking T=1 for perfect contacts) is given as $G = \frac{4e^2}{h}$, which evaluates to 155μS, equivalent to a resistance of 6.45KΩ. This fundamental resistance is termed as the quantum resistance.

$$R_Q = \frac{h}{4e^2} \tag{3.1}$$

Also, there is a contact resistance R_C due to the imperfect metal-nanotube contacts. If the length of CNT is less than the mean free path of electrons, then the resistance of CNT is independent of its length and is equal to the above stated fundamental resistance. But, if the CNT length is greater than the mean free path, then an additional resistance called the scattering resistance has to be taken account. This scattering resistance is represented as distributed resistance per unit length.

$$R_S = \frac{h}{4e^2}\frac{l}{\lambda}, \tag{3.2}$$

where l is the length of CNT and λ is the mean free path of electrons. λ is determined by the scattering mechanism, which depends on the temperature, voltage bias and length of the interconnect.

At high voltage bias (>160mV), the scattering due to optical or zone-boundary phonon emission dominates [30]. This backscattering leads to decrease in conductance with increase in bias voltage, and above a certain voltage, the current saturates i.e. the conductance vanishes. However, interconnects operate at low bias. At low voltage biases, acoustic phonon scattering dominates and the SWCNT shows perfect ohmic behaviour. So the above stated resistance modeling is completely valid.

However, for low voltage bias, at high temperatures (above 250K), scattering due to optical phonon absorption can no longer be neglected [20]. It must be taken into account, along with previously considered phonon scattering, to model the resistance of SWCNT interconnect.

$$R_{CNT}(T) = \frac{\mathrm{h}}{4\mathrm{e}^2} + \frac{h}{4e^2}\frac{l}{\lambda(T)} + R_C, for\ l > \lambda \tag{3.3}$$

where λ(T) is the temperature dependent mean free path of electrons.

$$\lambda(\mathrm{T}) = (\lambda_{\mathrm{AC}}^{-1} + \lambda_{\mathrm{Op,ems}}^{-1} + \lambda_{\mathrm{Op,abs}}^{-1})^{-1}, \tag{3.4}$$

where λ_{AC} is the MFP due to acoustic scattering, $\lambda_{\mathrm{Op,ems}}$ is the MFP due to optical emission and $\lambda_{\mathrm{Op,abs}}$ is the MFP due to optical absorption [20, 31].

$$\lambda_{\mathrm{AC}} = \lambda_{\mathrm{AC,300}}\frac{300}{\mathrm{T}}, \tag{3.5}$$

where $\lambda_{AC,300}$ (acoustic scattering length at 300K) ≈1600nm

$$\lambda_{\mathrm{Op,abs}} = \lambda_{\mathrm{Op,300}}\frac{\mathrm{Nop(300)+1}}{\mathrm{Nop(T)}}, \tag{3.6}$$

where $\lambda_{\mathrm{Op,300}}$ (spontaneous OP emission length at 300 K) ≈ 15 nm

The optical emission can be due to the electric field and due to optical absorption.

$$\lambda_{\mathrm{Op,ems}} = (1/\lambda_{\mathrm{Op,ems}}^{\mathrm{fld}} + 1/\lambda_{\mathrm{Op,ems}}^{\mathrm{abs}})^{-1} \tag{3.7}$$

$$\lambda_{Op,ems}^{fld}(T) = \frac{\hbar w_{Op}}{eV_{DD}} L + \frac{Nop(300)+1}{Nop(T)+1}\lambda_{Op,300}, \quad (3.8)$$

where $\hbar\omega_{Op}$ (OP emission threshold energy) ≈ 0.18eV

$$\lambda_{Op,ems}^{abs}(T) = \lambda_{Op,abs} + \frac{Nop(300)+1}{Nop(T)+1}\lambda_{Op,300} \quad (3.9)$$

where $Nop(T) = \frac{1}{[\exp(\hbar w_{Op}/K_B T)^{-1}]}$ is the OP occupation.

3.3.2 Calculation of Capacitance of SWCNT interconnect

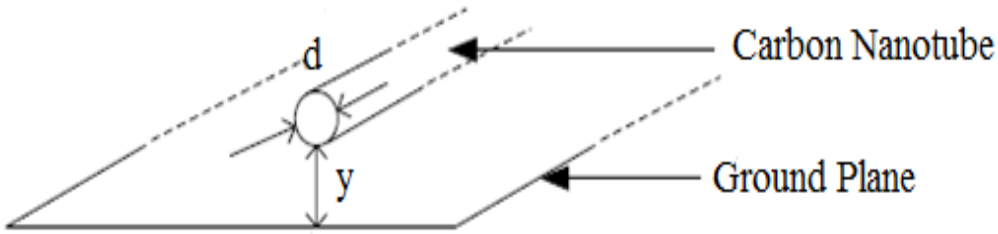

Fig. 3.7. Isolated SWCNT with diameter 'd' above distance 'y' from the ground [19].

Capacitance of SWCNT is due to two components: Electrostatic capacitance and Quantum capacitance.

The electrostatic capacitance of a carbon nanotube with diameter 'd' at 'y' distance above ground plane as shown in Fig.3.7 is given by [18].

$$C_E = \frac{2\pi\epsilon}{cosh^{-1}(2y/d)} \quad (3.10)$$

As y>2d, it can be approximated as:

$$C_E \approx \frac{2\pi\epsilon}{ln\frac{y}{d}} \quad (3.11)$$

This is the electrostatic capacitance per unit length.

According to the Pauli Exclusion Principle, an electron can be added only to the quantum states available above Fermi energy, E_F. The spacing between quantum states is given by

$$\delta E = \frac{dE}{dk}\delta k = \hbar v_F \frac{2\pi}{l}, \tag{3.12}$$

where l is the length of the CNT and v_F is the Fermi velocity.

The effective capacitance corresponding to this energy is called the Quantum Capacitance C_Q (per unit length).

$$C_Q = \frac{2e^2}{hv_F} \tag{3.13}$$

For carbon nanotube, $v_F = 8 \times 10^5$ m/s [19] gives C_Q=100aF/μm

The total capacitance C_{CNT} of carbon nanotube is obtained by the series combination of these two capacitances.

$$\mathrm{C_{CNT}}^{-1} = \mathrm{C_E}^{-1} + 4\mathrm{C_Q}^{-1} \tag{3.14}$$

The effective quantum capacitance considered is $4C_Q$ because of the parallel combination of four quantum capacitances (one capacitance each for four conducting channels in SWCNT).

3.3.3 Calculation of Inductance of SWCNT interconnect

The magnetic inductance is obtained by equating the stored magnetic energy with the inductive energy $\frac{1}{2}LI^2$. The magnetic inductance L_M per unit length is given as

$$L_M = \frac{\mu}{2\pi} ln \frac{y}{d} \tag{3.15}$$

Similarly, the kinetic inductance L_K per unit length is calculated by setting the kinetic energy equal to inductive energy.

$$L_K = \frac{h}{2e^2 v_F} \tag{3.16}$$

For carbon nanotube, $v_F = 8 \times 10^5$ m/s [18] gives L_K=16nH/μm

The total inductance per unit length L_{CNT} is given by the series combination of magnetic and kinetic inductance.

$$L_{CNT} = L_M + \frac{L_K}{4} \tag{3.17}$$

The effective kinetic inductance is $\frac{L_K}{4}$ because of parallel combination of four kinetic inductances.

3.4 SWCNT bundle interconnect

The resistance offered by an isolated singled-walled carbon nanotube is quite high. It keeps on increasing with increase in length, the minimum value (considering only intrinsic resistance with perfect contacts) being $\frac{h}{4e^2}$ (around 6KΩ). With such a large value of resistance, SWCNT is quite unsuitable to be used as a VLSI interconnect.

To reduce the resistance, carbon nanotubes are connected in parallel in X-Y plane to form a single effective interconnect wire [32]. By stacking up these parallel interconnects one above the other (in Z-direction) as shown in Fig.3.8, the effective resistance can be further reduced.

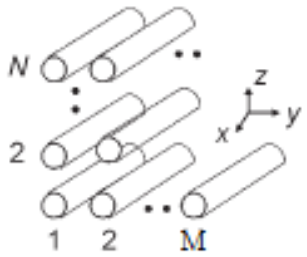

Fig. 3.8. Stacked CNT interconnects [32].

A carbon nanotube bundle interconnect is formed by identical metallic single-walled carbon nanotubes packed in a hexagonal fashion [19]. Each SWCNT with diameter ‘d’ is surrounded by six immediate neighbours, their centres uniformly separated by a distance ‘*x*’. As shown in Fig.3.9, the structure in which ‘x’ =‘d’ is called densely packed structure whereas the one with ‘x’>’d’ is called sparsely packed structure. Out of the two structures, the densely packed structure has better interconnect performance.

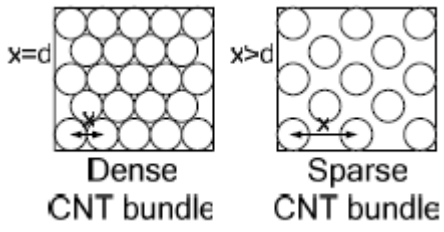

Fig. 3.9. Dense and sparse carbon nanotube bundle [19].

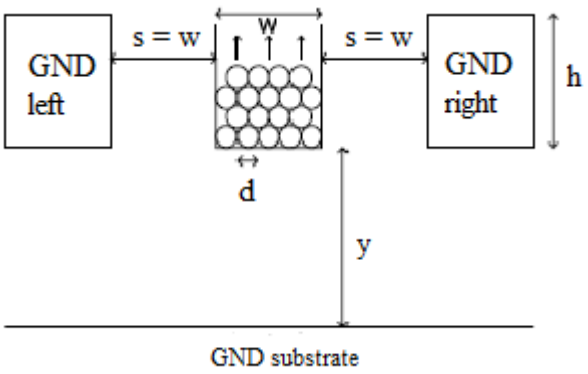

Fig. 3.10. Interconnect geometry for SWCNT bundle [19].

The interconnect structure to be taken into account is shown in Fig. 3.10. 'w' is the width of the interconnect, 'h' is the height of the interconnect, 'y' is the distance of the interconnect from ground substrate, and the separation 's' between adjacent interconnects is taken to be equal to width 'w'.

Table 3.1 ITRS 2012 based simulation parameters of interconnects for 22nm technology.

	Local	Intermediate	Global
Width 'w' (nm)	19	19	29
Height 'h'(nm)	38	38	68
ILD Thickness 'y'(nm)	38	35	43.5
Separation between adjacent bundles 's'(nm)	19	19	29
ε_{ox}(relative)	4.2	3.25	3.25

3.4.1 Calculation of number of CNTs in a bundle

Number of columns n_W in the SWCNT bundle is given as $n_W = \left\lfloor \frac{w-d}{x} \right\rfloor + 1$ (3.18)

Number of rows n_H in the SWCNT bundle is given as $n_H = \left\lfloor \frac{h-d}{(\sqrt{3}/2)x} \right\rfloor + 1$ (3.19)

where $\lfloor a \rfloor$ denotes the largest integer less than or equal to 'a'.

Then the total number of CNTs, n_{CNT} in the bundle will be:

$n_{CNT} = n_W n_H - \frac{n_H}{2}$, if n_H is even (3.20)

$n_{CNT} = n_W n_H - \frac{n_H - 1}{2}$, if n_H is odd (3.21)

3.4.2 Resistance of SWCNT bundle

Resistance of an SWCNT bundle is given by

$$R_{tot} = \frac{R_{CNT}}{n_{CNT}}, \quad (3.22)$$

where R_{CNT} is the resistance of an isolated SWCNT and n_{CNT} is the number of CNTs in a bundle.

3.4.3 Capacitance of SWCNT bundle

The quantum capacitance of the bundle is given as

$$C_{Q,bundle} = C_Q \times n_{CNT}, \quad (3.23)$$

where $C_Q = \frac{2e^2}{hvf}$ is the quantum capacitance (from equation 3.13) and n_{CNT} is the number of CNTs in a bundle.

The electrostatic capacitance of the bundle is given as

$$C_{E,bundle} = 2C_{en} + \frac{n_W - 2}{2} C_{ef} + \frac{3(n_H - 2)}{5} C_{en}, \quad (3.24)$$

where $C_{en} = \frac{2\Pi\varepsilon o\varepsilon x}{\ln(s/d)}$ and is calculated assuming the ground plane to be at a distance equal to the separation distance 's' from the "near" adjacent interconnect ,

$C_{ef} = \frac{(2\Pi\varepsilon x\varepsilon o)}{(log((s+w)/d)}$ and is calculated assuming the ground plane to be at a distance equal to the separation distance from the "far" adjacent interconnect

On obtaining the electrostatic and quantum capacitances of the bundle, the capacitance of the bundle per unit length can be calculated as:

$$\frac{1}{C_{bundle}} = \frac{1}{C_{Q,bundle}} + \frac{1}{C_{E,bundle}} \quad (3.25)$$

The total capacitance C_{tot} is:

$C_{tot=}$ C_{bundle} × length of interconnect (3.26)

3.4.4 Inductance of SWCNT bundle

Inductance of an SWCNT bundle is simply given by

$$L_{tot} = \frac{L_{CNT}}{n_{CNT}}, \quad (3.27)$$

where L_{CNT} is the Inductance of an isolated SWCNT (see equation 3.17) and n_{CNT} is the number of CNTs in a bundle(see equations 3.20, 3.21).

3.5 Modelling of circuit parameters of Copper Interconnects

Resistance of copper as a function of temperature is given as [33, 34]:

$$R(T) = Ro\ (1+ \alpha\ (T - To))\ , \quad (3.28)$$

where To=300K is the room temperature,

α is the temperature coefficient of resistance at room temperature (for copper α= $0.0039K^{-1}$), Ro is the resistance of copper at room temperature and is given as:

$$Ro = \rho_o.\frac{l}{w.h}\ , \quad (3.29)$$

where ρ_o is the resistivity of copper at room temperature.

Inductance and Capacitance are temperature independent parameters and are obtained using the following formulae [21, 29]:

Inductance is given as:

$$L_S = \frac{\mu_0 l}{2\pi}\left[ln\frac{2l}{w+h} + 0.5 + \frac{0.22(w+h)}{l}\right], \tag{3.30}$$

where l, w and h are respectively the length, width and height of the interconnect.

Capacitance with respect to ground is given as:

$$C_g = \epsilon\left[\frac{w}{y} + 2.22\left(\frac{s}{s+0.7y}\right)^{3.19} + 1.17\left(\frac{s}{s+1.15y}\right)^{0.76}\left(\frac{s}{h+4.53y}\right)^{0.12}\right] \tag{3.31}$$

Coupling capacitance between adjacent interconnects is given as:

$$C_C = \epsilon\left[1.14\frac{h}{s}\left(\frac{y}{y+2.06s}\right)^{0.09} + 0.74\left(\frac{w}{w+1.59s}\right)^{1.14} + 1.16\left(\frac{w}{w+1.87s}\right)^{0.16}\left(\frac{y}{y+0.98s}\right)^{1.18}\right] \tag{3.32}$$

3.6 Conclusion

The impedance parameters for both isolated SWCNT interconnects and SWCNT bundle interconnects are presented. The resistance of an isolated SWCNT is quite high so it is the SWCNT bundle which can be used as VLSI Interconnect. The modelling of parameters is temperature dependent. The equivalent circuit parameters of copper are also presented.

Chapter 4 Temperature dependent delay model for SWCNT bundle interconnect

4.1 Introduction

Delay is one of the most important parameters for performance estimation of a VLSI circuit. The overall logic stage delay comprises of two components: gate delay and interconnect delay. The driving point admittance at gate output can be simply modelled using a lumped capacitance. The gate delay is expressed as a function of load capacitance and input transition time by using k factor equations [35].

$$t_d = k(C_L, \tau) \tag{4.1}$$

But with decrease in feature size, the resistance of interconnect is increasing and becoming comparable to the gate resistance. The interconnect resistance provides resistance shielding i.e. the load capacitance seen by the gate reduces, leading to decrease in the gate delay. Thus, the resistance of interconnect can no longer be neglected. Various delay models for RC interconnects [12, 36, 37] were presented. Also, with increase in clock frequency and with wider wires, the inductance must also be taken into account to model the interconnect [11, 38-41]. So by taking both resistance and inductance into consideration, a Π model [13] for RLC interconnects was proposed, to estimate the driving point admittance at the output gate output. To express gate delay in the form of empirically derived k-factor equations, Π model parameters (R_π, L_π, C_1, C_2) must be taken into account. The look up-table will become 5D instead of 2D. It is impractical from storage point of view. To make Π model compatible with k-factor equations, it is replaced by an effective capacitance model [14]. Previously proposed effective capacitance models obtain the appropriate capacitance by running a number of iterations [14, 15, 42], and the driver is approximated by a voltage source and a resistor [15, 42]. A new effective capacitance model is presented which accurately represents driving transistor using alpha power law model [16] and all the four operating regions are considered. Also, the suitable value of effective capacitance is obtained in a single go, instead of undergoing a number of iterations.

4.2 Piecewise transient delay model of SWCNT bundle interconnect

The gate delay and gate output waveform is obtained by estimating the driving point admittance at gate output as an effective capacitance. This gate output waveform is then fitted into a ramp response and is used to drive the distributed interconnect. Thus the far end interconnect waveform and interconnect delay is obtained. The overall logic stage delay is obtained by summing up the two components.

4.2.1 Calculation of gate delay

The circuit consists of a CMOS inverter driving an RLC interconnect line. For computation of gate delay, as shown in Fig.4.1, the load seen by the gate is modelled by a π circuit, which is further mapped to an effective capacitance.

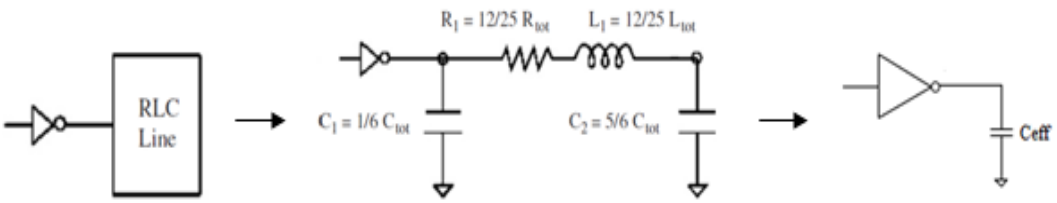

Fig.4.1. An effective capacitance model of the driving point admittance for the RLC Interconnect.

For effective capacitance to suitably replace the π model, the gate delay with capacitive load as well as pi-load should be the same. To accomplish this, the average current through the capacitive load is equated with that through pi-load upto 50% delay time, t_D . t_D is the time at which gate output reaches 50% of its final value.

To approximate t_D, the expression for gate output voltage with π load is obtained analytically. The circuit under consideration is shown in Fig.4.2.

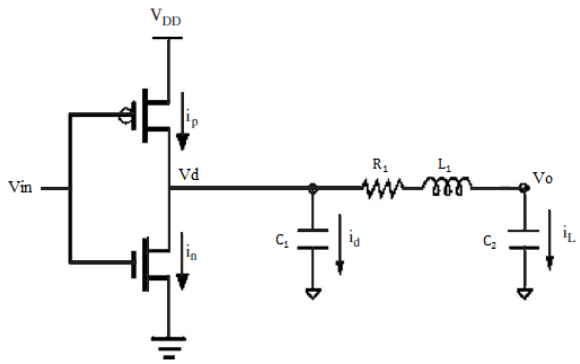

Fig.4.2. CMOS gate driving equivalent Π-model of an RLC interconnect line [17].

The driving transistor is modelled using alpha power law model [16]. The model in equation form is given as:

$$I_D = \begin{cases} 0, & V_{GS} \leq V_{T0} : \text{Cutoff Region} \\ k_l(V_{GS} - V_{T0})^{\alpha/2} V_{DS}, & V_{DS} < V_{D-Sat} : \text{Linear Region} \\ k_s(V_{GS} - V_{T0})^{\alpha}, & V_{DS} \geq V_{D-Sat} : \text{Saturation Region} \end{cases} \quad (4.2)$$

where V_{DSat} is the drain saturation voltage, k_l, k_s are the transconductance parameters in linear and saturation regions respectively, α is the velocity saturation index and V_{T0} is the threshold voltage.

A rising ramp with transition time τ is given as input to the CMOS inverter. Two types of ramp inputs are considered: fast input ramp and slow input ramp. For fast (slow) inputs, the nMOS device is in saturation (in the linear region) when the input voltage reaches its final value.

Four different regions of operation are considered for two cases of ramp input.

Fast input ramp:

Region 1($0<t<t_1$): t_1 is the time at which $V_{in} = V_{T0.}$ During this region, the nMOS transistor is cut off. Therefore $i_n = 0$. Thus KCL at near end of interconnect gives

$$i_d + i_L = 0 \quad (4.3)$$

$$i_d = C_1 \frac{dV_d}{dt}$$

$$i_L = C_2 \frac{dV_0}{dt}$$

where V_d is the voltage at the near end of interconnect and V_0 is the voltage at the far end of interconnect.

On applying KVL, we get $V_d = LC_2 \frac{d^2V_0}{dt^2} + RC_2 \frac{dV_0}{dt} + V_0$ (4.4)

Substituting the values of i_d, i_L and V_d in equation (2) gives the following differential equation

$$a\frac{d^3V_0}{dt^3} + b\frac{d^2V_0}{dt^2} + \frac{dV_0}{dt} = 0 \quad (4.5)$$

where $a = \frac{C_1C_2L}{C_1+C_2}$, $b = \frac{C_1C_2R}{C_1+C_2}$, $t_1 = \frac{\tau V_{T0}}{V_{DD}}$

The output V_0 remains equal to V_{DD} till time t_1.

Region 2 (t_1<t< Ƭ): The nMOS device operates in saturation and the input signal is varying linearly. -

Differential equation:

$$a\frac{d^3V_0}{dt^3} + b\frac{d^2V_0}{dt^2} + \frac{dV_0}{dt} + \frac{k_s}{(C_1+C_2)}\left(\frac{V_{DD}}{\tau}t - V_{T0}\right)^{\alpha} = 0 \qquad (4.6)$$

The current term is approximated by second order Taylor series at t=Ƭ/2 (where $V_{in} = \frac{V_{DD}}{2}$) as

$$\frac{i_n}{(C_1+C_2)} = A_0 + A_1t + A_2t^2 \qquad (4.7)$$

The solution of the differential equation is:

$$V_0(t) = K_1t^3 + K_2t^2 + K_3t - K_4e^{-(b-M)t/2a} - K_5e^{-(b+M)t/2a} + C_3, \qquad (4.8)$$

where $M = \sqrt{b^2 - 4a}$, $K_1 = \frac{-A_2}{3}$, $K_2 = A_2b - \frac{A_2}{3}$, $K_3 = 2aA_2 - 2b^2A_2 - A_0 + bA_1$, $K_4 = 2aC_2/b - M$, $K_5 = 2aC_1/b + M$,

C_1, C_2 and C_3 are the integration constants.

Region 3 (Ƭ < t < t2): The input has reached its final value and the nMOS transistor is still in saturation. At time t2, $V_d = V_{DSat}$. The differential equation is

$$a\frac{d^3V_0}{dt^3} + b\frac{d^2V_0}{dt^2} + \frac{dV_0}{dt} + A_3 = 0 \qquad (4.9)$$

where $A_3 = \frac{k_s}{(C_1+C_2)}(V_{DD} - V_{t0})^{\alpha}$

Solution is

$$V_0(t) = C_6 - A_3t - K_6e^{-(b-M)t/2a} - K_7e^{-(b-M)t/2a}, \qquad (4.10)$$

where $K_6 = 2aC_5/b - M$, $K_7 = 2aC_4/b + M$,

C_4, C_5 and C_6 are the integration constants.

Time t_2 is obtained by putting V_d equal to the drain saturation voltage.

$$V_d(t_2) = LC_2 \frac{d^2V_0}{dt^2} + RC_2 \frac{dV_0}{dt} + V_0 = V_{DSat} \quad (4.11)$$

Time t_D is obtained by putting V_d equal to $\frac{V_{DD}}{2}$

Region 4($t > t_2$): The nMOS transistor operates in linear region. The differential equation describing this state of operation is given as

$$a \frac{d^3V_0}{dt^3} + K_8 \frac{d^2V_0}{dt^2} + K_9 \frac{dV_0}{dt} + K_{10}V_0 = 0 \quad (4.12)$$

where

$$K_8 = \frac{nLC_2}{C_1 + C_2} + b \ , K_9 = \frac{nRC_2}{C_1 + C_2} + 1 \ , K_8 = \frac{n}{C_1 + C_2} \ , n = k_l(V_{DD} - V_{t0})^{\alpha/2}.$$

According to [16], k_l can be obtained from I_{D0} and V_{D0} as:

$$k_l = \frac{I_{D0}}{V_{D0}(V_{DD} - V_{t0})} \quad (4.13)$$

Solution of differential equation is:

$$V_0(t) = C_7 e^{(-1/2(\beta^{2/3} - 12aK_9 + 4K_8^2 + 4K_8\beta^{1/3} - 3\beta^{2/3} - 36aK_9 + 12K_8^2)t/\alpha\beta^{1/3})} \quad (4.14)$$

$$+ C_8 e^{(1/2(-\beta^{2/3} + 12aK_9 + 4K_8^2 + 4K_8\beta^{1/3} - 3\beta^{2/3} - 36aK_9 + 12K_8^2)t/\alpha\beta^{1/3})}$$

$$+ C_9 e^{(1/6(-\beta^{2/3} + 12aK_9 + 4K_8^2 + 4K_8\beta^{1/3})t/\alpha\beta^{1/3})},$$

Where C_7, C_8 and C_9 are the integration constants and

$$\beta = 36aK_8K_9 - 108a^2K_{10} - 8K_8^3$$

$$+12\sqrt{3}(4aK_9^3 - K_8^2K_9^2 - 18aK_8K_9K_{10} + 27a^2K_{10}^2 + 4K_8^3K_{10})^{\frac{1}{2}}a \quad (4.15)$$

Slow input ramps:

For slow input ramps, first two operating regions are same as that of fast input ramps. The only difference is that the second region is till time t2 instead of Ţ, where (t2< Ţ).

Region 3(t2<t<Ţ): The nMOS transistor operates in linear region and the input signal is varying linearly. The differential equation is given as:

$$a\frac{d^3V_0}{dt^3} + K_{11}\frac{d^2V_0}{dt^2} + K_{12}\frac{dV_0}{dt} + K_{13}V_0 = 0 \quad (4.16)$$

To solve this equation, it is assumed that the gate-source voltage of the nMOS is an average value $\tilde{V}_{in}$

$\tilde{V}_{in} = \frac{V_{in}(t_2)+V_{DD}}{2}$, where $V_{in}(t_2) = \frac{V_{DD}t_2}{\tau}$ (4.17)

Solution of differential equation is:

$$V_0(t) = C_{10}e^{(-1/2(\chi^{2/3}-12aK_{12}+4K_{11}^2+4K_{11}\chi^{1/3}-3\chi^{2/3}-36aK_{12}+12K_{11}^2)t/a\chi^{1/3})} \quad (4.18)$$

$$+ C_{11}e^{(1/2(-\chi^{2/3}+12aK_{12}+4K_{11}^2+4K_{11}\chi^{1/3}-3\chi^{2/3}-36aK_{12}+12K_{11}^2)t/a\chi^{1/3})}$$

$$+ C_{12}e^{((1/6(-\chi^{2/3}-12aK_{12}+4K_{11}^2+4K_{11}\chi^{1/3})t/a\chi^{1/3}))},$$

where $\chi = 36aK_{11}K_{12} - 108a^2K_{13} - 8K_{11}^3$

$$+12\sqrt{3}(4aK_{12}^3 - K_{11}^2K_{11}^2 - 18aK_{11}K_{12}K_{13} + 27a^2K_{13}^2 + 4K_{11}^2K_{13})^{1/2}a\,,$$

$k_l = \frac{I_{D0}}{V_{D0}(\tilde{V}_{in}-V_{t0})^{\alpha/2}}$, $m = k_l(\tilde{V}_{in}-V_{t0})^{\alpha/2}$, $K_{11} = \frac{mLC_2}{C_1+C_2} + b$, $K_{12} = \frac{mRC_2}{C_1+C_2} + 1$,$K_{13} = \frac{m}{C_1+C_2}$

And C_{10}, C_{11} and C_{12} are the integration constants.

Region 4 is same as that of fast input ramps.

From the above analysis, the values of $V_{d,}$ V_0 and t_D required for calculations of average current are obtained. Thus, as shown in Fig.4.3, to calculate the value of effective capacitance, the average current through effective capacitance load is equated with the average current through pi-load.

$$\bar{I}_{Ceff} = \bar{I}_{C\pi} \quad (4.19)$$

$$\frac{1}{t_D}\int_0^{t_D} I_{Ceff}dt = \frac{1}{t_D}\int_0^{t_D} I_{C\pi}dt \quad (4.20)$$

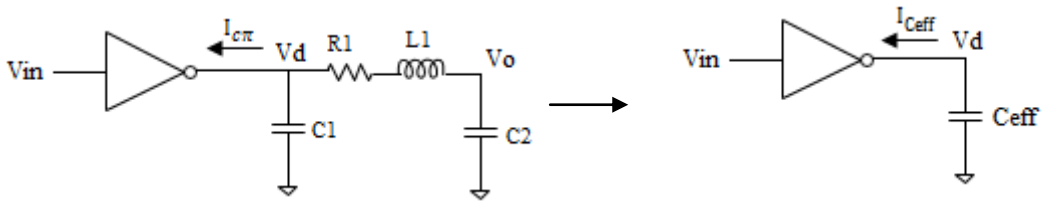

Fig.4.3. Mapping of Π-load into an equivalent effective capacitance load.

Average current through any capacitor C upto time T is given as

$$\bar{I_C}(t) = \frac{1}{T}\int_0^T C\dot{V_c}dt \tag{4.21}$$

Where V_c is the voltage across the capacitor and $\dot{V_c} = \frac{dV_c}{dt}$

For slow input ramps, equation (4.21) for capacitances C_{eff}, C_1, C_2 can be written as

$$\bar{I}_{Ceff}(t) = \frac{1}{t_D}\int_0^{t_D} C_{eff}\dot{V_d}dt = \frac{1}{t_D} C_{eff}\left(\int_0^{t_1}\dot{V_d}dt + \int_{t_1}^{t_D}\dot{V_d}dt\right) \tag{4.22}$$

$$\bar{I}_{C\pi} = \bar{I}_{\pi-C1} + \bar{I}_{\pi-C2} \tag{4.23}$$

$$\bar{I}_{\pi-C1}(t) = \frac{1}{t_D}\int_0^{t_D} C_1\dot{V_d}dt = \frac{1}{t_D} C_1\left(\int_0^{t_1}\dot{V_d}dt + \int_{t_1}^{t_D}\dot{V_d}dt\right) \tag{4.24}$$

$$\bar{I}_{\pi-C2}(t) = \frac{1}{t_D}\int_0^{t_D} C_2\dot{V_0}dt = \frac{1}{t_D} C_2\left(\int_0^{t_1}\dot{V_0}dt + \int_{t_1}^{t_D}\dot{V_0}dt\right) \tag{4.25}$$

where V_d is the near-end interconnect voltage , V_0 is the far-end interconnect voltage and t_D

is the time at which V_d reaches its 50% value.

For fast input ramps, equation (4.21) for capacitance C_{eff}, C_1, C_2 can be written as

$$\bar{I}_{Ceff}(t) = \frac{1}{t_D}\int_{t_1}^{t_D} C_{eff}\dot{V_d}dt = \frac{1}{t_D} C_{eff}\left(\int_0^{t_1}\dot{V_d}dt + \int_{t_1}^{\tau}\dot{V_d}dt + \int_{\tau}^{t_D}\dot{V_d}dt\right) \tag{4.26}$$

$$\bar{I}_{C\pi} = \bar{I}_{\pi-C1} + \bar{I}_{\pi-C2} \tag{4.27}$$

$$\bar{I}_{\pi-C1}(t) = \frac{1}{t_D}\int_{t_1}^{t_D} C_1\dot{V_d}dt = \frac{1}{t_D} C_1\left(\int_0^{t_1}\dot{V_d}dt + \int_{t_1}^{\tau}\dot{V_d}dt + \int_{\tau}^{t_D}\dot{V_d}dt\right) \tag{4.28}$$

$$\bar{I}_{\pi-C2}(t) = \frac{1}{t_D}\int_{t_1}^{t_D} C_2\dot{V}_0 dt \;\; = \frac{1}{t_D} C_2 \left(\int_0^{t_1} \dot{V}_0 dt + \int_{t_1}^{\tau} \dot{V}_0 dt + \int_{\tau}^{t_D} \dot{V}_0 dt \right) \qquad (4.29)$$

where V_d is the near-end interconnect voltage , V_0 is the far-end interconnect voltage and t_D

is the time at which V_d reaches its 50% value.

These values of average currents are substituted in equation (4.19) and thus the effective capacitance is obtained.

Using this value of effective capacitance, the gate output waveform and gate delay is obtained. As shown in Fig.4.4, these values are then compared with the values obtained when considering the Π-load.

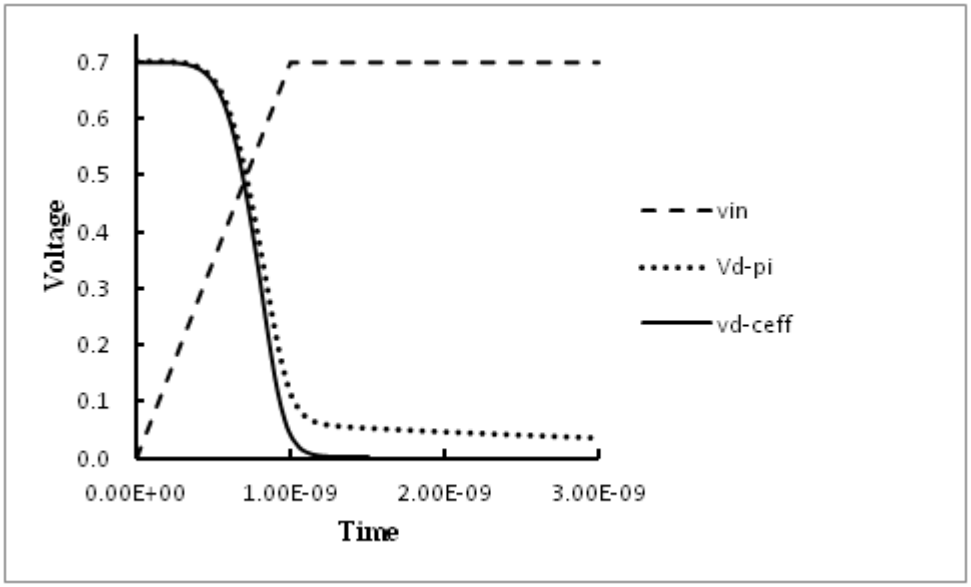

Fig.4.4. Comparison of gate output waveform when using a Π-load and an effective capacitance load to model the driving point admittance.

The simulated waveforms show that the till the 50% delay point (time when output reaches $\frac{V_{DD}}{2}$ value), the output voltage with capacitive load is almost identical to the output obtained using pi-load.

Tables 4.1 and 4.2 show the comparison of estimated value of gate delay with SPICE computed gate delay, for various values of resistance, inductance and capacitance. Table 4.1 shows estimated gate delay for fast input ramps (transition time of input taken

to be 0.1ns). Table 4.2 shows estimated gate delay for slow input ramps (transition time of input taken to be 1ns).

Table 4.1 Gate delay for fast input ramps using pi-load model and effective capacitance model

R(kΩ)	L(nH)	C(pF)	Effective Capacitance obtained(pF)	Gate delay with pi-load (ns)	Gate delay with effective capacitance load(ns)	Error%
2.9587	1.8196	3.1112	0.5530	0.1766	0.1733	1.86
2.3765	1.4557	2.4891	0.4490	0.1556	0.1542	0.89
1.7944	1.0918	1.8669	0.3443	0.1374	0.1354	1.45
1.2122	7.2784	1.2446	0.2365	0.1198	0.1156	3.5

Table 4.2 Gate delay for slow input ramps using pi-load model and effective capacitance model

R(kΩ)	L(nH)	C(pF)	Effective Capacitance obtained(pF)	Gate delay with pi-load (ns)	Gate delay with effective capacitance load(ns)	Error%
2.9587	1.8196	3.1112	0.5067	0.3107	0.2787	10.2
2.3765	1.4557	2.4891	0.41388	0.2887	0.2507	13.16
1.7944	1.0918	1.8669	0.33376	0.2687	0.2267	15.6
1.2122	7.2784	1.2446	0.30204	0.2533	0.2153	15.0
0.6301	3.6392	0.62238	0.31672	0.2403	0.2203	8.32

4.2.2 Calculation of interconnect delay

The near-end interconnect waveform V_d obtained in Section 4.2.1 is modelled by a ramp by fitting a straight line through the 20% and 80% points (see Fig.4.5). The interconnect delay is obtained by driving the RLC interconnect line by using this fitted ramp voltage.

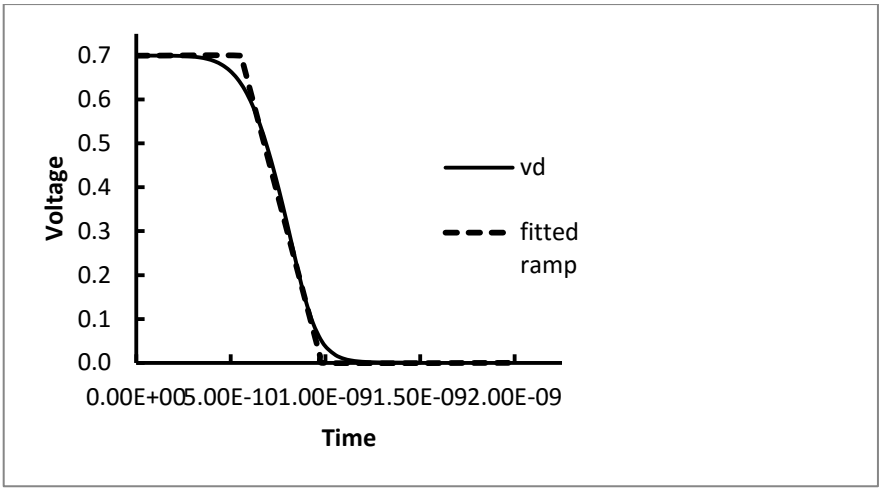

Fig.4.5 Fitting a ramp response to the gate output with effective capacitance as load.

The output waveform V_0 is obtained by numerical convolution of the approximated ramp voltage with the transfer function of the RLC distributed interconnect line [8]. The transfer function obtained using ABCD parameters is given as:

$$H(s) = \frac{1}{\left[\cosh(\theta h)+\frac{Z_S}{Z_0}\sinh(\theta h)\right]+\frac{1}{Z_r}[Z_0\sinh(\theta h)+Z_S\cosh(\theta h)\,]} \tag{4.30}$$

$$= \frac{1}{1+b_1 s+ b_2 s^2+ \ldots\ldots+ b_k s^k+ \ldots..}$$

$\theta = \sqrt{(r + sl)sc}$ is the propagation constant

$Z_0 = \sqrt{\frac{R+sL}{sC}}$ is the characteristic impedance

$r = \frac{R}{h}, l = \frac{L}{h}, c = \frac{C}{h}$ are resistance, inductance and capacitance per unit length respectively and h is the length of the interconnect.

The transfer function is approximated by considering only one pole.

$$\mathrm{H(s)} = \frac{1}{1+sb_1} \text{ where } b_1 = R_s C_l + R_s C + \frac{RC}{2} + RC_l \tag{4.31}$$

4.2.3 Overall logic stage delay

Now, as both the gate delay and the interconnect delay has been computed, the overall logic stage delay can be achieved by summing them up.

Table 4.3 presents 50% propagation delay (time from $\frac{V_{DD}}{2}$ point of V_{in} to $\frac{V_{DD}}{2}$ point of output V_o) values estimated from the proposed model and those computed by SPICE simulation. The delay is estimated for temperatures varying from 300K to 500K and lengths varying from 600μm to 1000μm. It is observed that the average error in the estimated delay as compared to SPICE computed delay is 7.9%.

Table 4.3 Propagation delay comparison using Spice simulation and using the proposed model.

Length (μm)	Temp (K)	R(kΩ)	L(nH)	C(pF)	Propagation delay(ns) with SPICE simulation	Propagation delay(ns) with proposed model	Error%
1000	300	2.9587	1.8196	3.1112	3.07	3.460	12.7
	350	3.1639	1.8196	3.1112	3.30	3.68	11.51
	400	4.5716	1.8196	3.1112	4.54	5.192	14.36
	450	6.5330	1.8196	3.1112	6.18	7.25	17.31
	500	9.0728	1.8196	3.1112	8.33	9.66	15.96
800	300	2.3765	1.4557	2.4891	2.09	2.292	9.66
	350	2.5407	1.4557	2.4891	2.24	2.432	8.57
	400	3.6669	1.4557	2.4891	3.0	3.4	13.33
	450	5.2360	1.4557	2.4891	4.03	4.751	17.89
	500	7.2678	1.4557	2.4891	5.49	6.474	17.92
600	300	1.7944	1.0918	1.8669	1.33	1.377	3.5
	350	1.9175	1.0918	1.8669	1.36	1.4546	6.95
	400	2.7621	1.0918	1.8669	1.80	1.992	10.66
	450	3.9389	1.0918	1.8669	2.42	2.7518	13.71
	500	5.4628	1.0918	1.8669	3.25	3.738	15.01
400	300	1.2122	0.72784	1.2446	0.7466	0.7292	-2.33
	350	1.2947	0.72784	1.2446	0.7706	0.7655	-0.66
	400	1.8582	0.72784	1.2446	0.9486	0.984	3.73
	450	2.6433	0.72784	1.2446	1.2086	1.325	9.63

	500	3.6601	0.72784	1.2446	1.5526	1.743	12.26
200	300	0.6301	0.36392	0.6224	0.3786	0.3542	-6.44
	350	0.67129	3.6392	0.6224	0.3826	0.3735	-2.37
	400	0.95303	3.6392	0.6224	0.4166	0.4015	-3.62
	450	1.3456	3.6392	0.6224	0.4666	0.4589	-1.65
	500	1.854	3.6392	0.6224	0.5426	0.5480	0.99

4.3 Thermally aware delay analysis of SWCNT bundle interconnect

With scaling down of technology, the operating temperature of the circuit is increasing. Variation in temperature can cause changes in the parameters of the circuit thus affecting its performance. Therefore, the analysis of thermal effects is of utmost importance.

The above proposed analytical model is employed to analyse the effect of temperature on delay of SWCNT bundle interconnect. The required temperature dependent parameters are calculated from model stated in Section 3.4. The output voltages obtained for the temperature varying from 300K to 500K are shown in Fig.4.6.

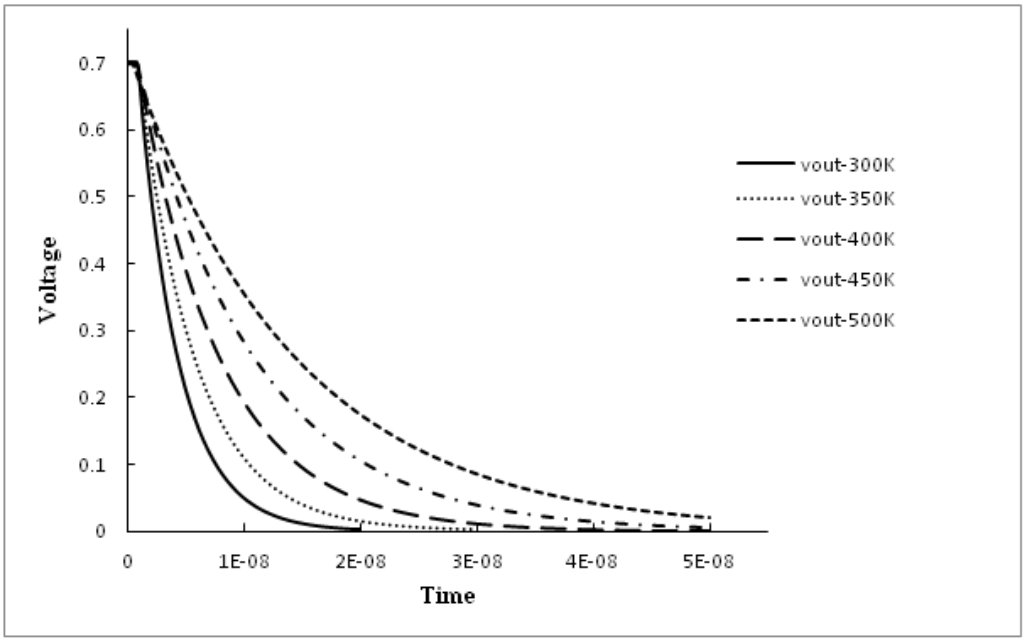

Fig.4.6. Comparison of output voltage waveforms at different temperatures.

The results suggest that with the increase in temperature, the delay increases. This is because the delay of a circuit is highly influenced by its resistance. With rise in temperature, the dominance of previously neglected optical phonon absorption leads to rise in low-bias resistance value, and hence rise in delay.

4.4 Conclusion

An analytical model for delay estimation of overall delay (gate delay as well as interconnect delay) of an RLC interconnect driven by CMOS inverter is presented. The gate delay computed using this model is compatible with k-factor equations, unlike the gate delay computed with Π-load. The transistor is represented by alpha power law model and all its regions of operation are considered. The average error in overall delay obtained is 7.9% of the delay obtained by SPICE simulations. Also, by using the proposed model, the overall delay and output waveform of SWCNT bundle at different temperatures (300K-500K) are obtained.

Chapter 5 Comparative Analysis between Interconnects of SWCNT Bundle and Copper

5.1 Introduction

As the technology continues to scale down, copper is faced with problem of increase in resistivity due to grain boundary effect and electromigration [43]. This poses a serious concern over the future use of copper as interconnect. Carbon nanotubes (CNTs), with their low resistivity and high current density, have emerged as strong contenders for use as interconnects in VLSI circuits [44]. As delay is one of the most important parameters for performance estimation of a VLSI circuit, the delay performances of copper interconnect and SWCNT bundle interconnect are compared in this chapter. The delay comparison is made at different lengths (200μm to 1000μm) and different temperatures (300K to 500K).

5.2 Delay Comparison of copper and SWCNT

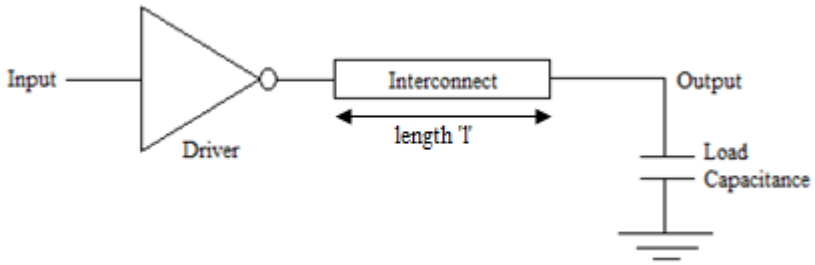

Fig.5.1. Interconnect being driven by an inverter and terminated by a load capacitance.

The circuit as shown in Fig.5.1 comprises of an Interconnect of length ‘l’ being driven by an inverter. The output is obtained across the load capacitance. Here the load capacitance represents the input capacitance of next stage. For performance estimation, the Interconnect is replaced by respective equivalent structures for copper interconnects

and SWCNT bundle interconnects, as shown in Fig.5.3 and Fig.5.4. The interconnect parameters are obtained based on the prediction of ITRS 2012, as presented in Table 3.1.

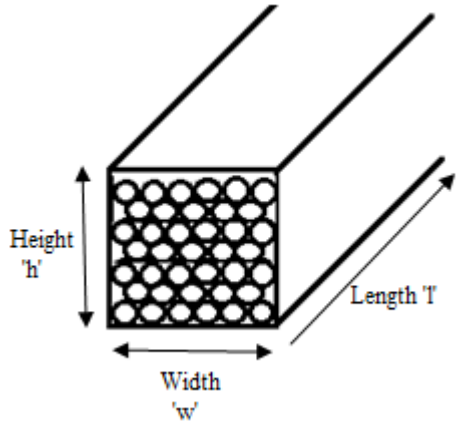

Fig. 5.2 Equivalent structure for SWCNT bundle interconnects.

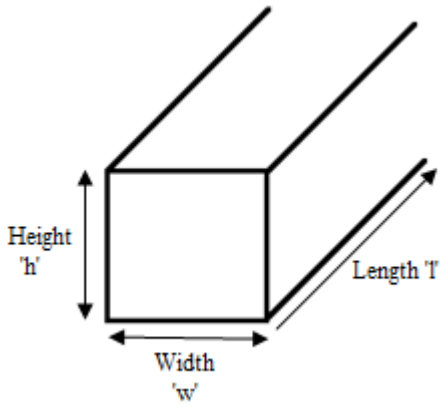

Fig. 5.3. Equivalent structure for copper interconnects.

The impedance parameters and delay models proposed in Chapters 3 and 4 respectively are employed for performance estimation of SWCNT interconnects and copper interconnects for 22nm technology node. The simulations are carried out for pulse input with frequency 0.1 Ghz. The load capacitance is taken to be 0.35pF. Optimum number of repeaters is used. The delay comparisons between SWCNT interconnects and copper interconnects are carried out at different levels (local, intermediate and global) and at different temperatures.

Table 5.1 shows the values of resistance of SWCNT bundle interconnects and copper interconnects, for interconnect length 1000μm at temperature 300K, estimated using both temperature dependent model and temperature independent model. It can be

observed that for SWCNT bundle, the value estimated using temperature dependent model is less than that obtained using temperature independent model.

Table 5.1 Resistance values for 1000μm long interconnect at T=300K.

Type of Interconnect	Resistance using temperature independent model (kΩ)	Resistance using temperature dependent model (kΩ)
Copper	26.673	26.673
SWCNT bundle	2.9587	2.2343

Table 5.2 shows that the average improvement in delay estimation of SWCNT bundle interconnect by thermally aware model over temperature independent model is 18.18%.The calculations are done at temperature 300K.

Table 5.2 Delay using temperature independent and temperature dependent model at different interconnect lengths.

Length of interconnect(μm)	Delay(ps) of SWCNT bundle in temperature independent model	Delay(ps) of SWCNT bundle in temperature dependent model	Percentage improvement (%)
1000	1255	1022.63	18.51
800	821.055	693.335	15.55
600	491.435	381.3	22.41
400	180.605	151.255	16.25
200	91.535	78.05	14.73

Fig.5.4 shows the variation of normalized delay with variation in temperature for both thermally aware and temperature independent model at 300K. It can be seen that the delay estimated by temperature independent model is more than that estimated by thermally aware model. This is because the resistance of SWCNT bundle modelled by thermally aware model is less.

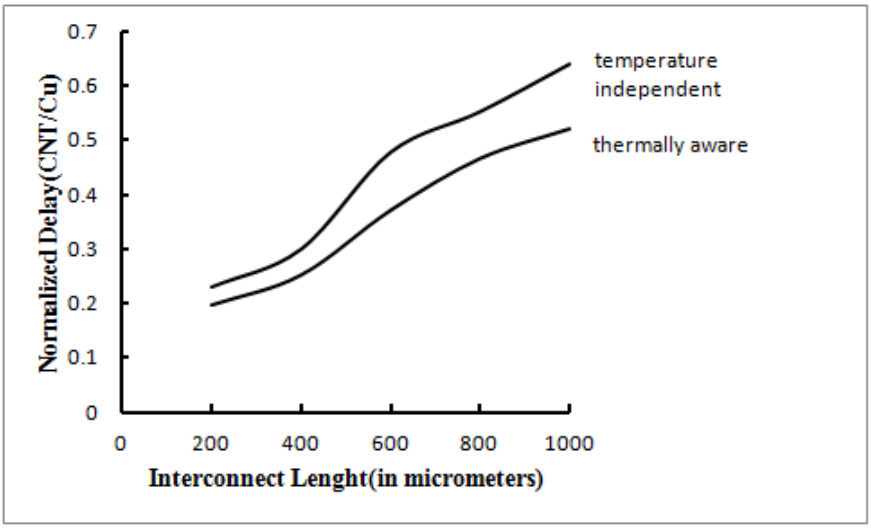

Fig.5.4 Normalized delay using temperature independent and temperature dependent models at different interconnect lengths.

Following are the tables (Table 5.3-5.7) depicting delays of SWCNT bundle and copper interconnects, at different lengths for temperature varying from 300K to 500K:

Table 5.3 Delay of SWCNT bundle and copper interconnects at temperature 300K

Length of interconnect(μm)	Delay of SWCNT bundle (ns)	Delay of Cu (ns)
1000	1.0226	1.96
800	0.6933	1.485
600	0.3813	1.0276
400	0.1512	0.6021
200	0.0367	0.1877

Table 5.4 Delay of SWCNT bundle and copper interconnects at temperature 350K

Length of interconnect(μm)	Delay of SWCNT(ns)	Delay of Cu(ns)
1000	1.33	2.395
800	0.8758	0.1805
600	0.5337	0.1245
400	0.2077	0.7663
200	0.0516	0.2448

Table 5.5 Delay of SWCNT bundle and copper interconnects at temperature 400K

Length of interconnect(μm)	Delay of SWCNT (ns)	Delay of Cu (ns)
1000	1.765	2.86
800	1.19	2.19
600	0.7253	1.56
400	0.2077	0.7663
200	0.0809	0.3182

Table 5.6 Delay of SWCNT bundle and copper interconnects at temperature 450K

Length of interconnect(μm)	Delay of SWCNT (ns)	Delay of Cu (ns)
1000	2.37	3.2
800	1.615	2.53
600	0.9703	1.79
400	0.4228	0.9305
200	0.1263	0.4079

Table 5.7 Delay of SWCNT bundle and copper interconnects at temperature 500K

Length of interconnect(μm)	Delay of SWCNT (ns)	Delay of Cu (ns)
1000	3.19	3.625
800	2.175	2.875
600	1.3	2.065
400	0.6203	1.315
200	0.20004	0.5229

After obtaining the individual delays of copper and SWCNT bundle interconnects, normalized delay (delay of SWCNT/delay of copper) for length varying from 200μm-1000μm, is computed and plotted with respect to the temperature.

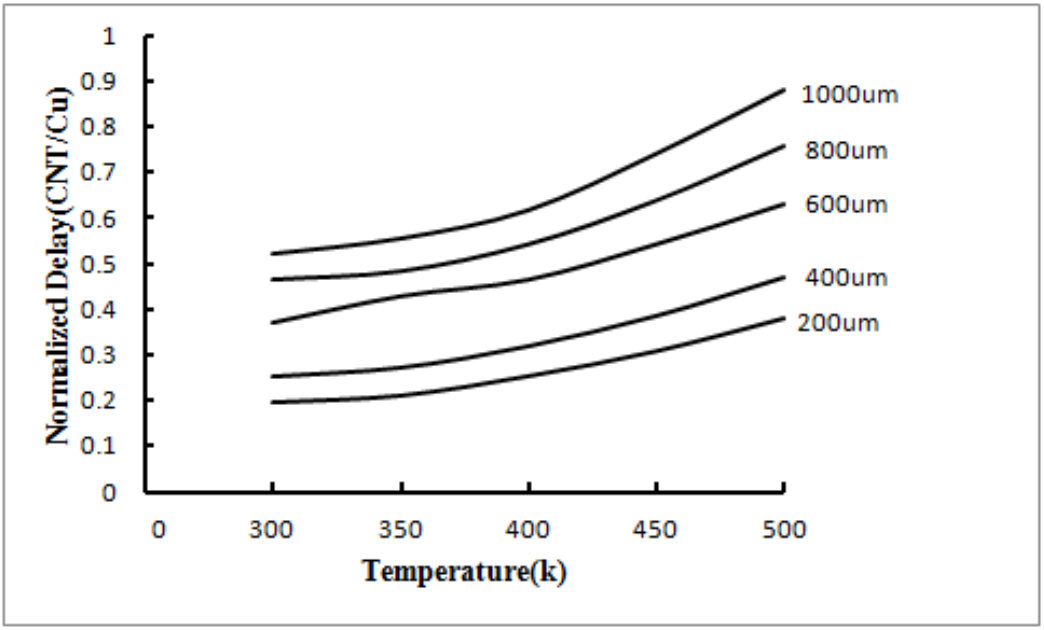

Fig. 5.5. Temperature dependent normalized delay (CNT/Cu) at different interconnect lengths.

The graph in Fig. 5.5 shows that the normalized delay increases with increase in temperature. Throughout, the delay offered by the SWCNT bundle interconnect is less than the delay offered by copper interconnects because of the low resistance of SWCNT bundle as compared to resistance value of copper. It is also observed that at any constant temperature, the delay increases with increase in the length of interconnect. It is due to the dependence of impedance parameters on the length of interconnect.

5.3 Conclusion

The resistance of SWCNT bundle obtained by thermally aware model is less than that obtained by temperature independent model. It is observed that delay obtained at different temperatures (300K to 500K) and interconnect lengths (200μm-1000μm) by SWCNT bundle interconnects is lower than the delay obtained by copper interconnects**.** It can be concluded that SWCNT bundle is a better interconnect than copper and thus can be considered as a potential future interconnect.

Chapter 6 Conclusion and Future Scope

6.1 Introduction

With progressive scaling of technology, the device dimensions are decreasing. Therefore the density of chip as well as deep submicron effects viz. surface roughness and grain boundary scattering are increasing. The longer wires leads to increase in the resistance of copper interconnect, thus limiting its performance. Thus there is an essential need to find appropriate replacement for copper interconnects. Carbon nanotube because of its remarkable mechanical strength and thermal stability are being researched upon on its applicability as a future VLSI interconnect.

6.2 Summary of Important Findings

The work done over the years on SWCNT interconnect bundle is discussed in brief in chapter 2. An overview of research done in modeling of circuit parameters of interconnect and estimation of interconnect delay is given.

6.2.1 Temperature- dependent circuit modeling of SWCNT bundle interconnect

Temperature dependent circuit modeling of both metallic SWCNT and copper is presented. The resistance of an individual SWCNT is quite high (nearly 6kΩ). Therefore, an SWCNT bundle is considered in the present analysis. To consider the effect of temperature on circuit parameters accurately, different type of scattering mechanisms are taken into account.

6.2.2 Temperature-dependent delay model for SWCNT bundle interconnect

An analytical temperature-dependent delay model for SWCNT bundle interconnect is proposed. The entire process to achieve the overall logic stage delay is composed of two parts; gate delay and interconnect delay. The gate delay and gate output waveform are obtained by approximating the driving point admittance at the output of the gate by an effective capacitance. The results are obtained for both slow and fast input ramps at different temperature, ranging from 300K to 500K. The SPICE simulation results, compared with analytically obtained results, show that the error is within permissible limits. The output at far end of interconnect is obtained by driving the distributed

interconnect with the gate output fitted into a finite ramp voltage. The overall delay, extracted from analytical approach for temperatures varying from 300K to 500K and lengths varying from 200μm to 1000μm, obtained is within 7.9% of the SPICE simulated delay.

6.2.3 Comparative Analysis between Interconnects of SWCNT Bundle and Copper

Comparison between delay performances of SWCNT bundles, extracted with and without using temperature-dependent circuit parameters is presented for temperature 300K. The thermally aware model gives 18.18% average improvement for interconnect lengths varying from 200μm to 1000μm. A comparative analysis of delay performance is carried out between conventionally used copper based interconnect and its potential successor, SWCNT bundle based interconnect for temperatures varying from 300K to 500K and lengths varying from 200μm to 1000μm. For the entire range of temperature as well as length, the delay obtained from SWCNT bundle interconnect, is less than that of copper counterpart. This is because of the high resistance offered by copper.

It can be concluded on the basis of aforementioned discussion that the carbon nanotubes are more reliable with respect to temperature as compared to copper. This is due to the fact that temperature-dependent resistance of carbon nanotubes is less sensitive to the temp-dependent scattering in deep-submicron technology nodes. Thus carbon nanotubes can suitably replace copper as VLSI interconnects.

6.3 Future Scope

An SWCNT bundle comprises of SWCNTs which can be either metallic or semiconducting in nature. For interconnect applications, fraction of metallic SWCNTs in the bundle desired is high. But due to lack of control on chirality, ensuring that all SWCNTs in a bundle are metallic becomes a difficult task. Therefore, improved fabrication techniques are required to predict the metallic or semiconducting nature of the bundle.

With increase in operating temperature of ICs, the thermal issues also need to be looked after. Though the temperature dependent delay analysis is being researched upon, but

no work has been done on temperature dependent crosstalk analysis. Therefore the temperature- dependent crosstalk needs to be analyses to predict the performance of a circuit at high temperatures.

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