APR Flow for High-Performance VLSI Blocks and Optimizing Design Metrics

Project report submitted in partial fulfilment of the requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

in VLSI DESIGN

Submitted By

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DECLARATION

I hereby declare that the Project report entitled "APR Flow for High-Performance VLSI Blocks and Optimizing Design Metrics" is in partial fulfilment of the requirement of the award of the degree of Master of Technology (VLSI Design) submitted at Electronics and Communication Engineering Department, Thapar Institute of Engineering & Technology (Deemed to be university), Patiala is a record of work carried out under supervision of Dr. Sudhanshu Tyagi (Assistant Professor, Electronics and Communication Engineering Department, Thapar Institute of Engineering & Technology), Dr. Jaswinder Kaur (Associate Professor, Electronics and Communication Engineering Department, Thapar Institute of Engineering & Technology) and Nagendra Singh Chandrakar (Engineering Manager, Intel Technology India Pvt. Ltd.) from June 2025 to June 2026. The matter in this has not been submitted in part to any other university or institute for the award of any other degree.

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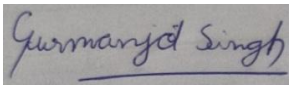

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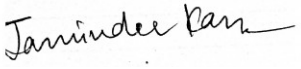

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The letter is to confirm the mentioned above has undergone internship at Intel Technology India Private Limited. We wish you all the best for your future assignments.

Yours Sincerely,
For Intel Technology India Pvt. Ltd.

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ABSTRACT

The efficiency of the physical design flow has become more and more important as integrated circuits grow into advanced technology nodes, making it harder to achieve optimal performance, power and area utilization commonly known as PPA. APR (Automatic Placement and Routing) directly impacts the design metrics like timing closure, congestion and manufacturability aspects which are the key components of this process. This paper provides a brief overview of the APR flow, requirement for optimizing the design metrics and the tools used for this process.

Standard APR flow begins with the floorplanning stage where the die area is partitioned into several blocks and macro placement is also defined in this stage only. Power grid is also defined in floorplanning stage. Then placement is done which arranges the standard cells to meet the timing requirements and multiple optimization stages are done to achieve the best QoR (Quality of Results). CTS (Clock Tree Synthesis) distributes the clock signal with minimal skew and latency. Routing stage connects all nets across metal layers to ensure proper communication between the components without any performance degradation. There are several tools available that are used in the industries that support APR to reduce the design flow complexity. This project involves the study of complete RTL (Register transfer level) to GDSII (Graphic Database System II) flow for a high performance VLSI (Very-Large-Scale Integration) block and also employing techniques to improve the design metrics to optimize the overall design. This study lays the groundwork for a robust and scalable physical design methodology that enhances performance while streamlining the APR flow for modern VLSI systems.

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LIST OF ABBREVIATIONS

PPA	Power, Performance, Area
APR	Automatic Placement and Routing
QoR	Quality of Results
CTS	Clock Tree Synthesis
RTL	Register transfer level
GDSII	Graphic Database System II
VLSI	Very-Large-Scale Integration
ASIC	Application Specific Integrated Circuit
DFT	Design for Test
STA	Static Timing Analysis
WNS	Worst Negative Slack
TNS	Total Negative Slack
PnR	Place and Route
DRC	Design Rule Check
LVS	Layout vs Schematic
ERC	Electrical Rule Check
GUI	Graphical User Interface
RTM	Runtime Manager
TCL	Tool Command Language
ECO	Engineering Change Order
LEC	Logical Equivalency Checks
PV	Physical Verification
FV	Formal Verification
RV	Reliability Verification
DEF	Design Exchange Format
PDN	Power Distribution Network
PVT	Process, Voltage, Temperature
SVT	Small Threshold Voltage

HVT	High Threshold Voltage
LVT	Low Threshold Voltage
ULVT	Ultra Low Threshold Voltage
NDR	Non-Default Rule
ESD	Electrostatic Discharge
DVFS	Dynamic Voltage and Frequency Scaling

CHAPTER 1
INTRODUCTION

Millions of transistors may be integrated onto a single semiconductor chip thanks to a method called VLSI. Its ability to make gadgets faster, smaller, and more power-efficient has completely changed the electronics industry. Modern digital systems are built on VLSI, which power everything from laptops and smartphones to industrial automation and vehicle electronics. Front-end design, which concentrates on logic and functionality, and back-end design, often referred to as physical design, which handles the chip's actual layout, are the two key areas of the VLSI design process. Physical design is essential because it converts a circuit's logical representation into a physical layout, guaranteeing that the chip satisfies specifications for area, power, and performance. Physical design is becoming more and more crucial to attaining the best results and guaranteeing a successful tape-out as technology nodes get smaller and designs get more intricate.

1.1 ASIC DESIGN FLOW

ASIC (Application specific integrated circuit) design flow is the process of making a chip from design specification stage to manufacturing of the chip. The process has multiple stages with each stage having its own significance and complications, see Fig. 1.1 which shows the different stages of ASIC Design flow. Some design metrics need to fulfilled at each stage of the design flow.

1. Starting from the specifications stage which describes the information which is required by the customer.
2. Then comes the architecture design stage in which high level block diagram is created. Here microarchitecture, memory hierarchy, and data paths are decided.
3. After that comes the RTL design which is the process of describing the logical functionality of a design by using any higher-level language like VHDL and Verilog.
4. Verification is done to ensure that RTL meets the specification
5. Then comes the synthesis part where the logical description is converted into a gate level netlist using different tools

6. DFT (Design for Test) inserts scan chains and other test structures and ensures the design is testable after fabrication.
7. Then there is Physical design stage which basically implements the logical design physically. This stage which includes:
    - Partitioning - It includes breaking up a circuit into smaller sub-circuits or modules which can each be designed or analyzed individually.
    - Floor planning - It involves determining the shapes and arrangement of sub-circuits or modules, as well as the locations of external ports and IP or macro-blocks. Power planning is also done in this stage where power (VDD) and ground (GND) nets are distributed throughout the chip.
    - Placement - It places the cells on their defined locations in a block.
    - CTS - It determines the buffering, gating and routing of the clock signal to meet prescribed skew and delay requirements.
    - Routing- In this stage the connectivity between all the components is done to ensure proper communication.
8. STA (Static timing analysis) analyzes the timing paths to ensure the design meets timing requirements.
9. Signoff stage does the final checks like timing, power, signal integrity and design rule checks and GDSII format is prepared for fabrication.
10. At last, the design is sent to foundry for manufacturing in the fabrication process.

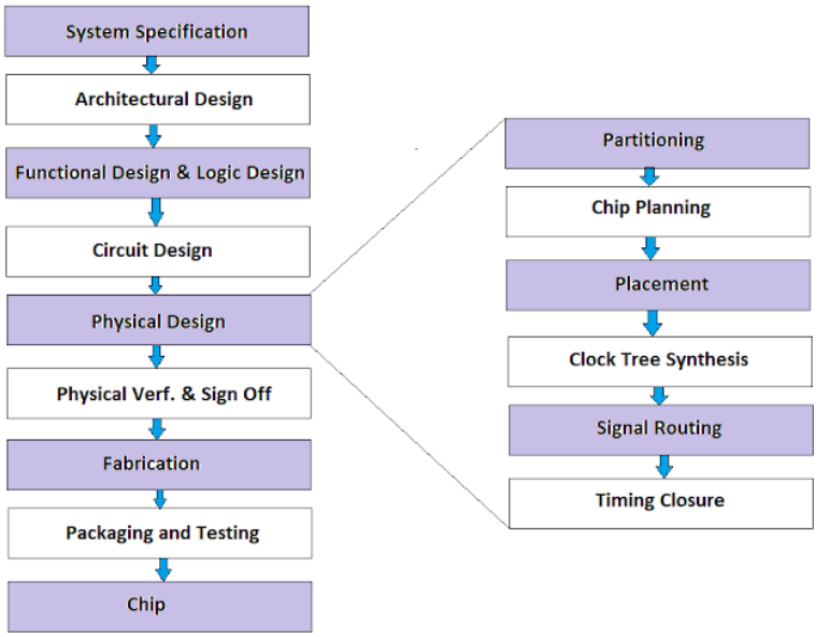

Fig. 1.1: ASIC Design Flow with expanded stages of Physical Design [32]

1.2 APR (AUTOMATIC PLACEMENT AND ROUTING)

APR is a very critical stage in the development of ASIC which involves the converting of synthesized netlist (logical representation) into a physical layout (GDSII) that can be manufactured on silicon. In order to satisfy time, power, and space requirements, standard cells and macros must be positioned carefully inside the chip design, and the connections must be routed across several metal layers. Floorplanning, power planning, placement, CTS, routing, and physical verification are some of the steps that are commonly included in the APR flow. WNS (Worst Negative Slack), TNS (Total Negative Slack), congestion, IR drop, and overall QoR are important design indicators that are directly impacted by each stage. Effective APR is crucial for effective tape-out in advanced technology nodes because it guarantees that the design satisfies performance goals while reducing power consumption and optimizing silicon utilization.

1.2.1 Design Metrics

Different design metrics should be kept in mind while doing PnR (Place and Route) are-

1. Timing - Setup and hold violations should be minimum and ensuring signals reach in the required timing windows. Skew and jitter should be minimum.
2. Power - At lower technology nodes, power dissipation becomes critical so ensuring very less power dissipation (shown in Fig. 1.2) using gating techniques becomes very critical.
3. Area - Cell Density should be balanced to avoid congestion and ensure routability. The chip area should be utilized properly to ensure efficiency.
4. Signal Integrity - Crosstalk should be minimized by spacing critical nets and shielding.
5. Manufacturability - Different checks like DRC (Design Rule Check), LVS (Layout vs Schematic) needs to be done to ensure that the design complies with the foundry rules. Effects like antenna effect and ERC (Electrical Rule Check) also needs to be verified.
6. Routing Quality - Routing should be done in a way that it doesn't degrade the timing and other metrics like shorts, opens in the net. Wire congestion should also be minimum.

PnR can be done by using any design tool provided by Synopsys, Cadence, Mentor graphics etc. The tool itself takes care for optimizing these design metrics but many times due to the complexity of the design the tool degrades some of the metrics. So, we have to take care of those metrics manually.

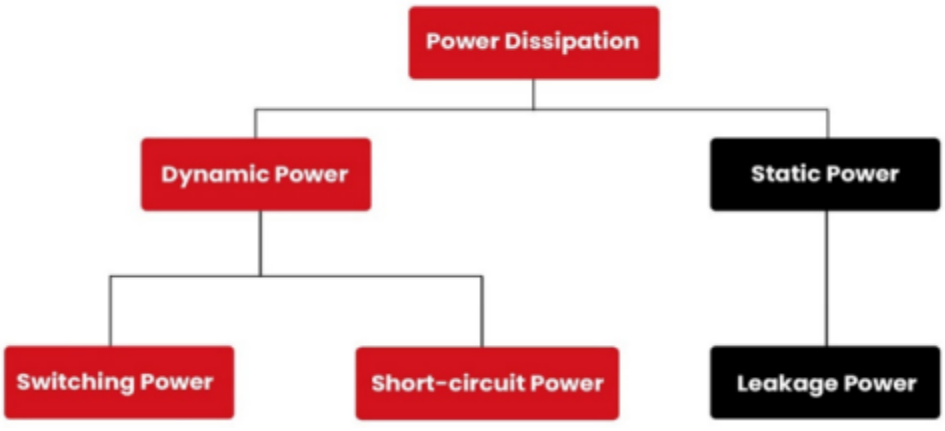

Fig. 1.2: Power Dissipation [1]

1.3 TOOLS AND TECHNOLOGIES

In PnR stage of physical design, several industry-standard tools are used to automate and optimize the layout of digital circuits. Popular tools include Synopsys Fusion Compiler, Cadence Innovus, and Siemens Olympus-SoC, each offering advanced capabilities for placement, routing, timing closure, and power optimization.

1.3.1 Synopsys Fusion Compiler

Synopsys Fusion Compiler is an advanced tool used to develop integrated circuits by converting hardware language, such as Verilog designs into physical layouts. It combines several stages of the physical design flow including synthesis, placement, clock tree synthesis, routing, and optimization within a single environment. This approach reduces the need for multiple design tools which streamlines the work flow and improves overall design efficiency. It is widely used for developing complex semiconductor devices including processors, AI accelerators and other high performance systems. It also supports advanced technology nodes like 5 nm and smaller nodes. These capabilities allow design teams to accelerate project completion while consistently achieving high-performance and power-efficient chip implementations.

1.3.2 Synopsys Lynx Design System

Lynx is a chip design management platform that helps engineers organize and run complex design flows more easily. By combining several tools and processes, such as synthesis, place and route, and verification, into a single automated and standardized environment, it functions as a control center. Managing big teams working on the same chip, tracking progress, and troubleshooting problems are all made simpler using Lynx. Despite having a strong foundation in RTL to GDSII flow automation, Lynx's tool-agnostic framework allows for the construction of any flow process. Examples of industry usage models include tool regression flows, circuit modeling, cell characterization, and RTL verification. The top-level GUI (Graphical User Interface) portal for environment setting, block management, and subsystems such as the Execution Monitor, Flow Editor, and QoR viewer is called RTM (Runtime Manager).

1.3.3 Scripting Language

Tcl (Tool Command Language) is a simple scripting language used in chip design tools like those from Synopsys. It enables engineers with task automation, controlling tool behavior, and customizing different stages of design flow. Instead of performing operations manually through interface, designers can use tcl scripts to configure tool settings and perform all the tasks in an efficient manner. In Physical Design, tcl plays an important role in automating processes like running design implementations, generating reports and modifying design constraints. Its integration with design tools simplifies design workflows, reduces manual effort, and improves productivity, making tcl an essential scripting language for modern VLSI design environments.

1.4 POST ROUTE EXIT STAGE

ECOs (Engineering Change Orders) are targeted modifications into a VLSI designs after stages such as synthesis, placement and routing. These changes help designers to resolve issues without repeating the design flow which makes ECOs an efficient solution during later stages of chip development. ECOs can be classified into several categories based on their purpose. Functional ECOs are used to correct logic related errors. Timing ECOs address setup and hold time violations to meet timing requirements. Power ECOs focus on lowering power consumption through design optimizations. Metal ECOs does modifications only in the upper metal layers. Post-silicon ECOs are implemented after chip fabrication to resolve critical issues that are identified during silicon validation or testing.

The ECO process begins by identifying design issues through verification or testing. Once the issue is analyzed, the required modifications are done to the gate level netlist. After these changes, LEC (Logical equivalency checks) is performed to verify that the updated design remains functionally correct according to the specifications. After this the new netlist is integrated back into the design and routing is updated to accommodate the changes. The design then undergoes a series of final verification steps including functional simulation, STA, and physical verification checks such as DRC and LVS.

This chapter covered the fundamentals of VLSI design as well as the importance of physical design in modern integrated circuits. The whole ASIC design process from design specification to fabrication as well as the function of APR in attaining the best possible PPA were covered. Important design parameters were described, including manufacturability, time, power, area, and signal integrity. There was also a summary of industry-standard technologies and tools used in physical design, such as Tcl scripting, Lynx Design System, and Synopsys Fusion Compiler.

CHAPTER 2
LITERATURE REVIEW

The paper titled “Physical Design: Methodologies and Developments”[1] by Abhay Chopde and Atharva M. Kulkarni provides a detailed look at the physical design process in VLSI, from RTL synthesis to final tape-out. The paper shows how continuous technology scaling have made Power, Performance and Area optimization significantly more challenging, creating the need for well-defined design methodologies supported by advanced tools. It reviews earlier work on device-level innovations, including CNTFET technology, traces the evolution of ASIC, FPGA and CPLD architectures and discusses the growing role of AI-based techniques in design automation. The paper also provides a detailed overview of the physical design flow covering floorplanning, power planning, placement, CTS, routing and timing closure while examining optimization approaches such as simulated annealing, genetic algorithms and particle swarm optimization.

The paper “Analysis, Physical Design and Power Optimization of Design Block at Lower Technology Node” [2] by Ganesh Prasad J, Sudha R. Karbari, Sajeesh Ammikkallingal and Sukanya Kamath Bellal shows the challenges of physical design and power optimization in advanced technology nodes, with focus on leakage power reduction, area utilization and timing closure within ASIC design flows. The authors adopt a top-down design methodology and evaluate three floorplanning strategies (Run1, Run2, and Run3) for high frequency design block, comparing their impact on utilization, cell density, routing congestion and leakage power.

The work “Best Practices for Floorplanning and Placement to Meet Timing Closure in mm-Scale SoC Designs” [3] by Ayodele Marvellous, Dario Garcia-Gasulla, Ian Walsh and Konstantinos Kotsis focus on effective floorplanning and placement strategies for mm-scale System on Chip designs. The authors discuss design practices that improve the chances of achieving timing closure while maintaining balance between PPA requirements. It emphasizes that physical design is iterative rather than linear, with early decisions about macro placement, aspect ratio, and power grid planning having a significant impact on subsequent stages. The paper examines timing-driven

placement methods - net-based and path-based guided by Static Timing Analysis metrics such as Worst Negative Slack and Total Negative Slack, emphasizing the importance of CTS and post-route optimization in resolving setup and hold violations.

Susie Maestre, Aileen Gumera, Jefferson Hora and Melvin Joey de Guzman described iSpatial physical restructuring as a method for enhancing performance, power, and area in digital IC design by bridging the gap between synthesis and physical design in their paper “Improving Digital Design PPA using iSpatial Physical Restructuring” [4]. Traditional synthesis lacks correct placement and routing data, and physical design has a limited optimization scope. The iSpatial flow (see Fig. 2.1) combines synthesis, placement, and routing engines to allow physically aware reorganization of important pathways after placement without returning to RTL.

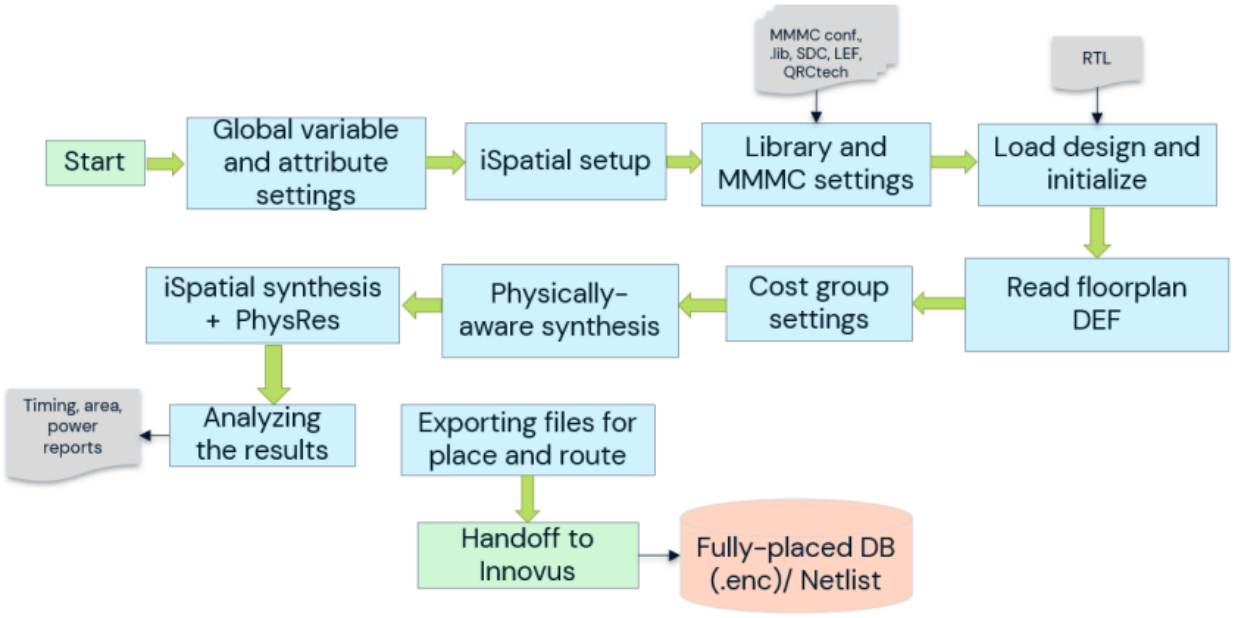

Fig. 2.1: The iSpatial Synthesis flow [4]

A physical-aware design methodology for analog and mixed-signal integrated circuits is proposed in the paper “Physical Aware Design Methodology for Analog & Mixed Signal Integrated Circuits” [5] by Haitham M. Eissa and Abd ElRahman ElMously to address layout-dependent effects like stress and well proximity, which have a significant impact on device performance at

deep submicron nodes. Traditional flows rely on trial and error and costly post-layout simulations, whereas the new method combines physical verification tools (Calibre LVS/DRC/DFM) with electrical models to forecast performance alterations early in the layout stage.

The evolution of placement in VLSI physical design and how it might be accelerated without sacrificing quality are examined in the study "Progress of Placement Optimization for Accelerating VLSI Physical Design" [6] by Yihang Qiu, Yan Xing, Xin Zheng, Peng Gao, Shuting Cai and Xiaoming Xiong. The paper reviews conventional placement techniques, including partitioning, heuristic based methods and analytical approaches such as quadratic and nonlinear placement. It also explains the limitations of these methods at advanced technology nodes where increasing design complexity, routing congestion, timing constraints and scalability challenges make conventional optimization techniques less effective (see Fig. 2.2).

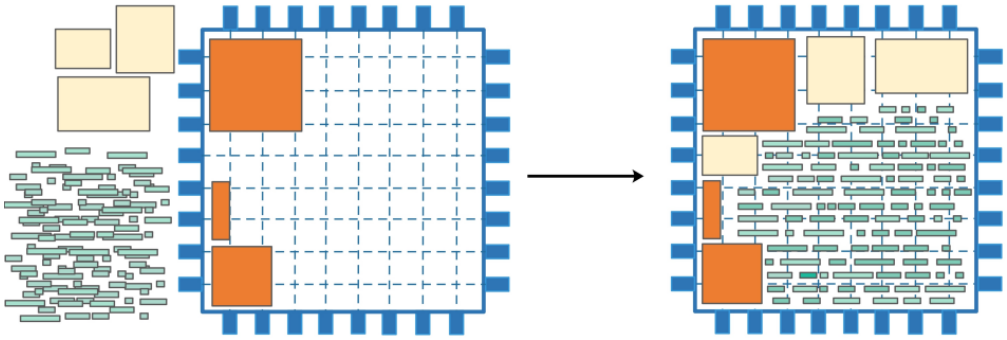

Fig. 2.2: Before and After cell placement [6]

The paper "A Framework for Block-Level Physical Design using ICC2 in 14nm Technology" [7] by M. Ishwarya Niranjana, J. Dhanasekar, N. Blesson and G. Daniel Immansingh presents a comprehensive block level physical design methodology implemented using Synopsys ICC2 for 14nm technology. The proposed flow covers floorplanning, power planning, global placement, legalization, CTS, routing, STA and sign-off verification for a design containing approximately 48k-65k standard cells across nine metal layers. The authors report a considerable reduction in timing violations after the CTS and routing stages. The overall flow demonstrates a manufacturable GDS implementation that achieves timing closure while satisfying DRC and LVS requirements.

In the paper “An Academic Framework for IC Physical Design Algorithms Development” [8] Dmitry Bulakh, Andrey Korshunov and Anton Datsuk introduce PDLab, a modular framework with a graphical user interface designed to support the development and evaluation of integrated circuit physical design algorithms. The framework integrates layout information from standard formats such as GDSII and LEF/DEF into a unified database, enabling efficient data management and layout processing. It also provides built-in support for common I/O operations and layout editing while allowing users to create executable design flows by combining functional modules.

Multi-bit flip-flops and multi-bit banking are examined as efficient ways to reduce flip-flop and clock-tree power at advanced nodes in the paper “Power Reduction in Advanced Technology Nodes Using Multi-Bit Flip-Flops and Banking Techniques in Physical Design” [9] by Selva Lakshman Murali. The author's post-layout simulations at 7nm and 5nm demonstrate that MBFFs reduce dynamic switching and clock burden. Additionally, integrating MBFFs with banking of adjacent registers reduces clock distribution complexity.

The paper titled “Research on Methods for Very Large Scale Integration Track Assignment Routing”[10] by Hui Yu, Shipeng Huang and Lu Ren enhances track-assignment routing by using single-axis Steiner backbones to extract local-net routability so that global routing better matches detailed routing, secondly modeling track assignment as an LSAP and using a CVAE-based generative neural network (H-CVAE) to generate high-quality assignment matrices rapidly and lastly using a tear-and-reassign refinement based on negotiation that trades a slight increase in wire length for a significant decrease in overlap-cost. Table 2.1 describes the comparison of Literature review done so far.

Table 2.1: Summary of Literature Review from [1] to [10]

Title of Paper	**Main Focus**	**Key Contribution**	**Research Gap**
Physical Design: Methodologies and Developments	Complete VLSI physical design flow	Discussed RTL-to-tapeout flow, optimization techniques, and AI-driven design automation.	Further research required on advanced-node automation and optimization.

Analysis, Physical Design and Power Optimization of Design Block at Lower Technology Node	Physical design and power optimization	Compared floorplanning methodologies for leakage power, congestion, and timing improvement.	Limited exploration of emerging technology nodes.
Best practices for floorplanning and placement to meet timing closure in mm-scale SoC designs	Floorplanning and timing closure	Presented timing-driven floorplanning and placement methodologies for large SoCs.	Additional work required for AI-assisted timing closure.
Improving Digital Design PPA using iSpatial Physical Restructuring	Physically-aware synthesis optimization	Improved PPA by integrating synthesis, placement, and routing information.	Scalability for highly complex designs requires further study.
Physical Aware Design Methodology for Analog & Mixed Signal Integrated Circuits	Analog and mixed-signal physical design	Introduced physically-aware methodologies for AMS circuits.	Requires adaptation to modern process nodes and mixed-signal SoCs.
Progress of Placement Optimization for Accelerating VLSI Physical Design	Placement optimization techniques	Reviewed modern placement algorithms and acceleration methods.	More focus needed on ML-driven placement solutions.
A Framework for Block-Level Physical Design	Block-level physical design flow	Demonstrated practical implementation using Synopsys ICC2.	Limited validation across multiple technology nodes.

using ICC2 in 14nm Technology			
An Academic Framework for IC Physical Design Algorithms Development	Physical design algorithm framework	Developed PDLab platform for testing and developing physical design algorithms.	Requires integration with industrial EDA flows.
Power Reduction in Advanced Technology Nodes Using Multi-Bit Flip-Flops and Banking Techniques in Physical Design	Clock power reduction	Reduced clock-tree power using MBFF and banking techniques.	Further optimization required for large-scale industrial designs.
Research on Methods for Very Large Scale Integration Track Assignment Routing	Routing optimization	Improved track assignment using neural-network-assisted optimization.	Needs evaluation on advanced technology nodes.

Joyce Ng Ting Ming, Ab Al-Hadi Ab Rahman and Nuzhat Khan's paper, “Wirelength estimation for VLSI cell placement using hybrid statistical learning” [11], introduces Hybrid-LRWL , a useful wirelength estimator that combines a statistical correction (learned regression) applied to HPWL for high-degree nets with accurate RSMT for low-degree nets. Tested on ISPD-2011 Superblue benchmarks, the hybrid technique significantly outperforms basic HPWL and RMST in accuracy while cutting runtime compared to complete RSMT by roughly 3.6 times and closely matching RSMT accuracy (mean error = 0.05%).

The W-shaped multilevel routing methodology, which combines congestion-aware global and detailed routing phases to enhance traditional V-shaped routing flows, is presented in the paper "Congestion-Driven Multilevel Full-Chip Routing Framework" [12] by Yao Hailong, Cai Yici and Hong Xianlong. In contrast to earlier frameworks like MARS and MR, WMR uses FLUTE-based Steiner tree decomposition and probabilistic congestion prediction to inform routing choices and enhance net distribution. Better handling of short nets, less local congestion, and higher routing completion rates are all made possible by the dual V-shaped flow, which consists of iterative coarsening and refining.

The paper "A Review on VLSI Floorplanning Optimization using Metaheuristic Algorithms" [13] by Rajendra Bahadur Singh, Anurag Singh Baghel and Ayush Agarwal presents a detailed overview of VLSI floorplanning methodologies with particular focus on the application of metaheuristic techniques for optimizing interconnect wirelength and chip area. The study discusses different floorplan representation and analyzes their influence on search space complexity and computational effort. The authors highlight the efficacy of several optimization methods on various benchmark circuits by comparing them, such as Genetic Algorithm, Simulated Annealing, Particle Swarm Optimization, and Ant Colony Optimization.

To address the drawbacks of conventional abstraction-based optimization in large, macro-dominated SoC designs, R. Venkatraman et al paper, "Optimization Quality Assessment in Large, Complex SoC Designs – Challenges and Solutions" [14] suggests a set of practical, design-conscious evaluation criteria. The authors point out that localized QoR problems are frequently concealed by traditional cost functions, particularly in routing, repeater synthesis, and placement. They introduce metrics including wirelength deviation tracking throughout routing stages, repeater tree topology validation, over-buffering analysis, and minimum-containing-rectangle based placement checks.

Einar J. Aas provides a standard framework for determining and assessing the efficacy and caliber of digital circuit design in his paper "Design Quality and Design Efficiency; Definitions, Metrics and Relevant Design Experience" [15] The likelihood that a finished design will meet its

requirements is used to model design quality, which is directly analogous to manufacturing yield and defect coverage. A holistic perspective of the design and test processes is made possible by the author's introduction of atomic design operations and verification coverage as fundamental components for calculating quality metrics.

Zhou et al. provide Active-Logic Reduction Technology in "A method to speed up VLSI hierarchical physical design in floorplanning" [16] in order to expedite hierarchical floorplanning in large-scale VLSI designs. Their technique uses simplified models and flex fillers to simplify netlists by up to 90%. This greatly reduces runtime and memory consumption without sacrificing timeliness or congestion quality. ART is a workable method for early timing closure and predictable design convergence in complicated hierarchical flows, as demonstrated by experimental findings that yield a 6.2× speedup and 2.8× memory reduction. Fig. 2.3 shows the Diagram of ART technology.

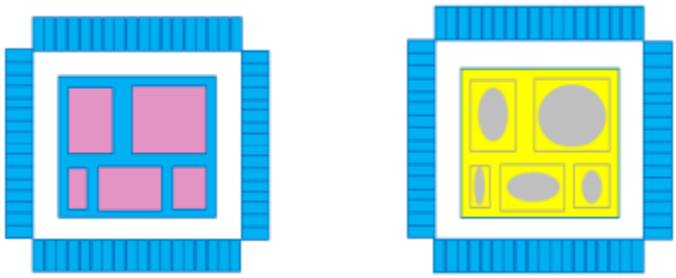

Fig. 2.3: Diagram of ART technology [16]

Jenila and Naidu examine machine learning and deep learning methods for placement and routing optimization in "A Survey on Learning-Based PnR Optimization for VLSI Physical Design Automation" [17]. In addition to comparing benchmarks and datasets, the study arranges techniques according to goals including wirelength, congestion, time, and power. While pointing up issues including scalability, data scarcity, and cross-node generalization, it also emphasizes the achievements of reinforcement learning and graph neural networks.

Dargar et al. use ICC2 tools to analyze placement methods for 40nm designs in "Analysis of Block Level PnR Flow to Increase the Cell Density in Less Congested Regions" [18]. To balance density,

they suggest redistributing cells into sparse areas by placing partial placement obstructions in crowded places. This paper demonstrates a practical approach for optimizing block-level PnR flow by mitigating congestion and improving timing performance as well as area utilization.

In “Challenges and Solutions in Modern VLSI Placement” [19], Jiang et al. discuss contemporary challenges in placement for large scale VLSI designs. The study presents analytical techniques such as dynamic step size conjugate gradient optimization, multilevel placement frameworks with NTUplace3 used as a case study for evaluation. Fig. 2.4 shows a resulting placement of the circuit newblue7. Although the paper identifies future needs in macro placement, routability-aware optimization and tighter integration of timing and power constraints, the reported results show improvements in wirelength reduction and overall density management.

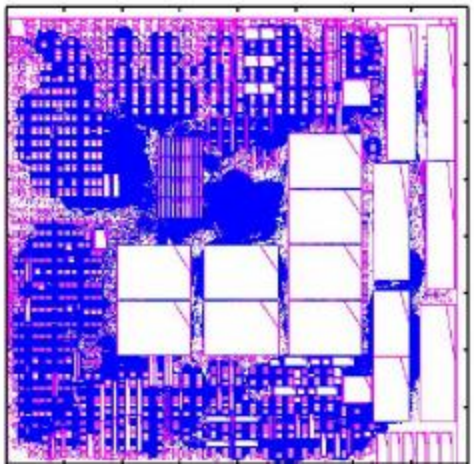

Fig. 2.4: A resulting placement of the circuit newblue7 [19]

In “Design and Optimization of Power, Area, and Delay in a 4-Bit SIPO Shift Register Using 90 nm CMOS Technology” [20], Uddin Forkan et al. present a compact CMOS based design focusing on power, area and delay optimization. The shift register is implemented using Cadence-based D flip-flops and NAND gate structures, achieving a power consumption of 0.45 mW, a silicon area of 110 × 75 μm^2 and a propagation delay of 0.65 ns. The results demonstrate improvements of approximately 18% in power, 16% in area and 8% in delay compared to earlier 90 nm implementations, making the design suitable for low-power and energy-efficient VLSI applications. Table 2.2 shows the comparison of literature review from [11] to [21].

Table 2.2: Summary of Literature Review from [11] to [21]

Title of Paper	Main Focus	Key Contribution	Research Gap
Wirelength Estimation for VLSI Cell Placement Using Hybrid Statistical Learning	Wirelength estimation	Proposed Hybrid-LRWL model with improved accuracy and runtime.	Requires testing on larger benchmark circuits.
Congestion-Driven Multilevel Full-Chip Routing Framework	Congestion-aware routing	Proposed W-shaped multilevel routing methodology.	Further optimization needed for highly congested designs.
A Review on VLSI Floorplanning Optimization Using Metaheuristic Algorithms	Floorplanning optimization	Compared GA, SA, PSO, and ACO-based floorplanning methods.	Limited analysis of AI-based optimization approaches.
Optimization Quality Assessment in Large, Complex SoC Designs – Challenges and Solutions	QoR assessment	Introduced advanced QoR evaluation metrics for large SoCs.	Additional validation on next-generation SoC architectures required.
Design Quality Measurement Using Verification Coverage and Relevant Design Experience	Design quality and verification metrics	Introduced quality metrics based on verification coverage and design operations.	Needs validation on larger industrial designs and advanced nodes.
A Method to Speed Up VLSI Hierarchical Physical Design in Floorplanning	Hierarchical floorplanning optimization	Proposed Active-Logic Reduction Technology achieving significant runtime and memory reduction.	Further evaluation required for complex heterogeneous SoCs.
A Survey on Learning-Based PnR Optimization for	ML/DL-based placement and	Reviewed reinforcement learning and graph	Dataset scarcity, scalability, and cross-

VLSI Physical Design Automation	routing optimization	neural network approaches for physical design.	node generalization remain challenges.
Analysis of Block Level PnR Flow to Increase the Cell Density in Less Congested Regions	Congestion-aware placement optimization	Improved timing and congestion through partial placement obstructions.	Validation needed on larger and more complex designs.
Challenges and Solutions in Modern VLSI Placement	Modern placement methodologies	Presented analytical placement techniques for wirelength and density optimization.	Additional work needed for timing and power-aware placement.
Design and Optimization of Power, Area, and Delay in a 4-Bit SIPO Shift Register Using 90nm CMOS Technology	Low-power sequential circuit design	Achieved reductions in power, area, and delay through CMOS optimization.	Limited to small-scale circuit implementation.
Efficient Synchronous FIFO Design: A Structured Approach Using ASIC Methodology	ASIC implementation of FIFO	Improved area, power, and timing through clock gating and optimized floorplanning.	Requires exploration for higher-speed applications.

In “Efficient Synchronous FIFO Design: A Structured Approach using ASIC Methodology” [21] Jenila et al. present a complete ASIC based flow for synchronous FIFO buffers, covering RTL development, synthesis, placement, routing and verification stages. The proposed design emphasizes efficient floorplanning to improve area utilization along with clock gating techniques to reduce dynamic power consumption. Implemented in 32 nm technology, the FIFO (see Fig. 2.5) demonstrates significant improvements over conventional approaches including approximately 30% reduction in area, 15% lower power consumption and improved timing slack, making it suitable for large scale ASIC integration.

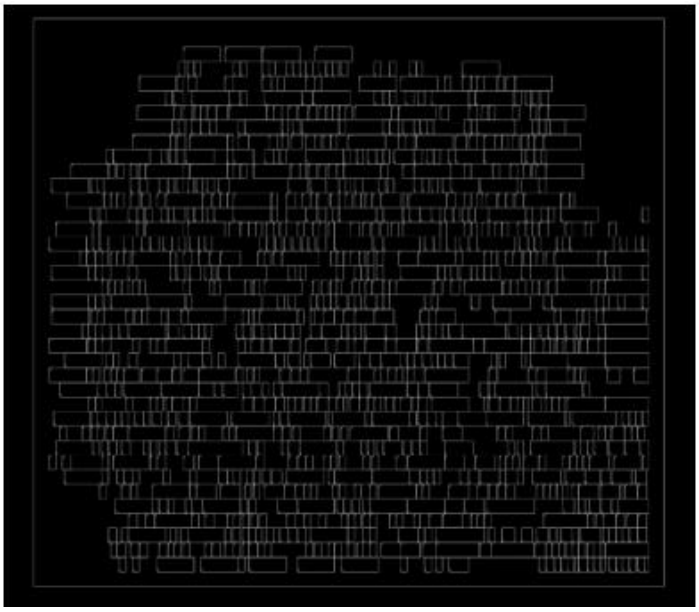

Fig. 2.5: Final Cell Placement of the Proposed FIFO Design [21]

In “Graph for VLSI Physical Design: An Extended Methodology to Explore Design Data and Boost Design Optimization” [22], Zhang et al. shows the application of graph theory in physical design by representing netlists and timing information as multi-level graph structures. The authors employ graph-based algorithms to identify high fanout registers, locate timing bottlenecks and guide design planning. Through case studies, the work demonstrates that graph-driven analysis offers a scalable approach to post-Moore design challenges by revealing hidden optimization opportunities and improving collaboration between digital and physical design teams.

In “IC Design Challenges and Opportunities for Advanced Process Technology” [23], Lee discusses the impact of advanced technology nodes on integrated circuit design. The paper highlights several lithography-related challenges, including mask coloring issues and RC variability. A key focus of the work is on design and process co-optimization, which requires close collaboration between designers, EDA tool developers and foundries. The study also identifies opportunities in areas such as color aware PnR, early stage parasitic estimation and reliability modeling to ensure robust and manufacturable designs at advanced process nodes.

A block-level place-and-route methodology optimized for 40nm designs is proposed by Kadarkarai et al. in "Implementation of a PnR Flow at Block Level to Achieve the High Utilization Rate" [24]. Using ICC2 tools, the flow incorporates enhanced CTS, optimum placement, hierarchical floorplanning, and congestion-aware routing. The method meets IR-drop and power constraints while achieving high silicon utilization when applied to a design with 34 macros and 38k cells. Results demonstrate better timeliness, decreased congestion, and efficient space utilization, proving the success of the personalized PnR strategy. Fig. 2.6 shows the placement of Standard cells as described in this work.

Fig. 2.6: Placement of Standard Cells [24]

Aravinth et al. provide a dynamic routing-based interconnection design that uses cutting-edge materials to reduce parasitic capacitance and inductance in "Novel Architecture for High-performance VLSI Interconnections: Reducing Latency and Power Consumption" [25]. When compared to traditional interconnects, the design provides average latency reductions of 28%, power savings of 22%, and throughput gains of 25%. The design provides a workable solution to bottlenecks in conventional VLSI interconnections and is appropriate for high-performance computing due to improved heat management and scalability.

Gundrathi et al. present an integrated approach to improve timing closure and physical DRC efficiency in ASIC flows in "Optimizing Timing and Physical DRC Performance in VLSI Design: A Comprehensive Approach" [26]. The method uses iterative ECO methods and sophisticated

optimization algorithms to speed up verification without sacrificing accuracy. When applied to a block-level design, the technique methodically tackles about 20K physical DRC violations and fixes setup and hold violations by cell resizing and buffer insertion. Results provide a strong foundation for dependable and effective VLSI design sign-off, with notable improvements in timing slack, clean closure after iterations, and decreased verification overhead.

Rangeetha et al. describe the backend flow of a 32-bit LEON SPARC processor utilizing Cadence Innovus at 45nm in “Physical Design Implementation and Measurement of Timing Metrics of 32-Bit LEON SPARC Processor Used in Space Applications” [27]. Floorplanning, placement, CTS, routing, and verification are all included in the design, and time metrics are examined at each stage. Design closure is confirmed by the results, which demonstrate improved slack following routing. Scalable to 64-bit, the processor's 35k instances and 1200 I/O pins make it ideal for space and military systems.

Almeida et al. present an RL-based framework in “Routability-Driven Detailed Placement Using Reinforcement Learning” [28] to enhance routability during detailed placement. While an RL agent optimizes placement to lower violations, a DRV predictor finds hotspots. This reduces wirelength overhead by avoiding repetitive rip-up and reroute cycles. The technique has potential for sophisticated nodes, allowing locations that more successfully balance time and congestion.

Bautista and Nunez test SPARC v8 cores across various synthesis processes and technologies in “Synthesis Experiments and Performance Metrics for Evaluating the Quality of IP Blocks and Megacells” [29]. Wide variations in performance are found when the area, power, and frequency of more than 100 implementations are examined. Their methodical approach supports fair comparisons with full-custom flows and reproducible IP evaluation by highlighting the impact of microarchitectural decisions and synthesis granularity on design quality.

In “VLSI Design Course with Commercial EDA Tools to Meet Industry Demand - From Logic Synthesis to Physical Design” [30], Loh et al. propose a structured academic program that utilizes Synopsys Design Compiler and IC Compiler to train students in industry-relevant VLSI design flows. The course integrates practical examples such as a 16-bit MIPS processor to demonstrate key stages including RTL modeling, logic synthesis, placement, CTS and routing. The program aims to bridge the gap between academic learning and industry requirements by exposing students to commercial EDA tools.

Evans et al. modify VLSI floorplanning and partitioning for power electronics in “VLSI-Inspired Design Automation for Scalable Power Electronics Layout Optimization” [31]. Their solution optimizes for electrical and thermal metrics, interfaces with PowerSynth, and synthesizes module layouts from netlists. A synthetic 3L-ANPC inverter achieves a 68% decrease in footprint, and case studies demonstrate lower inductance and temperature when compared to manual configurations. The paper shows how converter design is accelerated by automation influenced by VLSI. Table 2.3 shows the summary of Literature Review from [22] to [31]

Table 2.3: Summary of Literature Review from [22] to [31]

Title of Paper	Main Focus	Key Contribution	Research Gap
Graph for VLSI Physical Design: An Extended Methodology to Explore Design Data and Boost Design Optimization	Graph-based physical design analysis	Utilized graph theory for timing bottleneck identification and design optimization.	Needs tighter integration with commercial EDA tools.
IC Design Challenges and Opportunities for Advanced Process Technology	Advanced-node physical design challenges	Discussed FinFET, lithography, reliability, and parasitic effects at advanced nodes.	Future research required for sub-5nm technologies.
Implementation of a PnR Flow at Block Level to Achieve the High Utilization Rate	Block-level place-and-route	Achieved improved utilization, timing,	Scalability to larger hierarchical designs remains open.

	methodology	and congestion management.	
Novel Architecture for High-Performance VLSI Interconnections: Reducing Latency and Power Consumption	High-performance interconnect design	Reduced latency and power consumption using advanced interconnection architecture.	Manufacturing feasibility and large-scale deployment need study.
Optimizing Timing and Physical DRC Performance in VLSI Design: A Comprehensive Approach	Timing closure and DRC optimization	Developed iterative ECO-based methodology for timing and DRC fixes.	Further automation and runtime reduction are required.
Physical Design Implementation and Measurement of Timing Metrics of 32-Bit LEON SPARC Processor Used in Space Applications	Processor physical design implementation	Demonstrated complete backend flow and timing closure analysis.	Extension to larger processor architectures is needed.
Routability-Driven Detailed Placement Using Reinforcement Learning	Reinforcement learning for placement	Improved routability and reduced routing violations using RL techniques.	High computational complexity and training cost remain concerns.
Synthesis Experiments and Performance Metrics for Evaluating the Quality of IP Blocks and Megacells	IP quality assessment	Established methodology for comparing synthesized IP implementations.	Limited focus on advanced technology nodes.
VLSI Design Course with Commercial EDA Tools to Meet Industry Demand – From	Physical design education and training	Demonstrated industry-oriented learning using Synopsys tools.	More advanced design case studies can be incorporated.

Logic Synthesis to Physical Design			
VLSI-Inspired Design Automation for Scalable Power Electronics Layout Optimization	Layout optimization for power electronics	Applied VLSI floorplanning concepts to power electronics design.	Requires validation on larger industrial systems.

CHAPTER 3
OBJECTIVES

The main objective of this project is to understand the complete APR flow for a high-performance Digital design block with focusing on optimizing the key aspects such as timing, power, area and congestion.

1. The project starts by exploring each stage of APR like floorplanning, placement etc. individually and what all are the steps involved inside those stages and how the tool is optimizing the metrics in that stage.
2. Understanding of the industry standard tools like Synopsys Fusion Compiler and Synopsys Lynx will also be developed during the course of this project which is necessary for the completion of this project.
3. Some errors or failures are likely to occur during the PnR flow, so rectifying those errors will also be a part of the objectives.
4. Also checking the design metrics and try to optimize those metrics at each stage using different techniques will the most significant objective of this project.

The project aims to improve the efficiency, reliability and manufacturability at advanced technology nodes by identifying bottlenecks and implementing proper optimization techniques. These improvements help achieve better design quality while ensuring that the final implementation meets the required performance.

CHAPTER 4
FLOW OF THE PROJECT

The Register Level Simulation run, which forms the foundation of the physical design flow, is the first step in the project execution process. First, we collect crucial input from many teams. While the floorplan team distributes DP-related material, including important floorplan files, the RTL team updates the register-transfer level design at different stages. Clock-related constraints, which include all clock-related requirements and partition-level restrictions required for timing are also gathered. The Lynx Execution Monitor incorporates these inputs and sets up the RLS recipes to propel the flow.

Design planning, placement, CTS, routing, and post-route optimization are the main phases of the RLS flow. Specific goals, such as setup, first optimization, and final optimization, are included in each stage and need to be closely observed and verified. Regular review of log files is important to identify errors, warnings and fatal messages that may affect the flow. After completing major design milestones, the updated design database is checked into a common repository, making it accessible to further teams. This enables teams responsible for PV (Physical Verification), FV (Formal Verification) and RV (Reliability Verification) to perform their respective analyses and provide timely feedback before the design proceeds to the next stage.

Throughout the flow, the design database is checked in Fusion Compiler at each major stage to verify design correctness and monitor the progress. Detailed analyses, including timing path evaluation, port connectivity and consistency checks are performed to ensure that the design remains compliant with the specified constraints. Timing reports are generated and reviewed to identify and resolve setup and hold violations before moving to subsequent stages. As the design approaches completion, physical verification is carried out using Calibre. This includes DRC, LVS and antenna effect analysis to identify any potential issues. These verification steps confirm that the final layout satisfies foundry design rules, maintains logical correctness and is suitable for fabrication.

CHAPTER 5
PLACEMENT AND ROUTING

5.1 MACRO PLACEMENT

Macro placement is an important stage in the physical design flow as it directly influences chip area utilization, routing congestion and overall timing performance. The process begins by identifying all hard macros in the design using a hierarchical filter. These macros are then positioned according to the floorplan requirements with a predefined offset applied along the x-axis to establish an organized initial placement. This strategy helps reduce interconnect length and improves connectivity between macros and surrounding logic. Once the desired locations have been assigned, the macros are marked as fixed to prevent any unnecessary movement during further optimization stages. After macro placement is completed, the floorplan is verified to ensure compliance with design rules. Finally, the updated floorplan is exported as a DEF (Design Exchange Format) file preserving the physical locations of all design components for use in later stages of the implementation flow.

A soft placement blockage is made inside a specified area of the floorplan to direct routing and increase overall design efficiency. This obstruction efficiently reserves routing resources and optimizes time by limiting standard cell placement and permitting only buffer insertion. A hard placement obstruction is also included inside the macro zone. By doing this, it is ensured that no standard cells are positioned too near macros, which may otherwise result in routing problems, signal integrity problems, or placement violations.

Macros can be abutted if the pins are in center. And if the pins are on the edge of the macros proper spacing needs to be maintained. Macros should always be placed at the edge of core allowing enough room for standard cells in core area. Fig. 5.1 and Fig. 5.2 show the arrangement of macros in different scenarios.

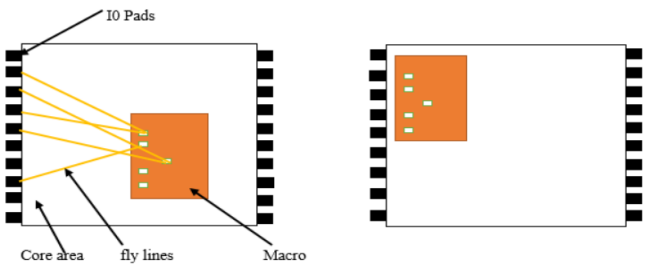

Fig. 5.1: macro to IO ports fly lines & macro places at the core boundry [31]

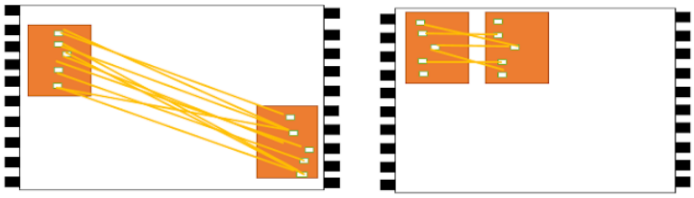

Fig. 5.2: macro to macro fly lines & macros placed near to each other [31]

5.2 STANDARD CELLS PLACEMENT

Standard cell placement is a crucial step in the physical design process that involves precisely locating synthesized logic cells inside the chip architecture. In order to maximize wirelength, congestion, and timeliness while maintaining adherence to design guidelines, these cells must be arranged in predetermined site rows. In order to balance density and reduce total wirelength, the placement process starts with a global placement phase that disperses cells throughout the floorplan. Detailed placement (legalization) comes next, when cells are positioned in accordance with legal locations, overlaps are eliminated and spacing restrictions are met. In order to minimize delay and enhance WNS and TNS, timing-driven placement further fine tunes the locations of cells along crucial pathways. In addition, modern placement algorithms includes power-aware optimization techniques that consider switching activity to reduce localized power hotspots. Congestion-aware placement strategies are also applied to distribute standard cells more evenly. An effective standard cell placement not only improves routability and supports timing closure but also contributes to lower power consumption.

5.2.1 Placement Strategies of Standard Cells

1. Timing driven – In this strategy timing is critical (Timing effort can be High/Medium/Low)
2. Congestion Driven - Congestion is critical and it should me minimum, Spread of cells is high. Preferred when less area available.
3. Area Driven - Replace multiple cells with one single cell by doing logic restructuring to recover area
4. Power driven - Power critical, not to use leaky cells e.g. mobiles, laptop

5.2.2 Quality Checks before Placing Of Standard Cells

There are some quality checks that needs to be performed before the placing of standard cells.

1. I/O Ports Fixed: All input/output ports are placed and locked.
2. Macro Placement: Macros are positioned and fixed to avoid movement.
3. Row Creation: Standard cell rows are generated for legal placement.
4. Placement Blockages: Blockages added to restrict cell placement near sensitive areas.
5. Power Routing: Initial VDD/VSS grid routed across the layout.
6. PG Shorts Check: Verified no shorts between power and ground nets.
7. Macro Overlaps: Ensured macros do not overlap with each other or other blocks.

5.2.3 Pre Placement Cells

1. End Cap Cells - To avoid breaking design rules and guarantee correct row termination, they are positioned at the edges of conventional cell rows. They help maintain the physical integrity of the design by eliminating open diffusion regions and properly enclosing the boundaries of placement rows.
2. Tap Cells - Tap cells are used to connect the substrate to the power supply rails (VDD or VSS) to prevent latch up and maintain proper biasing. They are inserted at regular intervals throughout the layout to ensure electrical stability.
3. I/O Buffers and Feedthrough Buffers - I/O buffers are used to transfer signals between the core logic and I/O pads while maintaining signal integrity across different voltage domains. Feedthrough buffers facilitate clean routing and temporal closure by assisting in the propagation of signals across blocks or rows without the need for functional logic.
4. Spare Cells - In order to enable upcoming ECOs, certain underused logic gates (such as inverters and NANDs) were added during preplacement. They increase design flexibility and turnaround time by enabling small feature upgrades without restarting the entire APR sequence.

5.2.4 Placement Stages

1. Global Placement - At this point, every standard cell is roughly dispersed over the layout. Cells may not yet be matched with legal locations and may overlap. Global placement aims to give approximate starting points that balance density and reduce total wirelength. At this point, timing optimization is also taken into account to guarantee that key pathways are prioritized. Fig. 5.3 show the global placement stage in the partition.

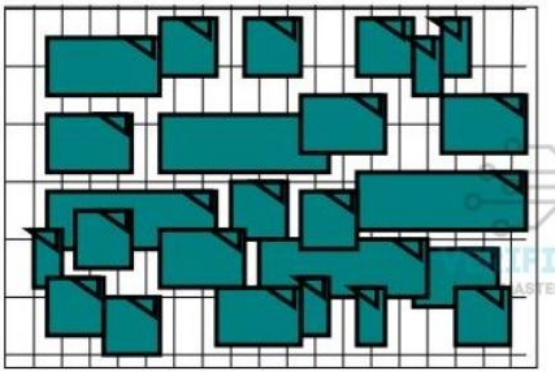

Fig. 5.3: Global Placement [32]

2. Detailed Placement - Cells are moved to acceptable locations in the placement rows following global placement. During this stage, cells are properly aligned within the placement rows and spacing regulations are satisfied. This step ensures that the design maintains timing integrity while adhering to physical restrictions. Fig. 5.4 shows the legalization of cells in the partition.

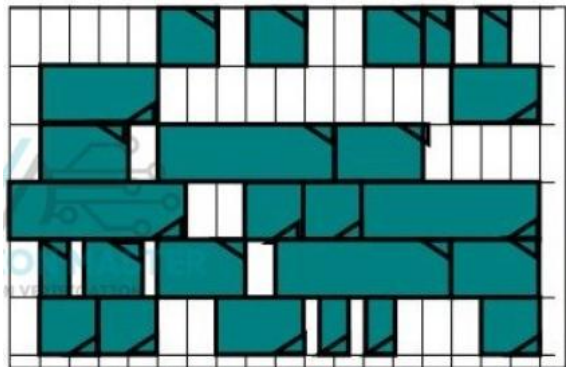

Fig. 5.4: Detailed Placement [32]

3. Placement Optimization - After legalization is completed, the placement undergoes further refinement through optimization techniques. This includes power aware placement to reduce hotspots, area optimization to balance density and timing driven improvements to optimize WNS and TNS. The primary objective is to achieve an optimized placement that supports efficient routing while meeting overall PPA requirements.

5.2.5 Tie Cells

Tie cells are specialized standard cells used to provide a fixed logic value in a reliable manner. They are used to supply constant logic 0 or logic 1, ensuring proper functioning of unused inputs. To provide stable logic levels, tie cells use regulated transistor architectures rather than just connecting gate inputs directly to VDD or VSS rails, which can result in reliability issues including leakage, noise sensitivity and electrostatic discharge damage.

Tie High Cell: This cell uses an intrinsic transistor configuration to securely connect the input to VDD, producing a constant logic "1". It ensures that a stable high voltage is maintained at the gate input. Tie High cells are commonly used for configuration pins, enable signals and unused inputs that need to be held at logic "1".

Tie Low Cell: This cell safely biases the input to VSS to deliver a constant logic "0". It eliminates direct rail connections and guarantees that the input is maintained at a steady low voltage, much as Tie High. Signals, reset pins, and unused inputs that need to stay at logic "0" are usually disabled using tie low cells.

5.3 ROUTING

One of the most important steps in the VLSI physical design cycle is routing, which turns a logical netlist into a manufacturable layout by creating the actual electrical connections between standard cells, macros, and I/O pins. It is crucial for making sure that all power, clock, and signal networks are connected in a way that complies with timing restrictions, design guidelines, and reliability standards. By decreasing wirelength, lowering parasitic capacitance and resistance, and maximizing signal integrity, a well-executed routing plan directly affects the three basic design criteria performance, power, and area. Since connectivity delays frequently predominate at advanced technology nodes and key nets must be carefully allocated to higher metal layers or insulated to fulfill setup and hold limitations, routing is also essential to timing closure. Routing also plays a key role in ensuring power integrity by implementing a strong PDN (Power Distribution Networks) with sufficient straps, rings and vias to minimize IR drop and mitigate electromigration. Beyond electrical correctness, routing is essential for manufacturability. Successful fabrication depends on adherence to complex design rules, effective congestion

management and efficient utilization of routing resources. As a result, routing is no longer viewed as an interconnection step. Instead, it is a critical optimization phase that ensures the design meets functional, performance, reliability and manufacturability requirements at advanced technology nodes.

5.3.1 Goals of Routing

1. Open/Short Checks - All nets must be properly connected with zero opens and shorts, this physical verification will ensure electrical correctness.
2. Setup and Hold Timing - Routing paths must be optimized to meet setup and hold timing requirements, specifically for all the critical nets that may include long nets also.
3. DRC Compliance - Clock routing must comply with all the design rule checks related to capacitance, transition time and layer constraints to avoid any violations.
4. Physical DRC - Routing must satisfy minimum spacing, width per metal layer and area rules to ensure manufacturability.

5.3.2 Stages of Routing

1. Global Routing – The first step in the routing process is called global routing, during which each net's estimated path across the chip architecture is designed. By segmenting the layout into routing areas and calculating wirelength, congestion, and layer consumption, it functions at a coarse level. Without designating precise tracks or vias, the objective is to identify workable routing pathways that reduce overall wirelength and steer clear of crowded locations. By offering a high-level roadmap for signal, clock, and power connections, global routing aids in the early detection of possible bottlenecks and directs the detailed routing engine. Fig. 5.5 shows the global routing stage.

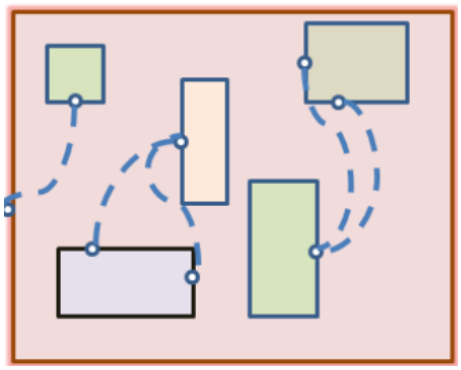

Fig. 5.5: Global Routing [33]

2. Track assignment – The intermediary step known as "track assignment" involves mapping the global routing pathways onto particular routing tracks that are accessible in each metal layer. In this process, each net's lawful tracks are chosen while taking routing direction restrictions, metal layer preferences, and spacing regulations into account. In addition to preparing the layout for detailed routing, track assignment guarantees that nets are dispersed effectively across the available routing resources.
3. Detailed Routing – The last and most exact step is detailed routing, when each net is given specific wire pathways, vias, and metal layers. It guarantees that all connections are finished while closely following DRC, which include area, width, and minimum spacing restrictions. In addition to being essential for timing closure, detailed routing fixes shorts, openings, antenna effects, and signal integrity problems. This stage finalizes the physical connectivity of the chip and has a direct impact on the overall PPA. Fig. 5.6 shows the detailed routing stage where connections are properly done through metal wires on different routing layers.

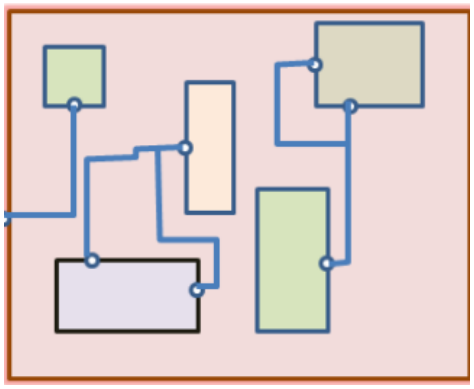

Fig. 5.6: Detailed Routing [33]

The placement and routing stage of the APR flow was discussed in detail in this chapter, with focus on their impact on overall design quality and performance. The chapter covered key pre placement requirements, tie cell insertion, standard cell placement techniques and different techniques used for macro placement. With a focus on time closure and manufacturability, routing techniques such as global routing, track assignment, and detailed routing were investigated. Achieving ideal PPA metrics, lowering congestion, and enhancing signal integrity all depend on these steps being implemented correctly.

CHAPTER 6
TIMING ANALYSIS AND OPTIMIZATION

6.1 INTRODUCTION TO TIMING IN VLSI DESIGN

One of the most important design parameters in VLSI physical design is timing. It establishes whether signals go through sequential and combinational pathways within the necessary clock cycle. The chip will function dependably at its target frequency without setup or hold violations if timing closure is achieved. Placement, routing, CTS, and parasitic effects all affect time in APR flow. To measure infractions and direct optimization, metrics like WNS and TNS are employed.

Timing controls whether data launched by one flip-flop is accurately caught by another at the subsequent clock edge in synchronous digital systems. Setup and hold time violations can lead to metastability, functional faults or total design failure. Therefore timing analysis is essential, it ensures reliable operation across all PVT (Process, Voltage, and Temperature) corners in addition to confirming the maximum operating frequency.

STA is the industry standard method for evaluating timing paths. It calculates slack values for all the timing paths. The two important metrics are WNS and TNS. Timing closure is achieved when all the critical paths meet their required constraints with zero slack. Modern APR flows integrate timing driven placement, CTS and routing to minimize skew, jitter and interconnection delays. To resolve timing violations iterative optimization techniques such as buffer insertion, route adjustments, and cell resizing. At advance technology nodes, timing closure becomes more complex, as optimization must also take care for signal integrity concerns i.e crosstalk, IR drop and electromigration effects.

6.2 TIMING METRICS

Timing metrics are fundamental indicators used to evaluate whether a VLSI design meets its performance requirements under specified operating conditions. They quantify the ability of signals to propagate through combinational and sequential paths within the allocated clock cycle.

6.2.1 Setup Time

The minimum time before the active clock edge during which input data must remain stable at a flip-flop. If data arrives late, a setup violation occurs, potentially causing incorrect data capture. Directly limits the maximum operating frequency of the design.

6.2.2 Fixing max delay (Setup) violations

We need to perform some sanity checks before fixing any max delay violations like:

- Check STA run log for errors/warnings
- Check the validness of the timing path
- Check launch and capture edges
- Check clock period

Now, the violation may be in data path or clock path. Depending on that fixes are applied.

Data path violations:

1. The Easiest way is to swap SVT (Small Threshold voltage)/HVT (High Threshold voltage) with LVT (Low Threshold voltage)/ULVT (Ultra low threshold voltage) cells which has less delay and are easy to drive. Also after replacing no PnR flow is required in ECO stage. Disadvantage is that leakage power is increased.
2. Upsizing the cell or increasing the drive strength of the cell which reduces the propagation delay but both area and power is compromised.
3. By adding buffers - since each cell can only drive the o/p capacitance up to a certain limit so buffers are required after certain distances. Disadvantage is that by adding a buffer area and power is compromised. Fig. 6.1 shows the addition of a buffer between two cells.

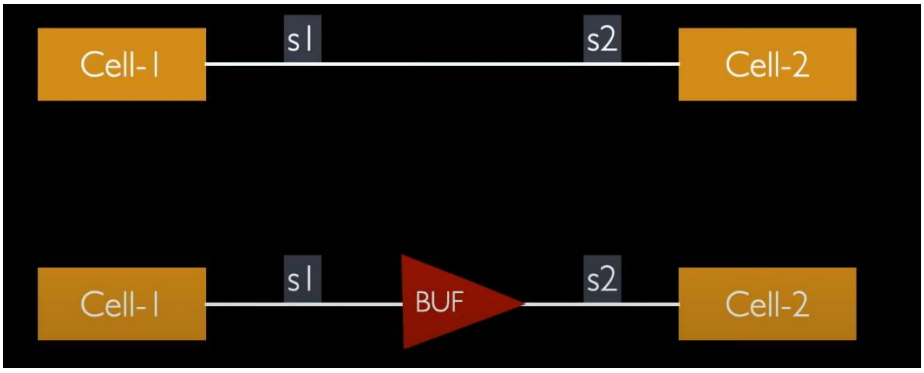

Fig. 6.1: Buffer added in the net to improve the quality

4. Routing basics like use less vias, avoid using detours in nets, use upper metal layers for routing as they have less resistance.
5. Inverters have better driving capability than buffers so using two inverters in a long net than a single buffer is better and recommended.

Clock path violations: The concept of clock push and pull is used to fix clock path violations which is: pull launch clock (by removing buffers) to decrease the clock latency of launch Flop/ Push the capture clock (by adding buffers) to increase the clock latency of capture flop.

6.2.3 Hold Time

The minimum time after the clock edge during which input data must remain stable. If data changes too early, a hold violation occurs, leading to metastability or functional errors. Ensures reliable data transfer between sequential elements.

6.2.4 Fixing min delay (Hold) violations

We need to perform some sanity checks before fixing any max delay violations like:

- Check STA run log for errors/warnings
- Check the validness of the timing path
- Check launch and capture edges
- Check clock period

Now, the violation may be in data path or clock path. Depending on that fixes are applied.

Data path violations:

1. Swapping of LVT/ULVT cell with SVT/HVT cell to increase the data path delay. But the setup margin need to be kept in mind.
2. Downsize cells - cell with less drive strength will add delay to the path.
3. Increase the wire length, introducing detours in routing, using lower metal layers.
4. By adding some low drive strength (provides large delay) buffers to increase the data path delay.

5. To fix larger magnitude of hold violations, delay cells can be used with larger delay, area and power can be used in place of buffers. In place of many number of buffers to be added, delay cells can be used.

Clock path violations: Push launch clock (by adding buffers) to increase the clock latency of launch Flop/ Pull the capture clock (by removing buffers) to decrease the clock latency of capture flop.

6.2.5 Fixing Max Transition Violations

The maximum signal rise or fall time permitted for nets in a design is known as the maximum transition. In order to prevent excessive delay or poor performance, it is defined in the technology library to guarantee that signals transition within acceptable speed ranges.

When a signal's slope beyond the designated threshold, a max transition violation happens. This is typically caused by excessive capacitive loading, lengthy interconnects, or inadequate driving cell drive strength. These needs to be fixed:

1. If violation is small, swap HVT cell with a LVT cell of the driver. The current will be increased which will improve the drivability.
2. Upsize the driver cell, as current is directly proportional to W/L ratio. Increase the drive strength according to the demand.
3. Split the fanout by cloning, by this the load will be distributed. Fig. 6.2 shows the splitting of a high fanout net into two nets of lesser fanout.

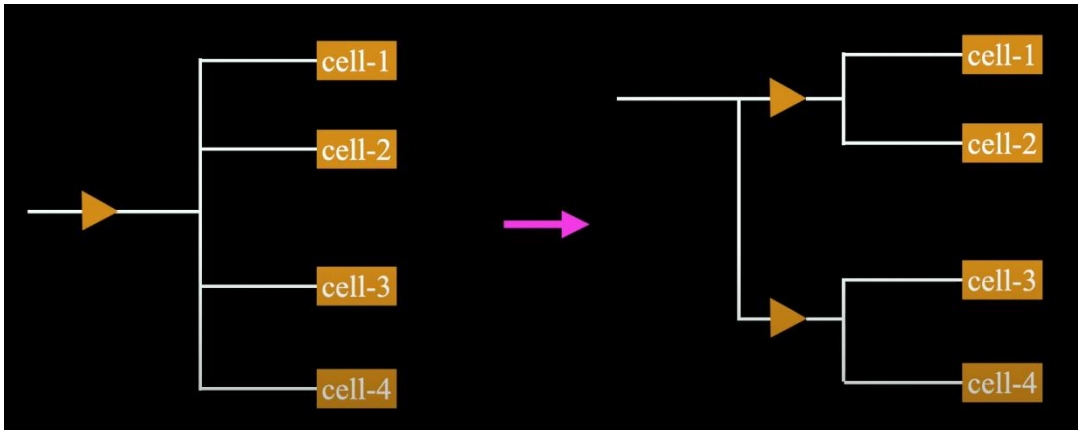

Fig. 6.2: Splitting the fanout

4. Split fanout by buffering, add buffers in fanout to split the load. Fig. 6.3 shows splitting of a fanout net and adding buffers in each branch which fixes the max transition violations.

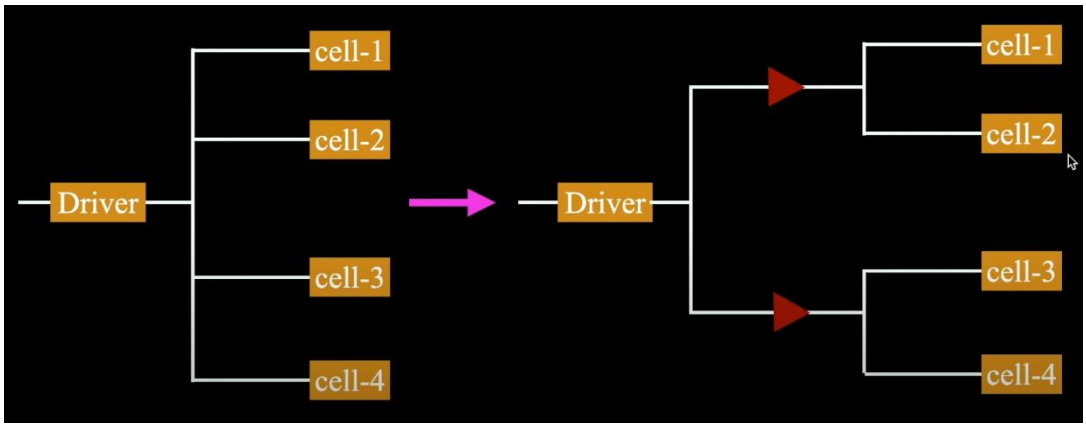

Fig. 6.3: Splitting the fanout and adding buffers in each branch

6.2.6 Fixing Max Capacitance Violations

Maximum capacitance refers to the upper limit of load capacitance that a driving cell output pin can safely drive, as defined in the technology library. This constraint ensures that the driver can switch its output within the required timing window without excessive delay or reliability issues.

Fixes:

1. Upsize the driver cell
2. Split fanout by cloning
3. Split fanout by buffering

6.2.7 Fixing Crosstalk Violations

In a VLSI design, crosstalk is undesired coupling between neighboring interconnects brought on by inductive effects and parasitic capacitance. When two nets are in close proximity to one another, the aggressor's switching activity may cause noise or delay changes in the victim's net. At advanced technology nodes, when wire spacing is decreased and connection density is high, crosstalk becomes a substantial contributor to timing uncertainty and signal integrity concerns.

Fixes:

1. Reduce coupling cap by using track reassignment in which the aggressor net is moved away from the victim net.
2. Break the long victim net.

3. By upsizing the victim net driver and by downsizing the aggressor net driver.
4. Apply NDR rules (NDR: Default rule is 1s, 1p, 1w (spacing, pitch, width). NDR is non default rule which is used to reduce the latency, noise and improve timing. 2w will lead to reduction in latency as more thick metal will lead to less resistance. 2s, 2p will lead to reduction in crosstalk.)
5. Shield victim net (Shield is generally a ground signal which is added wherever the aggressor net is going to prevent the victim net.) so that extra voltage coupled by the aggressor net can be discharged by the ground shield net.
6. Add buffers at right location in the victim net, but we need to do keep in mind the timing and power violations.

This chapter's main focus was on timing analysis and optimization strategies that are necessary to achieve timing closure. The effects of key timing factors on circuit performance were discussed, including setup time, hold time, transition time, capacitance, and crosstalk. To address timing violations, a number of techniques were used, including as buffering, fan-out optimization, cell resizing, threshold voltage optimization and clock route modifications. Reliable circuit operation under various process, voltage, and temperature circumstances is ensured by the effective implementation of these strategies.

CHAPTER 7
RESULTS AND OBSERVATIONS

7.1 FLOORPLANNING AND MACRO PLACEMENT

The Fig. 7.1 depicts below the placement of macro cells towards the core region of the design. Macros are placed near the boundary of the core region so that enough spacing can be maintained, thereby reducing congestion and improving the routability and timing performance, also effective macro placement ensures minimal wire length. This snapshot is took from fusion compiler.

Fig. 7.1: Macro Placement in the assigned partition

The Fig. 7.2, shows the hard placement blockages added around the macro regions to restrict standard cell placement in sensitive areas. Hard placement blockages prevent cells from being placed too close to the macros, thereby reducing routing congestion, overlap issues, and signal integrity problems.

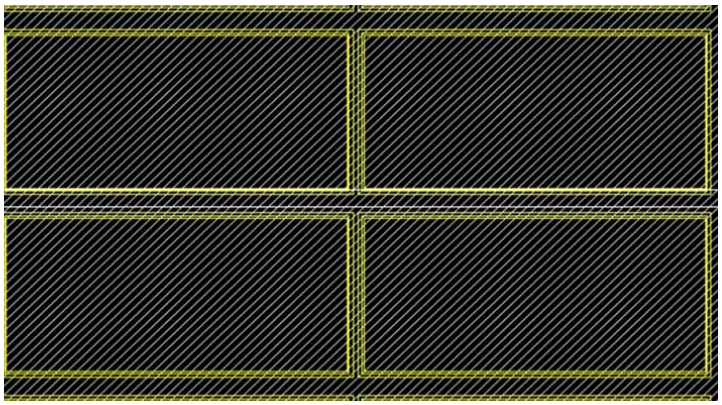

Fig. 7.2: Placement Blockages added in the partition

7.2 SHORTS REDUCTION TECHNIQUES

7.2.1 Shorts reduction using placement boundary box

The Fig. 7.3, shows the use of boundary boxes, which are restricted regions created around congested areas to control routing resources and limit excessive routing activity. This technique helps reduce shorts between neighbouring nets in highly congested regions. The yellow boxes are the boundary boxes created in the partition.

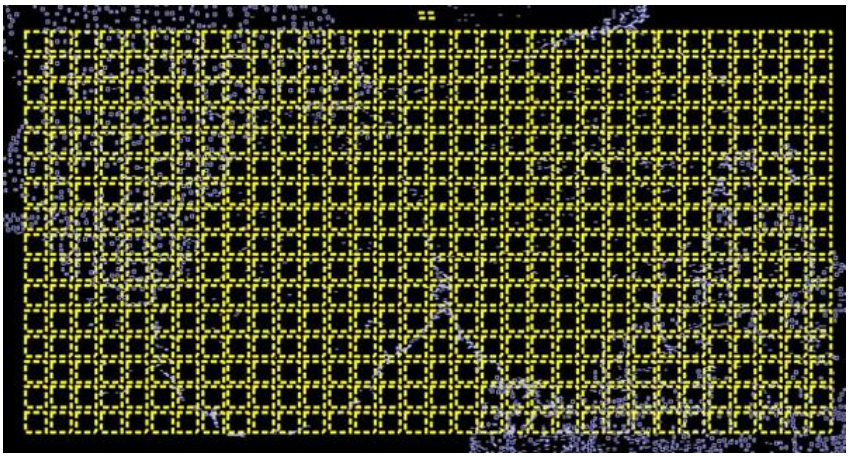

Fig. 7.3: Placement boundary box/bounds

7.2.2 Shorts reduction using manual script

There were terminal shorts coming in one of the blocks due to small M15 terminals getting created which caused in shorts across the block boundary. A script was used to remove those shorts. The

main idea was to select the die area and subtract the core area from that, and all the terminals present in that region smaller than a threshold value were removed which cleared all the terminal shorts. This script was then sourced in the flow itself. Fig. 7.4 shows the number of opens and shorts after the port-up and Fig. 7.5 shows all those shorts removed after sourcing the script.

⊞ Open	300	300
⊞ Short	115118	115118

Fig. 7.4: Shorts and opens before sourcing the script

```
Total number of short violations is 0.
Total number of open locations is 0 (0 open nets).
Total number of floating route violations is 0.
```

Fig. 7.5: Shorts and opens after sourcing the script

7.3 ROUTING OF OPEN SIGNALS

The Fig. 7.6 shows the routing of open nets identified during the physical design flow. In the left image, the net remains unrouted with no physical connection present, whereas in the right image, the net is successfully routed by establishing the required physical connection between the components.

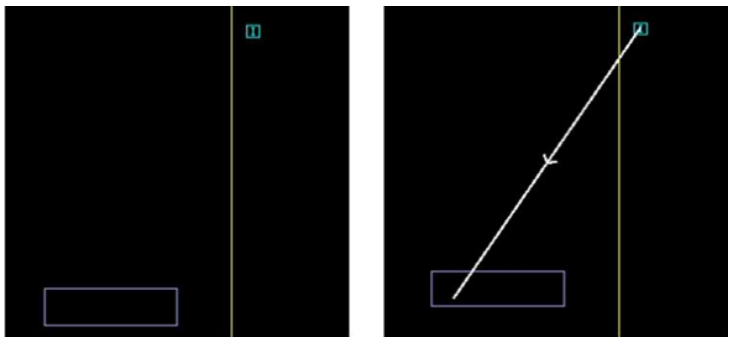

Fig. 7.6: Open Net Fixing (Before and After)

7.4 REGISTER OVERLAP

The Fig. 7.7 shows the register overlap issue caused due to register size changes during optimization. In the image, overlapping registers create shorts in the layout, the overlaps are removed after legalization and slight register movement, resulting in a clean and stable placement.

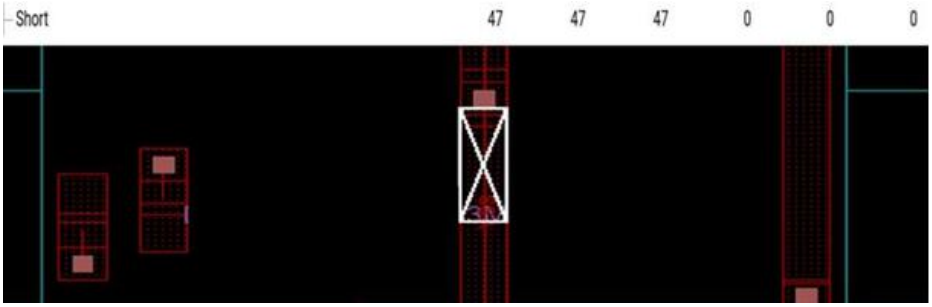

Fig. 7.7: Register Overlap issue which leads to shorts

7.5 TIE CELL ADDITION

The Fig. 7.8 displays the insertion of tie cells in the circuit that ensure the logic '0' or logic '1' connection through stable routing. Tie cells are preferred to connect the gate inputs to either Vdd (power) or ground rather than direct connection, as it avoids problems like gate-oxide breakdown, ESD (Electrostatic Discharge), and noise coupling. All the floating input pins cannot be left floating, so they need to be at least connected to a tie cell.

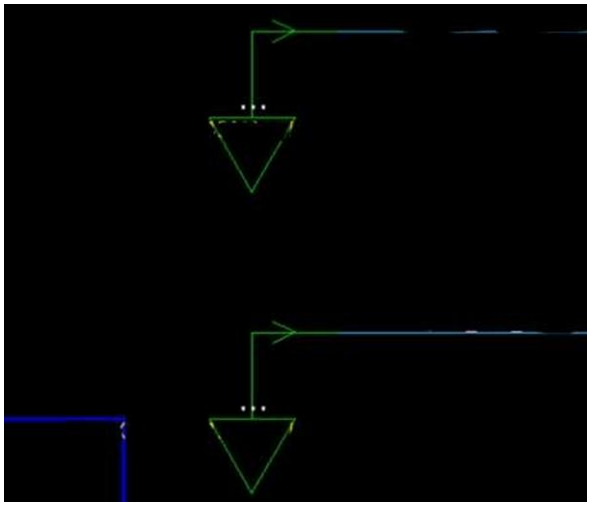

Fig. 7.8: Addition of tie cells to avoid VCLP issues

7.6 DATAPATH VIOLATION FIX

In the Fig. 7.9, it is shown that a routing net that was long and detected from the data path was optimized by segmenting it. This segmentation process was achieved through the use of buffers.

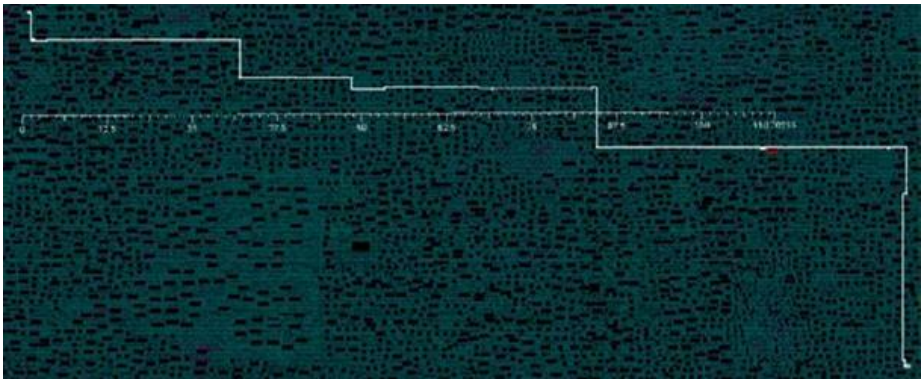

Fig. 7.9: Long net which violates the timing

7.7 TIMING FIX

7.7.1 Setup (max) violation fix

After multiple rounds in ECO timing violations were fixed and numbers got reduced in each round, it may also get degraded because of functional ECO which added few more flops which degrades the timing. Table 7.1 shows the initial timing report of ECO3, showing corner, WNS, TNS and number of violating paths. Table 7.2 to Table 7.4 describes the setup timing report in each successive ECO round. After ECO 10, in Table 7.5 we can see that the setup timing got converged for all the corners. All these timing numbers were taken from synopsys primetime.

Table 7.1: Setup timing after ECO3

Corner	WNS	TNS	Path
Corner 1	-0.0075	-0.051	12
Corner 2	0	0	0
Corner 3	0	0	0
Corner 4	-0.0046	-0.014	6
Corner 5	-0.95421	-26.89	29

Table 7.2: Setup timing after ECO4

Corner	WNS	TNS	Path
Corner 1	-0.028	-0.389	37
Corner 2	0	0	0
Corner 3	0	0	0
Corner 4	-0.095	-0.684	34
Corner 5	0	0	0

Table 7.3: Setup timing after ECO5

Corner	WNS	TNS	Path
Corner 1	-0.028	-0.382	36
Corner 2	0	0	0
Corner 3	0	0	0
Corner 4	-0.094	-0.673	32
Corner 5	0	0	0

Table 7.4: Setup timing after ECO8

Corner	WNS	TNS	Path
Corner 1	-0.049	-0.35	13
Corner 2	0	0	0
Corner 3	0	0	0
Corner 4	-0.011	-0.015	4
Corner 5	0	0	0

Table 7.5: Setup timing after ECO10

Corner	WNS	TNS	Path
Corner 1	0	0	0
Corner 2	0	0	0
Corner 3	0	0	0
Corner 4	0	0	0
Corner 5	0	0	0

7.7.2 Hold (min) violation fix

Similarly, hold violations were also fixed during the ECO stage. Table 7.6 shows the initial timing report of ECO3, showing corner, WNS, TNS and number of violating paths. Table 7.7 to Table 7.9 describes the hold timing report in each successive ECO round. After ECO 10, in Table 7.10 we can see that the hold timing has improved and only small violations are left. Hold violations were more degraded whenever new functional ECOs were consumed which explains the fluctuations in the timing numbers. All these timing numbers were taken from synopsys primetime.

Table 7.6: Hold timing after ECO3

Corner	WNS	TNS	Path
Corner 1	0	0	0
Corner 2	-0.0015	-0.002	2
Corner 3	0	0	0
Corner 4	0	0	0
Corner 5	-0.00156	-0.002	2

Table 7.7: Hold timing after ECO4

Corner	WNS	TNS	Path
Corner 1	-0.219	-0.899	6
Corner 2	-0.188	-0.717	8
Corner 3	-0.258	-1.0932	9

Corner 4	-0.181	-0.691	6
Corner 5	-0.188	-0.717	8

Table 7.8: Hold timing after ECO5

Corner	**WNS**	**TNS**	**Path**
Corner 1	-0.010	-0.010	1
Corner 2	-0.0055	-0.0057	1
Corner 3	-0.0088	-0.0108	3
Corner 4	-0.156	-0.675	19
Corner 5	-0.016	-0.048	4

Table 7.9: Hold timing after ECO8

Corner	**WNS**	**TNS**	**Path**
Corner 1	-0.014	-0.039	4
Corner 2	-0.003	-0.003	1
Corner 3	0	0	0
Corner 4	0	0	0
Corner 5	-0.0047	-0.0079	2

Table 7.10: Hold timing after ECO10

Corner	**WNS**	**TNS**	**Path**
Corner 1	0	0	0
Corner 2	-0.0002	-0.0004	2
Corner 3	0	0	0
Corner 4	0	0	0
Corner 5	-0.005	-0.047	20

Real-world outcomes from the APR flow's implementation showed how successful different optimization strategies are. Floorplanning, congestion control, shorts reduction, open-net routing, tie-cell insertion, register overlap resolution, and datapath optimization were all effectively improved. To gradually get rid of setup and hold time violations, several ECO iterations were carried out. Routability, temporal convergence, and overall design quality were all significantly improved in the final results. All the screenshots and timing values are taken from the fusion compiler and primetime.

CHAPTER 8
CONCLUSION AND FUTURE SCOPE

8.1 CONCLUSION

In this project a successful conversion of RTL, provided by the front-end team into a GDSII-ready layout, preparing the design for foundry manufacturing. Effective macro placement in the early phases of the flow allowed the block to reach timing convergence for both internal and interface timing. Starting from ramping up the basics and getting to solve the issues in real time, this work includes all the concepts required in an APR flow. Worked on different partitions which had different issues and required different approaches to resolve those. Reviewing Caliber reports and reporting the issues like max tran and max output cap. Delivered the FRAM view of the hip partitions. All timing violations, including clock and data transitions, were systematically addressed and fixed. Completed the ECO stage and did the successful tapeout for my partition. Did multiple rounds of ECO and resolved the issues and violations in each round and implemented multiple functional ECOs. All things considered, this work shows how to successfully implement a solid physical design flow and provides a solid basis for next developments in high-performance chip design.

8.2 FUTURE SCOPE

Future research will focus on investigating 3D IC architectures and chiplet-based designs, along with adapting the physical design flow for advanced technology nodes. It will also focus on the application of machine learning techniques to improve macro placement and routing. To improve design productivity and reduce turnaround time, techniques such as clock gating, DVFS (Dynamic Voltage and Frequency Scaling), automated ECO management, and AI driven early prediction of DRC and LVS violations will be incorporated, to support the development of next-generation high performance integrated circuits.

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3	Submitted to University of Birmingham	Student Paper
4	Govindu Vikas, Ch. Ganesh, L. Padma Sree. "RTL-to-GDSII Implementation of a Register Processor Top-Level Design in 28nm Technology", 2025 Third International Conference Emerging Applications of Material Science and Technology (ICEAMST), 2025	Publication
5	www.ci.salisbury.md.us	Internet Source
6	www.ijraset.com	Internet Source
7	arxiv.org	Internet Source
8	Jenila C, Ummadisetty Vishnu Sai, Dhosti Manoj Kumar Reddy, M V Sai Akhil, S Uday Prasad, S Manjunatha Chari. "Efficient Synchronous FIFO Design: A Structured Approac using ASIC Methodology", 2025 7th International Conference on Inventive Material Science and Applications (ICIMA), 2025	Publication
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10	www.datasheet.hk	Internet Source
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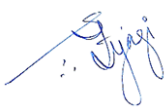

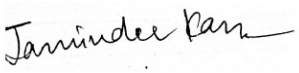

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