**Thesis**

**On**

# Analysis and Design of 14-Bit Self Calibrated DAC of SAR-ADC for Bio-Medical Application

Submitted towards the partial fulfillment of requirement for the award of degree of

## Master of Technology

## In

## VLSI Design

Submitted by

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# DECLARATION

I hereby declare that the dissertation entitled "Analysis and Design of 14-Bit Self Calibrated DAC implementation of SAR-ADC for Bio-Medical Applications" is an authentic record of my work carried out as a partial requirement for the award of degree of M.Tech. (VLSI Design) at Thapar University, Patiala, under the supervision of Dr. Alpana Agarwal, Associate Professor, ECED and refers other researcher's work which are duly listed in reference section.

The matter embodied in this thesis has not been submitted for award of any other degree at this or any other university.

9/6/14

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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# ABSTRACT

SAR-ADC is best suited for low power applications where power has a trade-off with speed. Use of redundant circuitry reduces the on chip area making it cost effective. DAC is one of the components of SAR-ADC that introduces error voltage due to mismatch and consumes large power other than comparator.

This work presents the analysis and design of the high resolution *i.e.* 14-bit Digital to Analog convertor (DAC) which is Self Calibrated for the capacitive mismatches. DAC that has been designed is a smart circuit which performs three operations consecutively they are sampling, subtracting voltages and digital to analog conversion. All this work is primarily focused for the Bio-Medical Applications and hence the operational parameters are selected accordingly. Sampling speed of DAC is 100kS/s *i.e.* very slow speed as we have a tradeoff with power here in this operational circuit design. 1.6 MHz clock speed is used for the analysis of the DAC. Proposed DAC uses self calibration technique which is a foreground calibration technique and is used for calibrating maximum of 20fF capacitance mismatch which is greater than the mismatch equivalent to LSB (Least Significant Bit) capacitor. Power for each conversion cycle is calculated which is very less in the order of nWatt and gain error is less than 0.5LSB. EDA tool used for design and analysis is Cadence® Virtuoso Analog Design Environment with 180nm technology and Cadence® Virtuoso Layout XL Environment for designing and verification of layouts.

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# Abbreviations

| | |
|---|---|
| SAR | Successive Approximation Register |
| ADC | Analog to Digital Converter |
| MOS | Metal Oxide Semiconductor |
| ICMR | Input Common Mode Range |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| CDAC | Calibration DAC |
| DAC | Digital to Analog Converter |
| SS | Slow NMOS Slow PMOS |
| FF | Fast NMOS Fast PMOS |
| FS | Fast NMOS Slow PMOS |
| SF | Slow NMOS Fast PMOS |
| TT | Typical NMOS Typical PMOS |
| CMOS | Complementary Metal Oxide Semiconductor |
| LSB | Least Significant Bit |
| MSB | Most Significant Bit |
| VLSI | Very Large Scale Integration |
| ENOB | Effective Number of Bits |
| SINAD | Signal to Noise and Distortion Ratio |
| INL | Integral Non Linearity |
| DNL | Differential Non Linearity |
| THD | Total Harmonic Distortion |
| NMOS | Negative-Channel Metal-Oxide Semiconductor |
| PMOS | Positive-Channel Metal-Oxide Semiconductor |

# Chapter 1

## MOTIVATION

In recent year's lot of improvements and achievements have been made in the Bio-medical domain. For example these days a diabetic could easily test his sugar level by just pinning an electronic device into his finger and it senses his blood sugar level just in a fraction and accordingly he could inject the required insulin level after consulting his doctor. This has been possible only due to recent advancements in the technology which is the ramification of human nature to exploit everything. Taking into consideration that insulin consumption of a person depends on his activity level like consumes less when just sitting idle and more when doing some physical exercise, so why not make a sensible device which could inject insulin according to his activity periodically rather than injection the whole sum of insulin for a week or for a month. So this can be done by making a sensor which senses the liquid level(defines sugar level) in our skin and after obtaining the information we could do analog and digital calibrations which require an precise data acquisition system and then accordingly can inject insulin using micro-infusion pumps, which is a nano-pump realized using MEMS technology. This is only a little application of how electronics can change in better the life of people. The block diagram for the realization of the complete system:


Figure-1.1 Snapshot of a Nano-pump

Source: www.diabetescaregroup.info

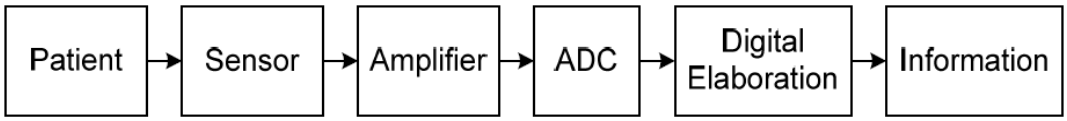



Figure-1.2 Block Diagram for measurement of parameters

As here the patient is being monitored by a sensor which senses the liquid level in the skin of diabetic and further sensor generates an analog signal of very low range (1µV-1mV) that need to be amplified for further processing. Then the role of digital celebration circuit which requires an important conversion from analog to digital signal which is being further processed to take out information and source the micro-pump to inject the insulin. Here we need a critical transformation from one signal domain to another and which must be précised according to our need for the bio-medical applications.

# Chapter 2

# INTRODUCTION

As in Universe everything that exists are analog in nature *i.e.* vary with time, but recent trends utilizes the digital signal processing for realizing the efficient and precise electronic systems. So, almost every electronic system design in today's era requires Analog-to-Digital Convertors (ADC). What we require is an efficient method for the conversion of analog signals into digital depending on requirement of the application. Various Architectures are in the market offering variations in parameters like resolutions, bandwidths, accuracies, packaging, power requirements, and temperature ranges. Most popular architectures are:

1. Flash (all decision made simultaneously)
2. Pipelined flash(with multiple flash stages)
3. Sigma-Delta (∑▲)
4. SAR *i.e.* Successive Approximation (Shift)Register

As per requirement of application (*i.e.* Biomedical Application) SAR-ADC suits the most. It provides the lower speed of operation with higher resolution and speed has a tradeoff with power *i.e.* less speed less power. Also the same circuitry is used recursively for data conversion thus saving lot of die area making system compact when compared to other high resolution ADC architectures and hence makes it cost effective.

## 2.1 SAR-ADC ARCHITECTURE

Successive-approximation A/D converters are a type of converter with feedback or cyclic converters. They are those in which the signal circulates in a closed loop, i.e. it uses the same blocks in every conversion step. This is in contrast with other type of converters, like cascade structure, where the signal proceeds from one block to the next one. In general is used to consider cyclic converters are those containing pre-subtraction. The main purpose of subtraction is first made here which is then followed by a comparison from the first estimated value. The analog input is compared with an already available VDAC. The difference voltage ε, representing the error signal, is then used to produce a new improved estimation. These estimated values are developed in the circuits of the feedback loop. According to the state of

the comparator, the block labeled “Digital Logic” has the purpose to control the counter to start counting in forward direction for a positive error signal and in a backward direction for a negative error signal. For modulo two counter, the output3 is in binary form. The DAC connected in the feedback loop now delivers the required first estimate VDAC of the input signal. In the next cycle, this value is subtracted from the input to give the error signal ε. The process is terminated after n clock cycles.

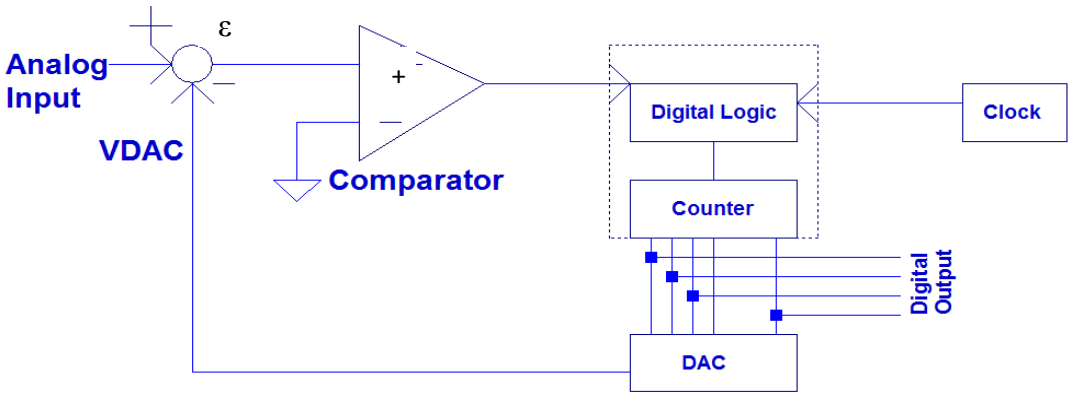



Figure-2.1 Block Diagram of SAR-ADC

However, due to circuit noise and drift, even if ε = 0, a stable state is never maintained, and the counter contents bounces up and down by one LSB in tracking the input value until conversion is stopped. Since the estimated value successively approaches the input signal until the error is diminished to a predefined value, this method is sometimes also called “servo technique” when referring to early mechanical motor-driven approach. The two blocks labeled “Digital Logic” and “Counter” become relatively simple in the case when the converter is to implement the successive approximation method, i.e. one bit per cycle. Then the two blocks essentially reduce to a Successive Approximation Register (SAR), shown in dashed lines in Fig-2.1.

## 2.2 Principle of Successive Approximation Algorithm

Initially highest bit (MSB) of the DAC is made logic 1 by the SAR logic. During the time interval from $0^{th}$ to $1^{st}$ step, the DAC output is compared to incoming analog signal. If the input is greater than the DAC output, the logic “1” at $b_N$ is permanently stored. If the input is less than the DAC output, the logic “1” is removed from $b_N$ and a logic “0” is permanently

stored in $b_N$. Then the logic "1" is applied to $b_{N-1}$. This adds ¼·VFS to the DAC output, setting it to either ¼·VFS or ¾·VFS, depending on the previous comparison. During the interval from 1st to 2nd step, the DAC output is again compared to the input signal. If the input is greater than the DAC output, the logic "1" at $b_{N-1}$ is permanently stored. If the input is less than the DAC output, the logic "1" is removed from $b_{N-1}$ and logic "0" is permanently stored in $b_{N-1}$. This sequence is repeated for each bit. The final state of all the bits will be the digital word that represents the analog input.

The successive approximation converter requires N clock cycles to complete N-bit conversion. A flow-graph for signed conversion using a successive approximation approach is shown in Figure 2.2.

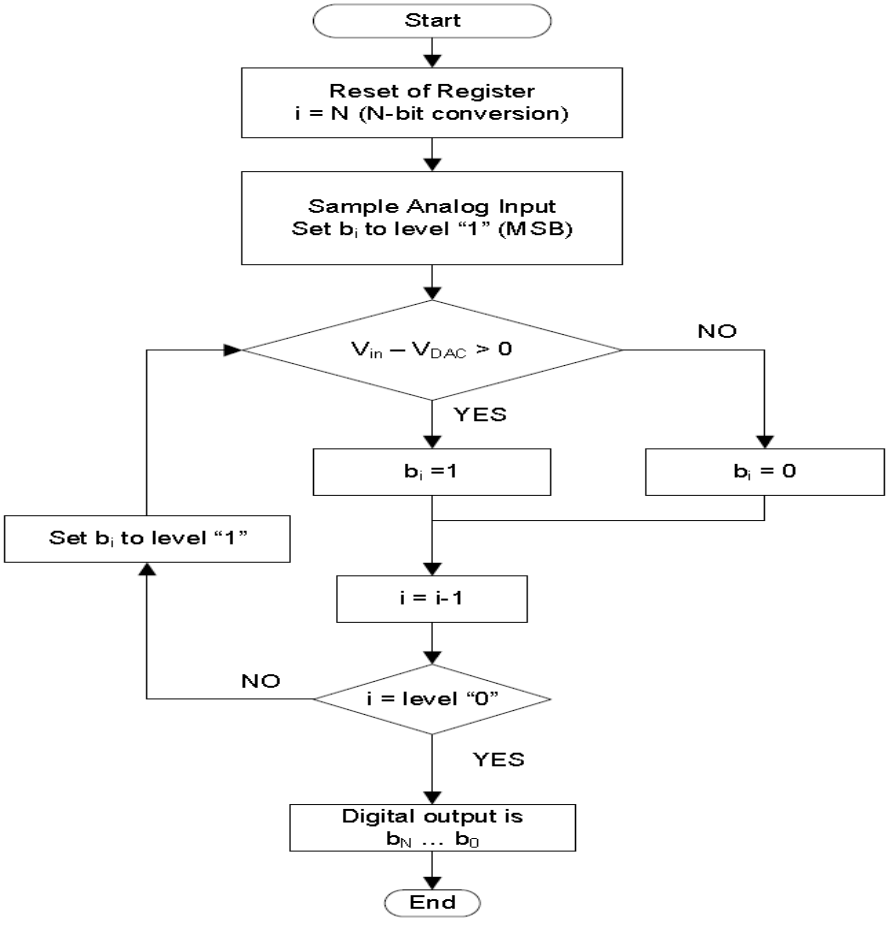



Figure-2.2 Operation principle of general N-bit SAR-ADC

## 2.3 DAC specifications

Block diagram of a DAC as shown in Fig. 2.3 where an N-bit digital word is converted into a single analog voltage. Output of the DAC is a voltage that is some fraction of a reference voltage (or current), such that

$$V_{out} = KV_{REF}D \tag{2.1}$$

Where K is a scaling factor and the digital word D is given as

$$D = \frac{D_0}{2^1} + \frac{D_1}{2^2} + \frac{D_2}{2^3} + \cdots + + \frac{D_{N-1}}{2^N} \tag{2.2}$$

Where N which is the total number of bits in a digital word and is the $i^{th}$-bit coefficient and is either 0 or 1. Therefore, the output of a DAC can be expressed by combining equations (2.1) and (2.2) to get

$$V_{out} = KV_{REF}\left(\frac{D_0}{2^1} + \frac{D_1}{2^2} + \frac{D_2}{2^3} + \cdots + + \frac{D_{N-1}}{2^N}\right) \tag{2.3}$$

Where $V_{out}$ is the analog voltage output, K is the scaling constant, and $V_{REF}$ is the reference voltage, and D is N bits wide.

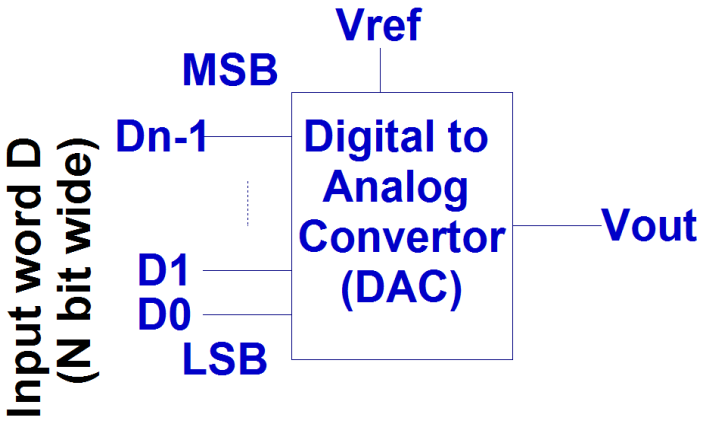



Figure 2.3 Block Diagram of Digital to Analog Convertor

### 2.3.1 Transfer curve

D versus $V_{out}$ is plotted as D is incremented from 000 to 111 for 3 bits, the transfer curve seen in Fig. 2.4 would be generated. The y-axis has been normalized to $V_{ref}$ . Various important characteristics are discussed here. It has been noticed that the transfer curve is not continuous. As the input is a digital signal, which is inherently discrete, the input signal can only have eight values and hence produce corresponding eight output voltages. If a straight line connected each of the output values, the slope of the line would ideally be one

increment/input code value. Also it has to be noted that the maximum value of the output is $7/8V_{ref}$. Since the case where digital word is equal to '000' the analog voltage should be equal 0V. 3-bit DAC can have possibly eight output voltages ranging from 0V to only 7/8 . This maximum analog output voltage that can be generated from a DAC is known as full-scale voltage ($V_{FS}$) and can be represented for any N-Bit DAC as

$$V_{FS} = \frac{2^N - 1}{2^N} * V_{ref} \tag{2.4}$$

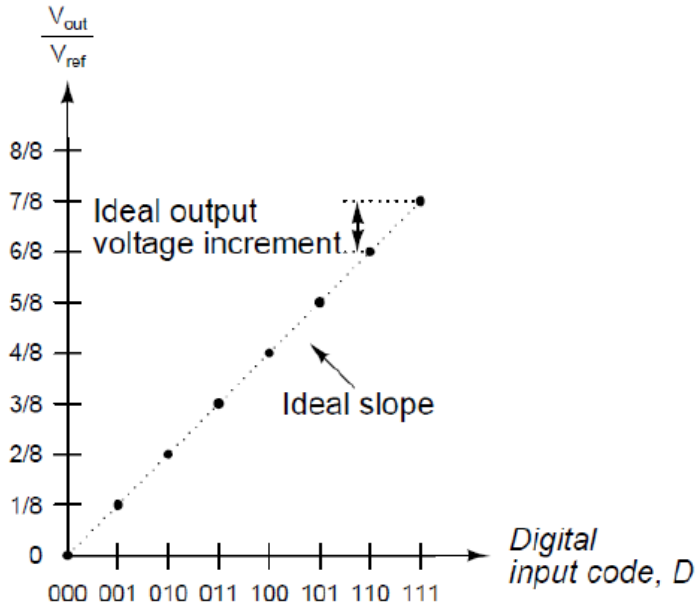



Figure 2.4 Ideal Transfer curve for 3-bit DAC

### 2.3.2 Least Significant Bit (LSB)

The rightmost value of the input digital word is known as least significant bit (LSB). The LSB defines the minimum analog voltage change at the output of a DAC. The LSB will always be denoted as D0. Unit LSB is represented as:

$$1LSB = \frac{V_{ref}}{2^N} \tag{2.5}$$

### 2.3.3 Most significant Bit (MSB)

The leftmost bit in the input digital word is called a most significant bit *i.e.* MSB. Generalizing to the N-bit DAC, the MSB would be denoted as $D_{N-1}$ . The MSB causes the output to change by $\frac{V_{ref}}{2}$.

### 2.3.4 Resolution

Smallest change in the analog voltage of a DAC with respect to the $V_{Ref}$ is known as the resolution of DAC. Resolution is typically given in terms of bits and represents the number of unique output voltage levels *.i.e.,* $2^N$ where N is the resolution.

### 2.3.5 Differential nonlinearity

Analog increments differ from their ideal variations due to non-ideal behavior of components. The difference between the non-ideal and ideal values is known as differential nonlinearity (DNL) and is evaluated as

$$DNL = max\left|\frac{V(i+1)-V(i)}{V_{LSB}} - 1\right| \quad (2.6)$$

The DNL specification measures how efficiently a DAC can generate analog LSB multiples at its output with uniformity. A DAC should have DNL less than ±½LSB to have accuracy considerably equal to N-bits. DAC with DNL more than ±½LSB is said to be non-monotonic, which means that the analog output voltage does not always increase as the digital input code is incremented. A DAC should always show monotonic behavior to fuction

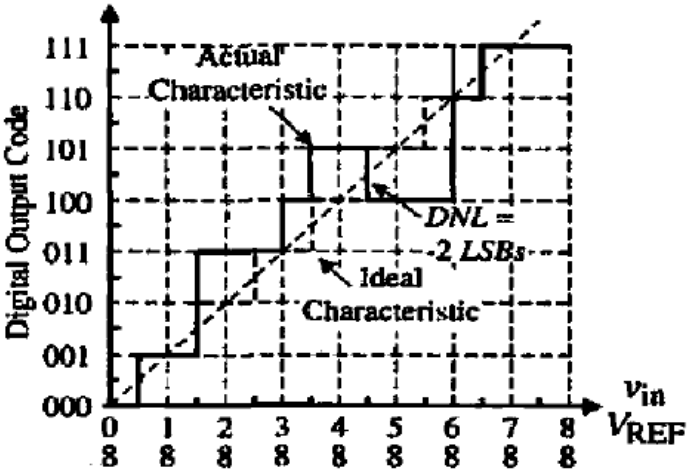



Figure 2.5 DNL Error

error free. DNL error is shown in Fig. 2.5.

### 2.3.6 Integral Nonlinearity

Integral Non-Linearity (INL) is the important static characteristic of DAC. It is defined as the maximum difference between ideal finite resolution characteristic and the actual finite characteristic measured vertically. INL defines the linearity of the overall transfer curve and is also called as running sum of DNL of a waveform and which can be defined as

$$INL - max\left|\frac{V(i)-i,V_{LSB}}{V_{LSB}}\right| \tag{2.7}$$

Practically N-Bit resolution data converter should have DNL and INL less than ±½LSB to function error free. INL Error is shown in Fig. 2.6

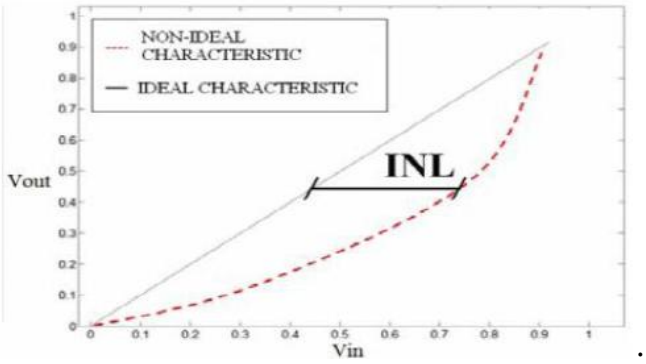



Figure 2.6 INL Error

### 2.3.7 Signal to Noise Ratio (SNR)

Signal-to-Noise Ratio (SNR) is defined as the ratio of full scale value to the rms value oof the quantization noise. In amplifier applications, this specification is typically measured using a sine wave input. For the DAC, a sampled sine wave is generated through an A/D. The SNR can reveal the true resolution of a data converter as the effective number of bits can be quantified mathematically.

$$Error\ energy: {e_{rms}}^2 = \frac{{V_{LSB}}^2}{12} \tag{2.8}$$

$$Signal\ energy: {S_{rms}}^2 = \frac{1}{2}\int_{t=0}^{t=T} A^2\, sin^2(wt)dt = \frac{A^2}{2} = \frac{2^{2N}{V_{LSB}}^2}{8} \tag{2.9}$$

$$SNR = \frac{\frac{2^{2N}{V_{LSB}}^2}{8}}{\frac{{V_{LSB}}^2}{12}} = \frac{3}{2}2^{2N} \approx (6.02N + 1.76)dB \tag{2.10}$$

### 2.3.8 Total harmonic Distortion (THD)

The total harmonic distortion is given by

$$THD = 10log\frac{{A_{2f}}^2+{A_{3f}}^2+{A_{4f}}^2+\cdots{A_{nf}}^2}{{A_{1f}}^2}[dB] \quad (2.11)$$

Five to ten harmonics are included in the THD, the rest is considered "noise"

### 2.3.9 Signal to Noise and Distortion (SINAD)

Signal-to-Noise-and-Distortion (SINAD) is the ratio of the root-mean-square (rms) signal amplitude to the mean value of the root-sum-square of all other spectral components, including harmonics, but excluding dc. SINAD is a good indication of the overall dynamic performance of a DAC because it includes all components which make up noise and distortion.

$$SINAD = \frac{S}{N+D} \quad (2.12)$$

### 2.3.10 Effective-Number-of-Bits (ENOB)

Effective number of bits can be calculated from SINAD which is more practical value as compared to SNR. Theoretically SNR of an ideal N-bit DAC can be calculated as SNR = 6.02N + 1.76[dB]. The equation can be solved for N and but SNR is replaced with the value of SINAD. Mathematically it can be represented as:

$$ENOB = \frac{SINAD - 1.76dB}{6.02} \quad (2.13)$$

# Chapter 3

# LITERATURE SURVEY

Literature survey was done on each of the SAR-ADC component respectively and they are:

1) Digital to Analog Convertor

2) Comparator

3) Digital Logic (*i.e.* Successive Approximation Register)

## 3.1 Literature Review on Digital to Analog Converter (DAC)

DAC is used as a data converter from digital input to analog output. Accuracy of ADC is very much dependent on the precision of DAC. Many architectural implementations for DAC are discussed in different references below.

### 3.1.1 R.Jacob Baker,HarryWLi,David E.Boyce, *CMOS circuit Design,Layout and simulation.* New York: The Institute of Electrical and Electronics Engineers.(1998)

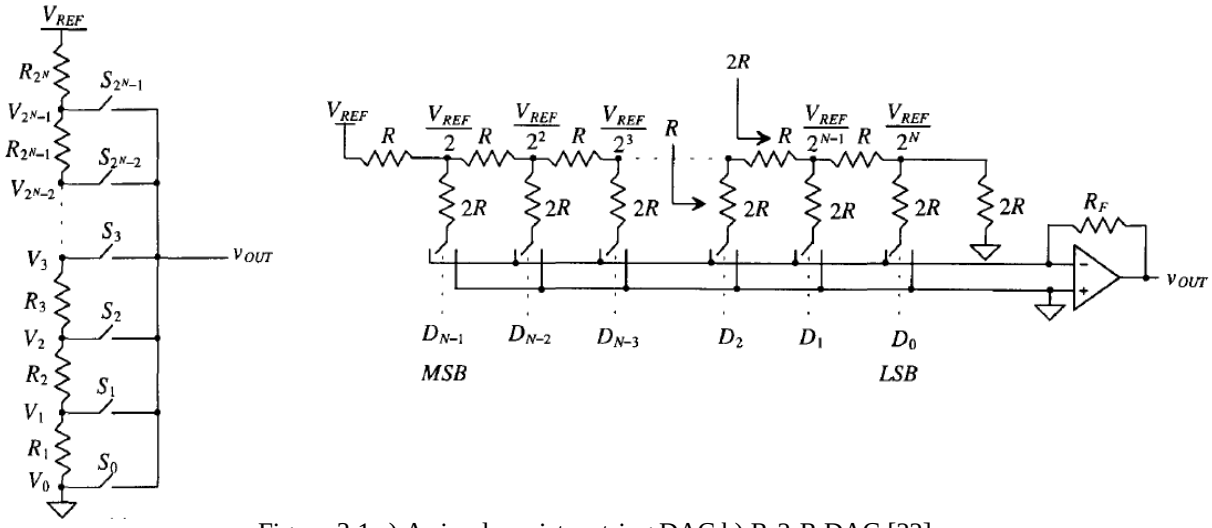



Figure-3.1 a) A simple resister string DAC b) R-2-R DAC [22]

These implementations has certain limitations like both structures utilizes large set of registers which directly affects power consumption (static power mostly) and also covers large chip area. With these implementations we would require Sample and Hold circuitry

which is being not utilized with capacitive array DAC implementation, hence saves lot of die area. So the implementations are almost obsolete specifically in application specific IC's.

### 3.1.2 A. Chandrakasan, N. Verma. An ultra low energy 12-bit rate-resolution scalable SAR ADC for wireless sensor nodes. *IEEE J. Solid-State Circuits , 42* (6), 1196-1205 (Jun. 2007).

Single-ended, instead of differential-ended, inputs can be used to greatly ease system complexity. Support of single-ended sampling is provided by means of pseudo-differential sampling, where one of the differential terminals can be set to reference ground. This approach is useful only if the common-mode signal is properly treated. This limitation can be removed by two ways:

1) Common-mode independent acquisition

2) Pre-amplifier auto-zeroing to the voltage of critical SAR decisions.

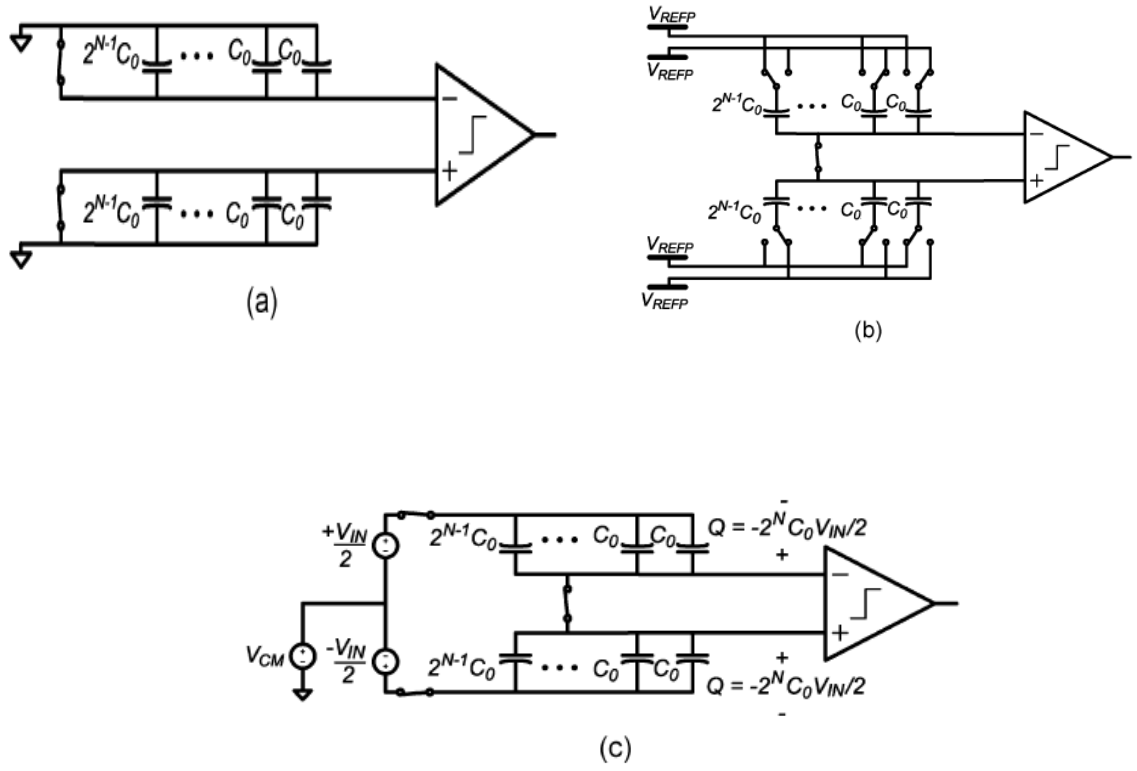



Figure-3.2 Basic capacitive array structures

Fig. 3.2(a), the capacitor arrays are purged of previous charge by shorting their top and bottom plates. Then, as shown in Fig. 3.2(b), they are switched so that an appropriate auto-zeroing reference can be generated for the comparator. Finally, input sampling is performed. During sampling, which is shown in Fig. 3.2(c), the top-plates of the differential capacitor arrays are shorted, and their voltage centered on midscale.

### 3.1.3 Andrea Agnes, Edoardo Bonizzoni, and Franco Maloberti . *Design of an Ultra-Low Power SA-ADC with Medium/High Resolution and Speed.*

To design a low power DAC is possible by avoiding the amplifiers. A possible way can be the use of switched capacitors structure which allows obtaining the right analog value at the output by switching some capacitances.

The main characteristics of this structure are that it:

- has no static power consumption;
- has a dynamic power proportional to the total capacitance used;
- has a total capacitance equal to 2N times the unitary capacitance Cu

Therefore is possible to reduce the value of the unitary capacitance for reducing the power consumption. The entire structure of capacitance can be used also as S&H block simply

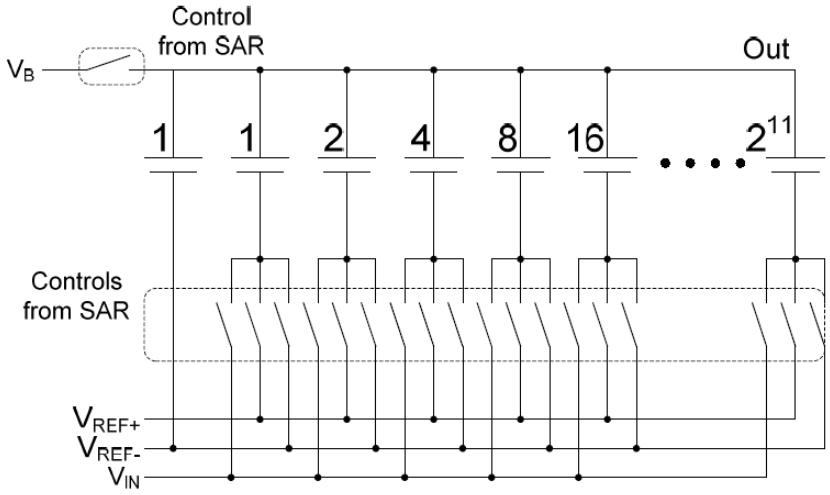



Figure-3.3 Simplified structure for DAC used as S/H as well as subtracting node [17]

sampling the value of the input signal on all the capacitance, in this way the capacitance continues to divide opportunely the reference voltages to obtain the correct value of the DAC output, but the charge accumulated on the capacitance subtract the sampled input signal from the ideal DAC output.

The design of this structure include to keep in account the usual errors introduced by capacitances. The first considered noise is the kT/C. As all the capacitances have the purpose to sample the input and then the kT/C limit impose the minimum value of the sum of all the capacitances. In particular it is necessary impose that the power of the introduced noise must be less than the power of the quantization noise, then results

$$\frac{kT}{C_{TOT}} < \frac{\Delta^2}{12}; \frac{kT}{C_{TOT}} < \frac{1}{12} \cdot \left(\frac{V_{Range}}{2^N}\right)^2 \quad \ldots (3.1)$$

sThat gives:

$C_{TOT} > 9.26\,pF$

But using this implementation for 14 bit resolution we would have:

- Large number of capacitors required which makes it massy and cumbersome.
- Large number of capacitors means large $C_{MSB}/C_{LSB}$ ratio so to implement unit capacitor ($C_U$) we would require very small capacitance as we can't increase $C_{MSB}$ after a range because of power limitations.
- So with large and heavy capacitors we are left with large power consumption and very low relative speed.

So the alternate solution is the "Bridge Solution" as shown in figure-3.4. This solution allows reducing the capacitors count as it divides the capacitive array into two parts and in between split capacitor (Cx) is placed. Maximum switching of the element on the right side array is $2^{N/2-1}$Cu while the lowest one is Cu. As the attenuation factor equal to $2^{N/2}$ due to which the maximum value of capacitor in the left side (array) is $2^{N/2-1}$Cu instead of ½Cu which allow to convert N/2 bits and LSB is represented by Cu.

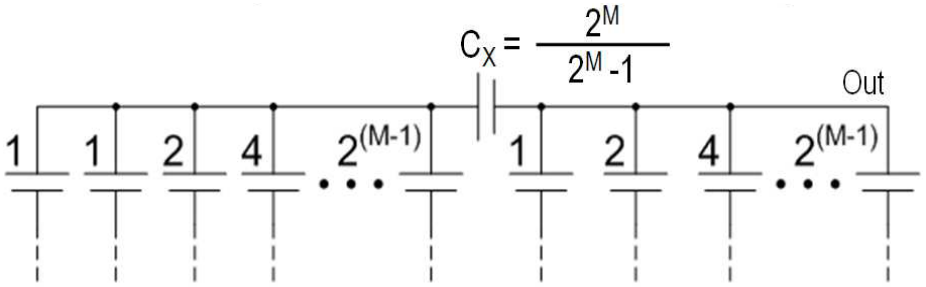



Figure-3.4 Structure of Bridge Solution [20]

Adding the capacitances the count goes from 2N down to 2 · 2N/2 − 1. Ratio of the sum of left side capacitances to the sum of the right side array capacitances including MSB must be equal to Cu *i.e.*

$$\frac{C_x \cdot 2^{N/2} \cdot C_u}{C_x + 2^{N/2} \cdot C_u} = C_u$$

that yields

$$C_x = \frac{2^{N/2}}{\left(2^{N/2}\right) - 1} \cdot C_u$$

**NOTE:**

1. As the $C_x$ is a function of $C_u$ so for accurate value a special care is required during layout.
2. Also we could only use this structure for even number of bits, as for odd its very difficult to assign precise value to $C_x$.

While its advantages like less total used capacitance means less power consumption and less silicon area diminishes its disadvantages. This means total required capacitance for 14 bit SAR-ADC is equal to

$$C_{TOT} = \left[2^{N/2} + \left(2^{N/2} - 1\right)\right] \cdot C_u = 255 C_u \qquad \ldots (3.2)$$

So this much of total capacitance is feasible, but the value of $C_x$ (which depends on $C_u$) to realize is very difficult with precision so in particular if we want to ensure a correct operation of the circuit with small value of unitary capacitance Cu. So another alteration can be done

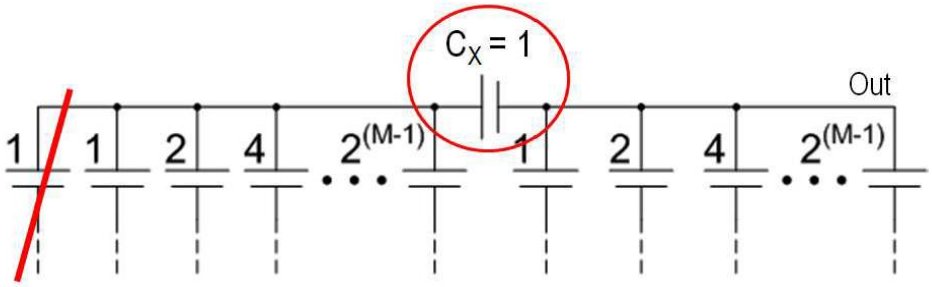



Figure-3.5 Modified capacitive array structure for DAC [20]

with the capacitance array structure to make $C_x$ realizable is to make equal to unitary capacitance (i.e. $C_u$). So a little modification could be made in the array structure in order to unitize the bridge capacitor is as shown in Figure-3.5.

This solution with modified bridge architecture has the main advantage of to reduce the problem in ratio between capacitances because also the attenuation capacitance is equal to unitary capacitance. But this solution doesn't realize the perfect DAC characteristic; in fact it introduces some errors (gain error). Total capacitance for this structure is:

$$C_{TOT} = \left[2 \cdot \left(2^{N/2} - 1\right)\right] \cdot C_u$$

Which gives: $C_{TOT} = 254 \cdot C_u$ for 14 bit (7 +7) solution. … (3.3)

As we have seen the imposed limitation on $C_{TOT}$ form Eqn.12 that give minimum value of Cu= 36.5 fF (using Eqn. 3.3)

The mismatch, instead, must be particularly precise because the attenuation capacitance realizes a factor of multiplication of the error. In particular the factor is equal to $2^{N/2}$, which implicates to require a unitary capacitance equal at least Cu= 360 fF. So for the safety margin we will take Cu=500fF which make total capacitance utilization:

$C_{TOT}$ = 254×500 fF = 127 pF

Now we can estimate the power consumption for 14-bit DAC.

For DAC:

$$P_{DAC} = f_s \cdot \sum_{i=1}^{14} E_i \cong f_s \cdot \frac{1}{2} \cdot C_{TOT} \cdot V_{ref}^2$$

⇨ $P_{DAC}$= 20.574 µW ( for $f_s$=100KS/s proposed)

For initial sampling step:

$$P_{Sample} = f_s \cdot E_S = f_s \cdot \frac{1}{2} \cdot C_{TOT} \cdot \left(\frac{V_{ref}}{2}\right)^2$$

⇨ $P_{SAMPLE}$= 5.1235 µW

Thus approx. total power consumption would be:

$P_{TOT}$= 25.715 µWatt

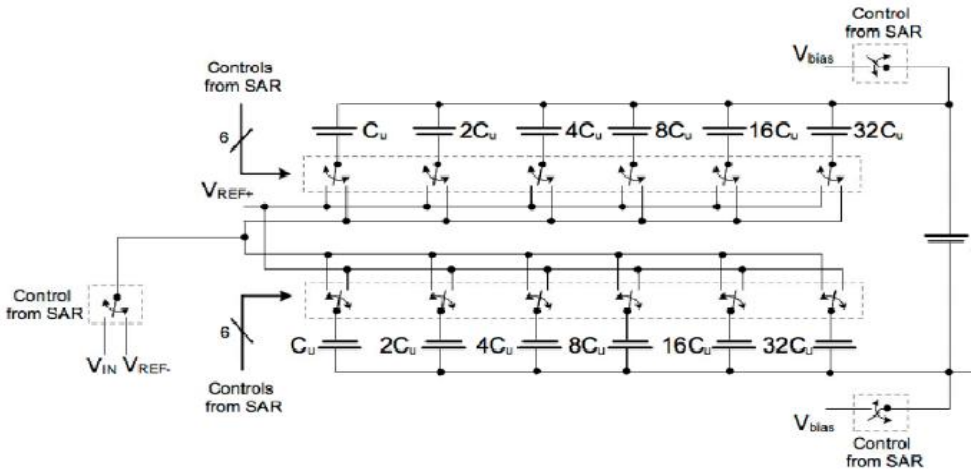



Figure-3.6 Complete DAC structure with Sample and Hold and subtraction node [10]

## 3.2 Literature Review for Comparator

The next basic building block taken in consideration is the comparator. The main function of a comparator is to deliver an output voltage which represents the results of a comparison between two voltages at its input.

### 3.2.1 Barot, N.. *Successive Approximation Analog to Digital Converter.* San Jose State University (30 April 2010).

Comparator compares the two analog input voltages and gives the digital output *i.e* either logic '1' or '0'. The output of the comparator is high *i.e.* '1' (or $V_{OH}$) when the difference

between the input terminals is positive. The output is low *i.e.* '0' (or $V_{OL}$) when the difference is negative, which clearly shown in figure 3.7.

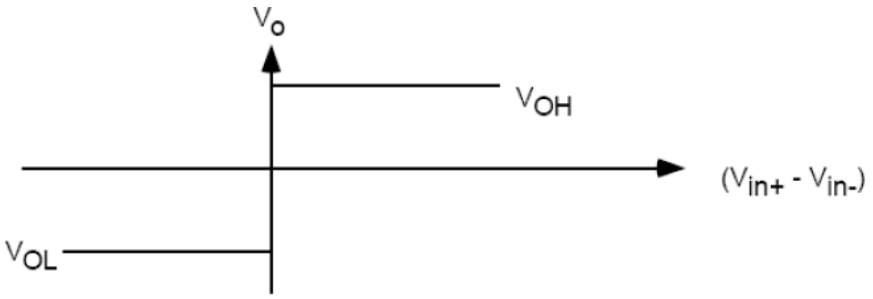



Figure-3.7 I/O characteristic of a comparator [21]

Ideally output of comparator is defined as

$$V_o = \begin{cases} V_{OH}\ if\ (V_{in+} - V_{in-}) > 0 \\ V_{OL}\ if\ (V_{in+} - V_{in-}) < 0 \end{cases}$$

Here reference voltage is 0V but not always, and we can see infinite gain but practical it is not feasible and instead we have finite gain as shown in figure-3.8.

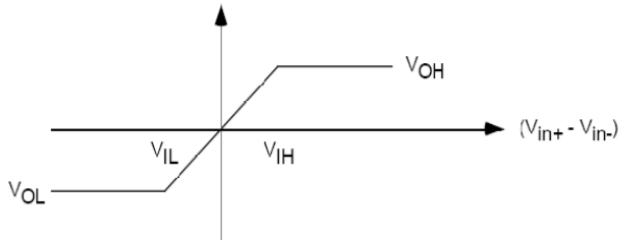



Figure-3.8 I/O characteristic of a comparator with finite gain [21]

We have

$$V_o = \begin{cases} V_{OH} & if\ (V_{in+} - V_{in-}) > V_{IH} \\ A_V\ (V_{in+} - V_{in-}) & if\ V_{IL} < (V_{in+} - V_{in-}) < V_{IH} \\ V_{OL} & if\ (V_{in+} - V_{in-}) < V_{IL} \end{cases}$$

The transition from logical "0" ($V_{OL}$) to logical "1" ($V_{OH}$) is not precise in practical comparators, but rather it has a finite width of uncertainty due to the finite gain of the circuit (gain error), which put a limit on the number of admissible comparison levels (resolution).

Slew rate is another important parameter of comparator. Slew rate is inversely proportional to the input voltage of comparator. Input offset is another important non-ideal parameter of comparator. The output of comparator is constant until or unless input voltage difference reaches the input offset voltage Vos.

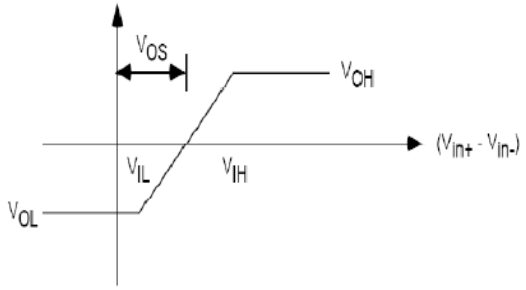



Figure-3.9 I/O characteristic of a comparator with finite gain and offset error [21]

Transfer characteristic of comparator with respect to input offset is shown in figure 3.9. The output is defined as follows:

$$V_o = \begin{cases} V_{OH} & if\ (V_{in+} - V_{in-}) > V_{IH} \\ A_V\ (V_{in+} - V_{in-}) - A_V\ V_{OS} & if\ V_{IL} < (V_{in+} - V_{in-}) < V_{IH} \\ V_{OL} & if\ (V_{in+} - V_{in-}) < V_{IL} \end{cases}$$

The structure of a comparator is similar to that of an operational amplifier only difference is that it comparator is operated in two extreme states logic "1" or logic "0" i.e. they are operated in either saturation or cut off region, which means there are over driven most of the time. So a special care must be taken for the adverse effect of overdrive. On the other hand, the response time or delay is more important than the bandwidth. Accuracy is further determined by offset voltage and voltage drift, as well as by offset current.

### 3.2.2 Yan Zhu, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Rui Paulo Martins, and Franco Maloberti. A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS. *IEEE JOURNAL OF SOLID-STATE CIRCUITS , 45* (6) (JUNE 2010).

Usually, the conventional scheme used to realize a low power comparator is done in Figure-3.10.

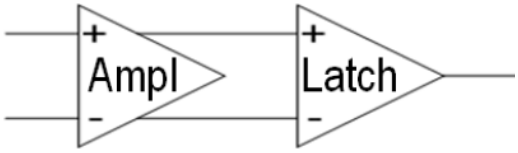



Figure-3.10 Typical realization of comparator [20]

The latch has the purpose to saturate its output voltage to VDD or VSS according to its inputs. In general a latch has the main purpose of the comparator, but it can response correctly only if its input differential voltage is enough large (typically > 20mV) to ensure the right accuracy in its operation. To overcome this limit is usually used to apply a preamplifier before the latch which has the purpose to amplifier the input signal. In our case it is necessary to use because the LSB is 700µV and then the required gain of the preamplifier must be at least 28.57 which means 33.52dB. A typical circuitry for comparator (preamplifier and dynamic latch) is shown in figure-3.11.

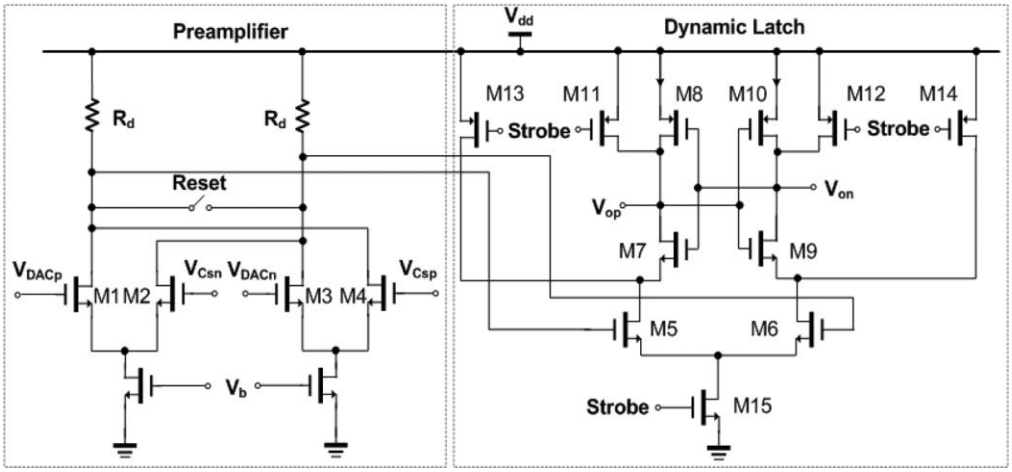



Figure-3.11 Comparator with the different stages [12]

So here we can see that we have a large numbers of driving MOS as an element which would consume power from 1.8V supply and as we have the dynamic operation (i.e. pre-charge and pre-discharge) which further increases power consumption which is well beyond our application requirement.

**3.2.3 Andrea Agnes, E. B. A 9.4-ENOB 1V 3.8µW 100kS/s SAR ADC with Time-Domain Comparator. *ISSCC 2008 / SESSION 12 / HIGH-EFFICIENCY DATA CONVERTERS / 12.5* (2008).**

Other concept could be used i.e. using the time domain instead of the voltage domain operation by using two voltages to time comparator and a logic which compares the time delays. The timing diagram shows the behavior of the $\Phi_S$ and the reference voltage $V_B$ and shows also how the digital output changes depending on the input signal.

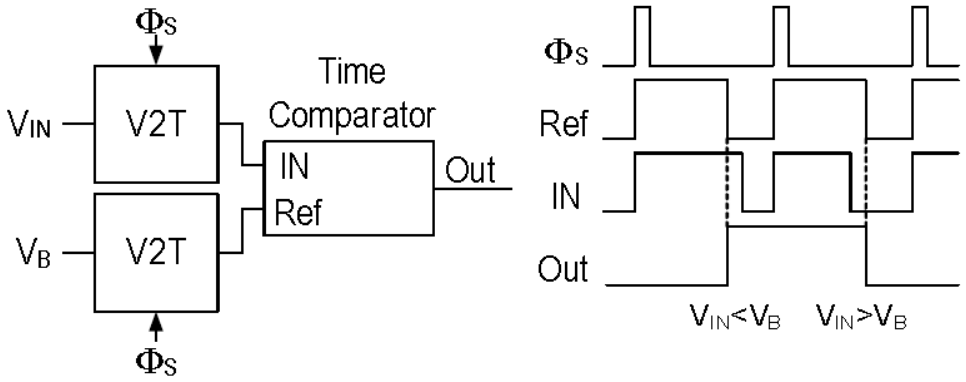



Figure-3.12 Block and Timing diagram of comparator [20]

The function of the block called "V2T" is to convert the amplitude of the input voltage into delay time from the raise edge of the clock. The next block, in cascade with the two V2T has the purpose to compare the delay times and choice if the V2T referred to input voltage is faster or slower than the V2T taken as reference. Then the output of the comparator (Out) is equal to logic level "1" or "0" according with the amplitude of $V_{IN}$ is less or more than reference voltage $V_B$ respectively. The schematic diagram for V2T (Voltage to time converter) is as shown in figure-3.13.

The supply voltage is VDD=1.8V to ground. When the phase $\Phi_C$ is low, the transistors M1, M4 and M6 are ON while the transistors M2, M3 and M5 are OFF. Therefore the initial conditions include that the capacitance C is charged to VDD and the parasitic capacitance $C_P$ is completely discharged. The input voltage $V_A$, applied on gate of transistor M3, is a constant voltage during each single conversion. The conversion starts when $\Phi_C$ is raised and the initial step is the V to I conversion by transistors M1, M2, M3 and the resistance RD,

which work as a constant current generator. This current is used to discharge the capacitor C, and then it has a constant discharge. When the voltage $V_C$, across the capacitor, falls below the threshold of transistor M5, the output of entire V2T raises. The presence of some inverter at the output has the only purpose to obtain a square wave with good edge in transitions.

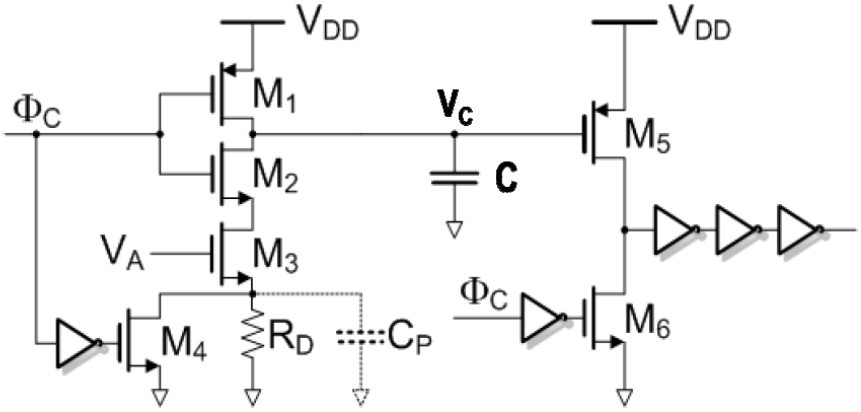



Figure-3.13 Schematic of Voltage to Time convertor (V2T) [10]

For the used configuration Td (given time) is inversely proportional to the input voltage. M4 discharges the parasitic capacitance $C_P$, and initial charging of $C_L$ is given by series connection of $C_P$ and $C_L$. Hence, voltage $V_C$ immediately falls to $V_{CF}$

$$V_{CF} = V_{DD}\frac{C_P}{C_L + C_P}$$

Hence, $C_L$ is discharged with the constant rate. The initial drop of $V_C$ positively reduces the Td but the discharging current remains almost constant. Splitting $C_L$ in two parts, $C_{L1}$ and $C_{L2}$, enhances the drop.

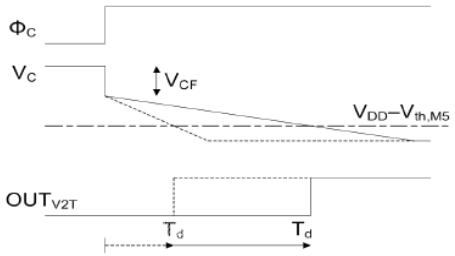



Figure-3.14 V2T main signal waveform [17]

The next step is the design of the block which realizes the time comparator. The operation principle of this block is to determine which signal is the first to raise. A simple method to

implement this algorithm is the use of a Delay Flip Flop (DFF). In fact if we connect the output of the V2T correspondent to the input signal to the input called “D” of the flip flop and the output of the other V2T to the input called “Clock” of the flip flop then we will obtain a right time comparison.

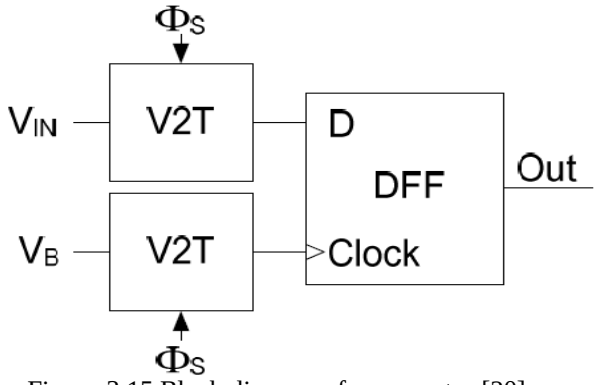


Figure-3.15 Block diagram of comparator [20]

The operation of the DFF is to copy to its output the assumed value of the D input in the same instant of time when the Clock signal raises. In this configuration, naturally, the value of reference voltage VB ensures the edge at the output of its V2T, while the output of the V2T correspondent to the input signal can raise before or it is able not raise. This way doing, when the Clock signal raises “read” the value of the D signal, and then if D signal raised before the output becomes “1”, while if D signal still has to raise the output becomes “0”. The implementation of this block with a simple DFF introduces only the errors referred to the respect the hold or the setup time to ensure the correct operation of the flip flop. Therefore the complete comparator adopted for this application will be as shown in figure-3.16.

### 3.3 Literature Review for Digital Logic (S.A.R.)

The main functions of digital logic is to memorize the sequence of bit output from comparator and realize the successive approximation algorithm for proponing the right sequence of data to DAC.

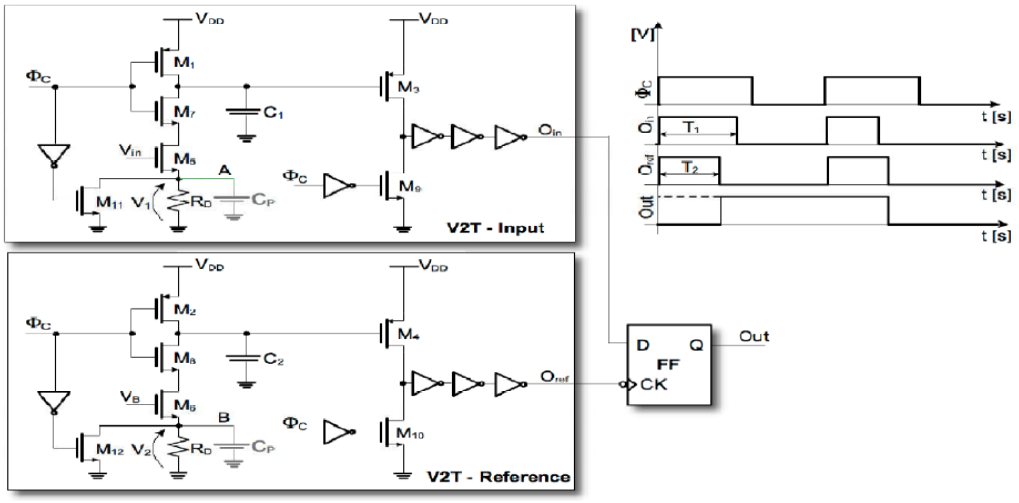



Figure-3.16 Comparator schematic and timing diagram adopted for our application [10]

### 3.3.1 Tesi di Dottorato, A. A. *Very Low Power Successive Approximation ADC for instrumentation application.* UNIVERSITÀ DEGLI STUDI DI PAVIA (2008-2009).

In order to realize these functions, the digital logic is divided in same functional blocks as shown in Fig. 3.17. The block called "Phase Generator" has the purpose to indicate to the "logic" on which bit the comparator is working, the "logic", instead, is the mind of successive approximation algorithm, ending there is the "PIPO Register" which has the function to sample the digital word at the end of conversion and hold it for all time required by the successive conversion steps.

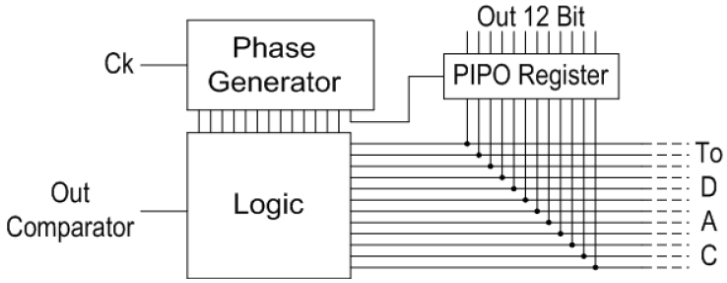



Figure-3.17 Main functional block in SAR Digital Block [20]

The realization of each block will be done by full custom design. In particular the "Phase Generator" will be designed with a cascade of DFF in series, as shown in Fig. 3.18. This structure has the purpose to indicate on which bit the converter is working.

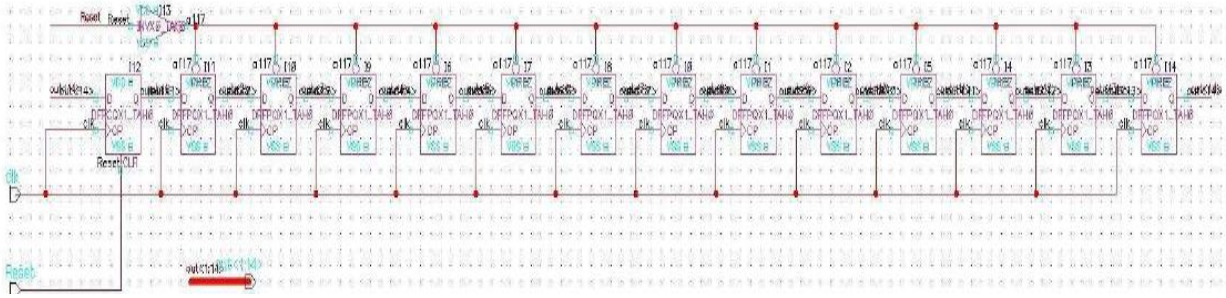


Figure-3.18 Chain if D-Flip Flop to generate a cyclic counter in one hot [20]

To obtain this goal there is an initial phase of reset during which all the DFF except the first one are set to logic level “1”, while the first one is set to “0”. During next steps the DFF continues to ‘transfer’ the “0” from 1st to 2nd, and then from 2nd to 3rd, and then from 3rd to 4th, and so on. When the 16th is “0” then the transfer is done means that the first sample is ready and then it is possible to transfer from 16th to 1st for restarting the transfer from the 1st to the other and obtaining another sample of the input. This principle of operation is like to have a counter with 14 bit and continually to count from 1 to 16 with one hot system.

The “Logic” block can be realized with twelve identical cells which have two main purpose: 1. to set respectively bit to logic level “1” when start its phase, 2. to copy the output of the comparator as soon as it have finished its comparison. The realization of a simple cell of these ones is based on the Set-Reset Flip Flop (SRFF), as shown in Fig. 3.19. The correspondent output of the “Phase Generator” enters in the pin called “NOT_Phi”, and then, as soon as that pin becomes “0” the SRFF set to “1” its output. The signals “Comp” and “Comp_ready” are the signal which indicate when the comparator is working and when the output of the comparator is ready respectively. In this way, if the all the signal confirm that the bit is the right one, the comparator is ready and its output is right, then the signal reset of the SRFF follows the comparator, which enters in the cell by pin called “Sampl”. Reset should not operate and the output is kept to “1”, while if “Sampl” is “0” the Reset should operate and the output is resettled to “0”.

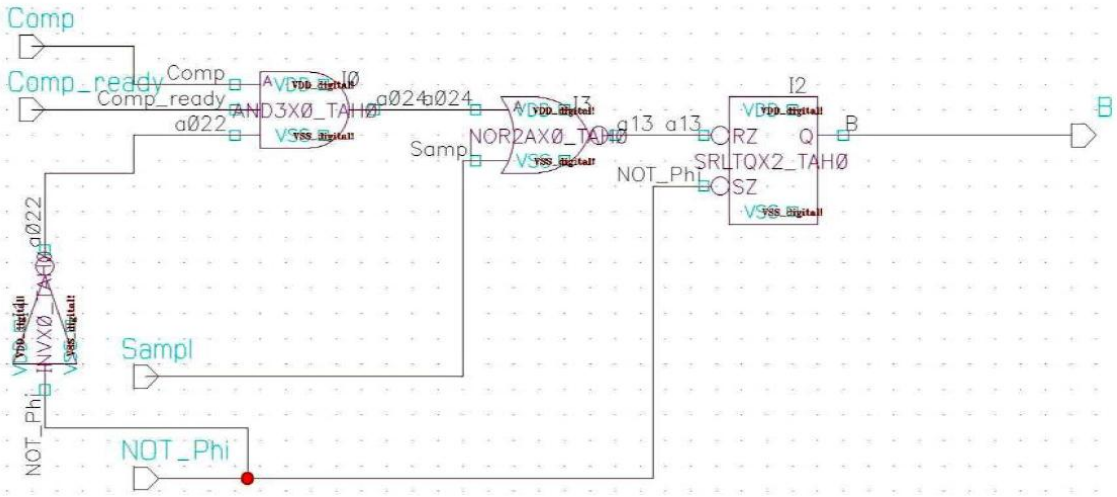



Figure-3.19 Schematic of one of the fourteen cell block "LOGIC" [20]

The last cell to design is the PIPO register, but it is realized with basic technique with 12 DFF which work in parallel, as shown in Figure-3.20.

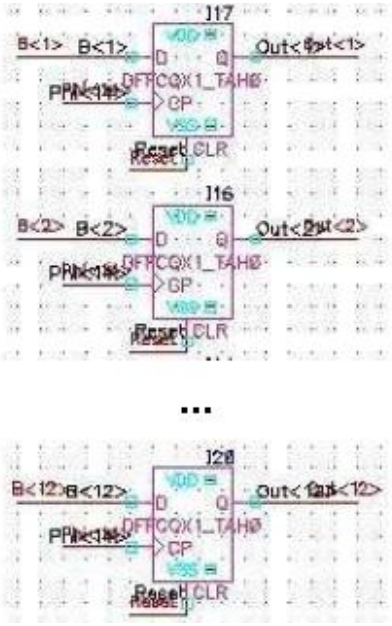



Figure-3.20 PIPO Register realized with D-Flip Flop [20]

Performance comparison of different SAR-ADC's designed in 180nm technology is described in Table1.

**Table 1: Performance comparison of the SAR-ADC in 0.18µm technology**

| Reference Year | [1] 2003 | [2] 2007 | [3] 2009 | [4] 2011 | [5] 2011 | [6] 2011 | [7] 2012 | [8] 2007 |
|---|---|---|---|---|---|---|---|---|
| **Resolution** | 8 | 8 | 10 | 10 | 10 | 10 | 10 | 12 |
| **Sampling Rate (kS/s)** | 4.1 | 200 | 100 | 1000 | 1 | 100 | 200 | 100 |
| **Power(µW)** | 0.850 | 2.47 | 1.3 | 7.16 | .0025 | 1.3 | 1.04 | 25 |
| **Supply voltage(V)** | - | | | 0.9 | 0.5 | 0.6 | 0.6 | 1 |
| **ENOB** | 6.9 | 7.44 | 8.7 | 8.4 | 8.52 | 9.3 | 9.34 | 10.5 |
| **DNL( LSB)** | - | 0.53 | - | - | - | - | - | 0.16 |
| **INL( LSB)** | - | 0.9 | - | - | - | - | - | 0.19 |
| **FOM (fj/step)** | 1700 | 65 | 31 | 21.56 | 6.8 | 21 | 8.03 | 172 |

# Chapter 4

## Design of 6-Bit SAR-ADC

A 6-Bit SAR-ADC is implemented just to get familiar with the operational behavior of components of SAR-ADC. Same design considerations were assumed as discussed in the literature review for SAR-ADC implementation. 0.8MHz clock speed was used for sampling and normal operation of SAR-ADC components. Vdd equal to 1.8V and Vss is taken as ground potential. Technology used is 180nm. Each component was designed first and then they were integrated to operate as a complete SAR-ADC.

### 4.1 Design of Digital to Analog converter (DAC)

Capacitive 6-bit DAC is implemented and this DAC serves the two operations:

1. Sample and Hold operation: Input is fed to the capacitive DAC through the transmission gate (as a switch). When switch is on, input is sampled on to the all six capacitors of DAC and when off, it is in hold state during which SAR-Algorithm is applied on to the DAC bits.

2. Subtracting Node: During the hold mode when Binary Search algorithm is implemented on the bits of DAC, the input is subtracted successively from the voltage level corresponding to each bit of DAC applied by the SAR-Cell. As when input is sampled the charge on each capacitor correspond to the voltage level of ($V_B$-$V_{IN}$), where $V_B$ is bias voltage same as taken as reference for comparator.

Structure of 6-bit DAC that has been implemented is shown in figure-4.1. This DAC is working as S/H circuit and subtractor.

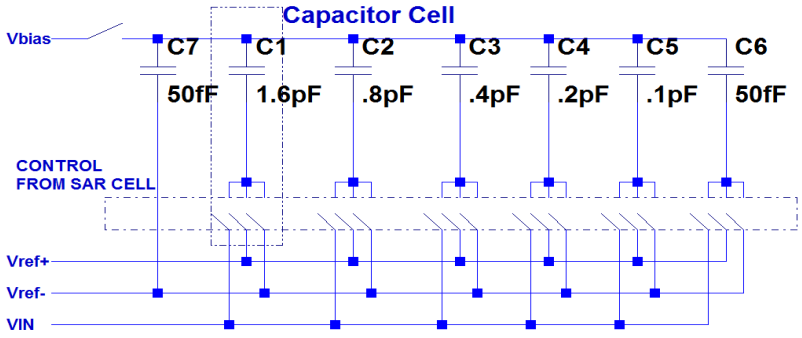



Figure-4.1 Structure of 6-bit DAC

All the switches here with in architecture are implemented by using transmission gates with PMOS AR (.54µm/.18µm) and NMOS with AR of (.27µm/.18µm). Switching action is being controlled by SAR-Cell working on binary search algorithm.

### 4.1.1 Capacitive Cell

Working of capacitive DAC can be well explained by operation of single capacitive cell as shown in Figure-4.2.In this cell two transmission gates are used and operated as a 2:1mux. For the first clock pulse SAR-Cell provide logic '0' and thus this first transmission gate (TG) becomes 'ON' and samples the $V_{IN}$ on to the capacitor, which is also at $V_{BIAS}$ potential for the same clock period only. Thus capacitor is charged to voltage ($V_{IN}$ -$V_{BIAS}$).

With the next clock pulse input SAR_Cell becomes logic '1' thus the next TG operates and now $V_{REF+}/2$ is applied to capacitor (if capacitor corresponds to MSB of DAC otherwise applies corresponding charge). Suppose if SAR_Cell has decided to make this bit logic '0' then TG one will still remain active and capacitor is discharged to $V_{REF-}$. There will be five more capacitors in parallel controlled by SAR_Cell for successive clock pulses.

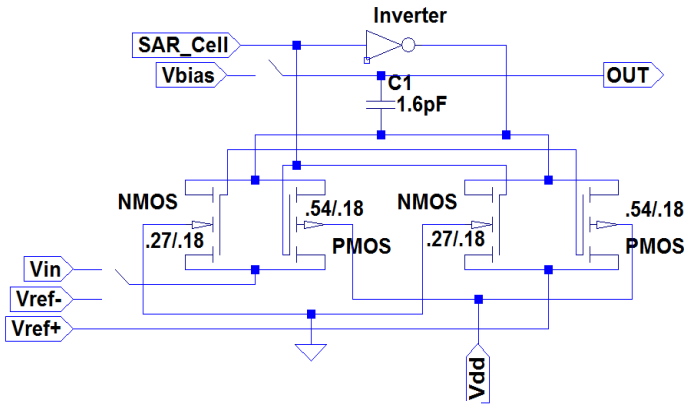



Figure-4.2 One Bit Capacitive Cell

### 4.1.2 Noise Limitation

Noise plays important role by limiting the performance of any analog device. In DAC thermal noise put the limitation on the minimum value of the capacitor i.e. unit capacitor and also limited by the technology (180nm) to the minimum of 30fF. So to calculate minimum value of unit capacitor kT/C noise plays crucial role. Minimum unit capacitor ensures us the minimum power consumption and minimum on-chip area.

Total capacitance of 6-bit DAC is calculated as:

$C_{TOT} = C + 2C + 4C + 8C + 16C + 32C + C = 64C$ … (4.1)

Also, $\frac{kT}{C_{TOT}} < \frac{\Delta^2}{12}; \frac{kT}{C_{TOT}} < \frac{1}{12} \cdot \left(\frac{V_{Range}}{2^N}\right)^2$

$C_{TOT} = 0.25122fF$ … (4.2)

Thus comparing (4.1) and (4.2), we get:

C = 0.003925fF

As technology limits us to minimum value of 30fF and we take 50fF as our unit capacitor value just for safety margins.

⇨ $C_u = 50fF$

### 4.1.3 DC Input operation of 6-Bit capacitive DAC

Architecture that has been analysed for DC input voltage of 1.8V is shown in Figure-4.3.

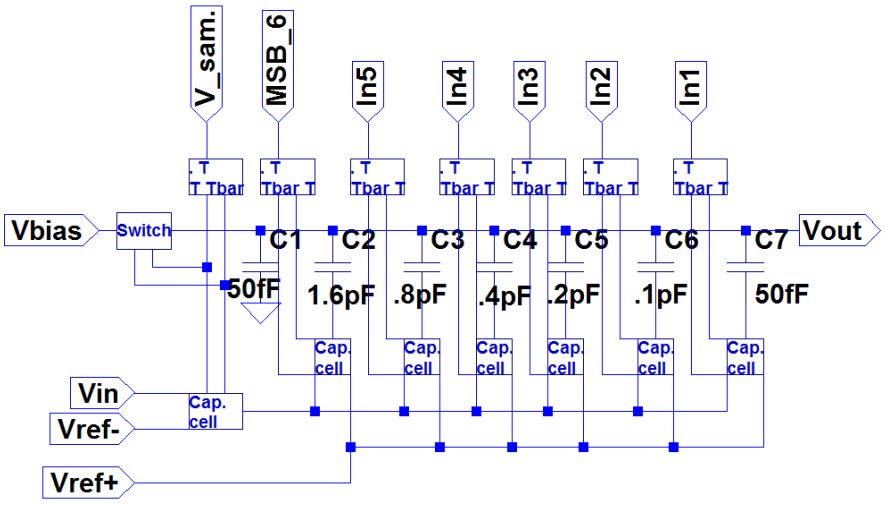



Figure-4.3 Architecture of 6-bit DAC analyzed.

For DC analysis:

$V_{in} = 1.8V$, $V_{bias} = 1.8V$, $V_{ref+} = 1.8V$ & $V_{ref-} = 0V$

During sampling phase input V_sam is given logic '0' from SAR_cell for first clock cycle and thus the input is sampled onto all the capacitors to voltage ($V_{IN}$ -$V_{BIAS}$). With next clock pulse logic '1' is provided on bit MSB_6. Thus the bottom plate of capacitor is connected to

$V_{ref+,}$ adding $V_{ref}/2$ potential on capacitor C2. Similarly logic one applied on to next adjacent capacitor with successive clock pulses.

After sampling for consecutive 7 clock periods logic '111111' is applied to all data bits (as shown in Figure-4.4) because input is 1.8V so as the reference voltage the output must increment periodically with clock pulses to max of 1.8V which corresponds to $V_{bias}$ at the output. Hence the subtraction is being performed.

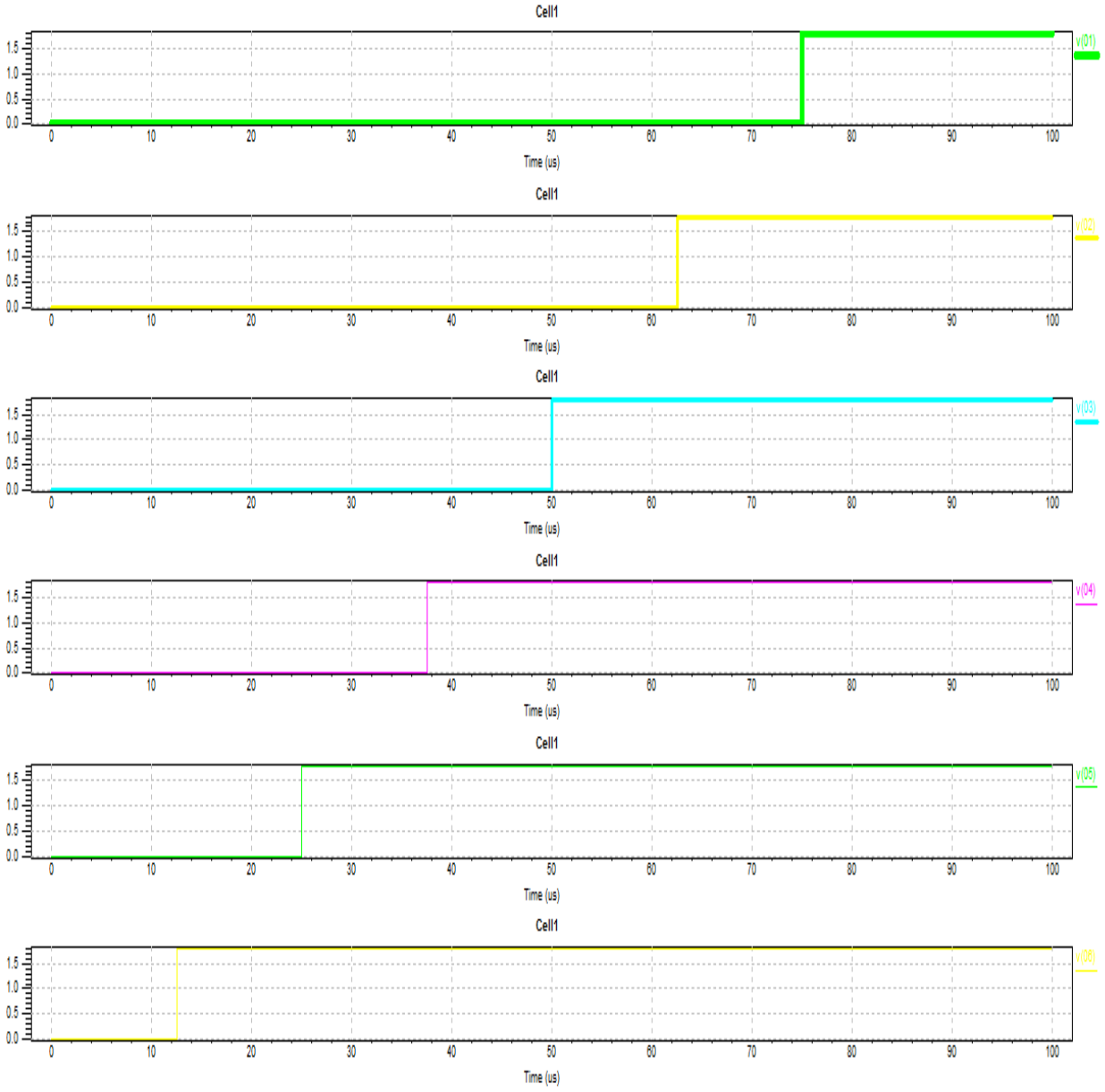



Figure-4.4 Digital input applied to DAC corresponds to '111111'

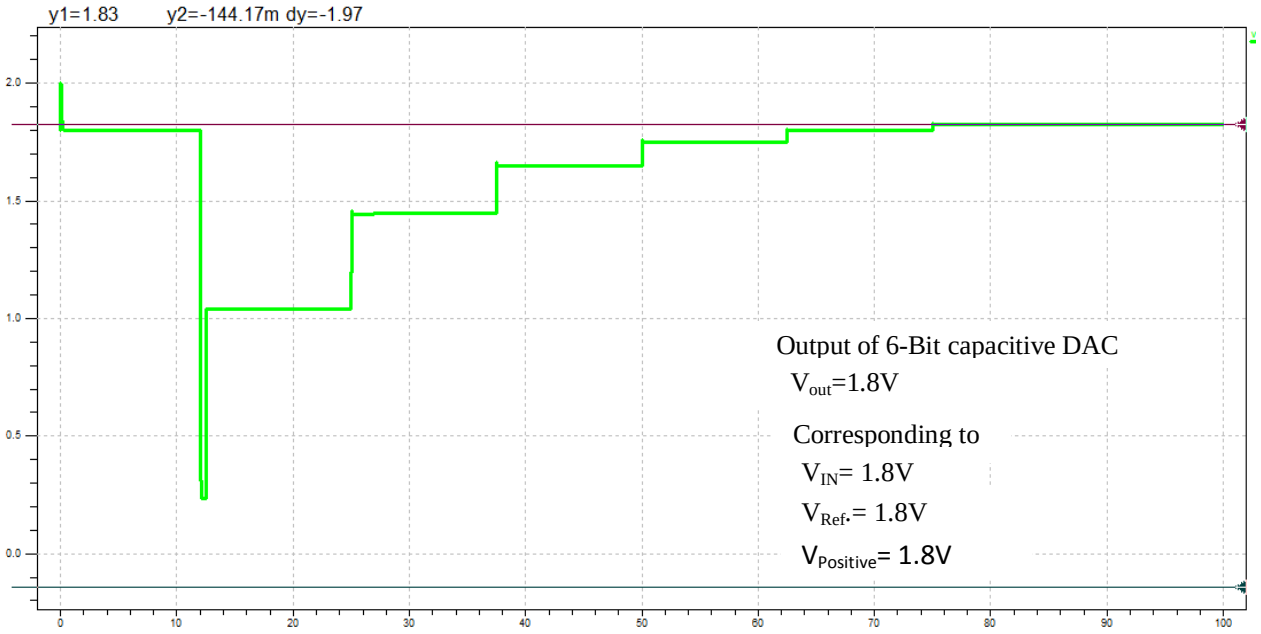



Figure-4.5 Output waveform of DAC

### 4.1.4 AC Input Operation of 6-Bit Capacitive DAC

For AC analysis of 6-bit DAC we need to select the input voltage frequency, maximum voltage swing and input supply offset. The circuit is working for 6 –bit resolution thus total of operational stages becomes six i.e. 6-bit operation of DAC, one for sampling and one for EOC (end of conversion). With EOC signal the digital output is stored in the registers. As for design consideration we had fixed our sample rate to 100kS/s. Thus maximum operating frequency becomes 0.8MHz.

Consideration:

$V_{INp\text{-}t\text{-}p}$ = 0.9V with 0V offset and maximum frequency 50 KHz (with in Nyquist criterion).

$V_{ref+}$= 1.8V and $V_{bias}$=0.9V

For the first clock cycle when input is applied to the DAC for sampling, the DAC capacitors are charged to potential ($V_{IN}$ -$V_{BIAS}$). Since from the simulation waveforms we can see that 0.35V of input is sampled on to the capacitors. Thus the SAR_Cell must provide the equivalent digital logic on the in bits of DAC. For 6-bit DAC and with 1.8V $V_{ref+}$ the logic must be '001100'. Hence the same logic input is provided corresponding to 0.35V and the output converges to the $V_{bias}$ i.e. 0.9V as shown in simulated waveforms in Figure-4.6.

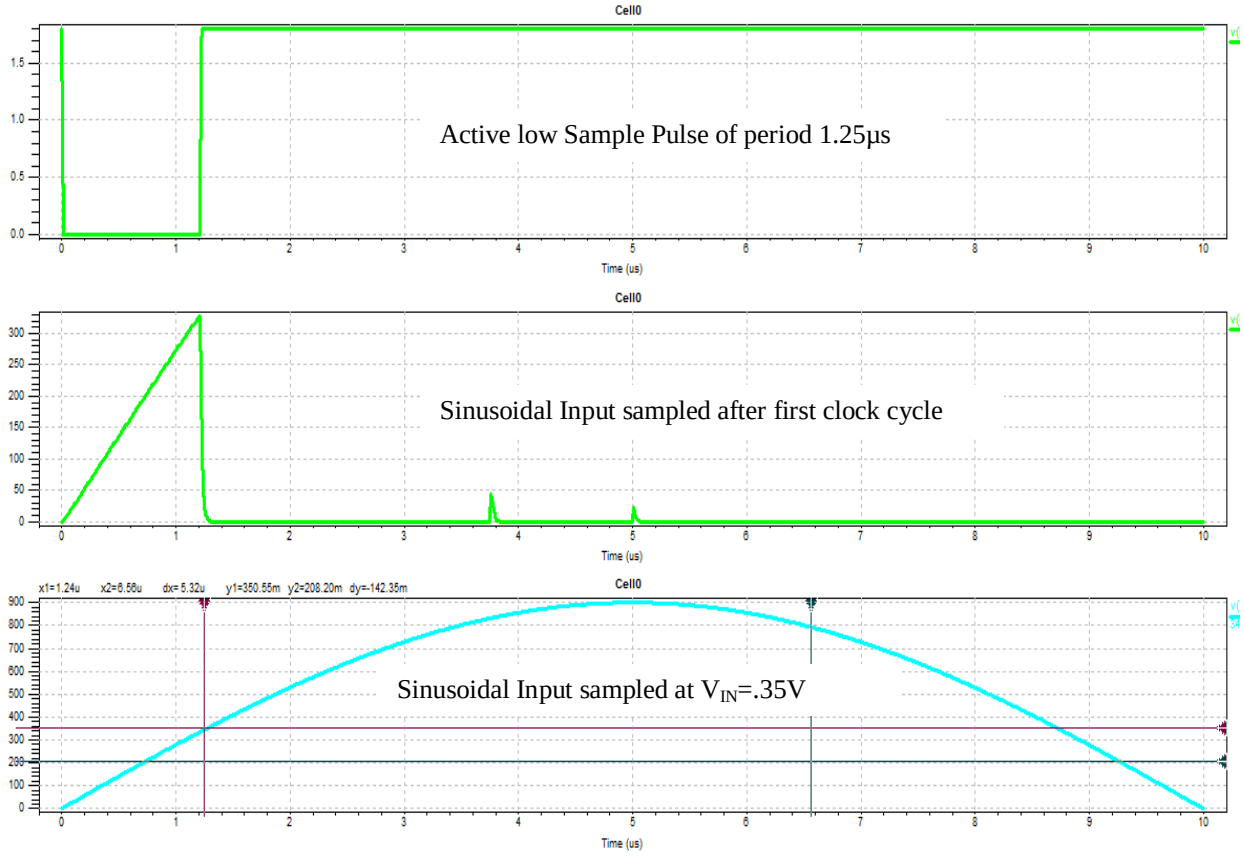



Figure-4.6 a) Sampling pulse b) sampled input c) input applied to DAC

First waveform represents the sampling cycle which comes from the SAR_Cell (phase generator) corresponds to first clock cycle out of eight and the next waveform represents part of the input signal that coupled to the plate of capacitors. The last waveform is the input signal with 0.9V peak to peak with zero offset. Analyzing we get that the input is sampled at 0.35V corresponding to time 1.24µs which is first clock period for SAR-ADC. From the output waveform we see $V_{out}$ comes to be 0.9V which is expected and shown in Figure-4.7.

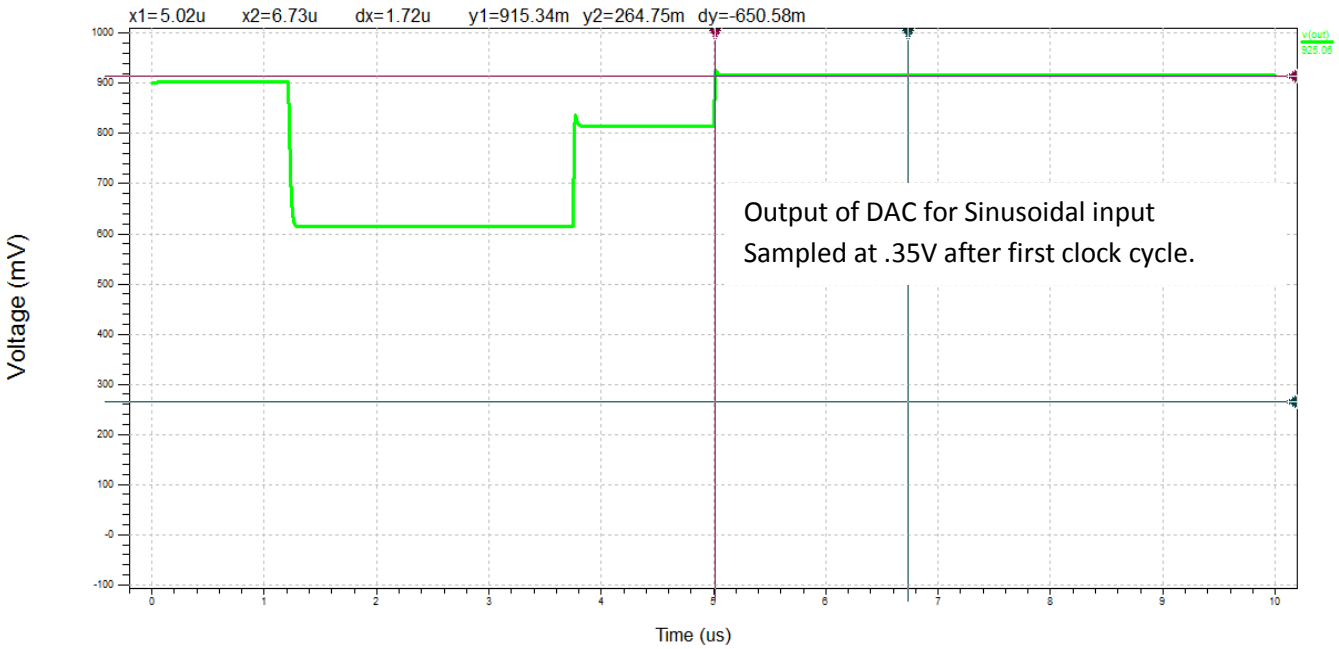



Figure-4.7 Output waveform of AC analysis

## 4.2 Design of Comparator

Comparator is a component that compares two analog signals and provides the digital output. In this work time domain comparator is implemented instead of voltage domain operation by using two voltages to time comparator and a logic which compares the time delays. The timing diagram shows the behavior of the $\Phi_S$ and the reference voltage $V_B$ and shows also how the digital output changes depending on the input signal.

The function of the block called "V2T" is to convert the amplitude of the input voltage into

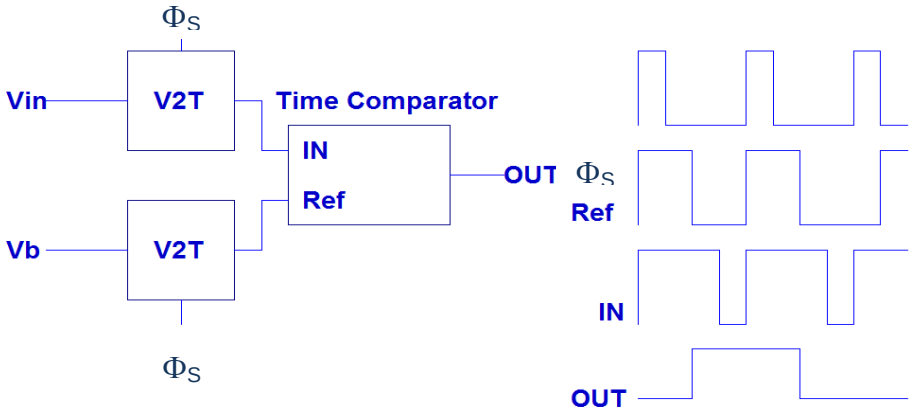



Figure-4.8 Block and Timing diagram of comparator

delay time from the raise edge of the clock. The next block, in cascade with the two V2T has the purpose to compare the delay times and choice if the V2T referred to input voltage is faster or slower than the V2T taken as reference. Then the output of the comparator (Out) is equal to logic level "1" or "0" according with the amplitude of $V_{IN}$ is less or more than reference voltage $V_B$ respectively. The schematic diagram for V2T (Voltage to time converter) is as shown in figure-4.9.

The supply voltage is VDD=1.8V to ground. When the phase $\Phi_C$ is low, the transistors M1, M4 and M6 are ON while the transistors M2, M3 and M5 are OFF. Therefore the initial conditions include that the capacitance C is charged to VDD and the parasitic capacitance $C_P$ is completely discharged. The input voltage $V_A$, applied on gate of transistor M3, is a constant voltage during each single conversion. The conversion starts when $\Phi_C$ is raised and the initial step is the V to I conversion by transistors M1, M2, M3 and the resistance RD, which work as a constant current generator. This current is used to discharge the capacitor C, and then it has a constant discharge. When the voltage $V_C$ across the capacitor falls below the threshold of transistor M5, the output of entire V2T raises. The presence of some inverter at the output has the only purpose to obtain a square wave with good edge in transitions.

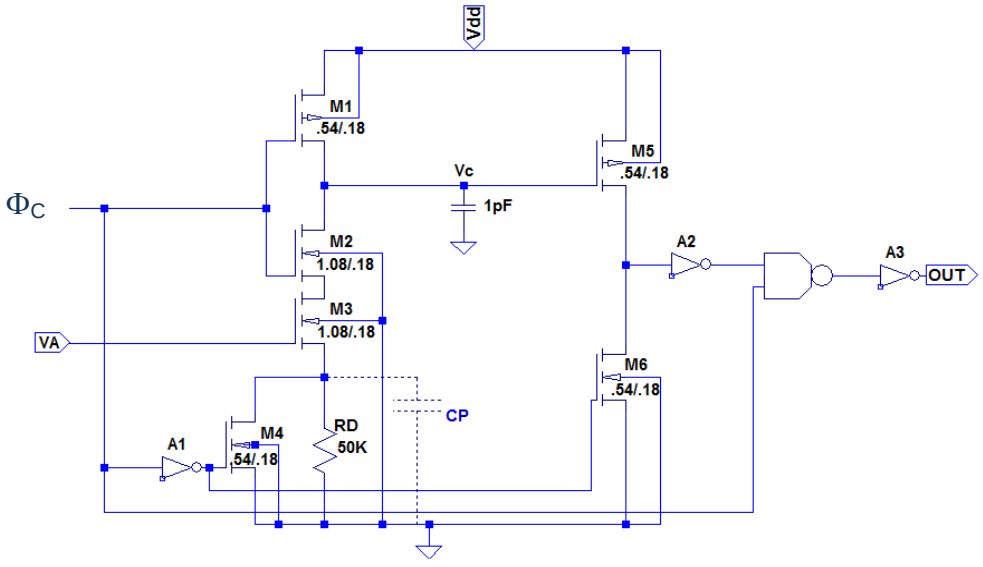



Figure-4.9 Schematic of Voltage to Time Convertor (V2T)

The next step is the design of the block which realizes the time comparator(as shown in Figure-4.10. The operation principle of this block is to determine which signal is the first to raise. A simple method to implement this algorithm is the use of a Delay Flip Flop (DFF). In fact if we connect the output of the V2T correspondent to the input signal to the input called "D" of the flip flop and the output of the other V2T to the input called "Clock" of the flip flop then we will obtain a right time comparison.

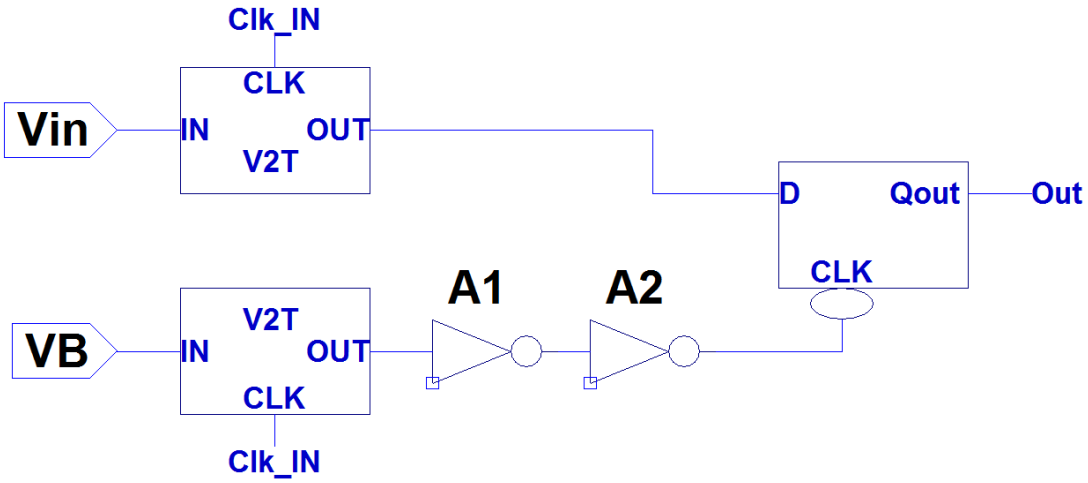


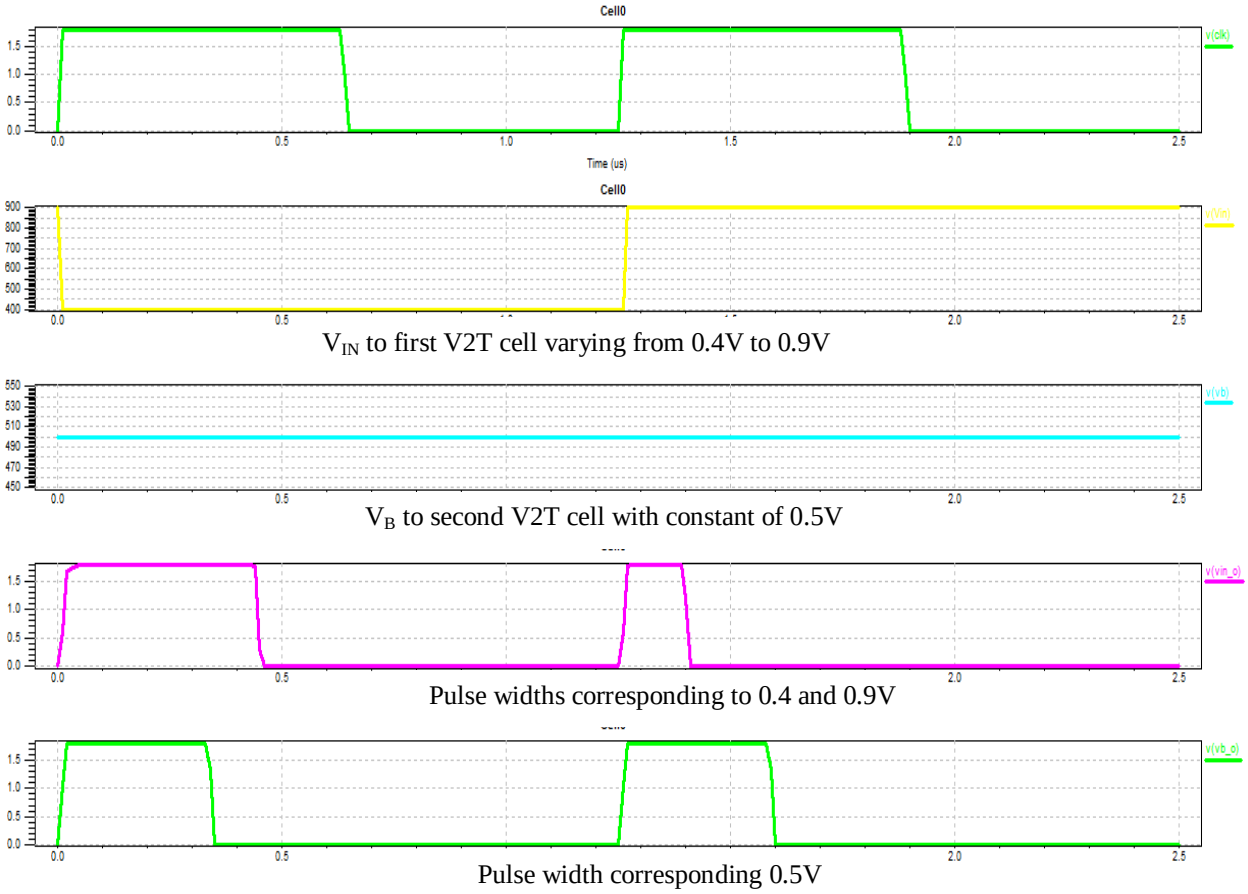

Figure-4.10 Block diagram of comparator

The operation of the DFF is to copy to its output the assumed value of the D input in the same instant of time when the Clock signal raises. In this configuration, naturally, the value of reference voltage VB ensures the edge at the output of its V2T, while the output of the V2T correspondent to the input signal can raise before or it is able not raise.

This way doing, when the Clock signal raises "read" the value of the D signal, and then if D signal raised before the output becomes "1", while if D signal still has to raise the output becomes "0". The implementation of this block with a simple DFF introduces only the errors referred to the respect the hold or the setup time to ensure the correct operation of the flip flop. Two inverters are cascaded in the V2T path because this signal is considered as clock signal for D flip flop, so there must be enough set up time for D (output of $V_{in}$).

**Simulations:**

Vin_o and Vb_o are the time domain waves we get from V2T cell corresponding to applied inputs Vin and Vb respectively. Now these waveforms is compared by time domain comparator which negative edge triggered D flip flop serves the purpose. To D flip flop Vin_o and Vb_o time domain signals are used as D input and clock input respectively and we get our output waveform as in figure-4.12**.**




$V_{IN}$ to first V2T cell varying from 0.4V to 0.9V

$V_B$ to second V2T cell with constant of 0.5V

Pulse widths corresponding to 0.4 and 0.9V

Pulse width corresponding 0.5V

Figure-4.11 a) Clock pulse b) Applied Input voltage to V2T c) Bias voltage of .5V applied to V2T d) Time domain waveform of input applied V2T e) Time domain waveform of bias applied V2T.

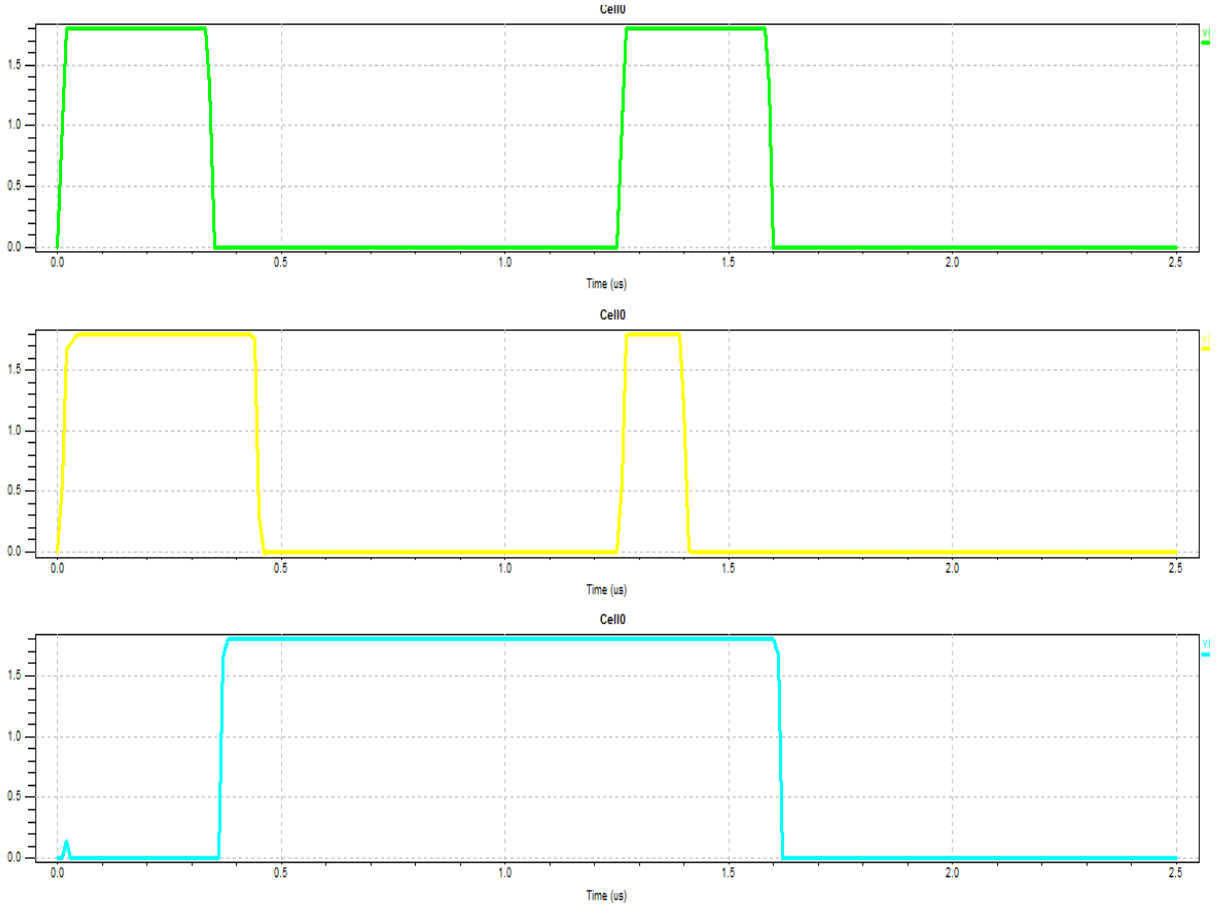



Figure-4.12 a) V2T output to Vb=0.5V b) V2T output to Vin=0.9V c) Comparator output

## 4.3 Design of Digital Logic (SAR CELL)

SAR Cell is the heart of the SAR-ADC. The main functions of digital logic is to memorize the sequence of bit output from comparator and realize the successive approximation algorithm for proponing the right sequence of data to DAC.

In order to realize SAR Cell, it is divided in same functional blocks as shown in Figure-4.13.

### 4.3.1 Phase Generator

The block called “Phase Generator” has the purpose to indicate to the “logic” on which bit the comparator is working, the “logic”, instead, is the mind of successive approximation algorithm, ending there is the “PIPO Register” which has the function to sample the digital word at the end of conversion and hold it for all time required by the successive conversion steps. The realization of each block will be done by full custom design. In particular the

"Phase Generator" will be designed with a cascade of DFF in series, as shown in Figure-4.14. This structure has the purpose to indicate on which bit the converter is working.

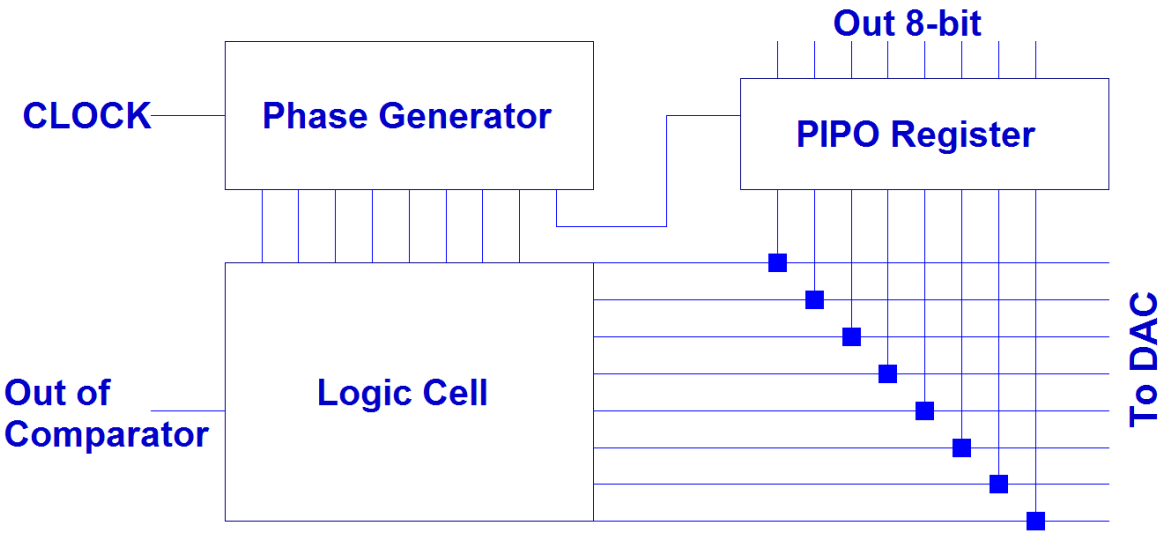



Figure-4.13 Structure of SAR Digital Logic

To obtain this goal there is an initial phase of reset during which all the DFF except the first one are set to logic level "1", while the first one is set to "0".

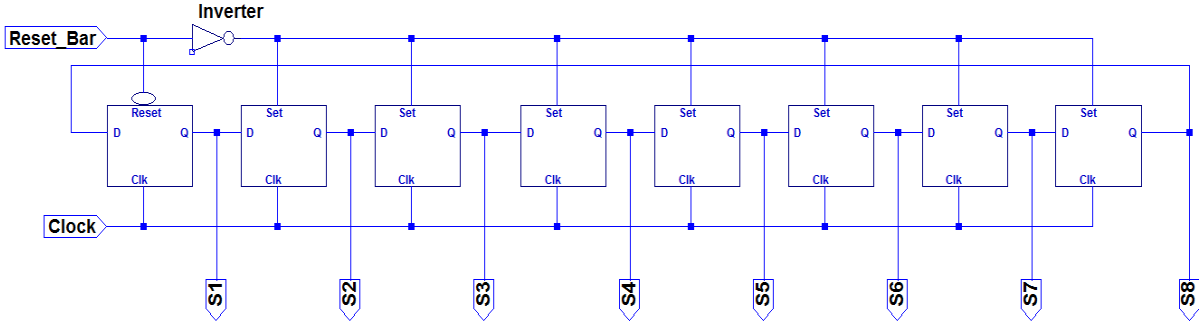



Figure-4.14 Chain if D-Flip Flop to generate a cyclic counter in one hot

During next steps the DFF continues to 'transfer' the "0" from 1st to 2nd, and then from 2nd to 3rd, and then from 3rd to 4th, and so on. When the 16th is "0" then the transfer is done means that the first sample is ready and then it is possible to transfer from 16th to 1st for restarting the transfer from the 1st to the other and obtaining another sample of the input. This principle of operation is like to have a counter with 14 bit and continually to count from 1 to 16 with one hot system.

**Simulations:**

For simulating results phase generator is reset for the first time when SAR-ADC is turned on and only for one clock cycle and then it operates on each clock cycle.

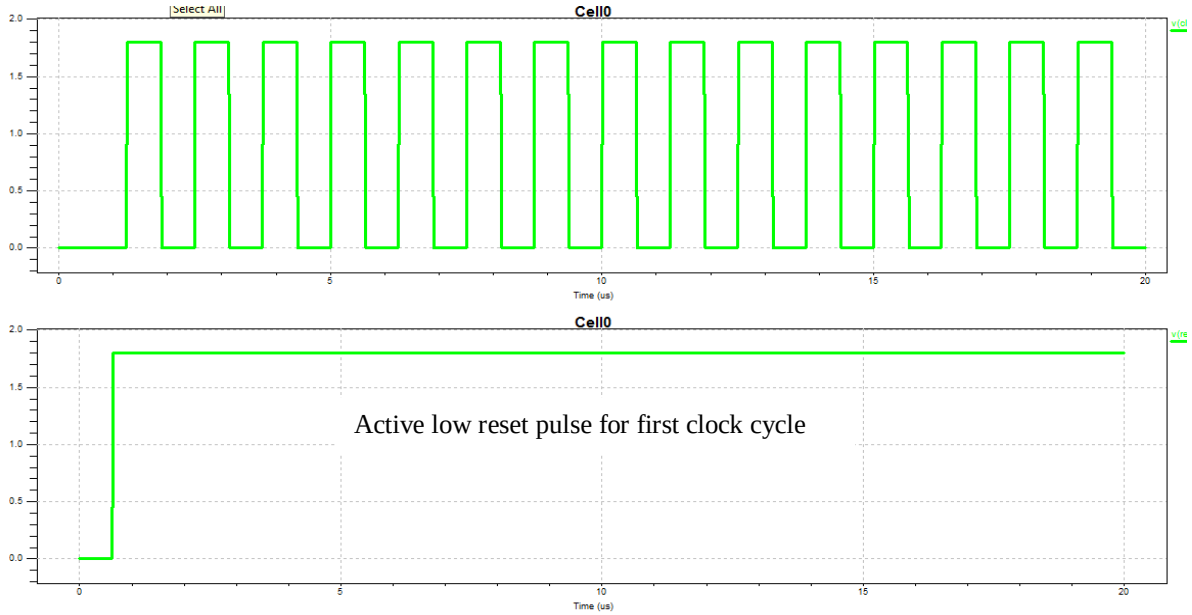
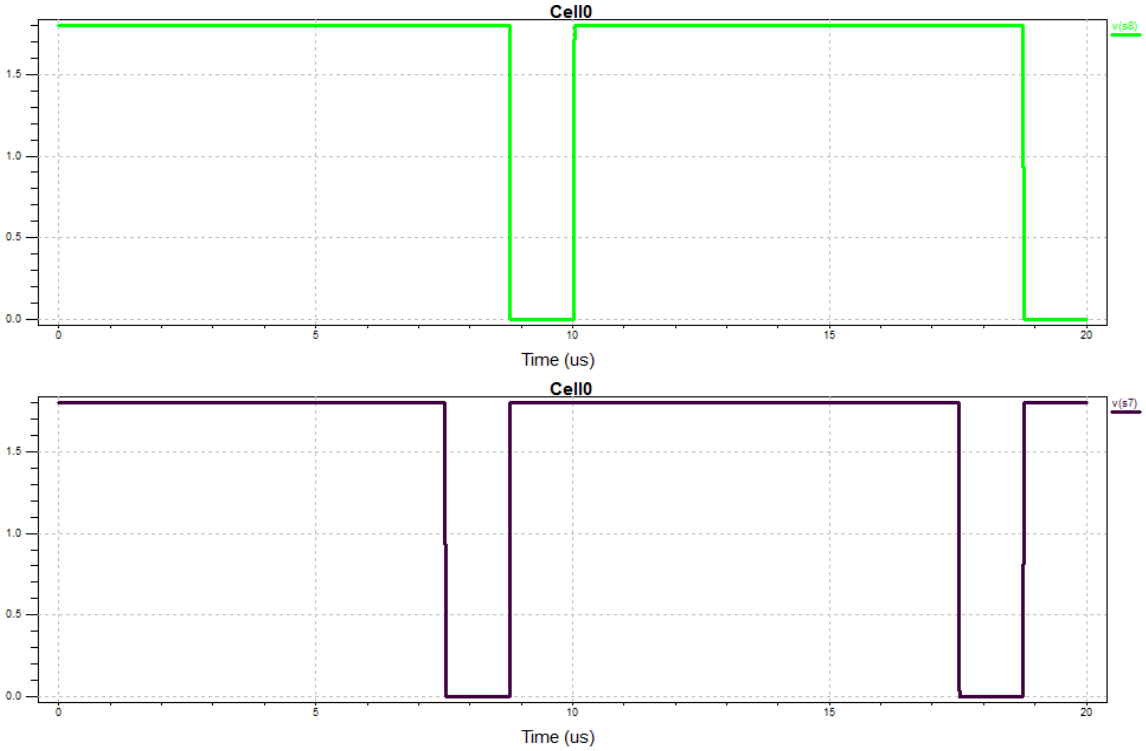



Figure-4.15 a) Clock pulse applied b) Active low reset for first clock cycle



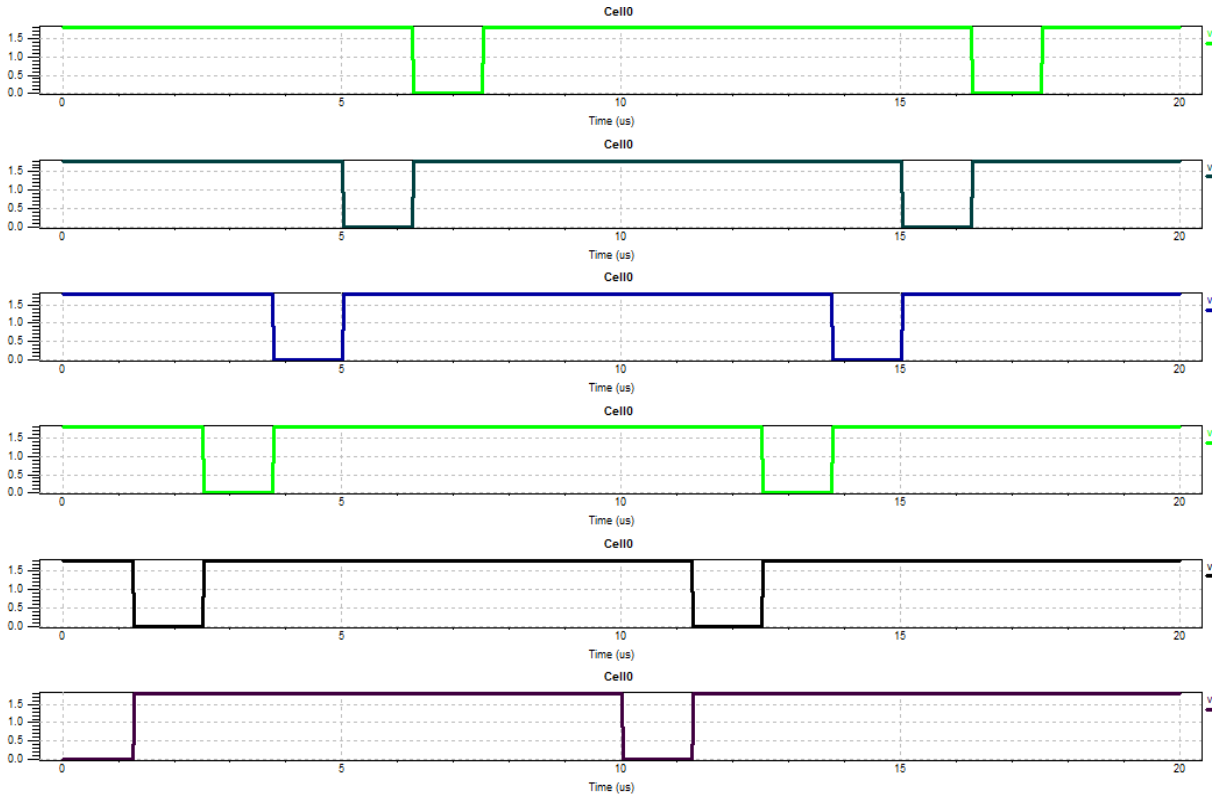



Figure-4.16 Output waveforms of phase generator

As in Figure-4.16 we can see from waveforms that for clock period of 10µs logic '0' is generated consecutively on each pulse and is fed as input to logic cell.

### 4.3.2 Logic Cell

The "Logic" block can be realized with twelve identical cells which have two main purpose: 1. to set respectively bit to logic level "1" when start its phase, 2. to copy the output of the comparator as soon as it have finished its comparison.

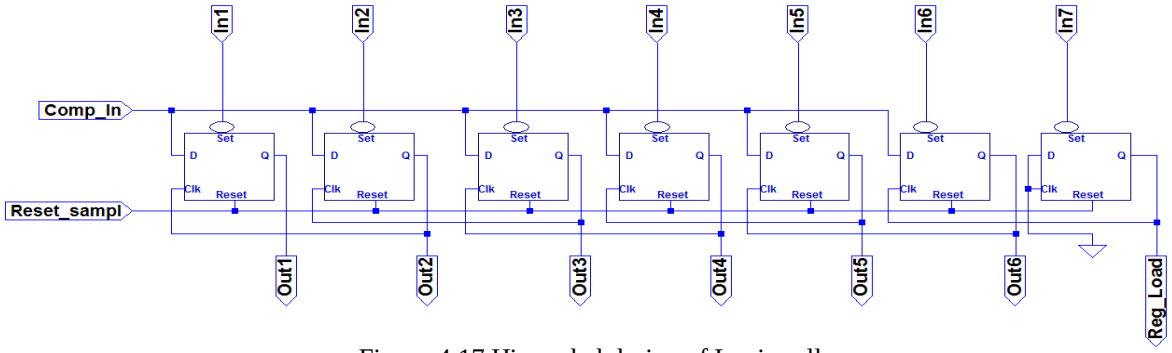



Figure-4.17 Hierarchal design of Logic cell

All the D flip flops have the active low set pins thus when logic ‘0’ is received from the phase generator (through In bits) it set the output Q to logic ‘1’ and is remained set till next flip flop sets whose output is given as clock to first flip flop and at that rising clock edge it reads the comparator output through Comp_In pin and transfer it to the output pin Q. Similarly all the other D flip flops are set and then read comparator output in next clock cycle as shown in Figure-4.18. After completion of the one conversion cycle these flip flops are reset during the sample period and at end of conversion i.e. when Reg_Load pin becomes high data is loaded into PIPO registers for the use.

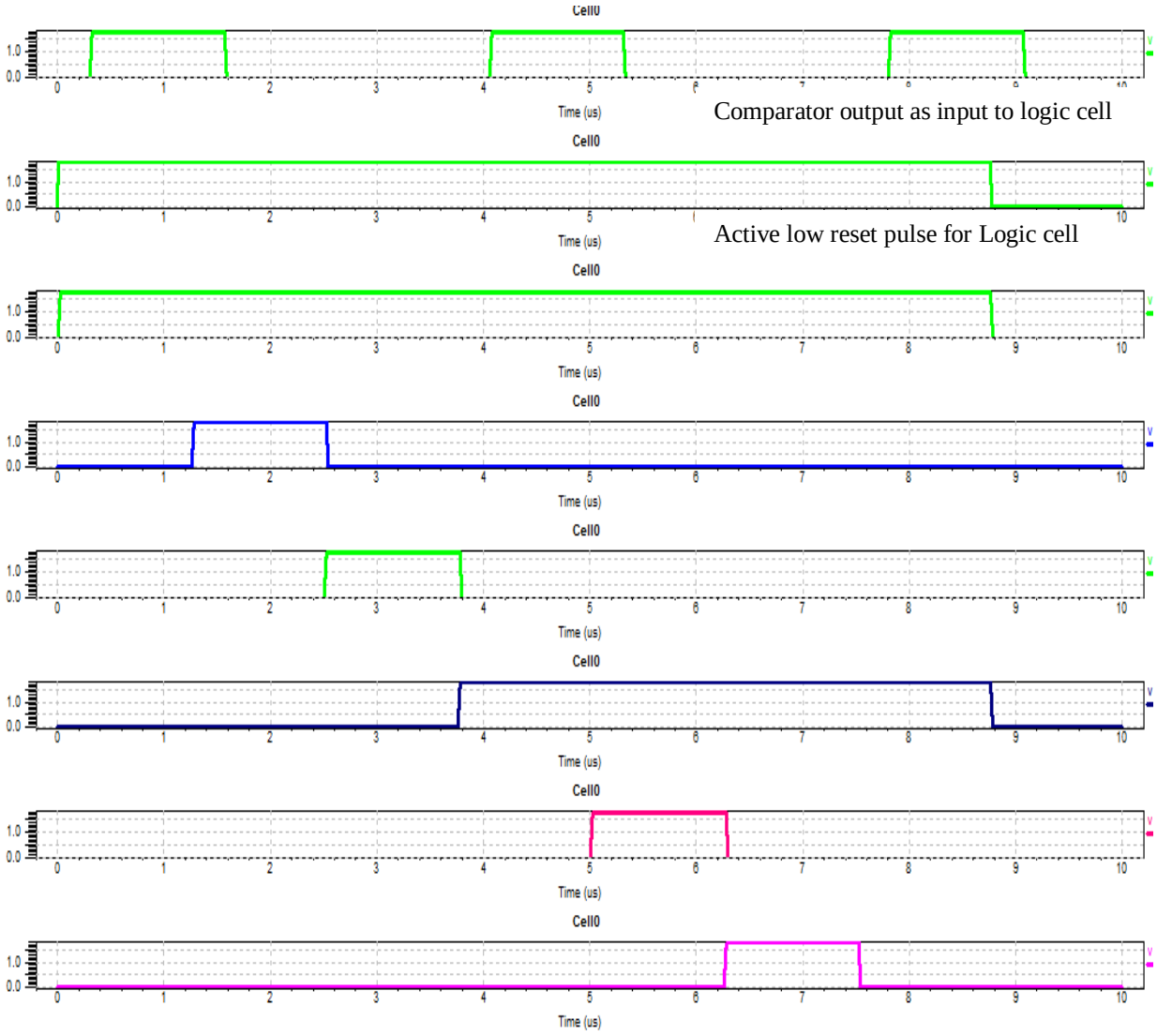



Figure-4.18Waveform showing output of logic cell by reading comparator output

### 4.3.3 PIPO Register

Parallel in parallel out register is used to store the digital output of a ADC for one conversion time period. It provides enough time span for the other application to utilize the processed digital word. Output Reg_load of logic cell is used to clock this PIPO register so that at end of conversion data can be loaded into it.

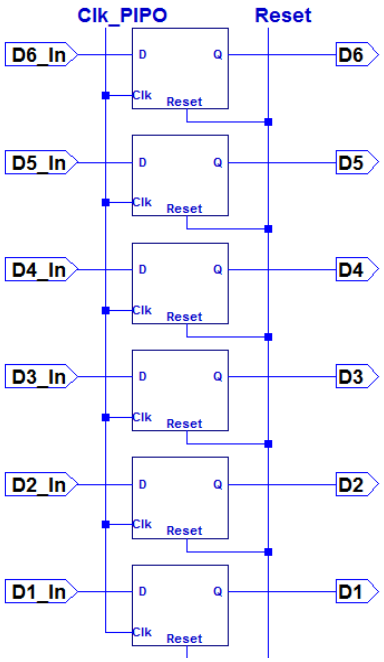



Figure-4.19 PIPO Register

### 4.4 Integration of SAR-ADC components

In this section all three SAR-ADC components DAC, Comparator and SAR cell were integrated and output waveform was analyzed by providing stimuli. The hierarchal design is shown in Figure-4.20.

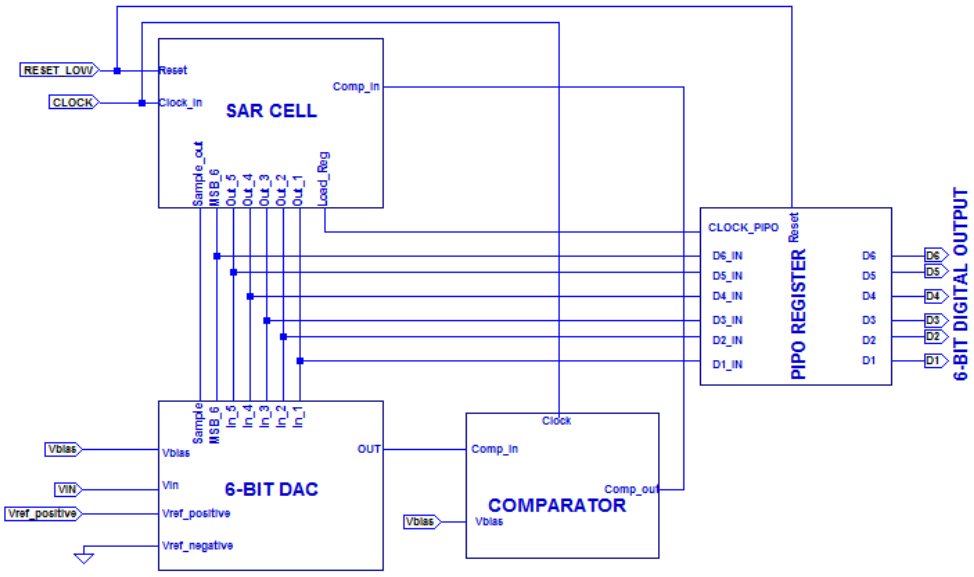


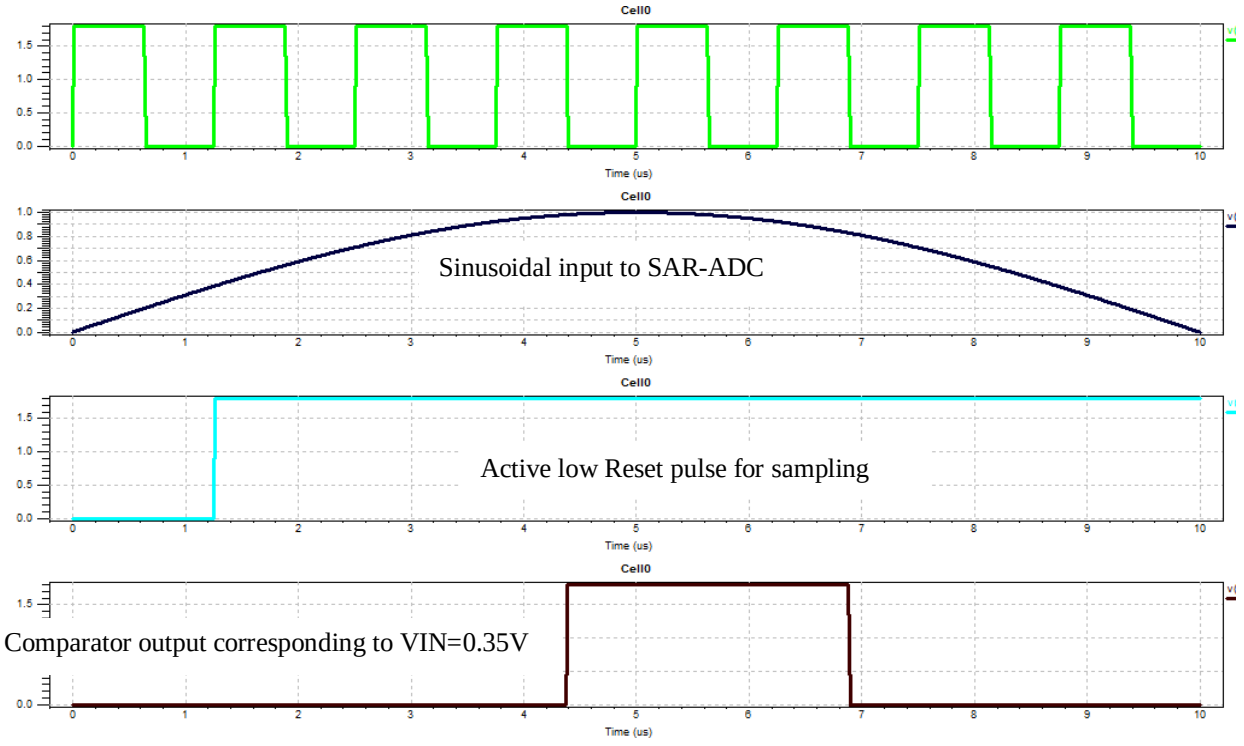

Figure-4.20 Hierarchal design structure of SAR- ADC implemented

During the integration of SAR-ADC it becomes necessity to utilize the buffers before providing digital signals (from SAR cell) to DAC and also when digital word is transferred to PIPO registers because if not the signal transferred has not that much strength (i.e. derive capability) so that it could derive an analog circuit. Therefore a buffer was designed to solve the purpose with minimum delay time.

**Simulation:**

For simulation the sinusoidal voltage of amplitude 1V and 0V offset was given throughe $V_{IN}$ port of six bit DAC with frequency of 50KHz (with in Nyquist criteria). $V_{BIAS}$ of 1V was applied instead of 0V as it reduces the offset at the output node. $V_{REF\_POSITIVE}$ of 1V was applied.

For the first time when SAR-ADC is turned on it is reset for the first clock cycle with period 1.25µs as the circuit is operating on 0.8MHz clock speed with period of 1.25µs. The simulation shown below is performed for one conversion cycle. The input sinusoidal is sampled at 0.38V and thus with 1V reference voltage the digital output expected is '001100'.



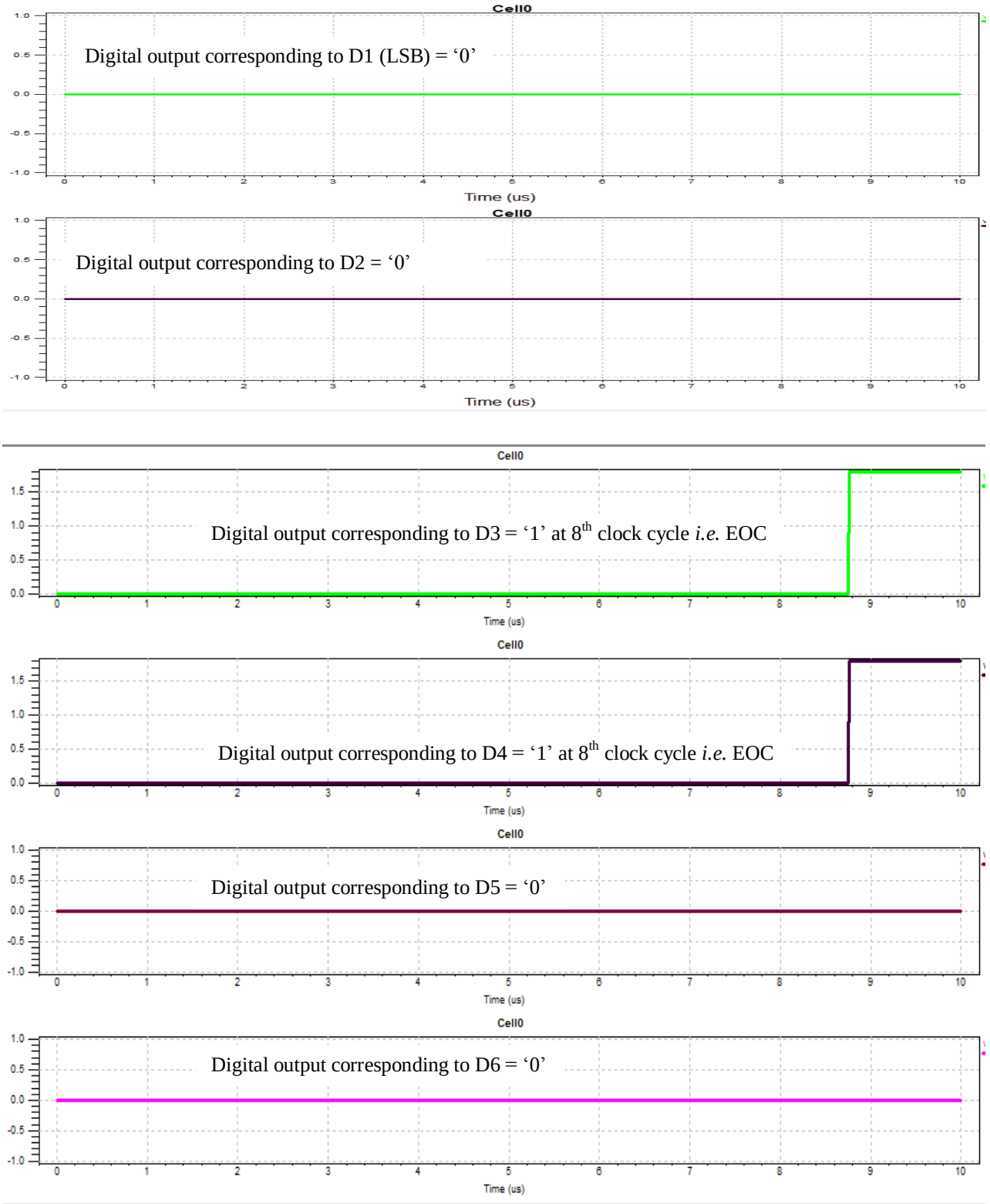



Figure-4.21 a) Clock input b) Vin c) Reset signal (active low) before start d) Comparator output

e),f),g),h),i),j) SAR-ADC 6-bit Digital output

# Chapter 5

## 14-Bit self calibrated DAC implementation for SAR-ADC

In this chapter design implementation and simulation results is discussed corresponding to the 14-bit DAC's that were implemented, one from the reference paper and another from the proposed architecture. Self Calibration technique is employed to reduce the capacitive mismatch and which comes into operation with the start up of the DAC and require first seven clock pulses only. After calibration it does its normal operation.

DAC here implemented is a smart circuit that does three operation successively, first sampling then as a subtracting node and at last conventional digital to analog conversion. SAR-ADC operates on "Binary Search Algorithm" where DAC bits are raised to logic 1 or logic 0 as per the decision made by Digital logic circuitry. So here according to the sampled input value equivalent digital bit corresponding to 1.8V reference voltage is provided to DAC by means of pulse signals which will be referred to as digital input of DAC.

### 5.1 Design Parameters of 14-Bit DAC

#### 5.1.1 Sample Speed

DAC implementation is application specific *i.e.* for Bio-Medical Applications and generally bound to minimum power consumption and to high resolution. DAC here has a tradeoff between power and speed. More speed means more power; hence sampling speed here opted for implementation is 100kSamples/s *i.e.* commonly used for operation of bio-medical applications.

#### 5.1.2 Clock Speed

DAC implemented requires 16 successive clock pulses to get an output digital code corresponding to the sampled analog input value. First pulse is for the sampling of input, next fourteen pulses if for normal DAC operation and the last pulse is for EOC .When EOC is high digital code is moved to the registers and can be used for further processing. So clock speed required is

$$Clock\ Speed = 16 * Sample\ Speed = 1.6MHz$$

$$Clock\ period = 1.6MHz^{-1} = 0.625 s.$$

### 5.1.3 Noise Limitation

Thermal noise plays the significant role on the operational behavior of the charge scaling DAC's. This imposes the limitation on maximum capacitance. Taking quantization error and thermal noise into consideration, the imposed limitation on $C_{Total}$ can be calculated as

$$\frac{kT}{C_{Total}} + \frac{LSB^2}{12} \leq \left(\frac{LSB}{2}\right)^2$$

$$LSB = \frac{V_{FS}}{2^N} = \frac{1.8}{2^{14}} = 0.1mV$$

For N=14,we got, $C_{Total} \geq 2.058pF$.

$$\text{Also, } C_{Total} = \left[2 \cdot \left(2^{N/2} - 1\right)\right] \cdot C_u$$

Cu is unit capacitance and we got, $C_{Total} = 254\, C_u$

That implies, $C_u \geq 8fF$.

In 180nm technology minimum capacitance we can take is 4fF. Thus using the minimum Cu is not preferred because a little mismatch could show a huge deviation from normal operational characteristics. Thus Cu used for the implementation of DAC is 15fF instead of 8fF.

### 5.1.4 MIM Capacitor Dimensions

Square plate Metal-Insulator-Metal capacitors were employed for implementing DAC and their dimensions are shown below in Table 2.

**Table 2: MIM Capacitor dimensions for DAC**

| Serial No. | Capacitor Bits (1 to 14) | Ideal Value (in fF) | Width (in µm) | Length (in µm) | Real Value (in fF) |
|---|---|---|---|---|---|
| 1. | 7 & 14 | 15 | 3.73 | 3.72 | 14.9925 |
| 2. | 6 & 13 | 30 | 5.33 | 5.33 | 30.0079 |
| 3. | 5 & 12 | 60 | 7.6 | 7.6 | 60.04 |
| 4. | 4 & 11 | 120 | 10.8 | 10.81 | 119.9895 |
| 5. | 3 & 10 | 240 | 15.34 | 15.35 | 240.0725 |
| 6. | 2 & 9 | 480 | 21.76 | 21.76 | 480.0255 |
| 7. | 1 & 8 | 960 | 30.83 | 30.84 | 960.0477 |

### 5.1.5 Stimulus

Supply voltage $V_{DD}$ considered for this application is 1.8V and $V_{SS}$ to be the ground voltage *i.e.* 0V. $V_{REF+}$ is 1.8V and is kept equal to the maximum input voltage ($V_{IN}$) swing which is having 0.9V as common mode signal. Any value of $V_{bias}$ can be chosen but probably for ease 0.9 V is selected. For analyzing the operation of DAC we provide all the input stimuli and see at which vale circuit is sampling the input value. Then accordingly we provide equivalent digital input successively by means of square pulses with time period equal to 0.625µs for example '1000000-0000000' for 0.9V input sampled value.

**Table 3 Design Parameters Tabulated**

| **Parameters** | **Value** |
|---|---|
| Technology | Cadence UMC_180nm Technology |
| Supply voltage | 1.8V |
| Power | < 800nW |
| Resolution | 14-bits |
| Sampling speed | 1.6MS/s |
| Gain Error | <1LSB |

### 5.2 DAC Implementation

14-bit capacitive DAC was implemented but instead of using normal DAC structure a split capacitor DAC approach was utilized because with normal DAC structure time for charging the capacitors would be very large and hence large dynamic power dissipation. As seen in Figure 5.1 capacitors didn't get much time to settle down their voltages due to large capacitances when sampled at 100kS/S. If we reduce the sampling rate to 10kS/s then they get more time to settle voltages across top plates as shown in Figure 5.2.

Thus to overcome this issue we employ split capacitor structure in which the total capacitance is effectively reduced and so does the delay and power dissipation but with this come other drawbacks such as non-integer value of split capacitor, *etc.*

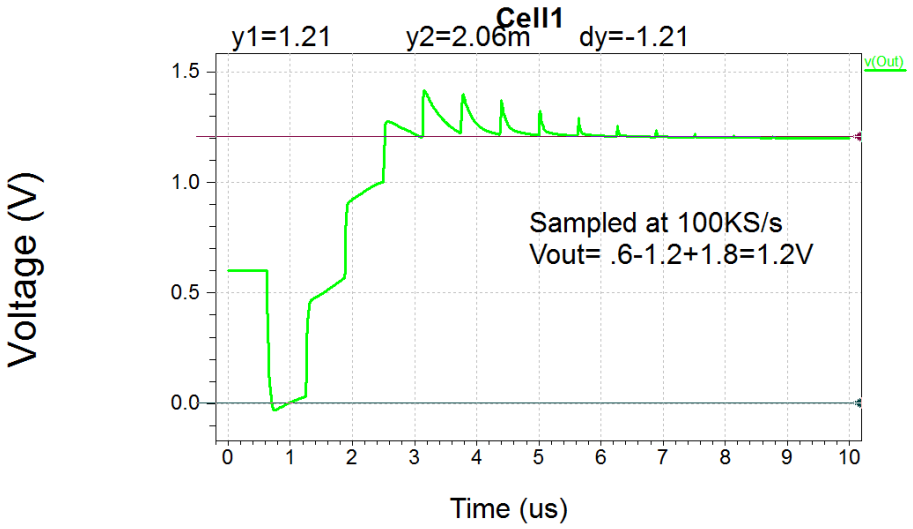



Figure-5.1 Non settling output DAC node

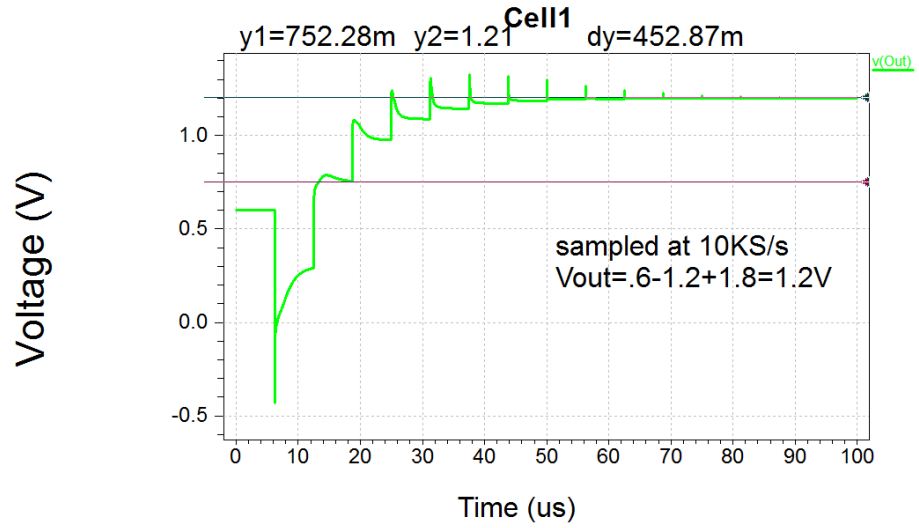



Figure-5.2 Reduced Sample rate to settle capacitor voltages

### 5.2.1 Split Capacitor DAC

As discussed in the parameter selection of DAC design the minimum capacitance or unit capacitor $C_u$ we will be using is 15fF. For Cu equal to 15fF the split-DAC structure is shown in Figure-5.3, where CP1 and CP2 are the parasitic capacitances and $C_s$ is the split capacitor. The capacitive cell shown in figure is implemented and operated in the same way as described in section 4.1.1 and shown in Figure-4.2.

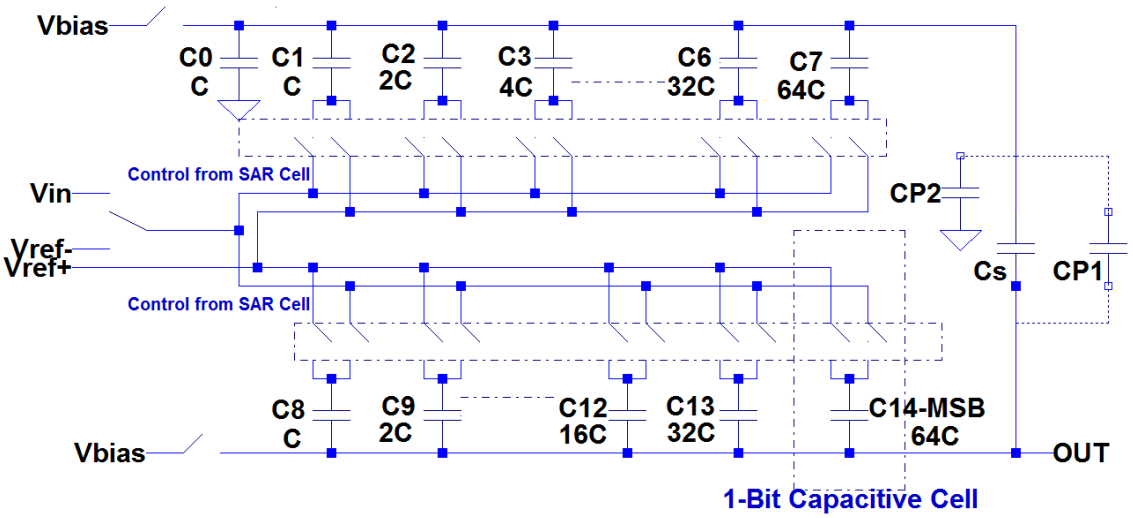



Figure-5.3 Structure split-capacitor DAC

The value of split capacitor $C_S$ is given by sum of capacitances on LSB side and sum of capacitance on MSB side *i.e.*

$$C_S = \frac{128}{127} * C_u = \left(1 + \frac{1}{127}\right) C_u \quad \ldots (5.1)$$

To fabricate a capacitor with this much accuracy is not possible as Cu itself is very small. So alternative is to use unit split capacitor instead of using exact or non-integer value of capacitor as shown in Figure-5.4. In general what is done Cs is kept equal to Cu and C0 as shown in figure is removed. Purpose of C0 is just to make sure maximum OUT voltage is 1LSB less to the full swing. Removing C0 thus in turn introduces gain error but is very less (*i.e.* corresponding to $\frac{Cu}{127}$ ) as compared to 1LSB and hence can be ignored.

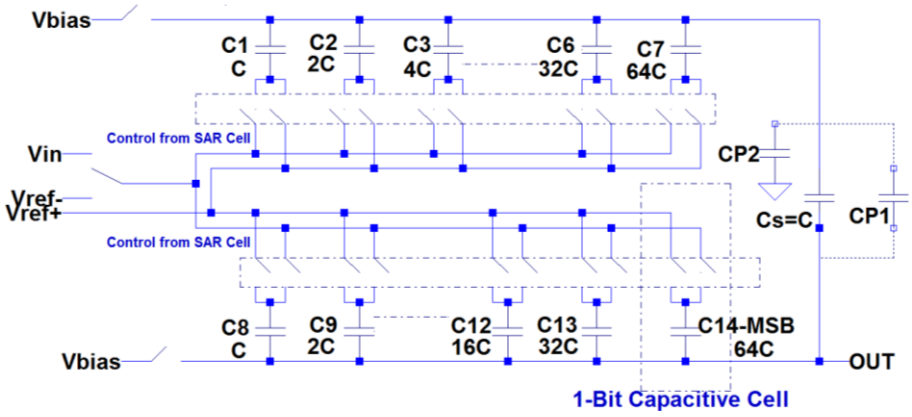



Figure-5.4 Unit Split Capacitor DAC

### 5.2.2 Proposed Split Capacitor DAC

In the proposed DAC unit split capacitor structure is used and C0 is also introduced. Thus circuit is having mismatches only due to value of Cs *i.e.* ($\frac{1}{127}$ Cu) less than expected value. The gain error for circuit should be less than previous unit split DAC. The structure for this DAC is shown in Figure-5.5.

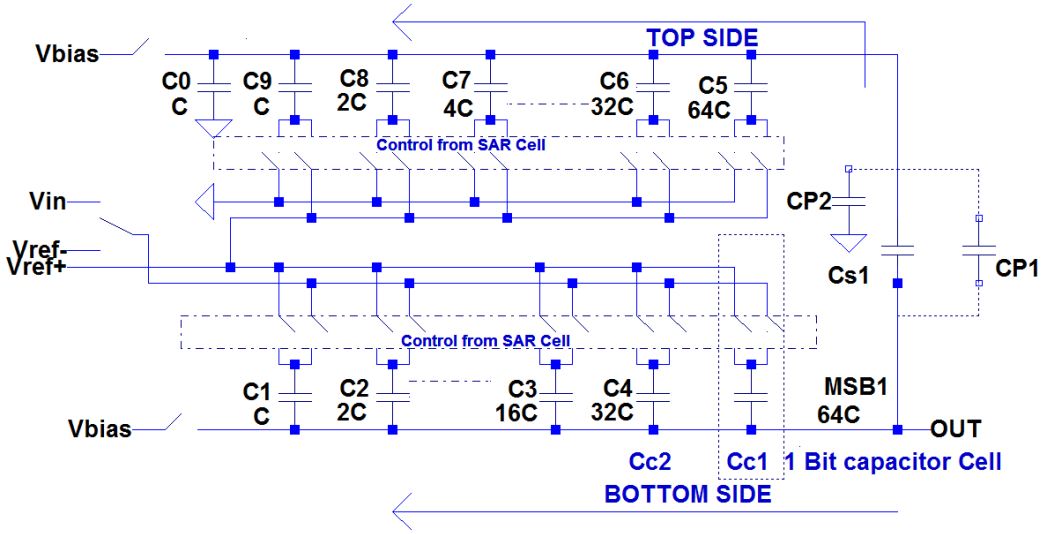



Figure-5.5 Proposed Split Capacitor DAC

Now for operation of a circuit input signal is give such that each bit of DAC is operated at logic '1' just to see full scale OUT voltage swing of DAC and this will show maximum variation at output due to mismatch corresponding to each bit. Initially 1.8V DC is given as an input to the circuit and common node voltage taken is also 1.8V (chosen randomly). Then after sampling pulse output should be 0V and with every digital input every bit of DAC rise successively to a voltage level corresponding to capacitance value finally will reach to its maximum output value $V_{REF+}$ *i.e.*1.8V as shown in Figure-5.6. Digital input is provided using digital pulse with same rate as that of system clock *i.e.* 1.6MHz.

The DAC that has been implemented has no mismatch in capacitances only it includes mismatch due to split capacitor $C_S$ and that is very small to observe on output of DAC. But due to process variations the value of the capacitors cannot be precisely fabricated. Hence contributes to mismatch in capacitance value which is very critical for high resolution or low

Cu values DAC. Hence a self calibration technique is introduced to reduce mismatch as discussed in next section.

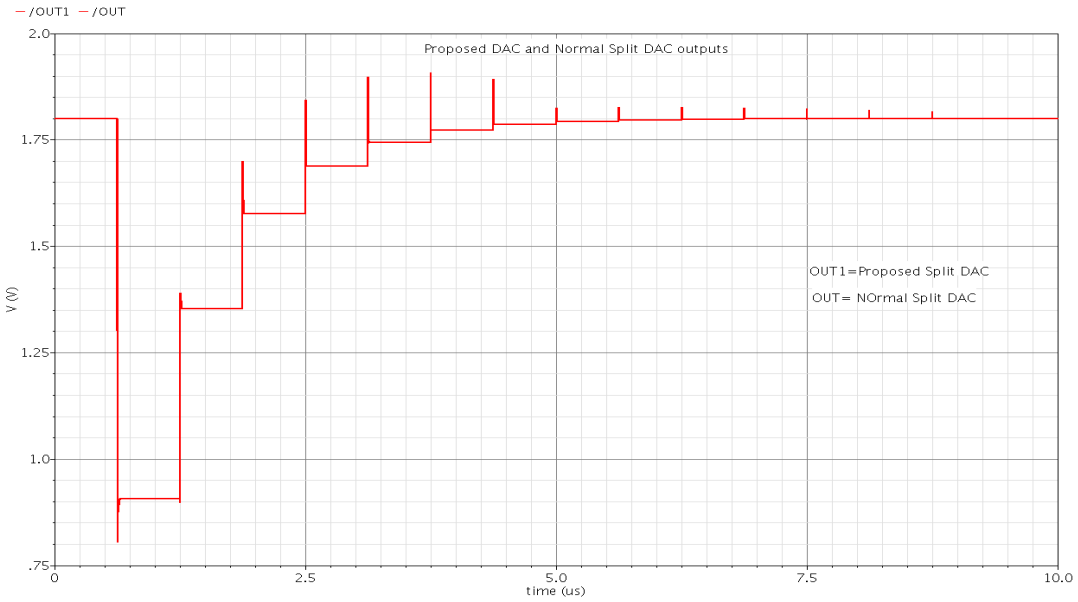



Figure-5.6 DAC output for maximum input swing voltage

### 5.2.3 Self Calibrated Unit Split DAC

In high resolution DAC's or DAC with low Cu value a little mismatch could result in large voltage variations at the output. Thus it is important to calibrate mismatch in such circuits. Here self calibration technique is utilized in the proposed circuit to reduce the capacitance mismatch. This is a foreground calibration technique hence it will be initiated automatically whenever the circuitry is turned on for first time and after using certain clock periods for calibration it will work with its normal operation as DAC.

We will be calibrating MSB capacitor frequently named as $C_{C1}$ with the rest of capacitances in the circuitry named as $C_{C2}$ are shown in Figure-5.7. This is because MSB capacitor stores half of the reference voltage and rest half is on the all other capacitors. Thus we will find mismatch voltage corresponding to capacitance mismatch which also include capacitance due to Cs and then will calibrate the mismatch.

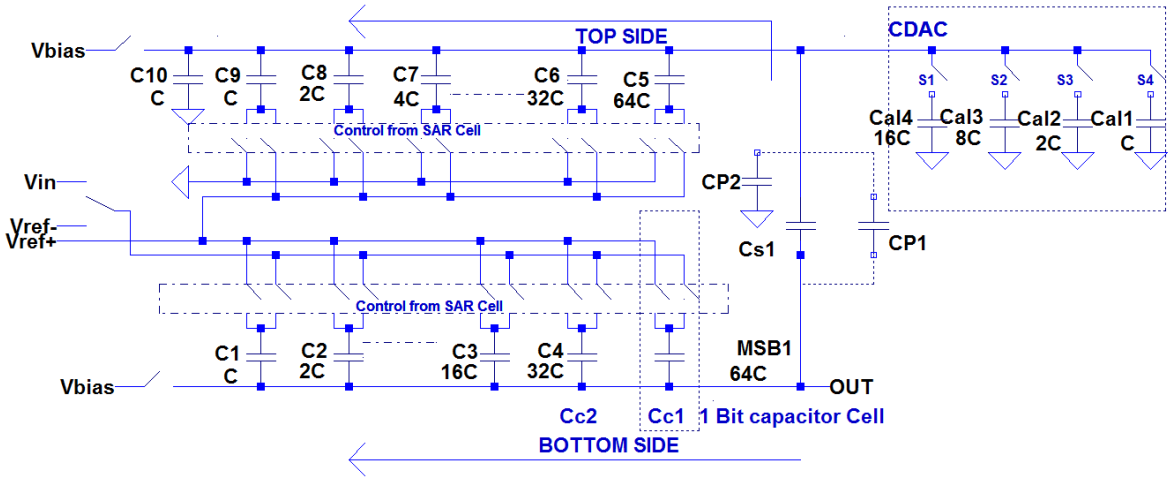



Figure-5.7 Proposed Self Calibrated DAC

The calibration is done in three phases:

1) Pre-charging: Initially all the bottom plates of CDAC as shown in Figure-5.7is grounded. Pre-charging is done by connecting top plates of Cc1 and Cc2 (*i.e.* all other DAC bits) to the common mode voltage and bottom plate of Cc1 and Cc2 to ground and $V_{REF+}$ respectively.

2) Charge Re-distribution: During charge re-distribution common node voltage is removed and the voltages at the bottom plates of Cc1 and Cc2 are swapped.

3) Mismatch Calibration: After charge re-distribution phase we will get the change in the out node voltage corresponding to mismatch in capacitor which is 20fF here intuitively added. For the corresponding change or difference in voltage is reduced using CDAC capacitors by adding charges to out not till it reaches its common node potential.

Operation of CDAC is simple at first only Cal4 will be introduced to the circuit by switch S1 and then the comparator will compare out node to the common mode voltage if it is less next switch S2 will turn on if more S1 will turn off. Thus CDAC calibrates in normal successive approximation manner.

Maximum mismatch that can occur in DAC is equivalent to 1LSB so maximum capacitance mismatch CDAC can calibrated here is 20fF and can be seen in Figure-5.8. From figure it can be seen that out node voltage is charged to 1.8V which is taken as common node voltage for instance.

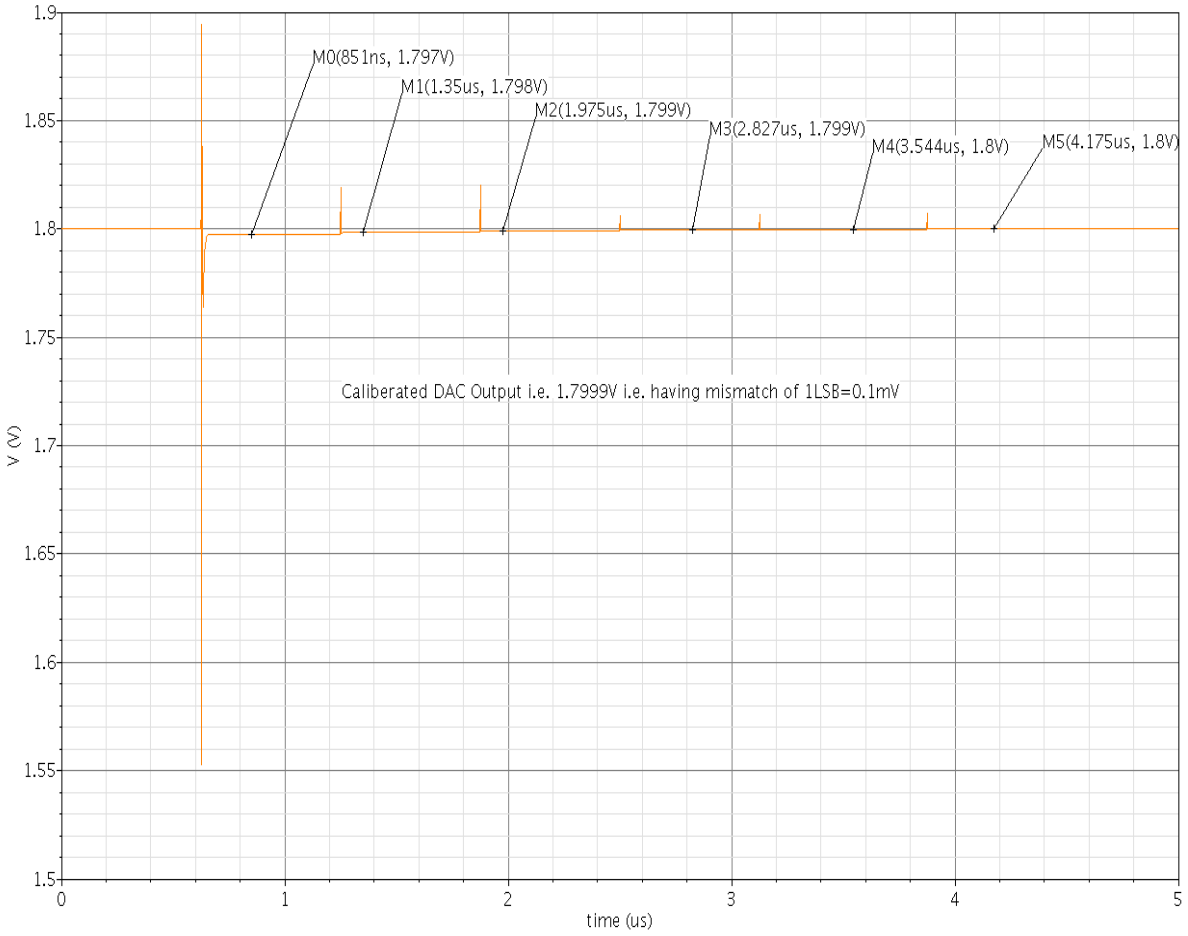



Figure-5.8 Calibration for 20fF capacitor mismatch.

Calibration will be done automatically when the chip is powered on and using the same successive approximation logic. It will consume initial seven clock pulses two for pre-charging and charge re-distribution and next 5 for mismatch calibration. After these clock pulses DAC will work with its normal operation. For the same input consideration as discussed in section 5.2.2 the output of DAC to obtain single digital output including calibration is shown in Figure-5.9.

From Figure-5.9 it is clear that after calibrating DAC is working fine for the complete input voltage swing on which it is sampled that is 1.8V here in case.

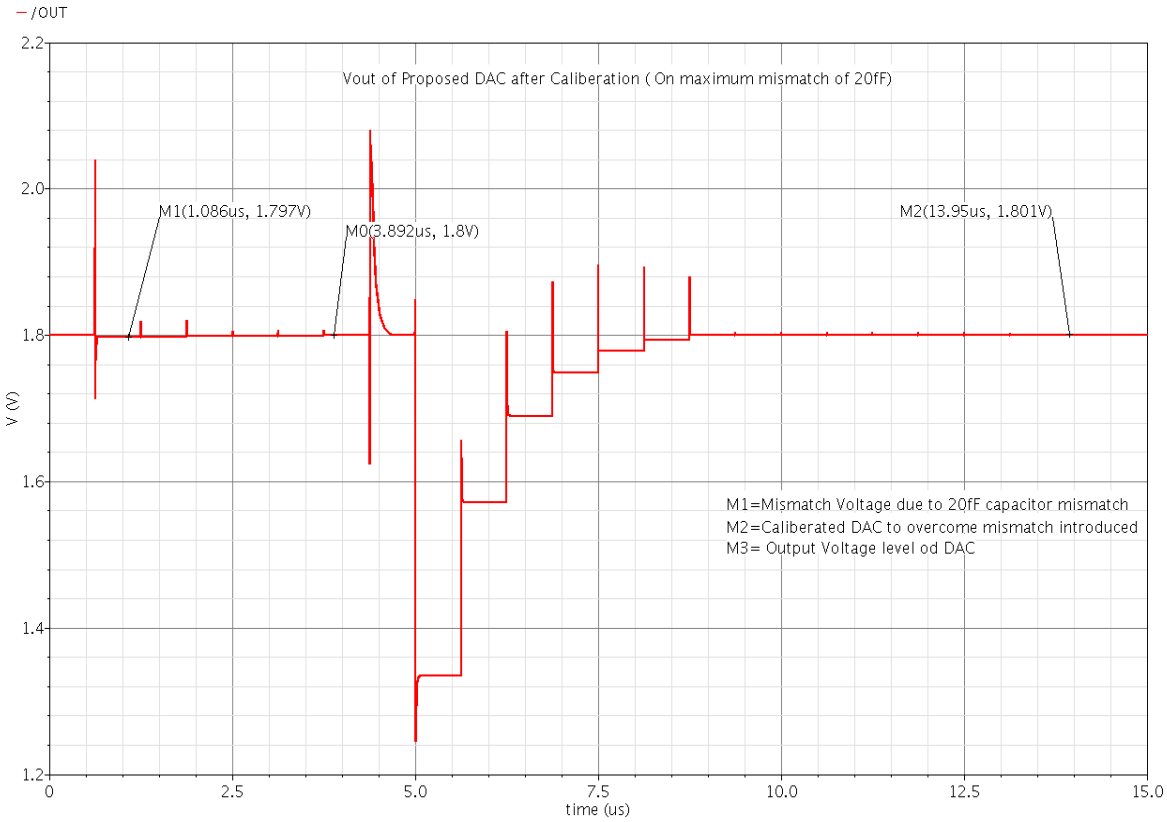



Figure-5.9 DAC output for one conversion cycle including Calibration

### 5.2.4 Corner Analysis

Corner analysis is done for the complete one conversion cycle of DAC including calibration. Five corners have been taken into consideration and they are ss, ff, sf, fs, tt for capacitor, resistance and mosfets. The corners analysis in Figure-5.10 shows that there is no significant transition in the out node after the DAC conversion cycle but little during the calibration phase but still at the end of calibration phase output settles to required OUT node voltage value.

## 5.3 Parameters Obtained

### 5.3.1 Power Consumption

Power consumed by DAC at every clock transition is shown in Figure-5.11 and the average power consumed by DAC for one conversion cycle including calibration is 515nWatt.

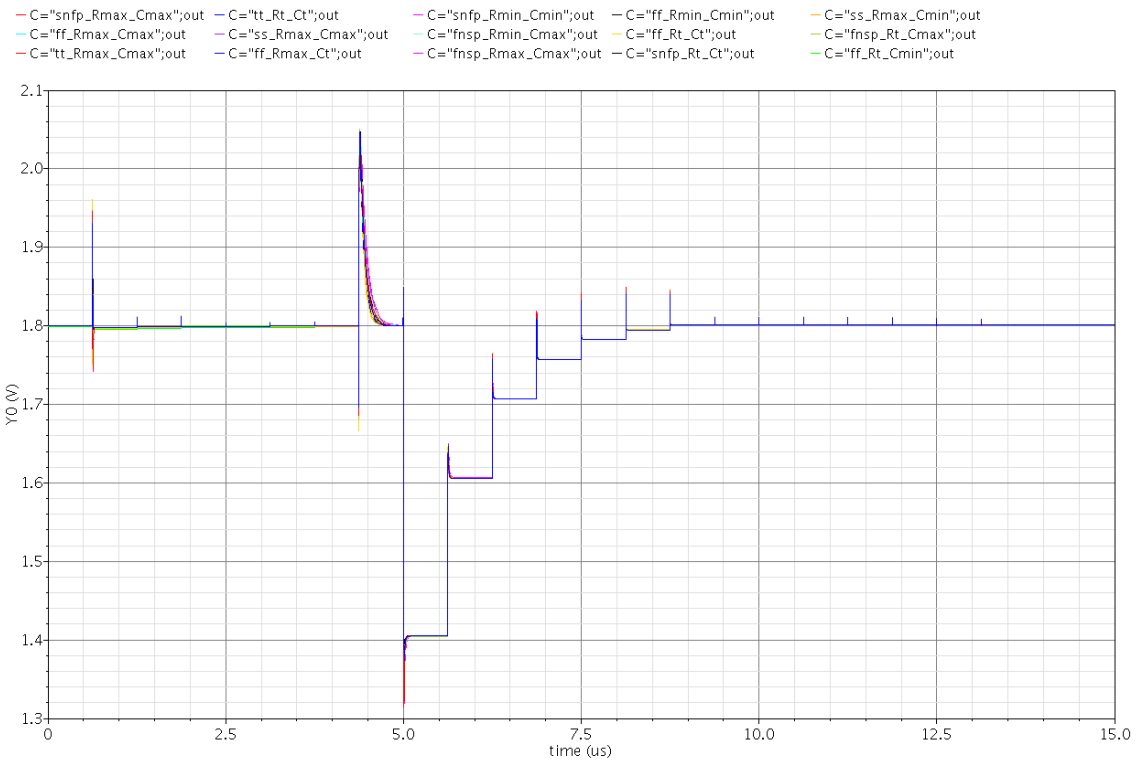



Figure-5.10 Corner Analysis of DAC conversion cycle including calibration phase

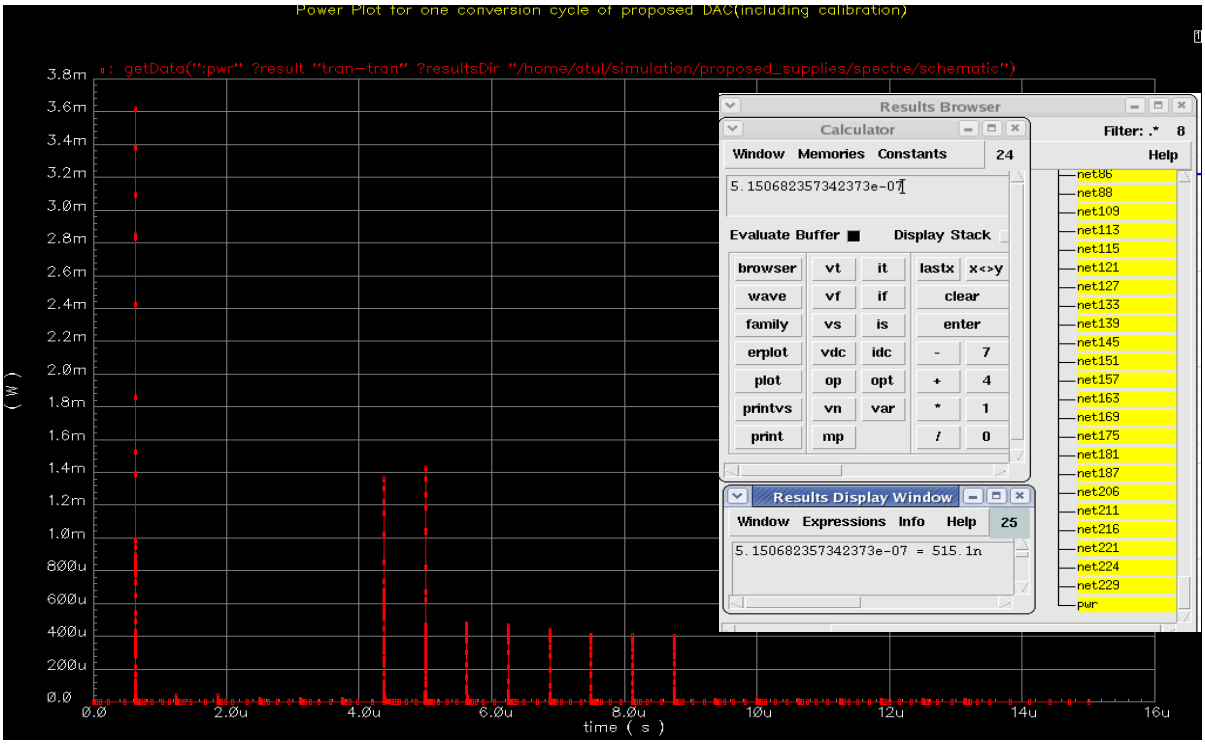



Figure-5.11 Instantaneous power on each clock transition

### 5.3.2 Gain Error

Gain Error for the proposed DAC with self-calibration technique obtained is 0.053mV *i.e.* well within 0.5LSB range (i.e. 0.5LSB= 0.054932V) as shown in Figure-5.12.

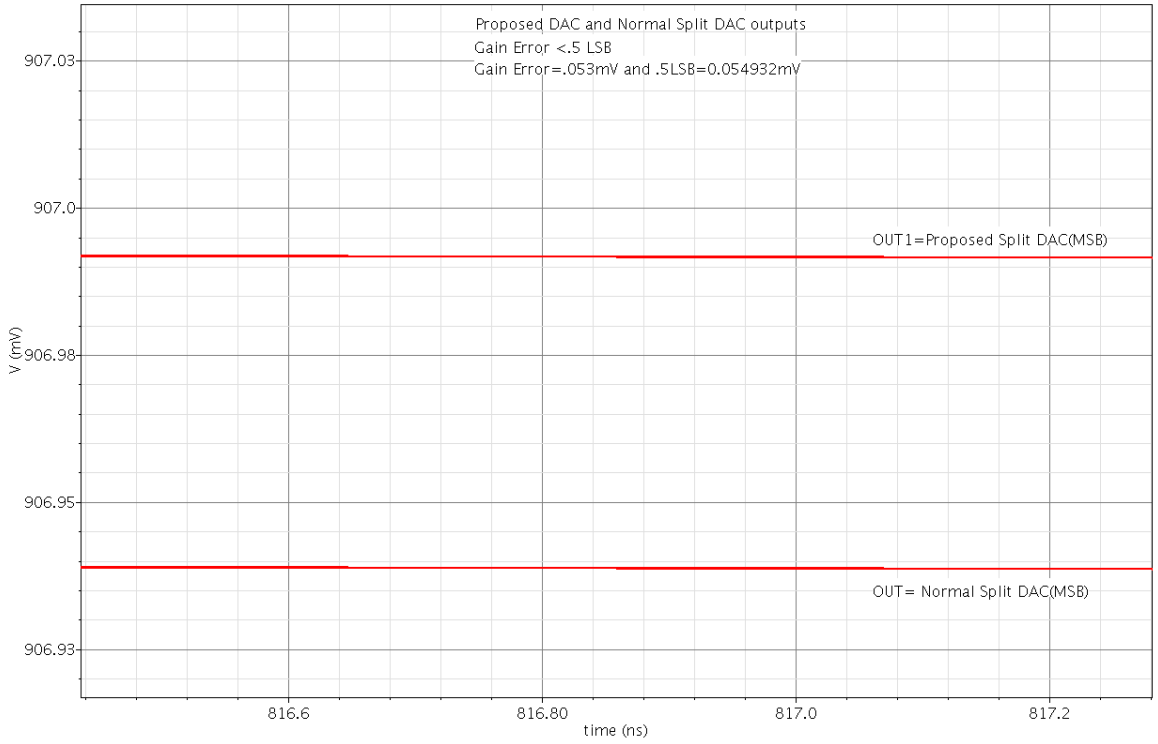



Figure-5.12 Gain error for Proposed DAC

## 5.4 Proposed DAC Symbol (DIP)

Symbol of the proposed DAC is implemented in Cadence Virtuoso having Dual Inline Package as shown in Figure-5.13.

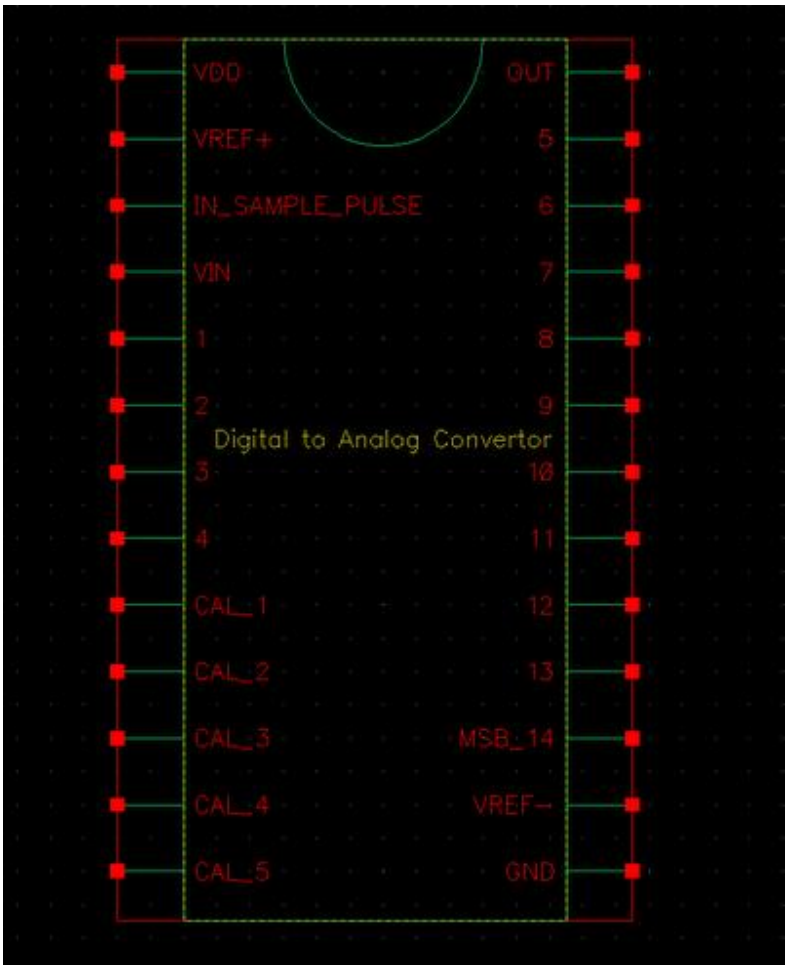



Figure-5.13 Proposed DAC symbol

## 5.5 Layout Design

Hierarchical layout design method has been used and implemented. EDA tool used is Cadence Virtuoso and micron rule is followed.

Design Rule Check (DRC) is performed in order to verify that layout fulfills all electrical and geometric rules provided by foundry and finally, LVS (Layout Vs Schematic) is performed on the layout design to provide equivalence between the Layout and Schematic.

### 5.5.1 Inverter Layout

Layout of the inverter designed is shown in Figure-5.14.

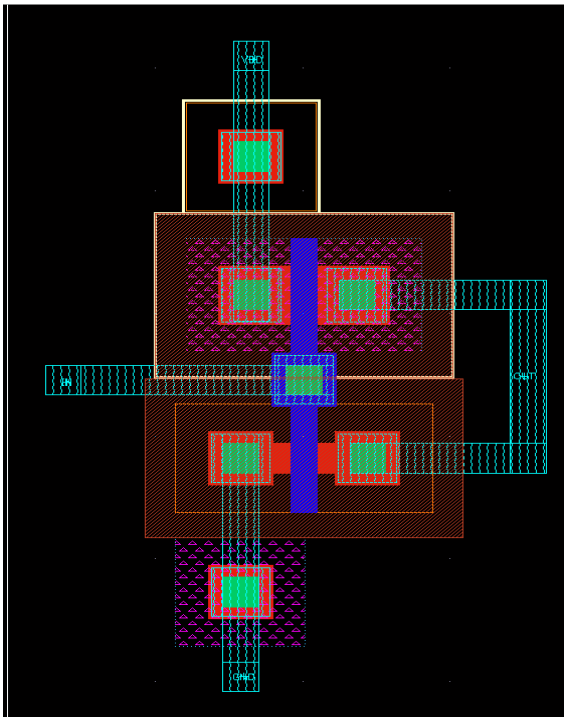


Figure-5.14 Layout of Inverter

### 5.5.2 MUX Layout

Layout of the MUX designed for the switching of analog input voltages on to the capacitors used as a bit is shown in Figure-5.15.

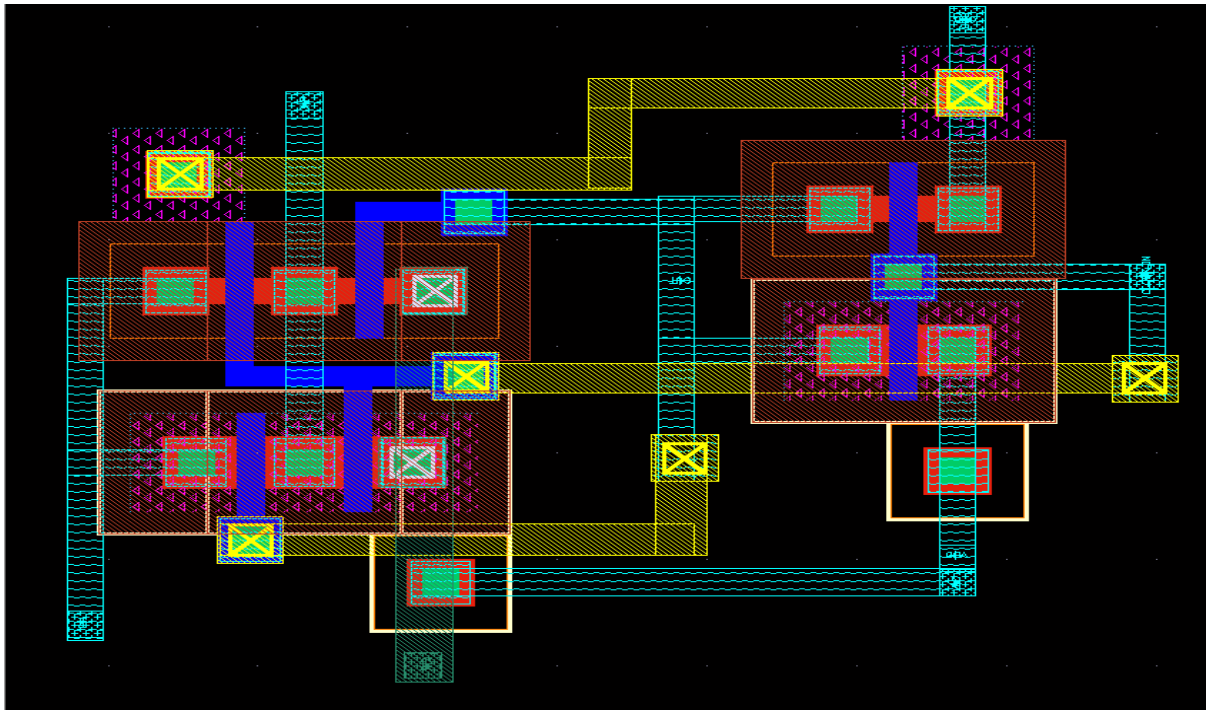


Figure-5.15 Layout of 2:1 MUX implanted using transmission gates

### 5.5.3 DAC Layout

Layout of the proposed DAC designed is shown in Figure-5.16.

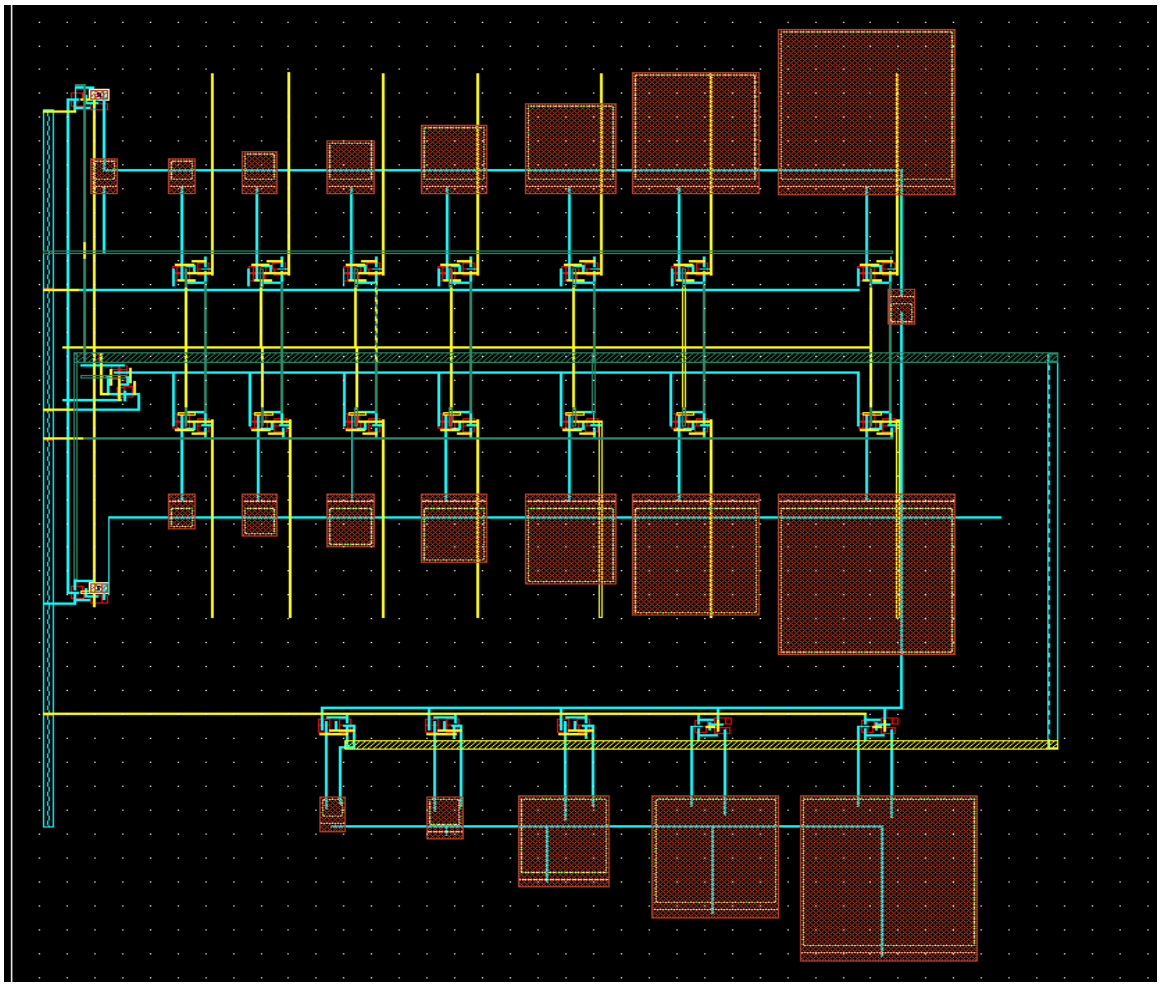


Figure-5.16 Layout of DAC

### 5.5.4 DAC RCX extracted View

Parasitic extracted view of proposed DAC is shown in Figure-5.17.

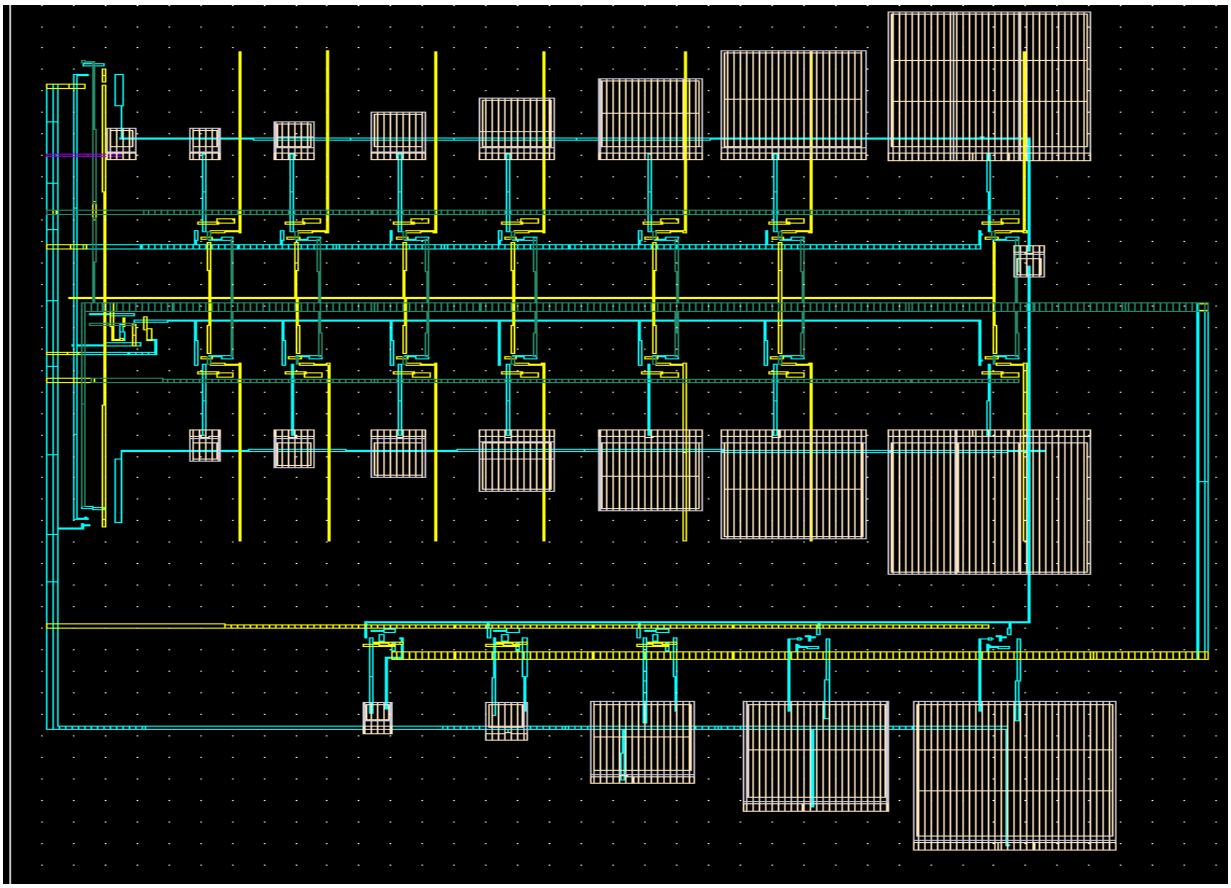


Figure-5.17 Extracted view of DAC

# Chapter 6

# Conclusion and Future Scope

## 6.1 Conclusion

In this thesis, first 6-bit SAR-ADC was analyzed and designed just to have the know-how of the working of SAR-ADC on each clock transition. A 6-bit SAR-ADC was chosen just for the simplification as for a high LSB the resolution of ADC should be as small as possible and thus linearity is not an issue while designing a high LSB SAR-ADC. Many issues come to picture while designing and were resolved with time for e.g. Set-Reset priority, timing issues with clock in comparator, loading effect while interfacing digital and analog components (DAC), *etc.* After interfacing all the components of SAR-ADC a digital sample was obtained from it, which shows difference of a LSB due to comparator offset but was well within margin of 1LSB.

Next, a 14-bit SAR-ADC was analyzed and designed. Initially conventional architectures of DAC was analyzed and implemented. Finally unit-split capacitor DAC was analyzed and implemented because of its various advantages over others like very less total capacitance hence very less power consumption, successively performs three operation hence reduces need of extra circuitry *etc.* Thus the circuit is optimized for low power consumption and consumes only 515nWatt (calibration included) to get single digital output. Next to improve its accuracy various self-calibration techniques were implemented on DAC to reduce the capacitance mismatch. Finally a self-calibration technique was proposed which is simple in its operation and requires only few clock pulses (number of pulses required depend on CDAC bits) during initial start-up of the chip. Maximum mismatch corresponding to 20fF can be calibrated with this technique which is greater than 1LSB mismatch. Gain error is very less for proposed architecture *i.e.* less than 0.5 LSB. Then layout was designed for proposed DAC architecture and corner analysis was done which shows no unusual variations in the circuitry. Cadence Virtuoso® was the EDA tool used for the purpose with UMC 180nm technology file.

### 6.2 Future Scope

DAC implemented here is single ended DAC thus have bounded SNR. To improve SNR differential DAC approach can be used which improves dynamic range of circuitry and reduces common mode noise which is dominating in high resolution DAC's.

Calibration technique here used is foreground calibration technique which is good for calibrating a capacitance mismatch which is optimal here but not very accurate. As mismatch here is calibrated before chip operated on any bit but in actual every bit has different capacitance mismatch which can be calculated while DAC is operated on a particular bit and then adding mismatch value corresponding to that bit at the end of operation. With this calibrating circuitry design becomes little complex as memory would be required to store each bit mismatch and hence will increase the power consumption. But the overall accuracy of DAC will be improved to a large extent.

**Table 4: Summary of SAR-ADC Circuits**

| **Reference Year** | **[1] 2003** | **[2] 2007** | **[3] 2009** | **[4] 2011** | **[5] 2011** | **[6] 2011** | **[7] 2012** | **[8] 2007** | **This Work** |
|---|---|---|---|---|---|---|---|---|---|
| **Resolution** | 8 | 8 | 10 | 10 | 10 | 10 | 10 | 12 | 14 |
| **Sampling Rate (kS/s)** | 4.1 | 200 | 100 | 1000 | 1 | 100 | 200 | 100 | 100 |
| **Power(µW)** | 0.850 | 2.47 | 1.3 | 7.16 | .0025 | 1.3 | 1.04 | 25 | 0.512 (excluding comparator) |
| **Supply voltage(V)** | - | | | 0.9 | 0.5 | 0.6 | 0.6 | 1 | 1.8 |
| **Gain Error** | - | - | - | - | - | - | - | - | <0.5LSB |

## Paper Published/Presented

- Atul Thakur and Alpana Agarwal, Low-Power Architectures and Self-Calibration techniques of DAC for SAR-ADC implementation, *International Journal Of Innovative Research In Electrical, Electronics, Instrumentation And Control Engineering (IJIREEICE)*, Volume-2, Issue 3, March 2014.
- Atul Thakur and Alpana Agarwal,Analysis and Design of 6-Bit DAC implemented for SAR-ADC for Bio-Medical Applications in 3rd National Conference on Advances in Metrology (Ad-Met – 2014), during February 19 – 21, 2014 at Thapar University, Patiala.
- Atul Thakur and Alpana Agarwal, Analysis and Design of 6-Bit DAC implemented for SAR-ADC for Bio-Medical Applications, Runner-up, Paper presentation contest organized by IET , during April-2014 at Thapar Unversity, Patiala.

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