INVESTIGATIONS ON SWITCHED CAPACITORS BASED MULTILEVEL INVERTERS FOR GRID CONNECTED PHOTOVOLTAIC POWER GENERATION SYSTEMS

A Thesis submitted in fulfillment of the requirements for the award of the degree of

Doctor of Philosophy

Submitted By

Ritika Agarwal

(Reg. No. 901904007)

Under the supervision of

Dr. Krishna Kumar Gupta

Dr. Shakti Singh

Electrical & Instrumentation Engineering Department

Thapar Institute of Engineering & Technology

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CERTIFICATE

I hereby certify that the work which is being presented in the Thesis entitled, ***"INVESTIGATIONS ON SWITCHED CAPACITORS BASED MULTILEVEL INVERTERS FOR GRID CONNECTED PHOTOVOLTAIC POWER GENERATION SYSTEMS"*** in fulfillment of the requirement for the award of the Degree of ***Doctor of Philosophy*** submitted in the ***Electrical & Instrumentation Engineering Department*** of the **Thapar Institute of Engineering & Technology** is an authentic record of my own work carried out under the supervision of **Dr. Krishna Kumar Gupta** and **Dr. Shakti Singh** and refer other researcher's work, which are duly listed in the reference section.

The matter presented in this Thesis has not been submitted for the award of any other degree of this or any other University.

Ritika Agarwal
Reg. No. 901904007

This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

Dr. Krishna Kumar Gupta
Assistant Professor

Dr. Shakti Singh
Assistant Professor

Date: 25/10/23

जय गुरु जी!!
शुकराना गुरु जी!!

.....dedicated to

My father ***Mr. Arun Agarwal***

Abstract

Renewable Energy Systems (RESs) continue to play significantly important role in addressing the concern over global warming. Among various RESs (viz. wind, solar, fuel cells, and hydro), solar energy is being harnessed prominently because it is freely available, there are no moving parts, and can be placed near the load centres. However, the Photovoltaic (PV) based electric power generation is characterized by intermittent output and wide operating range, and therefore requires grid interconnection through power converters or Power Conditioning Unit (PCU). From the viewpoint of easy maintenance and cost-effectiveness, the grid-connected structure can be advantageous for PV systems as they do not use the battery for energy storage. As far as PCU is concerned, the two-stage structure is generally used with PV systems having low and fluctuating output voltage. Such a two-stage structure is usually operated by utilizing a dc-dc converter to regulate the PV output voltage and maximize the output power with voltage boosting feature, and the power conversion process from dc-ac is achieved through an inverter.

Traditionally, a two-level inverter is widely used for grid connected systems, but these inverters are characterized by high dv/dt stress, more Electro Magnetic Interference (EMI), and no capability to handle higher voltage range with devices of lower voltage rating. To overcome these issues, Multilevel Inverters (MLIs) have become a preferred choice for low and medium-power dc-ac energy conversion applications to ensure high power quality. Conventional topologies of MLIs pose three major challenges: (a) they require a significantly large number of power devices for an increased number of levels in the output voltage waveform; (b) they required additional circuits and/or complex control methodologies to balance the voltages of the capacitors; and (c) they do not offer any inherent voltage gain, i.e. the voltage is limited to unity. The ongoing research aims to develop new MLIs that offer reduced component count, inherent voltage boosting, simplified voltage balancing, low-Cost Function (CF), suitability for grid connected PV system and easy extension for three phase version. For achieving these features, ‘Switched Capacitors’ based MLIs (SCMLIs) have emerged as suitable candidate.

In this work, three novel SCMLI topologies are presented for application in PV systems. The first one is a five-level grid connected inverter which effectively reduces CF by utilizing only six power switches and a single diode with a switched capacitor. This configuration eliminates the requirement for multiple isolated dc sources. The proposed topology can achieve a voltage boost of up to twice the input voltage with self- balancing of the capacitor. The operation and performance of proposed topology is ascertained through simulations and verified experimentally. An important limitation exhibited by this topology is in terms of large Peak Inverse Voltage (PIV) in a few of the power switches.

In order to address the limitations of first proposed topology a second topology is presented which synthesizes seven levels. The proposed topology offers voltage boosting capability of up to 1.5 times the maximum voltage level of the input dc voltage, without imposing high voltage stress on any power switches. Therefore, PIV of all switches are within operating voltage. Capacitors are self-balanced by employing switched-capacitors principle. Simulation studies and experimental validation are carried out. In the topology, however, due to non-complimentary nature of a few switches, the number of gate driver increases and it increases the CF.

A third topology proposed in this work to overcome the limitations of the previously mentioned topology is a self-balancing nine-level structure. This inverter is capable of producing a nine-level voltage with a gain of two, using only a single dc source, eight power switches, three capacitors, and two diodes. The proposed topology ensures that the capacitor voltages remain inherently balanced, thereby eliminating the need for additional circuitry. The complementary nature of the switches reduces the number of gate drivers required, resulting in a decreased CF. Additionally, this topology can be expanded to achieve a higher voltage gain and a greater number of levels in the output voltage. With a reduced number of switches and sources, it generates a high number of levels, and its output voltage has a better harmonic profile, which means it requires a smaller filter size. Furthermore, this proposed topology is highly reliable. Validations are made through simulations and experimental studies for single-phase version.

Lastly, an extension of the proposed seven-level topology to its respective three-phase version is presented. The three-phase topology, while retaining the main features of inherent voltage gain and self-balanced capacitors, synthesizes three-phase voltages with a single input

dc source, resulting in a thirteen-level line-to-line voltage. This topology too validated through simulation and experimental studies.

Keywords: Grid connected PV system, Multilevel inverter, Renewable Energy Systems, Switched capacitor, Self-boost, Single-phase, Three-phase.

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Ritika Agarwal

Contents

List of Figures

List of Tables

Abbreviations

Acronyms

BF	Boosting Factor
CF	Cost Function
CHB	Cascaded H-bridge
DC	Diode Clamped
DER	Distributed Energy Resources
EMI	Electro Magnetic Interference
ESR	Equivalent Series Resistance
FC	Flying Capacitor
FCMLI	Flying Capacitor Multilevel Inverter
HB	H-bridge
LSPWM	Level-Shifted Pulse-Width Modulation
MLI	Multilevel Inverter
MPPT	Maximum Power Point Tracking
MTTF	Mean Time to Failure
MTTR	Mean Time to Repair
MVS	Maximum Voltage Stress
NPC	Neutral Point Clamped
PCU	Power Conditioning Unit
PI	Proportional-Integral
PIV	Peak Inverse Voltage
PLL	Phase-Lock-Loop

PV	Photovoltaic
PWM	Pulse-Width Modulation
RESs	Renewable Energy Systems
SC	Switched Capacitor
SCMLI	Switched Capacitors based Multilevel Inverter
THD	Total-Harmonic-Distortion
TSV	Total Standing Voltage
UPF	Unity Power Factor

Chapter–1

Introduction

1.1 GENERAL

The electric power has mostly been generated through large scale projects using conventional resources such as thermal, hydroelectric, and nuclear. The implementation of such power plants has resulted in socio economic effects and concern for the environment. Even the Clean Air Act is enforced to regulate the pollution emitting from fossil fuel-based plants [1]. Because of these concerns, it is demotivating to expand the power generation through conventional arrangements.

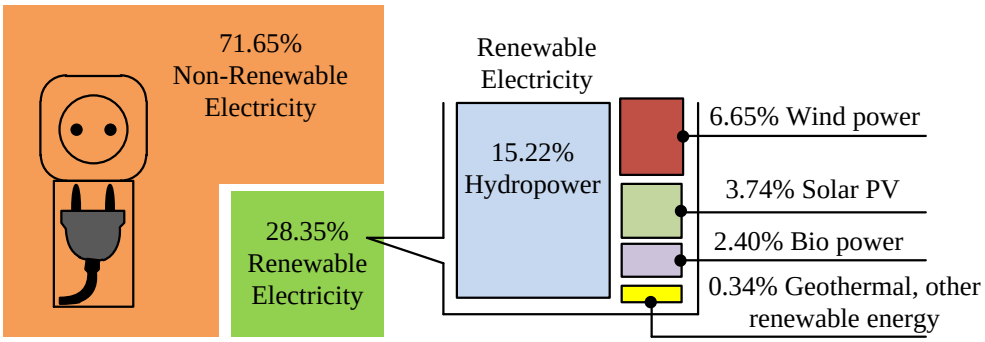


Fig. 1.1: *Estimated renewable energy share of global electricity production*

The power generation through renewable energy resources suffices the objective to mitigate the concern to the environment and climate change, which are arising with conventional power generation. Renewable power generation is also serving other goals such as sustainability, access to affordable electricity, and reliability. The present share of renewable energy is although 28.3% worldwide as shown in Fig.1.1 [2]. Among various renewable sources, wind and solar energy resources are being harnessed mostly because of their abundant availability and emission-free

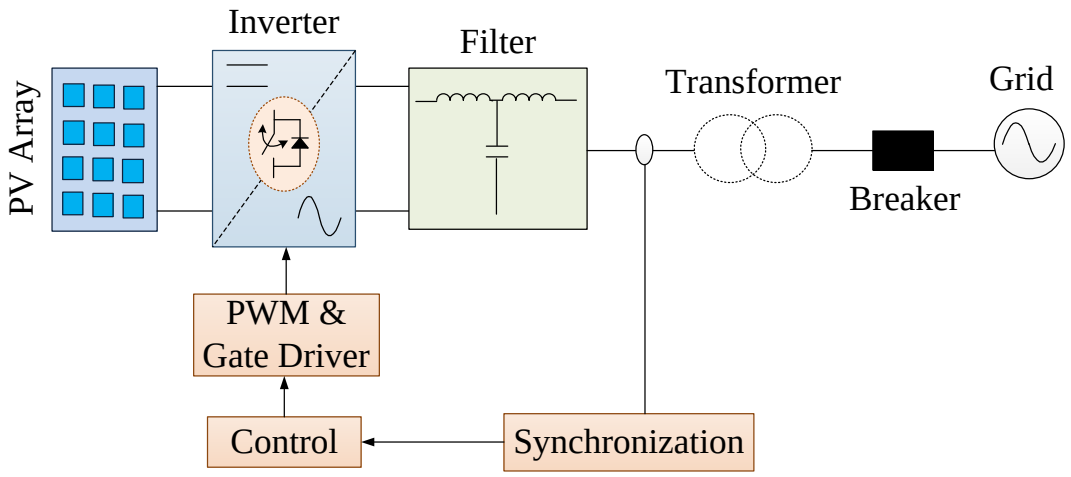


Fig. 1.2: *Typical arrangement of single-stage PV system*

conversion [3]. In addition, solar energy is characterized by advantages, namely more predictable output, modular space requirement, maintenance, and noise-free operation.

Nevertheless, the power generated from solar Photovoltaic (PV) is intermittent and largely depends on environmental conditions. The incident energy, the array temperature, and the PV voltage influence the extraction of solar energy. There is uncertainty around solar power due to changing weather and the season. The resulting stochastic nature will have a detrimental influence on the utility grid in grid-tied applications and loads in standalone mode.

1.2 TYPICAL ARRANGEMENT OF GRID-TIED PV SYSTEM

The key elements of the grid-tied PV system, presented in Fig.1.2, are PV array, inverter, and filter. These are briefed hereunder:

- **PV array:** The PV array is an interconnected arrangement of PV modules or panels that works as a single electricity-producing unit, whereas a large number of PV cells are connected in series to form a PV module [4, 5].

- **Inverter:** To transform the dc voltage produced by the PV array to ac voltage, inverters are used. The inverter is generally connected to the utility grid through a transformer. The inverter is usually controlled using carrier-based or space-vector-based Pulse-Width

Modulation (PWM) [6, 7]. Conversely, transformer-less inverter topologies have also been proposed in the literature and implemented for grid-tied applications.

- **Filter:** Modulation of inverter generates switched voltage waveform of the desired fundamental frequency (50 Hz in India). To separate the 50 Hz component from the other components, a filter is required between inverter output and grid [8].

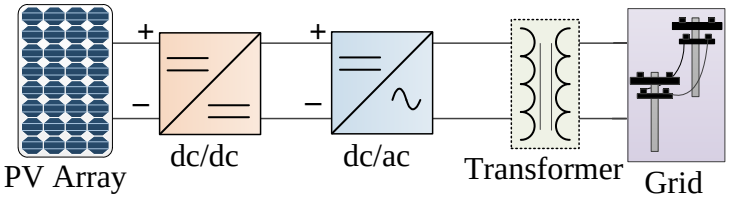
- **Controller:** A controller is an essential component that manages the flow of electricity between the PV system and the electrical grid. Its primary function is to ensure efficient operation, safety, and compliance with grid regulations [9].

1.3 POSSIBILITY OF DIFFERENT STAGES

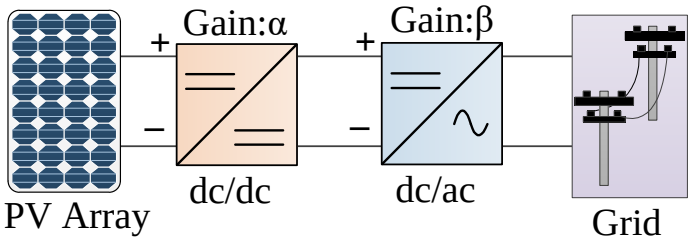
In the integration of solar PV systems with the electrical grid, two approaches are commonly used: PV to grid connected transformers and transformer-less systems [10, 11]. PV to grid connected transformers serve as intermediaries between the inverter output and the ac grid as shown in Fig. 1.3a. They step up the voltage to match the grid's requirements and synchronize power generation with the grid. On the other hand, transformer-less systems eliminate the need for a dedicated PV to grid connected transformer [12]. They directly convert dc power into ac power using dc-dc and dc-ac converter as shown in Fig.1.3b.

The choice between PV-to-grid connected transformers and transformer-less systems depends on the voltage requirement. To align the low PV voltage with the grid connection, a high-gain step-up transformer is used. In transformer-less system this gain can be achieved through a power electronics converter [13]. These systems are compact, cost-effective, and offer higher efficiency by eliminating energy losses associated with transformers.

In this system, consider a dc-dc converter with a gain of 'α' and a dc-ac inverter with a gain of 'β' , resulting in an overall gain of '$\alpha\beta$' [14]. Conventional ac-dc conversion topology (viz. a two-level full-bridge structure) operates with '$\beta = 1$' , requiring a high gain 'α' for the dc-dc converter to match the PV to grid voltage gain. However, this high-gain dc-dc converter increases the duty cycle and also enlarges the size of the inductor [15].



(a)



(b)

Fig. 1.3: *Grid-connected PV system based on (a) conventional two-stage with back-end transformer (b) conventional two-stage with front-end dc-dc boost converter*

The inductor value for this dc-dc converter can be determined using equation (1.1) [16].

$$L = \frac{(V_{\text{out}} - V_{\text{in}} + V_D) \times (1 - D)}{i_{\text{L}}|_{\text{pp}}^{\text{max}} \times f_{sw}} \tag{1.1}$$

Where, V_{out}: Output voltage of the dc-dc converter. V_{in}: Input voltage of the dc-dc converter. V_{D}: Voltage drop across the diode (if applicable). D: Duty cycle of the converter. $i_{\text{L}}|_{\text{pp}}^{\text{max}}$: Peak-to-peak current ripple in the inductor. f_{sw}: Switching frequency of the converter [15].

For boost dc-dc converter duty cycle (D):

$$D = 1 - \frac{V_{\text{in}}}{V_{\text{out}}} \tag{1.2}$$

If the dc-ac inverter with a value of 'β' greater than 1 is taken into account, the requirement for gain 'α' is reduced, which in turn decreases the size of the inductor in the dc-dc converter.

For dc-ac conversion stage, a Multilevel Inverter (MLI) is an advanced power conversion system that efficiently converts the dc output of renewable energy sources into grid-compatible ac voltage. By utilizing multiple voltage levels, it approximates a high-quality sinusoidal waveform, leading to enhanced efficiency, reduced harmonic distortion, and improved power quality [17]. This technology enables seamless integration of renewable energy systems with the electrical

grid, facilitating higher power transfer capabilities and promoting a more sustainable energy infrastructure. Conventional a MLI topologies, such as H-bridge, neutral point clamped, and flying capacitor-based topologies, are applicable for operation with gain '$\beta \leq 1$' . However, increasing the number of levels in these topologies requires an increase in the number of power devices and capacitors, thereby adding complexity to the power circuit. To increase the levels in the output waveform and reduce the switch counts with a gain of '$\beta > 1$' , a switched capacitors-based multilevel inverter has been designed and investigated [18].

1.4 KEY POWER CONVERTER FEATURES FOR PV TO GRID CONNECTED SYSTEMS

In a PV to grid-connected system, the power converter plays a crucial role in converting the dc power generated by the PV array into ac power that can be synchronized and fed into the electrical grid. Here are some key features of a power converter used in a PV to grid-connected system:

1. **Power factor:** A high power factor indicates efficient power usage and is desirable in grid-connected systems. Power converters in PV systems should be designed to maintain a high-power factor to minimize reactive power and optimize power transfer to the grid [19].

2. **Multilevel waveform:** Multilevel waveform helps to reduce a Total-Harmonic-Distortion (THD) and achieve better voltage regulation. Multilevel converters enable the generation of a staircase-like voltage waveform with multiple voltage levels, resulting in lower voltage stress on power devices and improved power quality for grid-connected systems [17, 20].

3. **Self-balancing:** As the levels of output waveforms increase, the dc source or capacitors experience challenges in maintaining a balanced output voltage. To address this issue and achieve voltage balancing, a converter self-balancing features offers a viable solution [21].

4. **Fault detection possibilities:** Fault detection is crucial for ensuring the safe and reliable operation of the electrical systems. These capabilities enable early detection of faults, facilitate prompt intervention, and contribute to system reliability, efficiency, and longevity [22].

5. **Self-boost:** The self-boosting capability is a crucial aspect of power converters in grid-connected PV systems. As it is necessary to boost the PV voltage, which typically done either by using dc-dc converter or a transformer. However, these components introduce added complexity to the circuitry and necessitate the inclusion of supplementary sensors. Therefore, having a self-boosting capability within converters becomes an essential requirement [23].

In order to fulfill these requirements, there is an opportunity to explore the potential of a multilevel inverter for integrating PV into the grid. A MLI possesses the capability to achieve the first two features mentioned. Among the various types, a special class known as the switched capacitor-based multilevel inverter stands out as it can achieve all the desired features, including self-boost. The objectives of this thesis are therefore identified as the investigation and development of the Switched Capacitors based Multilevel Inverter (SCMLI). Furthermore, a comprehensive review of MLIs (presented in the next chapter) highlights several challenges, among which the most significant is voltage balancing of the capacitors and incorporating self-boosting features, which are particularly suitable for PV-to-grid connected systems.

1.5 RESEARCH OBJECTIVES

The research work entitled **Investigations on Switched Capacitors based Multilevel Inverters for Grid Connected Photovoltaic Power Generation Systems** is carried out with the following objectives:

1. To investigate various topologies of switched-capacitor based multilevel inverters in the light of their suitability for grid integrated photovoltaic systems.

2. To conceptualize and design an interface for a grid-connected photovoltaic system with switched capacitor based multilevel inverter. To design multilevel converter interface for electric vehicle charging.

3. To develop a control methodology and experimentally verify the developed interface.

1.6 THESIS ORGANIZATION

The thesis is organized into seven chapters. It summarizes the specific contributions directed in achieving the above objectives and facilitate the presentation of the results obtained during this research. The brief description of these chapters is outlined as follows:

- **Chapter 1: Introduction**
  A brief introduction of the participation of the solar PV system on the total power generation and the general structure of the grid-tied PV system have been presented. The state-of-the-art in the field of research is addressed. This chapter also enlists the objectives of the present study and outlines the organization of the thesis.

- **Chapter 2: Literature Review**
  This chapter provides a comprehensive review on emergence of SCMLI. The MLI are also classified as single and multiple sources. The summary of research gaps, identified research objectives and thesis organization is also presented.

- **Chapter 3: Design of SC based Five-Level Inverter for Grid Connected PV System**
  This chapter deals with the analysis of a SC based five-level inverter for grid connected PV system. Design and self-balancing of capacitors voltage are discussed. Furthermore, a brief comparison with the recent topologies has been described. Finally, experimental results are presented to verify theoretical and simulation findings.

- **Chapter 4: Design of SC based Seven-Level Inverter for Grid Connected PV System**
  This chapter investigates the performance of a SC based seven-level inverter for grid connected PV system. The working principle of the proposed topology is explained and important mathematical formulations are presented. A comparative analysis has been presented to prove its superiority. Further, theoretical and simulation are validated experimentally.

- **Chapter 5: Design of SC based Nine-Level Inverter for Grid Connected PV System**
  This chapter presents the describes a nine-level SCMLIs with reduced device count and voltage stresses. Experiments have been conducted to validate the proposed topology. Additionally, a detailed comparison of state-of-the-art topologies has been made to prove the merits.

- **Chapter 6: Design of 3-ϕ SC based MLI for grid-connected PV system**

  This chapter investigates the presents a three-phase thirteen level SCMLI with a reduced device count is presented. Working principles and comparisons with the recent topologies are discussed in detail. To prove the efficacy and feasibility of the suggested topology, simulation and experimentation have been carried out.

- **Chapter 7: Main conclusions and scope for future work**

  This chapter presents a summary of the conclusions of the studies presented in previous chapters. Moreover, the scope of further research is also summarized in this chapter.

Chapter–2

Literature Review

2.1 GENERAL

The dc-ac conversion stage is an essential component of the PV to grid connected system and is responsible for converting dc input voltage into levelled ac voltage with high power factor and low harmonic distortion. The levelled Voltage fed to the grid through filtering components (inductors and/or capacitors) to match the grid voltage and grid current. The typical constituents of the inverter system are shown in Fig. 2.1, The aim is to modulate the power converter in a manner that the current 'I_g' injected to the grid acquires a sinusoidal shape and is in phase with the grid voltage

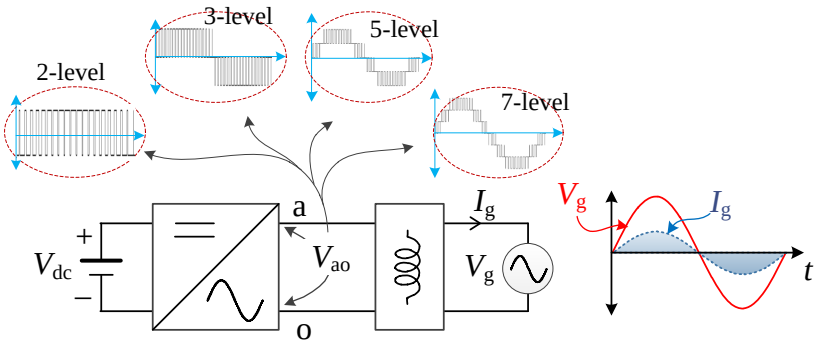


Fig. 2.1: *The typical constituents of the inverter system*

Grid current 'I_g' is controlled by controlling the terminal voltage V_{ao}, and with a better harmonic profile of V_{ao}, a much-improved shape of 'I_g' can be achieved [19]. MLI are based on the fact that a grid-connected voltage source inverter synthesizes a voltage to control the grid current. If the levelled voltage is improved by increasing the number of voltage levels, the grid

current can be consequently improved [17], as shown in Fig. 2.2. Inverter output voltage can be as high as 'N_L' levels, as shown in Fig. 2.2. MLIs offer numerous advantages, some of which are [24, 25]:

- **Advantages based on waveform:** include lower voltage ratings of power switches, a much better harmonic profile of the ac waveform, reduced dv/dt stress, small passive components, possibility of fault-tolerant operation, and so on.
- **Advantages based on topology:** Possibility of three-phase extension, include bidirectional operation, boost output voltage and so on.

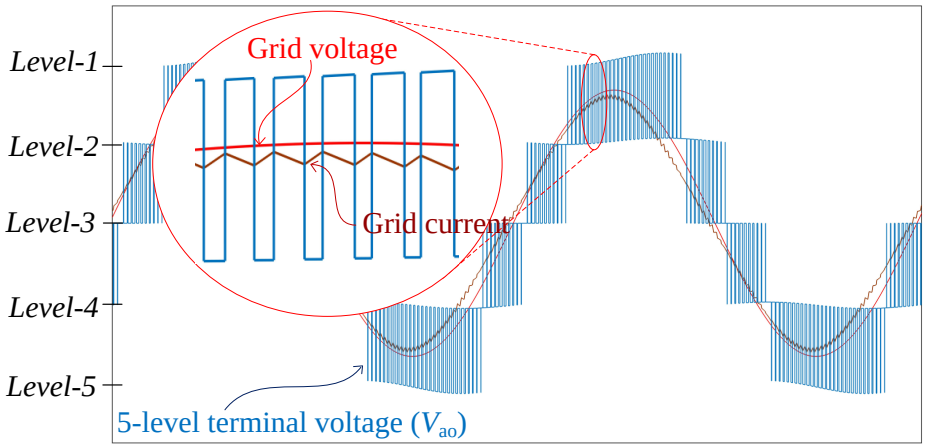


Fig. 2.2: *Waveform of improved level voltage*

Due to these advantages of MLIs, it is widely used in industries. To assess the effectiveness of MLIs, several parameters are considered. These evaluation criteria include:

1. **Resolution of the output waveform (number of levels, N_L):** A higher resolution multilevel waveform can reduce the output filter requirement, improve the lifetime of the load due to less dv/dt stress, and enhance efficiency by improving the harmonic profile of the load current [26, 27]. However, a higher resolution output may also increase the component count.
2. **Total component count:** Increasing waveform resolution and voltage gain may result in an increased component count, which can increase the volume, complexity, and losses in the system [28]. The component count includes the number of input dc sources (N_{IS}),

number of transistor switches (N_S), number of main and auxiliary diodes (N_D and N_{AD}), number of gate drivers (N_{GD}), and number of capacitors (N_C).

3. **Total Standing Voltage (TSV):** The overall semiconductor requirement and its cost are reflected in the TSV of the topology, which is obtained by adding the Peak Inverse Voltage (PIV) of all power switches and auxiliary diodes [29].

4. **PIV of power switches with respect to the operating voltage:** A topology with even a single switch that has a large PIV requirement is limited in its applicability to high-voltage, high-power applications [30]. It is desirable to keep PIV of all switches as low as possible compared to the operating voltage.

5. **Effective balancing of capacitors at various modulation indices:** The ease of voltage balancing of capacitors is an essential feature of SCMLIs and should be retained at all values of the modulation index [21, 31].

6. **Voltage-gain (β):** A higher voltage gain can decrease or eliminate the need for boosting before the input dc-link [18]. However, a higher gain may increase the component count and result in higher PIV of power switches.

Of these features, the ones discussed in (1) to (6) above can be quantified in terms of a Cost Function (CF) defined in [32].

$$CF = \frac{N_{IS}}{N_L} \times \left[N_S + N_D + N_A + N_{GD} + N_C + \left(\frac{\alpha \times TSV}{\beta} \right) \right] \tag{2.1}$$

The parameter 'α' is a weighting factor to determine the relative importance of TSV versus component count. A lower CF value corresponds to more favourable structural characteristics of the topology. Numerous authors have relied on CF as a means of assessing MLIs.

2.2 CLASSIFICATION OF MULTILEVEL INVERTERS

There are two primary classifications for MLIs: single-source topologies and multiple-source topologies. These categories can be further subdivided into single-phase and three-phase topologies. Within the single-source topologies, both single-phase and three-phase systems

are divided based on the gain of the respective topologies, as illustrated in Fig. 2.3.The basic conventional MLI topologies are Diode Clamped (DC) (Neutral Point Clamped (NPC), Flying Capacitor (FC)s and Cascaded H-bridge (CHB)s MLIs [33].

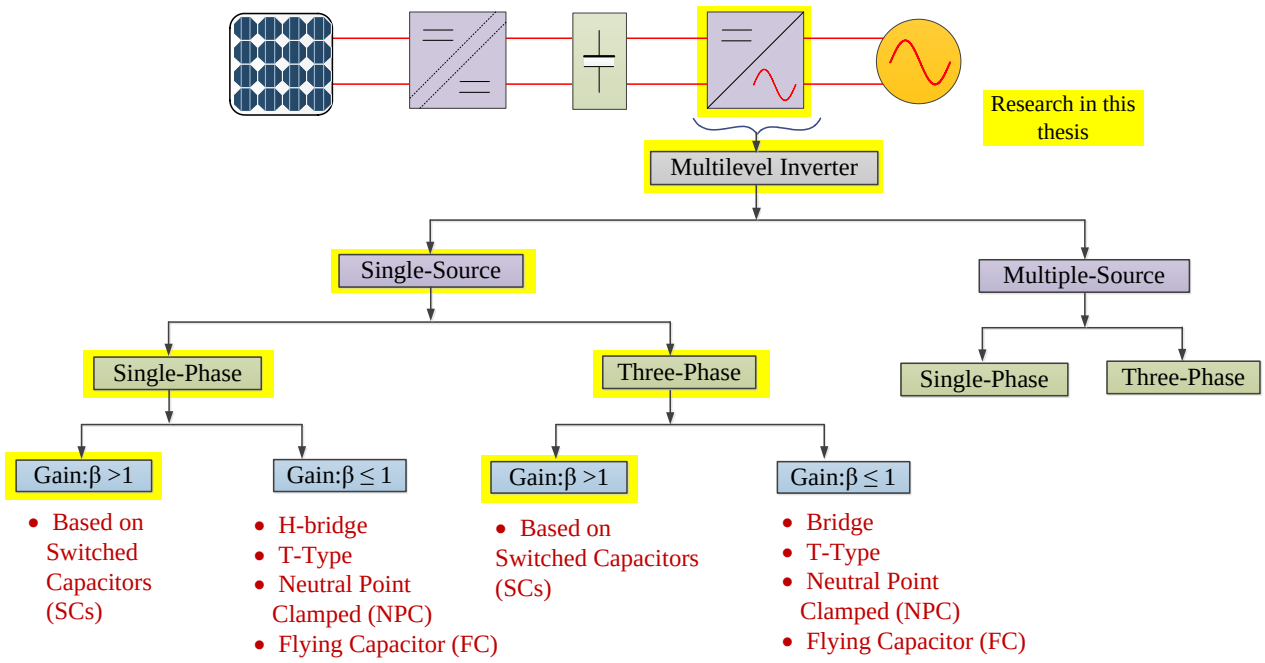


Fig. 2.3: *A classification of multilevel inverters*

2.2.1 Diode Clamped Multilevel Inverter (DCMLI)

The MLI topology for induction motor drives was proposed in the year 1981 by Nabae, Takahashi and Akagi [34]. The three level and five-level DCMLI structures are shown in Fig. 2.4. The DCMLI consists of dc bus capacitors, switches and clamping diodes. For an N_L-level inverter, the number of dc bus capacitors required are (N_L-1), number of clamping diodes is $(N_L-1)\times(N_L-2)$ and $2\times(N_L-1)$ switches. The voltage across each dc bus capacitor is $\frac{V_{dc}}{N_L-1}$. The drawback of diode clamped inverter is, it requires more number of clamping diodes. The reliability issues of this inverter are increases as the number of voltage levels increases because of more number of devices. In case of isolated voltage sources (instead of capacitors) the power balancing is an issue due to unequal load sharing. Moreover, in this topology, the voltage gain (β) is limited to 1.

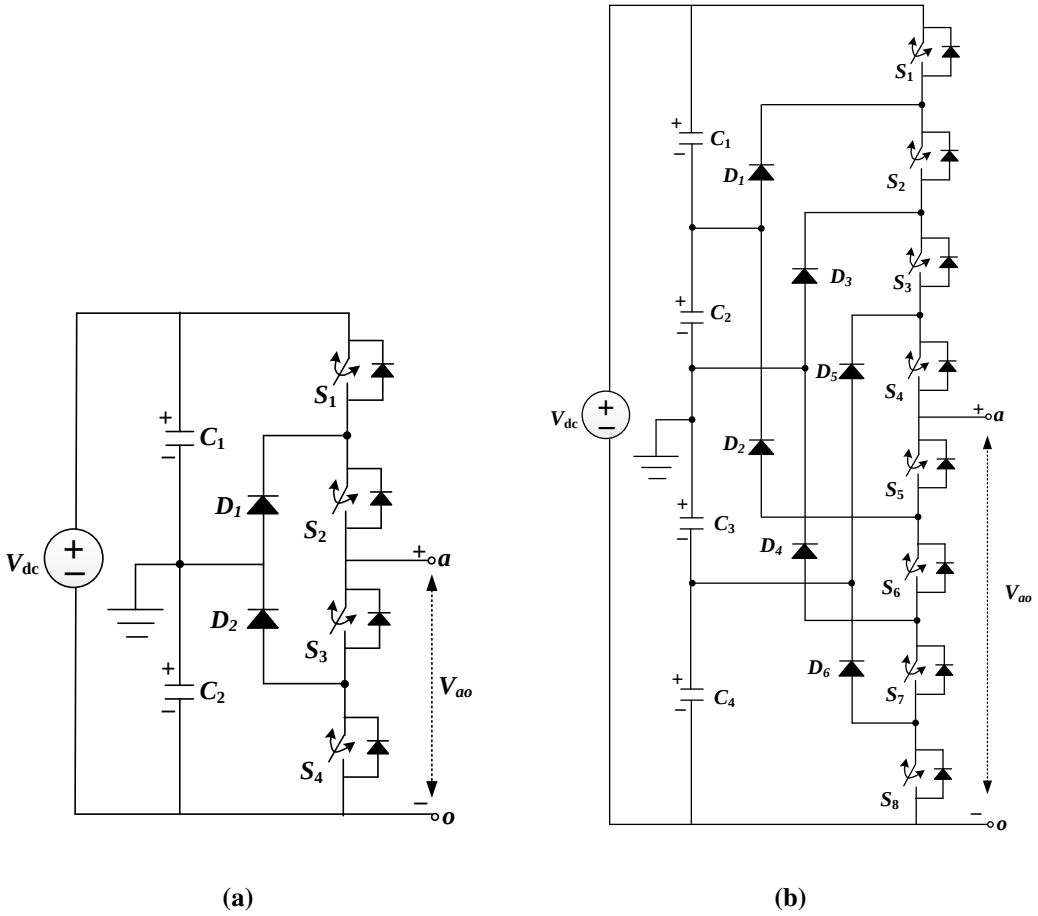


Fig. 2.4: *DCMLI topology (a) three-level (b) five-level*

2.2.2 Flying Capacitor Multilevel Inverter (FCMLI)

The Flying Capacitor Multilevel Inverter (FCMLI) was introduced by T.A Meynard and H.Foch in the year 1992 [35]. N_L-level FCMLI inverter requires (N_L-1) dc bus capacitors, $2\times(N_L-1)$ switching devices and $\frac{(N_L-1)\times(N_L-2)}{2}$ clamping capacitors. The three level and five-level FCs inverters are shown in Fig. 2.5. This topology does not require any clamping diodes, but it requires more number of capacitors. These capacitor voltages should be controlled within allowable voltage ripple. Here redundant switching states are possible for middle voltage levels. A large number of dc capacitors with pre-charging circuits. The inverter requires several banks of dc flying capacitors with different voltage ratings, each of which needs a separate pre-charging circuit. Furthermore, within this topology, the voltage gain (β) is constrained to a value of 1.

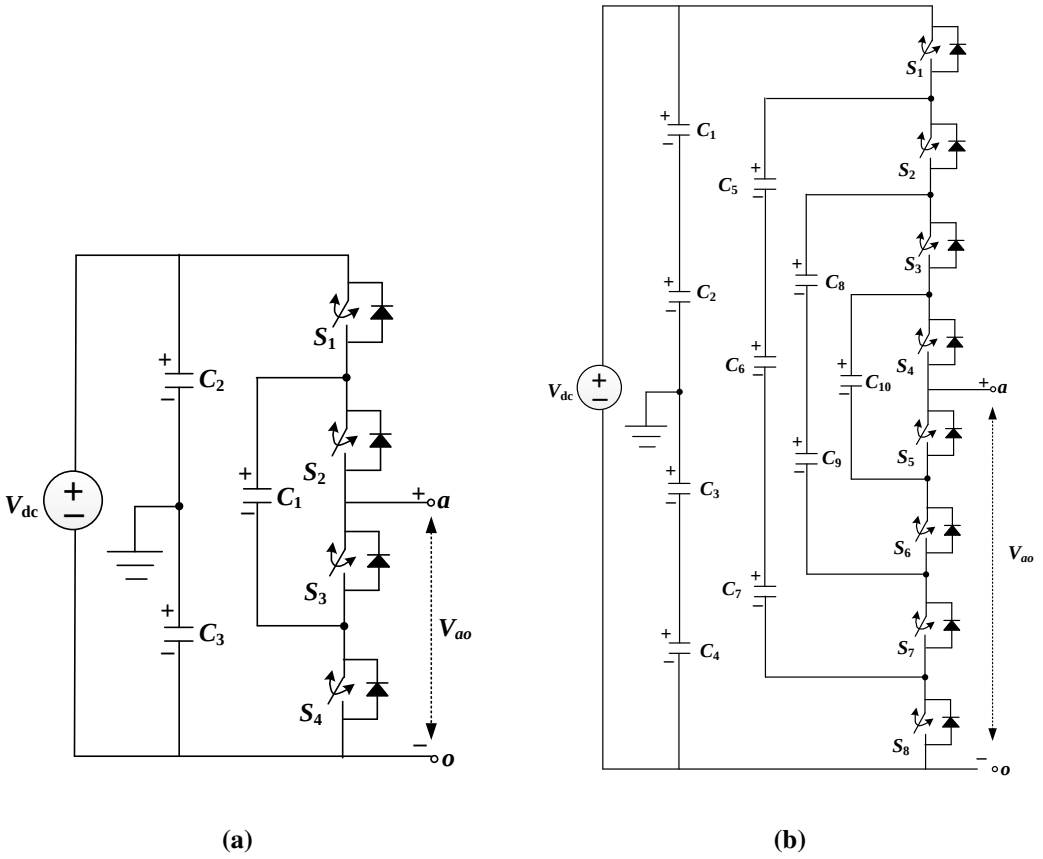


Fig. 2.5: *FCMLI topology (a) three-level (b) five-level*

2.2.3 Cascaded H-Bridge Multilevel Inverter (CHBMLI)

CHB MLI is another popular topology for high-power medium voltage drives [36–38], because it doesnt have capacitor voltage unbalancing issues. The three level H-bridge and five-level CHB inverters are shown in Fig. 2.6.

The CHBMLI have several notable features. Firstly, it employs a modular structure consisting of multiple units of identical H-bridge (HB) power cells, which effectively reduces manufacturing costs. Additionally, the inverter's output voltage waveform comprises multiple voltage levels with small voltage steps, resulting in significantly lower THD and rate of change of voltage (dv/dt) compared to a two-level inverter. Moreover, the CHBMLI allows for high voltage operation without the need for switching devices in series. By connecting the H-bridge power cells in cascade, it achieves high ac voltages while avoiding the challenges associated with equal voltage sharing among series-connected devices.

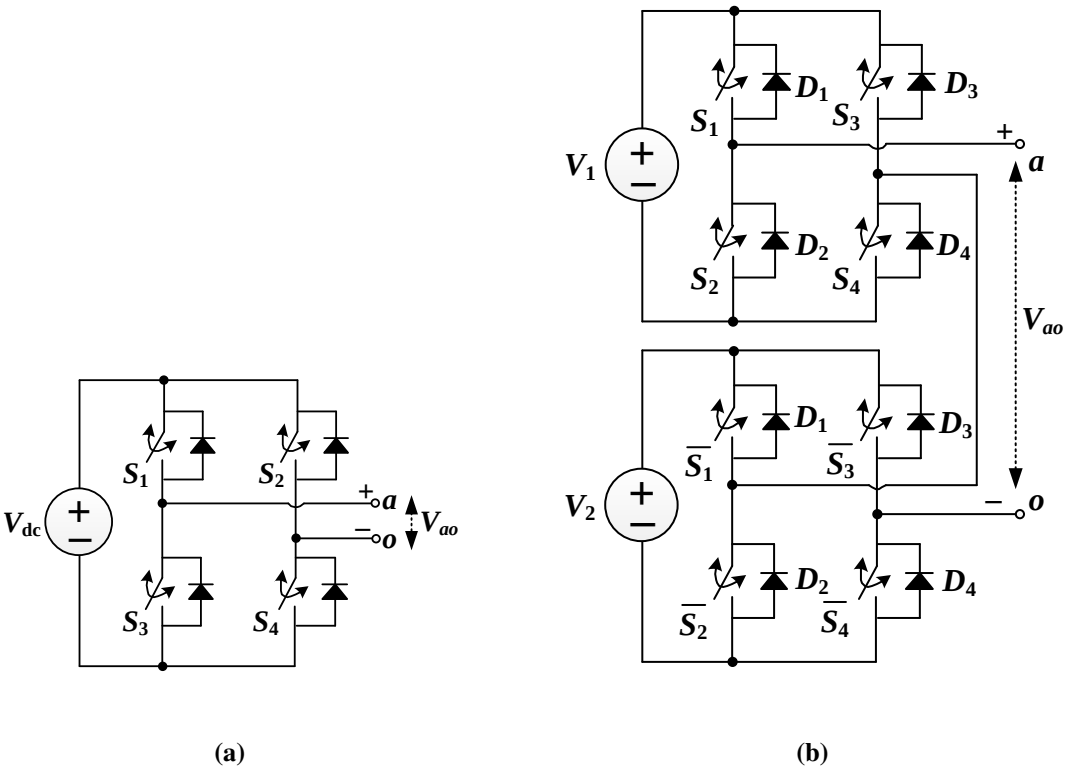


Fig. 2.6: *CHBMLI topology (a) three-level (b) five-level*

There are several drawbacks associated with the CHB inverter. Firstly, it requires multiple isolated dc supplies. Additionally, it can lead to unequal dc voltages, resulting in the loss of the merits offered by the modular structure. Furthermore, designing the switching pattern becomes more challenging due to the reduction in redundant switching states. Moreover, the voltage gain is limited to 1. As a result, this inverter topology has limited applications in the industrial sector. As all these conventional multilevel topologies have a large number of devices, researchers are also investigating reduced device count MLIs, which will be further discussed in the next subsection.

2.3 INVERTER TOPOLOGIES WITH REDUCED NUMBER OF SWITCHES

In literature, many MLI topologies with reduced number of components for achieving higher number of voltage level is presented [39]. In Fig. 2.7 five-level inverter topology is presented for multistring Distributed Energy Resources (DER), it requires six semiconductor devices

whereas conventional MLI topologies require eight semiconductor devices. Thus it also requires less number of driver circuits and components compared to conventional MLI topologies. Furthermore, within this topology, there exists a limitation where the gain β is restricted to unity and it requires multiple isolated dc supplies.

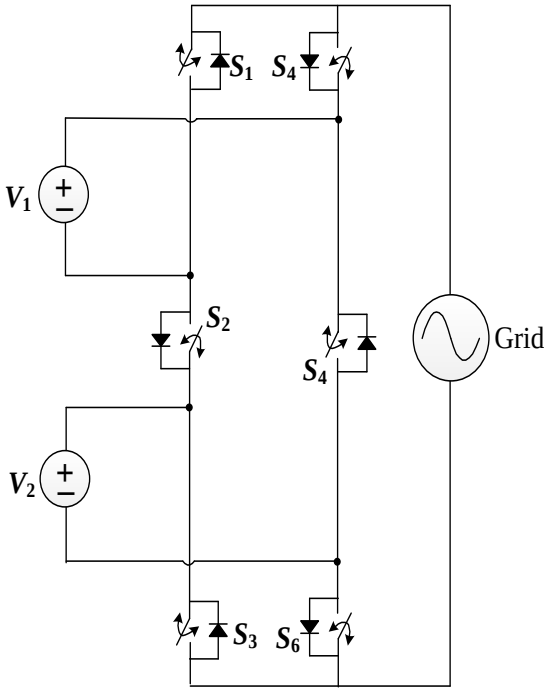


Fig. 2.7: *Single phase multistring five-level inverter topology*

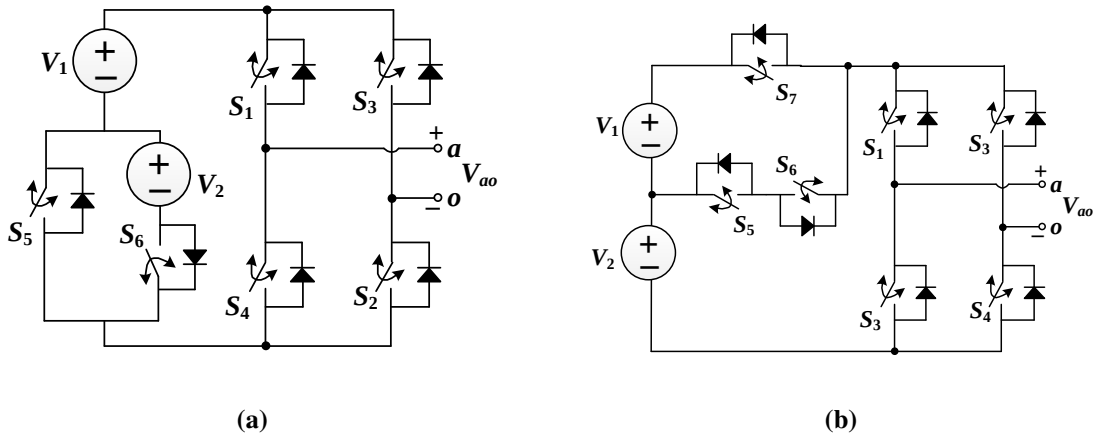


Fig. 2.8: *Single phase five-level inverter configuration*

The single phase five-level inverter topologies are proposed in [40, 41] with less number of components as compared to conventional five-level inverter topologies. The five-level inverter

topology presented in [40] is formed by one H-bridge cell and two extra switches connected between sources, as shown in Fig. 2.8a. However, this topology is unable to generate output voltage at load under HB switch failures. Another interesting five-level inverter topology is presented in [41], which is formed by one HB cell, one unidirectional switch and bidirectional switch, as shown in Fig. 2.8b. The bidirectional switch is capable of conducting current and blocking voltage in both directions. This bidirectional switch is currently available in markets as a module. This module requires only one isolated power supply instead of two for the gate driver. The topology requires same number of gate drive circuits as the topologies presented in Fig. 2.8. Furthermore, in both topologies, the voltage gain is constrained to a maximum value of 1.

All the discussed topologies have certain drawbacks, such as a high component count, the necessity for capacitor voltage balancing, the need for separate isolated dc supplies in the case of multisource topologies, and a maximum voltage gain limited to unity. To address these challenges and achieve voltage gains beyond unity, researchers have been investigating Switched Capacitor (SC) based topologies [42]. These SC-based topologies consist of various SC units, which play a crucial role in increasing the voltage levels and aiding in boosting the output voltage. These units further explored in the next section, provide promising solutions to mitigate the aforementioned issues.

2.4 SWITCHED CAPACITORS (SC) UNITS

The fundamental building block of an "SC unit" comprises a dc source along with diodes, capacitors, and switches. The available SC units can be classified into three distinct sub−groups: series−parallel SC (SPSC) units [28–30, 43–48] ; SC voltage doubler units [49–53]; and SC half−mode units [54–59]. Overview of these essential SC units, and their specific details are elaborated in the subsequent subsections.

2.4.1 Series−Parallel (SPSC) units

So far, numerous SCMLIs have utilized SPSC units as the main circuits, employing two distinct configurations. Type-I of this unit, as depicted in Fig. 2.9, necessitates two switches, one capacitor, and a single power diode [28–30, 47]. Assuming V_{dc} represents the input dc source value, the

output can generate two discrete positive-voltage levels: V_{dc} and $2V_{dc}$. SPSC Unit-II, illustrated in Fig. 2.10, operates on the same principle of capacitor charging/discharging, but it employs an additional capacitor and a power switch instead of a diode and a four-quadrant switch (T) [43–46].

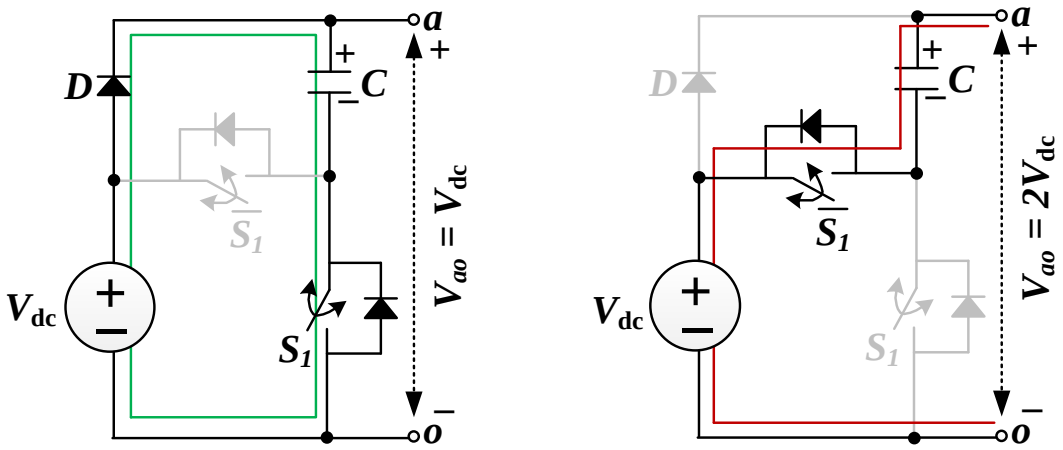


Fig. 2.9: *Operation of the capacitor in SPSC Unit-I during the (a) charging state and (b) discharging state*

The key distinction between these two fundamental units is that SPSC Unit-I lacks bidirectional power flow capability. Furthermore, unlike SPSC Unit-I, the discrete voltage levels in SPSC Unit-II are generated using the charged capacitor voltages, thereby preventing any dc offset during the generation of output voltage levels in SCMLIs. Depending on the configurations of certain developed SCMLIs, four-quadrant power switches, with a back-to-back connection of two standard MOSFETs, can be used in place of paralleled normal power switches in SPSC Unit-II [45, 60]. The maximum voltage rating of all semiconductor devices in both types of SPSC units remains within the voltage range of the input dc source.

2.4.2 SC Voltage Doubler Unit

The SC voltage doubler unit [49–52], is a two-port converter that comprises a single dc source, two capacitors, two complementary power switches, and two power diodes. Similar to the basic

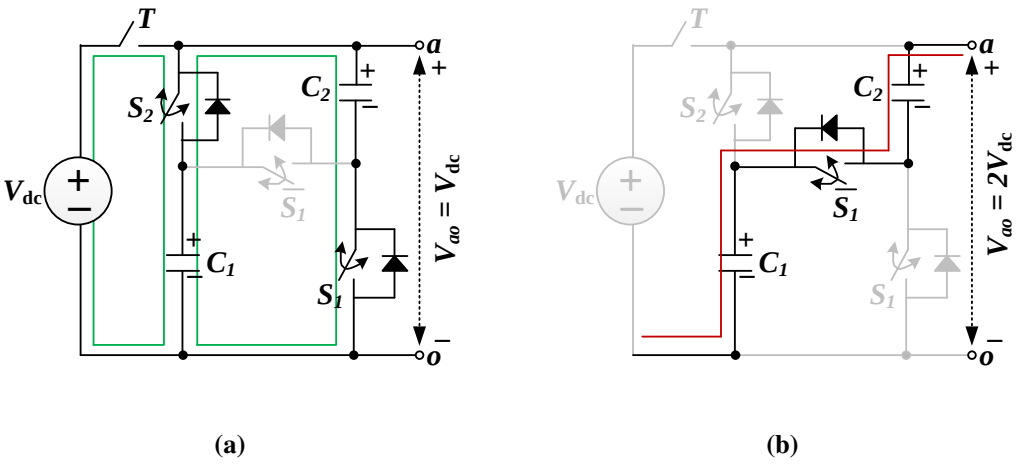


Fig. 2.10: *Operation of the capacitor in SPSC Unit-II during the (a) charging state and (b) discharging state*

SPSC units, both capacitors are charged in parallel to the input dc source, as illustrated in Fig. 2.11. Consequently, all the semiconductor components involved must tolerate the same Maximum Voltage Stress (MVS). Each capacitor has a diode and a power switch in its charging path since it is a two-port SC-based basic unit. This configuration allows for the generation of five output dc-link voltages: $0V_{dc}$, $\pm V_{dc}$, and $\pm 2V_{dc}$. While this basic SC unit offers operational flexibility, it lacks bidirectional power flow capability. To address this limitation, a modified version of the SC voltage doubler unit has been proposed in [53], which replaces the diodes with four-quadrant power switches. However, this enhancement comes at the expense of additional semiconductor devices.

2.4.3 SC Half–Mode Units

The possibility of charging the dc-link capacitors to a fraction of the input dc-source voltage can be achieved using SC half-mode units. Recently, various types of SC half-mode units have been introduced. Considering Fig. 2.12, which pertains to the capacitors' charging process in the SC half-mode Unit-I described in [54], it is evident that this unit requires four dc-link capacitors, two complementary switches, and two diodes to produce two discrete fixed values of dc-link voltages at its output. When it comes to charging each of the two dc-link output capacitors, only one diode and one power switch are involved.

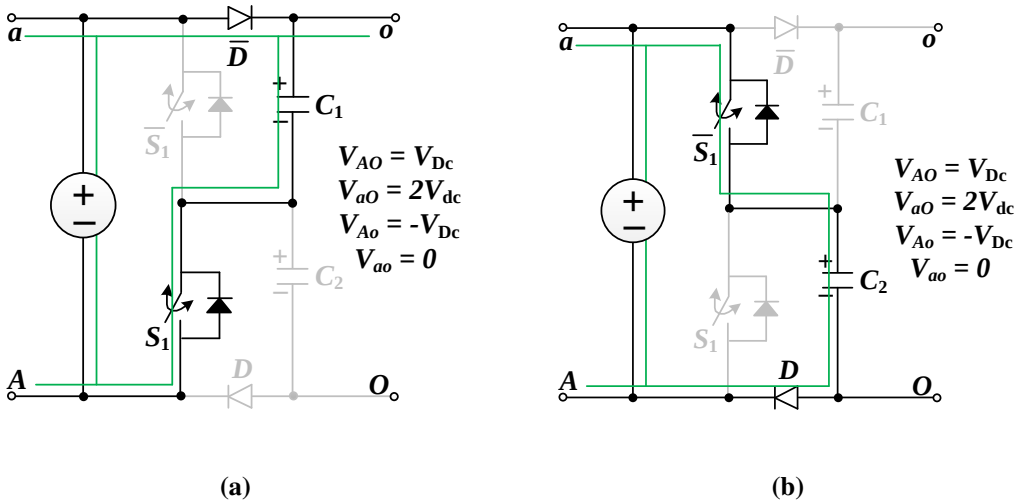


Fig. 2.11: *Charging operation of the capacitors in the SC voltage doubler unit (a) for C_1 and (b) for C_2*

The structure presented in [55] utilizes three power switches and the same number of power diodes as [54]. The capacitor charging operation of this structure is depicted in Fig. 2.13a. Referred to as SC half-mode Unit-II, this structure charges each involved capacitor at half the value of the main dc-link voltage through a capacitive charging path consisting of two diodes and a single power switch. The charging current of the capacitors is denoted as "i_{ch}" Another variant of SC half-mode unit capable of generating four identical positive dc-voltage levels at its output ($0.5V_{dc}$, V_{dc}, $1.5V_{dc}$, and $2V_{dc}$) is introduced in Fig. 2.13b [56]. As evident from the capacitor charging flow path in Fig. 2.13b, two capacitors are charged in parallel to the input dc source, while three power switches are integrated into the charging flow path. A similar multi-output SC-based basic unit employing half-mode operation of the capacitors is also proposed in [57, 58].

The final configuration in this family of SC-based basic units is a K-type converter presented in [59]. This unit offers two charging paths for the capacitors, as illustrated in Fig. 2.14. Similar to SC half-mode Unit-I, this structure also requires four dc-link capacitors and can produce two identical positive voltage levels, each being a quarter of the main dc-link voltage. In all SC-based half-mode units, capacitors C_1 and C_2 need to be connected in series and then parallel to the main dc-link capacitors, C_a and C_b , through several semiconductor devices for the purpose of charging. Consequently, considering the internal parasitic resistance of each dc-link capacitor, known as the "Equivalent Series Resistance (ESR)", a higher impedance can

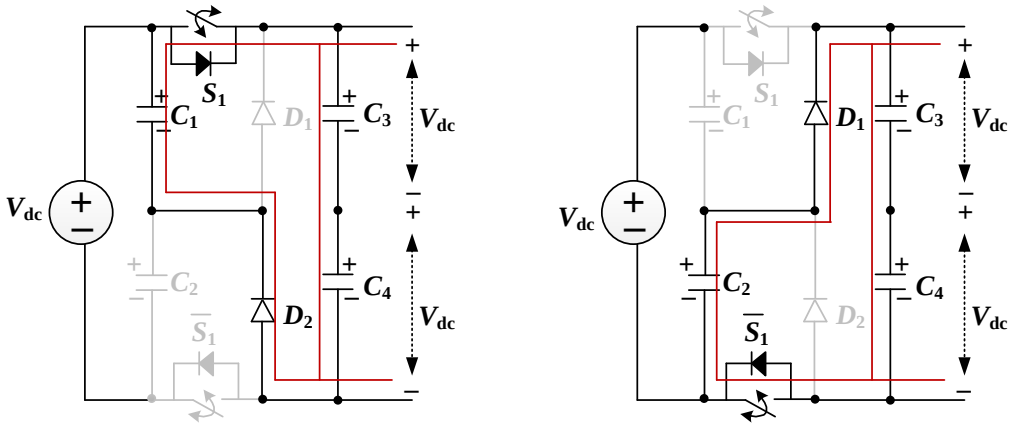


Fig. 2.12: *Charging operation of the capacitors in the SC half-mode Unit-I (a) discharging path of C_1 (b) discharging path of C_2*

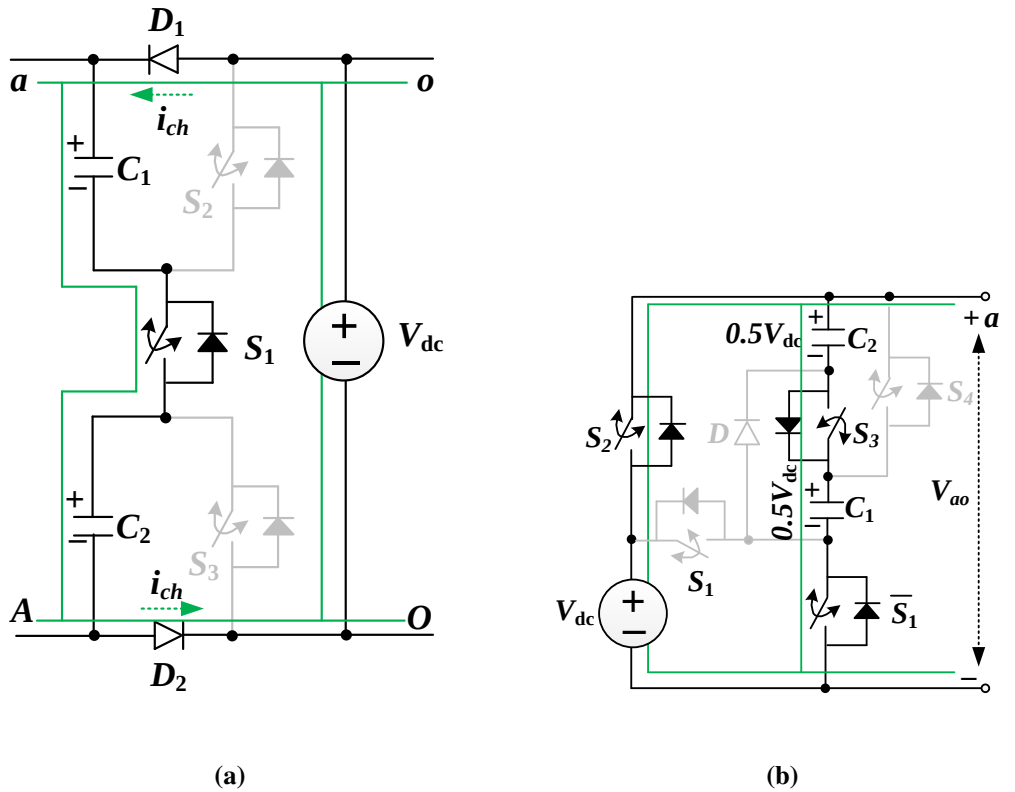


Fig. 2.13: *Charging operation of the capacitors in (a) SC half-mode Unit-II and (b) SC half-mode Unit-III*

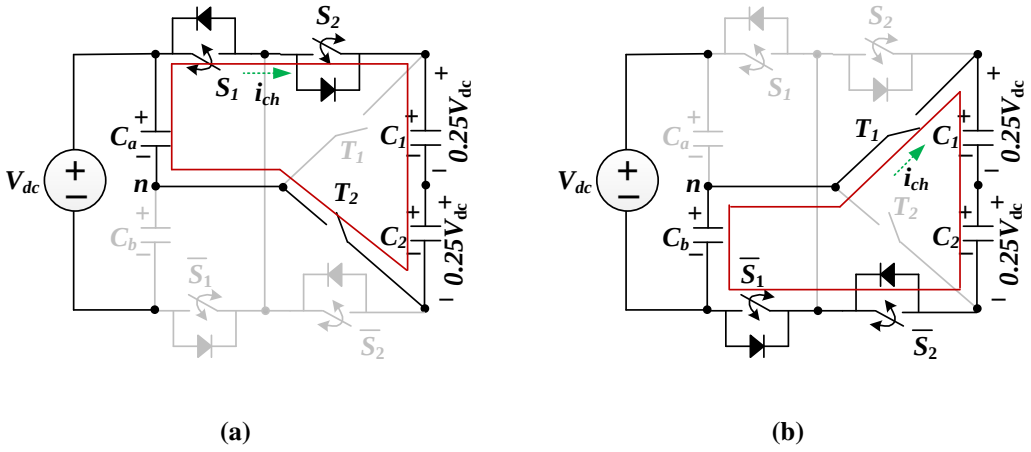


Fig. 2.14: *Charging operation of the capacitors in SC half-mode unit K-type. (a) discharging path of C_1. (b) discharging path of C_2.*

be introduced into the charging loop of the capacitors compared to other types of SC basic units. This elevated impedance assists in mitigating the charging current of the capacitors. Various topologies have been proposed in the literature by combining these SC units with conventional multilevel structures. This thesis analyzes these topologies, evaluates their suitability for PV to grid-connected systems, identifies their drawbacks, and introduces novel topologies that effectively overcome these limitations. These novel topologies are specifically designed for grid-connected applications and offer enhanced performance. The identified research areas and contributions are discussed in the next sections.

2.5 IDENTIFIED RESEARCH AREAS

After a review of the SCMLI topologies, the following areas have been identified for further investigations in this research work:

- Compared to conventional MLI, MLIs offer several advantages such as lower voltage ratings for power switches, a much better harmonic profile of the output waveform, reduced dv/dt stress, and the possibility of fault-tolerant operation. Therefore, a scope is identified to investigate the multilevel inverters, especially for their application in PV based power generation systems.

- Conventional MLIs topologies has ability to achieve only unity voltage gain. Therefore, this constraint has led to the identification of a promising area for further exploration and research in the development of MLIs with enhanced voltage gain capabilities.

- Existing MLIs require multiple capacitors for voltage regulation. Balancing these capacitors necessitates the use of multiple sensors, which adds to the complexity of controller in signal processing. Self-balancing of these capacitors is achieved by switched capacitor technique. Therefore, the scope is identified to develop a SCMLIs that can reduce the sensor requirements and the controller complexity.

- Modular dc-ac conversion is preferred because of its scalability and ability to augment configurations for higher voltage and current ratings. Furthermore, it enables easy extension to three-phase applications. Thus, the scope is identified to implement a modular topology for easy extension to three-phase systems.

2.6 RESEARCH CONTRIBUTION

The investigations have been carried out in the identified research areas to achieve the research objectives. The specific contributions to accomplish those research objectives are presented herewith and these different contributions are interpreted with simple schematics in Fig. 2.15.

- **Design of Switched Capacitors based Five-Level Inverter for Grid Connected PV System**

  In this study, a novel five-level grid connected inverter is presented that effectively reduces CF by utilizing only six unidirectional switches and a single diode with a switched capacitor. This configuration eliminates the requirement for multiple isolated dc sources. The proposed topology can achieve a voltage boost of up to twice the input voltage, generating a synthesized five-level waveform with high resolution and inherent voltage balancing of the capacitor. The operation and performance of proposed topology is ascertained through simulations and verified experimentally. This topology has limitation as it has a high PIV on the switches exceeding the operating voltage.

- **Design of Seven-Level Inverter for Interface with Grid-Connected PV System**

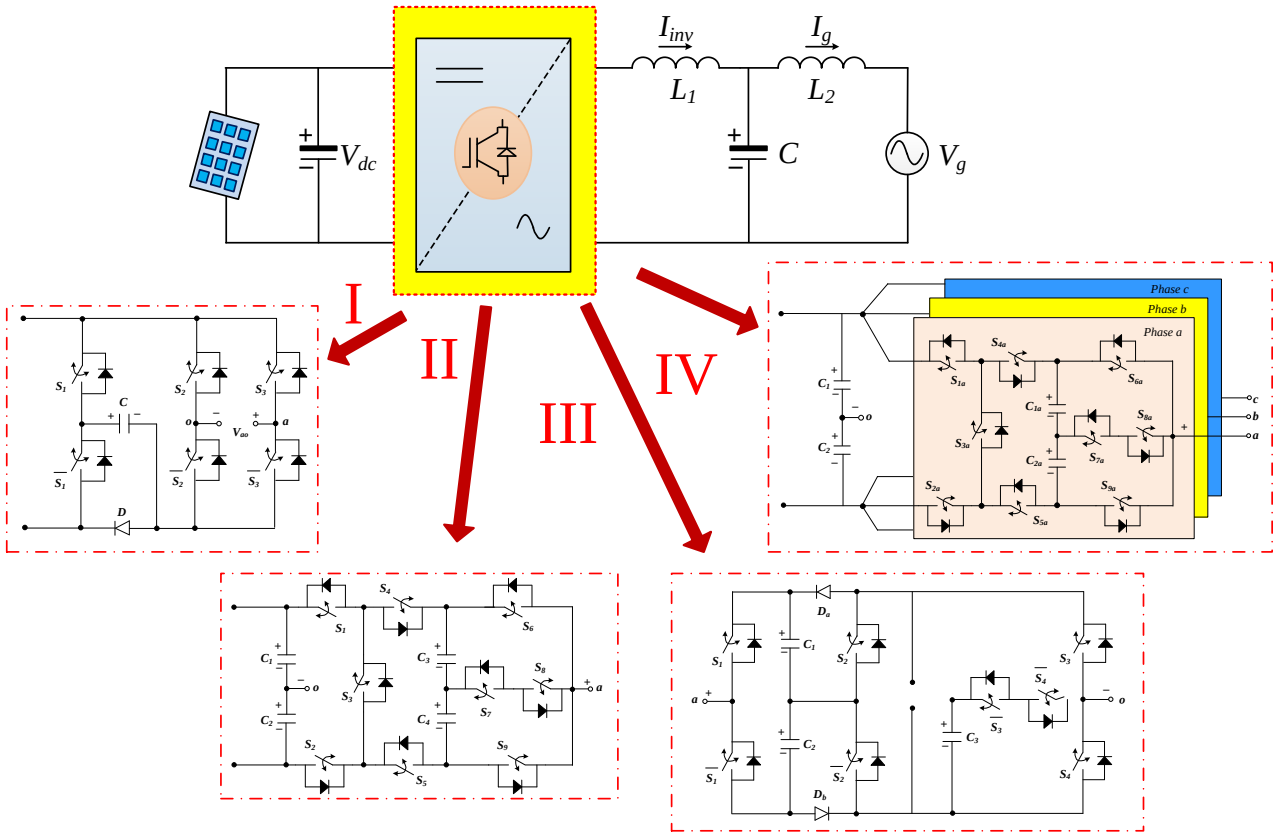


Fig. 2.15: *An illustrative simple schematic for the different contributions in this thesis*

In order to address the limitations of proposed five-level inverter a second proposed topology named as SC based seven-level inverter is presented. The proposed topology offers voltage boosting capability of up to 1.5 times the maximum voltage level of the input dc voltage, without imposing high voltage stress on any power switches. Therefore, PIV of all switches are within operating voltage. Capacitors are balanced through the charging and discharging phenomenon, eliminating the need for voltage balancing. Simulation studies are carried out and the experimental validation are obtained. In the topology, however due to non-complimentary switches the number of gate driver increases and it increases the CF.

- **Design of Switched Capacitors based Nine-Level Inverter for Grid Connected PV System**

  A new self-balancing nine-level inverter is presented which overcomes the limitations of previous topologies. This inverter is capable of producing a nine-level voltage with a gain of two, using only a single dc source, eight power switches, three capacitors, and

two diodes. The proposed topology ensures that the capacitor voltages remain inherently balanced, eliminating the need for additional circuitry. The complementary nature of the switches reduces the number of gate drivers required, resulting in a decreased CF. Additionally, this topology can be expanded to achieve a higher voltage gain and a greater number of levels in the output voltage. With a reduced number of switches and sources, it generates a high number of levels, and its output voltage has a better harmonic profile, which means it requires a smaller filter size. Furthermore, this proposed topology is highly reliable. Validations are made through simulations and experimental studies.

- **Design of 3-ϕ switched capacitor based MLI for grid-connected PV system**

  This work introduces an extension to a seven-level multilevel inverter proposed in this work, which results in a 3-ϕ thirteen-level inverter. This inverter is unique because it can balance and boost its own voltage using only one dc voltage source and two dc-link capacitors. Each phase of the inverter comprises of nine power switches and two capacitors. A simple modulation technique is used to generate seven voltage levels as a phase voltage and thirteen as a line voltage. The proposed topology has voltage boost capabilities, with a gain of three, as well as inherent voltage balancing capabilities of the capacitors. Additionally, it has a lower device count and lower PIV on switches. Simulation studies have been carried out, and experimental validation.

Chapter–3

Design of Switched Capacitors based Five-Level Inverter for Grid Connected PV System

3.1 GENERAL

This chapter presents a novel switched capacitors based five-level inverter designed for grid-connected PV systems. The inverter utilizes six unidirectional switches, one diode, and a single switched capacitor, and employs a simple modulation technique to generate optimal switching pulses. Comparative analysis with existing topologies shows that the proposed inverter requires fewer power devices, has a reduced TSV, and lower cost. The grid connected PV system is subjected to a specified control scheme, implemented in MATLAB/Simulink, and further validated through hardware proto-model.

3.2 DESCRIPTION OF TOPOLOGY

3.2.1 Power Circuit

The circuit topology of the proposed five-level inverter for a grid-connected PV system is depicted in Fig. 3.1. Six unidirectional switches, one diode, and one capacitor with a single dc source are used. In this topology, a leg of the switched capacitor is cascaded with the HB structure.

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doi: https://doi.org/10.1016/j.epsr.2022.108201.

The capacitor (C) is charged to the dc input voltage of (V_{dc}). The proposed inverter generates different output levels of 0, $\pm V_{\mathrm{dc}}$, $\pm 2V_{\mathrm{dc}}$

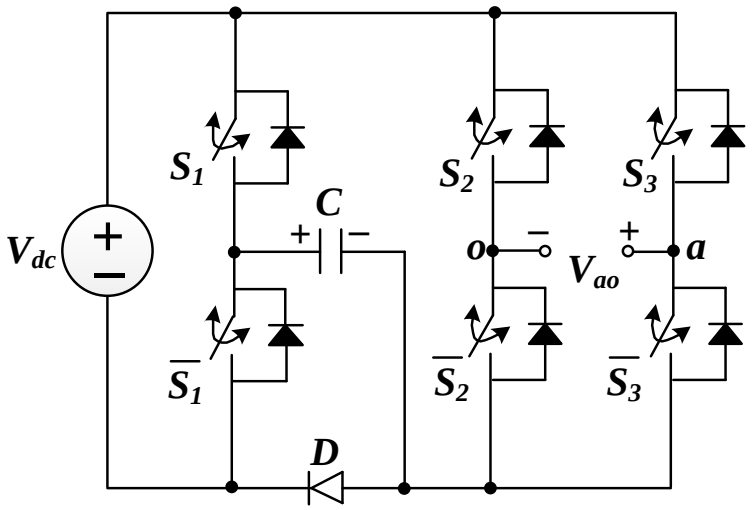

Fig. 3.1: *Schematic diagram of the proposed five-level inverter*

3.2.2 Description of the Voltage Levels

The operational states and capacitor parallel and series path (i.e., charging and discharging) for the proposed five-level inverter for a grid-connected PV power generation are shown in Table 3.1. It's worth noting that 1 and 0 represent the ON and OFF states of the power switches. The switches pairs (S_1, $\overline{S_1}$), (S_2, $\overline{S_2}$), (S_3, $\overline{S_3}$)are complementary. Capacitors states are shown by 'C' and 'D' i.e., charging and discharging, respectively. The path through which capacitors are charged is shown in green, and the positive and negative load current path are shown in blue and red shown in Fig. 3.2 and 3.3. The load current is assumed to be positive when it exits terminal 'a'and enters terminal 'o' .

- V_{ao}**=0**: It defines states μ_1 and μ_4 . As shown in Figs. 3.2a, 3.2b and 3.3a, 3.3b that the zero-voltage state generates across the load when switches S_1, S_2 and S_3 or S_1, $\overline{S_2}$ and $\overline{S_3}$ are ON, while turning OFF $\overline{S_1}$, $\overline{S_2}$ and $\overline{S_3}$ or $\overline{S_1}$, S_2 and S_3. As a result of being in parallel with the dc supply, the capacitor C gets charged to voltage V_{dc} through the switch S_1.

Table 3.1. *The operation states of the proposed five-level inverter*

Switching State	$V_{\mathbf{ao}}$	**Power Switches**						**Capacitors (C)**
		S_1	$\overline{S_1}$	S_2	$\overline{S_2}$	S_3	$\overline{S_3}$	
μ_1	0	1	0	1	0	1	0	C
μ_2	V_{dc}	1	0	0	1	1	0	C
μ_3	$2V_{\mathrm{dc}}$	0	1	0	1	1	0	D
μ_4	0	1	0	0	1	0	1	C
μ_5	$-V_{\mathrm{dc}}$	1	0	1	0	0	1	C
μ_6	$-2V_{\mathrm{dc}}$	0	1	1	0	0	1	D

- $\boldsymbol{V}_{\mathrm{ao}}$=$V_{dc}$: As depicted in Figs. 3.2c and 3.3c, power devices S_1, $\overline{S_2}$ and S_3 are conducting while $\overline{S_1}$, S_2 and $\overline{S_3}$ are OFF. The capacitor C is charged to the V_{dc} by parallel connection with the source. This operation defines the state μ_2.

- $\boldsymbol{V}_{\mathrm{ao}}$=$2V_{dc}$:It defines state μ_3. In this state, shown in Figs. 3.2d and 3.3d, power devices $\overline{S_1}$, $\overline{S_2}$ and S_3 are conducting while S_1, S_2 and $\overline{S_3}$ are OFF. In this state, by turning ON the switch $\overline{S_1}$ capacitor C appears in series with the dc source and gets discharged.

- $\boldsymbol{V}_{\mathrm{ao}}$=$-V_{dc}$: It defines state μ_5. By turning ON S_1 Capacitor C appeared across the dc source and got charged to voltage V_{dc}. The level $-V_{dc}$ is achieved when power switches S_1, S_2 and $\overline{S_3}$ conduct while turning OFF $\overline{S_1}$, $\overline{S_2}$ and S_3. This state is shown Figs. 3.2e and 3.3e.

- $\boldsymbol{V}_{\mathrm{ao}}$=$-2V_{dc}$: In this state, as shown in Figs. 3.2f and 3.3f by turning ON the switch $\overline{S_1}$ capacitor C appears in series with the source and gets discharged. The $-2V_{dc}$ level is achieved by conducting power switches $\overline{S_1}$, S_2 and $\overline{S_3}$ while turning OFF S_1, $\overline{S_2}$ and S_3. This operation defines the state μ_6.

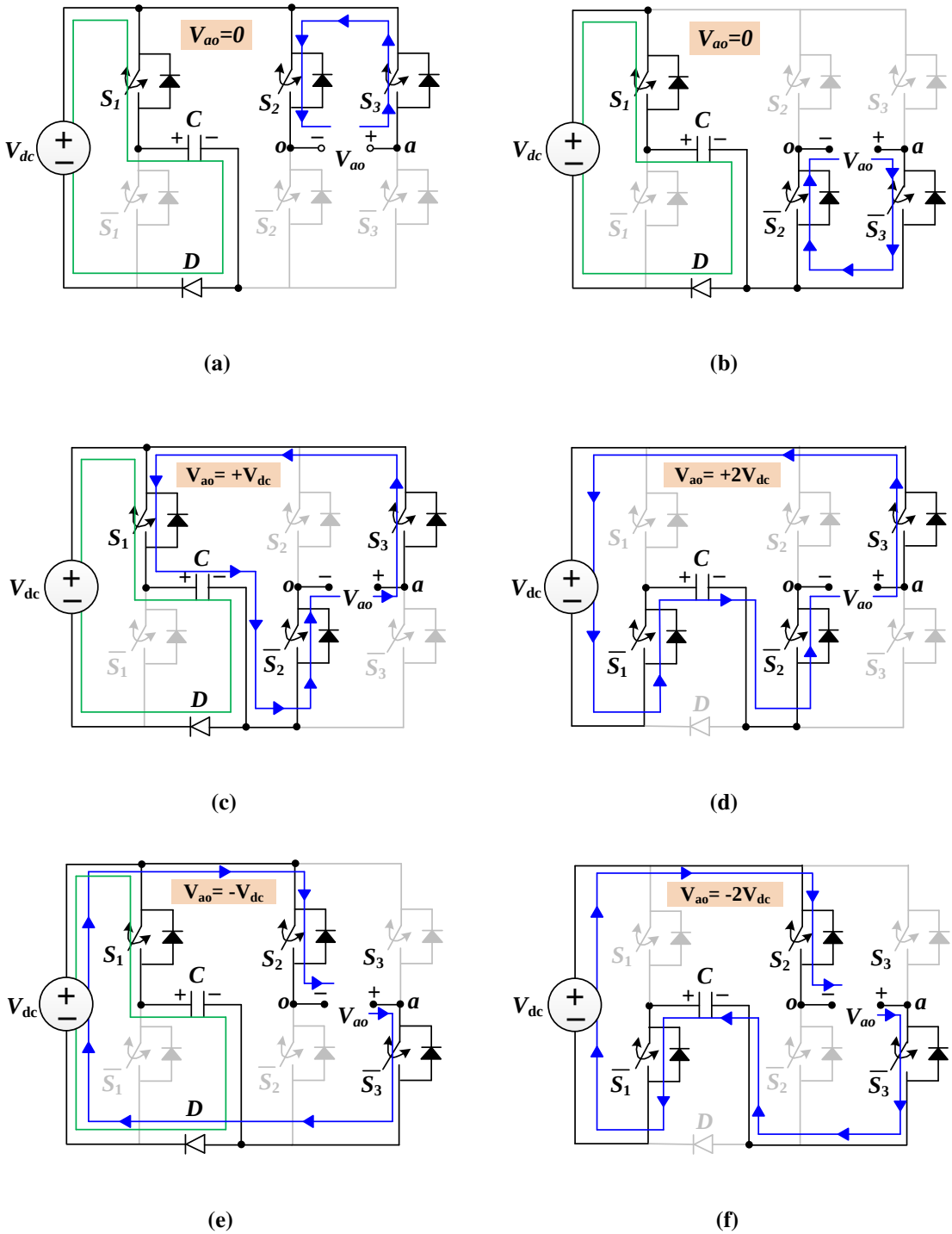

Fig. 3.2: *Various states of proposed topology with positive load current path (a) and (b)* V_{ao}*=0 (c)* V_{ao}*=+*V_{dc} *(d)* V_{ao}*=+2*V_{dc} *(e)* V_{ao}*=−*V_{dc} *(f)*V_{ao}*=−2*V_{dc}

3.3 MODULATION STRATEGY

Several modulation strategies have been implemented to generate gating pulses for control purposes [32]. To modulate MLIs, different modulating methods like high and low switching

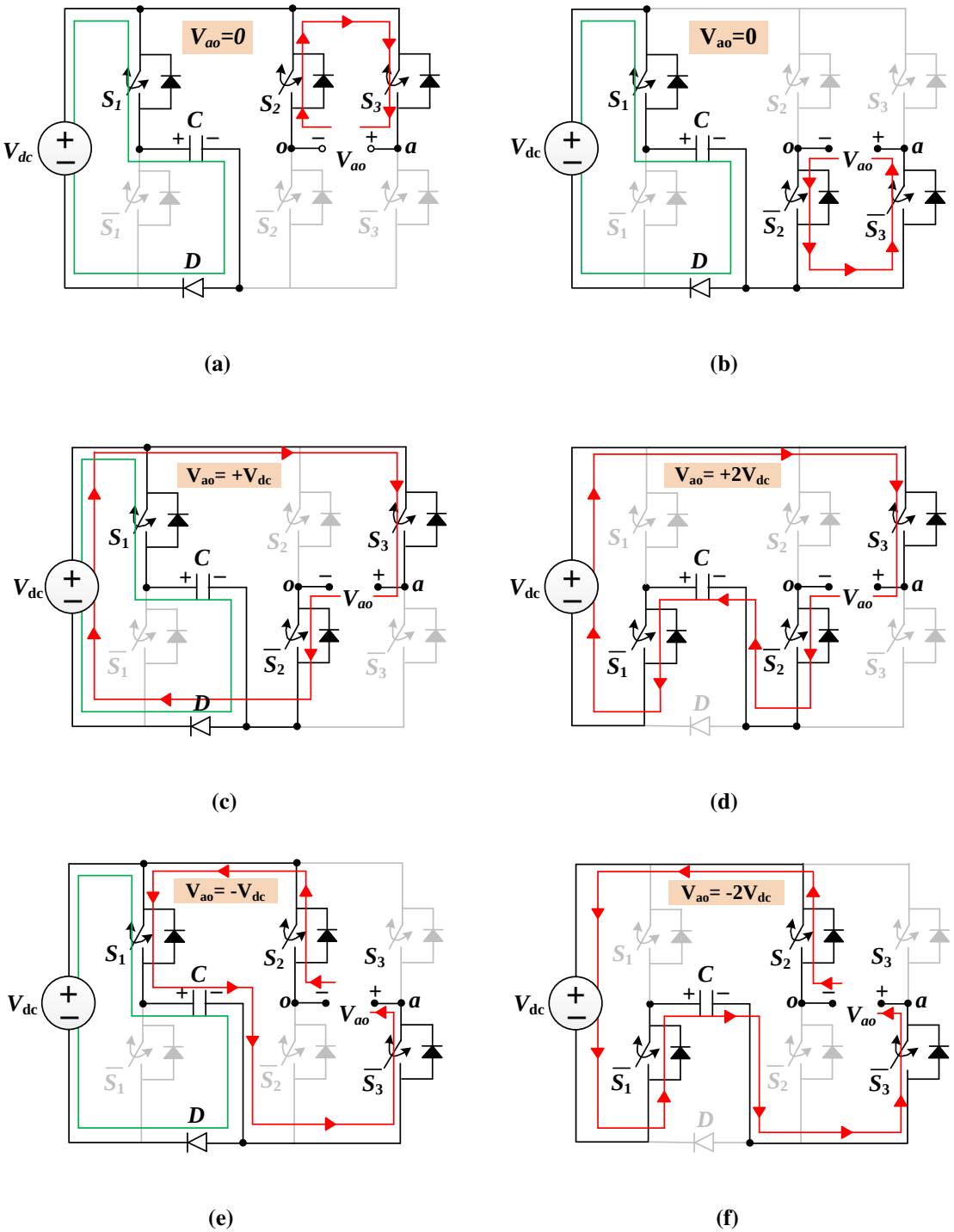

Fig. 3.3: *Various states of proposed topology with negative load current path (a) and (b)* V_{ao}*=0 (c)* V_{ao}*=+*V_{dc} *(d)* V_{ao}*=+2*V_{dc} *(e)* V_{ao}*=−*V_{dc} *(f)*V_{ao}*=−2*V_{dc}

frequency [61–63] are available. Any methods with suitable adaptation can be used to modulate the proposed topology. A simple Level-Shifted Pulse-Width Modulation (LSPWM) is used to modulate the proposed work, as shown in Fig.3.4. To generate a PWM signal, high-frequency

triangular signals are compared with the sinusoidal reference. The resulting pulses are used to switch devices corresponding to various voltage levels. As depicted in Fig.3.4, waveforms V_{crx} where x ∈ 1, 2 of the similar frequency (f_{cr}), phase angle, and maximum peak value (A_{cr}) are utilized for carriers. The voltage controller generates a reference signal (V_{ref}) with amplitude (A_{ref}) and frequency (f_{ref}). The absolute value $|V_{\text{ref}}|$ is compared to the high-frequency triangle signal V_{cr1} to V_{cr2} with a similar frequency and phase angle. As a result, the modulation index (M) can be calculated as follows:

$$M = \frac{A_{\text{ref}}}{2A_{\text{cr}}} \tag{3.1}$$

Where A_{cr} and A_{ref} are the amplitudes of the carrier and reference waveform respectively.

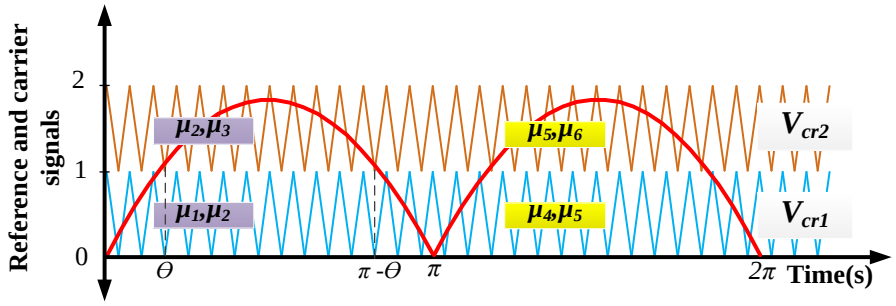

Fig. 3.4: *Modulation scheme for the proposed inverter*

When V_{cr1} is compared with absolute value $|V_{\text{ref}}|$ in the interval $0 \leq \omega t \leq \pi$, than the output voltage levels of 0, V_{dc} are produced by generating signals for states (μ_1 and μ_2). Similarly, when V_{cr2} is compared with absolute value $|V_{\text{ref}}|$ then, the voltage levels of V_{dc} and $2V_{dc}$ are produced by generating signals for states (μ_2 and μ_3).

For another interval ($\pi \leq \omega t \leq 2\pi$), the negative states are produced, and a zero level is generated by μ_4. When carrier signals V_{cr1}, V_{cr2} are compared with absolute value $|V_{\text{ref}}|$, the voltage levels of 0, $-V_{dc}$ and $-V_{dc}$, $-2V_{dc}$ are produced by generating signals for states (μ_4 and μ_5) and (μ_5 and μ_6), respectively. The above descriptions are executed in the state logic diagram shown in Fig. 3.5.

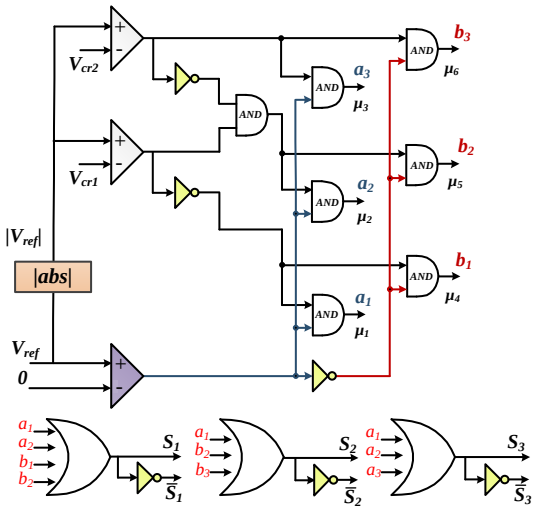

Fig. 3.5: *Modulation technique implemented using logic gates*

3.4 DESIGNING PARAMETER OF PROPOSED INVERTER

3.4.1 Rating of Components

PIV for all the power devices in the proposed topology is depicted in Table 3.2. Two switches and one diode (S_1, $\overline{S_1}$ and D) have a PIV 50% of the output voltage, whereas four switches (S_2, $\overline{S_2}$, S_3 and $\overline{S_3}$ have a PIV value 100% of the output voltage. The minimum current stress across the power devices is depicted in Table 3.3. Four power switches (S_2, $\overline{S_2}$,S_3 and $\overline{S_3}$) have current stress equal to load current (I_{ac}). Considering the unity factor load case with power ratings equal to P_o. So, I_{ac} can be calculated as:

$$I_{ac} = \frac{\sqrt{2} \times P_o}{2 \times M \times V_{dc}} \tag{3.2}$$

Table 3.2. *PIV across power switches and diodes*

PIV	Switches and Diodes
V_{dc}	S_1,$\overline{S_1}$ and D
$2V_{DC}$	S_2, $\overline{S_2}$, S_3 and $\overline{S_3}$

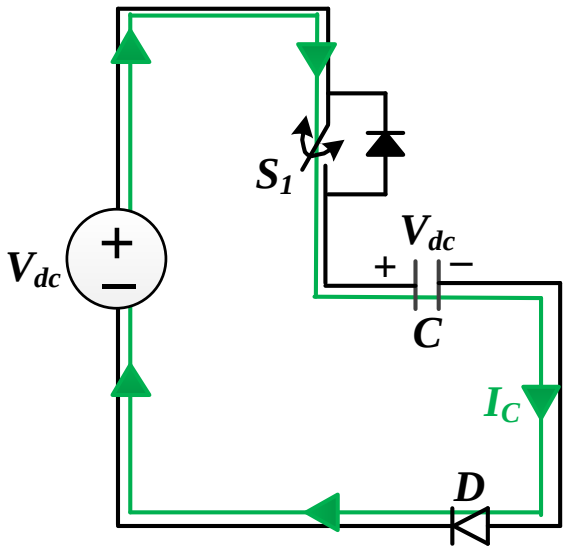

Fig. 3.6: *Current path for capacitors C*

Table 3.3. *Current flow through the power switches*

Current Stress	**Switches**
I_{ac}	S_2, $\overline{S_2}$, S_3 and $\overline{S_3}$
$I_{ac} + I_C$	S_1,and D

The switches S_1,and D have current stress due to the load current (I_{ac}) and capacitor charging current (I_C). I_C path is shown in Fig. 3.6, and it can be estimated as:

$$I_C = \left(\frac{V_{eq}}{R_{eq}}\right) \times exp\left(-\frac{t}{R_{eq} \times C}\right) \tag{3.3}$$

Where,

$$\begin{aligned} V_{eq} &= V_{dc} - V_C - V_D \\ R_{eq} &= r_{S_1} + r_D + R_{ESR_C} \end{aligned} \tag{3.4}$$

Where, R_{ESR_C} is the ESR of capacitor C.

3.4.2 Design of Capacitor

The proposed inverter uses the principle of the switched-capacitor approach to the maintained voltage of capacitor C to V_{dc}. When this capacitor discharges from supply to load, its ripples should not exceed 10% of its maximum voltage [64]. Discharging time and load current determines the voltage ripple of the capacitor. It is the worst-case scenario when a load is purely resistive [64]. As shown in Table 3.1, capacitor C experiences the maximum continuous discharge occurring from θ to $\pi - \theta$ in $+2V_{\mathrm{dc}}$ output level. Similar discharges occur in the negative cycle during the output voltage level of $-2V_{\mathrm{dc}}$. The maximum discharge for resistive load R_{L} can be articulated as: For C

$$\begin{aligned} \Delta Q_{\mathrm{C}} &= C \times \Delta V_{\mathrm{C}} \\ &= \int_{\frac{\theta}{\omega_{\mathrm{o}}}}^{\frac{\pi-\theta}{\omega_{\mathrm{o}}}} \frac{2V_{\mathrm{dc}}}{R_{\mathrm{L}}}\, dt \end{aligned} \tag{3.5}$$

By solving the above equation

$$\Delta Q_{\mathrm{C}} = \frac{V_{\mathrm{dc}}}{\omega_{\mathrm{o}} \times R_{\mathrm{L}}} \times (\pi - 2\theta) \tag{3.6}$$

And, it can be observed from Fig. 3.4 that,

$$\theta = sin^{-1}\left(\frac{1}{2M}\right) \tag{3.7}$$

$$\tag{3.8}$$

With a maximum allowed voltage ripple of 10%, we have:

$$\frac{100\Delta V_{\mathrm{C}}}{V_{\mathrm{dc}}} \leq 10 \tag{3.9}$$

Using these equations, we have:

$$C_1 \geq \frac{10}{\omega_{\mathrm{o}} \times R_{\mathrm{L}}}\left[\pi - 2sin^{-1}\left(\frac{1}{2M}\right)\right] \tag{3.10}$$

3.4.3 Power Losses

Power loss analysis is essential in designing an inverter for a given rating. The power losses in the proposed inverter are mainly due to the switching and conduction losses. The switching and

conduction power loss are described below:

$$P_{\mathrm{T}} = P_{\mathrm{C}} + P_{\mathrm{Spl}} \tag{3.11}$$

Where P_{T} = Total power losses; P_{c} = Total conduction losses andP_{Spl}= Switching power losses

3.4.3.1 Switching Power Losses

Switching losses are due to the turn ON and OFF operation of power switches which can be defined as [32, 65]:

$$P_{\mathrm{Spl}} = \frac{1}{2} \times V_{\mathrm{off}} \times I \times (t_{\mathrm{on}} + t_{\mathrm{off}}) \times f_{\mathrm{sw}} \tag{3.12}$$

Where t_{on} and t_{off} are the turn-on and turn-off times of the switch, f_{sw} is the switching frequency, I is the current during conduction and V_{off} is the blocking voltage.

3.4.3.2 Conduction Power Losses

Power losses occur due to conduction in a switch, and the power diode is obtained as [32]:

$$P_{\mathrm{cs}} \approx V_{\mathrm{on,s}} \times I_{\mathrm{s,avg}} + R_{\mathrm{on,s}} \times {I_{\mathrm{s,RMS}}}^2 \tag{3.13}$$

$$P_{\mathrm{cd}} \approx V_{\mathrm{on,d}} \times I_{\mathrm{d,avg}} + R_{\mathrm{on,d}} \times {I_{\mathrm{d,RMS}}}^2 \tag{3.14}$$

Where P_{cs} and P_{cd} are conduction power losses in a switch and power diode. $V_{\mathrm{on,s}}$ and $V_{\mathrm{on,d}}$ are on-state voltage drops across the transistor part and diode of a switch. $R_{\mathrm{on,s}}$ and $R_{\mathrm{on,d}}$ are on-state resistance of the transistor part and diode of the switch. $I_{\mathrm{s,avg}}$ and $I_{\mathrm{s,RMS}}$ are average and RMS currents through the transistor part. $I_{\mathrm{d,avg}}$ and $I_{\mathrm{d,RMS}}$are average and RMS currents through the diode of the power switch.

Based on the above analysis, power losses are calculated in PLECS based simulation model. IRFP460 MOSFETs were employed as power switches, and its datasheet was imported for power loss analysis Fig. 3.7 shows the distribution of power losses. Fig. 3.7a shows the power loss distribution in which switching loss across and conduction loss across $\overline{S_2}$, $\overline{S_3}$ are high as

compared to other transistors. With a combined efficiency of 95.90% with output power 215.29 W, all power switches and diodes incur total losses of 9.22 W. Fig. 3.7b shows the variation in efficiency with the change in the modulation index.

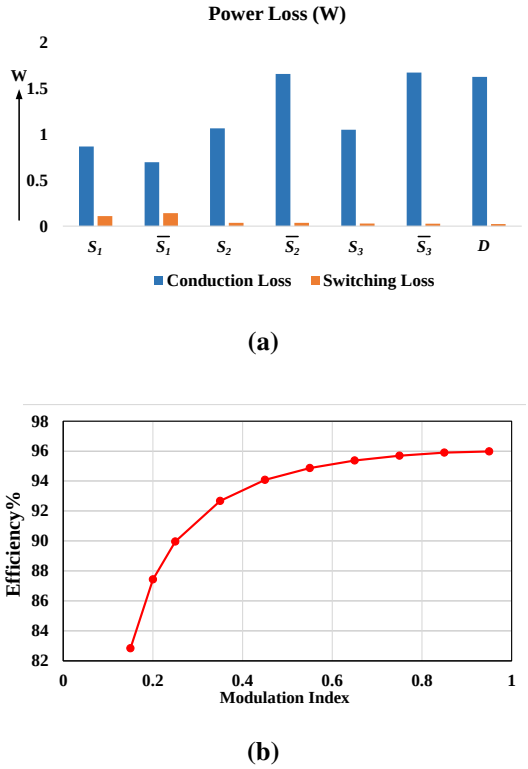

Fig. 3.7: *Distribution of power losses is calculated by measuring input power (224.50W) and output power (215.29W) (a) total losses (b) efficiency versus modulation index plot*

3.4.4 Control and Filter Design for Grid Connected Inverter

Closed-loop structure of the proposed inverter is shown in Fig. 3.8. The main components of this structure are PV array, proposed SCMLI , LCL filter to improve THD , controller, and the utility grid. The controller of this structure consists of a Maximum Power Point Tracking (MPPT) algorithm using perturb and observe method, and Phase-Lock-Loop (PLL) is utilized to extract the voltage angle and generate the synchronized current reference [66–68]. In this work, voltage and current are controlled by the proportional integral and proportional resonant controller, respectively. In Fig. 3.9, components of controller are shown in which output (V_{dc}^{*}) from MPPT block and source voltage (V_{dc}) is fed to voltage controller which produces reference

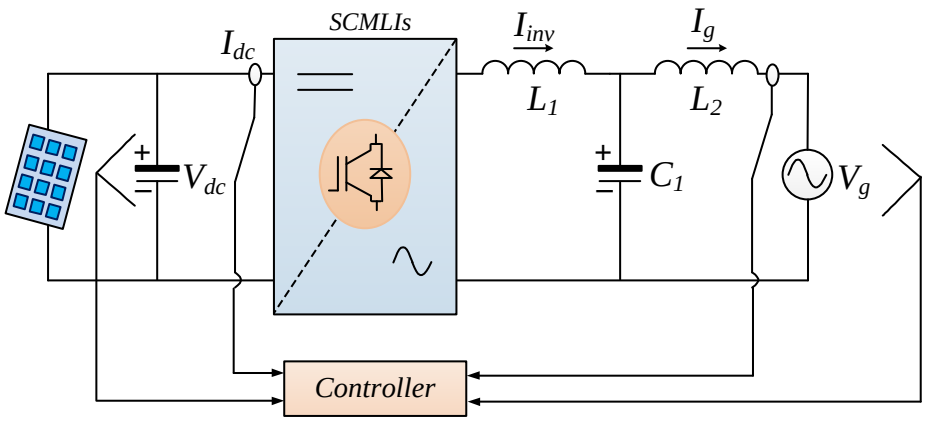

Fig. 3.8: *Closed-loop structure of single-phase grid connected inverter*

signal (I_{ref}) which multiplied with signal (Cosθ) from PLL block to produce reference grid current (I_{ref}Cosθ) which further fed to current controller. It produces the desired reference signal which further processes with PWM, described in Section 3.3, and generates a switching pulse. These pulses are fed to the power switches of the proposed inverter.

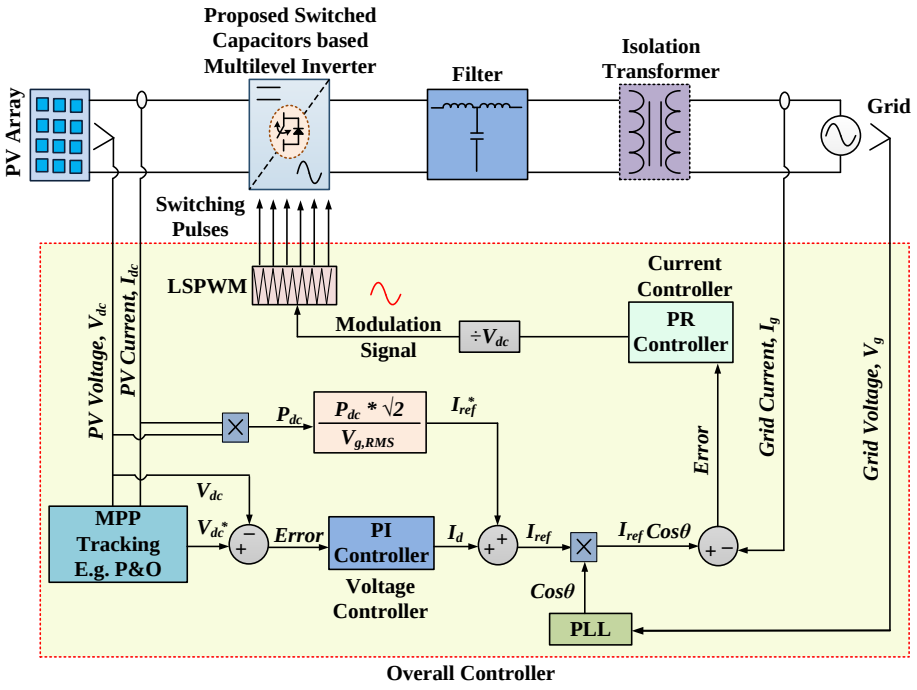

Fig. 3.9: *Complete block diagram of the control strategy.*

3.4.4.1 Designing of LCL filter

The inverter current comprises ripples and harmonics. This current is injected into the grid, resulting in high loss and power quality issues. An LCL filter is used at inverter output to provide a harmonics-free current to avoid these issues. The filter capacitor (C_1) is designed based on the reactive power absorbed at the rated conditions. The reactive power (Q) absorbed by the capacitor is limited to 5% of the rated power (P) [69].

$$\text{Reactive power}(Q) = \frac{{V_g}^2}{\frac{1}{2\times\pi\times f\times C_1}} \tag{3.15}$$

$$\frac{{V_g}^2}{\frac{1}{2\times\pi\times f\times C_1}} = 5\% \text{ of Rated power}(P) \tag{3.16}$$

$$C_1 = \frac{0.05 \times P}{V_g^2 \times 2 \times \pi \times f} \tag{3.17}$$

where, V_g is RMS value of grid voltage and f is fundamental frequency Similarly, value of inverter side inductor L_1 is selected based on the maximum permissible current ripple (ΔI_{ppmax}). The current ripples are limited to 20% of the rated current (I) and it is find through the rated power and grid voltage [69].

$$L_1 = \frac{V_{DC}}{4 \times f_{sw} \times \Delta I_{ppmax}} \tag{3.18}$$

The total inductance (L_1+L_2) is selected based on the maximum voltage drop across the inductor, which is limited to 10% of grid voltage (V_g)

$$V_{L1+L2} = I \times X_{L_1+L_2} = I \times 2 \times \pi \times f \times (L_1 + L_2) \tag{3.19}$$

$$L_1 + L_2 = \frac{0.1 \times V_g}{I \times 2 \times \pi \times f} \tag{3.20}$$

3.5 COMPARISON STUDY

Comparison research is carried out to analyse the proposed topology and evaluate it. The comparison is made in terms of the number of levels (N_L), the number of power switches and gate drivers (N_S and N_{GD}), the number of diodes (N_D), the number of capacitors (N_C), the number of input dc sources (N_{IS}), TSV and voltage boosting capabilities. Table 3.4 summarizes the comparative analysis.

CHB, [71, 72, 75, 76], as shown in Table 3.4, require two sources to provide five-level output, while the proposed topology only needs one source. Topologies in [70] and [77] are the voltage quadruple and doubler circuits. The voltage boosting capabilities of these circuits is viewed as an advantage compared to other topologies. However, in these topologies, the count of semiconductors and capacitors is larger than in the proposed topology. Topologies in [74] and [75] are voltage reducers. The proposed topology and [75] have an equivalent count of power switches, but the only resistive load is considered in topology [75] and requires two dc power supplies. As a result, the proposed topology has improved structural and performance features, requiring just a single source and fewer count of power switches, gate drivers, and diodes.

Table 3.4. *Comparison with other five-level topologies*

Topologies	N_L	N_S	N_{GD}	N_D	N_C	N_{IS}	TSV	Inherent Voltage Boosting
NPC	5	8	8	20	4	1	8	No
FC	5	8	8	8	10	1	8	No
CHB	5	8	8	8	2	2	8	No
[70]	5	12	12	12	4	1	20	Yes
[71]	5	8	7	10	0	2	10	No
[72]	5	8	8	8	0	2	12	No
[73]	5	8	7	10	1	1	10	No
[74]	5	7	7	8	3	1	13	No
[75]	5	6	6	7	2	2	11	No
[76]	5	8	6	8	4	2	10	No
[77]	5	7	7	10	2	1	9	Yes
Proposed	5	6	6	7	1	1	11	Yes

3.6 EXPERIMENTAL VERIFICATION

A simulation model is created in the SimPowerSystems toolbox in the MATLAB/SIMULINK software to test the performance of the proposed topology. Table 3.5 shows the value of different components and parameters.

Table 3.5. *Parameters of simulation*

Parameters	Values
dc Source	200V
Capacitors (C)	$1600\mu F$
Switching Frequency (f_{sw})	2000Hz
Fundamental Frequency (f)	50Hz
Resistive Load	500Ω
Inductive Load	100Ω ,100 mH

Fig. 3.10 depicts the simulation result to validate the proposed five-level inverter with the modulation index M = 0.85. Figs. 3.10a and 3.10b show the simulation results of voltage and current waveform with a resistive load (i.e.,500Ω) and an inductive load (i.e.,100Ω,100mH). Fig. 3.10c shows the ripple voltage of the capacitor. Fig. 3.10d and 3.10e represent transient in load. For t<sec, the load comprises a resistive load (i.e.,500Ω) and an inductive load (i.e.,100Ω,100mH), respectively. After t=1sec load changes to half of its earlier value. Consequently, the load current is changed significantly and gets double by decreasing load to half of the earlier values. Fig. 3.10f depicts the THD of load current with an inductive load (i.e.,100Ω,100mH).

Experimental tests are carried out on a laboratory-developed prototype (see Fig. 3.11) with the parameters listed in Table 3.6. The prototype is made up of discrete MOSFETs (SiHG47N6) driven by Si82071AB-IS drivers. The output voltage and input current are sensed using a Hall Effect-based voltage sensor (LEMLV25-P) and current sensor (HE025T01). The MOSFETs gate pulses are generated using the OPALRT-OP4510, which interfaces with the hardware using

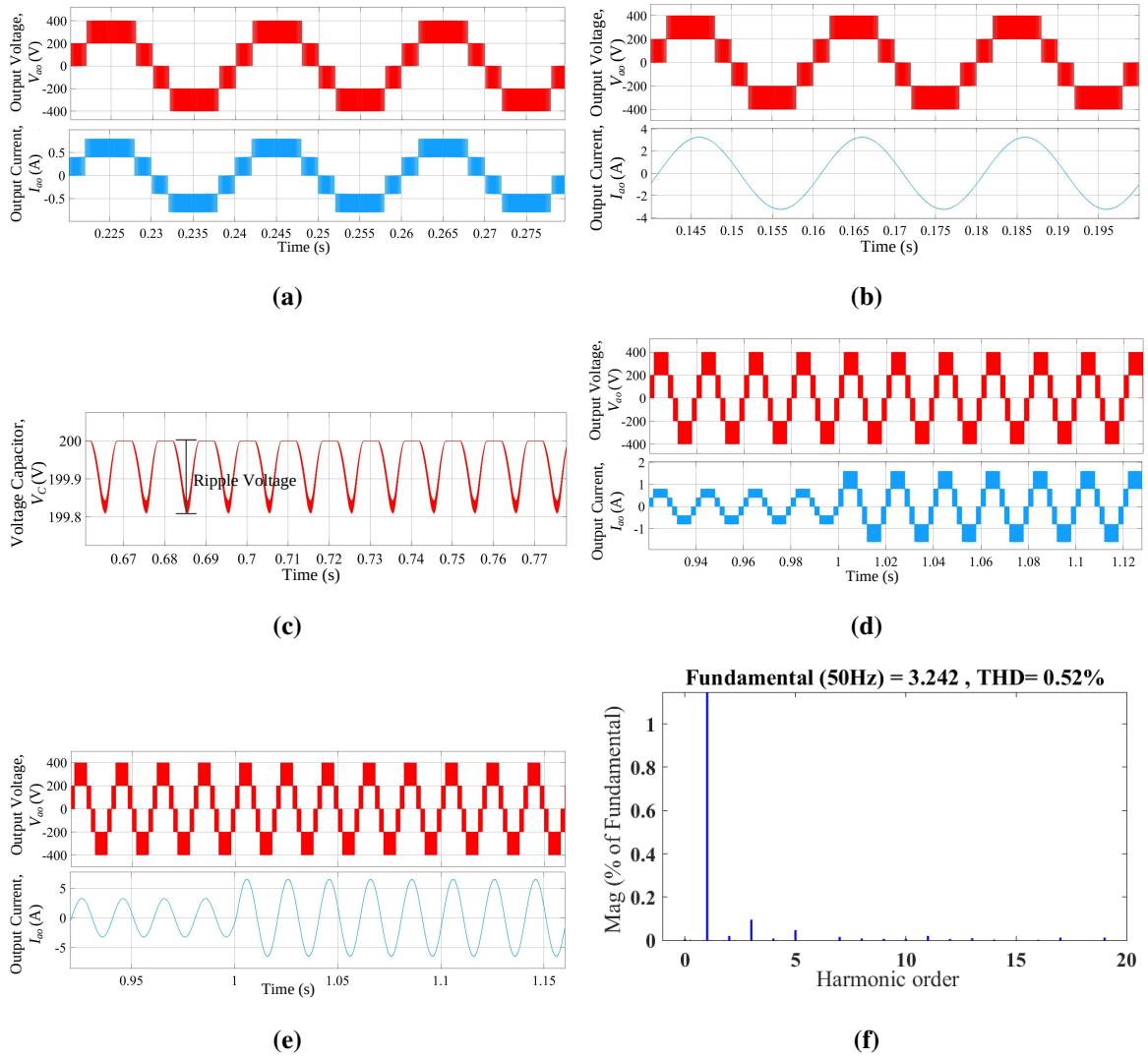

Fig. 3.10: *Simulation outcomes showing (a) waveform of voltage and current with a resistive load (500Ω) (b) voltage and current waveform with an inductive load (100Ω,100mH) (c) ripple voltage of capacitor (d) transition in resistive load from (500Ω) to (250Ω) (e) transition in inductive load from (100Ω, 100mH) to (50Ω, 50mH) (f) depicts THD of load current.*

MATLAB/SIMULINK on the host computer. A MAGNA-POWER programmable DC power supply (SL1000-6.0/415+HS) is used to provide the input dc supply of 200V. The prototype is designed to provide 2kW power at 230V RMS voltage with a 50Hz power frequency.

All experimental outcomes are illustrated in Fig. 3.12 to verify the simulation results of the five-level inverter and its closed-loop control. Fig. 3.12a depicts the waveform of voltage, current, and the capacitor voltage with a resistive load of 500Ω and having an amplitude of 400V, 0.8A, and 200V, respectively. Fig. 3.12b depicts the waveform of voltage, current, and capacitor

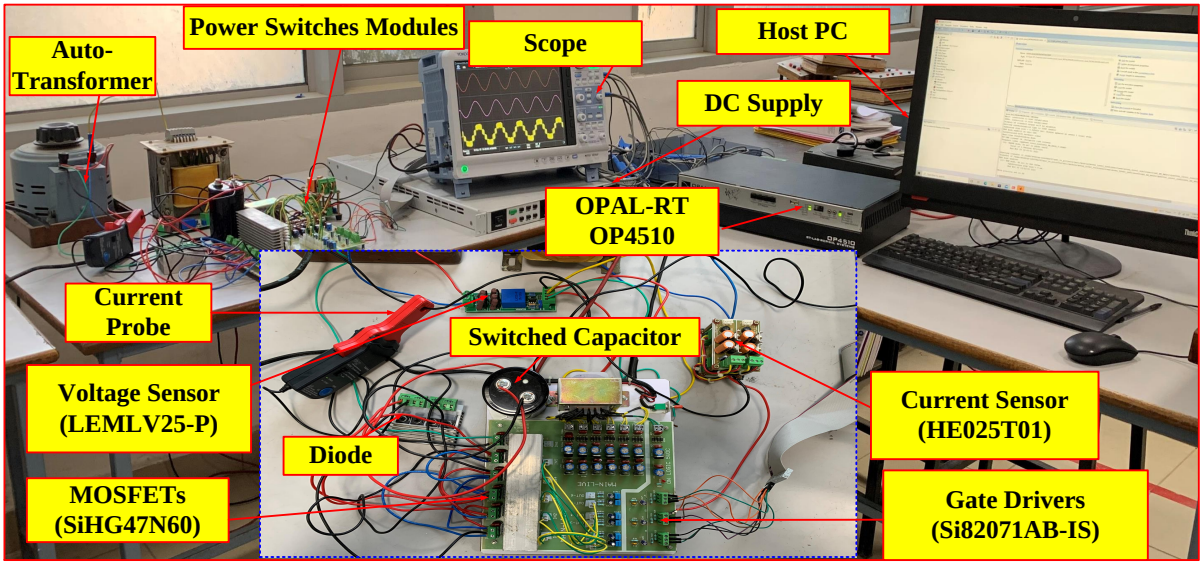

Fig. 3.11: *Experimental setup of the proposed work*

Table 3.6. *Experimental parameters and components specifications*

Parameters	Values
MOSFET	SiHG47N60
Isolated Gate driver IC	Si82071AB
Controller	Opal-RT OP4510
Voltage Senor	LEMLV25-P
Current Senor	HE025T01

voltage with inductive load (i.e.,100Ω ,100mH) and having an amplitude of 400V, 3.2A, and 200V, respectively. Fig. 3.12c depicts the voltage waveform of power switches (S_1 to $\overline{S_3}$). PIV of switches (S_1, $\overline{S_1}$) is 200V each, and for other switches, it is 400V each. Figs. 3.12d and 3.12e represent transients in the load.

The closed-loop performance characteristic is depicted in Fig. 3.12f. In this figure, the grid voltage is in phase with grid current and maintains a Unity Power Factor (UPF) with amplitudes 325V and 12A, respectively.

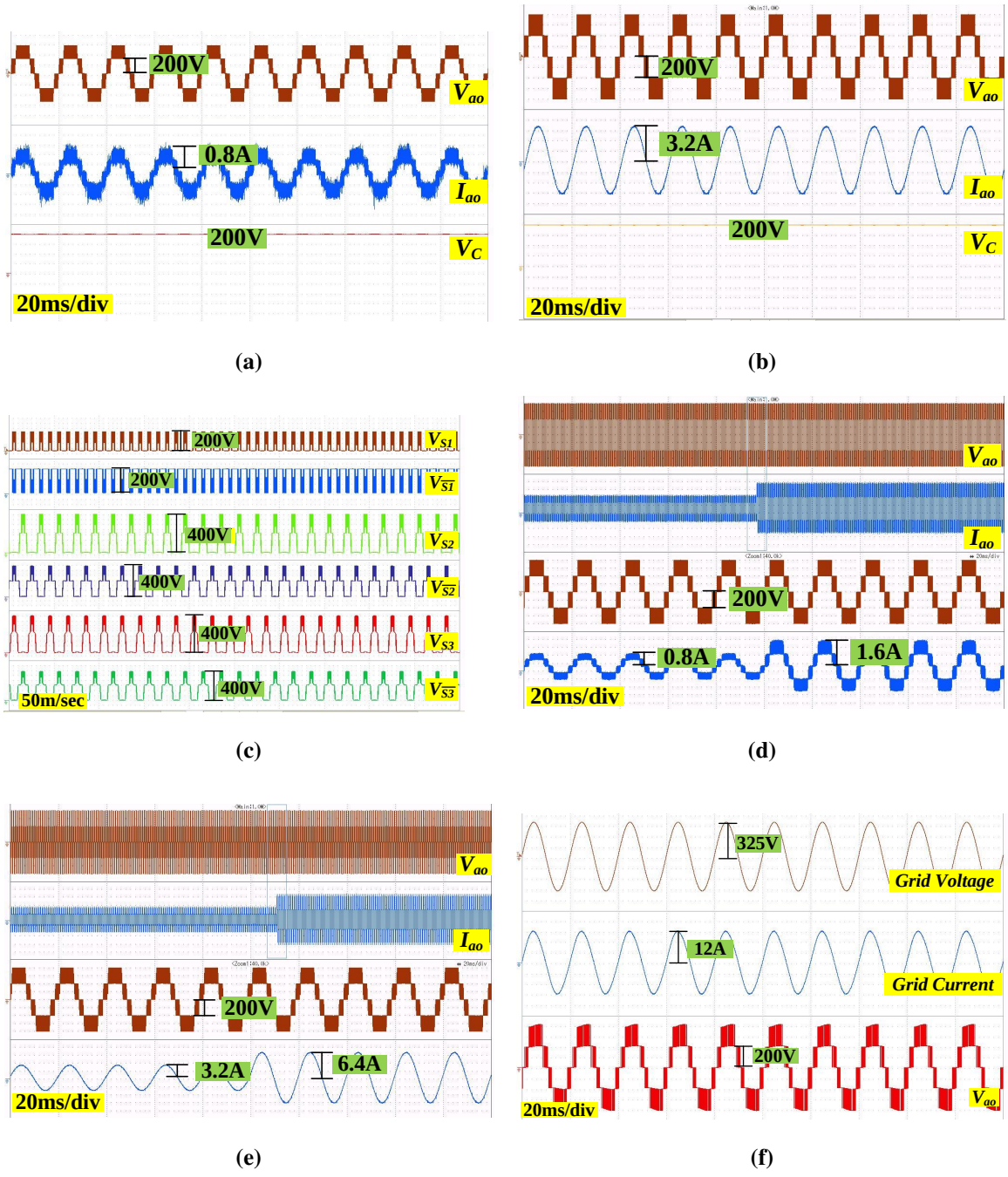

Fig. 3.12: *Experimental results showing (a) voltage, current, and capacitor voltage with a resistive load (500Ω) (b) voltage, current, and capacitor voltage with an inductive load (100Ω,100mH) (c) Switching signals for power switches (d) transition in resistive load from (500Ω) to (250Ω) (e) transition in inductive load from (100Ω, 100mH) to (50Ω, 50mH) (f) waveforms of grid connected system*

3.7 CHAPTER SUMMARY

This chapter presents a five-level inverter suited for the grid-connected PV system. The experimental results validate the proposed power circuit.

The following observations are made from this study:

- The proposed SCs based topology generates a five-level output voltage waveform, providing improved performance under dynamic conditions. It achieves this while maintaining a boosting factor of two, resulting in a significant increase in output voltage compared to the input voltage.
- This topology is designed to operate with a single dc source, which allows for the generation of a high number of voltage levels with a high boosting gain. By reducing the number of switches required, it simplifies the circuitry and improves overall system reliability.
- The system maintains a high-power factor, making it suitable for grid-connected applications. Power factor is an important parameter for efficient power transfer and ensures that the system operates in harmony with the utility grid.
- This topology enables single-stage power conversion from low-voltage dc to high-voltage ac, eliminating the need for multiple conversion stages and reducing energy losses.
- The total losses in the power switches of this topology amount to 9.22W. These losses include switching losses and conduction losses. With an overall efficiency of 95.90%, the system achieves a high level of energy conversion efficiency, ensuring minimal energy wastage and improved performance.

Chapter–4

Design of Seven-Level Inverter for Interface With Grid-Connected Photovoltaic System

4.1 GENERAL

Through the development of grid-connected SC-based five-level inverters in Chapter 3, it has been concluded that this topology is best suited for boost dc-ac conversion with stable operation in dynamic conditions. However, there is a requirement of an HB structure for generating negative levels, which results in a large PIV across the switches. Furthermore, as the number of levels increases for gating high-resolution waveforms, the PIV also increases. To address the limitations of the first proposed topology, a second topology is presented, which synthesizes seven levels. This proposed inverter incorporates self-voltage boosting while reducing the number of power switches. It achieves a voltage boosting capability of up to 1.5 times the input dc voltage, without subjecting the power switches to excessive voltage stress. As a result, the PIV of all power switches remains below the input source voltage. Moreover, the proposed topology eliminates the need for multiple power sources and voltage balancing of capacitors. The capacitors automatically achieve balance through the charging and discharging process. To generate suitable switching pulses for the inverter, a simple modulation technique is employed. The chapter includes a comparative analysis, comparing the proposed inverter to other SCMLIs. The closed-loop structure of the proposed inverter is investigated, and specific control strategies are implemented in MATLAB/Simulink. Additionally, an experimental prototype of the proposed

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doi: https://doi.org/10.1007/s00202-022-01535-2

topology is constructed and tested in both open and closed-loop configurations to validate its effectiveness.

4.2 DESCRIPTION OF TOPOLOGY

4.2.1 Circuit Topology

The structure of the proposed seven-level inverter is shown in Fig. 4.1. It has nine power switches and four capacitors. Each power switch in this topology consists of a transistor with an anti-parallel diode. The output voltage is labeled as V_{ao}. The dc-link consists of two parallel-connected capacitors C_1 and C_2 whose voltages are rated at half of the dc voltage. Input voltage is obtained from the PV panel which is V_{dc}. One dc source is sufficient to produce seven-level of voltages ($0, \pm 0.5V_{dc}, \pm V_{dc}, \pm 1.5V_{dc}$).

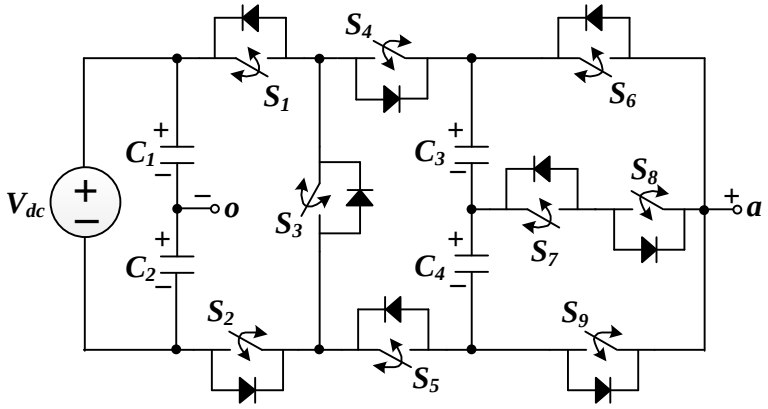


Fig. 4.1: *Schematic circuit of proposed seven-level inverter*

4.2.2 Modes of Operations

All the valid operating states for the proposed seven-level inverter are shown in Figs. 4.2 and 4.3. The path through which capacitors are charged is shown in green, and the positive and negative load current path is shown in blue and red respectively. Table 4.1 represents the switching states of the proposed topology in which '1' and '0' represent the ON and OFF operation of power

switches in particular state. Switching states of S_1=S_5, S_2=S_4 and S_7=S_8. Capacitors states of capacitors (C_3, C_4) are represented by 'C' (charging state), 'D' (discharging state), and '-' (idle state).The states are described below:

Table 4.1. *Switching states of proposed topology*

States	V_{ao}	Power Switches						Capacitors	
		S_1/S_5	S_2/S_4	S_3	S_6	S_7/S_8	S_9	C_3	C_4
λ_1,λ_5	0	1	1	0	0	1	0	C	C
λ_2	$0.5V_{dc}$	1	1	0	1	0	0	C	C
λ_3	V_{dc}	1	0	1	0	1	0	-	D
λ_4	$1.5V_{dc}$	1	0	1	1	0	0	D	D
λ_6	$-0.5V_{dc}$	1	1	0	0	0	1	C	C
λ_7	$-V_{dc}$	0	1	1	0	1	0	D	-
λ_8	$-1.5V_{dc}$	0	1	1	0	0	1	D	D

1. State λ_1&λ_5: In this state, the output voltage V_{ao}= 0 with continuous conduction of power switches S_1, S_2, S_4, S_5, S_7, and S_8 while power switches S_3, S_6, and S_9 are OFF. As a result, the capacitors C_1, C_2, C_3, and C_4 are parallel with the dc source and hence get charged to voltage $0.5V_{dc}$ as shown in Figs. 4.2a and 4.3a.

2. State λ_2: In this state, with continuous conduction of power switches S_1, S_2, S_4, S_5, and S_6 while power switches S_3, S_7, S_8, and S_9 are OFF, the output voltage of V_{ao}= V_{C1}= $0.5V_{DC}$ is obtained. As a result, the capacitors C_1, C_2, C_3, and C_4 are parallel with the dc source and hence get charge to voltage $0.5V_{dc}$ as shown in Figs. 4.2b and 4.3b.

3. State λ_3: In this state, with continuous conduction of power switches S_1, S_3, S_5, S_7, and S_8 while power switches S_2, S_4, S_6, and S_9 are OFF. Thus, the output voltage is V_{ao}= V_{C1}+V_{C4}= V_{dc} as shown in Figs. 4.2c and 4.3c.

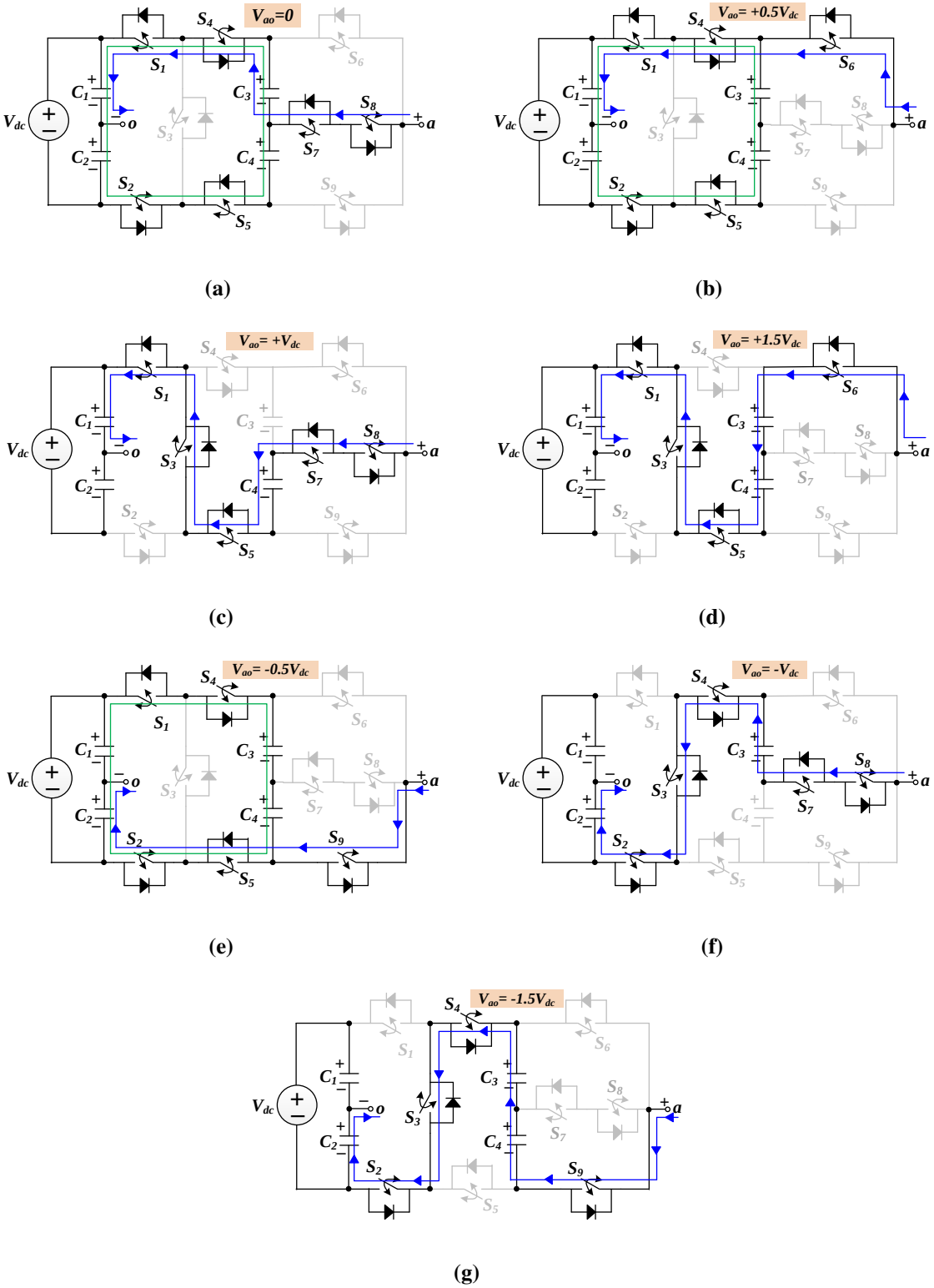


Fig. 4.2: *Different states of proposed topology with positive load current path (a) 0 (b) $0.5V_{dc}$ (c) V_{dc} (d) $1.5V_{dc}$ (e) $-0.5V_{dc}$ (f) $-V_{dc}$ (g) $-1.5V_{dc}$*

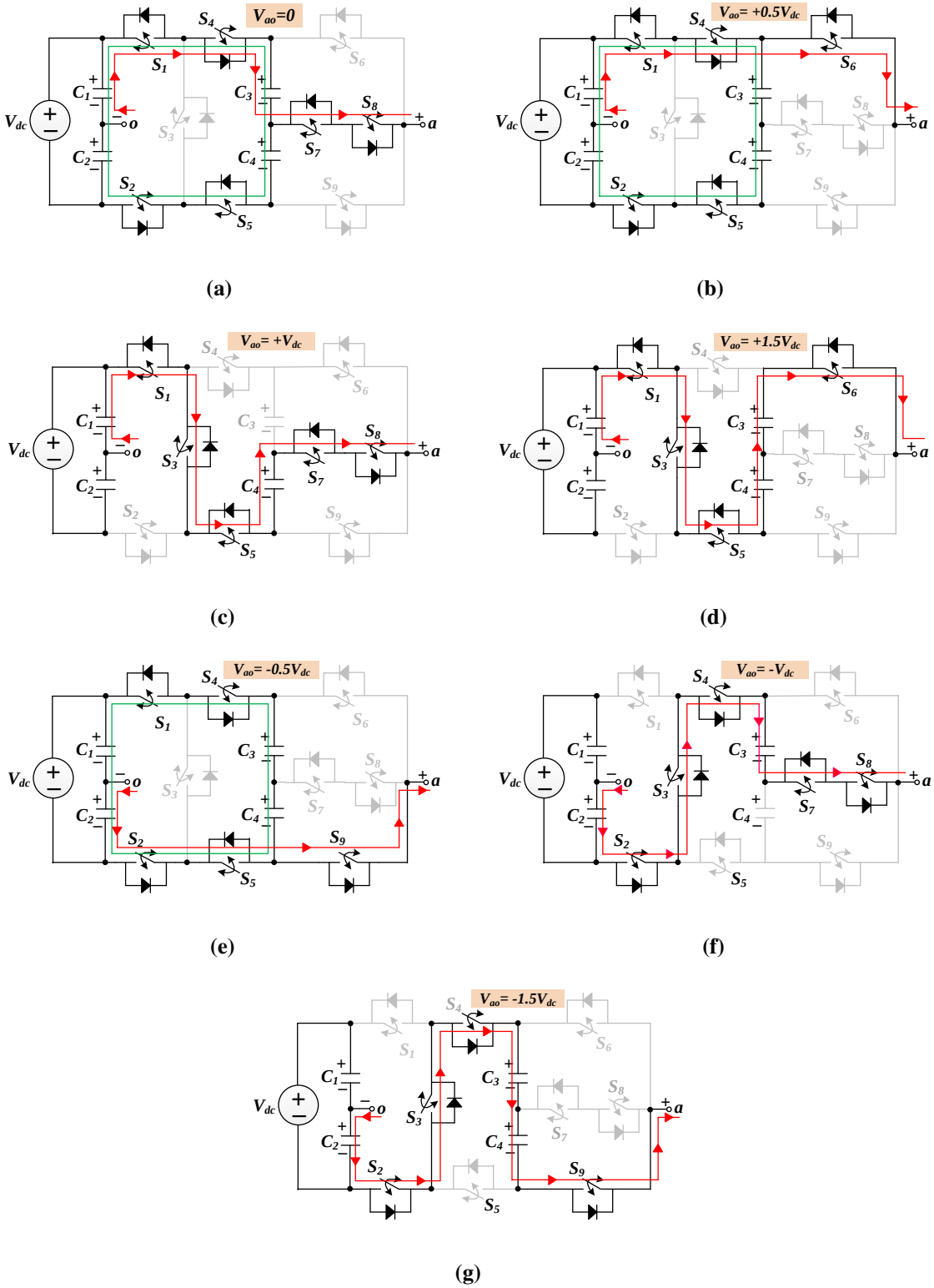


Fig. 4.3: *Different states of proposed topology with negative load current path (a) 0 (b) 0.5V_{dc} (c) V_{dc} (d) 1.5V_{dc} (e) −0.5V_{dc} (f) −V_{dc} (g) −1.5V_{dc}*

4. State λ_4: In this state, with continuous conduction of power switches S_1, S_3, S_5, and S_6 while power switches S_2, S_4, S_7 , S_8, and S_9 are OFF. As a result, the output voltage is V_{ao} = V_{C1}+V_{C3}+V_{C4}= $1.5V_{dc}$ as shown in Figs. 4.2d and 4.3d.

5. State λ_6: In this state, with continuous conduction of power switches S_1, S_2, S_4, S_5, and S_9 while power switches S_3, S_6, S_7, and S_8 are OFF. As a result, the output voltage is V_{ao}= $-V_{C2}$= $-0.5V_{dc}$ as shown in Figs. 4.2e and 4.3e.

6. State λ_7: In this state, with continuous conduction of power switches S_2, S_3, S_4, S_7, and S_8 while power switches S_1, S_5, S_6, and S_9 are OFF. As a result, the output voltage is V_{ao}= $-V_{C2}-V_{C3}$= $-V_{dc}$ as shown in Figs. 4.2f and 4.3f.

7. State λ_8: In this state, with continuous conduction of power switches S_2, S_3, S_4, and S_9 while power switches S_1, S_5, S_6, S_7, and S_8 are OFF. As a result, the output voltage is V_{ao} = $-V_{C2}-V_{C3}-V_{C4}$ = $-1.5V_{dc}$ as shown in Figs. 4.2g and 4.3g

4.3 MODULATION STRATEGY

Various methods are used for modulation of multilevel inverters namely, high-switching-frequency methods [61] and low-switching-frequency methods. The proposed topology can be modulated with any of these methods with an appropriate alteration. This topology is modulated by using LSPWM technique as shown in Fig. 4.4. In this scheme, triangular carrier signals are used to compare with sinusoidal reference signal and resultant pulse signals are used to provide switching to the power devices corresponding to the particular voltage level. As depicted in Fig. 4.4 three carrier waveforms V_{crj} (j = 1 to 3) of the same frequency *(f_{cr})*, phase, and peak-to-peak value *(A_{cr})* are used for carriers. A sinusoidal waveform *(V_{ref})* having amplitude *(A_{ref})* and frequency *(f_{ref})* are taken as the reference signal and its absolute value $|V_{ref}|$ is compared with the carriers. Therefore, modulation index *(M)* is denoted as:

$$M = \frac{A_{ref}}{3 \times A_{cr}} \tag{4.1}$$

Where A_{cr} and A_{ref} are amplitude of the carrier and reference waveform respectively. Various operating states are shown in Fig. 4.4 for the complete power cycle i.e., during $0 \leq \omega t \leq 2\pi$. It can be seen that during $0 \leq \omega t \leq \pi$ interval, V_{cr1} is compared with $|V_{ref}|$, the estimated voltage levels are $(0, 0.5V_{dc})$ which are obtained by imposing gate signals for states (λ_1, λ_2). In the same

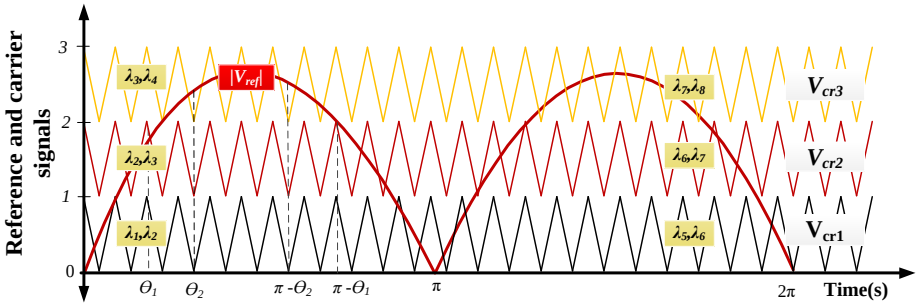


Fig. 4.4: *Reference and carrier waveforms to modulate the proposed seven-level inverter*

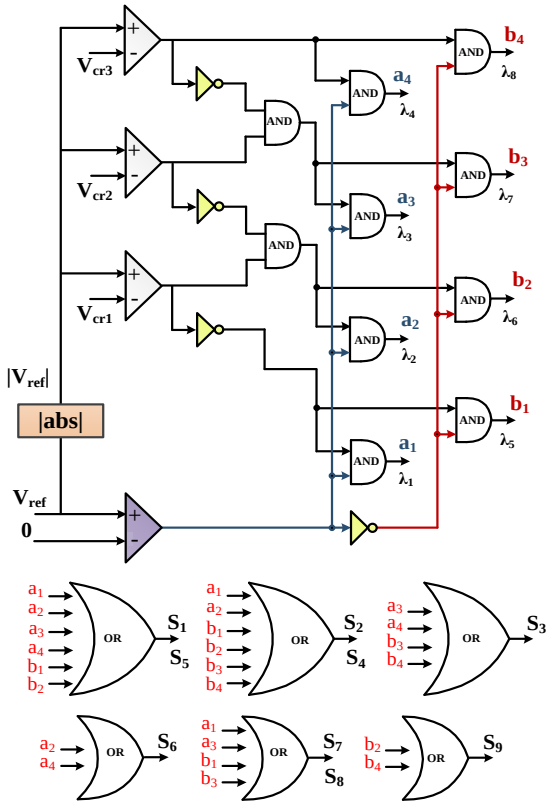


Fig. 4.5: *Logic gates based implementation of modulation scheme*

way, when V_{cr2} and V_{cr3} are compared with $|V_{ref}|$, the estimated levels during $0 \leq \omega t \leq \pi$ are $(0.5V_{dc}, V_{dc})$ and $(V_{dc}, 1.5V_{dc})$ which are obtained by imposing gate signals for states (λ_2, λ_3) and (λ_3, λ_4). For the other half cycle, i.e. during $\pi \leq \omega t \leq 2\pi$, the states for the negative half cycle are to be enacted and zero levels are obtained by the state λ_5. Therefore, for $\pi \leq \omega t \leq 2\pi$, when V_{cr1}, V_{cr2}, and V_{cr3} are compared with $|V_{ref}|$, the estimated levels are $(0, -0.5V_{dc})$, $(-0.5V_{dc}, -V_{dc})$ and $(-V_{dc}, -1.5V_{dc})$ which are obtained by imposing gate signals for states (λ_5, λ_6), (λ_6, λ_7) and (λ_7, λ_8). Based on the abovementioned description, the execution of the state-selection

logic is given in Fig. 4.5, in which gate signals for specific states are first obtained, and finally fed to OR gates for obtaining respective firing pulses for each power switch.

4.4 RATINGS OF COMPONENTS AND DESIGNING OF CAPACITORS

4.4.1 Voltage and Current Rating

PIV for the power switches in the proposed topology is shown in Table 4.2. The PIV rating of switches S_7 and S_8 is ≈ 34% of the operating voltage and for remaining switches, it is ≈ 67% of the operating voltage. Besides, the minimum current ratings of power switches are shown in

Table 4.2. *PIV of power switches*

PIV	Power Switches
$0.5V_{DC}$	S_7, S_8
V_{dc}	S_1 , S_2, S_3, S_4, S_5, S_6, S_9

Table 4.3. Four power switches (S_6, S_7, S_8, and S_9) need to carry only the load current (I_{ac}) and hence they should be rated at least at the value equal to the amplitude of the load current (I_{ac}). Considering, unity factor load case with power ratings equal to P_r, I_{ac} can be calculated as:

$$I_{ac} = \frac{\sqrt{2} \times P_r}{1.5 \times M \times V_{dc}} \tag{4.2}$$

where M is modulation index defined in equation (4.1)

The switches S_1, S_2, S_4, and S_5 need to carry two currents, the load current (I_{ac}) and the charging current (I_C) for the capacitors C_3 and C_4 and hence it should be rated at least equal to the sum of their peak values. The path for I_C is shown in Fig. 4.6 and it can be calculated as:

$$I_C = \left(\frac{V_{eq}}{R_{eq}}\right) \times exp\left(-\frac{t}{R_{eq} \times \frac{C_3 \times C_4}{C_3 + C_4}}\right) \tag{4.3}$$

Table 4.3. *Current through power switches*

Current Stress	Power Switches
I_{ac}	S_3, S_6,S_7,S_8,S_9
$I_{ac} + I_C$	S_1,S_2,S_4,S_5

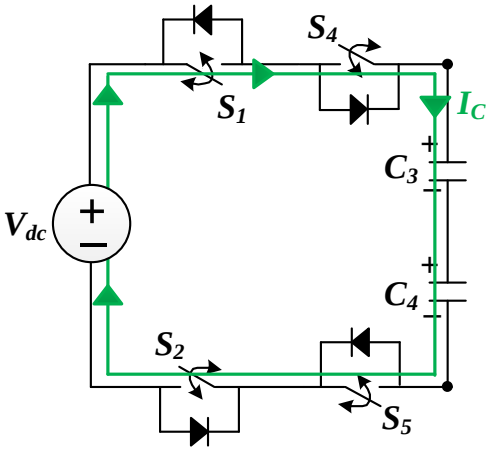


Fig. 4.6: *Charging path for capacitors C_3 and C_4*

Where,

$$V_{eq} = V_{DC} - V_{D_4} - V_{C_3} - V_{D_5} - V_{C_4}$$
$$R_{eq} = r_{D_4} + r_{D_5} + r_{S_1} + r_{S_2} + R_{ESR_{C_3C_4}} \tag{4.4}$$

Therefore, V_{D_4} and V_{D_5} are the on-state voltage drops across the diodes of switches S_4 and S_5 respectively. V_{C_3} and V_{C_4} are the voltages across capacitors C_3 and C_4 respectively. r_{D_4}, r_{D_5}, r_{S_1}, and r_{S_2} are the respective on-state resistances of the diode S_4, the diode of S_5, transistor part of S_1, and transistor part of S_2, and $R_{ESR_{C_3C_4}}$ is the ESR of the series combination of C_3 and C_4.

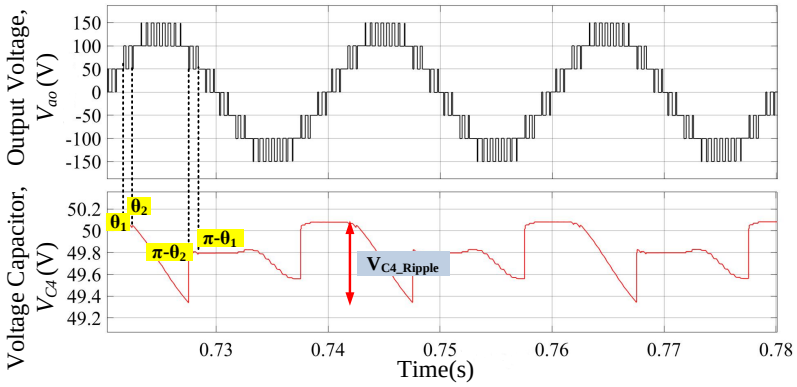


Fig. 4.7: *Ripple voltage across capacitor C_4*

4.4.2 Designing of Capacitors

Two capacitors C_3 and C_4 are maintained at $0.5V_{dc}$ each in the proposed inverter by using the principle of switched capacitor technique. Ripples that appear on them should not be more than 10% of the desired capacitors voltage when they discharge from supply to load [56]. The voltage ripple across the capacitors is determined by discharging time and the current across the load. The worst situation is when a load is purely resistive [30]. In capacitors C_3 and C_4 continuous maximum discharging happens in interval θ_1 to $\pi - \theta_1$ in the positive and negative cycle when obtaining continuously output voltage levels of $+V_{dc}$, $+1.5V_{dc}$, and $-V_{dc}$, $-1.5V_{dc}$ as shown in Fig. 4.7. The maximum discharge for resistive load R_L can be described as:

For C_3,

$$\begin{aligned}\Delta Q_{C_3} &= C_3 \times \Delta V_{C3} \\ &= \int_{\frac{\theta_1}{\omega}}^{\frac{\theta_2}{\omega}} \frac{V_{dc}}{R_L}\,dt + \int_{\frac{\theta_2}{\omega}}^{\frac{\pi-\theta_2}{\omega}} \frac{1.5V_{dc}}{R_L}\,dt + \int_{\frac{\pi-\theta_2}{\omega}}^{\frac{\pi-\theta_1}{\omega}} \frac{V_{dc}}{R_L}\,dt \end{aligned} \tag{4.5}$$

By solving this

$$\Delta Q_{C_3} = \frac{V_{dc}}{\omega \times R_L} \times (1.5\pi - 2\theta_1 - \theta_2) \tag{4.6}$$

And, it can be observed from Fig. 4.4 that,

$$\theta_1 = sin^{-1}\left(\frac{1}{3M}\right) \tag{4.7}$$

$$\theta_2 = sin^{-1}\left(\frac{2}{3M}\right) \tag{4.8}$$

With a maximum allowed voltage ripple of 10%, we have:

$$\frac{100\Delta V_{C_3}}{0.5V_{dc}} \leq 10 \tag{4.9}$$

Using these equations, we have:

$$C_3 \geq \frac{20}{2\pi \times f \times R_L}\left[1.5\pi - 2sin^{-1}\left(\frac{1}{3M}\right) - sin^{-1}\left(\frac{2}{3M}\right)\right] \tag{4.10}$$

A similar analysis for C_4 would show that it is equal to C_3, i.e.,

$$C_3 = C_4 \tag{4.11}$$

4.5 COMPARISON WITH OTHER TOPOLOGIES

Switched capacitor based multilevel inverter topology offers a high voltage gain and self-balancing capability whereas conventional topology like cascade H-bridge, diode clamped and flying capacitor offers a unity voltage gain but requires multiple dc source, more number of components which leads to increase in cost function. A proposed seven-level topology is compared with other recent seven-level topologies. The components for comparison are the number of levels (N_L), number of power switches (N_S), number of gate drivers (N_{GD}), number of isolated source (N_{IS}), number of diodes (N_D), number of capacitors (N_C), PIV, TSV, and CF.

Table 4.4 presented in this section summarized the comparative study of the proposed topology. Equal importance has been given to all the parameters while calculating CF which is further defined as:

$$\text{CF} = (\frac{N_{IS}}{N_L}) \times (N_S + N_{GD} + N_D + N_C + \frac{\alpha \times TSV}{\beta}) \tag{4.12}$$

where α is the weighing factor for assigning weightage to TSV in comparison to the component count and β is the voltage gain. Higher voltage gain reduces the requirement of any boosting circuit however it may lead to higher PIVs across the switches.

Higher voltage gain reduces the requirement of any boosting circuit; however, it may lead to higher PIVs across the switches. As shown in Table 4.4, [30] has higher PIV and CF compared

Table 4.4. *Comparison of proposed topology with other seven-level topologies*

Topologies	N_L	N_{IS}	N_S	N_D	N_{GD}	N_C	TSV	PIV	β	CF	
										$\alpha = 0.5$	$\alpha = 1.5$
[30]	7	1	10	0	10	2	18	3	3	3.57	4.42
[78]	7	2	7	2	7	1	8.5	1.5	1.5	5.66	7.28
[79]	7	1	10	0	10	3	13.5	1	1.5	3.92	5.17
[80]	7	1	12	0	12	2	16	2	3	4.09	4.85
[81]	7	1	14	0	14	2	14	1	3	4.62	5.28
[82]	7	1	10	0	10	4	9	1	1.5	3.85	4.71
[83]	7	1	16	0	16	2	16	2	3	5.23	6.00
Proposed	7	1	9	0	9	4	8	1	1.5	3.52	4.28

to the proposed topology. The topology proposed in [78] has less number of switches; however, it requires multiple dc source and power diodes. Although the topologies of [79–81] have a lower number of capacitors than the proposed one; however, these topologies have high TSV and high CF. From the resultant CF shown in Table 4.4, the proposed topology gives the less CF as compared to other topologies which implies that the proposed topology has better structural features.

4.6 EXPERIMENTAL VERIFICATION

The simulation results of the proposed seven-level inverter are taken in the MATLAB/SIMULINK to validate its practicability. In Table 4.5, simulation parameters are described. Modulation index (M) is set to 0.85. Figs. 4.8a and 4.8b presents the voltage and current output waveforms with a resistive load (i.e., 500Ω) and an inductive load (i.e., 50Ω, 120mH). Fig. 4.8c represents a sudden change in the load. For t < 1s, the load comprises of an inductive load (i.e., 50Ω, 120mH). After t = 1s load change to half the previous value. Therefore, load current is changed significantly and gets double by decreasing load to half of the earlier values. The proposed topology can

Table 4.5. *Parameters of simulation*

Parameters	Values
dc Source	100V
Capacitors (C_1, C_2, C_3, and C_4)	$1600\mu F$
Switching Frequency (f_{sw})	2000Hz
Fundamental Frequency (f)	50Hz
Resistive Load	500Ω
Inductive Load	50Ω ,120 mH

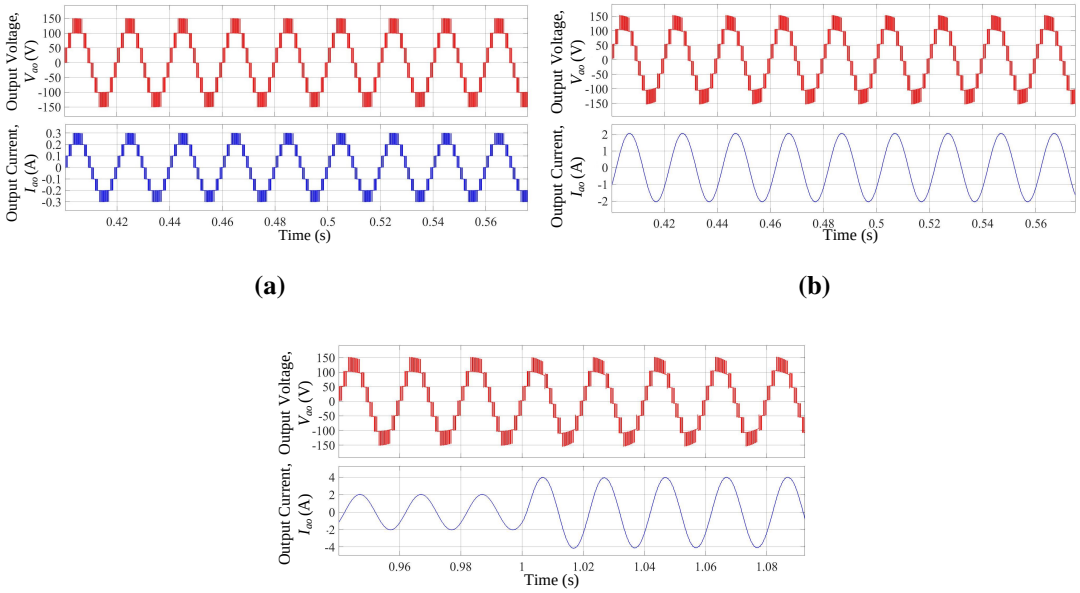
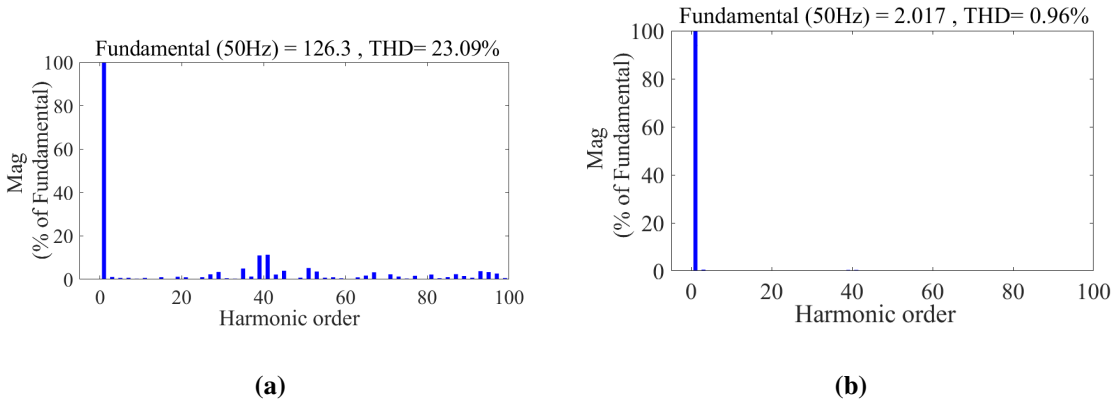


Fig. 4.8: *Simulation waveforms of the output voltage and current with (a) resistive load (i.e., 500Ω) (b) inductive load (i.e., 50Ω, 120mH) (c) transition in load from (50Ω, 120mH) to (25Ω, 60mH)*

generate seven levels with the amplitude of output voltage being 150V, and amplitude of output current changes with respect to change in load. Figs. 4.9a and 4.9b depict the THD of output voltage and current under an inductive load (i.e., 50Ω, 120mH) in which it can be seen that THD of output voltage and current is 23.09% and 0.96%, respectively. Fig. 4.10 shows the current through capacitors C_1, C_2, C_3, and C_4 under an inductive load (i.e., 50Ω, 120mH).



(a) **(b)**

Fig. 4.9: *Harmonic profile of the output voltage and current under an inductive load (i.e., 50Ω, 120mH).*

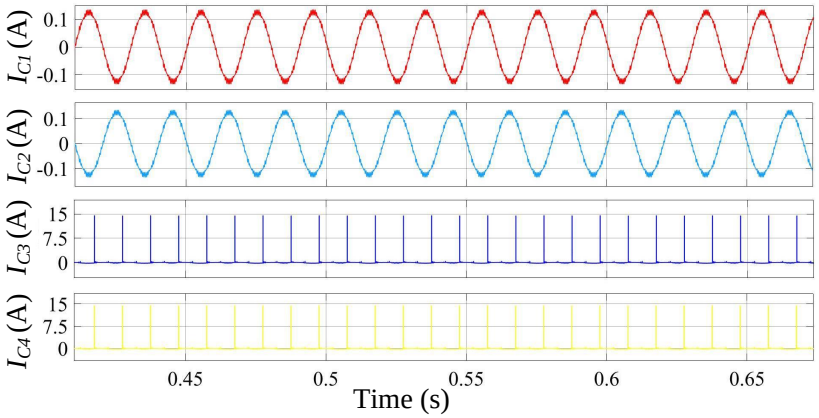


Fig. 4.10: *Current through capacitors C_1, C_2, C_3, and C_4 under an inductive load (i.e., 50Ω, 120mH).*

The waveforms at lower modulation indexes of 0.55 and 0.25 are shown in Figs. 4.11 and 4.12, respectively. Figs. 4.11a and 4.12a present the voltage and current output waveforms with a resistive load (i.e., 500Ω) having reduced levels with less peak value. Figs. 4.11b and 4.12b present the voltage and current output waveforms under an inductive load (i.e., 50Ω, 120mH). The waveforms for the over-modulation index of 1.25 are shown in Fig. 4.13. Fig. 4.13a presents the voltage and current output waveforms with a resistive load (i.e., 500Ω). Fig. 4.13b presents the voltage and current output waveforms under an inductive load (i.e., 50Ω, 120mH). Zero level is present in every value of the modulation index. At this level, all the capacitors (C_1, C_2, C_3, and C_4) are in parallel with the dc source which implies all the capacitors are balanced at their desired voltages.

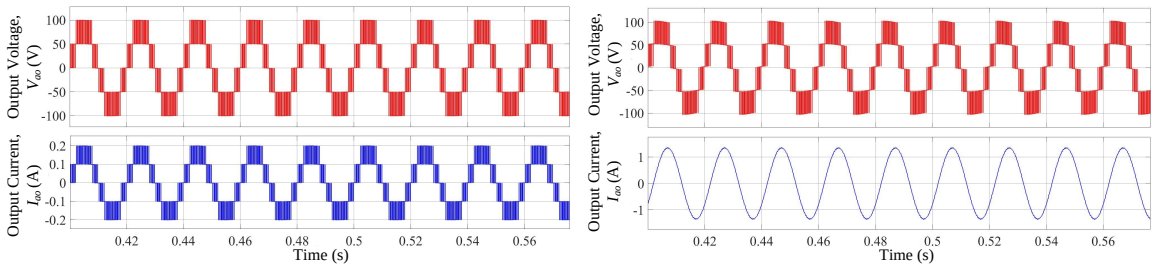


Fig. 4.11: *Output voltage and current waveforms for modulation index of 0.55 (a) resistive load (i.e., 500Ω) (b) inductive load (i.e., 50Ω, 120mH).*

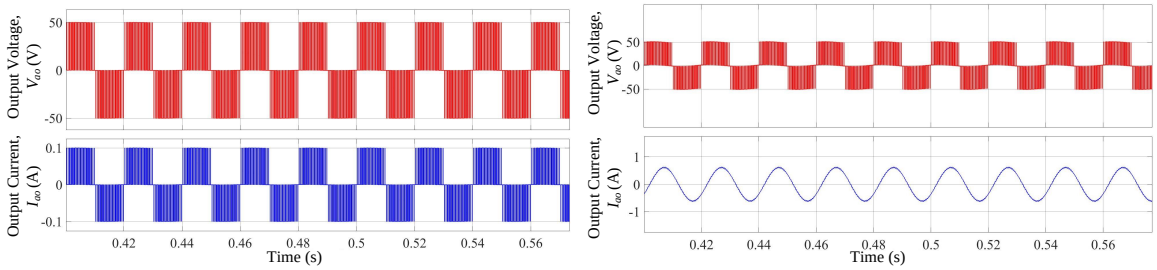


Fig. 4.12: *Output voltage and current waveforms for modulation index of 0.25 (a) resistive load (i.e., 500Ω) (b) inductive load (i.e., 50Ω, 120mH).*

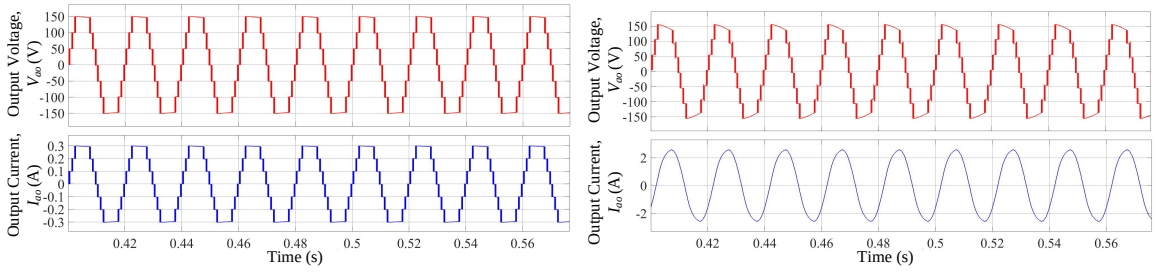


Fig. 4.13: *Output voltage and current waveforms for modulation index of 1.25 (a) resistive load (i.e., 500Ω) (b) inductive load (i.e., 50Ω, 120mH).*

The experimental photograph is shown in Fig. 4.14. OPAL-RT (OP4510) real-time controller was used in conjunction with MATLAB/Simulink to generate the desired gate signals for the power switches. These signals are obtained for modulation index of 0.85 and f_{sw}=2KHz. A prototype of the proposed seven-level SCMLI is designed further to validate the analysis and

simulation results. A MAGNA-POWER programmable DC power supply (SL1000-6.0/415+HS) is used as input dc supply of 100V. The device values chosen for the prototype are shown in Table 4.6.

Table 4.6. *Experimental parameters and components specifications*

Parameters	Values
MOSFET	SiHG47N60
Isolated Gate driver IC	Si82071AB
Capacitors (C_1, C_2, C_3, and C_4)	1600 μF
Controller	Opal-RT OP4510
Voltage Senor	LEMLV25-P
Current Senor	HE025T01

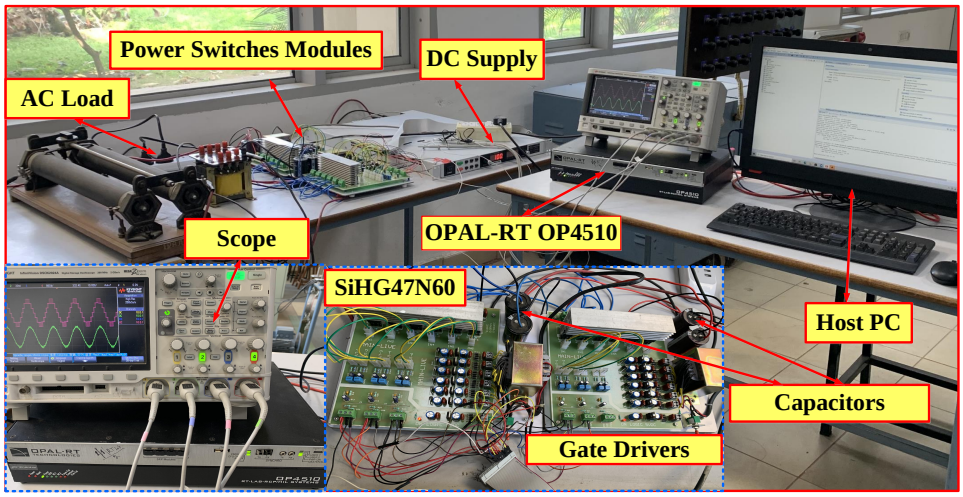


Fig. 4.14: *Photograph of experimental setup*

Fig. 4.15 shows the experimental results of the proposed inverter. Figs. 4.15a and 4.15b depicts the output voltage and current waveforms with a resistive load (i.e., 500Ω) and an inductive load (i.e., 50Ω, 120mH). Fig. 4.15c shows that capacitors C_1, C_2, C_3, and C_4 gets approximately charged to 50V, and they are within the range of 10% voltage ripples. Figs. 4.16a and 4.16b depict the voltage waveforms of switches S_1 to S_9. The PIV of the bidirectional switch

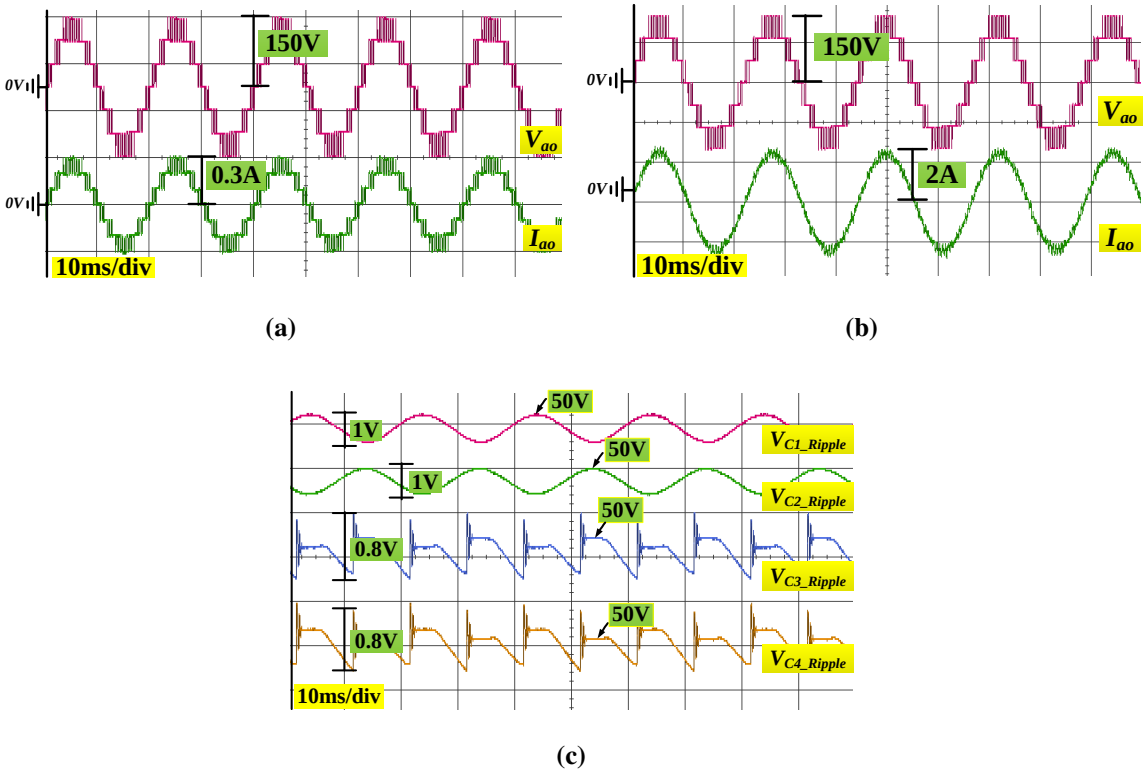


Fig. 4.15: *Experimental results showing (a) output voltage and output current with a resistive load (500Ω) (b) output voltage and output current with an inductive load (50Ω,120mH) (c) voltage across capacitors C_1, C_2, C_3, and C_4*

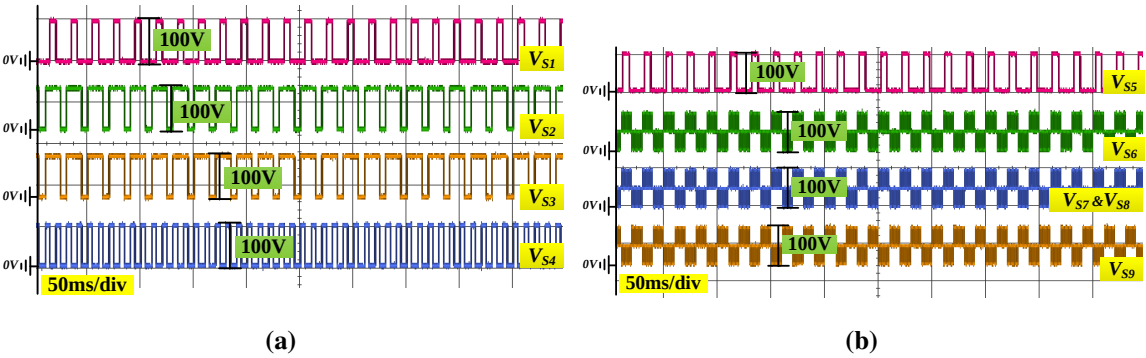


Fig. 4.16: *Experimental results showing switching signals for power switches*

(S_7 and S_8) is 50V for each, and for other switches, it is 100V. Therefore, PIV across the switches does not exceed input source.

The closed-loop performance characteristic is shown in Fig. 4.17. In this figure, the grid voltage is in phase with the grid current, resulting in a UPF. The amplitudes of the grid voltage and current are mentioned as 130V and 11.5A, respectively

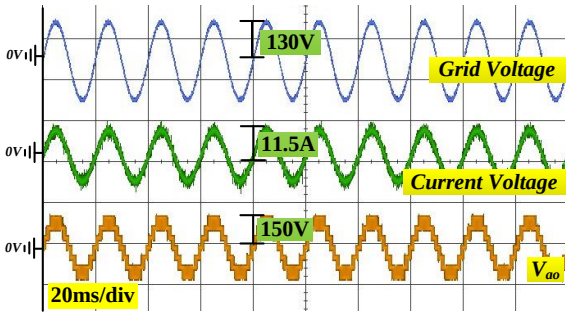


Fig. 4.17: *Experimental waveforms of grid connected system*

4.7 CHAPTER SUMMARY

This chapter presents a seven-level inverter suited for the grid-connected PV system. The experimental results validate the proposed power circuit. The following observations are made from this study:

- The proposed topology effectively manages voltage stress across the power switches, limiting it to a maximum value of V_{dc} and ensuring safe and reliable operation.
- With the use of only nine switches, it demonstrates the capability to generate a seven-level output voltage, providing greater flexibility and superior performance in various applications.
- Its design allows for seamless extension to 3-ϕ operation, enabling easy integration into 3-ϕ systems and expanding its range of applications.
- By utilizing a single dc source for both 1-ϕ and 3-ϕ configurations, the system simplifies the overall design, reducing complexity and enhancing efficiency.
- The self-balancing mechanism implemented through proper switching states ensures that all capacitors are evenly charged, optimizing voltage distribution and improving overall system stability.
- The reduced device count in the topology results in a low value of CF.

Chapter–5

Design of Switched Capacitors based Nine-Level Inverter for Grid Connected PV System

5.1 GENERAL

In the topology presented in Chapter 4, a structure is introduced to generate seven levels while using a low number of switching devices and achieving a low PIV voltage. However, the non-complementary nature of certain switches leads to an increase in the number of gate drivers and subsequently raises the CF value. To address this issue and further increase the number of levels while reducing the cost function, this chapter introduces a novel self-balancing nine-level inverter design. The objective of this design is to generate a nine-level voltage with a gain of two, utilizing only a single dc source, eight power switches, three capacitors, and two diodes. The proposed topology ensures inherent balance of the capacitor voltages without requiring additional circuitry. In this design, six power switches have a PIV equal to or less than the source voltage, while the remaining two switches have twice the PIV.

The complementary nature of the power switches employed in the proposed topology allows for a reduced number of gate drivers, simplifying the overall circuit complexity. Additionally, the self-balancing capability of the capacitor voltages contributes to a simplified control system. This chapter provides a comprehensive description of the topology, including

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doi: https://doi.org/10.1002/cta.3596

its mode of operation, modulation strategy, and capacitor design. To assess the advantages of the proposed inverter, a comparison is made with SCMLIs. The analysis highlights the superior features of the proposed design, showcasing its improved performance and efficiency compared to existing solutions. Finally, a nine-level prototype is constructed to validate both the theoretical analysis and the practical effectiveness of the proposed inverter.

5.2 DESCRIPTION OF TOPOLOGY

A single-stage circuit synthesizes nine-level with a single input source having an overall voltage gain of two. The circuit description and various switching states are discussed in this section.

5.2.1 Circuit Configuration

Fig. 5.1 depicts the proposed nine-level inverter. It comprises of eight power switches, three capacitors (C_1, C_2 and C_3), two diodes (D_a and D_b), and a single dc source V_{dc}. Each power switch in this topology consists of a transistor with an anti-parallel diode. Therefore, all switch has the capability for the two-way flow of current. The load terminals are shown with nodes 'a' and 'o'. The load voltage and load current are denoted as V_{ao} and I_{ao}, respectively. The load current is assumed to be positive when it exits terminal 'a' and enters terminal 'o'. The switches pairs (S_1, $\overline{S_1}$), (S_2, $\overline{S_2}$), (S_3, $\overline{S_3}$) and (S_4, $\overline{S_4}$) are complementary.

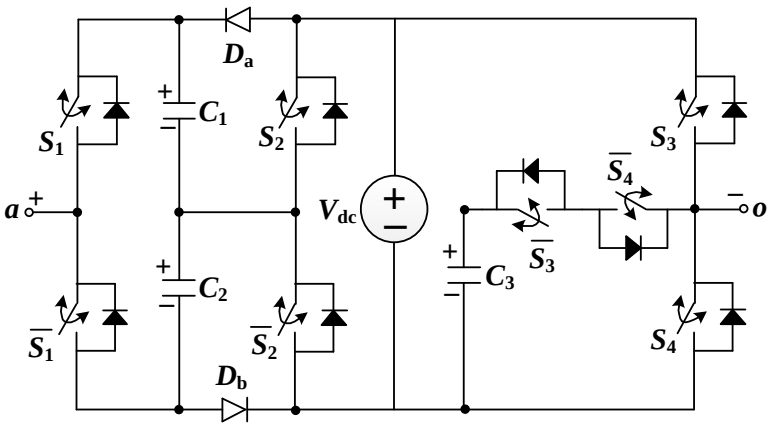


Fig. 5.1: *Schematic circuit of the proposed nine-level inverter*

Table 5.1. *Switching modes for different voltage levels*

States	V_{ao}	Conducting Devices		Capacitors					
		$I_{ao} > 0$	$I_{ao} < 0$	$I_{ao} > 0$			$I_{ao} < 0$		
				C_1	C_2	C_3	C_1	C_2	C_3
λ_1	0	$T(S_1)$, $D(\overline{S_2})$, $D(S_3)$, $T(\overline{S_4})$, D_a	$D(S_1)$, $T(\overline{S_2})$, $T(\overline{S_3})$, $D(S_4)$	C	-	-	C	-	-
λ_2	$0.5V_{dc}$	$T(S_1)$, $D(\overline{S_2})$, $T(\overline{S_3})$, $D(\overline{S_4})$, D_a	$D(S_1)$, $T(\overline{S_2})$, $D(\overline{S_3})$, $T(\overline{S_4})$	C	-	C	C	-	D
λ_3	V_{dc}	$T(S_1)$, $D(\overline{S_2})$, $T(\overline{S_3})$, $T(S_4)$, D_a	$D(S_1)$, $T(\overline{S_2})$, $T(\overline{S_3})$, $D(S_4)$	C	-	-	C	-	-
λ_4	$1.5V_{dc}$	$T(S_1)$, $T(S_2)$, $T(\overline{S_3})$, $D(\overline{S_4})$	$D(S_1)$, $D(S_2)$, $D(\overline{S_3})$, $D(\overline{S_4})$, D_b	D	C	C	C	C	D
λ_5	$2V_{dc}$	$T(S_1)$, $T(S_2)$, $T(\overline{S_3})$, $T(S_4)$	$D(S_1)$, $D(S_2)$, $D(\overline{S_3})$, $D(S_4)$, D_b	D	C	-	C	C	-
λ_6	0	$D(\overline{S_1})$, $T(S_2)$, $T(\overline{S_3})$, $T(S_4)$	$T(\overline{S_1})$, $D(S_2)$, $D(\overline{S_3})$, $D(S_4)$, D_b	C	-	-	C	-	-
λ_7	$-0.5V_{dc}$	$D(\overline{S_1})$, $T(S_2)$, $T(\overline{S_3})$, $D(\overline{S_4})$	$T(\overline{S_1})$, $D(S_2)$, $D(\overline{S_3})$, $T(\overline{S_4})$, D_b	-	C	C	-	C	D
λ_8	$-V_{dc}$	$D(\overline{S_1})$, $T(S_2)$, $D(S_3)$, $T(\overline{S_4})$	$T(\overline{S_1})$, $D(S_2)$, $T(S_3)$, $D(\overline{S_4})$, D_b	-	C	-	-	C	-
λ_9	$-1.5V_{dc}$	$D(\overline{S_1})$, $D(\overline{S_2})$, $T(\overline{S_3})$, $D(\overline{S_4})$, D_a	$T(\overline{S_1})$, $T(\overline{S_2})$, $D(\overline{S_3})$, $T(\overline{S_4})$	C	C	C	C	D	D
λ_{10}	$-2V_{dc}$	$D(\overline{S_1})$, $D(\overline{S_2})$, $D(S_3)$, $T(\overline{S_4})$, D_a	$T(\overline{S_1})$, $T(\overline{S_2})$, $T(S_3)$, $D(\overline{S_4})$	C	C	-	C	D	-

5.2.2 Modes of Operations

For the proposed inverter, there are two possibilities for load current, i.e., $I_{ao} > 0$ and, $I_{ao} < 0$ in each state, as shown in Figs. 5.2 and 5.3.

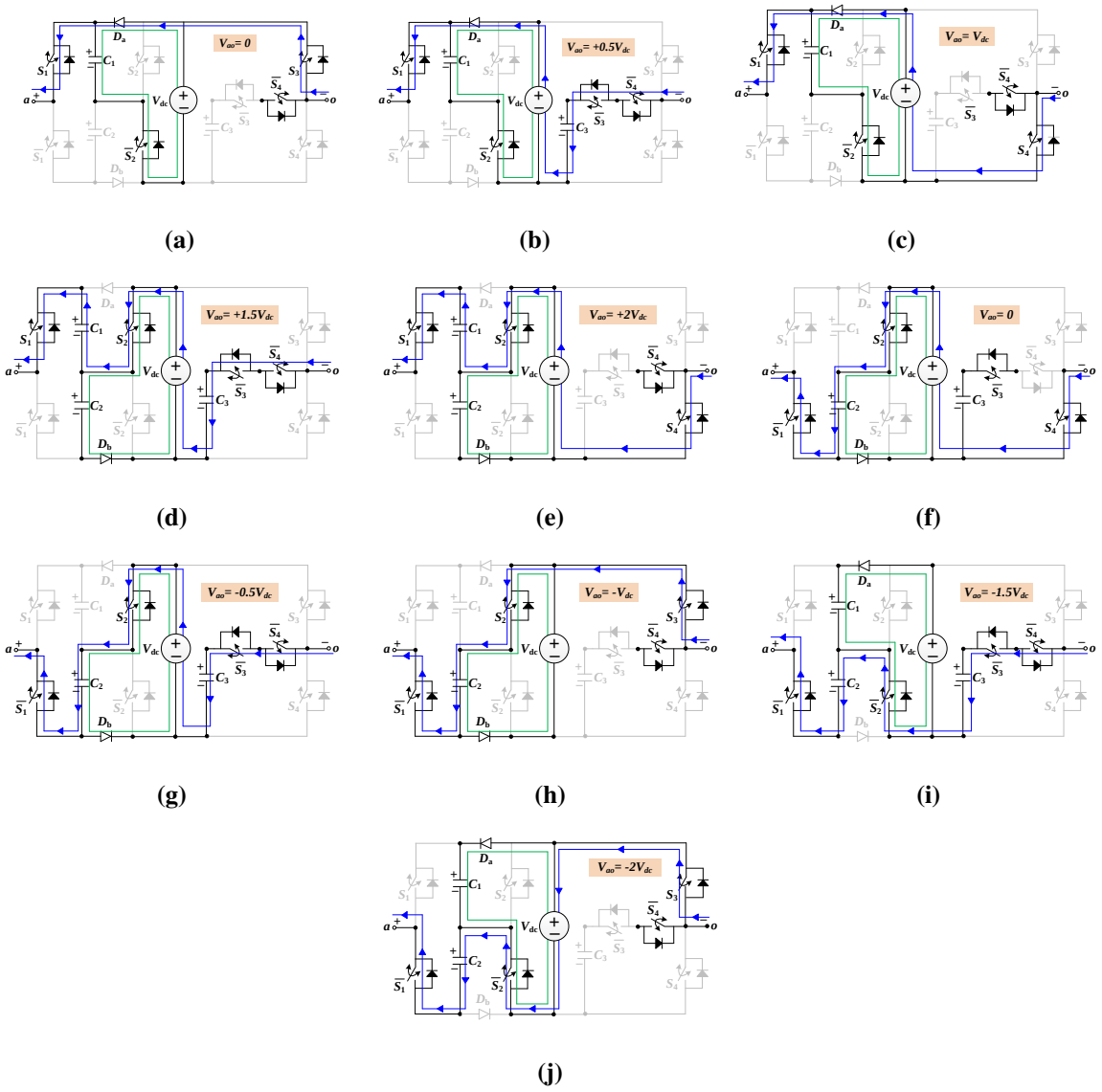


Fig. 5.2: *Different output states of the proposed nine-level inverter for ($I_{ao} < 0$) (a) State λ_1, (b) State λ_2, (c) State λ_3, (d) State λ_4, (e) State λ_5, (f) State λ_6, (g) State λ_7, (h) State λ_8, (i) State λ_9, (j) State λ_{10}*

In these figures, conduction paths are shown by the black line; the current path is indicated by blue ($I_{ao} > 0$) and red ($I_{ao} < 0$), and the capacitor charging path is shown by green lines. There may/may not be a capacitor charging path. Table 5.1 summarizes the various switching states, and '1' and '0' represent the ON and OFF states of power switches. Capacitors states are

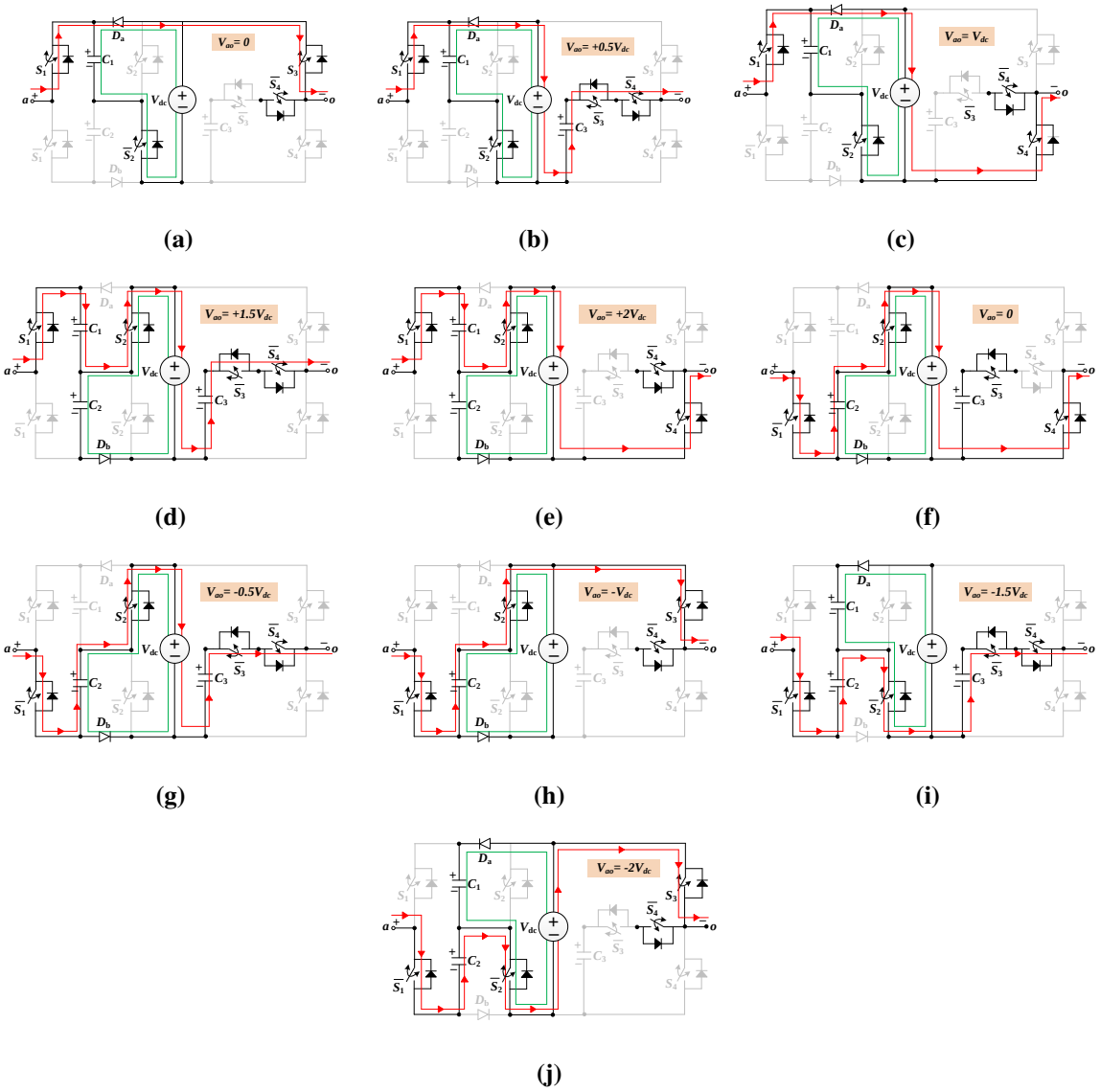


Fig. 5.3: *Different output states of the proposed nine-level inverter for ($I_{ao} > 0$) (a) State λ_1, (b) State λ_2, (c) State λ_3, (d) State λ_4, (e) State λ_5, (f) State λ_6, (g) State λ_7, (h) State λ_8, (i) State λ_9, (j) State λ_{10}*

shown by 'C' , 'D', and '-'i.e., charging, discharging, and idle state, respectively. A capacitor C_1 and C_2 are maintained voltage at V_{dc} as they are parallel with the input dc source in specific states, as shown in Figs. 5.2 and 5.3. Capacitor C_3 is in reversed series with positive load current ($I_{ao} > 0$) path and charging in levels $0.5V_{dc}$, $1.5V_{dc}$, $-0.5V_{dc}$, $-1.5V_{dc}$ as shown in Fig. 5.2(b), 5.2(d), 5.2(g), and 5.2(i) which is symmetric for the discharging path with the negative load current ($I_{ao} < 0$) as shown in Fig. 5.3(b), 5.2(d), 5.3(g), and 5.3(i). This symmetric operation results in the inherent balancing of the capacitor C_3.

The reverse blocking voltage of the power switch and the diode is essential for topology design. Out of eight switches, the maximum blocking voltage of two switches (S_1, $\overline{S_1}$) is twice the input supply voltage, i.e., $2V_{dc}$, for four switches (S_2, $\overline{S_2}$), (S_3, S_4) and two diodes (D_a, D_b), it is equivalent to the input supply voltage, i.e., V_{dc} and for the rest two switches ($\overline{S_3}$, $\overline{S_4}$), it is $0.5V_{dc}$. As a result, the TSV, which is the sum of maximum blocking voltages of all power switches and diodes, is $11V_{dc}$. Fig. 5.4 depicts the voltage stress of all switches when all voltage levels at the output are considered.

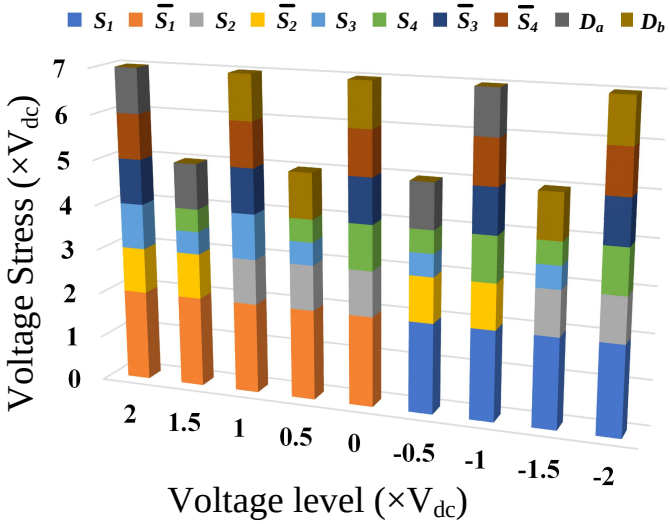


Fig. 5.4: *Voltage stress of power switches and diodes for all voltage levels*

5.3 MODULATION SCHEME

For the modulation of MLIs, high and low switching frequency methodologies have been used [84–86]. In this work, a LSPWM scheme generates the nine-level. The modulation index *(M)* is defined as:

$$M = \frac{A_{ref}}{3 \times A_{cr}} \tag{5.1}$$

Where A_{cr} and A_{ref} are amplitude of the carrier and reference waveform respectively. Fig. 5.5 depicts the generated reference signal (A_{ref}) with 50Hz frequency and high-frequency triangular signals (viz. $\pm A_{cr1}$, $\pm A_{cr2}$, $\pm A_{cr3}$, and $\pm A_{cr4}$) to modulate the proposed nine-level inverter. For generation of PWM signals, reference signal compared with carrier signal and generates high frequency switching pulses. When reference signal greater than carrier signals, the comparator will produce output '1' i.e., ON; otherwise, it will produce output '0' i.e., OFF.

The comparator will yield '0' if the reference signal is bigger than the carrier signals; otherwise, '1'.The switching pulses are obtained when the comparator output signals are added further to produce the aggregated signals 'a(t)' constant levels. The output of the desired signal is then sent to switches using the mappings illustrated in Fig. 5.6

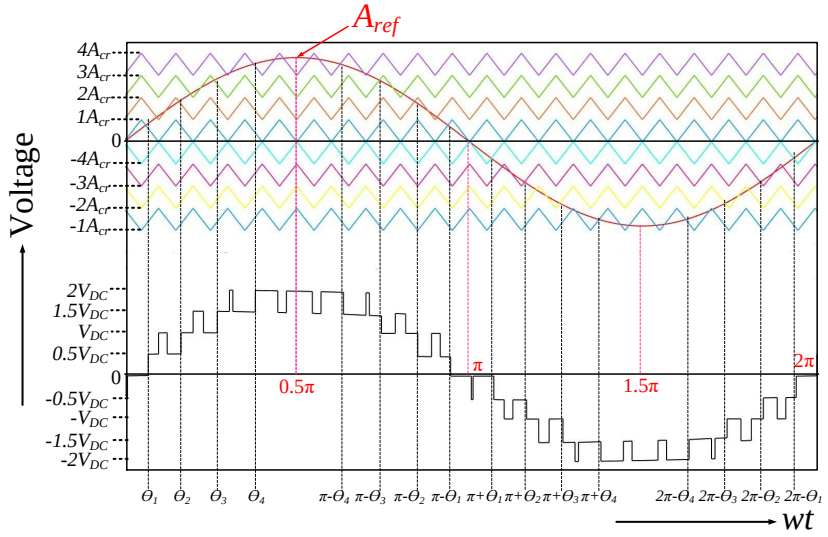


Fig. 5.5: *Generated reference and high-frequency triangular signals to modulate the proposed nine-level inverter*

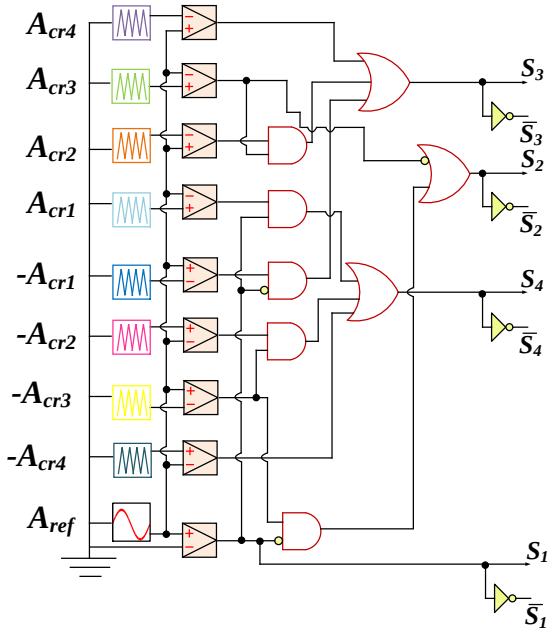


Fig. 5.6: *Modulation scheme of the proposed topology*

5.4 PIV RATING, CAPACITOR DESIGN, POWER LOSS AND RELIABILITY ANALYSIS

5.4.1 PIV Ratings of Power Switches and Diodes

Table 5.2 shows the PIV needs for the power switches and diodes in the proposed inverter. The PIV rating of four power switches and two diodes is 50% of the peak output voltage. For only two power switches it is 100% of the peak output voltage. For bidirectional power switch, it is 50% each of the peak output voltage.

Table 5.2. *PIV across power switches and diodes*

PIV	Switches and Diodes
$0.5V_{\mathrm{dc}}$	$\overline{S_3}$ and $\overline{S_4}$
V_{dc}	S_2, $\overline{S_2}$, S_3, S_4, D_{a} and D_{b}
$2V_{\mathrm{dc}}$	S_1 and $\overline{S_1}$

5.4.2 Capacitors Calculation

By using the switched-capacitors approach, the three capacitors C_1, C_2 and C_3 in the proposed inverter are kept at V_{dc}, V_{dc}, and $0.5V_{dc}$, respectively. Voltage ripples will emerge on these capacitors as they are discharged to supply the load, although they should not exceed 10% of the capacitors maximum voltages. The voltage ripple of the capacitor is determined by the discharge time and load current. When a load is only resistive, it considers the worst case [57]. For a resistive load R_L, the maximum discharge may be expressed as:

For C_1,

$$\begin{aligned}\Delta Q_{C_1} &= C_1 \times \Delta V_{C1} \\ &= \int_{\frac{\theta_2}{\omega}}^{\frac{\theta_4}{\omega}} \frac{1.5V_{dc}}{R_L}\,dt + \int_{\frac{\theta_4}{\omega}}^{\frac{\pi-\theta_4}{\omega}} \frac{2V_{dc}}{R_L}\,dt + \int_{\frac{\pi-\theta_4}{\omega}}^{\frac{\pi-\theta_3}{\omega}} \frac{V_{dc}}{R_L}\,dt \end{aligned} \tag{5.2}$$

By solving the above equation

$$\Delta Q_{C_1} = \frac{V_{dc}}{\omega \times R_L} \times (2\pi - 3\theta_3 - \theta_4) \tag{5.3}$$

And, it can be observed from Fig. 5.5 that,

$$\theta_3 = sin^{-1}\left(\frac{3}{4M}\right) \tag{5.4}$$

$$\theta_4 = sin^{-1}\left(\frac{1}{M}\right) \tag{5.5}$$

With a maximum allowed voltage ripple of 10%, we have:

$$\frac{100\Delta V_{C_1}}{V_{dc}} \leq 10 \tag{5.6}$$

Using these equations, we have:

$$C_1 \geq \frac{10}{2\pi \times f \times R_L}\left[2\pi - 3sin^{-1}\left(\frac{3}{4M}\right) - sin^{-1}\left(\frac{1}{M}\right)\right] \tag{5.7}$$

A similar analysis for C_1 would show that it is equal to C_2, i.e.,

$$C_1 = C_2 \tag{5.8}$$

For C_3,

$$\begin{aligned}\Delta Q_{C_3} &= C_3 \times \Delta V_{C3} \\ &= \int_{\frac{\pi+\theta_1}{\omega}}^{\frac{\pi+\theta_2}{\omega}} \frac{0.5V_{dc}}{R_L}\,dt + \int_{\frac{\pi+\theta_3}{\omega}}^{\frac{\pi+\theta_4}{\omega}} \frac{1.5V_{dc}}{R_L}\,dt\end{aligned} \tag{5.9}$$

By solving the above equation

$$\Delta Q_{C_3} = \frac{V_{dc}}{\omega \times R_L} \times (0.5(\theta_2 - \theta_1) + (1.5(\theta_2 - \theta_1)) \tag{5.10}$$

In equations 5.4 and 5.5 , the value of θ_3 and θ_4 is calculated, and for θ_1 and θ_2 it can be depicted from Fig. 5.5 that,

$$\theta_1 = sin^{-1}\left(\frac{1}{4M}\right) \tag{5.11}$$

$$\theta_2 = sin^{-1}\left(\frac{1}{2M}\right) \tag{5.12}$$

With a maximum allowed voltage ripple of 10%, we have:

$$\frac{100\Delta V_{C_3}}{0.5V_{dc}} \leq 10 \tag{5.13}$$

Using these equations, we have:

$$C_3 \geq \frac{20}{2\pi \times f \times R_L} \times \left[0.5(sin^{-1}\left(\frac{1}{2M}\right) - sin^{-1}\left(\frac{1}{4M}\right)\right) + 1.5(sin^{-1}\left(\frac{1}{M}\right) - sin^{-1}\left(\frac{3}{4M}\right))\Big] \tag{5.14}$$

5.4.3 Power Loss

The inverter efficiency can be defined as:

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}} + P_{\text{loss}}} \tag{5.15}$$

Where, P_{out}, P_{in}, and P_{loss} are the output power, input power, and total power losses, respectively. Switching and conduction losses account for most of the overall power loss in an MLI which is already explain in Chapter 3 (Section 3.4.3).

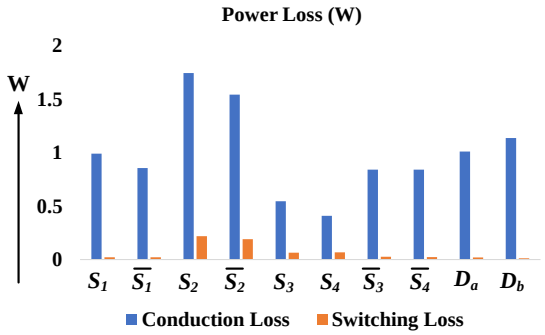


Fig. 5.7: *Switching and conduction power loss of the proposed topology*

Power losses are calculated in PLECS based simulation model. SiHG47N60 MOSFETs were employed as power switches, and its datasheet was imported for power loss analysis. Fig. 5.7 shows the power loss distribution in which switching loss across and conduction loss across S_2 and $\overline{S_2}$, are high as compared to other transistors. With a combined efficiency of 95.42% with output power of 220W, all power switches and diodes incur total losses of 10.59 W. Fig. 5.8 displays the variation in efficiency with change in modulation index. Fig. 5.9 shows the tested results in variation of efficiency with change in output power with different values of modulation index. Fig. 5.10 depicts the ripple loss in the capacitors (C_1, C_2, C_3) of the proposed topology. The switching and conduction losses across power switches and diodes are shown in Table 5.3.

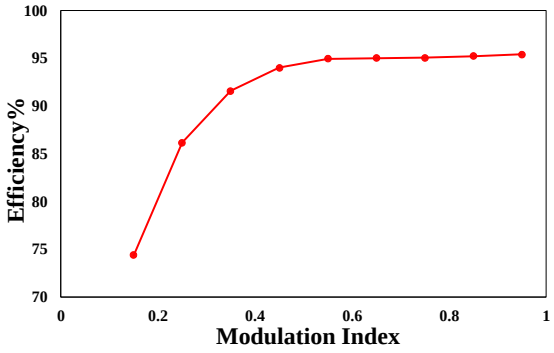


Fig. 5.8: *Efficiency versus modulation index*

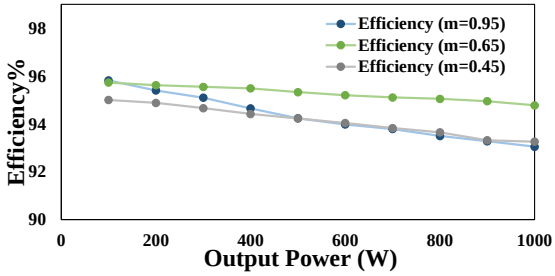


Fig. 5.9: *Efficiency versus output power with different modulation index*

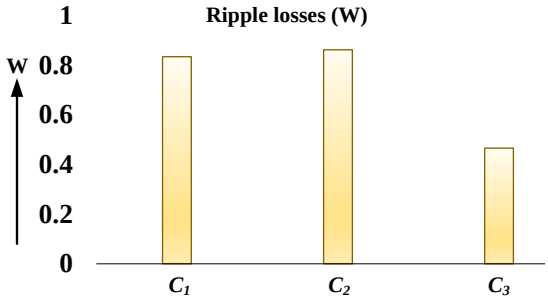


Fig. 5.10: *Ripple loss in capacitors (C_1, C_2, C_3)*

5.4.4 Reliability Analysis of Proposed Inverter

The probability that a system, subsystem, or specific component will perform desired functions for a predetermined observable period under the existing operating and environmental conditions/restrictions is known as reliability.

Table 5.3. *Distribution of switching and conduction losses*

Switches/Diodes	Conduction Losses (W)	Switching Losses (W)
S_1	0.9903	0.0209
$\overline{S_1}$	0.8562	0.0212
S_2	1.7452	0.2181
$\overline{S_2}$	1.5432	0.19
S_3	0.5451	0.0634
S_4	0.4094	0.0672
$\overline{S_3}$	0.8411	0.0261
$\overline{S_4}$	0.8411	0.0222
D_a	1.011	0.0186
D_b	1.1378	0.0107

Reliability analysis is used in order to quantify the risk level. The goal of this analysis is to identify the crucial parameters / components and determine the spare/maintenance design. The reliability profile, a different idea, offers details about the current condition of an item's health and remaining life. Based on the Military Handbook MIL-HDBK-217F [87], reliability is estimated for the proposed inverter. Additionally, the IEC/TR 62380 standard is used to verify the reliability of proposed inverter which considers temperature for reliability prediction for each component. Semiconductor devices, capacitors, and cooling systems are indeed the most vulnerable components in power electronics converters which leads to failure of system. The following is the equation for the probability function, $R_s(t)$ during the time period, t:

$$R_s(t) = e^{-(\lambda_{\text{system}} \times t)} \tag{5.16}$$

Where λ_{system}=λ_S+λ_C shows the failure rate of the system. The Mean Time to Failure (MTTF) can be calculated as:

$$MTTF = \int_0^{\infty} R_s(t)dt = \frac{1}{\lambda_{\text{system}}} \tag{5.17}$$

Table 5.4. *Parameter values used for reliability estimation*

Parameters	Value
λ_b of Switches	0.012
λ_b of Capacitors	0.00040
V_{rating}, Capacitors	200 V
θ_{jc}	1 (°C/W)
θ_{ca}	62 (°C/W)
T_a	25 °C
π_A	8
π_E	9
π_Q	8
C	1600 μF

The Mean Time to Repair (MTTR) defines as the average time that the system is in repairing condition. This parameter is obtained as:

$$MTTR = \frac{1}{\mu_{\text{system}}} \tag{5.18}$$

MTBF is the mean cycle time between the failures of the system. For systems with much higher repair rate than the failure rate, MTBF can be approximated by MTTF [7]:

$$MTBF = MTTF + MTTR = \frac{1}{\lambda_{\text{system}}} + \frac{1}{\mu_{\text{system}}} \approx \frac{1}{\lambda_{\text{system}}} \tag{5.19}$$

The failure rate switch (λ_S)and capacitor (λ_C) (failures/10^6 hours) can be calculated using the following:

$$\lambda_S = \lambda_b \pi_T \pi_A \pi_E \pi_Q \tag{5.20}$$

$$\lambda_C = \lambda_b \pi_T \pi_C \pi_S \pi_E \pi_Q \tag{5.21}$$

λ_b is a component's basic failure rate; π_T denotes the temperature factor. Temperature factor semiconductor switches can be stated as.

$$\pi_{(T|\text{switch})} = exp\left[-1925\left(\frac{1}{T_j + 237} - \frac{1}{298}\right)\right] \tag{5.22}$$

Table 5.5. *Reliability estimation of power switches and system*

Switch	λ_{switch} (failures/10^6 hours)	$\lambda_{\text{system}} = \lambda_{\text{switch}} + \lambda_C$ (failures/10^6 hours)	MTTF ≈ MTBF (Years/failures)
S_1	7.188	7.673	14.85
$\overline{S_1}$	7.223	7.708	14.78
S_2	9.891	10.376	10.98
$\overline{S_2}$	9.946	10.431	10.92
S_3	7.209	7.694	14.81
S_4	7.182	7.667	14.86
$\overline{S_3}$	7.182	7.667	14.86
$\overline{S_4}$	7.202	7.687	14.83

Capacitor temperature factor:

$$\pi_{(T|\text{cap})} = exp\left[\frac{-0.15}{8.617 \times 10^{-5}}\left(\frac{1}{T_a + 237} - \frac{1}{298}\right)\right] \tag{5.23}$$

The junction temperature, denoted as T_j, is provided by the following equation

$$T_j = T_c + \theta_{jc} P_{\text{loss}} \tag{5.24}$$

$\theta_{jc}$is the maximum junction to case thermal resistance. T_c, case temperature, given by the below equation

$$T_c = T_a + \theta_{ca} P_{\text{loss}} \tag{5.25}$$

T_a is the ambient temperature; $_{ca}$ the maximum case to ambient thermal resistance; π_A the application factor. π_S the voltage stress factor for a capacitor

$$\pi_s = \left(\frac{V_s}{0.6}\right)^{17} + 1 \tag{5.26}$$

V_s is the ratio of the applied voltage to the rated voltage of the component; π_Q the quality factor which is equal to 8 for Plastic quality; π_E the environment factor, which is equal to 9 for

component operating on the ground. π_C, capacitance factor, which is given by the below equation

$$\pi_C = C^{0.23} \tag{5.27}$$

C is the capacitance of the capacitor in μF. All the above-mentioned parameters are listed in

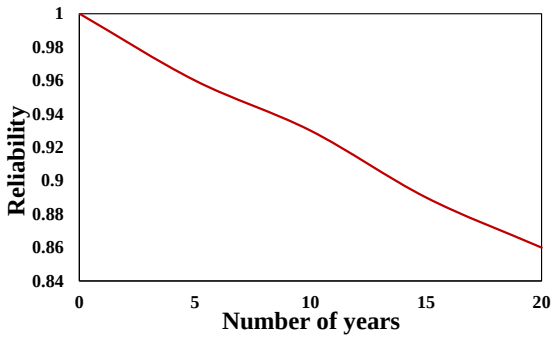


Fig. 5.11: *Reliability profile of the proposed inverter*

Table 5.4 along with their values, which are taken from MLI- HDBK-217F [87]. Table 5.5 shows failure rate of power switches (λ_S) along with total failure rate of system λ_{system} with respect to that particular power switch and mean time of failure (MTTF) of the proposed topology. The system's reliability is calculated for 20 years and shown in Fig. 5.11.

5.5 COMPARISON WITH OTHER TOPOLOGIES

To analyse and assess the proposed topology, comparison research is conducted. The comparison analysis is made in terms of the number of levels (N_L), the number of input dc sources (N_{IS}), the number of power switches and gate drivers (N_S and N_{GD}), the number of diodes (N_D), the number of capacitors (N_C), the number of additional device (N_A), TSV, PIV and CF. The cost function is defined as:

$$CF = \left(\frac{N_{IS}}{N_L}\right) \times \left\{N_S + N_D + N_A + N_{GD} + N_C + \left(\frac{\alpha \times TSV}{\beta}\right)\right\} \tag{5.28}$$

Where, α is the weightage factor for assigning weight to TSV, and β is voltage gain.

Table 5.6 summarizes the comparison of the proposed topology with other SCMLI topologies. It can be seen from the table that topologies [57, 88–90] have low PIV, but the components count increases.

Table 5.6. *Comparison of the proposed topology with other SCMLI topologies*

Topologies	N_L	N_{IS}	N_S	N_D	N_A	N_{GD}	N_C	TSV (V_{dc})	PIV	β	N_{COMP} /N_L	CF α=1
[57]	9	1	10	10	1	8	2	11	2	2	3.444	4.056
[88]	9	1	12	12	0	11	2	11	1	2	4.111	4.722
[89]	9	1	11	11	0	11	2	11	1	2	3.889	4.500
[44]	9	1	12	12	0	12	3	24	4	4	4.333	5.000
[91]	9	1	12	12	0	12	2	22	2	4	4.222	4.833
[92]	9	1	8	11	0	8	3	23	4	4	3.333	3.972
[90]	9	1	11	11	0	11	2	10	1	2	3.889	4.444
[93]	9	2	8	8	0	8	2	18	2	2	2.889	7.778
[94]	9	1	8	10	1	8	4	18	2	2	3.444	4.444
[95]	9	1	8	10	0	8	3	16	2	2	3.222	4.111
[96]	9	1	8	9	0	8	2	20	2	2	3.000	4.111
[97]	9	1	12	12	0	11	3	10.5	1	2	4.223	4.805
[98]	9	1	10	14	0	10	3	9.5	1	2	4.112	4.638
[99]	9	1	10	12	0	9	2	11	1	2	3.667	4.227
[100]	9	2	8	10	0	8	2	16	3	3	3.112	7.407
[101]	9	1	11	11	0	11	2	9	1	2	3.889	4.389
[102]	9	1	8	11	0	8	2	11	2	2	3.223	3.834
Proposed	9	1	8	10	0	4	3	11	2	2	2.778	3.389

Topologies presented in [44, 91, 92] have high voltage gain compared to proposed topology but require more components, increasing the CF. The topology illustrated in [94] synthesizes nine-level but is characterized by high TSV and the requirement of additional dc bus capacitors.

Table 5.7. *Comparison of The proposed topology with other SCMLI topologies in terms of efficiency, capacitor value and THD*

Topologies	Efficiency	C-value	THD	
			V_THD	I_THD
[57]	95% @1KW	1000μF	NA	NA
[88]	80.61% @15.47 W	NA	NA	NA
[89]	NA	4700μF	13.95%	NA
[44]	97.6% @2KW	4mF, 2 mF	16.68%	NA
[91]	NA	2200μF, 3300μF	NA	NA
[92]	93% @500W	3300μF	NA	1.8%
[90]	95.24% @1KW	1000μF	NA	NA
[93]	95.75%@1KW	2.0mF	NA	4.19%
[94]	95.51%@500W	1000μF, 820μF	15.9%	1.82%
[95]	96.4%@500W	860μF, 1200μF	NA	1.6%
[96]	96.47%@333.33 W	1000μF	NA	NA
[97]	97.55%@250W	2200μF, 4700μF	16.25%	1.2%
[98]	97%@500W	2200μF, 3300μF	7.97%	NA
[99]	97.86% @800W	4700μF	16.3%	NA
[100]	94.5% @104W	100μF	9.19%	3.13%
[101]	NA	1.2mF	13.51%	1.52%
[102]	97.58% @1.344kW	4700μF	3.39%	NA
Proposed	95.42% @220W	1600μF	15.57%	0.89%

In [93], although the number of switches is the same as the proposed topology, it requires more gate drivers and two dc sources. The topologies in [94, 95] synthesize nine-level but have high

TSV. In topology [96] although the number of switches is same but it requires a greater number of gate drivers.

Table 5.7 summarizes the comparison of proposed topologies with other in terms of efficiency, capacitor values and THD. It can be seen from table that topologies [97–99, 102] have large capacitors value as compare to proposed topology which leads to bulkiness of the system. Topology [100] has two input sources due to which its CF increases as compare to proposed topology and also has high THD in output current. In [101], components required to produce nine-level are high which increases it cost and have high THD. Moreover, in topologies [97, 99], THD in output voltage and current is also high, due to which filter size increase in the system. To overcome these issues, The proposed topology has a smaller number of switches with less gate drivers as switches are complimentary, which leads to low CF.

5.6 EXPERIMENTAL VERIFICATION

A MATLAB/Simulink environment has been used to investigate the proposed topology to verify the theoretical concept. Also, the viability of the proposed topology has been achieved by carrying out the experimental study on the laboratory-based prototype. Table 5.8 represents the parameters of the simulation. The concept of theoretical analysis of the proposed topology is verified through simulation results.

Table 5.8. *Parameters of simulation*

Parameters	Values
dc Source	100V
Capacitors (C_1, C_2, C_3)	1600μF
Switching Frequency (f_{sw})	2000Hz
Fundamental Frequency (F)	50Hz
Modulation index (M)	0.95, 0.65, 0.35, 0.15
Load (R-L, R)	R=50Ω, L=120mH; R=100Ω

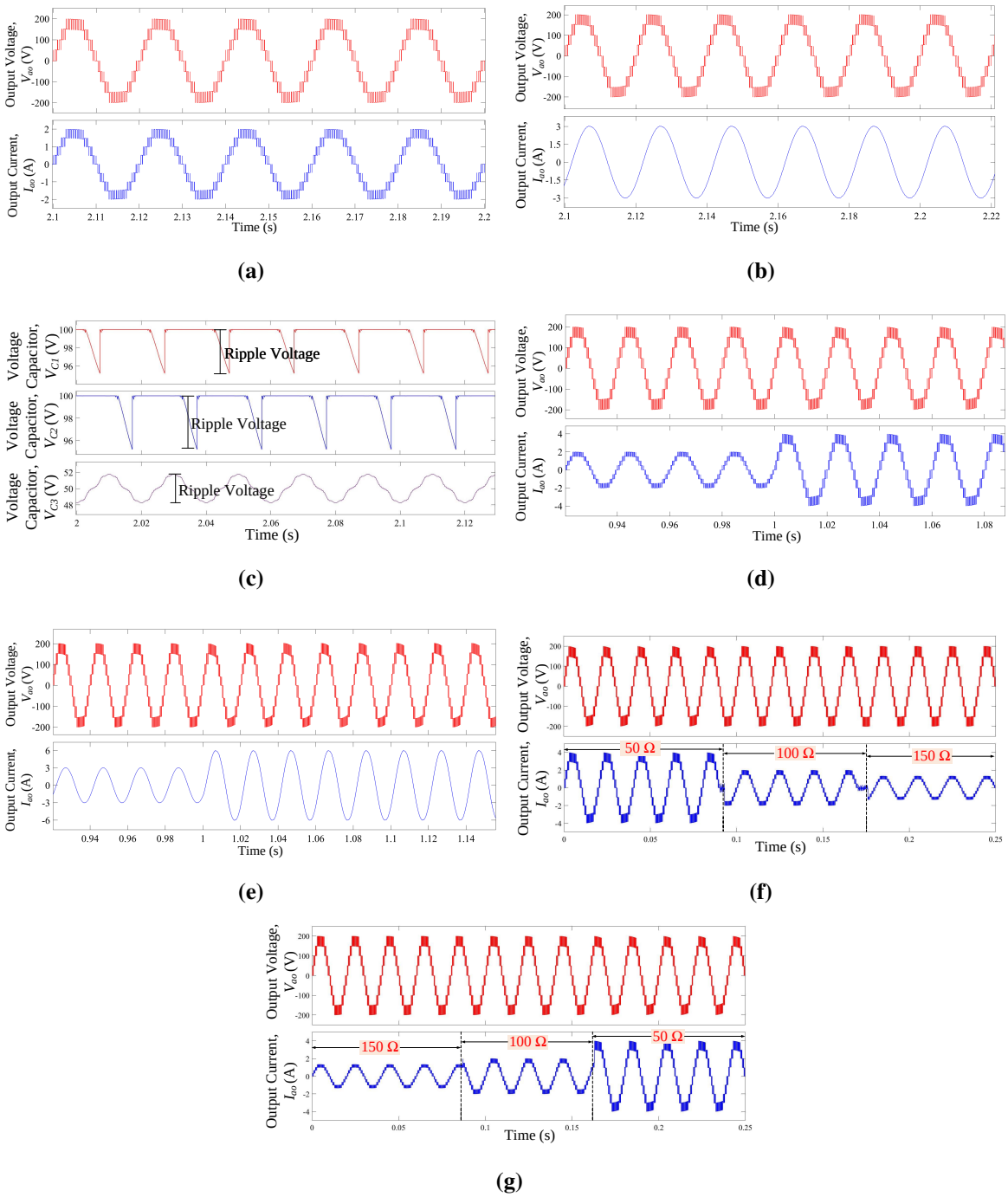


Fig. 5.12: *Simulation outcomes showing (a) waveform of voltage and current with R-load (100Ω) (b) voltage and current waveform with R-L load (50Ω,120mH) (b) ripple voltage of capacitor (d) transition in R-load from (100Ω) to (200Ω) (e) transition in R-L load from (50Ω, 120mH) to (25Ω, 60mH) (f) and (g) loading and unloading condition with change in R-load*

Fig. 5.12 depicts the simulation result to validate the proposed inverter with the modulation index M=0.95. Figs. 5.12a and 5.12a show the simulation results of voltage and current waveform with R-load (i.e.,100 Ω) and R-L load (i.e.,50Ω,120mH), respectively. Fig. 5.12c shows the ripple

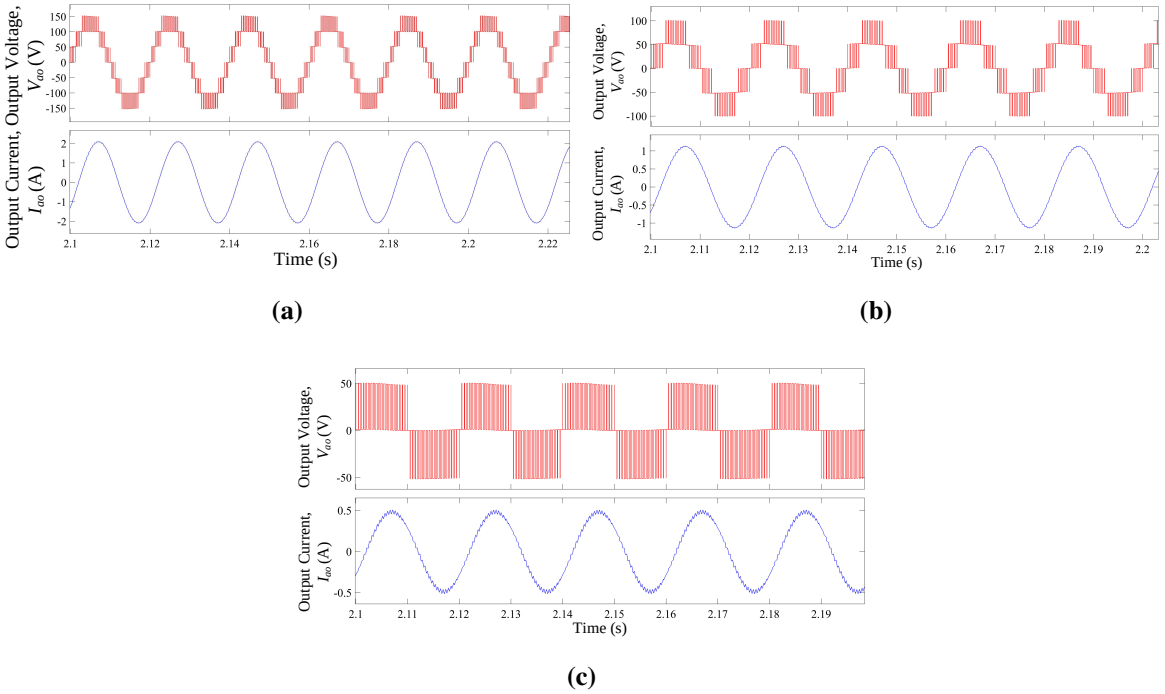


Fig. 5.13: *Simulation outcomes depicts the voltage and current waveform with R-L load (i.e.,50Ω,120mH) for (a) M=0.65 (b) M=0.35 (c) M= 0.15*

voltage of the capacitor. Figs. 5.12d and 5.12e represent transient in load. For t<1sec, the load comprises of R-load (i.e.,100Ω) and R-L load (i.e.,50Ω,120mH), respectively. After t=1sec, load changes to half of its earlier value. Consequently, the load current is changed significantly and gets doubled by decreasing the load to half of the earlier values. Figs. 5.12f and 5.12g depicts the loading and unloading condition with change in R-load. Fig. 5.13 depicts the simulation results of voltage and current waveform for different modulation indexes with R-L load (i.e.,50Ω,120mH).

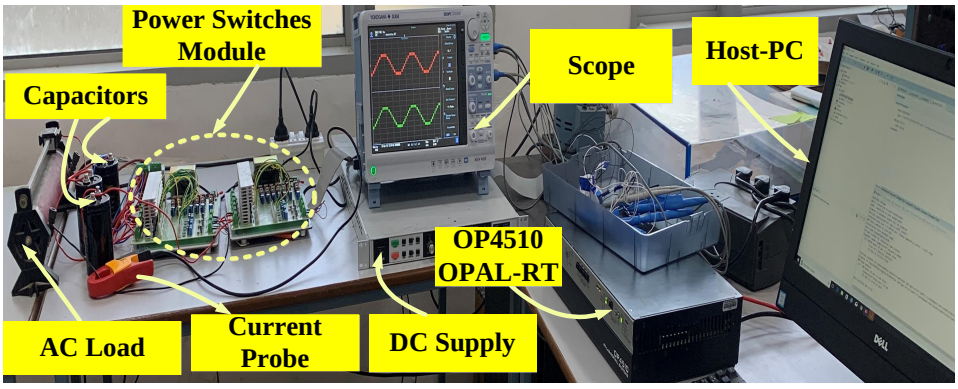
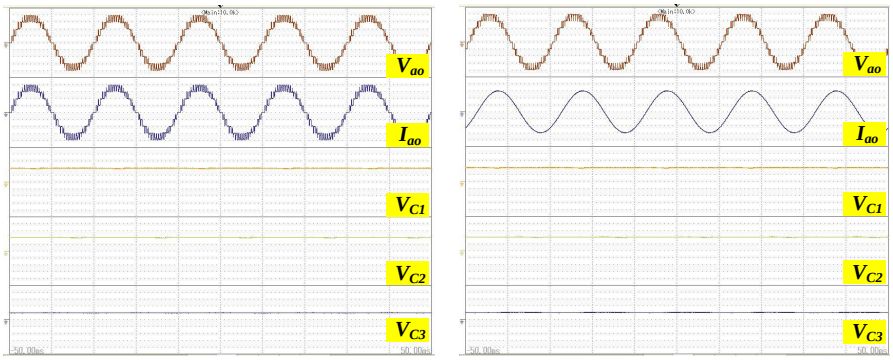


Fig. 5.14: *Hardware setup used for experimental validation*

Table 5.9. *Experimental Parameters*

Parameters	Values
dc Source	100V
Capacitors (C_1, C_2, C_3)	1600μF
Switching Frequency (f_{sw})	2000Hz
Fundamental Frequency(F)	50Hz
Modulation index (M)	0.95, 0.65, 0.35, 0.15
Load (R-L, R)	R=50Ω, L=120mH; R=100Ω
MOSFET	SiHG47N60
Gate driver IC	Si8274

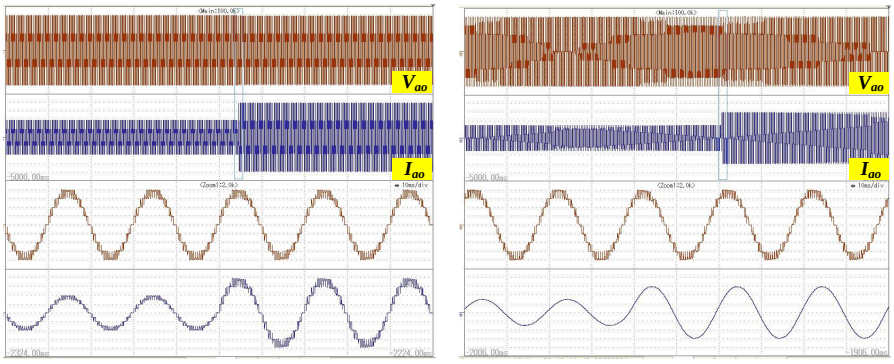
Experimental work on a laboratory prototype has been conducted to determine the viability of the proposed topology. The value of experimental components and parameters are shown in Table 5.9. The experimental setup is shown in Fig. 5.14.



(a) **(b)**

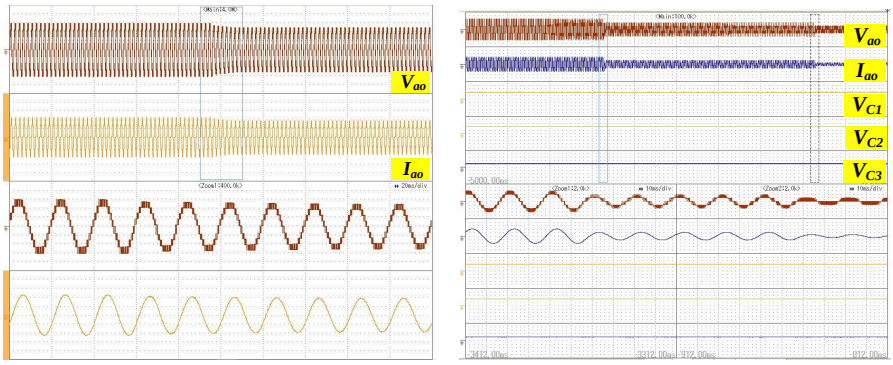
Fig. 5.15: *Experimental results showing (a) voltage, current and capacitors voltage with a resistive load (100Ω) (b) voltage, current and capacitor voltage with an inductive load (50Ω,120mH)*

To create the appropriate gate signals for power switches, the real-time controller (OPAL-RT OP4510) interfaces with the hardware using MATLAB/Simulink on the host computer. All experimental outcomes with M=0.95 are illustrated in Fig. 5.15, 5.16 and 5.17 to verify the



(a) **(b)**

Fig. 5.16: *Experimental results showing (a) transition in resistive load from (100Ω) to (50Ω) (b) transition in inductive load from (50Ω, 120mH) to (25Ω, 60mH)*



(a) **(b)**

Fig. 5.17: *Experimental results showing (a) change in input voltage from 150 V to 100V (b) change in modulation index (i.e., M=0.65 to 0.35 and M=0.35 to 0.15)*

simulation results of the proposed inverter. Figs. 5.15a and 5.15b show the experimental results of the voltage waveform, current waveform, and voltage of the capacitor with R-load (i.e.,100Ω) and R-L load (i.e.,50Ω,120mH), respectively. Figs. 5.16a and 5.16b represent transients in the load. Fig. 5.17a shows the change in input voltage from 150 V to 100V.

Fig. 5.17b depicts the change in modulation index (i.e., M=0.65 to 0.35 and M=0.35 to 0.15) in which at 0.65, seven-level are generated and for 0.35 and 0.15, five and three-level are generated, respectively. Also, it shows that all the capacitors are balanced at all modulation index values. The closed-loop performance characteristic is shown in Fig. 5.18. In this figure, the grid voltage is in phase with the grid current, resulting in a unity power factor. The amplitudes of the grid voltage and current are mentioned as 180V and 2.8A, respectively.

Fig. 5.19 shows the THD of output voltage with respect to modulation index. As the modulation index reduces, levels of the output voltage are also reduced, which therefore resulting into higher THD in output voltage.

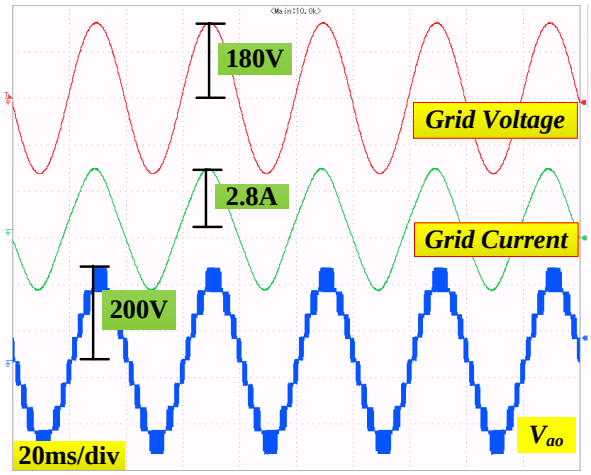


Fig. 5.18: *Experimental waveforms of grid connected system*

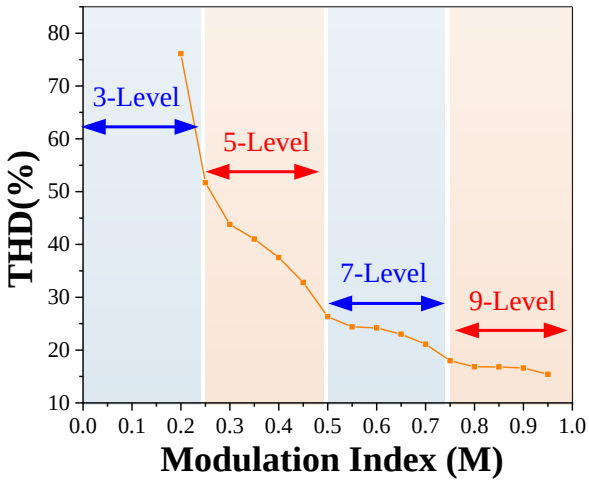


Fig. 5.19: *THD analysis of output voltage for different modulation index*

5.7 CHAPTER SUMMARY

This chapter presents a nine-level inverter suited for the grid-connected PV system. The experimental results validate the proposed power circuit. The following observations are made from this study:

- The proposed topology stands out with its simplicity, featuring a single input and only eight power switches that are controlled by four complementary gate drivers. This design minimizes component count and enhances system reliability.
- The self-balancing nature of the capacitors within the topology eliminates the need for additional sensors or complex control methods. This self-balancing capability simplifies the system and ensures voltage equilibrium without the need for external intervention.
- Simplified LSPWM control logic facilitates the generation of pulses through a complementary switching pair. This streamlined control approach reduces complexity and improves overall system efficiency.
- Notably, the proposed topology offers scalability, enabling the extension of voltage gain and the number of output voltage levels. This scalability feature provides versatility, allowing the topology to meet various voltage requirements for different applications.
- With total losses of 10.59W, the proposed topology achieves an impressive overall efficiency of 95.42% when delivering an output power of 220W. These figures highlight the topology's high efficiency and energy-saving capabilities.
- The improved harmonic profile of the output ac voltage enables the use of a reduced filter size, optimizing cost and system footprint. This advantage further enhances the topology's efficiency and cost-effectiveness.
- The reduced count of devices in the topology contributes to a low CF value, minimizing costs and improving system efficiency. This characteristic is beneficial in terms of both performance and economic considerations.
- Overall, the proposed topology ensures high reliability, providing a stable and dependable power conversion solution for various applications. Its simplified design, self-balancing capacitors, scalability, and impressive efficiency make it a promising choice in the field of power electronics.

Chapter–6

Design of 3-ϕ Switched Capacitor Based MLI for Grid Connected PV System

6.1 GENERAL

The proposed inverter is three phase extension of the topology proposed in chapter 4. The inverter operates with a single dc voltage source and utilizes two capacitors. Each phase of the inverter consists of nine power switches and two capacitors. By employing the LSPWM technique, the inverter generates seven voltage levels for each phase and 13 voltage levels for the line. Both simulation and experimental results validate the effectiveness of the proposed topology. In comparison to other three-phase SCMLIs, the presented circuitry demonstrates superior device count and capacitor voltage balancing capability.

6.2 CIRCUIT OF TOPOLOGY

The proposed three-phase SCMLI, which has a single dc voltage source, as shown in Fig. 6.2. Two dc-link capacitors, C_1 and C_2, are used to establish the neutral point, and they have equal voltage stress of $0.5V_{dc}$. There are two capacitors for each phase and nine power switches. In this topology, each power switch is made up of a transistor and an anti-parallel diode. Load terminals of the three phases are marked as a, b, and c. Mode of operations and switching states are already described in chapter 4 (Section 4.2.2).

The contents of this chapter are partly published in:

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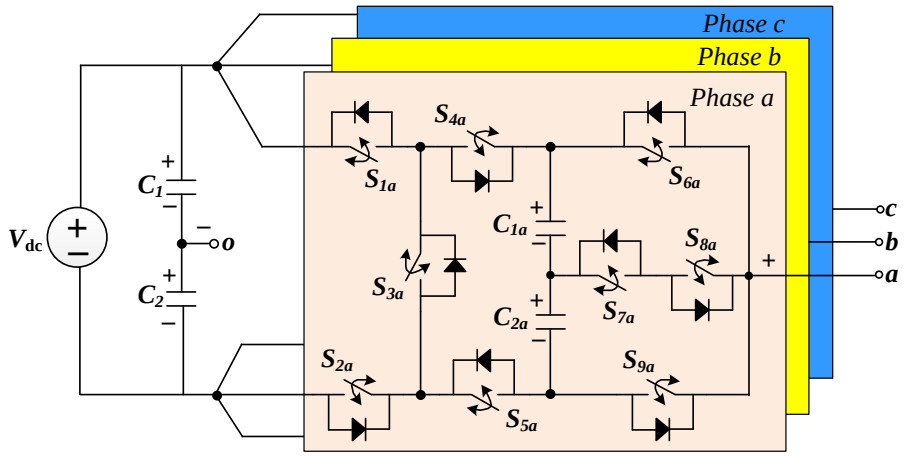


Fig. 6.1: *Three-phase proposed SCMLI topology*

6.3 MODULATION STRATEGY

To control the output voltage of the proposed SCMLI, several modulation algorithms, including multicarrier PWM and space vector modulation (SVM) can be employed. In this chapter, the LSPWM approach is employed to show the operation of the proposed SCMLI. Fig. 6.2 depicts the block diagram for modulating the proposed inverter. There are three reference signals V_{ref_a},

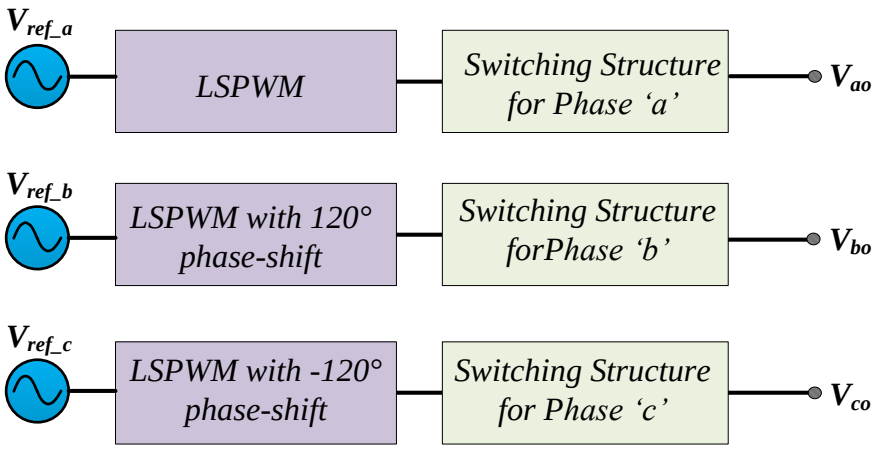


Fig. 6.2: *Block diagram to modulate the proposed inverter*

V_{ref_b}, and V_{ref_c} having phase angles of 0 °, 120°, and -120° respectively. Appropriate switching is provided to generate a gate signal for each leg. Switching for phase a is shown in Fig. 6.3 in which the absolute value of reference signal V_{ref_a} having phase angle of 0° is compared with three carriers V_{cr1}, V_{cr2}, and V_{cr3}, and output is fed to AND gates which create different switching

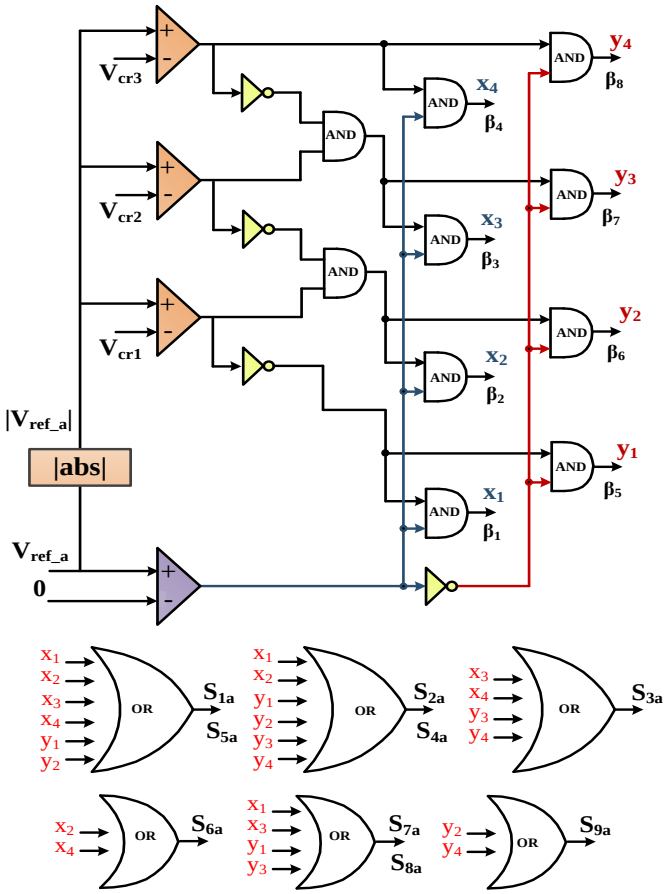


Fig. 6.3: *Logic gates-based implementation of the modulation scheme for phase 'a'*

states and further firing pulses for each power switch of phase a are obtained by feeding it into OR gates. The switching structures for phases b and c are obtained in a similar manner, using reference signals V_{ref_b} with a phase angle of 120° and V_{ref_c} with a phase angle of -120°. The modulation index (M) is denoted as:

$$M = \frac{A_{ref}}{3A_{cr}} \tag{6.1}$$

Where A_{ref} and A_{cr} are peak value of the carrier and reference waveform respectively.

6.4 CONTROL OF 3-ϕ GRID CONNECTED INVERTER

The control of three-phase grid connected inverter is crucial to ensure efficient and reliable operation. One widely used control technique for three-phase grid-connected inverters is based on the dq axis theory [103]. The dq axis theory is a mathematical transformation technique that simplifies the analysis and control of three-phase systems. It represents the three-phase variables

(voltages or currents) in a two-coordinate reference frame, consisting of a rotating d-axis and a q-axis. The d-axis is aligned with the positive sequence component of the system, while the q-axis is 90° ahead of the d-axis.

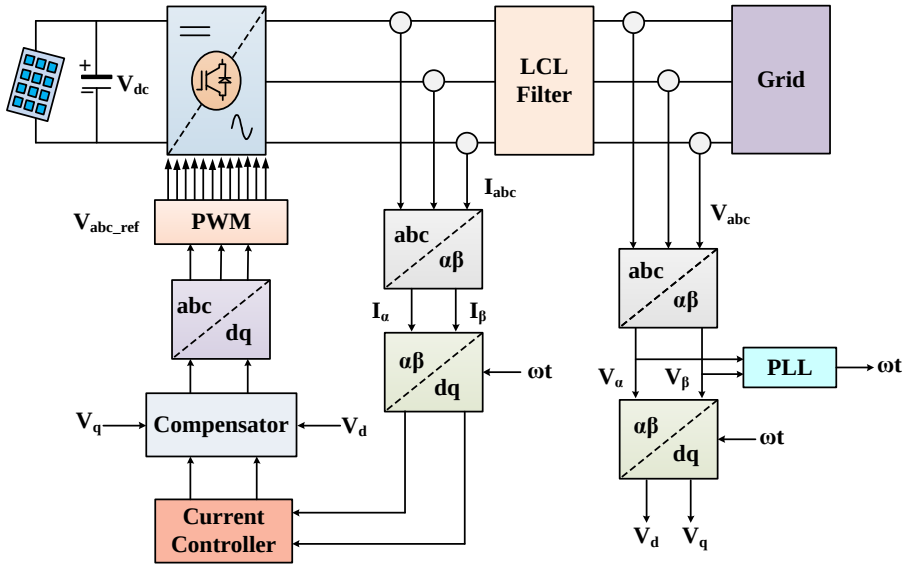


Fig. 6.4: *Complete block diagram of 3-ϕ inverter*

To control a three-phase grid-connected inverter using the dq axis theory, the following steps are typically followed:

- **Synchronization:** The grid-connected inverter needs to synchronize its output with the grid voltage. This involves extracting the grid voltage's frequency and phase angle using PLL techniques.
- **Clarke Transformation:** The 3-ϕ grid voltage or current signals are transformed into the stationary reference frame ($\alpha\beta$ frame) using the Clarke transformation. This transformation converts the three-phase signals into two components: the α-axis component, which represents the positive sequence component, and the β-axis component, which represents the negative sequence component.
- **Park Transformation:** The $\alpha\beta$ components obtained from the Clarke transformation are then transformed into the rotating reference frame (dq frame) using the Park transformation. This transformation rotates the $\alpha\beta$ components to align them with the d-axis and q-axis, simplifying the subsequent control calculations.

- **Current Control**: In the dq frame, the control objectives are typically achieved by controlling the d-axis and q-axis currents. The d-axis current is responsible for regulating the active power exchange between the inverter and the grid, while the q-axis current controls the reactive power exchange.

- **Current Control Loop:** A control loop is implemented to regulate the d-axis and q-axis currents. This loop compares the actual currents with the desired reference values and adjusts the inverter's switching signals accordingly. Various control techniques, such as Proportional-Integral (PI) controllers or more advanced control algorithms, can be employed for this purpose.

- **Inverter Modulation:** Once the d-axis and q-axis currents are controlled, the switching signals for the power switches are generated. These switching signals determine the PWM strategy for the inverter, enabling the generation of the desired ac voltage waveform.

6.5 COMPARISON WITH OTHER SCMLIS TOPOLOGIES

The voltage gain of traditional MLIs is unitary, however, the voltage gain of SCMLI topologies is larger than unitary. Accordingly, the proposed topology must be compared to alternative switched capacitor-based topologies. This study is based on the number of levels (N_L) number of input dc sources (N_{IS}), the number of switches (N_S), the number of gate drivers (N_{GD}), the number of diodes (N_D), the number of capacitors (N_C) and Boosting Factor (BF).

Table 6.1 shows that the topology [30] has high boosting factors but needs a large number of power switches for a three-phase configuration resulting in a higher cost function. Inverter topology [92], [104] is realized with minimum switches but required more numbers of diodes which further increases its cost. In topology [44] although it attains higher gain but required a huge number of power switches and diodes. In [70] only nine levels are obtained by using more switches. Therefore, the proposed topology is found superior in terms of the number of switches, overall cost, having a single dc source, and fewer switching capacitors.

Table 6.1. *Comparison with other 3-ϕ topologies*

Topologies	N_L	N_S	N_D	N_C	N_{IS}	PIV	BF
[30]	13	30	0	6	1	3	6
[44]	17	36	0	6	1	4	8
[92]	17	24	9	9	1	4	8
[70]	9	36	0	12	1	4	8
[82]	13	30	0	8	1	1	3
[104]	7	12	6	8	1	1.5	3
Proposed	13	27	0	8	1	1	3

6.6 EXPERIMENTAL VERIFICATION

To validate the practicability of the proposed three-phase SCMLI, the simulation model was built in MATLAB/ SIMULINK. The value of simulation components and parameters are shown in Table 6.2. Figs. 6.5a to 6.5c presents the three-phase output voltage and current waveforms with a resistive load (i.e.,500Ω) and M=0.95. In Fig. 6.5a three-phase line voltage has thirteen levels in steps of 50V and the peak value ≈300V is shown. Fig. 6.5b depicts three-phase output phase voltage has seven levels in steps of 50V and peak value ≈150V. In Fig. 6.5c, the three-phase

Table 6.2. *Parameters of simulation*

Parameters	Values
dc Source	100V
Capacitors (C_1, C_2, C_{1a}, C_{2a}, C_{1b}, C_{2b} , C_{1c} and C_{2c})	$1600\mu F$
Switching Frequency (f_{sw})	2000Hz
Fundamental Frequency (f)	50Hz
Resistive Load	500Ω
Inductive Load	50Ω ,120mH

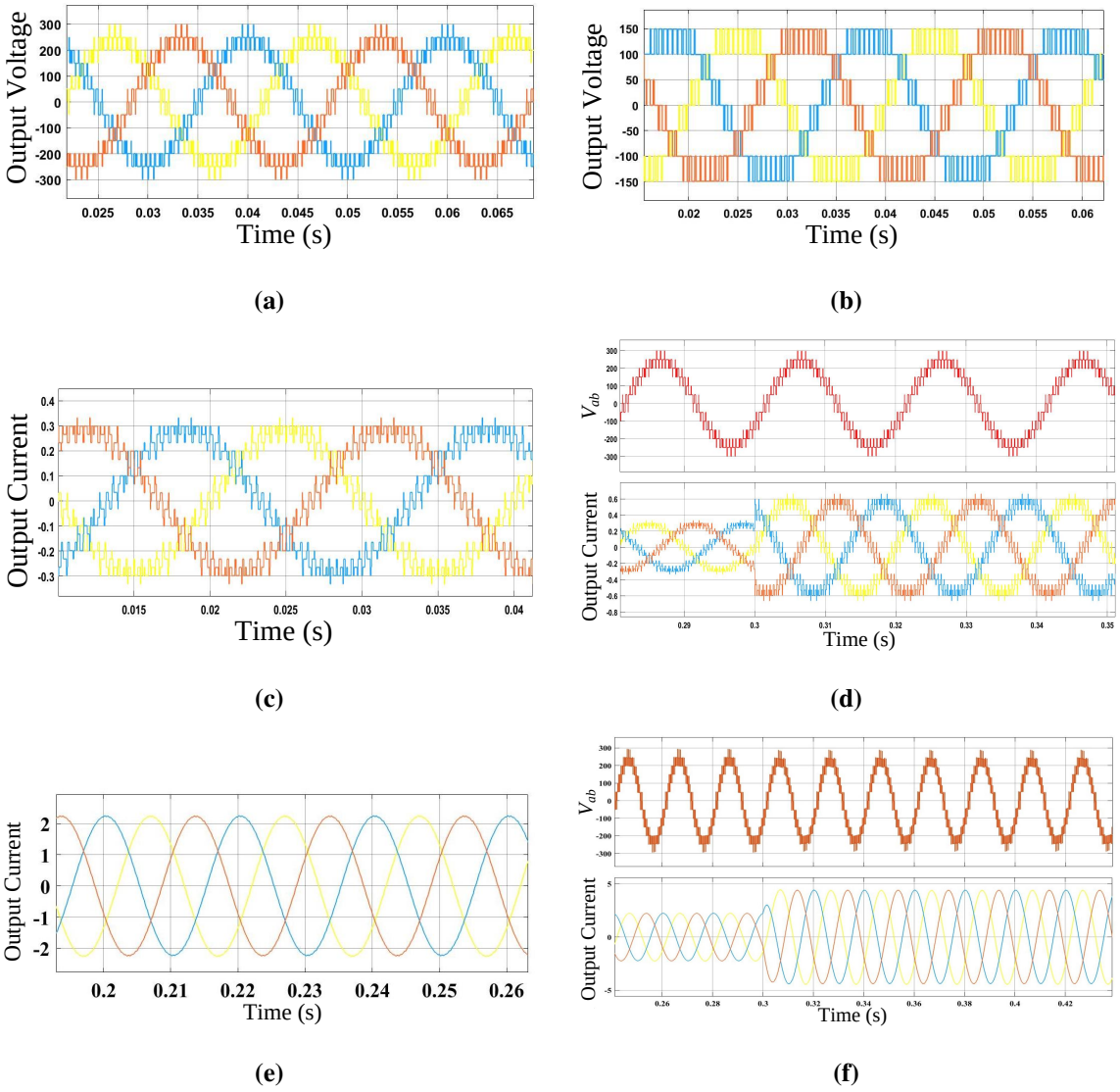
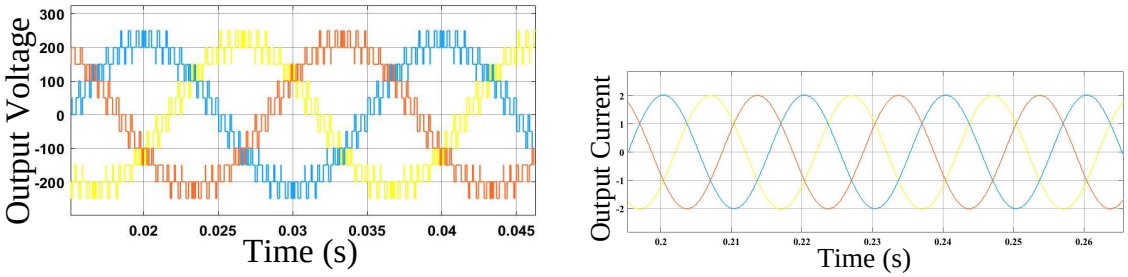


Fig. 6.5: *For M=0.95 simulation results showing (a), (b), (c) three-phase line voltage, phase voltage and load current with resistive load of 500Ω (d) transition in resistive load from (500Ω) to (250Ω) (e) three-phase output current with inductive load of (50Ω, 120mH) (f) transition in inductive load from (50Ω, 120mH) to (25Ω, 60mH)*

load current has an amplitude of 0.3A is shown. A resistive load transient is shown in Fig. 6.5d. For t<0.3sec, the load comprises a resistive load (i.e.,500Ω). After t=0.3sec load changes to half of its earlier value. Consequently, the load current is changed significantly and gets double by decreasing load to half of the earlier values. Three-phase output current with an inductive load (i.e.,50Ω,120mH) has an amplitude of 2.25A with M=0.95 is shown in Fig. 6.5e. Fig. 6.5f represents a transient in inductive load. For t<0.3sec, the load comprises an inductive load (i.e.,50Ω,120mH) After t=0.3sec load changes to half of its earlier value. By reducing the load to



(a) **(b)**

Fig. 6.6: *For M=0.85 simulation results showing (a) three-phase line voltage with resistive load 500Ω (b) Three-phase output current with inductive load of (50Ω, 120mH)*

half its previous levels, the load current is drastically altered and doubles. Fig. 6.6a depicts the three-phase line voltage has eleven levels in steps of 50V with resistive load 500Ω and the peak value ≈250V with M=0.85. Three-phase output current with load comprising resistance of 50Ω and inductance of 120mH has an amplitude of 2A with M=0.85 is shown in Fig. 6.5b.

The proposed SCMLI is further developed into a prototype in order to validate the simulation and analytical results. The MAGNA-POWER programmable DC power supply (SL1000-6.0/415+HS) is used to provide the input dc supply of 100V. Table 6.3 includes all additional experimental components and parameters. In Fig. 6.7, the experimental image is displayed. The real-time controller (OPAL-RT OP4510) connects with the hardware using MATLAB/Simulink on the host computer to generate the proper gate signals for power switches. These signals are produced with an f_{sw} frequency of 2 kHz and a modulation index of 0.95.

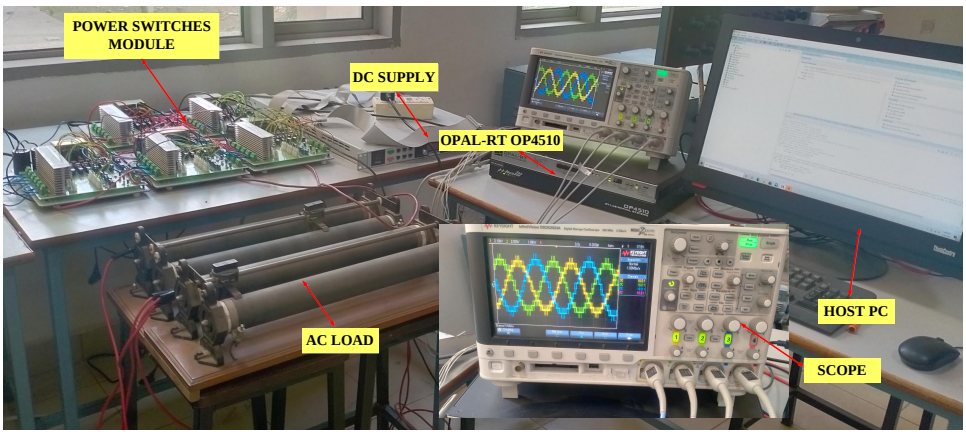


Fig. 6.7: *Experimental setup*

Table 6.3. *Experimental parameters and components specifications*

Parameters	Values
dc Source	100V
Switching Frequency (f_{sw})	2000Hz
Fundamental Frequency (f)	50Hz
Resistive Load	500Ω
Inductive Load	50Ω ,120mH
MOSFET	SiHG47N60
Isolated Gate driver IC	Si82071AB
Capacitors (C_1, C_2, C_{1a}, C_{2a}, C_{1b}, C_{2b} , C_{1c} and C_{2c})	$1600\mu F$
Controller	Opal-RT OP4510
Voltage Senor	LEMLV25-P
Current Senor	HE025T01

A resistive load (i.e.,500Ω) is taken into account in Fig. 6.8. Figs. 6.8a and 6.8b show the waveform of three-phase line and phase voltage with an amplitude of 300V and 150V respectively. The amplitude of the three-phase output current is 0.3A as shown in Fig. 6.8c. Figs. 6.8d and 6.8e shows that capacitors C_1, C_2, C_{1a}, C_{2a}, C_{1b}, C_{2b} , C_{1c} and C_{2c} get approximately charged to 50V, and they are within the range of 10% voltage ripples. When the ac load is reduced by a factor of 2 (i.e., 500Ω to 250Ω), the load current increase by a factor of 2, and load voltages remain the same are illustrated in Fig. 6.8f. When the load current fluctuates dynamically, it implies that the load voltages are extremely stable.

In Fig. 6.9, an inductive load (i.e.,50Ω,120mH) is considered. Fig. 6.9a shows the waveform of three-phase line voltages and currents with amplitude 300V and 0.29A respectively. Sudden change in inductive load is represented in Fig. 6.9b. The inductive load has a resistance of 50Ω and an inductance of 120mH till time t=t sec. After this time, an inductive load changes to half

its initial value. By reducing the load to half of its previous levels, the load current is drastically altered and doubles.

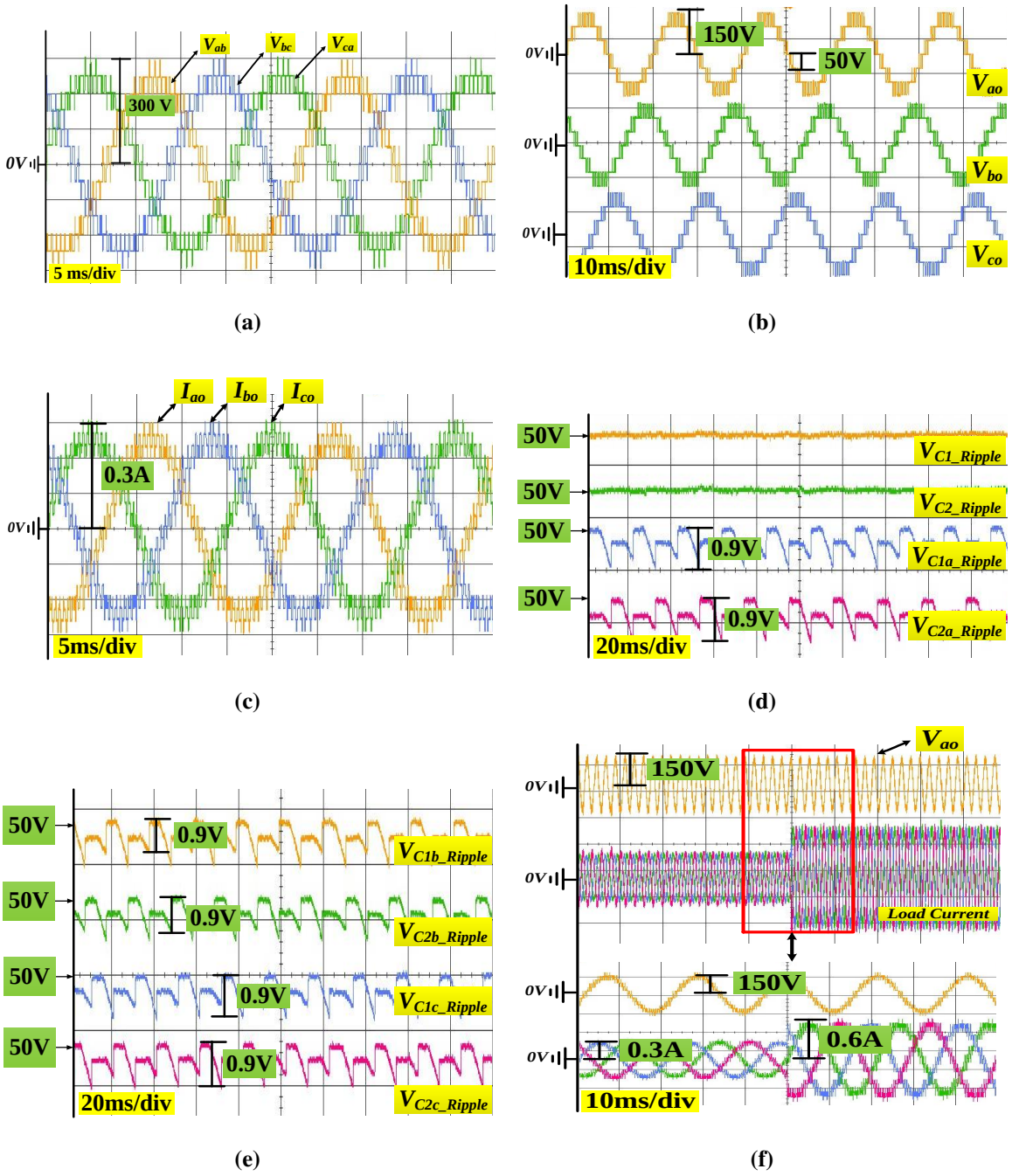


Fig. 6.8: *Experimental results with a resistive load of 500Ω showing (a), (b) three-phase line and phase voltages (c) three-phase output currents (d), (e) Capacitors ripple voltages (f) transition in resistive load from (500Ω) to (250Ω)*

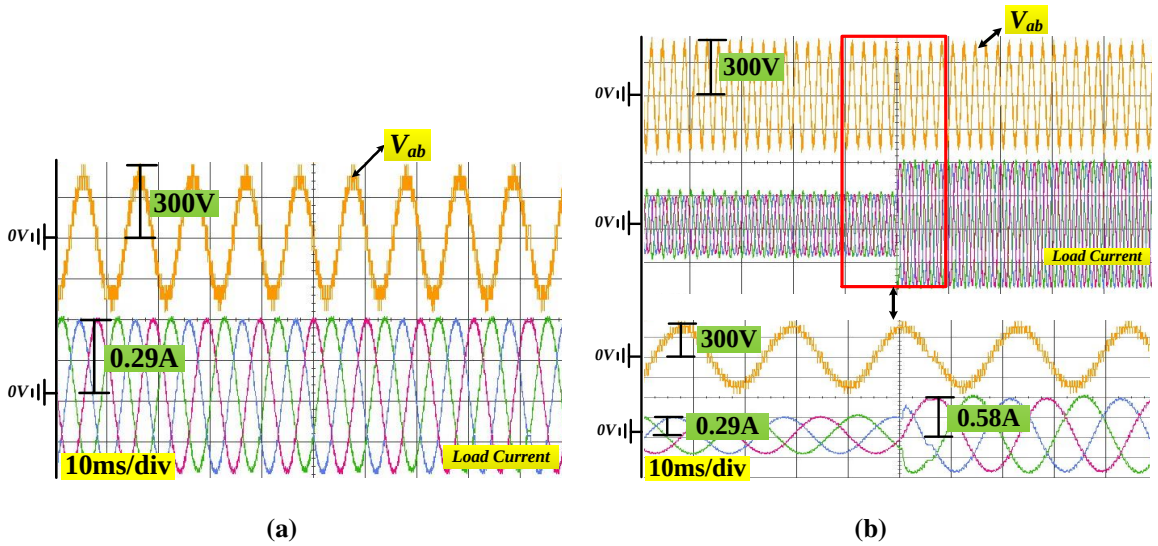


Fig. 6.9: *Experimental results with inductive load of (50Ω, 120mH) Showing (a) three-phase line voltages and currents (b) transition in inductive load from (50Ω, 120mH) to (25Ω, 60mH)*

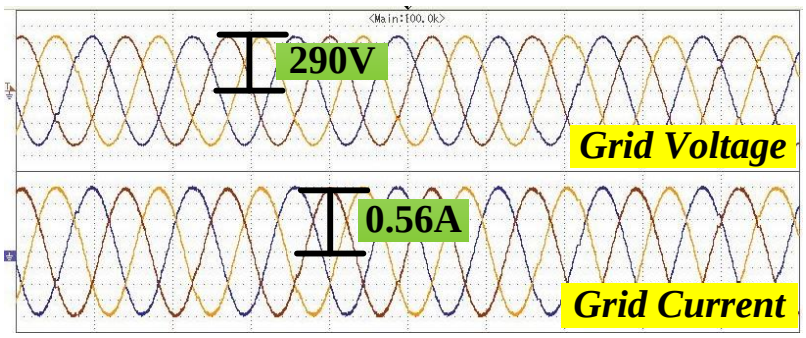


Fig. 6.10: *Experimental waveforms of three-phase grid connected system*

The closed-loop performance of three-phase inverter is shown in Fig. 6.10. In this figure, the grid voltage is in phase with the grid current, resulting in a unity power factor. The amplitudes of the grid voltage and current are mentioned as 290V and 0.56A, respectively

6.7 CHAPTER SUMMARY

This chapter presents a three-phase MLI suited for the grid-connected PV system. The experimental results validate the proposed power circuit. The following observations are made from this study:

- All controlled switches are designed to withstand a PIV up to the limit of the input dc voltage, ensuring reliable operation. The inverter showcases impressive boosting capability, achieving the highest voltage level at three times the input dc voltage.
- To enhance voltage quality, the inverter employs LSPWM along with phase shifting of the carrier signals, effectively reducing capacitor voltage ripples and enhancing overall output voltage performance.
- Notably, this inverter operates with a single dc source and utilizes self-balancing capacitors, which eliminates the need for additional balancing circuits or control methods. These features contribute to the inverter's simplicity and cost-effectiveness.
- The theoretical analysis of the proposed inverter is presented and further validated through experimental testing using a three-phase prototype. This validation reinforces the feasibility and practicality of the inverter design, demonstrating its potential for real-world applications.

Chapter–7

Conclusions and Scope for Future Work

7.1 MAIN CONCLUSIONS

In this work, it is established that switched capacitors based multilevel topologies can effectively function for grid-connected PV systems with following main advantages: self-balancing of capacitors, inherent voltage boosting capability in both single-phase and three-phase versions, low voltage stress on power switches as compared to the operating voltage, low dv/dt stress, better harmonic profile of the output voltage waveform, and so on. Following are some specific concluding remarks of significant importance:

- A novel five-level inverter is proposed which reduces CF using six switches, one diode, and a switched capacitor. It boosts voltage twice the input voltage, creating a high-resolution waveform with self-balancing of capacitors voltage. High PIV on some of the switches, however, is an important limitation of this topology.

- To address the limitations of the aforementioned five-level inverter, a new seven-level inverter is proposed. It can boost the input voltage by a factor of 1.5, without high voltage stress on switches, and the capacitors are self-balanced. However, non-complimentary nature of few of the power switches increase the number of gate drivers. As a further consequence, the CF increases too.

- To achieve a high-resolution waveform with less CF, a self-balancing nine-level inverter is presented, which requires only eight switches, three capacitors, and two diodes. The structure is validated for single-phase application.

- A three-phase version of seven-level inverter is also presented. It uses a simple modulation technique to generate seven levels in the phase voltage and thirteen levels in the line voltage. It also has a lower device count and lower PIV on switches.

7.2 SCOPE FOR FUTURE WORK

While this work has carried forward the research on SCMLIs mainly for photovoltaic application, there is an ample scope for further investigations. Following are a few suggestions for future research:

- The impact of employing the newly emerging wide-band-gap devices to SCMLIs can be studied, especially in the context of achieving higher switching frequencies and better power density.
- Another interesting approach to improve the efficiency and performance of SCMLIs would be the application of soft switching techniques which may greatly help in reducing the current stress of the power switches.
- Possibility of fault-tolerant operation is an important advantage of multilevel topologies. Such possibilities can be explored in SCMLIs with an application oriented approach for fault-detection and reconfiguration.

List of Publications

JOURNAL PUBLICATIONS (SCI)

1. Ritika Agarwal, Krishna Kumar Gupta, Shakti Singh, "A novel self-boosting 5-level inverter for grid-connected photovoltaic system," ***Electric Power Systems Research***, vol. 211, pp. 108201, 2022. (Impact factor: 3.818) **[Chapter 3]**
   doi: https://doi.org/10.1016/j.epsr.2022.108201

2. Ritika Agarwal, Krishna Kumar Gupta, Shakti Singh, "Switched capacitors based single-phase seven-level photovoltaic inverter with self-voltage balancing," ***Electrical Engineering***, vol. 104, pp. 3107-3117, 2022. (Impact factor: 1.630) **[Chapter 4]**
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3. Ritika Agarwal, Krishna Kumar Gupta, Shakti Singh, "A double boost 9-level switched capacitor-based multilevel inverter for photovoltaic applications," ***International Journal of Circuit Theory and Applications***, 51(7): 3288-3315, 2023. (Impact factor: 2.378) **[Chapter 5]**
   doi: https://doi.org/10.1002/cta.3596.

COMMUNICATED ARTICLE

1. Ritika Agarwal, Krishna Kumar Gupta, Shakti Singh, "A Switched-Capacitor Based Three-Phase Multilevel Inverter with Single DC Source for PV Application," communicated in ***Electrical Engineering,*** . (Impact factor: 1.630) **[Chapter 6]**

CONFERENCE PUBLICATIONS

1. Ritika Agarwal, Anekant Jain, Krishna Kumar Gupta, Shakti Singh, "Level Enhancement in Switched Capacitors based Multilevel Inverter using Level Doubling Network," *IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society, Brussels, Belgium*, 2022, pp. 1-6.
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