Design of ROIC with Temperature Compensation Circuitry for ISFET based pH Meter

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in
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CERTIFICATE

This is to certify that thesis report entitled "**Design of ROIC with Temperature Compensation Circuitry for ISFET based pH Meter**" is being submitted by **Megha Agrawal** in partial fulfillment of the degree of **Master of Technology in VLSI Design & CAD** of Thapar University, Patiala embodies work under my supervision at **Central Electronics Engineering Research Institute, Pilani** (Rajasthan) during the training period from January 2010 to June 2010.

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Declaration

I hereby certify that the work which is being presented in the thesis entitled, "**Design of ROIC with Temperature Compensation Circuitry for ISFET Based pH Meter**" in partial fulfillment of the requirement for the award of degree of M. Tech. (VLSI Design and CAD) at Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of ***Mr. Anil Kumar Saini***, Scientist, IC Design Group, CEERI, Pilani and ***Ms. Alpana Agarwal,*** Assistant Professor, ECED, Thapar University, Patiala.

The matter presented in this thesis has not been submitted in any other University/Institute for the award of any degree.

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Megha Agrawal

ABSTRACT

This work presents the design of readout circuitry of ISFET (Ion Sensitive Field Effect Transistor) based pH meter with temperature compensation using 0.18 μm UMC technology. The readout circuit is used for reading out the concentration of H+ ions, which denotes the pH value of solution. Any change in pH directly affects the threshold voltage of ISFET. To measure this change in pH, a gate CIMP (complementary ISFET/MOSFET pair) technique based sensing readout circuitry is designed, which is applicable in CMOS based Microsystems and also eliminates body bias effect. The performance of the pH meter is affected by temperature variation. The ISFET is thermally instable due to semiconductor properties and pH dependency on temperature, which in turn affects the pH reading of the solution at a temperature other than room temperature. In this work, V_T extractor based temperature compensation circuitry is designed for compensating the temperature variation effect of ISFET. Since the temperature coefficient of NMOS V_T extractor circuit is negative, it is used to cancel out the temperature variation of ISFET. A new architecture of PMOS V_T extractor is proposed, which has been used to implement a V_T extractors based voltage reference circuit. This voltage reference circuit provides temperature independent biasing to both readout circuit and temperature compensation circuitry for reducing effect of temperature on ISFET characteristics.

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Chapter 1

Introduction

Background

The desirable property of a micro system for biomedical applications is to realize chemically sensitive sensor such as pH sensor with CMOS technologies that have fast response, low cost, and higher accuracy. pH is a term defined for measurement of concentration of hydrogen ions in a solution. All human beings and animals depend on internal mechanisms to maintain the pH level of their blood. The blood flowing through our veins must have a pH between 7.35 and 7.45. Increasing value of pH up to 7.8 or decreasing up to 6.8 results in death. The electrophysiological activity of neurons in the brain can be adversely affected by a slight deviation from standard pH values. So it is essential to determine and analyze the true pH values for a variety of processes particularly in biological system in which a slight variation of pH values can prove fatal. Exceeding this range by as little as one-tenth of a pH unit could prove fatal. ISFET semiconductor technology enables the design of true solid state pH sensor. ISFETs use glass-free pH electrodes which provide reliable pH measurement in those areas where the use of glass may impose a danger. The ISFET was first introduced by P. Bergveld in 1970. It is similar to MOSFET except that an ion sensitive membrane is used to measure the ion concentration of solution. The ISFET based pH sensor is compatible with CMOS technology and have fast response, low cost, and higher accuracy [1, 2].

Motivation

ISFET is an ion sensitive sensor that is used for a wide range of biomedical applications such as medical diagnostics, monitoring clinical or environmental samples, fermentation

and bioprocess control and for testing pharmaceutical or food products. In order to extract the relevant signal from ISFET, it is necessary for the ISFET to be accompanied by an analog readout interface. The basic building blocks of ISFET based pH meter are ISFET sensing readout circuit, temperature compensation circuitry and Analog to digital converter. As ISFET is liable in critical applications like health care monitoring, its readout circuit becomes significantly important. Since the pH value varies with temperature so ISFET has large thermal inaccuracy. Although this limitation in application such as soil, wine, meat and environmental monitoring that do not require high precision are not critical, they cannot be ignored in biomedical application. Hence, to promote ISFET based applications become more valuable and important in biomedical related research, it is necessary to compensate these effects. In this thesis work, **a Readout Circuitry with temperature compensation for ISFET based pH meter** has been designed. The readout circuit is used for reading out the concentration of H+ ions which denotes the pH value of solution. Any change in pH directly affects the threshold voltage of ISFET. To measure this change in pH, ISFET is configured in such a way so that change in threshold voltage can be directly detected. For this purpose a sensing readout has been designed using Gate CIMP technique. ISFETs are thermally unstable due to properties of the semiconductor structure and the sensing films which lead to the inaccuracy in pH measurement. The pH value of a solution also depends upon the temperature. The pH values change by a significant amount on deviation of temperature of the solution from standard temperature 27°C. It is necessary for ISFET to be used under thermostatic condition to ensure accuracy. This is not convenient for many applications. So in order to obtain reliable output data, the interface circuitry for ISFET based pH sensor with appropriate temperature compensation is required. The temperature coefficient (TC) for output of sensing readout circuit is positive. In order to compensate this TC an input free V_T extractor is used. This V_T extractor circuit directly extracts the threshold voltage of MOSFET on its output. As the temperature coefficient of V_T extractor circuit is also negative so an inverting amplifier with scaling circuitry is used to invert this temperature coefficient. Now the outputs of both inverting amplifier and ISFET readout circuit are feed to a summing amplifier to mutually offset their temperature coefficient. So that temperature independent output voltage can be obtained.

To reduce the effect of temperature on ISFET characteristics, it is also desired to bias ISFET at isothermal point. For this purpose a voltage reference circuit is used. The classical voltage bandgap reference circuit (BGR) is not suited for a low voltage CMOS technology. A new architecture for a precision CMOS voltage reference has been overcomes the limitation of BGR. This voltage reference does not use any diodes or BJTs.

Thesis Organization

Chapter 1. (Introduction): This chapter contains the basic idea about what ISFET based pH meter and its advantages. This chapter also contains the chapter wise description of report structure.

Chapter 2. (Literature Survey): This chapter describes the ISFET structure, operation and discusses about the various ways for implementation of main building blocks of ISFET based pH meter.

Chapter 3. (Circuit Implementation): This chapter discusses the various calculation steps taken to design the key components like op-Amp, V_T extractors followed by designing of voltage reference, readout circuitry and temperature compensation circuitry. At last the layout of all blocks has been displayed.

Chapter 4. (Simulation Results): This chapter contains the pre layout and post layout simulation results of key components and major blocks.

Chapter 5. (Conclusion and Future prospects): All the work done has been concluded in this chapter in brief. The design has been analyzed for further Improvements which are possible and the improvements which have been brought about by this design.

Chapter 2

Literature Survey

2.1 Ion-Sensitive Field Effect Transistor (ISFET)

The ion sensitive transistors are solid-state miniature sensors based on silicon technology. From the chemical point of view, these sensors can be an attractive alternative in the market to the classical potentio-metric sensors because of their relatively good analytical performance, low price, and small size. An ISFET was introduced by P. Bergveld in 1970 and the first reported ISFET device was using a SiO_2 as a gate insulator layer.

2.1.1 ISFET Structure

The ISFET combines the chemical-sensitive properties of glass membrane with the impedance converting characteristics of the MOSFET. This combination forms the essential chemical transducer element of the conventional pH meter. The ISFET selectivity senses the specific ion in an electrolyte. It is a trans-impedance element, which has the features of low output impedance of MOSFET and the operation of ion sensitive membrane [3].

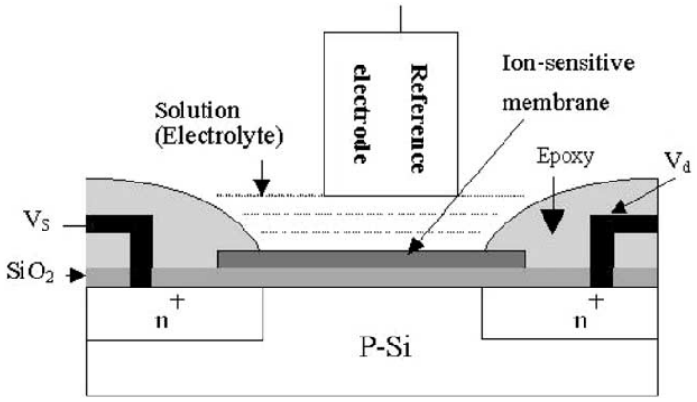


Figure 2.1: Cross section of ISFET device [3].

The ISFET (shown in figure2.1) is similar to MOSFET device where the gate metal electrode of the MOSFET is replaced by an electrolyte, which is in contact with the reference electrode, i.e., the silicon gate oxide is directly exposed to aqueous electrolyte solution. An external reference electrode is required for a stable operation of an ISFET. The ISFET sensitivity depends mainly on the choice of the gate insulator material. The most commonly used materials are silicon and metal oxides or nitrides. Among these materials, especially high sensitivity to the hydrogen ion concentration exhibits the aluminum oxide. ISFET can be used for the detection of various species in the surrounding electrolyte, other than the hydrogen ions by coating gate with a special membrane. A physical layout of one ISFET is shown in Fig 2.2. The L must be at least 20 mm, to insure a good contact with the liquid at the gate, and W must be at least 400 mm for an acceptable transistor.

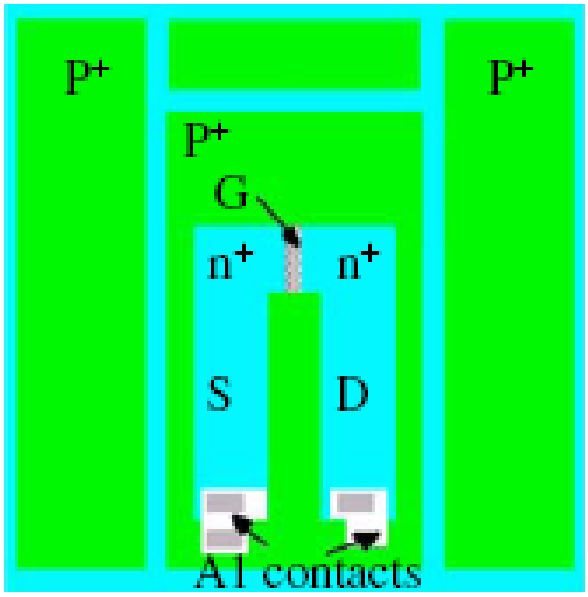


Figure 2.2: Layout of ISFET device [3].

Since the ISFET internal drain and source resistances seriously influence the ISFET's electrical behavior, they should be taken into account in the ISFET model. Moreover, a parasitic capacitances drain-substrate, source-substrate of several tens of pH has to be added to the ISFET simulation model.

2.1.2 Operation of ISFET

In ISFETs the classic gate of an ordinary FET is replaced by a more complex structure consisting of a reference electrode, an analyzed solution and a gate dielectric. The hydrogen ion concentration in the solution influences the gate potential, which in turn modifies the transistor threshold voltage. In this way, the ion concentration exercises electrostatic control on the drain-source current. Such structure is capable of sensing the concentration of the hydrogen ions and is used as a pH sensor. The basic ISFET is an exposed-gate-oxide FET and functions as a pH sensor. In figure 2.3, U_D denotes the drain-source voltage. The gate insulator of the ISFET senses the specific ion concentration generating an interface potential on the gate. Thus, the ISFET channel would be affected by the potential at the gate, which would modulate the current flow across the source and drain when the device is turned on. The concentration of the H+ ions could be thus measured by calibrating the amount of current flow. In other words, the relationship between the current and H+ ion concentration will allow that the pH value is depends to the measured current value. However, at a defined source-drain potential (U_D), changes in the gate potential can be compensated by a modulation of *U*. This adjustment can be carried out in a way that the changes in gate potential applied to the reference electrode exactly compensate for the changes in the gate oxide potential. The potential developed across the Al_2O_3 insulator layer directly depends on the number of H+ ions in contact with it [4, 5].

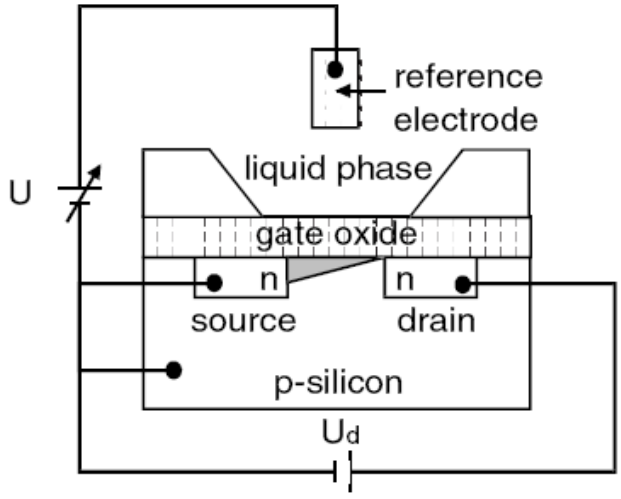


Figure 2.3: ISFET operation [5].

2.2 ISFET Modeling

The ISFET is a MOSFET-based device that uses an exposed gate insulator to measure ion concentration or local changes of charge densities in electrolyte solutions (figure 2.4). The response of the ISFET to pH can be explained by considering H+ -specific binding sites at the insulator surface. This theory, together with the Gouy–Chapman–Stern model of the potential profile in the electrolyte, and with the MOSFET physics, gives a complete description of the ISFET. To achieve a general model of ISFET, An ISFET is considered as two fully uncoupled stages: an electronic stage i.e., the MOSFET which is the starting structure of the ISFET and an Electro-chemical stage i.e., the electrolyte–insulator interface.

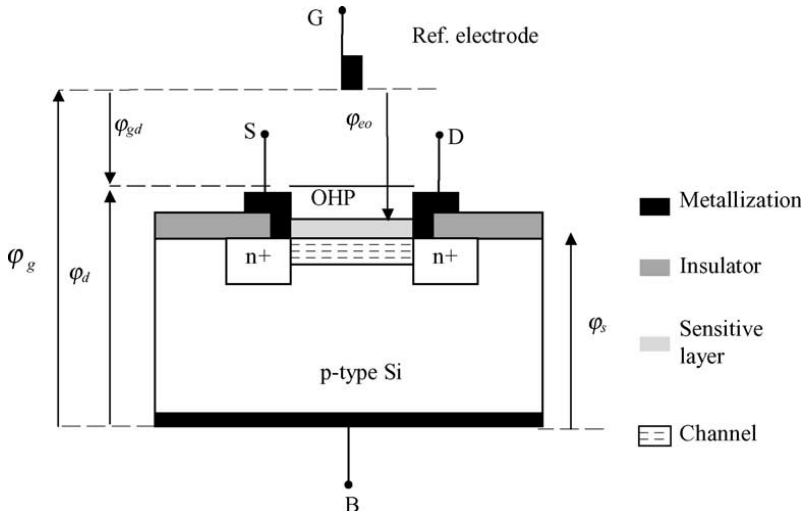


Figure 2.4: n-channel ISFET structure.

The condition of charge neutrality for the structure of figure 2.4 is given by

$$\sigma_o + \sigma_d + \sigma_s = 0 \qquad (2.1)$$

If it is considered that the charge density in the semiconductor σ_s is constant with respect to pH, and it is much smaller than the charge densities σ_d in the diffuse layer, and the charge density at the insulator electrolyte interface σ_o, the charge neutrality equation reduces to

$$\sigma_o + \sigma_d = 0 \qquad (2.2)$$

The electrochemical stage can be considered as uncoupled from the electronic stage. On applying the site-binding theory and the electrical double layer theory, we obtain:

$$\sigma_d = \sqrt{8\mathcal{E}_w kT_{c_{bulk}}} sinh\left(\frac{\Phi_{gd}}{2V_T}\right) = \alpha sinh\left(\frac{\Phi_{gd}}{2V_T}\right) \quad (2.3)$$

$$\sigma_d = qN_{sil}\left(\frac{H_b^2 exp\left(-2\frac{\Phi_{eo}}{V_T}\right) - K_A K_B}{H_b^2 exp\left(-2\frac{\Phi_{eo}}{V_T}\right) + K_A H_b^2 exp\left(-\frac{\Phi_{eo}}{V_T}\right) + K_A K_B}\right) + qN_{Nit}\left(\frac{H_b^2 exp\left(-\frac{\Phi_{eo}}{V_T}\right)}{H_b^2 exp\left(-\frac{\Phi_{eo}}{V_T}\right) + K_N}\right)$$
$$= qN_{sil} f_a(\Phi_{eo}, pH) + qN_{Nit} f_b(\Phi_{eo}, pH) \quad (2.4)$$

In equation (2.3), $\mathcal{E}_w$ is the permittivity of the electrolyte; C_{bulk} is the ion concentration in the electrolyte, N_{Sil} and N_{Nit} are the surface densities of the silanol sites and of the primary amine sites, respectively. K_A , K_B and K_N , are the binding site dissociation constants. H_b is the proton concentration in the bulk electrolyte, Φ_{eo} is the potential of the electrolyte–insulator interface, Φ_{gd} is the potential across the diffusion layer (Gouy–Chapman layer)as indicated in figure 2.4. V_T is the thermal voltage and its value is K_T/q. Equation (2.3) can also be written as equation (2.4) in which $f_a(\Phi_{eo}, pH)$ and $f_b(\Phi_{eo}, pH)$ are self explaining setting functions. Finally, the electrochemical properties of the insulator surface are combined with the physics of the MOSFET, resulting in an expression for the ISFET threshold voltage including terms derived from MOSFET theory as well as terms that are electrochemical in nature.

$$V_{th}(ISFET) = \left(E_{ref} + \Phi_{1j}\right) - (\Phi_{eo} - \chi_e) - \left[\frac{Q_{SS}+Q_{SC}}{C_{ox}} - 2\Phi_f + \frac{\Phi_{SC}}{q}\right]$$
$$= V_{th}(MOSFET) + \left(E_{ref} + \Phi_{1j}\right) - (\Phi_{eo} - \chi_e) - \frac{\Phi_m}{q} \quad (2.5)$$

In equation (2.5), Φ_f is the Fermi potential of the semiconductor, Q_{SS} is the fixed surface-state charge density per unit area at the insulator–semiconductor interface, Q_{SC} is the semiconductor surface depletion region charge density per unit area, Eref = (Erel + Eabs) is the potential of the reference electrode (Ag/AgCl considered here) relative to hydrogen electrode, Φ_{1j} is the liquid-junction potential difference between the reference solution and the electrolyte, χ_e is the electrolyte–insulator surface dipole potential, Φ_{SC} is the semiconductor work function and Φ_m is the work function of the metal gate (reference

electrode) relative to vacuum. The terms in equation (2.5) are practically constant with respect to pH, except the potential Φ_{eo} that depends on the pH parameter.

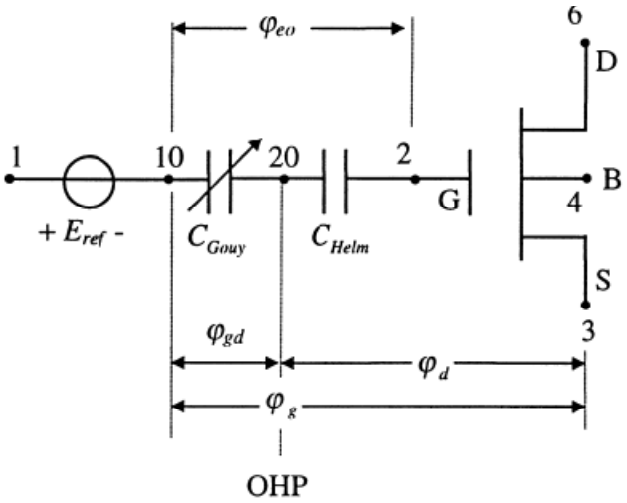


Figure 2.5: Equivalent electric circuit of ISFET [6].

This formulated approach leads to the ISFET equivalent circuit macro model shown in figure 2.5, where the capacitor C_{eq}, which takes into account the Gouy–Chapman or diffuse layer (C_{Gouy}) and the Helmholtz layer (C_{Helm}) , is defined as:

$$C_{eq} = \frac{C_{Gouy}C_{Helm}}{C_{Gouy}+C_{Helm}} \tag{2.6}$$

The dependence of the charge density of the diffuse layer σ_d on the potential of the electrolyte–insulator interface Φ_{eo} can be written also in the form:

$$\sigma_d = -\sigma_o = -C_{eq}\Phi_{eo} \tag{2.7}$$

On the other hand, the Gouy–Chapman and Helmholtz capacitances can be written as follows.

$$C_{Helm} = \frac{\varepsilon_{IHP}\varepsilon_{OHP}}{\varepsilon_{OHP}d_{IHP}+\varepsilon_{IHP}d_{OHP}} \tag{2.8}$$

$$C_{Gouy} = \frac{\partial \sigma_d}{\partial \Phi_{gd}} = \frac{\partial}{\partial \Phi_{gd}} \left[\sqrt{8 \mathcal{E}_w k T_{c_{bulk}}} sinh \left(\frac{\Phi_{gd}}{2 V_T} \right) \right]$$

For $\Phi_{gd} \ll 2V_T$, the Gouy–Chapman capacitance (C_{Gouy}) can be given by

$$C_{Gouy} \cong \sqrt{8 \mathcal{E}_w k T_{c_{bulk}}} \tag{2.9}$$

Where W and L, are the ISFET channel width and length, respectively; $\mathcal{E}_{IHP}$ and $\mathcal{E}_{OHP}$ are the inner and outer Helmholtz plane permittivities, respectively; d_{IHP} and d_{OHP} are the insulator–non-hydrated ion and the insulator–hydrated ion distances, respectively.
When equations (2.8) and (2.9) are introduced into equation (2.7), then equations (2.2) and (2.4) give the potential of the electrolyte – insulator interface, i.e.

$$\Phi_{eo} = \frac{q}{C_{eq}} [N_{sil} f_a(\Phi_{eo}, pH) + N_{Nit} f_b(\Phi_{eo}, pH)] \tag{2.10}$$

Thus the potential ϕeo is calculated from the solution of the "EIS system".
The expression for $V_{th(ISFET)}$ is

$$V_{th(ISFET)} = V_{th(MOSFET)} + EPH \tag{2.11}$$

Where $V_{th(MOSFET)}$ is the threshold voltage of MOSFET and EPH is the interface potential between sensing membrane and buffer solution i.e. ϕ_{eo}. Change in pH of electrode produce variation on the threshold voltage of equation (2.13) due to the ionic activity at electrolyte-insulator interface. Hence, the measurement of threshold voltage directly responds the pH concentration of electrolyte [6, 7].

2.3 ISFET Based pH Sensor

With the advantages of small size, reliability, rapid response, compatibility to standard CMOS technology and on-chip signal processing, Ion-Sensitive Field Effect Transistor (ISFET)-based pH meter is increasingly being applied in biomedical field. The key building blocks of ISFET based pH meter system are shown in figure 2.6. The system

consists of three major modules, including ISFET sensing readout circuitry, Temperature compensation circuitry and Analog to digital convertor. Other blocks are voltage reference circuit, LCD display driver and two point calibration circuit [8].

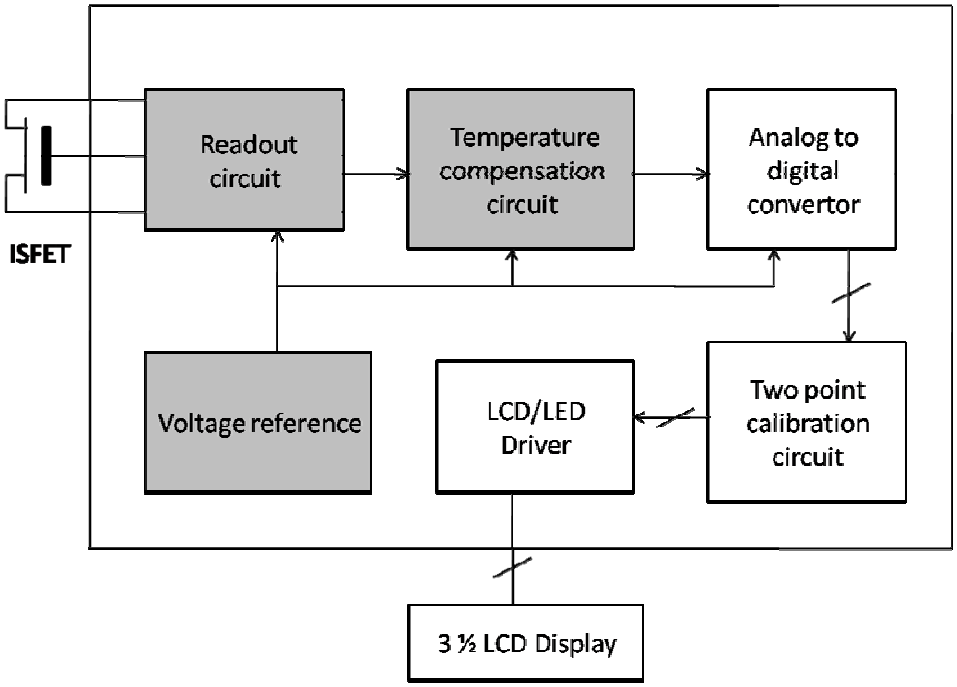


Figure 2.6: Basic building blocks of ISFET pH meter [8].

2.3.1 ISFET Sensing Readout Circuitry

The ISFET generates the voltage which is proportional to pH value of detective ions. Many architectures of readout circuit are available in literature. Some of them are disused here.

2.3.1.1 Floating-gate Constant Voltage Constant Current Circuit

The sensing readout circuit in figure 2.7 detects the ion concentration of the solution with features of Constant drain-source Voltage and Constant drain Current (CVCC) operation mode, and floating reference electrode. With this configuration, two constant voltages V_D and V_S are fed to the two positive terminals of the amplifiers cause the drain terminal (D) and the source terminal (S) of the transistor ISFET to keep a constant drain-source voltage difference. Furthermore, the off-chip resistor (R_{ext}) can be adjusted to set an athermal point for the ISFET to be at a constant drain current.

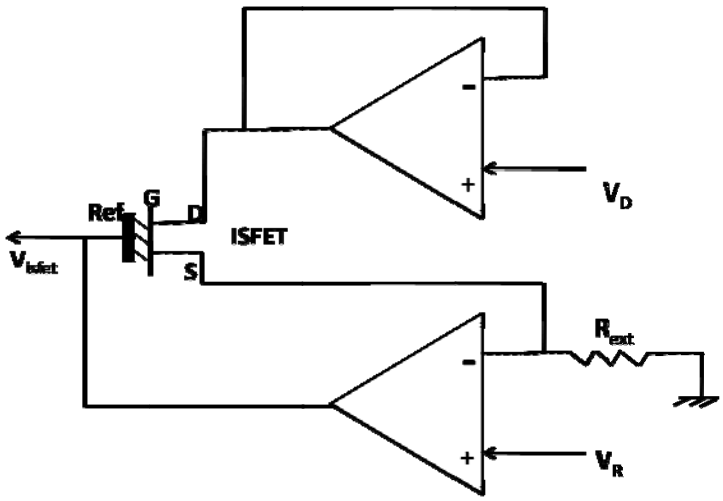


Figure 2.7: Floating gate CVCC circuit [9].

To maintain and operate the ISFET device at its linear region, the gate-source voltage variation of ISFET's threshold voltages should be directly proportional to the variations of the pH values. The potential difference between the gate sensing membrane (G) and the reference electrode (Ref) is determined by the ion concentration of the solution.

2.3.1.2 Zener-based Bridge-type Sensing Circuit

The bridge-type configuration shown in figure 2.8 contains a Zener diode biased bridge type sensing circuit with the reference electrode grounded. Because of this grounded reference electrode a single electrode can be used for multiple ISFET detection.

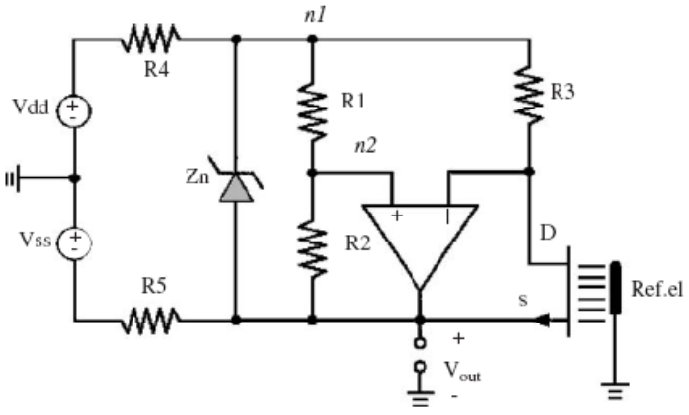


Figure 2.8: Zener-based bridge-type sensing circuit [3].

However, both sides of the zener diode are floating but cannot be integrated with ISFET-based micro-system in a standard CMOS technology.

2.1.3.3 Pechstein's Drain-output Bridge-type Sensing Circuit

Pechstein's drain-output bridge-type sensing circuit patented by Pechstein as shown in figure 2.9, is a similar approach in bridge-type Configuration, but it has revealed the following drawbacks: (a) ISFET itself serves as an input device and its channel resistance R_{DS} is an input resistor of the amplifier and (b) the drain potential is measured, but the ISFET circuit is loaded causing a variation in its operating point during measurement.

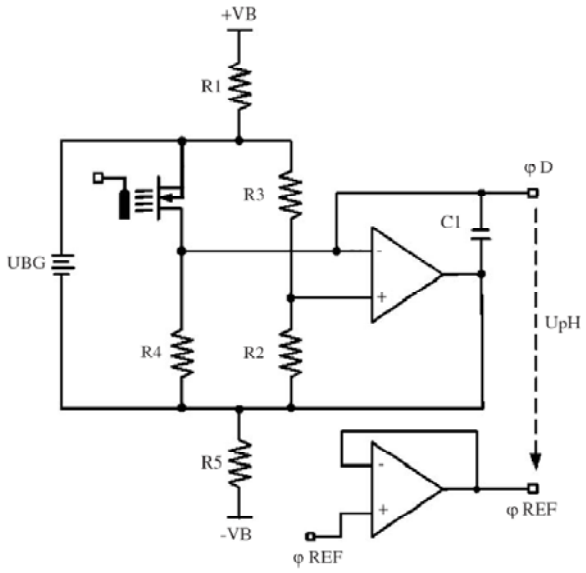


Figure 2.9: Pechstein's drain-output bridge-type sensing circuit [3].

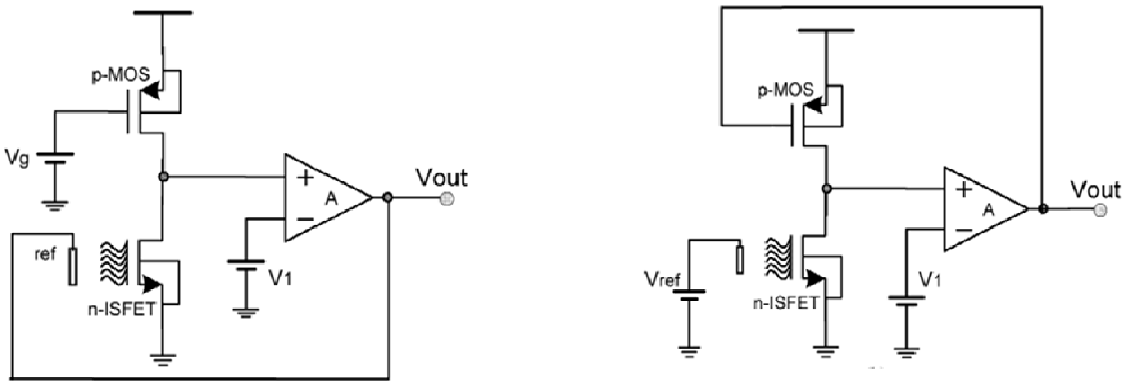
Because of these two drawbacks, the gain loop becomes more sensitive to environmental variation caused by biasing and buffer solutions.

2.1.3.4 Gate Feedback CIMP

In CMOS-based integrations n-channel ISFETs are mostly used due to low drift and high mobility properties and p-type substrate is globally and constantly grounded. In most of the existing readout techniques, the source of ISFET is not constantly biased, and is used as an internal node of the circuit, or a point of feedback application. Thus those suffer from body effect which influences the characteristics of ISFET sensor. However, even if

not influenced by pH, the threshold voltage V_T is not constant with respect to the voltage difference V_{BS} between the substrate and the source of the MOS transistor.

In 2004 Morgenshtein presented a gate CIMP (complementary ISFET/MOSFET pair) technique for readout circuitry of ISFET, which allows the elimination of body effect and solves the problems of applicability in CMOS based Microsystems. The direct feedback configuration of CIMP shown in figure 2.10 (a) consists of a complementary pair of n-channel ISFET and p-channel MOSFET. The gate of MOSFET is constantly biased, while the feedback is applied to reference electrode of ISFET.



(a) (b)

Figure 2.10: (a) Direct and (b) Indirect CIMP circuit with gate feedback [10].

The operational amplifier is used to perform double function: (1) preserving a constant V_{ds} bias in n-ISFET and p-MOSFET; (2) applying the feedback signal to the reference electrode. In this configuration the drain current of ISFET as well as V_{ds} remains constant. Figure 2.10 (b) shows an indirect feedback configuration of gate feedback CIMP. The reference electrode is constantly biased, while the feedback is applied to the gate of MOSFET. In this configuration the drain current is not constant, while V_{ds} remains constant during the operation.

2.3.2 Temperature Compensation Circuitry

There are many ways for compensating temperature effect on ISFET sensor. The following two are mainly used.

2.3.2.1 Temperature Compensation by using Diode:

A simple p-n diode, which has well known temperature characteristics and fabricated adjacent to the ISFET gate can provide fast and accurate temperature sensing and compensation (figure 2.11) .The measurement circuit configures the ISFET as a source follower, hence any change in the solution pH affects the solution-gate interface potential of the ISFET, which is detected at the ISFET source as a proportional voltage change. The diode is operated in forward bias with a constant current. Temperature changes affect the diode current which can only be observed as change in diode forward voltage since the current is kept constant. The Diode voltage is fed into an amplifier (A2) and the ISFET output is fed into an amplifier (A3) with different gains .Now the outputs of both A2 and A3 are fed into a summing amplifier to mutually offset their temperature coefficient to produce a temperature independent signal [11].

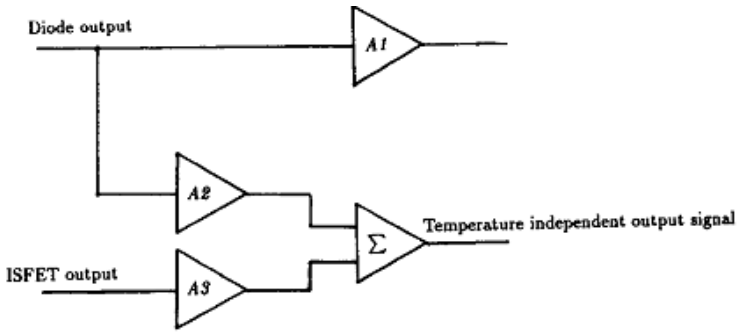


Figure 2.11: Temperature compensation circuitry using diode [11].

2.3.2.2 Temperature Compensation by using V_T Extractor

An input-free V_T extractor circuit is used to extract the threshold voltage of a MOS transistor. This V_T extractor circuit can be used as a temperature sensor. It has good linearity and reproducibility, and hence can be used for temperature compensation of ISFET. Figure 2.12 shows the compensating electronics to cancel the negative temperature coefficients (TC) generated by the ISFET with an adequate positive temperature coefficients provided by the inverting of the V_T extractor output signal [9]. The compensating electronics are completed by two components.

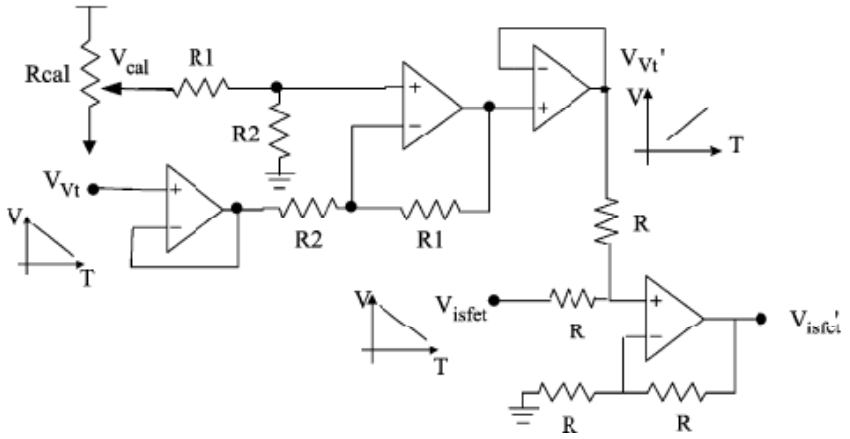


Figure 2.12: Temperature compensation circuitry using V_T extractor [9].

One is a scale circuit consisting of R_{cal}, R_1, R_2 and three operational Amplifiers, is used for inverting amplification of the V_T extractor output voltage (V_{VT}) with adjustable gains determined by:

$$V'_{VT} = V_{R_{cal}} - \frac{R_1}{R_2} V_{VT} \tag{2.12}$$

Thus, we can set V'_{VT} equals to 0 V at 0^0C and hence results in a positive temperature coefficient. Another block is a summing circuit to feed both the output voltages of V_T extractor V'_{VT} and ISFET (V_{isfet}) with different gains to mutually offset their temperature coefficients to produce a temperature independent output voltage to ADC.

2.3.3 Analog to Digital Converter

Since the output of temperature compensation circuitry is an analog voltage, an ADC is required for displaying this output or corresponding pH value of solution on LCD display. A circuit that can convert an analog voltage into a binary number proportional to the voltage is known as an analog-to-digital converter. Since biomedical field accuracy is a most important parameter, a Dual slope ADC (figure 2.13) can be used because it has more accuracy. Another advantage of this type of ADC is that there no need of DAC. The major components of this circuitry consist of an integrator, comparator and binary counter.

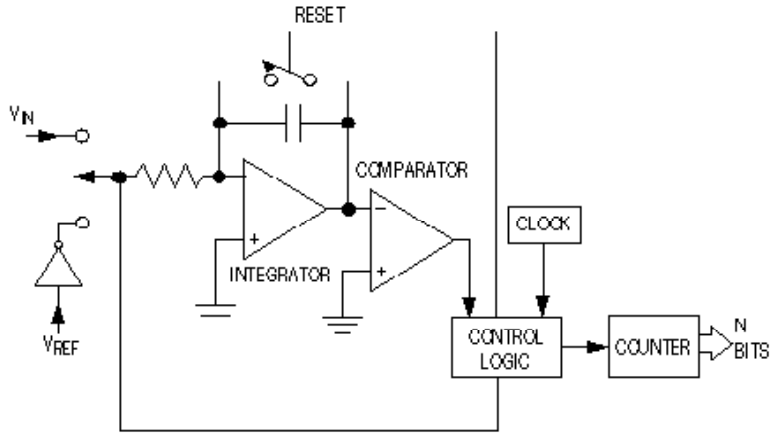


Figure 2.13: Dual slope analog to digital Converter [12].

A current, proportional to the input voltage, charges a capacitor for a fixed time interval T_{charge} (figure 2.14). At the end of this interval the device resets its counter and applies an opposite polarity (negative) reference voltage to the integrator input.

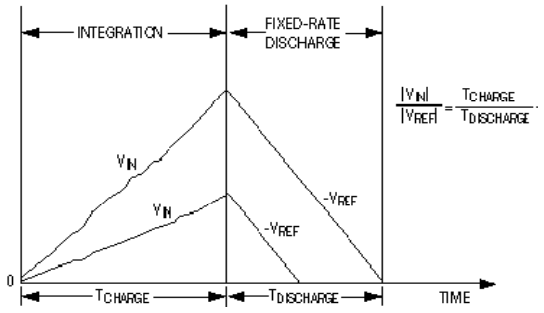


Figure 2.14: Waveform of the dual slope ADC [12].

With this opposite-polarity signal applied the capacitor is discharged by a constant current until the voltage at the output of the integrator reaches zero again. The time $T_{discharge}$ is proportional to the input voltage level and used to enable a counter. The final count provides the digital output, corresponding to the input level.

2.3.4 Other Blocks in ISFET Based pH Sensor

2.3.4.1 Voltage Reference

In order to reduce the influence of temperature on the ISFET characteristics, the optimum operating point of the ISFET can be chosen in the proximity of the ISFET is found to bias

at isothermal operating point. Bandgap reference is the most popular technique for both Bipolar and CMOS technologies to generate fixed dc reference voltage that does not change with temperature and power supply. It cancels the negative temperature dependence of a PN junction with positive temperature dependence from a PTAT (proportional-to-absolute-temperature) circuit. For providing the adjustable bias range, a bandgap reference voltage generating circuit has been modified by adding a three-bit programming option to generate proper and stable voltages with very low dependence on temperature.

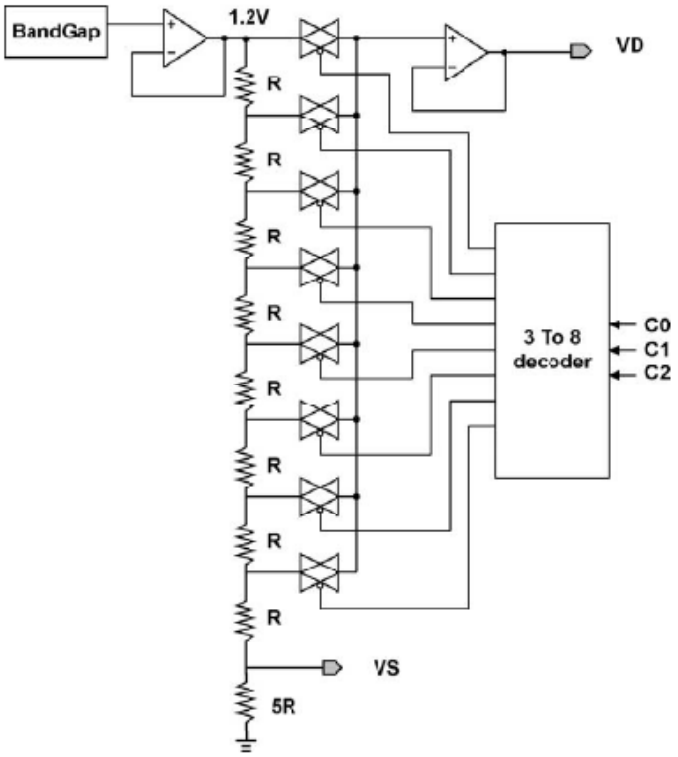


Figure 2.15: Programmable bandgap reference circuit [9].

The bandgap reference provides almost temperature and power supply independent biasing voltage. For more flexible control of constant voltage, the programmable bandgap reference circuit shown in figure 2.15 is used to supply its output references that have very little dependence on temperature and power supply to analog modules. It provides more flexible control of constant drain-source voltage [9].

2.3.4.2 LCD Display

In ISFET based pH meter the output from the ADC is in digital form so for displaying this output on the seven-segment LCD, an interface circuitry is required. Figure 2.16 shows the basic components of this LCD display driver, which are binary to BCD converter, BCD to seven segment decoder, LCD driver circuit and seven-segment LCD display.

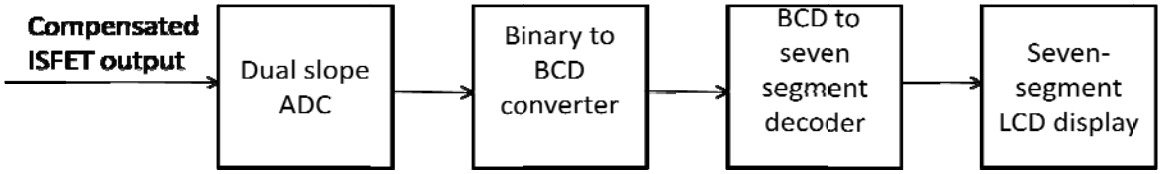


Figure 2.16: 3 ½ LCD display driver.

To display any binary output on the seven segments LCD, there is a need to convert the ADC output to a BCD code. After Binary to BCD conversion, to interface this BCD output to LCD display, there is a need of a LCD driver.

2.4 V_T Extractor

The threshold voltage is one of the most important characteristics of MOSFET. Accurate value of threshold voltage for various geometries and bias conditions has to be determined to characterize MOSFETs. Usually the threshold voltage of MOSFET is extracted either from graphical methods or from numerical methods which require considerable measurements and calculations. To overcome these disadvantages, threshold voltage extraction circuit is required to provide the threshold voltage of MOSFET on its output directly.

2.4.1 Principle of V_T Extractor

A V_T Extractor is a circuit that automatically extracts the threshold voltage of a MOSFET and delivers the extracted value on its output. This is advantageous for device characterization, compared to the common method employing linear regression, because the extractor circuit requires only a single measurement and it eliminates numerical

calculations. For a MOSFET in the saturation region, the threshold voltage can be determined by

$$V_T = V_{gs} - \sqrt{\frac{2I_D}{K}} \tag{2.13}$$

Where I_D is the drain current and $K = \mu C_{ox} W/L$, μ is the mobility of the carriers, $\boldsymbol{C_{ox}}$ is the gate capacitance per unit area, and W and L are the channel width and channel length of the MOSFET, respectively. Since normally K is unknown, V_T cannot be determined by using (2.13). The graphical method requires a $\sqrt{I_D}$ versus V_{gs} plot so that V_T can be determined by the intercept of the extrapolated curve with the V_{gs} axis. The application of this method is limited to MOSFET characterization because the determined value of V_T is not available in an electric quantity, which is required for temperature compensation circuitry of ISFET sensor.

The principle of the V_T extraction and can be explained with figure 2.17. A dc voltage V_B is applied to the gate of transistor M_1 and its drain current I_D is copied and applied via a current mirror to diode-connected transistor M_2.

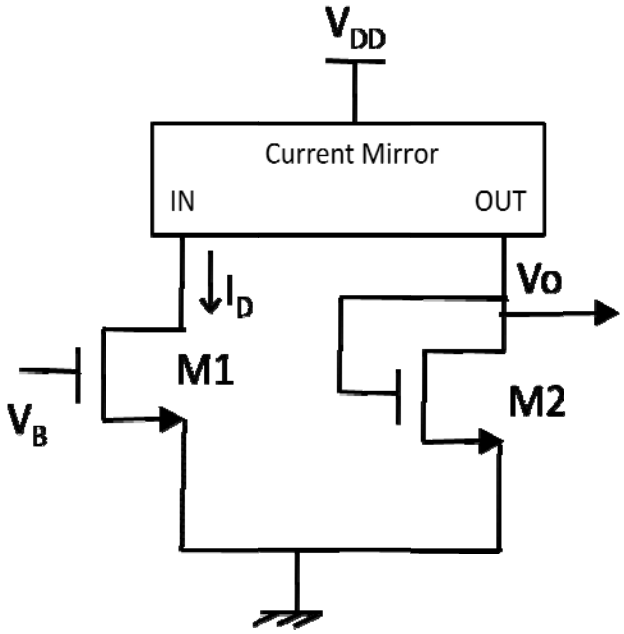


Figure 2.17: Principle of basic V_T extractor [13].

Assuming M_1 and M_2 to operate in saturation, we can apply square-law characteristic to them and obtain the output voltage.

$$V_o = \sqrt{K_1/K_2}\,V_{ref} + \left(1 - \sqrt{K_1/K_2}\right)V_T \tag{2.14}$$

This result is obtained under the assumption of $V_{T1} = V_{T2} = V_T$ which can be determined by

$$V_T = \frac{V_o - \sqrt{\frac{K_1}{K_2}}V_{ref}}{1 - \sqrt{\frac{K_1}{K_2}}} \tag{2.15}$$

Voltage V_O and V_B are known quantities since they can be measured. By contrast, the actual values of K_1 and K_2 are normally unknown. According to equation (2.15), however, the determination of V_T does not depend on the absolute value of *K* as in equation (2.13), but only on the *K* ratio, which is normally known and well under control. This is the most important and attractive advantage this technique offers.

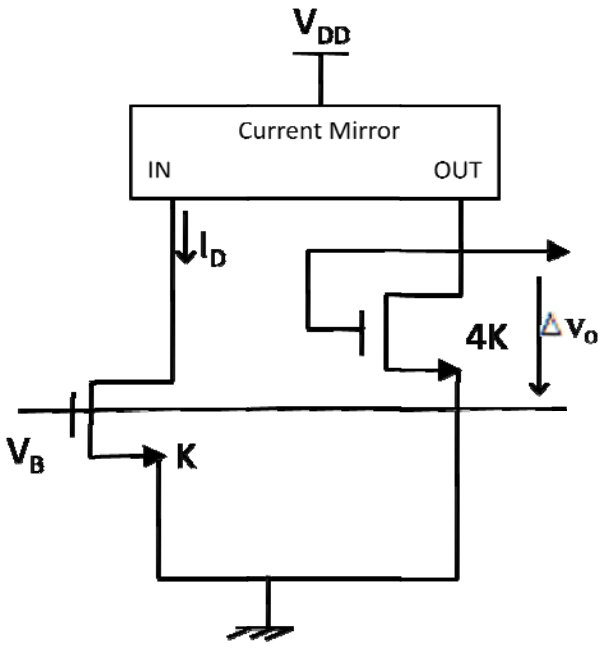


Figure 2.18: Implementation of V_T extractor with $\Delta V_O = V_T$ [13].

If $4K_1 = K_2$ then from equation (2.15)

$$V_T = 2V_O - V_B \quad (2.16)$$

Therefore, V_T can be obtained directly from V_O and V_B. The corresponding circuit implementation is shown in figure 2.18.

2.4.2 Four Terminals V_T Extractor

Figure 2.19 shows Wang's four terminal V_T extractor circuit with a current mirror. The sizes of M12 and M13 are four times of M11.

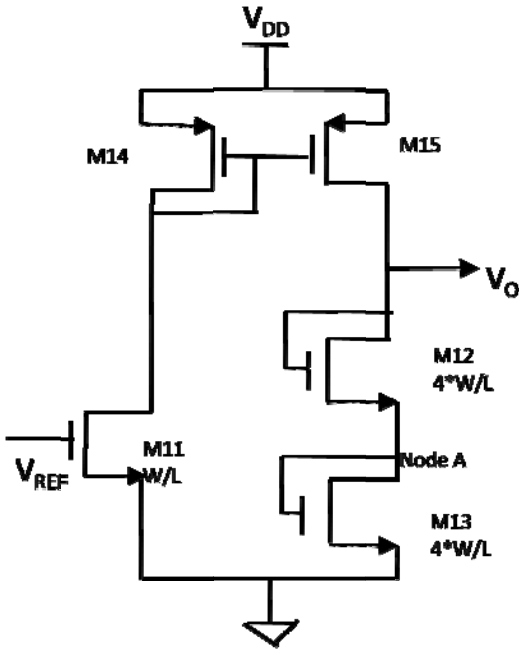


Figure 2.19: Four terminals V_T extractor [14].

The input voltage V_{REF} applied to M11, giving a current $I_D = (K / 2)(V_{REF} - V_T)^2$. This current is mirrored into, M12 and M13. Since M12 is identical to M13. And since I_D flows in each, they must have the same gate-to-source voltage ($V_{GS12} = V_{GS13}$).Hence the voltage at node A is half of V_O**.** The current in M13 is equal to $4(K / 2)(V_O/ 2 - V_T)^2$**.** Equating currents, gives following result.

$$V_T = V_O - V_{REF} \quad (2.17)$$

2.4.3 Input Free V_T Extractor

In Wang's four terminal V_T extractor, V_T is referenced to V_{REF} and not to ground. It is not possible to set V_{REF} equal to zero, as this would cut off M11-M13. The difficulty can be remedied by including a differential amplifier in the extractor circuit, giving a ground referenced threshold voltage of MOSFET on its output. Figure 2.20 shows the schematic for the input free V_T extractor; it has no V_{REF} input and thus it is a three-terminal circuit. Transistors M31 and M32 provide a bias voltage on the gate of M11**.** This voltage is also applied to the V_{LO} terminal of the differential amplifier.

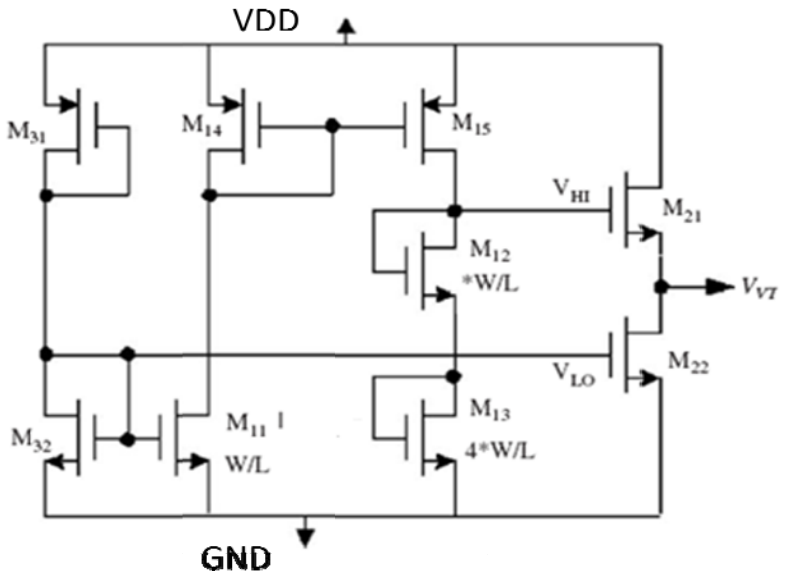


Figure 2.20: Schematic for the input free V_T extractor [14].

Transistors M11, M12, M13, M14 and M15 implement a Wang extractor circuit, whose output is applied to the V_{HI} terminal of the differential amplifier. M21 and M22 perform the subtraction of V_{HI} and V_{LO}**,** so the output voltage at the drain of M22 is the MOSFET threshold voltage (V_T) [14].

2.5 Operational Amplifier

2.5.1 Characteristics of Operational Amplifier

Operation amplifiers are key elements in analogue processing systems. The definitions of the most important features of operational amplifier are discussed here [8, 15].

2.5.1.1 Input Offset Voltage

If the differential input voltage of an ideal op-amp is zero, the output voltage is also zero. This is not true in real circuits: There are various reasons leads to a non-zero output. In order to bring the output to zero it is therefore required to apply a proper voltage at the input terminals. Such a voltage is the input offset voltage (V_{IO}).V_{IO} is normally modeled as a voltage source driving the non-inverting input. The input offset voltage of an operational amplifier is composed of two components, the systematic offset and the random offset. The systematic offset results from the design of the circuit and is present even when all of the matched devices in the circuit are indeed identical. The random offset results from mismatches in supposedly identical pairs of devices. Input offset voltage is of concern when DC accuracy of the circuit is required.

2.5.1.2 Input Common Mode Range

The input common mode voltage range, specifies the range over which the differential amplifier continues to sense and amplify the difference signal with the same gain. When the common-mode input voltage nears ground rail is required, then differential amplifier with P-FET input transistors is used. When the common-mode input voltage nears V_{DD} rail is required, then differential amplifier with N-FET input transistors is used. Rail-to-rail input op amps use complementary N- and P-type devices in the differential inputs. When the common-mode input voltage nears either rail, at least one of the differential inputs is still active, and the common-mode input voltage range includes both power rails.

2.5.1.3 Common Mode Rejection Ratio

It is the ratio of differential gain (A_{DIF}) to common mode gain (A_{CM}). An ideal amplifier will have a zero value of common mode gain therefore an infinite CMRR.

$$CMRR = \frac{A_{DIF}}{A_{CM}} \tag{2.18}$$

2.5.1.4 Power Supply Rejection Ratio

The ratio between the differential gain and the power supply gain leads to two PSRRs. PSRR shows the ability of the op-amp to reject spur signals coming from the power supply. For mixed-signal circuits, the PSRR is a very important issue. The power voltage

affects the bias point of the input differential pair because of the inherent mismatches in the input circuitry, changing the bias point changes the offset voltage, which, in turn, changes the output voltage.

2.5.1.5 Slew Rate

Slew rate is defined as the maximum output voltage rate either positive or negative. . Its unit is V/μs. It is measured using the op-amp in the unity gain configuration (figure 2.21). A large input step voltage fully imbalances the input differential stage and brings the op-amp output response into the slewing conditions. The slew rate performance of the CMOS differential amplifier depends on the value of bias current and the capacitance from the output node to ground. The slew rate of CMOS differential amplifier is given by

$$\text{Slew Rate (SR)} = dV_{OUT}/dt = I_{SS}/C \quad (2.19)$$

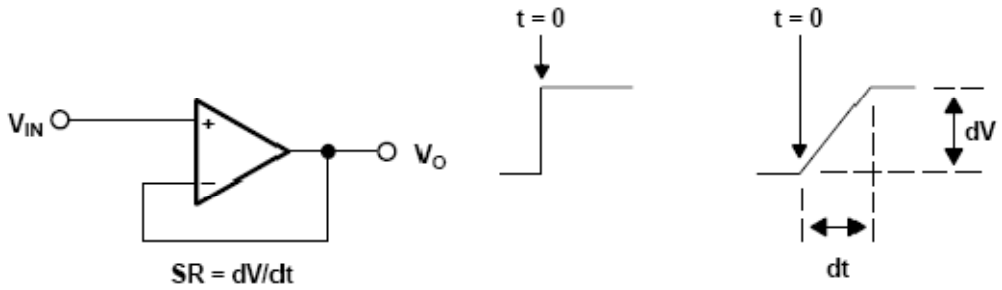


Figure 2.21: Slew rate measurement [15].

2.5.1.6 Output Swing

This is maximum swing at the output node without producing a considerable degradation of op-amp performance. The output swing is only a fraction of (V_{DD} - V_{SS}).Within the output swing range the response of the op-amp should conform to given specifications and the harmonic distortion should remain below the required level.

2.5.1.7 Equivalent Input Noise

The noise performance of a CMOS operational amplifier depends on the noise of the transistors used and circuit architecture. The noise of an MOS transistor is composed of white noise and flicker noise (1/f). In figure 2.22 at corner frequency, 1/f term becomes

equal to the white. 1/f noise dominates at higher frequencies while at lower frequency, white noise dominates.

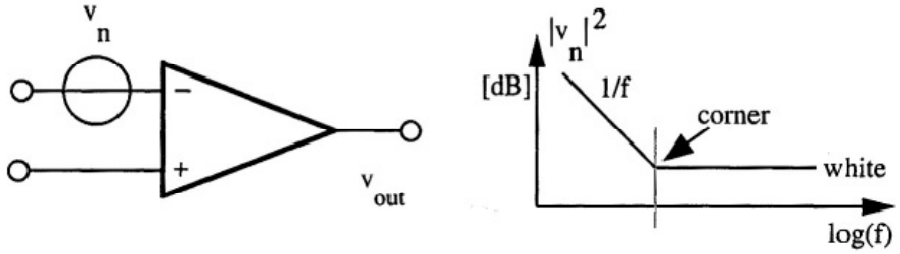


Figure 2.22: Equivalent input referred noise voltage and its spectrum [15].

The frequency at which the 1/f term becomes equal to the white one is called corner frequency.

2.5.1.8 Settling Time

This is the time that the output voltage requires, under given operating conditions, to achieve the expected output voltage within a given accuracy (usually 0.1% or better). The settling time is measured from the end of the slewing period. It critically depends on the phase margin: a poor phase margin leads to a ringing response that augments the settling period.

2.5.1.9 Unity Gain Frequency (UGB)

The small signal analysis determines the frequency response sketched by a set of zeros and poles. The frequency at which the gain (A_{DIF}) becomes 1 unit or 0 dB is called unity gain frequency.

2.5.1.10 Phase Margin

This is the phase shift of the small-signal differential gain measured at the unity gain frequency as shown in figure 2.23. For a phase margin less than 0°, the system is considered to be unstable. A marginally stable system has a phase margin between 0° and 45°. In order to ensure stability it is necessary to achieve a phase margin better than 60°. A lower phase margin (like 45° or less) will cause ringing in the output response. For

greater PM, the system is more stable but time response slows down. Thus PM = 60° is typically considered as optimum value.

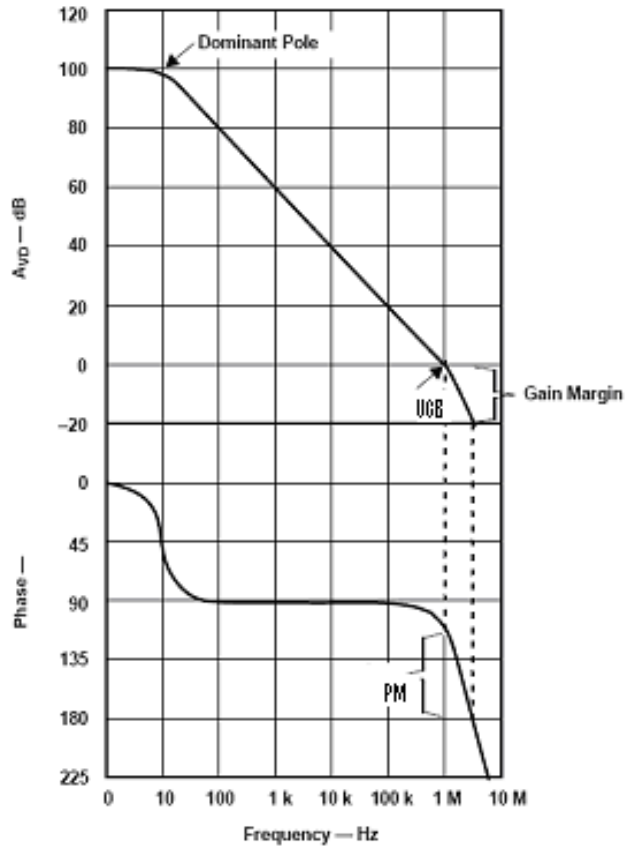


Figure 2.23: Gain & Phase plot.

2.5.2. Op-amp Topologies

2.5.2.1 Telescopic Cascode Operational Amplifier

The simplest version of a single stage OTA is the telescopic architecture. The input differential pair injects the signal currents into common gate stages. Then, the circuit achieves the differential to single ended conversion with a cascode current mirror. Note that the transistors are placed one on the top of the other to create a sort of telescopic composition. The small signal resistance at the output node is quite high. Such a high resistance benefits the small signal gain without limiting the circuit functionality when we require an OTA function. The schematic of telescopic cascode op-amp is shown in figure 2.24.

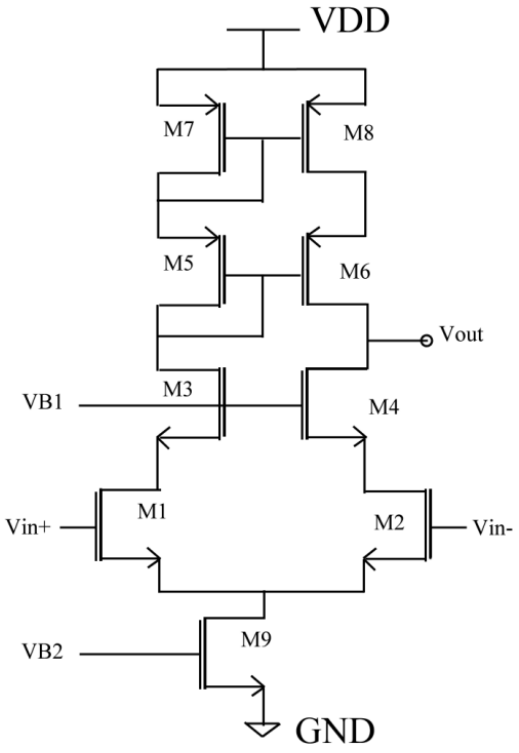


Figure 2.24: Telescopic cascode op-amp [16].

By inspection of the circuit, the derived expression of low-frequency small signal differential Gain is as follows:

$$A_O = g_{m1}\left(r_{ds8}g_{m6}r_{ds6}r_{ds2}g_{m4}r_{ds4}\right) \Big/ \left(r_{ds8}g_{m6}r_{ds6} + r_{ds2}g_{m4}r_{ds4}\right) \quad (2.20)$$

It is proportional to the square of the product of a transistor trans-conductance and an output resistance. Therefore, as expected, the telescopic cascade achieves a gain similar to the one of the two stages architecture. Moreover, by cascode configurations may be used to increase the voltage gain of CMOS transistor amplifier stages. This structure has been called a telescopic-cascode op-amp because the cascodes are connected between the power supplies in series with the transistors in the differential pair, resulting in a structure in which the transistors in each branch are connected along a straight line .The main potential advantage of telescopic cascade op amps is that they can be designed so that the signal variations are entirely handled by the fastest-polarity transistors in a given process.

In addition to the poor common-mode input range calculated another disadvantage of the telescopic cascode configuration is that the output swing is small.

2.5.2.2 Folded Cascode Op-amp

In order to remove the drawbacks of telescopic cascade op-amp, a folded cascode op-amp can be used. This architecture is used to improve PSRR. An important property of folded cascode op-amp is the capability of handling input common levels close to supply rails (V_{DD}, V_{SS}). In these types of op-amps, the small signal current is folded up or folded down [14, 16]. The load capacitance itself acts as compensation capacitance. The dominant pole is associated with the output C_L provides frequency compensation. Increasing C_L improves phase margin. One of the advantages of the folded cascade op-amp is that it has push-pull output. This means the op-amp can actively sink or source current from the load. The exact match of the currents in the differential amplifier is not demanded by the folded cascode op-amp since extra current can flow in or out of the current mirror. While the bias current in the conventional cascode delivers the current in both the input devices and the cascade devices since they are stacked together. The bias current of folded cascode (I_{ss}) supplies only the input devices. So additional current (I_{D3}) is required to add necessary bias current .There are two basic form of folded cascode op-amp. First is n-channel input folded cascode op-amp and second is p-channel input folded cascode op-amp.

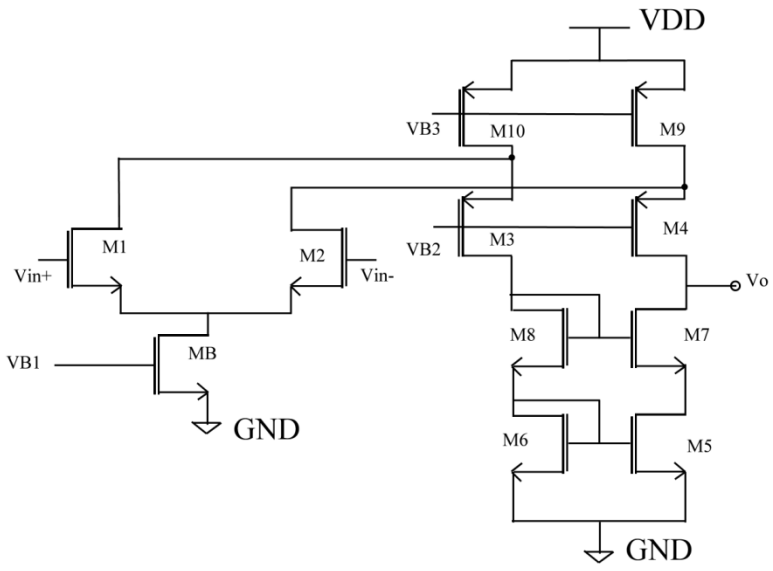


Figure 2.25: N-channel input folded cascode op-amp [16].

An N-channel input folded cascode op-amp is shown in figure 2.25, in which PMOS input device and NMOS cascode transistors are used. Such a circuit potentially provides a higher gain than the P-channel input folded cascode op-amp because of greater mobility of NMOS devices. When there is a need of input common levels closet to V_{DD}, then this topology is used.

In P-channel input folded cascode op-amp, NMOS input devices and PMOS cascode transistors are used. The PMOS input folded cascode has become the prime choice over its NMOS counterpart for its higher non-dominant poles, lower flicker noise, and input common mode level. A PMOS input pair is chosen so that a common-mode level close to ground could be accommodated. In p-channel input folded cascode op-amp which is shown in figure 2.26, the input CM level cannot be less than V_{b1}-V_{GS3}+|V_{THP}|. By using a cascode mirror in folded cascode op-amp, a gain of two stage op-amp can be achieved. The small signal gain P-channel input folded cascode op-amp is given by

$$A_{O1} = g_{m1}(R_{n,cascode}||R_{p,cascode}) = g_{m1}(g_{m4}r_{o4}r_{o6}||g_{m8}r_{o8}r_{o10}) \quad (2.21)$$

The maximum output voltage swing of folded cascode op-amp which is designed in figure 2.26 can be calculated.

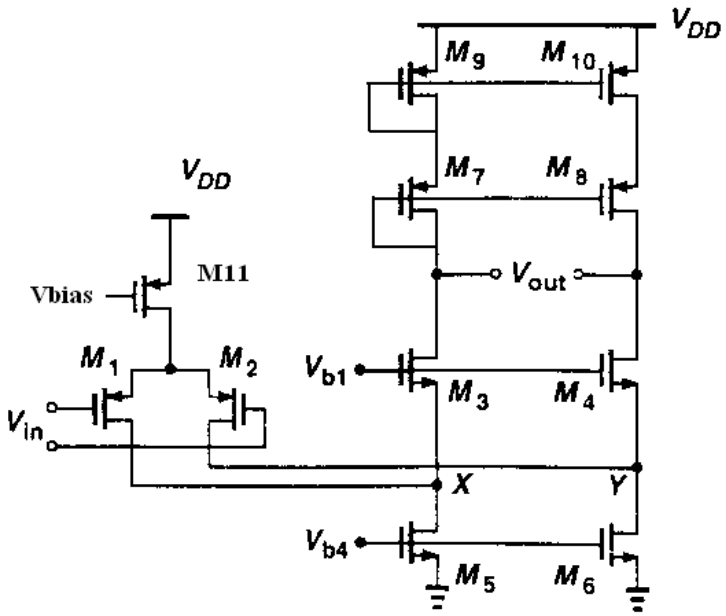


Figure 2.26: P-channel input folded cascode op-amp [16].

With proper choice of $V_{b1}$and V_{b4}, the lower swing is given by $V_{OD3}+V_{OD5}$ and the upper end by V_{DD} - ($|V_{OD7}|$ +$|V_{OD9}|$).Thus the peak to peak swing is equal to V_{DD} - ($V_{OD3}+V_{OD5}$ +$|V_{OD7}|$ +$|V_{OD9}|$).

2.5.2.3 Two Stage Op-amp

As specified by the name, the circuit is the cascade of two stages: the first stage usually consists of a high-gain differential amplifier. This stage has the most dominant pole of the system. A common source amplifier usually meets the specification of second stage, having a moderate gain. A typical CMOS differential amplifier stage is shown in figure 2.27. Differential amplifiers are often desired as the first stage in an op-amp due to their differential input to single –ended output conversation and high gain. The input devices in figure 2.27 are P-channel MOSFETs (PMOS). PMOS input devices are used more because of its improved slew rate and reduced 1/f noise. PMOS input devices also provide reduced power supply rejection due to the current mirror's low sensitivity to change in power supply voltage. The circuit in figure 2.27 uses the same reference current for the differential amplifier and the second stage. Therefore, the bias currents in the two stages will be controlled together. Observe that the conversion from differential to single ended is achieved in the first stage with a current mirror (M3-M4). As a matter of fact, the signal at the output of the differential pair is current. The current from M1is mirrored by M3-M4 and subtracted from the current from M2.

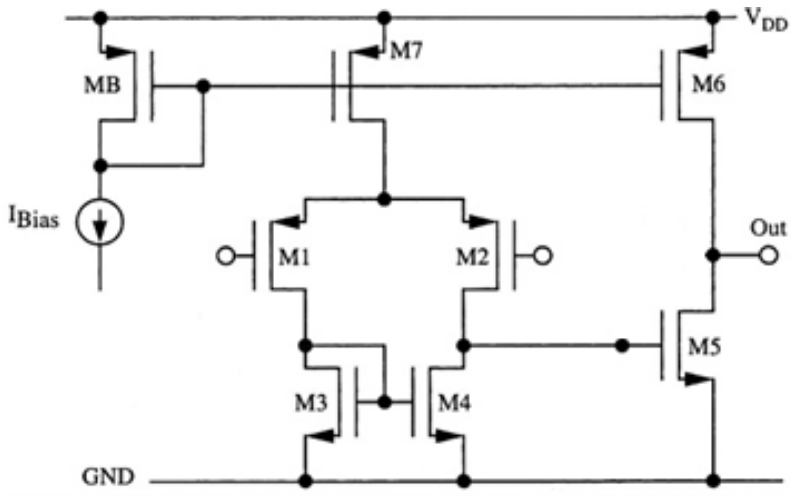


Figure 2.27: Two stage op-amp.

The signal contributions of the two currents multiplied by the output resistance of the first stage give the single-ended first stage output voltage. The resulting signal constitutes the input of the second gain stage. The low frequency gain is given by the product of the two gains. By inspection of the circuit we obtain

$$A_V = A_1 A_2 = \frac{g_{m1} g_{m5}}{(g_{ds2}+g_{ds4})(g_{ds5}+g_{ds6})} \tag{2.22}$$

The small signal equivalent circuit of the two stage amplifier in figure 2.27 can be represented with the simplified diagram in figure 2.28. Each stage is represented by a transconductance generator and the parallel connection of an output resistance and a load capacitance. The two *RC* networks contribute with two poles whose angular frequencies are

$$p_1' = \frac{1}{\tau_1} = \frac{1}{R_1 C_1}$$
$$p_2' = \frac{1}{\tau_2} = \frac{1}{R_2 C_2} \tag{2.23}$$

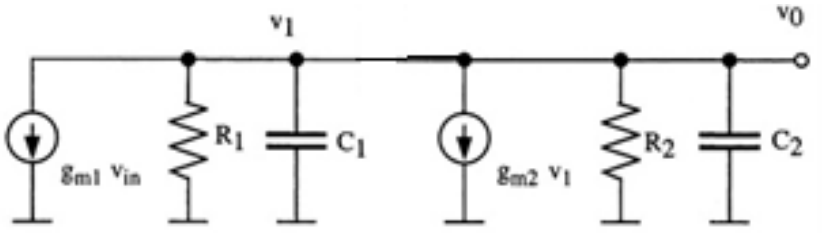


Figure 2.28: Small signal equivalent of two stage op-amp.

In this model, g_{m1} and g_{m2} are the trans-conductance of input transistors (M_1, M_5) in both stages. The output resistances (R_1, R_2) of the two stages are given by the parallel connection of r_{ds2} and r_{ds4}. The load capacitances (C_1, C_2) result from the parasitic elements of the transistors used and load capacitance.

2.5.2.4 Gain Boosting

In one stage op-amps such as telescopic and folded cascade topologies the objective is to maximize the output impendence so as to attain high voltage gain. The gain-boosting technique is used to further increase the output impendence without adding more cascade devices. The gain-boosting technique improves accuracy of cascoded CMOS circuits without any speed penalty. This is achieved by increasing the effect of the cascode transistor by means of an additional gain-stage, thus increasing the output impedance of the sub-circuit. Used in op-amp design, this technique allows the combination of the high-frequency behavior of a single-stage op-amp with the high DC-gain of a multistage design. this approach can be applied to a differential cascade stage as shown in figure 2.29 (a).The single ended amplifiers A_1 and A_2 in figure 2.29(a) can be replaced by one double ended differential pair (figure 2.29(b)), whose basic implementation is shown in figure 2.29(c).The minimum voltage at the drain of M3 is equal to $V_{OD3}+V_{GS5}+V_{ISS2}$, where V_{ISS2} is the voltage required across I_{SS2}.On the other hand this minimum voltage would be approximately one threshold voltage lower.

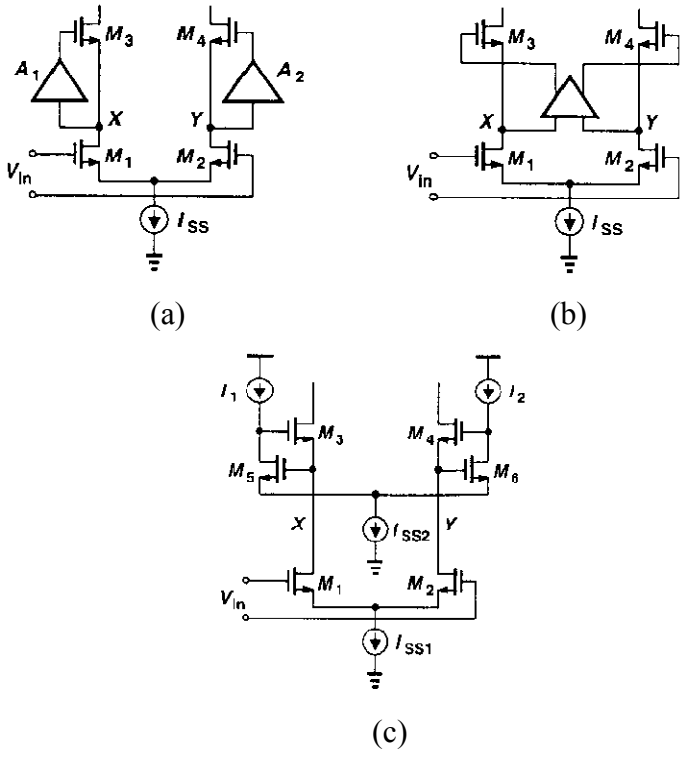


Figure 2.29: Boosting of the output impedance of a differential cascade stage [16].

2.6 Current and Voltage References

A precision voltage reference and current reference circuit is very important in the design of mixed-signal and analogue integrated circuits such as differential amplifier, ISFET readout circuit and data convertors [16].

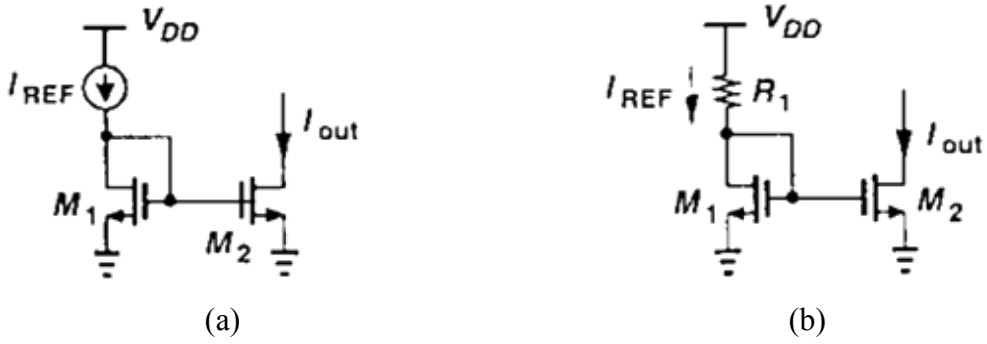
2.6.1 Current Mirror

Figure 2.30 (a) shows the basic current mirror which is a conventional method of biasing. Since $V_{GS1}= V_{GS2}$ the same current or a multiple of the current in M_1 will be copied to each stage on basis of the sizes of each transistor, provided all transistors stay in saturation region. The current I_{D1} is given by

$$I_{D1} = \frac{\beta_1}{2}(V_{GS1} - V_{THN})^2 \tag{2.24}$$

If M_2 is assumed in saturation region, the current flowing in M_2 is

$$I_{D2} = I_o = \frac{\beta_2}{2}(V_{GS2} - V_{THN})^2 \tag{2.25}$$



(a) (b)

Figure 2.30: Current-mirror biasing using (a) an ideal current source (b) a resistor [16].

Since $V_{GS1} = V_{GS2}$, the ratio of the drain currents is given by

$$\frac{I_{D2}}{I_{D1}} = \frac{W_2 L_1}{W_1 L_2} = \frac{\beta_2}{\beta_1} \tag{2.26}$$

This equation shows *W/L* ratio of the two devices to can be adjusted to achieve the desired output current. If I_{REF} does not vary with V_{DD} and channel length modulation of M_2 is neglected, then I_D remains independent of the supply voltage. A resistor is tied from V_{DD} to the gate of M1 (figure 2.30 (b)) .Now the output current of this circuit is sensitive to V_{DD}.

$$\Delta I_{out} = \frac{\Delta V_{DD}}{R_1 + 1/g_{m1}} \cdot \frac{(W/L)_2}{(W/L)_1} \tag{2.27}$$

These references are required to be stable over process, power supply voltage, and temperature variations.

2.6.2 Supply Independent Biasing

In order to get supply independent current, the circuit must bias itself i.e. I_{REF} must be derived from I_{out}. The idea is that if I_{out} is to be independent of V_{DD} then I_{REF} is the copy of I_{OUT}. In figure 2.31 M_3 and M_4 copy I_{out}, thereby defining I_{REF}. If M_1- M_4 operates in saturation and channel length modulation is neglected then the following relation can be obtained.

$$I_{out}=K \cdot I_{REF} \tag{2.28}$$

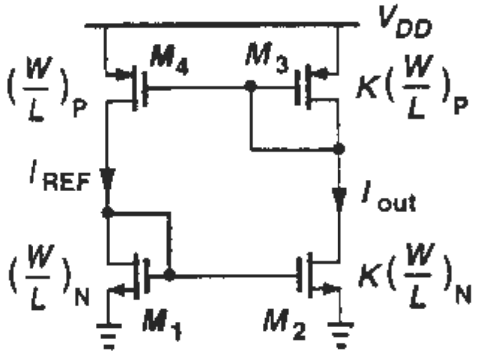


Figure 2.31: Simple supply independent current reference [16].

Since a current source is fed to each diode connected device, I_{out} and I_{REF} are relatively independent from V_{DD}. For defining currents uniquely a resistor R_S is used (figure 2.32(a)). This configuration is also known as beta multiplier reference. The width of M_2 is made *K* times larger than the width of M_1 and L_1=L_2, so that

$$\beta_2 = K \cdot \beta_1 \tag{2.29}$$

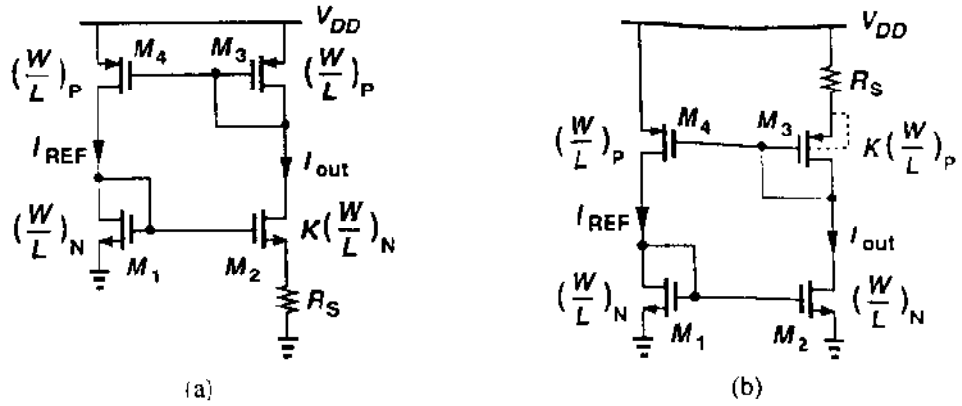


Figure 2.32: Beta multiplier reference [16].

Therefore it can be written

$V_{GS1} = V_{GS2} + I_{D2} R_S$

Or

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}} + V_{TH1} = \sqrt{\frac{2I_{out}}{\mu_n C_{ox} K(W/L)_N}} + V_{TH2} + I_{out}R_S \quad (2.30)$$

On neglecting body effect, we have

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}} \left(1 - \frac{1}{\sqrt{K}}\right) = I_{out}R_S,$$

And hence

$$I_{out} = \frac{2I_{out}}{\mu_n C_{ox}(W/L)_N} \cdot \frac{1}{{R_S}^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2 \quad (2.31)$$

This is the basic design equation for this reference. The size parameter *K* must always be greater than 1. In the above calculation, it is assumed that V_{TH1} and V_{TH2} are equal but in actual these are equal because the sources of M_1 and M_2 are at different potential. To avoid this problem the resistor is placed at the source of M_3 (figure 2.32 (b)) while tying source and bulk of each PMOS transistor for eliminating body effect.

2.6 .3 Temperature Independent References

Reference voltages and currents with little dependence to temperature prove useful in many analog circuits. As many process parameters vary with temperature, if a reference is temperature-independent, it is usually process independent as well. If two quantities

with opposite temperature coefficient are added with proper weighting, the resultant quantity theoretically exhibits zero temperature coefficient. For V_1 and V_2 with opposite temperature dependence, the coefficients c_1 and c_2 can be chosen in such a way that $Vref=c_1V_1+c_2V_2$ Thus, the reference voltage exhibits zero temperature coefficient.

2.6.3.1 Bandgap Voltage Reference

The bandgap voltage reference is required to exhibit both high power supply rejection and low temperature coefficient, and is probably the most popular high performance voltage reference used in integrated circuits today. Among various devices in the semiconductor technology, the characteristics of the bipolar transistors have proven the most reproducible and well-defined quantities that provide positive and negative temperature coefficients. Figure 2.33 shows the basic principle of bandgap Reference. The forward voltage of a p-n junction diode or the base-emitter voltage of bipolar transistor exhibits a negative TC. The PTAT term is realized by amplifying the voltage difference of two forward-biased diodes (i.e. base-emitter junctions).Thus a reference voltage with zero temperature coefficient is obtained and given by:

$$V_{ref} = V_{BE} + K.V_{PTAT} \quad (2.32)$$

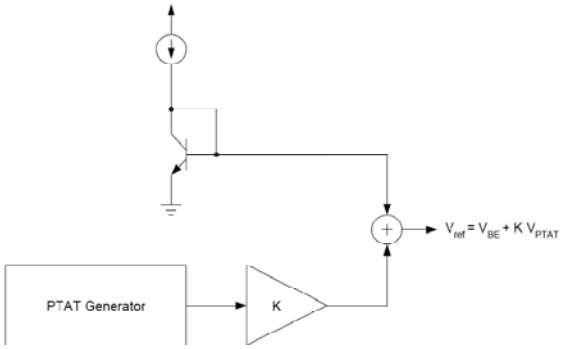


Figure 2.33: Principle of bandgap reference [16].

For bipolar transistor the collector current

$$I_C = I_S\, exp\left(V_{BE}/V_T\right) \quad (2.33)$$

Where $V_T = k.T/q$. I_S is the saturation current which is proportional to μkTn_i^2 where μ is the is the mobility of minor carrier and n_i is the carrier concentration of silicon. Again the temperature dependency of μ and n_i are represented by

$$\mu \propto \mu_0 T^m$$

$$n_i^2 \propto T^3 \, exp\left(-E_g/_{kT}\right)$$

Where $m \approx -3/2$ and $E_g \approx 1.12\, eV$ is the bandgap energy of silicon. Thus it is given by

$$I_S = bT^{4+m} \, exp\left(-E_g/_{kT}\right) \tag{2.34}$$

Where b is proportionality factor. For simplifying the analysis the I_C is assumed constant with temperature. On taking derivative of I_C with respect to T and by using the above equation, the temperature coefficient of base emitter voltage is obtained and given by

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_T}{T}\ln\frac{I_C}{I_S} - (4+m)\frac{V_T}{T} - \frac{E_g}{kT^2}V_T = \frac{V_{BE} - (4+m)V_T - E_g/q}{T} \tag{2.35}$$

This is negative and has revealing dependence on the magnitude of V_{BE} itself. Exact Cancellation of the dependence of V_{ref} to temperature is not possible because of component tolerances and second order effects such as the nonlinearity of the dependence of VBE on temperature. For PTAT term two bipolar transistor operate at unequal current densities are used (figure 2.34). Now the difference between their base-emitter voltages is given by

$$\Delta V_{BE} = V_{BE1} - V_{BE2}$$

$$= V_T \ln\frac{nI_0}{I_{S1}} - V_T \ln\frac{I_0}{I_{S2}} = V_T \ln n \tag{2.36}$$

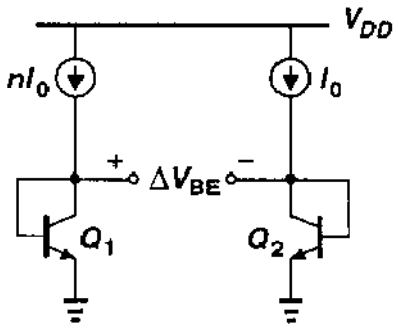


Figure 2.34: Generation of PTAT voltage [16].

Thus V_{BE} exhibit positive temperature coefficient, which is given by

$$\frac{\partial V_{BE}}{\partial T} = \frac{k}{q} \ln n \tag{2.37}$$

With the negative and positive TC, a reference (V_{REF}) having a zero temperature coefficient can be developed and given by

$$V_{REF} = \alpha_1 V_{BE} + \alpha_2 (V_T \ln n) \tag{2.38}$$

At room temperature $\frac{\partial V_{BE}}{\partial T} \approx -1.5\, mV/K$ whereas $\frac{\partial V_T}{\partial T} \approx +0.087 mV/K$. If α_1=1 then for zero TC, $\alpha_2 \ln n$ is chosen such that $\alpha_2 \ln n\,(0.087) = 1.5$

A conventional CMOS bandgap reference for n-well process is shown in figure 2.35. Transistors Q1 and Q2 are assumed to have emitter base areas of A_{E1} and A_{E2}, respectively.

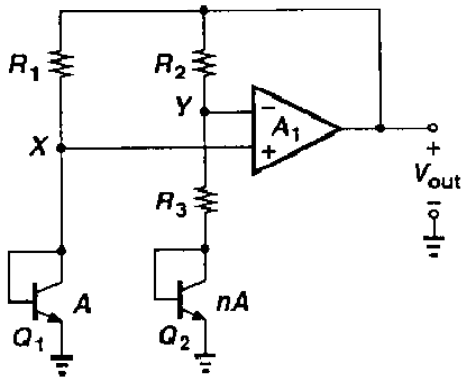


Figure 2.35: Implementation of bandgap reference [16].

If offset voltage of op-amp is assumed to be zero, then

$$V_{out} = V_{BE2} + \frac{V_T \ln n}{R_3}\left(1 + \frac{R_2}{R_3}\right) \quad (2.39)$$

Where n = A_{E2} / A_{E1}. The first term is the CTAT term and the second the PTAT term.

Chapter 3

Circuit Implementation

In this chapter the schematics and layouts of key components and building blocks have been designed. Cadence Composer is used to implement the schematics. For layout design Cadence Virtuoso layout editor is used. DRC, LVS and RCX have been performed by using Cadence Assura.

3.1 ISFET Model

For the project modeling, the ISFET used is an n-channel device with a gate insulator consisting of SiO_2 that is covered by an Al_2O_3 layer. The dimensions of the ISFET are 400/20 μm. The W/L must be in suitable size to ensure a good contact with the liquid at the gate. In addition to this, the W and L size affects the current flow across the drain and source.

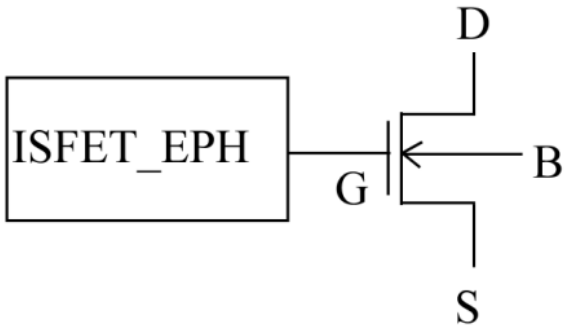


Figure 3.1: ISFET model.

A general model of ISFET has been achieved by considering it as two fully uncoupled stages: an electronic stage i.e., the MOSFET which is the starting structure of the ISFET

and an Electro-chemical stage i.e., the electrolyte–insulator interface. The expression for $V_{TH\ (ISFET)}$ is

$$V_{TH\ (ISFET)} = V_{TH\ (MOSFET)} + EPH \quad (3.1)$$

Where $V_{TH\ (MOSFET)}$ *is* the threshold voltage of FET and EPH is is the interface potential between sensing membrane and buffer solution. The EPH term is pH dependent and it is modeled using Verilog–A language. Then electrochemical stage is interfaced with electronic stage (MOSFET) as shown in figure 3.1.

The ISFET static model is obtained by considering the threshold voltage $V_{th\ (ISFET)}$ in the current equations of the MOSFET, i.e.

$$I_{ds} = \frac{\beta}{2}\left(V_{gs} - V_{th(isfet)}\right)^2 \quad \text{(Saturation region)} \quad (2.2)$$

$$I_{ds} = \frac{\beta}{2}\left(2\left(V_{gs} - V_{th(isfet)}\right)V_{ds} - V_{ds}^2\right) \quad \text{(Linear region)} \quad (2.3)$$

Where β = (μ Cox W/L) and μ, W and L are the electron mobility, the channel width and channel length respectively. V_{ds} is the drain- source voltage, V_{gs} is the gate-source voltage.

3.2 Op-amp Topology Selection

OP- amp is the key component for both ROIC and temperature compensation circuitry of ISFET based pH meter. In biomedical micro-system, circuits with higher accuracy are required. This indicates that the chosen topology of op amp must have high open loop and minimal noise with less power consumption.

Table 3.1: Comparison of various op-amp topologies

Op-amp	**Gain**	**Output Swing**	**Speed**	**Power Dissipation**	**Noise**
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-Stage	High	Highest	Low	Medium	Low
Gain-Boosted	High	Medium	Medium	High	Medium

From Table 3.1, it is clearly visible that a two stage amplifier is best suited configuration from all aspects. An Op-amp is desired to scale-up the temperature coefficient of V_T extractor. Since the output range of this V_T extractor is near to ground but less than $V_{DD}/2$, a p-input differential pair two stage amplifier is suitable. The circuit, in figure 3.2 uses the same reference current for the differential amplifier and the second stage. Therefore, the bias currents in the two stages will be controlled together. The conversion from differential to single ended is achieved in the first stage with a current mirror (M3-M4). The signal at the output of the differential pair is current. The current from M1is mirrored by M3-M4 and subtracted from the current from M2.The signal contributions of the two currents multiplied by the output resistance of the first stage give the single-ended first stage output voltage. The resulting signal constitutes the input of the second gain stage. For a two-stage op-amp single capacitor Miller compensation (SCMC), which significantly reduces the frequency of dominant pole and moves the output pole away from the origin is a common technique in op-amp design. As the transistor gain of the second stages increases, the dominant pole decreases and the non-dominant pole increases. In this way the two poles are being split apart and stabilize the feedback amplifiers by greatly narrowing the bandwidth. This simple pole splitting method also introduces a right half plane zero which causes negative phase shift. As a result, the stability is made a little poorer. The zero comes from the direct feed through of the input to the output through the Miller capacitor.

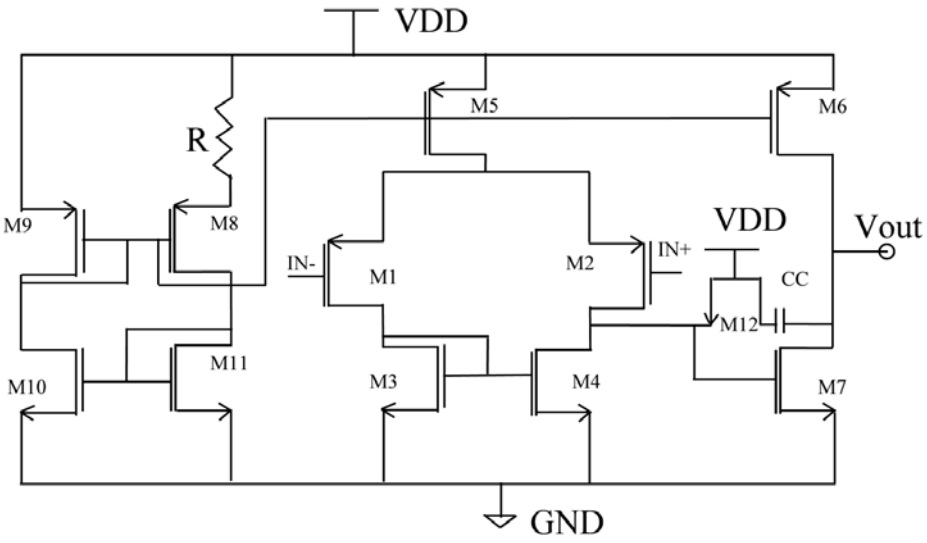


Figure 3.2: Two stage Op-amp.

To eliminate the RHP zero due to the feed through and increase the phase margin of the op amp, a nulling resistor is added in series with the compensation capacitor (SMCNR) to increase the impedance of the feed through path. A MOSFET, operated in linear region can be used for implementing this nulling resistor.

A beta multiplier current reference circuit is used for biasing, which provides supply independent current. The basic design equation for this reference is

$$I_{out} = \frac{2\left(1-\frac{1}{\sqrt{K}}\right)^2}{\mu_n C_{ox}\left(W/L\right)_N R^2} \quad (3.4)$$

Where K= $(W/L)_{M8}$ / $(W/L)_{M11.}$ Resister R is used for defining current value.

3.3 V_T Extractor

The MOSFET threshold voltage V_T at temperature T can be described by

$$V_T = V_{T_r} - \alpha(T - T_r) \quad (3.5)$$

Where V_{T_r} is the threshold voltage at room temperature T_r (300 K) and α is the temperature coefficient of threshold voltage. According to equation (3.5), as the temperature is increased, the threshold voltage of MOSFET is reduced. This relation is useful for temperature compensation in ISFET based pH meter and for implementing temperature independent voltage reference. The threshold voltage of MOSFET extracted either from graphical methods or from numerical methods requires considerable measurements and calculations. The applications of these methods are limited to MOSFET characterization because the determined value of V_T is not available in an electric quantity, which is required for temperature compensation circuitry of ISFET sensor. To overcome these disadvantages, threshold voltage extraction circuit is required to provide the threshold voltage of MOSFET directly on its output. A V_T Extractor is a circuit that automatically extracts the threshold voltage of a MOSFET and delivers the extracted value on its output.

3.3.1 NMOS V_T Extractor

An input free NMOS V_T extractor is shown in figure 3.3. Transistors M1, M2, M3, M4 and M5 implement a Wang extractor circuit.

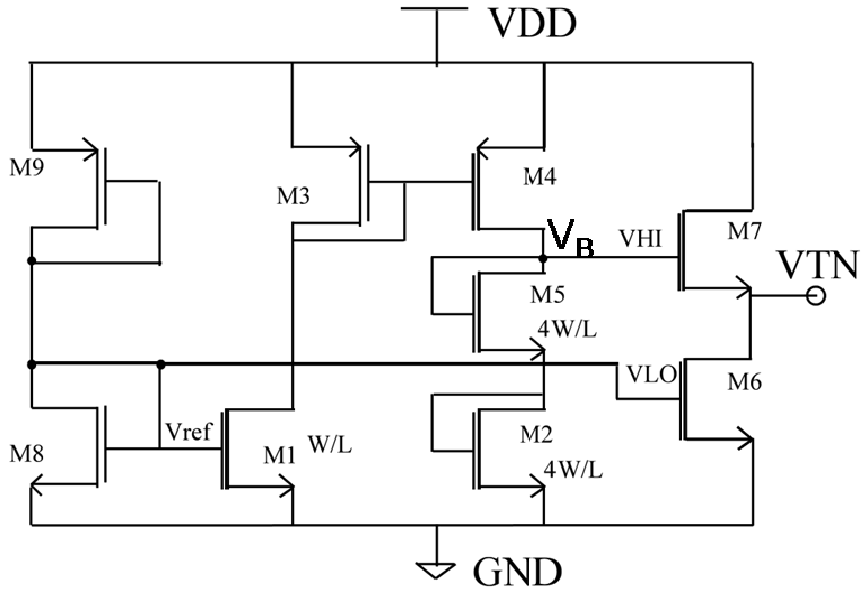


Figure 3.3: NMOS V_T extractor.

The sizes of M2 & M5 are four times of the M1. Since the sizes of both M3 and M4 are same, same current will be flowed through M1 & M2. On assuming M1 and M2 to operate in saturation and equating the current in both transistors, we get the following result.

$$(K / 2)(V_{ref} - V_T)^2 = 4(K / 2)(V_B / 2 - V_T)^2$$

$$V_B = V_T + V_{ref} \qquad (3.6)$$

Thus for extracting only the value of V_T, A differential amplifier is used which subtracts V_{ref} from V_B. Assume that the sizes of both M6 & M7 are identical and are in saturation. Since same current is flowed through both transistors, the gate to source voltage $V_{GS7}=V_{HI} - V_{TN}$, and $V_{GS6}=V_{LO}$ must also be identical. Thus the output put of this differential amplifier is the difference of V_{HI} and V_{LO}. i.e.

$$V_{TN}=V_{HI} - V_{LO} \qquad (3.7)$$

Since M7 is connected in a source-follower configuration, it is always saturated. Transistor M6 remains saturated if $V_{DS} > (V_{GS} - V_T)$ that is, if $V_{TN} > (V_{LO} - V_T)$. The constraints for saturated operation of both M6 and M7 are

$$V_{HI} > 2V_{LO} - V_T$$

$$V_{LO} > V_T$$

Transistors M8 and M9 provide a bias voltage (V_{ref}) on the gate of M1**.** This voltage is also applied to the V_{LO} terminal of the differential amplifier. Since this input free V_T extractor has no V_{ref}, it is a three-terminal circuit. The output (V_B) of Wang's V_T extractor is applied to the V_{HI} terminal of the differential amplifier. M6 and M7 perform the subtraction indicated in (3.6) and (3.7) so the output voltage (VTN) at the drain of M6 is the MOSFET threshold voltage (V_T).

3.3.2 PMOS V_T Extractor

The proposed input free PMOS V_T extractor is shown in figure 3.4 which directly extracts the threshold voltage of PMOS on its output. The size of M3 is four times of the M4. Since the sizes of both M1 and M2 are equal, same current will be flowed through M3 & M4. Transistors M9 and M10 are used for generating the reference voltage V_{ref}.

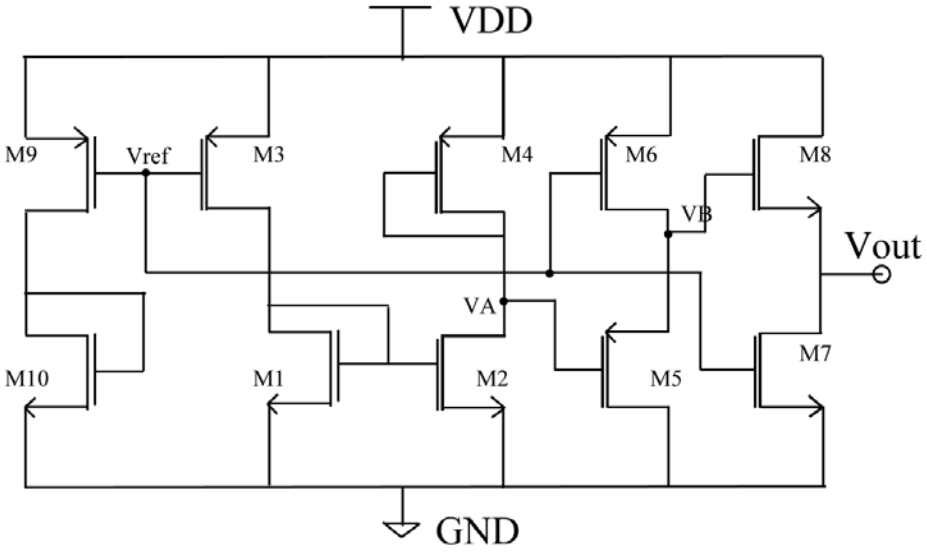


Figure 3.4: Proposed PMOS V_T extractor.

On assuming M1 and M2 to operate in saturation and equating the current in both transistors, we get the following result.

$$V_A = \sqrt{\frac{K_1}{K_2}} V_{ref} + (V_{DD} - |V_{TP}|)\left(1 - \sqrt{\frac{K_1}{K_2}}\right) \tag{3.8}$$

If $K_1 = 4\ K_2$, then equation (3.8) becomes

$$V_A = 2V_{ref} + (|V_{TP}| - V_{DD}) \quad (3.9)$$

For achieving the output voltage equal to |VTP|, two differential amplifier are used which simply subtract $(2V_{ref} - V_{DD})$ from V_A. Assume that the sizes of both M5 and M6 in PMOS differential pair are identical and are in saturation. Since same current is flowed through both transistors, the gate to source voltages must also be identical.

$$V_{ref} - V_{DD} = V_A - V_B$$
$$V_{ref} + |V_{TP}| = V_B \quad (3.10)$$

Similarly for NMOS differential pair, sizes of M7 and M8 are identical and both are in saturation. Then on equating the current in both transistors, we get

$$Vout = V_B - V_{ref} \quad (3.11)$$

From equation (3.10) and (3.11)

$$Vout = |V_{TP}| \quad (3.12)$$

Thus absolute value of PMOS threshold voltage $|V_{TP}|$ is directly extracted on output of PMOS V_T extractor.

3.4 Voltage Reference Circuit

For reducing the influence of temperature on ISFET characteristics, the ISFET should be biased at isothermal operating point. A new architecture for a precision CMOS voltage reference has been proposed and shown in figure 3.5 that can also be used in low power application. This voltage reference does not use any diodes or BJTs. Two linear voltages, one is the threshold voltage of P-MOSFET (V_{TP}) and the other is the N-MOSFET threshold voltage(V_{TN}), are combined to generate a reference voltage that is stable with temperature. The NMOS V_T extractor and PMOS V_T extractor are used for extracting V_{TN} and V_{TP}.

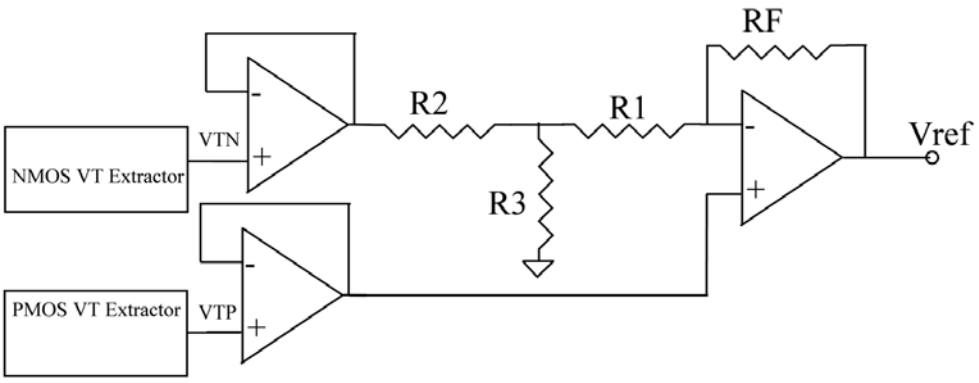


Figure 3.5: Temperature independent voltage reference using V_T extractors.

Both V_{TP} and V_{TN} have negative TCs but they are different in value. Hence, they can be subtracted with different weighting values to form a near zero-TC output voltage. An op-amp is used to form a subtractor circuit as shown in figure 3.5. The transfer function of this subtractor is

$$V_{ref} = \left(1 + \frac{R_F}{((R_2||R_3)+R_1)}\right) V_{TP} - \left(\frac{R_3||R_2||R_1}{R_2}\right)\left(\frac{R_F}{R_1}\right) V_{TN} \quad (3.13)$$

The coefficient R_2/R_3 is used to set the reference voltage to a desired level. The variable R_F/R_1 offers cancellation of temperature coefficient and provides temperature independent reference voltage.

3.5 Sensing Readout Circuit

In order to obtain a measuring signal, the ISFET has to be associated with an analog interface circuit. Zener-based bridge-type sensing circuit is not suitable for CMOS technology. All devices comprising an MOS device are made on a common substrate. In a standard CMOS technology, n-channel ISFETs are mostly used due to low drift and high mobility. In N-well CMOS technology, p-type substrate is globally and constantly grounded. In most of the existing readout techniques, such as Floating gate CVCC circuit, Pechstein's drain-output bridge-type sensing circuit the source of ISFET is not constantly biased, and is used as an internal node of the circuit, or a point of feedback

application and V_{BS} is not zero. The expression for the threshold voltage is modified to incorporate V_{BS} as follows:

$$V_T = V_{FB} + 2\Phi_B + \frac{\sqrt{2\varepsilon_{Si} \times q \times N_A \times (2\Phi_B + |V_{BS}|)}}{C_{OX}} \quad (3.14)$$

Where V_{FB} is the flat-band voltage, Φ_B is the bulk potential. V_{FB} contains terms, which reflect the interfaces between the liquid and the gate oxide, and the liquid and the reference electrode; which makes V_{FB} sensitive to the changes of pH. Terms Φ_B and Cox are assumed to be constant and uninfluenced by pH. This above expression shows the influence of V_{BS} on the value of V_T in integrated implementation of ISFET. The nonzero value of V_{BS} causes a change in V_T that is not due to the change of pH level. The error that occurs in case of body effect is significant, which limits the possibilities of source biasing in ISFET. Thus Gate feedback CIMP (complementary ISFET/MOSFET pair) design technique is the best choice for ISFET readout circuit in which body effect elimination is guaranteed. Figure 3.6 shows the schematic of an indirect feedback configuration of CIMP.

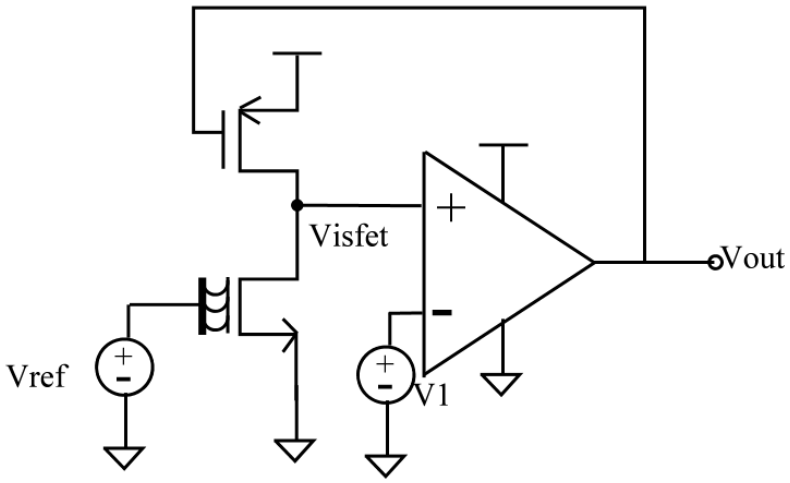


Figure 3.6: Sensing readout circuitry using indirect feedback gate CIMP.

In this reference electrode of N-ISFET is constantly biased with V_{ref} and the feedback is applied from output of op-amp to the gate of P-MOSFET. In this configuration, drain current is not constant, but V_{DS} does not change during the operation. The body effect elimination is also guaranteed. For operational analysis, this circuit can be represented by small-signal model as shown in figure 3.7. The parameters of amplifier and transistor at the saturation region are

$$g_0 = g_{ds} = I_d\lambda \tag{3.15}$$

$$g_m = \sqrt{2\beta \times |I_d| \times (1 + \lambda V_{ds})} \tag{3.16}$$

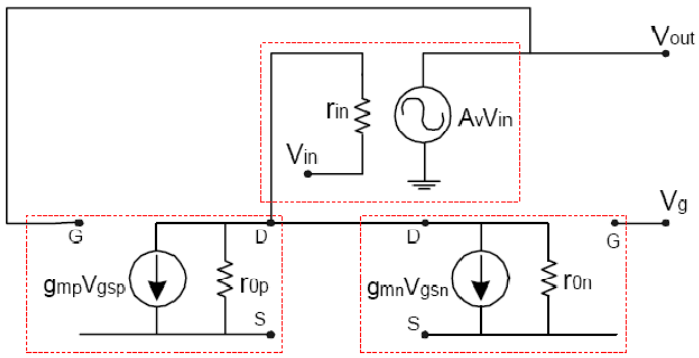


Figure 3.7: Small signal modal of Gate CIMP interface [10].

The threshold voltage (V_T) of ISFET is increased with increasing pH. As a result, drain current I_d decreases and trans-conductance g_0 also decreases. The voltage distribution in drain area changes and V_d falls. The input voltage V_{in} of op-amp increases. This causes a rising gate voltage V_g in the p-channel device. Due to this, there is a change in trans-conductance g_0, until the input node of operational amplifier adjusted to match the set point defined by V_1. The drain current I_d in saturation is expressed as follows:

$$I_d = \frac{\beta}{2} \times \left(V_{gs} - V_T\right)^2 \times (1 + \lambda V_{ds}) \tag{3.17}$$

Equation (3.17) can be rewritten as

$$I_{d_p} = a \times A_n \times \left(V_{g_p} - V_{s_p} - V_{T_p}\right)^2, \quad (3.18)$$

$$I_{d_n} = A_n \times \left(V_{g_n} - V_{s_n} - V_{T_n}\right)^2$$

Where constant A_n is defined for each device and depends on its dimensions and process parameters and it is given by

$$A_{(\lambda,\beta,V_{ds})} = \frac{\beta}{2} \times (1 + \lambda V_{ds}) \quad (3.19)$$

The ratio of p-channel and n-channel constants is defined by

$$a = \frac{A_{p(\lambda,\beta,V_{ds})}}{A_{n(\lambda,\beta,V_{ds})}} \quad (3.20)$$

Assuming an ideal amplifier with infinite input resistance ($r_{in} \rightarrow \infty$) the currents are equal, which as follows

$$I_{d_p} = I_{d_n}$$

$$\sqrt{a} \times \left(V_{g_p} - V_{s_p} - V_{T_p}\right) = \left(V_{g_n} - V_{s_n} - V_{T_n}\right) \quad (3.21)$$

The dependency of V_{g_p} on V_{T_n} can be described by

$$V_{g_p} = \frac{V_{g_n} - V_{s_n}}{\sqrt{a}} + V_{s_p} + V_{T_p} - \frac{V_{T_n}}{\sqrt{a}} \quad (3.22)$$

$$K_2 = \frac{V_{g_n} - V_{s_n}}{\sqrt{a}} + V_{s_p} + V_{T_p} = constant \quad (3.23)$$

$$V_{g_p} = K_2 - \frac{V_{T_n}}{\sqrt{a}} \quad (3.24)$$

Finally, the dependency of V_{out} on pH changes in saturation region can be described by the following expression

$$\Delta V_{out} = \Delta V_{g_p} = \frac{-\Delta V_{T_n}(pH)}{\sqrt{a}} \quad (3.25)$$

Thus shifting in threshold voltage of ISFET due to pH change can be directly read on the output of this circuit. The bias voltages V_1 and V_B are provided by Temperature independent Voltage Reference which was discussed in section 3.4.

3.6 Temperature Compensation Circuitry

The threshold voltage of ISFET V_{isfet} varies accordingly with the ph change or the ionic concentration of aqueous solution. Figure 3.8 gives the complete design of a temperature compensation circuit based on V_T extractor circuit. It consists of two blocks. In first block a scaling circuit is used to make the TC of V_T extractor equal to the TC of ISFET.

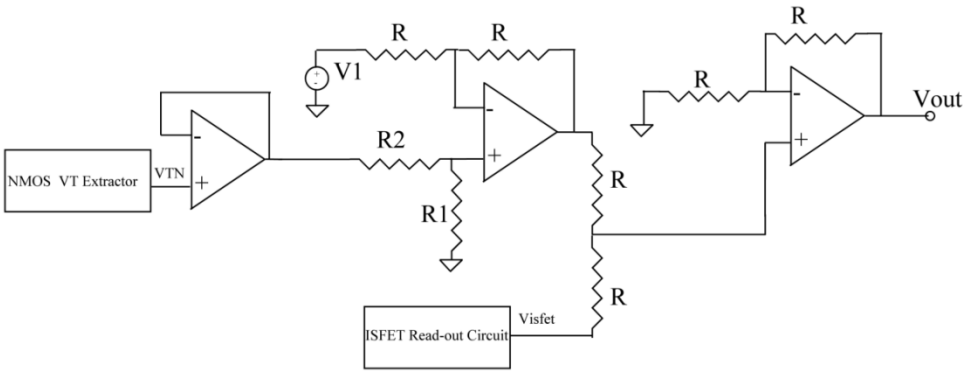


Figure 3.8: Temperature compensation circuitry using V_T extractor.

The V_{TNS} is the output of scaling block and it is given by

$$V_{TNS} = 2\left(\frac{R_1}{(R_1+R_2)}\right)V_{TN} - V_1 \tag{3.26}$$

For compensation, the value of R_2/ R_1 is calculated by using following relation

$$\frac{2}{\left(1+\frac{R_2}{R^1}\right)} = \frac{TC\ of\ ISFET}{TC\ of\ V_T\ Extractor} \tag{3.27}$$

Since the TC of ISFET is positive and the TC of V_{TNS} is negative but both have same magnitude of TC, a summing amplifier is used in second block which cancels out the positive TC of ISFET by the scaled TC of V_T extractor (V_{TNS}).

$$V_{out} = V_{TNS} + V_{isfet} \quad (3.28)$$

Thus a temperature independent output (V_{out}) is achieved using this temperature compensation circuit.

3.7 ROIC with Temperature Compensation Circuit

Figure 3.9 shows the complete schematic of ROIC with temperature compensation circuit. Voltage reference is used for providing isothermal biasing to read out circuitry.

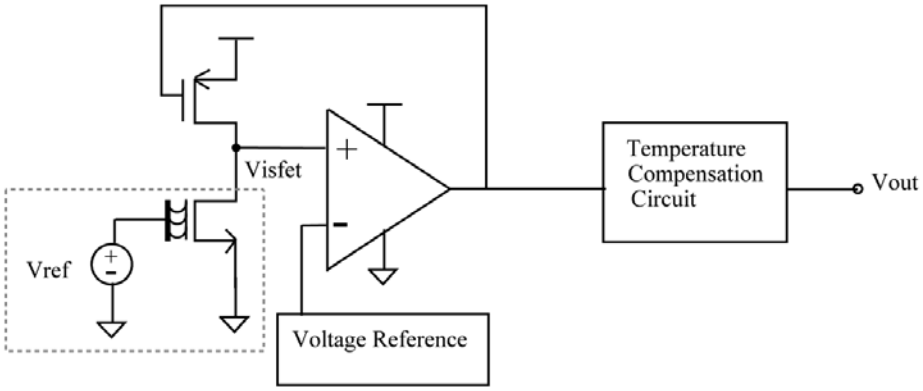


Figure 3.9: ROIC with temperature compensation circuitry.

3.8 Layout Design

Individual devices must be matched to get good response in analog circuit design. In fact almost all of the 'analog layout techniques' are actually methods for improving matching between different devices on a chip. Most analog circuit designs use a ratio based design technique (e.g. current mirrors) and thus matching is important. Some common techniques that help improve device matching are Multi-gate Finger Layout, use of dummy transistors.

3.8.1 NMOS VT Extractor

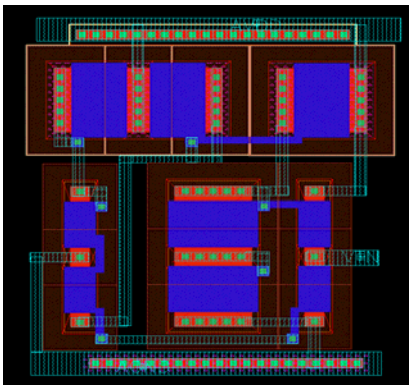


Figure 3.10: Layout of NMOS V_T extractor.

3.8.2 PMOS VT Extractor

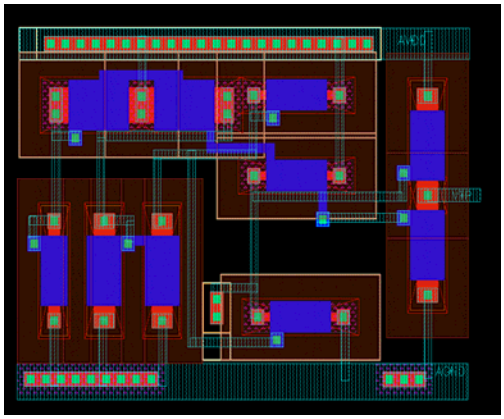


Figure 3.11: Layout of PMOS V_T extractor.

3.8.3 Two Stage Op-amp

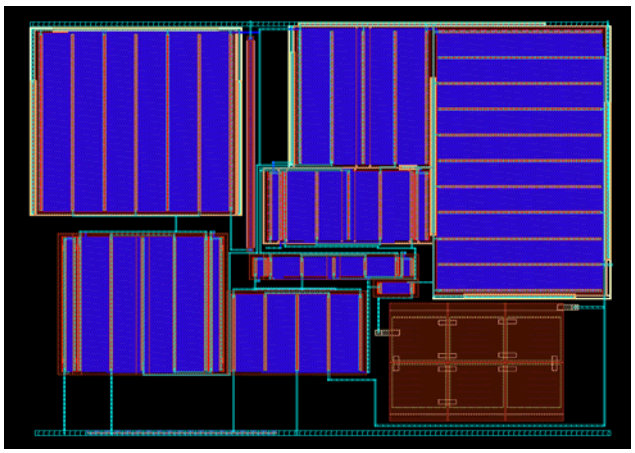


Figure 3.12: Layout of two stage op-amp.

3.8.4 Voltage Reference

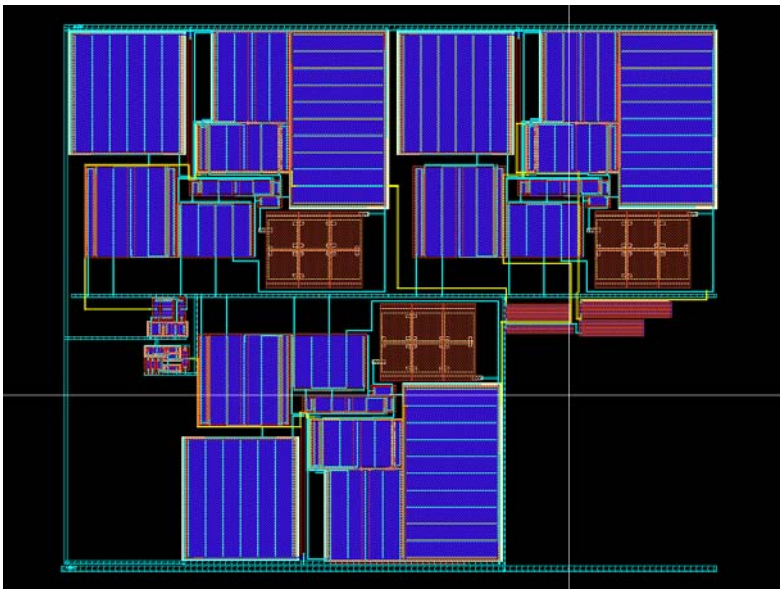


Figure 3.13: Layout of voltage reference circuit.

3.8.5 Temperature Compensation Circuit

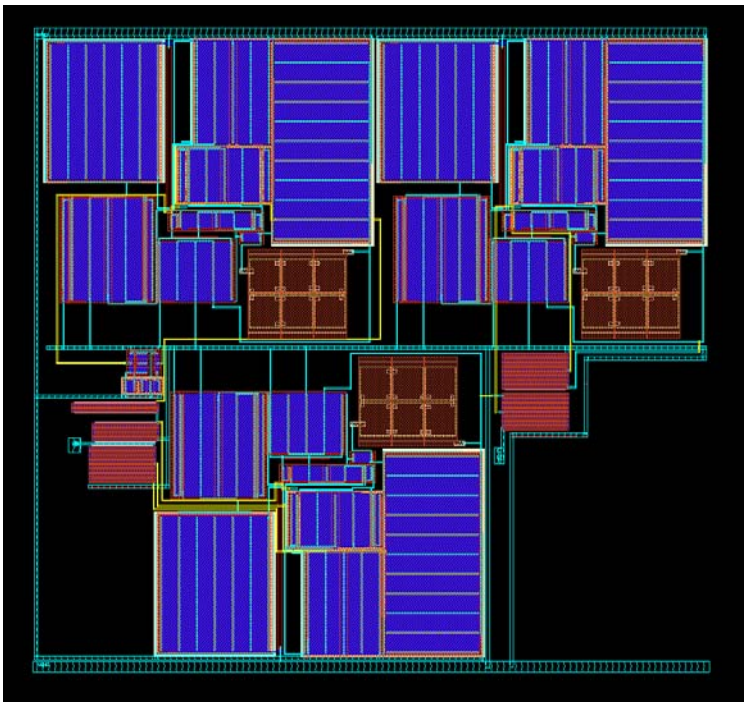


Figure 3.14: Layout of temperature compensation circuit.

3.8.6 Complete Layout of ROIC with Temperature Compensation Circuit

Figure 3.15 shows the layout of complete of ROIC with temperature compensation circuit. The doted rectangle in figure 3.9 is not included in it.

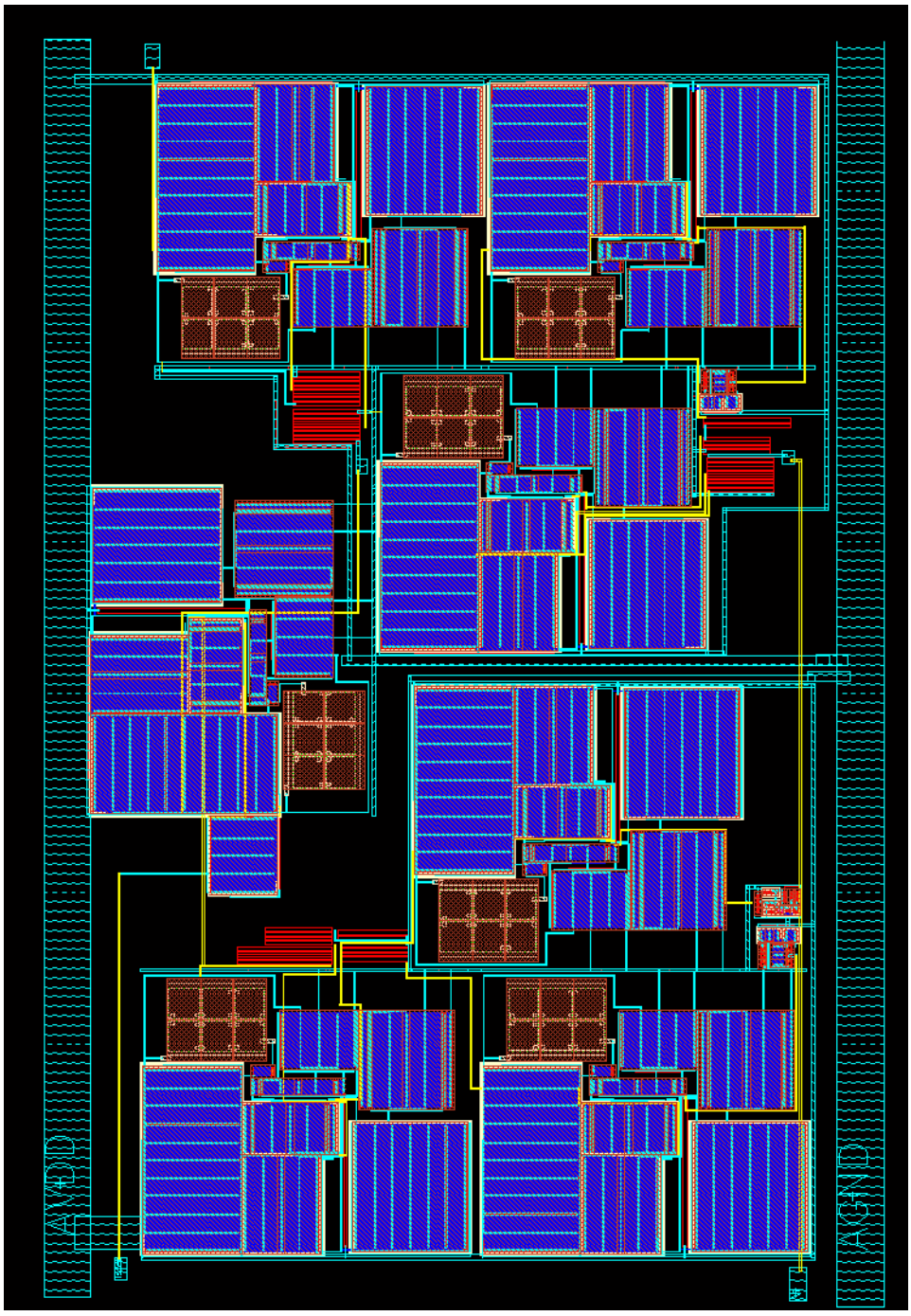


Figure 3.15: Layout of complete ROIC with temperature compensation circuit.

Chapter 4

Simulation Results

In this chapter the schematics and layouts of key components and building blocks discussed in last chapter, have been simulated for desired parameters with 3.3V power supply. Test simulations are performed using Spectre simulator.

4.1 Pre-Layout Simulation

4.1.1 NMOS V_T Extractor

The temperature variation response of input free NMOS V_T extractor is shown in figure 4.1.

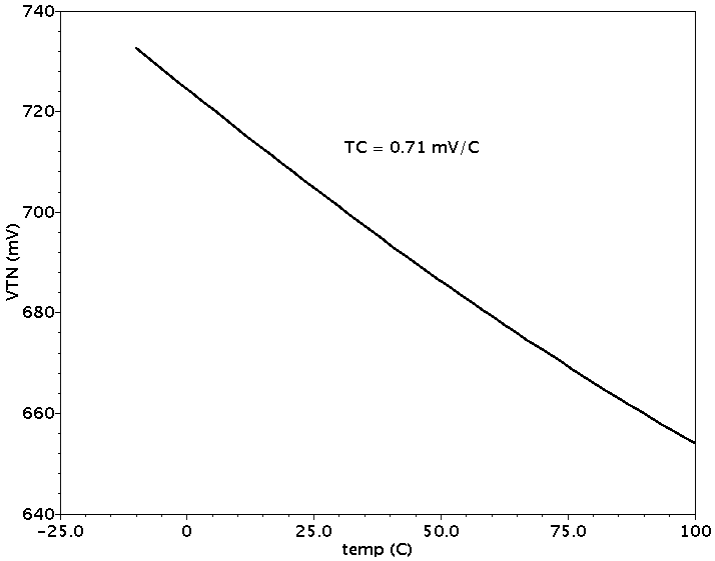


Figure 4.1 Measurement of temperature coefficient of NMOS V_T extractor.

The output of this V_T extractor displays linear and fast response to small changes in temperature with a negative TC of -0.71 mV/ ^{0}C for temperature range of -10 to 100^{0}C.

4.1.2 PMOS V_T Extractor

The temperature variation response of proposed PMOS VT extractor is shown in figure 4.2. It provides the PMOS threshold voltage 0.70V and its temperature coefficient is -0.15 mV/ ^{0}C for temperature range of -10 to 100^{0}C.

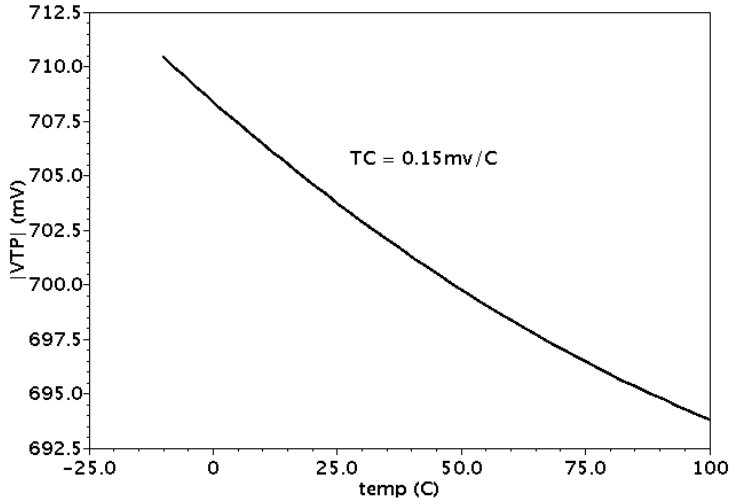


Figure 4.2 Measurement of temperature coefficient of PMOS V_T extractor.

4.1.3 Two Stage Op-amp

The simulations of two stage op-amp include AC response, Transient analysis, Common Mode Rejection Ratio and Input Common Mode Range.

4.1.3 .1 AC Response

This response is used for observing open loop gain, unity gain bandwidth (UGB), 3-dB bandwidth and phase margin of the circuit.

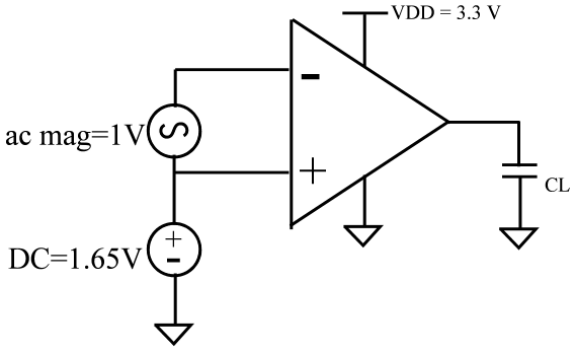


Figure 4.3: Test setup for AC response of the circuit.

In the test setup a differential AC signal of 1V is applied to the inputs along with the dc bias potential.

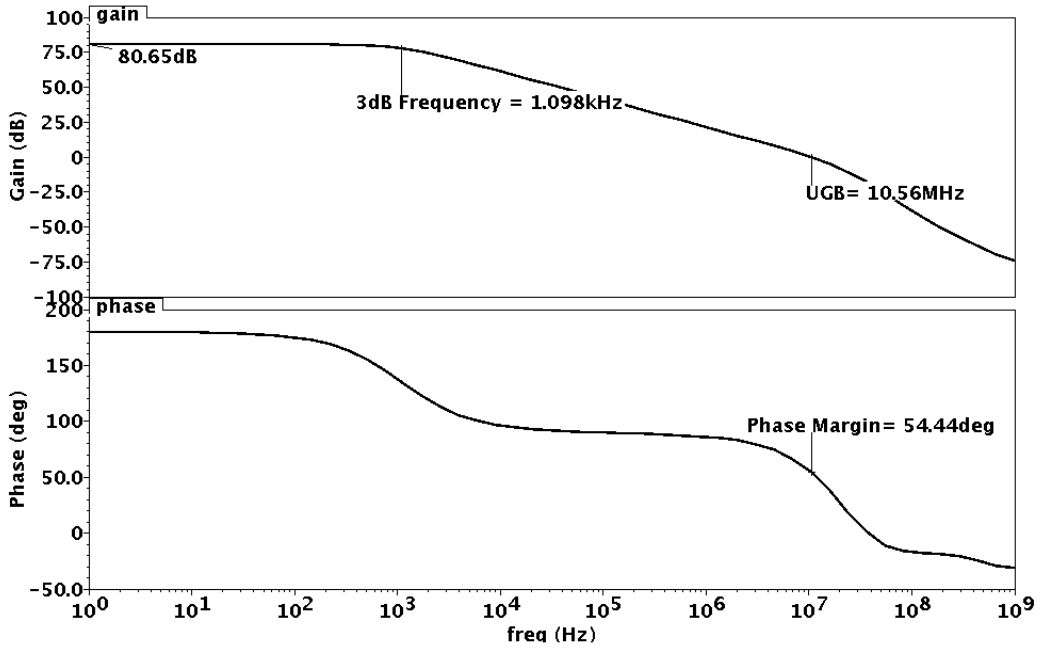


Figure 4.4: AC response of two stage op-amp

4.1.3.2 Transient Response

This response is used for observing slew rate and settling time of op-amp. In the test setup op-amp is used in unity gain configuration.

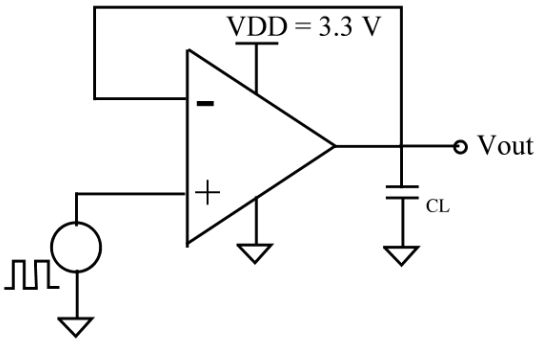


Figure 4.5: Test setup for transient response of the circuit.

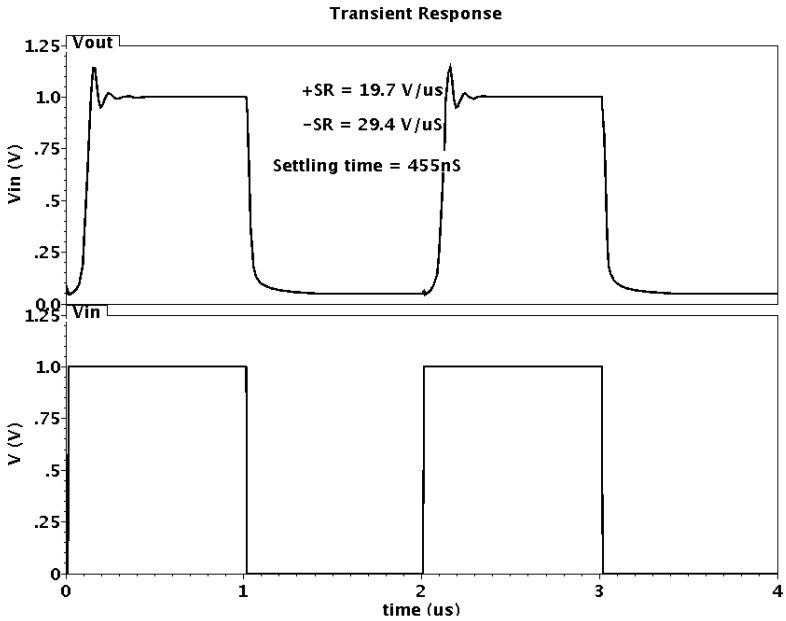


Figure 4.6: Transient response of two stage op-amp.

4.1.3.3 Common Mode Rejection Ratio (CMRR)

Before defining CMRR of the op-amp, we need to know the differential gain A_d(dB) as well as the common mode gain A_{CM}(dB) of the op-amp and the CMRR is obtained by A_d(dB)-A_{CM}(dB).

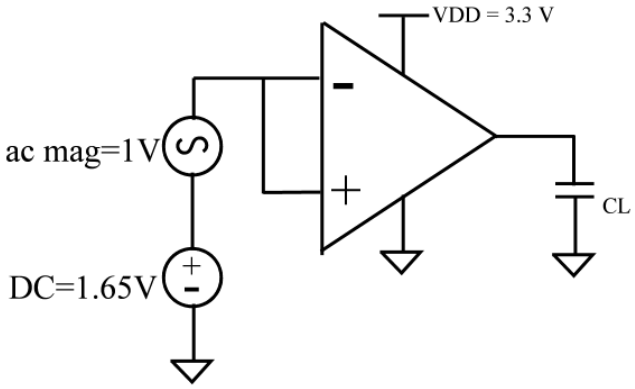


Figure 4.7: Test Setup for CMRR measurement.

The resulting CMRR response is shown in the figure 4.8.

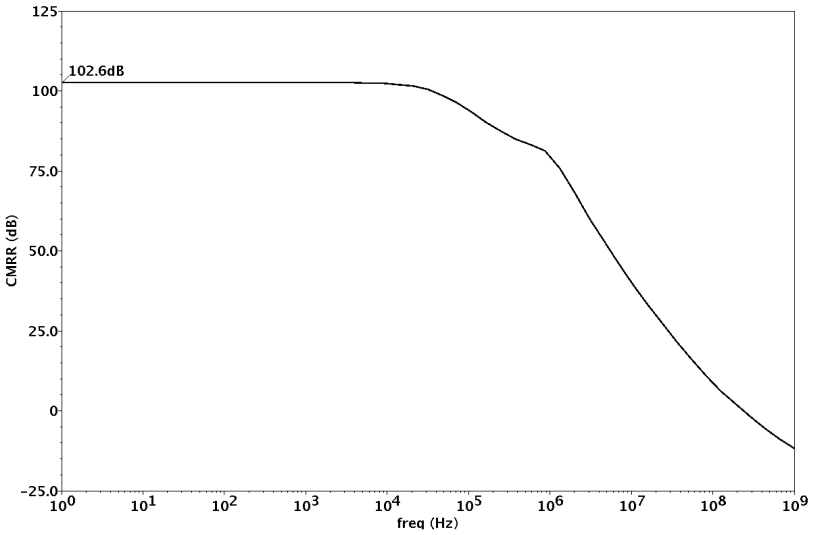


Figure 4.8: Measurement of CMRR.

4.1.3.4 Input Common Mode Range (ICMR)

This test is per formed to test the offset voltage and the input common mode range of the op-amp that is the range of op-amp for which there is a linear relationship between input and the output.

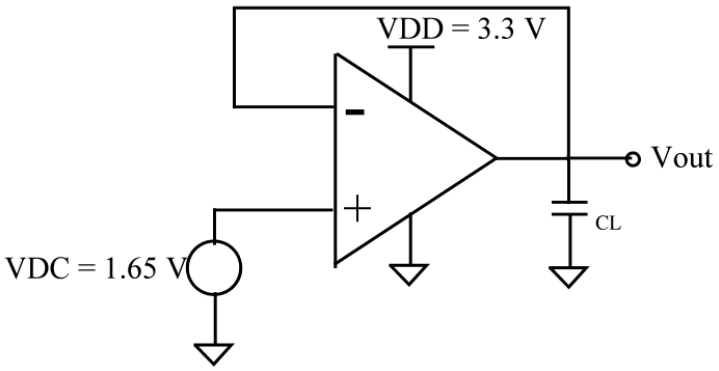


Figure 4.9: Test setup for ICMR.

The figure 4.9 shows the test set up for checking ICMR. The negative polarity output terminal is shorted with the inverting input terminal of the op-amp. A dc voltage source is applied at the non inverting terminal and a sweep is given to this voltage which results in a linear variation of output voltage. The output voltage varies linearly with input voltage

and bias transistor is in saturation region for a voltage range of 0.2V to 2.0V as shown in figure 4.10. This is called the ICMR range of op-amp.

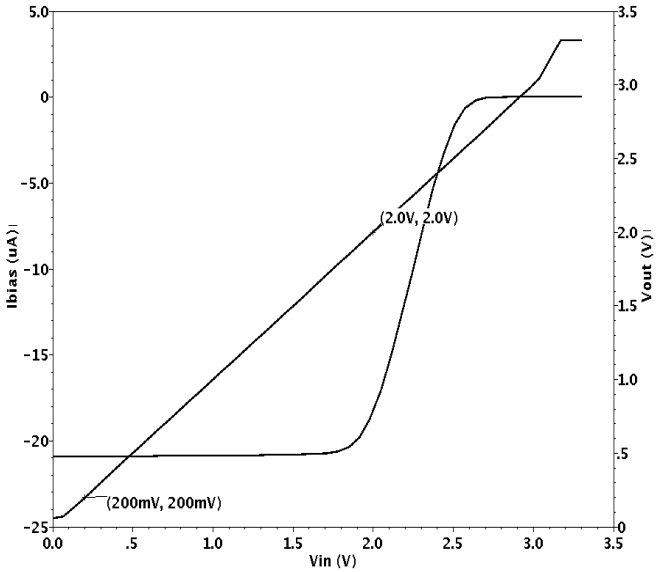


Figure 4.10: Measurement of ICMR.

An op-amp cannot be used outside the ICMR range because doing so will result in clipping of the signal.

4.1.4 Voltage Reference:

In the temperature independent voltage reference circuit, the values of R1 and R2 are fixed while the values of R3 and RF are changed according to the desired voltage levels. According to the TCs of NMOS VT extractor and PMOS VT extractor, the values of resistance for isothermal voltage reference of 1.2 V, 1V and 0.8 V have been given in Table 4.1.

Table 4.1: Value of resistances for different reference voltages

Vref (V)	R1 (K)	R2 (K)	R3 (K)	RF (K)	TCF (ppm/^{0} C)
1.2	10	10	5.3	14.6	45
1.0	10	10	7.1	10.3	54
0.8	10	10	15	5.5	69

The measured reference voltage of 1.2V as a function of temperature is shown in figure 4.11, demonstrating a TC of 45 ppm/^{0}C.

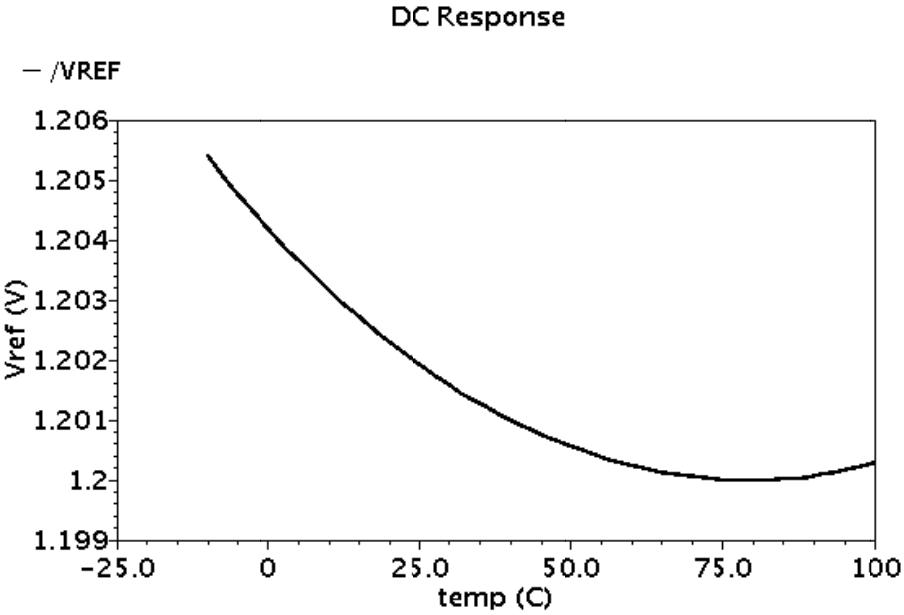


Figure 4.11: Temperature variation response of voltage reference for 1.2 V.

The temperature response of voltage reference for 1V and 0.8 are shown in figure 4.12.

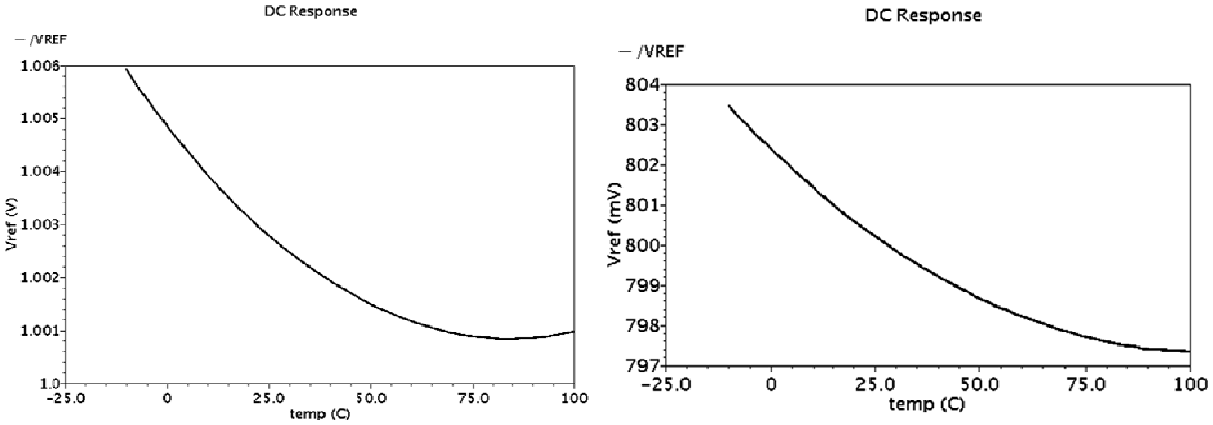


Figure 4.12: Temperature variation responses of voltage reference for 1.0V and 0.8 V.

4.1.5 Sensing Readout Circuit:

In order to verify the pH sensing performance of the designed ISFET system, a Verilog-A model of ISFET is used. The dimension of the ISFET is 400:20. The reference electrode

of ISFET has been biased at a fixed potential by using a voltage reference circuit. Simulated result in figure 4.13 shows good linearity between output voltage of sensing readout circuit with pH variation for the range of 1 to12.

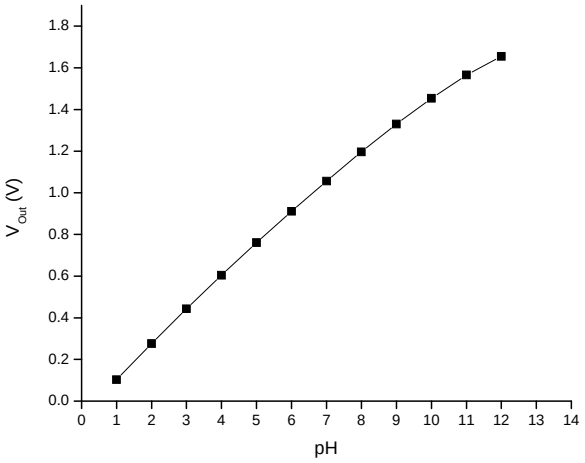


Figure 4.13: pH variation response of sensing readout circuit.

Figure 4.14 shows the output voltage of sensing readout circuit for pH= 4 and for pH=7 over a temperature range of -10 to 100 ^{0}C.

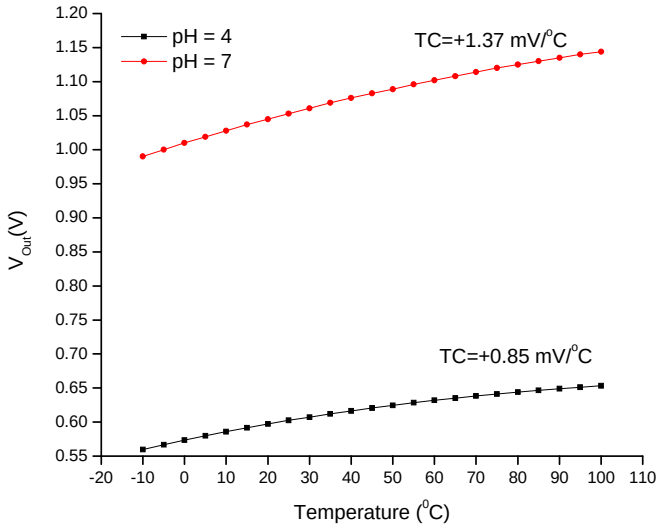


Figure 4.14: Temperature variation effect of sensing readout circuit without temperature compensation.

The values of temperature coefficient of ISFET are 0.85 mV/0C and 1.37 mV/^{0}C respectively for pH= 4 and for pH=7.

4.3 Temperature Compensation Circuit

The test results of sensing readout circuit in figure 4.14 show a linear dependence between the pH sensitivity of ISFET. The measured V_T extractor output voltage shown in figure 4.1 displays linear and fast response to small changes in temperature called a negative TC of –0.78 mV/^{0}C. This dependence can be scaled by adjusting the voltage V_1 and resistor R3 for equalizing the negative TC of V_T extractor to positive TC of ISFET. Temperature independent characteristics has been obtained by taking R3= 6.68K and R3= 0.4K respectively for pH = 4 and for pH = 7 in figure 3.8.

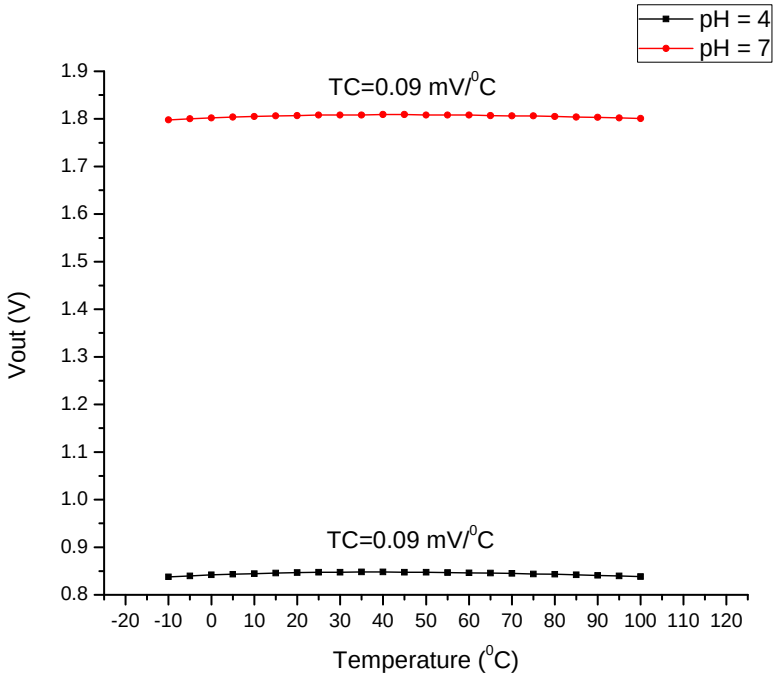


Figure 4.15: Temperature variation effect of sensing readout circuit with temperature compensation

The results shown in figure 4.15 demonstrate a very good compensation of temperature influence with the TC of 0.09mV/^{0}C.

4.2 Post-Layout Simulation

4.2.1 NMOS V_T Extractor

The output of this V_T extractor displays linear response to small changes in temperature with a negative TC of -0.71 mV/^{0}C for temperature range of -10 to 100^{0}C.

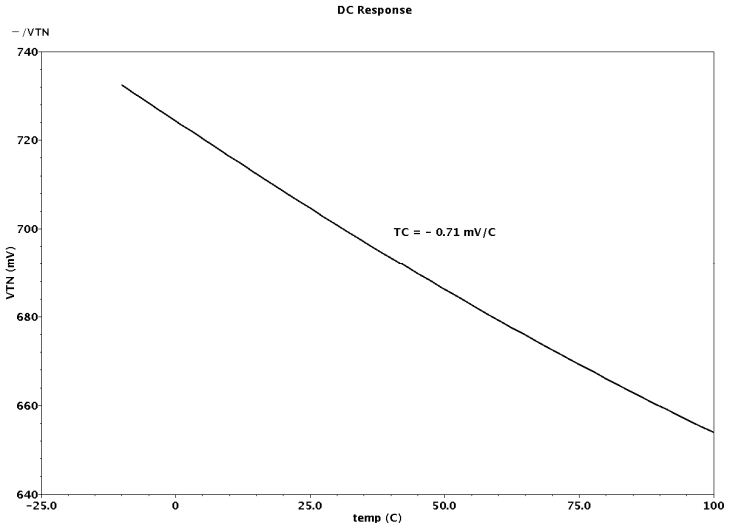


Figure 4.16 Temperature response of NMOS V_T extractor.

4.2.2 PMOS VT Extractor

The output of this V_T extractor displays linear response to small changes in temperature with a negative TC of -0.15 mV/^{0}C for temperature range of -10 to 100^{0}C.

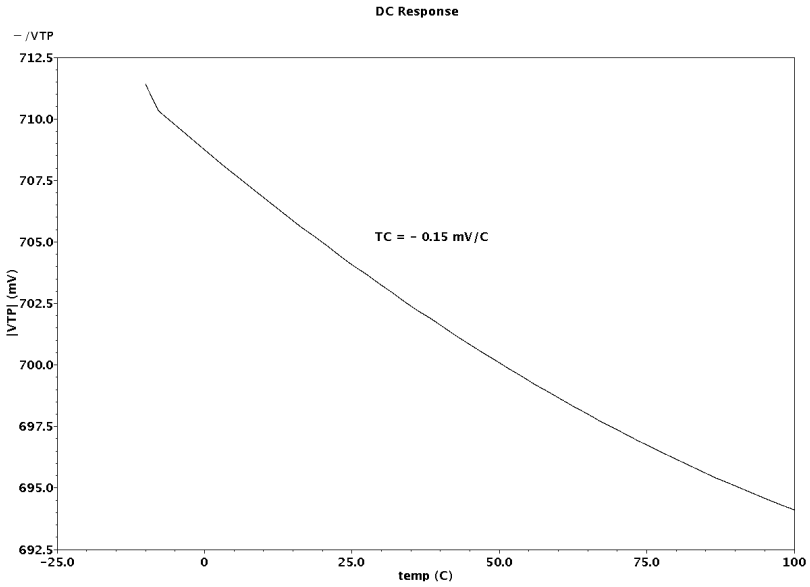


Figure 4.17 Temperature response of PMOS V_T extractor.

4.2.3 Two Stage Op-amp

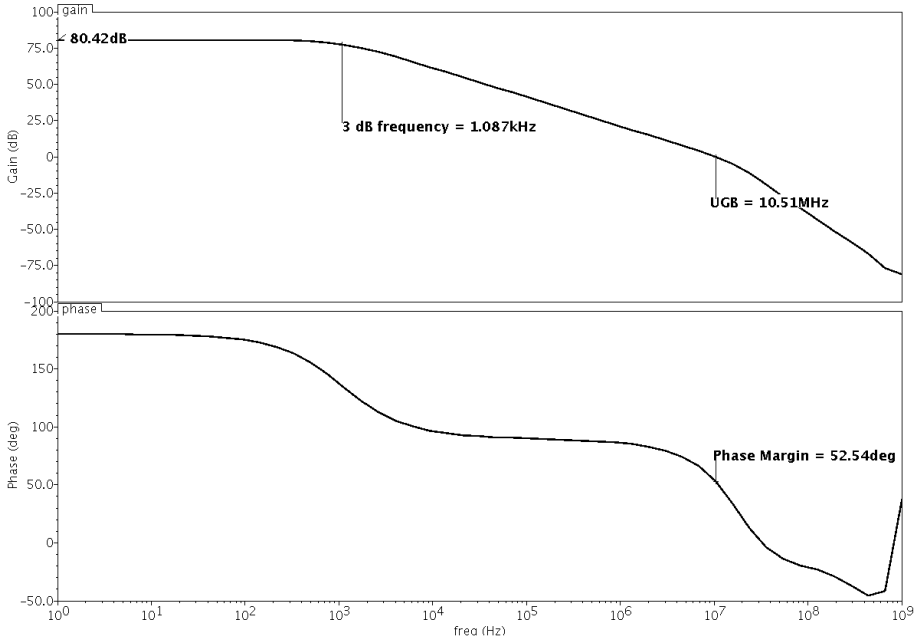


Figure 4.18: AC response of two stage op-amp.

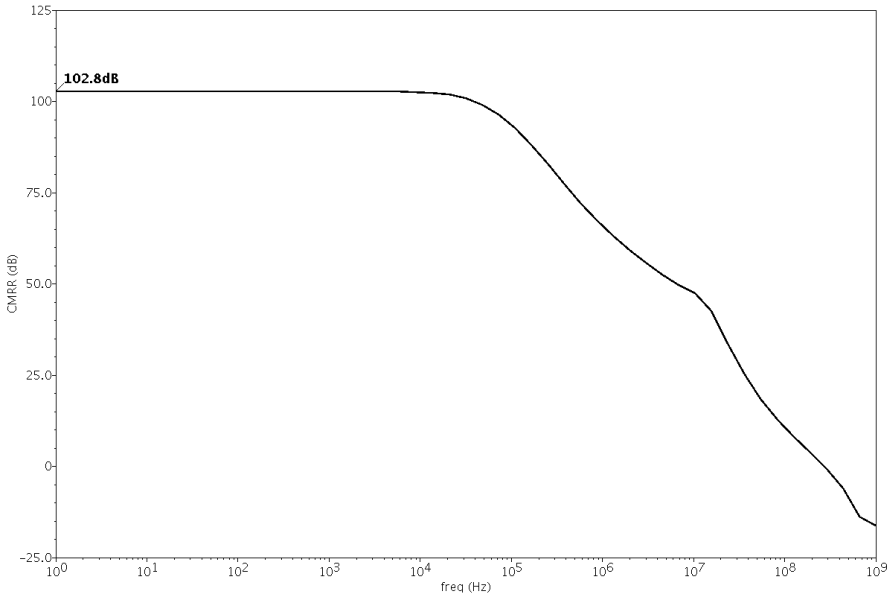


Figure 4.19: Measurement of CMRR.

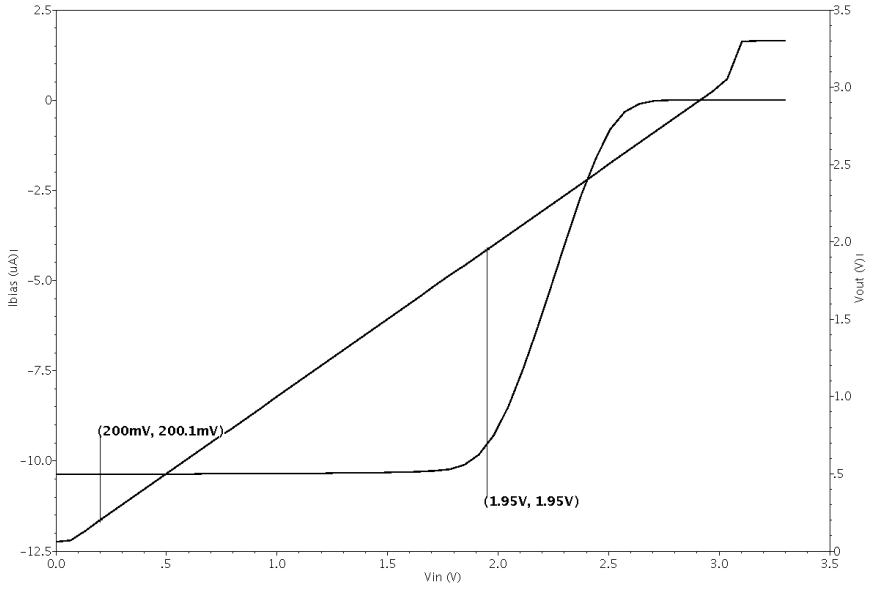


Figure 4.20: Measurement of ICMR.

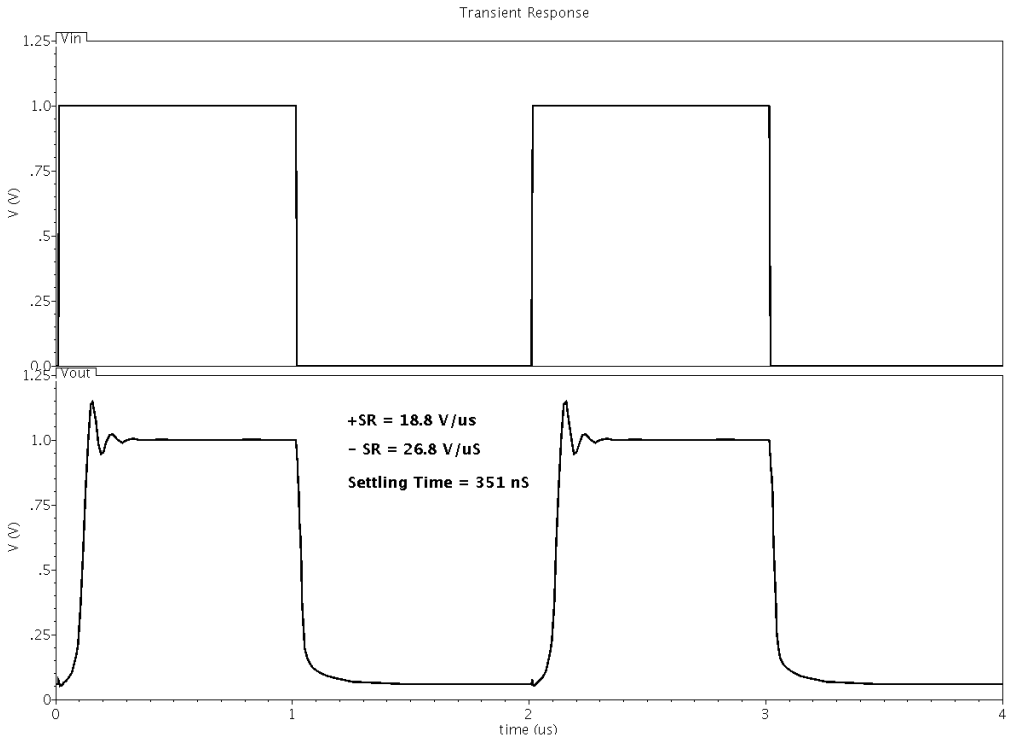


Figure 4.21: Transient response of two stage op-amp.

Table 4.2 summarized the measured performance parameter of two- stage op-amp for serving as a basic building block of the sensing readout circuit and temperature compensation circuit.

Table 4.2: Simulation results of two stage op-amp

Specifications	Target value	Pre layout Simulation	Post layout simulation
DC Gain	85 dB	80.6 dB	80.4 dB
Phase margin	60	54.4 deg	52.7 deg
Unity gain bandwidth	10 MHZ	10.5 MHZ	10.5 MHZ
ICMR	0.2V - 2.4V	0.22 – 2.0 V	0.22 – 1.9 V
CMRR	-	102.6dB	102.8 dB
Input offset voltage(systematic)	<1mV	8.9 µV	9 µV
Settling time (0.1%)	-	455 nS	452 nS
Slew rate	> 10V/ µS	19.7 V/µS (+ve) 29.4 V/µS (-ve)	18.8 V/ µS (+ve) 26.8 V/ µS (-ve)
Power Dissipation	500 µW	551.7 µW	547.3 µW
Load capacitance	1.5pF	1.5 pF	1.5pF
Power supply	3.3 V	3.3 V	3.3 V

4.2.4 Voltage Reference

In post layout simulation, the reference value has been varied by 0.9% from its desired value of 1.2 V as shown in Table 4.3.

Table 4.3: Simulation results of voltage reference circuit

Pre layout Simulation		Post layout Simulation	
Vref	TCF	Vref	TCF
1.2 V	45 ppm/^{0}C	1.21 V	39 ppm/^{0}C

The temperature variation of voltage reference is shown in figure 4.22.

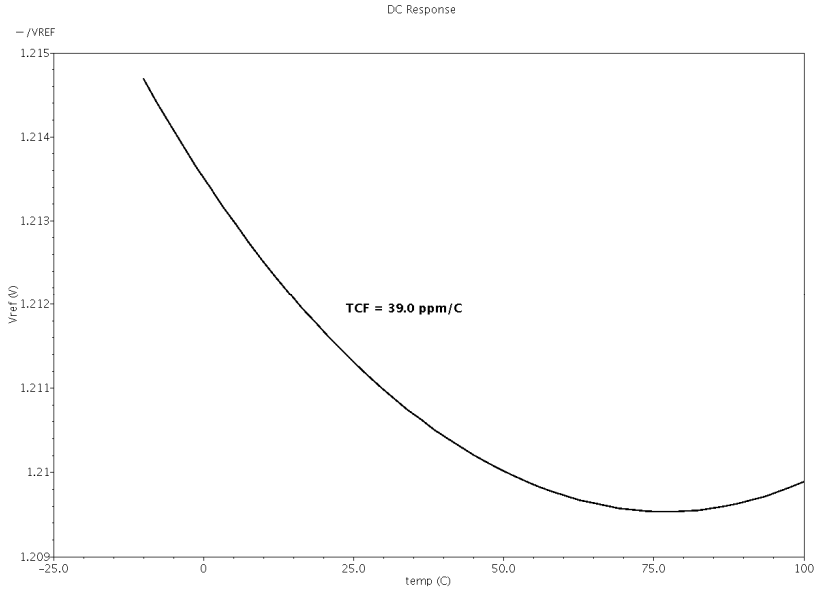


Figure 4.22: Temperature variation response of Voltage Reference for 1.2 V.

Chapter 5

Conclusion and Future Prospects

In this thesis work, a readout circuitry of ISFET based pH meter with temperature compensation has been designed in 0.18 μm CMOS technology using cadence tool. The electro-chemical stage of ISFET has been modeled using Verilog–A and thereafter electronic stage (MOSFET) is interfaced with it for achieving a complete model of ISFET. The sensing readout circuitry for ISFET based pH meter has been successfully designed for pH range of 1 to 12. The temperature coefficient of NMOS V_T extractor is - 0.71mV/^{0}C. A proposed input free PMOS V_T extractor has been designed which has temperature coefficient of - 0.15mV/^{0}C. A two stage op-amp which is a key component in both readout circuit and temperature compensation circuit has been implemented with gain of 80 dB. The temperature compensation circuitry has been designed using NMOS V_T extractor, which reduces the ISFET temperature coefficient to 0.09mV/^{0}C for the temperature range of -10^{0}C to 100^{0}C. For providing isothermal biasing to sensing readout circuit and temperature compensation circuit, a new voltage reference circuit has been successfully designed by using NMOS V_T extractor and PMOS V_T extractor. The layout of whole ROIC with temperature compensation has been designed using Virtuoso platform (Cadence) in 0.18 μm N-well CMOS process.

Due to the electro-chemical nature of ISFET, there is still a need to implement an accurate temperature dependent model for ISFET. The sensing readout circuitry can be modified for reading pH value from 0 to 14. This whole ROIC can be implemented with low supply voltage for reducing power consumption.

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Appendix

Verilog – A model of ISFET

Following is the Verilog-A code for electro-chemical stage of ISFET.

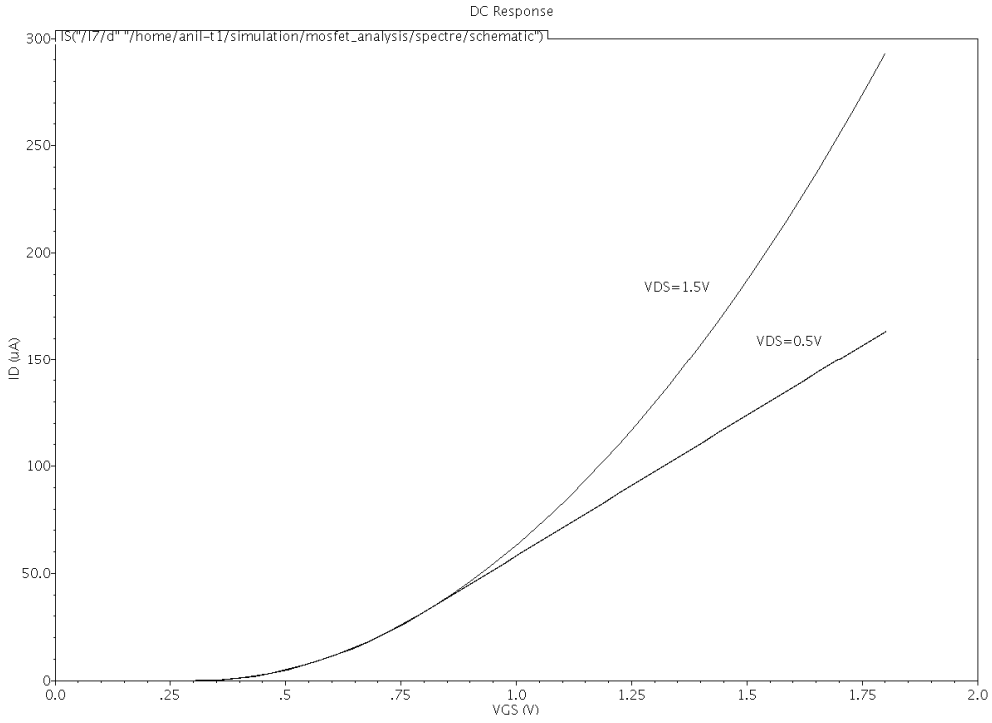
```
// VerilogA for verilog_models, ISFET, veriloga
`include "constants.vams"
`include "disciplines.vams"

module ISFET(ref,gm,ph);
        inout ref,gm,ph;
        electrical ref,gm,ph;
        real EPH;
        real T;
        electrical node;
        // PARAMETERS FOR ISFET
        parameter real  NAv     =  6.023E26; //Avogadros constant(1/MOLE)
        // ISFET geometrical parameters
        parameter real DIHP =0.1E-9;
        parameter real DOHP =0.3E-9;
        //ISFET electrochemical parameters
        parameter real KA = 15.8;
        parameter real KB = 63.1E-9;
        parameter real KN = 1E-10;
        parameter real Nsil = 3.0E+18;
        parameter real Nnit = 2.0E+18;
        parameter real Cbulk = 0.1;
        parameter real epso = 8.85E-12;
        parameter real epsihp = 32;     //relative permittivity of the Inner Helmholtz layer
        parameter real epsohp = 32;    //relative permittivity of the Outer Helmholtz layer
        parameter real epsw   = 78.5; //relative permittivity of the bulk electrolyte solution

        //Reference-electrode electrochemical parameters
        parameter real Eabs = 4.7;    //absolute potential of the standard hydrogen
electrode
        parameter real Erel = 0.2;
        parameter real Phim = 4.7;   //work function of the metal back contact
        parameter  real Philj = 1E-3; //liquid-junction potential difference between the ref
                                        solution and the electrolyte
        parameter real Chieo = 3E-3; //surface dipole potential
        real ET; //THERMAL COFFICIENT
        real sq;
```

```
        real CH,CD,CEQ,CB;
        real Eref;
        electrical x,y;

        analog begin
                T= $temperature;
                ET= (`P_Q /(`P_K * T));
                sq = sqrt(8*`P_EPS0*epsw*`P_K * T);
                CB = (NAv*Cbulk);
                CH = ((`P_EPS0*epsihp*epsohp) / (epsohp*DIHP + epsihp*DOHP));
                CD = (sq*ET*0.5)*sqrt(CB);
                CEQ = 1/(1/CD + 1/CH);
                V(ref,node) <+ Eabs - Phim - Erel + Chieo + Philj;
                Eref = V(ref,node);
                V(x)<+ log(KA*KB)+4.6*V(ph);
                V(y)<+ log(KA)+2.3*V(ph);
                V(gm,node) <+ (`P_Q / CEQ) * (Nsil * ((limexp(-2 * V(gm,node) * ET) –
limexp          (V(x))) / (limexp(-2 * V(gm,node) * ET) + limexp(V(y)) * limexp(-1 * V
                (gm,node)*ET) + limexp(V(x)))) + Nnit*((limexp(-1 * V(gm,node)*ET)) /
        (limexp(-1 * V(gm,node)*ET) + (KN/KA) * limexp(V(y)))));
        end
        capacitor #(.c(CEQ)) Cq(node,gm);
        resistor #(.r(1G)) RP1(x,gnd);
        resistor #(.r(1G)) RP2(y,gnd);
        resistor #(.r(1k)) RPH(ph,gnd);
endmodule
```

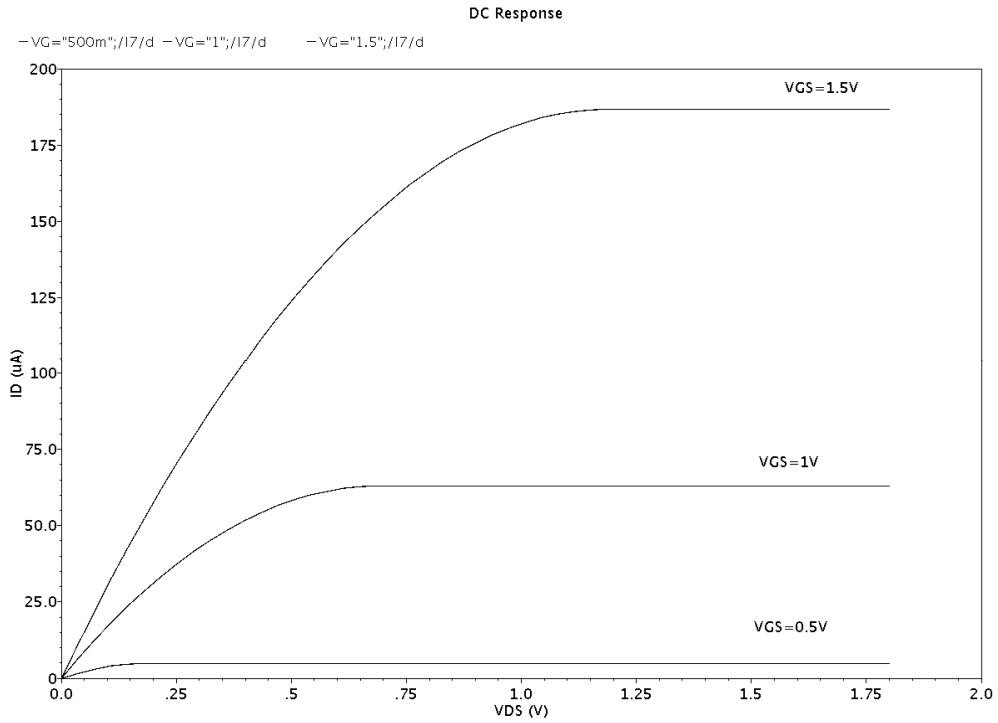
MOSFET level-1 Verilog-A model

```
// VerilogA for verilog_models, mosfet, veriloga
`include "constants.vams"
`include "disciplines.vams"

module mosfet(d,g,s,b);
        inout d, g, s, b;
        electrical d, g, s, b;
        real VG,VS, VD,VB,VGS,VDS,VOV;
        real beta, Id;
        parameter real L      =  10E-6  from[0.0:inf];
        parameter real W      =  10E-6  from[0.0:inf];
        parameter real VTO    =  0.3075    from[0.0:inf];
        parameter real KP     =  262.76E-6   from[0.0:inf];

        analog begin
                VG = V(g); VS = V(s); VD = V(d);VB = V(b);
                VGS= V(g) - V(s);
```

```
                VDS= V(d) - V(s);
                VOV = VGS - VTO;
                beta = KP * (W/L)/2;
                if (VGS < VTO)
                        I(d,s) <+ 0;
                else begin
                        if (VDS < VOV)
                                I(d,s)<+ beta * (2*(VOV)*VDS -(VDS*VDS));
                        else
                                I(d,s)<+ beta * (VOV * VOV);
                end
                Id = I(d,s);
        end
endmodule
```



I_D vs V_{GS} characteristics MOSFET.



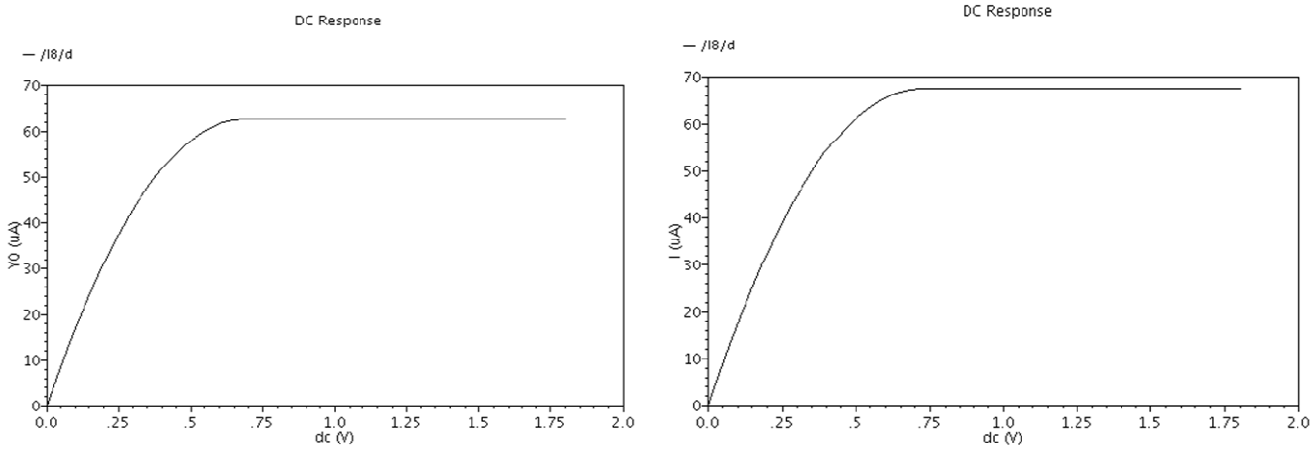
I_D vs V_{DS} characteristics MOSFET.

MOSFET level-2Verilog-A model

In this the temperature dependency for threshold voltage of MOSFET is also modeled. Since the temperature coefficient of threshold voltage is negative, drain current will be increased, as temperature is increased at same VDS and VGS.

```
/ VerilogA for verilog_models, mosfet, veriloga
`include "constants.vams"
`include "disciplines.vams"

module mosfet(d,g,s,b);
        inout d, g, s, b;
        electrical d, g, s, b;
        real VG,VS, VD,VB,VGS,VDS,VOV;
        real beta, Id,VT;
        parameter real L      =  10E-6  from[0.0:inf];
        parameter real W      =  10E-6  from[0.0:inf];
        parameter real Tnom = 300 from[0.0:inf]; // Room temperature  [K]
        parameter real Vtnom  =  307.5E-3  from[0.0:inf]; // Threshold voltage at Tnom
[V]
        parameter real Xn =1.0E-3;
        parameter real KP     =  262.76E-6   from[0.0:inf];
```

```
        real T; //parameter extraction temperature[K]
        analog begin
                T = $temperature;
                VT = Vtnom - ((T - Tnom)* Xn); //Temperature dependency of threshold
voltage
                VG = V(g); VS = V(s); VD = V(d);VB = V(b);
                VGS= V(g) - V(s);
                VDS= V(d) - V(s);
                VOV = VGS - VT;
                beta = KP * (W/L)/2;
                 if (VGS < VT)
                        I(d,s) <+ 0;
                else begin
                        if (VDS < VOV)
                        I(d,s)<+ beta * (2*(VOV)*VDS -(VDS*VDS));
                else
                        I(d,s)<+ beta * (VOV * VOV);
                end
                Id = I(d,s);
        end
endmodule
```



(a) (b)

I_D vs V_{DS} characteristic (a) at 27^0C (a) at 50^0C.