"Analytical Drain Current Model of Fully Depleted Silicon-On-Insulator MOSFET with Back-gate control"

Dissertation

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Submitted By

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DECLARATION

I, **Anjali Kumari Gupta** hereby declare that the work presented in this thesis entitled "**Analytical Drain Current Model of Fully Depleted Silicon-On-Insulator MOSFET with Back-gate control**" in fulfillment of the requirement for the award of degree of Master of Technology submitted at Electronics and Communication Engineering Department , Thapar University, Patiala is an authentic record of work carried out under supervision of Mr. Arun Kumar Chatterjee, Assistant professor, ECED, Thapar University from 2015 to 2017. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

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It is certified that the above statement made by the candidate is correct to the best of my knowledge and belief

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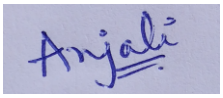

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ABSTRACT

SOI (Silicon-On-Insulator) technology has been acquiring a bundle of alertness and exercise in the integrated chip, and the portent of CMOS technology from a long decade while offering the superior performance with enhanced speed of operation and lowering the SCEs for sub-micron devices application in electronic industries. Recently, studies engross their concentration on Fully Depleted (FD) - SOI device due to their higher scalability relative to CMOS bulk technology and various new structures based on engineering techniques have been proposed. One of them is to design the model of an FDSOI with high k-dielectric material and with metal gate technology came into limelight for enhancing high drive current ratio.

In this thesis, firstly on the basis of device physics the value of surface potential, threshold voltage and Electric field for an asymmetrical FDSOI MOSFET is derived by using 2-D Poisson equations, then by using charge-sheet based model the drain current for the device has evaluated. The model discussed the device operation of back-gate controlling the threshold voltage of the front-gate for all the region of operations that is Accumulation, Depletion or Inversion, and also the influence of buried oxide thickness, doping concentration on threshold voltage with respect to back-gate biasing has depicted. Then transfer characteristics have been examined while varying the back-gate voltage at different Drain-voltage and buried-Oxide Thickness. Simulation of the device has been performed using TCAD Co-genda tool. Results of an Analytical Model have reflected the similar agreement when compared with published and simulation results.

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LIST OF ABBREVIATIONS

MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IC	Integrated Circuits
ITRS	International Technology Roadmap for Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
SCEs	Short-Channel Effects
DIBL	Drain-Induced Barrier Lowering
SOI	Silicon-On-Insulator
PDSOI	Partially Depleted Silicon-On-Insulator
FDSOI	Fully Depleted Silicon-On-Insulator
UTB	Ultrathin Body
BOX	Buried Oxide Layer
FET	Field-Effect Transistor
BP	Backplane
B-B Tunneling	Band to Band Tunneling

Chapter 1
INTRODUCTION

1.1 REVIEW

The integrated circuit is the essential element of semiconductor electronics, which mingles the fundamental elements on solitary semiconductor substrates – such as pn-Diode, Transistor like BJT and FET, Resistor, Capacitor(in units of Farads) and inductors. But the two vital electronic circuit's elements for silicon industry are transistors and memory devices. In certain applications now-a-days MOSFETs are also used. [1]

As envisaged by Moore's law, a magnificent exponential growth in the number of transistors per integrated circuit has foreseen by the semiconductor industry from several decades. According to the ITRS [2], the future technology inclination has been predicted in terms of physical dimensions and electrostatic limitations will entail the requirement of dimensional scaling of CMOS devices within the subsequent periods also the problem faced by the formal process and fabrication technologies of these devices. In order to entail with the device scaling in forthcoming future some of the new technologies have been proposed such as SOI, gate oxide which majorly includes high-k dielectric materials and Multi-gate MOSFETs. These technologies may require new fabrication methods so that these devices produced favorable device characteristics and device properties. [3] These nanoscale devices have a noteworthy perspective to transform the manufacturing and integration of electronic systems and scale further than the professed scaling restrictions of bulk CMOS.

1.2 REITERATE OF CMOS TECHNOLOGIES

Worldwide at the present time, a backbone of the semiconductor industry and a major component that modernize our life through an electronic application is Complementary Metal Oxide Semiconductor technology. From preceding decades the approach achievement in CMOS technology along with the measurable scalability is major concerns, which are achieved through Metal Oxide Semiconductor Field Effect Transistor, which is the essential edifice block of various application such as a microprocessor and various micro-electronic circuits.[4] But with the passage of time, the number of MOSFETs increases from millions to billions placed

simultaneously on the single chip in order to manufacture the microprocessor and other application circuits and fulfilling the purpose.

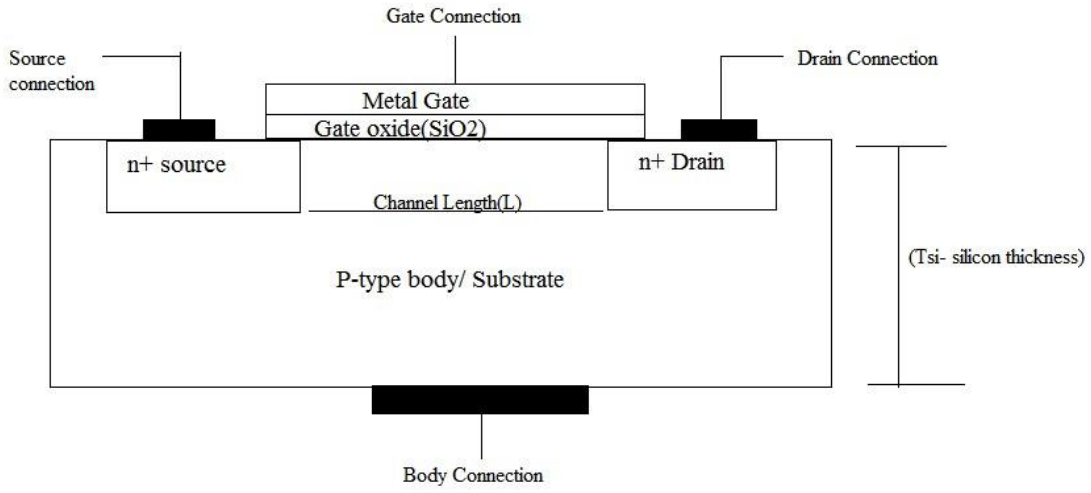

Figure 1.1 Representation of N-Channel MOSFET

As from figure1.1, of N-Channel MOSFET device which consists of source and drain which is n^+-type semiconductor regions respectively, and estranged by a substrate region which is of p-type semiconductor. On the other hand, a p-type MOSFET device is made up of with the opposite nature of doping in the source, drain and substrate regions respectively. Basically, the semiconductor material is considered as silicon but according to the requirements such as fast carrier transportation and another requirement, the semiconductor material may vary by the micro-electronics industry. A silicon dioxide, a thin layer of insulating material which is coated by a metal electrode is called a gate swathes the region align between the source and the drain. The insulator is named as the gate oxide. [5] Depending on the device nature whether it is NMOS or PMOS, in this case, NMOS is considered so basically the bias conditions are such that in which a drain comes into picture if the positive voltage is applied to it and the other two electrodes that are the source and the substrate are grounded. Under these conditions, where no voltage is applied to the gate electrode which results in the no current flow on the side sides of the device junction that is a drain-substrate junction and source-substrate junction. Therefore, the device acts as an open switch because there is no current flow between the source and the drain. On the other hand, if the large adequate positive voltage is pertained to the gate, forming a channel which is electron-rich underneath the oxide by 'spill out' an electron of the n-type

semiconductor source and drain regions. This continuous method of channel formation due to electron movements bridge between the source and drain allows the flow of current which turned on the transistor and act as a closed switch. Below the electron-rich channel layer is a hole region, have been revolted and flounce away when the positive voltage (+ve) is applied to gate terminal.

1.3 MOS SCALING THEORY

MOORE'S LAW: - It was the apprehension related to theory of scaling and its convention in practice which has made promising by the "Moore's Law" which depicted as a phenomenological scrutinization that reveals doubles of the transistor counts on IC in every two years[6] defined by G.Moore, as shown in Figure 1.2. It is perceptive that Law doesn't unrelenting forever. Conversely, certain predictions related to size and other design constrained, have verified to evade the most perceptive scientists. But the 'limit' of prediction has been miniaturizing approximately at the identical rate as the transistor size. Further technology scaling necessitates foremost changes in numerous areas, counting[7] as a) enhanced lithography procedures b) enhanced the transistor design with improved performance; c) voyage from bulk CMOS devices that are currently used to fresh material, structures, and technologies; d) improve radiation effects and enhance circuit sensitivity; e) improve the chip interconnects that is use of smaller wire connection in the circuits ; f) secure circuits; and g) convenient costs per chip; j) In order to maintain the scaling trends new dielectric with high k and different metals are introduced.

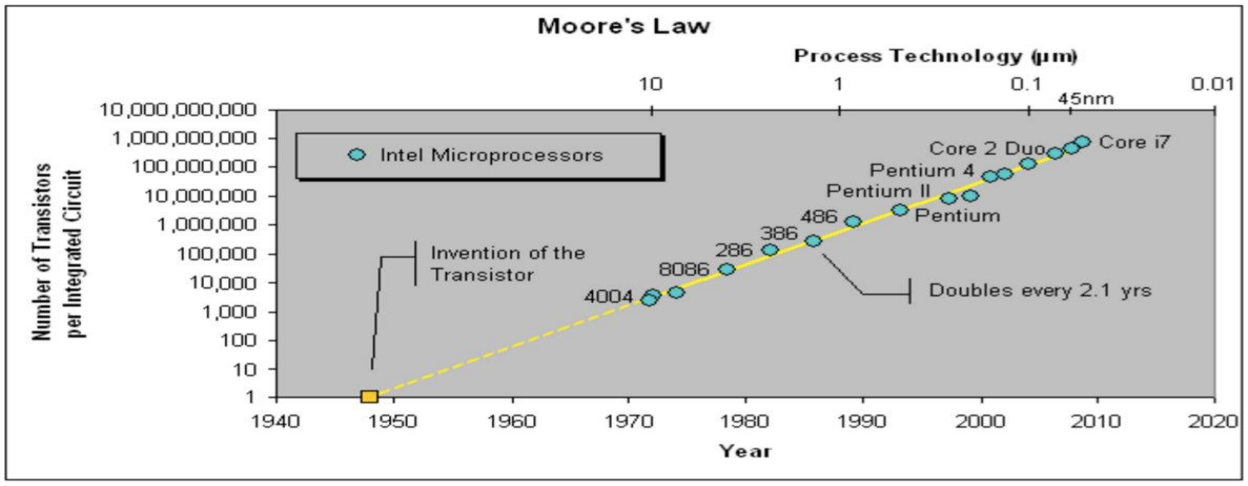

Figure 1.2 Moore's Law

1.4 NECESSITY FOR MOSFET SCALING

The main necessity is to involve billions of devices in a specified chip area makes the transistor smaller which results in a chip with the improved and same functionality. Also, the cost per IC is mainly correlated to the number of chips that can be produced per wafer, that in total makes the fabrication costs for a semiconductor wafer and generally it is relatively fixed. That's why, for plummeting the price per chip, smaller ICs allow more chips per wafer. In fact, once a new technology node has introduced the requirements of the number of the transistor have been doubled per chip in every 2-3 years. All these are the reason that facilitates the generation of smaller transistor now- a-days which are basically possible through scaling. [8]

1.4.1 Scaling

The Moore's law and the ITRS have been described some factor in order to scrutinize their role that includes scaling of transistors and also prominence the scaling's unparalleled aid to the massive advancement in the semiconductor industry. Without the unexpected transistor miniaturization, it might be unfeasible to fabricate a device that works at low power and have higher capacity. In order to maintain the scaling norm and from our previous review there are two types of scaling in general and their design rule (i) Constant- field scaling (ii) Generalized-field scaling. The basic principle implies about the improvements in the performance of a FET devices basically a MOSFET we must diminish transistor size by linear factor (k), together with the scaling of voltage and growing doping concentration while the electric field components as constant- hence the name constant field scaling [9] However, generally the scaling used the scaling of the parameters by scaling factor *K* Voltage, Physical dimensions (Length, Width) and doping Concentration.

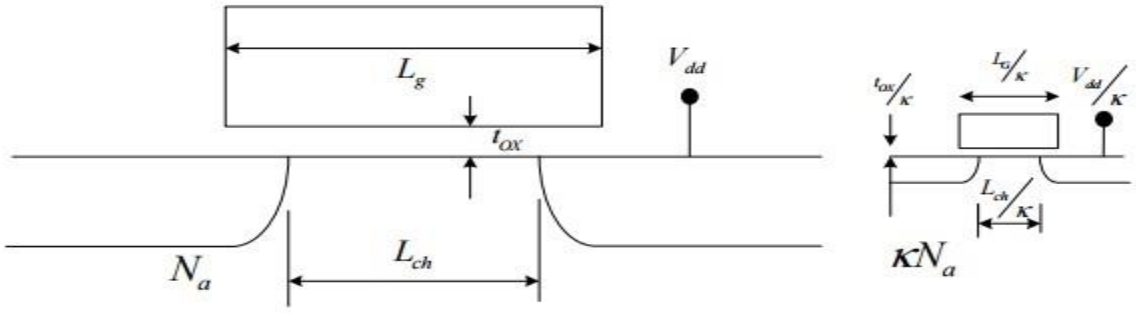

Figure 1.3 A Schematic of MOSFET Miniaturization and Presented a Scaled Device [10]

The scaled down device will have reduced the voltage (V_{dd}/k), vertical and horizontal dimension also reduced by scaling factor, while the doping concentration increased (kN_a) as shown in figure 1.3. But due to constant field scaling[10], there are a various advantage and shortcoming occurs in the device one of was the "ion implantation" that results during the fabrication of the device which is scaled. During fabrication the significant step is to precisely positioned the dopant in the shallower region of scaled devices such as S-D junction and channel and its shortcoming result in the carrier mobility degradation due to higher mobility in the channel and result of short channel effect due to reducing in V_T and the drawback on carrier mobility[11] result due to doping concentration as we know that the inverse relationship between the carrier mobility and the channel doping, which result in the squalor of scaled device performance.

1.4.2 Generalized Scaling rule

As the dimensions of the device penetrate in the sub-micron region, 2D effects become gradually noteworthy. The gradual field estimation turns out to be worthless and visualization in the change of field observers radically even if we fabricate the device by using the constant field scaling. As the gate length (L_g) of a MOSFET scaled more, the increase in the capacitive coupling of the channel potential to source and drain terminal with respect to the capacitive coupling to the gate terminal observes which indirectly resulting in the SCE, such as DIBL, threshold voltage roll-off, increase in the leakage current is approaching a rigorous apprehension that hinder the CMOS scaling that result in worsening of high performance technologies because of considerable submissive power consumption. These challenges of constant field scaling have been reported by two groups of researchers, who have coined the generalized scaling theory. According to the Brews [12] *et. al*., describe a minimum channel length parameter and retained the subthreshold characteristics of long channel devices in the scaled device based on the empirical formula as

$$L_{min} = A\left[x_j * t_{ox} * (W_{ms} + W_{md})^2\right]^{1/3} \qquad Eq(1.4.1)$$

Where A and t_{ox} is the constant proportionality constant and the oxide thickness respectively, L_{min} is the minimum value of channel length, W_{ms}, W_{md} is the depletion width of the source and drain respectively, x_j is the junction depth. The foremost advantages of generalized device scaling with respect to constant field scaling, that all the parameter is not scaled by one factor. The value of minimum channel length continuously reduced till we obtained the 10% increase in

the drain current. But only increase in drain current limit the short- channel effects but it predominantly determines by another parameter also channel length, oxide thickness, supply voltage, doping concentration, junction depth. The distinctive electrical feat of the SCE and DIBL chiefly depends on this parameter describe above and also shown by the equation [11][16]

$$SCE = 0.64\frac{\varepsilon_{si}}{\varepsilon_{ox}}\left(1+\frac{x_j^2}{L_{el}^2}\right)\frac{t_{ox}}{L_{el}}\frac{W_{dm}}{L_{el}}V_{bi} \qquad Eq(1.4.2)$$

$$DIBL = 0.80\frac{\varepsilon_{si}}{\varepsilon_{ox}}\left(1+\frac{x_j^2}{L_{el}^2}\right)\frac{t_{ox}}{L_{el}}\frac{W_{dm}}{L_{el}}V_{ds} \qquad Eq(1.4.3)$$

All these parameter $(L_g, N_a, t_{ox}, x_j, V_{dd})$[14] determines the EI of the scaled device, which further determines the values of SCE and DIBL. In the above equation the effective channel length is defined as $L_{el} = L_g - \Delta L$, where L_g is the gate length of the devices and the ΔL is the sub-diffusion length. From other researchers group, it was recommended that the physical dimension, doping concentration and supply voltages are scaled non-linearly by different factor and it provide the appropriate divergence between the field pattern obtained from the scaled and original device Baccarani[13] *et al*, and also other factors and techniques was described in their paper. Therefore, vigilant device blueprint is requisite so that the SCE effect was reduced. For bulk MOSFETs, a minimum L_g must be ~5*l*, where *l* is the characteristic length and is given by

$$l = 0.1\left(X_j T_{ox} T_{dep}^2\right) \qquad Eq(1.4.4)$$

Where X_j is junction depth, T_{ox} is the gate dielectric thickness and T_{dep} is the depletion depth of the channel generated in the device during operation. On the basis of previous studies these parameter must be scaled down together with respect to L_g to suppress the SCE in bulk MOSFETs. These expertise's of scaling work efficiently for numerous years, but as silicon technology enters into a scaled range that is in nanometer, elementary and practical restrictions hamper the scaling rule. Historically, after minimum channel length L_g another important factor is the gate dielectric thickness (t_{ox}) dimension inorder to enable the scaling of devices. Scaling the gate dielectric thickness upto to certain values, but after further reducing the dielectric thickness factor not only increase capacitive coupling of gate to channel but also increase the drive current(I_{on}). However, the gate dielectric thickness of SiO_2 is approaching the physical limits (<2nm) but beyond this limit it ensuing in increase of gate leakage current because of

tunneling of carrier transversely into the thin dielectric by quantum mechanical. Higher channel doping is required inorder to scale down T_{dep}. Far from the dielectric/channel interface the scale down in the dielectric thickness helps to eradicate leakage paths, beyond 100nm halo implant is mainly used to restrain the sub-leakage, and the average channel doping is increase, which leads to the demeans in mobility of carriers due to high vertical field while are others factor such as impurity scattering and B-B tunneling also become an important issue. Moreover as the X_j, channel junction depth scaled, the source/drain- channel coupling relative to the gate channel-coupling reduces, also results in the degradation of drive current of the devices due to increase in the parasitic resistance of source and drain junctions.

1.5 WHAT HAPPENS IN SCALED TRANSISTOR

By minimally scaling all the parameter, a number of physical effects can become pertinent as that is negligible in larger MOSFETs. These are:-

1.5.1 Drain-Induced Barrier Lowering (DIBL)

This consequence in the MOSFETs devices generally defines by the reduction in the threshold voltage with the increase in the drain voltages. In a long channel device the threshold voltage is independent on the drain voltages, but in short channel devices, the reduction in threshold voltage turns on the transistor prematurely, thus by lowering the barrier potential that surge the transfer of electrons from the source to the drain.

1.5.2 Velocity Saturation

As, the direct relationship between the electric field and the carrier velocity which results in the saturation of velocity at the higher electric field. This means that beyond the critical electric field carrier (electrons and holes) tends to alleviate their speed and eventually cannot move faster and is given by the approximation relation between the drift velocity and the electric field

$$v_d = \frac{\mu E}{1 + \frac{E}{E_c}} \qquad Eq(1.5.1)$$

Where μ is the carrier mobility, E is the electric field and E_c is the critical electric field (the point where the velocity gets saturate). When E>> E_c, $v_d$become equal to $\mu E = v_{dsat}$ and its value for electrons and holes in the Si are ~10^7 cm/s and ~0.6*10^7 cm/s respectively at temperature

$300K$ around $E_c = 10^5 V/_{cm}$. Drain current is restricted by velocity saturation as compared to pinch off region. It can only be happen in short channel devices when device aspect is diminish with no change in the drain bias.

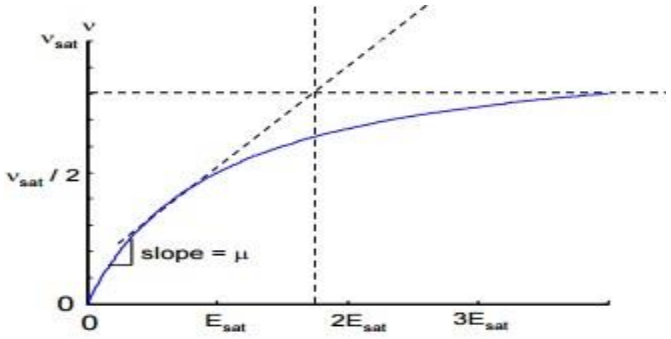

Figure 1.4 Carrier Velocity Saturation with Increasing Electric Field

1.5.3 Impact Ionization

This effect can be illustrated, due to the existence of a strong electric field in the lateral direction in short channel devices, it bestows the charge carrier with the elevated velocity, and consequently, high energy, the carrier with high energy spawns the "hot" carriers. These appear closely to the drain. .

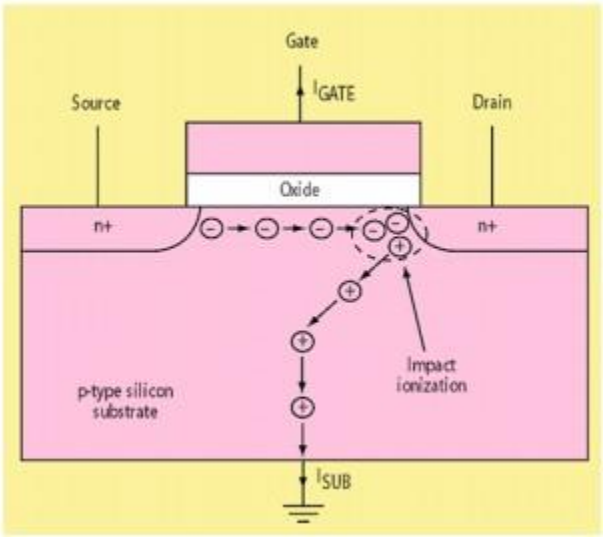

Figure 1.5 Illustration of Impact Ionization

Since these are a surge in the silicon lattice so, usually they have the affinity to collide with the atom of the structure. By obtaining enough energy, which conceded to the atom, upon collision

can thump out an electron from the VB to CB. This create the electron-hole pair by impact ionization, as hole generated is fascinated to the bulk and produce the parasitic substrate current and electron is moved to the drain. By this process, the source acts as emitter and drain is act as a collector by forming NPN transistor and bulk is act as a base. By long-lasting this process of generating the e-h pair due to high electric field and this newly generated electron act as the "hot" carrier that hammers out another atom of the lattice forming the avalanche effect which turns out the swamped current that the gate voltage can't manage as depicted in figure 1.5

1.5.4 Hot-Carrier Injection

The hot carrier elevated by the strong electric field has the adequate energy that gets enter in oxide and gets trapped in it. These trapped carriers amend the transistor retort in requisites of the gate voltage and amplify the threshold voltage and also accretion of an electron in the oxide might ground the "aging" of the transistor. This drawback can be improved by abate the electric field in the drain side so the generation of hot carriers is reduced which is possible by implanting the lightly doped drain along with the highly doped drain region and also to the source region of the MOSFET. As depletion regions of the lightly-doped implant are wider. With this, there is a larger expanse between diverse potentials, which trim down the electric field. However, another disadvantage that intensifying is an increase of parasitic resistance between the source and drain.

1.5.5 Surface Scattering

This effect worsens the current-voltage relationship of the transistor, as surface scattering occurs due to the zig-zag movement of the charge carriers due to the presence of an electric field that occurs due to the gate voltage applied to the transistor due to this the effective mobility reduces as compared to the bulk mobility.

1.5.6 Gate Oxide Charges

Due to the presence of high electric field observe in the channel become adequate, and it will energized the channel electrons upto a high kinetic energy, which finally transfer the energy from the channel to the oxide, that will degrade the oxide performance and alter the device threshold voltage and with span of time it lead to the failure of the oxide that becomes the major concerns, with the scaling down the dimension of the device. In scaled device the other dielectric are used which has high dielectric constants generally referred as high-k materials, the basic requirement of these dielectric in scaled device, to obtained the same effective capacitance of the

gate as it obtained through the thicker oxide. But the various step have to be taken into consideration to obtaining the same stability and other factors as obtained when silicon dioxide is used.

1.6 MOSFETS SCALING CRISIS AND EVOLUTION OF NANOELECTRONIC DEVICES

In today, major concern in the technology world is the scaling down of MOSFETs is endowing its limits. Researchers and all expertise around the globe are trying to learn new technique and utilizing their time to develop new device and the architecture in order to rigorously improving the speed of operation and the physical parameter like the packing density of the Integrated circuits (IC). Thus the evolution of new device with the help of new material completely vanishing the bulk MOSFETs. Scaling [14] of the device down from 10nm to 30nm when compared to today channel length of the devices which is 40nm and in the past era, the channel length was around 10um. Scaling around 90nm seriously achievable by using the strained silicon technology which, is based on the concepts of compressively stressed the channel and simultaneously raised the surface hole mobility of the PFET. Scaling around 65nm (gate length 37/65 nm) SiO_2 has been the favored as a gate insulator at the beginning of silicon technology. During continues process the oxide thickness has been condensed from 300 nm for the 10 um technology to 1.2 nm for the 65 nm technology. Basically, the thinner oxides raise the speed of operation and also improve the performance, but manufacturing the devices with this thin oxide is quite impossible but on the other hand, if the oxide thickness is larger it may cause damage to the devices because of increase in the electric field. For Silicon-Dioxide (SiO_2) films thinner than 1.5 nm, another important issue of tunneling arises. At 1.2 nm, SiO_2 seep out 1000A. of current. Similarly, if the IC contains a number of the device in an area then it would cause the leakage current of around 10A. But the solution to this leakage current reduction is possible by introducing the nitrogen in silicon-dioxide. Scaling around 45nm, engross high-k dielectric materials a substitute to silicon-dioxide. Zirconium Dioxide (ZrO_2), Aluminum Oxide (Al_2O_3) and Hafnium Oxide (HfO_2) because they have their dielectric constant higher to SiO_2. As the larger thickness of high dielectric oxide is equivalent to thin silicon di-oxide which hold the same capacitance and the channel current also thicker high k-dielectric drives lesser leakage current than that of low k-dielectric. Not only the dielectric but also the metal gate is also replaced by the normal Al to heavily doped extremely conductive polycrystalline silicon (poly-

Si) because of its ability to not to react with SiO_2 at a higher temperature. Continuously scaling down the device parameter from the conventional bulk MOSFETs to 22nm with the gate length of 12/30nm give rise to new technology. As the oxide thickness dwindles the gate gets perfect control on the channel. With the scaling of the length of the channel, the distance between the drain and the channel become increasingly important that the gate lose the control on the channel and device becomes weak. With the off condition of the N-channel MOSFETs the device still remains on and the leakage current flow between the drain and the source increase thus, damage the device and cause serious power consumption issues. Characteristically it is mandatory to exploit the gate-to-channel capacitance and to weaken the drain-to-channel capacitance, in order to improve the drain leakage current.Same effect of drain controlling is observed when the channel length is also scaled down to the lower level and create more hurdles. To eradicate deeply submerged leakage, it is necessary to provide more gate control to the channel which, is achieved by providing a gate control from more than one side of the channel also by considering another parameter of the device architecture. When the devices are controlled by more than one gate then it is called as multi-gate or sometimes also know has FINFET. According to the ITRS, there is an agreement among researchers and the scholars that CMOS devices [17] will discontinue to scaling by 2020. Some of the budding capable technologies that have the perspective to reinstate the current generation of CMOS, for ultimate scaling down.

1.7 NEW DEVICE TECHNOLOGIES - SOI MOSFETS

Scaling of traditional planar bulk- MOSFET is apposite tricky in following Moore's Law in proceed expertise module. Majorly due to inability to control the SCE and escalating unevenness in the device characteristics. Therefore, there is a harmony among the semiconductor industry experts that introduces the new technology device architecture at nanometer vital. The quintessence in following invention of the novel device structure is to boost up the control of gate terminal over the channel. Figure1.6 depicts the structures that show the fruition of transistor that facilitate to shorter gate length and this new technology device is so called as SOI.

1.7.1 SOI Technology

A major challenge in ultra-high density CMOS integrated circuits is the physical disconnection between individual devices considered in nanometers (nm), also a proper electrical isolation. The substrate wafers of SOI, as contrasting to usual wafers of bulk, not only unravel the crisis of electrical isolation between contiguous devices but also permit pioneering layouts of the device

consequent trivially enhanced performance than that of substrates of bulk CMOS circuitry. For this reason, SOI substrates wafers speedily became an imperative component of the IC technology. Figure 1.6 represents a cross-section of a bulk wafer in which individual devices are isolated by LOCOS isolation or shallow trench isolation (regions in red). A very thin layer of oxide is created once the substrate is formed, also by this kind of fabrication technology a better-quality isolation among devices is achievable which is proficient by etching off Si among devices after successful isolation among the device is obtain the replenishing produced narrow trenches with oxide. As a consequence, millions of device that are embedded within the oxide is achieved at a single fabrication. In this oxide layer which is created initially is termed as buried oxide [18]

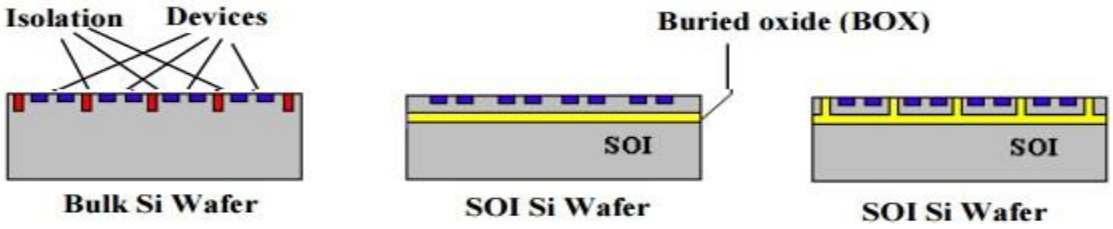

Figure 1.6 Generation of SOI Wafer[18]

This technology not only eradicates leakage current between devices but also consequences in the more rapidly switching device as parasitic capacitances related to source and drain regions are reduced. Also by reducing the thickness of the Si layer that is on the top of buried oxide layer help in further enhancement in the performance of CMOS circuit on SOI substrate. In the above figure1.6 same MOSFET architecture is shaped in the thicker and thinner active layer that is Si-layer.

1.7.2 Type Of SOI MOSFET

Depending upon the thickness of active layer over the insulator SOI is distinguished as Partially Depleted SOI and Fully Depleted SOI. PDSOI is termed as thick film Silicon SOI devices and the thickness is around 100-nm while on the other hand, FDSOI is termed as thin film Silicon SOI devices and the thickness is around 20-50nm.

(A) Partially Depleted SOI MOSFET

PDSOI technology [19] endow with considerable advances over the traditional bulk technology, and that makes it striking chiefly for high-performance applications. On the basis of Silicon thickness and the depletion width relation, PDSOI silicon thickness is greater than twice of depletion width ($t_{si} > 2_{W_{DM}}$) and the front and back-gate are decoupled electrostatically and both the potentials are independent. In this device, drain and source from a junction with substrate depletion region, if the thickness of substrate is thick enough, then a neutral region is also present, which is not depleted and hence called body as floating body. The main advantages of PDSOI includes the lower junction capacitance that result in the higher performance at a given dynamic power and the floating body effects result in dynamic threshold voltage that improve the performance and the body effect.

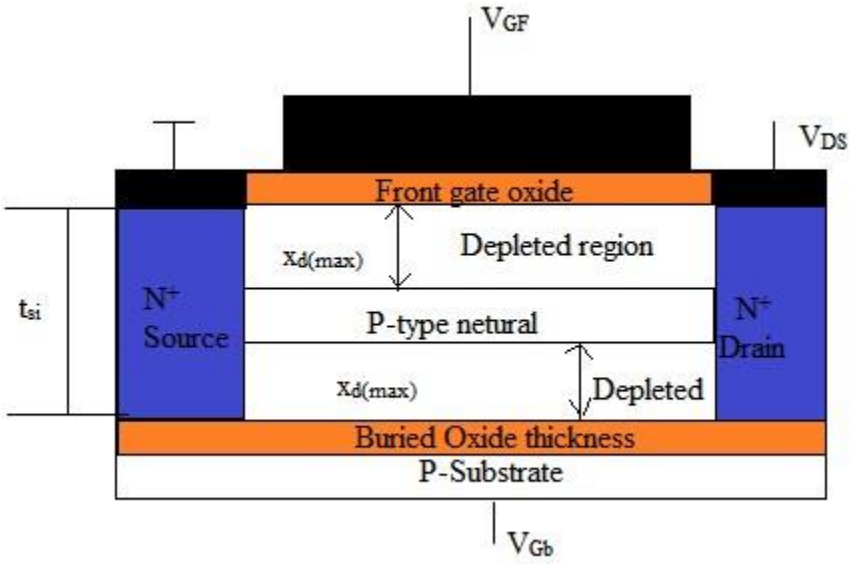

Figure 1.7 Cross Sectional View of PDSOI MOSFET

Apart from the advantages, the PDSOI show signs of kink effect and bi-polar latch-up phenomena, which tends to increase the off- state current (I_{off}), Impact ionizations is the major cause for the bi-polar latch-up, in this effect at the drain side more number of electron are integrate and when the device operated at high drain voltage gate lose their control over the channel and is very severe outcome of bi-polar phenomena, these all effect is characterized as the "***Floating-Body effect***" of SOI device. While the PDSOI floating body can provide enhanced

performance, it does result in several detrimental effects. These include bipolar currents that can dynamically discharge high nodes that are supposed to remain high; time varying threshold voltage (V_t) which result in the increased DIBL which requires more doping in the device to provide a similar (V_t) as bulk; and the lack of being able to supply a back bias unless using a body contacted device which takes up much more area [20]

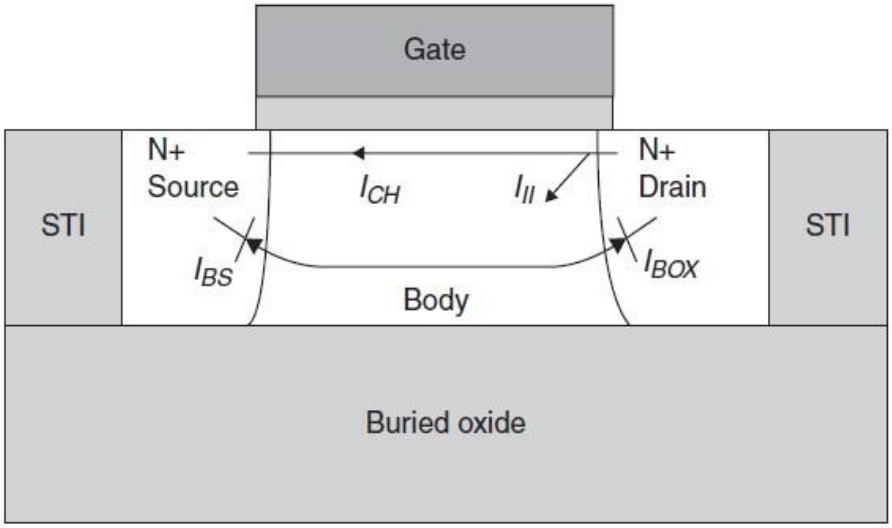

Figure 1.8 NMOS PDSOI MOSFET with Leakage Current [21]

Above figure1.8 shows the NMOS PDSOI device with source-drain floating diode formation with Substrate or body and the bias current due to latch-up. It is important to note that when the I_{off} of the PDSOI matches with that of bulk, which obtained at high threshold voltage and high doping of PDSOI indicate in the degrade in the performance. To retain with these parasitic effect, a body contact with devices is formed which indirectly helps in the reduction of kink effect which is present due to floating body. On the other hand if the body to the gate connections for the devices is made which helps in the variations of threshold voltages.

(B) Fully Depleted SOI MOSFET

FDSOI is the planar technology that involves the two effects. First, is the ultra-thin layer of insulator known as buried-oxide over which the base of silicon is grown. Then the thin Silicon film implements the transistor channel, which makes it as fully depleted type transistor. The FDSOI technology enables much better Electrostatic characteristics of the transistor over the bulk technology as shown in the figure 1.9. It lowers the parasitic capacitance between the source and

drain with respect to the substrate and also maintained the unidirectional flow of electron from source to drain. This technology allows the better control over the channel through the gate and also by polarizing the substrate underneath the device just like bulk technology.

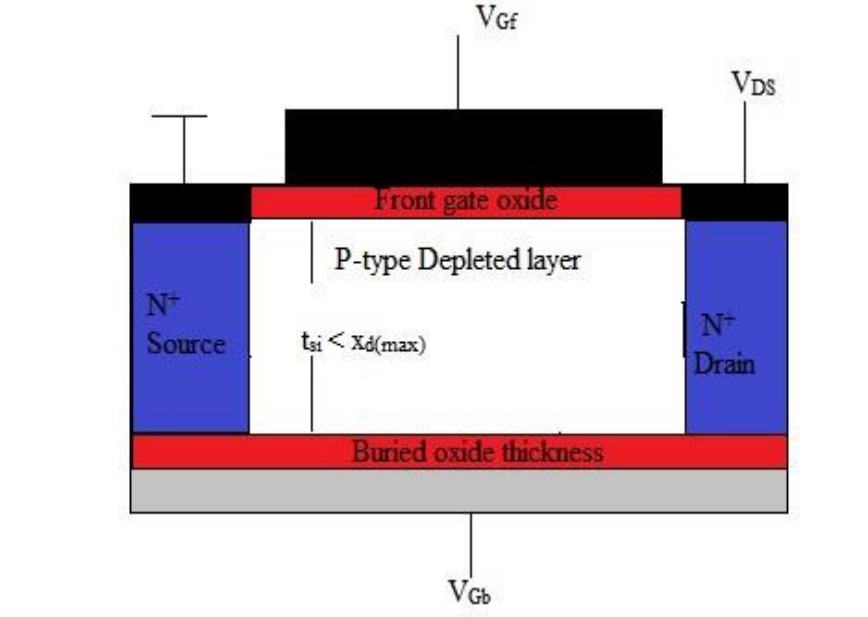

Figure 1.9 Cross Sectional View of Fully Depleted MOSFET

On the basis of thickness of the Silicon film and the depletion width FDSOI [22] relates that the thickness of the Silicon is lower than the depletion width ($t_{si} < W_{DM}$) and front and back-gate are electrostatically coupled means the potential at the back and front gates are dependent on each other thus changes the device characteristic according to potential and relation present on the device and it reflects on drain current, threshold voltage and the Subthershold slope [23]

1.8 THESIS ORANGIZATION

This thesis is alienated into five chapters and it is summarizing here:-

- **Chapter2: LITERATURE REVIEW**

In this chapter, we will describe the motivation that leads to the development of advanced technologies and reviews the basic of SOI and basically focused on the work projected by researchers by considering the benefits of SOI MOSFETs and concentrate on the drain current, threshold voltage model methods proposed by the prominent researchers.

- **CHAPTER3: MODELING OF SOI DEVICE**

In this chapter we define the Device Modeling and its types, then present our work by first analyzing the drain current for an asymmetrical FDSOI MOSFET with the help charge based

model by calculating all the required parameter in order to understand the concepts of thin film active layer SOI, then we focus our work on an analytical modeling of drain current by defining the potential equation in x and y-direction which indicate the position of effective conductive path attain in x-direction, and on this basis calculate the threshold voltage of the device with back-gate biasing to clearly understand the device characteristics.

- **CHAPTER4: RESULT AND DISCUSSION**

In this chapter, we present our work by analyzing the result obtained from the Model Evaluation through MATLAB, by plotting the graphs of equations that we model in chapter 3, and verified our results with the TCAD simulations, by assuming all the parameter required during simulation. And we have maintained the good agreement between the results of both analyses. Here we analyze the threshold voltage parameter, potential across the channel and the effect of drain current all these analyses has been considered by biasing the device with respect to the source terminal.

- **CHAPTER5: CONCLUSION AND FUTURE WORK**

In this chapter we summarize our model analysis we stipulated results with certain presumption and finally define the future work required by my model with proper extension in order to achieve a better result in near future by considering all the possible improvements.

Chapter 2
LITERATURE REVIEW

2.1 MOTIVATION

Since 1959, beginning of the IC technology, which has unwrapped the thriving path for an embark range of micro and nano-electronic applications, but certainly technology consequential based on the famous Moore's law that indicates the minimum gate length is incessantly reduced and that the scaling of characteristic length will be unrelenting in the predictable future. But the planar bulk CMOS technology has been operating tremendously over the past 40 years in the semiconductor industry. However, the conventional bulk-MOSFETs are forthcoming the scaling limits and arise a critical problem called in terms of SCE. Basically to control the one parameter "***Electrostatic Integrity***" by an increment in the doping concentration of channel and by diminished the thickness of gate oxide shows the dilapidation on "***channel mobility and gate leakage performance***". In due course of time, further transistor scaling spectacularly increases the statistical variability resulting from the discreteness of charge and granularity nature of matter. The prevailing source of this drawback is the arbitrary distinct dopant from the heavily doped channel region, which leads to the change in the electrical behavior of the devices/transistor and unfortunately limiting the maximum yield and performance in the nanoscale in CMOS application. Beyond 28-nm technology planar bulk- MOSFETs scaling doesn't provide the significant results, for this new device generation has to be architecture in order to enable the acquire results along with the benefits of scaling in near future. According to ITRS (International Technology Roadmap Semiconductor) that projected Ultra-thin Body Silicon on Insulator transistor approach over the Bulk-planar MOSFETs. Because UTB-SOI technology architecture can endure the very low channel doping concentration with the improved Electrostatic Integrity (EI) and spectacularly reduced the variability which arises from the random dopant. By SOI not only the EI will be improved but also the shows in the reduction of junction capacitance, which result in the high performance and faster switching. So, I have done a literature survey on SOI and comes up with it various approaches in terms of its Drain Current calculations and other parameters.

2.2 APPRAISES On SOI

Since the SOI MOSFET has a unique aspect of the charge controlling in the active layer commonly called as silicon body sheet that allows the current flow in the two channel because the SOI has two gates, and both the gate can simultaneously generate different current-voltage characteristic. The characteristic of the device can be calculated by considering the strong inversion region for front-gate and by varying accumulation and depletion region for back-gate many researcher and expertise work on this era and appear up with the analytical and compact model of the SOI device and simultaneously working on the fabrication of the SOI device which is basically influenced by the electrical characteristic of MOSFET. So, the characteristic of various types of SOI devices on the basis of film thickness was premeditated by the threshold voltage models which are illustrated below. With this a studied has begun in this era and in the year 1980 two author Worly and Sano et al came up with the analytical replica for the threshold voltage but on two different devices, as **Worly** had done the threshold voltage analysis**[24]** of an Silicon-On-Safire transistor, but result shows the similar behavior as shown in SOI transistor which is the charge coupling between the front and back gate, in characteristics of current-voltage was obtained only in one condition when back gate is in accumulation region. With this basis **Sano et al** (1980) studied and analyzed**[25]** the numerical behavior along with attributes of MOSFETs when fabricated on an epitaxial Si layer buried on the top of SiO_2 layer and different solution was obtained from number of methods like Poisson's equation, minority and majority carrier concentration calculation and also included the factor of carrier multiplication with impact ionization, by all these method the researcher consistently obtaining the result along with altering the specification of other parameters also, by doing so, the shift in the threshold was analyzed with respect to the reduction in silicon film thickness. One of the most simple benefits of thin-film SOI explained by one of the authors of 1982 **H.W. Lam et al [26]** is about the dielectric isolation characteristics have endorsed the evolution of new technologies. In this era author rigorously worked on the various methods to accomplish the thin-film SOI structure and some structures have been described by various author in 1980-1982 but the most refine method studied and get the positive response are the recrystallization of polysilicon films placed on the SiO_2 by various methods such as by laser annealing or by heating of the graphite strips another method is the shooting of oxygen into single-crystal silicon by all these new approaches of fabricated these thin film variance are observed in the output characteristic of the SOI MOSFETs as association with the conventional bulk MOSFETs due to reason of coupling of charge carrier

between the gates though, the back gate is here act as silicon substrate for single gate SOI. By this coupling phenomenon which makes SOI exclusive from other transistor and other researcher also projected exponentially and linearly on channel length and drain-substrate biases respectively dependencies due to the threshold voltage in short-channel device shown by solving the 2-D Poisson's equation by **Ratnakumar & Meindl** (1982)**[27]** these key parameters, turns a head around for other research scholars to work on these special characteristics and provide the various results and explains the working of this new device too. For these issues in 1983, expertise got to know the reason behind the coupling and its effect on characteristic is that, when the silicon film is completely depleted the coupling occurs, which makes the channel current of generated through front-gate as highly dependent parameter which consequence by the back-gate bias in thin-film SOI MOSFETs and come up with the study of charge coupling between the both gates and also calculate threshold voltage under all possible stipulation is derived from the new technology architecture alternative to Silicon-On-Sapphire(SOS). As from the previous studies by him and his co-worker on SOI (Silicon-On-Insulator) results that SOI film is thin, if device fabricated by involving the electrical properties of MOSFETs, they are influenced by the charge coupling between the front and back gates. For instance, the threshold voltage(V_{Tf}) of the front gate differ significantly by the bulk conventional counterpart but highly depends and influences by the properties and bias applied to the back gate substrate. By the end of the year 1983, **H.K. Lim [28]** and other co-workers demonstrated that front gate threshold voltage varies linearly with the back-gate voltage in the various region of operation. Along with that the researcher also analyzed how both the gates can be utilized basically a back-gate to manage channel conductance in the linear region and for the enrichment the SOI MOSFET performance by originating the expressions for the threshold voltage in closed form under all achievable conditions, may be the solution for the problem opted by **Ratnakumar & Meindl** (1982). This search on threshold voltage variations in various region like in accumulation, inversion, depletion goes on and the **Jerry G.Fossum [29]** one of the notorious author, in 1984 forward the work on charge density calculation and comes up with the I-V characteristics more considerably on the basis of charge-coupling when the V_D is lofty since the surface at the back is in close proximity to the drain hang about in depleted region for a wider range of (V_{Gb}) back gate voltage. In year 1983, the calculation of drain current in depletion approximation and its dependencies on the terminal voltages but particularly considering the assumption of mobility to be constant and the uniform doping, the output of this model limits its efficacy for giving the

physical insight and complexity aiding the design of SOI device and its application has been done by Barth et al. But his teamwork output calculation and theory had some drawbacks and also it doesn't matched up adequately with the experimental data so to overcome this **Jerry G.Fossum** presented the same analysis with same parameter assumption but in strong inversion region for 4-terminal devices and also it get acquainted with physical insight of the model devices, as the major concern at that time is the calculation of the inversion charge density in the channel and inversion charge density with the surface potential is act as linear function is achieve, but those two factor assumption will remain the disadvantage for a time begin also some kind of discrepancies were noted and result in the degradation of carrier mobility so research would be going on, on this factor and also on scaling issues. In 1985, group of the researchers **Balestra et al[30]**, depicted the effects of various parameter and its interface by calculating the threshold voltages for front and back channels respectively for both p and n- channel SOI MOSFET architecture were scrutinized and also obtained the drain current & potential equation as a function of both gate(front& back) threshold voltages by calculating the electron and hole densities obtained from the integration of Poisson's equation, in order to reduced the effect of interface parameters expertise search on other function methods to obtained the solution by solving the 2-D Poisson's equation then in 1987 **Lin & Wu** came up with the solution of equations by Green's function**[31]** and along with the calculation of threshold voltages and drain current, they also calculated the subthershold current all these calculation can be done either by considering the facts of thickness of Silicon film or not. On that fact, the researchers projected their studies on the calculation of valid threshold voltages equation obtained from the Poisson's formula and also considered the various assumptions regarded with the thickness of silicon film, one of the finest assumptions is pretentious that the sheet of charge with zero thickness rather than the silicon film for this, in 1989 **John B. Mckitterick & Anthony L. Cavigila**, derived the solution for thin film**[32]** from the previous studies that replacing the silicon film with that sheet of charge. From this results obtained for thin film is varying differently with respect to the thicker film or with the bulk devices transistor, the calculation has been done only by considering the one parameter which was independent of doping, for this fact of calculating the threshold voltage depends on the doping concentration as well, the author in 1990 has been modified the previous model of n-channel SOI MOSFET transistor and studied the characteristics again which reflected an augmentation in sub-threshold slope at larger drain voltages by improving the body doping concentration but along with that one drawback was also observed, that the lessening in

the threshold voltage shifts in negative direction with the floating-body and due to the diminished the threshold voltage by body effect as the forward biases junction is obtained between the body-to-source, this studied was shown by **[33]Matloubian et al.** But, in these entire analysis author showed the less concern on short channel devices, as mentioned by the many researchers that threshold voltage calculation majorly valid for long-channel devices, when above calculations are applied to the scaled devices then in 1991, researcher and his co-workers depicted the discrepancy of subthershold slope with reverence to temperature, drain and substrate bias respectively in deep submicron n-channel SOI device. As directed that if the substrate bias is increased in negative direction then the spiky subthershold voltages distinctiveness was observed at high drain bias and this course work was studied and analyzed by **Tokunaga et al.[34]** this dependencies for a substrate bias was clearly explained through the charge state model at lower SOI interface. On the other hand, in 1993, **[35]Guo & Wu** premeditated an analytical model of threshold voltage for the FDSOI MOSFET and by the 2-D Poisson's equation obtained the solution for V_{th} in all the regions by using the minimum surface-potential approximation and in this analysis DIBL effect was observed. Though, it is important to study the SCE and by other researcher it came under observation through the study of diverse SOI MOSFETs technology that S-factor results in the degradation of short-channel effect in FDSOI MOSFETs and in equivalent year, Joachim et al projected our major concerned on the calculation of the subthershold slope in ultra-thin FDSOI MOSFETs for the scaled devices, where the channel length was reduced down to 0.1um and along with that clearly explained the phenomenon that what makes in the improvement in the S-factor and which leads to the deprivation of S-factor at the scaled gate length, for all this Joachim and his teams proposed the modified 2-D analytical model and 2-D Poisson's solutions was achieved with exclusively modified boundary condition in order to obtained the potential distribution inside the BOX. After analyzing all the parameter it was concluded that by increasing the channel doping concentration the S-factor is improved but there are certain concerns due to its effects the degradation in S-factor these are (a) spiking in the capacitance in the channel in source and drain end basically due to potential distribution (b) inflection of the current (effective) due to variations in the channel thickness at different gate voltages (c) observing the subthershold current flow at the back gate channel. Similarly, in next coming year 1995, the prominent researcher scrutinized the threshold voltage of FDSOI in deep submicron region by using the 2D quasi model at the scaled down gate length, Banna and his co-worker studied the threshold voltage roll-off and drain dependencies in all these observation one

advantages was that the threshold voltage roll-off is lesser in FDSOI than in bulk technology devices. On the other hand the researcher has been doing their research work in field of 1D analysis of the devices with doped and undoped architecture and also on the SCE after slog of their research in 2000 **Ravariu et al [36]** analyzed the both kind of SOI technology partially and fully depleted with non-homogenous doping and designed an accurate model in order to calculated the electric field first rather than directly calculated the potential distribution. With the help of non-uniform doping, it was observed in the reduction of the threshold voltage as compared to the uniform doping in SOI devices and also the simulation has been conceded by various simulator, but in deep-submicron region the uniform doping in the body shows the better result in FD technology as was projected by other scholars, in 2005 **Kumar & Orouji [37**] proposed the analytical model for the SOI devices and gauged the surface potential profile and V_{th} along with electrically provoked the shallow extension of source and drain region (S/D), in his research he has done the calculation by using the different approach which was, dividing the SOI device in three region and find the potential distribution in those region by using the 2d Poisson's equation in this he also investigated the SCE, the main reason for his research work is to control the SCE with the extension of S/D region and it his work gained positivity, then in 2006, scholars continued the research of previous author for extension of S/D shallow region for reduction in SCE and hold an increasing the drive current, but **Kumar et al[38]** modified the analytical model architecture of SOI device by using the strained-Si technology and repeat the whole analysis and pointed out that gate length below 50-nm and even less than SCE has been controlled successfully with the extension, in his work he also considered the thickness of film, doping, also the gate workfuction and various other properties all these analysis obtained by 2D Poisson equation and by Gauss Law also validated results and simulations were carried out. By considering all the facts that explained above by our well-known researchers, In 2009 **Rathnamala et al[39]** projected an unified analytical threshold voltage model for an FDSOI MOSFETs and modified the research work of previous author on non-uniform doping profile, but in lateral and vertical direction and with the help of the boundary condition along with 2D Poisson equation scrutinize the threshold voltage calculation, in parallel to this analysis UTB and box FDSOI are considered one of the most prominent device below sub-28nm technology that help in reducing SCE with up to 70% in comparisons with other technology like fin-shaped FET and UTBB technology also shows strong coupling between the front and back-gate and indicated that threshold voltage was highly controlled by back-gate substrate bias instead by using the

diverse channel doping concentration that generate the variability due to RDF, and it has been observed in the analytical model modified device disposed by **Rathnamala** in 2010**[40]** with a non-uniform doping for an FDSOI device. However, thin buried oxide may also trigger strapping coupling from the drain and this possible if the body was doped lightly and it results in gate control loss over the channel, in order to get rid from this effect researcher, in 2011 proposed an amalgamation "***Backplane***" a highly doped layer beneath under the BOX C.**Fenouillet-Beranger et al [41]** worked on the low-power UTBOX and the BP (backplane) at 32-nm for an FDSOI technology in order to eliminated the drawback of thin-BOX and a fast compact model and accurate analytical model was describes the behavior of transistor properly under back-biases wide ranges. On the basis of back-plane theory various compact model for asymmetric-independent DG have been descripted and these all model were analyzed based on the various concepts like on the inversion charge, surface-potential and the threshold-voltage and all the calculation are done all the three regions of operation that is inversion, accumulation and the depletion among all these the surface potential model approved the great popularity and discussed both in long and short channel device but before move on to the DG devices the authors **S.Kandelwal et al.[42]** has been presented our research work with a compact model for ultra-thin SOI-MOSFET in 2012, which accurately provides an accurate results when the interface between the substrate and BOX is depleted and advanced the previous work by providing proper accuracy in requisites of numerical simulation, computational efficiency and obtaining the higher order drain-current and also covering the velocity saturation, mobility degradation and CLM by agreed all these analysis at scaled nanometer range that is 8-nm Si-thickness and 10-nm of BOX thickness .By continuing this research, In 2014, the threshold voltages of front and back-gates along with the ideality factor with back gate control was developed by **Fasarakis et al[43]** based on the minimum value of the front and back surface potentials for an analytical model for lightly doped FDSOI MOSFET with ultrathin body and BOX. In 2015, **[44]Theano A. Karatsoi et al** has been modified their previous work by significantly defined the threshold voltage in term of gate voltage with a new concept of effective conductive path, and in this researcher use electron density at ECP reaches the doping density of the Si-body, and on the basis of threshold voltage and ideality factor a complete charge based model analytical model with little variations for drain current that is valid in all the regions of operation along with bias at back-gate has been proposed also including the major SCE, with the validated and simulated result

Chapter 3
DEVICE MODELING

3.1 INTRODUCTION TO DEVICE MODELING

Modeling of a device is essential as it endows with the terminal behavior of the device in terms of their distinctiveness whether it is current-voltage, capacitance-voltage characteristics and the carrier transportation that takes place in the device. By the help of these parameters obtained from device modeling reveals the performance of the device in all regions of operations. Due to this, it is opportune to divides these models into two categories that are (i) Physical Devices Model (ii) Equivalent circuit-based models. The first category is based on the accurate device geometric behavior, doping profile and the semiconductor basics and equations related to it, last but not the least is the material characteristics and this model is used to study the terminal and transport phenomena of the devices. As the device scaling increases to every year, basic model methods are not used to provide an equivalent results for this we require the two and three dimensional solutions along with the semiconductor equations and will able to obtained the result by using numerical methods, which is often called as the numerical device simulators, which provides the insight detailed of the device operation in physical aspect and also provide the new characteristics of the devices. On the other hand, the equivalent circuits based model illustrates the electrical characteristics of the device by involving the electrical circuit's elements in such an approach that emulates the electrical incurable behavior of the device. For semiconductor devices, the circuits models are highly inaccurate and non-linear in nature and are robustly dependent on the DC bias, signal frequencies, and temperature. On these circuits based model is divided as the small-signal model and large-signal analysis models thus require three types of models DC, transients, and AC for static, large-signal dynamic and the small-signal models respectively.

There are various techniques implemented on computers that satisfied the numerical analysis for the physical models. Physical models are either solved with the semiconductor equation of carrier transports, Poisson's equation or the Boltzmann transport equation. Traditionally, most of devices characteristics are understood by the bulk transport solutions and others are providing the insight detailed explanation of the device physics. However, the inclination towards very

miniature geometry devices gives rise to the other methods that are used for device modeling in other certain conditions.

3.1.1 Different MOSFET Models

The rapid enlargements in the technology over the past 15 years have led to dramatic increase in the interest in device modeling. As the individual semiconductor devices scale decrease, the intricacy of the physical structures boosts up, the characteristics of the devices, those are obtained from the classical modeling concepts, some of the standards compact models is studied by the semiconductor industry are entitled here:-

(a) Potential Based Model

The surface-potential based model corresponds as the finest modeling approach of the MOSFETs devices currently in the semiconductor industry. The impetuses following the toggling from the threshold-voltage model to surface-potential based model goal loom in order to amplify the substantial requirement for compact modeling and consequently makes it further enviable for sophisticated MOS modeling devices with respect to the traditional modeling concepts and provide the various quantitative characteristic behavior. Surface-Potential is the potential at the interface of Si and oxide is an innate function of the terminal voltage that is finally obtained by the solving the SPE. Conventional Surface-potential based model is the basically known has the charge-sheet approximation does not direct to a useful result due to intricacy involving by an introduction of SCE effects for SC devices. Several of the models are based on this modeling emerge SP models applicable down to 100-nm are introduced by HISIM, Penn-state University, USA.

(b) Charge Based Model

A fundamental and primordial modeling guidelines approach is the charge based modeling. It is principally based on the analyzing the value of inversion charge density that includes the threshold voltage functions. This model is a provincial model because it enlightens the performance of the MOSFET discretely in all region of operation. So, these models calculate all the necessitate parameters, they are fairly empirical in the interfacing region and the device is not described accurately. The outstanding charge based models are level1, 2, 3 BISM 1, BISM 2, and auxiliary to BISM 5 is worn for sub-micron 100nm technology. In regards to inversion charge based models, inversion charge density is approximated by means of integrated charge control

model. Basically both the models sharing same grounds of calculation. For a classical long-channel MOSFETs, taking into consideration for constant mobility, the main parameters of the devices, drain current, total charges, transconductance and the capacitances all these are measured in terms of the inversion charges densities. The basic equations for the modeling of device behavior involve the Maxwell-Boltzmann equation, Poisson's equations, Gauss law and others semiconductor carrier transport equation either in equilibrium and non-equilibrium regions.

3.2 ANALYTICAL MODELING OF SOI MOSFET

In order to calculate the current-voltage characteristics of the devices, first, we analyze the SOI technologies is used now-a-days in integrated circuits and for other purpose in order to obtained high drive current and suppress SCE and also worked on scaled level with appealing manner. In our first analysis, we modeled the device by considering an Oxide made up of SiO_2 and then extended our analysis for the different high-k dielectric. Generally, SOI device is dividing into two major categories depending on the film thickness (i) Partially-depleted (ii) Fully-depleted SOI. The expression which modeled here is considered for thin-film silicon body just because from our prior studies we can analyze that thick-film device analysis is equivalent to bulk MOSFETs because chiefly semiconductor moves to new technology in order to obtained desired results. For modeling and learn about the working of SOI which is generally a four-terminal device, where the silicon film is essentially fabricated on the insulating layer of silicon-di-oxide, which has been developed over the silicon substrate. So in SOI, the front gate is made up conventional metal, with polysilicon or with other metal with high work-function as per the requirement and the back is silicon substrate, but it's is better than our bulk devices because back which is made up of silicon can act as a second gate and termed as back-gate and by this properties it makes the device for better controllability of gate on the channel and gate contends for the charge in the film body, which is depicted by the drain current equation which shows the dependence on the back-bias substrate firmly known as back-gate voltage(V_{gb}) which make it unique. So our analysis establishes from the computation of threshold voltage then progress to the drain current calculation along with the calculation of inversion charge density.

The four terminal n-channel SOI MOSFET structure along with the direction depicted in the structure is shown below in figure 3.1.In this device structure, the two channels are formed at two different interfaces which are Si- Front-oxide interface and Si- BOX interfaces respectively,

here the Front-oxide can vary as per the design and we have to model our device equations in such a manner which describes the effect of back-gate control on threshold voltage and the complete device operation is based on this unique feature of an FDSOI MOSFET.

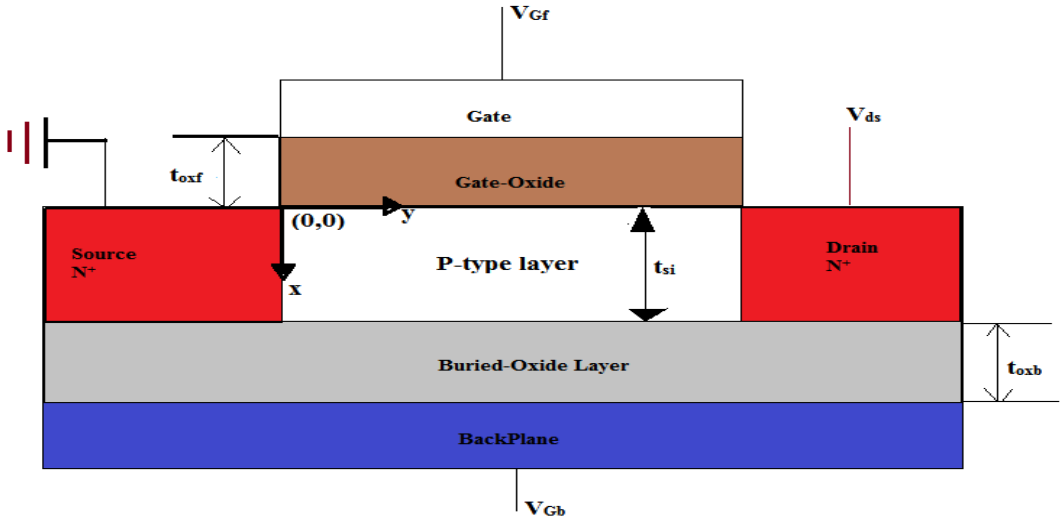

Figure 3.1 N- Channel FDSOI MOSFET

So the threshold voltage equation for thick-film SOI is similar to bulk device MOSFETs because their silicon thickness is greater than twice the thickness of depletion width, and also there is no indication of interaction between the front and back channel in any region of operations. The threshold voltage analysis for thin-film SOI devices is basically obtained by the second-order one-dimensional Poisson's equations in order to calculate the surface-potential as the function of the silicon film depth, indict in x-direction

$$\frac{d^2\varphi}{dx^2} = \frac{qN_a}{\varepsilon_{si}} \qquad \text{Eq(3.2.1)}$$

By integrating the equation (3.2.1) twice, we attained the surface-potential in x-direction along with the two constant c1 and c2

$$\varphi_{(x)} = \frac{qN_a}{\varepsilon_{si}}\, x^2 + \left(\frac{\varphi_{SB} - \varphi_{SF}}{t_{si}} - \frac{qN_a t_{si}}{2\varepsilon_{si}}\right) x + \varphi_{S1} \qquad \text{Eq (3.2.2)}$$

Where the constant c1 is equal to $\left(\frac{\varphi_{SB}-\varphi_{SB}}{t_{si}} - \frac{qN_a t_{si}}{2\varepsilon_{si}}\right)$ which is the obtained by the delta depletion approximation of the mobile charge at silicon surface and calculated by Gauss' law & then

constant is equivalent to electric field on the front surface at x=0, in this q is the charge, N_a is the doping concentration for acceptor atoms, t_{si} is the thickness of the silicon film ε_{si} is the dielectric constant of the silicon material φ_{SB} is the surface-potential at the back side and φ_{SF} is the front surface-potential , in order to calculate the constant c1 which is obtained from Gauss' law by using delta approximation, figure 3.2 decipts the field at the top and back, along with the variations in silicon film thickness

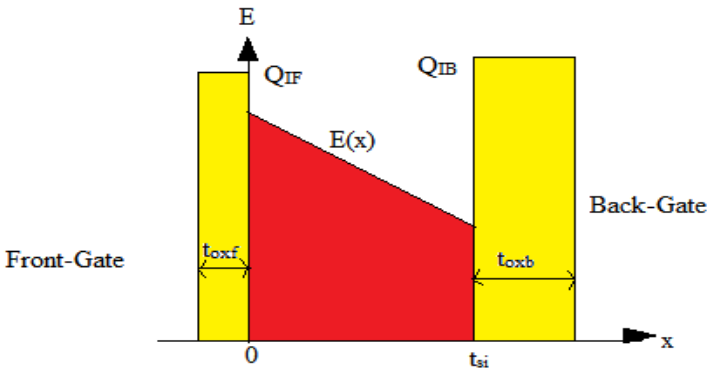

Figure 3.2 Variations of Electric Field in an FDSOI

$$\frac{dE}{dx} = \frac{-qN_a}{\varepsilon_{si}} \qquad \text{Eq(3.2.3)}$$

Thus, by integration dE factor in above equation (3.2.3) from the electric-field at the front surface for x=0 to the electric field at the thickness of silicon film t_{si}

$$\int_{E(0^+)}^{E(t_{si}^-)} dE = \frac{-qN_a}{\epsilon_{si}} \int_{0^+}^{t_{si}^-} dx \qquad \text{Eq(3.2.4)}$$

Solution to this integration,$E(t_{si}^-) - E(0^+) = \frac{-qN_a t_{si}}{\varepsilon_{si}}$ by doing some modification we can obtain the value of $E(0^+)$ that is the electric-field at the front surface and the electric field in the bulk is not zero as compared to bulk as it mainly depends on the presence of depleted charges and the acceptor carriers and it is indicated as $E(t_{si}^-)$, Electric-field at the bottom side, i.e, deep inside the bulk, and next step is to calculate the potential drop in order to get the band- bending, φ_{SF} and φ_{SB}

$$E(0^+) = E(t_{si}^-) + \frac{qN_a t_{si}}{\varepsilon_{si}} \quad \text{Eq(3.2.5)}$$

$$\Delta\varphi = (\varphi_{SF} - \varphi_{SB}) = \frac{1}{2}[E(0^+) + E(t_{si}^-)]t_{si} \quad \text{Eq(3.2.6)}$$

The equation (3.2.6) indicate the total potential drop across the thin film silicon by considering the area under the trapezoidal, as we are assuming the delta function so there is no voltage drop across the t_{si}. From above two equations (3.2.5) and (3.2.6) the final relation of electric-field at the surface is obtained which is equal to the constant c1 as represented in equation (3.2.2) in form of second-term.

$$E(0^+) = \left(\frac{\varphi_{SF} - \varphi_{SB}}{t_{si}}\right) + \frac{qN_a t_{si}}{2\varepsilon_{si}} \quad \text{Eq(3.2.7)}$$

$$E(t_{si}^-) = \left(\frac{\varphi_{SB} - \varphi_{SF}}{t_{si}}\right) - \frac{qN_a t_{si}}{2\varepsilon_{si}} \quad \text{Eq(3.2.8)}$$

By equation (3.2.7) final results are obtained for the front surface-potential at x- direction, similarly in order to calculate the voltage at both the surfaces by considering the electric field effect on the front- gate oxide as well as on back- gate oxide.First analysis holds for front surface potential, so the field effect in the front gate-oxide is

$$E_{(OF)} = \frac{[V_{GF1} - \varphi_{SF}]}{t_{oxf}} \quad \text{Eq(3.2.9)}$$

Where$V_{GF1} = V_{GF} - \varphi_{SF}$, in this V_{GF} is the applied gate voltage at the front-gate and t_{oxf} is the front gate-oxide thickness by taking the inversion charge into description

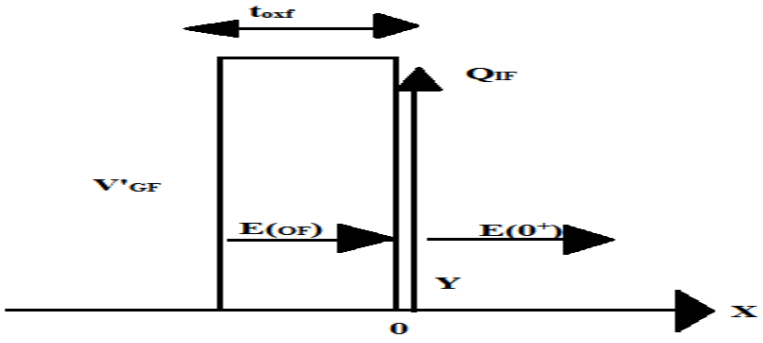

Figure 3.3 Effect of Flectric Field at Front Surface to calculate Voltage Parameters,

the equation (3.2.9) is obtained from the relation and figure 3.3 in this function φ_{SF} is represented as Y in figure 3.3

$$\varepsilon_{ox}E_{OF} = \epsilon_{si}E(0^{+}) - Q_{inv1} \qquad Eq(3.2.10a)$$

$$E(0^{+}) = \frac{\varepsilon_{ox}}{\varepsilon_{si}}E_{OF} + \frac{Q_{inv1}}{\varepsilon_{si}} \qquad Eq(3.2.10b)$$

$$E(0^{+}) = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{(V_{GF1} - \varphi_{SF})}{t_{oxf}}\right) + \frac{Q_{inv1}}{\varepsilon_{si}} \qquad Eq(3.2.11)$$

Equation (3.2.11) is obtained by using the basic equation of Gauss' law and we are considering the displacement field in the oxide whereQ_{inv1} is the inversion charge at the front gate surface Similarly, the analysis hold for back-gate with the change in the difference of voltage for the back-substrate that is $\varphi_{SB} - V_{GB1}$ where the $V_{GB1} = V_{GB} - \varphi_{SB}$ in this V_{GB} is the applied voltage at the back-substrate and the electric field at the surface from the back side and the t_{oxb} is the back-oxide thickness.

$$E(t_{si}^{-}) = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{(\varphi_{SB} - V_{GB1})}{t_{oxb}}\right) + \frac{Q_{S2}}{\varepsilon_{si}} \qquad \text{Eq(3.2.12)}$$

By all the equations solved above (3.2.8, 3.2.9, 3.2.11, 3.2.12), the voltage function is obtained for front-surface and the back-surface respectively. All the analysis is done in order to calculate the electric-field in terms of the difference in the potential on either side.

Thus, by equation (3.2.8) and (3.2.11), the front- gate voltage is equivalent to the basic equation of voltage that is[45]

$$V_{GF} = \varphi_{ms1} + \varphi_{SF} + \varphi_{ox1} \qquad \text{Eq(3.2.13)}$$

By rearranging, the final equation for front-gate voltage is written as[28]:-

$$V_{GF} = \varphi_{ms1} + \varphi_{ox1} + \left(1 + \frac{C_{si}}{C_{ox1}}\right)\varphi_{SF} - \frac{C_{si}}{C_{ox1}}\varphi_{SB} - \frac{\frac{1}{2}Q_{dep} + Q_{inv1}}{C_{ox1}} \qquad \text{Eq(3.2.14)}$$

Where $\varphi_{ms1}$is the difference between front gate work-function of the metal and the silicon film and φ_{ox1} is the potential drop across the front gate oxide which is obtained from the theory of bulk-technology$C_{si} = \frac{\varepsilon_{si}}{t_{si}}$ similarly other capacitance C_{ox1} and the C_{ox2} are the front-gate oxide

capacitance and back-gate oxide capacitance are calculated respectively while $Q_{dep} = qN_a t_{si}$ is the depletion charge in the silicon film. On the other hand, the back-gate oxide can be calculated by equation (3.2.9) and (3.2.12), the back- gate voltage is equivalent to the basic equation of voltage that is[45]

$$V_{GB} = \varphi_{ms2} + \varphi_{SB} + \varphi_{ox2} \qquad \text{Eq(3.2.15)}$$

By rearranging the above equation, the final equation for back-gate voltage is written as[28]:-

$$V_{GB} = \varphi_{ms2} + \varphi_{ox2} + \left(1 + \frac{C_{si}}{C_{ox2}}\right)\varphi_{SB} - \frac{C_{si}}{C_{ox2}}\varphi_{SF} - \frac{\frac{1}{2}Q_{dep} + Q_{S2}}{C_{ox2}} \qquad \text{Eq(3.2.16)}$$

Where $\varphi_{ms2}$is the difference between back gate work-function of the metal and the silicon film and φ_{ox2} is the potential drop across the back-gate oxide which is obtained from the theory of bulk technology.Similarly other capacitance C_{ox1} and the C_{ox2} which is the front-gate and back-gate oxide capacitance are calculated respectively. For comparing it with the bulk technology device gate voltage, the extra terms in equation (3.2.14) and (3.2.16) is indication of the extra potential drop across the oxide due to the different surface potential as two sides are coupled electrostatically. This factor indicates the dependencies of the back-gate voltage of the device and shows if we increase or decrease the surface potential respectively for a fixed front-gate voltage then it changes the threshold voltage at front side. Basically, these are the two voltages equations that portray the charge-coupling between the front and back gate in an FDSOI device transistor. Now as we know that SOI device has the property to operate in nine different regions, here we analyze the device in which front gate is at the edge of an inversion region and back-gate is in accumulation, depletion and inversion region with the respect of back-gate bias. The threshold voltage for front-gate for all the regions is calculated where φ_{SF} is approximately equal to $2\varphi_F$ (twice of Fermi-potential) which indicates the onset of inversion, which is further useful in the process of calculating the body effect coefficient. In equation (3.2.16) this can be calculated by applying the voltages for back substrate bias and also with all these calculations, drain current, transconductance and more importantly the threshold voltage variations with respect to the back-gate bias are calculated.

3.2.1 THRESHOLD VOLTAGE ANALYSIS FOR THIN FILM SOI MOSFET

Increasing the back-gate bias, the front surface potential is increased as observed from the equation 3.2.14, so to balance the equation, the front threshold voltage decreases, as observed from the generalized equation of threshold voltage of front gate. At threshold, $Q_{inv1} = 0.5Q_{dep}$ and the $\varphi_{SF} = 2\varphi_F$ because we considered the front-surface at onset of inversion from equation (3.2.16)

$$V_{TF} = \varphi_{ms1} + \varphi_{ox1} + \left(1 + \frac{C_{si}}{C_{ox1}}\right)2\varphi_F - \frac{C_{si}}{C_{ox1}}\varphi_{SB} - \frac{Q_{dep}}{2C_{ox1}} \qquad \text{Eq(3.2.17)}$$

we can observe from equation (3.2.17) that threshold-voltage (V_{TF}) depends on back gate surface potential (φ_{SB}) , and hence it directly varies withV_{GB}.

If the back surface is in accumulated region, the threshold voltage for the front region is calculated by using the equation(3.2.16). In this φ_{SB} is pinned to 0, and φ_{SF} is pinned to $2\varphi_F$ and the $Q_{inv1} = 0.5Q_{dep}$, $V_{GF} = V_{th1,accu2}$ is obtained from equation (3.2.14)

$$V_{th1,accu2} = \varphi_{ms1} + \varphi_{ox1} + \left(1 + \frac{C_{si}}{C_{ox1}}\right)2\varphi_F - \frac{Q_{dep}}{2C_{ox1}} \qquad \text{Eq(3.2.18)}$$

Correspondingly, if the back surface is in inverted region, the threshold voltage is calculated by using the equation(3.2.16), by considering the value of $\varphi_{SB} = 2\varphi_F$ indicates that the back-surface is at the onset of inversion similarly, φ_{SF} is pinned to $2\varphi_F$ and$Q_{inv1} = 0.5Q_{dep}$, finally the $V_{GF} = V_{th1,inv2}$ is obtained from equation (3.2.14)

$$V_{th1,inv2} = \varphi_{ms1} + \varphi_{ox1} + 2\varphi_F - \frac{Q_{dep}}{2C_{ox1}} \qquad \text{Eq(3.2.19)}$$

If back- gate is biased to an inverted region, which allows the current to flow even if $V_{GF} < V_{th1,inv2}$, this is something worthless for any practical application. So proper mode of operation for the SOI device is when back-bias is in depletion and accumulation region. If back-gate is in depletion region, the φ_{SB} value depends on the V_{GB} and it ranges from 0 to$2\varphi_F$, so before solving $V_{th1,dep2}$, the assessment of back-gate for which the back interface accomplishes accumulation,

which is obtained from equation (3.2.16), by considering the $\varphi_{SF} = 2\varphi_F$ and $\varphi_{SB} = 0$ at the accumulation region and the $Q_{S2} = 0$, the results as follows.

$$V_{GB}(acc) = \varphi_{ms2} + \varphi_{ox2} - \frac{C_{si}}{C_{ox2}} 2\varphi_F - \frac{Q_{dep}}{2C_{ox2}} \quad \text{Eq(3.2.20)}$$

Similarly, the back-inversion voltage is also calculated by considering$\varphi_{SB} = \varphi_{Sf} = 2\varphi_F$, $Q_{S2} = 0$, putting to equation 3.2.16

$$V_{GB}(inv) = \varphi_{ms2} + \varphi_{ox2} + 2\varphi_F - \frac{Q_{dep}}{2C_{ox2}} \quad \text{Eq(3.2.21)}$$

Finally, the value of back gate depleted is obtained which is between the accumulation voltage and inversion voltage for the back-gate bias $V_{GB}(acc) < V_{GB} < V_{GB}(inv)$ so on the bias of this front gate threshold voltage for back-depletion is calculated as follows, first calculate the value of φ_{SB} with respects to the depleted voltage, which is difference of the back-gate voltage and the back-gate in accumulation region because the back-gate is depleted only when $V_{GB} > V_{GB}(acc)$ which is obtained by subtracting and rearranging the equation (3.2.16) and (3.2.20)

$$\varphi_{SB} = \left(1 + \frac{C_{si}}{C_{ox2}}\right)[V_{GB} - V_{GB}(acc)] \quad \text{Eq(3.2.22)}$$

From equation (3.2.17) and by putting the value of φ_{SB} from the equation (3.2.22), the value of $V_{GF1} = V_{th1,dep2}$ is extracted

$$V_{th1,dep2} = \varphi_{ms1} + \varphi_{ox1} + \left(1 + \frac{C_{si}}{C_{ox1}}\right) 2\varphi_F - \frac{Q_{dep}}{2C_{ox1}} - \frac{C_{si}}{C_{ox1}}\left(1 + \frac{C_{si}}{C_{ox2}}\right)[V_{GB} - V_{GB}(acc)]$$

$$V_{th1,dep2} = V_{th1,accu2} - \frac{C_{si}}{C_{ox1}}\left(1 + \frac{C_{si}}{C_{ox2}}\right)[V_{GB} - V_{GB}(acc)] \quad \text{Eq(3.2.23)}$$

From the above equation (3.2.18) and (3.2.19) we can attain the net shift in the threshold voltage:-

$$\Delta V_{TF} = [V_{th1}(accu2) - V_{th1}(inv2)] \quad \text{Eq(3.2.24)}$$

$$\Delta V_{TF} = \frac{C_{si}}{C_{ox1}} 2\varphi_F = \frac{\varepsilon_{si} t_{OF}}{\varepsilon_{ox} t_{si}} 2\varphi_F \quad \text{Eq(3.2.25)}$$

this indicates that the shift in the threshold voltage for the SOI devices generally depends upon the device physical parameter such as the thickness of oxide,the silicon film and the dielectric

constant of oxide, so by using the high-k dielectric material in our device with large thickness which is equivalent to the silicon dioxide of thin thickness and generate the similar threshold voltages without generating further SCEs in devices, similarly the slope of the threshold voltage curve is obtained with respect to back-gate voltage by differentiating the equation (3.2.23), the result as follows

$$\frac{dV_{th}}{dV_{GB}} = -\frac{t_{OF}}{t_{si}} \frac{1}{\left(1+{}^{C_{ox2}}/_{C_{si}}\right)} \qquad \text{Eq(3.2.26)}$$

This indicates the variation of front-threshold voltage with respect to back-gate.

3.2.3 COMPUTATION OF THE DRAIN CURRENT OF SOI MOSFET

In order to obtain the value of drain current, decipher it by using the Ohm's law in rudimentary segment of the inversion channel, for front-gate surface and by apply the charge-based model to reach the final current firstly calculate the Q_{inv1} along the y-direction from (y=0) source end to (y= L) drain side. The General equation of drain current on the basis of Ohm's law ia as follows:-[46]

$$I_D = W\mu_n Q_{inv1}(y)\frac{d\varphi_{sF}(y)}{dy} \qquad \text{Eq(3.2.27)}$$

A Solution of drain current in the different region of back-gate is obtained by the postulation of classical gradual- channel, constant-mobility, with no presence of diffusion current means zero concentration gradient, we also consider the uniform silicon doping in the channel region. Further solving the equation (3.2.27), the drain current equation yield from 0 to L.[46]

$$I_D = \frac{W}{L}\mu_n \int_{2\varphi_F}^{2\varphi_F+V_{DS}} Q_{inv1}(y)d\varphi_{SF}(y) \qquad \text{Eq(3.2.28)}$$

By making certain assumptions in order to make the device fully depleted silicon film and consider the thickness of silicon film equivalent to zero either in accumulation or in inversion layer at the interface. On the other hand, we obtain the inversion charge density in the front-channel by rearranging the equation (3.2.14)

$$-Q_{inv1}(y) = C_{ox1}\left(V_{GF} - \varphi_{ms1} + \frac{Q_{ox1}}{C_{ox1}} - \left(1+\frac{C_{si}}{C_{ox1}}\right)\varphi_{SF}(y) + \frac{C_{si}}{C_{ox1}}\varphi_{SB}(y) + \frac{Q_{dep}}{2C_{ox1}}\right) \qquad \text{Eq(3.2.29)}$$

In above equation put the value of $\varphi_{ox1} = \frac{Q_{ox1}}{C_{ox1}}$ which generally indicates sum of charges whether it is depletion charge or inversion charge considered as whole divided by oxide capacitance and value of charge may vary with respect to bias and the value of back-surface potential is calculated by re-arranging the equation (3.2.16)

$$\varphi_{SB}(y) = \frac{C_{ox2}}{C_{si} + C_{ox2}}\left(V_{GB} - \varphi_{ms2} + \frac{Q_{ox2}}{C_{ox2}} + \frac{C_{si}}{C_{ox2}}\varphi_{SF}(y) + \frac{Q_{dep}}{2C_{ox2}} - \frac{Q_{s2}(y)}{C_{ox2}}\right) \quad \text{Eq(3.2.30)}$$

From above calculation of inversion charge density in y-direction and back-surface potential on the basis of different cases regarding back-surface interface to the film from either side drain or source, drain current for different region is estimated.

- Considering the first region where the back interface is accumulated from source to drain side, for this first retain the value of back-gate voltage and the condition for the value of back-gate is $V_{GB} < V_{GB,acc}(L)$ where L is the length of the device to which channel is formed. For this the value of $V_{GB,acc}(L)$ is equal to the back-gate voltage in accumulation minus the drain voltage because in this condition is $\varphi_{SB}(y) = 2\varphi_F + V_{DS}$ thus by using the equation (3.2.16) the results are as follows

$$V_{GB,acc}(L) = V_{GB,acc} - \frac{C_{si}}{C_{ox2}}V_{DS} \quad \text{Eq(3.2.31)}$$

By putting all the values in equation (3.2.28), the drain current in accumulation is obtained, the calculation is as follows

$$I_{D,acc2} = \mu_n \frac{W}{L} \int_{2\varphi_F}^{2\varphi_F + V_{DS}} C_{ox1}\left(V_{GF} - \phi_{ms1} + \frac{Q_{ox1}}{C_{ox1}} - \left(1 + \frac{C_{si}}{C_{ox1}}\right)\phi_{SF}(y) + \frac{C_{si}}{C_{ox1}}\phi_{SB}(y) + \frac{Q_{dep}}{2C_{ox1}}\right) d\phi_{SF}(y) \quad \text{Eq(3.2.32)}$$

By integrating the above equation (3.2.32) with respect to the limits further equation can be solved as

$$I_{D,acc2} = \mu_n \frac{W}{L} C_{ox1}\left[\left[V_{GF}\phi_{SF}(y) - \phi_{ms1}\phi_{SF}(y)\right] + \frac{Q_{ox1}}{C_{ox1}}\phi_{SF}(y) - \frac{1}{2}\left(1 + \frac{C_{si}}{C_{ox1}}\right)\phi_{SF}{}^2(y) + \frac{C_{si}}{C_{ox1}}\phi_{SB}(y)\phi_{SF}(y) + \frac{Q_{dep}}{C_{ox1}}\phi_{SF}(y)\right]_{2\phi_F}^{2\phi_F + V_{DS}} \quad \text{Eq(3.2.33)}$$

Where$\varphi_{SB}(y)$ is equal to zero for calculation of drain current in accumulation region,thus putting the limit for $\varphi_{SF}(y)$ in the above-integrated equation from $2\phi_F to\, 2\phi_F + V_{DS}$ then by substituting the above value in place of $\varphi_{SF}(y)$ the middle portion of drain current somewhat look like as

$$I_{D,acc2} = \mu_n \frac{W}{L} C_{ox1} \left[\left(V_{GF} - \phi_{ms1} + \frac{Q_{ox1}}{C_{ox1}} \right) V_{DS} - \frac{1}{2} \left(1 + \frac{C_{si}}{C_{ox1}} \right) (2\phi_F + V_{DS} - 2\phi_F)^2 + \frac{Q_{dep}}{C_{ox1}} V_{DS} \right] \quad \text{Eq(3.2.34)}$$

On further solving equation (3.2.34) and comparing it with the equation (3.2.18), the final drain current equation is as follows:-

$$I_{D,acc2} = \frac{W}{L} \mu_n C_{ox1} \left[\left[V_{GF} - V_{th1,acc2} \right] V_{DS} - \left(1 + \frac{C_{si}}{C_{ox1}} \right) \frac{{V_{DS}}^2}{2} \right] \quad \text{Eq(3.2.35)}$$

And if the drain voltage reaches it saturation value, drain current equation (3.2.34) 34 is modified as per the value of $V_{DSat,acc2}$ and this is obtained by taking derivate of the drain current with respect to the drain voltage

$$V_{Dsat,acc2} = \frac{V_{GF} - V_{th1,acc2}}{1 + \frac{C_{si}}{C_{ox1}}} \quad \text{Eq(3.2.36)}$$

By putting the value of $V_{DSat,acc2}$ in above equation(3.2.24), the final value of saturate drain current is equivalent to:-

$$I_{Dsat,acc2} = \frac{1}{2} \frac{W}{L} \frac{\mu_n C_{ox1}}{1 + {C_{si}}/{C_{ox1}}} \left(V_{GF} - V_{th1,acc2} \right)^2 \quad \text{Eq(3.2.37)}$$

- On the other hand, consider the second assumption analysis of back-gate interface that is both drain and source is depleted so in order to obtain the drain current at this region, calculated the value of $V_{GB,dep}$ in terms of surface potential, the combination of the capacitance and charge present at the interface, basically the condition that satisfy the depletion region lies between $V_{GB,acc} < V_{GB,dep} < V_{GBinv}$ and the value of V_{GBinv} can be scrutinized above in equation (3.2.21) and in equation equate the value of $\varphi_{ox2} = \frac{Q_{ox2}}{C_{ox2}}$ with minus sign and for back-depleted consider the value of charge at the surface basically as 0, $Q_S = 0$ by all these condition, from equation (3.2.28, 3.2.29, 3.2.30), the drain current in depletion region is calculated and mediator step is as follows:-

$$I_{D,depl2} = \mu_n \frac{W}{L} C_{ox1} \int_{2\phi_F}^{2\phi_F+V_{DS}} \left[\left(V_{GF} - \phi_{ms1} + \frac{Q_{ox1}}{C_{ox1}} - \left(1 + \frac{C_{si}}{C_{ox1}}\right)\phi_{SF}(y) + \frac{C_{si}}{C_{ox1}}\phi_{SB}(y) + \frac{Q_{dep}}{2C_{ox1}}\right)\right] \quad \text{Eq(3.2.38)}$$

Also, by putting the value of $\varphi_{SB}(y)$ in equation (3.2.38) and integrate it simultaneously with respect to the front surface-potential

$$I_{D,depl2} = \mu_n C_{ox1} \frac{W}{L}\left[\left(V_{GF}\phi_{SF}(y) - \phi_{ms1}\phi_{SF}(y)\right) + \frac{Q_{ox1}}{C_{ox1}}\phi_{SF}(y) - \frac{1}{2}\left(1 + \frac{C_{si}}{C_{ox1}}\right)\left(\phi_{SF}(y)\right)^2 + \frac{C_{si}}{C_{ox1}}\phi_{SB}(y)\phi_{SF}(y)\frac{Q_{dep}}{2C_{ox1}}\phi_{SF}(y)\right]_{2\phi_F}^{2\phi_F+V_{DS}} \quad \text{Eq(3.2.39)}$$

Similarly, the integration of $\varphi_{SB}(y)$ that occur in the above drain current equation can be implied as

$$\phi_{SB}(Y) = \left[\frac{C_{ox2}}{C_{si} + C_{ox2}}\left(V_{GB}\phi_{SF}(y) - \phi_{ms2}\phi_{SF}(y) + \frac{Q_{ox2}}{C_{ox2}}\phi_{SF}(y) + \frac{1}{2}\frac{C_{si}}{C_{ox2}}\left(\phi_{SF}(y)\right)^2 + \frac{Q_{dep}}{2C_{ox2}}\phi_{SF}(y)\right)\right]_{2\phi_F}^{2\phi_F+V_{DS}} \quad \text{Eq(3.2.40)}$$

Further solving the integration by putting the value of limit and rearrange all the parts of equation, the final output of drain current can be predicted also with the value taken from the equation of $V_{th1,dep2}$ from equation (3.2.23), the drain current is as follows

$$I_{D,depl2} = \frac{W}{L}\mu_n C_{ox1}\left[\left(V_{GF} - V_{th1,depl2}\right)V_{DS} - \left(1 + \frac{C_{si}}{C_{ox1}(C_{si} + C_{ox2})}\right)\frac{{V_{DS}}^2}{2}\right] \quad \text{Eq(3.2.41)}$$

As the drain voltage increases and reach up to the saturation value, the drain current abruptly changes to drain current saturation. The value of $V_{DSat,dep2}$ is calculated by differentiatating the above equation with respect of drain voltage and consider it equivalent to zero. The final equation is as follows

$$V_{Dsat,depl2} = \frac{V_{GF} - V_{th1,depl2}}{1 + \frac{C_{si}C_{ox2}}{C_{ox1}(C_{si} + C_{ox2})}} \quad \text{Eq(3.2.42)}$$

The following saturation current for depletion region is:-

$$I_{Dsat,depl2} = \frac{W}{L}\frac{1}{2}\frac{\mu_n C_{ox1}}{1+\frac{C_{si}C_{ox2}}{C_{ox1}(C_{si}+C_{ox2})}}\left(V_{GF}-V_{th1,depl2}\right)^2 \quad \text{Eq(3.2.43)}$$

By this method, drain current is estimated and attained their simulation results by using back-gate bias and also we can plot the characteristics between the drain current and front-gate voltage with constant drain-voltages for different back-gate voltages ,correspondingly output characteristic is also examined between the drain current and drain-voltage at different gate-voltage(front) with constant back-gate bias at different back interface and their conclusion are discussed in next chapter, all is good with this analysis and modeling of SOI in order to understand the basic of device and other parameter but as the device is scaled and successively due to scaling the SCEs increases, for this further analysis is going on with number of variations in the above equation , by adding certain terminology and by changing a constant parameter into variable or vice-versa then after so many conclusion, here we perform Analytical modeling of UTBB-FDSOI at scaled channel length and also considering the high-k dielectric material and high metal gate with appropriate work-function and basically focusing on the calculation of inversion charge density defined for once but valid for all regions and also obtained the single drain current equation which holds excellent results for different back-interface either for accumulation interface or for inversion layer interface. So this will reduce our previous work and define a new horizon. After that, we also calculate saturate drain current with mobility and CLM effect for our model.

3.3 ANALYTICAL MODELING OF DRAIN CURRENT OF UTBB FDSOI MOSFET

For modeling a device equation, we designed a device with an asymmetric n-channel configuration with different oxide thickness for the front-gate oxide(t_{oxf}) and buried oxide thickness(t_{oxb}) for this modeling of drain current, our calculation is ongoing with the calculation of threshold voltage in terms of gate voltage in such a manner to attain the turn-on condition of the device which quantitatively termed as the gate-voltage at which the lowest amount of carrier charge sheet density at effective conductive path reaches a threshold voltage of the charge density and the value of the threshold charge density is obtained in terms of drain bias and another geometrical parameter. So basically for all this assumptions, first calculate the threshold voltage based on the density of carrier present at the front and the back channel simultaneously as in this carrier density is electron which can be observed from the previous analysis of the researcher. And it has been accurately observed that the threshold voltage in terms of gate voltage at which the sum of the carrier densities from both sides of the channel is equivalent to the doping density.

Similarly for this modeling (N-type UTBB FDSOI), we start from this concept of threshold voltage but also add the feature of effective conductive path which is possible if we consider the device with thinner front-gate oxide which implies that the carrier density is equivalent to doping density of silicon body at the effective conductive path somewhere in the channel from the front-interface. Basically, it can be defined in terms of equation as[43]:-

$$n_i e^{\frac{\phi(x_c,y_m)}{V_{th}}} = N_A \qquad Eq(3.3.1)$$

the term which is defined in exponential is equivalent to the channel position at the conductive path and at that position the minimum potential, equivalent to gate voltage which shows the lesser subthreshold region and SCEs. N_A Doping density Silicon body, V_{th} is the thermal voltage and n_i is the intrinsic carrier concentration of silicon. The potential at the minimum conductive path $\phi(x_c, y_m)$ can be defined as[44]:-

$$\phi(x_c, y_m) = \phi 1(x_c, y_m) + \phi 2(x_c, y_m) V_{gf1} \qquad Eq(3.3.2)$$

The value of the constant terms related to surface potential value can be obtained from the previous stimulated result of the calculation of the surface potential of the asymmetric FDSOI MOSFET with lightly doped silicon body because silicon film considered is thin with lightly doped which help in reducing the mobility degradation and also eliminate the random dopant fluctuations adverse effects in order to control the device characteristics in better way. On the other hand, we must carry out the simple analytical solution for the potential distribution along the channel of silicon which may be in square or in rectangular in nature. Before proceeding, consider a systematic view of the FD transistor with desired cross-sectional area as shown below in figure 3.4 where t_{si} is silicon body thickness, L is channel length, t_{oxf} front oxide thickness and, t_{oxb} back oxide thickness along with front gate electrode and the backplane that further acts as the back-gate when biasing is applied to it. The silicon body is lightly doped with the acceptor atom, N_A is the acceptor atoms concentration. The threshold voltage is determined or adjusted by proper work-function of the metal, a gate material. If we consider the 3-D view of our model device then W channel width is also considered.

The 2-D Poisson's equation with apporpriate boundary conditions is used in order to derive the potential distribution. In weak inversion, the potential distribution within the silicon channel for an asymmetric device is written as follows

$$\frac{\delta^2\phi(x,y)}{\delta^2 x}+\frac{\delta^2\phi(x,y)}{\delta^2 y}=\frac{qN_A}{\varepsilon_{si}} \qquad 0<x<t_{si}\,,0<y<L \qquad Eq(3.3.3)$$

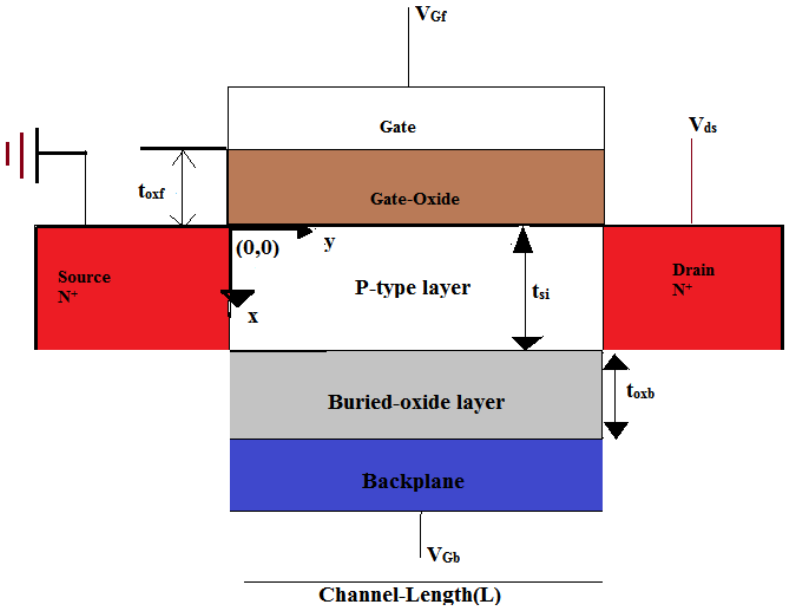

FIGURE 3.4 Cross-Section View of UTBB FDSOI MOSFET

By presuming, the vertical electrical field at the gate-oxide interface, along x-direction by applying the Gauss' law, the boundary condition at the channel-gate oxide interface is written as:-

$$\frac{d\phi(x,y)}{dx}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{(\varphi_{sy}(y)-V_{gf1})}{t_{oxf}}\ at\ x=0 \qquad Eq(3.3.4)$$

$$\frac{d\phi(x,y)}{dx}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\left(V_{gb1}-\varphi_{sb}(y)\right)}{t_{oxb}}\ at\ x=t_{si} \qquad Eq(3.3.5)$$

By solving the above equation (3.3.3, 3.3.4, 3.3.5) and on the basis of prior assumptions with proper simulation, the potential distribution can be obtained as[43]

$$\phi(x,y)=A+\frac{1}{\left(e^{\frac{2L}{\lambda}}-1\right)}\left[(V_{bi}+V_d-A)\left(\left(e^{\frac{L+y}{\lambda}}\right)-\left(e^{\frac{L-y}{\lambda}}\right)\right)\right.$$
$$\left.+(V_{bi}-A)\left(\left(e^{\frac{2L-y}{\lambda}}\right)-\left(e^{\frac{y}{\lambda}}\right)\right)\right] \qquad Eq(3.3.6)$$

In this A is constant, V_{bi} is the built-in potential, V_d is the drain voltage, ε_{ox} is the dielectric constant of the oxide, ε_{si} is the silicon dielectric constant while, A is defined as the parameter which is equivalent to the sum of the gate voltages along[43]

$$A = \alpha V_{gf1} + \beta V_{gb1} \qquad Eq(3.3.7)$$

with some constant added to each gate voltage which is defined in terms of the physical parameter of the device which is channel length, the thickness of the front-oxide, back-oxide, dielectric constant of silicon or the oxide. Further solving the equation(3.3.6) the expression for potential is defined as

$$\emptyset(x,y) = A + \frac{e^{L+y/\lambda}}{e^{2L/\lambda}-1}(V_{bi}+V_d) - A\frac{e^{L+y/\lambda}}{e^{2L/\lambda}-1} - \frac{e^{L-y/\lambda}}{e^{2L/\lambda}-1}(V_{bi}+V_d) + A\frac{e^{L-y/\lambda}}{e^{2L/\lambda}-1}$$
$$+ V_{bi}\frac{e^{2L-y/\lambda}}{e^{2L/\lambda}-1} - V_{bi}\frac{e^{\frac{y}{\lambda}}}{e^{2L/\lambda}-1} - A\frac{e^{2L-y/\lambda}}{e^{2L/\lambda}-1} + A\frac{e^{\frac{y}{\lambda}}}{e^{2L/\lambda}-1} \qquad Eq(3.3.7a)$$

By rearranging the equation(3.3.7a)

$$\phi(x,y) = A\left[1 - \frac{e^{L+y/\lambda}}{e^{2L/\lambda}-1} + \frac{e^{L-y/\lambda}}{e^{2L/\lambda}-1} - \frac{e^{2L-y/\lambda}}{e^{2L/\lambda}-1} + \frac{e^{\frac{y}{\lambda}}}{e^{2L/\lambda}-1}\right] + \frac{e^{L+y/\lambda}}{e^{2L/\lambda}-1}(V_{bi}+V_d)$$
$$- \frac{e^{L-y/\lambda}}{e^{2L/\lambda}-1}(V_{bi}+V_d) + V_{bi}\frac{e^{2L-y/\lambda}}{e^{2L/\lambda}-1} - V_{bi}\frac{e^{\frac{y}{\lambda}}}{e^{2L/\lambda}-1} \qquad Eq(3.3.7b)$$

In equation (3.3.7b) put the value of constant A from the equation(3.3.7)

$$\phi(x,y) = \alpha V_{gf1} + \beta V_{gb1}\left[1 - \frac{e^{L+y/\lambda}}{e^{2L/\lambda-1}} + \frac{e^{L-y/\lambda}}{e^{2L/\lambda-1}} - \frac{e^{2L-y/\lambda}}{e^{2L/\lambda-1}} + \frac{e^{\frac{y}{\lambda}}}{e^{2L/\lambda-1}}\right] + \frac{e^{L+y/\lambda}}{e^{2L/\lambda-1}}(V_{bi}+V_d) -$$
$$\frac{e^{L-y/\lambda}}{e^{2L/\lambda-1}}(V_{bi}+V_d) + V_{bi}\frac{e^{2L-y/\lambda}}{e^{2L/\lambda-1}} - V_{bi}\frac{e^{\frac{y}{\lambda}}}{e^{2L/\lambda-1}} \qquad Eq(3.3.7c)$$

From the equation (3.3.7c) , rearranging the final equation of potential distribution in such a manner that the constant βV_{gb1} is come along with front surface potential $\phi 1(x,y)$ as here we have to analyse the change in front-surface potential with respect to change in back-gate voltage. So, the final equation of potential distribution in both the direction which defines the effective

conductive path value(x_c) and the value of the minimum potential at that position(y_m) is written as follows on the basis of equation(3.3.6) the value of two constant of equation (3..3.7c)

$$\phi 1(x_c, y_m) = \frac{\left(\left(e^{\frac{2L-y_m(x_c)}{\lambda(x_c)}}\right)-\left(e^{\frac{y_m(x_c)}{\lambda(x_c)}}\right)V_{bi}\right)+\left(\left(e^{\frac{L+y_m(x_c)}{\lambda(x_c)}}\right)-\left(e^{\frac{L-y_m(x_c)}{\lambda(x_c)}}\right)(V_{bi}+V_{ds})\right)}{\left(e^{\frac{2L}{\lambda(x_c)}}\right)-1} +$$

$$\frac{\left(\left(e^{\frac{L-y_m(x_c)}{\lambda(x_c)}}\right)-\left(e^{\frac{-y_m(x_c)}{\lambda(x_c)}}\right)V_{bi}\right)+\left(\left(e^{\frac{L}{\lambda(x_c)}}\right)-\left(e^{\frac{y_m(x_c)}{\lambda(x_c)}}\right)\left(\left(e^{\frac{y_m(x_c)}{\lambda(x_c)}}\right)-1\right)V_{gb1}\beta(x_c)\right)}{\left(e^{\frac{2L}{\lambda(x_c)}}\right)-1} \qquad Eq(3.3.8)$$

$$\phi 2(x_c, y_m) = \alpha(x_c)\left[\frac{\left(1-\left(e^{\frac{-y_m(x_c)}{\lambda(x_c)}}\right)V_{bi}\right)+\left(\left(e^{\frac{L}{\lambda(x_c)}}\right)-\left(e^{\frac{y_m(x_c)}{\lambda(x_c)}}\right)\right)}{\left(e^{\frac{L}{\lambda(x_c)}}\right)+1}\right] \qquad Eq(3.39)$$

Also the constant in the equation (3.3.7) shows an abrupt change in the value, with a shift in the silicon thickness by a factor of effective conductive path(x_c) this can be written as

$$\alpha(x_c) = \frac{\varepsilon_{si}t_{oxb} + \varepsilon_{ox}(t_{si} - x_c)}{\varepsilon_{si}(t_{oxf} + t_{oxb}) + \varepsilon_{ox}t_{si}} \qquad Eq(3.3.10)$$

$$\beta(x_c) = \frac{\varepsilon_{si}t_{oxf} + \varepsilon_{ox}x_c}{\varepsilon_{si}(t_{oxf} + t_{oxb}) + \varepsilon_{ox}t_{si}} \qquad Eq(3.3.11)$$

Where, V_{gb1} and V_{gf1} are equivalent to the subtraction of the applied gate- voltage with the flat-band voltage, which indirectly equal to the work-function, a difference between the metal gate and the silicon for front side and back side respectively. Thus, from the equation (3.3.1) and equation (3.3.2) the value of the threshold voltage is written as:-

$$V_{tf} = V_{fbf} + \frac{V_{th}}{\phi 2(x_c, y_m)} ln\left(\frac{N_A}{n_i} e^{-\frac{\phi 1(x_c, y_m)}{V_{th}}}\right) \qquad Eq(3.3.12)$$

From this equation it is clear that the front-threshold voltage (V_{tf}) depends on the back-gate voltage(V_{Gb}) which is observed from the constant term of the potential distribution that is $\phi 1(x_c, y_m)$. It is better from our previous modeling because in this threshold voltage for every applied back-bias is described or examined by only one equation which is shown above in

equation (3.3.12), only to this equation back-bias can be either in accumulated region or in depleted region result obtained from this is more efficient from the previous one or may be approximately same, in this analysis our next model parameter is the charge sheet density defining the channel charges as this is also based on the charge-based model in order to calculate the drain current equation basically we calculated the charges in the subthreshold region or in the strong inversion region. On the basis of the bulk MOSFET theory the charge is in terms of charge sheet density in a different region, we can be derive from the basic equation of the charge in terms of capacitance and voltage, in order to describe the charge sheet density in inversion mode in terms of voltages which can be described as:-

$$Q'_I = -\sqrt{2q\varepsilon_s N_A}\left[\left(\sqrt{\varphi_S + \phi_t e^{\frac{(\varphi_S - 2\phi_F)}{\phi_t}}} - \sqrt{\varphi_S}\right)\right] \qquad Eq(3.3.13)$$

This charge equation is valid in the entire region such as weak, moderate and inversion region, as previous discussed the surface potential φ_S and is equal to the Fermi-potential which indicates the onset inversion. Consider the second term in the above equation (3.3.13) which equivalent to constant

$$\varepsilon = \phi_t e^{\frac{(\varphi_S - 2\phi_F)}{\phi_t}} \qquad Eq(3.3.14)$$

In weak inversion, the value of surface potential is less than the twice of Fermi potential so the function$\sqrt{\varphi_S + \varepsilon}$ can be expressed in term of Taylor series expansion mostly upto second term

$$\sqrt{\varphi_S + \varepsilon} = \sqrt{\varphi_S} + \frac{1}{2\sqrt{\varphi_S}}\,\varepsilon \qquad Eq(3.3.15)$$

On the basis of above two equations, the equation (3.3.13) can be represented as charge in weak inversion region

$$Q'_I = -\frac{\sqrt{2q\varepsilon_s N_A}}{2\sqrt{\varphi_S}}\left[\phi_t e^{\frac{(\varphi_S - 2\phi_F)}{\phi_t}}\right] \qquad Eq(3.3.16)$$

After this next step is to mention the surface potential in terms of voltages and in UTBB model the equation (3.3.16) can be modified and presented charge sheet density in weak inversion region which is same equation with some minus of drain voltage in exponential term

$$Q_i^{wi} = n_f C_{oxf} V_{th} e^{\frac{(V_{gf} - V_{tf} - n_f V_y)}{n_f V_{th}}} \qquad Eq(3.3.17)$$

Where the function V_y is varied across the channel from 0 to V_{ds} equivalent to source and drain sides respectively and n_f is the ideality factor, similarly, the charge sheet density equation in the strong inversion mode is obtained from the bulk MOSFET charge sheet approximation concepts which are written as

$$Q_i^{si} = C_{oxf}\left(V_{gf} - V_{tf} - n_f V_y\right) \qquad Eq(3.3.18)$$

Thus, these two values of charges density in weak and strong inversion can be represented in single equation term in order to observe the charge density from Subthreshold to the region of strong inversion in single row, and this can be carried out by the help of interpolating function and the normalized sheet charge density is equivalent to

$$q_i = n_f ln\left(1 + e^{\frac{(V_{gf} - V_{tf} - n_f V_y)}{n_f V_{th}}}\right) \qquad Eq(3.3.19)$$

Where the value of ideality factor is a comprises of constant which is observed from the previous references attains at the interface region basically from the front-side, after all calculation next step is to derive the expression for drain current by considering the charge in an entire region or channel, not in sheet form. On the basis of a drift-diffusion equation, the drain current somewhere in the mid of channel along y-direction is given by:-

$$I_{ds} = W\mu C_{oxf} V_{th} q_i \frac{dV_y}{dy} \qquad Eq(3.3.20)$$

For solving the equation 3.3.20 which is of drain current first we have to calculate the value of $\frac{dV_y}{dy}$ which can be obtained by differentiating the equation 3.3.19 and in that equation the value of $q_i = \frac{Q_i}{C_{oxf}}$ and differentiate the equation with respect to y the result is equivalent to

$$\frac{dq_i}{dy} = \frac{n_f}{V_{tf}}\left(e^{-q_i/n_f} - 1\right)\frac{dV_y}{dy} \qquad Eq(3.3.21)$$

The calculation of drain current first is calculated normally without considering any effect like CLM or Velocity saturation with constant mobility and the scholar presented the solution of this

equation result by solving it with dilogarithm function but for our modeling it can be further solved by generalized integration method where the integrate value varies from the normalized charges in source and drain side electrodes, the equation with integration limits and with the value of derivate function can be expressed as

$$\int_0^L I_{ds} = W\mu C_{oxf} V_{th} \frac{V_{th}}{n_f} \int_{q_s}^{q_d} \frac{q_i}{\left(e^{-q_i/n_f} - 1\right)} \frac{dq_i}{dy} \qquad Eq(3.3.22)$$

Upon solving the left-hand side of integration factor of equation (3.3.22)

$$I_{ds} = \frac{W}{L} \mu C_{oxf} V_{th} \frac{V_{th}}{n_f} \int_{q_s}^{q_d} \frac{q_i}{\left(e^{-q_i/n_f} - 1\right)} \frac{dq_i}{dy} \qquad Eq(3.3.23)$$

And the right-hand side of the integration of equation (3.2.22) can be solved by considering the integration by parts formula for this certain assumption can be considered:-

$$\left(e^{-q_i/n_f} - 1\right) = u \qquad Eq(3.3.24)$$

On differentiating the equation (3.3.24) in order to calculate the value of dq_i which is equivalent to

$$dq_i = -\frac{du(n_f)}{e^{-\frac{q_i}{n_f}}} \; and \; again \; by \; putting \; final \; value \; dq_i = -\frac{du(n_f)}{u+1} \qquad Eq(3.3.25)$$

By putting all these values in above equation of I_{ds} but as if now do not focus on the limits, the equation can be addressed as

$$I_{ds} = \frac{W}{L} \mu C_{oxf} V_{th} \frac{V_{th}}{n_f} \int \frac{(\ln u + 1){n_f}^2}{u(u+1)} du \qquad Eq(3.3.26)$$

And using the formula of integration by parts, assume the second terms further constant, all this can be done in order to simplify the equation and solve easily without considering whole terms So the constant is equivalent to

$$v = \frac{1}{u(u+1)} \qquad \text{Eq (3.3.27a)}$$

$$I_{ds} = \frac{W}{L}\mu C_{oxf} V_{th} \frac{V_{th}}{n_f} {n_f}^2 \int v.\ln(u+1)\, du \qquad \text{Eq (3.3.27b)}$$

$$I_{ds} = \frac{W}{L}\mu C_{oxf} V_{th} \frac{V_{th}}{n_f} {n_f}^2 \ln(u+1) \int v\, dv - \int \frac{1}{u+1} \int v du \qquad Eq(3.3.27c)$$

While the integration of v can be calculated on the basis of basic integration formula

$$\int v dv = \int \frac{1}{u(u+1)} du \qquad Eq(3.3.27d)$$

$$\int v dv = \int \frac{1}{\left(u+\frac{1}{2}\right)^2 - \left(\frac{1^2}{2}\right)} du \qquad Eq(3.3.27e)$$

$$v = \frac{1}{2 * 0.5} ln\left(\frac{u+\frac{1}{2}-\frac{1}{2}}{u+\frac{1}{2}+\frac{1}{2}}\right) \qquad Eq(3.3.27f)$$

By putting the value of integration factor of v from the equation (3.3.27f to 3.3.27c) then equation become as

$$I_{ds} = \frac{W}{L}\mu C_{oxf} V_{th} \frac{V_{th}}{n_f} {n_f}^2 \ln(u+1) \frac{1}{2 * 0.5} ln\left(\frac{u+\frac{1}{2}-\frac{1}{2}}{u+\frac{1}{2}+\frac{1}{2}}\right) - \int \frac{1}{u+1}\left[\frac{1}{2 * 0.5} ln\left(\frac{u+\frac{1}{2}-\frac{1}{2}}{u+\frac{1}{2}+\frac{1}{2}}\right)\right] \qquad Eq(3.3.27g)$$

On solving the second terms of the equation (3.3.27g) again by integration by part again and final equation can be expressed as and in that equation putting the value of constant u from equation (3.2.24)

$$I_{ds} = \frac{W}{L}\mu C_{oxf} V_{th} \frac{V_{th}}{n_f} {n_f}^2 \ln(u+1)\left(\ln\left(\frac{u}{u+1}\right)\right) + ln\left(\frac{u}{u+1}\right) \qquad Eq(3.3.28)$$

$$I_{ds} = \frac{W}{L}\mu C_{oxf} V_{th} \frac{V_{th}}{n_f} {n_f}^2 \ln\left(e^{-q_i/n_f}\right)\left[ln\left(1-e^{-q_i/n_f}\right) + ln\left(1-e^{-q_i/n_f}\right)\right] \qquad Eq(3.3.29)$$

And neglecting the higher order integration terms from equation (3.3.28) by assuming that the reciprocal value of the u tends to decrease in terms of the area under the curve. So, after

reduction, the equation (3.3.29) can be written. On further solving the equation the final equation of I_{ds} by using the Taylor series expansion of logarithms and neglecting the higher order terms in the series

$$I_{ds} = \frac{W}{L}\mu C_{oxf} V_{th} \frac{V_{th}}{n_f} {n_f}^2 \frac{-q_i}{n_f}\left[ln\left(1 - e^{-q_i/n_f}\right) + ln\left(1 - e^{-q_i/n_f}\right)\right] \quad Eq(3.3.30a)$$

$$I_{ds} = \frac{W}{L}\mu C_{oxf} V_{th} \frac{V_{th}}{n_f} {n_f}^2 \left(1 - \frac{q_i}{n_f}\right)\left[ln\left(1 - e^{-q_i/n_f}\right)\right] \quad Eq(3.3.30b)$$

$$I_{ds} = \frac{W}{L}\mu C_{oxf} V_{th} \frac{V_{th}}{n_f} {n_f}^2 \left(\frac{q_i}{n_f} - 1\right)\left[\left(e^{-q_i/n_f}\right) + \frac{1}{2}\left(e^{-q_i/n_f}\right)^2\right] \quad Eq(3.3.30c)$$

By replacing the exponential terms in their power series and neglecting the higher order terms

$$I_{ds} = \frac{W}{L}\mu C_{oxf} V_{th} \frac{V_{th}}{n_f} {n_f}^2 \left(\frac{q_i}{n_f} - 1\right)\left[1 - \frac{q_i}{n_f} + \frac{1}{2}\left(\frac{q_i}{n_f}\right)^2 + \frac{1}{2}\left(1 - \frac{2q_i}{n_f} + \frac{1}{2}\left(\frac{2q_i}{n_f}\right)^2\right)\right] Eq(3.3.31)$$

On further multiplication of the $\left(\frac{q_i}{n_f} - 1\right)$ to the larger bracket and solve it, the final drain current equation is evaluated as follows with every other parameter is constant and also included the limits to varies from normalized charge at source end to drain end

$$I_{ds} = \frac{W}{L}\mu C_{oxf} V_{th} \frac{V_{th}}{n_f} {n_f}^2 \left[\frac{3}{2} - \frac{7}{2}\frac{q_i}{n_f} + \frac{5}{2}\left(\frac{q_i}{n_f}\right)^2\right]_{q_d}^{q_s} \quad Eq(3.3.32)$$

By putting the limits in the drain current equation (3.3.32) the final equation is obtained as:-

$$I_{ds} = \frac{W}{L}\mu C_{oxf} V_{th} \frac{V_{th}}{n_f} {n_f}^2 \left[\frac{3}{2} - \frac{7}{2}\frac{(q_s - q_d)}{n_f} + \frac{5}{2}\left(\frac{(q_s - q_d)}{n_f}\right)^2\right] \quad Eq(3.3.33)$$

If in our model effective mobility is considered instead of constant mobility then due to phenomenon of velocity saturation, there is a slight change in the drain current equation that is mobility factor is changed and in equation of drain current instead of μ, μ_{eff} and the value of mobility can be expressed as:-

$$\mu = \frac{\mu_{eff}}{1 + \frac{\mu_{eff}}{v_{sat}}\left|\frac{d\phi_s}{dy}\right|} = \frac{\mu_{eff}}{1 + \frac{\mu_{eff} * V_{th}}{v_{sat}}\frac{dq_i}{dy}} \quad Eq(3.3.34a)$$

The value of change in inversion charge density with respect to channel length can be obtained from equation(3.3.19) that can be solved as differentiating the equation(3.3.19) to obtain $\frac{dq_i}{dy}$ which is further obtained in equation(3.3.21), then the equation of drain current with effective mobility can be expressed as[44] with modification in the drain current equation

$$I_{ds} = \frac{\mu_{eff}}{L + \frac{\mu_{eff} V_{th}((q_s - q_d))}{v_{sat}}} W C_{oxf} V_{th} \frac{V_{th}}{n_f} {n_f}^2 \left[\frac{3}{2} - \frac{7}{2}\frac{(q_s - q_d)}{n_f} + \frac{5}{2}\left(\frac{(q_s - q_d)}{n_f}\right)^2\right] \quad Eq(3.3.34)$$

Now as we mentioned above that for this analysis we considered the channel-length modulation effect, which occurs in saturation region, results in the shortening of the channel length by the net shift to original length and this is due to the applied drain bias at very high range, thus in order to calculate the value of net shift in channel length, we have to model a drain saturation voltage, which is quite obviously obtains by differentiating the equation (3.3.34) for that only consider the third terms of the square brackets because this is only the factor which is mainly dominant above threshold voltage, and explicitly depends on the drain voltage at y=L, the value of normalized charge at the source and the drain end is calculated by equation (3.3.19) by putting the value of voltage that varies from 0 to L along y-direction which is 0 and drain voltage respectively. Finally, the value of drain saturation voltage is calculated by differentiating the drain current equation with respect to drain voltage and make it equivalent to zero.

After rearranging the equation of drain current which also considered the mobility degradation effect, the evaluated equation of drain current is attained as follows :-

$$I_{DS} = \frac{1}{2n_f} \frac{W \mu_{eff} C_{ox1} v_{sat} {V_{th}}^2 (q_s - q_d)}{\frac{L v_{szt}}{(q_s - q_d)} + \mu_{eff} V_{th}} \quad Eq(3.3.35)$$

Before differentiation consider certain assumption and then apply the differentiation quotient formula which depicted as

$$a = W \mu_{eff} C_{ox1} v_{sat} {V_{th}}^2 , b = \mu_{eff} V_{th}(2n_f), c = L v_{sat}(2n_f) \quad Eq(3.3.36a)$$

$$I_{DS} = \frac{a(q_s - q_d)}{c(q_s - q_d)^{-1} + b} \quad Eq(3.3.36)$$

On differentiating it with respect to drain current so, in above equation, a factor q_d depends on drain voltage as it indicates the normalized charge at the drain end.

$$\frac{dI_{DS}}{dV_d} = \left[\frac{\left(c\left((q_s - q_d)\right) + b(q_s - q_d)^2\left(a * \frac{dq_d}{dV_d}\right) - c.a(q_s - q_d)\frac{dq_d}{dV_d}\right)}{(c(q_s - q_d)^{-1} + b)^2}\right] \qquad Eq(3.3.37a)$$

$$\left(c\left((q_s - q_d)\right) + b(q_s - q_d)^2\left(a * \frac{dq_d}{dV_d}\right) - c.a(q_s - q_d)\frac{dq_d}{dV_d}\right) = 0 \qquad Eq(3.3.37b)$$

On further solving the equation (3.3.37b) and rearrange it, the equation seems like

$$-2ac\frac{dq_d}{dV_d} + ba({q_s}^2 + {q_d}^2 - 2q_s q_d)\frac{dq_d}{dV_d} = 0 \qquad Eq(3.3.37e)$$

In this the derivate equation q_d is un-known so; first we calculate the value of the normalized charge at drain side by using equation (3.3.19)

$$q_d = n_f ln\left(1 + e^{\frac{V_{gf} - V_{tf} - n_f V_d}{n_f V_{th}}}\right) \qquad Eq(3.3.37f)$$

By using equation (3.3.37f) the equation (3.3.37e) and putting the value of constant a, b and c from above equation (3.3.36a), result is attains as:-

$$2v_{sat}L = \mu_{eff}V_{th}\left({q_s}^2 + \left[n_f ln(1 + e^x)\right]^2 - 2q_s n_f ln(1 + e^x)\right) \qquad Eq(3.3.37g)$$

Where $x = \frac{V_{gf} - V_{tf} - n_f V_d}{n_f V_{th}}$ and apply the power series expansion of logarithm and exponential and further replacing the higher order terms the quadratic equation with making constant y= $ln(1 + e^x)$ the equation results as

$$2\frac{c}{b} = \left[{q_s}^2 + {n_f}^2 y^2 - 2q_s n_f y\right] \qquad Eq(3.3.37h)$$

By quadratic equation formula apply the power series expansion of logarithm and exponential and further replacing the higher order the value of x is equivalent to

$$x = n_f V_{th} \sqrt{\left(-{n_f}^2 {V_{th}}^2\right) + \left(-{n_f}^2 {V_{th}}^2\right)\left(\frac{q_s}{n_f} + \sqrt{\frac{2{q_s}^2}{{n_f}^2} - \frac{2c}{b}}\right)} \qquad Eq(3.3.38)$$

By putting the value of x the value of saturation drain voltage is

$$\frac{V_{gf} - V_{tf} - n_f V_{dsat}}{n_f V_{th}} = n_f V_{th} \sqrt{\left(-{n_f}^2 {V_{th}}^2\right) + \left(-{n_f}^2 {V_{th}}^2\right)\left(\frac{q_s}{n_f} + \sqrt{\frac{2{q_s}^2}{{n_f}^2} - \frac{2L v_{sat}}{\mu_{eff} V_{th}}}\right)} \; Eq(3.3.39)$$

$$V_{dsat} = \sqrt{\left(\frac{{v_{sat}}^2}{\mu_{eff}}\right) + \frac{2q_s v_{sat} V_{th} L}{\mu_{eff}}} - \frac{v_{sat} L}{\mu_{eff}} + \frac{q_s V_{th}}{n_f} - q_s V_{th} \qquad Eq(3.340)$$

After finding the drain saturation voltage the bet shift in the channel length with the application of higher drain bias can be taken from the bulk technology CLM effect with a fitting parameter in order to improve the performance of the device in saturation region and also due to improve the SCE.

$$\Delta L = \frac{V_{ds} - V_{dsat}}{V_E} \; and \; the \; effective \; channel \; length \; is \; L_{eff} = L - \Delta L \; \text{Eq(3.3.41)}$$

Putting the value of effective channel length in place of channel length in drain current equation and finally obtain the drain-current equation including the CLM effect.

Chapter 4
RESULT AND DISSCUSION

An analytical drain model has been developed for an asymmetrical FDSOI MOSFET and the model equations has been plotted through MATLAB tool.Various Drain Current Characteristics has been taken by varying different device parameters such as buried oxide thickness, back gate voltage. Result has been calculated by considering the high-k dielectric material, hafnium di-oxide, in our analysis has as front gate oxide. The model is compared with the simulations results obtained through the TCAD Co-genda by considering the CVT mobility model. Generally, the model parameter for an FDSOI MOSFET which has taken into consideration during simulation is as follows. For an asymmetrical device with silicon thickness $t_{si} = 7nm$ with uniform channel doping concentration $N_A = 10^{16}/cm^3$ and the doping concentration of source and drain is $N_{SD} = 10^{21}/cm^3$ also the doping of the substrate is maintained to be highly doped, $N_{SB} = 10^{18}/cm^3$, and the thickness of the front gate oxide and buried oxide is $t_{oxf} =$ 1.55 nm and $t_{oxb} = 25$nm respectively, with the channel length, L of 30 nm and channel width W=0.5um.

4.1 Threshold Voltage Calculation

Figure 4.1 depicts the threshold voltage analysis of an asymmetrical FDSOI MOSFET, the variations in front-gate threshold voltage along with the back-gate bias are considered for a device with channel length L=30 nm and silicon thickness of 7nm while front-gate effective oxide is 2nm with buried oxide thickness of 25nm, and suitable doping densities are required by the device. From the equation (3.2.14) and (3.2.16) which are the gate voltage equations for front gate and back-gate, as equation describes the dependencies of threshold voltage value defined on the basis of surface potential that is created at the back and front interface with the application of back-gate voltage and depicted the change in region of operation of the device.

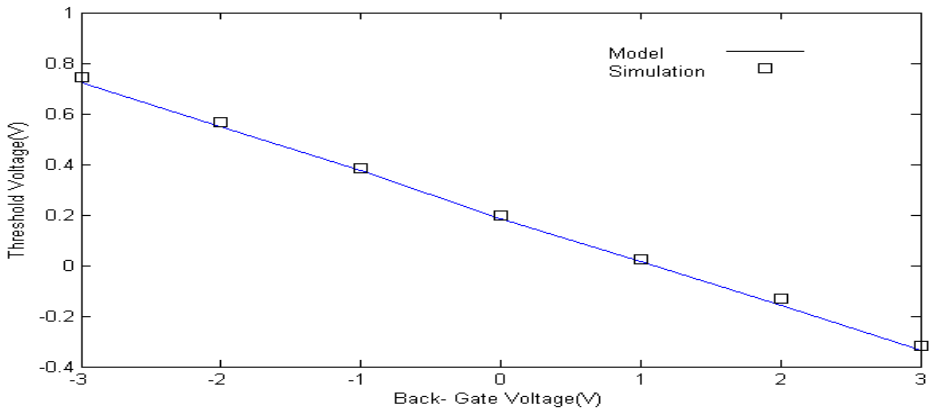

Figure 4.1 Threshold Voltages Versus Back-Gate Voltage

If we fixed the front-gate potential, V_{GF}, there is some front surface potential, φ_{SF}, then by changing the back-gate potential V_{GB}, it shifts the front-surface potential as its denoted by the equation(3.2.14) and (3.2.16) that is positive back- gate voltage, pulls down the front-surface potential and lowering the front-gate threshold voltage making invert the front-surface, as two gates are electrostically coupled, while on the other hand with negative back- gate voltage makes the front-surface potential increases thus, increase the front-gate threshold voltages. this observation is clearly understood from the figure 4.1 and the figure is plotted by using the MATLAB tools for equation (3.3.12) which also decipts the same dependencies and also the model and TCAD simulations found to be in good agreement with each other.

4.1.1 Threshold Voltage at different Buried Oxide Thickness

Threshold voltage is the important parameter for the device analysis which indicates the onset of the device operation and it varies easily with minute variations in the device parameter whether it is thickness of the devices, length or the doping concentration of the device, which changes the devices characteristics by its own so it is necessary to maintain the appropriate relation between the operating power and the drive current of the devices. Here, we have observed the threshold voltage variations with respect to the back-gate voltage of an asymmetrical FDSOI MOSFET, at different buried oxide thickness. This indicates the exclusive characteristics of an FDSOI that tune that threshold voltage varies to lower values if possible even after device fabrication. Figure 4.2 it is obtained that considering the active layer thickness of 7nm and channel length of 30nm, generally buried oxide is considered to minimize the SCEs and electrostatic coupling from the drain to the channel, it has been observed that threshold voltage decrease with the thicker buried

oxide for all channel length, and the impact of back-gate voltage on front and back surface is reduced and device characteristics changes, so it needed to be thinner to achieve better stability.

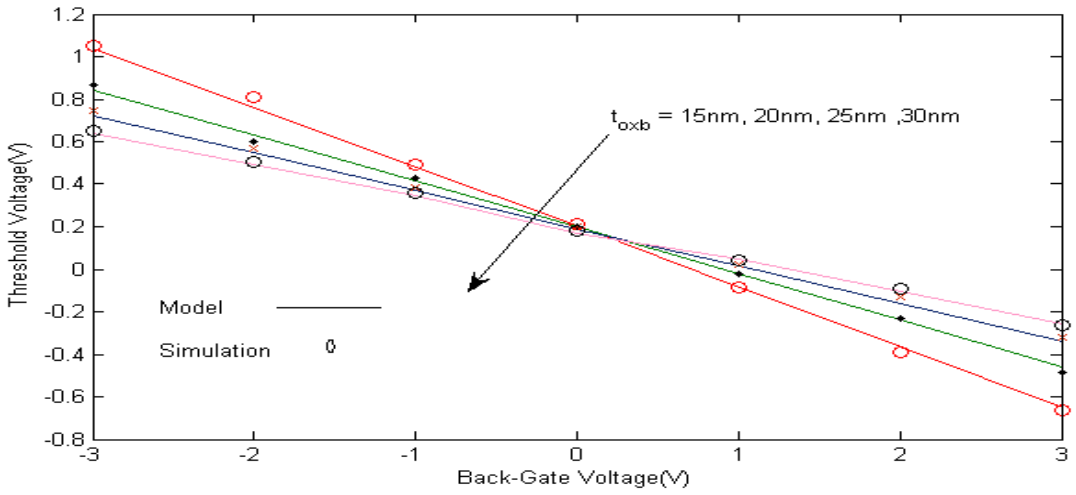

Figure 4.2 Threshold Voltage Along With Back-Gate Voltage at Different Buried Oxide Thickness

4.1.2 Threshold Voltage at different channel doping

Figure 4.3 analyze the threshold voltage with respect to back-gate bias at different channel doping concentration, and it has been observed that threshold voltage increase with the channel doping concentration but the device get more prone to short- channel immunity.

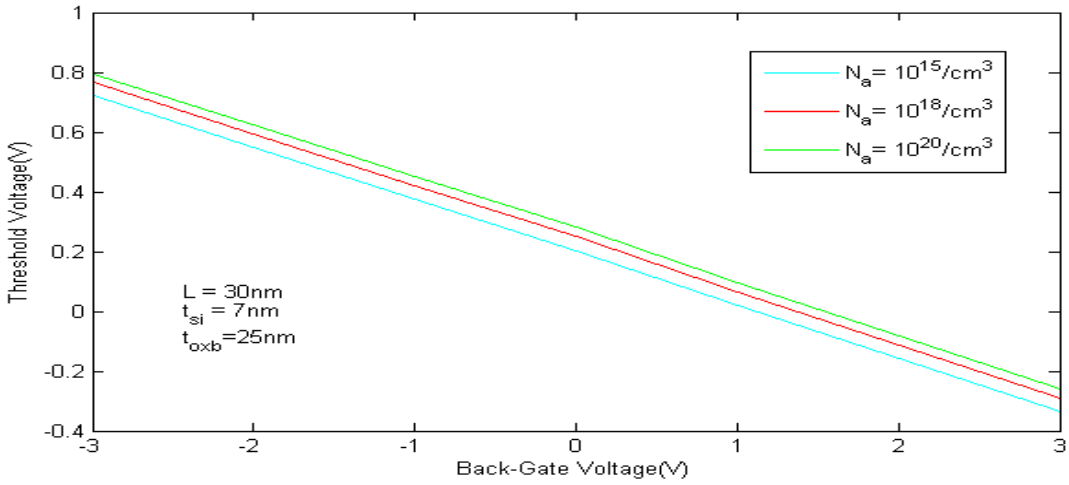

Figure 4.3 Threshold Voltage Along With Back-Gate Voltage At Different Doping Concentration

4.2 Potential along with channel length

With the fixed applied front-gate voltage and back-gate voltage at different drain-voltages, the potential (v) is calculated from the model and validate with the TCAD along with the channel length L= 30nm. It has been observed from the above graphs that the potential is fixed at L=0nm which is at source side and at L=30nm which is at the drain voltage is changed. For first curve, the line obtained from model which has attained its values around 0.96v at 30 nm is due to applied drain bias of 0.1v and second curve obtained from model which has attained its values as 1.52v at 30nm is due to applied drain bias of 1v. The shifts in the curve has been attained due to the shift in the potential as we move from source to drain side, as the potential at the drain side is keep on increasing due to the presence of more charge carrier accumulated near the drain side, the analysis is considered with baising at the source terminal.

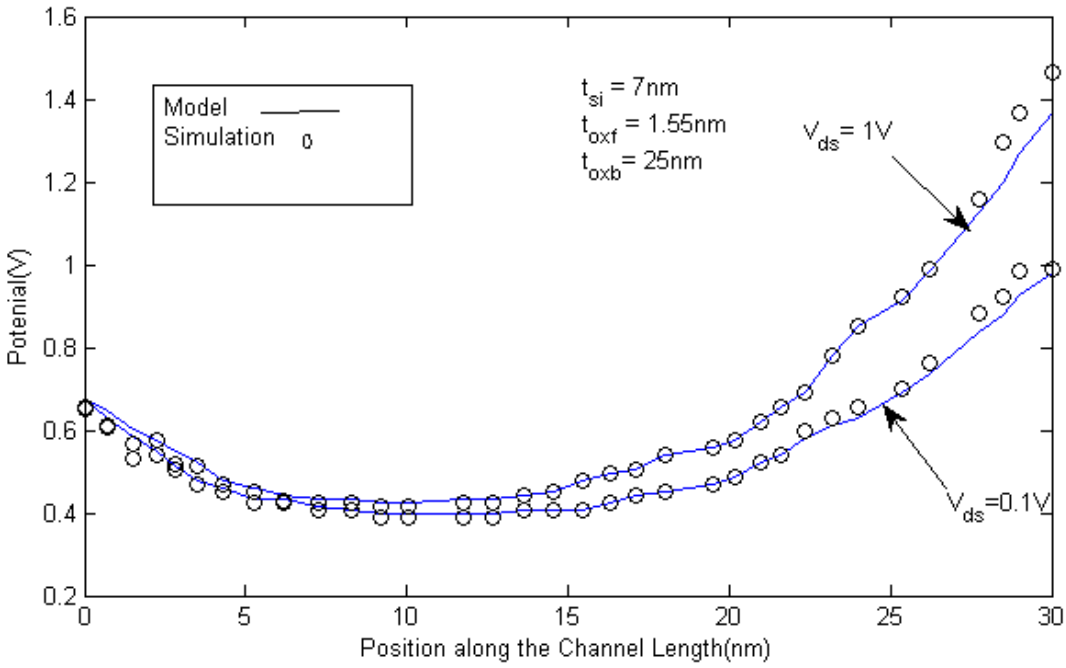

Figure 4.4 Curve Showing the Variations of Potential Across the Channel Length

As we also know from the concepts of energy band diagram that, if we keep on increasing the drain voltage the energy band diagram at the drain side keep on decreasing by decreasing the potential barrier between the source and drain terminal in the channel region, increasing the potential energy at the drain side due to the accumulation of carrier. Figure 4.4 also indicate the same concepts, the potential is lowered at the mid value of the channel length and its levels shift as drain voltage varies.

4.3 Drain Current Characteristics

There are two kind of drain current characteristics as transfer and output characteristics with respect to front-gate voltage and drain current respectively.

4.3.1 Transfer Characteristics

Figure 4.5 and Figure 4.6 respresent the transfer characteristics of FDSOI MOSFET for drain bias 0.1v and 1v respectively when different back-gate bias is applied. Doping in active layer has been sustained to be $1x10^{16}$ $/cm^3$ with the thickness of 7nm. The value of channel length has been considered 30nm with the front-gate oxide thickness of 1.55nm which is effective oxide thickness as compared to the usual oxide and the buried oxide thickness is 25nm has been considered.

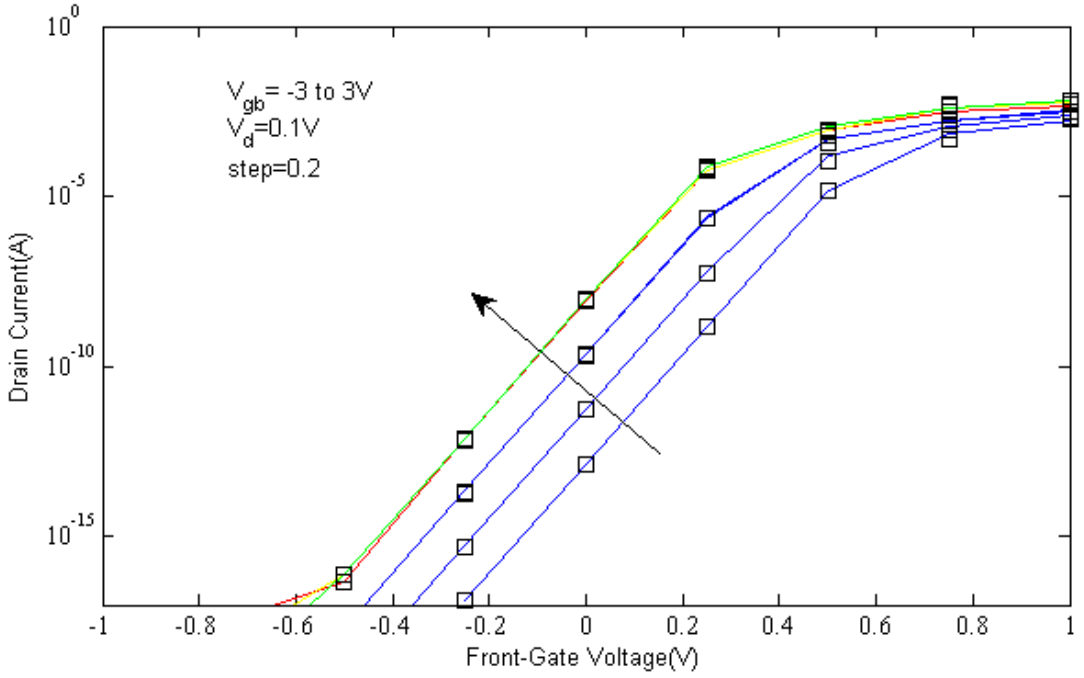

Figure 4.5 Drain Current versus Front-Gate voltage at Different Back-Gate Voltage at Constant Drain Voltage(V_{ds} = 0.1v)

In our analysis effective Silicon-oxide thickness is considered in order to avoid tunneling or other leakages, the value of the threshold voltage has been carried out in above graphs at 25nm buried oxide thickness, All the simulations has been carried out using the TCAD tool and model has been plotted through the MATLAB. Both the graphs which has been obtained from both tools shows the good relationship with minute variations, all the analysis of drain current can be carried

by considering reference terminal to be at source. The basic difference between the two figures 4.4 and 4.5 is observation of the shift in onset of the drain current as drain voltage varied from 0.1V to 1V.

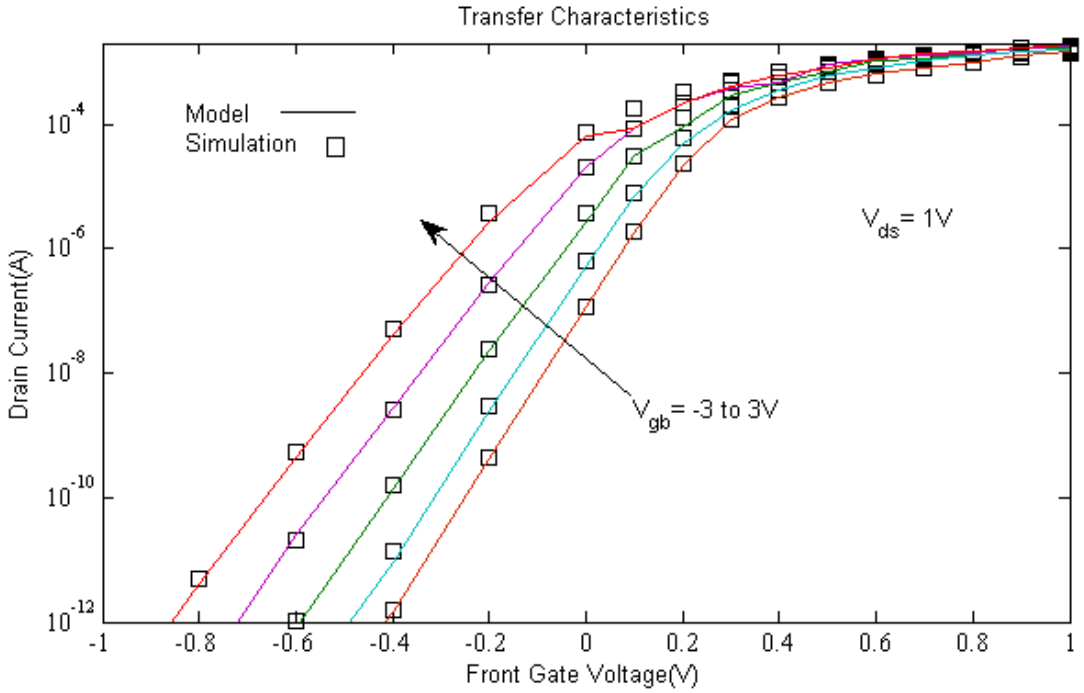

Figure 4.6 Drain Current versus Front-Gate voltage at Different Back-Gate Voltage at Constant Drain Voltage(V_{ds} = 1v)

Basically these characteristics indicate that with the positive back-bias voltage, the back-channel interface gets inverted first making the device on at lower threshold voltage, make it more prone to SCE and at this region device is control by back-gate rather than by front-gate.

4.3.3 Output Characteristics

The characteristics has been described in figure 4.7 of FDSOI MOSFET with the different values of the front-gate bias by considering the back-gate in an depletion or an onset of inversion region

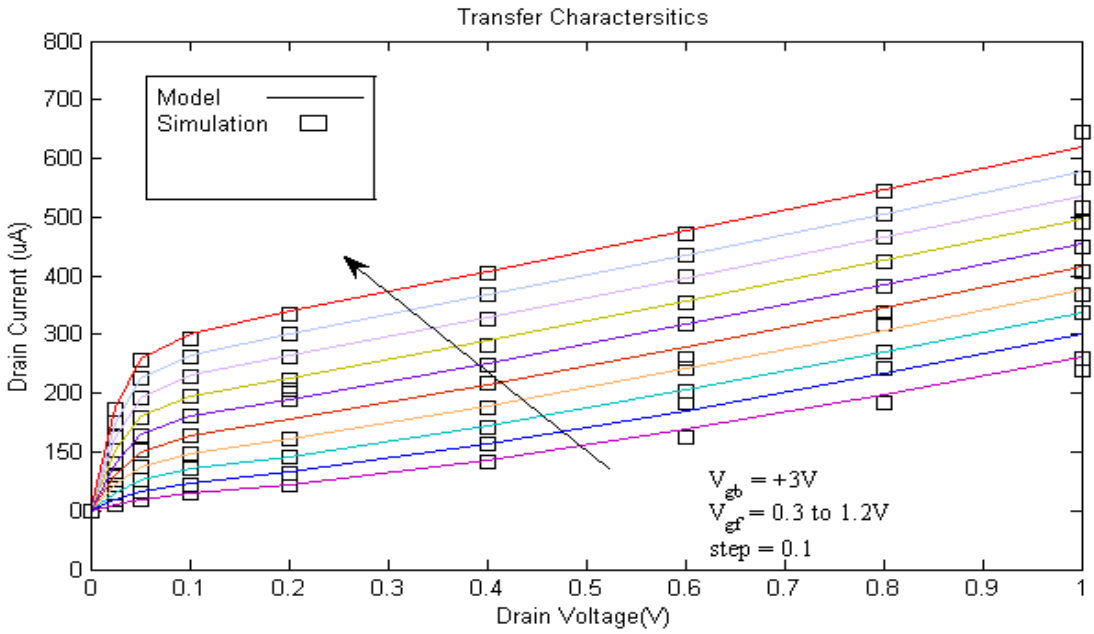

Figure 4.7 Drain current versus Drain voltage at Different Front-Gate Voltage

All the analysis has been carried out with the consideration of the biasing with respect to the source terminal, and the model output has been obtained from the MATLAB tool by plotting the equation which is calculated by an analytical modeling of the drain current and it has been observed that at lower drain voltage values, drain current is increasing but it starts saturate at higher drain voltages which is quite analogous with the traditional bulk MOSFET output characteristics with increased drain current values has been attained from this model. While on the other hand the front-gate voltage variations indicate the regions of operations of the devices. The model and the simulations results show the good agreement with appropriate output drain current values.

4.4 Transfer Characteristics at Different Buried oxide thickness

After analysis the threshold voltage of an asymmetrical FDSOI MOSFET with different buried oxide thickness along with the variation of back-gate biasing. We have observed the shift in the the threshold voltage due to reduction of buried-oxide thickness, the variations has been observed in figure 4.2 with the change in thickness of the buried oxide as it indicate the strong coupling effect in the device, and by the help of equation (3.2.14) and (3.2.16), the relation between the front-gate potential and back-gate potential has been depicted. The figure with respect to this analysis can be examined as below:-

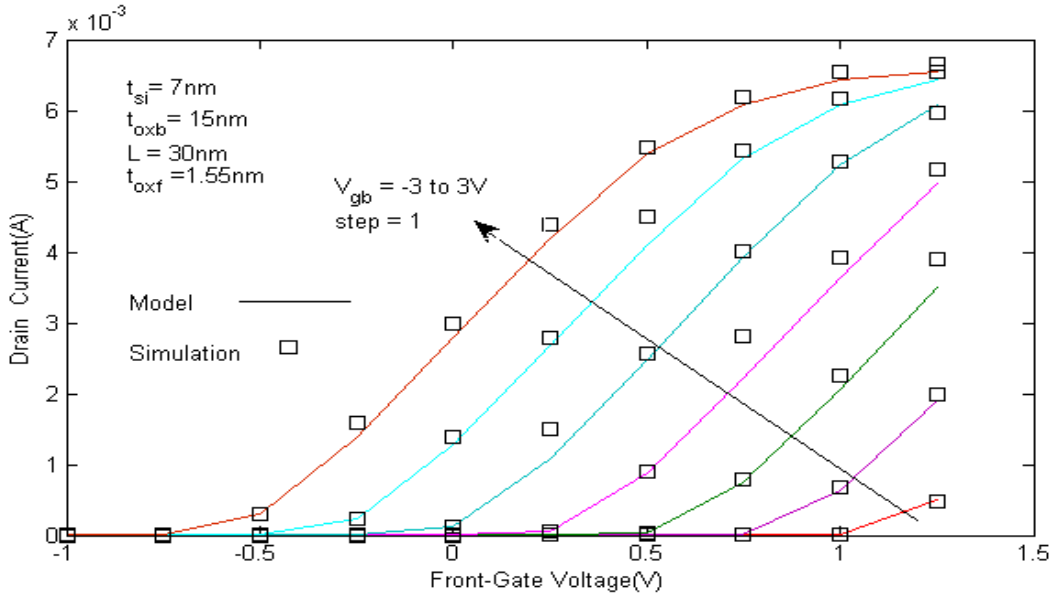

Figure 4.8(a) Drain-Current Curve at Buried Oxide Thickness 15nm

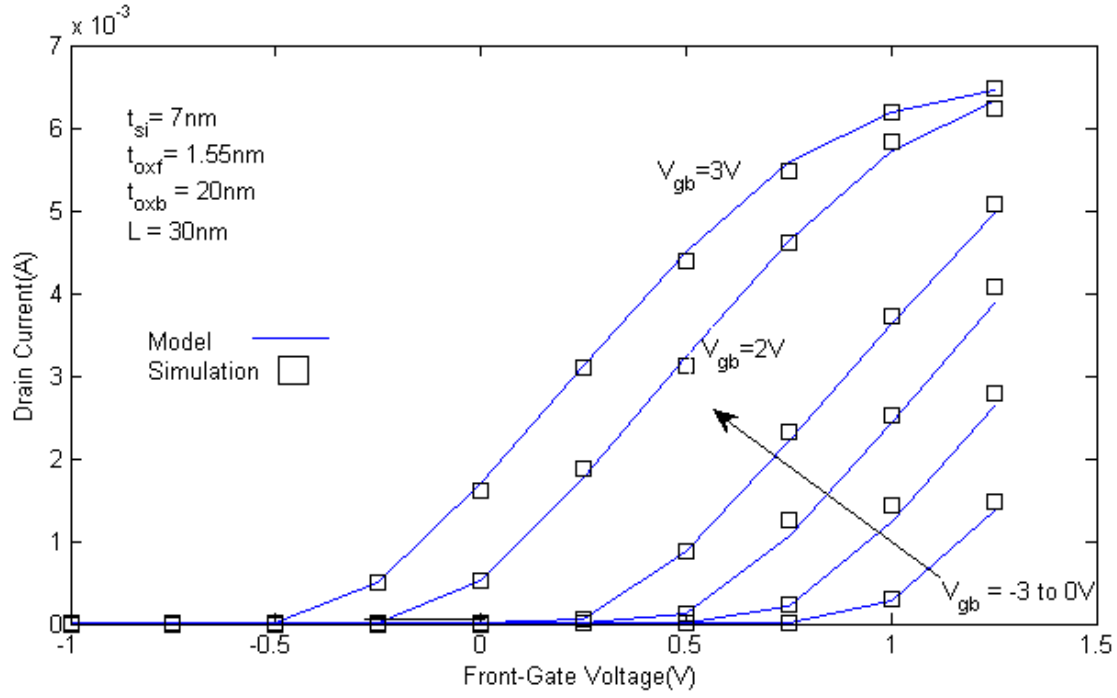

Figure 4.8(b) Drain-Current Curve at Buried Oxide Thickness 20nm

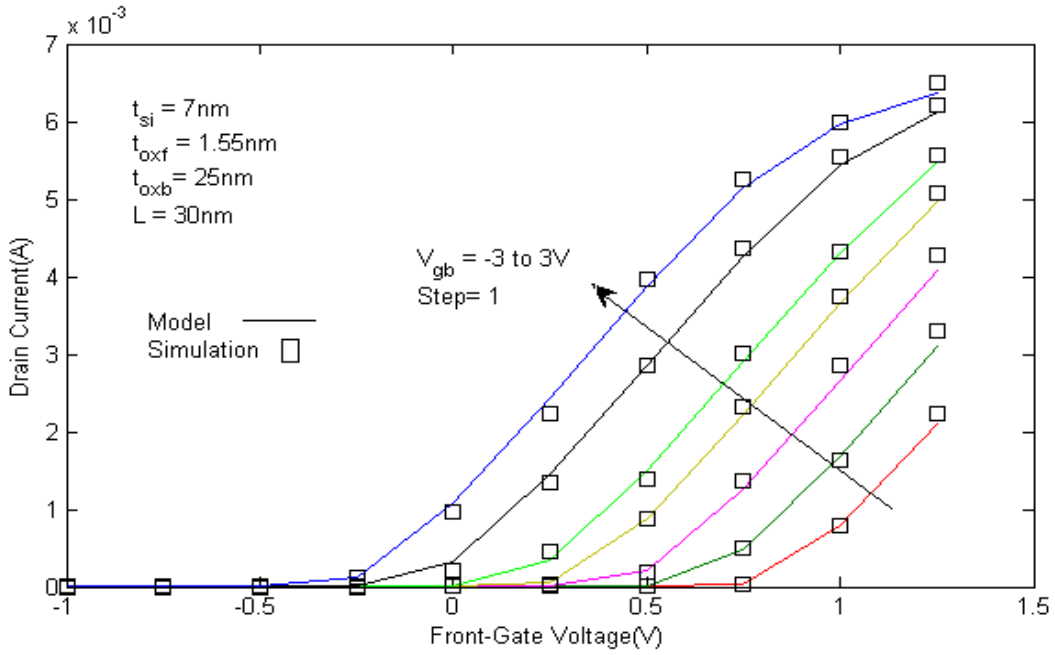

Figure 4.8(c) Drain-Current Curve at Buried Oxide Thickness 25nm

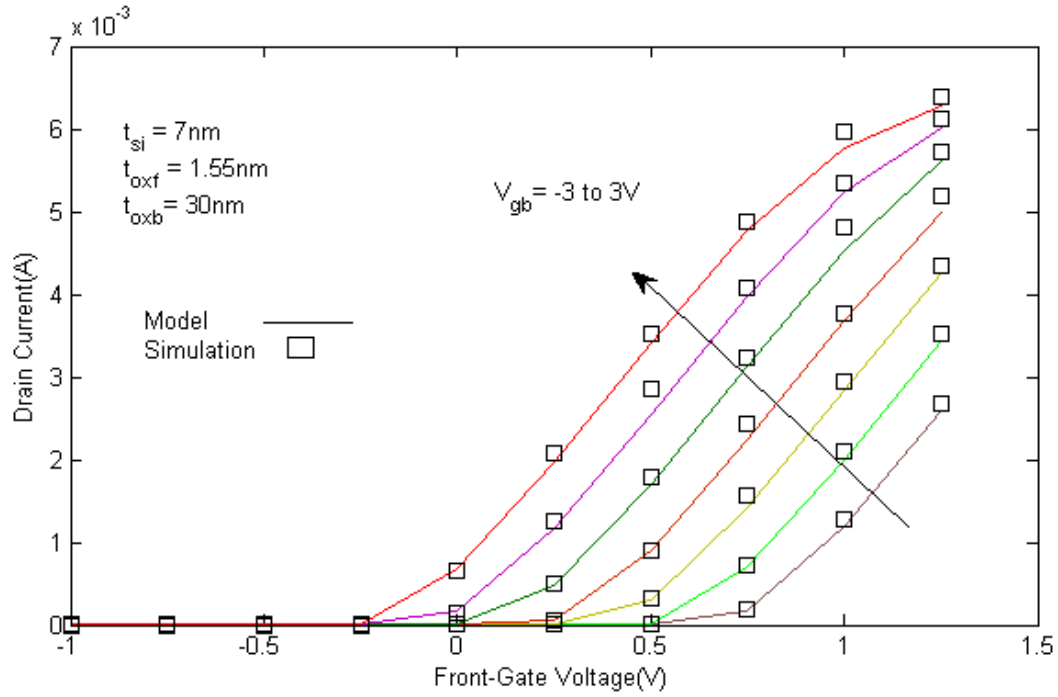

Figure 4.8(d) Drain-Current Curve at Buried Oxide Thickness 30nm

The entire above figure can be analyzed at fixed drain voltage bias and channel doping concentration to be p-type as $1*10^{16}/cm^3$ and biasing with respect to source terminal are considered.

Chapter 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion

An analytical drain current model of an asymmetrical FDSOI MOSFET has been presented. By this model we have calculated various parameters which have been studied and results have been calculated. Parameters such as potential along the channel, threshold voltage of the device and the drain characteristics of the devices, has been obtained from an analytical model have been obtained by the MATLAB tool and with simulation result has been obtained through TCAD are compared.

In this work, the effect on threshold voltage (V_{tf}) on device characteristics has been studied by varying the device parameter that is buried oxide thickness (t_{oxb}) and channel doping concentration (N_A) with respect to back-gate voltage(V_{gb}). It has been observed that the front threshold voltage of the device can be tuned by varying the back-gate biasing because front-surface potential is a function of back-surface potential. By this method we can control the device with back-gate bias. It is observed that to achieve better stability we should fabricate our device by using thinner buried oxide, t_{oxb} .The drain charachteristics of the device have been calculated by considering the high-k dielectric material which is used with equivalent oxide thickness in order to reduce the outcomes due to silicon di-oxide thickness scaling. For an analytical analysis the 2-D Poisson equations has been considered and basic concepts of conventional bulk-MOSFET with certain assumption, as closed form solution of Poisson equation is not available. Here in our work we present the comparison study of the drain current by considering front-gate oxide as hafnium di-oxide with certain drain voltages and it has been observed that high drive current has obtained when we use the hafnium di-oxide and it improvement in $\frac{I_{on}}{I_{off}}$ current ratio. By all our analysis we have attained the good agreement of our model and simulation result upto desired extents with certain assumptions and some variations are also neglected on the other hand.

5.2 Future Scope

The model which we have developed on certain device parameters shows the improved results with respect to PDSOI MOSFET, and here we simply carried out the basic draft of the nano-scale devices with certain variations in the parameters, more work can be done with possible extensions

or already undergoing inorder to approach another higher level. According to my model, the possible outcomes can be represented as follows:-

1. Threshold voltage is highly shifted due to change in the various structural parameters so, these parameters need to be optimized in order to achieve the stability in the threshold voltages.
2. Analysis can be improved with consideration of oxide trapped charges and better high-k dielectric material with proper understanding of the back-gate bias impact.
3. Use of strained silicon, gate oxide stack and instead of using the single gate material the dual gate material with proper work-function inorder to maintain the fixed positions of surface potential aligned to certain length as whole device structure potential along the length is not affected by change in parameter of like work-function of the gate material, drain voltage, this dual material concepts will be used inorder to further suppress the SCEs.
4. Improvement of source and drain resistance can be possible by providing appropriate stacked region in drain and source along with normal N-type doping which finally improve the drive current capability.
5. Along with the buried oxide layer, the region of ground-plane can also be used so that the electrostatic characteristic can be improved or threshold voltage become stable.
6. The complete AC analysis for RF Applications can be done in future with possible change in the design inorder to meet the criteria in which device is used.
7. Analysis of the developed model can be approached with consideration of quantum effects for detailed analysis of device to achieve proper results in nano-scale.

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