AN ANALYTICAL STUDY OF HIGH POWER SCHOTTKY BARRIER DIODE ON 4H SILICON CARBIDE (SiC) WAFERS

A Thesis

SUBMITTED FOR THE AWARD OF THE DEGREE OF

DOCTOR OF PHILOSOPHY

BY

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NOVOMBER-2010

CERTIFICATE

Certified that the thesis entitled ***"AN ANALYTICAL STUDY OF HIGH POWER SCHOTTKY BARRIER DIODE ON 4H SILICON CARBIDE (SiC) WAFERS"*** being submitted by Mr. Rajneesh Talwar to the Department of Electronics and Communication Engineering, Thapar University, Patiala in fulfillment of the requirements for the award of degree of "Doctor of Philosophy" is a record of bonafide research work carried out by him. He has worked under my guidance and supervision and fulfilled the requirements of submission of this thesis which has reached the requisite standard. The matter presented in this thesis does not incorporate any material previously published or written by any other person except for references in the text. The results contained in this thesis have not been submitted in part or full to any other institute or university for the award of a degree.

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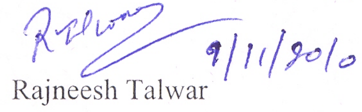
ACKNOWLEDGEMENT

Although the knowledge may exist everywhere yet the Teacher is the point where it shines and spreads as light. I am extremely glad and thankful to God for giving me a chance to work under the supervision and guidance of Dr.A.K.Chatterjee, Professor and Head, Department of Electronics and Communication Engineering, Thapar University, Patiala who helped me to grow out of the ashes of my shortcomings and failures. His charismatic, hard working, honest personality spreads the knowledge and enlightenments in the lives of not only his students but also humanity. To me, he is next to God & parents who was always with me through thick and thin. Also Mrs. C. Chatterjee, wife of Dr.A.K.Chatterjee, has equally contributed to completion of this work by sparing Dr.Chatterjee after college hours for me and deserves special thanks.

I am grateful to Dr.K.K.Raina, Deputy Director & Dean of Faculty Affairs, Thapar University, Patiala and Dr. Ravinder Agarwal, Head, University Scientific Instrumentation Centre, Thapar University, Patiala for their valuable guidance, support, sympathetic and encouraging attitude throughout this work.

I am also greatful to Dr Susheel Mittal, Dean (Research & Sponsored Projects) for always encouraging to complete the work in time and keeping a check on it. I am modestly bowing my head at the feet of the divine Lord to thank them all for their love, support and sacrifices. I wish to express my thanks to all persons who with their encouraging, caring words, constructive criticism and suggestions have contributed directly or indirectly in a significant way towards completion of this work. I gratefully acknowledge for the best wishes and prayers of my friends. A boat held to its moorings will see the floods pass by; but detached of its moorings, may not survive the flood. The support of all the members of my family kept me encouraging to work even while facing the blues. I take pride in being the son of ideal parents who sacrificed their little joys to bring me to the realization of my dreams and their hopes. It is said that realization comes to those who are immersed in love. I owe a lot to my family members. It is my parents who being teacher‘s are responsible to provide me the encouragement for research work and for my falling in love with academics. I am also thankful to my brothers Mr. Sanjay

and Mr. Ajay who supported me from time to time during my research work. I am grateful to my wife, Mrs. Nidhi Talwar who encouraged me constantly in completing this work; to my daughter, Arunima who remained deprived of my love and care during this period. I am laying before you the result of numerous sleepless nights, strenuous hard work, determined and gritty solutions of the fights with my own self, but everything is possible only with the grace of Almighty.



Rajneesh Talwar

ABSTRACT

Silicon carbide (SiC) has been under intensive investigation as an enabling material for a variety of new semiconductor devices in areas where silicon devices cannot effectively compete. These include high-power high-voltage switching applications, high temperature electronics, and high power microwave applications in the 1 - 10 GHz frequency range. In recent years, activity in silicon carbide (SiC) device development has increased considerably due to the need for electronic devices capable of operation at high power levels and high temperature. The main strength of silicon carbide is that it can resist high field strengths; it offers better heat-conducting capacity than copper at room temperature and it has a large energy band gap, which means that electrical components continue functioning even when the temperature rises. With very high thermal conductivity (~5.0 W/cm), high saturated electron drift velocity (~2.7 x 10^7 cm/s) and high breakdown electric field strength (~3 MV / cm), SiC is a suitable material of choice for high temperature, high voltage, high frequency and high power applications. Schottky barrier diodes (SBD's) are used as high-voltage rectifiers in many power switching applications. Whenever current is switched to an inductive load such as an electric motor, high-voltage transients are induced on the lines. To suppress these transients, diodes are placed across each switching transistor to clamp the voltage excursions. PN junction diodes could be used for this application, but they store minority carriers when forward biased and extraction of these carriers allows a large transient reverse current during switching. Schottky barrier diodes are rectifying metal-semiconductor junctions, and their forward

current consists of majority carriers injected from the semiconductor into the metal. Consequently, SBD's do not store minority carriers when forward biased, and the reverse current transient is negligible. This means the SBD can be turned off faster than a PN diode and dissipates negligible power during switching.

SiC Schottky barrier diodes are especially attractive because the breakdown field of SiC is about 8× higher than in silicon. In addition, because of the wide bandgap, SiC SBD's should be capable of much high temperature operation than silicon devices. SiC SBD can be fabricated with the 4H/SiC material and with Ti, Ni and Au etc Schottky metals. But the performance of Schottky diode will depend on the barrier height of the metal. Lower barrier height gives less voltage drop in forward bias but gives a higher leakage current. Special edge termination is required to minimize field crowding at the edge of the metal contact.

A 4H-SiC Schottky Barrier diode has much higher breakdown voltages because of a ten times greater electric field strength of SiC compared with silicon. 4H-SiC unipolar devices have higher switching speeds due to the higher bulk mobility of 4H-SiC compared to other polytypes. The most important parameters that quantify the efficient design of 4H-SiC Schottky barrier diode are blocking voltage (V_B), Specific-on-resistance (R_{on-sp}) and forward voltage drop (V_F). For rectifiers the static on-state losses can be expressed in the forward voltage drop over the diode (V_F) and the specific on-resistance (R_{on-sp}) in the drift region, which accommodates the specified blocking voltage.

In SiC SBD the epilayer plays an important role in device design. For Schottky diode the switching power losses are very low and design strategy

is to minimize the static power losses for a rated blocking voltage. The most important design parameters are consequently the drift resistance, epitaxial doping and Schottky contact properties (barrier height and current ideality factor).At the time of fabrication of SiC SBD the drift region is lightly doped so that it can support the high blocking voltage and could be used for high power application. But when it is lightly doped the on-resistance of device will increase and power dissipation across the device will also increase .So there is a tradeoff between the doping level and the on-resistance of the device. So it is necessary to optimize the device performance at a particular level according to the application requirements.

The research work carried out here on 4H-Silicon Carbide Schottky barrier diode has been an attempt to understand the performance of the device with respect to power dissipation and breakdown voltage for a linearly graded doping profile in the drift region of the device. The doping profiles used are uniformly doped and linearly graded doping profiles. Although a lot of work has been has been described in the literature over the last two decades, no specific work has been reported in which the graded profiles have been used in the drift region of 4H-SiC Schottky Barrier Diode (SBD) for this type of analysis. The ultimate aim for making this study is to provide a linearly graded profile in the drift region of SBD with lower doping at the top of the device to a higher doping near the drain. This type of profile will help in increasing the breakdown voltage while at the same time will reduce the resistance at the lower end of the device and thereby reduce the overall specific on-resistance. In this work, it has been established that the power dissipation is minimum in the linearly graded profile evaluated at a current density of 1000 Amps/cm^2. Hence it is possible to design and develop 4H-SiC SBD's which can yield higher breakdown voltages at a lower device

thickness by using linearly graded drift region. Thinner devices with higher breakdown voltages and lower power dissipation can be developed by using linearly graded profiles in the epitaxially grown drift regions of 4H-SiC Schottky barrier diodes.

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ABBREVIATIONS AND SYMBOLS

CVD	: Chemical Vapor Deposition
eV	: Electron Volt
HTCVD	: High Temperature Chemical Vapor Deposition
HVDC	: High Voltage Direct Current
INTER	: International Thermonuclear Experimental Reactor
LPE	: Liquid Phase Epitaxy
MESFET	: Metal-Semiconductor Field Effect Transistor
MOSFET	: Metal-Oxide Semiconductor Field Effect Transistor
SBD	: Schottky Barrier Diode
SBH	: Schottky Barrier Height
SiC	: Silicon Carbide
SiO_2	: Silicon dioxide
VPE	: Vapor Phase Epitaxy
E_G	: Energy bandgap
E_C	: Energy of conduction band edge
E_{fm}	: Metal Fermi Level
ϕ_m	: Metal Work Function
ϕ_S	: Semiconductor Work Function
E_{fs}	: Semiconductor Fermi Level
E_0	: Vacuum Level

ϕ_{Bn}	: Barrier height of SBD with n-type semiconductor
ϕ_{Bp}	: Barrier height of SBD with p-type semiconductor
ϕ_B	: Barrier height
V_{bi}	: Built-in voltage
χ_S	: Electron affinity of semiconductor
$\in_S$	: Permittivity of semiconductor
$\in_0$	: Permittivity of free space
V_a	: Applied voltage to Schottky Contact
N_d	: Doping concentration of n-semiconductor
J	: Current Density
J_F	: Forward Current Density
V_F	: Forward Voltage Drop
η	: Ideality Factor
A^*	: Richardson's constant
k	: Boltzman's constant
T	: Temperature
q	: Electronic Charge
$\Delta\phi_b$	: Potential Barrier lowering
n_i	: Intrinsic Carrier Concentration
Γ_g	: Generation time
C	: Capacitance

A : Schottky Diode Area

a : Width of Schottky contact

V_n : Potential between conduction band and Fermi level under flat band conditions

δ : Interfacial film width

I : Current

R_S : Series Resistance

V_B : Breakdown Voltage

E_c : Critical electric field

R_{on-sp} : Specific on-resistance

μ_n : Electron mobility

W : Depletion width

J_L : Leakage Current Density

E_m : Maximum Electric Field

V_R : Reverse Bias Voltage

P_D : Power Dissipation

α : Concentration gradien

CHAPTER 1

INTRODUCTION

1.1 PREAMBLE

SiC is attractive for applications stated earlier because of its extreme thermal stability, wide bandgap energy and high breakdown field. The thermal stability of SiC promises long term reliable operation at high temperatures, but it also presents problems in certain fabrication steps, e.g. selective doping, where impurities must be introduced by ion implantation due to the exceedingly low diffusion coefficients of common dopant impurities at reasonable processing temperatures. Because of the wide bandgap energy (3.0 eV and 3.25 eV for the 6H and 4H polytypes respectively), leakage currents in SiC are many orders of magnitude lower than in silicon and the intrinsic temperature is well over 800°C. These electronic properties make SiC attractive for high temperature electronic applications. In addition, the breakdown field in SiC is around 8x higher than in silicon. This is critical for power switching devices, since the specific on-resistance scales inversely as the cube of the breakdown field. Thus, SiC power devices are expected to have specific on-resistances 100 - 200x lower than comparable silicon devices [1]. Finally, SiC is the only compound semiconductor which can be thermally oxidized to form a high quality native oxide (SiO_2).

Although it offers substantial advantages over silicon, SiC is still immature as a semiconductor material. Single crystal wafers of SiC have only been commercially available since around 1990 [2] and a number of critical material and processing issues are still under active investigation. The main limitations of the technology are in the area of crystal growth and will be addressed in more detail below. In addition, certain critical fabrication processes are still under development.

The most important of these fabrication issues are :

(i) activation of ion implanted impurities, (ii) formation of thermally stable low resistance ohmic contacts and (iii) thermal oxidation (or deposition) of high quality dielectric films suitable for MOS devices. In the following sections a review of the current status of the technology in four critical areas: crystal growth, selective doping, ohmic contact formation and thermal oxidation is presented.

Before the mid-1950's, SiC was available only through the industrial Acheson process for making abrasive materials [3]. In 1955, a laboratory sublimation process for growing α-SiC crystals was developed by J. A. Lely at Philips Research Labs in Eindhoven [4]. In 1987, students from the NCSU group founded a small company, Cree Research, to produce SiC wafers commercially. The introduction of 25 mm single crystal wafers of 6H-SiC by Cree in 1990 catalyzed the current resurgence in SiC research and initiated an unprecedented level of device development in this material. At present, 35 mm diameter wafers of both 4H and 6H SiC are commercially available from Cree Research (Durham, NC, USA) and from Advanced Technology Materials, Inc. (Danbury, CT, USA). 50 mm diameter wafers have been used in the production of blue LEDs at Cree and 75 mm diameter wafers have been prototyped by both Cree and Westinghouse (now Northrop Grumman).

Epitaxial layer growth of SiC is done by chemical vapor deposition (CVD) on slightly off-axis substrates (3.5 degrees for 6H and 8 degrees for 4H). The use of off-axis substrates enables step-controlled epitaxy [5] in which steps on the growth surface expose several alternating silicon and carbon planes, thereby transferring stacking information which preserves the polytype in the epitaxially grown film. E. Janzen, et al. [6] of Linkoping University reported a modified CVD technique capable of growing films up to 100 microns thick with a background doping level of $1x10^{14}$ cm^{-3}. Carrier lifetimes in these lightly doped layers are on the order of 1 microsecond. These results are very exciting because they would theoretically enable the fabrication of power devices having blocking voltages in excess of 10 kV.

Selective doping of SiC is accomplished by ion implantation, since the diffusion coefficients of aluminium and nitrogen are so low that thermal diffusion is impractical. The implantation and activation of nitrogen to produce n-type regions is well understood and activated concentrations above $1x10^{19}$ cm^{-3} can be obtained easily. P-type selective doping, however, is an area of current research. The two common p-type dopants, aluminium and boron, produce relatively deep acceptor levels (211 meV and 300 meV respectively), but aluminium is generally used because of its smaller ionization energy. To minimize amorphization during implantation, it is common to implant at elevated temperatures, typically around 650°C for nitrogen and up to 1100°C for aluminum. Boron can be successfully implanted at room temperature.

Ohmic contacts are of great importance to power devices, since the high current densities give rise to high voltage drops even across small resistances. Ohmic contacts to n-type material are typically formed by annealed nickel. The contacts are annealed at high temperatures, typically between 850 - 1050° C, in argon or vacuum. Contacts to p-type material have been more difficult. The p-type contacts are typically formed by annealed aluminium or by a bilayer of aluminium covered with titanium. Anneal temperatures are similar to those used for nickel contacts, but the contact resistivities are in the 10^{-3} to 10^{-5} ohm-cm range, depending upon the doping level [7].

The thermal integrity of the metallization system is of importance for high temperature applications. Nickel ohmic contacts used for n-type material have been shown to be stable upto very high temperatures (negligible change in resistance after 329 hours at 650° C or after short thermal cycles to 1300° C) [7], but aluminium p-type contacts will not be capable of high temperature operation. The use of metal silicides, as recently reported for p-type ohmic contacts [8], will enable operation at much higher temperatures.

In the last few years, however, the picture has improved considerably. Work at laboratories and other locations, including Cree Research, has lead to a reduction in interface state density on p-type SiC to 10^{11} eV^{-1} cm^{-2} range, comparable to that obtained on n-type SiC. Several

studies [9-11] have shown that the aluminium dopant is not responsible for either interface states or fixed charges on p-type material.

One final area which is attracting attention is that of deposited insulators. One reason is the desire for an insulator having a dielectric constant comparable to or higher than that of the substrate. This is important for power devices because the electric field in SiO_2 is approximately 2.5x higher than the peak field in SiC, due to the dielectric constant ratio. Thus, in many cases the maximum blocking voltage of SiC power devices is limited by the SiO_2 and not by the semiconductor. An insulator having a higher dielectric constant would have a correspondingly lower electric field at a given operating voltage. AlN and TiO_2 are among the insulators under investigation, but this work is still at a very preliminary stage.

1.2 SILICON CARBIDE POLYTYPES

Silicon is the basic material dominating the electronics industry today. Silicon Carbide (SiC), however, has superior properties for power devices as compared to silicon. The main strength of silicon carbide is that it can resist high field strengths, it offers better heat-conducting capacity than copper at room temperature and it has a large energy band gap, which means that electrical components continue functioning even when the temperature rises. With very high thermal conductivity (~5.0 W/cm), high saturated electron drift velocity (~2.7 x 10^7 cm/s) and high breakdown electric field strength (~3 MV / cm), SiC is obviously a material fit for high temperature, high voltage, high frequency and high power applications[1]. Table 1.1 lists some electrical properties of the common SiC polytypes in comparison to that of Si and GaAs [11,12].

Table 1.1. Comparison of properties of SiC with Si and GaAs at room temperature [11,12]

Property	Units	Silicon	GaAs	6H-SiC	4H-SiC
Bandgap	eV	1.11	1.43	2.9	3.2
Dielectric const	ϵ_r	11.8	12.8	9.7	9.7
Breakdown Field (N_d=1x10^{17}cm-^{3})	V/cm	6x10^{5}	6.5X10^{5}	3.5X10^{5}	3.5X10^{5}
Saturated Velocity	cm/sec	1x10^{7}	1x10^{7}	2x10^{7}	2x10^{7}
Electron Mobility	cm^{2}/V-sec	1350	6000	380 $\perp$ to c-axis 380	800 $\perp$ to c axis
Hole Mobility	cm^{2}/V-sec	450	330	95	120
Thermal Conductivity	W/cm-º K	1.5	0.46	4.9	4.9

The most important property of SiC is its large bandgap, which is nearly three times that of silicon. The large Si-C bonding energy makes SiC resistant to chemical reaction and radiation. Silicon carbide belongs to a class of semiconductors commonly known as wide band gap semiconductors, where conventional semiconductors like Si and GaAs cannot adequately perform under extreme conditions. The wider band gap of SiC also enables one to design smaller, higher density devices that would withstand high voltages. Also, the thermal conductivity of SiC (4.9 W/cm-°K) is much larger than that of Si and GaAs and is a major advantage for SiC–based devices. The high thermal conductivity of SiC lowers the need for special packaging and system cooling for successful device operation[13]

SiC has equal parts of silicon and carbon, both of which are group IV elements. The distance 'a' between neighboring silicon or carbon atom is approximately 3.08 Å for all polytypes. The carbon atom is situated at the center of mass of the tetragonal structure outlined by the four neighboring Si atoms (see Figure 1.1). The distance between the C atom and each of the Si atoms are approximately 2.52 Å. The height of the unit cell, 'c', varies between different polytypes. Therefore, the ratio of c/a differs from polytype to polytype. This ratio is 1.641, 3.271, and 4.908 for the 2H, 4H, and 6H-SiC polytypes, respectively.

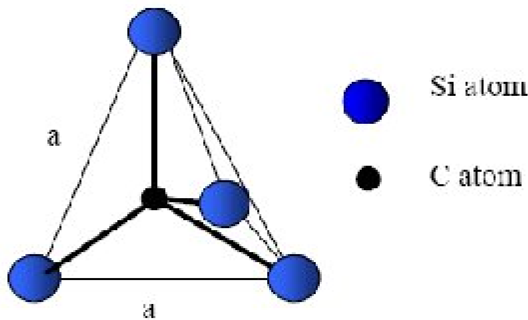

Figure 1.1. The tetragonal bonding of a carbon atom with its four nearest silicon atoms[7].

The polytype is a variation of crystalline material in which the stacking order of planes in the unit cell is different. Each SiC bilayer, while maintaining the tetrahedral bonding scheme of the crystal, can be situated in one of three possible positions with respect to the lattice (A, B, or C). The bonding between Si and C atoms in adjacent bilayer planes is either of a Zinc-blende (Cubic) or Wurtzite (Hexagonal) nature depending on the stacking order [14]. As shown in Figure 1.2, if the stacking is ABCABC...the cubic polytype commonly abbreviated as 3C-SiC, is obtained.

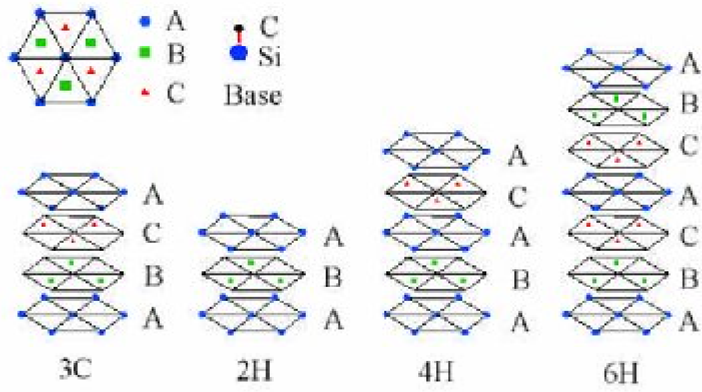

Figure 1.2. The stacking atomic sequence of common 3C-, 2H-, 4H-, and 6H-Silicon Carbide crystal[15].

The purely Wurtzite ABAB... stacking sequence is called 2H-SiC. The 4H-SiC (ABAC...) and 6H-SiC (ABCACB...) are also shown in Figure 1.2 [15]. These two types of SiC are the most common hexagonal polytypes. 4H-SiC consists of equal amounts of cubic and hexagonal bonds, while 6H-SiC is two-thirds cubic. All the polytypes of SiC are referred to in a hexagonal coordinate system as consisting of three a-planes with coordinates a_1, a_2, a_3 and a c-axis coordinate. The c-axis is the direction of stacking of the hexagonally close packed layers and the three a-plane axes are all in the plane perpendicular to c-axis (see Figure 1.3), with 120-degree angle between a-planes. Commercially available SiC bulk material is generally cut and polished 3~8 degrees off-axis towards <11 2 0> for avoiding the growth of 3C inclusions in the epitaxial layers of 4H, called step-controlled epitaxy by Matsunami et al. [16]. Two different faces perpendicular to the c-axis, Si (0001) and C (0001) exist in commonly used SiC with the silicon face being commonly used for device applications since the quality of epitaxial growth is better in this case than that on the carbon face.

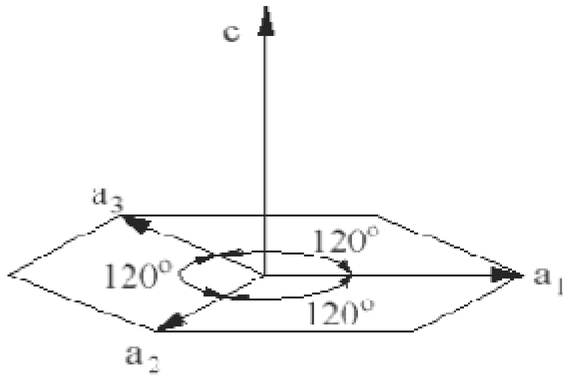

Figure 1.3 The Miller indices describing the hexagonal structure [15]. The three a-plane coordinates a_1, a_2 a_3 and the c axis coordinate are shown here.

Silicon Carbide occurs in many different crystal structures (called polytypes) with each crystal structure having its own unique electrical and optical properties. The difference between the polytypes is the stacking order between the double layers of carbon and silicon atoms. In Fig 1.2, the stacking sequence is shown for the three most common polytypes 3C, 4H and 6H-SiC. Cubic and hexagonal crystal structures of Silicon Carbide are shown in Fig. 1.4. If we designate a Si-C atom pair in an A- plane in a close packed lattice as A, in the B-plane as B and in the C-plane as C, then we can generate a series of lattice unit cells by variation of SiC plane stacking sequence along the principal crystal axis.

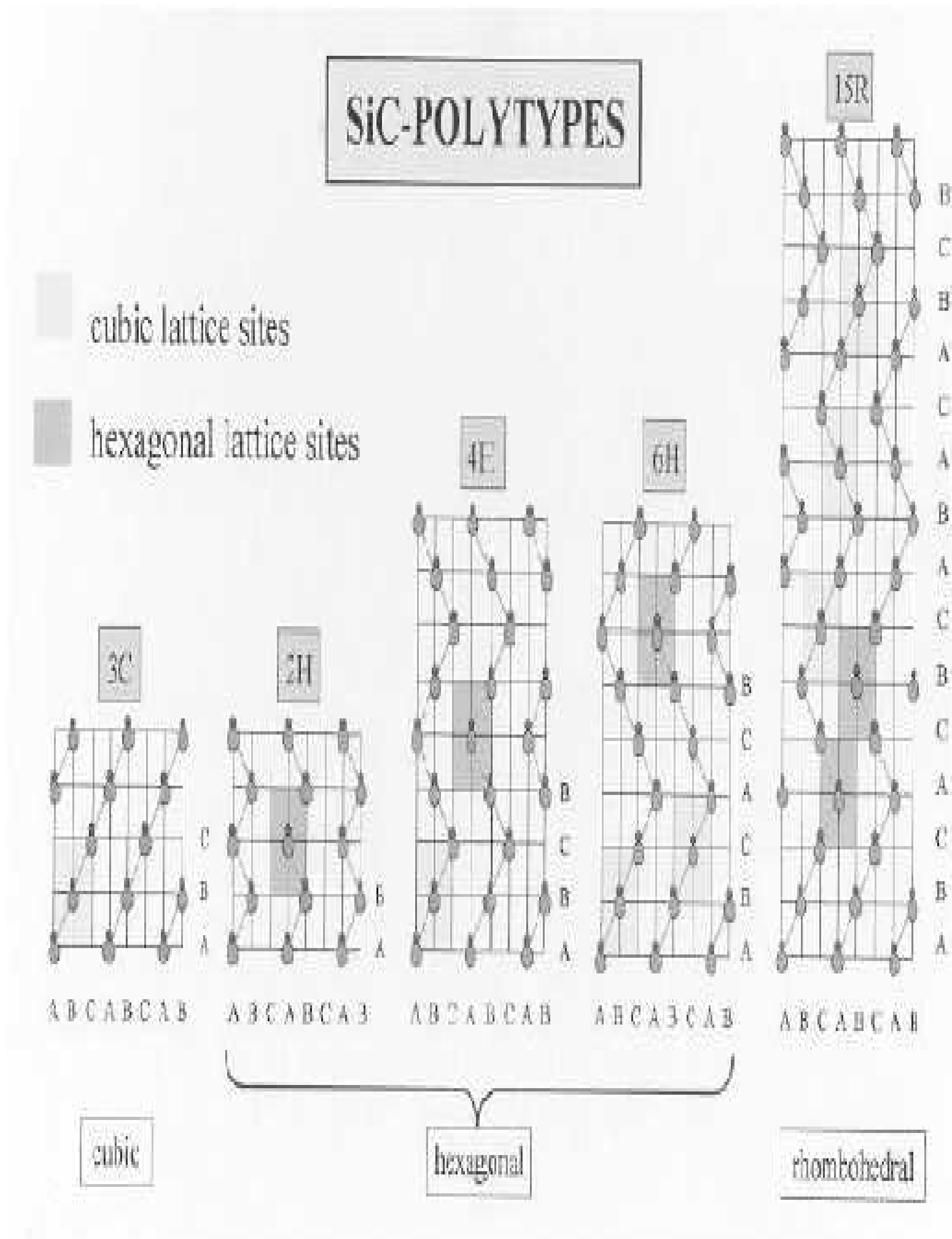

Figure 1.4 Stacking sequence of the most common polytypes of SiC [13]

The ABCABC... stacking, will generate the 3C-SiC zinc-blende lattice, and ABAB... stacking, will generate the 2H-SiC wurtzite lattice. Other stacking sequences, such as ABACABAC.. will generate 4H-SiC; and ABCACB... will generate 6H-SiC. The number of atoms per unit cell varies from polytype to polytype, significantly affecting the

number of electronic energy bands and vibrational branches possible for a given polytype. This diversity in electronic and vibrational band structures profoundly affect the physical properties of the different polytypes. Some of the differences are given in Table 1.1

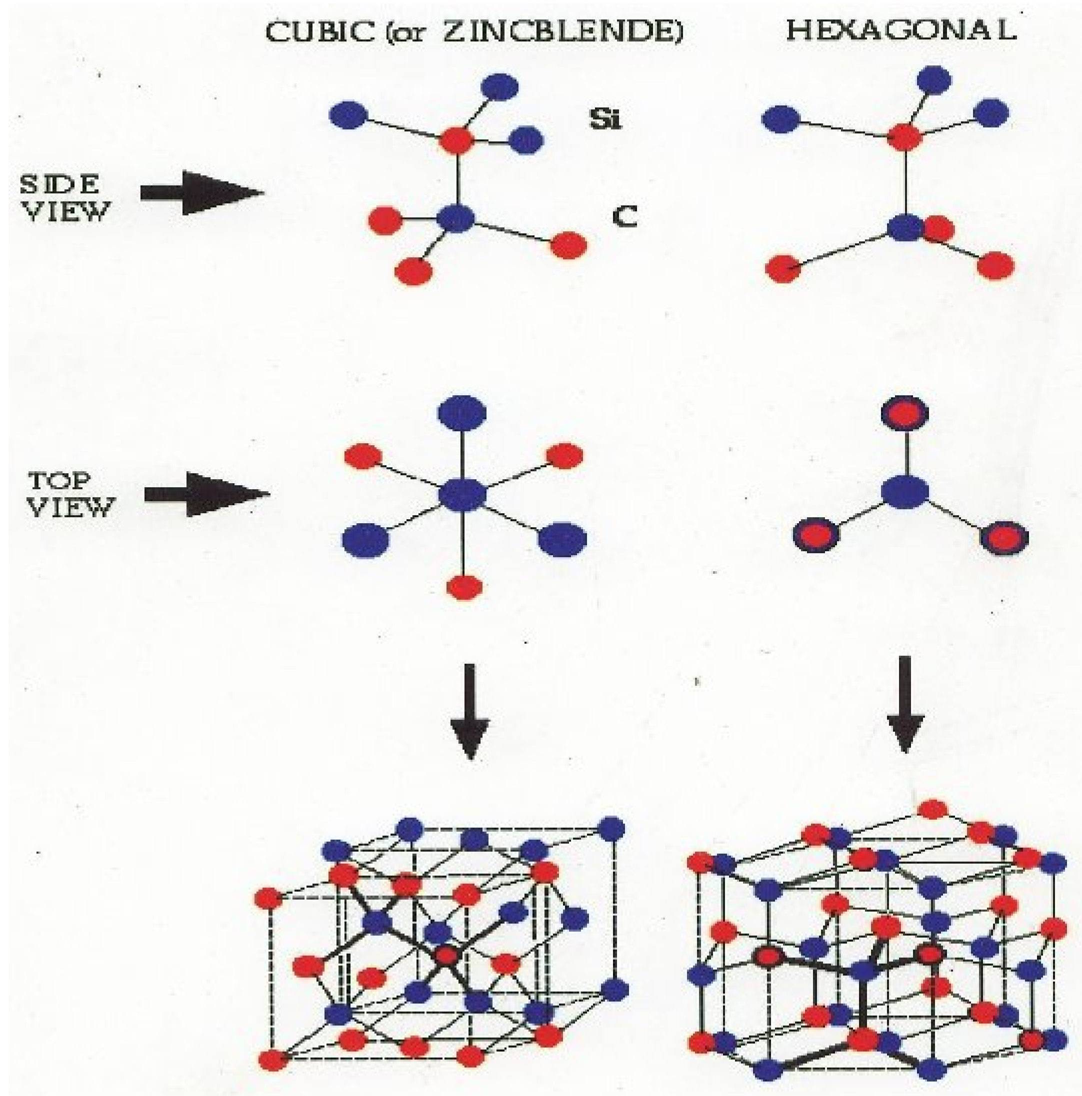

Fig 1.5 Crystal structure of Silicon Carbide

Considering the 6H-SiC polytype, the hexagonal site gives rise to the lowest donor level with an activation energy of approximately 85 meV ($\Delta E_h = E_c$-85 meV). The two cubic sites, k_1 and k_2, yield deeper donor levels with activation energies of 138 meV ($\Delta E_{k1} = E_c$-138 meV) and 142 meV ($\Delta E_{k2} = E_c$-142 meV), respectively. In the 4H-SiC polytype there

are only two inequivalent sites, one hexagonal and one cubic [1]. In 3C-SiC there is of course only one cubic site and in 2H there is only one hexagonal site. The 6H-SiC polytype can thus be characterized as having donors (or acceptors) which are 33% hexagonal, whereas the 4H- and 2H-SiC polytypes are 50% and 100% hexagonal, respectively [1].

Of the numerous polytypic forms of Silicon Carbide, 4H- and 6H-SiC electronic devices are presently the most promising due to the availability and quality of reproducible single - crystal wafers of these polytypes. The availability of 6H-SiC and 4H-SiC polytypes in bulk wafer form has helped SiC to emerge as a material with one of the relatively mature wide band-gap semiconductor technologies. SiC is a material with immense potential for use in heterostructure electronic devices and takes advantage of differing band gaps, carrier mobilities, etc. However, there are many crucial crystal growth and device fabrication issues that have to be addressed before SiC-based devices and circuits are ready for scale up and reliable incorporation into electronic systems. The most important issue is controlled and repeatable doping in SiC device structures.

1.3 DOPING IN SILICON CARBIDE

The material advantages of Silicon Carbide are being exploited in the development of high power and high temperature semiconductor devices. However, in order to achieve the theoretically calculated advantages, advancements are needed in the growth techniques and dopant incorporation [17]. For a pure semiconductor the concentration of free holes and electrons is a function of thermal energy which determines the percentage of broken covalent bonds in the material. For an intrinsic semiconductor, the free electron concentration (n) and the free hole concentration (p) are equal (i.e., $np = n_i^2$ where n_i is the intrinsic carrier concentration).

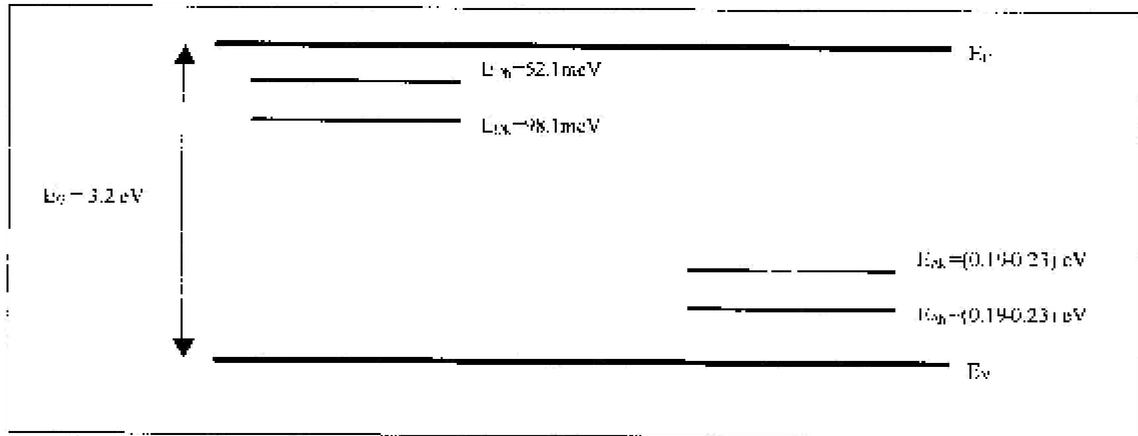

Fig 1.6 Band structure of n-type (left) and p-type (right) 4H-SiC showing the split energy levels due to the varying crystal symmetry[17].

In the band structure picture shown in Fig 1.6, impurity states are created much closer to the conduction band in the case of n-type (donor) doping and much closer to the valence band in the case of p-type (acceptor) doping. Donors donate electrons to the conduction band whereas acceptors accept electrons from the valence band, thus creating holes in the valence band. In either case, it is easy to liberate electrons (or holes) for conduction at low thermal energy, provided the activation energy of the dopant levels is on the order of 3 kT [18]. The holes are positively charged with charge +q since a hole is really the absence of an electron of the charge -q. Holes can move through the crystal, since a nearby electron can jump into a hole, filling it up, but leaving a hole nearby. Such materials are called p-type semiconductors, because it is the positive charge (hole) that can be viewed as a quasi - particle which can move freely in the material.

Doping in Silicon Carbide may be performed during epitaxial layer growth or after crystal growth by ion implantation. Ion implantation is more selective in nature but of lower quality than doped epilayers due to crystal damage created during ion bombardment. Typically, the first step in making Silicon Carbide semiconductor devices is to grow epitaxial layers using Chemical Vapor Deposition (CVD), which allows single-crystal layers (called epitaxial layers or "epilayers") of varying electrical conductivity to be grown.

The Silicon Carbide epilayers are produced in the CVD process by thermally decomposing silicon and carbon source gases (called precursors) onto boule - derived SiC substrates. The electrical character is changed by adding dopants into the gas stream(either nitrogen (for n-type) or trimethylaluminium and/or boron (for p-type) material), during the CVD SiC epilayer growth.

Ion Implantation generates crystallographic defects (vacancies, interstitials, etc.) which can serve to form complexes with donors and acceptors in the lattice.

1.4: HYDROGEN PASSIVATION OF SILICON CARBIDE

The specific physical and electronic properties of Silicon Carbide make it one of the promising semiconductors for use in electronic devices, especially those applications where operation at high power, extreme temperature, or high radiation levels is needed. Many of these applications require the growth of thick, high quality epitaxial layers with controlled doping concentrations and carrier lifetimes. This has led to significant progress in the technologies for both bulk and epitaxial growth in the past few years. During processes such as CVD, hydrogen is known to be trapped at defects or impurities and alters the electrical properties [19]. This effect is known as "hydrogen passivation".

In addition to the observed hydrogen passivation of shallow impurities in SiC crystals, it is important to know whether, and how, hydrogen present in the epi-reactor can passivate doping impurities during the growth of the material [20]. One problem is that hydrogen passivation makes it difficult to know the true free carrier concentration in the material. Also, variations in hydrogen incorporation affect the net doping density and make process control difficult.

The intrinsic material advantages of Silicon Carbide are currently being exploited in the development of high power and high frequency semiconductor devices for service in high temperature, corrosive and high radiation environment[21]. However, in order to obtain the theoretically calculated advantages of using SiC, advancements are needed both in the field of bulk growth and epilayer growth of SiC [21]. For example, improvements in the bulk growth of SiC are needed for the elimination of device limiting defects such as micropipes and closed-core screw dislocations [21]. Other advancements are also needed in the growth process of epitaxial layers in Silicon Carbide. In particular, dopant incorporation both during the growth of SiC epilayers or by ion implantation must be understood and reliably controlled which will help to achieve desired device results [21]. In Silicon Carbide, hydrogen incorporation is known to occur during epitaxial growth by chemical vapor deposition. It has also been observed that hydrogen incorporation occurs during plasma treatment, ion implantation or treatment in hydrogen gas [20]. In most reports, hydrogen trapping at defects plays a significant role. The process temperatures necessary to induce detectable mobility of hydrogen in SiC crystals are in excess of 900°K [20]. Hydrogen forms complexes with known dopants in SiC (both donors and acceptors) and has been observed to make them electrically inactive [22]. The presence of hydrogen, therefore, reduces the effective carrier density within the material and masks the true dopant level.

Hydrogen passivation has been observed in both p-type and n-type SiC with the detection of the latter being less observable. But before presenting the model, one has to take into account various factors such as the atomic number of the dopant species, its activation energy in the SiC lattice, number of valence electrons, etc. All of these values have been tabulated in Table 1.2.

Table 1.2: Atomic Number and Activation Energies of the common dopants in SiC[3]

	N donor	Al acceptor	B acceptor
Atomic Number	7	13	5
Activation Energy in 4H-SiC	$E_{Dh}=E_C - 52.1meV$ $E_{Dk}=E_C - 91.8meV$	$E_A=E_V+(0.19\text{-}0.23)$ eV	$E_A=E_V+(0.285\text{-}0.39)$ eV
Activation Energy in 6H – SiC	$E_{Dh}=E_C - 81meV$ $E_{Dk1}=E_C - 137.6meV$ $E_{Dk2}=E_C - 142.4meV$	$E_A=E_V+(0.20\text{-}0.25)$ eV	$E_A=E_V+(0.27\text{-}0.40)$ eV

The most common acceptor impurities (A1 or B) can be introduced during growth or afterwards by ion implantation. A substitutional atom with a group – III valency normally acts as an acceptor in SiC since there is a deficit of one valence electron to complete the tetrahedral bonding. At sufficiently high temperatures, it ionizes and gives rise to p-type conduction. On the other hand, an atom with a group – V valency normally acts as a donor in SiC since there is an excess of one valence electron. Since SiC is a compound semiconductor, an additional variable is which lattice site (Si or C) the dopant occupies. Boron and Aluminum are known to substitute for the silicon site in the structure and nitrogen is known to replace carbon.

The free carrier concentration has been observed to decrease after hydrogenation due to hydrogen – dopant complex formation. The free concentration has been observed to increase after de–hydrogenation (annealing the sample at high temperatures to break the bonding existing between complexes).

1.5 ION IMPLANTATION

Impurity doping is the controlled amounts of impurity incorporation into semiconductors. The practical use of impurity doping has been mainly to change the electrical properties of semiconductors. Diffusion and ion implantation are the two key methods of impurity doping.

Until early 1970s, impurity doping was done mainly by diffusion at elevated temperatures. In this method the dopant atoms were placed on or near the surface of the wafer by deposition from the gas phase of the dopant or by using doped-oxide sources. The doping concentration decreases monotonically from the surface and the profile of the dopant distribution was determined by the temperature and diffusion time.

Many doping operations have been performed by ion implantation. In this process the dopant ions are implanted into the semiconductor by means of an ion beam. The doping concentration has a peak distribution inside the semiconductor and the profile of the dopant distribution is determined mainly by the ion mass and the implanted–ion energy. Ion implantation is used for fabricating discrete devices and integrated circuits..

Ion implantation has been established as the main method for selective doping of SiC as most impurity atoms have very low values of diffusion coefficients. With ion implantation the electrical or chemical properties of the target can be modified. Typical ion doses vary from 10^{11} to 10^{16} ions/cm^2 with energies in the range of keV or GeV.

The depth profile of implanted ions can roughly be described by a Gaussian distribution with a maximum at R_p and a width ΔR_p, known as straggle . The projected range R_p increases approximately linearly with energy. The straggle ΔR_p also increases with increasing energy.

The implantation at elevated temperatures is known to be effective to reduce implantation induced damage and to improve the electrical activation of implanted ions.

Ion implantation in covalent semiconductors is accompanied by the formation of intrinsic point defects due to elastic collision processes between the ion and lattice atoms.
For high ion energies the energy loss is almost entirely to target electrons, whereas in the low-energy regime atomic collisions with vacancy cascade formation prevail. The density of point-defect formation in the region near the end of the ion range is thus much higher than in the rest of the ion track, which we refer to as the trace region.

Recently, there has been an interest in the fabrication of microelectronic circuits that can operate as high-power/high speed devices in both elevated-temperature and high-radiation environments where Si integrated circuits (ICs) would fail. The wide band-gap semiconductor, SiC (E_G = 3.0 eV for the 6H polytype and 3.25 eV for 4H), is the leading contender for such applications [23]. Its high breakdown electric field (~8 times that of Si) and high thermal conductivity (~ 3.3 times higher than Si) are attractive for the fabrication of high-power circuits. Additional benefits of SiC are high electron saturation drift velocity (twice that of Si) as well as the ability to create semi-insulating layers by group V doping[24], traits that are useful for making microwave frequency range devices. Monolithic *n*-type metal–oxide semiconductor (NMOS) digital ICs [25], MOS analog ICs[26] complementary metal–oxide-semiconductor (CMOS) ICs[27], high performance microwave devices[28], insulated-gate bipolar transistors(IGBT) [29] and CCD image sensors[30] have all been made using SiC.

For making planar ICs, selective area doping is required. Thermal diffusion is precluded for this purpose in SiC due to the small diffusivity of impurities at operating temperatures (1800°C), where the surface integrity of the material can be maintained. As a result, ion

implantation is the only possible selective area doping technique available for SiC. The group V and group III elements constitute the commonly used donor and acceptor dopants, respectively in SiC. Nitrogen implantation yields n-type layers with good donor activation in SiC[31-34]. Nitrogen implanted n-type layers with room-temperature carrier concentrations as high as 10^{19} cm^{-3} have been achieved[31-34]. This behavior is due to the fact that N is a relatively shallow donor (E_D = 80 meV) for 6H–SiC [35]. In SiC, Aluminium implantation, on the other hand, will produce p-type layers in SiC[34,36,37]. Due to the high acceptor binding energy (E_A=240 meV) for 6H–SiC[38] of Al, at room temperature it is not possible to obtain the same level of hole concentration as the electron concentration that has been achieved for N-implanted material.

Since the ionization energy of Phosphorus(P), in 6H–SiC, is comparable to that of N[39], P implantation in SiC has the potential of producing n-type layers with high carrier concentrations even at room temperature. In addition, since it's atomic mass is not high enough to cause excessive lattice damage during implantation, phosphorus has become the most popular donor impurity in Si processing. The P atoms are believed to reside predominantly on Si lattice sites[40], whereas N locates predominantly on C sites[41]. Hence, if it is possible to activate P implants satisfactorily, then the co-implantation of P and N may be useful in obtaining high carrier concentrations by populating both Si and C sites with P and N, respectively. This is important since high carrier concentrations are needed to obtain low contact resistance and low neutral region resistance in SiC devices, an attribute especially critical for attaining optimum performance in high power and microwave devices. Though Boron(B) is a deep acceptor impurity with $E_A \approx 350$ meV[42], its low mass, and its availability in gaseous source form (BF_3) make B implantation an attractive choice for obtaining deep p-type regions of low carrier concentration in SiC. The p–n junctions made by the B implantation exhibited lower leakage currents than those formed by the Al implantation [43]. However, Al is preferred over B because it's acceptor level is shallower and can yield higher

hole concentrations, which is important for making low-resistance ohmic contacts. Deep B implantation at the junction and an overlapping shallow Al implant at the surface looks attractive for obtaining planar p–n junctions in n-type SiC.

The range statistics [the two moments of the implant depth distribution, namely, projected range (Rp), range straggle (ΔRp) of the implanted ions have been established at various energies by analyzing the secondary ion mass spectrometry (SIMS) atom concentration depth profiles of implants using suitable mathematical formulae.[44]

1.6 SILICON CARBIDE DEVICES

Silicon carbide has several unique properties that can lead to enhanced performance in devices, as discussed below. These properties include higher breakdown field, wider band gap, lower thermal generation rate and lower intrinsic carrier concentration.

1.**Power MOSFETs**

The breakdown electric field of SiC is approximately 8x higher than silicon. This makes it possible to design power switching devices having correspondingly higher blocking voltages than their Silicon counterparts. More importantly, the specific on-resistance (i.e. resistance-area product) of a power device scales inversely as the *cube* of the breakdown field, so the on-resistance of SiC power MOSFETs are 100-200x lower than comparable devices in Silicon.

2.**Lateral Power MOSFETs**

The maximum blocking voltage of vertical power devices in SiC is presently limited by the thickness of commercially available epilayers. The first lateral power MOSFETs developed in SiC devices exhibited blocking voltages of 2.6 kV.

3.**Schottky Barrier Diodes**

Schottky barrier diodes (SBD's) are attractive as power rectifiers because they do not store minority carriers in the on-state and therefore can be switched off quickly with negligible reverse current. It is widely felt that SBD's will be the first SiC power devices to go into commercial production. SBD's are fabricated on 4H-SiC that exhibit blocking voltages of 5k V and 10kV, equal to the current world record.

4.IMPATT Diode Microwave Oscillators

IMPATT diodes are two-terminal semiconductor devices that generate RF power by introducing a 180° phase shift between current and voltage waveforms at microwave frequencies. The first IMPATT diodes were fabricated in 4H-SiC. These devices exhibit microwave oscillations at around 8 GHz when operated in X-band waveguide cavity under pulsed bias.

5.**CMOS Integrated Circuits**

The first 6H-SiC CMOS digital integrated circuits were completed in September 1996. A second generation was completed in March 1997. These were the first SiC CMOS circuits fabricated with an implanted P-well process and the first to operate on a single 5 V power supply.

6.**Nonvolatile Memories**

The thermal generation rate in semiconductors is proportional to the intrinsic carrier concentration n_i and n_i decreases *exponentially* with band gap energy. Wide band gap semiconductors have dramatically lower thermal generation, with the thermal generation rate of 6H-SiC being about 16 order-of-magnitude lower than Silicon. This makes it possible to construct on-transistor memory cells in SiC which retain information for many years without power or refreshing.

7.**Charge Coupled Devices**

CCDs are unique MOS devices in which charge packets are shifted laterally along the semiconductor surface by appropriate clock pulses applied to surface electrodes. CCDs are

widely used as imagers in video cameras and digital still cameras. The first CCD was developed in SiC, where the wider bandgap makes it possible to image scenery in the UV portion of the spectrum without being overwhelmed by visible light.

8.**NMOS Integrated Circuits**

The low thermal generation rate in SiC makes it possible to operate integrated circuits at much higher temperatures than Silicon. The first digital integrated circuits in SiC were developed in late 1993. These early circuits were implemented in enhancement mode NMOS.

1.7 LITERATURE SURVEY

It was in 1938 that German physicist Walter H. Schottky created a theory that explained the rectifying behavior of a metal-semiconductor contact as dependent on a barrier layer at the surface of contact between the two materials. The metal semiconductor diodes later built on the basis of this theory are called Schottky barrier diodes. Since then a continuous research and development has been in progress in this field. In March 1993, Mohit Bhatnagar and B.Jayant Baliga showed theoretically that an ideal SiC Schottky rectifier can provide a breakdown voltage as high as 5000V with a forward voltage drop of only 3.85V at 300°K for a current density of 100Amps/cm^2 . R.Raghunathan in 1995 showed for the first time that breakdown voltage of 1000V can be achieved for 4H-SiC Schottky barrier diode. In June 1995, Akhira Itoh et al. showed that high performance of high-voltage rectifiers could be realized utilizing 4H-SiC Schottky barrier diodes. A typical breakdown voltage of 800V could be achieved[45]. Akhira Itoh et al. showed in 1996 that using highly resistive layers formed by B^+-edge termination can help in improving the reverse blocking characteristics of 4H-SiC Schottky rectifiers[46].In June15, 1998, Hitachi announced the release of Schottky barrier diode, the HSB0104YP containing two diode elements. This new product made possible high speed switching at the picosecond level. It had a reverse voltage of 40V.

ROHM developed the “ROBOSIL-40” SBD with an ultra low V_F (forward voltage) with B_V (Backward voltage) of 40V, providing an extremely low V_F of only 0.29V.In July 1998, Purdue University reported, 4H-SiC SBD’s using both Ni & Ti as Schottky metals. These diodes have been fabricated, which have reverse-blocking voltages of 1720V and 1480V respectively. In 1999, V.K Saxena et al. fabricated 1kV 4H and 6H-SiC Schottky diodes utilizing a metal oxide overlap structure for electrical field termination. The same year, Purdue University group fabricated Ni-Schottky diodes on a 50μm epilayer of 4H–SiC. These diodes exhibited blocking voltages as high as 4.9kV. In 2001, models for the electron mobility in 4H, 6H, and 3C-SiC were explained in a paper by Matthias et.al.[47]. A number of experimental mobility data and Monte Carlo(MC) results reported in the literature have been evaluated and serve as the basis for model development. The proposed models describe the dependence of the electron mobility on doping concentration, temperature and electric field.

Royal Institute of Technology, Department of Microelectronics & IT, Stockholm, reported in 2002 that Schottky rectifiers in SiC are candidates to replace Si-PIN diodes in 300-3000V blocking voltage range. Nuremberg, Germany, 14th May, 2002, Dynex Semiconductors Ltd, a leading power semiconductor company announced that the company has been awarded a research & development grant in a new Program (ESCAPEE) to develop 3.3KV Schottky Barrier Diode technology from SiC. Marinsz et. al. showed the result of investigation of the forward and reverse current-voltage(I-V) characteristics of 4H-SiC Schottky rectifiers with Nickel as the contact metal[48].In 2003, P.Tobias et.al. showed that Metal-Insulator–Silicon Carbide devices can be used for gas sensing in automotive exhausts, because the large band gap of silicon carbide allows high temperature operation. Researchers at the Silicon Carbide lab of Rutgers University in New Jersey, demonstrated 1.79KV, 6.6A 4H-SiC merged PIN-Schottky diodes in 2004.

In 2006, Silicon Carbide as energy efficient wide band gap device was discussed [49], which showed that SiC Schottky diodes allowed up to a 25% reduction in losses in power supplies for computers and servers when used in the power factor correction circuit. For motor control, SiC Schottky allowed a >35% reduction in losses as demonstrated for a 3HP motor drive.

In 2007 Electrical and Computer Engineering Department , Purdue University, put up the analysis of Schottky and PIN Diodes on epitaxial 4H-SiC wafers. In 2009, a method to theoretically calculate current-voltage characteristics of Schottky barrier diode defined by the diode equation was given, using iteration method and C++ programming. The diode equation is split into two functions. A set of values of current and voltages was generated using C++ program. The analysis has been made using 4H-SiC diode with contacts of Nickel, Titanium & Gold [50].

1.8. SILICON CARBIDE SCHOTTKY BARRIER DIODES

SiC Schottky barrier diodes are especially attractive because the breakdown field of SiC is about 8x higher than in silicon. In addition, because of the wide bandgap, SiC SBD's should be capable of a much higher temperature operation than silicon devices.. Special edge termination is required to minimize field crowding at the edge of the metal contact. The cross-section of the device is shown in Fig. 1.7.The barrier heights for Ti and Ni on 4H-SiC at room temperature are 0.8 and 1.3V, respectively. The lower barrier height with Ti gives lower forward voltage drop but higher reverse leakage current as compared to the Ni barrier. The reverse blocking voltages are 1480 and 1720 V respectively.

Ni Schottky diodes have been fabricated on a 115 µm epilayer of 4H-SiC. These diodes exhibited blocking voltages as high as 10 kV, the highest yet reported for a SiC Schottky diode.[51].

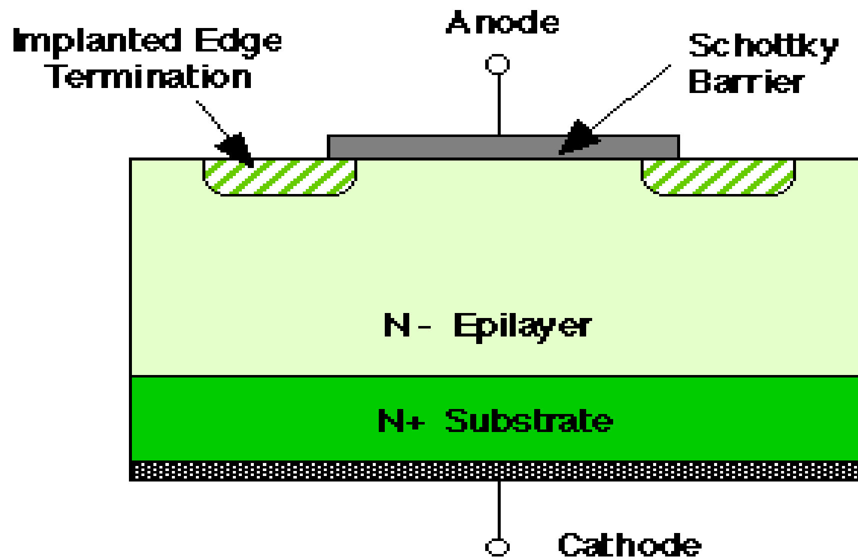

Figure 1.7. Cross-section of an implant-edge-terminated Schottky barrier diode (SBD) in SiC [52].

1.9 OBJECTIVE OF RESEARCH

The present work focuses on the calculation of current density against forward voltage, to cross-verify the results with the published data, provide a method to theoretically analyze 4H-SiC Schottky barrier diode, calculate width of depletion region, effective doping concentration of linearly graded profiles, breakdown voltages, specific on-resistance and power dissipation along with mathematical analyses. This work has been carried out along the following lines:

1. Study and analysis of Schottky Barrier diode(SBD) on 4H-SiC wafers.
2. Development of a method to plot V_F-J_F characteristics of 4H-SiC SBD's.

3. Analysis of 4H-SiC using uniformly doped profile in the epilayer.
4. Analysis of 4H-SiC with linearly graded profile in the epilayer.
5. Analysis of 4H-SiC with low power dissipation for large breakdown voltages.
6. Comparison of results obtained in 3& 4.

1.10 RESEARCH WORK BREAKUP /OUTLINE

Chapter 1 focusses on Silicon Carbide and its details: crystal growth, thermal oxidation, polytypes of Silicon Carbide i.e 3C, 4H, 6H, doping in SiC, hydrogen passivation of Silicon Carbide devices. Comparison of properties of SiC with Si and GaAs at room temperature is also taken up in brief. This chapter also discusses ion implantation and different Silicon Carbide devices.

Chapter 2 describes the details of Schottky barrier diodes: formation of Schottky barrier, equivalent band diagram, current transport mechanism in forward biased and reverse biased Schottky barrier diode, capacitance in Schottky barrier diodes, series resistance, breakdown voltage and Fermi level pinning in Schottky barrier diode.

Chapter 3 describes the various parameters associated with 4H-SiC Schottky barrier diode: specific on resistance, forward voltage drop, breakdown voltage and reverse leakage current .Further the chapter describes the method to plot V_F-J_F characteristics using iteration method and C++ programming for three different metals. The results have been compared with published experimental data and deviations accounted for.

Chapter 4 discusses the 4H-SiC Schottky barrier diode [53-57] with linearly graded doping in the drift region and also deals with the importance of a linearly graded profile in the drift region of a 4H-SiC Schottky Barrier Diode.

Chapters 5 compares the profiles i.e Uniform and Linearly Graded Doping profiles, with respect to power dissipation of the device [58-60] of the latter found to be considerably lower at any given current density as compared to its value obtained for a uniformly doped drift region. The corresponding values of breakdown voltages obtained are similar to those obtained with uniformly doped wafers of 4H-SiC. This chapter analyses the punch-through and avalanche breakdown voltage calculations for uniform and linearly graded doping profiles.

Conclusion and future scope of work is presented in Chapter 6. The (V_F - J_F) plots of the 4H-SiC diodes obtained by the C++ Program tallies well in the case of metal contacts of Ni, Ti and Au, but for some finite range of the forward drop V_F. The method would be useful in generating such characteristics where experimental facilities do not exist, which may help in analyzing the differences that may arise between theoretical and experimental results so that a better theoretical model can be developed.

The linearly graded epitaxial drift regions of 4H-SiC SBD′s have consistently lower power dissipation than uniformly doped epitaxial layer devices. A tally of such an effect can be verified by comparing the power dissipation of the device when evaluated at a current density of 1000 amperes per cm^2. The curves for uniformly doped epitaxial layer devices with a doping level of 10^{14} per cc with the linearly graded profile and a gradient of 3.88 x 10^{16} cm^{-4}, at an effective carrier concentration, N_{eff} of 3.905 x 10^{14} shows that there is a 74.4% drop in power dissipation. When the drop in percentage power dissipation is evaluated at other current density levels, it is found that the amount of drop in percent power dissipation

remains at the same level. However this is not so in the case of other sets of curves and this type of tally shows a constant decline in the amount of percent decline in power dissipation for a given N_{eff} compared to nearly similar levels of doping in uniformly doped profiles. In other words, compared to uniformly doped epitaxial layers, the linearly graded profiles show a significantly lower power dissipation in these devices. The percentage fall in power dissipation is found to increase with a decrease in concentration gradient from 74.4% at a gradient of 3.88×10^{16} cm^{-4} to 7.74% at a gradient of 4.316×10^{19} cm^{-4}.

CHAPTER 2

SCHOTTKY BARRIER DIODES

Metal-to-semiconductor contacts are of great importance since they are present in every semiconductor device. They can behave either as a Schottky barrier or as an Ohmic contact dependent on the characteristics of the interface. The metal-semiconductor junction is a Schottky contact and behaves like the Schottky barrier, is known as Schottky Barrier diode. The structure of a metal-semiconductor junction is shown in Figure 2.1. It consists of a metal in contact with a piece of semiconductor. An ideal Ohmic contact is one in which no potential exists between the metal and the semiconductor.

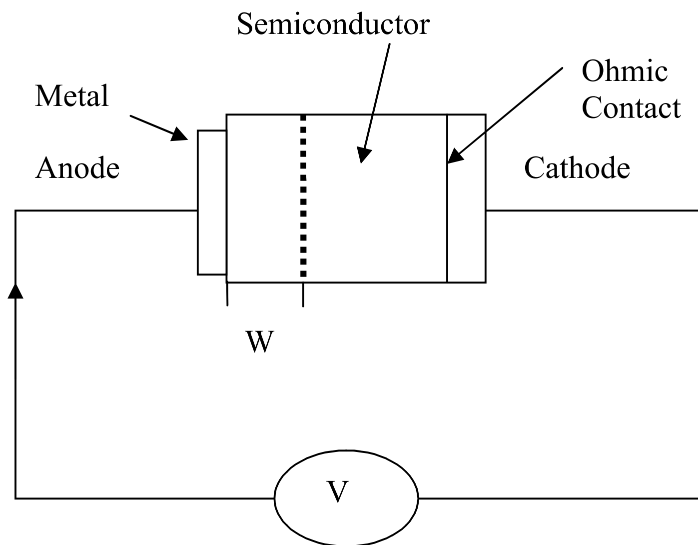

Figure 2.1 Structure of a metal-semiconductor junction

Schottky barrier diodes have many benefits compared to other rectifying devices, such as fast switching speeds and relatively easy fabrication. Coupled with the large amount of data that can be extracted through measurements, Schottky barrier diodes provide a great research platform. However, it is first necessary to understand the physics behind what makes a Schottky barrier diode work. Once this is established, then useful data can be taken and device characteristics extracted.

2.1 IDEAL ELECTROSTATICS OF SCHOTTKY BARRIER DIODES

2.1.1 Schottky Barrier Formation

The formation of an ideal Schottky contact depends on the work functions of the two materials being brought into intimate contact with each other. When a metal and a semiconductor are brought together, two outcomes are possible: either a Schottky contact or an Ohmic contact can form. Both types of contacts are extremely important to solid state research. The factor that determines the nature of contact forms is the difference between the metal and the semiconductor work functions. A metal's work function is determined by the energy required to knock a valence electron from the metal into free space, or "vacuum". This measurement is often done through use of the photoelectric effect. The metal work function ϕ_m is an intrinsic property of the metal and is constant assuming there is no worry of depleting the valence electrons; in other words, there are a

lot of metal atoms. Thus, the metal work function ϕ_m can be described as the vacuum level, E_0, subtracted from the energy level where the valence electrons sit, which is known as the metal's Fermi level, E_{fm}.

$$\phi_m = E_0 - E_{fm} \tag{2.1}$$

A work function for the semiconductor ϕ_S can also be defined using the steps as those for a metal. This concept can be seen in Figure 2.2 with

$$\phi_S = \chi + (E_C - E_{fs})_{FB} \tag{2.2}$$

where χ is known as the semiconductor electron affinity and is an invariant property of the semiconductor, E_{fs} is the semiconductor Fermi level with $(E_C - E_{fS})_{FB}$ the difference between conduction band edge and semiconductor Fermi level under flat band conditions. The equilibrium position of the Fermi level in the semiconductor is not an invariant value. It is positioned based on conductivity type and doping concentration meaning that $(E_C - E_{fs})_{FB}$ can be varied. This means that unlike the metal work function, the semiconductor's work function can be varied.

When a metal and a semiconductor are brought in contact, the respective Fermi-levels must coincide in thermal equilibrium as shown in Figure 2.2(b). There are two limiting cases such as the ideal case (referred to as Schottky-Mott limit [61]) and a practical case (known as the Bardeen limit [62]) to describe the relationship between a metal and a semiconductor. Figure 2.2 shows the energy band diagram for the ideal case (Schottky-Mott limit) with the absence of surface states.

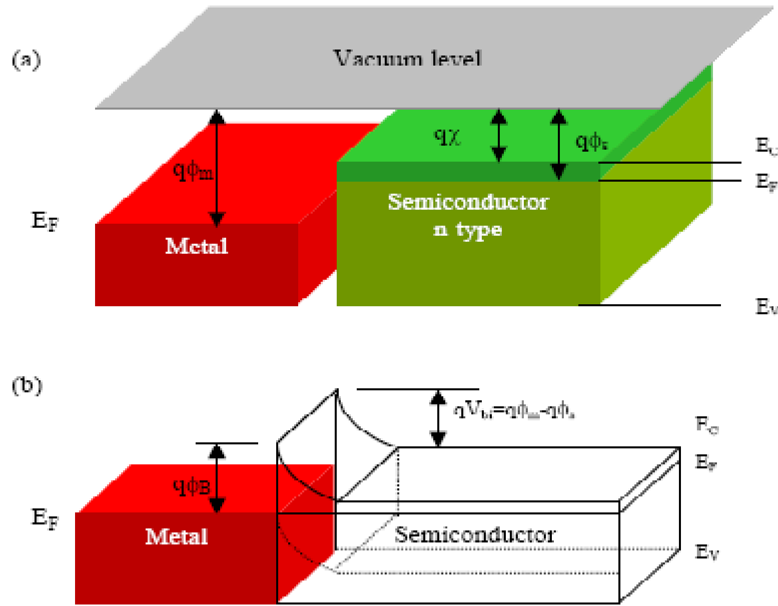

Figure 2.2 The formation of a barrier between the metal and the semiconductor when (a) Neutral and isolated and (b) in perfect contact without any oxide between them [61].

In this case the barrier height ϕ_{Bn} for n-type semiconductor can simply be determined to be the difference between the metal work function (ϕ_m) and electron affinity (χ_s) of the semiconductor:

$$q\phi_{Bn} = q(\phi_m - \chi_s) \quad . \tag{2.3}$$

For a given semiconductor and a metal, the sum of the barrier height on ϕ_{Bn} on n- and ϕ_{Bp} on p-type semiconductor is expected to be equal to the energy bandgap:

$$q(\phi_{Bn} + \phi_{Bp}) = E_G \tag{2.4}$$

This relationship for Schottky-Mott limit implies that the control of the barrier height is achieved by the choice of the metal. The second limiting case is the Bardeen limit [62] where a large density of states is present at the semiconductor to metal interface. In the Bardeen limit the barrier height ϕ_B is completely independent of the metal work function

ϕ_m in contrast to the Schottky-Mott limit and the Fermi level is said to be pinned by the high density of interface states.

Utilizing Figure 2.2 as a visual guide, the Fermi levels of the two dissimilar materials do not match when the two material's vacuum levels are set equal. The instant the metal and semiconductor are brought in contact, their Fermi levels still do not align. However, a splitting in Fermi levels signifies non-equilibrium conditions exist. This is obviously not the case since no external perturbation is being applied. Therefore, to get to equilibrium conditions, transference of electrons between the semiconductor and the metal will occur. This will create a depletion region at the interface of the metal and semiconductor. Under equilibrium conditions, the Fermi level is invariant with position (i.e. ΔE_f) = 0 as shown below in Figure 2.3.

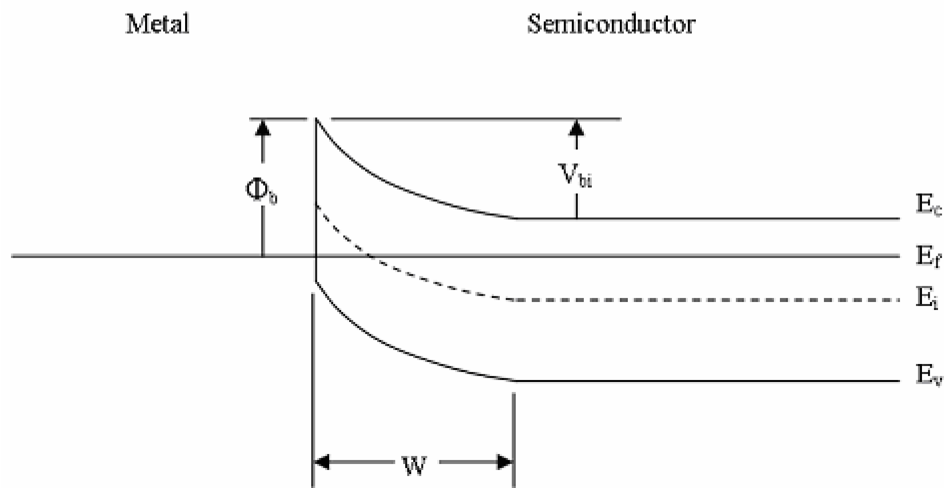

Figure 2.3 Equilibrium band diagram of rectifying Schottky contact on an n-type semiconductor [61].

Depending on the difference in work function between the metal and semiconductor, an ideal metal-semiconductor contact can either be Ohmic or rectifying. The conditions for Ohmic and rectifying contacts are given below in Table 2.1.

Table 2.1. Type of contact formed based on work function variations in an Ideal Schottky contact

	n-type	p-type
$\phi_m > \phi_s$	Rectifying	Ohmic
$\phi_m < \phi_s$	Ohmic	Rectifying

The rectifying contact as shown in Figure 2.3 has a built-in potential, V_{bi} that can be equated from the Schottky barrier height and semiconductor doping level as

$$V_{bi} = \frac{1}{q}[\phi_b - (E_C - E_{fs})_{FB}] \tag{2.5}$$

where $\phi_b = \phi_m - \chi$ is the Schottky barrier height and q is the charge on an electron. Using one-sided abrupt junction, such as those used for p^+-n junctions, the usual electrostatic variables can be obtained for non-punch through devices.

$$\text{Electric Field, E(x)} = \frac{-qN_d}{K_s \epsilon_0}(W - x) \ , \tag{2.6}$$

$$\text{Voltage, V(x)} = \frac{-qN_d}{2K_s \epsilon_0}(W - x)^2 \tag{2.7}$$

Depletion Width, $W = \sqrt{\frac{2K_s \in_0}{qN_d}(V_{bi} - V_a)}$ (2.8)

where the preceding variables are defined as follows:

N_d is the doping of the semiconductor (in contact with the metal),

K_s is the permittivity of the semiconductor,

$\in_0$ is the permittivity of free space,

V_a is the voltage applied to the Schottky contact and

x is distance from the metal-semiconductor interface.

2.1.2 CURRENT TRANSPORT MECHANISM

2.1.2.1 Current in a Forward Biased Schottky Barrier Diode

The Schottky barrier diode is a unipolar device. In other words the current flow is dominated by only one type of carrier; in this case it is the majority carrier. There are four different ways that a majority carrier can participate in current flow [63] and they are shown in Figure 2.4.

These four different methods, as labeled in the Figure 2.4, are:

1. Thermionic Emission.

2. Tunneling.

3. Recombination in the depletion region.

4. Recombination in the quasi-neutral region.

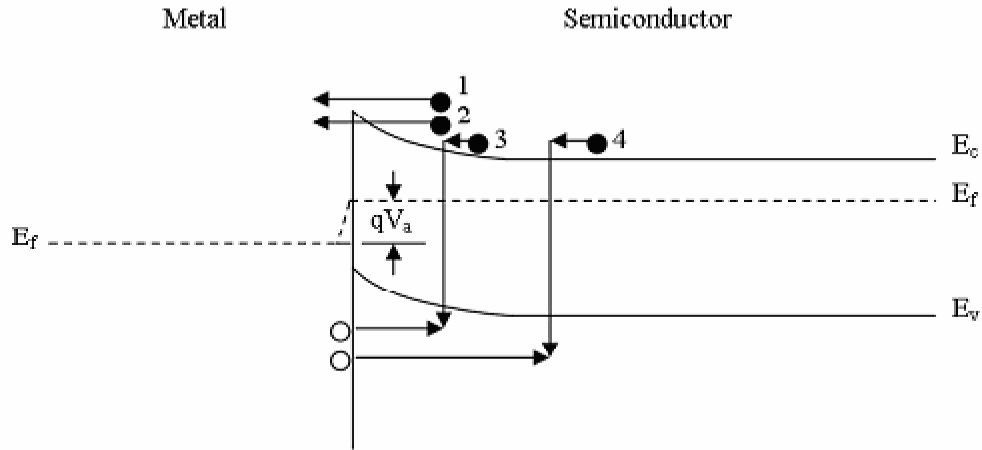

Figure 2.4 Current transport methods in a forward biased Schottky Barrier Diode [64].

The current density, J, through the Schottky barrier diode can be given by the equation [65]:

$$J = A^{*}T^{2}e^{\frac{-q\phi_b}{kT}}[\exp(\frac{qV_a}{\eta kT}) - 1] \qquad (2.9)$$

where A^{*} is the Richardson's constant, T is the temperature, V_a is the applied gate bias, k is Boltzmann's constant and η is the ideality factor. For Silicon Carbide, Richardson's constant is theoretically set at $146 \frac{Amps}{K^2 cm^2}$. Equation (2.9) is based on the reasonable assumption that the majority of the forward bias current is due to thermionic emission of majority carriers from the semiconductor to the metal. In forward bias, the other three transport mechanisms make negligible contributions to current as compared to thermionic emission.

2.1.2.2 Current in a Reverse Biased Schottky Barrier Diode

Like the forward biased regime of the Schottky barrier diode, the reverse biased diode also has four transport methods that give rise to leakage current [66]. These four methods, as labeled in Figure 2.5 are:

1. Thermionic emission.
2. Thermionic field emission.
3. Field Emission.
4. Generation in the depletion region.

These transport methods, along with leakage due to defects in the substrate, combine to produce the overall leakage current in a reverse biased Schottky barrier diode.

To describe the current flow in a reverse biased SBD the following equation is used:

$$J = A^{*}T^{2}e^{\frac{-q\phi_b}{kT}}[e^{\frac{qV_a}{\eta kT}} - 1] \approx A^{*}T^{2}e^{\frac{-q\phi_b}{kT}} \quad (2.10)$$

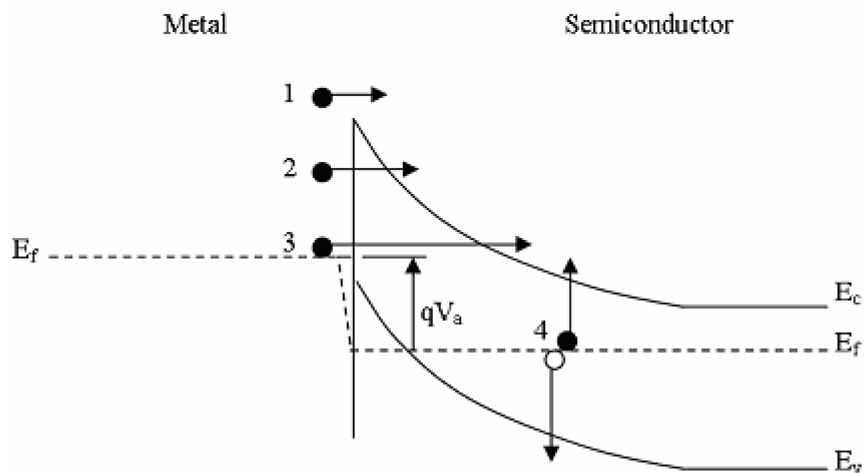

Figure 2.5 Current transport methods in a reverse biased Schottky Barrier Diode [66].

The approximation is made based on the exponentially decreasing effect of applied gate bias due to the negative applied bias, V_a , as can be seen from the reverse current equation (2.10), the barrier height, ϕ_b, is an important variable to know as precisely as possible. Hence, it is important to consider the image-force barrier lowering that occurs in a Schottky contact. This lowering of the potential barrier for carrier emission is known as the Schottky effect. The idea behind barrier lowering is that an electron inside the semiconductor will see a positive induced charge on the metal surface. This force of attraction creates an image force which serves to decrease the Schottky barrier by a value $\Delta\phi_b$. The potential barrier lowering can be calculated as [65]:

$$\Delta\phi_b = \sqrt{\frac{qE}{4\Pi K_s \in_0}} \tag{2.11}$$

Thus, as the electric field E increases, so too does the barrier height lowering. Notice that thermionic emission is dependent on the barrier height of the Schottky barrier diode. It can be seen from Figure 2.4 lowering of barrier height will correspond to higher thermionic emission.

Taking the image-force barrier lowering into consideration and plugging it into the reverse bias current equation, J_R becomes

$$J_R = A^* T^2 e^{\frac{-q\phi_b}{kT}} e^{\frac{q\Delta\phi_b}{kT}} = A^* T^2 e \frac{-q\Delta\phi_b}{kT} \tag{2.12}$$

$$= Je^{\frac{-q\Delta\Phi_b}{kT}} \quad .$$

The generation of electron hole pairs in the depletion region can also be easily described quantitatively. This leakage component can be equated as:

$$J = \frac{qn_i}{2\Gamma_g} \quad , \tag{2.13}$$

where n_i is the intrinsic carrier concentration and Γ_g is the generation lifetime. As can be seen from this equation, the reverse leakage due to generation in the depletion region is directly proportional to the width of the depletion region. Therefore, as the Schottky barrier diode is more strongly reverse biased, the depletion region will widen. However, the intrinsic carrier concentration of Silicon Carbide is small due to its wide bandgap, making the leakage current due to generation in the depletion region negligible.

To quickly, qualitatively explain the other two leakage current transport mechanisms, thermionic field emission and field emission are leakage mechanisms that depend on tunneling of carriers. Thermionic field emission happens when tunneling occurs above the Fermi level of the metal, while field emission depends on tunneling at the Fermi level of the metal. Tunneling is not an important current mechanism in Schottky contacts.

2.1.3 CAPACITANCE IN SCHOTTKY BARRIER DIODE

A useful technique for determining not only barrier height, but also the average ionized doping concentration profile is measuring the capacitance, C, of a deeply depleted Schottky barrier diode. To perform the measurement, a small a.c. signal is superimposed

on top of a d.c. bias. The a.c. signal provides a measurable charge fluctuation at the edge of the depletion region. The d.c. bias is used to sweep the Schottky barrier diode further into reverse bias. This increasing depletion width reduces capacitance as given by

$$C = \frac{K_S \in_0 A}{W} \quad , \tag{2.14}$$

where C is the measured capacitance and A is the area of contact. Knowing the width of the depletion region as a function of applied bias from equation (2.8), a doping profile can be extracted from this measurement. If there is a uniform doping concentration in the Schottky barrier diode, a plot of ($\frac{1}{C^2} - V$)will produce a straight line as shown in Figure 2.6. The average doping concentration can be extracted from the slope of the plot and is given as [65] :

$$N_d = \frac{2}{2K_s \in_0 A^2 \frac{d(1/C^2)}{dV}} \tag{2.15}$$

In addition, from the intercept of the extrapolated ($\frac{1}{C^2} - V$) line into the voltage axis, the barrier height can be found by employing :

$$\phi_b = V_{bi} + V_n + \frac{kT}{q} \quad , \tag{2.16}$$

where V_{bi} is the voltage axis intercept and V_n is the potential between the conduction band edge and the Fermi level under flat band conditions. Figure 2.6 below shows a typical plot of $(\frac{1}{C^2} - V)$ with a uniform doping concentration.

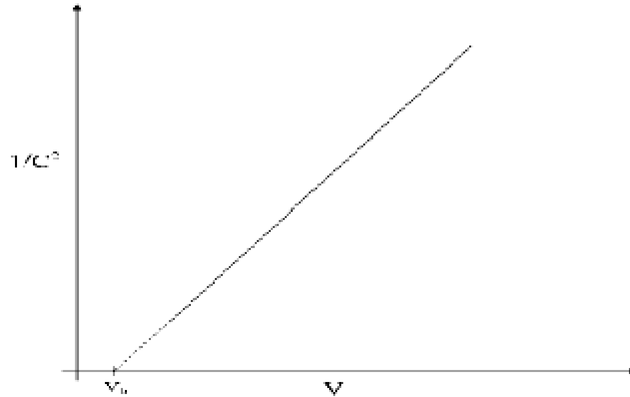

Figure 2.6 Plot of a typical $(\frac{1}{C^2} - V)$ for an SBD [65].

2.1.4 NON-IDEAL SCHOTTKY BARRIER DIODE EFFECTS

When SBDs are actually fabricated, there are many factors that contribute to their deviating from the ideal. Thus, non-idealities are as important to discuss as idealities.

2.1.4.1 Fermi Level Pinning

One important non-ideality of Schottky diodes is known as Fermi level pinning. This concept was originally presented by Bardeen in 1947. Fermi level pinning happens due to electrically active surface states on the semiconductor. These states appear because of the interruption that the surface causes to the semiconductor's lattice periodicity. Considering the states to be electrically active, when all the surface states are filled they have no net

charge. This neutral condition is often denoted as the potential Φ_0 which is measured with respect to the valence band. If there is a lack of electrons to fill the surface states, then the surface is net positive and acts donor-like in nature because the states would like to be filled with electrons. If there is an excess of electrons at the surface, then the opposite occurs and the states become acceptor-like trying to get rid of electrons to reach neutrality.

Consider a thin film between the metal and the semiconductor that allows electrons to flow, but can support a voltage. This thin film could be a native oxide such as SiO_2. If the thin film can withstand the potential difference between the metal and semiconductor work functions and there are a sufficient number of surface states, then the band bending inside the semiconductor is set by Φ_0. Hence, the barrier potential, ϕ_b, is no longer controlled by the difference between the metal and semiconductor work functions, but is instead pinned by surface states [67]. This signifies a counterpoint to the ideal Schottky model. This situation is known as the Bardeen limit. In the Bardeen limit, the barrier potential can be found as

$$\phi_b = E_g - \phi_0 \tag{2.17}$$

Figure 2.7 displays an equilibrium condition of the Fermi level pinning present under the Bardeen limit. The width of the interfacial film is denoted by δ.

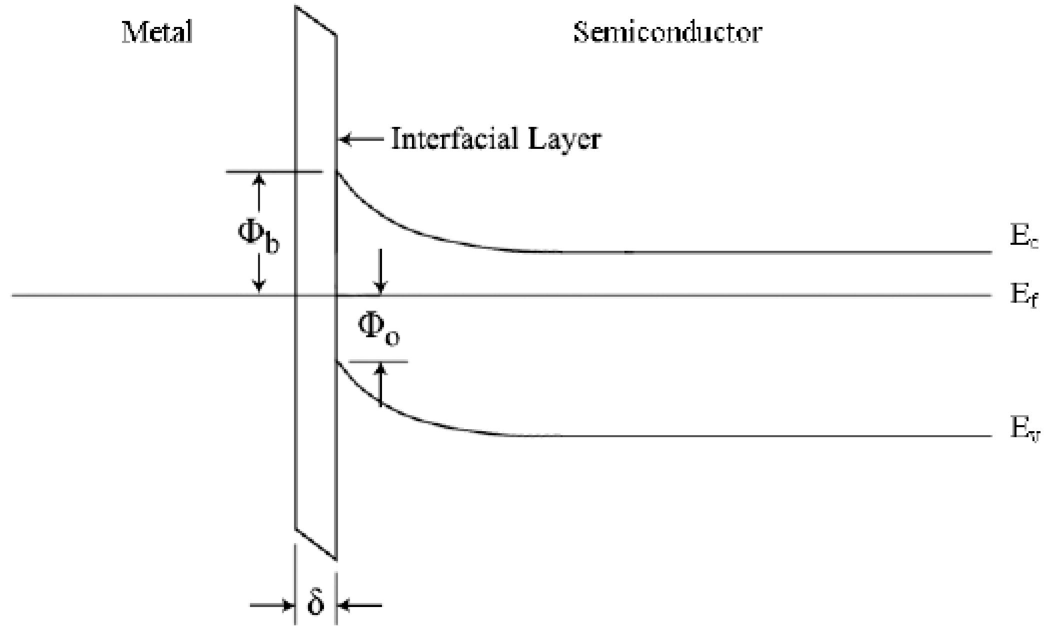

Figure 2.7 Fermi level pinning in a Schottky diode [67].

Through empirical testing, it has been found that most Fermi level pinning occurs at $\phi_0 \approx E_G / 3$, where E_G is the bandgap of the semiconductor. This is true of Si, Ge, and GaAs. There are many cases where a semiconductor does not fall strictly under the Bardeen or Schottky case. SiC is one such semiconductor.

To determine where a semiconductor falls between these polar cases, a simple testing method has been created. Multiple metal-semiconductor contacts are made using varying metals. The barrier height of each type of contact is measured and then a plot is made of the respective barrier heights versus each respective metal's work function. The equation for the plot is

$$\phi_b = S\phi_m + C_O \tag{2.18}$$

where C_O is a constant. Taking the slope of the plot gives $S = \frac{d\phi_b}{d\phi_m}$,where S is known as the index of interface behavior. If S = 1, then the contacts are purely in the Schottky limit since the barrier height follows the metal work function one-to-one. If S = 0, then the contacts follow the Bardeen limit because regardless of what contact metal is used the barrier height remains constant. For 4H-SiC, literature varies greatly on the value of S. Towards the Schottky limit, Defives found S = 0.76 and Itoh found S = 0.70. Towards the Bardeen limit, Bozack places S ≈ 0.4 and Han found S = 0.23. Regardless of exact values, all reports agree that SiC does not follow the Schottky limit exactly. This indicates that different surface preparation techniques affect the value of ϕ_b.

2.1.4.2 Series Resistance

As the applied voltage to a diode increases, the current responds in an exponential manner. In real world this exponential rise cannot continue forever. There has to be a limiting factor. This comes in the form of a series resistance. Series resistance is the resistance of the diode in series, which encompasses voltage drops due to effects such as contact resistance and the electric field in quasi-neutral regions not being truly zero. Modeling the effect of series resistance is quite simple. All that needs to be done is to substitute ($V_a - IR_s$) in equation (2.9) for V_a.

Under low forward bias conditions, this resistance does not play a large role in I-V curves due to the low current. As current increases, so too does the effect of series resistance. At high forward bias, series resistance is the dominating factor.

2.1.4.3 Breakdown Voltage in a Schottky Barrier Diode

An important characteristic of power devices is the blocking voltage that the device can handle before “breaking down”. The breakdown of a device is characterized by the impact ionization of carriers within the depletion region. Applying larger reverse bias leads to an increase in the peak electric field inside the device as established by equation (3.6). As the electric field grows, the acceleration of the carriers being swept through the depletion region is increased. The acceleration will increase to the point where the carrier has enough energy to ionize an atom in the semiconductor lattice; in other words, create an electron-hole pair. This is known as impact ionization.

Impact ionization can begin to occur unbounded if the electron-hole pair that is originally created through impact ionization gains enough energy to impact ionize another lattice site. The newly created electron-hole pair causes impact ionization at another site and so on. As newly created electron-hole pairs create their own new electron-hole pairs, an avalanche of electron-hole pair generation begins. This exponentially increasing avalanche process causes the current to quickly tend towards (negative) infinity. As such, this snowball effect of electron-hole pair creation is rightly named avalanche breakdown. This occurs at the breakdown voltage, V_{BAv} which can be found as

$$V_{BA_V} = \frac{K_s \in_0 E_c^{\,2}}{2qN_d} \tag{2.19}$$

where Ec is the critical electric field and N_d is the doping of the epilayer, provided the epilayer is not under punch-through. This is the simplest definition of breakdown.

The other type of breakdown is known as the punch-through breakdown. Under increasing reverse bias, the depletion region widens and eventually touches the device terminals resulting in carrier injection into the device from the end contacts. The current rises significantly as the diode enters breakdown. This type of breakdown is known as punch-through breakdown and corresponding reverse-bias voltage is called the punch-through breakdown voltage (V_{BPT}).

CHAPTER 3

Theoretical Technique to generate the Current-Voltage Characteristics for Nickel, Gold and Aluminium as Contact Metals for 4H-Silicon Carbide Schottky Barrier Diode.

This chapter deals with an introduction to Schottky Barrier Diode’s followed by Schottky Barrier Diode performance with the related parameters and equations . The Theoratical technique using iteration has been presented with the results which have been tallied with experimental values and eventually ends with a conclusion for improvement of the theoretical technique developed here.

3.1 SiC SCHOTTKY BARRIER DIODE

Schottky barrier diodes (SBD's) are used as high-voltage rectifiers in many power switching applications. Whenever current is switched to an inductive load such as an electric motor, high-voltage transients are induced on the lines. To suppress these transients, diodes are placed across each switching transistor to clamp the voltage excursions. PN junction diodes could be used for this application, but they store minority carriers when forward biased and

extraction of these carriers allows a large transient reverse current during switching. Schottky barrier diodes are rectifying metal-semiconductor junctions and their forward current consists of majority carriers injected from the semiconductor into the metal. Consequently, SBD's do not store minority carriers when forward biased and the reverse current transient is negligible. This means the SBD can be turned off faster than a PN diode and dissipates negligible power during switching.

A cross section of SiC Schottky Barrier diode is shown in Fig.3.1 below which is a reproduction of Fig. 1.7.

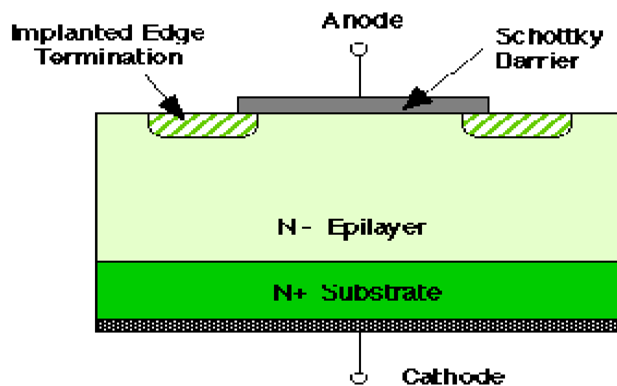

Figure 3.1 Cross section of an implant-edge-terminated Schottky barrier diode in SiC [68].

SiC Schottky barrier diodes are especially attractive because the breakdown field of SiC is about 8× higher than in silicon. In addition, because of the wide bandgap, SiC SBD's should be capable of much higher temperature operation than silicon devices. SiC SBD can be fabricated with the 4H-SiC material with Ti, Ni and Au as Schottky metals. But the performance of Schottky diode will depend on its barrier height. Lower barrier height gives less voltage drop in forward bias but gives higher leakage current. Special edge-termination is required to minimize field crowding at the edge of the metal contact.

3.2 SiC SCHOTTKY DIODE PERFORMANCE

Schottky diodes are of interest for high-power devices because they are majority carrier devices and consequently have very fast switching times and almost zero reverse recovery current. Here, some important parameters of Schottky barrier diodes for power rectifiers are described.

3.2.1 Specific on-resistance

For high-power device application, the specific on-resistance should be as low as possible. It is shown in equation (3.1) and is the sum of the specific on-resistance of epilayer, $(R_{on\text{-}sp})_{Epi\text{-}layer}$ and that of the substrate $(R_{on\text{-}sp})_{substrate}$. Since the latter is heavily doped $(R_{on\text{-}sp})_{substrate}$ can be neglected. Hence

$$R_{on\text{-}sp} = (R_{on\text{-}sp})_{Epi\text{-}layer} + (R_{on\text{-}sp})_{substrate} \approx (R_{on\text{-}sp})_{Epi\text{-}layer}$$

$$R_{on-sp} = \frac{W}{q\mu_n N_d} = \frac{4V_B^{\,2}}{e\mu_n E_C^{\,3}} \qquad (3.1)$$

where , W is the thickness of epilayer and substrate,

V_B is the breakdown voltage,

N_d is the epilayer doping and

μ_n is the electron mobility in the epilayer and substrate.

Using equation (3.1), the specific on-resistance versus the breakdown voltage for different semiconductors such as Si, 4H-SiC, and GaN have been calculated and are shown in Figure 3.2.The straight line (theoretical line) for Si, 4H-SiC and GaN is calculated assuming that the specific on-resistance of the substrate is $\leq 10^{-7}$ Ωcm^2. The contribution of the specific on-resistance for the substrate is also plotted in the same figure for the 4H-SiC.As shown in Figure 3.2, SiC has large advantage for high power application in comparison to Si. In order to design 1kV devices the specific on-resistance should theoretically be lower than

10^{-4} Ωcm^2.

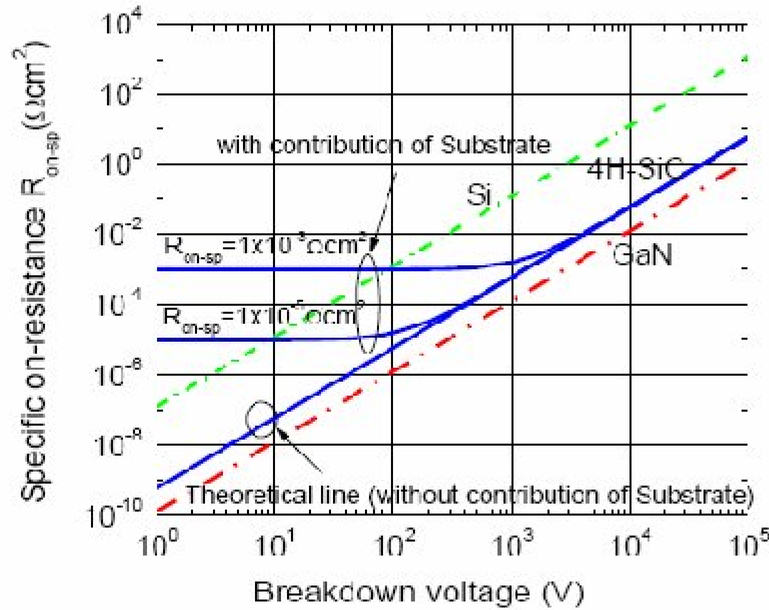

Figure 3.2 Specific on-resistances R_{on-sp} versus the breakdown voltage V_B for Si, 4H-SiC and GaN [69].

3.2.2 Forward voltage drop

Forward voltage drop across the Schottky barrier diode is given by [70]

$$V_F = \frac{\eta kT}{q}\ln(\frac{J_F}{A^*T^2}) + \eta\phi_B + R_{on-sp}J_F \tag{3.2}$$

where η is the ideality factor, which is equal to 1 for an ideal diode, k is the Boltzman's constant, J_F is the forward current density, and $A*$ (146 Amps $K^{-2}cm^{-2}$) [69] is the Richardson's constant. With the help of equation 3.2 the drop across the SiC Schottky barrier diode, V_F , can be calculated and is a function of temperature. If the value of barrier height $\O_B$ is set equal to zero and that of specific on-resistance, R_{on-sp} is negligible then logarithmic term in equation (3.2) will be nearly constant and negative. This will indicate that forward voltage drop V_F decreases linearly with temperature(T).

3.2.3 Breakdown voltage and reverse leakage current

The breakdown voltage depends on the critical field, epilayer doping, thickness and edge termination. The breakdown is given by [71]:

$$V_B = \frac{\epsilon_s E_c^{2}}{2qN_d} \tag{3.3}$$

where critical electric field Ec, with doping N_d of epilayer can be determined. The same dependence can be established using the empirical equation for 4H-SiC [72]:

$$E_C = \frac{2.49 \times 10^6}{1 - \frac{1}{4}\log(\frac{N_d}{10^{16}})} \tag{3.4}$$

Hence using equation (3.3) and (3.4) the relation between breakdown voltage and epilayer doping as also the relation between critical field and doping can be found. These relations provide an important result which indicates that a decrease in epilayer doping does not necessarily increase the breakdown voltage since the decrease in doping may correspondingly decrease the critical field. The reverse leakage current is affected by Schottky barrier height, temperature, and image force barrier height lowering. First of all, the reverse leakage current density (J_L) without the contribution of the image force lowering has been found to be:

$$J_L = -A^* T^2 \exp(\frac{-q\phi_B}{kT}) \tag{3.5}$$

Using equation (3.5), a plot of the leakage current of a Schottky rectifier as a function of the temperature and Schottky barrier height has been obtained and is shown in Figure 3.3.It is seen that the leakage current density of the Schottky rectifier increases rapidly with the temperature.

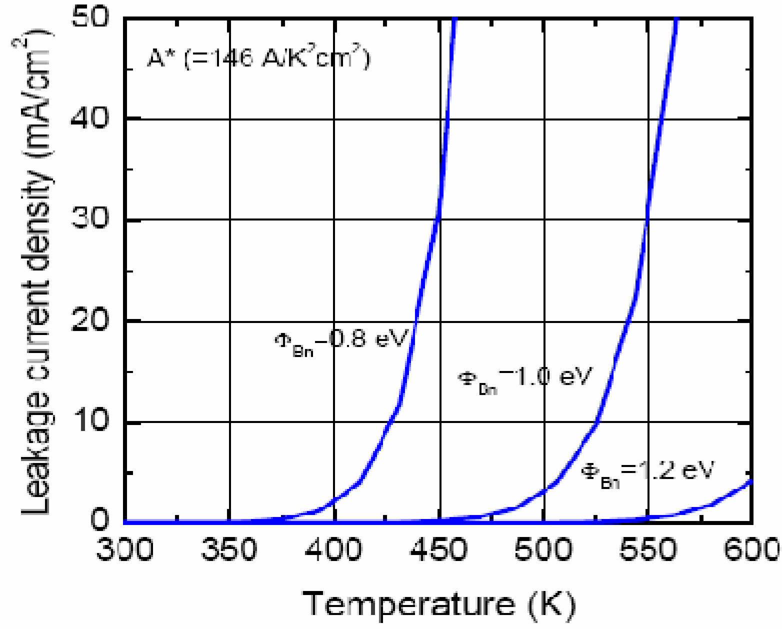

Figure 3.3 Reverse leakage current versus temperature and Schottky barrier heights [69].

3.2.4 Schottky barrier lowering

Under reverse bias, there is a reduction of the Schottky barrier height due to the image force lowering. When an electron approaches a metal, the requirement that the electric field must be perpendicular to the surface enables the electric field to be calculated as if there is a positive charge of magnitude q located at the mirror-image of the electron with respect to the surface of the metal. The barrier height reduction $\Delta \O_B$ reduction due to the image force lowering is given by [69]:

$$\Delta\phi_B = \sqrt{\frac{qE_m}{4\pi \in_s}} \ , \tag{3.6}$$

where E_m is the maximum electric field given by :

$$E_m = \sqrt{\frac{2qN_d}{\in_S}(V_R + V_{bi})} \tag{3.7}$$

Here V_R is the reverse bias voltage and V_{bi} is the built-in potential for SiC contact.

Finally leakage current density with image force barrier height lowering is given by:

$$J_L = -A^* T^2 \exp(-\frac{\phi_B}{kT}) \exp(\frac{\Delta\phi_B}{kT}) \tag{3.8}$$

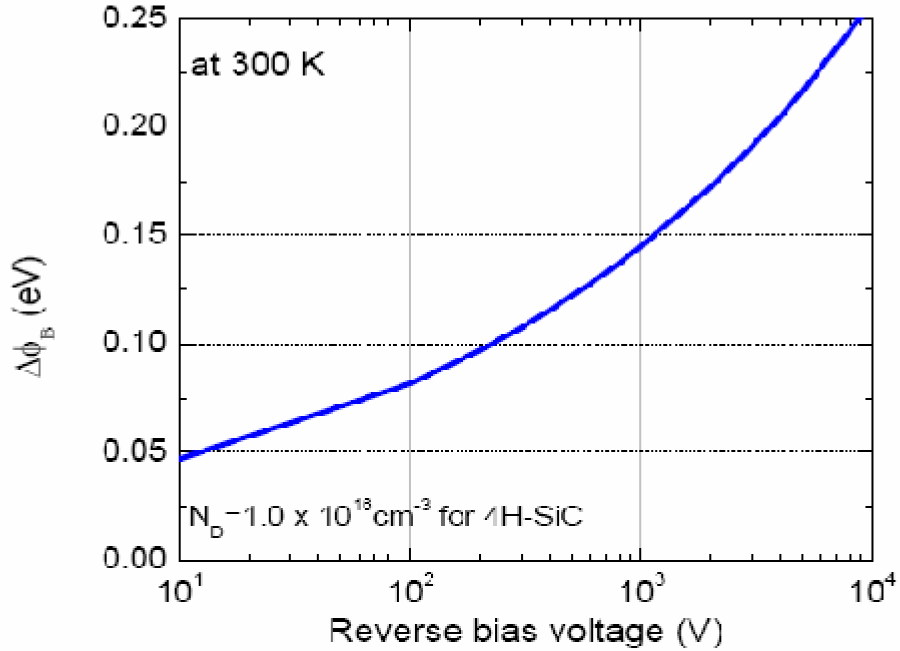

Figure 3.4.The calculated Schottky barrier height reduction, $\Delta\varnothing_B$ at room temperature due to image force lowering versus reverse bias voltage [69].

3.3 THEORATICAL TECHNIQUE TO PLOT THE CURRENT-VOLTAGE (V_F-J_F) CHARACTERISTICS OF THE SCHOTTKY BARRIER DIODE

A 4H-SiC Schottky Barrier diode has a much higher breakdown voltage because of the ten times greater electric field strength of SiC compared with Silicon (Si). 4H-SiC unipolar devices have higher switching speeds due to the higher bulk mobility of 4H-SiC compared to other polytypes. The most important parameters that quantify the efficient design of 4H-SiC

Schottky barrier Diode are blocking voltage (V_B), specific-on-resistance ($R_{on\text{-}sp}$) and forward voltage drop (V_F).For rectifiers the static on-state losses can be expressed in the forward voltage drop over the diode (V_F) and the specific on-resistance ($R_{on\text{-}sp}$) in the drift region, which accommodates the specified blocking voltage.

In SiC SBD the epilayer plays an important role in device design. For Schottky diode the switching power losses are very low and design consideration is needed to minimize the static power losses for a rated blocking voltage. In the equation of V_F, given in equation (3.8), the static-on losses are split between forward voltage drops over the Schottky junction plus the on-resistance of diode. For Schottky diode the most important design parameters are consequently the drift resistance (depending on epitaxial doping and epilayer thickness) and Schottky contact properties (depending upon barrier height and the ideality factor).

At the time of fabrication of SiC SBD, the SiC epilayer is lightly doped so that it can support the high blocking voltage and could be used for high power applications. When the SBD is biased the on-resistance of lightly doped region will increase and the power dissipation across the device will also increase .So there is a tradeoff between the doping level and the on-resistance of device. Hence it is necessary to optimize the device performance at a particular level according to the application requirements.

3.3.1 Current –Voltage Characteristics

The current-voltage characteristics of the Schottky barrier diode defined by the diode equation can be obtained by using a C++ Program. The diode equation was split into two functions and the current density for a specified forward voltage, V_F was evaluated at a point where the equality of these two functions was seen to hold. A set of values of current density, J_F and voltage, V_F were generated using this equality. The device parameters, i.e., the area, barrier height and doping levels were obtained from published work. These were found to

tally well with experimental results. The analysis has been made using 4H Silicon Carbide diodes with contacts of Nickel, Titanium and Aluminium.

The current-voltage relationship of the Schottky barrier diode has been obtained by Bethe[73], W.Schottky[74] and Crowell and Sze[75]. These have been experimentally verified by Chang and Sze[76] with devices having pre-determined parameters and dimensions. However, it is sometimes useful to obtain a solution for the current density J_F in terms of forward drop, V_F directly from the diode equation for specific values of V_F. Since the diode equation cannot be solved directly, the C++ program was used which could give by iteration the equality of two functions into which the diode equation was split. The set of values of J_F and V_F obtained using the C++ program were found to tally well with experimental results using contacts to Nickel by Saxena and Steckl[77], Sochacki[78], Titanium by Matsnnami[79] and Gold by Akira Itoh[80].

The basic device structure using a partial metal overlap over the Schottky contact by Itoh et. al[79] is shown in figure below:

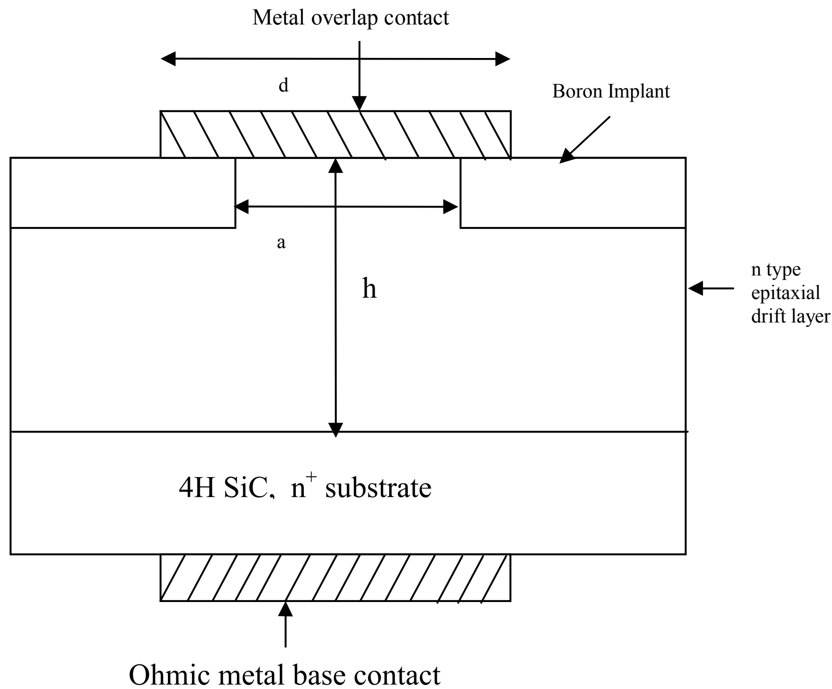

Figure 3.5 The basic 4H-SiC Schottky Barrier Diode structure

The device consisered uses an n^+-type 4H-SiC substrate on top of which a lightly doped n-type epilayer exists. The thickness of the epilayer is 'h' and boron implant from the top of the epilayer can be done with a gap in the centre over which a metal contact with finite diameter 'd' was made . The diameter of the Schottky contact was 'a'.

The (V_F-J_F) equation of the Schottky diode using thermionic emission theory is given by[77]. This can be quoted as:

$$J_F = J_S\left[\exp\left(\frac{qV_D}{\eta kT}\right) - 1\right], \tag{3.9}$$

where

$$J_S = A^* T^2 \exp\left(-\frac{q\phi_B}{\eta kT}\right), \tag{3.10}$$

is the reverse saturation current of the SBD.

Here V_D is the voltage drop on the ideal diode i.e. at the Schottky contact, k is the Boltzman's constant (CV/K), q is the electronic charge in Coulombs, A^* is the effective Richardson's constant in Amps $K^{-2}cm^{-2}$ and ϕ_B is the Schottky barrier height in volts. The Schottky barrier diode is shown in Figure 3.5.

It has a series resistance, namely the specific on-resistance R_{on-sp}, which is due to the resistance of the drift region R_D, the substrate R_{sub} and the contacts.

This is shown in Figure 3.6 .

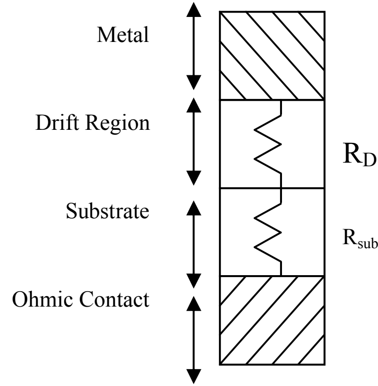

Figure 3.6 Equivalent circuit diagram of 4H-SiC Schottky Barrier Diode.

R_{on-sp} may be approximated at low and medium current levels to the resistance of the drift layer of thickness 'h'. The basic current voltage equation for such a diode has been derived by Baliga[81] and Bhatnagar et. al.[82]. The forward drop V_F of the diode can be expressed as

$$V_F = V_D + J_F R_{on-sp} \tag{3.11}$$

where V_D is the forward drop across the Schottky contact and the second term is the drop over the n-epilayer.

Combining equation (3.11) with equations (3.9) and (3.10) above gives V_F :

$$V_F = \frac{\eta KT}{q} \ln\left(\frac{J_F}{A^* T^2}\right) + \phi_B + J_F R_{on-sp} . \tag{3.12}$$

Specific on-resistance, R_{on-sp} can be calculated using the trapezoidal current flow model given by Baliga[81]. This is shown in Figure 3.7

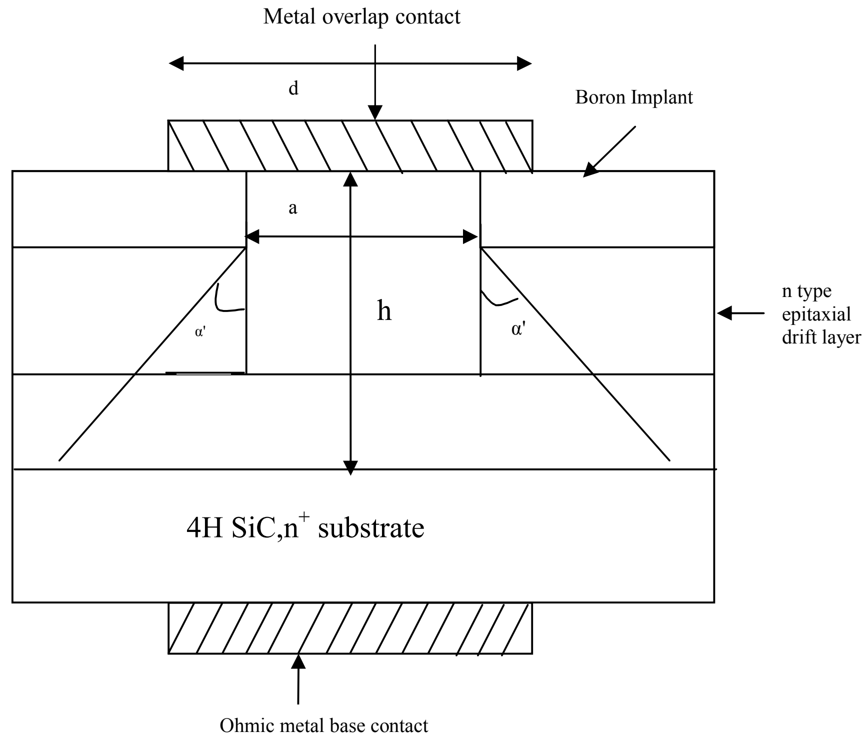

Figure 3.7 Trapezoidal current flow model of 4H-SiC Schottky Barrier Diode

The ohmic contact at the base was grounded and the top metal contact was given a negative bias. The current flow in the device starts from the Schottky contact at the top and spreads out to form the trapezoidal current profile, α' is the angle the inclined sides of the trapezoid makes with the vertical. The specific on-resistance of the device can be expressed as

$$R_{on-sp} = \rho_D \frac{L_G}{\tan\alpha'} \ln\left[1 + \frac{2h}{a}\tan\alpha'\right] \quad (3.13)$$

where ρ_D is the specific resistance of the epilayer. The value of α' was set at 26^0 so that a small angle current flow profile could be maintained across the epilayer.

The equation (3.2) can be rewritten as:

$$-\frac{\eta KT}{q}\ln\left(\frac{J_F}{A^*T^2}\right) = -V_F + \eta\phi_B + J_F R_{on-sp} \quad (3.14)$$

The left handside could be represented by function F_1 and that on the right handside denoted by function F_2. Hence the equation above can be written as $F_1 = F_2$.

A C++ program was then developed and run for a fixed value of V_F with known values of other parameters for a given range of values of J_F. The value of J_F for which $(F_1 - F_2)$ tends to zero or a minimum value was taken as the required value of J_F for a fixed value of V_F. This process was repeated for other values of V_F and a set of values of 'J_F versus V_F' was obtained. This set of calculations were repeated in the case of metal contacts for 4H-SiC using Ni, Au and Ti. The results obtained were made to tally with the current-voltage plots of the 4H SiC diodes obtained experimentally and given in references [5-8]. These are presented below.

3.3.2 Results of V_F-J_F plot for Ni/4H SiC SBD

The design parameters for 5kV-Ni/4H-SiC Schottky barrier diode are obtained from experimental data [77-78]as follows:

Barrier Height ($\O_B$) = 1.59 eV

Ideality Factor (η) = 1.05

Temperature (T) = 300° K

kT/q = 0.0259 V.

Richardson Constant (A) = 146 Amps $cm^{-2}K^{-2}$

$R_{on\text{-}sp}$ = 4.49 x 1 e-3 Ω-cm^2

The calculated (V_F-J_F) set of values and the experimentally reported[77-78] values are shown in Table 3.1. A plot of the two sets of values for (V_F-J_F) are shown in Fig. 3.8

Table 3.1

The calculated (V_F-J_F) set of values and the experimentally reported values for Ni/4H-SiC

S.No	Forward Voltage(V_F) (V)	Current Density(J_F) [ITERATION METHOD] (Amps/cm^2)	Current Density(J_F) [EXPERIMENTAL] (Amps/cm^2)
1	0	-3.95	-5.5
2	1	1.65	-4
3	1.5	2.15	1.8
4	2	2.39	2.4
5	3	2.66	2.6
6	3.5	2.75	2.8
7	4	2.82	3

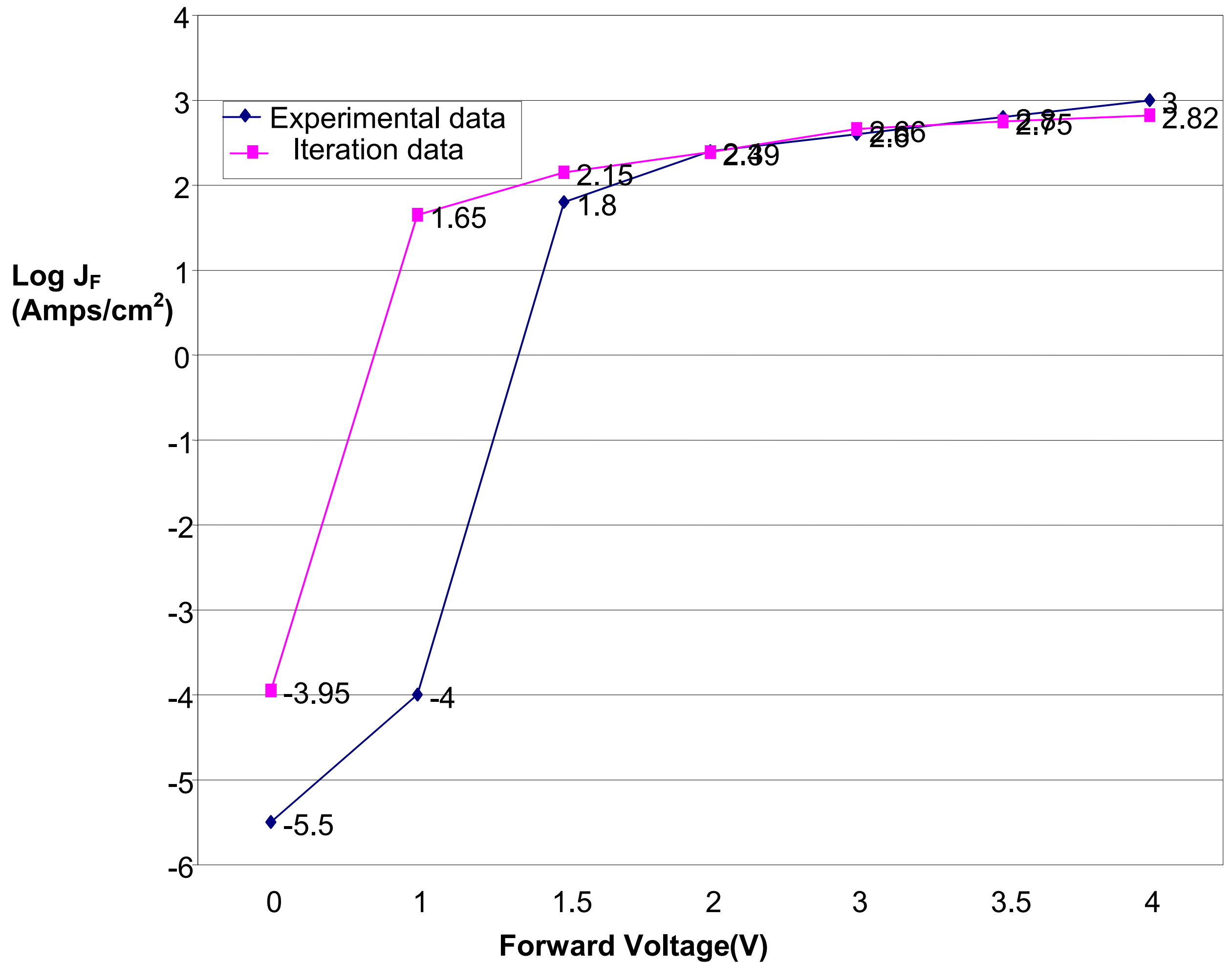

Figure. 3.8 Plots of (V_F-Log J_F) for Ni/4H-SiC SBD

3.3.3 Results of V_F- J_F plot for Ti/4H SiC SBD

The design parameters for 5kV-Ti/4H-SiC Schottky barrier diode obtained from [79] are as follows

Barrier Height ($Ø_B$)	= 1.17 eV
Ideality Factor (η)	= 1.03
Temperature (T)	= 300° K
kT/q	= 0.0259 V
Richardson Constant (A^*)	= 146 Amps $cm^{-2}k^{-2}$
Doping	= 7 x $10e^{15}$
R_{on-sp}	= 1.45 x 1 e-3 Ω-cm^2

The calculated (V_F-J_F) set of values and the experimentally reported[79] values for Ti/4H SiC are shown in Table 3.2 . A plot of the two sets of values for ($V_F – J_F$) are shown in Fig. 3.9.

Table 3.2

The calculated (V_F-J_F) set of values and the experimentally reported values for Ti/4H SiC

S.No	Forward Voltage(V_F) (V)	Current Density(J_F) [ITERATION METHOD] (Amps/cm^2)	Current Density(J_F) [EXPERIMENTAL] (Amps/cm^2)
1	0.0	.06701	1x 10e-6
2	0.2	1.6899	1x 10e-3
3	.4	25. 310	30
4	.6	103.65	80
5	.8	211	150
6	1	330.490	250
7	1.2	454.914	450
8	1.4	582.402	600
9	1.6	711.799	760
10	1.8	842.599	880
11	2.0	974.398	950

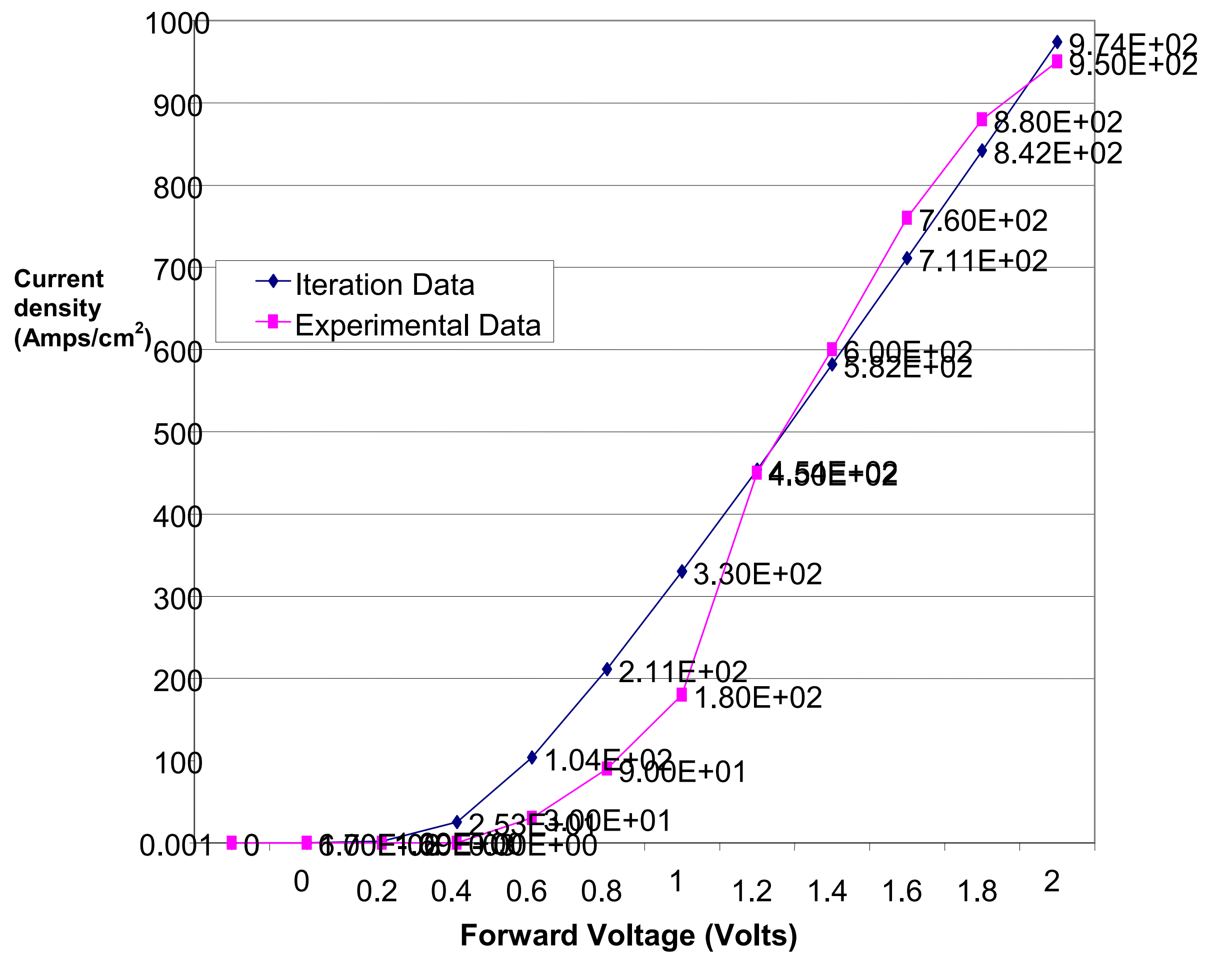

Figure 3.9 Plot of (V_F-J_F) for Ti/4H-SiC SBD

3.3.4 Results of V_F-J_F plot for Au/4H SiC SBD

The design parameters for 5kV-Au/4H-SiC Schottky barrier diode are obtained from experimental data [80]as follows:

Barrier Height (ϕ_B) = 1.73 eV

Ideality Factor (η) = 1.08

Temperature (T) = 300° K

kT/q = 0.0259 V

Richardson Constant (A) = 146 Amps $cm^{-2}k^{-2}$

$R_{on\text{-}sp}$ = 1.4 x 1 e-3 Ω-cm^2

The calculated (V_F-J_F) set of values and the experimentally reported[80] values for Au/4H SiC are shown in Table 3.3

Table 3.3

The calculated (V_F-J_F) set of values and the experimentally reported values for Au/4H SiC

S.No	Forward Voltage(V_F)	Current Density(J_F) [ITERATION METHOD] (Amps/cm^2)	Current Density(J_F) [EXPERIMENTAL] (Amps/cm^2)
1	.1	.00012	1e-8
2	.3	.00286	1e-6
3	.5	.064	1e-2
4	1	50	50
5	2	648	500
6	3	1329	1200
7	4	2024	1800

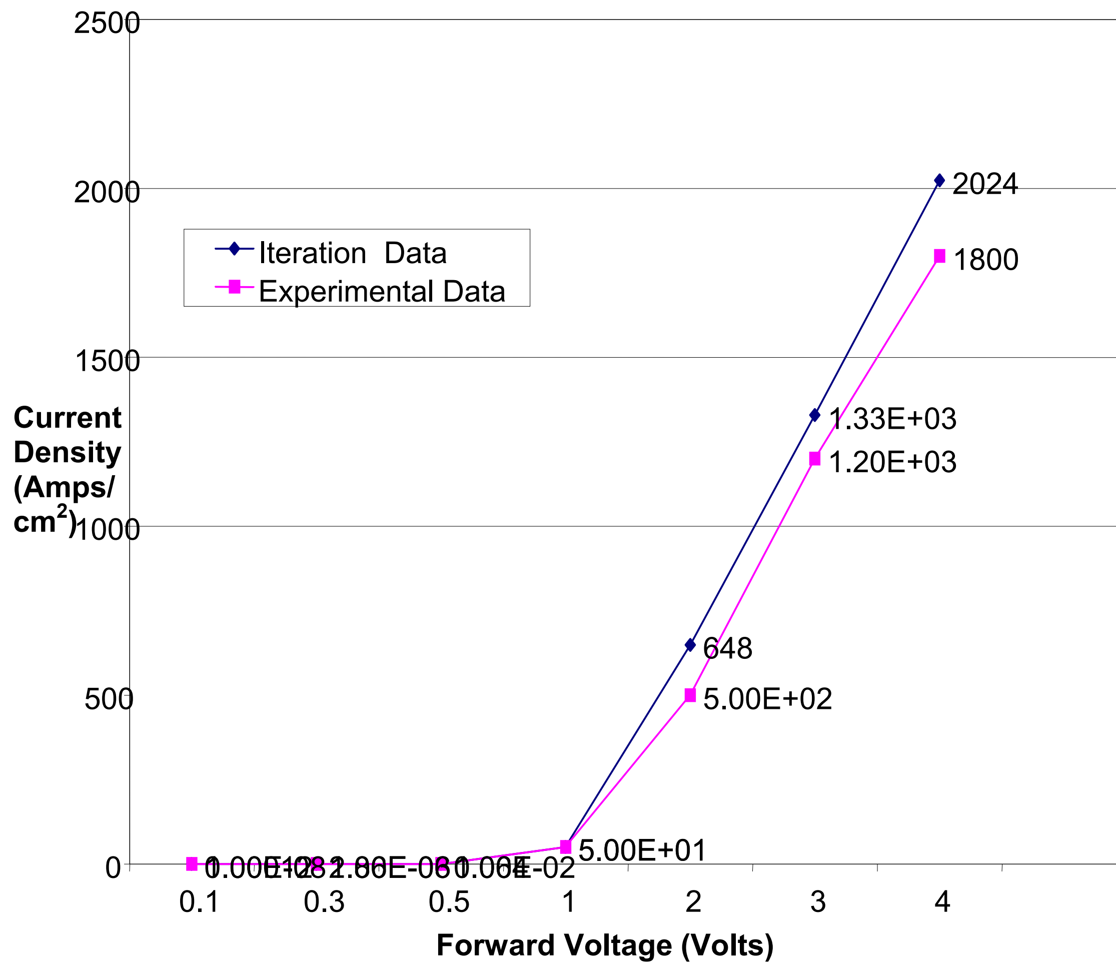

Figure. 3.10 Plots of (V_F-J_F) for Au/4H-SiC SBD.

3.4 RESULTS AND DISCUSSIONS FOR THE GRAPHS OBTAINED

The ($V_F - J_F$) plots of the 4H SiC diodes obtained by the C++ program tallies well in the case of metal contacts of Ni, Ti and Au but for some finite range of the forward drop V_F. In the case of Nickel shown in Figure 3.8 the deviation between the results using the C++ program and the experimental results obtained by Saxena et. al.[77] showed a deviation in the low voltage region for V_F less than about 1.2V but the curves tallied with each other at higher values of V_F. Similarly deviations were found to exist for the Titanium contact again upto 1.2V and at higher voltages the graphs matched with each other. This is shown in Figure 3.9 where the results obtained using C++ program has been compared with those obtained by Itoh. et. al.[79]. The best tally of the results of this work could be seen in Figure 3.10 for Au as contact metal where marginal deviation of the curve were found to exist at voltages exceeding 1.2V and they merged with each other at values of V_F less than 1V. The results shown in Figure 3.10 were plotted alongside those obtained by Itoh et. al.[80].

The deviation in the characteristic curves for nickel contact shown in Figure 3.8 is primarily because of the low value of Richardson's coefficient that were used in [77] because the effective Richardson's coefficient A^* was found to be much lower than 146A/cm^2/K^2. This results in a higher value of V_F for a specified value of J_F.

The experimental results for Titanium contact shown in Figure 3.9[79] had larger deviations from the results obtained by the C++ program in the low voltage region with $V_F < 1.2$V. However, the barrier height for Titanium was found to depend on the polarity of the crystalline phase i.e. $\phi_B = 1.17$V, for the C face and 1.1V for the SiC face. Such variations in ϕ_B may be responsible for voltage drops at the contact at high and low current levels. The present work has not taken into account such variations in ϕ_B.

The results of the C++ program for the gold (Au) contact metal shown in Figure 3.10 were seen to tally well with experimental results of Itoh et. al.[80] for all range of voltages. The effective Richardson's coefficient A^* was taken to be $146A/cm^2/K^2$ for both theory and experimentation.

3.5 CONCLUSION

The iteration method discussed above was used to draw the current-voltage characteristics of a 4H-SiC SBD. This technique can also be applied to generate characteristics of other devices from the relevant device equations where experimental facilities do not exist. The analysis of the difference between theoretical and experimental results , if available , can help in the design and development of better devices. The diode equation can be modified to include a better fit with experimental results, such as image force barrier height lowering, tunneling current and may be even minority carrier injection.

CHAPTER 4

Estimation of Power Dissipation of a 4H-SiC Schottky Barrier Diode with a Linearly Graded Doping profile in the Drift Region

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The power dissipation, P_D of the SBD is dependent on the on-state current density, J_{on}, the device cross-sectional area, A and the specific on-resistance, R_{on-sp} of the device. The value of R_{on-sp} on the other hand is the sum of the n-type epitaxial layer and n^+-substrate resistances and is inversely proportional to the doping level, N_d of the epilayer. Hence by increasing the magnitude of doping level, N_d it is possible to reduce the value of R_{on-sp} and thereby reduce the related power dissipation P_D of the device; however a large value of N_d would reduce the magnitude of the device breakdown voltage.

A novel way of reducing the power dissipation of the SBD has been developed and presented in this chapter which is based upon using a linearly graded doping profile in the epilayer, also called the drift region of the device. In this case the doping level near the contact at the top of the device was taken to be low and increased linearly towards the substrate below with a gradient , 'α' (cm^{-4}). An equation for evaluating the effective doping level (N_{eff}) of the SBD

using the gradient α was developed and the magnitude of the specific on-resistance, R_{on-sp} evaluated using 'N_{eff}' as the doping level of the device. The power dissipation of the device was calculated using N_{eff} as the epilayer doping level. The low doping level near the contact would give a wider depletion region and correspondingly a higher value of breakdown voltage(V_B). Two values of breakdown voltages, namely punch-through breakdown voltage i.e V_{BPT} and avalanche breakdown voltage, V_{AvBV} were estimated for this type of doping profile. In most cases of gradient 'α', the values of the two breakdown voltages were found to be almost equal. The chapter ends with a conclusion of discussion on the results of variation of power dissipation, P_D and the breakdown voltages V_{BPT} and V_{AvBV} with the magnitude of the gradient, α of the linearly graded profiles used.

4.1 THEORETICAL FORMULATION

The common device structure of a 4H-SiC is shown in Figure 4.1 and it's equivalent circuit is also drawn in Figure 4.2.

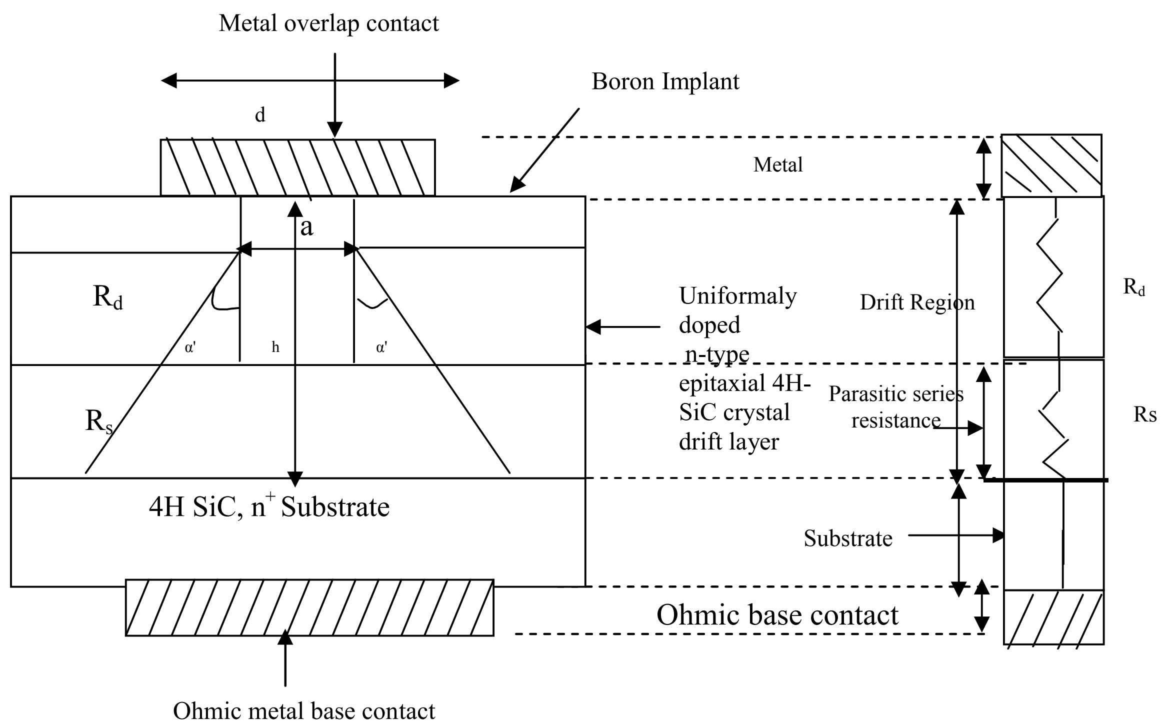

Figure 4.1The structure and regions of a 4H-SiC SBD

Figure4.2. Equivalent circuit of SBD shown in Figure 4.1

The SBD shown in Figure4.1 consists of a block of n-type 4H-SiC crystal with a given height 'h'. The metal contact at the top has a cross-sectional area 'A' and there is a base contact which may be formed using a metal or an alloy. Boron implant is made for edge termination on either side of the Schottky contact. An overlap exists between the top metallic contact of width'd' and the contact length 'a' as shown in Figure4.1. The current flow from the top contact is considered trapezoidal in shape spreading through the drift region by an angle 'α'' with the vertical at the corner edge of boron implant beneath the contact. A standard value of $\alpha'=26^{O}$ is taken for this model[83], which allows a small spread of current from the top contact to a uniform flow into the n^+-substrate below. The equivalent circuit shown in Figure 4.2 of the SBD has a specific on-resistance (R_{on-sp}) which is the sum of the series specific on-resistance of the drift region (R_D) and that of the parasitic series resistance (R_s) with uniform current flow. Beneath this region is the n^+-type heavily doped substrate region whose resistance may be considered to be zero. The equation to evaluate R_{on-sp} of the device can be given by[83].

$$R_{on-sp} = \rho_D \frac{d}{\tan\alpha'} \ln[1 + \frac{2h}{a}\tan\alpha'] \tag{4.1}$$

$$R_{on-sp} = \rho_D \frac{a}{\tan\alpha'} \ln[1 + \frac{2h}{a}\tan\alpha'] \tag{4.2}$$

where d=a for minimum overlap of contact metal has been considered.

$$\rho_D = \frac{1}{\mu_N e N_d} \tag{4.3}$$

and N_d is the donor density in the n-type epitaxial layer.

In the model proposed here for the 4H-SiC SBD, the epitaxial layer is not uniformly doped but is linearly graded with a gradient α. The device has the lowest doping level, No, near the contact, increasing with the gradient to any desired doping level, N at the substrate. This is shown in Figure4.3. The equivalent circuit of the device, with R_d being replaced by R_d' and the new parasitic series resistance Rs′< Rs has been used as Rs′ has a lower value than Rs as the doping level is more near the substrate than at the contact near the top of the device. The doping level N_d of the epitaxial layer would have to be replaced by the effective doping level N_{eff} of the linearly graded drift layer.

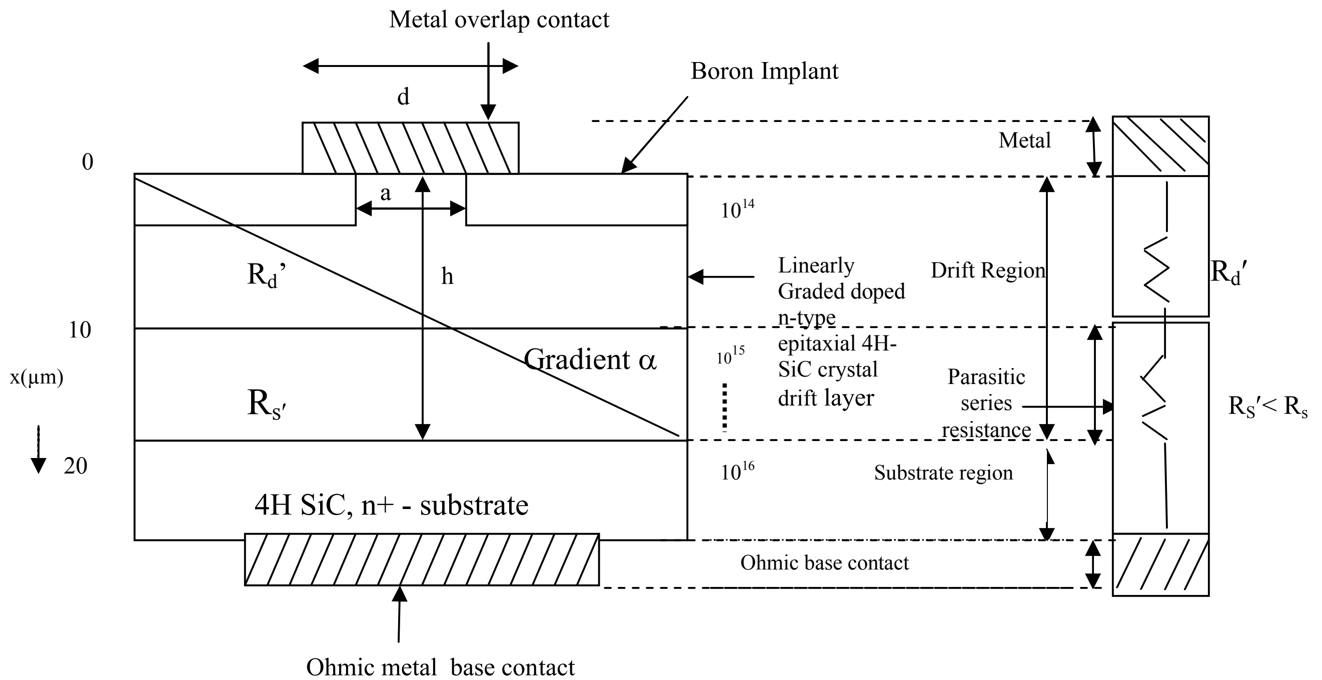

Fig4.3 The 4H-SiC SBD with a linearly graded drift region doping profile with gradient α .

Fig4.4 The Equivalent Circuit of the SBD shown in Fig4.3.

4.1.1Formulation of N_{eff}

Consider the cross-section of the epitaxial layer of Figure 4.3 shown in Figure 4.5. The resistance dR of a thin element of thickness dx at a distance x from the top of this device can be expressed as,

$$dR= \frac{1}{\mu_n^{'} eN(x)} \frac{dx}{A} \tag{4.4}$$

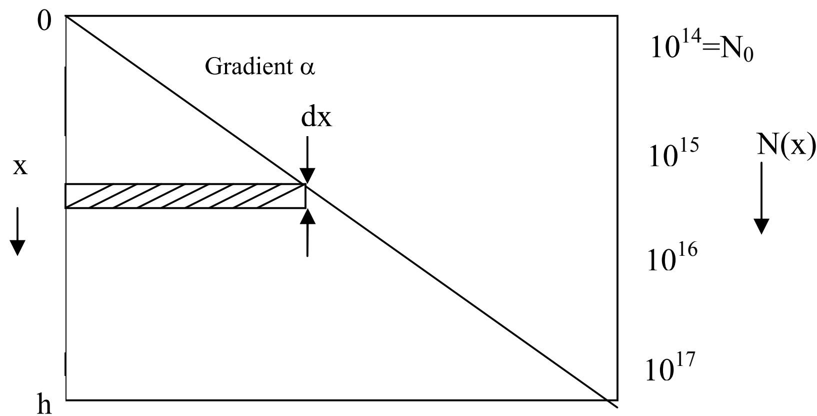

Fig4.5 Cross-section of drift region of a 4H-SiC SBD with linearly graded profile and gradient α

where A is the cross-sectional area in a direction perpendicular to the figure. The total resistance R of this layer can be evaluated by writing $N(x) = No + \alpha x$ and integrating within limits of x from 0 to h, where h is the height of the device. This gives

$$R = \int_0^h \frac{1}{\mu_n^{'} eA} \frac{dx}{(No + \alpha x)} \tag{4.5}$$

writing $Z= No + \alpha x$, $dZ=\alpha dx$ gives,

$$R = \frac{1}{\mu_n' eA} \int_{N_0}^{N_0+\alpha h} \frac{dZ}{\alpha Z} = \frac{1}{\mu_n' eA\alpha} \ln\left[\frac{N_0 + \alpha h}{N_0}\right] = \frac{1}{\mu_n' eA\alpha} \ln\left[1 + \frac{\alpha h}{N_0}\right] \quad (4.6)$$

If the effective concentration of this layer is N_{eff} then R may also be written as

$$R = \frac{1}{\mu'_n e N_{eff}} \frac{h}{A} \quad (4.7)$$

Comparing equations. (4.6) and (4.7), N_{eff} may be written as :

$$N_{eff} = \frac{\alpha h}{\ln(1 + \frac{\alpha h}{No})} \quad (4.8)$$

The magnitude of $R_{on\text{-}sp}$ of the linearly graded drift layer i.e $R'_{on\text{-}sp}$ can be obtained from equation (4.2) with ρ_D replaced by ρ_D'

$$R'_{on-sp} = \rho_D' \frac{\alpha}{\tan \alpha} \ln[1 + \frac{2h}{a} \tan \alpha'], \quad (4.9)$$

where $\rho_D' = \frac{1}{\mu_n' e N_{eff}}$ (4.10)

with μ_n' being the value of mobility corresponding to doping level, N_{eff} of the drift region.

4.1.2 The device height 'h'

The height 'h' of the device has been set using a specific value of reverse bias voltage as the punch through breakdown voltage. This is also set close to the avalanche breakdown voltage of the device using the condition $\alpha_p W = 1$, the condition for avalanche breakdown and has been set equal to W, the depletion width at punch through and α_p is the hole impact ionization coefficient, wherein it has been assumed that hole in n type wide depletion region in the drift layer started the ionization process [84].

4.1.3 The Calculation of Power Dissipation (P_D)

The equation for power dissipation P_D can be written as [85]:

$$P_D = \frac{1}{2}\left(J_{on}{}^2 A R_{on-sp} + J_L A V_B\right), \tag{4.11}$$

where J_{on} is the on-state current density, A is the device cross-sectional area for current flow, V_B is the reverse blocking voltage and J_L is the leakage current density .For a 50% duty cycle, the magnitude of J_L in SiC devices is too small compared to silicon devices and hence the second term in eq. (4.11) can be neglected giving:

$$P_D = \frac{1}{2}(J_{on}{}^2 A R_{on-sp}) \ . \tag{4.12}$$

4.1.4 Evaluation of the On-state Current Density(J_{on})

The current-voltage equation of the Schottky diode using thermionic emission theory has been given by Bethe [86]:

$$J_F = J_S[\exp(eV_D/\eta kT)-1], \tag{4.13}$$

where,

J_F is the on-state forward current density and

V_D is the voltage drop across the Schottky diode.

Here J_s is the reverse leakage current density given by :

$$J_s = A^* T^2 \exp(-e\, \varphi_B/\eta kT). \tag{4.14}$$

The term A^* in eq. (4.14) is the Richardson's constant in (Amps cm^{-2}K^2), φ_B is the barrier height in volts and T is the device temperature in ^oK.

The basic current–voltage equation for such a diode has been derived by Bhatnagar et.al[87]. The diode forward voltage drop (including drift layer) V_F can be expressed as

$$V_F = V_D + J_F R_{on-sp} \tag{4.15}$$

Combining equations (4.13) through (4.15) and writing J_{on} for J_F the voltage V_F may be expressed as:

$$V_F = \frac{\eta kT}{e}\ln\left(\frac{J_{on}}{A^*T^2}\right) + \varphi_B + J_F R_{on-sp} \quad . \tag{4.16}$$

Values of J_{on} for different values of V_F in the on-state of the diode was obtained by iteration by a simple technique and C++ program[50]. Under forward bias and in the on state, the magnitude of V_D and V_F are small. Hence effect of barrier height lowering, $\Delta\phi$ has not been included in equations (4.14) and (4.16) above.

The calculations for power dissipation were performed knowing N_d, N_{eff}, $R_{on\text{-}sp}$, $R'_{on\text{-}sp}$ and the magnitude of J_{on} and V_F, for linearly graded drift layers of the 4H-SiC SBD's .

4.1.5 Calculation of Breakdown Voltages

The punch through breakdown voltage V_{PBV} was determined at a high reverse bias voltage, V_R for a uniformly doped semiconductor of 4H-SiC SBD and the depletion region width W at this voltage was set equal to the device height 'h'. The avalanche breakdown voltage was obtained using the condition α_p W=1 , to give the magnitude of α_p. The critical field Ec corresponding to this value of α_p was obtained from the data of Ayalew[88]. The magnitude of avalanche breakdown voltage V_{AvBV} was then obtained using the equation :

$$V_{AvBV} = \frac{2}{3} E_c W' \quad \text{, for linearly graded drift region of SBD.} \qquad (4.17)$$

The depletion region width was calculated using the formula:

$$W' = \sqrt[3]{\frac{12 \in_S (V_g + V_R)}{e\alpha}} = \sqrt[3]{\frac{12 \in_s V_R}{e\alpha}} \quad \text{, for linearly graded drift region SBD,} \qquad (4.18)$$

where V_g is the gradient voltage and $V_g \ll V_R$, the applied reverse voltage equal to the avalanche breakdown voltage.

In equation (4.18), ϵ_s denotes the permittivity of 4H-SiC and α is the concentration gradient which is 10^{14} near the top of the device increasing linearly to 10^{15}, 10^{16} ------, near the substrate over the device height 'h'.

The calculation of Ec for avalanche breakdown in a linearly graded profile was made using equation (4.18):

$$E_C = \frac{e\alpha W'^2}{8\varepsilon_S}, \tag{4.19}$$

where W' is the depletion region width at breakdown.

4.2 CALCULATIONS AND RELATED GRAPHS

The device height 'h' was kept 231μm, the depletion region width at 5kV for a uniformly doped drift region with doping of 10^{14}per cc. The concentration gradients (cm^{-4}) selected arbitrarily are 10^{14}-10^{15}, 10^{14}-10^{16}, 10^{14}-10^{17} and 10^{14}-10^{18} per cc, over the device height of 231μm. This gave the concentration gradient 'α' in each case. The effective carrier concentration 'N_{eff}' per cc, for linearly graded epitaxial layer was calculated using equation (4.8). The value of the average doping dependent carrier mobility μ_n for any specific concentration gradient was obtained from Roschkc and Schwierz for 4H-SiC [89]. The specific on-resistance R'on-sp was calculated using equation (4.9), treating the medium doping level as equal to N_{eff}. The depletion region width 'W'' for a reverse bias voltage of 5kV was calculated using equation(4.18). The power dissipation for a given concentration gradient for the current

density levels were calculated using equation (4.12) with the same value of the device cross-sectional area 'A' and the corresponding values of R′on-sp. The results are shown in Table 4.1.

Table 4.1

Calculation of power dissipation P_D of 4H-SiC SBD with linearly graded drift region

Current density (Amps/cm^2) ↓	Neff = 3.905 x 10^{14} atoms per cc	Neff = 2.148 x10^{15} atoms per cc	Neff = 1.446 x10^{16} atoms per cc	Neff = 1.085 x10^{17} atoms per cc
	μ_n= 960 cm^2 per Vs	μ_n = 950 cm^2 per Vs	μ_n = 900 cm^2 per Vs	μ_n = 600 cm^2 per Vs
	Ron-sp=0.04038Ω-cm^2	Ron-sp=0.07418 Ω-cm^2	Ron-sp= 11.63 x10^{-3} Ω-cm^2	Ron-sp=2.325 x10^{-3} Ω-cm^2
J_{on}	P_D(1) Watts ↓	P_D(2) Watts ↓	P_D(3) Watts ↓	P_D(4)Watts ↓
100	0.15849	29.115e-3	4.565e-3	912.56e-6
200	0.63396	0.1164	18.260e-3	3.650e-3
400	2.5358	0.4658	73.042e-3	14.60e-3
600	5.7056	1.048	164.34e-3	32.85e-3
800	10.143	1.863	0.29217	58.40e-3
1000	15.849	2.9115	0.4565	91.25e-3

4.2.2. Calculation of Breakdown Voltage

The punch through breakdown voltage for the linearly graded epitaxial layer was obtained from the depletion region width 'W'', for a given concentration gradient 'α' of 3.88 x $10^{16}cm^{-4}$ .The device height 'h' nonetheless was set at 231 μm, the device height used for uniformly doped drift region devices. The value of the critical field, Ec, for linearly graded profile was calculated using equation (4.19) and the value of W' obtained at 5kV was treated as the depletion width for avalanche breakdown. This was repeated for other values of breakdown voltages and gradient 'α'.The magnitude of V_{AvBV} was then calculated using equation (4.17).The results are shown in Table 4.2.

Table 4.2

Breakdown voltages of 4H-SiC SBD for linearly graded epitaxial layer

Device height=h=W=231μm

S.No	GRADIENT $\alpha(cm^{-4})$	W' (μm)	$E_C = \left(\frac{e\alpha W'^2}{8\varepsilon_S}\right)$ (V/cm)	V_{AvBV}(kV) $=\frac{2}{3}E_C W'$	V_{PBV}(kV)
1	3.88 x 10^{16}	201.07	3.72 x 10^5	4.986	5
2	4.27 x 10^{17}	90.3	8.25 x 10^5	4.966	5
3	4.31 x 10^{18}	41.8	2.86 x 10^6	4.966	5
4	4.31 x 10^{19}	19.4	3.84 x 10^6	4.966	5
5	4.4 x 10^{19}	22.7	5.26 x 10^6	7.960	8

4.3 CONCLUSION

An analysis of the data presented in Table 4.1 shows that power dissipation P_D for 4H-SiC SBD’s having a linearly graded drift region profile decreases with increase in the magnitude of N_{eff}, the effective drift region doping concentration. Since N_{eff} increases with the magnitude of concentration gradient ‘α’, the power dissipation also decreases with increase in the value of α. The result for the estimated breakdown voltages, V_{AvBV} and V_{PBV} shown in Table 4.2 for α of 3.88×10^{16} cm^{-4}, the critical field, Ec was found to increase with α. The breakdown voltage V_{AvBV} and V_{PBV} changed very little from 5kV. However at a value of α of $4.4 \times 10^{19} cm^{-4}$ V_{AvBV} was found to rise to 7.96 kV as against V_{PBV} of 8kV. The device height h=W' could be substantially reduced for the punch through breakdown voltages V_{PBV} given in Table 4.2. Hence thinner devices with higher breakdown voltages and lower power dissipation may be designed using linearly graded profiles in the drift region of 4H-SiC SBD’s.

CHAPTER 5

Comparison of Estimated Values of Power Dissipation and Breakdown Voltages of a 4H-SiC SBD for Linearly Graded and Uniformly Doped Drift Regions.

The calculation of the estimated values of power dissipation and breakdown voltages, V_{PBV} and V_{AvBV} for linearly graded drift region for a 4H-SiC SBD had been performed and the values quoted therein. The present chapter focusses on the relative decrease in the values of power dissipation and the increase in breakdown voltages of these devices compared to those with uniformly doped drift regions. It has been theoretically established in Chapter 4 that linearly graded drift region devices for a given value of the effective doping level, N_{eff} when tallied for power dissipation, P_D with uniformly doped drift region devices having a doping level $N_d \approx N_{eff}$, can yield a much lower value of P_D.

At the same time, calculations for highest attainable breakdown voltages show that for a given device height 'h' , linearly graded devices yield a breakdown voltage of about 8kV as against 5kV for devices having uniformly doped drift regions.

5.1 INTRODUCTION

The calculation of power dissipation using uniformly doped drift regions has been presented first, followed by the estimated breakdown voltages. These results have been compared with those obtained in Chapter 4 for linearly graded profiles in the drift region of these devices. A comparison of the results of power dissipation and breakdown voltages for these two types of devices has been presented at the end. The final results show the superiority of linearly graded drift region devices over uniformly doped ones.

5.2 POWER DISSIPATION OF UNIFORMLY DOPED DRIFT REGION DEVICES.

5.2.1 The Specific on Resistance ($R_{on\text{-}sp}$)

The calculation of the power dissipation of the uniformly doped drift region 4H-SiC SBD's was performed using the same set of equations i.e equation (4.11) and (4.12) used in Chapter 4 with the effective concentration N_{eff} of the drift region being replaced by the drift region doping level, N_d . The structure and regions of the 4H-SiC SBD with the uniformly doped drift region are shown in Fig 5.1 and its equivalent circuit shown alongside in Fig. 5.2.

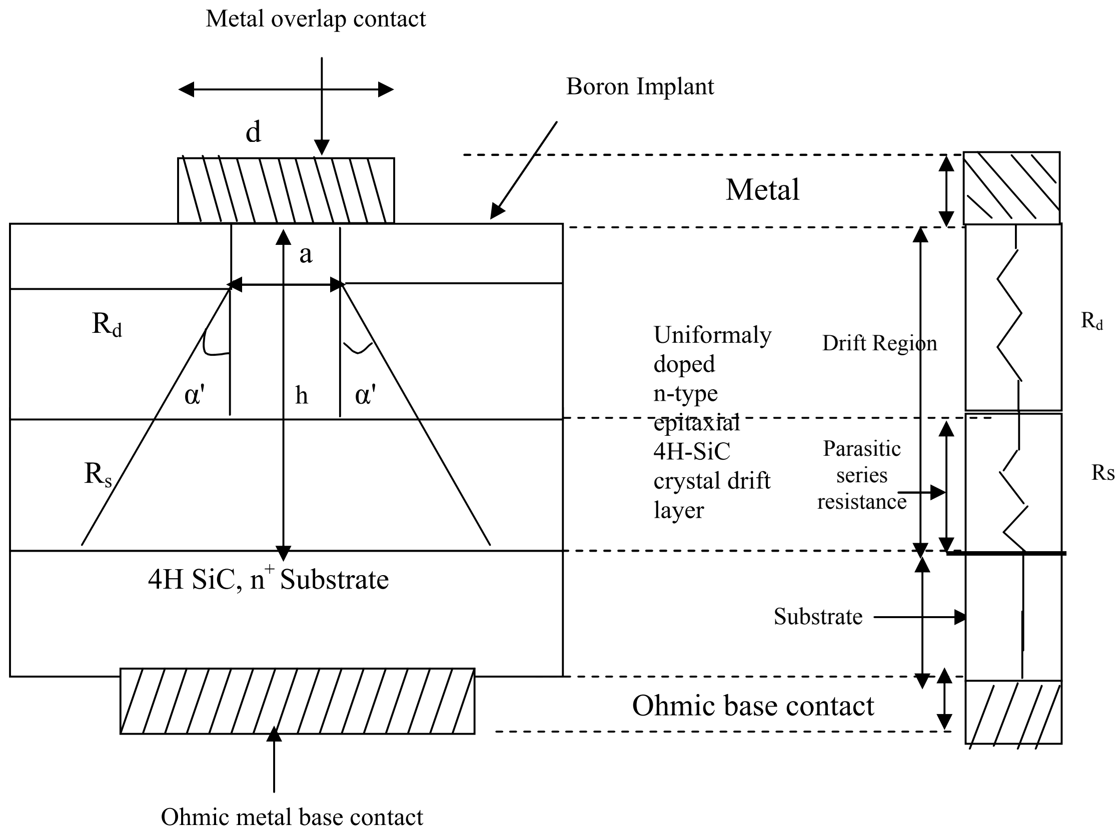

Fig.5.1 The structure and regions of a Uniformly doped 4H-SiC SBD

Fig5.2 Equivalent circuit of SBD shown in Fig5.1

The specific on resistance, Ron-sp of the device can be expressed as:

$$R_{on-sp} = \rho_D \frac{d}{\tan\alpha'} \ln[1 + \frac{2h}{a} \tan\alpha'] \qquad (5.1)$$

where the symbols have their usual significance.

The specific resistance, ρ_D is given by

$$\rho_D = \frac{1}{\mu e N_d} \quad , \qquad (5.2)$$

where d=a for minimum overlap of the contact metal has been used.

The drift region resistance is represented by R_D and the parasitic series resistance by $R_{S.}$

5.2.2 Device Height 'h' and breakdown voltages (V_{PBV} & V_{AvBV})

The device height 'h' has been set using a specific value of reverse bias voltage of 5kV as before and the lowest doping level of 10^{14} per cc which gave a depletion region width W of 231µm. Thus the condition W=h has been used to determine the device height 'h'. This value of the reverse bias voltage is the value of the punch thru breakdown voltage,V_{PBV}. The condition $\alpha_p W = 1$ gave the value of α_p , the hole ionization coefficient. The corresponding field which generated this value of W was obtained from the data by Ayalew[88]. This gave the critical field Ec and the magnitude of the avalanche breakdown voltage V_{AvBV} for the uniformly doped drift region devices given by :

$$V_{AVBV} = \frac{1}{2} E_C W \ . \tag{5.3}$$

The depletion region width W for a given reverse voltage V_R is given by

$$W = \sqrt{\frac{2\varepsilon_s (V_{bi} + V_R)}{eN_d}} \approx \sqrt{\frac{2\varepsilon_s V_R}{eN_d}} \tag{5.4}$$

where V_{bi} is the built in potential and $V_{bi} << V_R$. At breakdown, $V_R = V_{AvBV}$.

5.2.3 Power Dissipation (P_D)

For a given on-state current density J_{on} and specific on-resistance $R_{on\text{-}sp}$, the value of power dissipation, P_D can be calculated using equation (4.11), neglecting the contribution of the reverse current density, J_L. This may be written as :

$$P_D = \frac{1}{2}(J_{on}^2 A R_{on-sp}) \quad , \tag{5.5}$$

where A is the device cross-sectional area

5.3 CALCULATION OF POWER DISSIPATION (P_D)

The device height 'h' was set equal to the depletion region width 'W' using equation (5.4) corresponding to a reverse bias of 5kV for the uniformly doped epitaxial layer with a doping level of 10^{14} per cc. The value of W obtained was 231μm with ϵ_s=9.7 for 4H-SiC. The doping dependent mobility values were obtained from Roschke and Schwierz (89). The magnitude of R_{on-sp} was calculated using equation (5.1) with α=26º and Schottky contact of length 'a' of 100μm.The contact width was taken to be 78.5×10^{-6} cm^2.

The on state current density(J_{on}) values were then selected, ranging from 100 to 1000 amps/cm^2. The corresponding values of power dissipation (P_D) were then calculated using equation (5.5). This was repeated for drift region doping levels of 10^{15}, 10^{16} and 10^{17} per cc. The results are shown in Table 5.1

Table 5.1

Calculation of power dissipation (P_D) of 4H-SiC SBD with uniformly doped drift region

Current density J_{on} (Amps per cm^2) ↓	$N_d = 1x\ 10^{14}$ atoms per cc	$N_d = 1x\ 10^{15}$ atoms per cc	$N_d = 1x\ 10^{16}$ atoms per cc	$N_d = 1x\ 10^{17}$ atoms per cc
	μ_n= 960 cm^2 per Vs	μ_n = 950 cm^2 per Vs	μ_n = 900 cm^2 per Vs	μ_n = 600 cm^2 per Vs
	Ron-sp=1.577Ω-cm^2	Ron-sp=159.38x10^{-3} Ω-cm^2	Ron-sp=16.82x10^{-3} Ω-cm^2	Ron-sp=2.52 x 10^{-3} Ω-cm^2
	$P_D(1)$ Watts ↓	$P_D(2)$ Watts ↓	$P_D(3)$ Watts ↓	$P_D(4)$ Watts ↓
100	0.6195	62.55x10^{-3}	6.601 x 10^{-3}	989.1 x 10^{-6}
200	2.478	0.2502	26.40 x 10^{-3}	3.956 x 10^{-3}
400	9.912	1.0008	0.1056	15.82 x 10^{-3}
600	22.302	2.2518	0.2376	35.607 x 10^{-3}
800	39.649	4.0032	0.4225	63.30 x 10^{-3}
1000	61.95	6.255	0.660	98.91 x 10^{-3}

The plots of power dissipation, P_D versus current density for uniformly doped and linearly graded drift region devices for a 4H-SiC SBD has been obtained from Table.4.1 and Table 5.1. These are shown in Fig. 5.3.

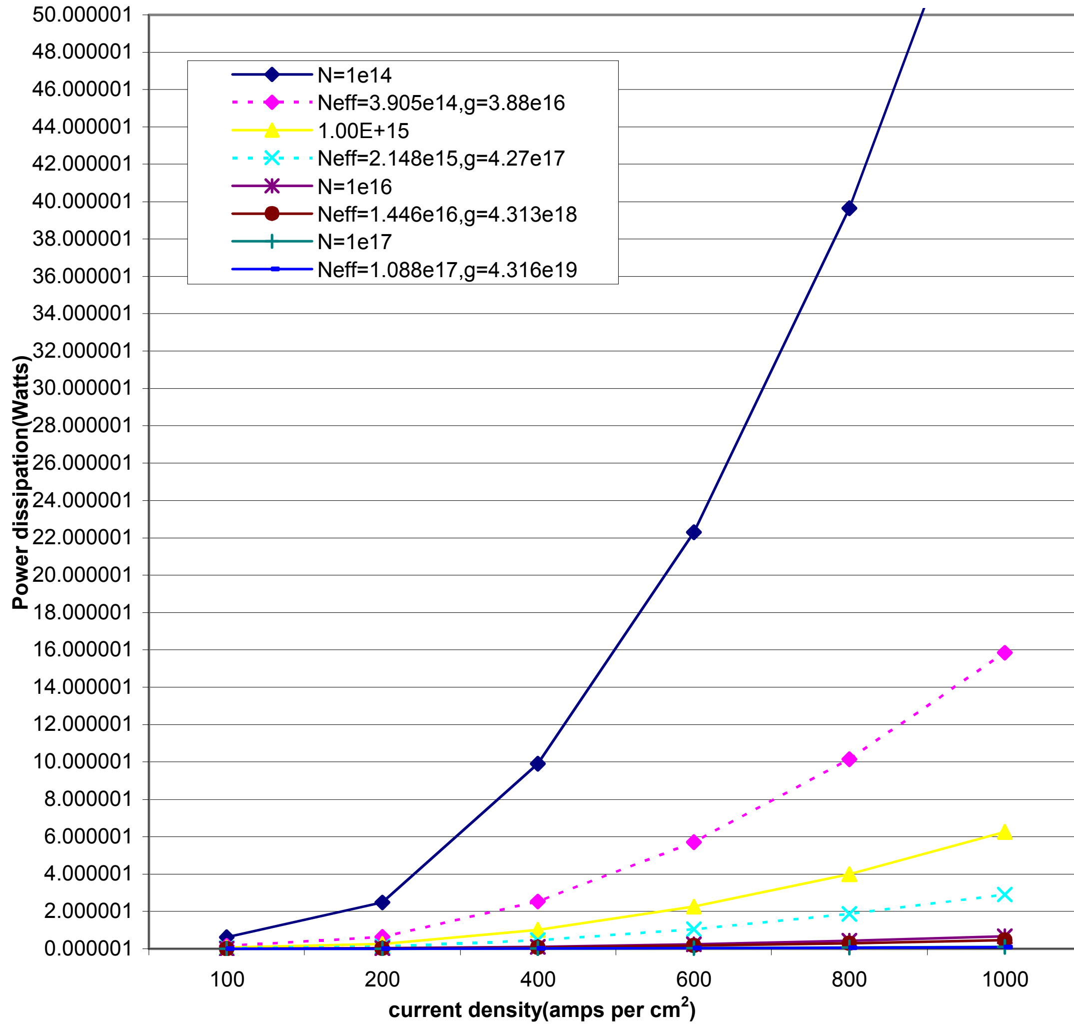

Figure 5.3 Plot of power dissipation versus on-state current density for uniform and linearly graded drift region in 4H-SiC SBD.

It can be seen from an analysis of the plots of Fig 5.3 that for nearly same values of doping levels N_d for uniformly doped and N_{eff} for linearly graded drift region devices, the fall in power dissipation is significant at high current density levels. Thus for $N_d=10^{14}$ per cc and $N_{eff}= 3.905x10^{14}$ per cc at a gradient of $3.88x\ 10^{16}\ cm^{-4}$,the percentage drop in power dissipation is as high as 74.4 at a value of J_{on} of 1000 amps/cm^2. This percentage drop decreases with increasing magnitude of doping levels and concentration gradient, falling to values as low as 7.74% at a gradient of $4.32x10^{19}\ cm^{-4}$ at the same value of J_{on}. This has been shown in Fig. 5.4.

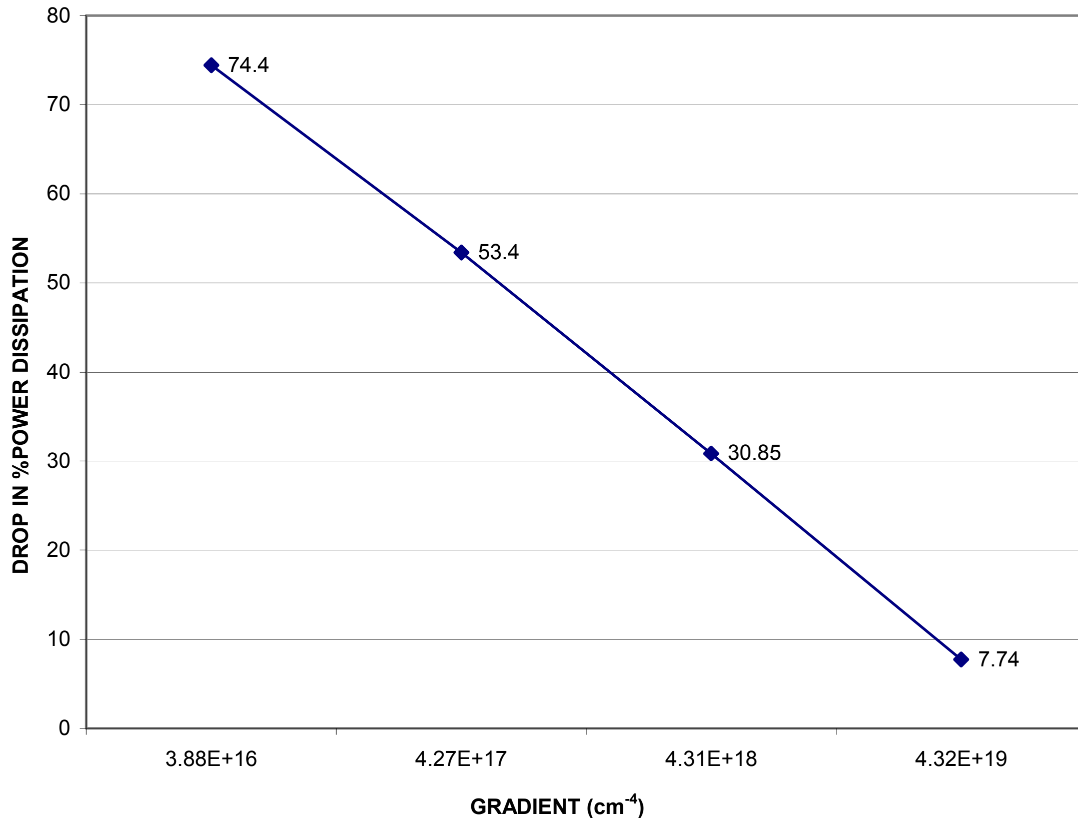

Figure 5.4. Percentage drop in power dissipation versus concentration gradient in a 4H-SiC SBD compared to SBD's with uniformaly doped drift regions.

5.4 CALCULATION OF BREAKDOWN VOLTAGES (V_{PBV} and V_{AvBV})

The punch through breakdown voltage, V_{PBV} was set for a breakdown voltage of 5kV for a 4H-SiC SBD with a uniformly doped drift region having a doping level of 10^{14} per cc. The corresponding device height was equal to the depletion region width 'W' at this voltage which was found to be equal to 231µm. The condition of avalanche breakdown $\alpha_p W=1$ was then used which gave the value of α_p for W = 231 µm. The magnitude of Ec, the critical field for avalanche breakdown was obtained from Ayalew [88] from this value of α_p. The avalanche breakdown voltage V_{AvBV} was then calculated using equation (5.3), knowing Ec and W, the depletion region width at breakdown. This was repeated for values of doping levels of 10^{15},10^{16}, 10^{17} per cc. The results are shown in Table 5.2.

Table 5.2

Breakdown voltages of 4H-SiC SBD for Uniformly doped epitaxial layer

Device height=h=W=231µm

S.No	Doping Level , N_d (per cc)	W(µm)	α_p	Ec(V per cm) x 10^6	V_{AvBV}(kV)	V_{PBV}(kV)
1	10^{14}	231	44.05	1.33	14.94	5
2	10^{15}	71.78	139.31	1.66	5.95	5
3	10^{16}	22.7	440.05	1.82	2.06	5
4	10^{17}	7.17	1394.7	2.12	0.7575	5

5.5 CONCLUSION

The analysis of power dissipation, P_D for 4H-SiC Schottky Barrier Diodes given in this Chapter for uniformly doped drift regions and those estimated in Chapter 4 for linearly graded drift regions shows that for a given value of the drift region doping level N_d approximately equal to N_{eff} for linearly graded regions, the latter always yield a lower value of P_D. This decline in power dissipation on a percentage basis becomes significant at higher values of on-state current density levels, J_{on}. However, as the doping level is increased the percentage decline in power dissipation also decreases falling from 74.4% at doping levels of 10^{14} per cc to 7.74% at doping levels of 10^{17} per cc. The corresponding concentration gradients range from 3.88×10^{16} cm^{-4} to 4.32×10^{19} cm^{-4}.

The avalanche breakdown voltages, V_{AvBV} for uniformly doped drift region devices can be made to vary from a maximum of 5kV at a drift region doping level N_d of 10^{14} per cc to a minimum of 757.5V at a value of N_d of 10^{17} per cc. The corresponding device thickness may range from 231µm to 7.17µm respectively. However, linearly graded drift region devices have avalanche breakdown voltage of about 5kV for gradients ranging from 3.88×10^{16} cm^{-4} to 7.96kV at a gradient of 4.4×10^{19} cm^{-4}.The corresponding device thickness may change from 201.07µm to22.7µm. Hence it is possible to design and develop 4H-SiC SBD's which can yield higher breakdown voltages at a lower device thickness by using linearly graded drift regions. Depletion width W' for linearly graded profiles is shown in Table 5.2. Hence thinner device with higher breakdown voltages and lower power dissipation can be developed by using linearly graded profiles in the epitaxially grown drift regions of 4H-SiC Schottky barrier diodes. Finally, if the device height is reduced from the standard 231µm to lower values shown in Table 4.2, the

magnitude of R_{on-sp} and P_D would decline further. The parasitic series resistance and hence R_{on-sp} would be still smaller than what it would be if the device height was kept at 231μm.

CHAPTER 6

Conclusion and scope of future work

Substantial work has been done by various workers on the performance, analysis, device design, power dissipation and breakdown mechanisms of 4H-SiC Schottky barrier diodes (SBD). These have already been discussed in Chapters 1 and 2.The contents of Chapter 3 however, are a deviation from this norm, in that, a simple theoretical technique to generate the (V-I) characteristics of an SBD has been proposed here, primarily by using the technique of iteration and the C++ program.

The basic (V-I) equation of the 4H-SiC SBD giving the forward drop (V_F) given in equation (3.2) has been selected. This equation connects V_F with current density (J_F) and other variables of the device like the barrier height ($\O_B$), the ideality factor η, the specific on-resistance(R_{on-sp}) and Richardson's constant (A^*). The technique proposed here has been used as a direct solution of the diode's current-voltage equation can not be obtained. The characteristics obtained were made to tally with experimental data obtained by other workers for three SBD's , namely ,4H-SiC contacts to Nickel (Ni), Titanium (Ti) and Gold(Au). For the case of Nickel-SiC SBD, a deviation in the theoretically obtained curves was obtained at low voltages but the theoretically obtained curves tallied well with experimental data at higher voltages. Similar deviations in the results for the Titanium contact was seen for voltages upto 1-2 V but the results agreed reasonably well at higher

voltages. However the best tally of the two results was found in the case of gold contact as shown in Fig. 3.10 as marginal deviations were seen to exist over all the ranges of currents and voltages used. A better fit to these curves could be obtained by including modifications such as image force barrier height lowering, tunneling current and minority carrier injection. The ultimate aim of presenting this technique is to facilitate the process of solving such device equations wherein non-linear relations exist between two variables of a device.

The question of obtaining 4H-SiC SBD's with low power dissipation P_D and high breakdown voltages has been the subject of study in this work. The simplified equation of power dissipation given in equation(4.11) and modified by neglecting the contribution due to leakage current as in equation(4.12) has been considered. The dominant parameter that controls the power dissipation as seen from this equation is the specific on-resistance (R_{on-sp}). The magnitude of Ron-sp for various drift region doping levels for uniformly doped drift regions have been obtained and so also the corresponding values of power dissipation at preset values of current density (J_{on}) .The magnitude of power dissipation can be reduced by reducing the magnitude of R_{on-sp} which could be reduced by increasing the value of N_d, the drift region doping level. This was done by having a linearly graded doping profile with a low carrier concentration near the top metal contact increasing to a higher value of carrier concentration near the base metal contact with a concentration gradient of α cm^{-4} over the device height 'h' of 231 μm. The equation to evaluate the effective carrier concentration (N_{eff}) in the case of such a profile has been developed in Chapter 4 and is given in equation (4.8). The power dissipation of such a device has been

calculated at various values of current densities (J_{on}) and the results shown in Table 4.1 have been tallied for devices at a J_{on} of 1000Amps/cm^2 with those obtained for uniformly doped profile presented in Table 5.1. A comparative study of the data presented for a J_{on} of 1000Amps/cm^2 showed that power dissipation for $N_d \approx N_{eff}$ for the two profiles has significantly low values for linearly graded profiles as compared to uniformly doped profiles. The percentage decline in power dissipation of linearly graded profiles decreases with increase in doping levels (N_d or N_{eff}) of uniformly doped or linearly graded drift region devices respectively. Since N_{eff} increases with concentration gradient 'α' as given by equation (4.8), the power dissipation P_D and percentage decline in P_D also decreases with increase in α . This can be seen from Fig. 5.4, which has been evaluated for a current density of 1000Amps/cm^2. The doping level N_d of 10^{14} per cc of uniformly doped drift region devices and N_{eff} of 3.905x10^{14} per cc for linearly graded drift region devices at a gradient of 3.88x10^{16} cm^{-4} has a percentage drop in power dissipation of 74.4%. This value is found to be as low as 7.74% at a gradient of 4.32x 10^{19} cm^{-4} at the same value of J_{on}

Calculation of breakdown voltages shown in Table 5.2 shows that for uniformly doped epitaxial layer devices, doped to a level of 10^{15} per cc the punch through and avalanche breakdown voltages are almost equal to 5kV. Linearly graded epitaxial layer devices show a similar avalanche breakdown at 5.265kV for a gradient of 4.4 x 10^{19} cm^{-4} for which the punch through breakdown voltage is 8kV. This device can therefore have a breakdown voltage of 5.265 kV even if the value of punch through breakdown voltage is 8kV.

An analysis of the results shown in Tables 5.2 and 4.2 shows that the critical fields 'Ec' increases with doping level in the case of uniformly doped epitaxial layer devices but increases with gradient α in the case of linearly graded epitaxial layer devices. However, the magnitude of Ec is somewhat higher in the case of the former than those in the latter. The depletion region width in devices with uniformly doped profiles are normally larger than those in linearly graded ones. This can be seen from the Table 5.2 for uniformly doped epitaxial layers with a doping level of 10^{15} per cc which gives a depletion region width of 71.78μm for a breakdown voltage of 5kV. The results for linearly graded devices show that the depletion region width is only 19.4 μm at a gradient of $4.31 x 10^{19} cm^{-4}$ for the same breakdown voltage. This means that device height for the same breakdown voltage can be substantially reduced using linearly graded profiles than those using uniformly doped profiles, making it possible to design and develop thinner devices.

In conclusion it may be said that 4H-SiC SBDs with linearly graded epitaxial layers have considerably lower power dissipation but need not necessarily provide a higher avalanche breakdown voltage. Lastly the device height 'h' of 231μm used in this work may be difficult to grow in 4H-SiC using epitaxial technology. However wafers with better crystalline perfection may be selected for making these devices.

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LIST OF RESEARCH PAPERS PUBLISHED AND PRESENTED

[P.1] "A method to calculate the voltage-current characteristics of 4H SiC Schottky barrier diode", *Maejo Int. J. Sci. Technol. 3*(02), 287-294, 2009.

[P.2] "Estimation of Power Dissipation of a 4H-SiC Schottky barrier diode with a linearly graded doping profile in the drift region", *Maejo Int. J. Sci. Technol. 3*(03), 352-365,2009.

[P.3] "Comparison of Power Dissipation in Ni/4H SiC Schottky Barrier Diode with Uniform and Linear graded Doping Profiles", Journal of Electronic Devices, Vol.6, pp194-196, 2008

[P.4] "Calculation and plot of V-Jf Characteristics for 4H-SiC (An Upcoming Material) for Schottky Barrier Diode with different contact Metals", International Conference on "Innovative

dynamic studies of Materials at the Nanoscale" , held at Gyeong-Ju, Korea, from 29th June-3rd july,2008

[P.5] "Calculation of power dissipation in SiC-based Schottky barrier diode having uniform doping", International Conference on "Ultra-High Temperature Ceramics: Materials for extreme environment Applications", held at Lake Tahoe, California, from 3-8August, 2008

[P.6] **"**An approach to Calculate and plot V-I Characteristics for 4H-SiC Schottky barrier diode (a Power Device) for different contact metals using iteration method and C++ programming", International Conference on "Semiconductor Technology for Ultra Large Scale Integrated Circuits and Thin Film Transistors", held at Il Ciocco Hotel and Conference Center, Barga, Italy , from 29 July – 3 August 2007

[P.7] **"**Silicon carbide (upcoming material) for semiconductor devices", National Conference on "Technologies of 21st Century", held at Punjab University, India on 8-9th April 2006