"LOW-VOLTAGE TRANSCONDUCTOR AND ITS APPLICATIONS"

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CERTIFICATE

I hereby certify that the work which is being presented in the thesis entitled: **"LOW-VOLTAGE TRANSCONDUCTOR AND ITS APPLICATIONS"** in partial fulfilment of the requirements for the award of the Degree of Master of Technology in VLSI AND CAD Engineering (Department of Electronics and Communication Engineering) is an authentic record of my own carried out under the supervision of Mr. Rishikesh Pandey, Assistant Professor, ECED.

The matter embodied in this thesis has not been submitted in any other University/Institute for the award of any degree.

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ABSTRACT

In this thesis, a CMOS linear floating resistor circuit is presented which is based on a transconductor circuit. The circuit topology is capable of implementing both positive and negative resistance. The introduced floating resistor has simple circuit implementation and its resistance is tunable by adjusting the gate voltage of a MOS transistor. The floating resistor has been simulated using Cadence Spectre analog simulation environment with BSIM3v3 version 3.2 model parameters. The simulation results show that the floating resistor presents a constant resistance of 0.87MΩ to 1.86MΩ when the adjust voltage ranges from -380mV to -200mV and the corresponding adjusted current is 1μA to 5μA, with ±0.9V voltage supplies. The cutoff frequency is about 1MHz.

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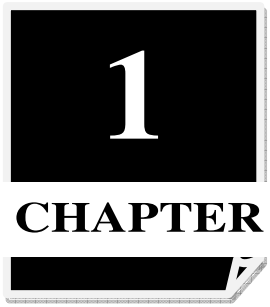
μ	Charge carrier mobility
C_{gs}	Gate-source capacitance
C_{gd}	Gate-drain capacitance
C_{ox}	Normalized oxide capacitance
F	Frequency
g_m	Transconductance
Id	Drain current
K	Boltzmann constant
K_p	PMOS process transconductance parameter
K_n	NMOS process transconductance parameter
L	Channel length
W	Channel width
V_{cm}	Common-mode input voltage
V_{dd}	Positive supply
V_{ss}	Ground supply
V_{ds}	Drain-source voltage
V_{sat}	Saturation voltage
V_{gs}	Gate-source voltage
V_{th}	Threshold voltage
V_{th0}	Threshold voltage at V_{sub}= 0V
V_o	Output Voltage

V_{in}	Input Voltage
V_{adj}	Adjusted Voltage
I_o	Output Current
I_{in}	Input Current
I_{adj}	Adjusted Current
Z_o	Output Impedance
Z_{in}	Input Impedance
R_L	Source Resistance
FF	Fast-Fast
FnSp	Fast-n-Slow-p
SnFp	Slow-n-Fast-P
LVS	Layout Vs schematic



INTRODUCTION

1.1 BACKGROUND

In recent years, digital signal processing has progressively supplanted analog signal processing in chip design. This is due to it having lower development costs, better precision performance and dynamic range, as well as being easier to test. The role of analog circuits has been mostly restricted to electronic applications of interfacing digital systems to the external world. Nevertheless, when precise computation of numbers is not required(as is the case in systems designed for perception of a continuously changing environment), and massively parallel collective processing of signals is needed, low precision analog VLSI (very large scale integration) has proven to be more convenient than digital in terms of cost, size and/or power consumption [1]. In recent years mixed signal application-specific integrated circuits (ASICs) have become increasingly popular. The cooperative coexistence of analog and digital circuits is very beneficial since they compensate for each other's weaknesses. Hence, although in many aspects digital electronics is superior; in reality it requires a symbiotic relationship with analog.

Since the invention of the transistor more than 50 years ago, the progress of micro-electronics can be summarized as follows: 15 per cent decrease in feature size per year, 30 per cent cost decrease per year, 50 per cent performance improvement and 15 per cent semiconductor market growth rate. The numbers speak for themselves. This exponential evolution made many experts in the 1990s assert that fundamental limits were about to be reached. Fortunately, technical innovations made it possible to shrink the technologies to

smaller dimensions than the predicted 0.18µm. However, as the dimensions of the devices reduce, a new constraint arises: the interconnect delays and the fact that they directly affect the CV^2 power dissipation. In the past, this was not a problem as the capacitances were scaled down together with the dimensions. Recently this scaling relationship has been replaced to being proportional to the total length of wires, L, in the circuit. The interconnect power dissipation can therefore be rewritten as kV^2L (where k is the dielectric permittivity). Hence, the most significant parameter in the reduction of the interconnect power is the voltage and new strategies are required to operate circuits at lower power supply voltages [2]. However, this is not the only motivation fuelling the eagerness of researchers to operate circuits at lower voltages. The other one is related to the magnitude of the electric fields in the devices. These grow proportionally as the dimensions are scaled down, which increases the risk of dielectric breakdown. This can additionally be compensated for by reducing the voltage differences across the devices. Hence a low voltage power supply is beneficial.

The fast development of electronic-based entertainment, computing and communication tools, especially portable ones, has provided a strong technology drive for microelectronics during the last ten years. System portability usually requires battery supply and therefore weight/energy storage considerations. Unfortunately, battery technologies do not evolve as fast as the applications demand. Therefore the challenge, derived from market requirements, is to reduce the power consumption of the circuits. In addition to consumer products, battery lifetime is a crucial factor in some biomedical products which have to be either worn or implanted within the patients for a long period of time; such systems are continuously increasing in number and in scope. Investigation into low power biomedical systems is another interesting quest for microelectronic designers [3-6].

The choice of fully integrated VLSI complementary metal oxide semiconductor (CMOS) implementations is based on their lower cost and design portability. Furthermore, CMOS technologies allow the possibility of integration with micro electro mechanical systems (MEMS). These are the most important reasons that have directed the semiconductor industry towards CMOS mixed signal designs, and place CMOS technologies as the leader in the microelectronics semiconductor industry [7]. Adapting of existing techniques and

presented of some original design methods specific to latest micron technologies represents the key elements of the presented research methodology

1.2 MOTIVATION

The various active resistor circuits have been presented for replacing inaccurate passive resistors [8]-[13]. G. moon et. al. [8] have introduced linear floating resistor that was composed of two enhancement-type PMOS transistors has been presented. C. A. Papazoglou et. al. [9] and H. Zouaoui-Abouda et. al. [10] have been introduced floating resistors that are based on current conveyors and their resistances depended on the thermal voltage. S. A. Mahmoud [11] has summarized two commonly used circuit configurations for realizing floating resistors, and has been presented a floating resistor tunable by two voltage supplies, which provided currents to the sources of input transistors. M. Kushima et. al. [12] have described a floating resistor circuit which are based on the linear relationship of Ids vs. V_{ds} of a MOS device working in the linear region, and some other MOS transistors, working in the saturation region, served as voltage shifters to compensate the variation in the gate voltage of the device that works in the linear region.

1.3 TRANSCONDUCTOR

The electrical symbol with gm on it represents an ideal operational transconductance amplifier (OTA) modified to have two outputs. A common transconductance circuit has two terminals V_+ and V_- for taking input voltages and an output terminal Io for sinking current. As an ideal transconductance, no currents are allowed to flow through the input ports, and the output voltage can be any value, dependent on its loading circuit by $V_{out} = R_{oland} \times I_0$. The output current and the input voltages have the relation that is described as:

$$I_0 = g_m(V_+ - V_-) \tag{1.1}$$

Where g_m is the transconductance. The transconductance block shown in Fig.1.1 has two output currents. The one with positive sign is the same as the Io in equation (1.1), and the one with negative sign is identical in magnitude but opposite in direction.

Operational transconductance amplifiers (OTAs) are important building blocks for various analog circuits and systems. Depending on system needs, an OTA must satisfy many design requirements. As CMOS technologies evolves well into the ultra-deep-sub micrometer regime, the supply voltage decreases and device characteristics deteriorate. These conditions pose severe challenges in amplifier designs. For example, the transistor intrinsic gain more in deep-sub micrometer processes is typically low due to inferior device output impedance. Cascoding transistors can raise the circuit impedance and thereby boost the gain.

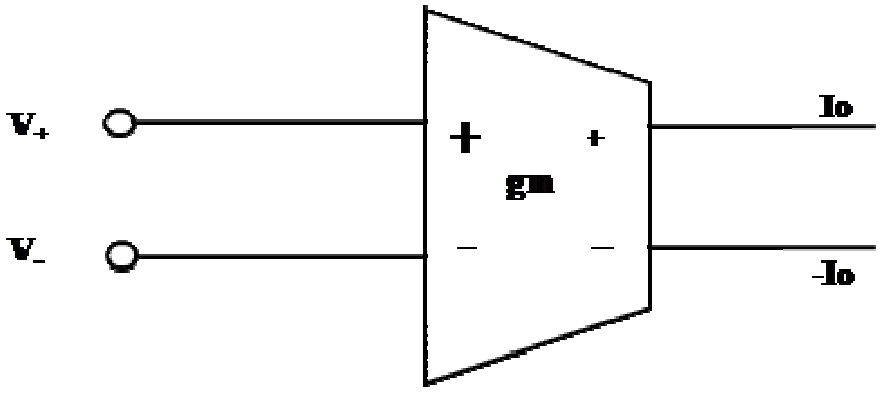


Fig.1.1: Block Diagram of Transconductance

However, this is at the cost of reduced output swing, and such circuit becomes infeasible if the supply voltage is further decreased. Alternatively, a cascade multistage amplifier is often used in low-voltage operation. Although a multistage OTA is seemingly suitable for low-voltage operation, it incurs higher power consumption. This is attributed to increased numbers of amplifying stages.

1.4 THESIS ORGANIZATION

Chapter 2 describes the literature survey of the different circuits of the resistors. Chapter 3 describes the design of a CMOS linear floating resistors. In this chapter the presented floating resistor circuit is based on transconductor element and the value of its resistance is controlled by the gate voltage of the MOS transistor and can be selected to be positive or negative by changing feedback connections. Chapter 4 describes various simulation results and layouts of the circuits discussed in chapter 3 with Cadence Design Environment. All the simulations have been performed using BSIM3v3 model parameter in 0.18µm CMOS process technology. Chapter 5 summarizes and draws conclusion from this work.

1.5 CONTRIBUTIONS

My work in this thesis is summarized as follows:

1. Investigate the different circuits of resistors using MOSFETs.
2. Design and simulate a transconductor.
3. Design and simulate positive and negative floating resistors.
4. Simulate and generate the Layout and Post-Layout of transconductor and positive and negative floating resistors.

2 CHAPTER

LITERATURE SURVEY

To design the precision integrated circuits (ICs), it is not suitable to use the passive resistors [14]. It is possible to achieve floating resistors in silicon technology by using poly silicon or diffusion is as in a monolithic integrated circuit. However, these resistors occupy large silicon chip areas and it is difficult to achieve precise values. Moreover, the resistance values cannot be tuned [15]. The resistance simulator can be implemented both floating and grounded resistors but the floating resistor is more convenient to use than the grounded resistor one. The positive resistance simulator is required in the instrumentation systems, programmable amplifiers, filters, oscillators and etc. While the negative resistance simulator is very useful in various applications such as impedance matching, instrumentation system, cancelling resistance circuit, improving the quality factor in resonant circuit [16]. In general, the resistance simulator is realized as the passive resistor in order to achieve low power consumption, easy to fabrication and can be electronically controlled so it is very suitable to use in the automatic control system. The resistance simulators in CMOS technologies have been presented. Their supply voltage share quite low and they are only able to operate at high frequency. Floating resistors in silicon technology can be found in applications such as continuous-time filters, amplifiers, and artificial neural networks (ANN), etc.

Several researchers have described floating resistors [9]-[14], [17]-[19]. C. A. Papazoglou et. al. [9] have described the electronically tunable floating resistor. The resistance value is independent of the MOS threshold voltage $V_{T,}$ the mobility μ_0 and the gate oxide capacitance (C_{OX}). Its resistance value is approximately 50kΩ to 100kΩ for an input voltage range ±1V using ±5V power supply. The power consumption for zero input voltage is very low.

H. Zouaoui-Abouda et. al. [10] have described floating controlled resistor based on second-generation current controlled-conveyors. This floating controlled resistor allows the value of the resistancs in the order of several tens of kilo-ohms and frequency response in the order of 100MHz.

S. A. Mahmoud [11] has described two commonly used circuit configurations for realizing floating resistors and presented a floating resistor tunable by two voltage supplies, which provided currents to the sources of input transistors.

M. Kushima et. al. [12] have described a floating node voltage controlled linear variable resistor circuit with low power consumption of 132.5 μW. This presented resistor circuit has high linearity and a wide controlling voltage that does not depend on the supply voltage. The value of resistance is varied from 58kΩ to 1600kΩ.

Sakurai et. al. [13] have described square -law programmable floating resistor based on the method using the saturation region of an enhancement-type MOSFET. While such a resistor is mainly intended for single-ended and first quadrant mode of conduction, where it achieves a nonlinearity of .03% full scale in the 0-10 V voltage range, it can also be used as a floating element and operated in the first as well as third quadrant mode of conduction (i.e. with V and I both either positive or negative) with some degradation in linearity and voltage range

M. Banu et. al. [14] have presented a method implementing floating voltage-controlled resistors in CMOS technology using the triode region of an enhancement-type MOSFET. The method takes advantage of the cancellation of the first-order nonlinearities of two MOS transistors in physical proximity.

J. Babanezhad et. al. [17] have presented a method using the triode region of a depletion-type MOSFET.

H. O. Elwan et. al. [18] have presented a CMOS floating linear resistor circuit with a wide linearity range. The circuit uses 14 transistors all operating in the saturation region.

Li Wang et. al. [19] has introduced have described CMOS floating resistor based on a transconductor. The circuit topology is capable of implementing both positive and negative

resistance and its resistance is tunable by adjusting the gate voltage of a MOS transistor and can be selected to be positive or negative by changing feedback connections.

2.1 CIRCUITS DESCRIPTION

2.1.1 ELECTRONICALLY TUNABLE FLOATING RESISTOR [9]

A block diagram presenting the parts of the tunable resistor circuit is shown in Fig.2.1. In this configuration, there is a linearization circuit which provides a linear relationship between the voltage and current of terminals A, B corresponding to a tunable resistance R.

The squaring circuit along with the V_T voltage shifter and the MOSFET, set resistance value R independent of transistor parameters. Details of these circuits are given below.

2.1.1.1 LINEARIZATION CIRCUIT

The MOS based circuit presented in Fig.2.2 simulates a resistor which is electronically tunable but not yet dependent process parameter. It is supposed that all NMOS transistor have same V_T. Nothing that the source voltage of the transistor M_2 is $V_{S2} = V_A$. The saturation current equation for the M_2 transistor is

$$I_b = K_2(V_1 - V_A - V_T)^2 \tag{2.1}$$

Where

$$K_2 = 0.5\mu_0 c_{0x} \frac{W_2}{L_2}$$

$$V_1 = V_A + \sqrt{\frac{I_b}{K_2}} + V_T \tag{2.2}$$

similarly from M_3 assuming that $K_2 = K_3$

$$V_2 = V_A - \sqrt{\frac{I_b}{K_2}} - V_T \tag{2.3}$$

Where V_2 due to the voltage follower consisted of transistors M_4 - M_{10} is transferred to the sources of M_{22}. Suppose M_{12} operates in saturation region as M_{11}, the current I_1 and I_2

flowing through the transistor M_{12} and M_{11} respectively are given by the following relation below:

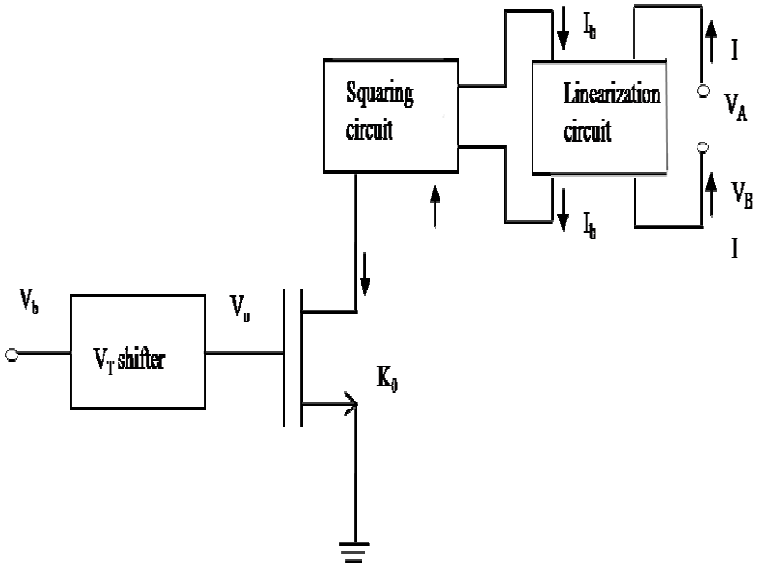


Fig 2.1: Block Diagram of the Complete Resistor Circuit

$$I_1 = K_{12}(V_1 - V_B - V_T)^2 = K_{12}(V_A + \sqrt{\frac{I_b}{K_2}} - V_B)^2 \tag{2.4}$$

$$I_2 = K_{11}(V_B - V_2 - V_T)^2 = K_{12}(V_B + \sqrt{\frac{I_b}{K_2}} - V_A)^2 \tag{2.5}$$

Assuming that $K_{11} = K_{12}$, from equations above it follows that current I from the terminal A to terminal B is given by the relation

$$I = I_1 - I_2 = 4K_{12}\sqrt{\frac{I_b}{K_2}}(V_A - V_B) \tag{2.6}$$

Thus the equivalent resistance has the value

$$R = \frac{V_A - V_B}{I} = \frac{1}{4K_{12}}\sqrt{\frac{K_2}{I_b}} \tag{2.7}$$

This can be tuned by the external current source I_b. The condition for conduction of transistor M_1 and M_2 after some simple calculation are proved to be

$$|V_A - V_B| < \sqrt{\frac{I_b}{K_2}} = \frac{1}{4RK_{12}} \tag{2.8}$$

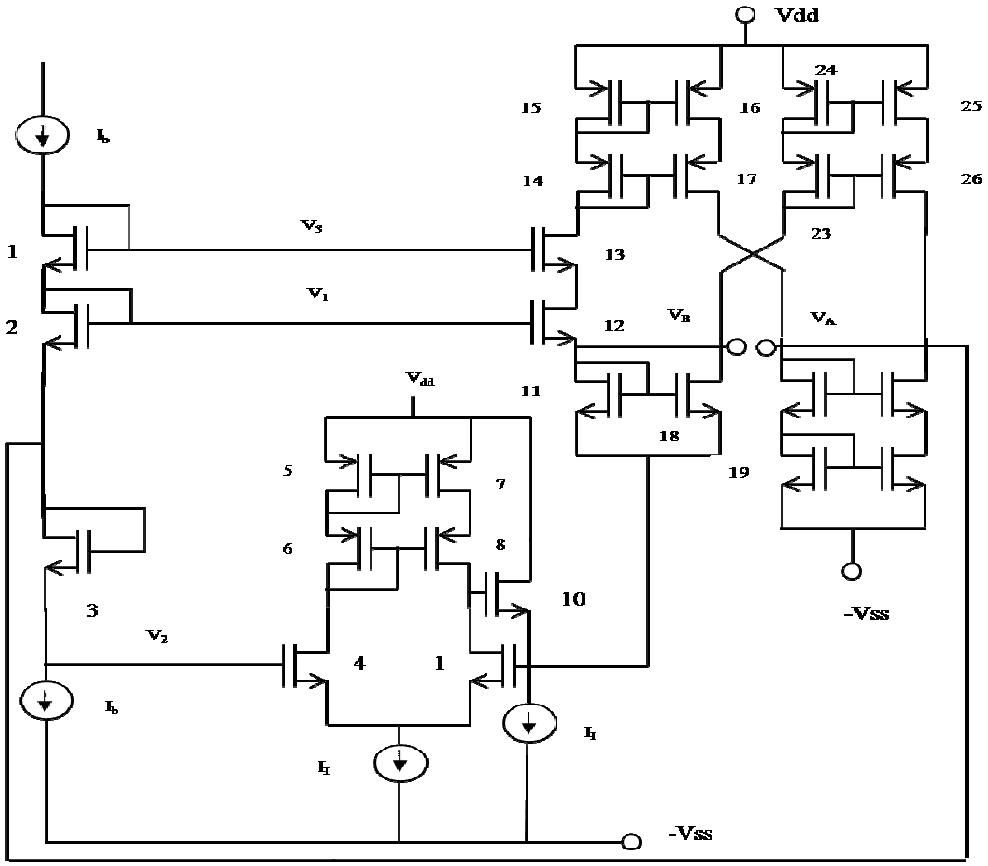


Fig 2.2: Linearization Circuit

This equation defines differential input for the proper operation. Obviously the high values of the equivalent resistance R restrict the operating voltage range.

2.1.1.2 V_T VOLTAGE SHIFTER

Fig.2.3 gives an output voltage V_0 equal to V_b+ V_T and hence provides a current proportional to the square of the input voltage [20].

That is

$$I_{b2} = K_0 V_b^2 \tag{2.9}$$

2.1.1.3 SQUARING CIRCUIT

The squaring circuit [21] which has employed is shown in Fig. 2.4. Two external biases current I_{b1} and I_{b2} act to this circuit. The output current I_b of the squaring circuit [21] is given by the following equation:

$$I_b = I_{b1}^2(8I_{b2})^{-1} \tag{2.10}$$

And for proper operation it must be

$$|I_{b1}| < 4I_{b2} \tag{2.11}$$

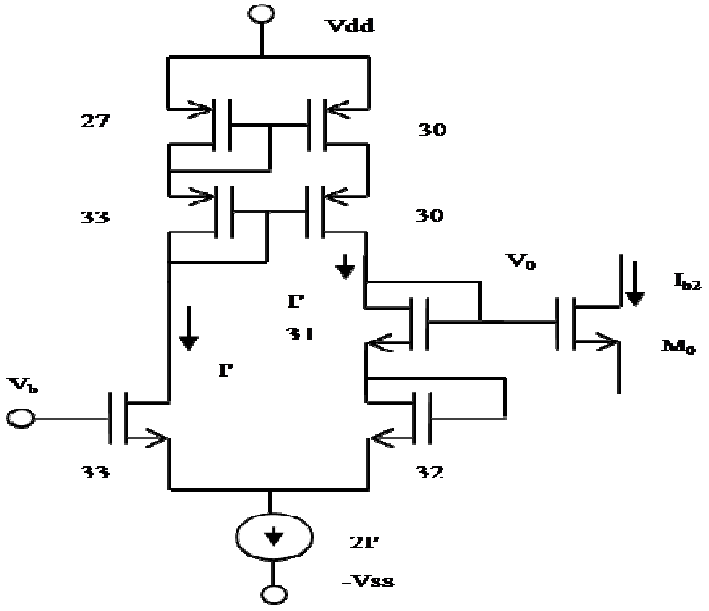


Fig 2.3: V_T Voltage Shifter

2.1.1.4 COMPLETE RESISTOR CIRCUIT

Employing equation (2.7), (2.9) and (2.10) the value of the equivalent resistance is proved to be given by the relation

$$R = \frac{\sqrt{2}}{2}\sqrt{\frac{K_2K_0}{K_{12}^2}}\frac{V_b}{I_{b1}} \tag{2.12}$$

For the proper operation it must be

$$|I_{b1}| < 4K_0V_b^2 \tag{2.13}$$

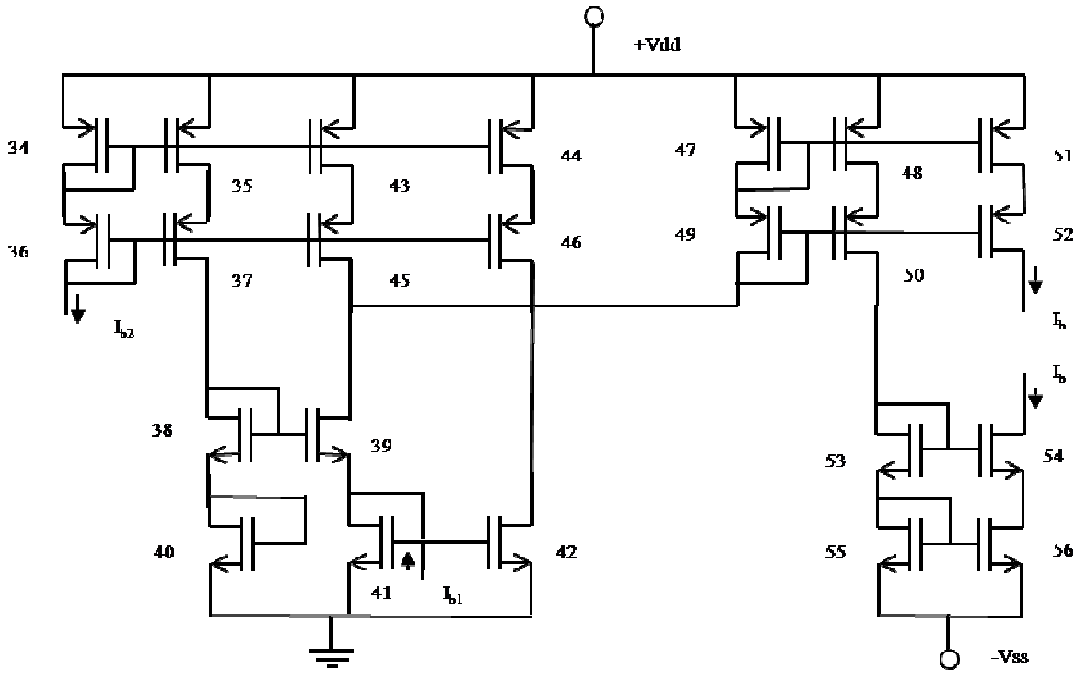


Fig 2.4: Squaring Circuit

The resistance value being depend upon on the ratio $\frac{K_2K_0}{K_{12}^2}$ is independent of the C_{0X} and μ_0 and depends on the ratio of $\frac{W_2W_0}{W_{12}^2}$ and $\frac{L_{12}^2}{(L_2L_0)}$. This can be accurately specified in an integrated circuit. The value of resistance can be tuned either by the bias voltage V_b or by the current I_{b1}.

2.1.2 TEMPERATURE EFFECT

Carrier mobility and MOSFET K-constant depends on the temperature according to the following equation:

$$\mu_0(T) = \mu_0(T1)\left(\frac{T}{T1}\right)^{-\frac{3}{2}} \tag{2.14}$$

$$K(T) = K(T1)(T/T1)^{-\frac{3}{2}} \tag{2.15}$$

Where μ_0 and K values are function of MOS K-constants [8], [13], [18], [20] and [22] suffers from a strong dependence on temperature. This is evident for the resistance implemented by the linearization scheme alone, because as soon as K_{12}, K_2 are given by equation similar to (2.14), from (2.7) one has

$$R(T) = R(T1)(T/T1)^{\frac{3}{4}} \tag{2.16}$$

However, the resistance given by Eq. (2.12) is a function of the ratio $\frac{K_2K_0}{K_{12}^2}$ with K_2, K_0, K_{12} obeying to Eq. (2.14).

2.1.3 SECOND ORDER EFFECT

There are several second-order effects causing deviations from the ideal square-law behavior of (2.1). The effect of mobility reduction and channel length modulation of the circuits will be considered. It will be shown that these effects cause the harmonic distortion of the current flowing through the circuit [13]. Body effect is negligible because substrate of the transistor has been connected to the respective source. Second order effect play more accurate numerical result for the circuit performance, while current mirror and voltage follower are supposed to be ideal for simplicity sake [13]. Second order effects will be studied for the linearization circuit. Voltage shifter V_T and the squaring circuit serve to provide an appropriate current for biasing linearization circuit, second order effects on these two circuits alter only the resistance value and cause no harmonic distortion of the resistor current.

2.1.3.1 MOBILITY REDUCTION

Mobility reduction in an MOS transistor may be modelled by

$$\frac{\mu_s}{\mu_0} = \left(\frac{U_{CRT}\varepsilon_{si}}{C_{OX}(V_{GS}-V_T)}\right)^{U_{EXP}} \tag{2.17}$$

Where μ_s is the reduced carrier's mobility, μ_0 is the zero field mobility, U_{CRIT} is the critical field for mobility reduction and U_{EXP} is the critical field component. Mobility reduction exits when

$$\frac{U_{CRIT}\varepsilon_{si}}{C_{OX}} < V_{GS} - V_T \tag{2.18}$$

A resistor is to be implemented to be tunable in the range 50kΩ – 100kΩ with an input signal range (-1, 1) V employing transistors with sizes as in Table 2.1. The effect of mobility degradation can be neglected for the transistor M_2 and M_3

Table 2.1: Sizes of the Transistor Resistor Simulator

MOSFET	W/L(μm)	MOSFET	W/L(μm)
M_0	20/20	M_4,M_9	10/10
M_5-M_8, M_{14}-M_{21}	200/5	M_{13}	192/3
M_{23}-M_{30},M_{34}-M_{37}	200/5	M_{11}-M_{12}, M_{22}	8/100
M_{42}-M_{56}	200/5	M_{31}-M_{32}	10/100
M_1,-M_{10}	50/5	M_{33}	5/200
M_2,M_3	5/100	M_{38}-M_{42}	200/30

2.1.3.2 CHANNEL LENGTH MODULATION

Channel length modulation causes the drain current to be dependent on the drain voltage. This will cause mainly second and third order distortion components. The distortion due to channel length modulation can be reduced by increasing the channel length of the devices. To determine the channel length modulation as below relation:

$$L' \cong L\left(1 - \frac{X_D}{L\sqrt{N_{EFF}}}\sqrt{V_{DG} + V_T}\right) \tag{2.19}$$

Where $X_D = \sqrt{\frac{2\varepsilon_{si}}{qN_{SUB}}} = \frac{0.22\mu m}{\sqrt{V}}$ and L, L′ is the nominal and the effective channel length respectively. It is evident that the effect is limited for the high value of L and further it can be reduced by providing $V_{DG} \cong 0$ MOSFETS.

For the linearization circuit, high values are given to the ratios W/L of transistors M_1 and M_{13}in order to reduce the channel length modulation for M_{12} as it explained straightway. It can be shown that

$$V_{DG12} = \left(\sqrt{\frac{K_2}{K_1}} - \sqrt{\frac{K_{12}}{K_{13}}}\right)\frac{1}{4RK_{12}} - \sqrt{\frac{K_{12}}{K_{13}}}\,(V_A - V_B)$$

From above equation if we choose K_1 and K_{13} such that $\sqrt{\frac{K_2}{K_1}} > \sqrt{\frac{K_{12}}{K_{13}}}$, then

$$V_{DG12_{\min\,(max)}} = \left(\sqrt{\frac{K_2}{K_1}} - \sqrt{\frac{K_{12}}{K_{13}}}\right)\frac{1}{4R_{max(min)}K_{12}} \mp \sqrt{\frac{K_{12}}{K_{13}}}\,|V_A - V_B|_{max} \qquad (2.20)$$

It is desirable to have $V_{DG_{min}} \cong 0$ for transistor M_{12} to work always saturation region and $V_{DG12_{max}}$ as low as possible in order to reduce channel length modulation. Eq. (2.20) is solved for the ratio $\frac{K_{13}}{K_1}$ for $V_{DG12_{min}} = 0$ and is found that

$$K_{13}/K_1 = (4R_{max}K_{12}|V_A - V_B|_{max} + 1)^2\left(K_{12}/K_2\right) \qquad (2.21)$$

Now, to obtain a low value for $V_{DG12_{max}}$, from Eq.(2.20), given the values of K_2 and K_{12} which define the resistance value along with the input range, we choose high value of K_1 which in in turn results to a high value for K_{13}, according to Eq. (2.21).

2.1.4 SIMULATION RESULTS

The circuit of Fig. 2.1 has been simulated using PSPICE. The dimensions of the MOSFETs are shown in Tables 2.1, while I= 0.5μA, I_f = 100μA. For V_b = 0.5V and I_{b1} in the range 10μA-20 μA, with ±5V power supply, the circuit has been simulated for resistance variation in the range 50KΩ-100KΩ with input range for linear operation (-1, 1) V.

The simulated variation of the resistance with respect to the bias current is shown in Fig.2.5 along with the theoretical. The closeness between PSPICE simulation and theoretical results (maximum deviation = 2%), points out that accurate values of the resistance can be implemented by the presented circuit.

The circuits of Fig.2.2 and Fig. 2.1 have been tested for the same nominal resistance value at 27 ^{0}C for the temperature range 0 ^{0}C - 100 ^{0}C. PSPICE simulation shows that the dependence of the resistance value on temperature is strong (2250ppm) for the uncompensated circuit of Fig.2.2 while the variation is much lower for the compensated circuit of Fig 2.1 (370ppm).

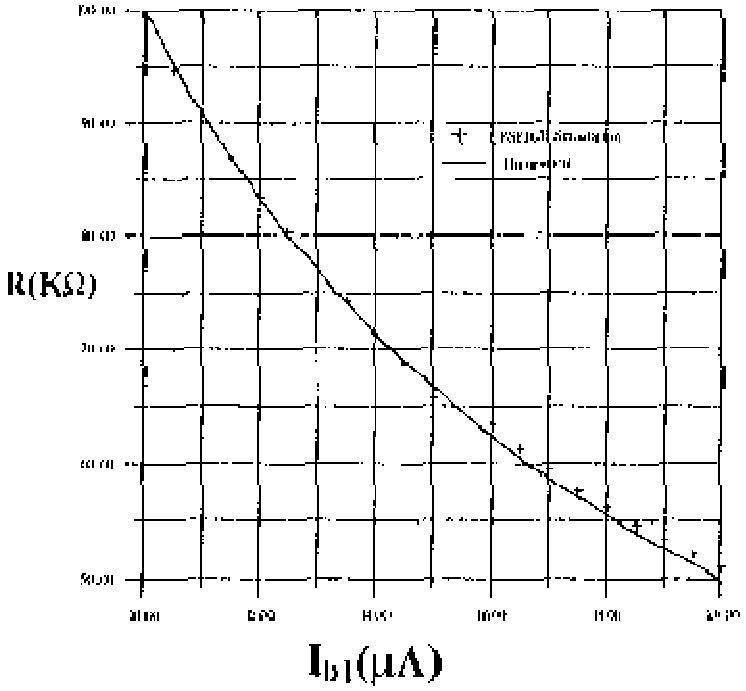


Fig.2.5: Resistance Value Vs Bias Current

However, to ensure the frequency response of the presented resistor simulator, a voltage divider has been formed, consider of the tunable resistor (tuned at the value of 100KΩ) and a grounded fixed resistor of the same value. The PSPICE AC analysis of the divider shows a cut-off frequency at about 7MHz. Finally, the power consumption of the circuit for V_{AB}=0 has been found by PSPICE simulation to be approximately 4.5mW and 5.2mW for I_{b1}=10μA and 20μA respectively.

2.2 FLOATING NODE VOLTAGE CONTROLLED LINEAR VARIABLE RESISTOR CIRCUIT [12]

2.2.1 OPERATION MOSFET AS A CONTROLLED LINEAR RESISTOR

The drain current of an enhancement mode MOSFET can be expressed as:

- in the saturation region

$$I_{DS} = \frac{K}{2}(V_G - V_S - V_T)^2 \tag{2.22}$$

- in the linear region

$$I_{DS} = K\left(V_G - V_S - V_T - \frac{V_{DS}}{2}\right)V_{DS} \tag{2.23}$$

A MOSFET operating in the linear region is useful for low-power supply voltage operation. MOSFET as a controlled linear resistor and all voltages are referred to a common point. Suppose we can keep the gate voltage constant such that

$$V_G = V_{BIAS} + \frac{V_D + V_S}{2} \tag{2.24}$$

where V_{BIAS}, some constant voltage and second term is is the common mode input voltage.

Substituting (2.24) into (2.23) then yields an expression for the drain-source resistance as

$$R_{DS} = \frac{V_{DS}}{I_{DS}} \tag{2.25}$$

$$= \frac{1}{K(V_{BIAS} - V_T)} \tag{2.26}$$

We see that, as for as the condition of Eq. (2.24) is satisfied, we obtain a constant resistance between the drain and the source independently of the applied differential voltage $V_{DS.}$

Fig.2.6 (a) shows a floating node voltage-controlled linear variable resistor circuit which satisfied the condition of Eq. (2.24). The circuit consist 6 n-channel MOSFETs and 3 p-channel MOSFETs. Fig.2.6 (b) shows the symbol for a floating node voltage-controlled linear variable resistor. The transconductance parameters and threshold voltages of the n-channel MOSFET M_{ni} (i = 6) are defined as K_{ni} and V_{tni}, respectively. The transconductance parameters and threshold voltages of the p-channel MOSFET M_{pi} (i=2) are defined as K_{pi} and V_{Tpi} respectively. We assume that $K_{n1}=K_{n2}=K_{n3}=K_{n4}=K_{n5}=K_{n6}=K_{na}$ and $K_{pl}=K_{p2}=K_{pa}$, respectively.

Since the drain-to-source current of the M_{n1} is equal to that of M_{n2}, we can get:

$$\frac{K_{na}}{2}(V_s - V_a - V_{Tn1})^2 = \frac{K_{na}}{2}(V_a - V_{Tn2})^2 \quad (2.27)$$

Since $V_{Tn1} = V_{Tn2,}$ we, can obtain as:

$$V_a = \frac{1}{2} V_s \quad (2.28)$$

Since the drain-to-source current of the M_{n5} is equal to that of M_{n6}, we can get:

$$\frac{K_{na}}{2}(V_D - V_b - V_{tn5})^2 = \frac{K_{na}}{2}(V_b - V_{tn6})^2 \quad (2.29)$$

Since $V_{Tn5} = V_{Tn6,}$ we, can obtain as:

$$V_b = \frac{1}{2} V_D \quad (2.30)$$

Since the drain-to-source Current of the M_{P1} is equal to that of M_{p2} we can get:

$$\frac{K_{pa}}{2}\left(V_C - V_{DD} - V_{tp1}\right)^2 = \frac{K_{na}}{2}\left(V_a - V_G - V_{tp2}\right)^2 \quad (2.31)$$

Since $V_{Tpl} = V_{Tp2}$, we can obtain as:

$$V_G = V_s - V_c + V_{DD} \quad (2.32)$$

Since the drain-to-source current of the M_{n3} is equal to that of M_{n4}, we can get:

$$\frac{K_{na}}{2}(V_{DD} - V_{Bias} - V_C - V_{tn3})^2 = \frac{K_{na}}{2}(V_b - V_{tn4})^2 \quad (2.33)$$

Since $V_{Tn3} = V_{Tn4}$, we can obtain as:

$$V_C = V_{DD} - V_{BAIS} + V_b \quad (2.34)$$

From Eq. (2.28), Eq. (2.30), Eq. (2.20), and Eq. (2.24), the terminal voltage V_G is given by

$$V_G = V_{Bias} + \frac{V_D + V_S}{2} \quad (2.35)$$

From Eq. (2.35), the output current I_{out} is given by

$$I_{out} = I_{in} \tag{2.36}$$

$$= K_p \left(V_G - V_S - V_{Tp} - \frac{V_R}{2}\right) V_R \tag{2.37}$$

$$= K_p\,(V_{BIAS} - V_{Tp})\,V_R \tag{2.38}$$

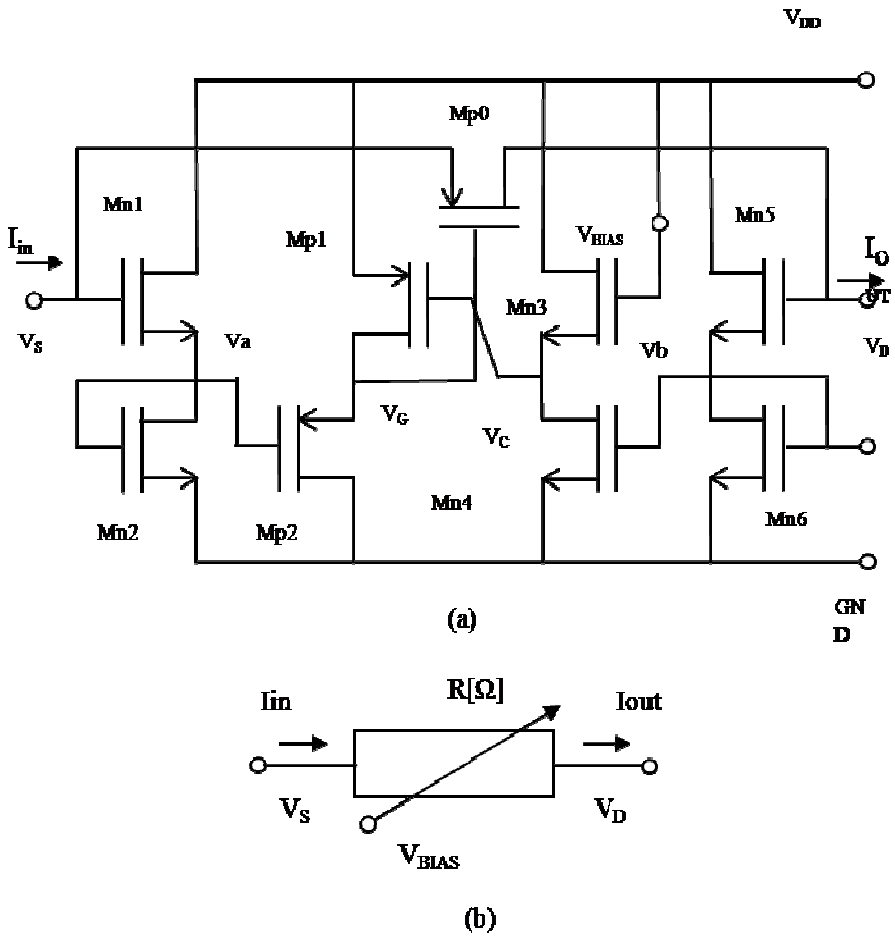


Fig 2.6: (a) Floating Node Voltage-Controlled Resistor

(b) Symbol of Floating Node Resistor

Where K_p is the transconductance parameters of M_{po}, V_{Tp} is the threshold voltage of M_{po}, V_{BIAS} is the bias voltage to the presented circuit, and $V_R = V_D - V_S$ from Eq. (2.38), the presented circuit operates as the floating node variable resistor. The resistance value R of the circuit can be given by

$$R = \frac{V_R}{I_{out}} \tag{2.39}$$

$$= \frac{1}{K_p(V_{BIAS} - V_T)} \tag{2.40}$$

From Eq. (2.40), R can be varied by $V_{BIAS.}$

2.2.2 SIMULATION RESULTS

Fig.2.7 shows the relationship between I_{out} and $V_R = V_D - V_S$ under the condition that V_{BIAS} are varied from 0V to 2.0 V in the step 0.2V and also it is understood that the presented circuits, as a floating node variable resistor circuit, operate as a linear variable circuit.

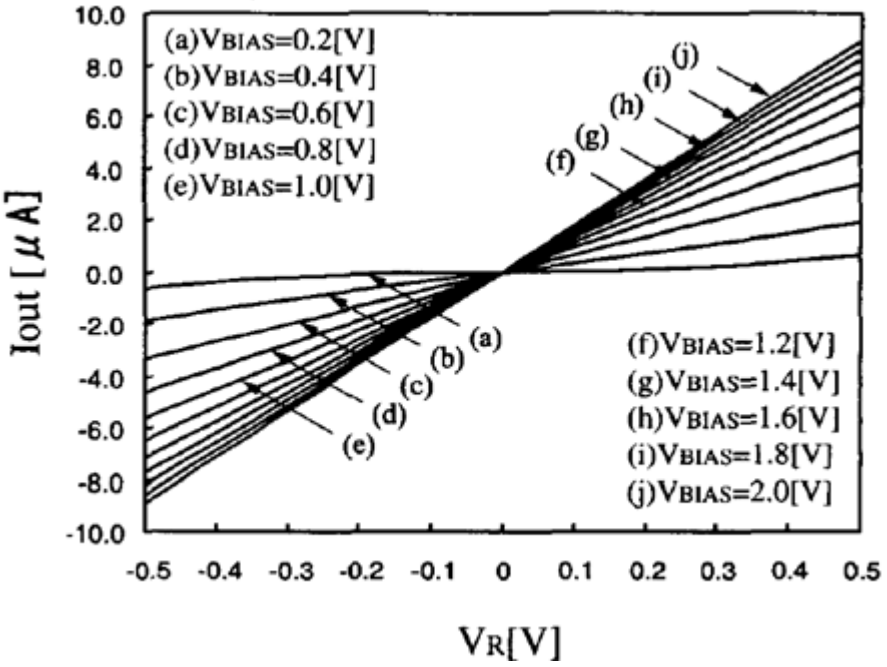


Fig.2.7: DC Transfer Characteristics Relation between I_{out} and Terminal Voltage

Fig.2.8 shows the relationship between V_{BIAS} and R. The resistance values of 58 kΩ to 1600 kΩ can be obtained with 0 V ≤ V_{BIAS} ≤ 1.5V.

Fig.2.9 shows an application as an RC filter by using controlling voltage (V_{BIAS}) = 2 volts. The simulation result of the frequency response of the RC filter by using the presented variable resistor circuit is shown in Fig.2.10 and Fig.2.11. Fig.2.10 shows the relationship

between gain and frequency and Fig.2.11 shows the relationship between the phase (degree) and frequency.

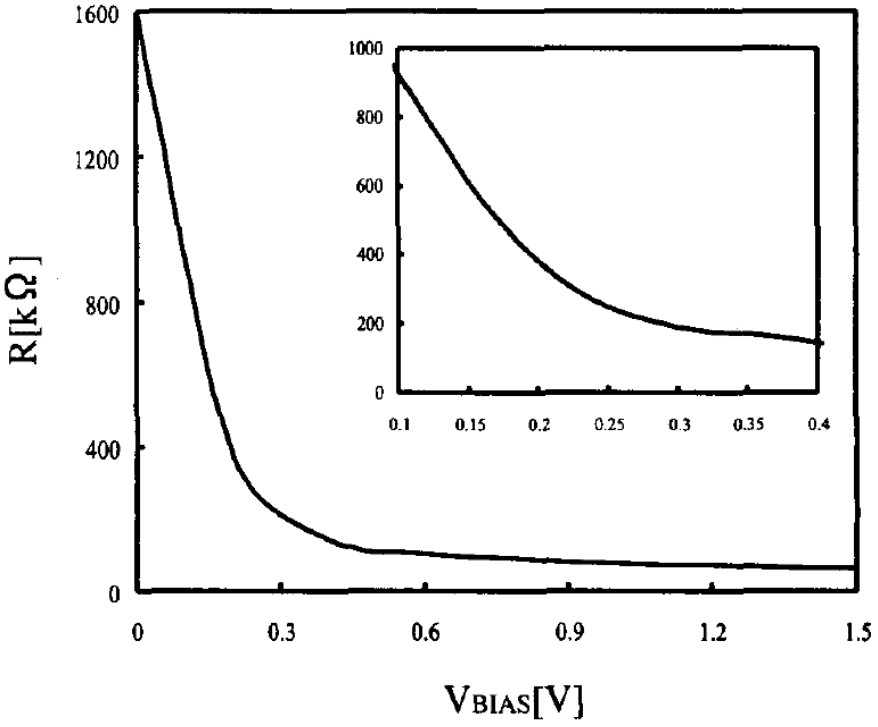


Fig.2.8: DC Transfer Characteristics Bias Voltage and Resistance

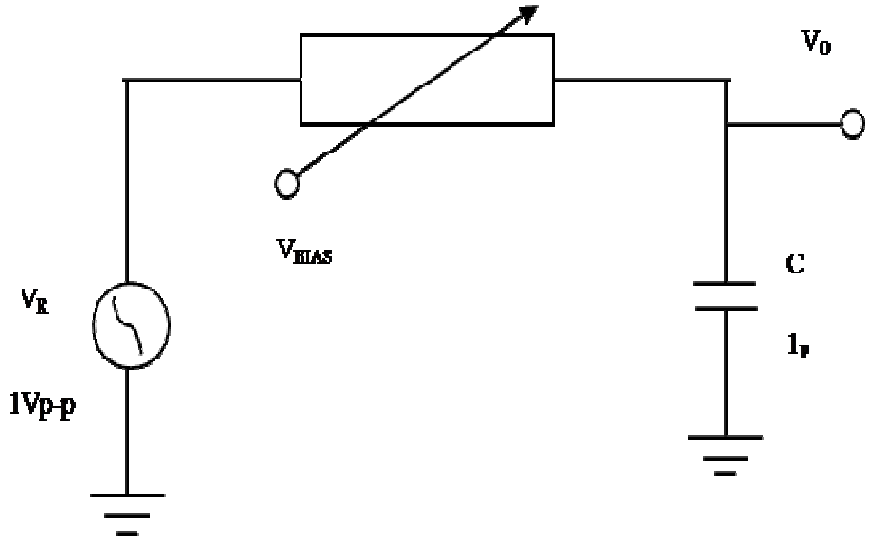


Fig.2.9: RC Filter using Presented Variable Resistor Circuit

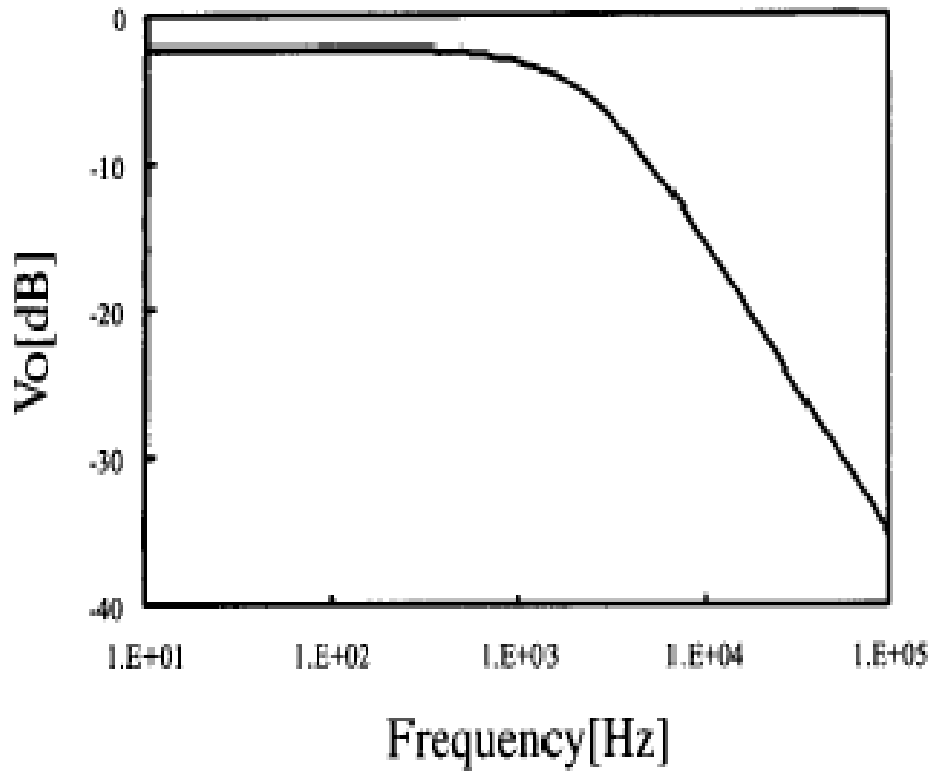


Fig.2.10: Frequency Response of RC Filter (Relationship between Gain, V_O [dB] and Frequency Hz)

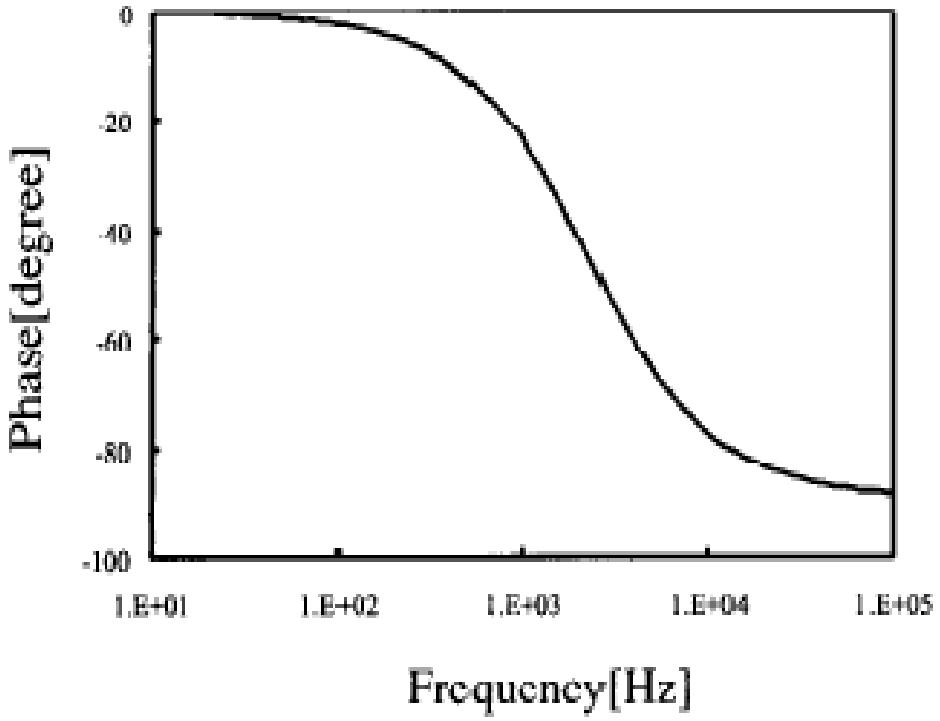


Fig.2.11: Frequency Response of RC Filter (Relationship between Phase [degree] and Frequency Hz)

2.3 CMOS FLOATING RESISTOR [11]

The CMOS floating resistor circuit is shown in Fig.2.12; the nodes 1 and 2 are the two terminals of the resistor. The matching transistors M_1, M_2, M_3 and M_3 are the basic transistors of the resistors and the remaining transistors perform the current transfer to the two nodes 1 and 2. All transistors are assumed to be operating in the saturation region with their sources connected to the substrate/bulk. The MOS drain current in the saturation is given by:

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2 \tag{2.41}$$

Where, $K = \frac{1}{2}\frac{W}{L}\mu_0 C_{OX,}$ μ_n is the electron mobility, C_{ox} is the oxide capacitance per unit area $\frac{W}{L}$ is the transistor aspect ratio and V_T the threshold voltage.

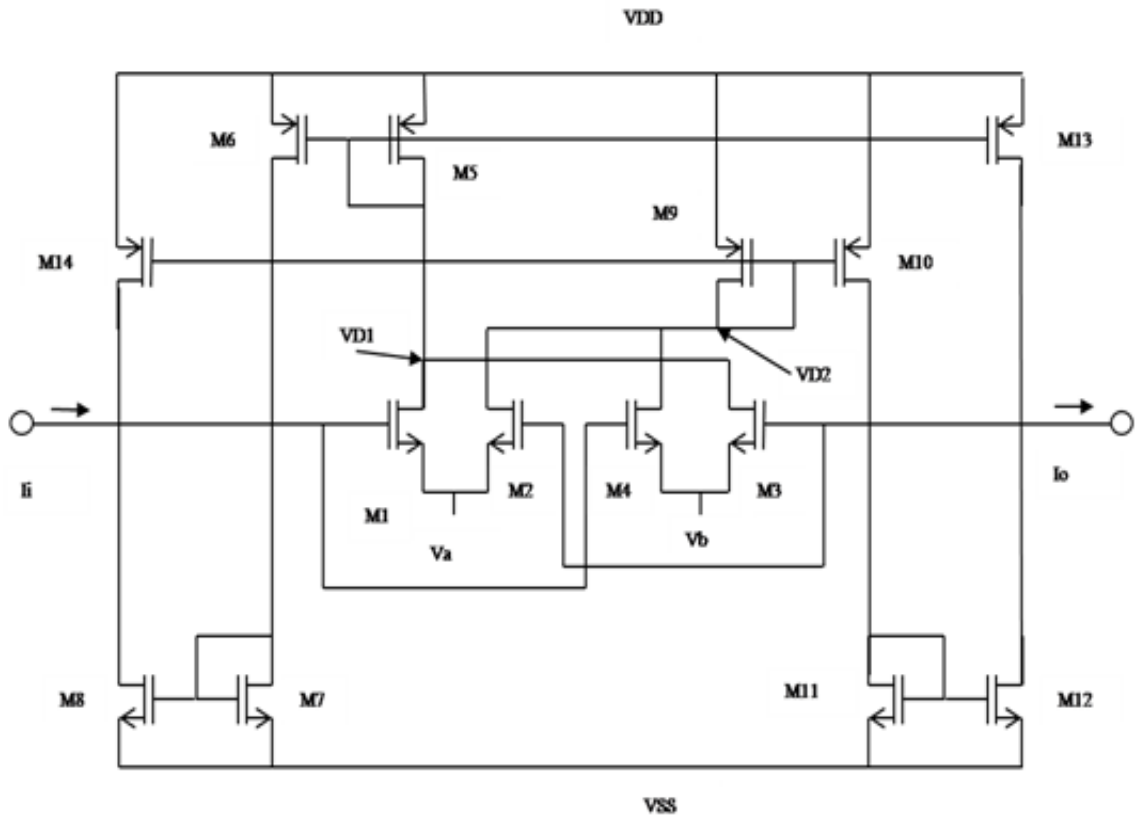


Fig.2.12: CMOS Floating Resistor

$$I_i = I_0 = (I_1 + I_3) - (I_2 + I_4) \tag{2.42}$$

Where,

$$I_1 = \frac{K}{2}(V_1 - V_a - V_T)^2 \tag{2.43}$$

$$I_2 = \frac{K}{2}(V_2 - V_a - V_T)^2 \tag{2.44}$$

$$I_3 = \frac{K}{2}(V_2 - V_b - V_T)^2 \tag{2.45}$$

$$I_4 = \frac{K}{2}(V_1 - V_b - V_T)^2 \tag{2.46}$$

Therefore, the current flowing through the resistor is given by:

$$I_i = I_0 = K(V_b - V_a)(V_1 - V_2) \tag{2.47}$$

Therefore, the CMOS circuit in Fig.2.12 simulates a floating resistor between the nodes 1 and 2 and its value is controlled by the differential voltage (V_b - V_a), independent of the threshold voltage and is given by:

$$R = \frac{(V_1 - V_2)}{I_0} = \frac{(V_1 - V_2)}{I_0} = \frac{1}{K(V_b - V_a)} \tag{2.48}$$

From Eq. (2.48), for $V_b > V_a$, the circuit operates as a resistor with positive resistance and when $V_b < V_a$, the circuit operates as a negative resistor.

2.3.1 SECOND ORDER EFFECT

The above analysis of the propose circuit were based on so far on the assumption that all the transistors characterized by the perfect square-law drain current equation. In the reminder of this section, the second order effects such as mobility reduction and channel length modulation will help to calculate the linearity error in the presented circuit will be discussed separately.

2.3.1.1 MOBILITY REDUCTION

The simplified I-V characteristic of an NMOS transistor can be modelled:

$$I_D = \frac{K}{2} \frac{(V_{GS} - V_T)^2}{1 + \theta(V_{GS} - V_T)} \tag{2.49}$$

Where θ is the mobility degradation parameter , by taking mobility reduction effect of the currents of the basic four transistors M_1, M_2, M_3 and M_4, The resistor current is given by;

$$I_i = I_0 = K(V_b - V_a)(V_1 - V_2)\Psi \tag{2.50}$$

Where Ψ is given by:

$$\Psi = \frac{K}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{2.51}$$

The error resulting from the mobility reduction can be reduced by making the common mode of the input voltages is close to (0.5 (V_a + V_b) + V_T).

2.3.1.2 CHANNEL LENGTH MODULATION

The drain current of the MOS transistor with the effect of channel length modulation is given by:

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{2.52}$$

Where λ is the channel length modulation parameter, by taking channel length modulation effect of the currents of the basic four transistors M_1, M_2, M_3 and M_4, The resistor current is given by:

$$I_i = I_0 = K(V_b - V_a)(V_1 - V_2) + \Delta \tag{2.53}$$

Where, Δ is given in terms of the drain voltages V_{D1} and V_{D2} of (M_1, M_3) and (M_2, M_4) respectively by:

$$\Delta = \frac{K\lambda}{2}\left(a_0 + a_1 {V_a}^2 + a_2 V_a + b_1 {V_b}^2 + b_2 V_b\right) \tag{2.54}$$

And

$$a_0 = (V_{D2} - V_{D1})\left({V_1}^2 + {V_2}^2 + 2{V_T}^2 - 2V_T(V_1 - V_2)\right) \tag{2.55}$$

$$a_1 = 2(V_1 - V_2) + (V_{D2} + V_{D1}) \tag{2.56}$$

$$a_2 = {V_2}^2 - {V_1}^2 + 2V_{D1}(V_2 - V_T) - 2V_{D2}(V_2 + V_T) \quad (2.57)$$

$$b_1 = -2(V_1 - V_2) + (V_{D2} - V_{D1}) \quad (2.58)$$

$$b_2 = {V_1}^2 - {V_2}^2 + 2V_{D1}(V_1 - V_T) - 2V_{D2}(V_2 - V_T) \quad (2.59)$$

From the above equations, the channel length modulation error A is neglected at small input voltages (V_1 and V_2,) and also small biasing voltages (V_a and V_b).

2.3.2 SIMULATION RESULTS

PSPICE simulations have been carried out to verify the performance of the presented CMOS floating resistor circuit using model parameters of 0.35µm CMOS process provided by MOSIS. The supply voltages are equal to ± 1.5 V. Fig. 2.13 illustrates the I-V DC characteristics between the resistor current and the input voltage V_1 for different values of V_2 with the biasing voltages V_a = -1.05 V and V_b = -0.85 V. It is shown that the presented CMOS resistor features a linear resistor over the input differential voltage range from -0.5 V to 0.5V and resistance value of R = 50 kΩ.

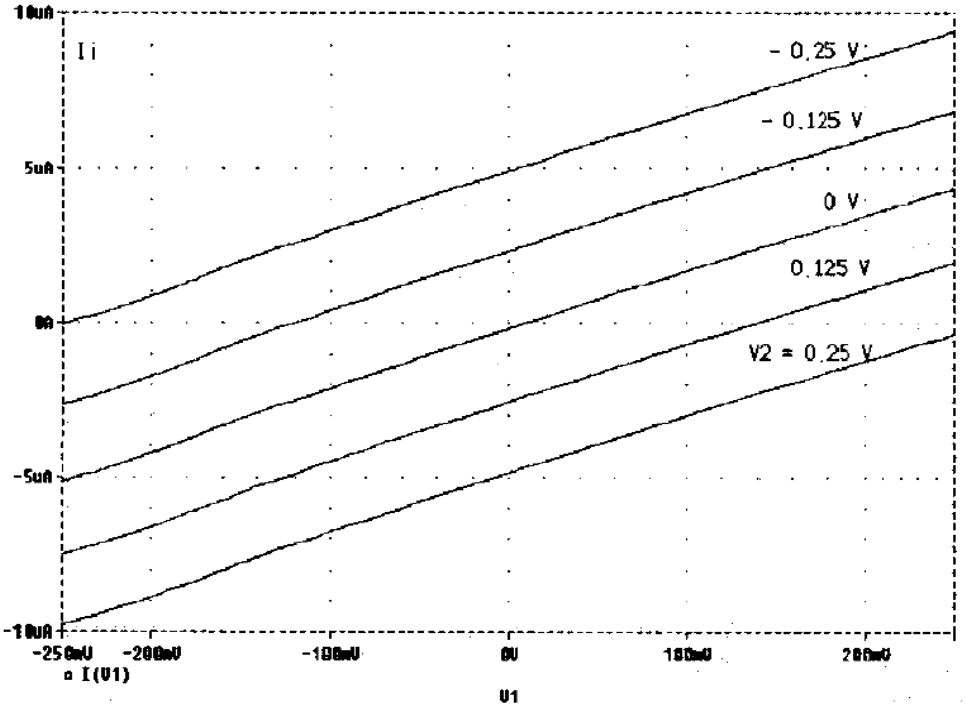


Fig.2.13: The I-V Characteristics of the Presented Floating Resistor Circuit with V_2 as Parameter

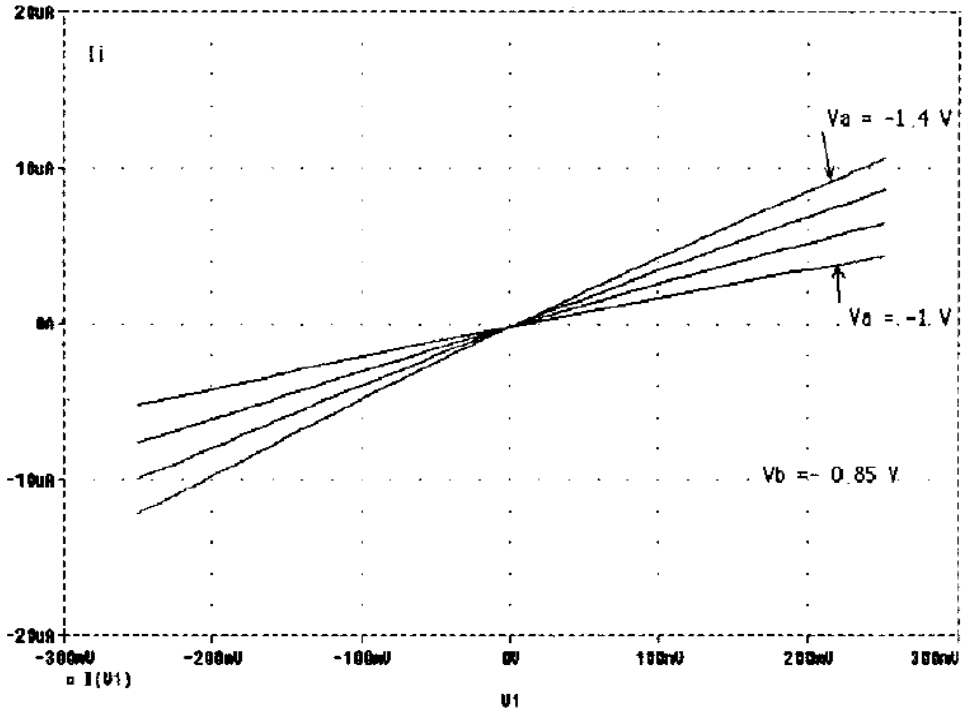


Fig.2.14: The I-V Characteristic of the Presented CMOS Floating Resistor with $V_2 = 0V$

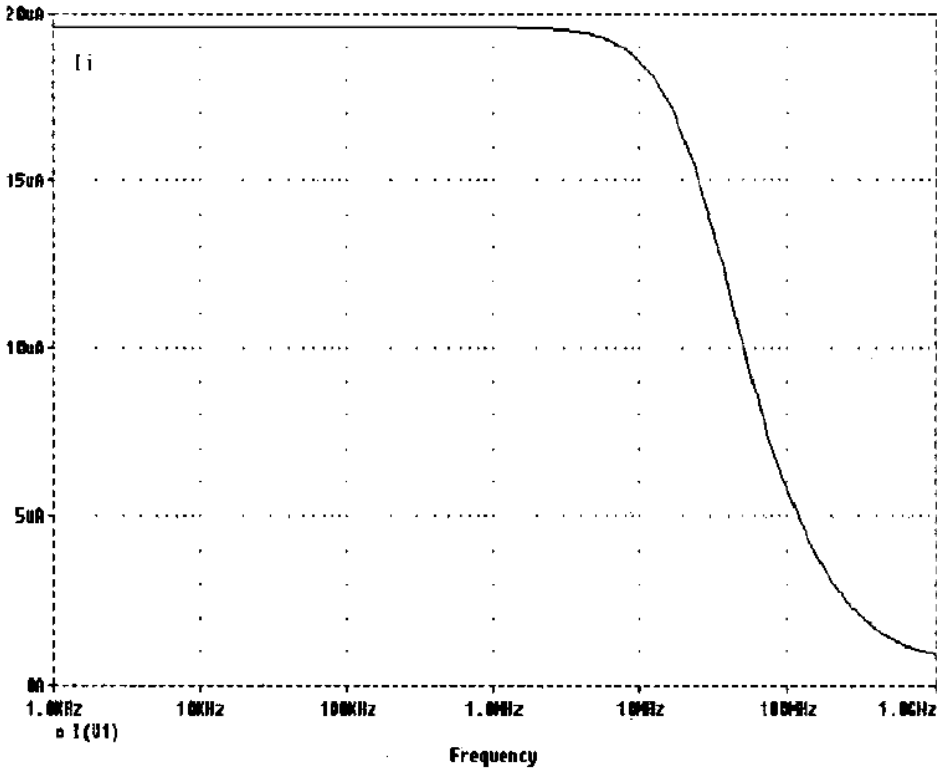


Fig.2.15: The Magnitude Frequency Response of the CMOS Resistor Current

Fig.2.14 illustrates the I-V DC characteristics between the resistor current and the input voltage V_1 for V_2 equal zero volt with the biasing voltage V_a scanned from -1 V to -1.4 V and V_b = -0.85 V. It is shown that the presented CMOS resistor features a linear resistor over the single ended input voltage range from -0.25 V to 0.25V and resistance values from R=25 KΩ to R = 50 kΩ . The THD is less than 0.4 % for a 100 KHz 0.2V peak-to-peak sinusoidal input. The standby current of the presented circuit is less than l00pA. Fig.2.15 indicates the magnitude frequency response of the CMOS resistor current flat to 10MHz.

Fig 2.15 shows the magnitude frequency response of the CMOS resistor current flat to 100MHz.

2.4 FLOATING CONTROLLED RESISTOR

The presented circuit uses an approach to implement high value controlled floating resistors using CMOS current controlled conveyors (CCCIIs)

2.4.1 CMOS SECOND GENERATION CCCII [10]

A second-generation CCCII is identical to a second-generation current conveyor (CCII) with its intrinsic resistance R_X, at port X, which is adjustable with the bias current [14], [15]. The ideal controlled conveyor with a positive current transfer from X to Z is described by the following matrix relationship that exists between voltages and currents of its input–output ports [14], [15].

$$\begin{pmatrix} i_y \\ v_X \\ i_Z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & R_X & 0 \\ 0 & 1 & 0 \end{pmatrix} \begin{pmatrix} v_Y \\ i_X \\ v_Z \end{pmatrix}$$

In this expression the current transfer $\frac{I_Z}{I_X}$ is equal to 1 for the ideal positive CCCII. Its input impedance on port Y is infinite. The port Z, which is equivalent to a current generator, has infinite output impedance.

Fig.2.16 and fig.2.17 shows the schematic implementation of the CCCII and its electrical symbol respectively. This circuit operates in class AB, and all transistors work in strong inversion region. Two NMOS transistor M_1, M_2 and two PMOS transistor M_3, M_4 uses a mix trans-linear loop. DC bias provided by control current Iss. This gives to the circuit high-

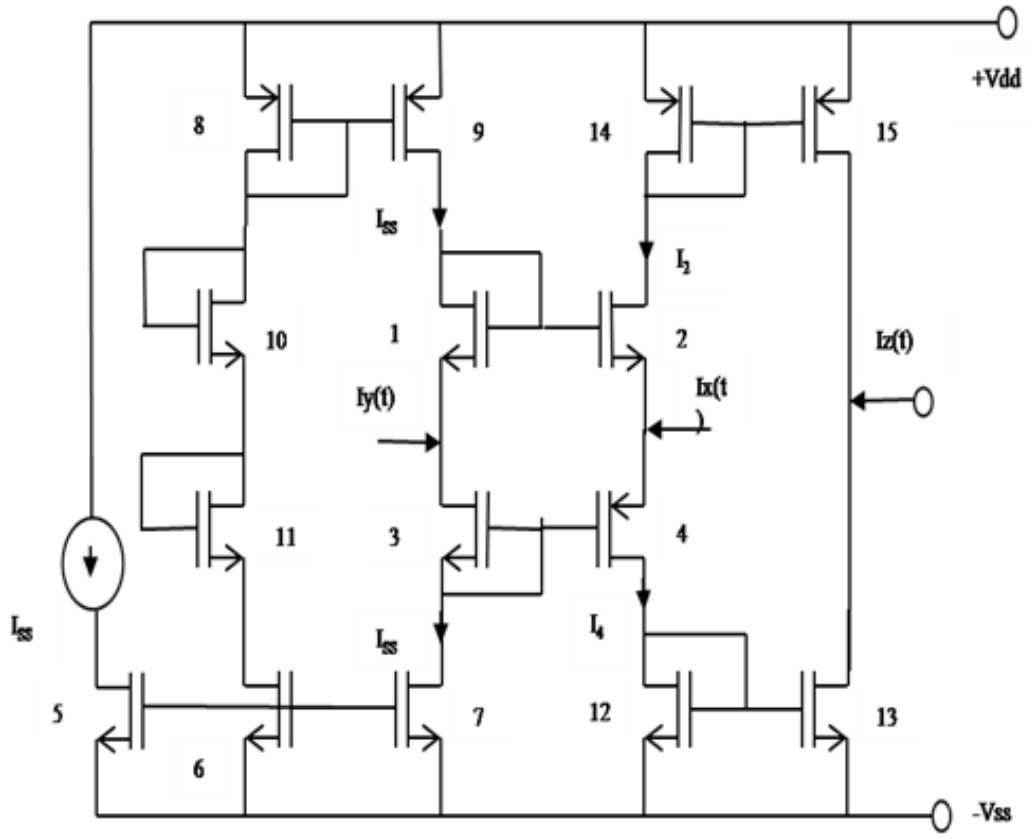


Fig 2.16: CMOS CCCII. Schematic Diagram

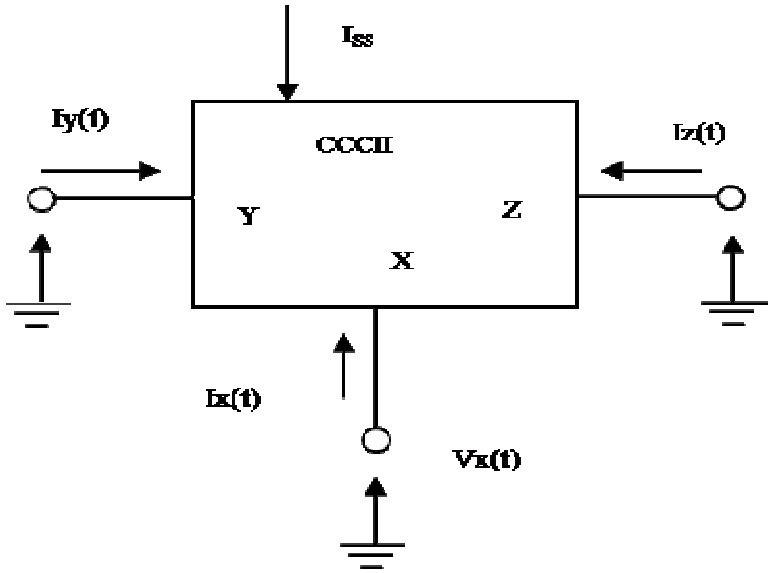


Fig.2.17: CMOS CCCII Electrical Symbol

input impedance at port Y. For low- magnitude input current iX (t), the mixed loops force the drain currents of transistors M1 to M4 to be equal to Iss. This consequently gives VX (t) = VY (t) [14], [15] and [23]. This equivalent follower presents at port X a small signal intrinsic resistor R_X i.e. inversely proportional to the square root of the bias current I_{SS} [14], [15]. Two complementary current mirrors (M_{12}, M_{13}) allow duplicating on port Z the input current at X; then i_Z (t) = i_X (t).

Fig.2.18 the theoretical implementation of the high-value controlled floating resistor realized from two positive CCCIIs above [14], [15]. A load resistor R_L is connected between ports X of both positive CCCII. The output stage of CCCII is constituted by a current divider. Then, the output currents at ports Z_1' and Z_2' are connected in a cross coupled way to the high-input impedance ports Y_1 and Y_2. These inputs are the access point of the floating resistor R_E. The resistance is adjustable by the bias current I_{SS1}=I_{SS2} =I_{SS}, is given by R_E= n ($2R_X$+R_L), where R_X is the intrinsic resistance at port X of each CCCII.

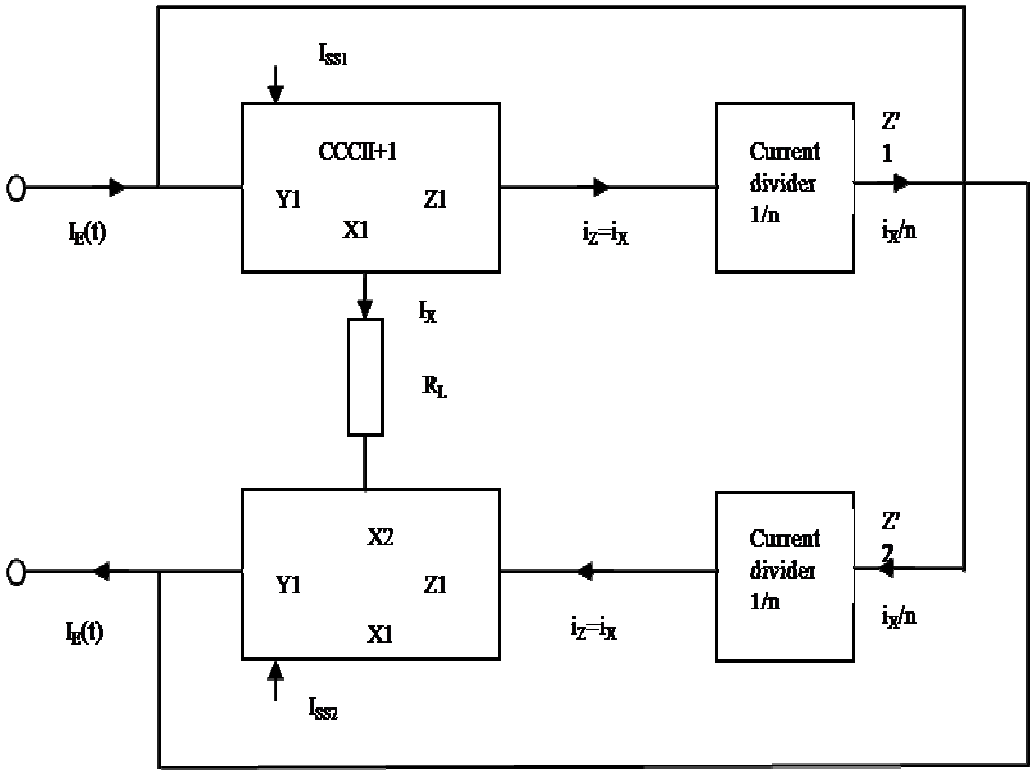


Fig2.18: Symbolic Implementation of Floating Resistor

For the negative floating controlled resistor R_E= n ($2R_X$+R_L) When the output Z′ are directly connected to the corresponding input Y of the same CCCII. The output current at X to be mirrored to port Z after division by the number of transistors M_{12}, M_{14} that are connected in parallel then $i'_Z(t) = \frac{i_{X(t)}}{n}$ where n is the value of this resistor depends on both the CCCII bias current because R_X is controlled by I_{SS} and the load resistor value R_L, between, respectively, each port Y, Z and the ground, the CCCI exhibits parasitic equivalent impedances [14], [15], respectively, (R_Y || C_Y) and (R_Z || C_Z).

When the parasitic impedances of each conveyor are taken into account, the effective input impedance of the circuit in Fig.2.18 is given by R_E = n ($2R_X$ + R_L) ||$2R_P$||C_P/2, where R_P = (R_Y|| R_Z) and C_P=C_Y +C_Z. Where the theoretical study of the noise current sources at each port of the CCCII shows that to decrease the equivalent noise in ports X, Y, and Z, it is in fact necessary to minimize the noise of the current mirrors [24]. Then, a compromise on the size of transistors (M_5 to M_9 and M_{12} to M_{15}) has been used to reduce the noise current source of the floating resistance.

2.4.2 SIMULATION RESULTS

The floating resistor has been designed and simulated for n = 8using the 0.8-µm CMOS technology from Austria Micro System [25]. The supply voltage is ±3.3 V. For bias current equal to 100µA and a load resistance R_L of 10 kΩ, the frequency response of the CMOS floating resistor of 68 kΩ has a 3-dB cutoff frequency of about 20MHz.

Table 2.2: Cut of Frequency of the Floating Resistor

R_E as a Function of I_{SS}, for R_L = 0 kΩ, with n=8 and V= ± 3.3V

I_{SS}, µA	20	50	100	150	200
f_{-3dB}, MHz	54	87	115	140	160

This results from the above parasitic capacitance Cp of about 0.12pF. Table2.2 gives the corresponding values of the cutoff frequencies for R_L = 0kΩ and for various values of ISS. We can see that as I_{SS} increases, the cutoff frequency also increases.

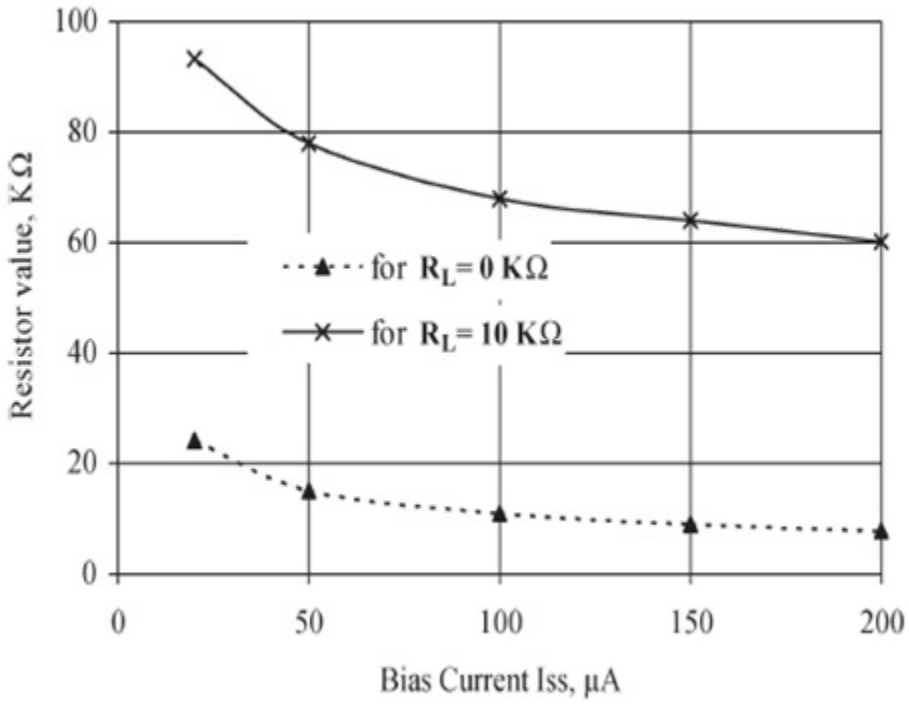


Fig.2.19: Variation of the Resistor Values R_E as a Function of the Bias Current I_{SS} = 0µA

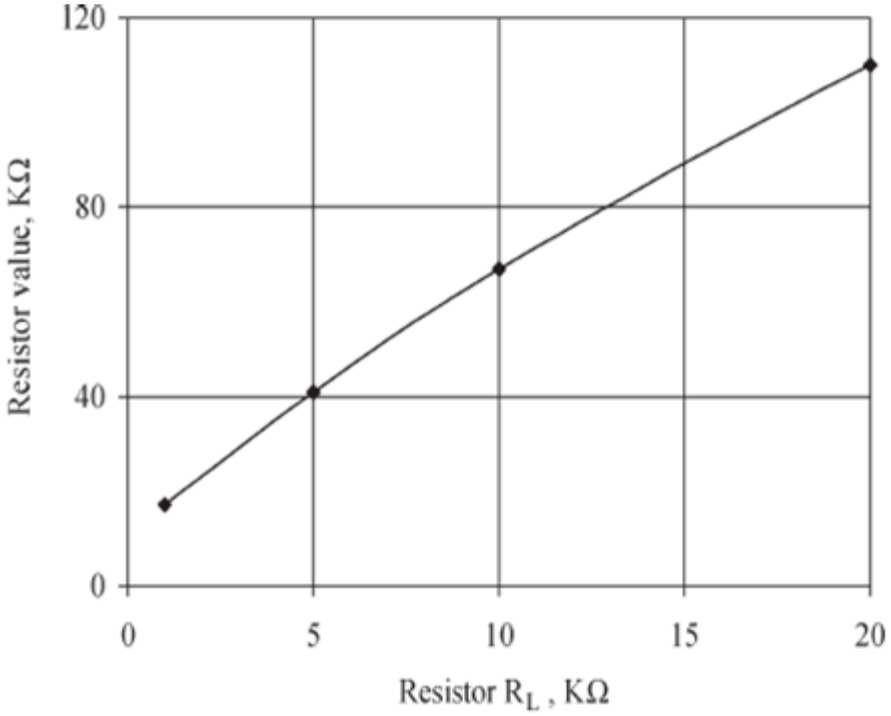
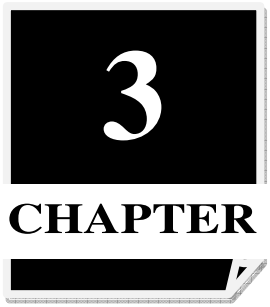


Fig.2.20: Variation of the Resistor Values R_E as a Function of the Load Resistor for I=100µA

Fig.2.19 represents, for R_L = 0 and 10 kΩ, the variation of the value of the resistor as a function of I_{SS}. With R_L = 0 kΩ, the value of the resistor decreases from 24.2 to 7.8 kΩ when I_{SS} varies between 20 and 200μA.

The variation of this resistor as a function of the load resistor R_L when I_{SS} = 100μA is given in Fig.2.20. Its values increase from 11 to 110 kΩ when R_L varies from 0 to 20 kΩ. Note that higher values can also be obtained using greater values of n.

This floating resistor has been successfully used to compensate the parasitic negative resistance of a balanced CMOS controlled integrator in order to increase its dc finite gain value and consequently its frequency range of operation [10]. It has also been used to compensate the negative resistor of an active floating inductance used in an adjustable low-pass third-order image rejection filter. This filter is characterized by a 5-MHz cutoff frequency and 63-dB attenuation for the rejected signal at 9MHz.



AN ADJUSTABLE FLOATING RESISTOR

3.1. CMOS FLOATING RESISTOR

Floating resistors in silicon technology can be found in applications such as continuous-time filters, amplifiers, and artificial neural networks (ANN), etc. Passive resistors made with polysilicon or diffusion area have disadvantages of sensitivity to temperature and consequently poor stability in values, low sheet resistance and area inefficiency.

In the context of optimizing electronic structures performances for operating in the neighborhood of technological limits, the design of integrated circuits moves away from automatized area specific to any approaching of a technical project, becoming, after successive overrunning of the technological barriers, art and inspiration, much more than systematic and rigorous treating of the fundamental concepts. Adapting of existing techniques and proposal of some original design methods, specific to latest micron technologies represents the key elements of the presented research methodology. The reduction of costs necessary for design and implementation of integrated active resistor circuits, performances maximization, obtained by applying original techniques presented in this paper, associated with the reduction of power consumption and of the supply voltage enlarge the utilization area of these circuits at a series of portable circuits. A very important trend in VLSI designs, especially for latest micron technologies is the continuous reducing of the layout area. In CMOS circuits, parasitic bipolar transistors and especially classical resistors having a surface consumption proportional to the value of the resistance represent the largest area consumers. Thus, resistances greater than 10 kΩ are not efficient to obtain

using the classical approach. The new method for reducing the occupied area for large values of the active resistance is to implement a circuit named active resistor using exclusively MOS transistors in order to simulate a linear current-voltage characteristic, similar to that of a classical resistor. The area of utilization for active resistors includes, but are not limited to amplitude control in low distortion oscillators, voltage controlled appliers and active RC filters.

Analogue circuits are commonly designed using simple circuits as building blocks (e.g. differential pairs and current mirrors). Apart from the elegance of simple solutions, there are other good reasons for this design practice: adding components tends to limit the high frequency potential of circuits (additional nodes) and tends to increase the noise level and power consumption. Hence, "squeezing" maximal performance out of a minimal set of components seems to be a very viable design philosophy.

In MOS transistor circuits, transistors are the main components. The primary transistor property that is exploited in many circuits like the differential pair and the current mirror is the transconductance of a MOS Transistor. Consequently, the principle operation of many CMOS circuits can be understood considering them as transconductance based circuits, i.e. circuits with a transfer function that is mainly determined by the transconductance of MOS transistors. Important reasons for this design practice are the good matching of the transconductance values of equally biased MOSTs (better than 0.5% current matching is possible). The electronics variability of the transconductance of MOS Transistors. This allows for on-chip self-correction for spread in IC-processing. The large range of transconductance values that the transconductance of a MOST can take which is much larger than the achievable conductance range for integrated resistors.

CMOS active resistors are extensively used in analog integrated circuit for replacing the large value passive resistor, having the great advantage of a much smaller area occupied on silicon. Passive resistor made with polysilicon or diffusion area has disadvantages of sensitivity to temperature and consequently poor stability in values a low sheet resistance and area inefficient. The wide range of application for CMOS floating resistor in silicon technology such as continuous time filter, amplifier, artificial neural network. Passive resistor

made with polysilicon or diffusion area have disadvantage of sensitivity to temperature and consequently poor stability in values and low sheet resistance and area inefficiency. Thus, various active resistor circuits have been presented for replacing inaccurate passive resistors [8]-[13]. In [8], a linear floating resistor that was composed of two enhancement-type PMOS transistors was presented. [9]- [10] introduced floating resistors that were based on current conveyors and their resistances depended on the thermal voltage. [11] summarized two commonly used circuit configurations for realizing floating resistors, and presented a floating resistor tunable by two voltage supplies, which provided currents to the sources of input transistors. [14] described a floating resistor circuit which was based on the linear relationship of Ids vs. V_{ds} of a MOS device working in the linear region, and some other MOS transistors, working in the saturation region, served as voltage shifters to compensate the variation in the gate voltage of the device that works in the linear region.

The CMOS circuit for the realizing floating resistor has been presented [19]. In this circuit a modified linear transconductor is used which provides two copies of output currents. The currents are equal in magnitude and opposite direction. The resistance of this circuit is adjustable by controlling the gate voltage of a MOS transistor and can be selected to be positive are negative by changing the feedback connections.

The transconductance block shown in fig.3.1 has two output currents. The one with positive sign and is same as the I_0 in Eq. (1.1) and the one with negative sign is identical in magnitude but opposite in direction. The positive and the negative output current are feedback to provide currents to the input terminals and depicted in the figures, and the value of the currents are proportional to the difference of the difference of the input voltages, as described by Eq. (1.1). Thus circuit behaves exactly the same as a linear resistor with two terminals V_+ and V_-.

Fig.3.1 (a) depicts the circuit configuration for a positive resistance $1/g_m$. To implement a negative resistor, we only need to switch the connection between the output and inputs as illustrated in Fig. 3.1(b).

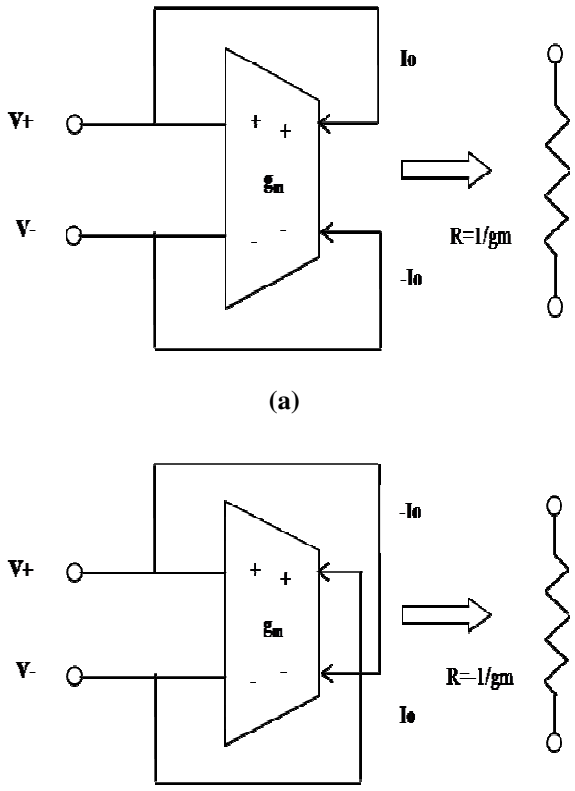


Fig.3.1 (a) Positive Floating Resistor Based on Modified Linear Transconductance

(b) Negative Floating Resistor Based on Modified Linear Transconductance

3.2 CMOS CIRCUIT REALIZATION

Since the presented circuits are based on transconductance, a brief review of transconductance is given in this section. To implement a linear transconductance is using differential pairs as shown in Fig.3.2 [26]. Here we assume that the bodies of the transistors are connected to their sources.

An ideal transconductance has infinite input and output impedance Here M_1 and M_2 are the NMOS input stage, whose tail current I_{adj} is provided by the current sink transistor M_9. The current distribution in the two input transistors M_1 and M_2 is controlled by their gate voltages, and these two currents are transmitted to the output stage by current mirrors that are composed of $M_3 - M_8$. The output I_o current is the difference between the two currents passing through transistors M_6 and M_8. By varying the sink current I_{adj} and the amplification factors of the current mirrors, the transconductance of the differential pair can be adjusted.

The transistors M_1 and M_2 are identical and both working in the saturation region, neglecting the channel length modulation, the source currents of M_1 and M_2 are expressed as:

$$I_{M1} = \left(\frac{K_1{}'W_1}{2L_1}\right)[(V_{GS1} - V_T)^2] = K_1(V_{Gs1} - V_{Tn})^2 \quad (3.1)$$

$$I_{M2} = \left(\frac{K_2{}'W_2}{2L_2}\right)[(V_{GS2} - V_T)^2] = K_2(V_{Gs2} - V_{Tn})^2 \quad (3.2)$$

$$I_{M1} = K_{1,2}(\Delta V + V_{GS2} - V_{Tn})^2 \quad (3.3)$$

$$I_{M2} = K_{1,2}(V_{GS2} - V_{Tn})^2 \quad (3.4)$$

where V_{tn} is the threshold voltage of NMOS transistors, ΔV is the Difference between the two voltage inputs and $K_{1,2}$ is the fabrication-dependent parameter of M_1 and M_2.

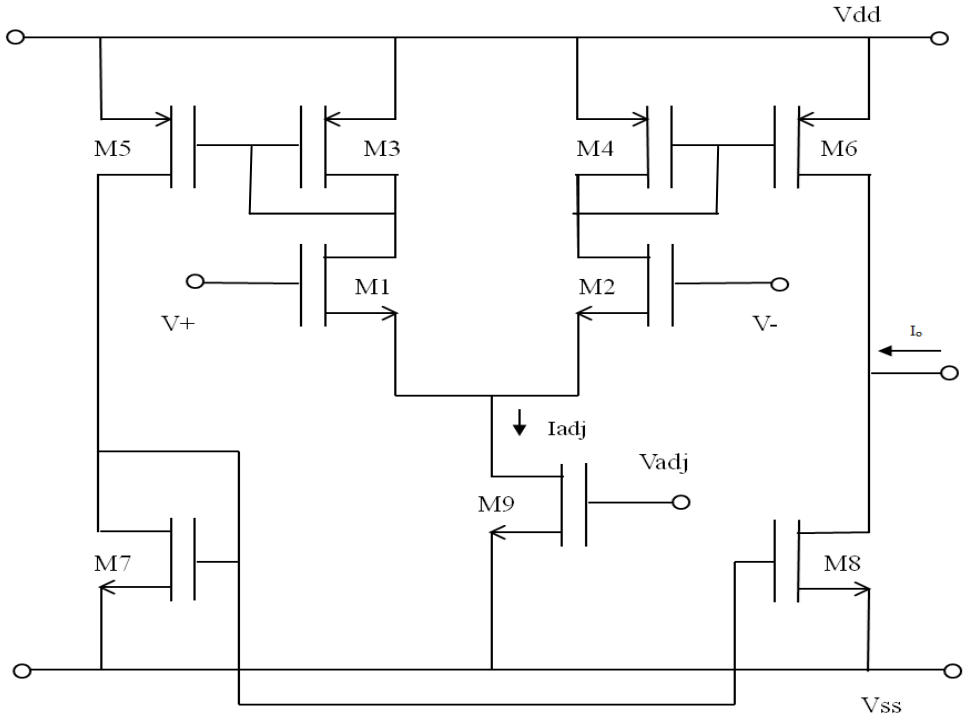


Fig.3.2: CMOS Differential Pair Circuit

The fabrication-dependent parameter K of a transistor is decided by the transistor aspect ratio W/L, electron mobility μ_0, and gate oxide capacitance C_{OX}.

$$K = \frac{1}{2}\frac{W}{L}\mu_0 C_{OX} \tag{3.5}$$

$$\Delta V = V_+ - V_- = V_{gs1} - V_{gs2} \tag{3.6}$$

From Eqs. (3.3) and (3.2), we can derive the following equations by using

$$I_{adj} = I_{M1} + I_{M2}$$

$$I_{M1} = \frac{1}{2}\left(Iadj + K_{1,2}\Delta V\sqrt{\frac{2Iadj}{K1,2} - \Delta V^2}\right) \tag{3.7}$$

$$I_{M2} = \frac{1}{2}\left(Iadj + K_{1,2}\Delta V\sqrt{\frac{2Iadj}{K1,2} - \Delta V^2}\right) \tag{3.8}$$

$$g_m = \frac{I_{M8} - I_{M6}}{\Delta V^2} = A\frac{I_{M1} - I_{M2}}{\Delta V} = AK_{1,2}\sqrt{\frac{2I_{adj}}{K_{1,2}} - \Delta V^2} \tag{3.9}$$

where A is the amplification factor of the current mirrors composed of $M_3 - M8$, and M_4 and M_6, composed of $M_3 - M_8$, and M_4 and M_6, i.e. $A = (I_{M8}: I_{M1}) = (I_{M6} : I_{M6})$. when ΔV^2 is much smaller than $2I_{adj}/K_{1,2}$ and is ignored, g_m is a constant $A\sqrt{2K_{1,2}I_{adj}}$ .The input terminals of the differential pair are the gates of M_1 and M_2 and consequently take nearly no currents and, thus, the circuit in Fig.3.2 work as a linear transconductor. Equations (3.1) - (3.9) are satisfied under the condition that all the transistors in Fig. 3.2 work in the saturation region. Input voltages cannot be too high in order to let M_1 and M_2 meet this constraint, expressed in equation, $V_{gs} - V_t < V_{ds} \Rightarrow V_{gd} < V_t$. Considering that the gate voltages of M_1 and M_2 are the input voltages, and their drain voltages can be derived from M_3 and M_4, we can find the upper bound limit on V_+ and V_- referenced to ground:

$$V_+ < V_{dd} + V_{tn} + V_{tp}\sqrt{\frac{I_{adj}}{K_9}} \tag{3.10}$$

$$V_- < V_{dd} + V_{tn} + V_{tp}\sqrt{\frac{I_{adj}}{K_9}} \tag{3.11}$$

The lower bound limit of the input voltages exists because of the saturation working requirement on M_9. By using $V_{gd} < V_t$ on M_9, we can derive:

$$V_+(orV_-) > V_{adj} + \sqrt{\frac{I_{adj}}{K_9}} \tag{3.12}$$

In order to let the differential pair in Fig.3.2 work as a linear transconductance, ΔV needs to be limited into a certain range. Ignoring the slight changes in I_{adj} caused by the variation of V_{DS9}, the non-linearity of the transconductance relies on the term ΔV^2 in Eq. (3.9). Take a Taylor series expansion on the square root of Eq. (3.9) and take an approximation by ignoring high order terms, we have:

$$g_M = AK_{1,2}\sqrt{\frac{2I_{adj}}{K_{1,2}}}\left(1 - \frac{K_{1,2}\Delta V^2}{2I_{adj}}\right)^{\frac{1}{2}}$$

$$\approx AK_{1,2}\sqrt{\frac{2I_{adj}}{K_{1,2}}}\left(1 - \frac{K_{1,2}\Delta V^2}{4I_{adj}}\right) \tag{3.13}$$

where, the first part of the right side of the equation $AK_{1,2}\sqrt{\frac{2K_{1,2}I_{adj}}{K_{1,2}}}$ is a constant, and the second part $AK_{1,2}\sqrt{\frac{2K_{1,2}I_{adj}}{K_{1,2}}}\,\frac{K_{1,2}\Delta V^2}{4I_{adj}}$ varies along ΔV, and, thus, causes a nonlinearity. Given the maximum allowable transconductance difference in ratio η, i.e. $\eta = \max[(g_{m0} - g_m)/g_{m0}]$ where g_{m0} is the transconductance at ΔV = 0, and gm is an arbitrary transconductance, from Eq. (3.13), we can derive the range of ΔV:

$$\frac{K_{1,2}\Delta V^2}{4I_{adj}} < \eta \quad \Rightarrow \quad \frac{4I_{adj}}{K_{1,2}} \tag{3.14}$$

Hence, according to Eq. (3.14), in order to achieve a good linearity of the transconductance, the magnitude of the differential input ΔV needs to be kept much smaller than $I_{adj}/K_{1,2}$, or at the same ΔV , I_{adj} can be enlarged, under the restriction that all transistors are still in the saturation region, described by Eq. (3.10)- (3.12).

To the presented differential pair circuit can be easily added another current output to serve as the modified linear transconductance described in section 3.1. Then, following the method introduced earlier, a positive floating resistor can be realized by connecting the inputs and

outputs of the differential pair. This is illustrated in Fig.3.3. The transistors and wires drawn with dotted lines are newly added upon the circuit shown in Fig.3.2.

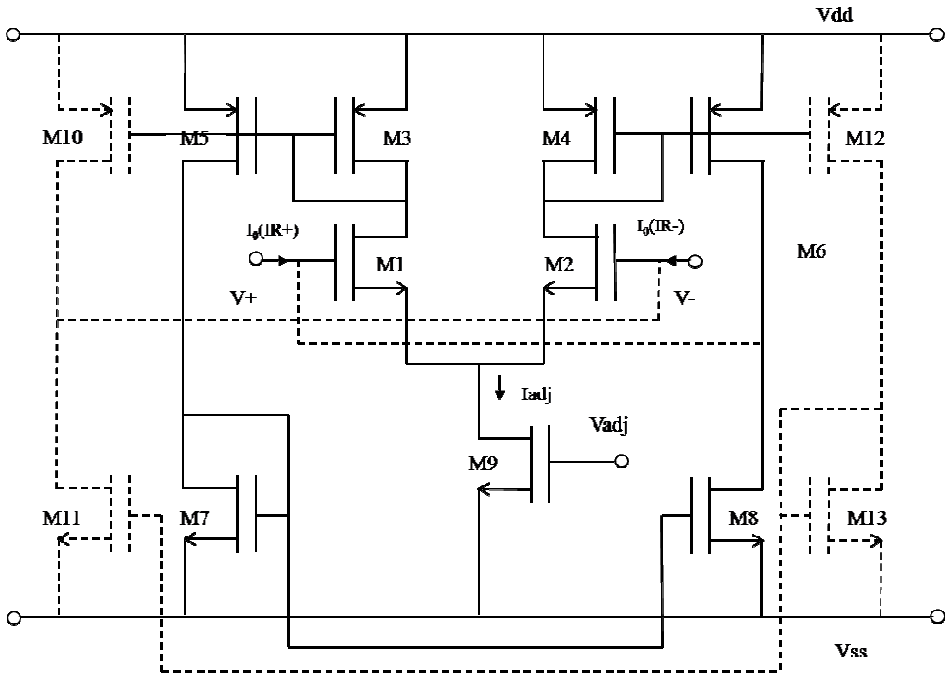


Fig.3.3: CMOS Linear Floating Resistor

The added transistors make the circuit topology of the left side and the right side perfectly symmetrical. When $V_+ > V_-$, the current flowing into the V_+ port is provided by M_6 and M_8, and the current flowing out of the V_- port is sourced from M_{10} and M_{11}. The circuit configuration in Fig.3.3 shows the case of a positive resistance, which is, from Eq. (3.13), expressed by:

$$R = \frac{1}{g_m} \approx \frac{1}{A\sqrt{2K_{1,2}I_{adj}}}$$

$$= \frac{1}{A(V_{adj} - V_{tn} - V_{ss})\sqrt{K_{1,2}K_9}} \qquad (3.15)$$

To obtain a negative resistance, we only need to switch the feedback connections in the circuit in Fig.3.3, following the way illustrated in Fig. 3.1(b).

The CMOS floating resistor shown in Fig.3.3 being non-ideal two terminal devices, can experience current difference in two terminals, that is the current flowing into V+ is different from the current flowing out of V- due to the impact from the external circuits. This happens when the currents in the output transistors in Fig. 3.3 do not mirror properly the current decided by the input stage. Hence, good current mirrors are important to ensure the resistor properties of the circuit, and therefore cascode current mirrors are used in the modified CMOS Linear Floating Resistor shown in Fig. 3.4. In the modified Floating Resistor circuit, cascode current mirrors composed of M_7, M_7' , M_8, M_8', M_{11}, M_{11}', M_{13}, and M_{13}', have been replaced current mirror composed of M_7, $M_{8,}$, M_{11}, and M_{13} in Figure 3.3.

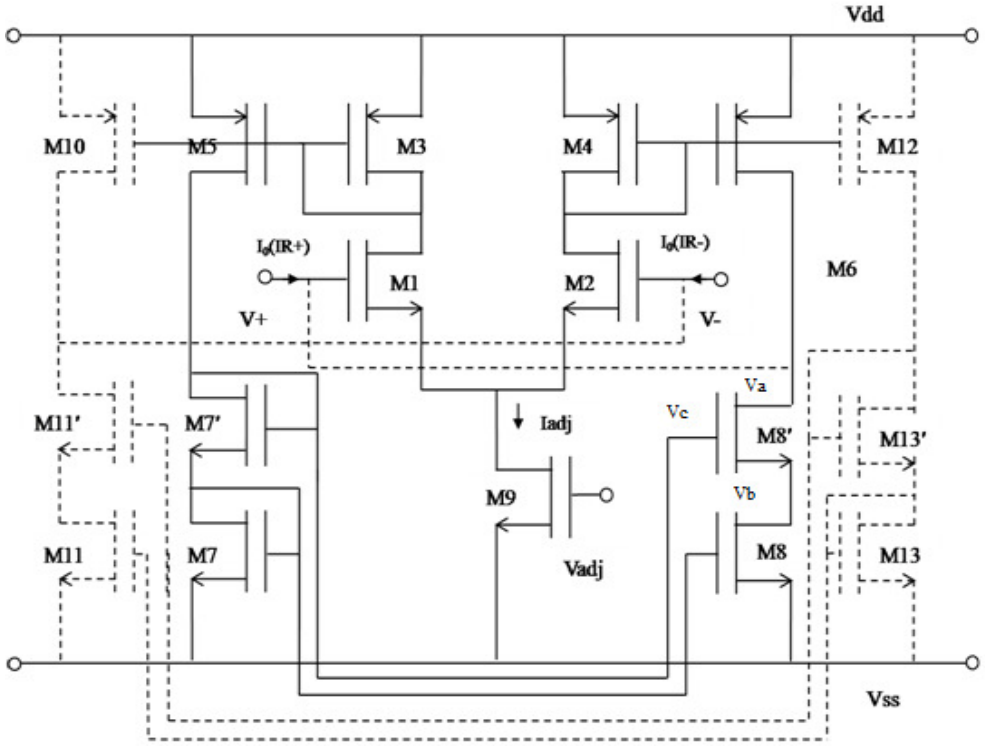


Fig. 3.4: Modified CMOS Linear Floating Resistor

4 CHAPTER

SIMULATION RESULTS AND LAYOUT DESIGN

The CMOS differential pair circuit, CMOS linear floating resistor, and modified CMOS linear floating resistor have been simulated using Cadence Spectre analog simulation environment with BSIM3v3 version 3.2 model parameters. The BSIM3v3 version 3.2 model parameters are given in Appendix A.

4.1 SIMULATION RESULTS

4.1.1 SIMULATION RESULTS OF CMOS DIFFERENTIAL PAIR CIRCUIT

The CMOS differential pair circuit shown in Fig.3.2 has been simulated using Cadence Spectre analog simulation environment with BSIM3v3 version 3.2 model parameters. The circuit is operated at supply voltages of ± 0.9V. The aspect ratios of the transistors are listed in Table 4.1. Fig. 4.1 shows the I-V characteristics of the CMOS differential pair circuit for the various values of adjusted voltage (V_{adj}) varies from -380mV to -200mV with the increment of 20mV. V_- is fixed to ground and V_+ is scanned to achieve the voltage change across the circuit. The V_+ is varied from -180mV to 180mV with the increment of 10mV. The output current (I_{out+}) have been measured at various adjusted voltages (V_{adj}) for V_+= -100mV and 100mV and listed in Table 4.2. The total power dissipation of the CMOS differential pair is 7.92µW.

Table 4.1: Aspect Ratios of the Transistors used in Spectre Simulation. Δ = 0.2µm.

M_1,M_2	M_3,M_4	M_5,M_6,	M_7,M_8	M_9
15Δ:45Δ	50Δ:30Δ	15Δ:140Δ	20Δ:140Δ	12Δ:45Δ

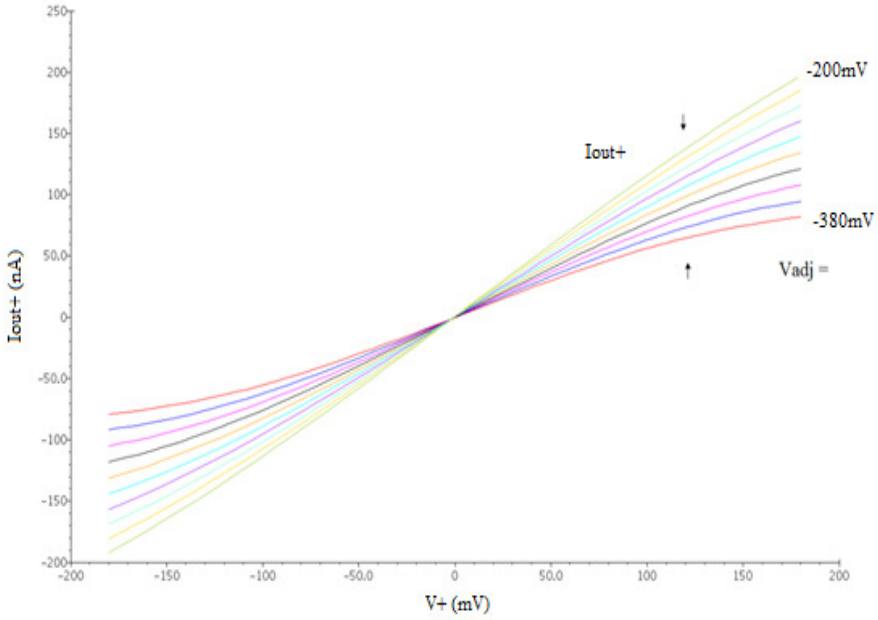


Fig4.1: I-V Characteristics of the CMOS Differential Pair Circuit

Table 4.2: Output Current of the CMOS Differential Pair Circuit

V_{adj} (mV)	I_{adj} (µA)	I_{out+} (nA)	
		V_+ (100mV)	V_+ (-100mV)
-200	4.0908	115.72	-113.49
-220	3.6792	109.49	-107.62
-240	3.2869	103.98	-101.58
-260	2.9152	96.782	-95.393
-280	2.5655	90.282	-89.065
-300	2.2381	83.672	-82.59
-320	1.9333	76.942	-75.975
-340	1.6502	70.942	-69.207
-360	1.3924	63.125	-62.301
-380	1.1587	56.07	-55.288

4.1.2 SIMULATION RESULTS OF CMOS LINEAR FLOATING RESISTOR

The CMOS Linear Floating Resistor circuit shown in Fig.3.3 has been simulated using Cadence Spectre analog simulation environment with BSIM3v3 version 3.2 model parameters. The circuit is operated at supply voltages of ± 0.9V. The aspect ratios of the

transistors are listed in Table 4.3. Fig. 4.2 shows the I-V characteristic of CMOS linear floating resistor. V– is fixed to ground, and V+ is scanned to achieve the voltage change across the circuit. The two groups of curves in this figure are the currents flowing into two different resistor terminals. With V_{adj} scanned from -400mV to -220mV, the simulated circuit presents a resistance from 0.93MΩ to 2.0MΩ in the linear working region. The resistances at different V_{adj} are provided in Table 4.4. The total power dissipation of the CMOS floating resistor is 7.58μW.

Table4.3: Aspect Ratios of the Transistors used in Spectre Simulation. Δ = 0.2μm.

M_1,M_2	M_3,M_4	M_5,M_6,M_{10},M_{12}	M_7,$M_8$$M_{11}$ M_{13}	M_9
15Δ:45Δ	50Δ:30Δ	15Δ:140Δ	20Δ:140Δ	12Δ:45Δ

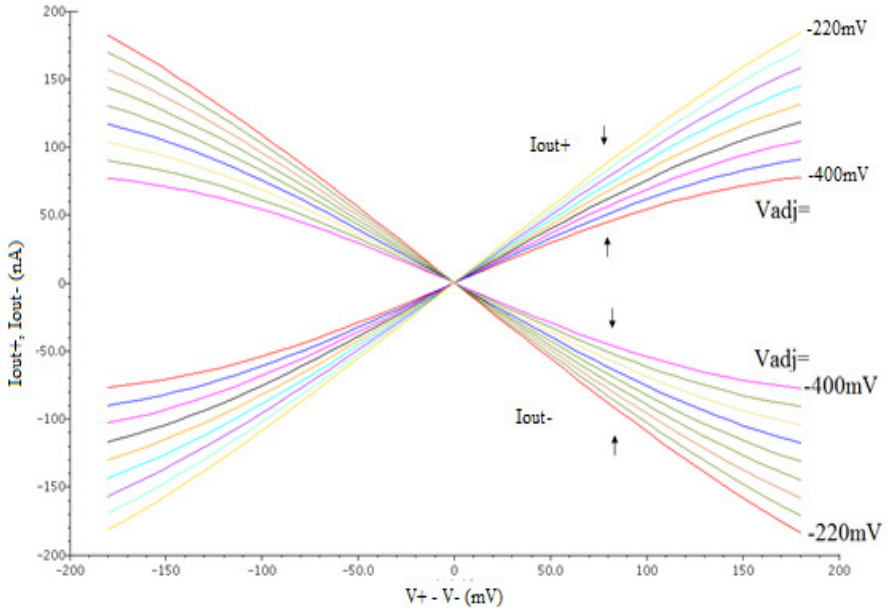


Fig4.2: I-V Characteristics of CMOS Linear Floating Resistor

Table 4.4: Resistance of CMOS Linear Floating Resistor at Different V_{adj}

V_{adj} (mV)	-220 (mV)	-240 (mV)	-260 (mV)	-280 (mV)	-300 (mV)	-320 (mV)	-340 (mV)	-360 (mV)	-380 (mV)	-400 (mV)
R(MΩ)	0.93	0.98	1.04	1.12	1.21	1.37	1.44	1.66	1.81	2.00

4.1.3 SIMULATION RESULTS OF MODIFIED CMOS LINEAR FLOATING RESISTOR

The modified CMOS floating resistor circuit shown in Fig.3.4 has been simulated using Cadence Spectre analog simulation environment with BSIM3v3 version 3.2 model parameters. The circuit is operated at supply voltages of ± 0.9V. The aspect ratios of the transistors are listed in Table 4.5. Fig. 4.3 shows the I-V characteristic of modified CMOS floating resistor. V− is fixed to ground, and V+ is scanned to achieve the voltage change across the circuit. The two groups of curves in this figure are the currents flowing into two different resistor terminals. With V_{adj} scanned from -380mV to -200mV, the simulated circuit presents a resistance from 0.87MΩ to 1.86MΩ in the linear working region. The resistances at different V_{adj} are provided in Table 4.6. The total power dissipation of the modified CMOS linear floating resistor is 7.58µW.

Table 4.5: Aspect Ratios of the Transistors used in Spectre Simulation. Δ = 0.2µm.

M_1, M_2	M_3,M_4	M_5,M_6,M_{10},M_{12}	M_7,$M_8$$M_{11}$ M_{13} M_7', M_8', M_{11}' M_{13}'	M_9
15Δ:45Δ	50Δ:30Δ	15Δ:140Δ	20Δ:140Δ	12Δ:45Δ

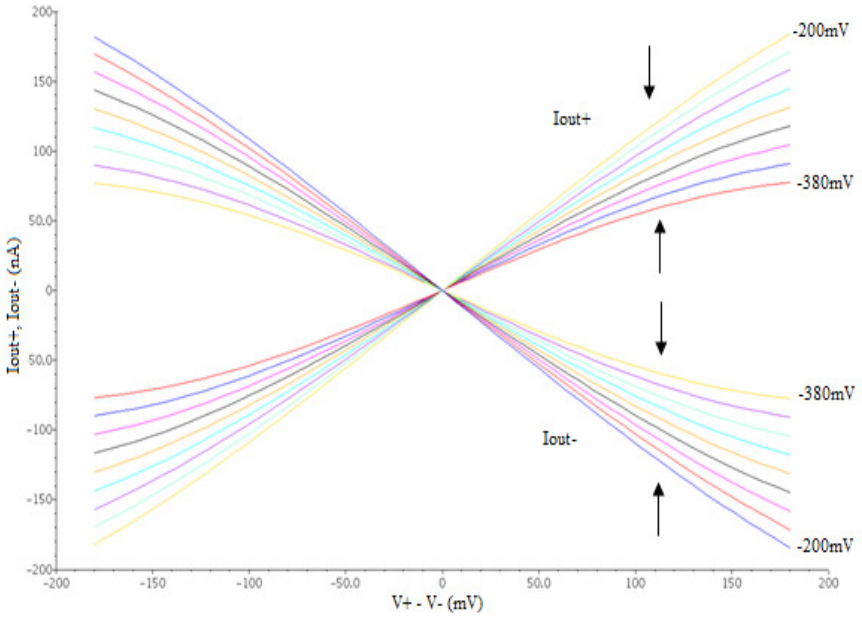


Fig. 4.3 I-V Characteristics of the Modified CMOS Linear Floating resistor

Table 4.6 Resistance of CMOS Linear Floating Resistor at Different V_{adj}

V_{adj} (mV)	-200 (mV)	-220 (mV)	-240 (mV)	-260 (mV)	-280 (mV)	-300 (mV)	-320 (mV)	-340 (mV)	-360 (mV)	-380 (mV)
R(MΩ)	0.87	0.92	0.97	1.04	1.12	1.21	1.32	1.46	1.63	1.86

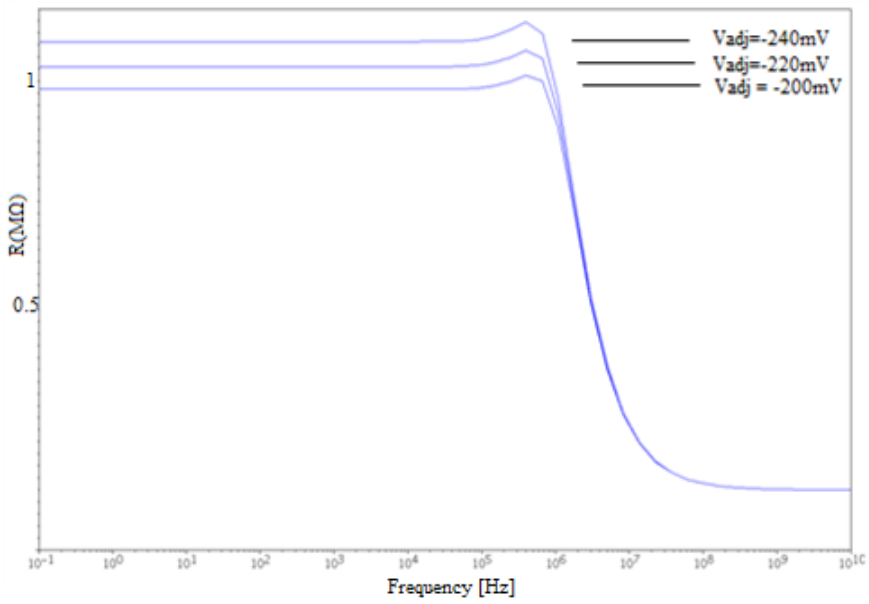


Fig 4.4: Frequency Response of the Modified CMOS Linear Floating Resistor

Fig. 4.4 shows the frequency response of the modified CMOS linear floating resistor. The DC components of the inputs are set to V+ = V− = 0V. An AC signal is applied at V+ and its magnitude is 0.1 V. All the curves in Fig.4.4 show an up-turn at around 1MHz. This can be caused by the parasitic capacitances C_{gd} of M_1 and M_2, which short high-frequency signals and consequently introduce a zero in the frequency response. By adjusting V_{adj} to I_{M9}, the transconductances of MOS devices M_1-M_4 are enlarged, so that the zero as well as the pole is slightly shifted to a higher frequency. This is shown in Fig. 4.4.

The simulation of CMOS floating Resistor described in section 4.1.2 ignores the body effect though it is included in the simulation. Since N-well technology is used in our simulation circuit, PMOS transistors can be in separate wells and their bodies can be tied to their sources to cancel the body effect. The bodies of NMOS transistors are all connected to V_{ss}. This introduces the body effect to the NMOS devices that are not sourced to V_{ss}, i.e. the two input transistors, and the upper part of the transistors that

compose cascode current mirrors. For the sake of clarity, Fig. 3.4 shows the NMOS transistors that are affected by the body effect, namely, M_7', M_8', M_{11}' and M_{13}'. The existence of the body effect helps to reduce the current mirror output current change caused by the channel-length modulation effect. Take M_8 and M_8' in Fig. 3.4 as an example, when the current mirror output V_a increases, the gate-source voltage of M8′ decreases, which leads to the enhancement of M_8' threshold voltage due to the body effect and consequently causes a larger gate-source voltage of M_8' This negative feedback on the gate-source voltage of M_8' helps to reduce the change on V_b, assuming V_c depends on M_7' only and is fixed, and, thus, assists to minimize the output current change. This reducing influence of the body effect on current mismatch is also applicable to PMOS cascode current mirrors. Therefore, to save layout areas, all PMOS transistors of cascode current mirrors can connect their bodies to Vdd to enable them sharing a single N-well. While the input transistors M_1 and M_2 are also influenced by the body effect, the changes on their threshold voltages are equal and cancel each other, because their sources are connected to the same point. Therefore, Eq. (3.13) is still satisfied, and the resistance of the floating resistor shown in Fig.3.4 remains expressed by Eq. (3.15).

4.2 PROCESS CORNER SIMULATION

After completing the schematic simulation at typical corner, it is necessary to check the circuit performance at every expected corner of the process variation.

Table 4.7: Process Corner Simulation Results of the CMOS Differential Pair Circuit

V_{adj} (mV)	SS corner		FF corner		FS corner		SF corner	
	I_{out+} (nA) at V_+=100mV	**I_{out+} (nA) at V_+= -100mV**	**I_{out+} (nA) at V_+=100mV**	**I_{out+} (nA) at V_+= -100 mV**	**I_{out+} (nA) at V_+=100mV**	**I_{out+} (nA) at V_+= -100 mV**	**I_{out+} (nA) at V_+=100mV**	**I_{out+} (nA) at V_+= -100 mV**
-200	92.633	-91.41	140.47	-138.8	123.0	-120.2	108.48	-106.77
-220	86.991	-85.91	133.73	-130.8	116.2	-114.3	102.39	-100.96
-240	81.098	-80.25	126.92	-124.2	110.1	-108.1	96.19	-94.49
-260	75.180	-74.46	120.02	-117.6	103.6	-101.8	89.90	-88.50
-280	69.177	-68.47	113.04	-110.9	97.01	-95.46	83.49	-82.58
-300	63.064	-62.47	105.96	-104.1	90.28	-88.91	76.98	-76.15
-320	56.856	-56.30	98.763	-97.10	83.44	-82.23	70.30	-69.55
-340	50.576	-50.04	91.442	-89.95	76.50	-75.40	63.51	-62.81
-360	44.269	-43.73	83.98	-82,64	69.44	-68.44	56.61	-55.94
-380	38.007	-37.47	76.37	-75.15	62.22	-61.35	49.65	-49.01

Tables 4.7, 4.8, and 4.9 shows the process corner simulation results of CMOS Differential Pair, CMOS floating resistor, and modified CMOS floating resistor, respectively.

Table 4.8: Process Corner Simulation Results of the CMOS Linear Floating Resistor

	SS corner		**FF corner**		**FS corner**		**SF corner**	
V_{adj} (mV)	**I_{out+} (nA) at V_+=100mV**	**I_{out+} (nA) at V_+= -100mV**	**I_{out+} (nA) at V_+=100mV**	**I_{out+} (nA) at V_+= -100 mV**	**I_{out+}(nA) at V_+=100mV**	**I_{out+} (nA) at V_+= -100 mV**	**I_{out+} (nA) at V_+=100mV**	**I_{out+} (nA) at V_+= -100 mV**
-220	82.84	-82.16	136.31	-136.07	121.83	-121.32	106.03	-106.78
-240	76.32	-75.18	129.71	-129.13	116.67	-117.22	99.62	-99.26
-260	70.71	-70.37	122.52	-122.49	110.67	-110.63	94.255	-94.96
-280	64.73	-64.32	114.28	-114.31	104.21	-103.9	87.794	-87.517
-300	60.69	-60.24	107.66	-107.01	97.357	-97.001	81.208	-80.935
-320	54.19	-53.86	103.23	-103.56	90.405	-90.111	74.488	-74.255
-340	48.33	-47.12	98.75	-98.31	83.348	-83.051	67.631	-67.359
-360	42.22	-41.03	83.806	-83.633	76.183	-75.884	60.652	-60.303
-380	35.76	-35.37	78.84	-78.477	68.915	-68.816	53.586	-53.321
-400	28.43	-28.02	72.96	-72.824	61.563	-61.273	46.496	-46.249

Table 4.9: Process Corner Simulation Results of the Modified CMOS Linear Floating Resistor

	SS corner		**FF corner**		**FS corner**		**SF corner**	
V_{adj} (mV)	**I_{out+} (nA) at V_+=100mV**	**I_{out+} (nA) at V_+= -100mV**	**I_{out+} (nA) at V_+=100mV**	**I_{out+} (nA) at V_+= -100 mV**	**I_{out+} (nA) at V_+=100mV**	**I_{out+} (nA) at V_+= -100 mV**	**I_{out+} (nA) at V_+=100mV**	**I_{out+} (nA) at V_+= -100 mV**
-200	85.62	-85.23	148.31	-148.07	125.83	-125.32	109.03	-108.78
-220	79.48	-79.16	141.01	-140.13	117.67	-117.22	102.62	-101.26
-240	73.66	-73.38	133.65	-133.49	110.67	-110.63	94.255	-93.96
-260	67.74	-67.48	126.61	-126.31	104.21	-103.9	87.794	-87.517
-280	61.73	-61.48	119.28	-119.01	97.357	-97.001	81.208	-80.935
-300	55.69	-55.40	111.86	-115.56	90.405	-90.111	74.488	-74.255
-320	49.19	-49.26	104.31	-104.31	83.348	-83.051	67.631	-67.359
-340	43.33	-43.10	96.63	-96.633	76.183	-75.884	60.652	-60.303
-360	37.22	-37.01	88.806	-88.477	68.915	-68.816	53.586	-53.321
-380	31.76	-31.07	80.824	-80.824	61.563	-61.273	46.496	-46.249

4.3 LAYOUT DESIGN

4.3.1 LAYOUT DESIGN OF CMOS DIFFERENTIAL PAIR CIRCUIT

The layout of the CMOS Differential Pair Circuit has been designed using Virtuoso Layout Editor shown in Fig. 4.5. The Design Rule Check (DRC) and Layout versus Schematic (LVS) and Parasitic Extraction (RCX) of this circuit has also been performed. The extracted view of the CMOS Differential Pair Circuit is shown in Fig. 4.6. The circuit extraction has been performed after the layout design is completed, in order to create a detailed netlist (or circuit description) for the LVS and the simulation tool. The circuit extractor is capable of identifying the individual transistors and their interconnections (on various layers), as well as (usually) the parasitic resistances and capacitances that are inevitably present between these layers. Thus, the "extracted netlist" can provide a very accurate estimation of the actual device dimensions and device parasitics that ultimately determine the circuit performance. The extracted netlist file and parameters are subsequently used in Layout-versus-Parasitic Extraction (RCX).

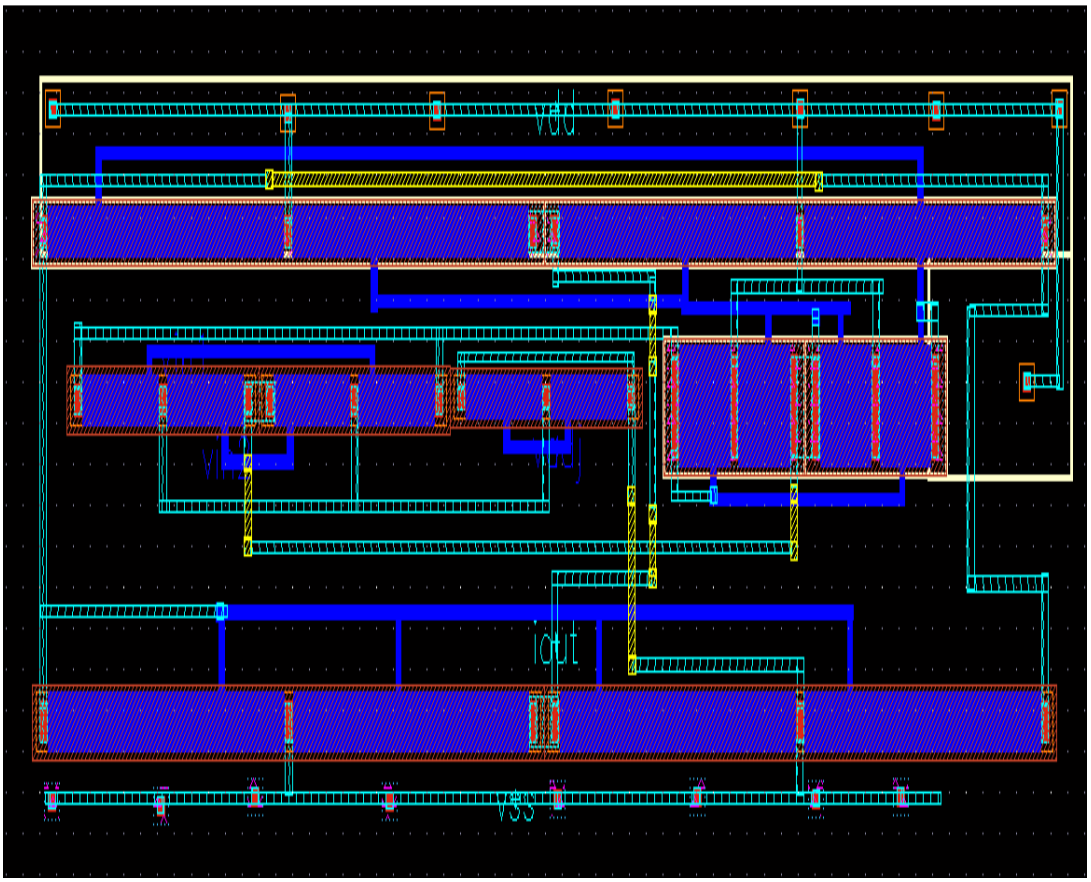


Fig. 4.5: Layout of the CMOS Differential Pair Circuit

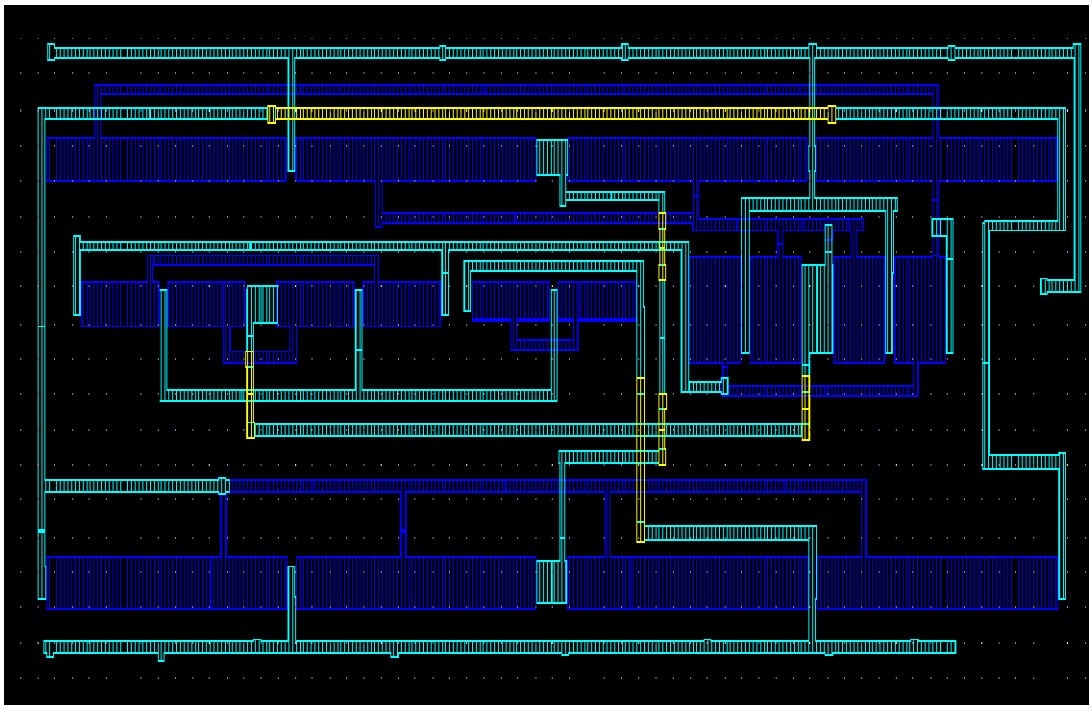


Fig 4.6: Extracted View of the CMOS Differential Pair Circuit

4.3.2 LAYOUT DESIGN OF CMOS LINEAR FLOATING RESISTOR

The layout and extracted view of CMOS floating resistor are shown in Figs.4.7 and 4.8, respectively.

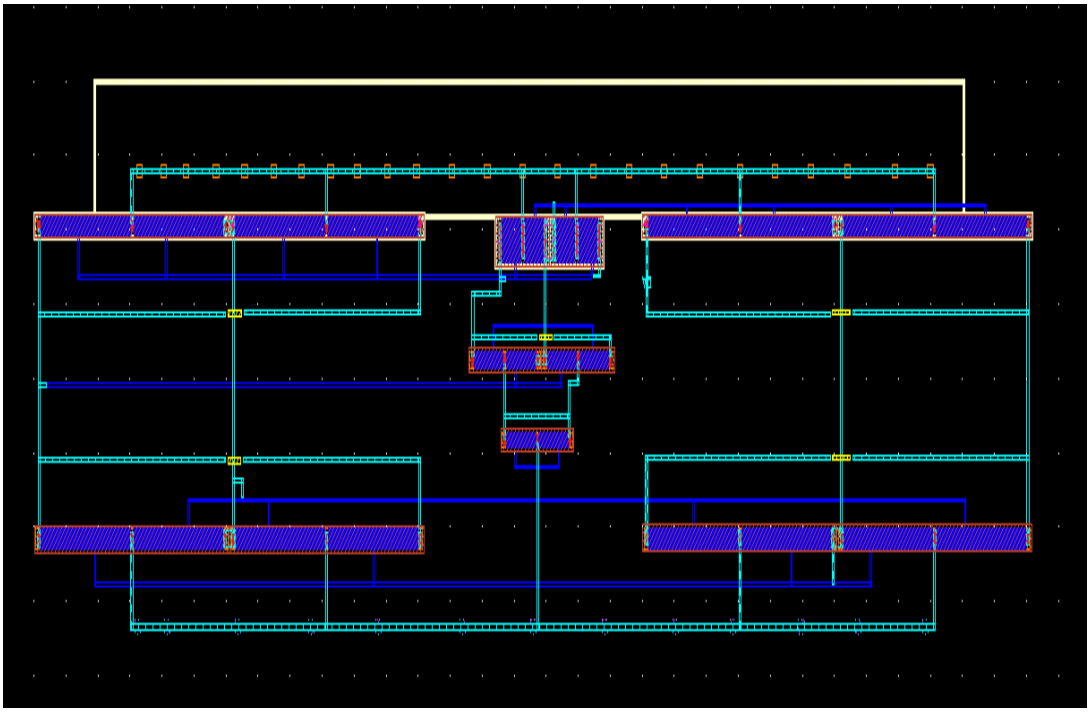


Fig4.7: Layout of the CMOS Linear Floating Resistor

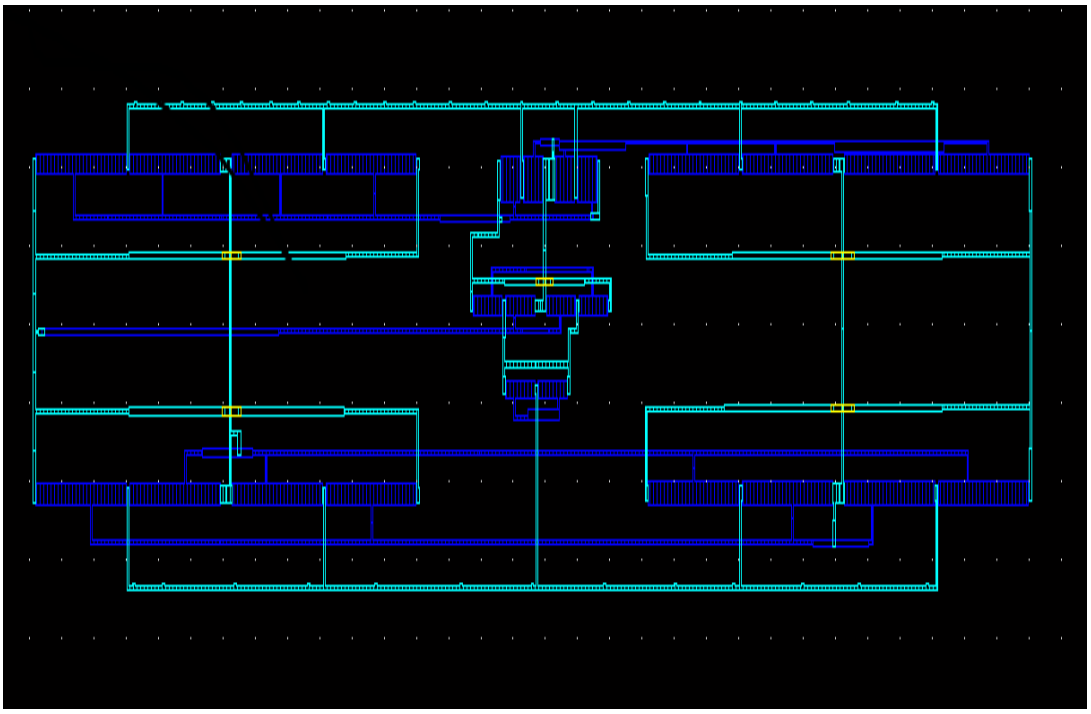


Fig.4.8: Extracted View of the CMOS Linear Floating Resistor

4.3.3 LAYOUT DESIGN OF MODIFIED CMOS LINEAR FLOATING RESISTOR

The layout and extracted view of modified CMOS floating resistor are shown in Figs.4.9 and 4.10, respectively.

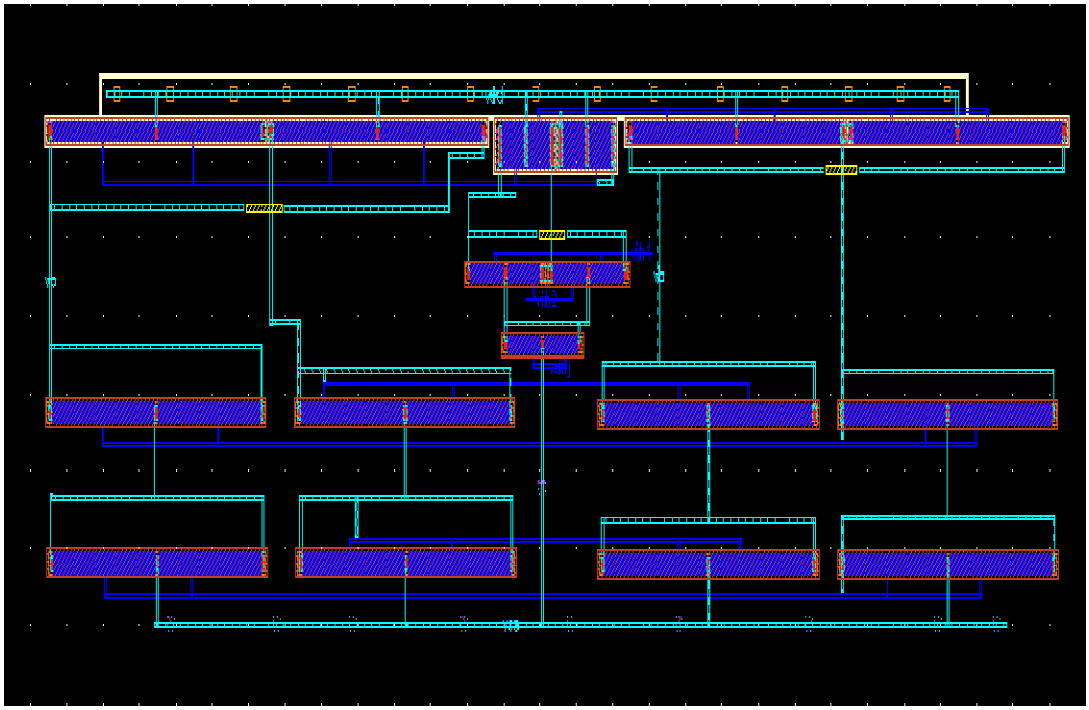


Fig.4.9: Layout of the Modified CMOS Linear Floating Resistor

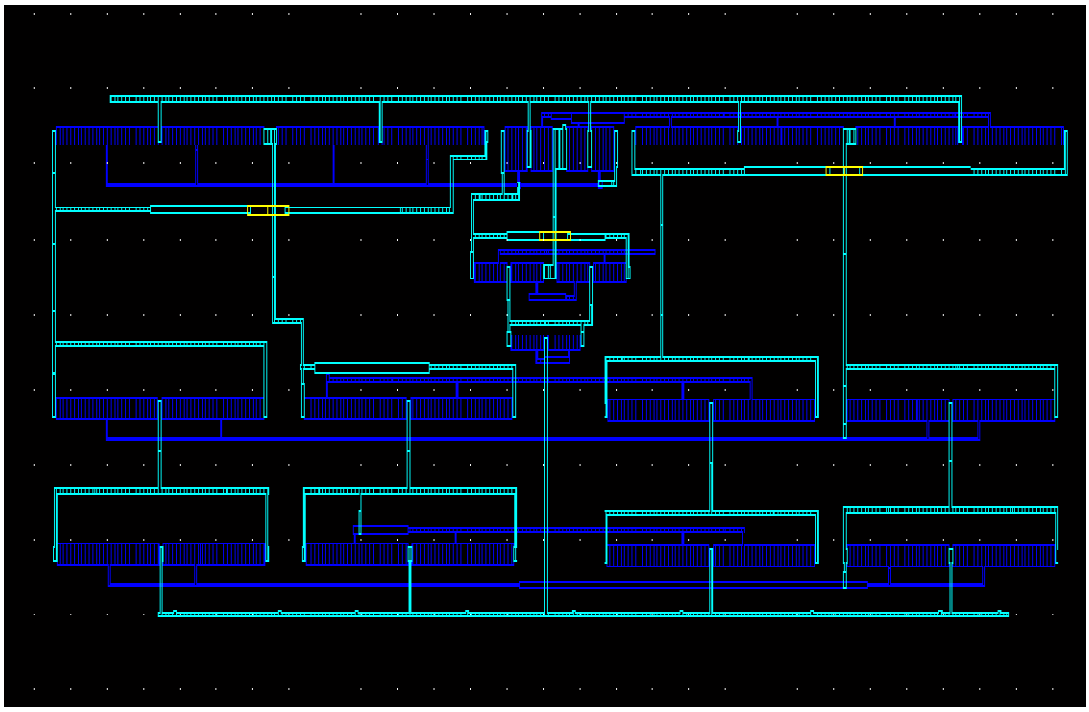


Fig.4.10: Extracted View of the Modified CMOS Linear Floating Resistor

4. 4 POST LAYOUT SIMULATION RESULTS

4.4.1 SIMULATION RESULTS OF CMOS DIFFERENTIAL PAIR CIRCUIT

The post layout simulation has been done using extracted netlist. The I-V characteristics of the CMOS differential pair circuit is shown in Fig.4.11.

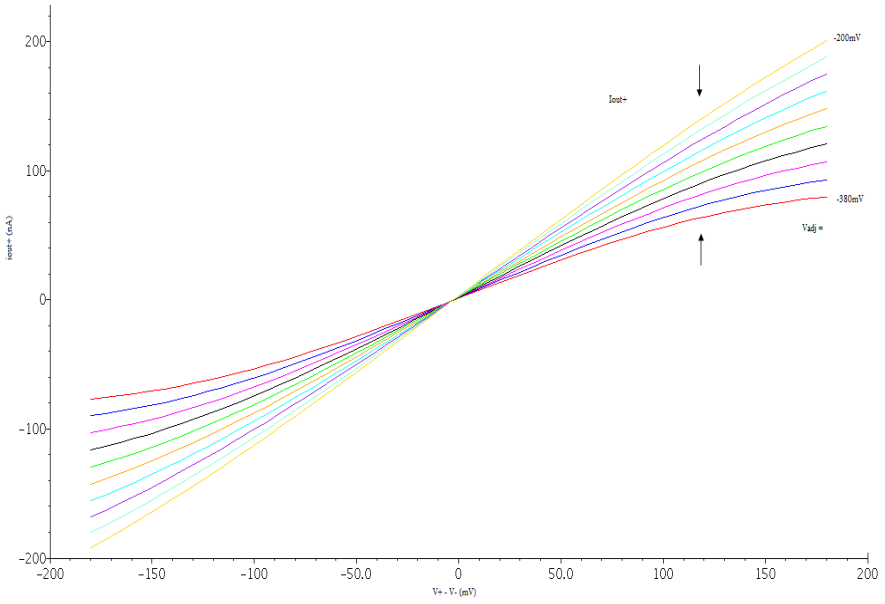


Fig.4.11: I-V Characteristics of the CMOS Differential Pair Circuit

for the various values of adjusted voltage (V_{adj}) varies from -380mV to -200mV with the increment of 20mV. V_- is fixed to ground and V_+ is scanned to achieve the voltage change across the circuit. The V_+ is varied from -180mV to 180mV with the increment of 10mV.

4.4.2 SIMULATION RESULTS OF CMOS LINEAR FLOATING RESISTOR

The I-V characteristic of CMOS linear floating resistor is shown in Fig. 4.12. V– is fixed to ground, and V+ is scanned to achieve the voltage change across the circuit. The two groups of curves in this figure are the currents flowing into two different resistor terminals. With V_{adj} scanned from -400mV to -220mV, the simulated circuit presents a resistance from 0.93 MΩ to 2.0 MΩ in the linear working region.

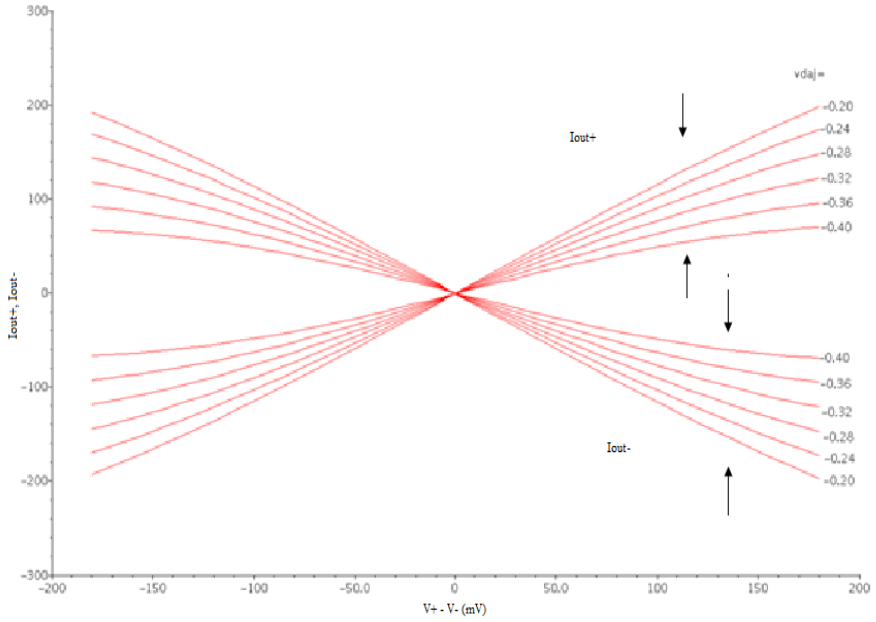


Fig4.12: I-V Characteristics of CMOS Linear Floating Resistor Circuit

4.4.3 SIMULATION RESULTS OF MODIFIED CMOS LINEAR FLOATING RESISTOR

The I-V characteristic of modified CMOS linear floating resistor is shown in Fig. 4.13. V– is fixed to ground, and V+ is scanned to achieve the voltage change across the circuit. The two groups of curves in this figure are the currents flowing into two different resistor terminals. With V_{adj} scanned from -380mV to -200mV, the simulated circuit presents a resistance from 0.87 MΩ to 1.86 MΩ in the linear working region.

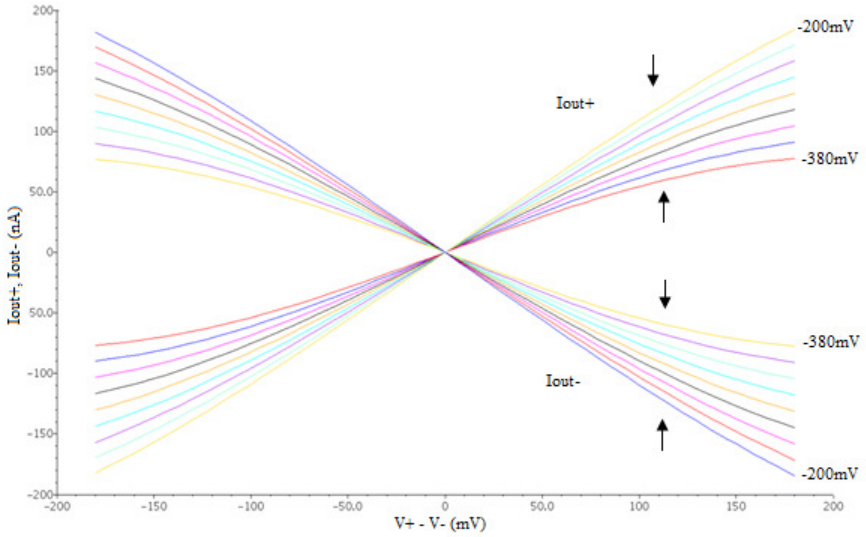
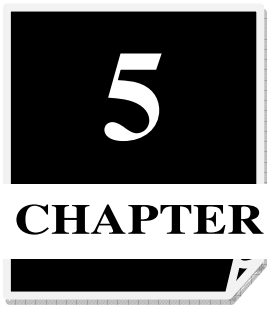


Fig.4.13: Post-Simulation I-V Characteristics of the Modified CMOS Linear Floating Resistor



CONCLUSIONS

A scheme of making a transconductance-based floating resistor has been presented. The introduced transconductor circuit has a simple topology and can be configured to work as either a positive or negative floating resistor. The circuit is suitable for low voltage/low power analog signal processing applications. The circuit is designed in the basis to be independent of the MOS parameters and temperature. These qualifications allow the practical implementation of an accurate resistor simulator, with a resistance value independent from the process parameters and approximately constant over a wide temperature range. Spectre simulation show that the presented floating resistor offers a variation of its resistance around (0.87MΩ - 1.86MΩ) for an input range is (±0.1V) using (±0.9V) power supply and can be adjusted with the gate voltage of a current source MOS transistor. The analysis of the body effect shows that the body has little influence on the presented floating resistor. To save layout areas, all PMOS transistors of cascode current mirror can connect their bodies to V_{dd} to enable them sharing a single N-well.

APPENDIX A

SPICE BSIM3v3 VERSION 3.2 MOS MODEL PARAMETERS

The typical parameters are listed below:

NMOSFET MODEL PARAMETERS

model bsim_mos_transistor_mos bsim3v3 type=n

version=3.2	binunit=1	mobmod=1
capmod=2	nqsmod=0	noimod=2
tox=4.2e-09 + dtox_n_18_rf	toxm=4.2e-09	xj=1.6e-07
nch=3.745e+17	rsh=8	ngate=1e+23
vth0=0.3075 + dvth0_n_18_rf	k1=0.4578	k2=-0.02638
k3=-10.88	k3b=0.2379	w0=-8.813e-08
nlx=4.279e-07	dvt0=0.4042	dvt1=0.3237
dvt2=-0.8602	dvt0w=0.383	dvt1w=6e+05
dvt2w=-0.025	lint=1.587e-08	wint=1.022e-08
dwg=-3.396e-09	dwb=1.346e-09	u0=332.1 du0_n_18_rf
ua=-1.17e-09	ub=2.407e-18	uc=4.355e-11
vsat=8.1e+04	a0=1.93	ags=0.5072
b0=1.486e-06	b1=9.064e-06	keta=0.01752
a1=0	a2=1	voff=-0.1208
nfactor=1.038	cit=-0.001511	cdsc=0.002175
cdscd=0	cdscb=0.0008241	eta0=0.005504
etab=-0.001459	dsub=0.001592	pclm=0.741
pdiblc1=0.005061	pdiblc2=0.006001	pdiblcb=0
drout=0.001592	pscbe1=4.866e+08	pscbe2=3e-08
pvag=-0.2958	rdsw=9.905	prwg=1.1
prwb=0	wr=p_wr	alpha0=0
alpha1=0	beta0=30	xpart=1
cgso=1.55e-10 *(1+dcgso_n_18_rf)	cgdo=1.55e-10 *(1+dcgdo_n_18_rf)	cgbo=0
cgsl=3e-11*(1+dcgsl_n_18_rf)	cgdl=3e-11 *(1+dcgdl_n_18_rf)	ckappa=0.6
cf=2.33e-11 *(1+dcf_n_18_rf)	clc=1e-07	cle=0.6
dlc=4e-08	dwc=0	vfbcv=-1
noff=1	voffcv=0	acde=1
moin=15	noia=1.31826e+19	noib=1.44544e+05
noic=-1.24516e-12	em=4.1e+07	af=1

ef=0.92	kf=0	lmin=1.8e-07
lmax=1.805e-07	wmin=5e-06	wmax=1.05e-04
xl=-1.05e-08 + dxl_n_18_rf	xw=0 + dxw_n_18_rf	js=1e-06
jsw=7e-11	cj=0.00103 *(1+dcj_n_18_rf)	mj=0.443
pb=0.813	cjsw=1.34e-10 *(1+dcjsw_n_18_rf)	mjsw=0.33
tnom=25	ute=-1.286	kt1=-0.2255
kt1l=-4.175e-09	kt2=-0.02527	ua1=2.153e-09
ub1=-2.673e-18	uc1=-3.832e-11	at=1.449e+04
prt=-46.18	xti=3	wl=0
wln=1	ww=7.262e-16	wwn=1
wwl=0	ll=-1.062e-15	lln=1
lw=2.996e-15	lwn=1	lwl=0
llc=-6.64e-15	lwc=0	lwlc=0
wlc=0	wwc=0	wwlc=0
lvth0=-0.0001 + dlvth0_n_18_rf	wvth0=0.06027 + dwvth0_n_18_rf	pvth0=0 dpvth0_n_18_rf
lnlx=-2.854e-08	wnlx=0	pnlx=0
lnfactor=0.032	wua=-1.88e-11	wu0=0.54
pub=3.8e-20	pw0=1.3e-09	lua=1.5e-11
lub=9.76e-20	wrdsw=0	weta0=0
wetab=0	leta0=0.001574	letab=0
peta0=0	petab=0	wpclm=0
wvoff=-0.0004078	lvoff=-0.004208	pvoff=-0.0003788
wa0=-0.04731	la0=-0.4667	pa0=-0.02649
wags=0.004242	lags=0.3028	pags=0
wketa=0	lketa=-0.01942	pketa=0
wute=0.06373	lute=0	pute=0
wvsat=5066	lvsat=0	pvsat=0 dpvsat_n_18_rf
lpdiblc2=-0.004752	wat=7067	wprt=0
ldif=8e-08	hdif=2.6e-07	n=1
pbsw=0.88	cjswg=5e-10 *(1+dcjgate_n_18_rf)	ctp=0.000914
ptp=0.000924	cta=0.000919	pta=0.00158
elm=5	tlevc=1	

PMOSFET MODEL PARAMETERS

model bsim_mos_transistor_mos bsim3v3 type=p

mobmod=3	version=3.2	capmod=2
binunit=1	nqsmod=0	noimod=2
tox=4.2e-09 + dtox_p_18_rf	toxm=4.2e-09	xj=1e-07
nch=6.131e+17	ngate=1e+23	vth0=-0.4325 dvth0_p_18_rf
k1=0.5704	k2=0.006973	k3=-2.833
k3b=1.326	w0=-1.943e-07	nlx=2.56e-07
dvt0=0.4885	dvt1=0.09578	dvt2=0.1287
dvt0w=-0.1261	dvt1w=2.479e+04	dvt2w=0.6915

lint=-1.041e-08 wint=-1.525e-07 dwg=-1.151e-07
dwb=-1.039e-07 u0=90+du0_p_18_rf ua=1.49e-09
ub=4.646e-19 uc=-0.09587 vsat=4.75e+04
a0=1.35 ags=0.3818 b0=-3.088e-07
b1=0 keta=0.01044 a1=0
a2=1 voff=-0.1073 nfactor=0.984
cit=-0.001067 cdsc=0.0007578 cdscd=0
cdscb=0.0001 eta0=1.071 etab=-0.9291
dsub=1.919 pclm=0.553 pdiblc1=0.007
pdiblc2=0.008005 pdiblcb=0 drout=0.157
pscbe1=4.866e+08 pscbe2=2.8e-07 pvag=-0.888
rdsw=202.1 prwg=1.2 prwb=0
wr=p_wr alpha0=0 alpha1=0
beta0=30 cgdo=1.254e-10 *(1+dcgdo_p_18_rf) cgbo=0
cgso=1.254e-10 *(1+dcgso_p_18_rf) xpart=0 cf=1.533e-10*(1+dcf_p_18_rf)
dlc=7.01e-08 cgsl=2e-11*(1+dcgsl_p_18_rf) cgdl=2e-11*(1+dcgdl_p_18_rf)
ckappa=0.6 clc=1e-07 cle=0.6
dwc=2.3e-07 vfbcv=-1 noff=1
voffcv=0 acde=1 moin=15
noia=3.57456993317604e+18 noib=2.5e+03 noic=2.6126e-11
em=4.1e+07 af=1 ef=1.1388
kf=0 lmin=1.8e-07 lmax=1.805e-07
wmin=5e-06 wmax=1.05e-04 xl=-2e-09
dxl_p_18_rf
xw=0 + dxw_p_18_rf js=3e-06 jsw=4.12e-11
cj=0.00114*(1+dcj_p_18_rf) mj=0.395 pb=0.762
cjsw=1.74e-10 *(1+dcjsw_p_18_rf) mjsw=0.324 tnom=25
ute=-0.4484 kt1=-0.2194 kt1l=-8.204e-09
kt2=-0.009487 ua1=4.571e-09 ub1=-6.026e-18
uc1=-0.0985 at=1.203e+04 prt=0
xti=3 ww=1.236e-14 lw=-2.873e-16
ll=6.635e-15 wl=0 wln=1
wwn=1 wwl=0 lln=1
lwn=1 lwl=0 llc=-1.31e-14
lwc=0 lwlc=0 wlc=0
wwc=0 wwlc=0 lvth0=0.0057
dlvth0_p_18_rf
wvth0=-0.0148 + dwvth0_p_18_rf lu0=-3 lnfactor=0.03
pvth0=0.0031+ dpvth0_p_18_rf lnlx=-1.584e-08 wrdsw=10.07
weta0=0 wetab=0 wpclm=0
wua=2.7e-09 lua=-2.37e-10 pua=5.855e-11
wub=0 lub=0 pub=0
wuc=0 luc=0 puc=0

wvoff=-0.009816 lvoff=-0.0009871 pvoff=-9.833e-05
wa0=-0.04807 la0=-0.281 pa0=0.08661
wags=-0.04177 lags=0.04454 pags=-0.04076
wketa=0 lketa=-0.012 pketa=0
wute=-0.2682 lute=0 pute=0
wvsat=-1.42e+04 lvsat=0 pvsat=-350
dpvsat_p_18_rf
lpdiblc2=0.003012 wat=-6405 wprt=216.6
n=1 pbsw=0.665 cta=0.001
ctp=0.000753 pta=0.00155 ptp=0.00124
ldif=8e-08 rsh=8 rd=0
rsc=0 rdc=0 hdif=2.6e-07
rs=0

The variations in the values of the parameters for different corners are given below:

NOTE: In **CADENCE** following notations are used for corners:

tt : typical NMOS and typical PMOS

ff : fast NMOS and fast PMOS

ss : slow NMOS and slow PMOS

fnsp : fast NMOS and slow PMOS

snfp : slow NMOS and fast PMOS

SECTION tt

dcd_n_18_rf=0
dcgs_n_18_rf=0
drgate_n_18_rf=0
dtox_n_18_rf=0.0000e+00
dxl_n_18_rf=0.0000e+00
dxw_n_18_rf=0.0000e+00
dvth0_n_18_rf=0.0000e+00
du0_n_18_rf=0.0000e+00
dlvth0_n_18_rf=0.0000e+00
dwvth0_n_18_rf=0.0000e+00
dwu0_n_18_rf=0.0000e+00
dpvth0_n_18_rf=0.0000e+00
dpvsat_n_18_rf=0.0000e+00
dcf_n_18_rf=0.0000e+00
dcgdo_n_18_rf=0.0000e+00
dcgdl_n_18_rf=0.0000e+00
dcgso_n_18_rf=0.0000e+00
dcgsl_n_18_rf=0.0000e+00
dcj_n_18_rf=0.0000e+00
dcjsw_n_18_rf=0.0000e+00
dcjgate_n_18_rf=0.0000e+00
dcd_p_18_rf=0
dcgs_p_18_rf=0

drgate_p_18_rf=0
dcgdl_p_18_rf=0.0000e+00
dcgsl_p_18_rf=0.0000e+00
dcf_p_18_rf=0.0000e+00
dtox_p_18_rf=0.0000e+00
du0_p_18_rf=0.0000e+00
dxl_p_18_rf=0.0000e+00
dxw_p_18_rf=0.0000e+00
dvth0_p_18_rf=0.0000e+00
dlvth0_p_18_rf=0.0000e+00
dwvth0_p_18_rf=0.0000e+00
dpvth0_p_18_rf=0.0000e+00
dpvsat_p_18_rf=0.0000e+00
dcgdo_p_18_rf=0.0000e+00
dcgso_p_18_rf=0.0000e+00
dcj_p_18_rf=0.0000e+00
dcjsw_p_18_rf=0.0000e+00
dcjgate_p_18_rf=0.0000e+00

SECTION ss

dcd_n_18_rf=0.1
dcgs_n_18_rf=0.15
drgate_n_18_rf=0.35
dtox_n_18_rf=1.0000e-10
dxl_n_18_rf=2.2000e-08
dxw_n_18_rf=-2.0000e-08
dvth0_n_18_rf=1.4500e-02
du0_n_18_rf=-1.0000e+01
dlvth0_n_18_rf=1.4000e-03
dwvth0_n_18_rf=1.1000e-02
dwu0_n_18_rf=-4.5000e+00
dpvth0_n_18_rf=-1.0000e-03
dpvsat_n_18_rf=1.4000e+02
dcgdo_n_18_rf=-0.1
dcgso_n_18_rf=-0.1
dcgdl_n_18_rf=-0.1
dcgsl_n_18_rf=-0.1
dcf_n_18_rf=0.15
dcj_n_18_rf=0.1
dcjsw_n_18_rf=0.1
dcjgate_n_18_rf=0.1
dcd_p_18_rf=0.1
dcgs_p_18_rf=0.15
drgate_p_18_rf=0.35
dcgdl_p_18_rf=-0.1
dcgsl_p_18_rf=-0.1
dcf_p_18_rf=0.15
dtox_p_18_rf=1.0000e-10

du0_p_18_rf=-0.0e+00
dxl_p_18_rf=1.0000e-08
dxw_p_18_rf=-2.0000e-08
dvth0_p_18_rf=-1.4000e-02
dlvth0_p_18_rf=0.0000e-00
dwvth0_p_18_rf=-1.0000e-02
dpvth0_p_18_rf=3.0000e-04
dpvsat_p_18_rf=4.6000e+01
dcgdo_p_18_rf=-0.1
dcgso_p_18_rf=-0.1
dcj_p_18_rf=0.1
dcjsw_p_18_rf=0.1
dcjgate_p_18_rf=0.1

SECTION ff

dcd_n_18_rf=-0.1
dcgs_n_18_rf=-0.15
drgate_n_18_rf=-0.35
dtox_n_18_rf=-1.0000e-10
dxl_n_18_rf=-1.3600e-08
dxw_n_18_rf=2.0000e-08
dvth0_n_18_rf=-1.4500e-02
du0_n_18_rf=1.0000e+01
dlvth0_n_18_rf=-7.0000e-04
dwvth0_n_18_rf=-1.0100e-02
dwu0_n_18_rf=2.0000e+00
dpvth0_n_18_rf=6.5000e-04
dpvsat_n_18_rf=-8.0000e+01
dcgdo_n_18_rf=0.1
dcgso_n_18_rf=0.1
dcgdl_n_18_rf=0.1
dcgsl_n_18_rf=0.1
dcf_n_18_rf=-0.15
dcj_n_18_rf=-0.1
dcjsw_n_18_rf=-0.1
dcjgate_n_18_rf=-0.1
dcd_p_18_rf=-0.1
dcgs_p_18_rf=-0.15
drgate_p_18_rf=-0.35
dcgdl_p_18_rf=0.1
dcgsl_p_18_rf=0.1
dcf_p_18_rf=-0.15
dtox_p_18_rf=-1.0000e-10
du0_p_18_rf=0
dxl_p_18_rf=-8.0000e-09
dxw_p_18_rf=1.5000e-08
dvth0_p_18_rf=1.8000e-02
dlvth0_p_18_rf=-1.0000e-03

dwvth0_p_18_rf=8.5000e-03
dpvth0_p_18_rf=1.0000e-05
dpvsat_p_18_rf=-2.1000e+01
dcgdo_p_18_rf=0.1
dcgso_p_18_rf=0.1
dcj_p_18_rf=-0.1
dcjsw_p_18_rf=-0.1
dcjgate_p_18_rf=-0.1

SECTION snfp

dcd_n_18_rf=0.05
dcgs_n_18_rf=0.075
drgate_n_18_rf=0.175
dtox_n_18_rf=0.0000e+00
dxl_n_18_rf=1.1000e-08
dxw_n_18_rf=-1.0000e-08
dvth0_n_18_rf=1.3000e-02
du0_n_18_rf=-5.0000e+00
dlvth0_n_18_rf=1.1000e-03
dwvth0_n_18_rf=4.7000e-03
dwu0_n_18_rf=-2.0000e+00
dpvth0_n_18_rf=-5.5000e-04
dpvsat_n_18_rf=6.0000e+01
dcgdo_n_18_rf=0.0000e+00
dcgso_n_18_rf=0.0000e+00
dcgdl_n_18_rf=0.0000e+00
dcgsl_n_18_rf=0.0000e+00
dcf_n_18_rf=0.075
dcj_n_18_rf=0.05
dcjsw_n_18_rf=0.05
dcjgate_n_18_rf=0.05
dcd_p_18_rf=-0.05
dcgs_p_18_rf=-0.075
drgate_p_18_rf=-0.175
dcgdl_p_18_rf=0
dcgsl_p_18_rf=0
dcf_p_18_rf=-0.075
dtox_p_18_rf=0.0000e+00
du0_p_18_rf=0
dxl_p_18_rf=-4.0000e-09
dxw_p_18_rf=1.0000e-08
dvth0_p_18_rf=1.7000e-02
dlvth0_p_18_rf=-3.0000e-04
dwvth0_p_18_rf=3.5000e-03
dpvth0_p_18_rf=9.0000e-05
dpvsat_p_18_rf=-3.0000e+01
dcgdo_p_18_rf=0.0000e+00
dcgso_p_18_rf=0.0000e+00
dcj_p_18_rf=-0.05

dcjsw_p_18_rf=-0.05
dcjgate_p_18_rf=-0.05

SECTION fnsp

dcd_n_18_rf=-0.05
dcgs_n_18_rf=-0.075
drgate_n_18_rf=-0.175
dtox_n_18_rf=0.0000e+00
dxl_n_18_rf=-9.5000e-09
dxw_n_18_rf=1.0000e-08
du0_n_18_rf=6.0000e+00
dvth0_n_18_rf=-1.2300e-02
dlvth0_n_18_rf=-7.0000e-04
dwvth0_n_18_rf=-4.6000e-03
dwu0_n_18_rf=1.7000e+00
dpvth0_n_18_rf=4.1000e-04
dpvsat_n_18_rf=-7.0000e+01
dcgdo_n_18_rf=0.0000e+00
dcgso_n_18_rf=0.0000e+00
dcgdl_n_18_rf=0.0000e+00
dcgsl_n_18_rf=0.0000e+00
dcf_n_18_rf=-0.075
dcj_n_18_rf=-0.05
dcjsw_n_18_rf=-0.05
dcjgate_n_18_rf=-0.05
dcd_p_18_rf=0.05
dcgs_p_18_rf=0.075
drgate_p_18_rf=0.175
dcgdl_p_18_rf=0
dcgsl_p_18_rf=0
dcf_p_18_rf=0.075
dtox_p_18_rf=0.0000e+00
dxl_p_18_rf=4.5000e-09
dxw_p_18_rf=-1.0000e-08
dvth0_p_18_rf=-1.3000e-02
du0_p_18_rf=0
dlvth0_p_18_rf=-3.0000e-04
dwvth0_p_18_rf=-5.0000e-03
dpvth0_p_18_rf=1.3000e-04
dpvsat_p_18_rf=3.4000e+01
dcgdo_p_18_rf=0.0000e+00
dcgso_p_18_rf=0.0000e+00
dcj_p_18_rf=0.05
dcjsw_p_18_rf=0.05
dcjgate_p_18_rf=0.05

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