PERFORMANCE ANALYSIS OF MIXED CNT BUNDLE AS VLSI INTERCONNECTS

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DECLARATION

I hereby declare that the work which is being presented in this thesis entitled **"Performance analysis of Mixed CNT Bundle as VLSI Interconnects"** in partial fulfillment of requirements for the award of the degree of Masters of Technology in VLSI Design from Thapar University, Patiala is an authentic record of my own work carried out during the period from July 2013 to June 2014 under the supervision of Dr. Mayank Kumar Rai (Asst. Professor).

The matter embodied in this thesis work has not been submitted anywhere else for the award of any degree.

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ABSTRACT

Performance of a VLSI circuit is strongly influenced by Interconnect delay. As technology scaled down, interconnects delay dominates the gate delay. The present VLSI interconnect material i.e. copper (Cu) is facing various problems such as electro migration, surface scattering and grain boundary scattering as the technology is scaled down. These problems are severe and degrade the performance of Cu interconnect. Due to these reasons there is dire need for an alternative material to Cu interconnects which can perform better than it. Carbon nanotubes (CNTs) are one of the proposed alternatives to Cu interconnect which are susceptible to problems encountered due to technology scaling. Also they offer high thermal conductivity and large current carrying capacity over Cu. In this dissertation, temperature dependent performance analysis of mixed CNT bundle as a VLSI interconnect has been analyzed. The temperature dependent circuit parameters and performance analysis in terms of delay, power dissipation and power delay product (PDP) of mixed carbon nanotube (CNT) bundle interconnect with two different structures (MCB1 and MCB2) have been analyzed using an improved temperature dependent resistance model of single walled CNT (SWCNT) at 22nm technology. A similar analysis is carried out for single walled CNT (SWCNT) and multi walled CNT (MWCNT) bundle with conventional metal (copper) conductors and comparisons are made between results obtained through these analyses at 22nm technology node over a temperature range from 300K to 500K. The effects of various parameters such as interconnect length, diameter on propagation delay, power and PDP have also been analyzed. The SPICE simulation results reveal that at temperature variation ranging from 300 K to 500K, compared to bundle of SWCNT and MWCNT with copper interconnects, power delay product (PDP) in mixed CNT bundle of structure2 (MCB2), is low. Simulated results further reveal that with rise in temperature, MCB1 and MCB2 with tube diameter of d_{SWCNT}=0.7nm and d_{MWCNT}=2nm, perform better in terms of delay compared to other viz. SWCNT bundle, MWCNT bundle and copper. Based on these comparative results, an improved structure of mixed CNT bundle has been proposed as a better alternative to bundled SWCNT and MWCNT.

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LIST OF SYMBOLS

VDD	Positive supply voltage
h	Planck's Constant
d	Tube diameter
y	ILD Thickness
x	Separation between centres of two neighbouring tubes
w	Width of interconnect
h	Height of Interconnet
L	Length of Interconnect
C_{OX}	Oxide capacitance
λ	Mean Free Path
λ_{eff}	Effective Mean Free Path
ε_{ox}	Oxide permittivity
t_{ox}	Oxide thickness
μ	Permeability
n_h	Number of rows in SWCNT bundle
n_w	Number of columns in SWCNT bundle
n_{CNT}	Number of CNTs in SWCNT bundle
ρ	Resistivity of Cu
d_{max}	Outermost shell diameter of MWCNT
d_{min}	Innermost shell diameter of MWCNT
K_B	Boltzmann constant
λ_{AC}	Acoustic MFP
λ_{OP}	Effective optical MFP
$\lambda_{OP,abs}$	Effective optical MFP due to scattering by absorption

$\lambda_{OP,ems}$	Effective optical MFP due to scattering by emission
N_{OZ}	Optical phonon zone boundary occupation
N_{OP}	Optical phonon occupation
R'_{t-ESC}	Fundamental resistance of CNT bundle considered as ESC
R'_{ESC}	Scattering Resistance of CNT bundle considered as ESC
L'_{K-ESC}	Kinetic inductance of CNT bundle considered as ESC
L'_{e-ESC}	Magnetic inductance of CNT bundle considered as ESC
C_{q-ESC}	Quantum capacitance of CNT bundle considered as ESC
C_{e-ESC}	Electrostatic capacitance of CNT bundle considered as ESC

ABBREVIATIONS

VLSI	Very Large Scale Integration
CNT	Carbon Nanotube
IC	Integrated Circuit
ITRS	International Technology Road map for semiconductors
RLC	Resistance, Inductance and Capacitance
SWCNT	Single Wall Carbon Nanotube
MWCNT	Multi Wall Carbon Nanotube
MCB	Mixed Carbon Nanotube Bundle
SPICE	Simulation Program with Integrated Circuit Emphasis
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
MFP	Mean Free Path
PDP	Power Delay Product
ESC	Equivalent Single Conductor

CHAPTER - 1

INTERCONNECTS

1.1 Introduction

A thin film of conducting material used to provide electrical connection between two or more nodes of a circuit/system formed in the silicon chip is termed as VLSI interconnect. This interconnection is used to provide power supply, clock, and ground supply to a device and also to provide the output of one device to another device. The interconnection line which is itself a three dimensional structure should have a non-negligible resistance and capacitance. But this is not the case. As the devices are scaling down, delay caused by interconnect has become a very important factor. So it is important to realize an accurate equivalent circuit model for interconnects, so that an accurate analysis of delay caused by interconnects can be done and accordingly the best performing material can be chosen as interconnect for VLSI applications.

1.2 Types of Interconnects

There are basically three types of interconnects: local, intermediate and global interconnects. Local interconnects consist of very thin lines and are usually used to connect gates and transistors within a functional block. They usually span only a few gates and occupy first and, sometimes, second metal layers. Intermediate interconnects are used to provide clock and to distribute signal within a functional block. These are designed slightly wider and taller than local interconnects to provide lower resistance (as resistance decreases when area increases). Global interconnects are used to provide clock and signal distribution between the functional blocks and to deliver power/ground to all functional blocks. Global interconnects occupy the top one or two layers, and they are as long as half the chip perimeter. It is mandatory that low-resistivity global interconnects should be used because as the bias voltage decreases and the total current consumption of the chip increases. Also it is very important to have very less propagation delay in case of interconnects especially in case of global interconnects as they are larger in length and also as these are used to provide clock , so clock skew can occur if they have large propagation delay. Global interconnects should also have small resistance so that voltage level of power supply has not been dropped.

1.3 Problems in existing VLSI interconnects

As feature size is reducing continuously, die size has been increased. Due to this reason, length of some of the on chip interconnects has been increased as technology is scaled down. Earlier the most commonly used material for interconnects was aluminum. The reason to choose aluminum was its good conductivity and adherence on silicon dioxide. It also forms a good ohmic contact with silicon. Due to increase in device density with technology scaling, interconnect current density increased. At high current densities, aluminum suffers from electro migration. Electro migration is caused by the movement of atoms in a metallic conductor which is induced by the passage of a direct current. Its magnitude is proportional to the mobility and the current density [1]. Electro migration results in damages e.g. open or shorts in the line, local heating and stress concentration. Later copper was introduced as an alternative to aluminum, having higher conductivity and is several times more resistant to electro migration than aluminum. With equal reliability for IC-applications, copper can also withstand about five times more current density than aluminum. Melting point of copper is also higher than aluminum which provides thermal stability to copper. Because of these various advantages, copper became the preferred interconnect material for submicron and deep submicron high density, high performance chips. As the technology is further scaled down, interconnect of copper for global signal is facing serious performance degradation. This is because of increase in the resistivity of copper (Cu) due to electron surface scattering and grain boundary scattering [2]. As the dimensions are reduced rapidly, they become comparable to mean free path of electrons in copper (~ 40 nm at room temperature), resulting in scattering from the interface which cannot be neglected. Due to surface scattering, resistivity of copper increases [2]. Another problem with copper interconnect is grain boundary scattering. Grain boundaries are defined as the interfaces in a polycrystalline structure where crystals of different orientation meet. The grain boundaries basically contain dislocation and impurities. As the grain size is reduced, electron scattering increases which results in the reduction of mobility and increase in resistivity [2]. Another effect of dimension scaling is increase in current density of copper. Thus as technology scales, propagation delay increases due to the increase in resistance of the Cu interconnect. Besides increase in delay, power dissipation of interconnect also increases due to increase in current density and increase in frequency of operation. The rise in power dissipation also causes increase in heating which results in electro migration. As these limitations of copper interconnect is technology dependent and are going to be more and more severe for the future generation of VLSI chips, so it is time to look for an alternative material. To

abate this problem, alternative solutions are under consideration for interconnects of future generation chips.

1.4 Future materials for VLSI interconnects

Various materials have been discussed in literature to replace of Cu as interconnect. Some of which are: Carbon nanotubes, Graphene nano ribbons and optical interconnects. Optical interconnects refers to the medium of data transmission in which the data signal is transmitted as an optical carrier modulated wave (light) through an optically transparent media such as optical fibre, planar optical waveguide or air. Carbon nanotubes consist of a single atomic layer of graphene which is rolled up to form a cylindrical shape, has been proposed as a future VLSI interconnects. CNTs are attractive interconnect materials because they have high thermal conductivity (5800W/mK), and high thermal and mechanical stability, and also have the ability to carry current in excess of 10^{14}A/m^{2} current density even at temperatures higher than 200°C and Fermi velocity comparable with that of a metal [3]. Graphene nano ribbons (GNRs) have been recently proposed as one of the potential candidates for both transistors and interconnects. Similar to the carbon nanotubes (CNTs), GNRs can also be either semiconducting or metallic, depending on the geometry, Compared to Cu, both GNRs and CNTs have large carrier mean free path (MFP), and also have the ability to conduct much larger current densities. But CNT has been chosen over GNR because of two reasons. Firstly, GNRs have a problem of edge scattering, due to which effective MFP reduces, while CNTs have no such issue. Secondly, while mono-layer graphene has large MFP and conductivity, multi-layer graphene turns to graphite and has much lower conductivity per layer due to inter-sheet electron hopping [4].

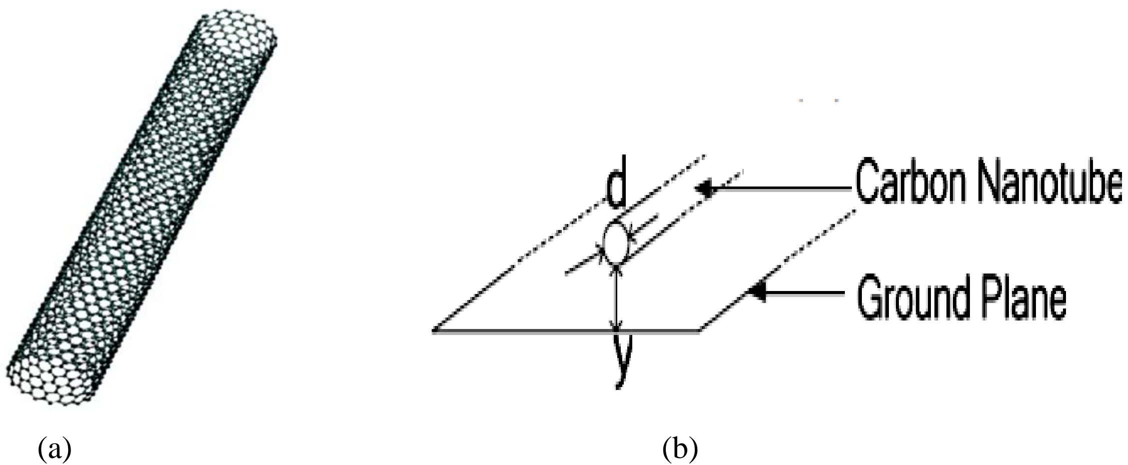
1.5 Carbon Nanotubes

The Carbon Nanotubes are seamless cylinders made from one atomic layer of (graphene), having diameters of the order of a nanometer. There are basically three types of CNTs. Single walled CNT (SWCNT) and Multi walled CNT (MWCNT) and Mixed CNT. CNTs formed by only one thin wall of graphene sheet are SWCNTs.The CNTs which consist of a multiple of concentric SWCNT like graphene tubes, are termed MWCNT. Mixed CNTs are mixture of both structures SWCNTs and MWCNTs. Carbon Nanotubes can be either metallic or semiconductor depending on the direction in which CNTs are rolled up (chirality), giving rise to zigzag (mostly semiconducting), armchair (metallic), or chiral nanotubes (mostly semiconducting). For interconnect applications, the metallic

ones are useful. MWCNTs are found to be mostly metallic, whereas a large fraction of CNTs in a SWCNT bundle are semiconducting. The metallic CNTs are attractive interconnect materials because of their high thermal and mechanical stability, thermal conductivity and high current density [3]. But a good contact formation is difficult with CNT and this unavoidable contact imperfection increases resistance. CNT resistance is reported to be in the range 7 KΩ - 100 KΩ [5]. Such a high resistance is a major disadvantage; if an isolated CNT is used as interconnect. Due to this reason, CNTs are always used in bundles in which CNTs are arranged in parallel to each other. This arrangement reduces the resistance between the ends of CNT bundle.

1.5.1 Single Walled Carbon Nanotubes

An isolated SWCNT consists of one atomic layer of graphene is shown in Fig. 1.1(a) and on ground plane is shown in Fig.1.1 (b). There are 4 parallel conducting channel in SWCNT (N=4) due to spin and sub lattice degeneracy of electrons [5]. The one dimensional equivalent circuit diagram of SWCNT is shown in Fig. 1.2.



(a) (b)

Figure 1.1(a) SWCNT structure.(b) SWCNT, with diameter 'd', over ground plane at a distance 'y' below it.[6].

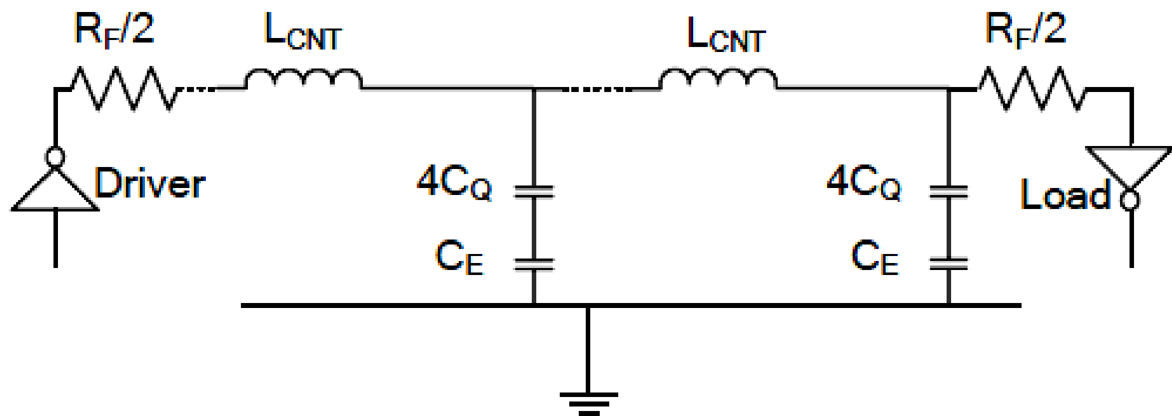


Figure 1.2 One dimensional Equivalent circuit diagram for an isolated SWCNT, length less than the mean free path of electrons, assuming ideal contacts [5].

R_F is the fundamental resistance associated with SWCNT, which is divided by two at both the ends; L_{CNT} is the total inductance associated with SWCNT which consists of magnetic inductance and kinetic inductance. The magnetic inductance is due to the total magnetic energy resulting from the current flowing in the wire. Kinetic inductance arises from kinetic energy stored in each conducting channel of the CNT, so total kinetic inductance is divided by 4. C_E is the electrostatic capacitance between the CNT and the ground plane. C_Q is the quantum capacitance of the channel, as there are 4 channels in single SWCNT, so it will be multiplied by 4.As the resistance of SWCNT is very high, it cannot be used alone and is always used in bundles. There are three types of bundles: flat CNT array, dense CNT bundle and sparse CNT bundle as shown in Fig. 1.3.

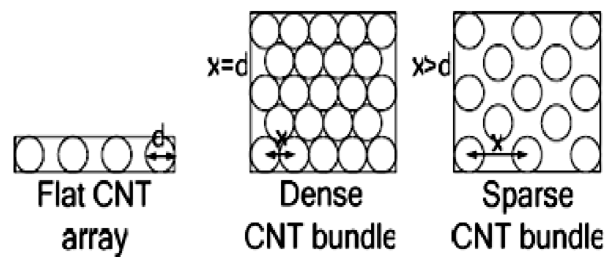


Figure 1.3 Flat CNT array and CNT bundles with varying density of metallic CNTs [6].

Performance of CNT bundle interconnects is much better than flat arrays. Present fabrication techniques cannot ensure all CNTs in a bundle are metallic. Presence of semi-conducting CNTs (considered to be insulating [7]) and varying density of metallic CNTs are modeled using inter-CNT

distance, *x.* A CNT-bundle interconnect is assumed to be comprised of hexagonally packed similar metallic SWCNTs. Every CNT is surrounded by six immediate neighbors and their centers are uniformly separated by a distance ‘x’. The densely packed structure with ‘x’=‘d’ (CNT diameter), shown in Fig. 1.3, will lead to best interconnect performance [6]. In reality, all CNTs of a bundle are not metallic. Non-metallic CNTs do not contribute to current conduction and their presence is taken into account by considering sparsely populated bundles as shown in Fig. 1.3.

1.5.2. Multi Walled Carbon Nanotubes

Multi walled CNT contains concentric SWCNTs. While SWCNTs can be either metallic or semiconducting depending on their chirality, MWCNTs are always metallic. Also, MWCNTs have almost same current carrying capacity as metallic SWCNTs but their fabrication is easier than SWCNTs due to easier control of the growth process. However, SWCNTs can be modeled more easily than MWCNTs due to its simple structure. On the other hand, analysis and design of MWCNT interconnect is bit difficult due to the complex structure formed by a large number of concentric tubes. A multiwall CNT structure is shown in the Fig. 1.4 [8]. Here D_{max} is the outermost diameter of MWCNT and D_{min} is the innermost diameter of MWCNT. H is the height above ground plane and d is the vanderwall gap.

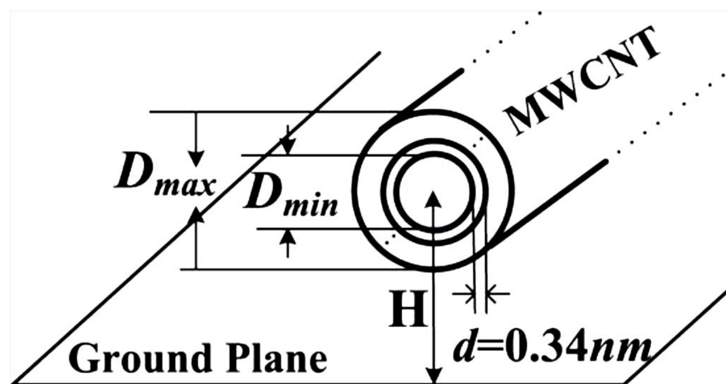


Figure 1.4 Geometry of an MWCNT on a ground plane [8].

For analytical purpose equivalent circuit model for MWCNT is shown in Fig. 1.5. [8]. Firstly, the impedance parameters viz. resistance, inductance and capacitance of each shell is calculated and then the equivalent impedance parameters of MWCNT are calculated using the model given in Fig. 1.5 [8].

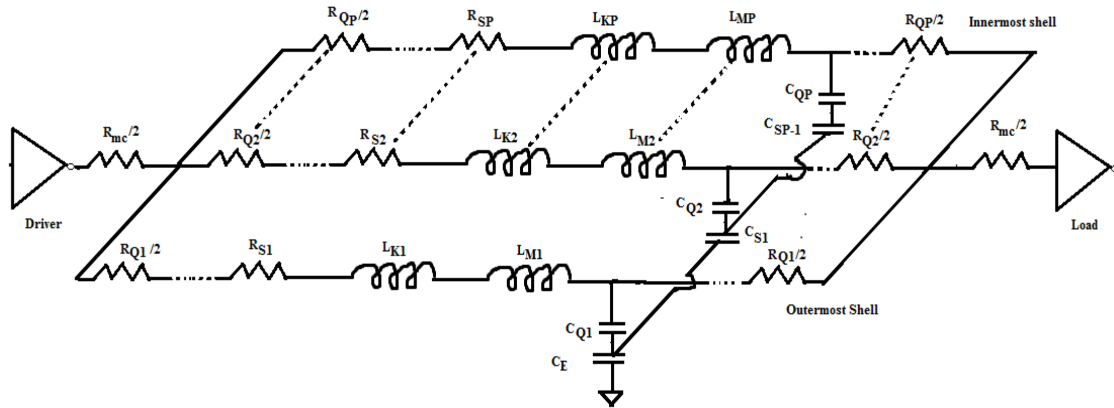


Figure 1.5. Equivalent distributed circuit model of an MWCNT with p shells [8].

In Fig. 1.5 R_{mc} is lumped imperfect contact resistance and R_Q is the lumped quantum resistance per shell, R_S is distributed scattering resistance which is present when the length of CNT becomes greater than mean free path of CNT, L_K is kinetic inductance, L_M is magnetic inductance , M is mutual inductance, and C_Q is quantum capacitance per shell. Only the outermost shell has electrostatic capacitance C_E with the ground. The shell-to-shell capacitance C_S only have $p - 1$ distributed components for the entire MWCNT.

1.5.3 Mixed Bundle Carbon Nanotubes

Most existing studies are focused on the SWCNT, as they show more desirable material properties than MWCNTs. To reduce the effect of intrinsic ballistic resistance present in single SWCNT, bundles of SWCNTs in parallel are more in favor. However, the CNT bundles are generally a mixture of both SWCNTs and MWCNTs called as Mixed CNT Bundle (MCB). Experimental results [9-11] demonstrate that a realistic nanotube bundle is a mixed bundle of single- and multi-wall CNTs. The structure for mixed CNT is shown in Fig.1.6.

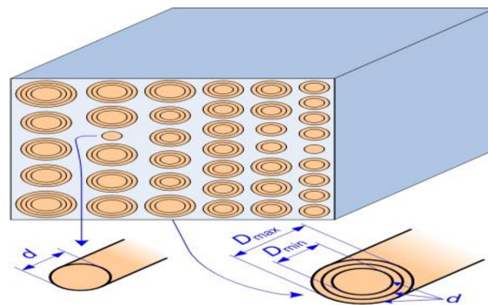


Figure 1.6 A CNT mixed-bundle consists of SWCNTs with a diameter *d* and MWCNTs with shells of various diameters d ($D_{min} \leq d \leq D_{max}$) [12].

Other structures of mixed CNT have been proposed by earlier studies [13] and new hierarchical model has been developed to do the complicated analysis of mixed CNT bundle by developing equivalent single conductor (ESC) models for the structures of bundled SWCNT and MWCNT interconnects. The detail analysis of these structures will be done in the next chapters.

1.6 Conclusion

In this chapter various problems associated with present VLSI interconnects have been discussed and an overview of CNT is presented, which are proposed as an alternative to Cu interconnect. Different types of CNT and their equivalent circuit models have been discussed which are used to calculate the equivalent impedance parameters of each type of CNT. Once the impedance parameters are calculated, propagation delay of interconnect can be estimated using either lumped or distributed model. As MCB contains both SWCNT which offers low resistance and MWCNT which offers low capacitance, hence it may perform better as interconnect than both the CNTs and can be a better alternative to copper interconnect for global signals.

CHAPTER – 2

LITERATURE REVIEW

2.1 Introduction

Several works on the recent researches and developments in the field of CNT as VLSI interconnects has been reported [14]-[54]. A succinct review based on the study of these papers is presented here. Initially in the reported works, the equivalent model of various CNTs has been derived. Various impedance parameters are calculated for the accurate estimation of propagation delay and compared with the propagation delay of Cu interconnects at deep sub micron technology nodes. Dependence of various parameters such as effect of diameter, length and distance between tubes has been studied on propagation delay and power dissipation. Some of earlier studies have also been discussed about the crosstalk effect in CNT interconnects. Some of them have also proposed structures for CNTs which can give better performance as interconnect. Further, a few studies have also reported the dependence of temperature on the impedance parameters and hence on the performance of SWCNT bundle interconnects.

2.2 SWCNT Bundle as VLSI Interconnects

P. J. Burke, 2002. [5] proposed a technique to directly excite Luttinger liquid collective modes in CNT at gigahertz frequency. He calculated the magnetic and kinetic inductance, fundamental resistance, electrostatic and quantum capacitance by modeling the nanotubes as a transmission line using ref. [42]. He described a model for CNT using the concept of interacting electrons in one dimension. First he calculated the impedance parameters considering the spinless electrons. Then he compared the wave velocity for interacting electrons versus non-interacting electrons. He has also discusses two types of modes of channels in 1-D quantum wire- charge and spin mode.

A Naeemi, et al., **2004[43]** have discussed the model for CNT and also have derived the formulae for the propagation delay of CNT and Cu interconnect. They have shown that for all practical lengths, a single level of nanotubes above a ground plane has latency larger than that of a copper wire because of its very small wave propagation speed. A bundle of nanotubes, however, has a smaller latency especially for long lengths. This, they have also proved mathematically. They have

also discussed that initially ideal CNT become disordered once they are physisorbed on a surface. As a result electron mean free path in real carbon nanotubes is finite. Electron-phonon scattering that is dominant in copper wires is inelastic. In contrast, electron-defect scattering, which is the major scattering mechanism in CNT is elastic because of which electron waves in nanotubes do not loose their phase coherency. The incident electron wave and reflected waves therefore interfere and resistance increases exponentially with length. They have also told that there is a critical length beyond which the resistance of the carbon naotube bundle becomes larger than Cu wire and have also derived a formula for it. They have also shown that the performance enhancement in CNT is a function of length. They have also shown that the performance enhancement increases with increase in the electron mean free path. It is also shown that the maximum performance enhancement that can be achieved using nanotube bundles is proportional to the product of reciprocal driver resistance and resistance of copper interconnect whose length is equal to the mean free path of electrons in CNT.

Naeemi and J. D. Meindl 2005 [44] have discussed that for shorter interconnects the driver resistance is very high than interconnect resistance. So it is a dominant factor for the propagation delay. So to reduce the propagation delay it is must to decrease the interconnect capacitance. They have also shown that for the monolayer carbon nanotubes on a thick dielectric layer have capacitance 2 times smaller than Cu wire. So it can be used as a shorter interconnect, as at that level driver resistance is quite dominant and latency is determined by capacitance. They have also shown that this is true only for carbon nanotube on thick dielectric layer not for thin dielectric layer and also not true for CNT bundle which has large capacitance as compared to Cu wire. They have also told that as in CNT electrons can only move in one dimension so phase space for scattering is very limited, therefore they have large mean free path. They have also told that for large bias voltage electron back scattering effect is predominant and hence mean free path is less. They have also told that advantage of monolayer carbon nanotubes smaller capacitance can be taken if the driver size should be low because as aspect ratio is increased, driver resistance is decreased and become comparable with bundle resistance and hence in this case dealy for Cu wires will be less.

Srivastava, N. and Banerjee, K., 2005[6] analyzed the applicability of CNT for VLSI interconnects. As high resistance CNT cannot be used isolated, so they discussed the bundle concept for CNT and developed an equivalent model for CNT bundle. They discussed the type of

arrangements in bundles of SWCNT and also derived the formulae to calculate the number of CNT in the bundle for best performance. Then they calculated resistance, capacitance and inductance for CNT bundle. They also compare the performance of the CNT bundle with copper interconnects. They have shown that for local interconnects the resistance of CNT is higher than Cu if contacts are not perfect. On the other hand, if the contacts are perfect, resistance is much less than Cu interconnects (with maximum densely packed CNT bundles). They have also conducted the experiment to compare the propagation delay of Cu and CNT which shows that for densely packed bundles, propagation delay of local interconnects is higher than that with Cu wires across all technology generations even if contacts are perfect. They have given the reason of higher resistance of minimum sized drivers and capacitance of CNT bundle of local interconnects for this. They observed that the performance of CNT bundles with perfect contacts becomes better than Cu wires if the distance between adjacent metallic CNTs forming a bundle is increased. However, with realistic imperfect contacts the delay is still higher than Cu wires. This interesting result shows that slightly lower metallic CNT density improves local interconnect performance which counters the expectation in previously reported works of them [44]. They have also told there that it is very difficult to achieve the maximum packing density for CNTs [44], and these lower densities may be more easily achievable. A small decrease in CNT density improves local interconnects performance as it reduces the capacitance of the bundle without increasing resistance too much. They have shown with the help of the experiment that there exists an optimal point where optimum performance can be achieved with the CNT bundle. They also pointed to the fact that, if the imperfect contact resistance is held constant, a reduction in CNT density may not lead to the same improvement in performance as technology scales. They have shown that for intermediate and global interconnects, the performance of CNT-bundle interconnects is better than copper wires and improving with technology scaling even if the contacts are imperfect because at this length Cu resistance becomes very high.

M. K. Rai and S. Sarkar, 2011[45] have discussed the influence of tube diameter of the SWCNT on the impedance parameters of the SWCNT interconnect and also shown the effect of change in diameter on the propagation delay and power consumption. In this paper, first they have discussed the equivalent model of SWCNT and shown mathematically the dependence of impedance parameters on the diameter of the carbon nanotube. They have also shown the effect of technology scaling on resistance of CNT and Cu interconnects is shown that the resistance of CNT increases

much slowly than the copper interconnects with technology scaling because of surfacing in Cu interconnects. They have shown that the resistance and inductance of CNT increases with increase in diameter for a particular length and larger length has larger resistance whereas capacitance has shown the opposite behavior i.e. it decreases with increase in diameter. So diameter will also affect the propagation delay which is shown by them that there is an optimized value of the diameter of the tube for a particular technology for which the propagation delay with respect to the copper interconnect will be minimum. They have also shown the influence of the diameter of tube on the relative power consumption ($power_{CNT}$ / $power_{Cu}$) which decreases with increase in diameter and technology scaling. It is also shown that for a particular technology as diameter increases the relative power also decreases but still the power consumption of SWCNT is more than that of Copper interconnect. They have shown that tube diameter can control SWCNT-interconnect delay and this can also be utilized to improve power dissipation in SWCNT interconnect. For low-power, tubes of larger diameters are preferable whereas for higher speed either an optimum diameter (if available), else a lower diameter should be chosen. If both low power and high speed are the requirements then a compromise may be made between the two.

Mayank Kumar Rai, Nivedita and Sankar Sarkar, 2011[46] have reviewed the work carried out to explore the applicability of CNT as future VLSI interconnects. In this paper they have described the equivalent model of SWCNT and SWCNT bundle and derived the formulae for impedance parameters. They have compared the performance of CNT bundle with Cu interconnects and it is shown that for a densed bundle for interconnect length less than 1.6µm, the propagation delay is worse than Cu interconnects and it degrades with technology scaling, but in case of sparse bundle performance of CNT interconnect is better. They have shown that with increase in pitch for local interconnects delay increases, whereas for semi global and global interconnects the propagation delay is decreased by a large amount with respect to copper and relative delay become constant for global interconnects. They have also shown that the in semi global or global levels relative to copper, CNT performance improves with advancement of technology node. They have also reported that pitch influences semi global and global relative performance of CNT, so to achieve best performance of CNT interconnects, the pitch should be reduced as much as possible.

2.3. MWCNT Bundle as VLSI interconnects

Hong Li, Wen-Yan Yin, Kaustav Banerjee, and Jun-Fa Mao, 2008 [8] have considered MWCNTs. They have done a detailed investigation of MWCNT-based interconnect performance. They have presented a compact equivalent circuit model of MWCNTs for the first time, and evaluated the performance of MWCNT interconnects and compared it against traditional Cu interconnects, as well as SWCNT based interconnects, at different interconnect levels (local, intermediate, and global) for future technology nodes. They have discussed that MWCNT are mostly metallic in nature and if they are semiconducting, even then the difference between the conduction band and Fermi energy level is very small which can be easily overcome by the environment temperature. They have also discussed that multiple shells in an MWCNT can contribute to conductance if proper end contacts can be made and can also exhibit conductance values comparable to SWCNT. They have discussed about [47]-[49] in which properly contacted MWCNTs have been implemented to achieve low resistance with the contribution of inner shells. They have calculated the number of channels in a MWCNT and also derived the formulae for impedance parameters by obtaining an equivalent circuit model for MWCNT. Here they have discussed that in contrast to SWCNT, MWCNT exhibit mutual inductance and coupling capacitance. They have compared MWCNT, SWCNT, and Cu interconnects their equivalent resistivity in order to comprehend the intrinsic differences between them. For SWCNT bundles, they have considered them to be densely packed but for two cases: one in which all the CNTs in the bundle are metallic, and other in which CNTs in the bundle have random chiralities, which implies that only 1/3 of CNTs are metallic and contribute to conductance. They observed that for long lengths ($l > 10\ \mu m$), the resisitivity of MWCNTs could be several times lower than that of Cu wire and becomes increasingly comparable to that of SWCNT bundles. For global interconnects they observed that the delay of MWCNT interconnects is smaller than that of Cu interconnects and that the improvement in delay performance in the case of MWCNT interconnects increases for longer lengths. They have also shown that the normalized tunneling conductivity value has minor impact on the performance enhancement. They observed that the delay ratio increases with increasing wire width (i.e., the performance enhancement of MWCNT interconnect decreases).However, if the width of global interconnect is increased; the diameter of MWCNTs could also be increased accordingly. For intermediate interconnects they have also observed better performance in terms of delay of MWCNT than Cu interconnects. For short local interconnects, they have shown that the delay of MWCNT interconnects is marginally larger

than that of Cu .When compared to SWCNT bundles, they observed if SWCNTs can be densely packed and have high (near 100%) metallic fraction, MWCNT interconnects do not exhibit any evident advantages. However, in the case of SWCNT bundles with random chiralities (or low density), MWCNT interconnects can outperform SWCNT bundles, even at long lengths. Therefore, they have concluded that since MWCNTs are easier to fabricate with less concern about chirality and density control, they can be attractive for immediate use as horizontal wires in VLSI, including local, intermediate, and global level interconnects.

2.3. Mixed CNT Bundle as VLSI Interconnects

Tafseer Alam et al. 2011[50] have calculated the capacitance for mixed CNT bundle by first calculating the number of CNTs in the bundle (MWCNT and SWCNT). Then they observed the effect of diameter of CNT on capacitance which shows that with increase in diameter bundle capacitance increases but beyond a certain point capacitance starts decreasing. They have told that because beyond this point (3.8 nm), CNTs in bundle come closer to each other. However, the number of tubes in bundle remains constant which leads to decrease in capacitance. They have also shown that total capacitance of CNT bundle decreases when inner to outer diameter ratio is increased. If inner to outer diameter ratio is increased, then number of shell will decrease. Due to this, number of channel per shell will also decrease. Subsequently, the capacitance of bundle will decrease. They have also observed the capacitance with respect to the probability of metallic tubes in the bundle. With increase in probability, capacitance increases because the number of channels per shell increases. They have also compared the capacitance of mixed CNT bundle with Cu interconnects. For all types of interconnect capacitance of mixed CNT is smaller than capacitance of Cu interconnects. They have concluded that the reduction in CNT bundle capacitance increases with downscaling. Therefore, mixed CNT bundle is a prospective alternative to Cu for Intermediate and global interconnects for very deep sub micron technology nodes.

Nisarg D. Pandya et al. [13] have proposed the two structures for the mixed CNTs. One in which all the tubes which conduct maximum current are placed at centre of the bundle(structure 1) and the second structure in which all the tubes which conduct least or no current are at middle of mixed bundle(structure 2). They have calculated the impedance parameters for individual CNT and then they have derived an equivalent model for the mixed CNT bundle describing all impedance parameters.

They have also derived the formula for coupling capacitance. They have observed the propagation delay under the influence of dynamic crosstalk for opposite transition at two adjacent (aggressor and victim) lines. Crosstalk delays are evaluated for different global interconnect lengths at fixed transition time and spacing (between aggressor and victim). They have observed that the propagation delay for structure 1 is more as compared to structure 2 at different global interconnect lengths. However, power dissipation for structure 2 is more than structure 1. On the other hand, propagation delay under the influence of dynamic crosstalk is demonstrated for two different MCB (mixed CNT bundle) structures at a wide range of global interconnect lengths. They observed that crosstalk induced time delay improves by 55.5% for structure 1 as compared to structure 2. This improvement is more progressive with increasing interconnect lengths. The reason behind is the structural difference of mixed CNT bundles.

B. K. Kaushik et.al, 2012 [51] have proposed RLC model for mixed CNT bundle and its performance have been analyzed to address the crosstalk delay and power dissipation. They have proposed two structures for MCB structure1, in which SWCNT and DWCNT are present and structure 2 in which SWCNT and MWCNT are present. For these structures and SWCNT bundle and DWCNT bundle they have estimated the power dissipation and crosstalk delay performance under the condition of opposite switching at aggressor and victim line at different global interconnect length. They have observed that both the performances are significantly improved for structure 2 in comparison to structure1. They have observed 86.01% improvement in crosstalk delay and 61.33 % improvement in power performance for Structure 2 in comparison to SWCNT bundle. The reason they have told is parasitic capacitance. As the number of SWCNT, DWCNT or MWCNT increases, the equivalent resistive and inductive parasitic reduces. The reduction is more for MWCNT as compared to SWCNT and DWCNT.

S.D.Pable, Mohd. Hasan, Mohd. Ajmal Kafeel, 2011 [52] contributed towards reducing the crosstalk effects on switching delay using optimum interconnect height and thickness under sub threshold conditions. They have also observed that in sub threshold region global interconnect delay is dominated by driver resistance and interconnect capacitances. They have observed effect of aspect ratio scaling of driver on mixed CNT bundle resistance and capacitance. They observed that by replacing Cu wire by mixed CNT bundle provides 13% improvement in delay in sub threshold region at aspect ratio =1.5. However, delay variation due to crosstalk introduced by adjacent signal

transition reduced by 31.58% for Cu and 20% for mixed CNT bundle interconnects at AR=1.5 over AR=3. They have also observed that reducing AR in case of super threshold region shows insignificant improvement in delay variation by crosstalk effect. From simulation results they observed that mixed CNT bundle shows significant improvement in delay over Cu wire. They also reported that interconnect geometry parameters provided by ITRS for super threshold circuits will not give the optimum performance for sub threshold region. There is need to redesign the same to reduce the delay as well as crosstalk effects. They have also proposed aspect ratio optimization technique which significantly reduces the delay as well delay variation by crosstalk effect.

2.4. Temperature Dependent Analysis of SWCNT Interconnects

Eric Pop et al. [53] have analyzed the temperature dependent analysis of SWCNT interconnects for the first time. They calculated temperature dependent effective mean free path taking into consideration acoustic phonon scattering and optical phonon scattering and analyzed the dependence of resistance on temperature. They have done the analysis for both low bias and high bias regime and in high bias regime, self heating is also taken into consideration. They also measured experimentally the breakdown voltage for metallic SWCNT of varying lengths. They observed the variation of mean free path and the resistance of SWCNT of different length with respect to temperature. They analyzed the mean free path decreases and hence resistance increases exponentially with rise in temperature.

Amir Hosseni et al. [54] observed the temperature dependent performance of SWCNT bundle interconnect in terms of delay using their thermally aware model for SWCNT. They calculated the temperature dependent impedance parameters of SWCNT bundle using the formulae given by earlier studies [6], [53] for different tube diameters of SWCNT for 1mm length. They observed that resistance of SWCNT bundle increase with rise in temperature and hence the propagation delay. They also estimated the relative improvement in accuracy in estimation of delay using their thermally aware model instead of conventional temperature-independent model. They observed that thermally aware model achieved improvement in the delay estimation accuracy of about 51.3%. They also observed that SWCNT-based interconnects offer more than 5 times reduction in delay at dimensions of about 10-20nm for 27 ^{0}C to 127 ^{0}C temperature range.

2.5. Conclusion

In this chapter, work done by earlier studies has been discussed. The earlier researches prove that CNTs are certainly an alternative for Cu as VLSI interconnects. Most of the work was primarily focused on SWCNT bundle interconnects. The dependence of delay, power and power delay product (PDP) on various parameters of CNT such as diameter, length and tube separation has been discussed in literature. Only a few studies have analyzed the temperature dependent performance analysis of SWCNT. As mixed CNTs contain both SWCNT and MWCNT and have the advantageous properties of both, so they have been proven to be better alternative to Cu interconnect in the literature.

CHAPTER – 3

ANALYSIS AND METHODOLOGY

3.1 Introduction

The various impedance parameters value for different lengths and different diameters value for SWCNT and MWCNT bundle, Mixed CNT Bundle and Cu are calculated using script written in MATLAB using the appropriate formulae given in the literature [5]-[6],[8],[13],[45]-[46],[53]-[56]. The value of impedance parameters of CNT is then compared with each other. The impedance parameters values obtained from MATLAB are then used in lumped and distributed models. Using these models simulation is carried out in tanner EDA tool with optimised aspect ratio of the driver and optimised number of repeaters. SPICE simulation based 90% average propagation delay is calculated using the average of rise time and fall time. Average power dissipation is also obtained from simulation. These values are then compared with each other to find the best alternative to Cu interconnects.

3.2 Technology and Simulation Parameters

Table 3.1 Values used for the calculations [8], [45], [57]

Technology	22nm
V_{dd}	0.7V
Width (W) of global interconnect	32 nm
AR(aspect ratio) for global interconnect	3
Thickness (H) of global interconnect	96nm
Separation(s) between adjacent bundle of interconnect	32nm
Oxide thickness(t_{ox})	76.8nm
ε_{OX}(relative)	2.05
ρ(Cu)	4.2μΩcm
Contact Resistance (R_c)	24KΩ
C_{load}	1pF

3.3 Interconnect Delay Model

To calculate the delay across an interconnect, it is represented in terms of a model consisting of impedance parameters (resistance, capacitance and inductance).In this model input is given through an inverter and output is taken from load capacitance between which interconnect is applied representing its impedance parameters. There are two types of interconnect models which are described below.

3.3.1 Lumped RLC Model

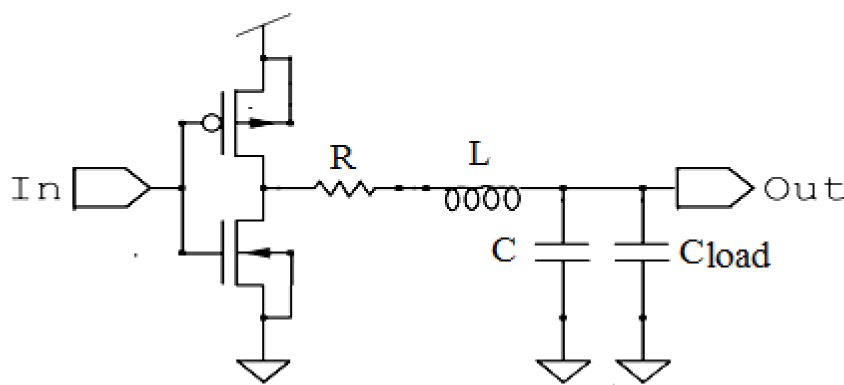


Figure 3.1 Lumped RLC model for interconnect.

As shown in Fig. 3.1 input is given through an inverter and output is taken from load capacitance between which interconnect is applied representing its impedance parameters. Here R, L, C values calculated for the CNT bundle or other interconnects in MATLAB are put to calculate delay and power dissipation for that interconnect. The values of NMOS and PMOS are decided according to the technology, load capacitance is kept at 1pF and the operating frequency of input is 0.1 GHz. Model files for NMOS and PMOS are written in TSPICE and then the simulation is carried out. Delay is calculated from waveform editor and the power is calculated from .out file generated by the tanner tool itself after simulation. Delay and power is calculated for different aspect ratio (AR) of CMOS and then the optimum AR is chosen at which PDP is maximum.

3.3.2 Distributed RLC Model

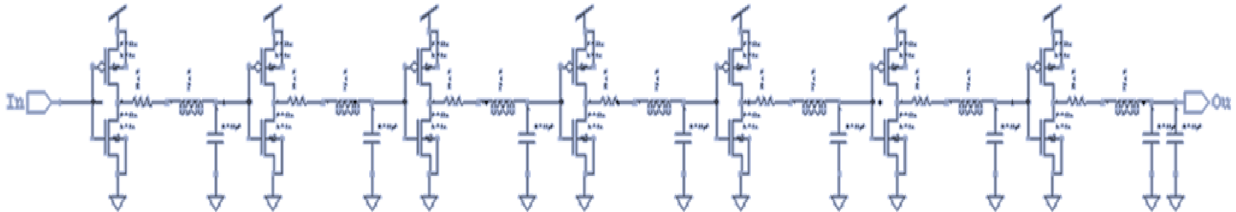


Figure 3.2 Distributed RLC model for interconnect.

The problem in lumped RLC model is that for high value of impedance parameters, the output does not have full voltage swing. So interconnects (specially global) are represented with a distributed RLC model in which impedance is distributed between the repeaters such as if there are n repeaters then RLC between the two repeaters will be divided by n+1 and these repeaters provide the full voltage swing and better delay values[58]. Hence for interconnect, optimum no. of repeaters are calculated which gives the best PDP (power delay product).

3.4 CONCLUSION

In this chapter, various simulation parameters interconnect models and tools used for calculations and simulations have been discussed. Distributed RLC model has been chosen to simulate the interconnect impedance parameters, as the analysis has been done for the global lengths in which the use of repeaters is necessary to have full voltage swing. The optimum no. of repeaters and aspect ratio of driver has been chosen to have the best performance in terms of power delay product (PDP).

CHAPTER – 4

INFLUENCE OF TUBE DIAMETER ON DELAY AND POWER ANALYSIS OF SWCNT BUNDLE

4.1 Introduction

CNTs has been chosen as future VLSI interconnects because of their much lower resistivity and longer mean free path (λ) as compared to Cu. The one major problem with CNT is its high intrinsic resistance (6.4KΩ) [5], which can be alleviated using bundle of CNT in which all the CNTs are arranged in parallel. The parallel combination will reduce the resistance. The performance of CNTs is also influenced by the tube parameters such as diameter of single CNT which decides the number of CNTs in bundle and hence affects the resistance and capacitance of tube and the SWCNT bundle and MWCNT bundle as well.

4.2 Impedance Parameters of SWCNT

The equivalent circuit diagram of SWCNT has been discussed in the previous chapters. The resistance (R), capacitance (C), and inductance (L) of SWCNT is formulated in the literature [5], [6], [45] and is given by

$$R_f = R_C + \frac{h}{2Ne^2} \qquad \text{(for } L < \lambda) \qquad (1),$$

$$R_{CNT} = R_C + \frac{h}{2Ne^2}\left[\frac{L}{\lambda}\right] \qquad \text{(for } L > \lambda) \qquad (2),$$

$$C_E = \frac{2\pi\epsilon}{\ln\frac{y}{d}} \qquad (3),$$

$$C_Q = \frac{2e^2}{hv_f} \qquad (4),$$

$$L_M = \frac{\mu}{2\pi}\ln\left(\frac{y}{d}\right) \qquad (5),$$

$$L_K = \frac{h}{2e^2 v_f} \qquad (6),$$

where R_f is the fundamental quantum resistance associated with single SWCNT. R_C is the contact resistance which is present due to the formation of imperfect contacts. R_{CNT} is the resistance for interconnect length (L) greater than mean free path (λ) of CNT. h is Planck's constant, L is the length

of the SWCNT. The mean free path of CNT which is assumed to 1000*d [6], where d is the diameter of SWCNT. y is the distance of SWCNT from the ground plane, Ɛ is the permittivity and μ is the permeability. C_E is the electrostatic capacitance per unit length between the CNT and the ground plane. C_Q is the quantum capacitance per unit length of the channel, as there are 4 channels in single SWCNT, which are considered as parallel, so it will be multiplied by 4. Fermi velocity $v_f = 8*10^5$ m/s. L_M is the magnetic capacitance per unit length due to the total magnetic energy resulting from the current flowing in the wire. L_K is kinetic inductance per unit length which arises from kinetic energy stored in each conducting channel of the CNT. The four parallel conducting channels in a CNT results in an effective kinetic inductance of $L_K/4$.

To calculate the number of CNTs in the bundle expressions are given by the ref. [6]. SWCNTs are usually connected parallel to decrease the resistance as shown in Fig. 4.1.

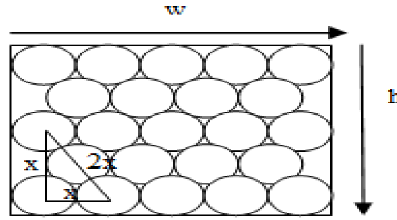


Figure 4.1 Dense bundle of metallic SWCNTs [6].

The number of CNTs in a bundle is given by the following Eq. [6]:

$$n_{CNT} = \begin{cases} n_w n_h - (n_h/2) \text{ if } n_h \text{ is even} \\ n_w n_h - \left(\frac{n_h - 1}{2}\right) \text{ if } n_h \text{ is odd} \end{cases} \quad (7),$$

where $n_w = \left\lfloor \left\{\frac{w-d}{x}\right\} \right\rfloor$ is the number of "columns" , $n_h = \left\lfloor \frac{h-d}{(\sqrt{3}/2)x} \right\rfloor + 1$ is the number of "rows" in the interconnect bundle, w is the width of the bundle, d is the tube diameter, x is the separation distance between two SWCNT, h is the height or thickness of the bundle and n_{CNT} is the total number of CNTs. Therefore, the total bundle resistance is formulated as

$$R_{SWCNT\ bundle}(T) = R_{CNT}(T)/n_{CNT} \quad (8)$$

But according to Fig. 4.1, the actual value of n_w is given as:

$$n_w' = \left\lfloor \left\{\frac{w-d}{x}\right\} \right\rfloor + 1 ;$$

and hence new improved value of CNT is given by:

$$n_{CNT}' = \begin{cases} n_w' n_h - (n_h/2) \text{ if } n_h \text{ is even} \\ n_w' n_h - \left(\frac{n_h - 1}{2}\right) \text{ if } n_h \text{ is odd} \end{cases} \quad (9)$$

It can be seen from the Eq. (9) that the number of columns n_w has been increased with a factor 1in a bundle composed of tubes. Hence, this increased number of columns dependence on new number of SWCNTs (n'_{CNT}) has a significant effect on the impedance parameters of a SWCNT bundle interconnect. Therefore, the improved total bundle resistance is given by:

$$R'_{SWCNT\,bundle}(T) = R_{CNT}(T)/n'_{CNT} \quad (10)$$

The total effective capacitance of bundle of SWCNT is given by Eq. (11),Where C_E^{Bundle} and C_Q^{Bundle} are the total electrostatic capacitance and total quantum capacitance per unit length of bundle of SWCNT and are calculated by (12) and (13)[6],[45].

$$C_{Bundle} = \frac{C_E^{Bundle} . C_Q^{Bundle}}{C_E^{Bundle} + C_Q^{Bundle}} \quad (11),$$

$$C_E^{\ Bundle} = 2\ \frac{2\pi\varepsilon}{\ln(\frac{s}{d})} + \frac{n'_w - 2}{2}\ \frac{2\pi\varepsilon}{\ln(\frac{s+w}{d})} + \frac{3(n_h - 2)}{5}\ \frac{2\pi\varepsilon}{\ln(\frac{y}{d})} \quad (12),$$

where s is the separation between adjacent bundle and w is the width of a bundle.

$$C_Q^{Bundle} = n'_{CNT} . \frac{2e^2}{hv_f} \quad (13)$$

The inductance per unit length of a CNT bundle is given by the parallel combination of the inductances corresponding to each CNT forming the bundle, as shown in Eq. (14), where L_M and L_K are the magnetic and kinetic inductance of an isolated CNT.

$$L_{Bundle} = \frac{L_M + (L_K/4)}{n'_{CNT}} \quad (14)$$

4.3 Impedance Parameters of MWCNT

As discussed above, MWCNT consists of concentric SWCNTs (also called shells) and the number of shells N_{shell} in an MWCNT is given by [8]:

$$N_{shell} = 1 + \left(\text{inter}\left(\frac{d_{max} - d_{min}}{2d}\right)\right) \quad (15),$$

where "Inter{·}" indicates that only the integer part is taken into account. d_{max} is the diameter of outermost shell of MWCNT , d_{min} is the diameter of innermost shell which generally has the value equals to $d_{max}/2$ and d is the vanderwall gap. Number of channels in a shell is given by:

$$N_{channel}(D) \approx a \cdot D + b,\ D > 3\,nm \quad (16),$$

where D is the diameter of the shell, a = 0.0612 nm^{-1}, and b = 0.425

The shell of a MWCNT has three types of resistance: quantum resistance R_Q, scattering-induced resistance R_S, and contact resistance R_{mc}. Note that R_S only comes into role if the length of the nanotube is larger than the electron MFP. R_Q and R_S are intrinsic, and R_{mc} is due to fabrication process. The value of the intrinsic conductance (G) is determined by:

$$G^{-1} = R_Q + R_S . L = \frac{h}{2e^2N} + \frac{h}{2e^2N} \cdot \frac{L}{\lambda} \qquad (17),$$

where $h/2e^2 \sim 12.9$ kΩ, and L, λ and N are the length, MFP, and number of conducting channels of the shell, respectively. λ =250d [59], where d is the diameter of each shell. The imperfect contact resistance R_{mc} can range from zero to hundreds of kilo-Ohms for different growth processes. MWCNT consists of concentric shells and the total resistance of MWCNT is given as:

$$R_{MWCNT} = R_{mc} + \frac{1}{\sum_{i=1}^{p} \frac{1}{R_{Qi}+R_{Si}}} \qquad (18),$$

where i depict the shell number and p is the total number of shells calculated by Eq. (15). Inductance and capacitance of each shell is same as that of SWCNT given by the Eq. (3)-(6).

Electrostatic capacitance with the ground will be there for the outermost shell of MWCNT only. There is one more capacitance exist in MWCNT which is called shell-to-shell capacitance C_S and is given as

$$C_S = \frac{2\pi\epsilon}{\ln\left(\frac{D_{out}}{D_{in}}\right)} \qquad (19)$$

The total capacitance and inductance of MWCNT can be calculated using the MWCNT model [8].

A MWCNT bundle is shown in Fig. 4.2. The MWCNTs in a bundle are considered parallel as for the case of SWCNT bundle and then total resistance of bundle is calculated by dividing the resistance of a MWCNT by the number of MWCNTs in a bundle and is given by

$$R_{MWCNT\,bundle} = R_{MWCNT}/n_{MWCNT} \qquad (20),$$

where R_{MWCNT} is the resistance of single MWCNT calculated by eq. (16) and n_{MWCNT} is the number of MWCNTs in a bundle as shown in Fig. 4.2. Similarly total inductance and total capacitance per unit length of MWCNT bundle is given by

$$L_{MWCNT\,bundle} = L_{MWCNT}/n_{MWCNT} \qquad (21),$$

$$C_{MWCNT\,bundle} = \frac{\frac{C_{Q_MWCNT}}{n_{MWCNT}}.C_{E_MWCNT}}{\frac{C_{Q_MWCNT}}{n_{MWCNT}} + C_{E_MWCNT}} \quad (22),$$

where L_{MWCNT} is the total inductance per unit length of MWCNT. C_{Q_MWCNT} is quantum capacitance and C_{E_MWCNT} is electrostatic capacitance per unit length of MWCNT calculated using eq. (3)- (6) and model given by ref. [8].

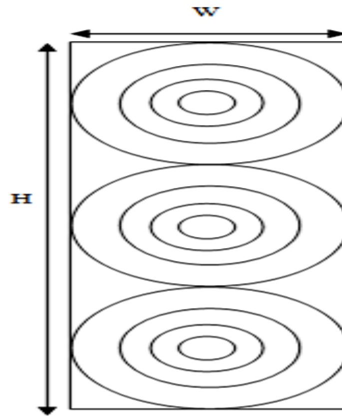


Figure 4.2 MWNCT bundle interconnect.

4.4 Impedance Parameters of Cu Interconnect

Cu interconnect delay and power are used as normalizing parameters for CNT bundle interconnects delay and power respectively so that a relative measure of CNT interconnect delay and power with respect to that of copper interconnect can be obtained. So it is necessary to calculate the impedance parameters of Cu interconnect to calculate the delay and power of Cu interconnect. The R, L, C values of Cu interconnect are given as [2], [45]:

$$R_{Cu} = \frac{\rho(T).L}{w.H} \quad (23),$$

$$\rho(T) = \rho_0[1 + \alpha(T - T_0)] \quad (24),$$

where $T_{0=}$ 300 K (27° C) and $\rho_0 = 4.2e\text{-}8\Omega m$ and $\alpha_0 = .0039$ /K.

$$Cg = Eox*((w/H)+(2.22*(w/(w+(.7*H)))^{3.19})+((1.17*(w/(w+(1.15*H))).^{76})*$$

$$((H/(5.53*H)\ )^{.12})))*L*10^{-12} \quad (25),$$

$$L_S = \frac{\mu L}{2\pi}\left[\ln\left(\frac{2L}{w+H}\right) + \frac{1}{2} + 0.22\left(\frac{w+H}{L}\right)\right] \quad (26),$$

where Cg is capacitance with respect to ground. L_S is the self inductance L= length of interconnect, w= width of interconnect. H= thickness, Eox= relative permittivity of SiO_2, μ= permeability.

4.5 Impedance Analysis

The technology and various parameters chosen for the calculations and simulation have been discussed in chapter 3. The impedance parameters are calculated using MATLAB. The impedance parameters for SWCNT bundle are calculated using the new corrected value of number of CNTs i.e. n'_{CNT} given by the eq. (9). Figure 4.3, 4.4 and 4.5 shows the variation in resistance, capacitance and inductance of SWCNT bundle with diameter for different values of length respectively. It is observed that as tube diameter increases, resistance and inductance of SWCNT bundle increases and capacitance decreases. This is because of decrease in number of CNTs in a bundle with increase in tube diameter (eq. 9). It is also observed that higher the length of interconnect; greater would be its resistance, capacitance and inductance.

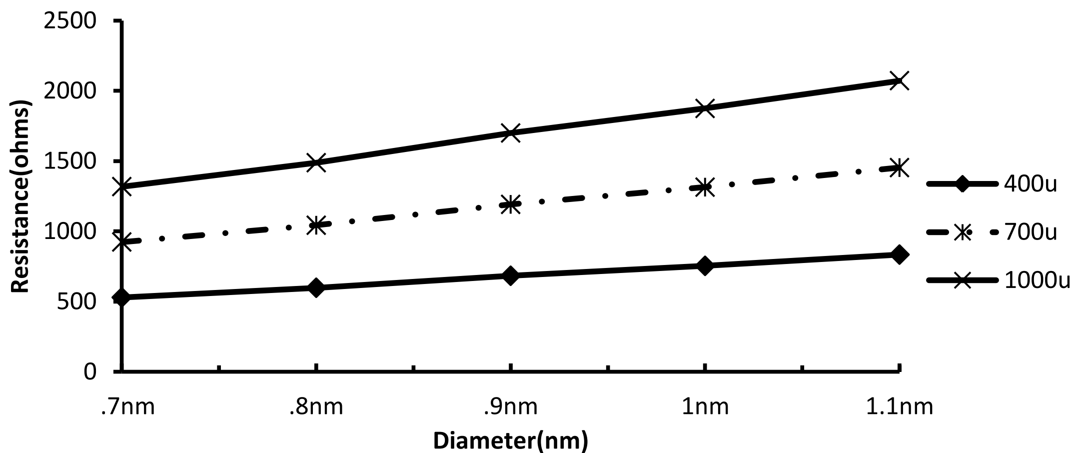


Figure 4.3 Variation in Resistance of SWCNT bundle with diameter for different values of length at 22nm technology.

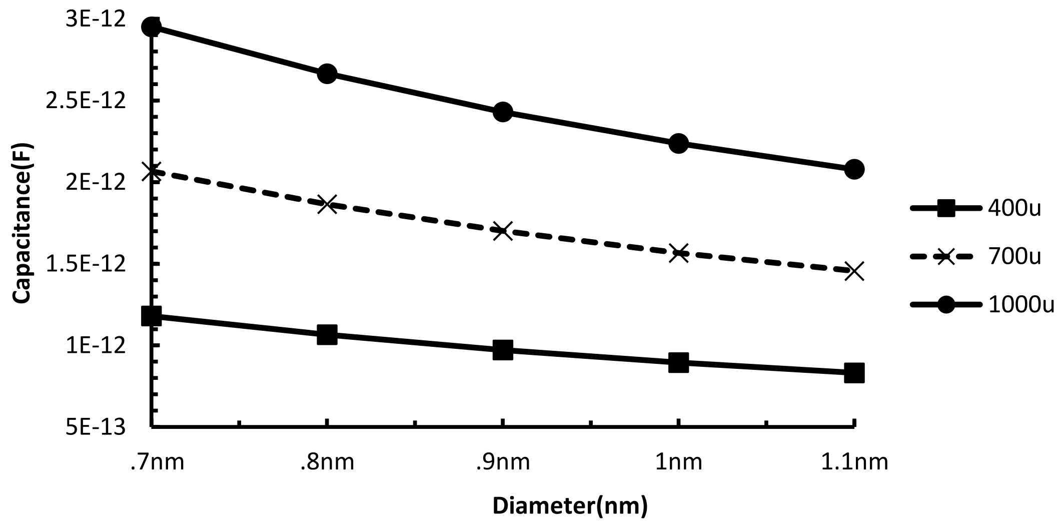


Figure 4.4 Variation in Capacitance of SWCNT bundle with diameter for different lengths at 22nm technology.

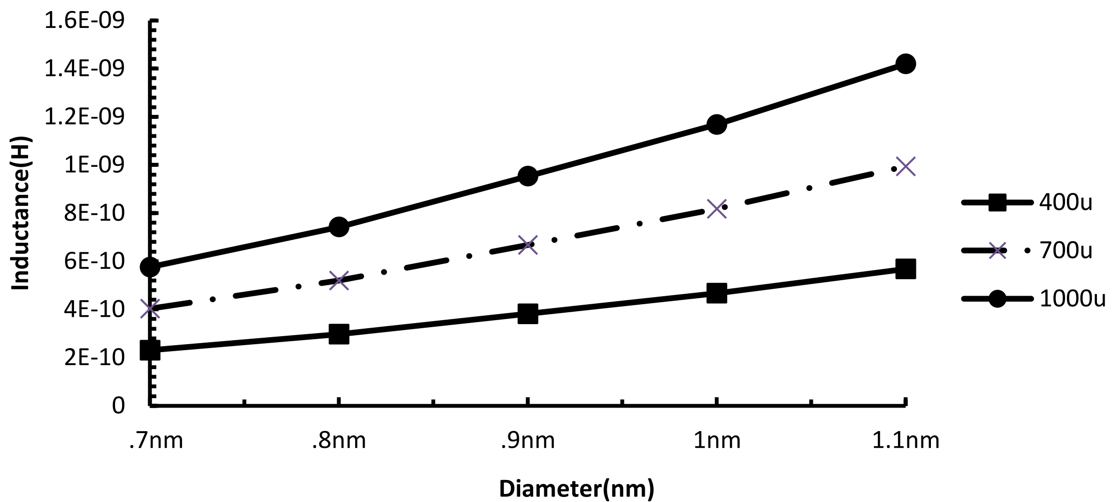


Figure 4.5 Variation in inductance of SWCNT bundle with diameter at diff. values of length for 22nm technology.

Table 4.1 shows the difference in value of resistance, capacitance and inductance for SWCNT bundle with tube diameter 1nm and interconnect length 1000μm using old and new n_{CNT} formula. As number of columns has increased by 1, number of CNTs in a bundle has been increased, due to which there is an increase in capacitance and decrease in resistance and inductance which will affect the delay of CNT. Hence it is necessary to take into consideration this change in formula.

Table 4.1 Value of resistance, capacitance and inductance for SWCNT bundle with tube diameter 1nm and interconnect length 1000μm using old and new n_{CNT} formula at 22nm technology

Formula of n_{CNT}	Resistance (Ω)	Capacitance (pF)	Inductance(nH)
Old n_{CNT}	1935.828	2.22	1.21
New n_{CNT}	1874.373	2.24	1.17

Figure 4.6, 4.7 and 4.8 show the variation in resistance, capacitance and inductance of MWCNT Bundle with diameter (D_{max}) =32nm with length. It is observed that value of impedance parameters increases linearly with increase in length of interconnect. It is also observed that resistance of MWCNT bundle at each length is greater than SWCNT Bundle for every choice of tube diameter. But the capacitance of MWCNT bundle is much lesser than SWCNT bundle.

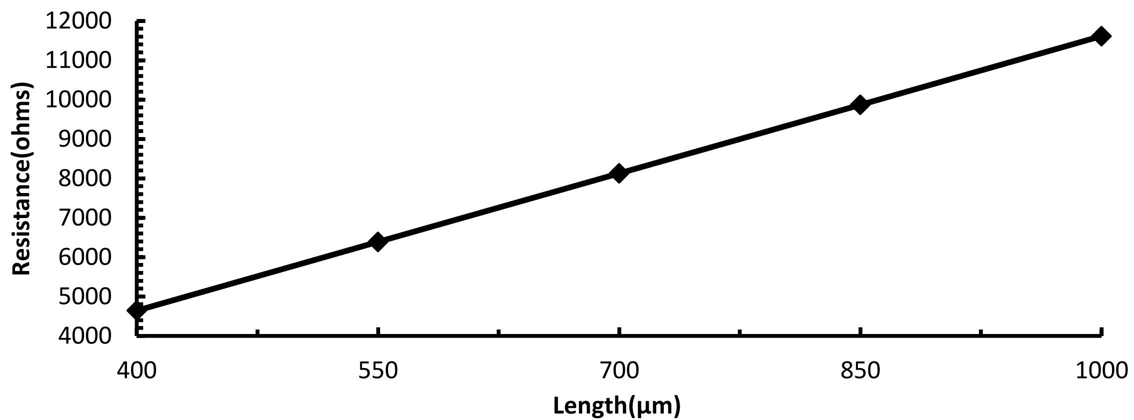


Figure 4.6 Variation in resistance of MWCNT bundle (D_{max}=32nm) with length at 22nm technology.

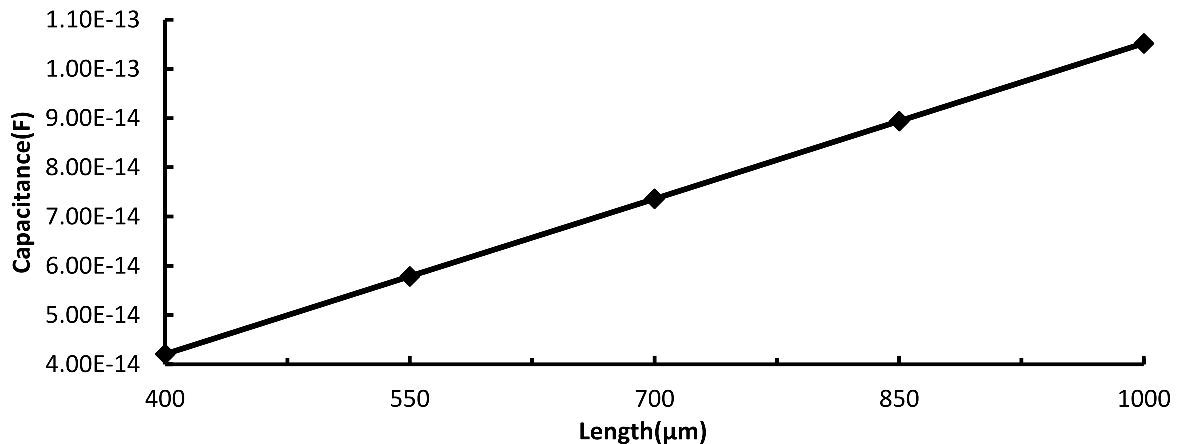


Figure 4.7 Variation in capacitance of MWCNT bundle (D_{max}=32nm) with length at22nm technology.

Figure 4.8 variation in inductance of MWCNT bundle (D_{max}=32nm) with length at 22nm technology.

4.6 Performance Analysis

Performance analysis of SWCNT bundle with different tube diameters and MWCNT bundle with different has been studied in terms of propagation delay and power .Copper interconnect delay and power are used as normalizing parameters for CNT bundle interconnects delay and power respectively so that a relative measure of CNT interconnect delay and power with respect to that of copper interconnect can be obtained.

4.6.1 Delay Analysis

Figure 4.9 shows the variation of normalized propagation delay with respect to diameter of SWCNT bundle using an improved and old n_{CNT} formula [6]. It is observed that normalized delay decreases with increase in diameter for both cases, but there is significant difference between the normalized delay of both which cannot be neglected. Hence new accurate model should be used which offers lesser delay and is more accurate.

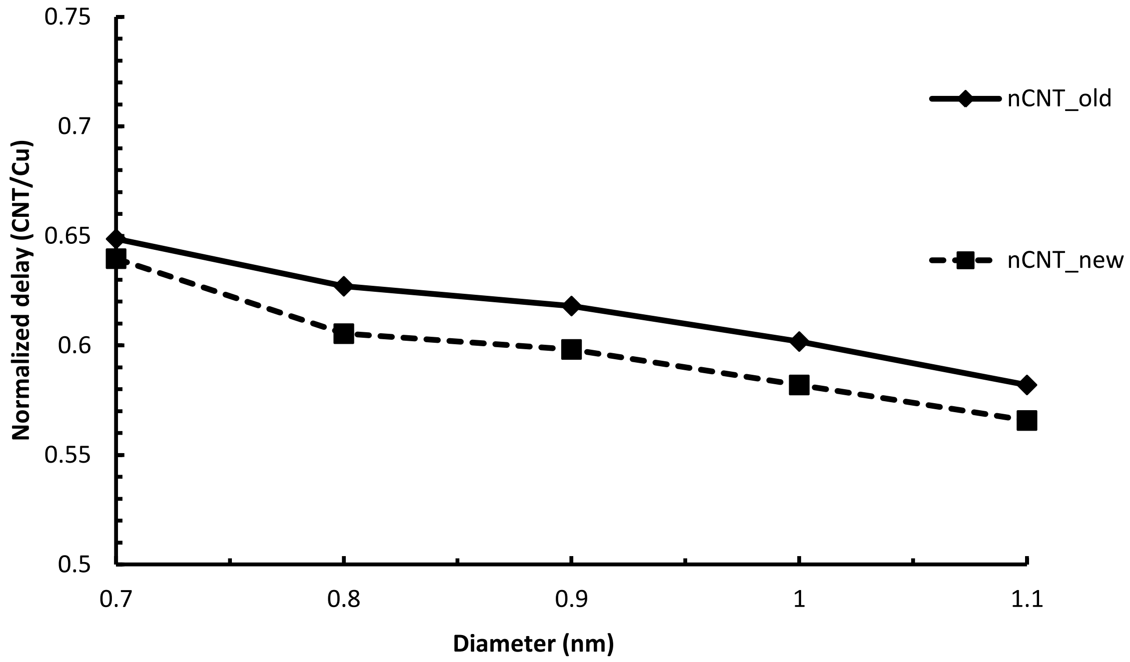


Figure 4.9 Normalized delay variation of SWCNT bundle with respect to tube diameter for new value of n_{CNT} and old value of n_{CNT} given by ref. [6] for 1000μm length at 22nm technology.

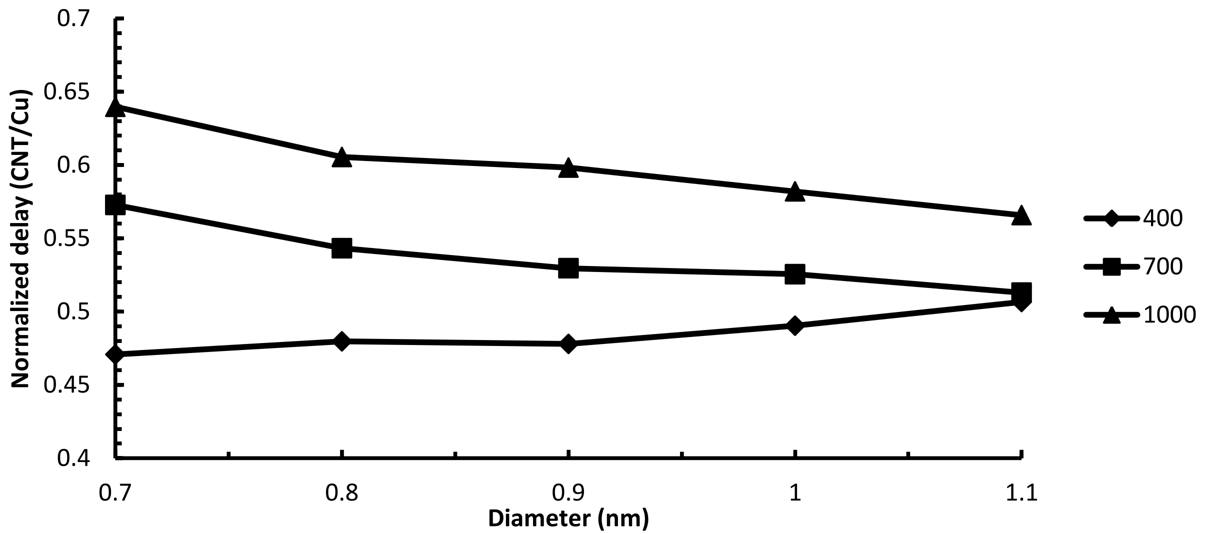


Figure 4.10 Variation in normalized delay of SWCNT bundle with tube diameter for different lengths (in μm) at 22nm technology.

Figure 4.10 shows the variation of normalized propagation delay with respect to diameter of SWCNT bundle for three different lengths. The results reveal that for different lengths normalized delay is minimum for different tube diameters. Therefore to achieve high performance in terms of delay using CNTs diameter should be chosen wisely according to the length of interconnect.

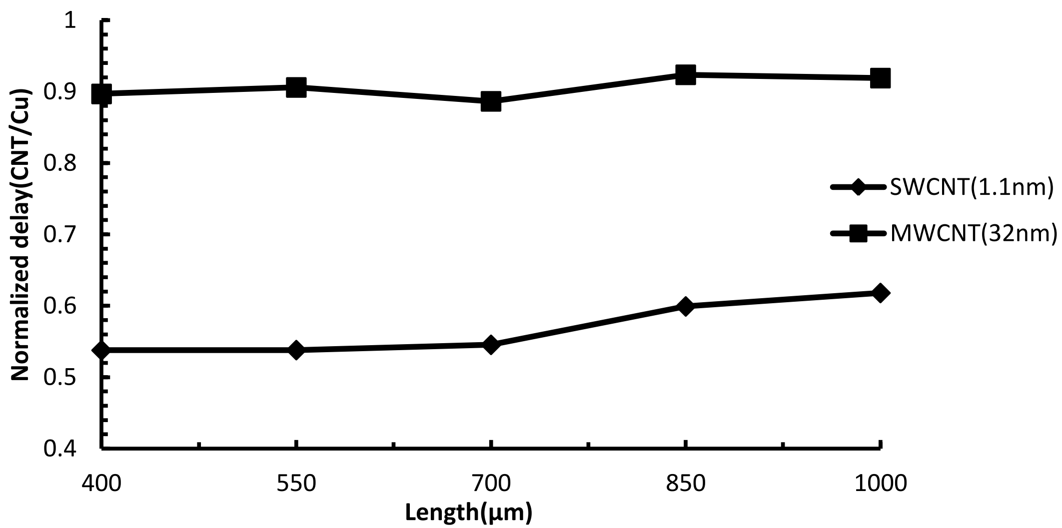


Figure 4.11 Variation in normalized delay of SWCNT bundle (d=1.1 nm) and MWCNT bundle (D_{max}=32nm) with length for 22nm technology.

Figure 4.11 shows the variation of normalized propagation delay with respect to length of SWCNT bundle (d=1.1nm) and MWCNT bundle (D_{max}=32nm). It is observed that although both structures have lesser propagation delay than Cu interconnect, but the SWCNT bundle with diameter 1.1nm offers lesser delay than MWCNT bundle with outermost diameter 32nm for all range of length given in fig. 4.10. This is because of the very low resistance of SWCNT bindle as compared to MWCNT bundle.

4.6.2 Power Analysis

Figure 4.12 shows the variation of normalized power with respect to diameter of SWCNT bundle for three different lengths. The results revealed that for different lengths normalized power is minimum for higher tube diameter. This is because of the fact that the capacitance of SWCNT bundle decreases with increase in tube diameter. Therefore to achieve low power dissipation using CNTs higher tube diameter should be chosen for the given length of interconnect.

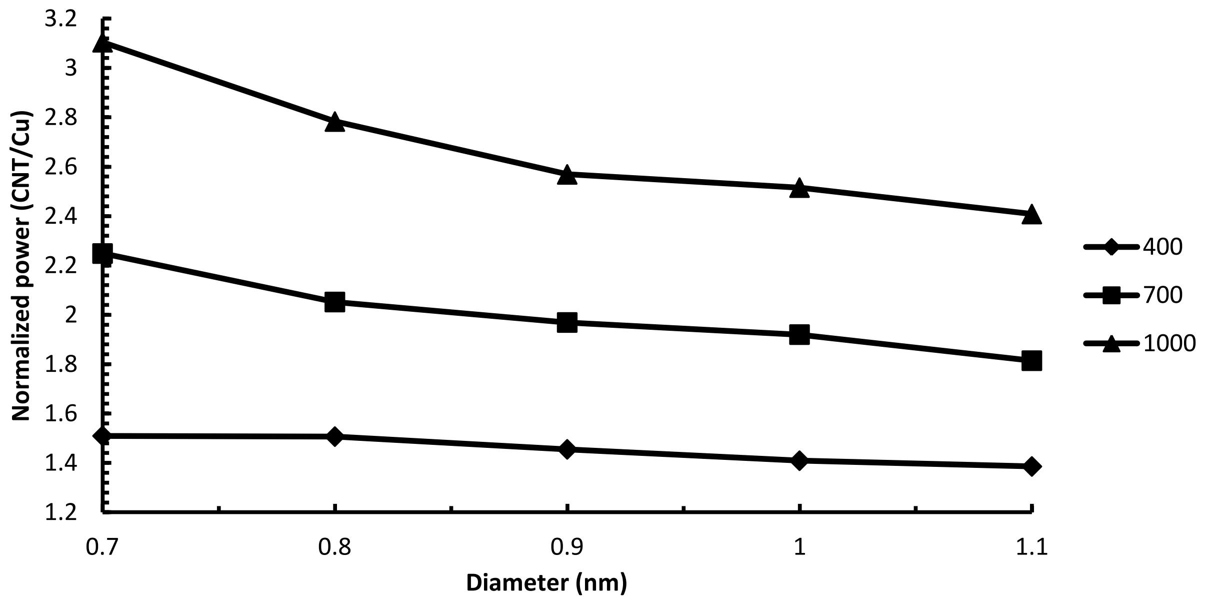


Figure 4.12.Variation in normalized power of SWCNT bundle with tube diameter for different lengths (in μm) at 22nm technology.

Figure 4.13 shows the variation of normalized power with respect to length of SWCNT bundle (d=1.1nm) and MWCNT bundle (D_{max}=32nm). It is observed that SWCNT bundle have more power dissipation than Cu interconnect. On the other hand power dissipated through MWCNT bundle is almost same as that of Cu interconnect. This is because of the very low capacitance value of MWCNT bundle as compared to SWCNT bundle. Therefore, for low power applications, MWCNT bundle interconnect is better choice.

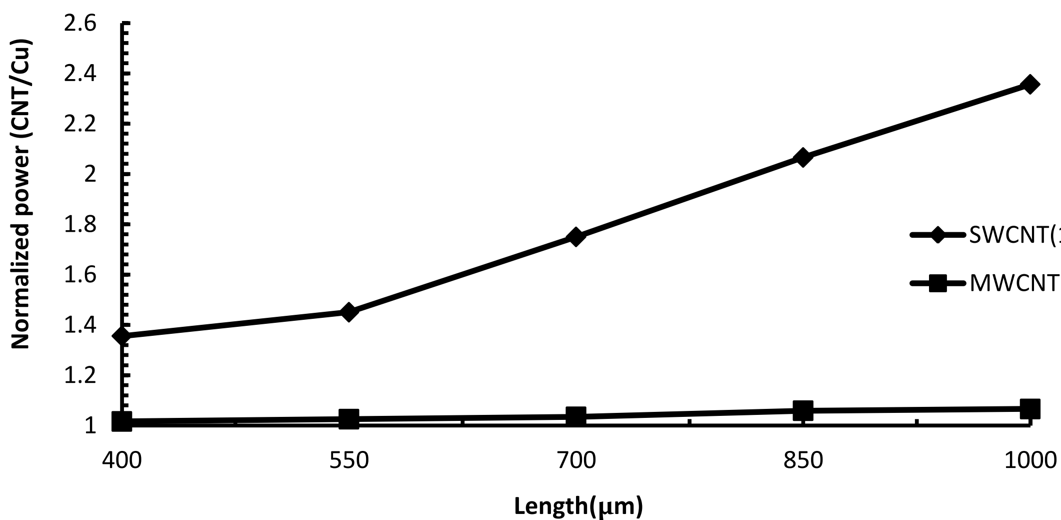


Figure 4.13 Variation in normalized power of SWCNT bundle (d=1.1nm) and MWCNT bundle (D_{max}=32nm) with length at 22nm technology.

4.7 Conclusion

In this chapter, the influence of various parameters such as length and diameter on delay and power of SWCNT, MWCNT and Cu interconnect has been analyzed. Simulated results reveal that the optimum diameter should be chosen wisely to get better performance in SWCNT bundle and for high speed VLSI applications, SWCNT bundle is better choice than Cu and MWCNT bundle. But for low power applications, MWCNT bundle is better one.

CHAPTER -5

TEMPERATURE DEPENDENT PERFORMANCE ANALYSIS OF MIXED CNT BUNDLE INTERCONNECTS

5.1 Introduction

Due to the present trends in device scaling, thermal issues have now emerged as a major challenging factor in the possible usage of nanotubes for designing high performance integrated circuits. Integrated circuits often operate at temperatures much greater than room temperature. So, if CNTs are to be employed in integrated circuit applications, it is critical to understand how their electrical

characteristics will vary at temperatures greater than room temperature. Therefore, it is important to investigate the effect of temperature variation on the electrical transport of CNTs, if CNTs are proposed as an alternative to the conventional metal (copper) for future interconnects. Only a few studies investigated the effect of temperature variation on the performances of CNTs [53]-[56], [60]. Their analyses show that electron transport is limited by the phonon scattering mechanism. Eric Pop et al. [53], [55] also found the strong temperature dependence of the optical phonon absorption rate which have a considerable influence on the electrical resistance of CNTs operating in high bias regime where Joule self heating must be taken into account. Ashok Srivastava et al. [60] studied Joule heating in CNT based VLSI interconnects for various length of CNT interconnects and analyzed the influence of bias voltage on scattering parameters, Amir Hosseini et al. [54] presented a thermally aware model for SWCNT which achieved an average of 51.3% accuracy in delay estimation of SWCNT bundle interconnects.

The temperature variations have the significant effect on interconnect resistance which will affect the performance of CNT bundle in terms of delay, power and power delay product(PDP). In this chapter, a complete temperature dependent impedance and performance analysis in terms of delay, power dissipation and PDP of mixed CNT bundle interconnects over a temperature range from 300 to 500K, have been presented. In addition, the performance of mixed CNT bundle has also been compared with SWCNT bundle, MWCNT bundle and Cu interconnect over a temperature range from 300 to 500K. Results obtained through simulation show that the temperature variation in high speed ICs play an important role to optimize the interconnect performance in terms of PDP.

5.2 Temperature Dependent Impedance Parameters of Interconnects

5.2.1 Effective Mean Free Path

As the high performance ICs have great variation in temperature, it is necessary to include factor of temperature in the calculation of resistance of interconnect. The resistance of a CNT is dependent on the electron mean free path which is further dependent upon acoustic phonon and optical phonon scattering [53]. Where scattering is a function of temperature which affects the mean free path (MFP) as the temperature rises. The electron–electron scattering mechanism is negligible in CNT and the main source of scattering in CNT is the electron–phonon scattering [53]. Acoustic, optical emission and absorption scattering phenomena are the different types of electron–phonon scattering that

present in metallic SWCNTs. Therefore, combining the effect of all type of scattering the effective mean free path (λ_{eff}) can be written as [53]

$$\lambda_{eff} = \{\lambda_{AC}{}^{-1} + \lambda_{OP}{}^{-1} + \lambda_{OP,abs}{}^{-1}\} \quad (1),$$

where λ_{AC} is the acoustic MFP dependent upon elastic electron scattering with acoustic phonons and λ_{OP} is the effective optical MFP due to inelastic scattering caused by optical phonon emission and $\lambda_{OP,abs}$ is the effective optical MFP due to scattering caused by absorption of phonon . Acoustic phonon scattering is the main origin of the ohmic resistance at low-bias conditions in metallic SWCNTs. λ_{AC} is proven to be directly dependable on both temperature and diameter. Therefore, λ_{AC} can be written as

$$\lambda_{AC}(d, T) = \frac{\lambda_{AC,300}}{d_0}\frac{300\ d}{T} \quad (2),$$

where $\lambda_{AC,300}$=1600 nm is the reported acoustic MFP for tube diameter d_0 = 1.8 nm at 300 K [55]. In case of high-bias conditions, the electric field that is generated along the CNT (E = V/L) accelerates the electrons and increases their kinetic energy. When the electron energy reaches the optical phonon energy level, a phonon will be emitted with energy $h\Omega$ ($h\Omega$ ~ 0.16-0.2 eV) [55] .where as $\lambda_{OP,abs}$ is given by:

$$\lambda_{OP,abs} = \frac{\lambda_{OP,300} d}{d_0}\frac{N_{OP}(300)+1}{N_{OP}(T)+1} \quad (3),$$

where $\lambda_{OP,300}$ = 15 nm is the measured spontaneous effective emission length for diameter d_0 at 300 K [53]. N_{OP} is the optical phonon occupation and is given by the equation:

$$N_{OP}(T) = 1/\exp\left({h\Omega}/{K_B T} - 1\right) \quad (4),$$

where K_BT is the thermal energy (K_B is the Boltzmann's constant). In addition, optical scattering can occur when an electron acquires the required energy by absorbing another optical phonon, respectively or after electrons gain sufficient energy from electric field (fld) [53], [55]. Therefore, λ_{OP} can be written as:

$$\lambda_{OP,ems}(d, T) = \left(1/\lambda_{OP,ems}^{fld} + 1/\lambda_{OP,ems}^{abs}\right)^{-1} \quad (5),$$

where $\lambda_{OP,ems}^{fld}$ is the MFP due to the electric-field acceleration based scattering. $\lambda_{OP,ems}^{fld}$ can be written as:

$$\lambda_{OP,ems}^{fld}(d, T) = \frac{(h\Omega - K_B T)L}{qV} + \frac{\lambda_{OP,300} d}{d_0}\frac{N_{OP}(300)+1}{N_{OP}(T)+1} \quad (6)$$

The first term represents the distance that the electron needs to accelerate and gain the enough energy to emit a phonon, while the second term represents the distance that the electron travels after gaining the energy before emitting the phonon.

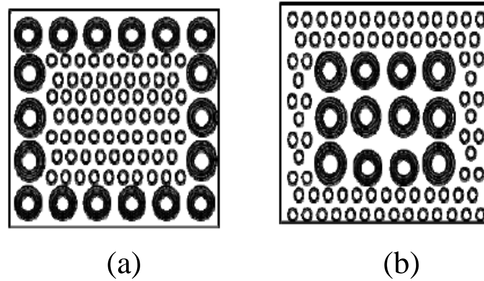
$\lambda_{OP,ems}^{abs}(d,T)$ measures the scattering effect due to absorbing an optical phonon and can be written as

$$\lambda_{OP,ems}^{abs}(d,T) = \frac{\lambda_{Oz,300} d.(N_{OZ}(300)+1)}{d_0.N_{OZ}(T)} \quad (7)$$

The existence of the hot phonon phenomenon that is caused by severe self heating is not considered in this analysis. In the present study, low bias condition is considered, where the generated electric field is not large enough to create the hot phonons [55].

5.2.2 Mixed CNT Bundle Impedance Parameter Calculations

Individual SWCNTs suffer from an intrinsic ballistic resistance of approximately, which can cause excessive delay. To reduce the impact of the individual tube, bundles of SWCNTs in parallel are more in favor. However, the CNT bundles are generally a mixed CNT bundles consisting of multiwall as well as single wall CNT. Experimental results [9]-[11] demonstrated that a realistic nanotube bundle is a mixed bundle of single- and multi-wall CNTs. The two possible structures for mixed CNTs are as shown in fig. 5.1.



(a) (b)

Figure 5.1(a) Structure 1 shows MWCNTs at periphery and all the SWCNTs are at the middle portion of bundle. (b) Structure 2 shows SWCNTs at periphery and all the MWCNTs are at the middle portion of bundle [13].

The first structure (structure1) of MCB is arranged in such a way that all the tubes conducting maximum current are placed at centre of the bundle as shown in Fig. 5.1(a). The second structure (structure 2) shows that all the tubes which conduct least or no current are at middle of mixed bundle as shown in Fig. 5.1(b) [13]. The primary advantage of using structure 1 is that conduction mainly occurs through the tubes at center of the bundle, while tubes at the outer periphery serve as the shields from neighboring CNT bundles [13]. These tubes (central or peripheral) can either be

SWCNTs or MWCNTs, which can be either metallic or semiconducting in nature. The structure of mixed bundle is more complicated than SWCNTs or MWCNTs. That's why it is not possible to do direct analysis of these bundles. Therefore, a new hierarchical model has been developed [13] by considering two CNTs, one SWCNT and one MWCNT. Equivalent single conductor (ESC) models are developed both for the structures of bundled SWCNT and MWCNT interconnects. These different interconnect models are combined to develop the equivalent RLC model of MCB interconnect structure as shown in Fig. 5.2.

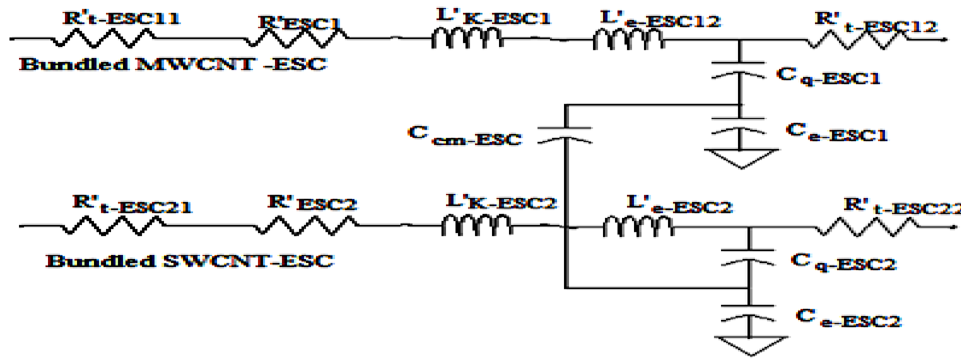


Figure 5.2 Equivalent *RLC* model of MCB based interconnect [13].

In Fig. 5.2 R'_{t-ESC}, R'_{ESC}, $L'_{K\text{-}ESC}$, $L'_{e\text{-}ESC}$, $C_{q\text{-}ESC}$, $C_{e\text{-}ESC}$ are total resistance, kinetic inductance, magnetic inductance, quantum capacitance and electrostatic capacitance of SWCNT bundle and MWCNT bundle respectively. These impedance parameters can be calculated by the appropriate expressions given for SWCNT and MWCNT bundle discussed in previous chapter. In Fig. 5.2 coupling capacitance (C_{cm-ESC}) has been considered between bundles of SWCNT and MWCNT, which is given by the formula:

$$C_S = \frac{\pi\epsilon}{\cosh^{-1}\left(\frac{S_p}{D}\right)} \quad (8),$$

where S_p is the spacing between the SWCNT bundle and MWCNT bundle for both MCB structures and is considered to be as 2.6nm and D is the average diameter of SWCNT and MWCNT.

The total temperature dependent resistance of mixed CNT bundle (R_{MCB}) can be defined as a function of temperature dependent resistance of SWCNT and MWCNT bundle given as:

$$R_{MCB}(T) = \{R_{SWCNT\ bundle}(T)\ ||\ R_{MWCNT\ bumdle}(T)\} \quad (9)$$

Number of SWCNT and MWCNT in the bundle is calculated using the following formulae given below.

FOR MCB structure 1 (MCB 1):

The no. of columns and no. of rows of MWCNT bundle is given by:

$$n_{mw} = \text{floor}\left(\frac{w-d_{max}}{d_{max}} + 1\right);\ n_{mh} = \left\lfloor\frac{h-d_{max}}{d_{max}}\right\rfloor + 1\ ,$$

where w is the width of interconnect, h is the height of interconnect and d_{max} is the outermost diameter of MWCNT. The total number of MWCNTs is given by:

$$n_{MWCNT} = 2 * (n_{mw} + n_{mh}) - 4 \qquad (10)$$

The no. of columns and no. of rows of SWCNT bundle is given by:

$$n_{w} = \text{floor}\left(\frac{w-\left(d+\left(2*\left(d_{max}+S_p\right)\right)\right)}{x} + 1\right); \qquad n_{h} = \left\lfloor\frac{h-\left(d+\left(2*\left(d_{max}+S_p\right)\right)\right)}{(\sqrt{3}/2)x}\right\rfloor + 1$$

where d is the diameter of SWCNT and x is the separation distance between centers of two adjacent SWCNT. The no. of SWCNTs in the bundle is given by:

$$n_{CNT} = \begin{cases} n_w n_h - (n_h/2) \text{ if } n_h \text{ is even} \\ n_w n_h - \left(\frac{n_h-1}{2}\right) \text{ if } n_h \text{ is odd} \end{cases} \qquad (11)$$

FOR MCB structure 2 (MCB 2)

The total number of MWCNTs is chosen as 12 as depicted in fig. 5.1(b). Hence the no. of columns and no. of rows of SWCNT bundle is given by:

$$n_{w1} = \text{floor}\left(\frac{w-\left(d+\left(2*\left(2*d_{max}+S_p+3*d_1\right)\right)\right)}{x} + 1\right);\ n_{w2} = \text{floor}\left(\frac{\left(\left(2*\left(2*d_{max}+S_p+3*d_1\right)\right)\right)-d}{x} + 1\right);$$

$$n_{h1} = \left\lfloor\frac{h-d}{(\sqrt{3}/2)x}\right\rfloor + 1 \quad n_{h2} = \left\lfloor\frac{h-\left(d+\left(2*\left(d_{max}+S_p\right)\right)\right)}{(\sqrt{3}/2)x}\right\rfloor + 1$$

where d is the diameter of SWCNT and x is the separation distance between centers of two adjacent SWCNT. The no. of SWCNTs in the bundle is given by:

$$n_{CNT1} = \begin{cases} n_{w1} n_{h1} - (n_{h1}/2) \text{ if } n_{h1} \text{ is even} \\ n_{w1} n_{h1} - \left(\frac{n_{h1}-1}{2}\right) \text{ if } n_{h1} \text{ is odd} \end{cases} \qquad (12)$$

$$n_{CNT2} = \begin{cases} n_{w2} n_{h2} - (n_{h2}/2) \text{ if } n_{h2} \text{ is even} \\ n_{w2} n_{h2} - \left(\frac{n_{h1}-1}{2}\right) \text{ if } n_{h2} \text{ is odd} \end{cases} \qquad (13)$$

$$n_{CNT} = n_{CNT1} + n_{CNT2} \qquad (14)$$

The total resistance of SWCNT bundle can be defined using temperature dependent resistance of individual SWCNT. Where, the resistance of an individual SWCNT with N conducting channel can be formulated as [54]

$$R_{CNT}(T) = R_C + \frac{h}{2N(d,T)e^2} \qquad (\text{for } L < \lambda) \qquad (15),$$

$$R_{CNT}(T) = R_C + \frac{h}{2N(d,T)e^2}\left[\frac{L}{\lambda_{eff}(T)}\right] \qquad (\text{for } L > \lambda) \qquad (16),$$

where R_C is the contact resistance, h is the Planck's constant, e is the electron charge, $\lambda_{eff}(T)$ is the temperature dependent effective electron mean free path (MFP), which is the average distance between successive scatterings and formulated by Eq.(1) and calculated using eq. (1)-(7). L is the length of interconnect and N is the number of available conducting channels for SWCNT. Here, for the sake of proper calculation of SWCNT resistance, R_C value is assumed to be 24 kilo-ohms [54].
MWCNTs consists of several concentric SWCNTs which are also called shells and by calculating the temperature dependent resistance of each shell and then considering all the shells in parallel combination resistance of MWCNT can be calculated. By using the calculation of SWCNT bundle and MWCNT bundle, impedance parameters of mixed CNT bundle can be calculated using the model given in fig. 5.2. The other impedance parameters viz. capacitance and inductance for MWCNT bundle and SWCNT bundle are calculated using the formulae discussed in the previous chapter.

5.3 Impedance Analysis

The impedance parameters for bundles of SWCNT, MWCNT and mixed CNT bundle (MCB) by using the tubes of varying diameter are calculated using the formulae given in the this chapter and previous chapter for a temperature range 300-500 K at low bias conditions [53] assuming an interconnect of length 1000μm.

Fig. 5.3 shows the variation of temperature dependent resistance estimated using an improved and old model [6]. It shows that with rise in temperature, resistance estimated using an improved model is observed less compared to old model and is more accurate.

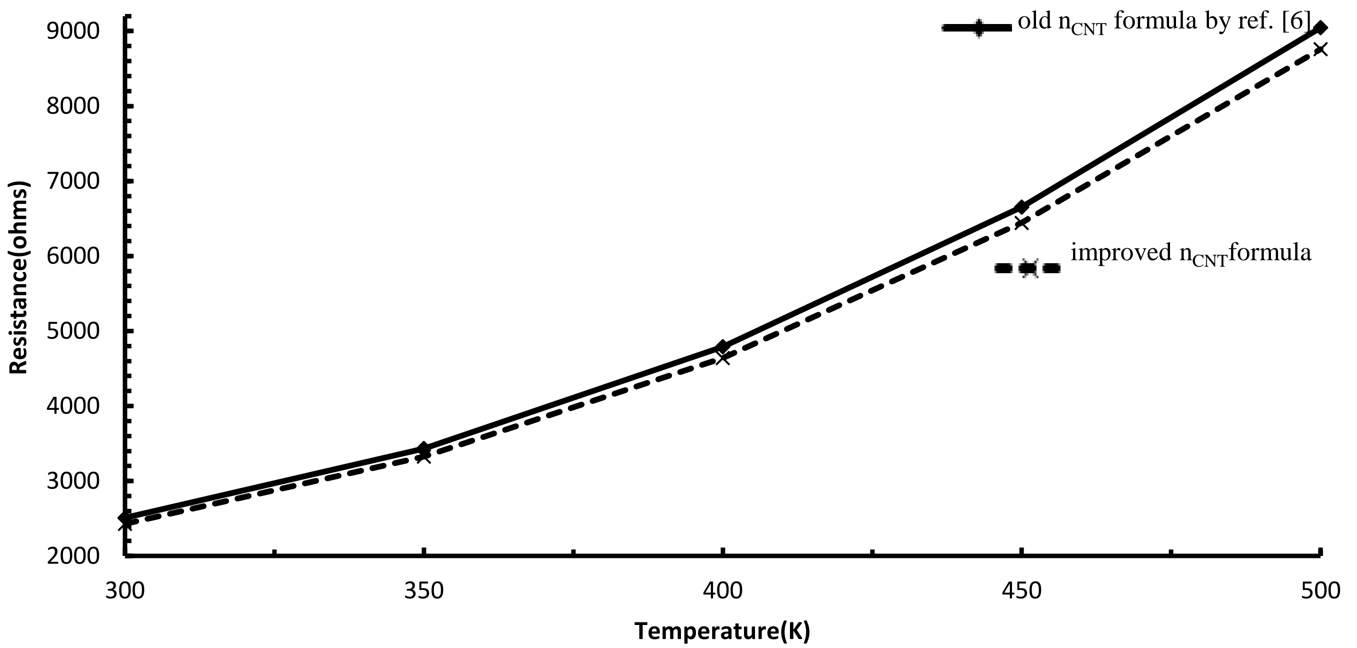


Figure 5.3 Change of resistance of SWCNT bundle (with diameter=1nm) with respect to temperature for new improved formula of n_{CNT} and old formula of n_{CNT} given by ref. [6] at 22nm technology.

Fig. 5.4 and fig. 5.5 show the variation of temperature dependent resistance of MCB1 and MCB2 respectively with different tube diameter of SWCNT bundle (0.7-1.1nm) and MWCNT Bundle (4nm &2nm). In this analysis, an improved model of SWCNT bundle resistance is used. It is observed that the resistance of MCB1 and MCB2 increases with rise in temperature. It has also been noted that as the tube diameter of SWCNT and MWCNT decreases, resistance of MCB1 and MCB2 decreases due to increase in number of CNTs in bundle.

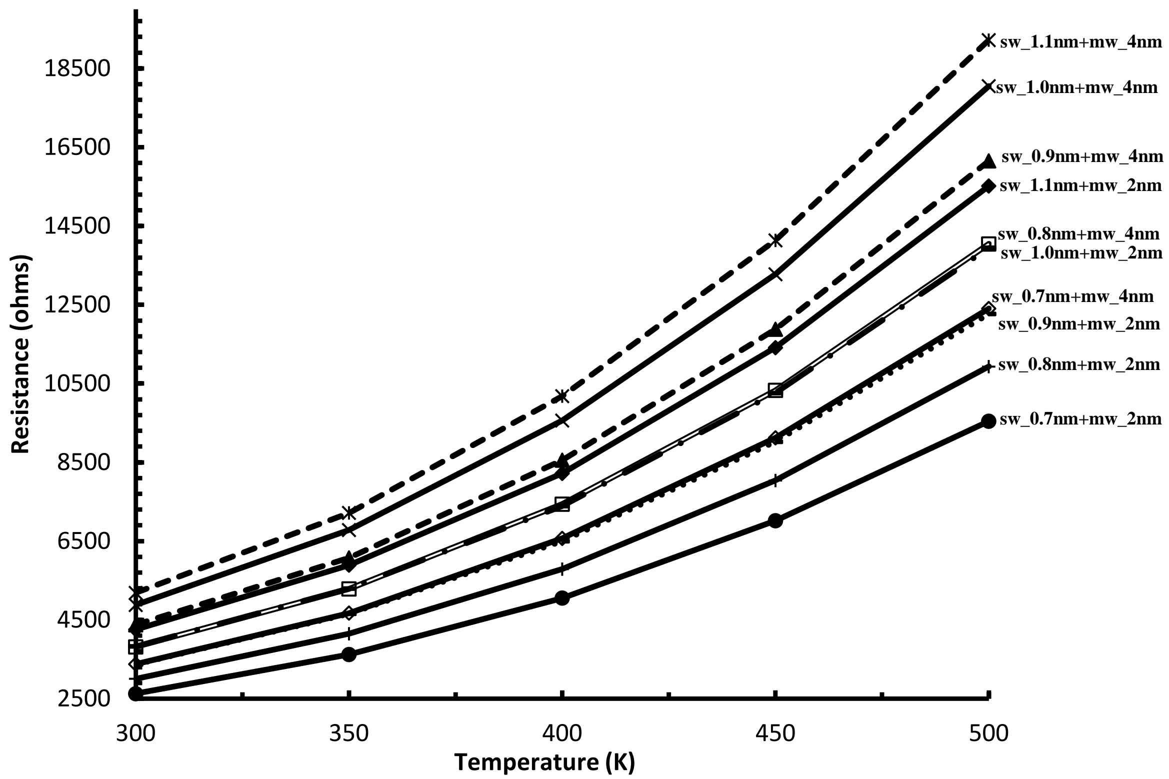


Figure 5.4 Variation of resistance of MCB structure 1 with different diameter of SWCNT bundle (0.7-1.1nm) and MWCNT Bundle (4nm &2nm) with respect to temperature at 22nm technology.

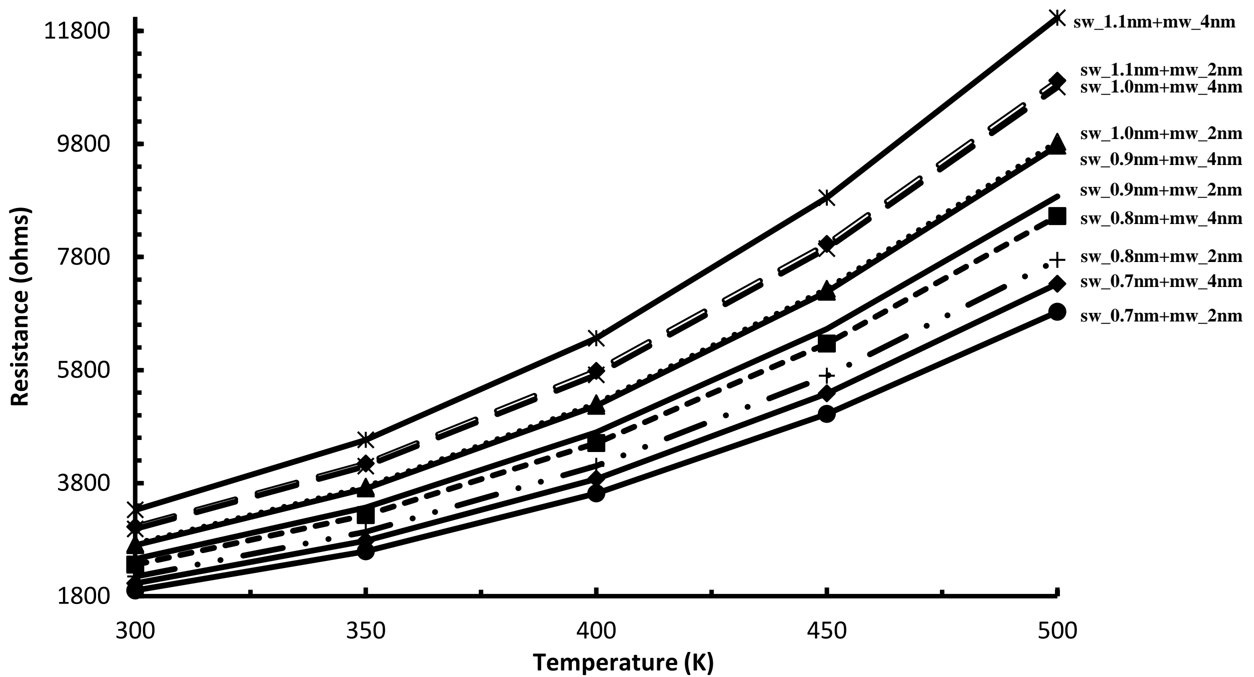


Figure 5.5 Variation of resistance of MCB structure 2 with different diameter of SWCNT bundle (0.7-1.1nm) and MWCNT Bundle (4nm &2nm) with respect to temperature at 22nm technology.

Fig. 5.6 shows the variation of resistance of SWCNT (with d=1nm) and MWCNT Bundle (d_{max}=32nm), MCB structure 1 and structure 2 with diameter of SWCNT (=0.7nm) and MWCNT Bundle (=2nm) with respect to temperature. The MCB1 and MCB2 with these tube diameter values offer least resistance. It is observed from the graph that resistance of each CNT bundle is less than the resistance of copper and MCB2 with the given tube diameters of SWCNT and MWCNT offers least resistance.

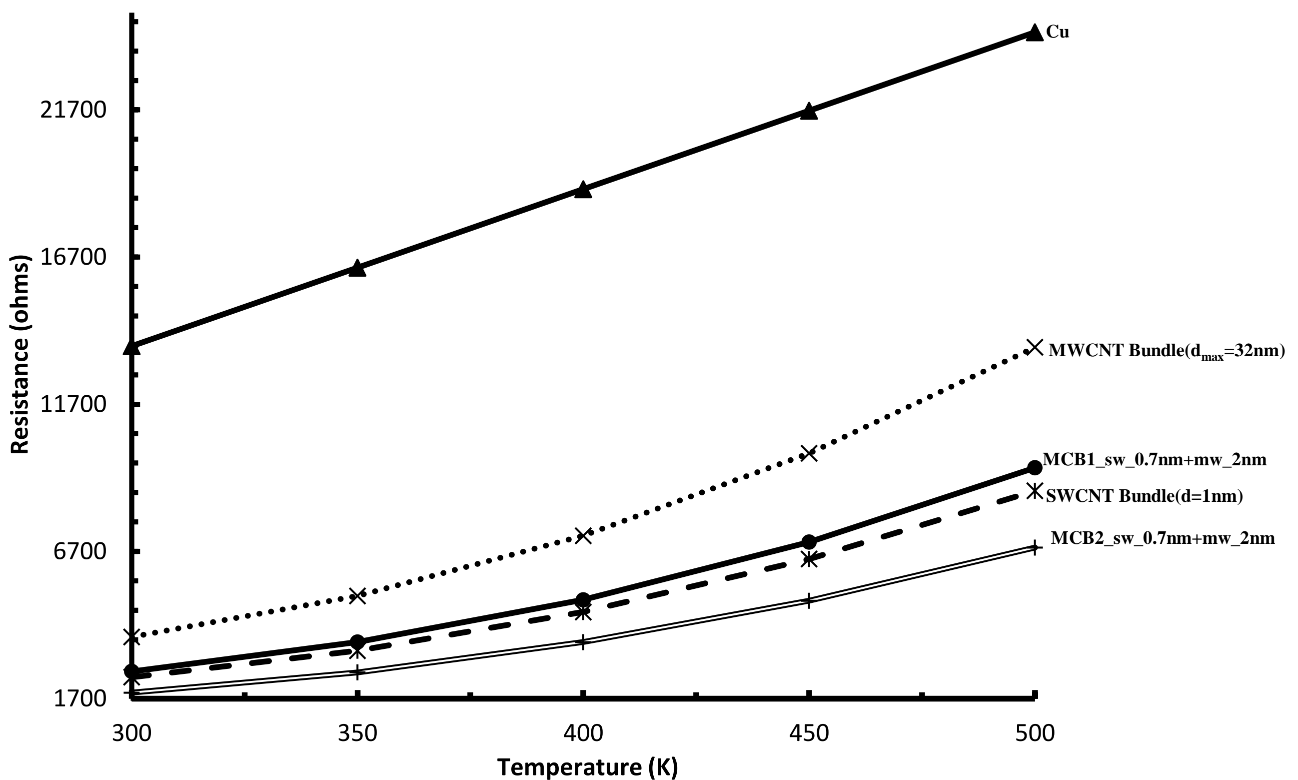


Figure 5.6 Variation of resistance of Cu, SWCNT (with d=1nm) and MWCNT Bundle (d_{max}=32nm), MCB structure 1 and structure 2 with diameter of SWCNT (=0.7nm) and MWCNT Bundle (=2nm) with respect to temperature at 22nm technology.

Table 5.1 shows the value of impedance parameters for Cu, SWCNT Bundle (with d=0.7nm-1.1nm) and MWCNT Bundle (with d_{max}=32nm) for 22nm technology at 300K. It has been noted that capacitance of both MWCNT bundle and SWCNT bundle is more than capacitance of Cu interconnect but the capacitance of MWCNT bundle is much lesser than SWCNT bundle and as the tube diameter increases, capacitance of SWCNT bundle decreases, but the inductance and resistance shows the opposite trend as depicted in the table 5.1. Note that capacitance and inductance values are independent of temperature.

Table 5.1 Resistance, Inductance and Capacitance values for Cu, SWCNT Bundle (with d=0.7nm-1.1nm) and MWCNT Bundle (with d_{max}=32nm) for 22nm technology at 300K

Interconnect Type	Inductance(pH)	Capacitance(pF)	Resistance(Ω)
SWCNT Bundle (d=0.7nm)	0.140	2.950	1708.230
SWCNT Bundle (d=0.8nm)	0.176	2.660	1928.556
SWCNT Bundle (d=0.9nm)	0.220	2.430	2202.508
SWCNT Bundle (d=1nm)	0.263	2.240	2428.672
SWCNT Bundle (d=1.1nm)	0.314	2.080	2685.168
MWCNT Bundle (dmax=32nm)	4490	0.105	3792.104
Cu	2030	0.015	13671.880

Table 5.2 gives the value of capacitance and inductance of MCB structure 1 and 2 at different diameters of SWCNT (0.7nm-1.1nm) and MWCNT (4nm &2nm). It is observed from these values MCB structures capacitance is comparable to the capacitance of copper and also their resistance is much lesser than the resistance of copper interconnects and as the tube diameter of SWCNT and MWCNT decreases, capacitance of both structures also decreases like resistance and inductance.

Table 5.2 Resistance, Inductance and Capacitance values for MCB, structure1 and structure 2 with different diameter of SWCNT bundle (0.7-1.1nm) and MWCNT Bundle (4nm &2nm) for 22nm technology at 300K

Structures	MCB Structure 1			MCB Structure 2		
Diameter of SWCNT and MWCNT	Inductance (nH)	Capacitance (pF)	Resistance (Ω)	Inductance (nH)	Capacitance (pF)	Resistance (Ω)
SW(d=0.7nm)&MW(d=4nm)	1.140	0.155	3376.466	0.683	0.150	2025.449
SW(d=0.8nm)&MW(d=4nm)	1.490	0.168	3814.395	0.908	0.162	2356.228
SW(d=0.9nm)&MW(d=4nm)	1.920	0.187	4375.375	1.170	0.180	2700.5
SW(d=1.0nm)&MW(d=4nm)	2.410	0.217	4877.171	1.440	0.208	2986.824
SW(d=1.1nm)&MW(d=4nm)	2.810	0.279	5185.488	1.760	0.264	3325.308
SW(d=0.7nm)&MW(d=2nm)	0.885	0.075	2625.823	0.691	0.072	1898.567
SW(d=0.8nm)&MW(d=2nm)	1.170	0.076	3004.953	0.894	0.074	2146.144
SW(d=0.9nm)&MW(d=2nm)	1.470	0.078	3370.009	1.160	0.075	2458.754
SW(d=1.0nm)&MW(d=2nm)	1.850	0.079	3828.016	1.420	0.076	2725.902
SW(d=1.1nm)&MW(d=2nm)	2.260	0.081	4253.936	1.740	0.078	3025.684

5.4 Performance Analysis

Temperature dependent performance analysis of SWCNT bundle, MWCNT bundle and MCB structures with different tube diameters of SWCNT and MWCNT has been studied in terms of propagation delay, power and power delay product (PDP) . Again in this chapter, Cu interconnect delay, power and PDP are used as normalizing parameters for CNT bundle interconnects delay, power and PDP respectively so that a relative measure of CNT interconnect delay and power with respect to that of copper interconnect can be obtained.

5.4.1 Temperature Dependent Delay Analysis

Fig. 5.7 shows the variation of delay of SWCNT bundle with respect to temperature for both old [6] and improved model of resistance. This result reveal that SWCNT bundle with an improved model gives better performance in terms of delay with rise in temperature compared to old model.

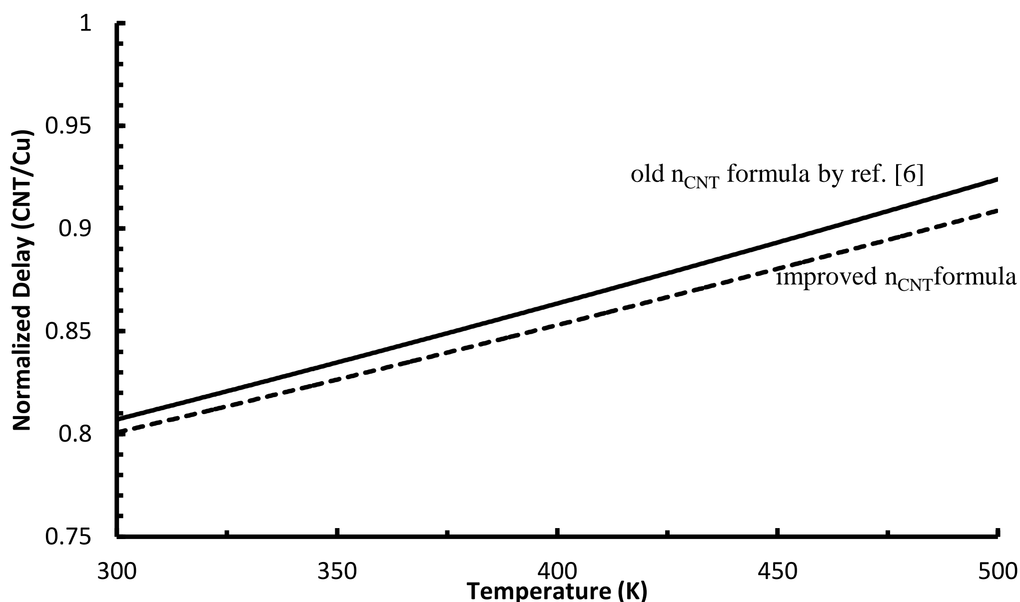


Figure 5.7 Normalized delay variation of SWCNT bundle (with diameter=1nm) with respect to temperature for new improved formula of n_{CNT} and old formula of n_{CNT} given by ref. [6] at 22nm technology.

Table 5.3 shows average relative improvement in accuracy of delay estimation using temperature dependent model instead of conventional temperature-independent model for different tube diameters of SWCNT. Conventional temperature independent delay analysis of SWCNT bundle done in chapter 4 is compared with temperature dependent analysis of SWCNT bundle. Difference in the

value of normalized delay has been observed. It is observed that on an average of 46% accuracy has been achieved in the delay estimation of SWCNT bundle interconnects at temperature 300K.

Table 5.3 Average relative improvement in accuracy of delay estimation using temperature dependent model instead of conventional temperature-independent model

Diameter of SWCNT(nm)	Temperature independent model	Temperature dependent model	Percentage change
0.7	0.921053	0.63964	43.99555
0.8	0.896761	0.605405	48.12572
0.9	0.878543	0.598198	46.86479
1	0.840081	0.581982	44.34828
1.1	0.834008	0.565766	47.41226

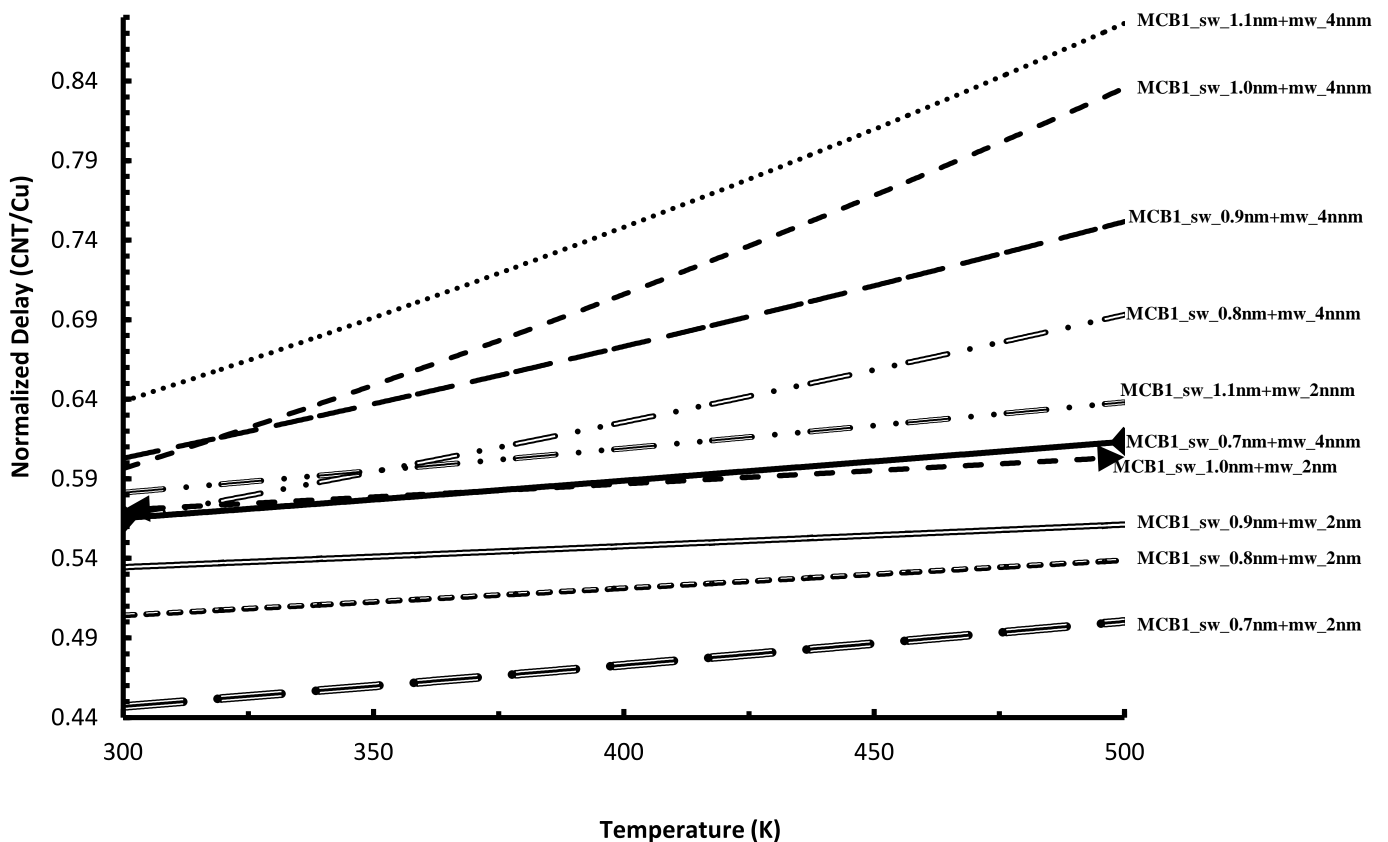


Figure 5.8 Normalized delay variation of MCB structure 1 with different diameter of SWCNT (0.7-1.1nm) and MWCNT (4nm &2nm) with respect to temperature at 22nm technology.

Fig. 5.8 and Fig. 5.9 show the normalized propagation delay of MCB1 and MCB2 as a function of temperature. It is observed that propagation delay is increasing with rise in temperature. Result further reveals that MCB1and MCB2 of lower tube diameter of both SWCNT and MWCNT has lower delay. This is due to the decrease in value of capacitance and resistance of MCB1 and MCB2 as diameter decreases. It is also observed that change in tube diameter of both SWCNT and MWCNT have significant effect on normalized delay of MCB1, but for MCB2 change in tube diameter of MWCNT do not have significant effect on normalized delay as they have in less amount.

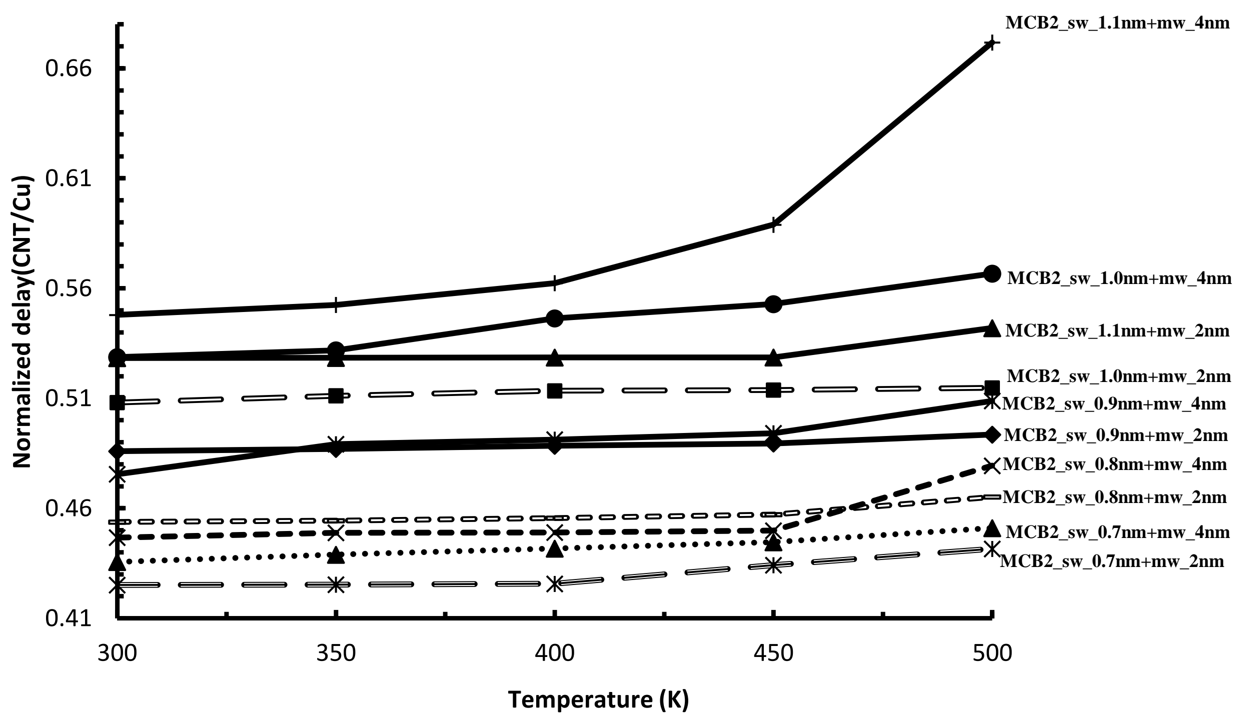


Figure 5.9 Normalized delay variation of MCB structure 2 with different diameter of SWCNT (0.7-1.1nm) and MWCNT (4nm &2nm) with respect to temperature at 22nm technology.

Fig.5.10 shows the normalized delay variation of MCB1 and MCB2 with diameter of SWCNT=0.7nm and MWCNT=2nm, MWCNT bundle and SWCNT bundle with respect to temperature. It is observed that MCB1 and MCB2 perform even much better than MWCNT bundle and SWCNT bundle. This is due to the dominance of smaller value of capacitance of MCB structure 1 than the capacitance of SWCNT bundle and MWCNT bundle and MCB2 offers least delay. So, it

MCB2 is a better alternative to copper interconnect out of all the CNTs discussed here for high speed applications.

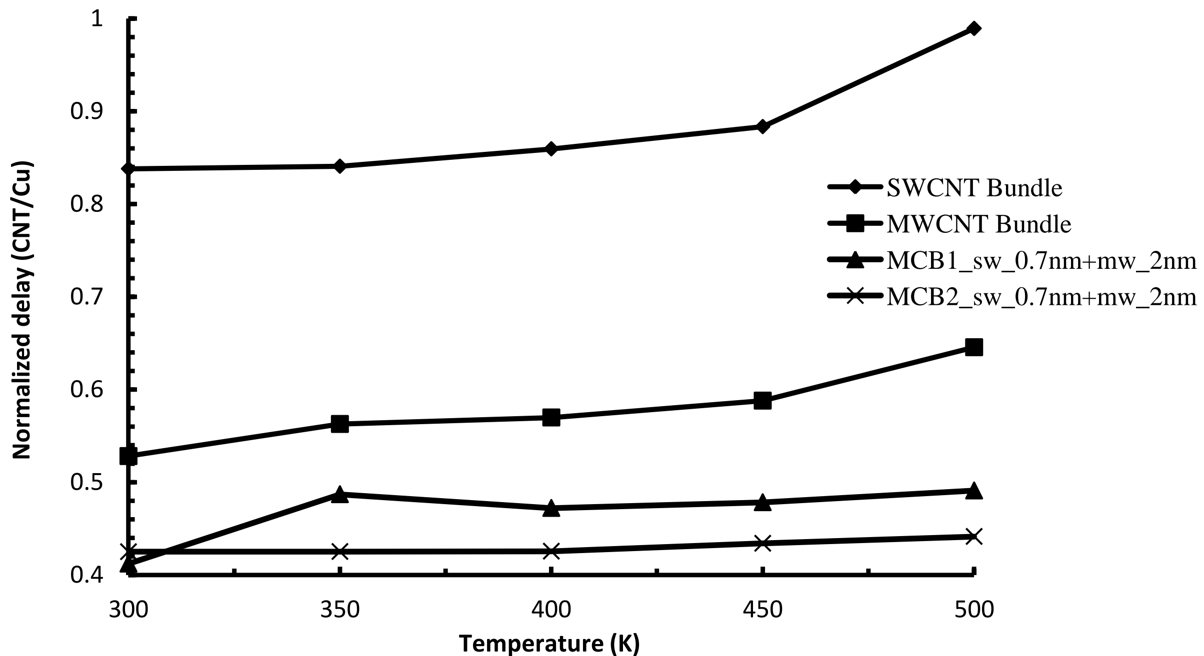


Figure 5.10 Normalized delay variation of SWCNT Bundle (with d=1nm) and MWCNT Bundle (d_{max}=32nm), MCB1 and MCB 2 with diameter of SWCNT (0.7nm) and MWCNT (2nm) with respect to temperature at 22nm technology.

5.4.2 Temperature Dependent Power Analysis

Table 5.4,5.5 and 5.6 shows value of normalized power of MCB structure 1 and 2 at different diameters of SWCNT (0.7nm-1.1nm) and MWCNT (4nm &2nm), SWCNT bundle (d=1nm) and MWCNT bundle (d_{max}=32nm) respectively with respect to temperature. It is observed that normalized power of SWCNT bundle is greater than the normalized power of both MCB structures, but MWCNT and MCB are comparable in terms of normalized power and according to all these results, out off all the CNT bundles discussed here MCB2 with SWCNT diameter=0.7nm and MWCNT diameter= 2nm would be the best alternative to copper interconnect, as it has both normalized delay and normalized power lesser than SWCNT bundle, MWCNT bundle and MCB 1 with same diameters of SWCNT and MWCNT.

Table 5.4 Normalized power values for MCB1 and MCB 2 with different diameter of SWCNT (0.7-1.1nm) and MWCNT Bundle (4nm &2nm) for temperature range (300-500K) for 22nm technology

Structures	MCB STR1					MCB STR2				
Temperature / Diameter	300K	350K	400K	450K	500K	300K	350K	400K	450K	500K
SW=0.7nm MW=2nm	1.09	1.13	1.17	1.21	1.23	1.09	1.12	1.17	1.22	1.25
SW=0.8nm MW=2nm	1.09	1.12	1.16	1.21	1.23	1.09	1.12	1.17	1.22	1.24
SW=0.9nm MW=2nm	1.09	1.12	1.16	1.20	1.21	1.09	1.12	1.16	1.21	1.17
SW=1.0nm MW=2nm	1.09	1.12	1.16	1.20	1.21	1.09	1.12	1.15	1.21	1.23
SW=1.1nm MW=2nm	1.09	1.11	1.15	1.19	1.21	1.09	1.12	1.16	1.21	1.22
SW=0.7nm MW=4nm	1.13	1.17	1.21	1.25	1.25	1.09	1.16	1.10	1.27	1.29
SW=0.8nm MW=4nm	1.14	1.17	1.21	1.25	1.25	1.14	1.17	1.22	1.27	1.30
SW=0.9nm MW=4nm	1.15	1.18	1.21	1.24	1.24	1.15	1.18	1.22	1.28	1.29
SW=1.0nm MW=4nm	1.17	1.20	1.22	1.24	1.24	1.16	1.20	1.24	1.21	1.29
SW=1.1nm MW=4nm	1.20	1.22	1.22	1.23	1.24	1.19	1.23	1.26	1.30	1.30

Table 5.5 Normalized power values for SWCNT Bundle with different tube diameter (d=0.7-1.1nm) for temperature range (300-500K) for 22nm technology

Temperature / Diameter of SWCNT (nm)	300K	350K	400K	450K	500K
0.7	3.13	3.24	3.39	3.64	3.84
0.8	2.90	3.04	3.19	3.41	3.59
0.9	2.72	2.87	3.01	3.23	3.37
1.0	2.54	2.68	2.88	3.08	3.21
1.1	2.42	2.57	2.77	2.96	3.09

Table 5.6 Normalized power values for MWCNT Bundle (with d_{max}=32nm) for temperature range (300-500K) for 22nm technology

Temperature (K)	Normalized power (MWCNT/Cu)
300	1.08
350	1.13
400	1.17
450	1.22
500	1.22

5.4.3 Temperature Dependent PDP Analysis

Fig. 5.11 and 5.12 show variation of normalized PDP of MCB 1 and MCB2 with different diameter of SWCNT (0.7 to1.1nm) and MWCNT (4nm &2nm) with respect to temperature. It is observed that PDP is increasing with rise in temperature. Result further reveals that MCB1and MCB2 of lower tube diameter of both SWCNT and MWCNT has lower PDP.

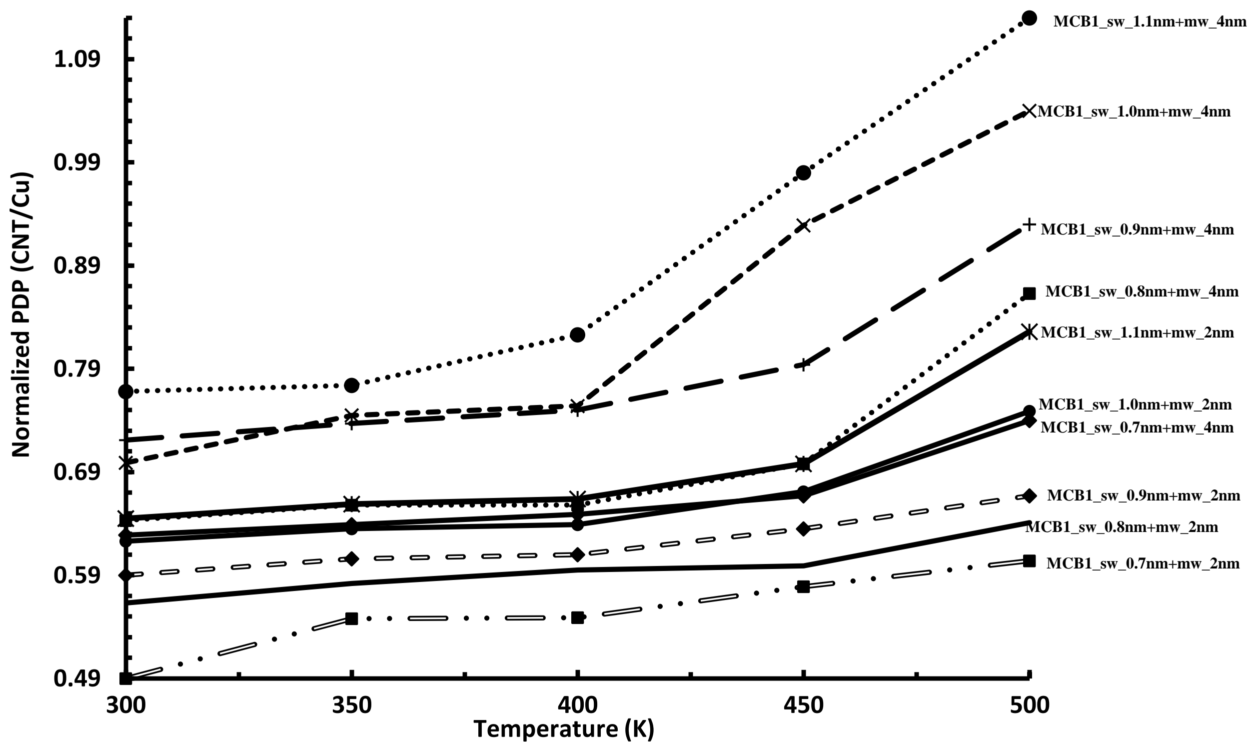


Fig. 5.11 Normalized PDP variation of MCB structure 1 with different diameter of SWCNT (0.7-1.1nm) and MWCNT (4nm &2nm) with respect to temperature at 22nm technology.

This is due to the decrease in value of capacitance and resistance of MCB1 and MCB2 as diameter decreases. Also change in tube diameter of both SWCNT and MWCNT have significant effect on

normalized delay of MCB1, but for MCB2 change in tube diameter of MWCNT do not have significant effect on normalized delay as they have in less amount.

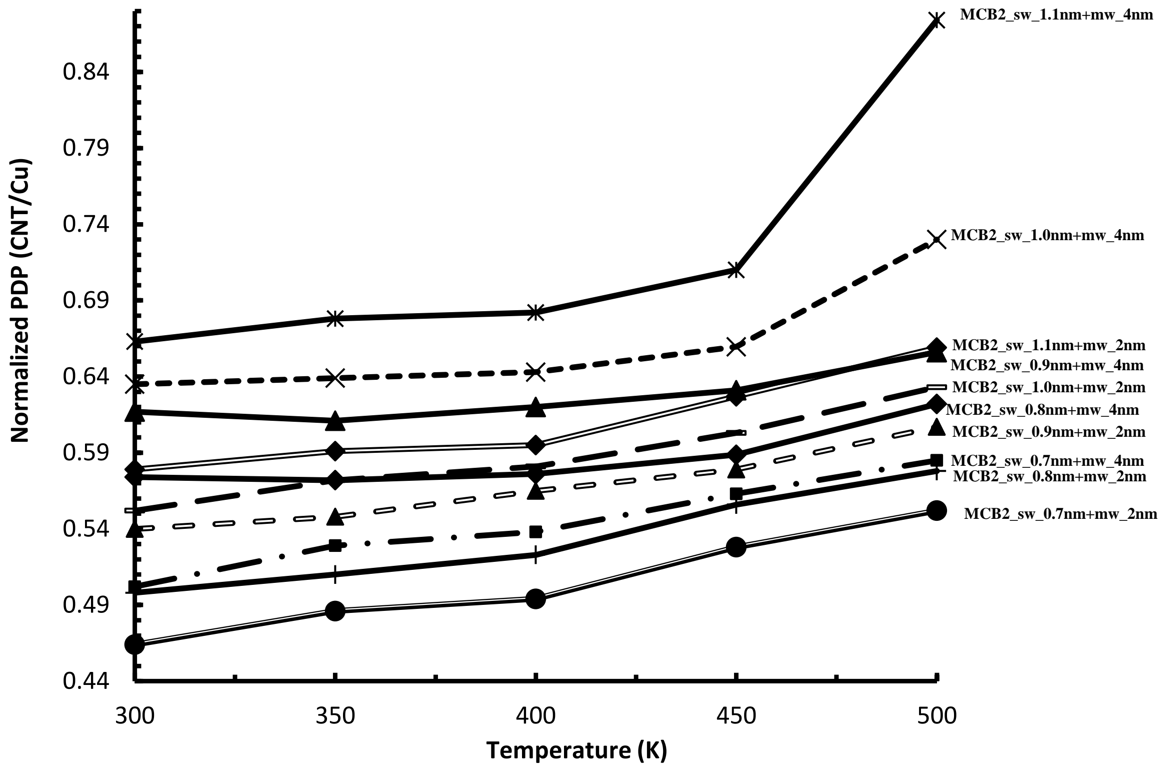


Figure 5.12 Normalized PDP variation of MCB 2 with different diameter of SWCNT (0.7-1.1nm) and MWCNT (4nm &2nm) with respect to temperature at 22nm technology.

Fig. 5.13 shows variation of normalized PDP of SWCNT bundle (d=1nm), MWCNT bundle (d_{max}=32nm) and MCB1 MCB2 with optimized diameter of SWCNT and MWCNT with respect to temperature. Results reveal that PDP of SWCNT is greater than PDP of copper and PDP of MWCNT bundle MCB 1 and MCB 2 is lesser than PDP of copper in which MCB2 with SWCNT diameter of 0.7nm and MWCNT of diameter 2nm is giving the best performance in terms of delay and power.

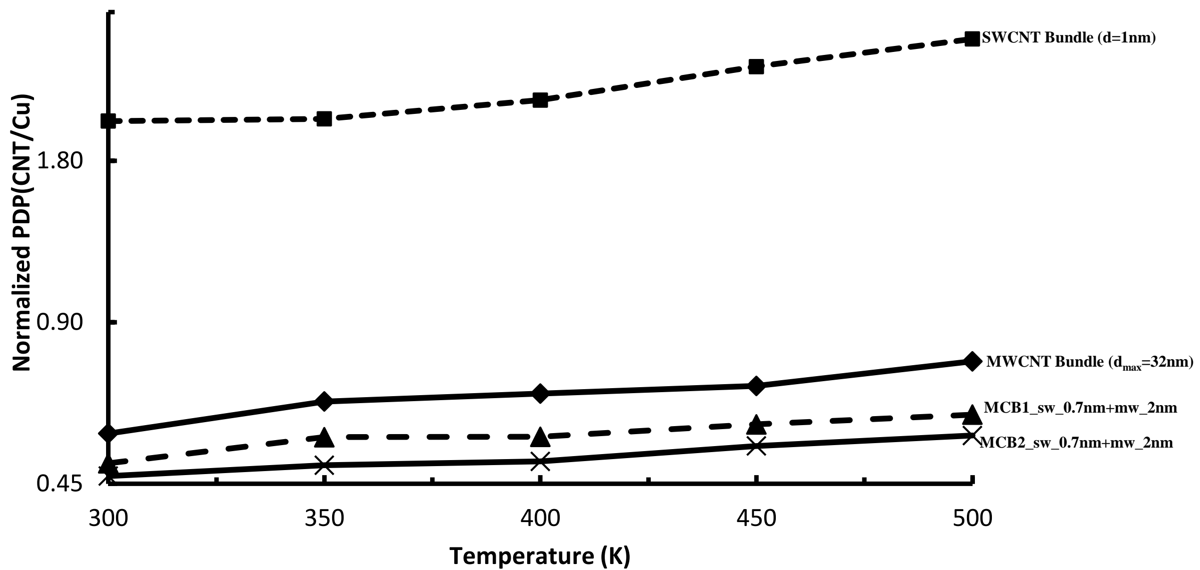


Figure 5.13 Normalized PDP variation of SWCNT (with d=1nm) and MWCNT Bundle (d_{max}=32nm), MCB structure 1 and structure 2 with diameter of SWCNT (0.7nm) and MWCNT (2nm) with respect to temperature at 22nm technology.

5.5 CONCLUSION

In this chapter temperature dependent analysis of CNT bundle interconnects has been done. It has been analyzed that the due to the dependence of mean free path on temperature resistance of all CNTs is increasing with rise in temperature and it is inaccurate to consider same value of mean free path at different temperature. Results reveal 46% average relative improvement in accuracy of delay estimation using temperature dependent model instead of conventional temperature-independent model. Although the resistance of MWCNT bundle is greater than SWCNT bundle interconnect but its capacitance value is very less. So in mixed bundle CNT, as we have the combination of both, it offers lesser propagation delay as compared to SWCNT bundle and MWCNT bundle interconnect when the optimum diameter of SWCNT and MWCNT are chosen. It is also revealed by the SPICE simulation results that MCB structure2 is offering lesser propagation delay as compared to MCB structure1 as it has the more number of maximum current conducting CNTs (i.e. SWCNT). It has also been observed that MCB2 with optimum tube diameters of SWCNT and MWCNT offers least PDP compared to MCB1, SWCNT bundle and MWCNT bundle. Hence MCB2 interconnect is the best alternative which can be used as a future VLSI interconnect keeping in mind both high speed and low power requirements.

CHAPTER – 6

CONCLUSION

Performance analysis of mixed CNT bundle VLSI interconnects at 22nm technology node is presented in the dissertation. As the technology is scaling down, the problems encountered with copper interconnects are briefly discussed which reveal the need for an alternative material to Cu as VLSI interconnect. One of the proposed alternatives i.e. CNTs and its types has been discussed here. Due to device scaling, thermal issues have now emerged as a major challenging factor in the possible usage of nanotubes for designing high performance integrated circuits. The high performance integrated circuits often operate at temperatures much greater than room temperature. So, it is critical to understand how their electrical characteristics will vary at temperatures greater than room temperature. The temperature dependent performance analysis has been done for SWCNT, MWCNT and mixed CNT bundle structures. An average percentage change of 46% has been observed in the delay estimation of SWCNT bundle using the improved temperature dependent model instead of using the old temperature independent model. It has been observed that the propagation delay of an interconnect increases with rise in temperature. Also the change in the performance of SWCNT bundle has been observed using the accurate formula for number of CNTs in the bundle instead of using the formula given in literature [6]. Temperature dependent performance analysis of two structures of MCB (MCB1 and MCB2) has been done and comparisons are made to Cu, SWCNT bundle and MWCNT bundle interconnect. The dependence of performance of these two structures on tube diameter of SWCNT and MWCNT has also been studied. Simulated results reveal that due to the decrease in the resistance and capacitance of MCB with decrease in tube diameter, MCB structures with lower tube diameter offers lesser delay. It has also been observed that out of all types CNTs discussed in this study, MCB2 (d_{SWCNT} =0.7nm & d_{MWCNT} =2nm) performs best in terms of delay and PDP due to its much lower resistance and capacitance value. Hence MCB structure 2 has been proposed as preferred material for VLSI interconnect keeping in mind both high speed and low power requirements.

LIST OF PUBLICATIONS

[1]. Amandeep Kaur, Mayank Kumar Rai, "Temperature Dependent Delay Analysis of SWCNT Bundle as VLSI Interconnects", *International Multi Track Conference on Science, Engineering & Technical Innovation* pp. 578-582, June 2014.

[2]. Amandeep Kaur, Mayank Kumar Rai, "Temperature Dependent Delay Analysis in MWCNT Bundle as VLSI Interconnects", *proc. Second International conference on Emerging Research in Computing*, *Information, Communication and Applications (ERCICA) (ELSVEIR),* August 2014.

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APPENDIX

A.1 PTM level 54 model

.model nmos nmos level = 54

```
+version = 4.0      binunit = 1         paramchk= 1         mobmod = 0
+capmod = 2         igcmod = 1          igbmod = 1          geomod = 1
+diomod = 1         rdsmod = 0          rbodymod= 1         rgatemod= 1
+permod = 1         acnqsmod= 0         trnqsmod= 0         +tnom = 27
toxe = 6.5e-010     toxp = 4e-010       toxm = 6.5e-010     +dtox = 2.5e-010
epsrox = 3.9        wint = 5e-009       lint = 1.35e-009    +ll = 0 wl = 0
lln = 1             wln = 1             +lw = 0             ww = 0
lwn = 1             wwn = 1             +lwl = 0            wwl = 0
xpart = 0           toxref = 6.5e-010   xl = -9e-9          +dlcig = 1.35e-009
+vth0 = 0.3692      k1 = 0.2            k2 = 0              k3 = 0 +k3b = 0
w0 = 2.5e-006       dvt0 = 1            dvt1 = 2            +dvt2 = 0
dvt0w = 0           dvt1w = 0           dvt2w = 0           +dsub = 0.078
minv = 0.05         voffl = 0           dvtp0 = 1e-011      +dvtp1 = 0.1
lpe0 = 0            lpeb = 0            xj = 7.2e-009       +ngate = 1e+023
ndep = 1.2e+019     nsd = 2e+020        phin = 0            +cdsc = 0
cdscb = 0           cdscd = 0           cit = 0             +voff = -0.13
nfactor = 2.3       eta0 = 0.0045       etab = 0            +vfb = -1.058
u0 = 0.0181         ua = -5e-010        ub = 1.7e-018       +uc = 0
vsat = 200000       a0 = 1              ags = 0             +a1 = 0
a2 = 1              b0 = 0              b1 = 0 +            keta = 0.04
dwg = 0             dwb = 0             pclm = 0.06         +pdiblc1 = 0.001
pdiblc2 = 0.001     pdiblcb = -0.005    drout = 0.5         +pvag = 1e-020
delta = 0.01        pscbe1 = 2.0e+009   pscbe2 = 1e-007     +fprout = 0.2
pdits = 0.01        pditsd = 0.23       pditsl = 2300000    +rsh = 5
rdsw = 60           rsw = 30            rdw = 30            +rdswmin = 0
rdwmin = 0          rswmin = 0          prwg = 0            +prwb = 0
wr = 1              alpha0 = 0.074      alpha1 = 0.005      +beta0 = 30
```

agidl = 0.0002	bgidl = 2.1e+009	cgidl = 0.0002	+egidl = 0.8
aigbacc = 0.012	bigbacc = 0.0028	cigbacc = 0.002	+nigbacc = 1
aigbinv = 0.014	bigbinv = 0.004	cigbinv = 0.004	+eigbinv = 1.1
nigbinv = 3	aigc = 0.0213	bigc = 0.0025889	+cigc = 0.002
aigsd = 0.0213	bigsd = 0.0025889	cigsd = 0.002	+nigc = 1
poxedge = 1	pigcd = 1	ntox = 1	+xrcrg1 = 12
xrcrg2 = 5	+cgso = 7e-011	cgdo = 7e-011	cgbo = 0
cgdl = 7.5e-013	+cgsl = 7.5e-013	clc = 1e-007	cle = 0.6
cf = 1.1e-010	+ckappas = 0.6	ckappad = 0.6	vfbcv = -1
acde = 195	+moin = 15	noff = 1	voffcv = 0
+kt1 = -0.154	kt1l = 0	kt2 = 0.022	ute = -1.1
+ua1 = 1e-009	ub1 = -1e-018	uc1 = -5.6e-011	prt = 0
+at = 33000	+fnoimod = 1	tnoimod = 0	noia = 6.25e+041
noib = 3.125e+026	+noic = 8.75e+009	em = 41000000	af = 1
ef = 1	+kf = 0	tnoia = 1.5	tnoib = 3.5
ntnoi = 1	+jss = 1.2e-006	jsws = 2.4e-013	jswgs = 2.4e-013
njs = 1	+ijthsfwd= 0.1	ijthsrev= 0.1	bvs = 10
xjbvs = 1	+jsd = 1.2e-006	jswd = 2.4e-013	jswgd = 2.4e-013
xjbvd = 1	+pbs = 1	cjs = 0.0018	mjs = 0.5
pbsws = 1	+cjsws = 1.2e-010	mjsws = 0.33	cjswgs = 2.1e-010
cjd = 0.0018	+cjswd = 1.2e-010	mjswd = 0.33	pbswgd = 1
cjswgd = 2.1e-010	+mjswgd = 0.33	tpb = 0	tcj = 0
tpbsw = 0	+tcjsw = 0	tpbswg = 0	tcjswg = 0
xtis = 3	+dmcg = 0	dmci = 0	dmdg = 0
dmcgt = 0	+dwj = 0	xgw = 0	xgl = 0
+rshg = 0.4	gbmin = 1e-010	rbpb = 5	rbpd = 15
+rbps = 15	rbdb = 15	rbsb = 15	ngcon = 1

.model pmos pmos level = 54

+version = 4.0	binunit = 1	paramchk= 1	mobmod = 0
+capmod = 2	igcmod = 1	igbmod = 1	geomod = 1
+diomod = 1	rdsmod = 0	rbodymod= 1	rgatemod= 1

+permod = 1 acnqsmod= 0 trnqsmod= 0 +tnom = 27
toxe = 6.7e-010 toxp = 4e-010 toxm = 6.7e-010 +dtox = 2.7e-010
epsrox = 3.9 wint = 5e-009 lint = 1.35e-009 +ll = 0
wl = 0 lln = 1 wln = 1 +lw = 0
ww = 0 lwn = 1 wwn = 1 +lwl = 0
wwl = 0 xpart = 0 toxref = 6.7e-010 xl = -9e-9
+dlcig = 1.35e-009 +vth0 = -0.25399 k1 = 0.2 k2 = -0.01
k3 = 0 +k3b = 0 w0 = 2.5e-006 dvt0 = 1
dvt1 = 2 +dvt2 = -0.032 dvt0w = 0 dvt1w = 0
dvt2w = 0 +dsub = 0.1 minv = 0.05 voffl = 0
dvtp0 = 1e-011 +dvtp1 = 0.05 lpe0 = 0 lpeb = 0
xj = 7.2e-009 +ngate = 1e+023 ndep = 4.4e+018 nsd = 2e+020
phin = 0 +cdsc = 0 cdscb = 0 cdscd = 0
cit = 0 +voff = -0.13 nfactor = 2.3 eta0 = 0.0037
etab = 0 +vfb = -1.058 u0 = 0.0023 ua = -5e-010
ub = 1.6e-018 +uc = 0 vsat = 78000 a0 = 1
ags = 1e-020 +a1 = 0 a2 = 1 b0 = 0
b1 = 0 +keta = -0.047 dwg = 0 dwb = 0
pclm = 0.1 +pdiblc1 = 0.001 pdiblc2 = 0.001 pdiblcb = 3.4e-008
drout = 0.6 +pvag = 1e-020 delta = 0.01 pscbe1 = 2e+009
pscbe2 = 9.58e-007 +fprout = 0.2 pdits = 0.08 pditsd = 0.23
pditsl = 2300000 +rsh = 5 rdsw = 60 rsw = 30
rdw = 30 +rdswmin = 0 rdwmin = 0 rswmin = 0
prwg = 096 +prwb = 0 wr = 1 alpha0 = 0.074
alpha1 = 0.005 +beta0 = 30 agidl = 0.0002 bgidl = 2.1e+009
cgidl = 0.0002 +egidl = 0.8 aigbacc = 0.012 bigbacc = 0.0028
cigbacc = 0.002 +nigbacc = 1 aigbinv = 0.014 bigbinv = 0.004
cigbinv = 0.004 +eigbinv = 1.1 nigbinv = 3 aigc = 0.012731
bigc = 0.00115 +cigc = 0.0008 aigsd = 0.012731 bigsd = 0.00115
cigsd = 0.0008 +nigc = 1 poxedge = 1 pigcd = 1
ntox = 1 +xrcrg1 = 12 xrcrg2 = 5 +cgso = 7e-011

cgdo = 7e-011 cgbo = 0 cgdl = 3e-011 +cgsl = 3e-011

clc = 1e-007 cle = 0.6 cf = 1.1e-010 +ckappas = 0.6

ckappad = 0.6 vfbcv = -1 acde = 1 +moin = 15

noff = 1 voffcv = 0 +kt1 = -0.14 kt1l = 0

kt2 = 0.022 ute = -1.1 +ua1 = 1e-009 ub1 = -1e-018

uc1 = -5.6e-011 prt = 0 +at = 33000 +fnoimod = 1

tnoimod = 0 noia = 6.25e+041 noib = 3.125e+026 +noic = 8.75e+009

em = 41000000 af = 1 ef = 1 +kf = 0

tnoia = 1.5 tnoib = 3.5 ntnoi = 1 +jss = 2e-007

jsws = 4e-013 jswgs = 4e-013 njs = 1 +ijthsfwd= 0.1

ijthsrev= 0.1 bvs = 10 xjbvs = 1 +jsd = 2e-007

jswd = 4e-013 jswgd = 4e-013 xjbvd = 1 +pbs = 1

cjs = 0.0015 mjs = 0.5 pbsws = 1 +cjsws = 9.4e-011

mjsws = 0.33 cjswgs = 2e-010 cjd = 0.0015 +cjswd = 9.4e-011

mjswd = 0.33 pbswgd = 1 cjswgd = 2e-010 +mjswgd = 0.33

tpb = 0 tcj = 0 tpbsw = 0 +tcjsw = 0

tpbswg = 0 tcjswg = 0 xtis = 3 +dmcg = 0

dmdg = 0 dmcgt = 0 xgw = 0 +xgl = 0

+rshg = 0.1 gbmin = 1e-012 rbpb = 50 rbpd = 50

+rbps = 50 rbdb = 50 rbsb = 50 ngcon = 1