Design of Two-stage High Gain Operational Amplifier Using Current Buffer Compensation for Low Power Applications

Thesis submitted in partial fulfillment of the requirement for the award of degree of

Master of Technology

in

VLSI Design & CAD

Submitted by

Sachin Kumar Rajput
Roll No. - 60761018

Under the supervision of

Mr. B. K. Hemant
Project Faculty, ECED
Thapar University

Department of Electronics & Communication Engineering
Thapar University
Patiala-147004, INDIA
June - 2009

CERTIFICATE

I hereby declare that the work which is being presented in the thesis entitled, "**Design of Two-stage High Gain Operational Amplifier Using Current Buffer Compensation for Low Power Applications**", in partial fulfillment of the requirements for award of degree of **Master of Technology in VLSI Design and CAD** at **Thapar University, Patiala**, is an authentic record of my own work carried out under the supervision of **Mr. B. K. Hemant, Project Faculty** and refers other researcher's work which are duly listed in reference section.

The matter embodied in this thesis has not been submitted for the award of any other degree of this or any other university.

Sachin

Date: 15-07-09

Sachin Kumar Rajput

Roll. No. – 60761018

This is to certify that the above statement made by the candidate is correct and true to the best of knowledge.

Mr. B. K. HEMANT
Project Faculty, ECED
Thapar University,
Patiala

Counter signed by

Dr. A. K. CHATTERJEE
Professor and Head,
Electronics & Communication Engg. Department,
Thapar University,
Patiala-147004.

Dr. R. K. SHARMA 21/7/09
Dean of Academic Affairs,
Thapar University,
Patiala-147004

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Abstract

A need for high bandwidth operational amplifiers exists for certain applications. This requires research in the area of op amp bandwidth extension without affecting other parameters drastically. This thesis discusses the existing compensation methods for operational amplifiers and current buffer compensation approach has been adopted to design a high gain low power operational amplifier. This approach provides improved gain-bandwidth product (GBW) with good swing. The proposed classic two-stage op amp produces an open loop gain above 78 dB, gain- bandwidth product (GBW) of 5.82 MHz and 63.9^{o} phase margin in 0.35 μm CMOS technology. The circuit is operated at the supply voltage of 3.3 V with power dissipation of 144.3 μW.

The ability of the method adopted, to use the smaller compensation capacitor, C_c, which improves the slew rate, also beneficial for the area of compensation circuit.

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Chapter 1

Introduction

1.1 Background

Operational amplifiers (op amps) are the most versatile and an integral part of many analog and mixed-signal systems. They are employed from dc bias applications to high speed amplifiers and filters. General purpose op amps can be used as buffers, summers, integrators, differentiators, comparators, negative impedance converters, and many other applications. Its performance makes significant impact on the analog systems. With the improved computer aided design (CAD) tools, advancements of semiconductor modeling, steady miniaturization of transistor scaling, and the advanced fabrication processes, the integrated circuit market is growing rapid and continuously. Nowadays, due to the industry trend of applying standard process technologies to implement both analog circuits and digital circuits on the same chip, complementary metal-oxide semiconductor (CMOS) technology has become dominant over bipolar technology for analog circuit design in a mixed-signal system. While many digital circuits can be adapted to a smaller device level with a smaller power supply, most existing analog circuitry requires considerable change or even a redesign to accomplish the same feat. With transistor length being scaled down to a few tens of nanometers, analog circuits are becoming increasingly more difficult to improve upon. So, when transistor is scaled, the higher becomes its packing density, the higher its circuit speed, and the lower its power dissipation [1]. The rules for analog circuits are quite different to those applied to digital circuits. Voltage scaling plays important role in low power circuit design. However analog circuits benefit marginally from scaling, as the minimum size transistors cannot be used in analog circuits because of noise and offset voltage constraints. The major difference is the fundamental limits to the reduction of the power consumption. Decreasing, the supply voltage unfortunately does not reduce the power consumption of analog circuits. This is mainly due to the fact that the power consumption of analog circuits at a given temperature is basically set by the required signal-to-noise ratio (SNR) and the frequency of operation (or the required bandwidth).

In an effort to increase the intrinsic gain of CMOS devices, the trend in the MOSFET design industry is to shrink the gate oxide thickness, t_{ox}, which unfortunately reduced the

tolerance at the gate for high voltage levels. So, for reliability purposes, it is advantageous to reduce the maximum voltage supply V_{DD} but this trend of supply voltage reduction forces analog designers to face challenges such as reduced input common mode range, output swing and linearity. Designing of high-performance analog circuits is becoming more challenging with the persistent trend toward reduced supply voltages as V_{T0} does not scale in a linear fashion with the reduction in minimum device length at the same rate as V_{DD}. Some fabrication processes offer low V_{T0} which suites for analog blocks.

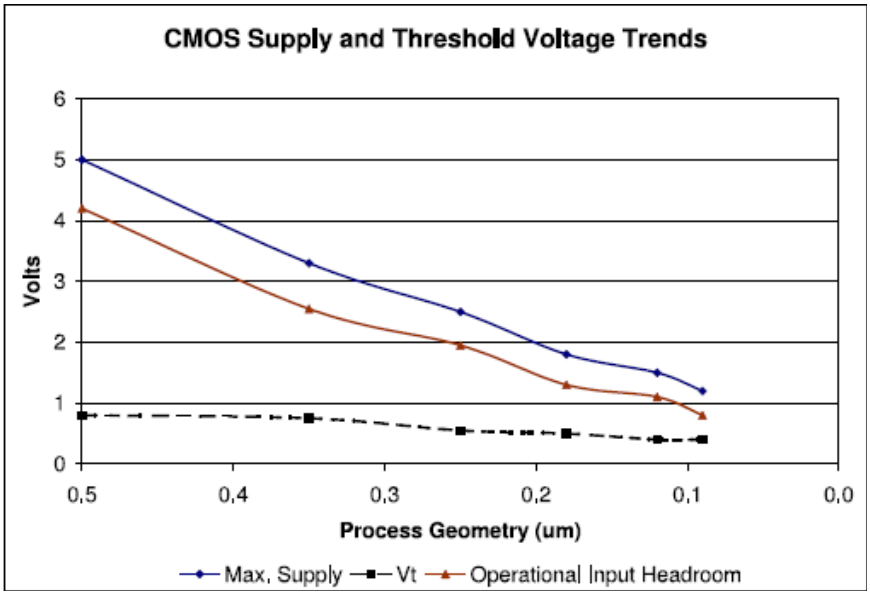

Figure 1.1: CMOS operating voltage trends in advanced silicon processes [2].

Operational amplifiers with moderate DC gains, high output swings and reasonable open-loop gain bandwidth product (*GBW*) are usually implemented with two-stage structures. The open loop gain of op amps in CMOS technology is lower compared to bipolar counterpart due to the inherently lower transconductance of CMOS devices as well as the gain reduction due to short channel effects that come into play for submicron CMOS processes. As a result gain enhancing methods often required to improve the gain. These methods require more complicated circuit structures and higher power supply voltage, and may produce a limited output voltage swing. Multiple stage amplifiers may be used for higher gain analog circuit designs [3]. To achieve high gain, a conventional cascode amplifier, which increases the gain by stacking up transistors, is not suitable in low-voltage design as the cascode structure results in small voltage swings. Instead, a

multistage amplifier is widely used to boost the gain by increasing the number of gain stages horizontally. However, all multistage amplifiers suffer from the closed-loop stability problem due to the presence of multiple poles. Different frequency-compensation topologies for multistage amplifiers have been used in different circuits. Nested-Miller compensation (NMC) is a basic well-known technique for compensating multistage amplifiers but it suffers from reduced bandwidth when gain stages increases. Some other techniques also have been used recently with some modification to the NMC. However, as all published compensation topologies use passive capacitive-feedback networks, the bandwidth of the amplifier is still limited for high-speed applications in low-power condition. However in the recent time some techniques has been proposed which reduced the compensation capacitor value effectively which results in greatly reduced physical dimension and both the bandwidth and transient responses are improved.

1.2 Motivation

The design of complex systems with analog, digital, and switched-capacitor building blocks integrated on one chip suffers from large signal variations on the power supply lines. Especially in those cases where low-level signals have to be measured, the use and development of high performance amplifiers are necessary. In analog building blocks, the main building blocks are operational transconductance amplifiers (OTA's). For this reason the performance of such amplifiers must be studied and analyzed as function of the power supply variations [4]. The performance of a system influenced by power supply variations can be described by the power supply rejection ratio (PSRR).

Performance of an op amp depends on numerous electrical characteristics, e.g., gain-bandwidth, slew rate common-mode range output swing offset etc. Two stage operational amplifiers (op amps) are often used to achieve both high dc gain and large output voltage swing. These op amps require frequency compensation. A current buffer in series to the Miller compensation capacitor is one of the possible solutions. It is very efficient both for PSRR and gain bandwidth (GBW) and does not reduce the op amp output swing unlike the voltage buffer approach [5]. This approach also gives a tradeoff between power consumption and area of compensation circuit by reducing the required value of compensation capacitor which suited well where the heavy capacitive load must be

driven. Ability to use smaller C_c provides a higher degree-of-freedom in trading noise performance with power consumption.

1.3 Applications

There are many applications in which high gain low power op amp with flexible noise performance can be used. Some of which are giving below:

- Low noise and low power op amp is used in medical field.
- Active Filters and Signal Processing.
- In sensors applications.

1.4 Thesis Organization

The thesis is divided into six chapters and its outline is described as given below.

🗁 **Chapter 1: Introduction**

Brief overview of issues related to modern CMOS technology, necessity of frequency compensation, motivation of the project and outline of the thesis.

🗁 **Chapter 2: Literature Review**

This chapter starts with the operational amplifier overview and describing the need and the various frequency compensation techniques used in op amp designing.

🗁 **Chapter 3: Operational Amplifier Compensation Strategy**

This chapter describes the Miller Compensation strategy and the comparable study of RC, voltage buffer and current buffer compensation with advantage/disadvantage of current buffer over the others.

🗁 **Chapter 4: Operational Amplifier Design Procedure**

This chapter discusses the various calculation steps taken to design the final design and the equations followed to implement the design.

Chapter 5: Simulation Results and Layout

This chapter contains various simulations results of the final circuit, Layout and LVS report.

🗁 **Chapter 6: Conclusion**

This Chapter which is the concluding chapter, the design has been analyzed for further improvements which are possible.

Chapter 2

Literature Review

2.1 Operational Amplifier Overview

2.1.1 Op-Amp Basics and Its Parameters

Operational amplifiers are an integral part of many analog and mixed signal systems. Op amps with vastly different levels of complexity are used to realize functions ranging from dc bias generation to high speed amplification or filtering.

In this chapter ideal op amp and its parameters values, basic op amp structure and its parameters such as gain bandwidth product, common mode rejection ratio, power supply rejection ratio etc are discussed.

Ideally op amp is differential amplifier with two inputs and one output, infinite gain, infinite input resistance so that no loading effect can occur and zero output resistance.

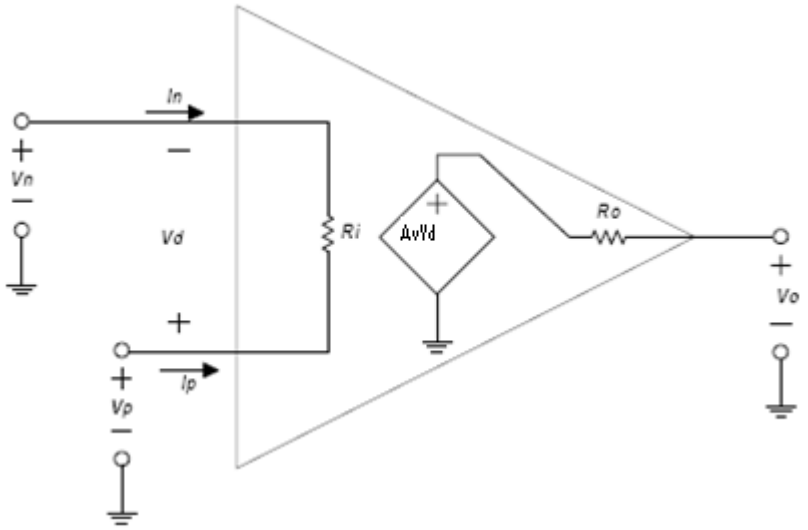

Figure 2.1: Standard op amp notation.

The Thevenin amplifier model is shown in Fig. 2.1 below, showing standard op amp notation. It amplifies the voltage difference, $V_d = V_p - V_n$, on the input port and produces a voltage, V_o, on the output port that is referenced to ground. The ideal op amp model was

derived to simplify circuit calculations and is commonly used by engineers in first order approximation calculations. The ideal model makes three simplifying assumptions:

- Gain $A_v = \infty$
- Input Resistance $R_i = \infty$
- Output Resistance $R_o = 0$

Applying these assumptions to Fig. 2.1 results in the ideal op amp model shown in Fig. 2.2

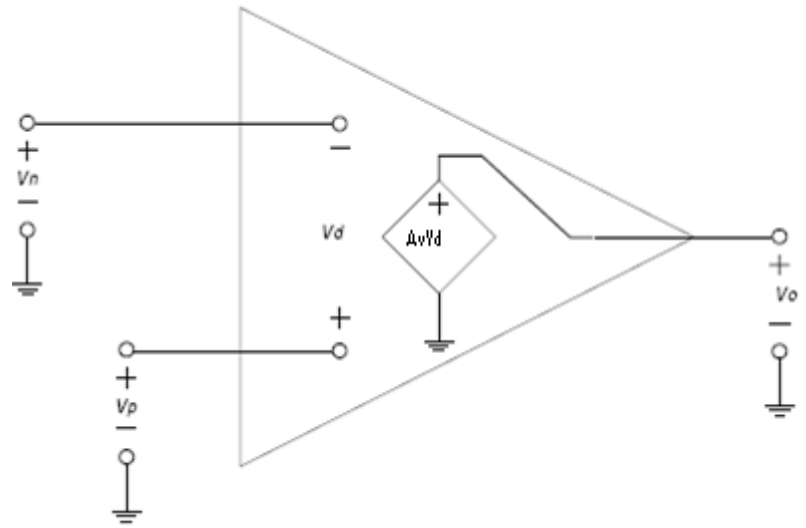

Figure 2.2: Ideal op amp model.

Other simplifications can be derived using the ideal op amp model

- $I_n = I_p = 0$

Because $R_i = \infty$ we assume $I_n = I_p = 0$. There is no loading effect at the input.

- $V_o = A_v \times V_d$

Because $R_O = 0$ there is no loading effect at the output.

- $V_d = 0$

If the op amp is in linear operation, *VO* must be a finite voltage. By definition $V_o = A_v \times V_d$. On rearranging, $V_d = V_0 / Av$. Since Av = ∞, $V_d = Vo/\infty = 0$. This is the basis of the virtual short concept.

- Common mode gain = 0

The ideal voltage source driving the output port depends only on the voltage difference across its input port. It rejects any voltage common to V_n and V_p.

- Bandwidth = ∞
- Slew Rate = ∞

No frequency dependencies are assumed.

- Drift = 0

There are no changes in performance over time, temperature, humidity, power supply variations, etc.

2.1.2 Operational Amplifiers

We can define as a "high-gain differential amplifier". By *high* we mean a value that is adequate for the application, typically in the range of 10^1 to 10^5. Since op amps are usually employed to implement feedback system, their open loop gain is chosen according to the precision required of the closed loop circuit.

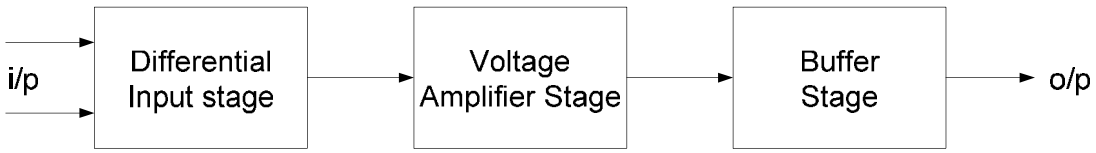

Figure 2.3: Typical two-stage op-amp.

A *classic* op amp architecture is made up of three stage as shown in Fig. 2.3, even though it is referred to as a "two-stage" op amp, ignoring the buffer stage (third stage). The first stage usually consists of a high-gain differential amplifier. This stage has the most dominant pole of the system. A common source amplifier usually meets the specification of second stage, having a moderate gain. The third stage is most commonly implemented as a unity gain source follower with a high frequency and negligible pole [6].

With the two stage classic op-amp architecture, high gain stages are difficult to achieve with Complementary Metal Oxide Semiconductor (CMOS) technology and basic

amplifier topologies. A typical CMOS differential amplifier stage is shown in Fig. 2.4. Differential amplifiers are often desired as the first stage in an op amp due to their differential input to single ended output conversation and high gain. The input devices in Fig. 2.4 are p-channel MOSFETs (PMOS). PMOS input devices are used more because of its improved slew rate and reduced 1/*f* noise [6]. PMOS input devices also provides reduced power supply rejection due to the current mirror's low sensitivity to change in power supply voltage.

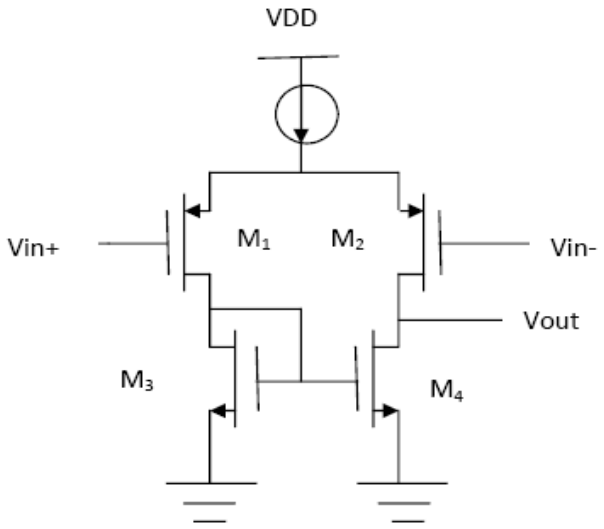

Figure 2.4: CMOS differential input stage.

For the CMOS differential input stage, the gain and bandwidth are calculated as

$$A_1 = g_{m1}(r_{ds2} \parallel r_{ds4}) \tag{2.1}$$

and

$$\omega_1 = \frac{1}{Cout(r_{ds2} \parallel r_{ds4})} \tag{2.2}$$

respectively. Implementation of cascade scheme can increase the moderate gain of this stage to a high value. The stage's dominant pole has an output capacitance, $C_{out,}$ consisting of mainly, the drain-to-bulk capacitance of M_2 and M_4. Although often negligible, another pole and zero are generated by M_1 and M_3 [7].

The second stage implementation of a common source amplifier shown in Fig. 2.5. Similar to the first stage, additional cascade devices can increase gain of this stage. Higher gains are often desirable for this stage when using Miller compensation techniques, although higher gains leads to lower bandwidth and the designer has to decide between these tradeoffs based on the specifications of the system.

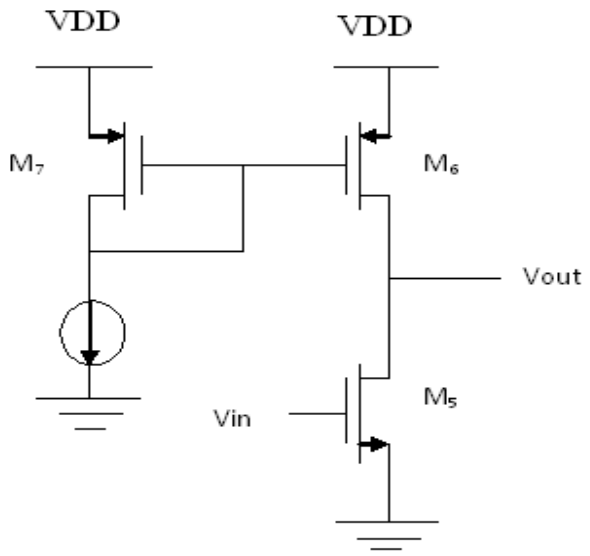

Figure 2.5: Common source amplifier stage.

For the circuit in Fig. 2.5, the gain and bandwidth are calculated as

$$A_2 = -g_{m5}\left(r_{ds5} \parallel r_{ds6}\right) \tag{2.3}$$

and

$$\omega_2 = \frac{1}{C_{out}(r_{ds5} \parallel r_{ds6})} \tag{2.4}$$

respectively. The output capacitance is dominated by the drain-to-bulk capacitance of M_5 and M_6.

The final output stage is normally realized with a simple source follower as shown in Fig. 2.6. With gain less than, but closer to unity, the source follower acts as a buffer for the previous two stages, reducing the overall gain negligibly and barely affecting the overall bandwidth with its high frequency pole. The gain for the source follower is defined as

$$A_3 = \frac{g_{m8}}{G_L + g_{m8} + g_{ds8} + g_{ds9}} \tag{2.5}$$

Where, G_L is the load conductance that the stage will drive.

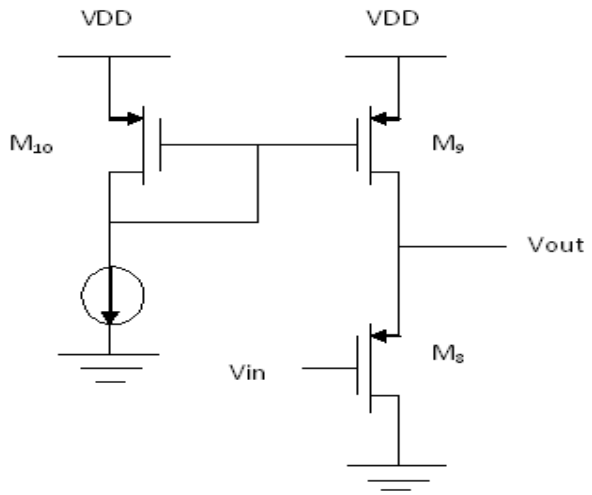

Figure 2.6: Source follower.

2.1.3 General Considerations

As the negative feedback is used widely in application in processing of analog signal, feedback system, however, suffer from potential instability, i.e. they may oscillate. Let us consider the negative feedback system shown in Fig. 2.7, the closed - loop transfer function as

$$\frac{Y}{X}(s) = \frac{H(s)}{1 + \beta H(s)} \tag{2.6}$$

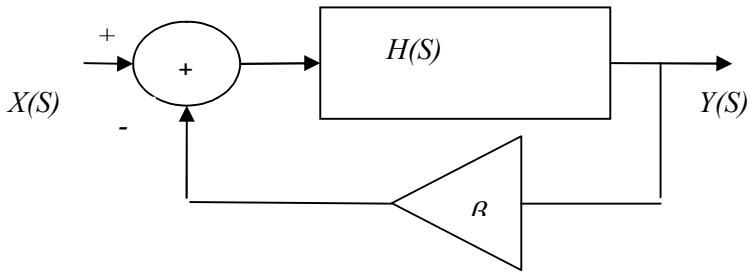

Figure 2.7: Basic negative feedback system.

If $\beta H(s = j\omega_1) = -1$, the gain goes to infinity, and the circuit can amplify its own noise and may oscillate at frequency ω_1. This condition can be expressed as

$$|\beta H(j\omega_1)| = 1$$

$$\angle \beta H(j\omega_1) = -180°,$$

which is known as "Barkhausen's Criteria" (β is assumed constant, less than or equal unity and independent of frequency). As negative feedback itself introduces 180° of phase shift, and the capacitance within amplifier's gain stages cause the output signal to lag behind the input signal by 90° for each pole they create. If the sum of these phase lags reaches 360° and gain is sufficient, the feedback signal will be add in phase to the original noise to allow oscillation buildup. The conditions can be summarize as excessive loop gain at frequency for which the phase shift reaches -180° or, excessive phase at frequency for which the loop gain drops to unity. So to avoid instability we must have $\angle \beta H$ more positive than -180° for $|\beta H| = 1$.

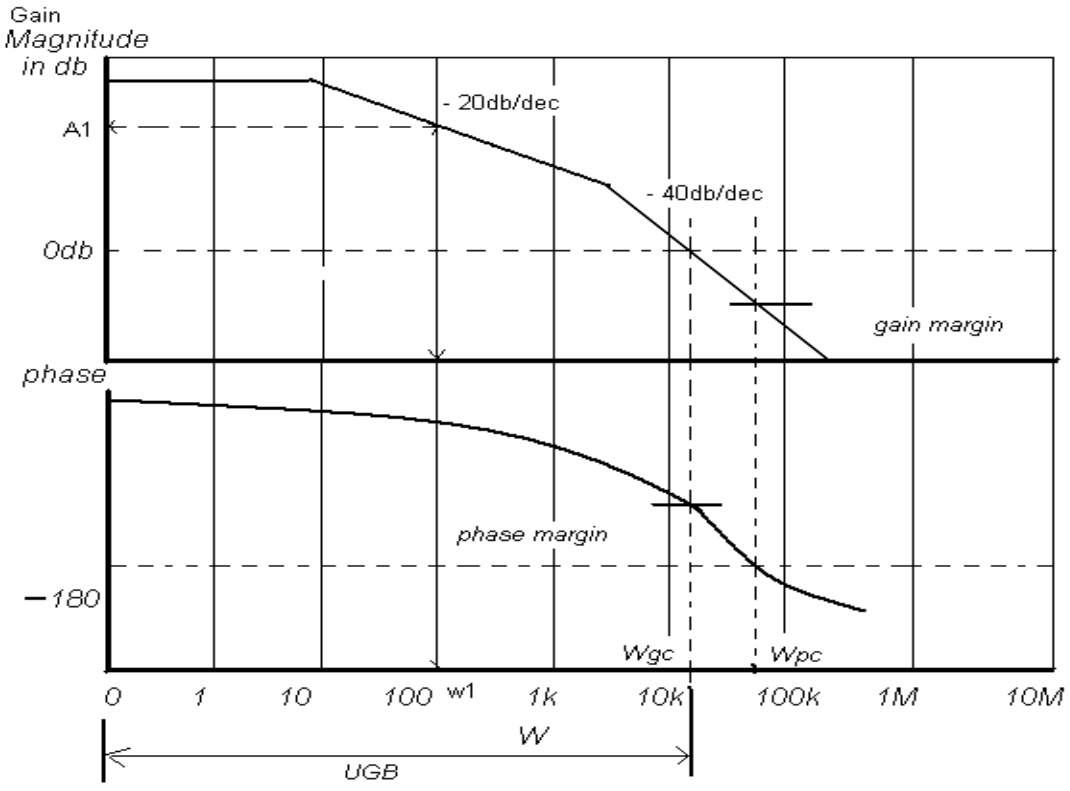

Figure 2.8: Showing unity gain bandwidth (UGB), gain margin (GM), phase margin (PM).

In a stable system, the gain crossover point must occur well before the phase cross over point. If β is reduced (less feedback is applied), then the magnitude plots of Fig. 2.8 are shifted down, there by moving the gain cross over closer to the origin and making the feedback system more stable. For the worst case stability (β = 1), we often analyze the magnitude and phase plots for $\beta H = H$.

2.1.4 Stability (Phase Margin)

After designing each op-amp stage and connecting them together, the op amp usually has poor performance and unstable in the unity feedback configuration. The main merit of the stability is the phase margin, the phase shift at unity gain frequency i.e. $|\beta H|$ must drop to unity before $\angle\beta H$ crosses -180°.

The phase of βH at the gain crossover frequency can serve as a measure of stability: the smaller $|\angle\beta H|$ at this point, the more stable the system.

Phase margin (PM), defined as:

$$\text{PM} = 180° + \angle\beta H(\omega = \omega_1), \tag{2.7}$$

where ω_1 is the gain crossover frequency.

For a phase margin less than 0°, the system is considered to be unstable while for a phase margin between 0° and 45°, system is marginally stable. $Y(j\omega_1)/X(j\omega_1) = 1/\beta$, suggesting a negligible frequency peaking i.e. the step response of the feedback system shows little ringing and providing a fast settling for PM = 60°. For a greater PM, the system becomes more stable but time response slows down. Thus PM = 60° is typically considered the optimum value [8].

For a two stage op-amp, the open-loop transfer function is given by

$$A(s) = \frac{A_1 A_2 \omega_1 \omega_2}{(s+\omega_1)(s+\omega_2)} \tag{2.8}$$

which assume that $A3$ is close to unity and that ω_3 is very high and negligible. The magnitude and phase function are

$$\left|A(j\omega_t)\right| = \frac{A_1 A_2 \omega_1 \omega_2}{\sqrt{\left(\omega_1\omega_2 - \omega_t^2\right)^2 + \left(\omega_t(\omega_1 + \omega_2)\right)^2}} \tag{2.9}$$

and

$$\angle A(j\omega_t) = -\left(180 + \arctan\left(\frac{\omega_t(\omega_1 + \omega_2)}{\omega_1\omega_2 + \omega_t^2}\right)\right) \tag{2.10}$$

In order to determine the phase margin, the corresponding unity gain frequency must be derived from the magnitude function. The phase can be calculated at the derived unity gain frequency. After calculating the initial phase margin, the necessary compensation steps can take place to stabilize the circuit [7].

2.1.5 Operational Amplifier Performance Parameters

Large signal voltage amplification, A_v: The open loop gain of an op amp determines the precision of the feedback system employing the op amp. The required gain can be adjusted according to the application. Trading with the parameters such as speed and output voltage swings, the minimum required gain must therefore be known. A high open loop gain is also necessary to suppress nonlinearity.

Av is the ratio of the peak-to-peak output voltage swing to the change in input voltage required to drive the output.

$$A_v = \frac{V_{o(p-p)}}{V_{in}} \tag{2.11}$$

Differential voltage Amplification, A_{VD}: The ratio of the change in the output to the change in differential input voltage producing it with the common-mode input voltage held constant.

$$A_{vd} = \left.\frac{\Delta V_o}{\Delta V_{in}}\right|_{Vincm,const} \tag{2.12}$$

Unity gain bandwidth, *UGB:* The range of frequencies within which the open-loop voltage amplification is greater that unity.UGB is shown in Fig. 2.8.

Gain bandwidth product ,*GBW*: The product of the open-loop voltage amplification and the frequency at which it is measured. From Fig. 2.8, Gain bandwidth product is

$$GBW = A_1 \times \omega_1 \tag{2.13}$$

Maximum-output swing Bandwidth, *BOM*: The range of frequencies within which the maximum output voltage swing is above a specified value.

Common-mode rejection ratio, *CMRR:* The ratio of differential voltage amplification to common-mode voltage amplification. CMRR falls off as the frequency increases.

$$CMRR = A_{DIFF} / A_{COM} \tag{2.14}$$

This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply voltage rejection ratio, *SVRR:* The absolute value of the ratio of the change in supply voltages to the change in input offset voltage.

$$SVRR = \Delta V_{Cc} \pm / \Delta V_{os} \tag{2.15}$$

Slew rate, *SR*: The average time rate of change of the closed-loop amplifier output voltage for a step-signal input.

$$SR = dv/dt \tag{2.16}$$

In op amps we trade power consumption for noise and speed. To increase slew rate, the bias currents within the op amp are increased.

Gain margin, *GM*: The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input.

Phase margin, *PM*: The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop amplification is unity. Gain and phase margins are measures of stability for a feedback system, though often times only phase margin is used rather than both. Based the

magnitude response of the loop gain, $|Av|$, gain margin is the difference between unity and $\left|A_v\left(W_{180^\circ}\right)\right|$ where W_{180° is the frequency at which the loop gain phase, is -180°, called as Phase crossover frequency. Phase margin is the phase difference between phase of A_v *(W0dB)* and -180° where W*0dB* is the frequency at which $|A_v|$ is unity, called unity gain frequency. Gain and phase margins are illustrated in Fig. 2.8. A marginally stable system has phase margins between 0^o and 45^o. A suggested phase margin is 65^o when designing a circuit.

Common-mode input voltage range, V_{ICR}: The range of common-mode input voltage that if exceeded may cause the operational amplifier to cease functioning properly.

Maximum peak output voltage swing, V_{OM}: The maximum positive or negative voltage that can be obtained without waveform clipping when quiescent dc output voltage is zero.

Maximum peak-to-peak output voltage swing, $V_{O(PP)}$: The maximum peak-to-peak voltage that can be obtained without waveform clipping when quiescent dc output voltage is zero.

Equivalent input noise voltage, *Vn*: The voltage of an ideal voltage source (having internal
impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source.

Equivalent input noise current, *In*: The current of an ideal current source (having internal impedance equal to infinity) in parallel with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a current source.

All op amps have associated parasitic noise sources. Noise is measured at the output of an op amp and referenced back to the input; thus, it is called equivalent input noise. The spectral density of noise in op amps has a 1/f and a white noise component. 1/f noise is inversely proportional to frequency and may dominate the devices noise at frequencies well into the megahertz range [9]. White noise is spectrally flat.

Average noise figure, *F*: The ratio of the total output noise power within a designated output frequency band when the noise temperature of the input termination(s) is at the reference noise temperature at all frequencies to that part of caused by the noise temperature of the designated signal input termination within a designated signal-input frequency.

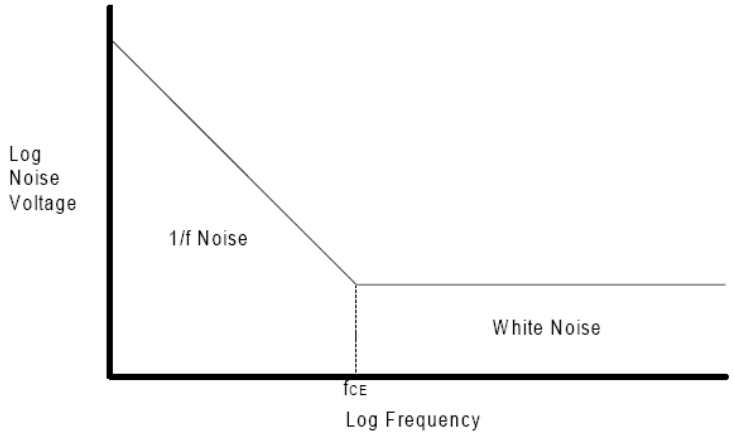

Figure 2.9: Typical op amp input noise spectrum.

Input resistance, *Ri*: The resistance between the input terminals with either input grounded.

Differential input resistance, *Rid*: The small-signal resistance between two ungrounded input terminals, Fig. 2.10.

Output resistance, *Ro*: The resistance between an output terminal and ground.

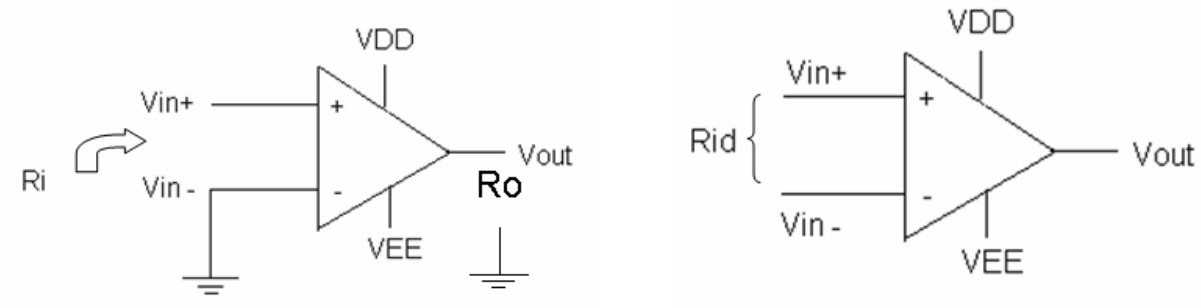

Figure 2.10: Showing *Ri*, *Rid* and *Ro*.

Input offset voltage, *Vio*: The dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to zero or other level, if specified.

Input offset current, I_{IO}: The difference between the currents into the two input terminals with the output at the specified level, Fig. 2.11.

Input bias current, I_B: The average of the currents into the two input terminals with the output at the specified level, Fig. 2.11.

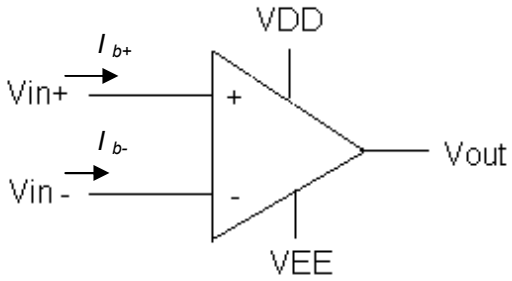

Figure 2.11: Op amp input bias current and input offset current.

$$\left.\begin{aligned} I_B &= (I_{b+} + I_{b-})/2 \\ I_{io} &= I_{b+} - I_{b-} \end{aligned}\right\} \tag{2.17}$$

2.2 Operational Amplifier Compensation

The single stage amplifier typically has good frequency response and could achieve a phase margin of 90^o assuming the gain bandwidth is ten times higher than the single pole. However, due to low dc gain of single stage amplifier, op amps requires at least two or more gain stages which results in multiple pole system. The poles contribute to the negative phase shift and may cause the phase margin become zero before reaching unity gain frequency. This negative phase margin is responsible for the system to oscillate. The process of altering the amplifier circuit to increase the phase margin and which ensures stability of closed loop circuit is known as “compensation”.

After designing each stage and connecting them together, an op-amp commonly is unstable in the unity feedback system. Using the measurement technique described, methods to compensate the op-amp can be employed.

2.3 Basic Frequency Compensation Techniques of Operational Amplifiers

2.3.1 Parallel Compensation

Parallel compensation is a classical way to compensate the op amp. A capacitor is connected in parallel to the output resistance of a gain stage of the operational amplifier to modify the pole. It is not commonly used in the integrated circuit due to the large capacitance value required to compensate the op amp, which costs considerable die area.

2.3.2 Pole Splitting - Single Capacitor Miller Compensation (SCMC)

For a two-stage op amp Single Capacitor Miller Compensation (SCMC), which significantly reduces the frequency of dominant pole and moves the output pole away from the origin (this effect is called "pole splitting"), is a common technique in op-amp design. In this method, a capacitor, C_c, is connected in parallel with the second stage, as shown in Fig. 2.12.

Miller's theorem states that the impedance seen in parallel with a gain stage can be modeled as an impedance connected from the input of that gain stage to the ground, and an impedance

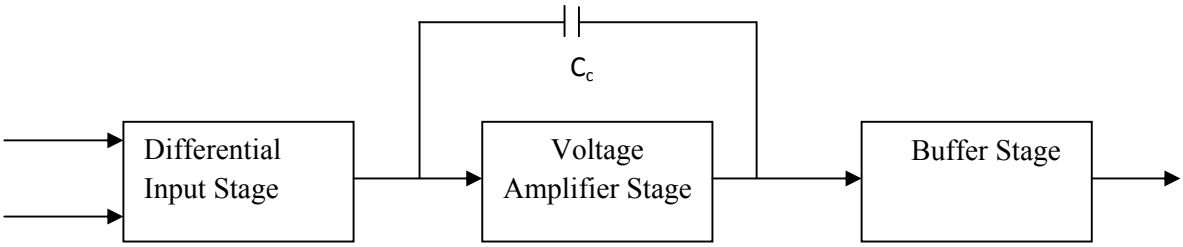

Figure 2.12: Implementation of pole-splitting (Miller Compensation).

connecting from the output of that gain stage to the ground. Since the impedance in this case is purely capacitive and the second stage has inverting gain, the first capacitor has a reflected capacitance of C_c (1 + A), where A is the gain of the second stage. When a large capacitor is needed to reduce the pole of the first stage, it can be generated by a smaller

capacitor and the described Miller multiplication. The second capacitor has a value much closer to the compensation capacitor C_c, especially for large gains [6].

Before the implementation of pole-splitting, the first and the second stage have pole frequencies

$$\omega_1 = \frac{1}{R_1 C_1} \tag{2.18}$$

and

$$\omega_2 = \frac{1}{R_2 C_2} \tag{2.19}$$

respectively, where R_1,C_1 and R_2,C_2 are the output resistance and capacitance of each stage.

After compensation, these frequencies becomes

$$\omega_1 = \frac{1}{R_1\left(C_1 + C_c\left(1 + A\right)\right)} \tag{2.20}$$

and

$$\omega_2 = \frac{1}{R_2\left(C_2 + C_c\left(1 + \frac{1}{A}\right)\right)} \tag{2.21}$$

due to the Miller capacitance seen in parallel.

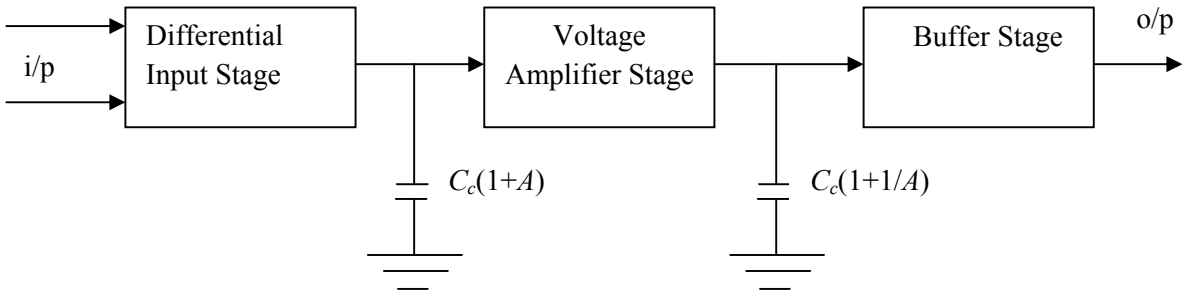

Figure 2.13: Miller equivalent of circuit in Fig. 2.12.

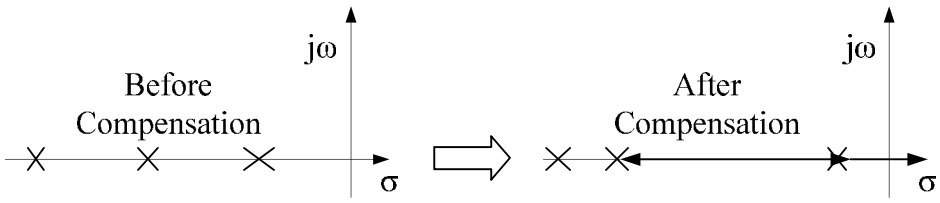

Figure 2.14: Pole splitting.

Due to reduced frequency of first stage, op amp's phase improves that makes op amp more stable than before compensation. In the process of making the op-amp stable, one of the significant tradeoff is bandwidth. If the first stage bandwidth is reduced, the overall bandwidth will be reduced. Due to technology demands, bandwidth and phase margin should be optimized and the other factors that should be considered are, such as voltage swing, slew rate, common mode rejection, power consumption. Some of the compensation techniques developed focus on optimizing these different factors based on their specific application.

While designing the op-amp with cascade topology, the zeros are quite far from the origin, in two-stage op amps incorporating Miller compensation, a nearby zero appears in the circuit. As with poles in left half plane, a zero in the right half plane contributes more phase shift, thus moving the phase crossover toward the origin. From Bode approximations, the zero slows down the drop of the magnitude, thereby pushing the gain crossover away from the origin which results in stability degradation.

Two effective means have evolved for eliminating the effect of the right half-plane zero. One approach has been to insert a source follower in the path from the output back through the compensation capacitor to prevent the propagation of signals forward through the capacitor. An even simpler approach is to insert a nulling resistor in series with the compensation capacitor [10].

2.3.3 Single Capacitor Miller Compensation with a Nulling Resistor

In practice we can move the zero so as to cancel the first nondominant pole. This occurs if the value of nulling resistor (R_z) is chosen such that the frequency of zero is same as that of the first nondominant pole.

The possibility of canceling the nondominant pole makes this technique quite attractive, but it also has some drawbacks.

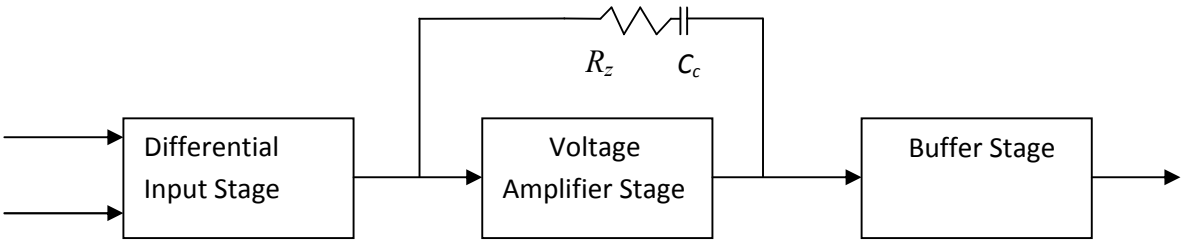

Figure 2.15: Addition of R_z in series with compensation capacitor.

First, the load capacitance seen by an op amp may vary in switched-capacitor circuit during the period which requires a corresponding change in R_z which complicates the design. Second drawback relates to the actual implementation of R_z. As the nulling resistor realized by a MOS transistor in the triode region, R_z changes substantially as output voltage excursions are coupled through C_c to node X of MOS transistor, which degrade the large-signal settling response [8].

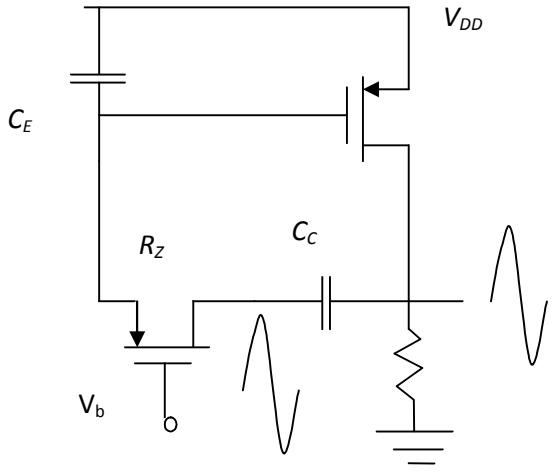

Figure 2.16: Effect of large output swing on R_z.

2.4 Other Multistage Operational Amplifier Compensation Techniques

Although SCMC and SMCNR are quite simple to implement into a design, several other techniques are popular for compensation in op amps consists of multiple gain stages. Some frequency-compensation topologies are as below:

2.4.1 Nested Miller Compensation (NMC) and the Variants

- Nested Miller Compensation (NMC)
- NMC using nulling resistor (NMCNR)
- Reversed nested Miller compensation (RNMC)
- Multipath NMC (MNMC)
- Nested Gm-C compensation (NGCC)

As multistage amplifiers have more poles and zeros than do single stage amplifiers. The frequency and time responses become more complicated than those of the single stage op amps. So multistage amplifiers suffer closed loop stability problems. Since a 'Single Miller Compensation' is used for the simple two-stage amplifier; the extended version of the SMC compensation, nested Miller compensation (NMC) [11, 12] is applicable to amplifiers with three or more stages. Because of the rapid bandwidth reduction, op amps with more than four stages are rarely investigated. There are some drawbacks related to the NMC approach. The total of N-1 nested compensation capacitors must be placed between the dominant node and the other nodes to split the individual poles from the dominant output pole to stabilize an N stage op amp. The nesting topology of the compensation capacitor reduces the bandwidth substantially [12, 13]. The necessity to drive the compensation capacitors along with the capacitive load requires the output stage to have a high transconductance to attain wide bandwidth and high slew rate. Consequently, elevated power consumption is unavoidable especially for large load capacitor [3].

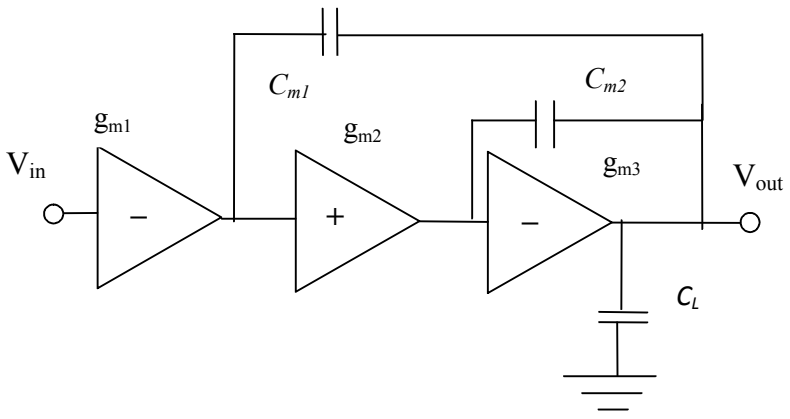

Figure 2.17: Structure of a three-stage NMC amplifier.

To overcome the bandwidth degradation problem, the modifications to the NMC are developed. NMC using nulling resistor (NMCNR) [6], multipath NMC (MNMC) [11, 12,

13], reversed nested Miller compensation (RNMC) [14], nested Gm-C compensation (NGCC) [15] have been presented.

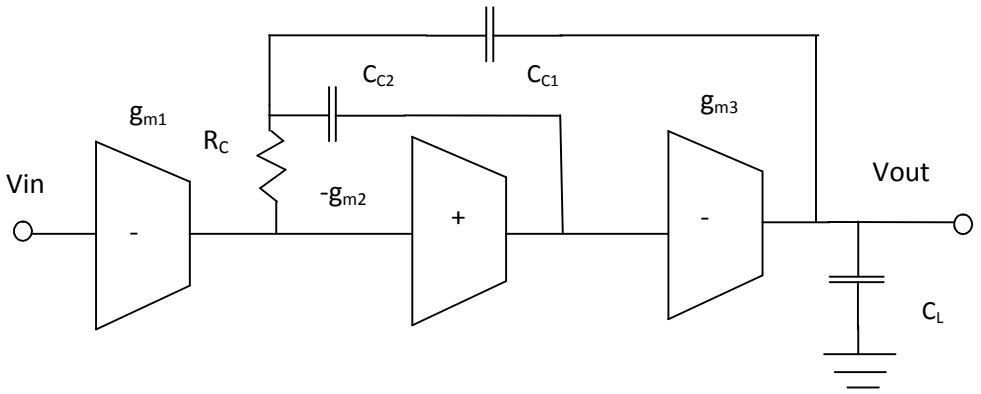

Figure 2.18: Block diagram of the basic RNMC.

RNMC improves the bandwidth over NMC by the reversed compensation topology compared to NMC as shown in Fig. 2.18. The RNMC technique sets the second gain stage negative and the output stage positive. The inner compensation capacitor does not load the output node.

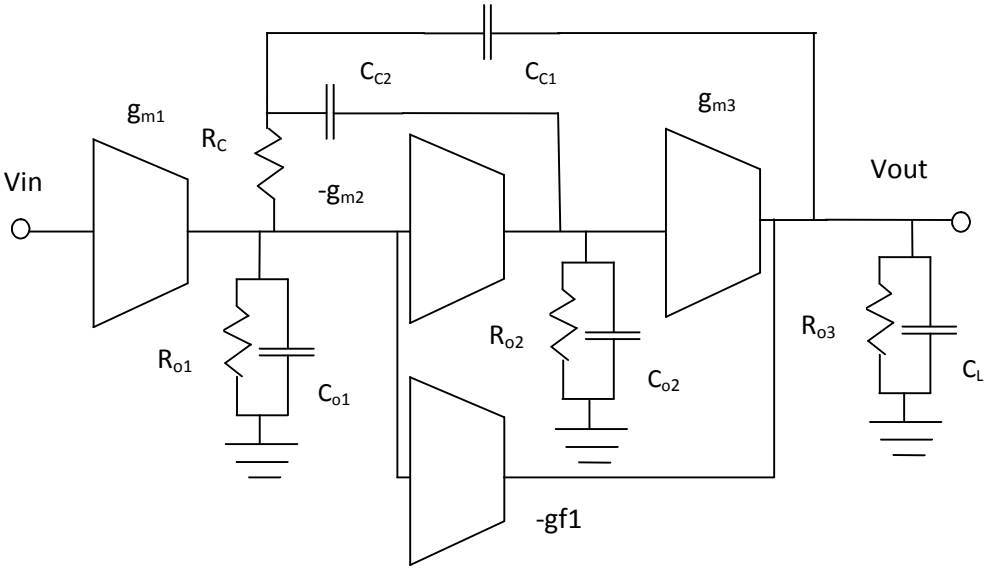

Figure 2.19: Block diagram of RNMCFNR.

The difference between NMC and MNMC is the added feedforward amplifier stage -gmf connected between the input of the first stage and the input of the last stage of the multistage op amp as shown in Fig. 2.20.

The feedforward stage added can produce a LHP zero to counteract the second nondominant pole to broaden the bandwidth. For both NMC and MNMC methods, it is

required that the load tranconductance be much larger than the first and second stage tranconductances. It is difficult to meet this condition for low-power designs. In this topology circuit complexity and power consumption increased. Moreover, the pole zero doublets may seriously degrade the settling time of the amplifier [16].

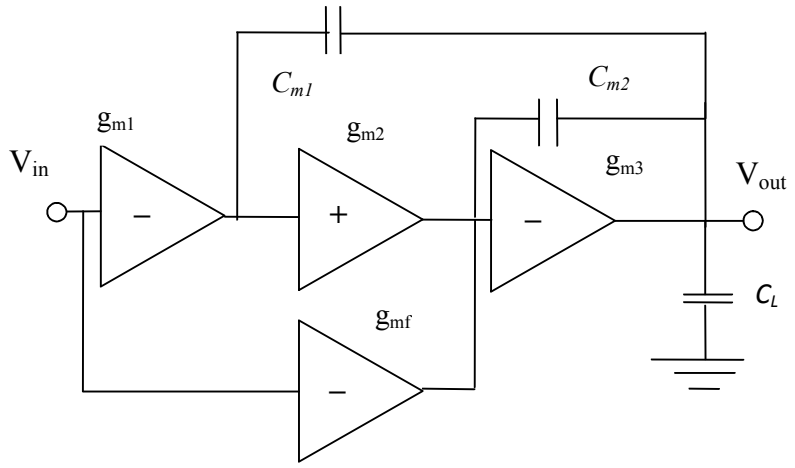

Figure 2.20: MNMC.

Thus, another method was proposed, called NGCC. The difference between NGCC and MNMC is that NGCC replicates the feed-forward Gm N-1 times for an N stage op amp recursively as shown in Fig. 2.21 that eliminates all zeros in the system.

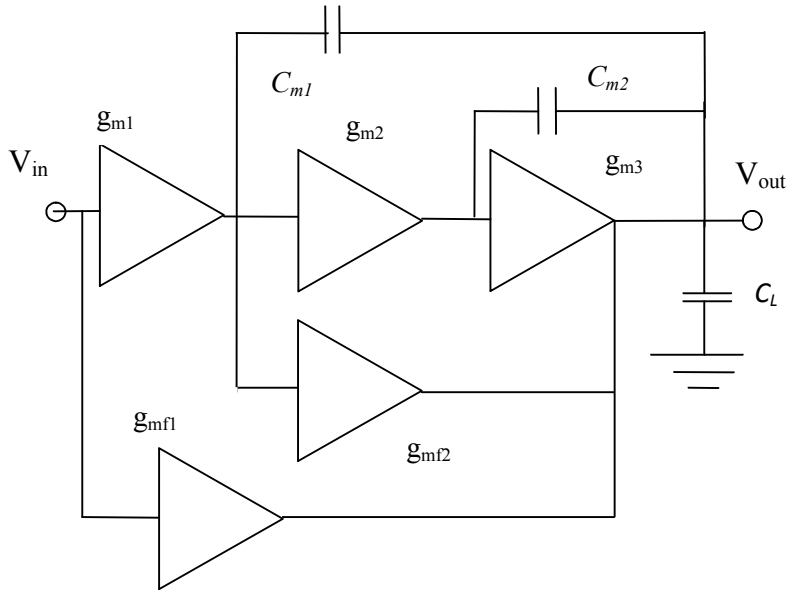

Figure 2.21: NGCC.

Compared to MNC, NGCC has simpler stability conditions due to the much simpler transfer function which makes the op amp design more facile.

All of the compensation techniques mentioned above use Miller capacitors whose sizes are related to the load capacitor value. The required sizes of the compensation capacitors would shoot up with larger capacitive loads which does not make these techniques preferable one for low area need. The experimental results of the varied versions of NMC showed that the bandwidth does not get improved significantly for considerable capacitive loads [11, 17].

2.4.2 Single Miller Feed-Forward Compensation (SMFFC)

Compensation techniques mentioned above are not suits well due to large capacitive loads.The demand for lower power, lower area, capability for driving large capacitive loads and stable high gain bandwidth of amplifiers calls for improved frequency compensation patterns. The topologies using a single Miller capacitor in three stage amplifiers could greatly reduce the needed sizes of the compensation capacitors compared to NMC related schemes and result in amplifiers with smaller chip area. The topology of the SMFFC op amp is represented in Fig. 2.22.

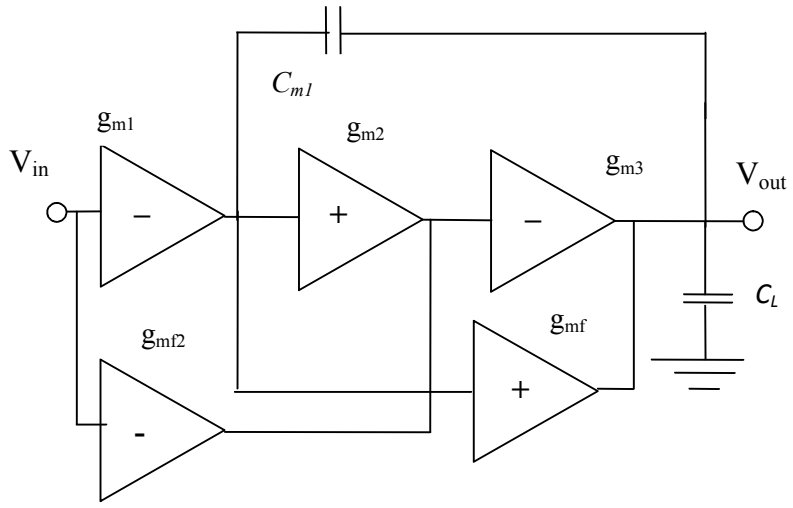

Figure 2.22: SMFFC.

Instead of using pole zero cancellation, SMC with one forward path adopts the separate pole approach [11] for compensation in the situation of large capacitive loads. SMFFC employs two forward paths and provide a LHP zero to compensate the first nondominant pole to alleviate the bandwidth reduction and improve the phase margin.

For the gain distribution like Av1 >> Av2 ≥ Av3, the second and third poles of the amplifier would be placed at higher frequencies that lead to a coarse single pole system for an easier frequency compensation strategy. The appropriate selection of the moderate gain of the second stage will then decrease the compensation capacitor size. Unfortunately, this method does not truly resolve the compressed gain bandwidth issue due to the super high gain of the first stage and the nature of the pole separation.

Gain enhanced feedforward path compensation (GFPC) [18] is much like the modified SMC version with one feedforward path, but for two stage amplifiers.

2.4.3 Nonstandard NMC Schemes

Due to the drawback in driving the large capacitive loads for enhancing the bandwidth, MNMC, NGCC, or NMCFNR topologies compared to NMC is not significant. For the significant increase in the bandwidth of the multistage amplifier, other nonstandard NMC topologies such as embedded tracking compensation (ETC) [13] , damping-factor-control frequency compensation (DFCFC) [19, 20], and active feedback frequency compensation (AFFC) [21] have been developed to remove the capacitive nesting structure which actually reduce the output capacitive load due to Miller capacitors. The ETC topology extends the bandwidth by using the pole-zero cancellation approach through the embedded compensation network without connection to the output load while the DFCFC amplifier improves the bandwidth by the pole-splitting method and uses a damping-factor-control block to ensure stability when the inner Miller capacitor is removed. AFFC , use an active-capacitive-feedback network, in which an active positive gain stage is added in series with the dominant compensation capacitor so that the required compensation capacitor in AFFC is smaller than that in all reported passive compensation topologies.

2.4.4 No Capacitor Feed Forward (NCFF)

One feedforward compensation scheme for multistage operational transconductance amplifiers with no Miller capacitors is proposed by Thandri and Silva Martinez [22].

In this compensation scheme the negative phase shift of poles is cancelled by the positive shift of left-half-plane (LHP) zeroes caused by feedforward path. This scheme results in

faster circuits with good phase margin, improved low frequency gain while does not compromised with bandwidth.

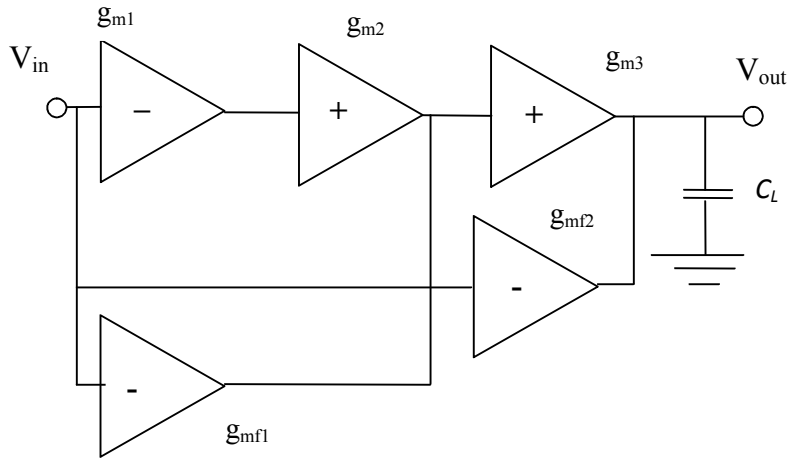

Figure 2.23: NCFF.

During the design there are some design consideration has to be consider: the feedforward and second stage must place the nondominant poles after the overall unity gain frequency of the amplifier to alleviate phase deduction; the pole zero cancellation should happen at high frequencies to achieve better time domain response. The transient response might be degraded severely by the pole-zero doublets. The complexity of the presence of extra poles and zeros can cause the design of the NCFF scheme to be very difficult.

2.4.5 Negative Miller Capacitance Compensation (NMCC)

The negative Miller capacitance compensates high speed CMOS op amps composed of an operational transconductance amplifier (OTA) and a buffer. Basically, NMCC removes or cancels capacitance from a node. The OTA is compensated with a capacitor Cc connected between the input and output of the buffer as in Fig. 2.24.

The op amp drives a parallel combination of a capacitor C_L and a resistor R_L the effective capacitance seen at the input and output of the buffer is

$$C_{eff,in} = C_c(1 - A) \tag{3.1}$$

and

$$C_{eff,out} = C_L + C_c\left(1 - \frac{1}{A}\right) \tag{3.2}$$

where '*A'* represent the gain of buffer.

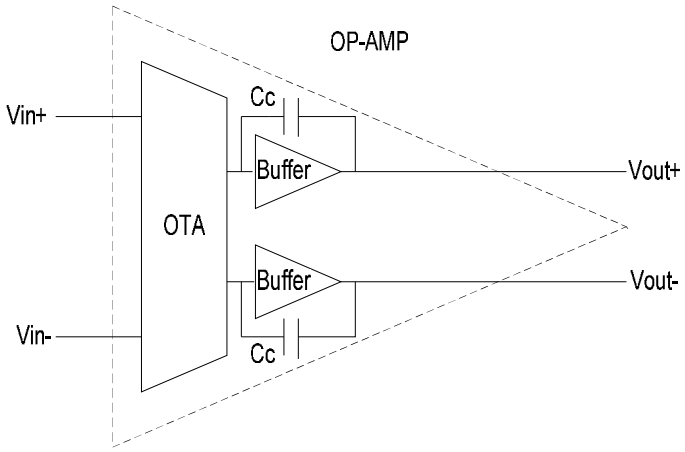

Figure 2.24: Op-amp bandwidth extension method [23].

Since the gain of the buffer is always smaller than one, the reflected Miller capacitor C_c $(1- 1/A)$ at the output will be negative. The effective capacitance seen at the output of the op-amp is smaller than the original load capacitance.

This effect pushes the first non-dominant pole (*i.e.*, the pole closest to the origin after the dominant pole) to a higher frequency. Implementation of this scheme into a circuit design has two distinct advantages:

- Removing undesired capacitance.
- When node capacitance is removed, the associated bandwidth and phase margin of that circuit improved.

Chapter 3

Operational Amplifier Compensation Strategy

The two-stage operational transconductance amplifier (OTA) in Fig. 3.1 is a widely used analog building block. Indeed, it identifies a very simple and robust topology which provides good values for most of its electrical parameters such as dc gain, output swing, linearity, CMRR, etc. To avoid closed-loop instability, frequency compensation is necessary in op amp design. For two-stage CMOS op amp, the simplest compensation technique is to connect a capacitor across the high gain stage. This results in the pole splitting phenomena which improves the closed-loop stability significantly. However, due to the feed-forward path through the Miller capacitor, a right half-plane (RHP) zero is also created. An uncompensated right half-plane zero drastically reduces the maximum achievable gain-bandwidth product, since it makes a negative phase contribution to the open-loop gain at a relatively high frequency. In order to compensate the right-half plane zero, an appropriate design approach is essential. Such a zero can be nullified if the compensation capacitor is connected in conjunction with either a nullifying resistor or a common-gate current buffer. After compensation of right half-plane zero, the maximum gain-bandwidth product is limited by second pole.

Various techniques for the compensation of the right half-plane zero in two stage CMOS op amp have been proposed and as well adopted. A compensation technique was proposed which uses a nulling resistor in series with the compensation capacitor. In an another solution a voltage buffer is introduced in compensation branch which breaks the forward path through the compensation capacitor while the other one uses a current buffer to break the forward path. Both current and voltage buffers can be adopted for compensation of the right half-plane zero due to their advantages over nulling resistor as it is more sensitive to process and temperature variation.

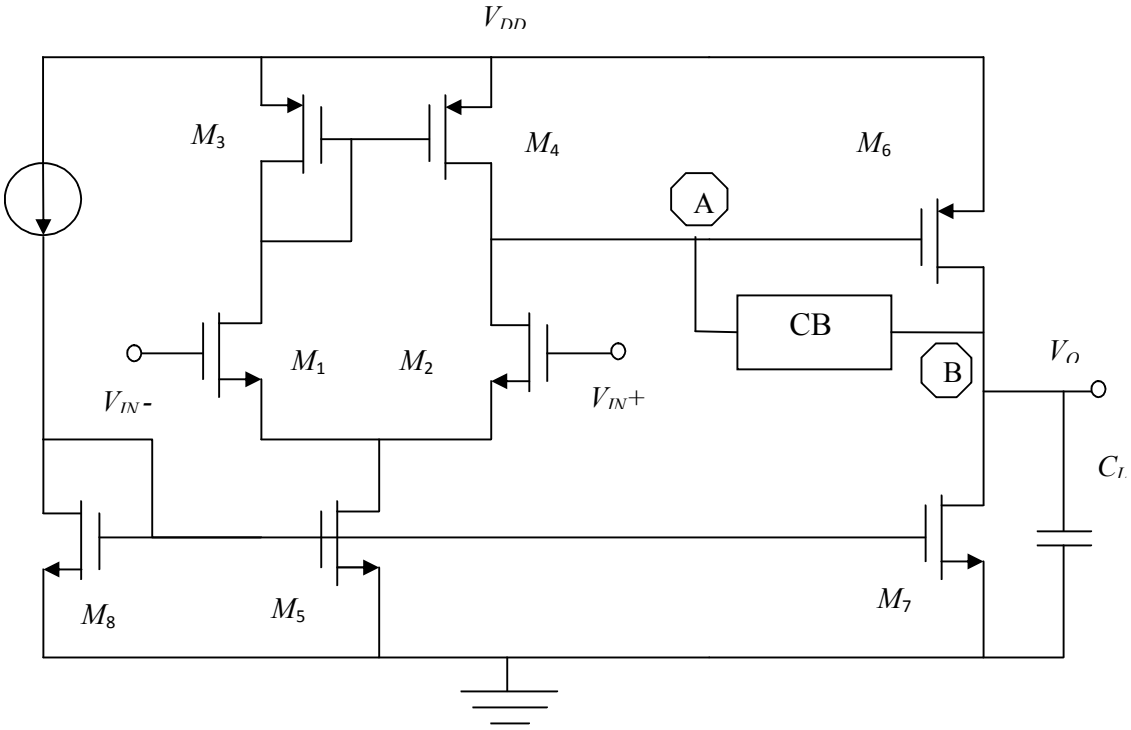

Figure 3.1: Two-stage op amp.

3.1 Optimized Design Approaches

To achieve a high gain-bandwidth product a very high g_{m5} value is required. However, it has been shown that it is possible to take advantage of techniques for compensation of the right half-plane zero to obtain a better frequency response. The original of these techniques was applied to NMOS op amps and then to CMOS op amps. Three different solutions for compensation are:

- Nulling Resistor Approach
- Voltage Buffer Approach
- Current Buffer Approach

3.1.1 Nulling Resistor Approach

The most popular compensation technique is that based on the nulling resistor, since it can be implemented using only an MOS transistor biased in the triode region.
In this approach the left half-plane zero introduced by the nulling resistor R_C in Fig. 3.1,

$$f_z = \frac{1}{2\pi}\frac{g_{m5}}{(g_{m5}R_C - 1)C_C} \tag{3.1}$$

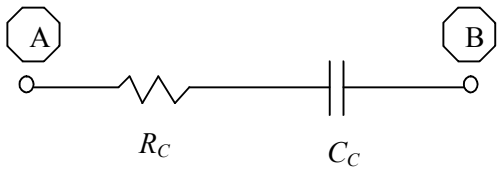

Figure 3.2: RC compensation block.

is exploited to compensate for the second pole. Therefore, the compensation sets the following condition,

$$\frac{g_{m5}}{C_L} = \frac{g_{m5}}{(g_{m5}R_{CR} - 1)C_{CR}} \tag{3.2}$$

where C_{CR} and R_{CR} are the new compensation capacitor and resistor, respectively.
Once this compensation is achieved, the new second pole is

$$f_{SP} = \frac{1}{2\pi R_{CR} C_{o1}} \tag{3.3}$$

where C_{o1} is the equivalent capacitance at the output of the first stage and is equal to C_{db2} + C_{db4} + C_{gs5}. This second pole does not depend on the load capacitance; hence a higher gain-bandwidth product can be achieved by nulling resistor approach. In order to achieve the desired phase margin the dominant pole (or equivalently f_{GBW}) can be choose accordingly.

3.1.2 Voltage Buffer Approach

The adoption of an ideal voltage buffer (i.e., with zero output resistance) to compensate the right half-plane zero gives the same second pole as in 3.1.1 and hence, the same W_{GBW}. Usually, the simple common drain in Fig. 3.3 is employed and connected between nodes A and B in Fig. 3.1.

Taking into account for the finite output resistance of the buffer which is about equal to $1/g_{m9V}$, the compensation branch introduces a left half-plane zero at $f_z = g_{m9V} /2\pi C_{CV}$. Therefore, a pole-zero compensation with the original second pole is achieved by setting

$$\frac{g_{m5}}{C_L} = \frac{g_{m9V}}{C_{CV}} \tag{3.4}$$

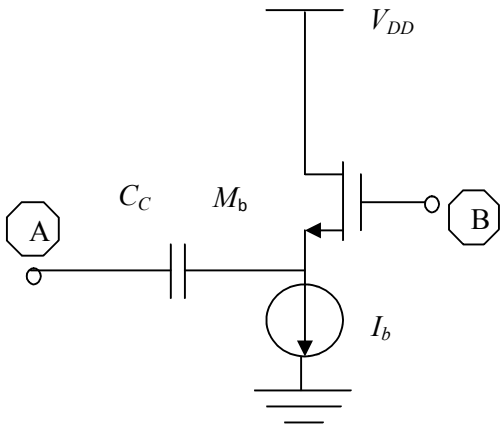

Figure 3.3: Voltage buffer compensation block.

This compensation shows high accuracy since it only depends on matching tolerances between transconductances and capacitors.

The approaches based on nulling resistor and voltage buffer give the same compensation capacitor and hence the same gain-bandwidth product. However, a voltage buffer in the compensation branch greatly reduces the output swing preventing its use in many practical cases [24].

3.1.3 Current Buffer Approach

The compensation based on current buffer (i.e., block CB in Fig. 3.1 replaced by the circuit in Fig. 3.4).This approach is very efficient both for the gain-bandwidth and the PSRR performance. It also does not have the drawback of the voltage buffer which reduces the amplifier output swing.

In this design approach the minimum allowable value of C_C is much smaller. The ability to use smaller provides a higher degree-of-freedom in trading noise performance with power consumption. For this purpose, the common gate in Fig. 3.4 can be used which is connected between nodes A and B in Fig. 3.1.

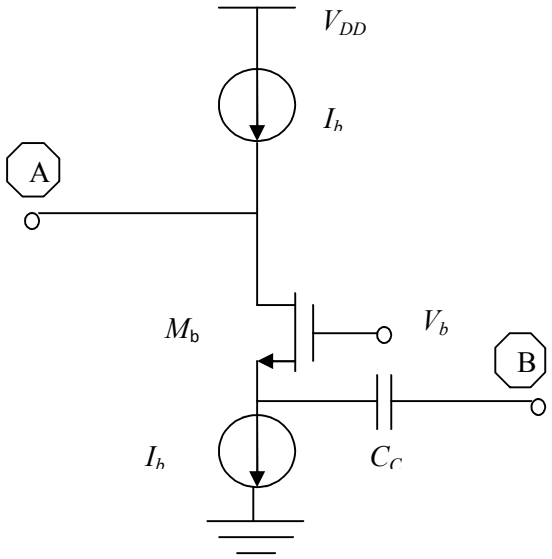

Figure 3.4: Current buffer compensation block.

3.1.4 Comparison of Design Approaches Based on Performance Parameter

The comparison of the above discussed design approaches is presented in the table given below which are based on simulation results [5].

Table 3.1: Comparison on the basis of C_C, UGB, Power.

Design Approach	**Compensation capacitor, C_C** (pF)	**UGB** (MHz)	**Power** (μW)
Nulling Resistor	2.5	5	590
Voltage Buffer	0.8	20	630
Current Buffer	0.75	28	790

Results show that the compensation with current buffer reduces the gain, but produces the best gain-bandwidth product. The small value requirement of C_C makes it suitable for circuit design where high capacitive load had to drive.

A better and commonly used implementation is achieved by placing the current buffer in the differential stage, in series with the source coupled pair. Circuit design in this way

reduces the complexity of the circuit, improve the both low frequency PSRR and gain, and the power dissipation remains less, compare to the nulling resistor approach.

3.2 Advantage /Disadvantage with Current Buffer Approach

- **Advantages**

- Good GBW
- High PSRR
- Improved slew rate (low C_C value)
- Area efficient (low C_C value)
- Power and area tradeoff
- Does not reduce output swing (unlike voltage buffer)

- **Disadvantage**

- Gain reduces
- Low noise performance
- Increased offset

Chapter 4

Operational Amplifier Design Procedure

For simplicity, both the mobility reduction due to the normal field and the velocity saturation effect associated with MOS devices will be neglected. The following MOSFET, strong- inversion, square-law equations:

$$I_D = \frac{u_{n,p} C_{ox}}{2}\left(\frac{W}{L}\right) V_{eff}^2 \tag{4.1}$$

$$g_m = \sqrt[2]{2u_{n,p} C_{ox} \frac{W}{L} I_D} \tag{4.2}$$

$$g_m = \frac{2I_D}{V_{eff}} \tag{4.3}$$

Where $V_{eff} = V_{GS} - V_{tn}$ for NMOS and $V_{eff} = V_{SG} - V_{tp}$ for PMOS, is used throughout the design. Strong inversion typically requires values of V_{eff} greater than approximately 200 to 250 mV for bulk MOSFET's at room temperature [25]. The small-signal equivalent circuit of the op amp in Fig. 4.1 is presented in Fig. 4.2. The small-signal transfer function of the CMOS according to the equivalent circuit shown in Fig.4.2 is

$$A(s) \cong \frac{\omega_u}{s} \times \frac{1 + s\dfrac{C_C + C_{gs9}}{g_{m9}}}{s^2\left(\dfrac{C_L C_{gs6}}{C_C g_{m6}} \times \dfrac{C_C + C_{gs9}}{g_{m9}}\right) + s\left(\dfrac{C_L C_{gs6}}{C_C g_{m6}} + \dfrac{C_{gs6}}{g_{m6}}\right) + 1} \tag{4.4}$$

Where

$$\omega_u \cong A_0 \omega_{p1} = \frac{g_{m1}}{C_C} \tag{4.5}$$

is the unity-gain frequency, also commonly known as gain-bandwidth product, of the op amp. The dc gain of the op amp is given by

$$A_0 = g_{m1} g_{m6} R_1 R_2 \tag{4.6}$$

and op amp's dominant pole frequency can be given as

$$\omega_{p1} \cong \frac{1}{g_{m6} R_1 R_2 C_C} \tag{4.7}$$

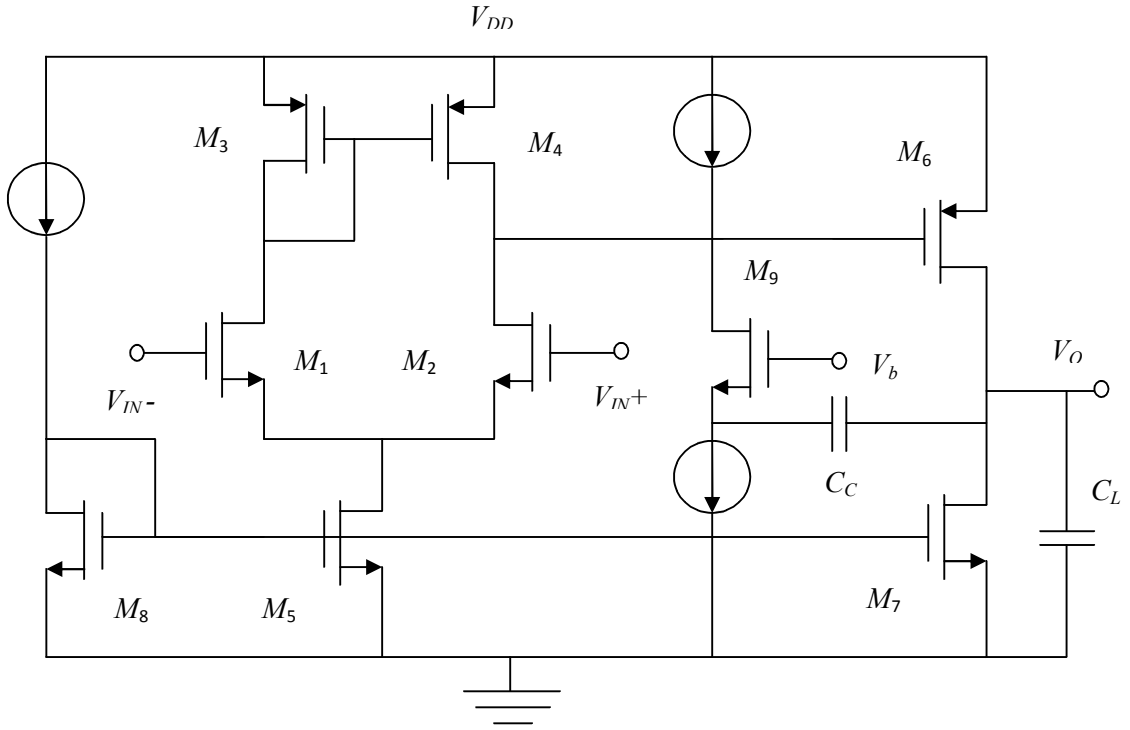

Figure 4.1: Two-stage CMOS op amp with Miller capacitor and a common-gate current buffer.

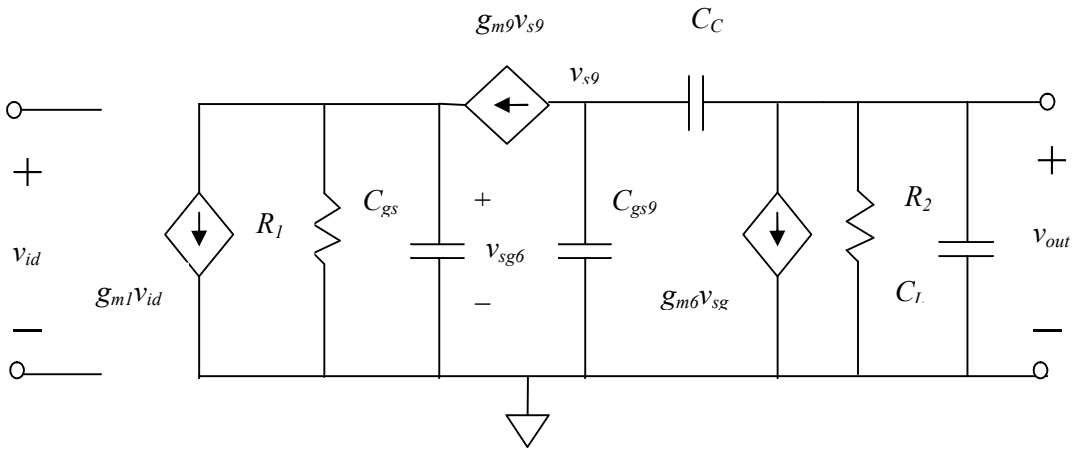

Figure 4.2: Small-signal equivalent circuit of the op amp in Fig. 4.1.

4.1 Basic Operational Amplifier Equations

4.1.1 Output Swing

Defining V_{HR}^{out} as the op amp head room voltage at output, according to Fig. 4.1

$$V_{HR}^{out+} = V_{DD} - V_{out(\max)}$$

$$V_{HR}^{out-} = V_{out(\min)} - V_{SS}$$

which yields

$$V_{HR}^{out+} = V_{eff\,6} \tag{4.8}$$

$$V_{HR}^{out-} = V_{eff\,7} \tag{4.9}$$

4.1.2 Common-Mode Range

If V_{HR}^{CM} is defined as the op amp head room voltage of the input common-mode range, i.e.,

$V_{HR}^{CM+} = V_{DD} - V_{CM(\max)}$ and $V_{HR}^{CM-} = V_{CM(\min)} - V_{SS}$ according to Fig. 4.1, it can be shown that

$$V_{HR}^{CM+} = V_{eff\,3} - V_{tn} \tag{4.10}$$

$$V_{HR}^{CM-} = V_{eff\,5} + V_{tn} + V_{eff\,1,2} \tag{4.11}$$

4.1.3 Internal Slew Rate

The slew rate associated with C_C can be found to be

$$SR = \frac{I_{D5}}{C_C} \tag{4.12}$$

4.1.4 External Slew Rate

The slew rate associated with C_L can be found to be

$$SR = \frac{I_{D7} - I_{D5}}{C_L} \tag{4.13}$$

Combining (4.12) and (4.13),

$$I_{D7} = SR(C_C + C_L) \tag{4.14}$$

Combining (4.3), (4.5, (4.12), and $I_{D5} = 2I_{D1} = 2I_{D2}$ yields

$$V_{eff} = \frac{SR}{\omega_u} \tag{4.15}$$

4.1.5 Offset Voltage Minimization

Systematic offset is caused by current imbalance in the output stage, i.e., between I_{D6} and I_{D7}, when there is no input voltage. Under such a condition,

$$I_{D3} = I_{D4} = \frac{I_{D5}}{2}$$

and so

$$V_{DS4} = V_{SD3}$$

Since

$$V_{SG6} = V_{SD4},$$

$$V_{SD3} = V_{SG3},$$

=> $$V_{SG3} = V_{SG6},$$

=> $$\frac{I_{D6}}{I_{D3}} = \frac{2I_{D6}}{I_{D5}} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_3}$$

Now when considering M_5 and M_7, I_{D7} / I_{D5} = $(W/L)_7$ / $(W/L)_5$, which yields the minimization of current imbalance in output stage by the following condition:

$$\frac{\left(\frac{W}{L}\right)_{5,8}}{2\left(\frac{W}{L}\right)_{3,4}} = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_6} \tag{4.16}$$

which can be used to minimize the offset voltage.

4.1.6 Input-Referred Thermal Noise Spectral Density

The input-referred thermal noise spectral density of the two-stage op amp in Fig. 4.1 can be shown to be

$$S_n(f) = 4kT\left\{2\left(\frac{2}{3g_{m1,2}}\right)\right\}\left[1+\frac{g_{m3,4}}{g_{m1,2}}\right] \tag{4.17}$$

From (4.3), (4.10), and (4.12),

$$g_{m3} = \frac{C_C SR}{V_{HR}^{CM+} + V_{tn}} \tag{4.18}$$

From (4.5), (4.17), (4.18),

$$S_n(f) = 4kT\left\{2\left(\frac{2}{3\omega_u C_C}\right)\right\}\left[1+\frac{SR}{\omega_u\left(V_{HR}^{CM+} + V_{tn}\right)}\right] \tag{4.19}$$

The quiescent power consumption of the two-stage op amp shown in Fig. 4.1 can be found to be

$$P = \left(2I_{D5} + I_{D7}\right)V_{\text{sup}} \tag{4.20}$$

In terms of slew rate the power consumption is given by

$$P = SR\left(3C_C + C_L\right)V_{\text{sup}} \tag{4.21}$$

4.1.7 Compensation Strategy and Phase Margin Control

By (4.4), under the condition

$$\frac{g_{m9}}{C_C + C_{gs9}} = \frac{g_{m6}}{C_{gs6}} \tag{4.22}$$

the nondominant poles of $A(s)$, i.e., the roots of the polynomial

$$B(s) = s^2\left(\frac{C_L C_{gs6}}{C_C g_{m6}} \times \frac{C_C + C_{gs9}}{g_{m9}}\right) + s\left(\frac{C_L C_{gs6}}{C_C g_{m6}} + \frac{C_{gs6}}{g_{m6}}\right) + 1 \tag{4.23}$$

are real and given by

$$p_2 = -\frac{g_{m6}C_C}{C_{gs6}C_L} \tag{4.24}$$

$$p_3 = -\frac{g_{m9}}{C_C + C_{gs9}} = -\frac{g_{m6}}{C_{gs6}} \tag{4.25}$$

p_3 cancels the finite zero of the transfer function,

$$z = -\frac{g_{m9}}{C_C + C_{gs9}} \tag{4.26}$$

and $A(s)$ reduced to

$$A(s) \cong \frac{\omega_u}{s} \times \frac{1}{1 - \frac{s}{p_2}} \tag{4.27}$$

According to (4.27), the phase margin of the op amp, considered for 100% feedback,

$$\phi_M = \tan^{-1}\frac{|p_2|}{\omega_u} = \tan^{-1}\frac{\omega_{T6}C_C}{\omega_u C_L} \tag{4.28}$$

where,

$$\omega_{T6} = \frac{g_{m6}}{C_{gs6}} = \frac{3}{2}\frac{u_p}{L_6^2}V_{eff6} \tag{4.29}$$

is the transition frequency of M_6. By combining the (4.28), (4.29) and (4.22), (4.28), (4.29) respectively, we get:

$$L_6 = \sqrt{\frac{3u_p V_{eff6}C_C}{2\omega_u C_L \tan\phi_M}} \tag{4.30}$$

$$g_{m9} = \tan\phi_M \omega_u C_L\left(1 + \frac{C_{gs9}}{C_C}\right) \tag{4.31}$$

By using, $g_m = \sqrt{2u_n C_{ox}\left(\frac{W}{L}\right)I_D}$, $C_{gs} = \frac{2}{3}WLC_{ox}$ and (4.31);

$$I_{D9} = \frac{(\tan\phi_M \omega_u C_L)^2\left(C_C + \frac{2}{3}W_9 L_9 C_{ox}\right)^2}{2u_n C_{ox}\left(\frac{W_9}{L_9}\right)} \tag{4.32}$$

which shows there is a tradeoff between power consumption and area of the compensation circuit [26].

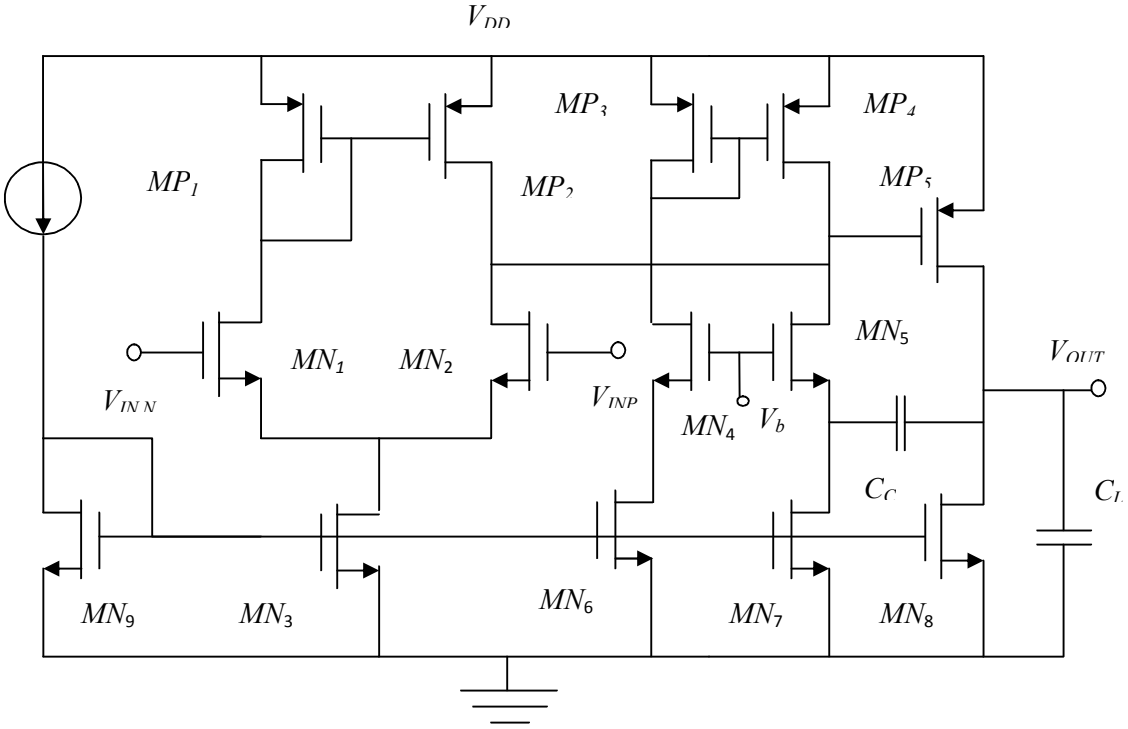

Figure 4.3: Op amp design with current buffer.

Table 4.1: Operational Amplifier Devices Size

Devices	Width (µm)/Length (µm)
MN1, MN2	6.3/7
MN3, MN9	4.2/1.4
MP1, MP2	5.25/6.3
MN4, MN5	14/1.4
MN6, MN7	5.6/1.4
MN8	31.5/1.4
MP3, MP4	31.15/17.5
MP5	18.2/1.4
C_C	0.5 pF
C_L	5 pF

4.2 Layout

The layout of analog integrated circuits is often driven by several issues that are generally not important in digital circuits. Therefore it is important for the layout engineer and designer to be aware of these issues.

4.2.1 Important Analog Issues

1. Matching of Devices

Matching of individual devices is of paramount concern in analog circuit design. In fact almost all of the 'analog layout techniques' are actually methods for improving matching between different devices on a chip. Matching is important because most analog circuit designs use a ratio based design technique (e.g. current mirrors). Some common techniques that help improve device matching are Multi-gate Finger Layout and Common-Centroid Layout [27].

2. Noise

Noise is important in all analog circuits because it limits dynamic range. In general there are two types of noise, random noise and environmental noise. Random noise refers to noise generated by resistors and active devices in an integrated circuit; environmental noise refers to unwanted signals that are generated by humans. Two common examples of environmental noise are switching of digital circuits and 60 Hz 'hum'. In general, random noise is dealt with at the circuit design level. However they are some layout techniques which can help to reduce random noise. Multi-gate finger layout reduces the gate resistance of the poly-silicon and the neutral body region, which are both random noise sources. Generous use of Substrate plugs will help to reduce the resistance of the neutral body region, and thus will minimize the noise contributed by this resistance.

Environmental noise is also dealt with at the circuit level. One common design technique used to minimize the effects of environmental noise is to employ a 'fully-differential' circuit design, since environmental noise generally appears as a common-mode signal. However Substrate plugs is also very useful for reducing substrate noise, which is a particularly troublesome form of environmental noise encountered in highly integrated mixed-signal systems and Systems-On-a-Chip (SOC). Substrate noise occurs when large amount digital circuits are present on a chip. The switching of a large number

of circuits discharges large dynamic currents to the substrate, which cause the substrate voltage to 'bounce'. The modulation of the substrate voltage can then couple into analog circuits via the body effect or parasitic capacitances. Substrate plugs minimizes substrate noise because it provides a low impedance path to ground for the noise current.

Issues that are important in digital circuits are still important in analog layout. Foremost among these is parasitic aware layout. It is important to minimize series resistance in digital circuits because it slows switching speed. Series resistance also slows analog circuits, plus it introduces unwanted noise. Parasitic capacitance is avoided in digital circuits because it slows switching speed and/or increases dynamic power dissipation. Stray capacitance has the same effect in analog circuits (bias current must be increased to maintain bandwidth and/or slew rate when extra load capacitance is present) plus it can lead to instability in high gain feedback systems.

4.2.2 Definition of Important Terms

1. **Multi-gate Finger Layout** refers to implementing a single, wide transistor as several narrow transistors in parallel. This minimizes the gate resistance and it also makes it easier to match the transistor with other devices.

2. Common-Centroid Layout refers to a layout style in which a set of devices has a common center point. This is used to minimize the effect of linear process gradients (e.g. oxide thickness) in a circuit.

3. Substrate plugging simply refers to making an ohmic contact to the substrate. This technique is used in digital circuits to minimize latch-up. In analog circuits it is used to minimize latch-up and for the reasons discussed above.

Chapter 5

Simulation Results and Layout

The amplifier is to be powered from a 3.3 volts power supply. The different bias voltages which are required by op amp circuit are produced by bias circuit. Based on the proposed compensation technique a CMOS op amp has been designed and simulated in a standard 0.35 μm CMOS technology. The power consumption is 144.34 microwatt.

5.1 Test Results

This design provided a gain of 42.26 dB from first stage and 35.95 dB from second stage making overall gain as 78.21dB with a common mode rejection ratio of 89.05 dB. ICMR is in between 0.5 volt to 3.1 volt. Unity gain bandwidth obtained was 5.82 MHz. Slew rates obtained were 7.11 V/μs for positive transition and 5.59 V/μsfor negative transition. The phase margin came out to be 63.97 degree making design relatively stable. The positive PSRR is 117.73 dB and negative PSRR is 99.44 dB.

5.1.1 AC Response

In Fig. 5.1, one method of measuring the AC performance is presented.

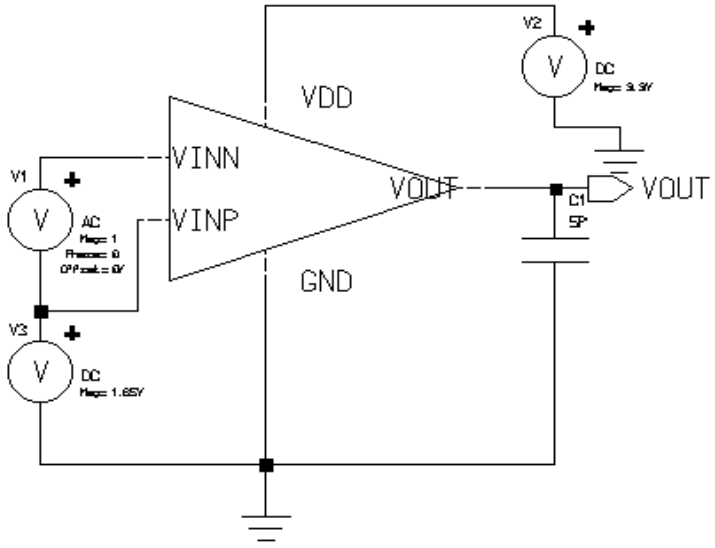

Figure 5.1: Configuration for simulating the open loop frequency response of op amp.

In this configuration, the amplifier is open loop, and the AC small signal is applied at the input.

In Fig 5.2, a Bode and phase plot for 3.3V, 27°C is shown. As can be seen, the open loop gain is above 78.21dB, and a phase margin is 63.97 degree.

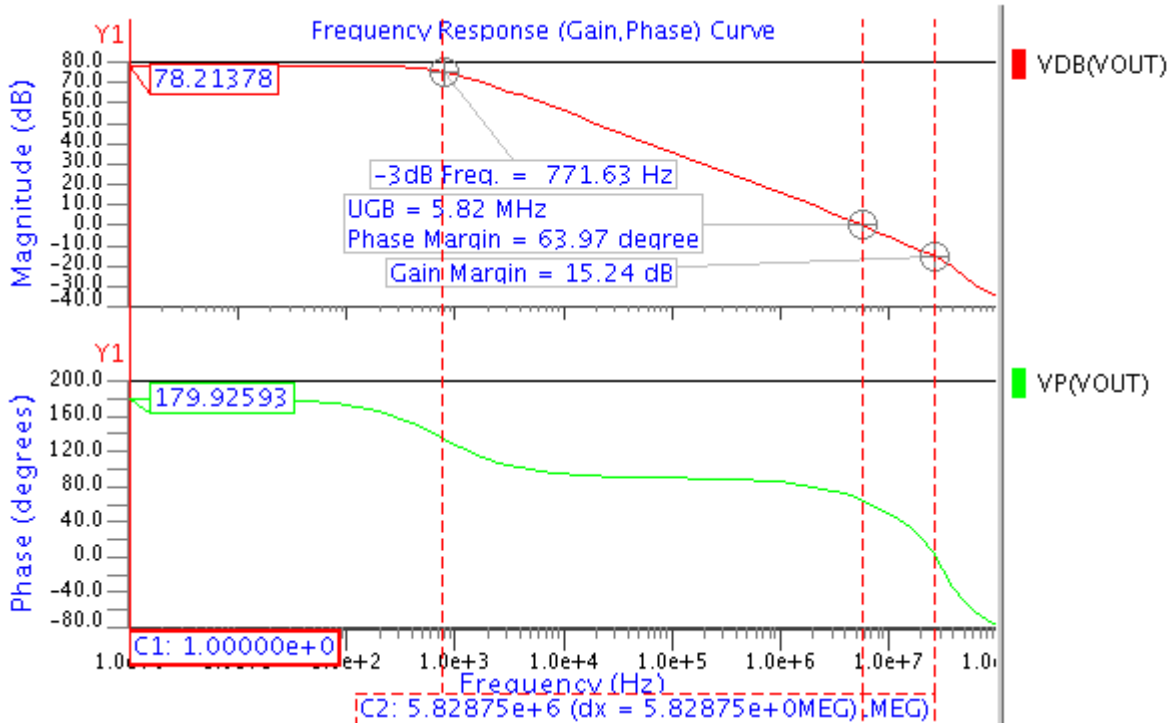

Figure 5.2: Frequency response of op amp.

5.1.2 Transient Results

A transient simulation of the amplifier in open loop gain configuration with the sinusoidal signal at the input with a 1.65 volt dc bias.

Transient results from Fig. 5.4 shows the swing as (0.1251V – 2.9595V) 2.83 volt. In the Fig.5.4, $V_{out(p-p)} = 2.83439\text{V}$ and $V_{INN} = 500\mu V$,

thus $Gain = \dfrac{2.83439}{500\mu} = 5668.78 = 75.07dB$.

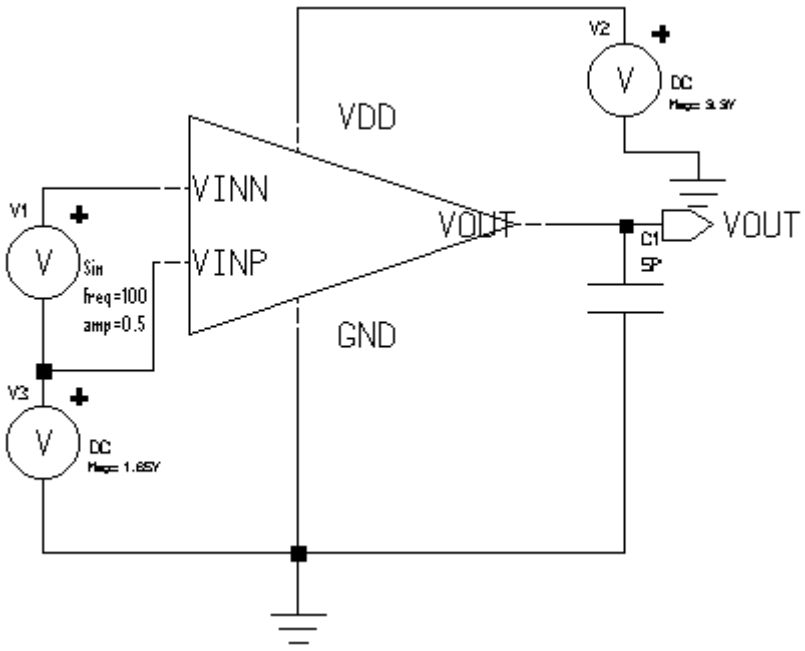

Figure 5.3: Schematic for the simulation of the transient response.

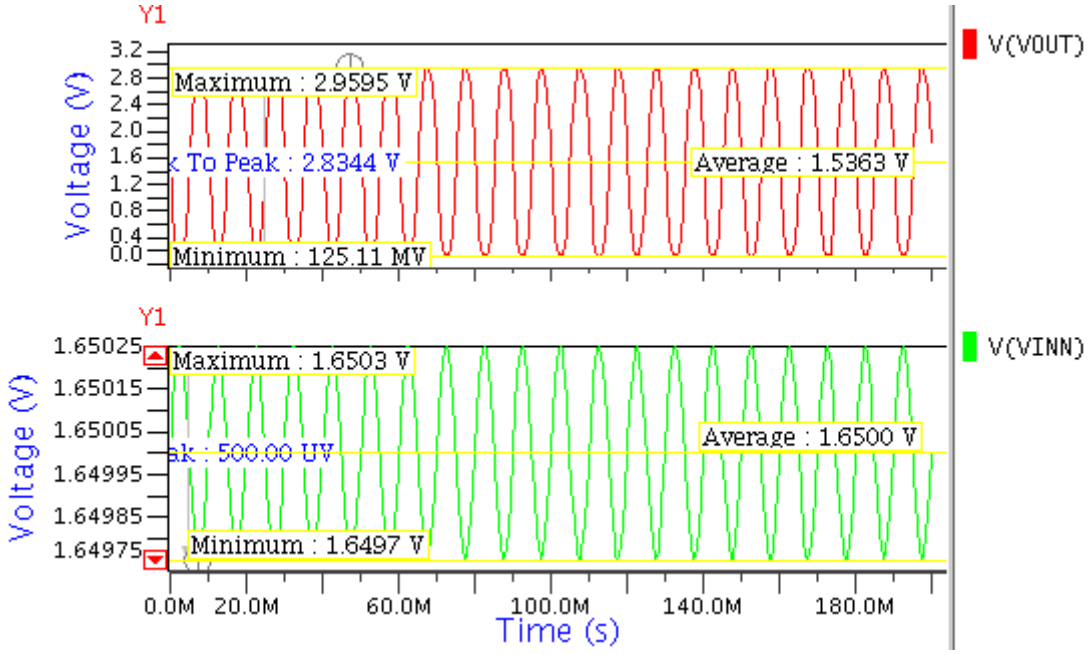

Figure 5.4: Output and input signals for transient analysis without unity feedback.

5.1.3 Step Response

In Fig. 5.5, a step from ground to VDD is applied at the input with unity feedback configuration. As was measured, the amplifier's slew rate is 7.1163 V/µs for the rising edge and 5.5892 V/µs for the falling edge as shown in fig. 5.6.

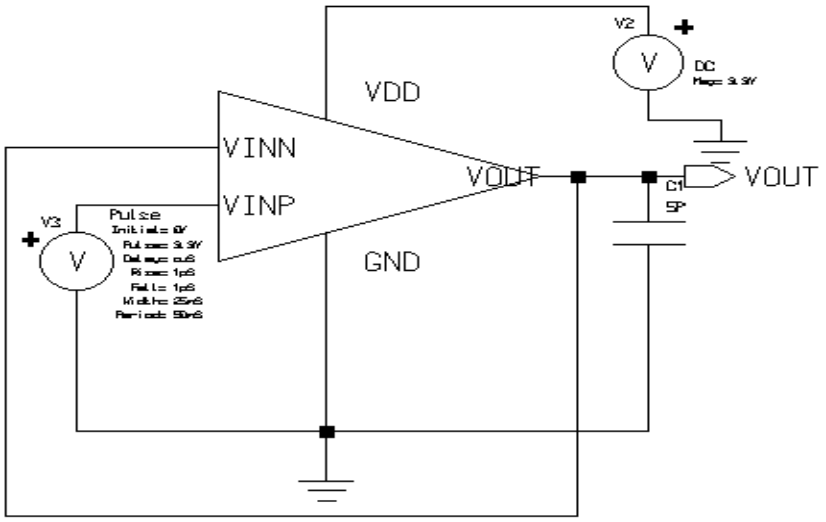

Figure 5.5: Schematic for the simulation and measurement of the slew rate.

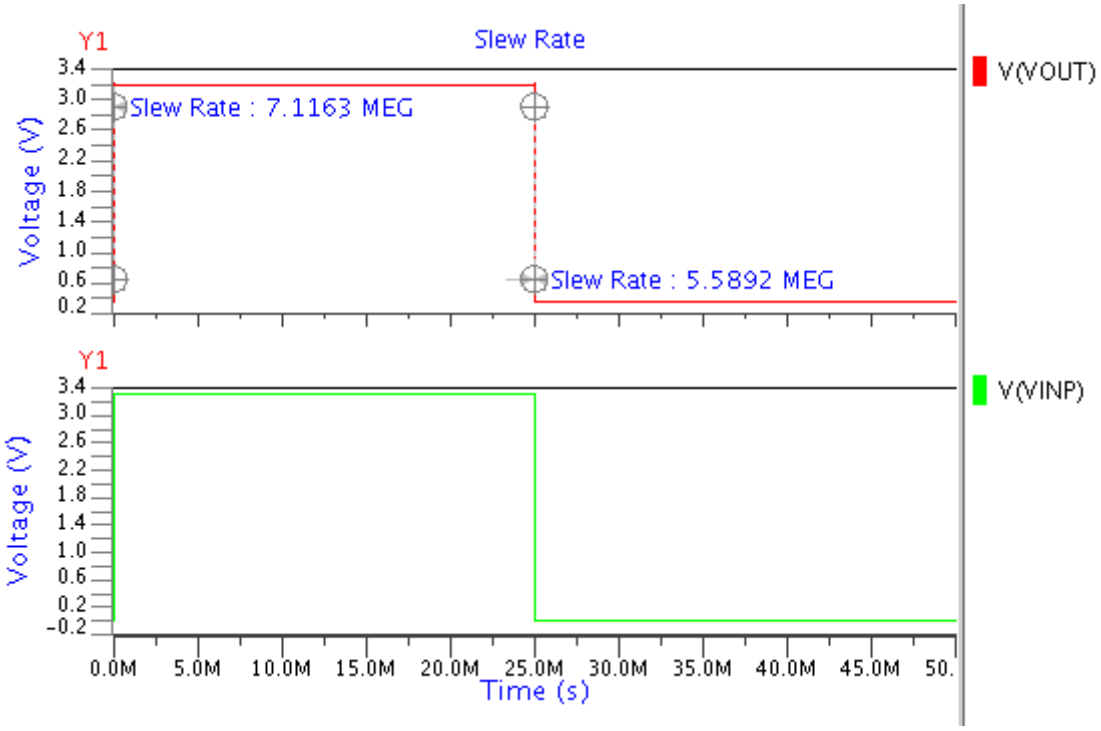

Figure 5.6: Slew Rate for the rising and falling edge with unity gain configuration.

5.1.4 Settling Time

The unity gain follower configuration is also use for settling time and peak over shoot measurement. This is the length of time for the output voltage of an operational amplifier to approach, and remains within, a certain tolerance of its final value. This is usually specified for a fast full-scale input step. Op amp is biased as shown in fig. 5.5. Fig. 5.7 shows settling time for different tolerance value.

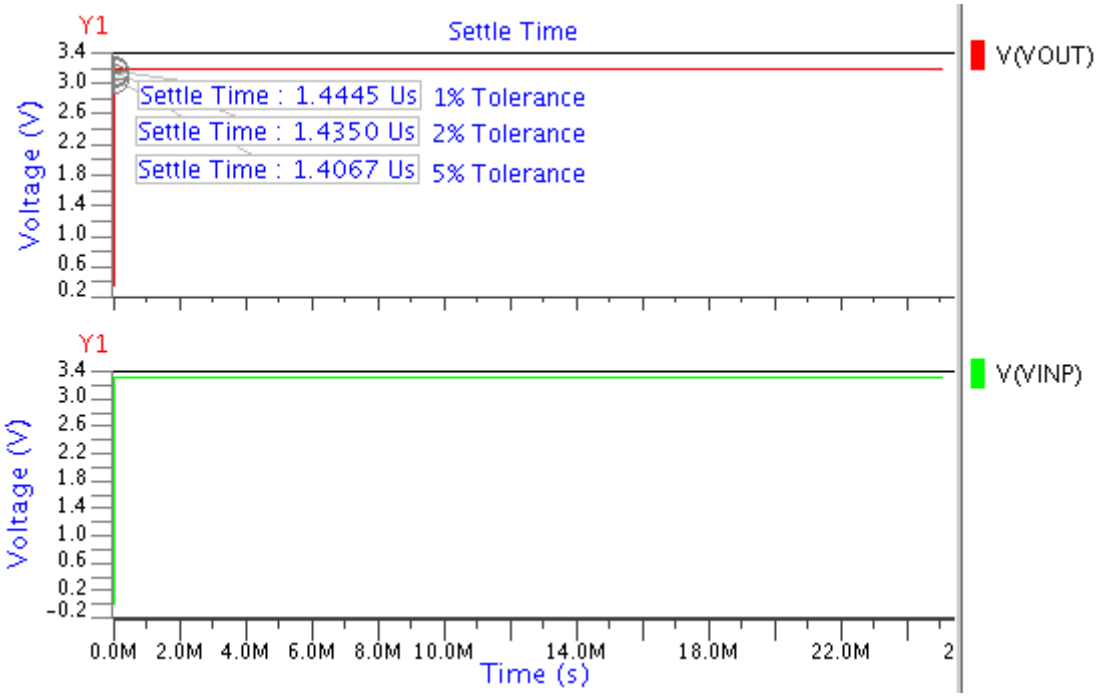

Figure 5.7: Settling time for the different tolerance values with unity gain configuration.

Table 5.1: Variation of Settling Time of op amp with different Tolerance values

Tolerance (%)	**Settling Time** (μs)
1	1.44
2	1.43
5	1.40

5.1.5 Common Mode Rejection Ratio

In order to simulate common mode rejection, first we find the common mode gain .For common mode gain the same ac signal is applied with 1.65 dc bias at both the terminal. The magnitude of ac source is 1 volt. When the simulator sweeps the frequency, there will be a 1V AC source on both the positive and negative inputs and hence the AC signal at the output will be the common mode gain. The previously calculated gain (from Fig. 5.2) can be divided by this gain to give the CMRR. The common mode rejection ratio was found to be 89.05 dB at low frequency.

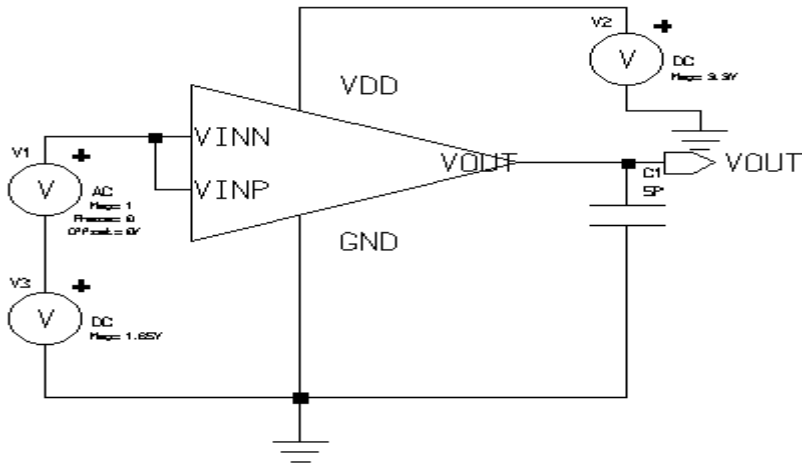

Figure 5.8: Schematic for the simulation of common mode gain and CMRR.

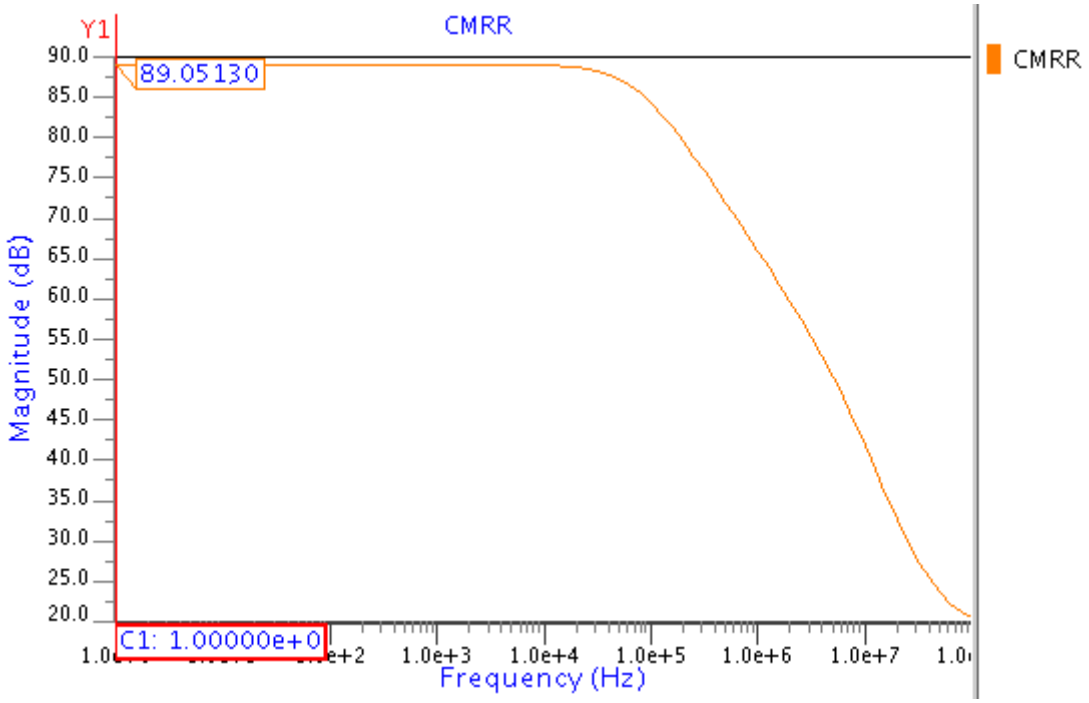

Figure 5.9: Common mode rejection ratio (CMRR).

5.1.6 Power Supply Rejection Ratio

PSRR was measured by placing a 1V AC signal on the power supply where the amplifier is in unity gain feedback configuration. PSRR is equal to the ratio of the AC signal at the output node to the AC signal on V_{DD}.

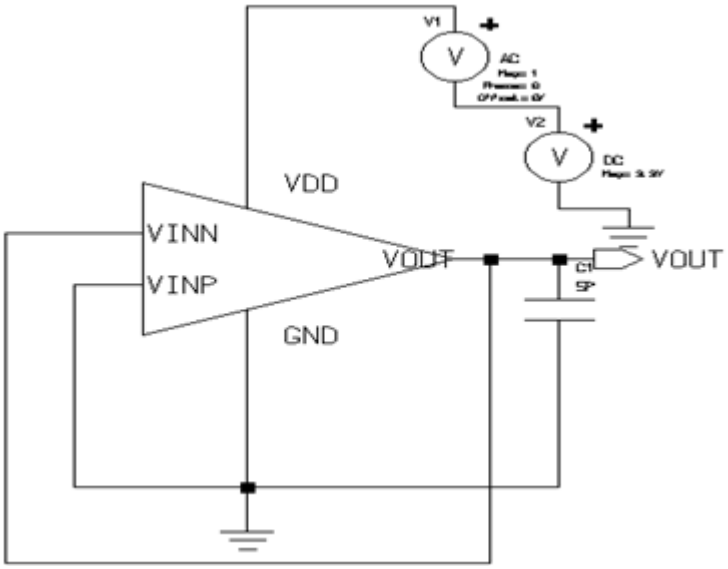

Figure 5.10: Schematic for the simulation of PSRR.

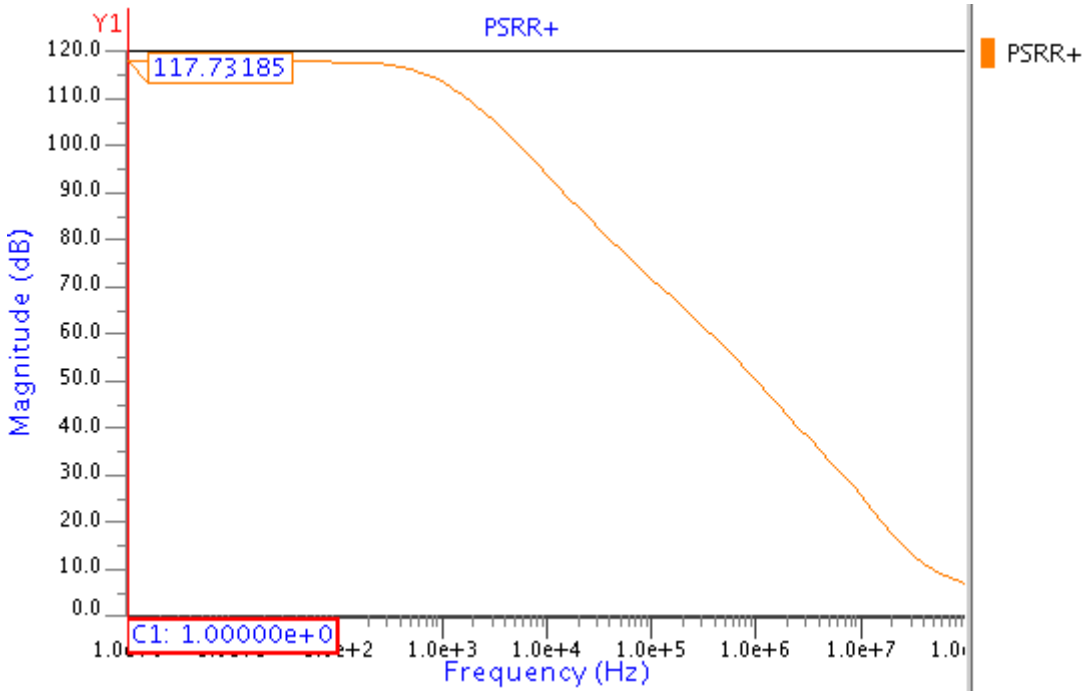

Figure 5.11: Power supply rejection ratio.

5.1.7 Effect of Common Mode Variation on the DC Gain

The amplitude and the phase are heavily dependent upon the applied common-mode input voltage *Vcm*, which is varied from 0.8 V to 3.1 V by the step of 0.1 V. The gain and phase plot variation is shown in fig. 5.12.

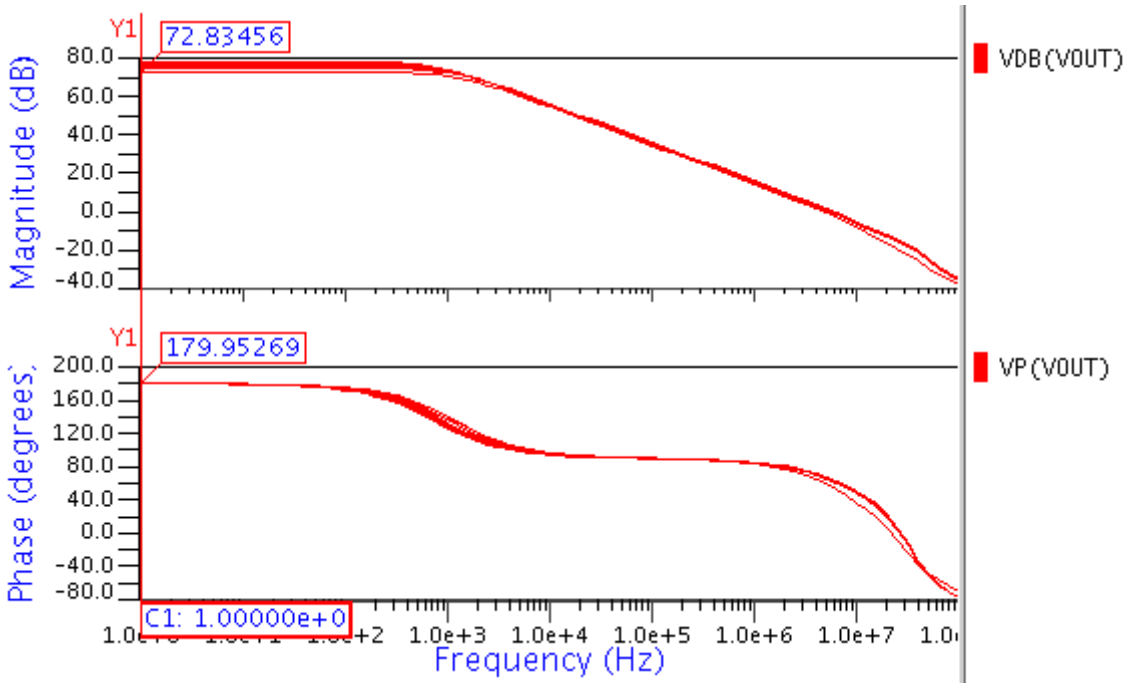

Figure 5.12: Gain and phase plot vs frequency with common mode variation.

5.1.8 Input Output Characteristics Using Unity Gain Configuration

For linearity test op amp is biased in the unity gain follower configuration as shown in fig. 5.13.Now input dc voltage is varied from 0 volt to 3.3 volt. Now the input and output is compared. The op amp is linear for input 0.50 – 3.1 V for which output match with input.

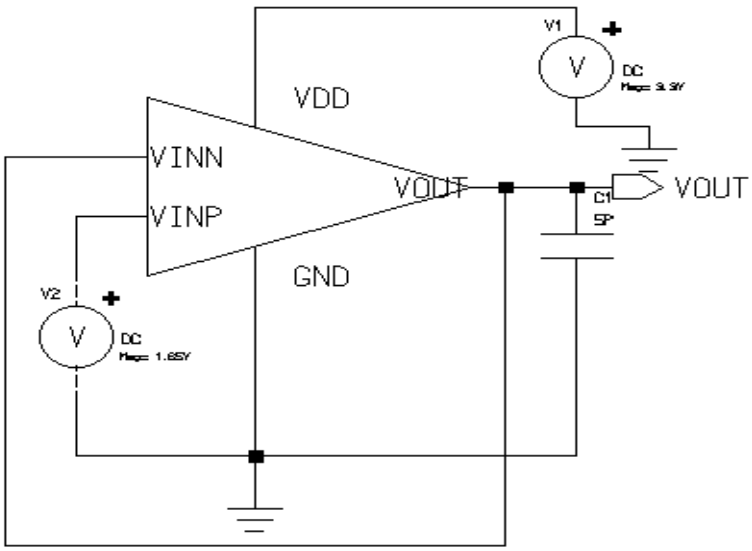

Figure 5.13: Schematic for the simulation of input common-mode range.

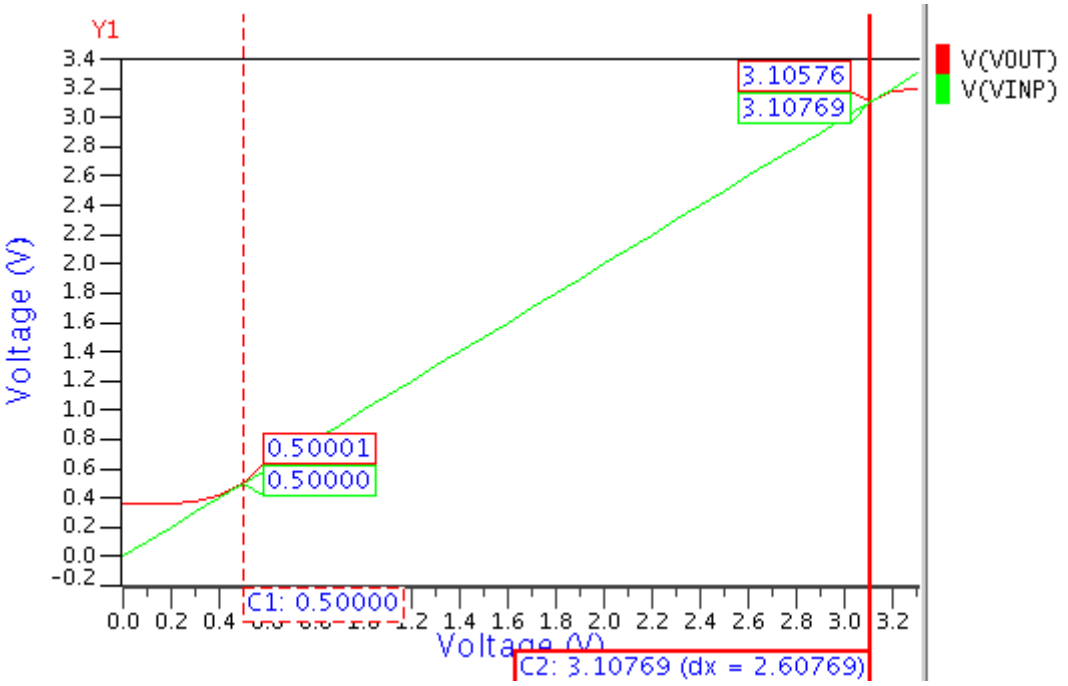

Figure 5.14: Simulation result of input common-mode range (Linearity test).

5.1.9 Variation of Frequency Response with Load Capacitance

Fig. 5.15-5.17 shows the effect of variation of load capacitance (1pF, 5pF, 10pF) on the frequency response of the op amp.

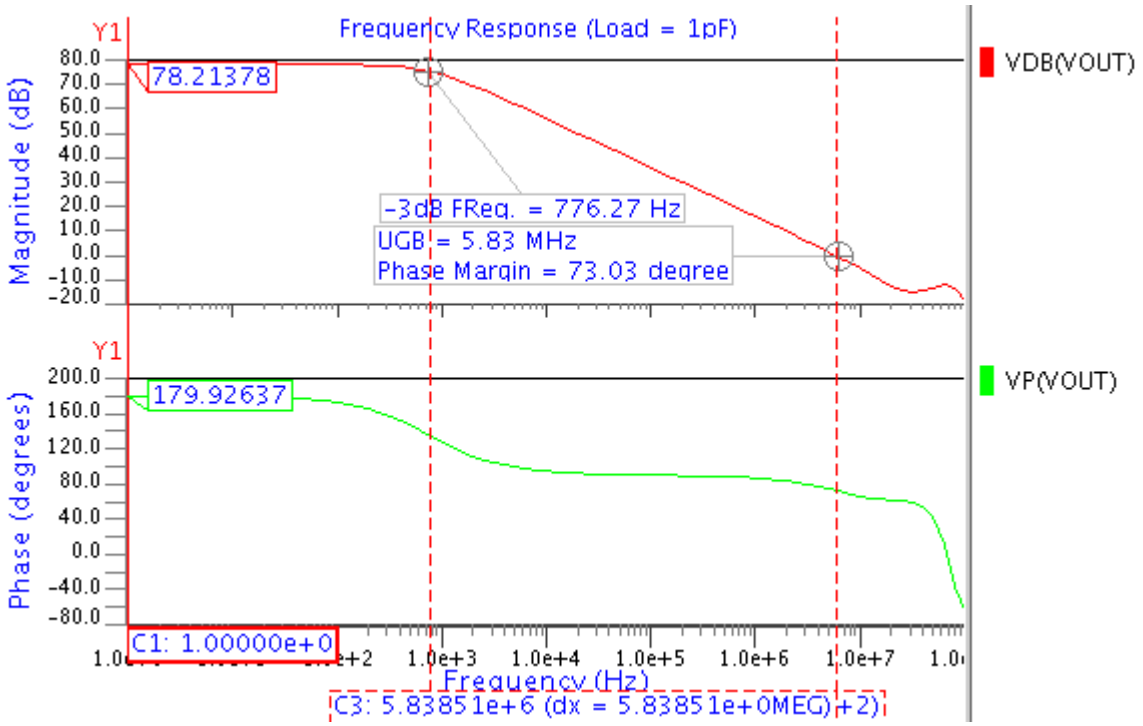

Figure 5.15: Frequency response at load capacitance 1pF.

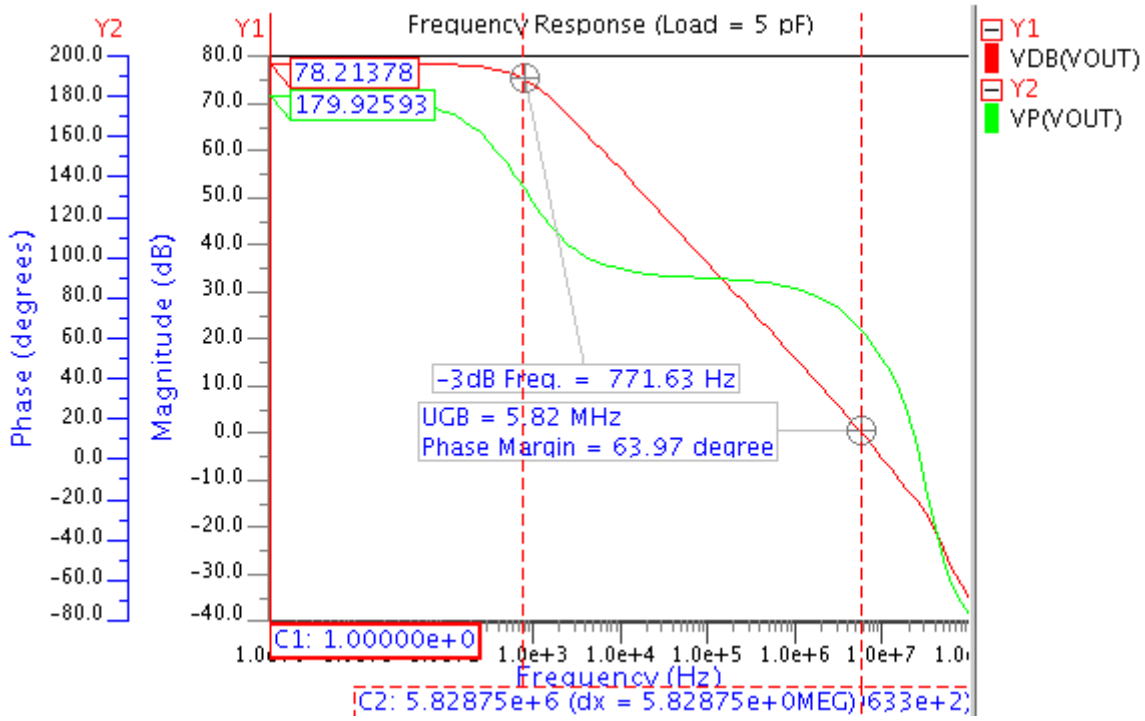

Figure 5.16: Frequency response at load capacitance 5pF.

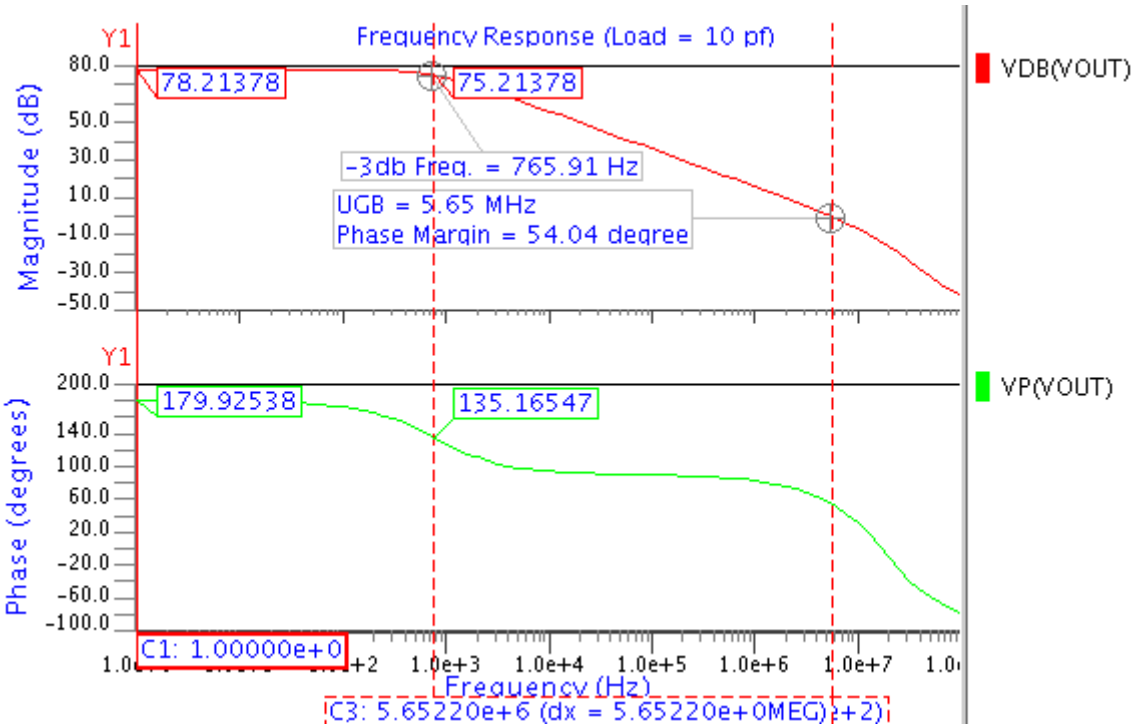

Figure 5.17: Frequency response at load capacitance 10pF.

Table 5.2: Variation of Unity Gain Bandwidth and phase margin with change in the Load Capacitance (C_L)

Load capacitance (C_L) (pF)	**Unity gain Bandwidth** (MHz)	**Phase Margin** (degree)
1	5.83	73.03
5	5.82	63.97
10	5.65	54.04

Table 5.2 shows there is not very much variation on the UGB and phase margin with the variation in the load capacitance (C_L) similar is the case with the slew rate it does not change significantly with the variation in load capacitance. But these three parameters changes significantly with compensation capacitance (C_c).

5.1.10: Effect of Variation of Compensation Capacitance (*Cc*)

Figures given below show the effect variation of *Cc* on the frequency response.

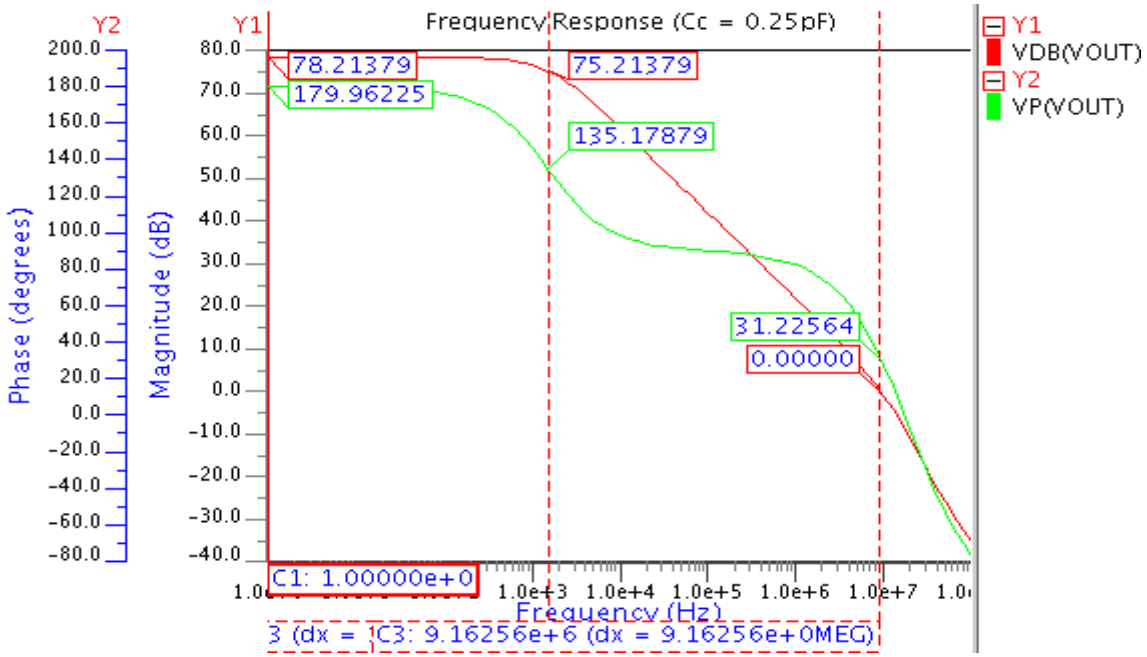

Figure 5.18: Frequency response variation with *Cc* =0.25pF.

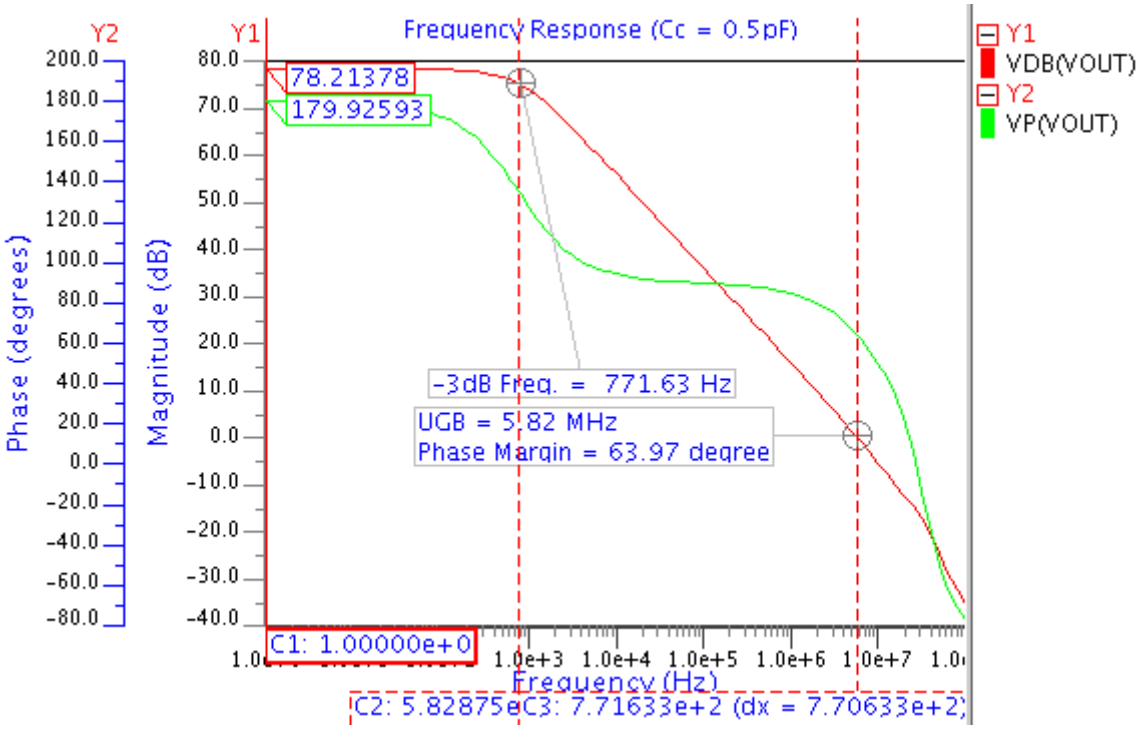

Figure 5.19: Frequency response variation with *Cc* =0.5pF.

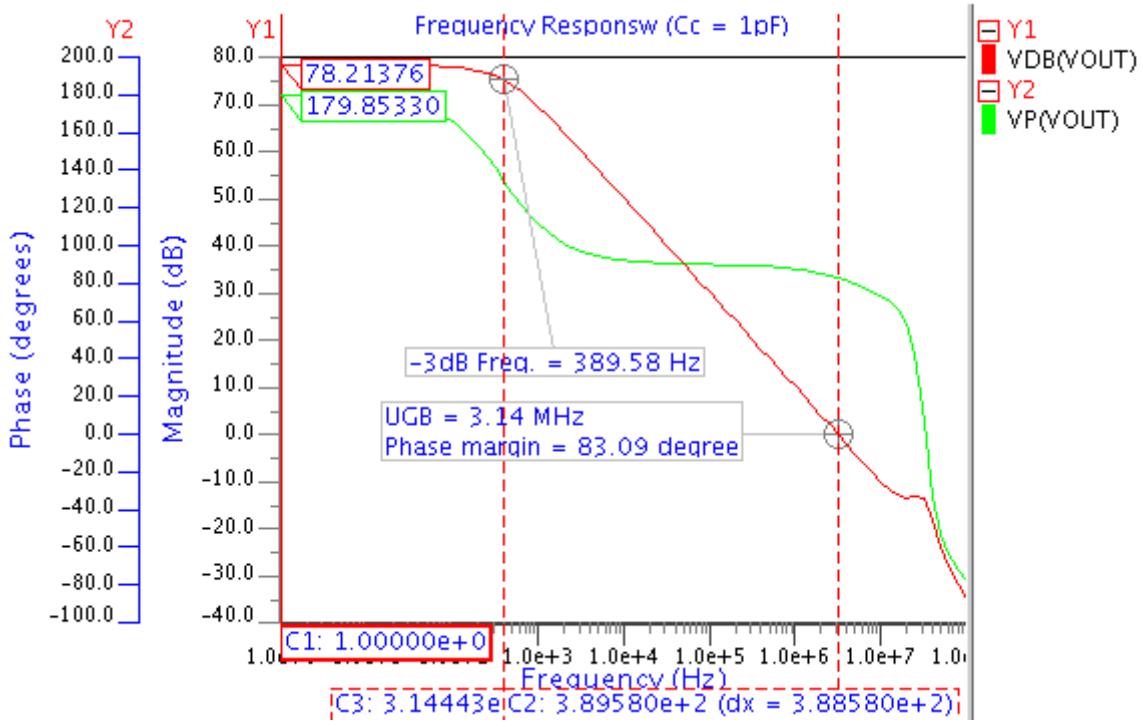

Figure 5.20: Frequency response variation with *Cc* =1pF.

Table 5.3: Variation of Unity Gain Bandwidth and phase margin with change in the compensation capacitance (*Cc*)

Compensation Capacitor *Cc* (pF)	**Unity Gain Bandwidth** (MHz)	**Phase Margin** (degree)
0.25	9.16	31.22
0.50	5.82	63.97
1.00	3.14	83.09

Table 5.3 shows the unity gain bandwidth and phase margin changes with compensation capacitance.

5.1.11 Effect of variation of Temperature on Frequency Response

Fig. 5.21 shows the effect of variation of temperature from -20^{o} to +100^{o} on AC response.

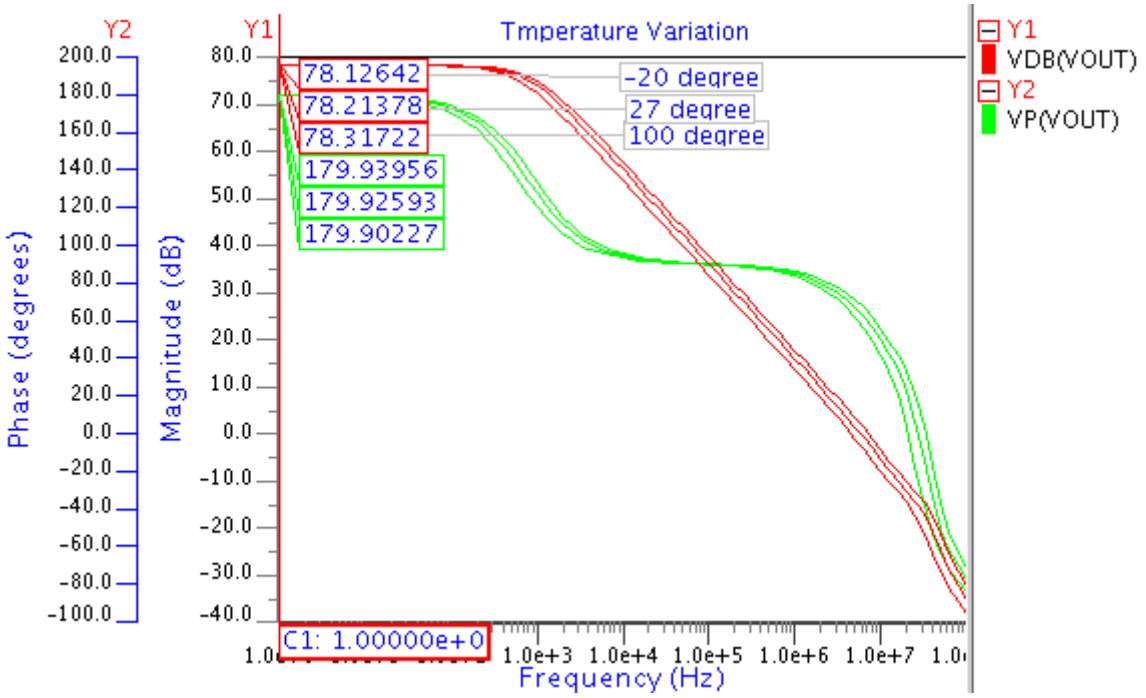

Figure 5.21: Frequency response with temperature variation -20°C to +100°C.

Table 5.4: Variation of UGB and phase margin with change in the temperature

Temperature (Celsius)	**Unity Gain Bandwidth** (MHz)	**Phase Margin** (degree)
-20º	7.08	64.12
+27º	5.82	63.97
+100º	4.47	64.11

Results shows as the temperature increase DC gain increases and UGB decreases.

5.1.12 Variation of slew rate with change in the compensation capacitor values (*Cc*)

Fig. 5.22 shows the variation of the slew rate with the compensation capacitance. Slew rate is inversely proportional to this capacitance value.

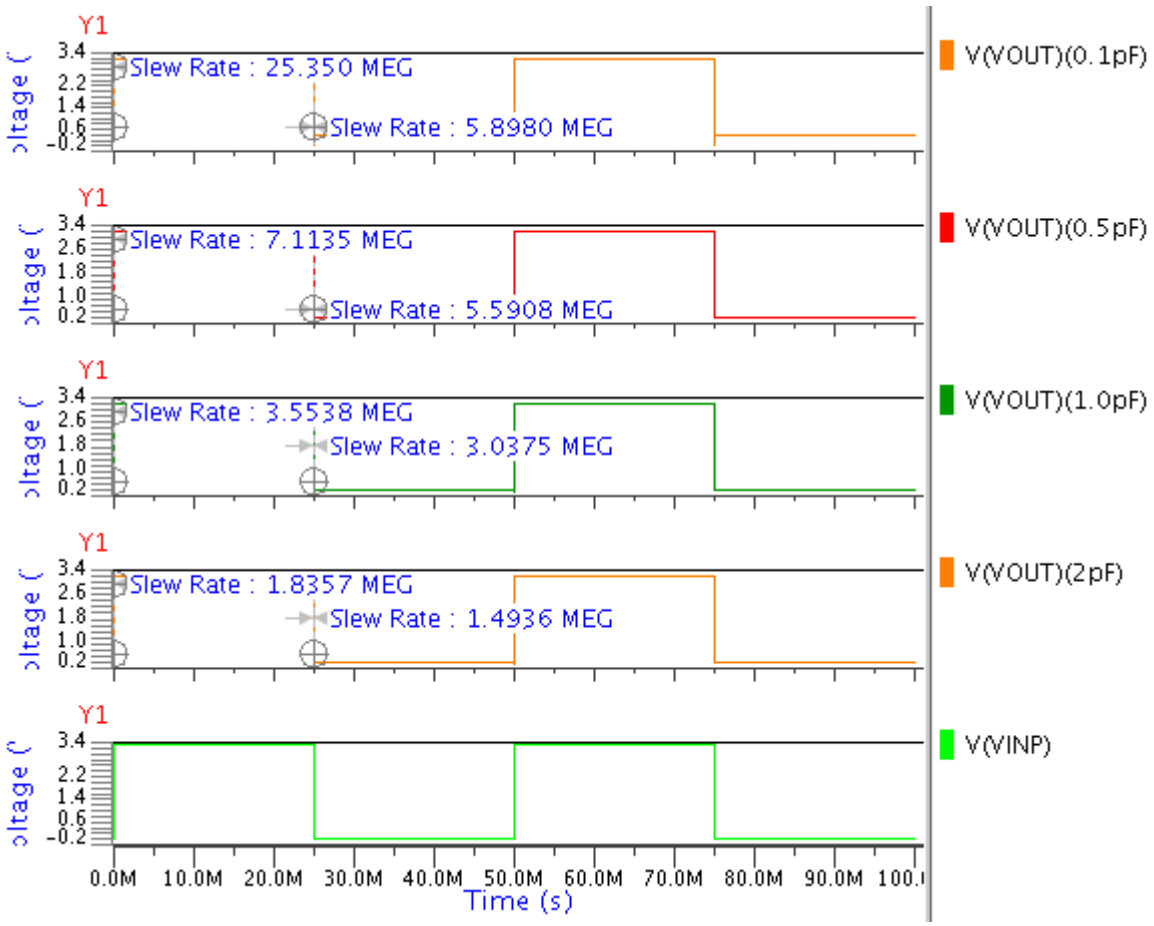

Figure 5.22: Variation of slew rate with change in the compensation capacitor values.

Table 5.5: Variation of slew rate with change in the compensation capacitance (*Cc*)

Cc (pF)	**+ve SR** (V/μs)	**-ve SR** (V/μs)
0.25	25.35	5.89
0.50	7.11	5.59
1.00	3.55	3.03

Results from Table 5.5 shows that slew rate varied inversely with compensation capacitor values.

5.1.13 Simulation Results Summary

Table 5.6: Simulation Results of Op Amp

Specification parameters	**Target specifications**	**Typical Results**
Low frequency gain (dB)	>80	78.21
Unity Gain Bandwidth (MHz)	5	5.82
Phase Margin (degree)	65	63.97
Slew Rate(+ve) (V/μs)	5 .5	7.11
Slew Rate(-ve) (V/μs)	5 .5	5.58
CMR (Volt)	0.65 – 2.65	0.5 – 3.10
OS (Volt)	0.2 – 3.1	0.125-2.95
PSRR (dB)	-	117.73
CMRR (dB)	-	89.05
Settling Time (1%) (μs)	-	1.44
Power Dissipation (μW)	-	144.34

Table 5.6 shows that the values of op amp parameter such as UGB, slew rate, and CMR are in good agreement with target specifications, while the dc gain of 78.21 dB with a variation of 2.23% and phase margin of 63.97° with a variation of 1.58 % is achieved.

5.2 Process Corner Simulation

Thus it is necessary to check the circuit performance at every expected corner of the process variation. The simulation done considering all probabilities of process parameter variation is called as process corner simulation. Here in this simulation process parameter like oxide thickness, mobility and electrical parameter threshold voltage are considered with variations of 6%, 6%, and 8% respectively.

5.2.1 AC Response

The following figures (Fig. 5.23 to Fig. 5.26) show process corner simulation for AC analysis of the op amp.

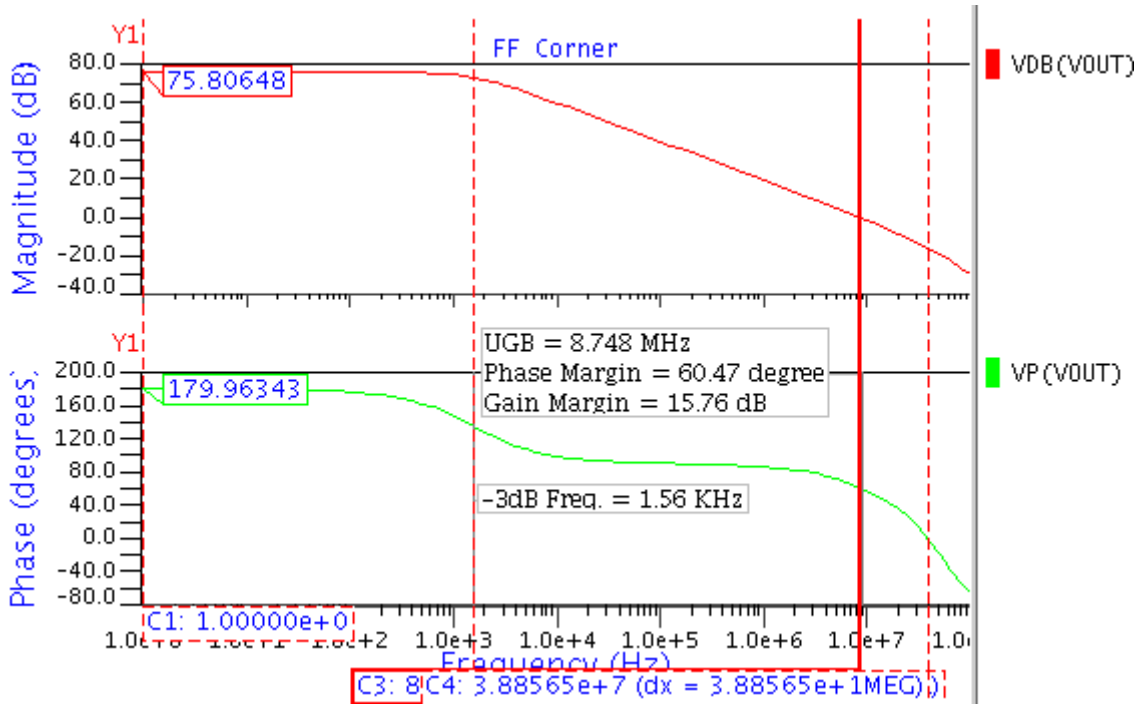

Figure 5.23: Process corner F-F simulation for AC response.

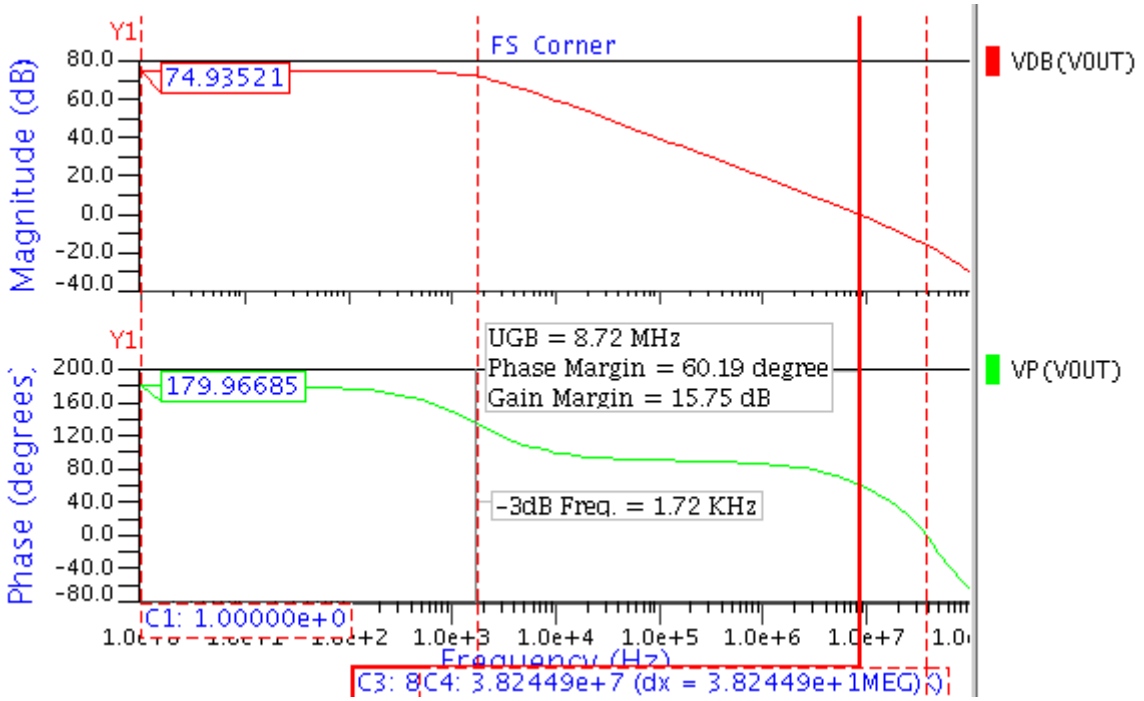

Figure 5.24: Process corner F-S simulation for AC response.

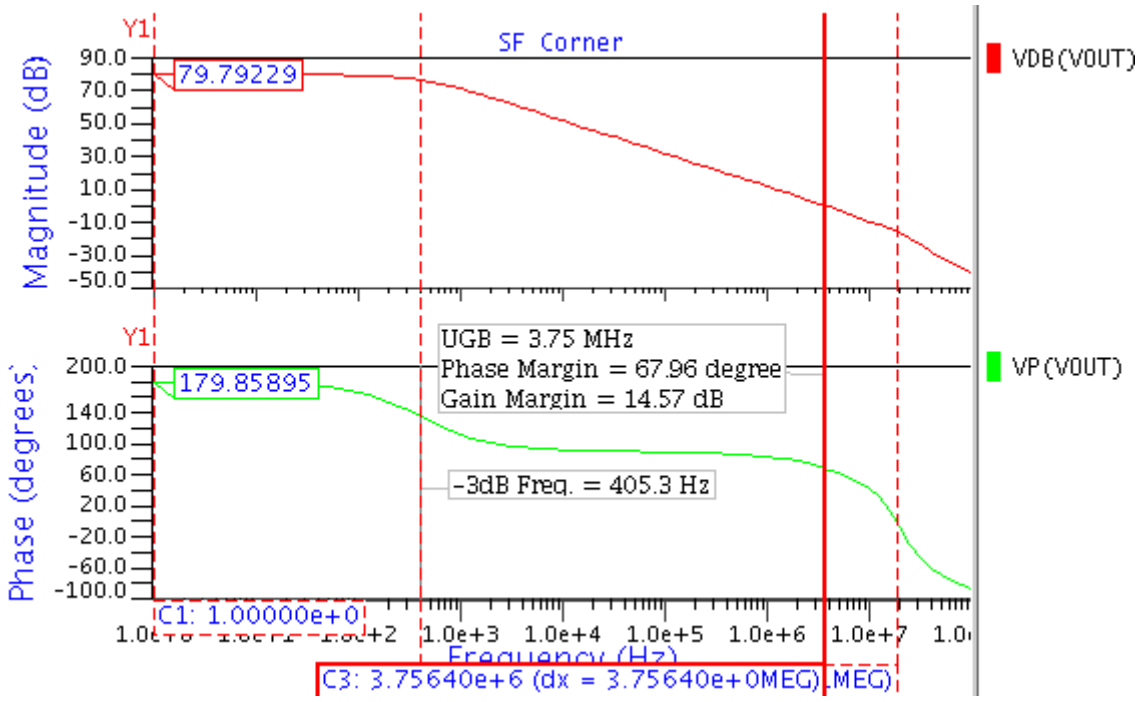

Figure 5.25: Process corner S-F simulation for AC response.

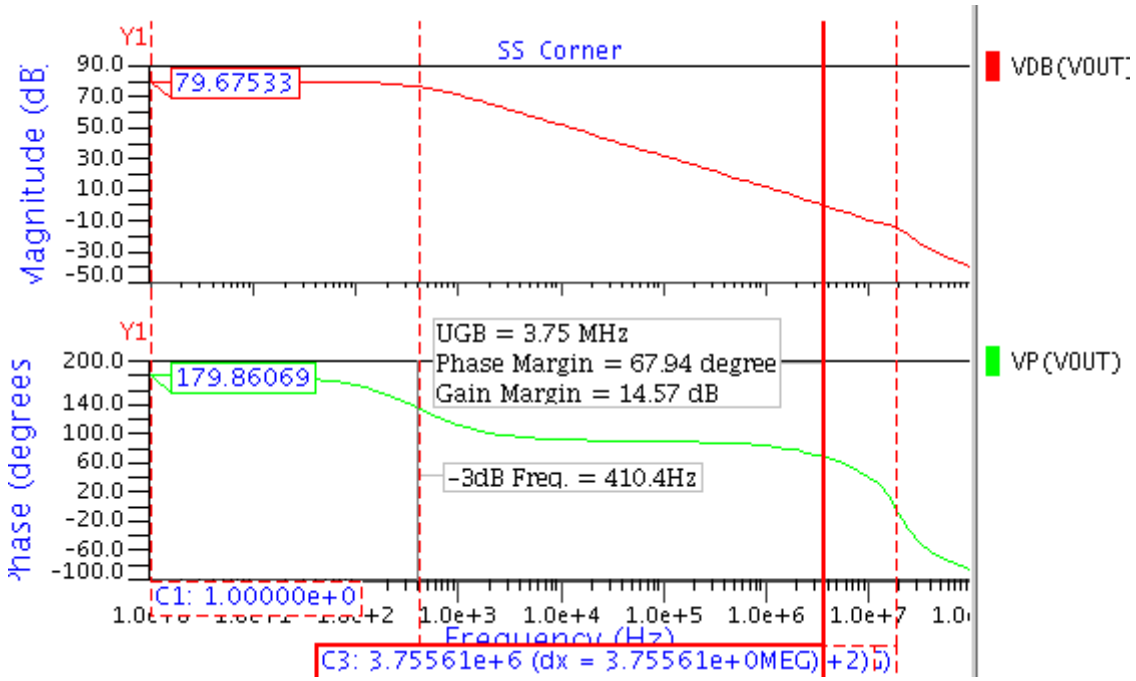

Figure 5.26: Process corner S-S simulation for AC response.

5.2.2 CMRR

Fig. 5.27 shows process corner simulations results for CMRR for all four process corners.

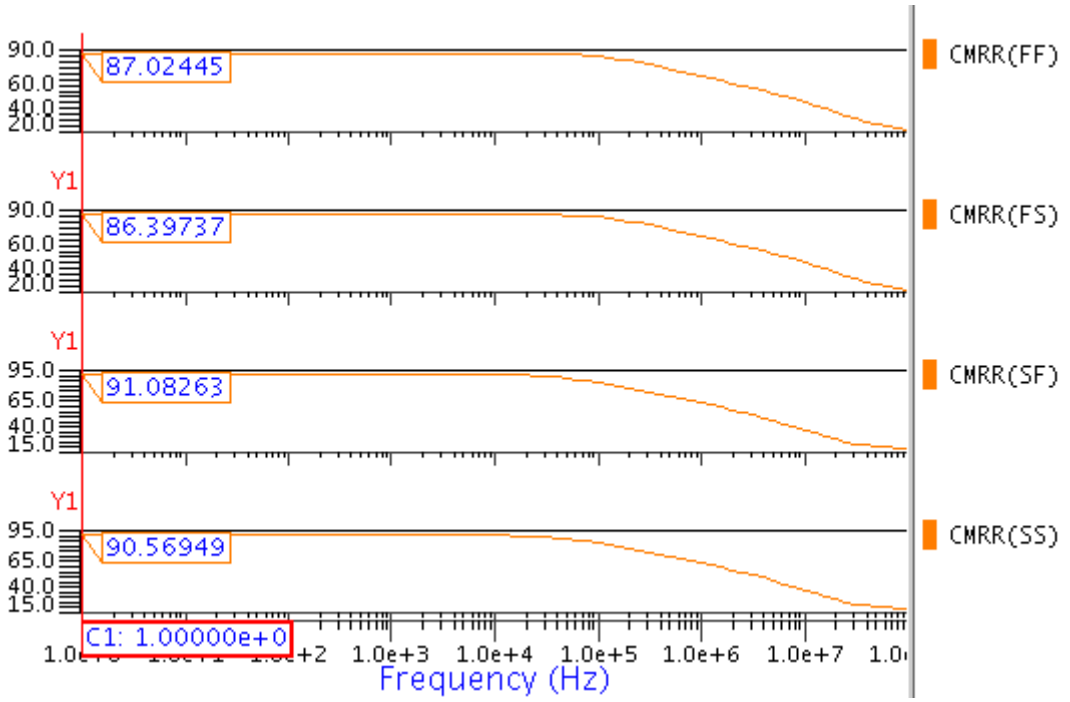

Figure 5.27: Process corner S-S simulation for CMRR.

5.2.3 PSRR

Fig. 5.28 shows process corner simulation results for positive PSRR.

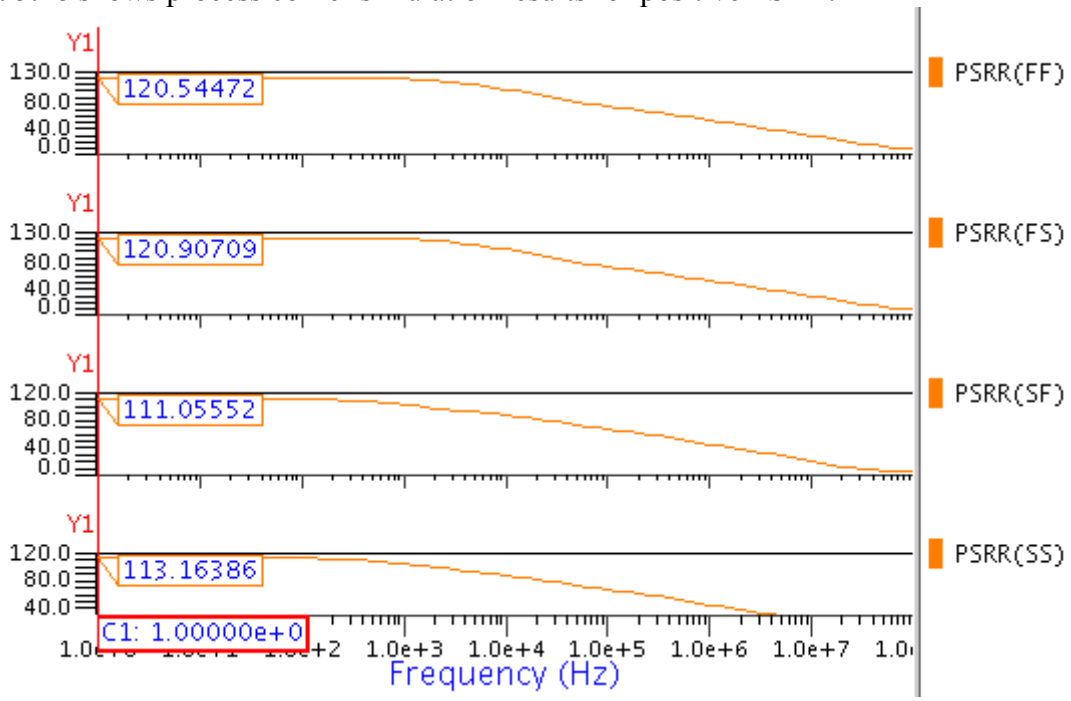

Figure 5.28: Process corner simulations for PSRR.

5.2.4 Slew Rate

Fig. 5.29 shows process corner simulation results for positive slew rate.

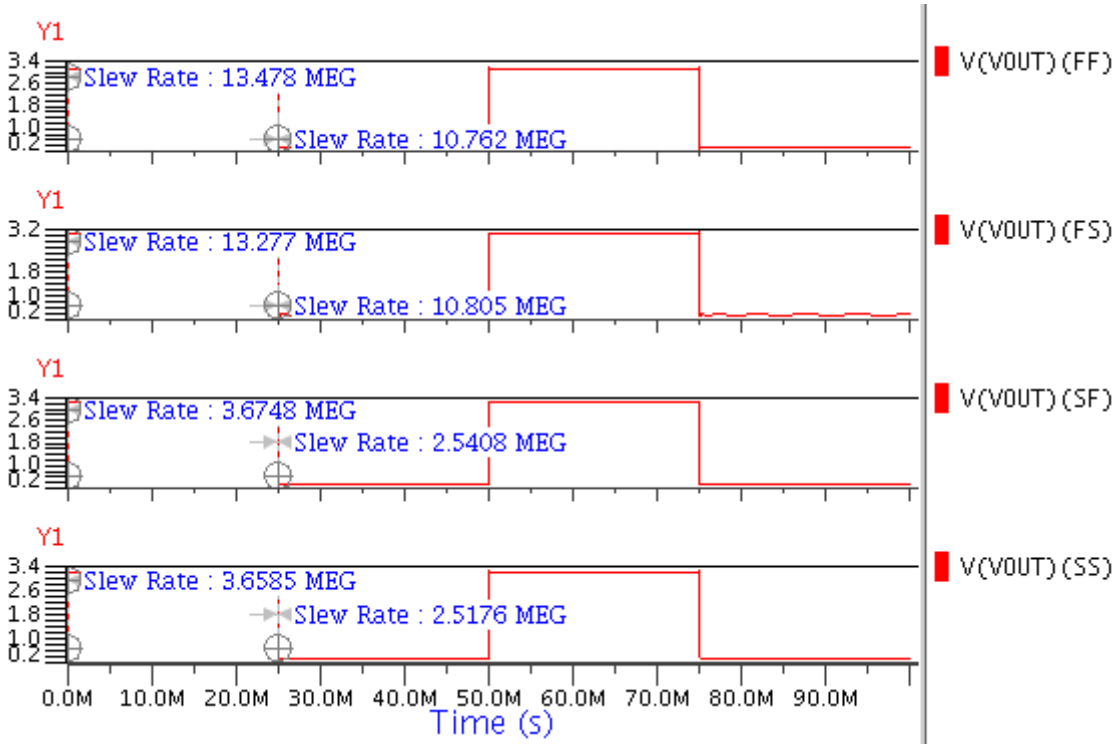

Figure 5.29: Process corner simulations for slew rate.

5.3 Process Corner Simulation Results Comparison

The table below shows the different parameters value for typical, SS, FS, FF and SF process corners.

Tables 5.7: Complete process corner simulation with typical values

Specifications		**Typical Value**	**Process corner FF**	**Process corner FS**	**Process corner SF**	**Process corner SS**
Power Dissipation (μW)		144.34	284.51	285.39	74.10	74.59
DC Gain (dB)		78.21	75.80	74.93	79.79	79.67
UGB (MHz)		5.82	8.74	8.72	3.75	3.75
3dB Frequency (Hz)		771.63	1.56×10^3	1.72×10^3	405.3	410.4
Phase Margin		63.97°	60.47	60.19	67.96	67.94
Gain Margin (dB)		15.24	15.76	15.75	14.57	14.57
Slew rate (V/μs)	+ve SR	7.11	13.47	13.27	3.67	3.65
	-ve SR	5.58	10.76	10.80	2.54	2.51
CMRR (dB)		89.05	87.02	86.39	91.08	90.56
PSRR (dB)		117.73	120.54	120.90	111.05	1113.16

5.4 Layout of Operational Amplifier

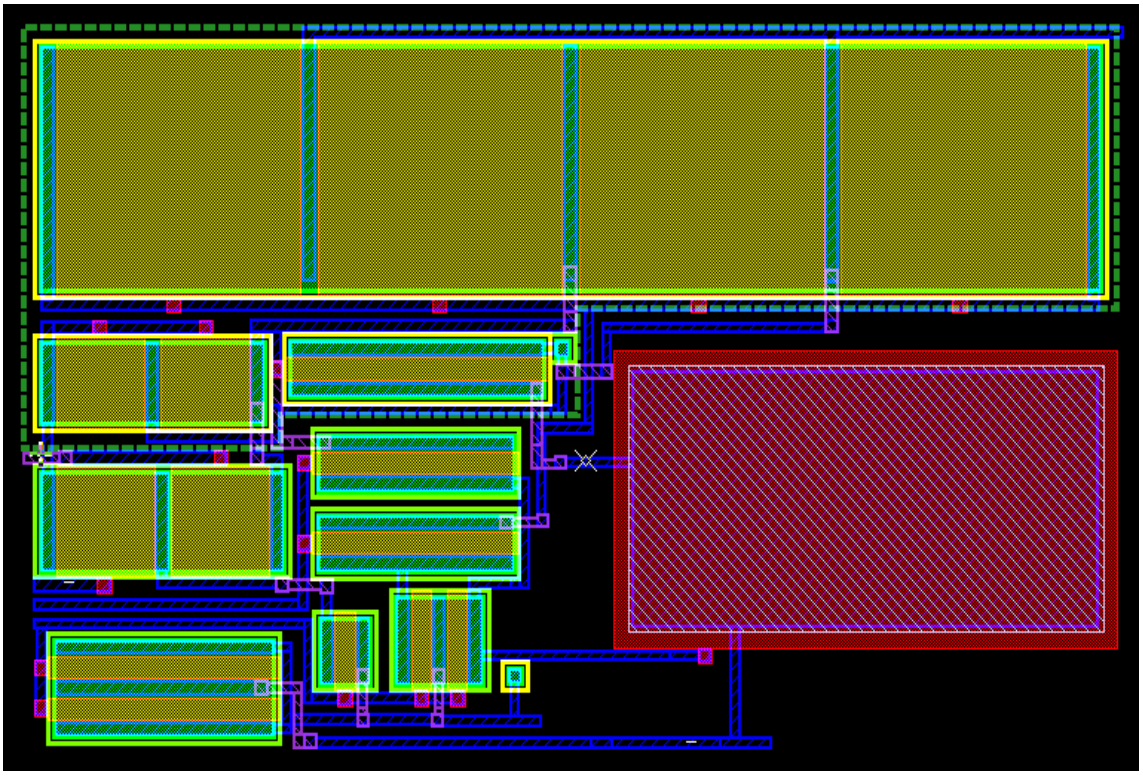

Figure 5.30: Layout of designed op amp with compensation capacitor.

5.4.1 LVS and PEX results

This design is DRC clean, and layout of the circuit is matched with schematic, both DRC and LVS are verified by the Calibre.

Source Netlist

```
* LVS netlist generated with ICnet by 'sachin' on Tue Jul  7 2009 at 03:47:36

*
* Globals.
*
.global GND

*
* Component pathname : /home/sachin/finalnew
*
.subckt finalnew  VOUT GND_esc1 VB VBB VDD VINN VINP

        *.connect GND GND_esc1
        MN1 N$7 VINN N$6 GND n L=7u W=6.3u
        C2 N$4 VOUT notchedrow 500f
        C1 VOUT GND notchedrow 5000f
        MN8 VOUT VB GND GND n L=1.4u W=31.5u
        MP5 VOUT N$1 VDD VDD p L=1.4u W=18.2u
        MN7 N$4 VB GND GND n L=1.4u W=5.6u
        MN6 N$3 VB GND GND n L=1.4u W=5.6u
        MN5 N$1 VBB N$4 GND n L=1.4u W=14u
        MN4 N$2 VBB N$3 GND n L=1.4u W=14u
        MP4 N$1 N$2 VDD VDD p L=17.5u W=31.15u
        MP3 N$2 N$2 VDD VDD p L=17.5u W=31.15u
        MN3 N$6 VB GND GND n L=1.4u W=4.2u
        MP2 N$1 N$7 VDD VDD p L=6.3u W=5.25u
        MP1 N$7 N$7 VDD VDD p L=6.3u W=5.25u
        MN2 N$1 VINP N$6 GND n L=7u W=6.3u
.ends finalnew
```

Layout Netlist

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* File: final_layout.pex.netlist
* Created: Tue Jul  7 03:50:30 2009
* Program "Calibre xRC"
* Version "v2006.2_30.26"
*
.include "final_layout.pex.netlist.pex"
.subckt finalnew  VOUT GND VDD
*
* VB VB
* VBB VBB
* VINN VINN
* VDD VDD
* GND GND
* VOUT VOUT
* VINP VINP
MN8__1 N_VOUT_MN8__1_d N_VB_MN8__1_g N_GND_MN8__1_s N_GND_MN8__1_b n L=1.4e-06
+ W=1.575e-05 AD=1.89e-11 AS=1.7325e-11
MN8__2 N_VOUT_MN8__2_d N_VB_MN8__2_g N_GND_MN8__2_s N_GND_MN8__1_b n L=1.4e-06
+ W=1.575e-05 AD=1.89e-11 AS=1.7325e-11
MN1 N_N$7_MN1_d N_VINN_MN1_g N_N$6_MN1_s N_GND_MN8__1_b n L=7e-06 W=6.3e-06
+ AD=6.93e-12 AS=7.56e-12
MN2 N_N$1_MN2_d N_VINP_MN2_g N_N$6_MN2_s N_GND_MN8__1_b n L=7e-06 W=6.3e-06
+ AD=6.93e-12 AS=7.56e-12
MN4 N_N$2_MN4_d N_VBB_MN4_g N_N$3_MN4_s N_GND_MN8__1_b n L=1.4e-06 W=1.4e-05
+ AD=1.54e-11 AS=1.54e-11
MN5 N_N$1_MN5_d N_VBB_MN5_g N_N$4_MN5_s N_GND_MN8__1_b n L=1.4e-06 W=1.4e-05
+ AD=1.54e-11 AS=1.54e-11
MN3 N_N$6_MN3_d N_VB_MN3_g N_GND_MN3_s N_GND_MN8__1_b n L=1.4e-06 W=4.2e-06
+ AD=4.62e-12 AS=4.62e-12
MN6 N_N$3_MN6_d N_VB_MN6_g N_GND_MN6_s N_GND_MN8__1_b n L=1.4e-06 W=5.6e-06
+ AD=6.16e-12 AS=6.72e-12
MN7 N_N$4_MN7_d N_VB_MN7_g N_GND_MN7_s N_GND_MN8__1_b n L=1.4e-06 W=5.6e-06
+ AD=6.16e-12 AS=6.72e-12
MP1 N_N$7_MP1_d N_N$7_MP1_g N_VDD_MP1_s N_VDD_MP1_b p L=6.3e-06 W=5.25e-06
+ AD=5.775e-12 AS=6.3e-12
MP3__1 N_N$2_MP3__1_d N_N$2_MP3__1_g N_VDD_MP3__1_s N_VDD_MP1_b p L=1.75e-05
+ W=1.5575e-05 AD=1.71325e-11 AS=1.869e-11
MP2 N_N$1_MP2_d N_N$7_MP2_g N_VDD_MP2_s N_VDD_MP1_b p L=6.3e-06 W=5.25e-06
+ AD=5.775e-12 AS=6.3e-12
MP5 N_VOUT_MP5_d N_N$1_MP5_g N_VDD_MP5_s N_VDD_MP1_b p L=1.4e-06 W=1.82e-05
+ AD=2.002e-11 AS=2.002e-11
MP4__1 N_N$1_MP4__1_d N_N$2_MP4__1_g N_VDD_MP4__1_s N_VDD_MP1_b p L=1.75e-05
+ W=1.5575e-05 AD=1.869e-11 AS=1.869e-11
MP4__2 N_N$1_MP4__2_d N_N$2_MP4__2_g N_VDD_MP4__2_s N_VDD_MP1_b p L=1.75e-05
+ W=1.5575e-05 AD=1.869e-11 AS=1.869e-11
MP3__2 N_N$2_MP3__2_d N_N$2_MP3__2_g N_VDD_MP3__2_s N_VDD_MP1_b p L=1.75e-05
+ W=1.5575e-05 AD=1.71325e-11 AS=1.869e-11
C2 N_N$4_C2_pos N_VOUT_C2_neg 499.392f
C1 N_GND_C1_pos N_VOUT_C1_neg 5.00291p
```

Chapter 6

Conclusion and Future Scope

6.1 Conclusion

In this thesis a two stage high gain low power operational amplifier has been designed. In the design of the operational amplifier the compensation capacitor play an important role for power consumption and noise parameters. As the power consumption decreases with the compensation capacitor value, current buffer approach has been used which is less sensitive to process variations. The operational amplifier has been designed and simulated using Eldo (Mentor Graphics) in 0.35 μW CMOS process technology. The operational amplifier achieves dc gain 78.21 dB, unity gain bandwidth 5.82 MHz, phase margin 63.97°. Also the power consumption, PSRR, and CMRR of the operational amplifier are obtained as 144.3μW, 117.73 dB, and 89.05 dB respectively.

6.2 Future Scope

Due to the nature of the wide research topic, there are still several areas of improvement for future work in this op amp. Parameters such as the power-supply rejection ratio, mismatched offset and noise can be improved by increasing the device area while maintaining the W/L ratio constant.

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