“A Comparative Study of Performance of Memristor Based Logic Design Family and Circuits”

A Thesis Submitted in Fulfillment of the Requirement for the Award of the Degree of

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In

VLSI Design

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DECLARATION

I, VIVEK RATURI hereby declare that the work presented in this thesis entitled **"A Comparative Study of Performance of Memristor based logic design family and circuits"** in partial fulfillment of the requirement for the award of degree of Master of Technology submitted at Electronics and Communication Engineering Department, Thapar University, Patiala is an authentic record of work carried out under supervision of Dr. Mayank Kumar Rai (Assistant Professor, ECED, Thapar University, Patiala). The matter presented in this this has not been submitted either in part or full to any other university or institute for the award of any other degree.

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It is certified that the above statement made by the candidate is correct to the best of my knowledge and belief.

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ABSTRACT

Memristor is a passive component with variable resistance which depends on the amplitude of previous applied voltage across it. The application of Memristor in field of memories is not a new concept. Moreover, it can be used in neuromorphic, analog and digital applications. From many years ago, all the logic operations were performed using CMOS design methodology. The semiconductor industry is focusing on continuous scaling of technology. But the scaling in technology is on the edge of saturation level, therefore more scaling is difficult to attain. So the industry is shifting its focus on finding an alternative of CMOS technology for performing logic operations.

One of the promising substitutes for CMOS technology is Memristor. The resistive switching characteristics of Memristor make it a suitable candidate to be used for logic implementation. In this thesis, the focus is on the usage of Memristor for implementation of logic gates. Two types of logic styles are considered. In first logic style, logic is performed within memory (IMPLY logic family) where as in other, voltage decides logic where memristors are used for computation purpose only (Hybrid CMOS logic family). Basic logic gates of each family are constructed and various design constraints that affects the feasibility of logic are analysed. A design approach to design AND, OR and NOT gate based on Memristor which provides better trade-off between area, power and speed as compare to both logic styles is proposed. A comparative study of IMPLY logic family, Hybrid-CMOS logic family and proposed logic family is also presented.

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LIST OF ACRONYMS

VLSI	Very Large Scale Integration
MRL	Memristor Ratioed Logic
TEAM	Threshold Adaptive Memristor Model
IMPLY	Memristor Based Material Implication
MAGIC	Memristor Aided Logic

CHAPTER

1

`INTRODUCTION

1.1 MEMRISTOR OVERVIEW

Up to 1971, there were only three known passive circuit elements i.e. Resistor, Inductor and Capacitor and they present following relations-

$dv = R.di$(Relates voltage and current, known as Ohm's Law)

$dq = C.dv$(Relates charge and voltage)

$d\emptyset = L.di$(Relates flux with current)

Moreover it is also known that,

$$I = \frac{dq}{dt}$$

$$V = \frac{d\emptyset}{dt}$$

Where, $\emptyset$ represent flux linkage, Q represent charge, I represent current, R represent resistance, L represent inductance, C represent capacitance andT represents time.

Leon Chua analyzed these relationships and proved mathematically that there should be a fourth fundamental passive element which links charge with flux linkage and named it memristor [2]

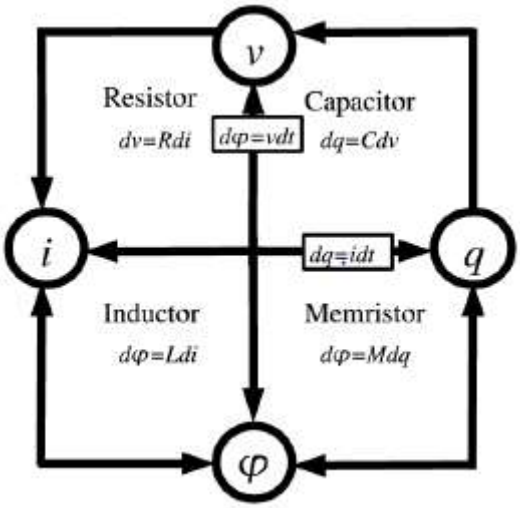


Figure 1.1: Relationship between fundamental elements [2].

Memristor is denoted by M and holds relation given by-

$$d\emptyset = M.dq \qquad 1.1$$

$$\mathrm{M(q)} = \frac{\mathrm{d}\emptyset}{\mathrm{dq}} \qquad 1.2$$

Divide denominator and numerator of R.H.S of equation (2), we get

$$V = M(q).I(t) \qquad 1.3$$

Where, M (q) represents memristance of Memristor.

So memristor defines contraction of “memory plus resistance” because of its property that it remember its recent resistance even if the voltage supply is disconnected. So it is a passive circuit element that has two terminals and it changes its resistance on the basis of polarity of voltage and time to which that voltage is applied and if the voltage supply is disconnected, then it memorizes the most recent resistance until the supply is given again.

1.2 ANALOGY WITH PIPE

Analogy of memristor looks very similar like behavior of pipe. Suppose resistor is analogous to a pipe, electric charge is analogous to the flow of water through that one pipe and resistance is analogous to the diameter of that pipe.

Up to 1971, resistance resembles to have a fixed diameter pipe but memristor is analogous to a pipe whose diameter changes as a function of amount of water and its direction. When water flow in only 1 direction then, diameter of that pipe expands (means decrease in resistance). But when water flow in opposite direction then, diameter of that pipe shrinks (means increase in resistance), also when we turn off the water flow then memristor memorizes the last diameter when the last water flow went inside that pipe. This property of memristor makes him a powerful candidate to be used as memory cell in non-volatile memory.

1.3SYMBOL OF MEMRISTOR

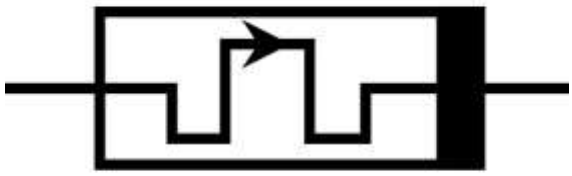


Figure 1.2: Symbol of memristor

Fig.1.2 shows the symbol of memristor. When the current flows in the same direction as indicated in the Fig. 1.2 (out of black strip) the value of memristance increases and vice versa.

1.3 DISCOVERY OF MEMRISTOR

Professor Widrow in 1960 proposed a new element named memistor [16].The proposed device has 3 terminals and the conductance between two terminals was defined as a function of time integral of current over third terminal (charge of 3rd terminal).memristor and Memistor seems similar but later it was proved that they are different.

In 1968, a paper was published by F.Argal [17], having the experimental results same as presented by Stanley Williams related to memristor model later [3].

In 1971, Leon Chua theoretically defined memristor by presenting a missing relation between flux linkage and charge [2].

Leon Chua and S.M. Kang in 1976gave two basic theoretical approaches to model device [4] and raised their theory to high order non-linear circuit elements [18].

S. Thakoor in 1990 presented an electrically programmable device having variable resistance using Tungsten oxide [19].

Bout and Rajgobal after 4 years, in 1994 presented an article [20] about Alas|GaAs|alas quantum well diodes having I-V characteristics similar to Memristor.

In between 1994 to 2008, researchers presented a number of other devices from all over the world having the characteristics exactly like that of memristor but no one was able to link their work with that of memristor proposed byL.O.Chua [4].

In 2008, we have first fabricated memristor device developed by IQS lab team of HP labs leaded by Stanley Williams. In 2008, DimtriStrukov, G. S. Snider, D. R. Stewart, and S. Williams [3], provides a link between Chua's Memristor and their two terminal device. They also proposed charge controlled memristor and flux controlled memristor as-

For a charge controlled memristor, the voltage (V (t)) across it is given by-

$$V(t) = M\big(q(t)\big).I(t) \tag{1.4}$$

$$M\big(q(t)\big) = \frac{d\emptyset(q)}{dq} \tag{1.5}$$

I (t) represent current through memristor.

For a current controlled memristor, the current is given by-

$$\mathrm{I(t)} = \mathrm{W}\big(\emptyset(\mathrm{t})\big).\mathrm{V(t)} \tag{1.6}$$

$$\mathrm{W}(\emptyset) = \frac{\mathrm{dq}(\emptyset)}{\mathrm{d}\emptyset} \tag{1.7}$$

Where M (q) has unit of resistance and W (q) has unit of conductance.

Power dissipation in both types of memristors is given by-

$$P(t) = M\big(q(t)\big).I^2(t) \quad 1.8$$

$$P(t) = W\big(\emptyset(t)\big).V^2(t) \quad 1.9$$

In 1976, L. O. Chua and his student S. M. Kang defined memristive system in [4] given by:

$$y = g(x,u,t).u \quad 1.10$$

$$\frac{dx}{dt} = f(x,u,t) \quad 1.11$$

Where 'u' is the input of system, 'y' is the output of system, 'x' is the state variable, 'g' is a continuous n-dimensional scalar function, 'f' is a continuous n-dimensional function.

1.5WORKING OF Tio_2MEMRISTOR

In 2008, Stanley Williams presented an article describing how a solid state device behaves like memristor. In this device, there is no concept of flux linkage, neither having capability of charge storage like capacitor but still able to achieve the dependence of resistance on current's history [3].

The device presented by HP has two thick electrodes (one of platinum and one of titanium) of 5nm and in between these two electrodes, a film of Titanium di-oxide (Tio_2) of 50nm was there. This Tio_2 film consists of two different layers one of which is pure Tio_2 and in other about 2.5% of oxygen is missing and thus it is oxygen deficient (Tio_{2-x}) close to top electrode. Since Tio_{2-x} is oxygen deficient so vacancies are donor and thus positively charged so for this reason Tio_{2-x} is conductive and have low resistance and Tio_2 layer has high resistance.

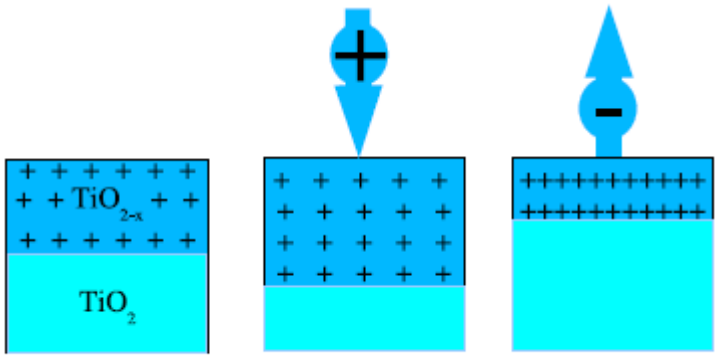


Figure1.3: Working of memristor.

Fig. 1.3 shows the working of memristor. When positive voltage is applied to top electrode, the positive charged vacancies are repelled and moves down to pure Tio_2 layer this result in a decrement in width of Tio_2 and increment in width of Tio_{2-x}, so device resistance drops to minimum value R_{on}. When negative voltage is applied, the positively charged donors are attracted by it and thus Tio_{2-x} decreases in width and Tio_2 increases in width and thus after some time , device reaches to its highest resistance $R_{off.}$. This gives the idea of memristor to be used as a voltage dependent switch. If at any instant, voltage is turned off, the resistance of devices freezes to its last value until voltage cannot be applied again. This provides the concept of using memristor in non-volatile memories and also provides information related to write time.

1.6 TYPES

Based on materials, a number of memristors are implemented. Since hysteresis is a sign of Memristor, so researchers have done large number of experiments with different materials to get the same results presented by Chua [2]. Some of them are:

1.6.1 Tio_2 Memristor

In 1960, the property of Tio_2 have resistive switching was described .After that in between 1960 to 2008, about 300 papers related to Tio_2 were published [21].

In 2000, an article published by IBM presenting similar structure presented later by HP [22].But in 2008, U.S patent application was published by H.P describing the construction of memristor [3]. The working and construction of this memristor is explained above in section 1.4.

1.6.2 Polymeric Memristor

In 2004, Kringer proposed polymeric structure of memristor [23], where polymer is dynamically doped with inorganic dielectrics so that the switching can be improved with the aim of creating memory cells for non-volatile memory. Here in this structure, in between active thin films and electrodes a passive layer is used so that ion extraction from electrode can enhance.

In 2009, Berzina published his improved experimental results on Polymeric memristor which was controlled electrochemically [24].

1.6.3 Ferroelectric Memristor

In 1963, first proposal of Ferroelectric memristor was given [25], where an idea of developing memory through ferroelectric material and how by permanent polarizing

ferroelectric material the conductance of semiconductor material can be changed was described. In 2012, an idea of sandwiching a ferroelectric barrier between two platinum electrodes was given [26]. Application of negative and positive voltage across the junction theoretically results in the switching of resistance from R_{off} to R_{on} or from R_{on} to R_{off} respectively, where $R_{off} >> R_{on}$. Because the dynamics of ferroelectric material is changeable, so always they provide the advantage to fine tune the memristor resistance by electronic process that too without doing a large change in structure thus enhance the reliability of device.

1.6.4 Semiconductor Oxide Memristor

In 2010, first time Sio_2 substrate having characteristics similar to memristor comes into picture [30]. Switching study of memrisistive device based on silicon where silicon-silicon rich oxide was used as active layer was done by Mehonic Et Al. Resistive switching was seen in silicon rich oxide layer and diffused metallic ions has nothing to do with the formation of conductive channel. This device has I-V characteristics similar to pinched hysteresis of memristor and a resistance ratio of $r = \frac{\text{Roff}}{\text{Ron}} = 104$ is achieved or ever higher is also possible.

1.6.5 Graphene Oxide Memristor

By using the film of graphene oxide, Choi proposed construction of memristor [28], this is similar to HP memristor but they replaced Tio_2 with graphene oxide. A thick plastic (6.5 cm^2) was taken and on that they deposited wires of Al (50um wide), then they spin a solution of suspended graphene oxide flakes so a thin film of overlapped flakes was ready and then an array of Al wires was deposited and thus they have 25 memristors of 50um width.

In 2012, S.Williams and HP lab team presented a defected graphene based memristor [29]. It has two electrodes, just after 1^{st} electrode we have defected graphene layer and number of ions next to this layer and then 2^{nd} electrode. For electric field generation, a voltage source is also required. When electric field is active, we have a conducting channel between graphene layer and 2^{nd} electrode.

1.6.6 Resonant Tunneling Diode Memristor

To achieve behavior like that of memristor, in between drain and source, the layers are specially doped in quantum well diodes [27].

1.6.7 Spin MemristiveSystems

Spin memristive systems mainly depends on electron spin degree of freedom. Here in these, polarization of electron spin is altered by magnetic domain movement which separates the

two polarities and this result to have I-V characteristics similar to pinched hysteresis of Memristor. In 2009, Wang Et Al. reported three possible spintronic memristors [31]. Depending on electron transport and electronic interactions, they proved that spintronic device able to have memorized behavior similar to memristor. In 2011, proof of spintronic memristor based on experimental results was given [32].

Also some semiconductor based spintronic structures exists having characteristics exactly to that of memristor [33]. In case of nanostructures, the mechanism depends on ionic transport but here, mechanism depends on electron spin degree of freedom. When the change is experienced in external voltage, then due to diffusion the polarization of electron spin is delayed and this delay responsible for hysteresis loop exactly similar to that of memristor.

1.7 APPLICATIONS OF MEMRISTOR

1.7.1 Programmable Resistors

Programmable resistors are helpful in some analog circuits like filters, amplifiers. A programmable resistor using memristor having good resolution was proposed in [40, 41].

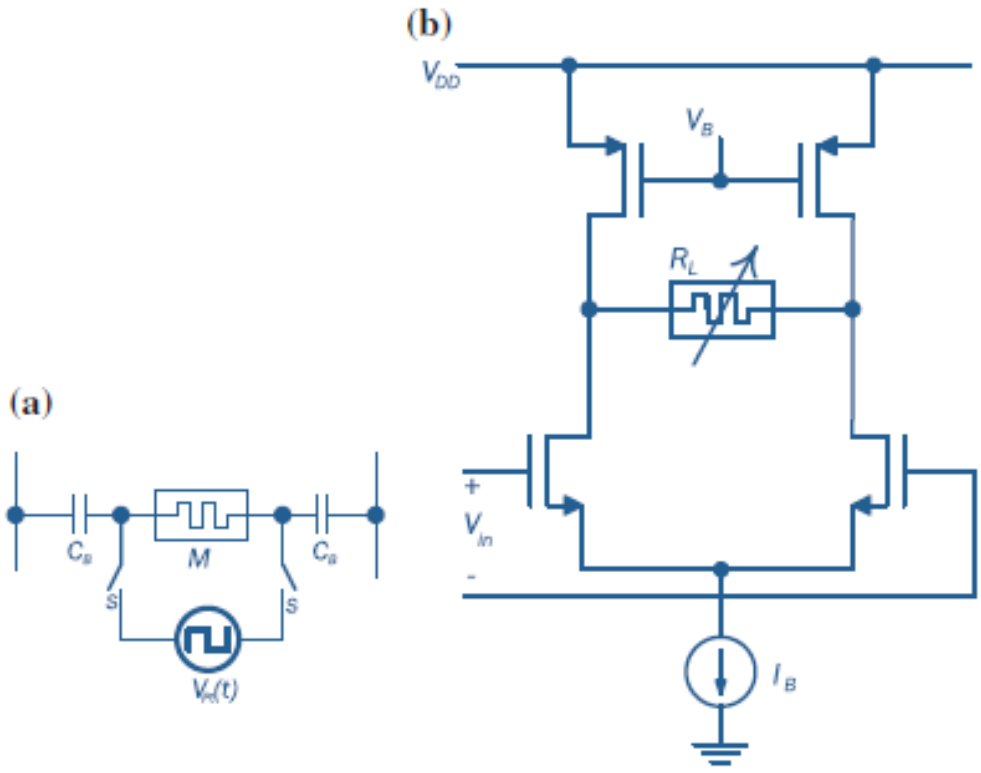


Figure 1.4: (a) programmable resistor circuit using Memristor, (b) use of programmable resistor to achieve programmable gain in amplifier [40, 41].

Simple switches are used in a floating memristor. During normal mode, a programmable memristor provides high resistance (R_{off}). While in programming mode, memristor provides low resistance (R_{on}). Even order mismatch and DC mismatch is blocked by blocking capacitors $c_{s.}$

1.7.2 Sinusoidal Oscillators Based On Memristor

Basic principle is replacement of few or all resistors with memristor in oscillators and analyzes the response [36-38]. In [37] resistors are replaced by memristors in family of Wein bridge oscillators and with oscillation they also achieve the frequency of oscillation.

Some oscillators where memristors are used instead of resistor was presented in [39], all resistors (R_x) are replaced by memristors (R_{m-x}).

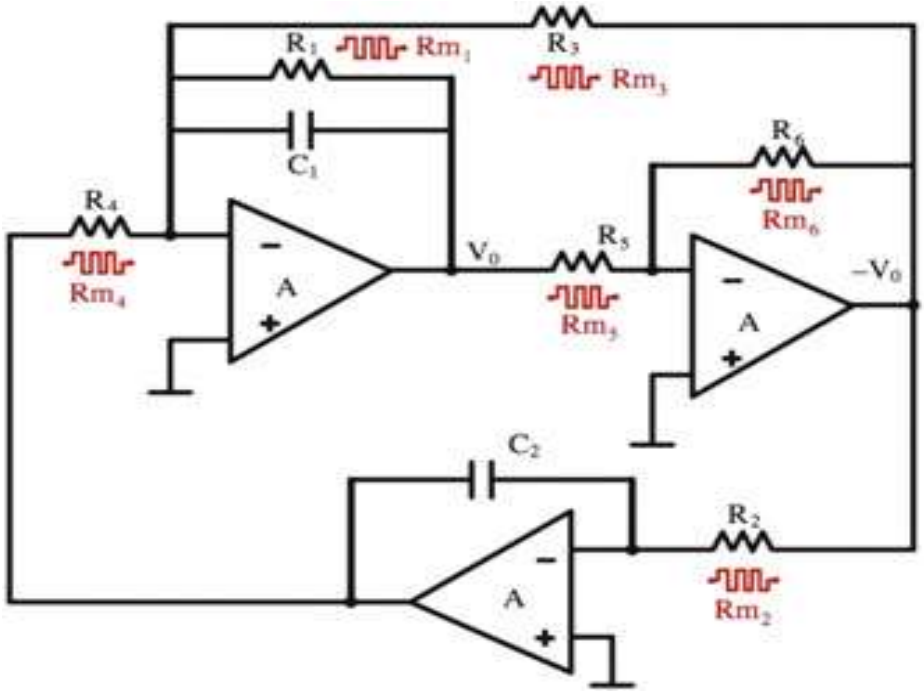


Figure 1.5: Circuit diagram of resistor less oscillator based on memristor [39].

1.7.3 Neuromorphic Circuits

The architectures that mimic the behavior of neurons are mixed analog-digital architectures. To design synapse electronically, major design constraints are dynamic memory and flexibility. Some experiment were done by many researchers where they analyzed small animal brains (like rat, cat) [42-45] and an approach for memristor to be used as synapse was proposed [50, 51].

Pershin et al. proposed memristor emulator where two electronic synapses are connecting three electrponic neurons behaves like a associative memory [47].

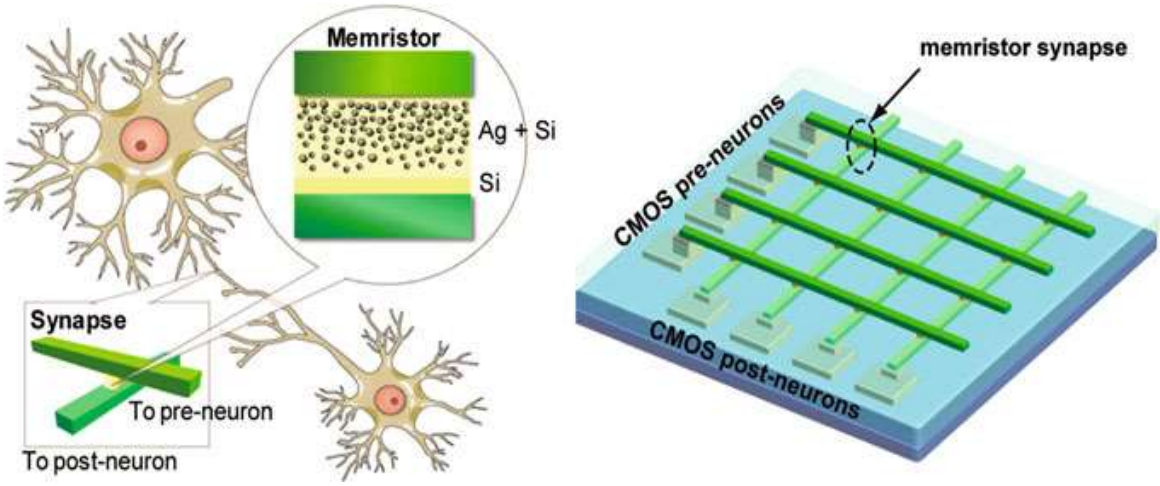


Figure 1.6: Memristormimics synapses in brain [47].

1.7.4 Chaotic System

Because memristor is a non-linear element, it can be very useful for random number generation and encryption, so present a simplicity for chaotic systems. Chua modeled memristor to create a chaotic attractor having negative conductance and a capacitor [48].

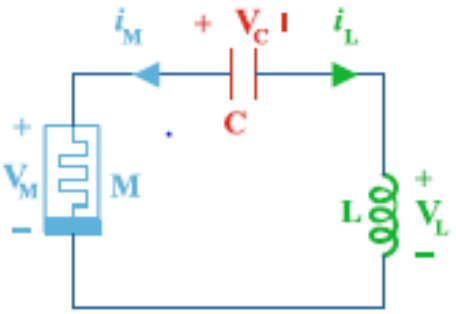


Figure 1.7: Chaotic Oscillator [49].

After that Muthuswamy and Chua validate some facts about Chiotic oscillator [49] where a memristor was used in series with inductor and capacitor as shown in fig. 1.7

Around same time, chaws were generated by memristor practically was proposed by Muthuswami [50, 51].

In [49], memristor was controlled by charge where as in [50], memristor was controlled by flux.

Using HP memristor, a chaotic circuit was presented in [52]. Here two memristors are connected in parallel here in this, an inductor, two capacitors, a negative resistor with two memristors connected anti parallel.

For some security reasons chaotic system are more commonly used, but to fit synchronization between transmitter and receiver is always problematic [53]. A novelty in synchronization between 4 systems was proposed in [54]. In [54], theoretical proofs and numerical simulations validating secure communication using proposed approach was given.

An inductance free chaotic oscillator was proposed in [54], here a flux controlled Memristor, and a RC network and a twin oscillator was used. Here periodic chaotic behavior is observed.

1.7.5 Memristor Based Memories

Memristor can be used in resistive random access memory (RRAM). It consists of two electrodes and a switching material in between these electrodes. Resistivity of this material can be changed by applying external voltage. Resistance switching property of memristor makes it a suitable candidate to be used in memories also it provides high logic density. Before its physical implementation, use of resistive switching in making memories was described in [55-57].

HP labs validates that CMOS was compatible with memristor, faster than CMOS and also can work at low power [33, 58, and 59]. In [58], fabrication of 1×17 cross point array of memristor was done to validate non-volatile feature of memristor in which oxygen vacancies are responsible for switching behavior of resistance.

Application of memristor as non-volatile memory was mathematically reported in [60] so memories can be designed using memristive systems.

SRAM based on memristor was also proposed in [61] to achieve low cell area, low power consumption during store/restore, fast bit to bit operation during store/restore.

1.7.6 Logic Implementation

Usage of Memristor for logic gate implementation is one of the exiting memristor application .A lot of approaches are there to use it but no permanent methodology to design logic gates exists.

Two main logic styles to design logics with memristor are as follows:

1). Logic inside memory, where resistance is considered as logic (Mainly IMPLY Logic) [11].

2). Logic as voltage where Memristor only used for computation purpose (Hybrid CMOS-MEMRISTOR logic). Here both CMOS and memristor are required and voltage decides logic [12].

1.8RESEARCH MOTIVATION

The behavior of memristor to memorize the recent value when we cut off the power supply makes it a suitable candidate to be used for memory applications. It can be also used for implementation of logics. From long ago, all logic operations are performed using CMOS design methodology. In the early stages of research, it was predicted thatall the Boolean operations cannot be performed using memristor, but now we can implement any Boolean operation using memristors. Presently, there is an idea of using memristor in CPU architecture by integrating MOSFET transistors with memristors but in near future there is a possibility that even these transistors can be replaced by combination of memristors, so that the same chip can be used for both memory and computation.

1.9 RESEARCH OBJECTIVES

In this chapter, investigation is done on some important properties of memristor. The properties of memristor and its uses make it a suitable candidate to be used in fast, non volatile devices having large density. Memristor also provides strength to CMOS technology and there is possibility of its commercial availability in near future. In hybrid CMOS, by CMOS-memristor integration, the logic count within same area without scaling CMOS inverters can be increased and hence increase the logic density. The memory based on memristor has crossbar structure similar to IMPLY-GATE, so the same memory cell can be used to store data as well as to perform logic inside same memory, this gives the idea of storage and computation within samesame architecture, thus increase the logic density. However for this, a complex decision making unit is required which can decide that either memristor can be used for computation purpose or for storage, also take the decisions about control voltage signals V_{cond}, V_{set} and V_{resret}.

As the research in the field of memristors is on its early stage, therefore many questions are there regarding design methodology. The main objectives of this thesis are-

- To do the parametric analysis of memristor with the aim to achieve large sized non – linear hysteresis curve having less power dissipation.
- To analyze the feasibility of logic implementation by different memristor based logic families and to analyze the factors effecting logic with memristors.
- To do a comparative study of memristor based logic families with the aim of achieving a better tradeoff between power consumption, speed and area.

1.10THESIS ORGANIZATION

The dissertation is divided into seven chapters where all the aspects of logic implementation with memristors are discussed in detail.

Chapter 1 briefly introduces the topic of this thesis. The detailed theory of memristor with its types and its applications in various fields are discussed.

Chapter 2 contains the brief review of the previously done work on field of memristor. The chapter starts with the origin of the memristors to the advance studies done on memristors. Various research papers and letters related to the topic are discussed. Research motivation and objectives of thesis are presented.

Chapter 3 contains a brief discussion on various physical models of memristor. A detailed parametric analysis of memristor is done with the aim of achieving low power dissipation.

Chapter 4 contains a complete analysis of logic implementation with memristors. Two different approaches to design logic gates with memristor are examined and a brief discussion on design constraints of both types of logic styles is done.

Chapter 5 contains a proposed logic design approach to design AND, OR and NOT gate based on Memristor.

Chapter 6 discusses the results of chapter 4 and chapter 5. A comparative study of Memristor based logic families and outcomes of thesis are also presented.

Chapter 7 contains the conclusion of thesis and according to the obtained results. Future scope of memristor in the field of logic implementation is presented.

CHAPTER

2

LITERATURE SURVEY

2.1 INTRODUCTION

As our semiconductor Industry wants to scale devices more and more and we reached at the saturation level of Moore's law and we cannot do more scaling anymore[1].One of the possible alternate of CMOS design technology can be memristor. Memristor can be used in memory arrays, neuromorphic networks, logic implementation etc.

This chapter describes the work done by many researchers in this field and possibility of use of memristor in developing logics. In section 2.2, we have shown the analysis done by different researchers in the field of memristor.

2.2 LITERATURE REVIEW

Leon O. Chua, 1971 [1], theoretically first defined the two terminals memristor theory by building a scientific relationship between charge ($q(t) = \int_{-\infty}^{t} i(t)dt$) and flux linkage ($\emptyset(t) = \int_{-\infty}^{t} v(t)dt$) by using Maxwell equations and Electromagnetic theories. In this many unique characteristics of memristor are defined which are not achievable using resistor, inductor and capacitor alone and named memristor as forth fundamental passive circuit element.

Leon O. Chua and Sung Mo Kang, 1976[4], presented the scientific theory of memristor and nonlinear system with dynamic nature (memristive systems). In this paper, they presented an important zero crossing Lissajous curve property of memristor called as hysteresis nature of memristor and also the variation of its hysteresis nature with frequency was presented.

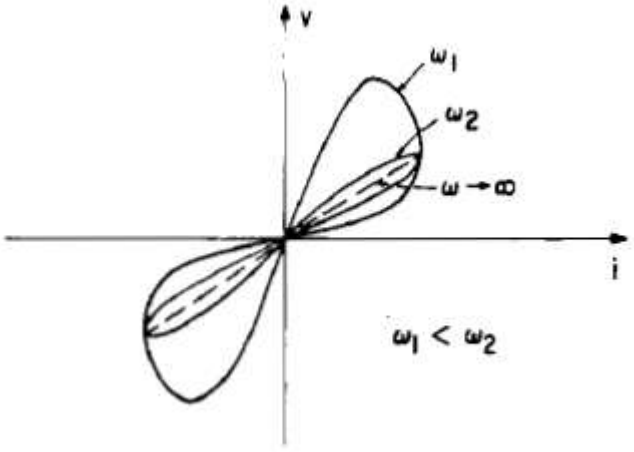


Figure 2.1: Hysteresis behaviour of Memristor [4].

They analyze that at low frequencies, the behavior of memristor is like a non linear resistor with memory effects while at high frequencies they behave simply like a linear resistor.

The dynamical system is described by-

$$V = R(w, i).i \qquad 2.1$$

$$\frac{dw}{dt} = f(w, i) \qquad 2.2$$

Where, W is astate variable and R, f are explicit time functions.

Stanley Williams (H.Plabs),2007[6], [7], proposed his idea to achieve the characteristic of memristor on the basis of nanoscale films, however there is no concept of flux-linkage and charge according to theory of memristor but relates the dependence of resistance on its current history. In 2008, H.P LABS presented the first fabricated memristor which consists of Tio_2 (50 nm) and two electrodes of 5nm, one of titanium and other of platinum. There are two layers of tio_2 one is slightly depleted of oxygen(Tio_{2-x} near platinum electrode).in this device, the charge carriers are oxygen vacancies so resistance of depleted device is much lower than that of non- depleted layer. So resistance of device depends on how much charge passed in particular direction.

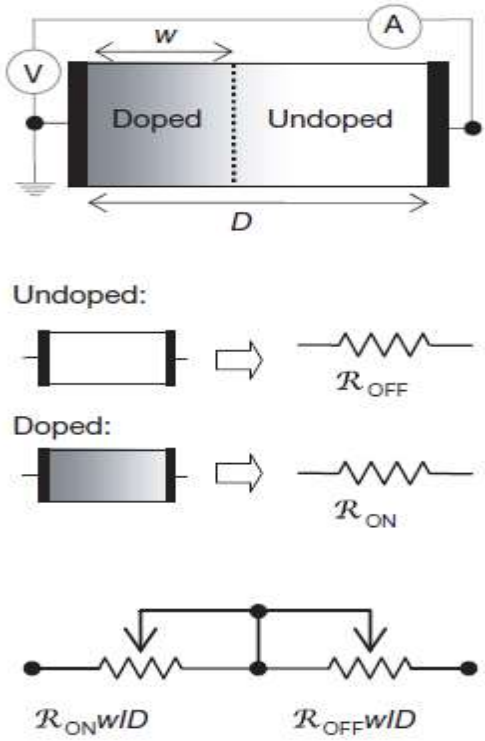


Figure 2.2: Simplified variable resister model of memristor proposed by Stanley Williams [3].

R. S. Williams, G. S. Snider, D. B. Strukov and , D. R. Stewart,2008 [3], presented the first physical model of memristor with W as internal state variable. A sandwiched structure of memristor is presented where a film of semiconductor is sandwiched between the contacts of metal and this sandwiched film has variable concentration of dopants. The high concentration region has low resistance (R_{on}) where as low concentration region has high resistance (R_{off}) and total resistance of device they presented is the series combination of these two variable resistances. Fig. 2.2 shows the Simplified variable resister model of memristor proposed by Stanley Williams

J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, R. S. Williams and D. R. Stewart, April 2010, [10], Proposed their idea of using dynamical memristor for implementing logic functions. They presented their view of using memristor to execute IMP (material implication) and it is the basic two variable Boolean functions.

According to [10], if A & B are two variables then,

A IMP B = ((NOT A) OR B)

An idea of familiarity of memristor switches simultaneously as logic gates(to perform logic) and also as latches (for memory) within same device is proposed, where instead of using voltage or charge, memristance (resistance) can be used as internal state variable.

S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser,2011[9] proposed a design methodology for implementing the combinational logic by using memristor (IMPLY logic-gate),where the logic is defined by resistance. Various design issues of this IMPLY-GATE is considered. They also proposed a model which determines the tradeoff between state drift and write time. Linear ion drift model is not practical to meet characteristics of IMPLY-GATE so necessity of new memristor model which will include the current threshold is proposed.

Shahar Kvatinsky, K. Talisveyberg, D. Fliter, E. G. Friedman, A.Kolodny, and U.C. Weiser, November 2015 [65] compared different models of memristor and represent these models in verilog-A with their relevant window functions that are acceptable for EDA tools like spice.

Shahar Kvatinsky, A. Kolodny, E. G. Friedman, U. C. Weiser, January 2013 [8], Published a paper in which a brief discussion on several models of memristor is done and for digital applications, memory. A non-linear model is presented called TEAM (Threshold adaptive memristor model) model. Two important assumptions that are considered in this model are-

(A). A minimum threshold for change in state variable is considered

(B). Rather than exponential dependency the derivative of internal state variable and current has polynomial dependence.

Analysis of previous memristor models and a comparative study of TEAM model with previous models are done in this paper and how the other models fit into this model is also discussed. A macro model of TEAM model in Spice is presented. According to this paper, TEAM model boost runtime of simulation by 47.5 percent with a mean error of 0.2 percent.

Shahar Kvatinsky, N. Wald, G. Satat, E. G. Friedman, A. Kolodny, and U. C. Weiser, 2014 [11] proposed a design methodology for IMPLY-GATE using memristors, where the logic is in memory (resistance determines logic). They also proposed the design constraints of IMPLY logic family. They observed that the value of $R_g$should be-

$$\text{Ron} < Rg < Roff \quad 2.3$$

$$\frac{vset}{vcond} < \frac{\text{Roff}}{\text{Ron}} \quad 2.4$$

They observed that if we increase the value of R_g, then the state drift problem decreases but write time of the circuit increases so tradeoff is proposed, according to this paper, preferable value of R_g is given by-

$$\text{Rg} = \sqrt{\text{Ron} \,.\, \text{Roff}} \quad 2.5$$

S. Kvatinsky, D. Belousov, S. Liman, G. Satat, N. Wald, E. G. Friedman, A.Kolodny, and U. C. Weiser, September 2014 [66] presented a paper on MAGIC (memristor aided logic). For both input and output a separate memristor is used. MAGIC NOR gate is analyzed having structure similar to crossbar memory based on memristors so can be used in non-von Neumann architectures. The MAGIC logic family contains AND, OR, NOR, NAND and NOT gates. The logic is stored in memory, single voltage is applied which gets divided between memristors according to their logic values which decides about switching of memristor.

S. Kvatinsky, N. Wald, G. Satat, A. Kolodny, , E. G. Friedman and U. C. Weise, August 20 [11] presented the application of memristor using CMOS and proposed MRL (Memristor Ratioed Logic) family, where OR,AND operation are performed by using memristors and together with CMOS inverter they can perform any operation.

The voltage degradation problem is also discussed here also a comparative study of MRL Logic Family with CMOS Technology in term of area, power is done. An optimized 8-bit full adder is presented which can save 50% (approx.) area, power consumption is reduced by 30% with 44% less connections required as compare to CMOS design.

Yang Zhang, Yi Shen, Xiaoping Wang, and Lina Cao, May 2015 [13], proposed a novel design for memristor use in logic gates and propesed the design of AND, OR, NOT gate with less number of operation steps as comparision with IMPLY Logic[12]. Like IMPLY-GATE, the logic is directly stored in memory so can be used in computer's Non-Von Neumann architectures. A novel design of Logic switch using memristor(M.S switch) is proposed, also using this proposed M.S switch, a memory cell having less power dissipation and read time is proposed.

Mehri Teimoori, Arash Ahmadi, Shahpor Aliresaee, Majid Ahmadi [14], May 2016 proposed the whole hybrid CMOS-Memristor logic family by using the combination of 1

CMOS inverter and 4 Memristor structure. By using this design structure the output of OR, AND, XOR gate is obtained at the same instant which can be used to implement complex circuits where area and power dissipation are the major design constraints. They proposed 1-bit full adder using this design structure which requires 4 mosfet transistos and 10 memristors instead of 8 mosfet transistors and 18 memristors presented in [12].

Qiao Chen, Xiaoping Wang, Haibo Wan, and Ran Yang, February 2017 [67] analyzed the IMPLY logic gate. They observed that IMPLY logic suffers from a limitation that in material implication the memristor was not able to reach the lowest value. They presented a circuit structure that can overcome the limitations of IMPLY logic. They simulated their proposed design and verify its correctness.

CHAPTER

3 MEMRISTOR MODELS AND PARAMETRIC ANALYSIS

3.1 INTRODUCTION

Since the research in the field of memristors is on its early stage, therefore there is a need of a simple mathematical model that can implement the logics and sufficiently describe its functionality and behavior. At the same time, it should be sufficiently accurate compared to that of a physical memristor. In section 3.2, some mathematical models are briefly discussed. Since memristor can be highly useful in many applications, therefore the I-V characteristics become very important. In section 3.3, parametric analysis of memristor is done aiming to have large sized non –linear hysteresis curve having less power dissipation.

3.2 PHYSICAL MODELING

This section presents a brief analysis of some popular models.

3.2.1 Linear Ion Drift Memristor Model

In 2008, R. S. Williams, G. S. Snider, D. B. Strukov and D. R. Stewart [3], presented the first physical model of memristor on successful fabrication of device with 'W' as internal state variable. Use of only one state variable in its mathematical implementation gives simplicity to this model. A sandwiched structure of memristor is presented where a film of semiconductor is sandwiched between the contacts of metal and this sandwiched film has variable concentration of dopants. The region with high concentration dopants has low resistance (R_{on}), whereas the region with low concentration dopants has high resistance (R_{off}) and the total resistance of the device is series combination of these two variable resistances. At very high electric field, vacancies can move freely throughout device which is responsible for change in conduction which changes memristance accordingly. But this theory has a problem, because at the boundary, the charged ions slow down and are unable to reach to the boundary. If the charge carriers reach to the boundary then no physical charged ions exists in device and W becomes zero which is not possible. Also doped region cannot cover the entire device, happening of which makes D=W (width of entire device= width of doped region) and undoped region get diminished so therefore a window function is needed with derivative of state variable.

Mathematical description of Memristor is given as-

$$V(t) = M(q).I(t) \quad 3.1$$

$$M(q) = \left(\text{Ron}.\frac{\text{W(t)}}{\text{D}} + \text{Roff}.\left(1 - \frac{\text{W(t)}}{\text{D}}\right)\right) \quad 3.2$$

$$W(t) = \left(\mu.\frac{\text{Ron}}{\text{D}}.\text{q(t)}\right) \quad 3.3$$

$$\frac{dw(t)}{dt} = \left(\mu.\frac{\text{Ron}}{\text{D}}.\text{I(t)}\right) \quad 3.4$$

Where D represents device thickness, W (t) represents State variable (equal to length of oxygen deficient Tio_{2-x}), M (q) represents memristance, V (t) represents voltage across memristor, I(t) represents current across memristor, μ represents ion-mobility.

This model is simple, easy computable and easy understandable however reduction in non-linearity is disadvantage of this model.

3.2.2 Non-Linear Ion Drift Memristor Model

Linear ion drift memristor model define the hysteresis behavior of memristor but electrodynamics imposed few limitations to this model. By some experimental results and research it was proved that the fabricated memristor is non-linear in nature so linear ion drift model does not meet the sufficient accuracy. So we move towards non-linear memristor model [16], here state derivatives & voltage are related non-linearly as-

$$I(t) = W^n(t).\beta \sinh\big(\alpha V(t)\big) + \chi\big[exp\big(\gamma V(t)\big) - 1\big] \quad 3.5$$

$$\frac{dW(t)}{dt} = \alpha V^m(t).f(t) \quad 3.6$$

Where,$\alpha, \beta, m, \chi, n$ are fitting parameters,V(t)represents voltage across memristor, I(t) represents current through memristor, and W is a state variable can take any value in interval of [0,1].This model is of asymmetric type, in OFF state, the exponential part becomes dominant one and thus I-V characteristics look same as P-N junction type. In ON state, the sinh part becomes dominant and thus we have tunneling process type I-V characteristics.

This model defines the practical memristor in more reasonable way and also provides the benefits of fast writing and stability in reading. This model is voltage sensitive, thus for a read a low voltage is used so switching time increases and thus stability in reading is achieved. For write, a high voltage is used so we can write in small interval of time.

3.2.3 Simmons Tunneling Barrier Memristor Model

Above discussed models are inaccurate as they cannot sufficiently define the HP fabricated memristor so new model was proposed [33].Above explained models modeled memristor as a device having 2 different resistors (one for doped (R_{on}) & other for undoped region (R_{off})) connected in series fashion, in this model a electron tunnel barrier is considered in series with a resistor. Dependency of movement of ions was considered exponential in nature so make it to behave like a non-linear memristor having asymmetric switching.

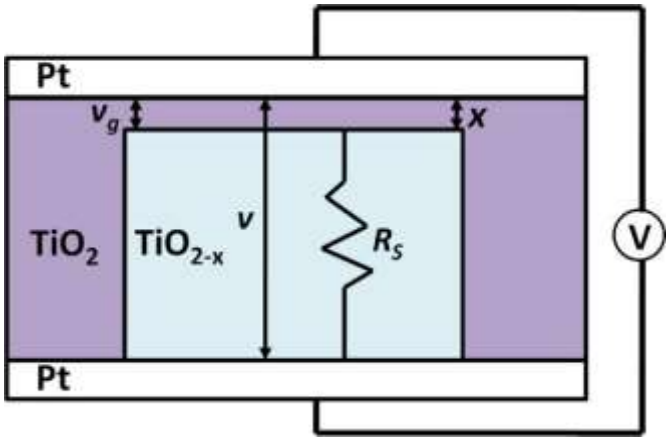


Figure 3.1: Simmons tunnel barrier Memristor physical model [33].

In Fig.3.1, oxide region width is state variable (x) and on application of voltage (V), v_g gets developed over undoped region and v represents the internal voltage of device.

By using [34], the voltage-current relationship was given as-

$$\frac{dx(t)}{dt} = f_{off}.sinh\left(\frac{i}{i_{off}}\right).e^{-e^{\left(\frac{w-\alpha_{off}}{w_c}-\frac{|i|}{b}\right)}} - \frac{x}{w_c}(OFFswitching, i > 0) \quad 3.7$$

$$\frac{dx(t)}{dt} = f_{on}.sinh\left(\frac{i}{i_{on}}\right).e^{-e^{\left(\frac{w-\alpha_{off}}{w_c}-\frac{|i|}{b}\right)}} - \frac{x}{w_c}(ONswitching, i < 0) \quad 3.8$$

Where,$f_{off}, \alpha_{off}, f_{on}, \alpha_{on}$ are fitting parameters and i_{on}, i_{off} are device threshold currents.

$\alpha_{on}, \alpha_{off}$ Impose a bound on state variable [x] and always $|f_{on}| \gg |f_{off}|$.

Disadvantages-

1).complicated model, it defines only specific device so is not generic in nature.

2). No explicit relationship between V(t) and I(t).

3.2.4 TEAM (Threshold Adaptive Memristor Model)

In 2013, S. Kvatinsky et al. presented a model for memristor [8], this model is generic as well as simple and also it can fit to all the models of memristor mentioned above with some small negligible error pursuit.

Here two important assumptions are made-

1). A threshold is defined, below which the change in state variable is inexperienced.

2).The current and state variable is related polynomially instead of exponential relationship presented in above models.

In [8], the voltage-current relationship was given as-

$$V(t) = \left[R_{on} + \frac{R_{off} - R_{on}}{x_{off} - x_{on}} . (x - x_{on})\right] I(t)$$

OR

$$V(t) = \left[R_{on} . exp\left(\frac{\lambda}{x_{off} - x_{on}} . (x - x_{on})\right)\right] I(t) \qquad 3.9$$

Where $\lambda = ln\left(\frac{R_{off}}{R_{on}}\right)$

Here two I-V relationships were given in [8], in first one state variable [x] and memristance are linearly related (define the first two models) where as in second I-V relationship, the state variable [x] and memristance are exponentially related (define Simmons tunneling barrier Memristor model).

The derivative of state variable is given as-

$$\frac{dx}{dt} = \begin{cases} \left(k_{off}\left(\frac{I(t)}{I_{off}} - 1\right)^{\propto_{off}} . f(x)\right) & 0 < I_{off} < I \\ \left(k_{on}\left(\frac{I(t)}{I_{on}} - 1\right)^{\propto_{on}} . f(x)\right) & 0 < I_{on} < I \\ 0 & otherwise \end{cases} \qquad 3.10$$

Where k_{off}, k_{on} defines the state change.

$\propto_{off}, \propto_{on}$ defines the linearity.

I_{off}, I_{on} defines minimum current threshold.

R_{on}, λ defines the edge resistances and x_{off}, x_{on} are fitting parameters.

In [8], on average the mean error found in case of TEAM memristor model is 0.2% and increase the runtime of simulation by 47.5%.

3.3 PARAMETRIC ANALYSIS OF MEMRISTOR

In chapter 1 and 2, we have discussed about the applications of memristor in memories, in performing logics. Also hysteresis behavior of memristor is analyzed. To design memories, the major design constraints are Power Consumption, Large size, Lower chip design, and lower retention time.

So to use memristor in memories, it should produce a non-linear hysteresis loop. Power consumption in memories depends on size of hysteresis loop (as loop size increases then power dissipation also increases). In this section, we are doing the parametric analysis of memristor using "Linear ion drift model". We used the CADENCE VIRTUOSO TOOL to obtain large non- linear memristor hysteresis loop and several parameters that affect this loop are analyzed here.

3.3.1 Hysteresis Behavior of Memristor

For this linear ion drift model is used and this model is simulated in Cadence Virtuoso tool. The parameters used are-

$\mu v = 1e-14 m^2 v^{-1} s^{-1}, D = 10nm, \text{Ron} = 100\ \Omega, \text{Roff} = 200000\ \Omega, \qquad \text{dt} = 0.5\text{e}-03$

Sinusoidal voltage source (V_{sin}) of 0.5 Hz frequency and $\pm 2V$ amplitude is applied across memristor.

Fig. 3.2(a) shows the schematic of memristor used for analysis in cadence virtuoso while corresponding I-V characteristics of memristor is shown in Fig .3.2(b).

The large size non-linear hysteresis loop obtained is the evident of memristor switching character. Initially it starts with high resistance and as the amplitude of V_{sin}increases, the current (I_{sin}) across memristor also slowly increases and thus resistance drops because of charge flow in memristor. With the increase in V_{sin}, I_{sin} increases rapidly until V_{sin} reaches its maximum value, then as V_{sin} decreases, I_{sin} slowly decreases but still there is a charge flow in device so resistance continues to drop and this give us on-switching loop. When V_{sin} becomes negative, then we experience an increase in device resistance which is responsible for off switching loop.

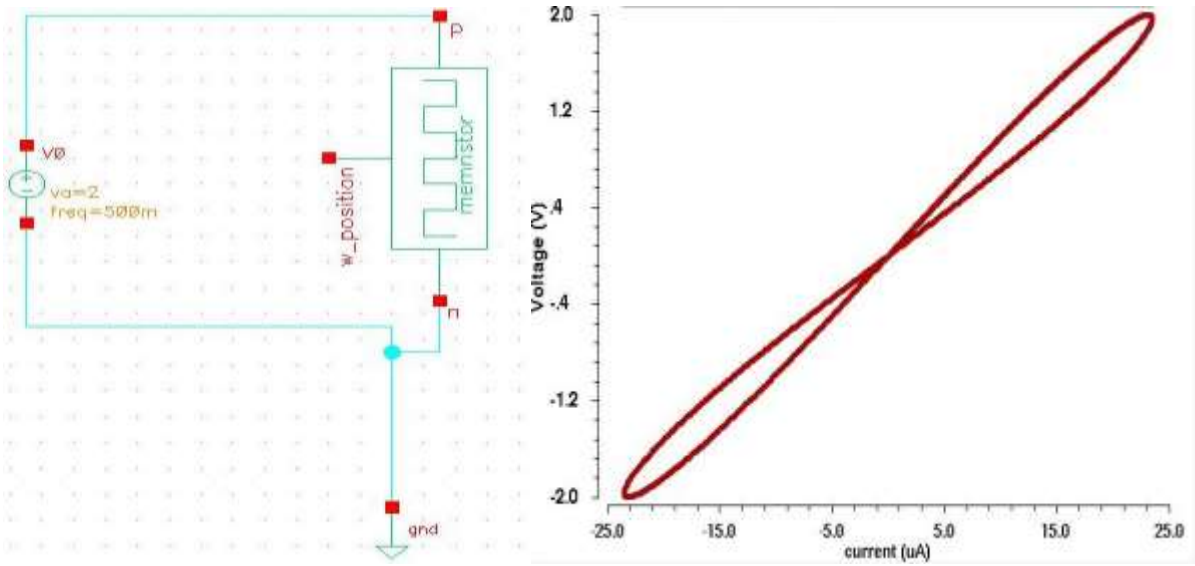
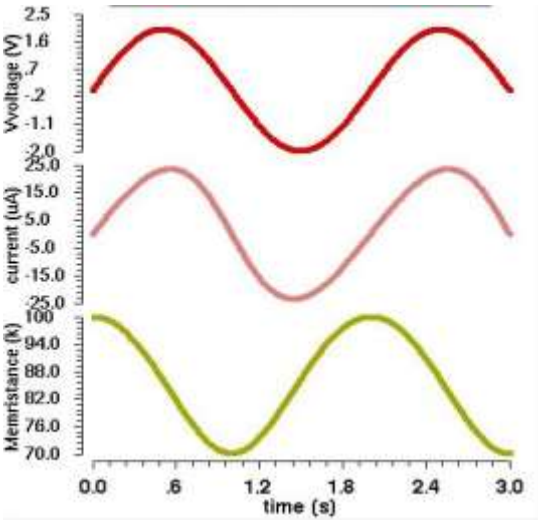


Figure 3.2(a)Figure 3.2(b)

Sinusoidal voltage source (V_{sin}) of 0.5 Hz frequency and $\pm 2V$ amplitude is applied across Memristor.

3.3.2 Variation in Frequency

For a fixed V_{sin} of $\pm 2V$ amplitude, device thickness of D=10nm and ion mobility of $1e-14m^2v^{-1}s^{-1}$, we simulate memristor for different frequencies presented in table 3.1.



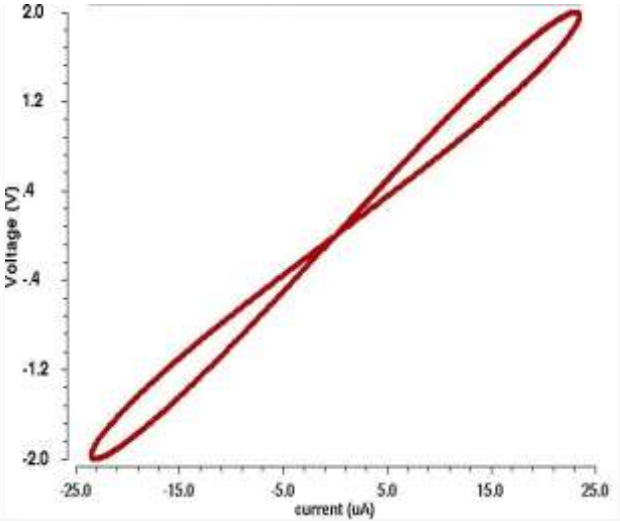


Figure 3.3(a) **Figure 3.3(b)**

Fig. 3.3(a) is showing the variation in voltage, current and memristance at frequency of 0.5 Hz and corresponding I-V characteristics of memristor is shown in Fig .3.2(b).

TABLE 3.1 -The non-linear variations in current, memristance and Drift velocity of memristor for a fixed V_{sin} of $\pm 2V$ amplitude, device thickness of D=10nm and ion mobility of $1e-14m^2v^{-1}s^{-1}$ and variable frequency.

Frequency (Hz)	Voltage (V)	Current (μm)	Drift Velocity (nm/s)	Memristance (KΩ)
Initial value	**0**	**0**	**0**	**100**
0.5	**2**	**23.5008**	**2.35**	**85.065**
1	**2**	**21.45**	**2.14**	**93.15**
3	**2**	**20.43**	**2.043**	**97.85**
5	**2**	**20.20**	**2.020**	**98.5**

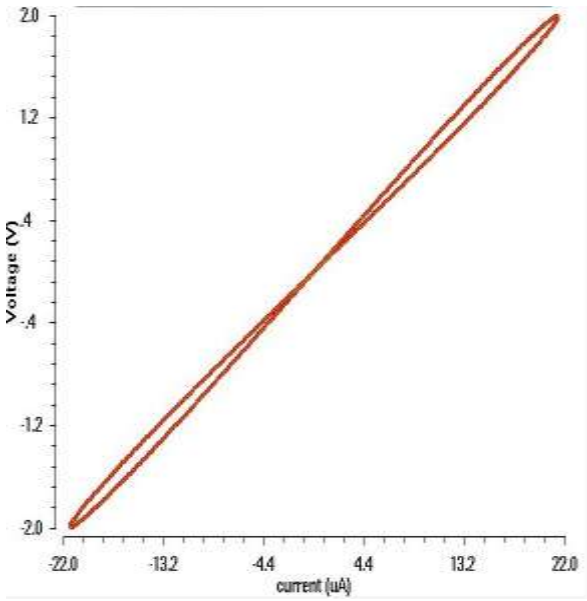


Figure 3.3(c)

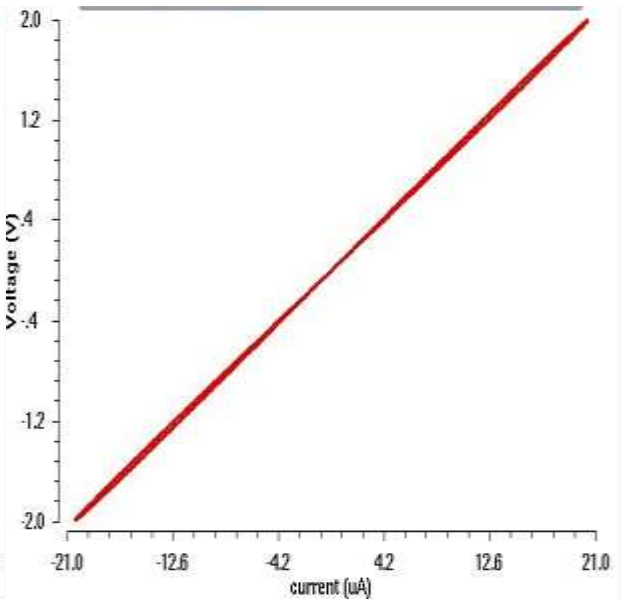


Figure 3.3(d)

Fig. 3.3(c), Fig. 3.3(d), Fig. 3.3(e) showing the I-V characteristics for frequency of 1 Hz, 3 Hz and 5 Hz respectively.

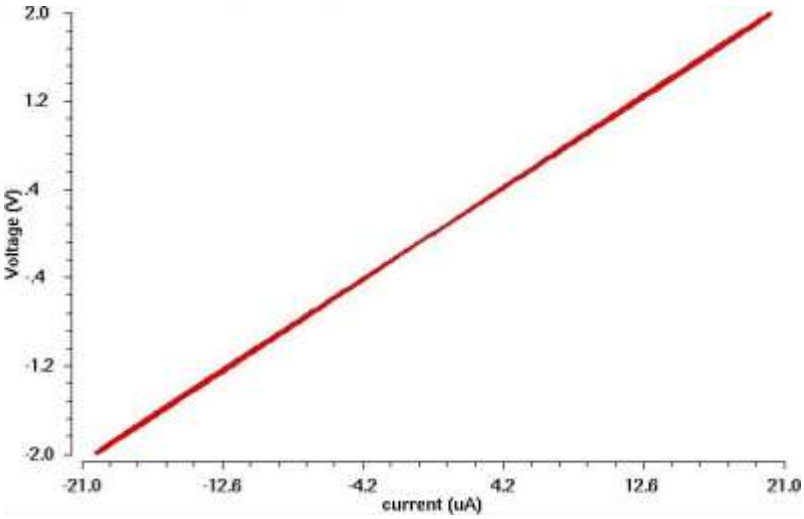


Figure 3.3(e)

From Fig. 3.3(a), 3.3(b), 3.3(c) it can be concluded that as the frequency increases, we experience a decrease in drift velocity and thus increase in memristance i.e. doping region width decreases and thus non-linear I-V curve changes to linear one with increase in frequency. Now with the decrease in frequency, the non-linearity increases but that too also for a limited range of frequency.

3.3.3 Variation in Amplitude of V_{sin}

For a fixed V_{sin} of 0.5 Hz frequency, device thickness of D=10nm and ion mobility of $1e-14m^2v^{-1}s^{-1}$, we simulate memristor for different amplitudes of V_{sin} presented in table 3.2

Fig. 3.4(a) is showing the variation in voltage, current and memristance by supplying external voltage of 1volt and Fig. 3.4(b) is showing the corresponding I-V characteristics of memristor.

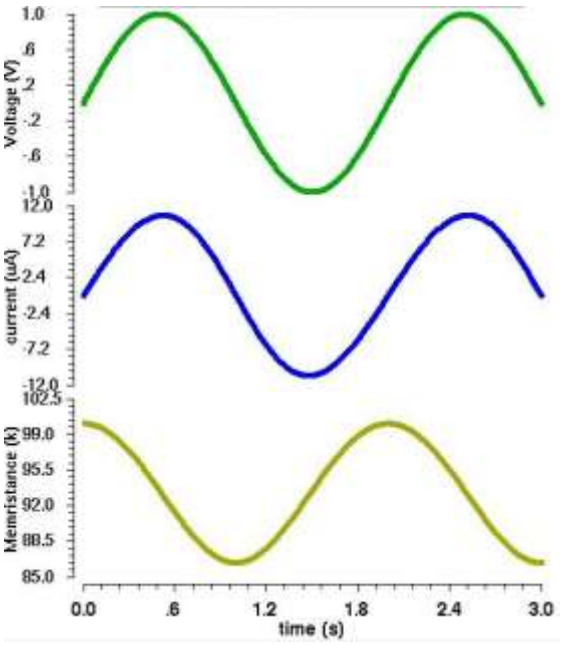


Figure 3.4(a)

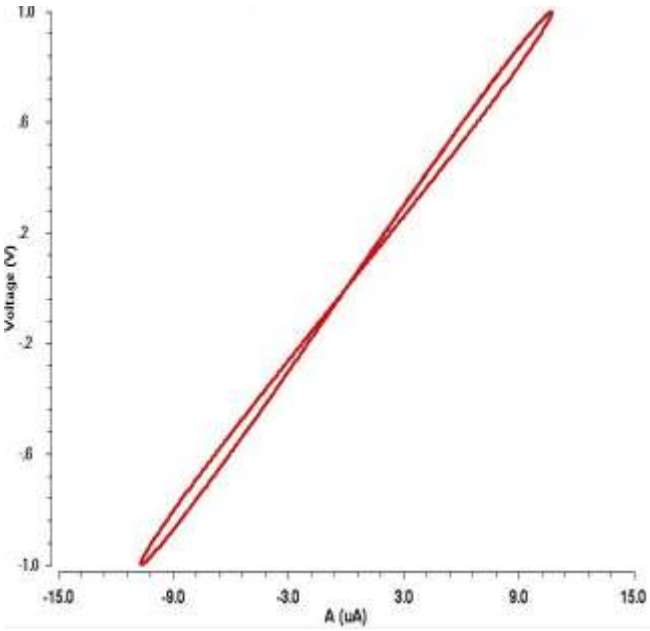
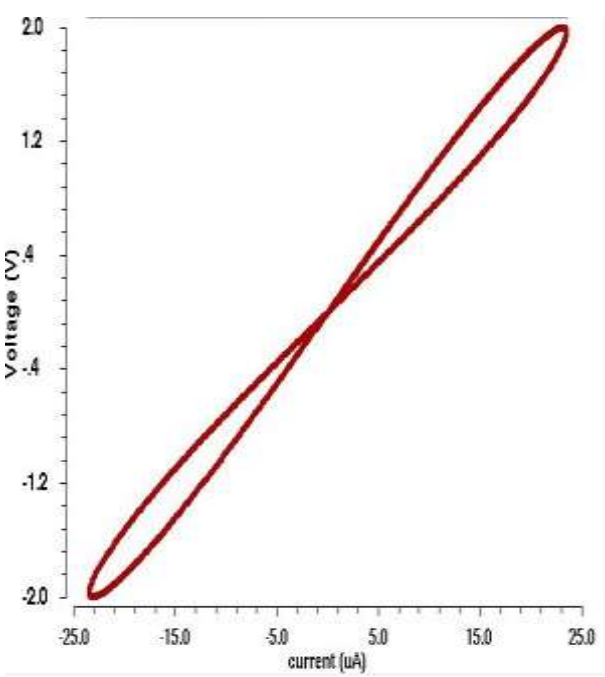


Figure 3.4(b)

TABLE 3.2- The non-linear variations in current, memristance and Drift velocity of memristor for a fixed V_{sin} of 0.5 Hz frequency, device thickness of D=10nm and ion mobility of $1e-14m^2v^{-1}s^{-1}$ and variable voltage.

Voltage (V)	Frequency (Hz)	Memristance (KΩ)	Drift Velocity(nm/s)	Current (μA)
Initial value	**0**	**100**	**0**	**0**
1	**0.5**	**93.2**	**1.0727**	**10.727**
2	**0.5**	**85.065**	**2.35008**	**23.5008**
3	**0.5**	**74.35**	**4.032**	**40.32**



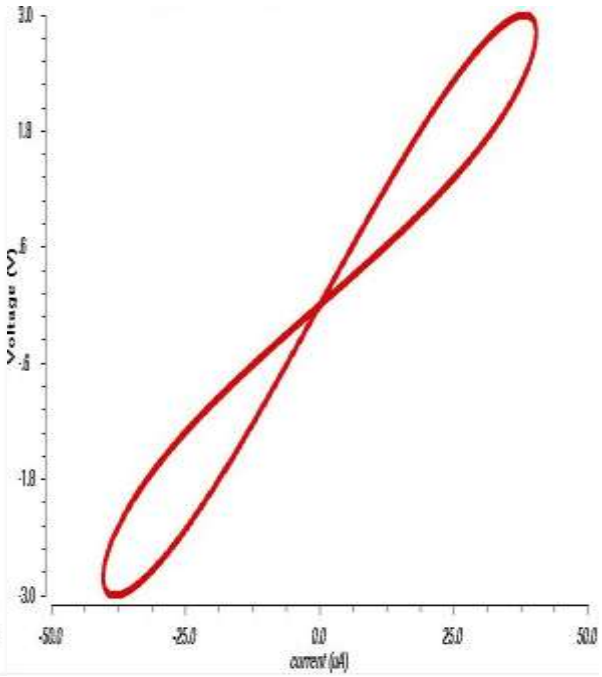


Figure 3.4(c) **Figure 3.4(d)**

Fig. 3.4(c) and 3.4(d) are showing the I-V characteristics for voltage of 2V and 3V respectively.

From Fig. 3.4(a), Fig. 3.4(b), Fig. 3.4(d) it can be concluded that as the amplitude of V_{sin} increases, the current drift velocity increases, current increases and thus a increase in size of non-linear hysteresis loop is seen resulting in decrease in memristance and vice versa.

3.3.4 Variation in thickness of Memristor:

For a fixed V_{sin} of $\pm 2V$ amplitude, ion mobility of $1e-14 m^2 v^{-1} s^{-1}$, frequency of 0.5 Hz , we simulate memristor for different thicknesses which are presented in Table 3.3.

TABLE 3.3- The non-linear variations in current, memristance and Drift velocity of memristor for a fixed V_{sin} of $\pm 2V$ amplitude, ion mobility of $1e-14 m^2 v^{-1} s^{-1}$, frequency of 0.5 Hz and variable thickness.

Thickness(D)	Current(μA)	Drift Velocity(pm/s)	Memristance (KΩ)
10nm	**23.5008**	**1.9989**	**85.065**
10μm	**19.989**	**2350**	**100**

Fig. 3.5(a) is showing the I-V characteristics for a thickness of 10nm and Fig. 3.5(b) showing the I-V characteristics for a thickness of 10μm.From Fig. 3.5(a), Fig. 3.5(b) it can be

concluded that as the thickness of memristor increase from nanometer range to micrometer range, a change in hysteresis curve from non-linear to a linear one is seen because in micrometer range, the current and drift velocity are diminished by a large factor and memristance of memristor remains unchanged.

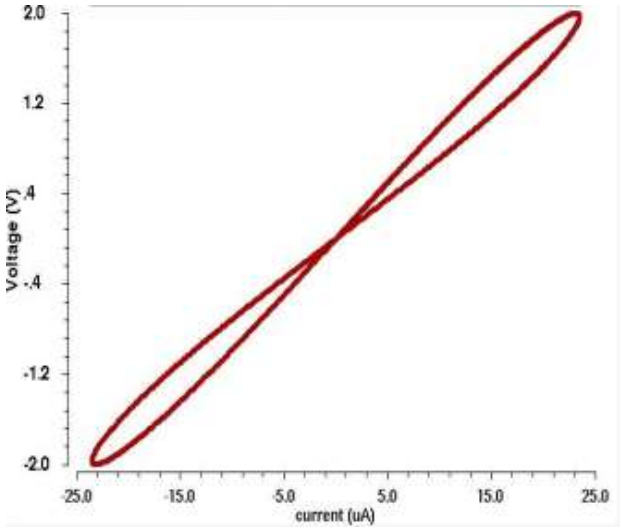


Figure 3.5(a)

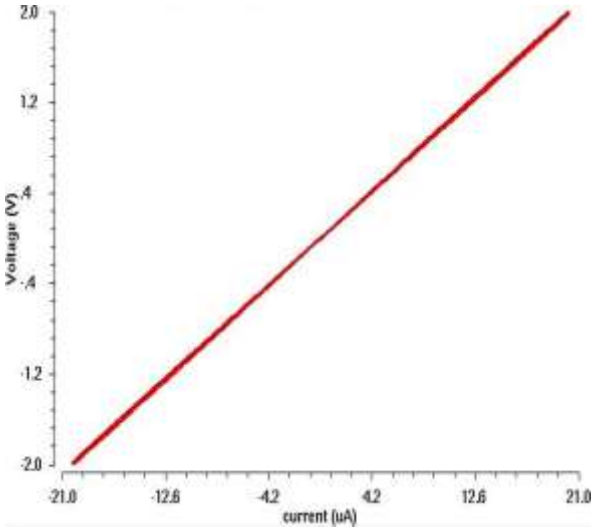


Figure 3.5(b)

3.3.5 Variation in mobility:

For a fixed V_{sin} of $\pm 2V$ amplitude, device thickness of D=10nm and frequency of 0.5 Hz, we simulate memristor for different ion mobility which are presented in table 3.4.

TABLE 3.4- The non-linear variations in current, memristance and drift velocity of memristor for a fixed V_{sin} of $\pm 2V$, thickness of 10nm, frequency of 0.5 Hz and variable mobility.

Mobility (m^2/v-s)	Memristance (KΩ)	Drift Velocity (nm/s)	Current (μA)
Initial value	**100**	**0**	**0**
1e-14	**85.065**	**2.35008**	**23.5008**
1e-15	**98.7**	**2.025**	**20.25**
1e-16	**100**	**2.0015**	**20.015**

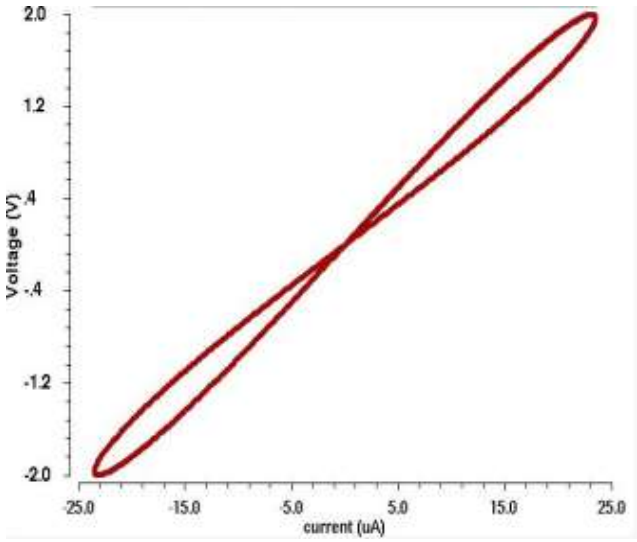


Figure 3.6(a)

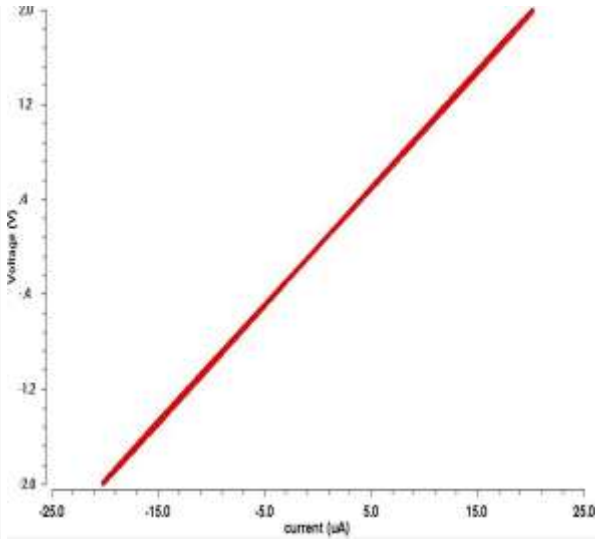


Figure 3.6(b)

Fig. 3.6(a) is showing the I-V characteristics of memristor for ion mobility of 1e-14 m^2/v-s and Fig. 3.6(b) is showing the I-V characteristics of memristor for ion mobility of 1e-14 m^2/v-s

From fig. 3.6(a) and Fig. 3.6(b) it can be concluded that when the ions mobility increases, the ions reach to the boundary early, so drift velocity gets diminished to zero early when doped region width reaches to its upper limit early and memristance falls to its minimum value. Similarly drift velocity diminished to zero early when doped region width reached to its lower limit and memristance reaches to its maximum value so current increases rapidly and a linear curve is obtained instead of non-linear loop.

3.4 CONCLUSION

I-V characteristics are very important for memristor to be used for a particular desired application. Different I-V curves can be achieved by varying different parameters of memristor for different applications such as for logic implementation. For memory applications a large size hysteresis loop is needed which can be achieved at nanometer thickness range, also the same curve can be achieved at higher amplitude of V_{sin} having low frequency. However, large thickness (micrometer range) of memristor produces linear I-V curve hence can be used as load resistor or in operational amplifiers as a feedback resistor having high resolution but the same curve can be achievable at low amplitude of V_{sin} having high frequency.

For memristor to be used in memory applications, memristor should consume less power also produce the large sized non –linear hysteresis loop. But complexity is more in achieving both

at the same instant because if we increase the amplitude of V_{sin} then memristor will produce the large sized hysteresis loop but consume more power. Hence, a detailed parametric analysis using Linear ion drift model was done with aim to increase area of loop with less power dissipation and reached to an observation that to achieve the required memristor, it should be used at lower amplitudes of V_{sin} having low frequencies.

CHAPTER

4

LOGIC IMPLEMENTATION USING MEMRISTORS

4.1 INTRODUCTION

Usage of memristor for logic gate implementation is one of the exiting memristor application .A lot of approaches are there to use it but no permanent methodology to design logic gates exists. Two main logic styles to design logics with memristor are as follows-

1). Logic inside memory, where resistance is considered as logic (Mainly IMPLY Logic) in [9].

2). Logic as voltage where memristor only used for computation purpose (Hybrid CMOS-MEMRISTOR logic). Here both CMOS and memristor is required and voltage decides logic.

In this chapter we analyzed the memristor behavior to be used as logic gate and also discussed some design constraints for both type of logic styles.

4.2 IMPLYLOGIC

4.2.1 IMPLY Logic Analysis

In [39], a brief discussion on IMPLY logic gate based on memristor was done. All two variable operations can be realized by using IMPLY logic gate. In [39], Borghetti described how a Memristor can be used to describe material implication and then by using material implication he describe how all two variable fundamental Boolean function can be realized.

Here in Fig.4.1, the load resistance 'R_g' is connected between two memristors P and Q using a horizontally connected nanowire and ground. Logic values of two memristors Q and P represent the states of Q and P respectively. Logic '1' or '0' is assigned to each of these memristors Q or P by tri-state drivers. Here resistance of memristors P and Q are considered as logic values of P and Q respectively, where high resistance (R_{off}) is considered as logic '0' and low resistance (R_{on}) is considered as logic '1'.

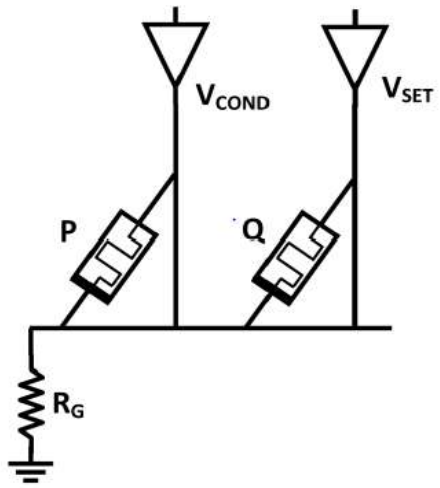


Figure 4.1: IMPLY logic gate implementation [12].

Fig. 4.1 shows the implementation of IMPLY logic gate .The inputs are given to the memristor P and Q, and final state of memristor Q is considered as output (when input value of Q gets diminished).

Table 4.1 Truth table of IMPLY logic gates

Case number	**R_P**	**R_Q**	**P**	**Q**	**Q'=$P \rightarrow Q$=((NOT P) OR Q)**	**Final R_Q**
Case-1	**R_{off}**	**R_{off}**	**0**	**0**	**1**	**R_{on}**
Case-2	**R_{off}**	**R_{on}**	**0**	**1**	**1**	**R_{on}**
Case-3	**R_{on}**	**R_{off}**	**1**	**0**	**0**	**R_{off}**
Case-4	**R_{on}**	**R_{on}**	**1**	**1**	**1**	**R_{on}**

The load resistor 'R_g' is chosen as-

$$R_{on} < R_g < R_{off}$$

Voltage V_{set} is applied to memristor Q and $V_{cond}$is applied to memristor P and holds relation-

$$|V_{set}| > |V_{cond}|$$

Since for all practical purposes always we consider a minimum current threshold, so here also in memristor case a critical voltage 'V_c' is considered. V_c is the minimum voltage beyond

which only we can experience any change in memristance of Q and P. So required design conditions are-

$$|V_{set}| > |V_c| > |V_{cond}|$$

$$(|V_{set}| - |V_{cond}|) < |V_c|$$

4.2.2 IMPLY Logic Gate Operation

In Fig. 4.1, the current can flow only in top to bottom direction (because of polarity of V_{cond} and V_{set}) increase in memristance of Q and P is experienced. Thus if at the beginning of logic evaluation the memristance of Q is high (logic '0'), then the final value of Q will always remains same.

Case 1- When P='0' and Q='0', since both P and Q have initially high resistances so when we applied V_{cond} and V_{set} to P and Q respectively then because $R_{off} \gg R_g$ so we have approximately zero voltage at the central node and thus most of the drop falls on P and Q only and this results into switching of Q to logic '1'.

Case 2- When P='0' and Q='1', then Q maintains its logic state.

Case 3- When P='1' and Q='0', we have approximately V_{cond} at the central node and thus V_{cond}- V_{set} falls on Q which is not sufficient to switch the logic state of Q. However a change in state of Q is observed since state of Q is drifting from '0' to '1' this is called as state drift and it decide the robustness of circuit.

Case 4- When P='1' and Q='1', then Q maintains its logic state.

Case 1 determines the time needed for operation while case 3 determines the robustness of IMPLY logic gate.

4.2.3 Simulation results

Since in [9], it was proved that the linear model does not give the expected results for IMPLY logic family so the TEAM model is used here and the parameters used here are-

$$\mu v = 1e-14 m^2 v^{-1} s^{-1}, D = 3nm, \text{Ron} = 1\text{k}\,\Omega, \text{Roff} = 100\text{k}\,\Omega, i_{off} = -i_{on} = 100\text{fA},$$

$$\text{k}_{\text{off}} = -\text{k}_{\text{on}} = 0.00000005, \text{dt} = 1\text{e}-12$$

In Fig. 4.2, right memristor is Q left memristor is P. There is also one extra output in each memristor (w-position) which is not used. Resistor used to connect nodes, R=0 is taken because resistance is not needed only used to assure connection at different nodes.

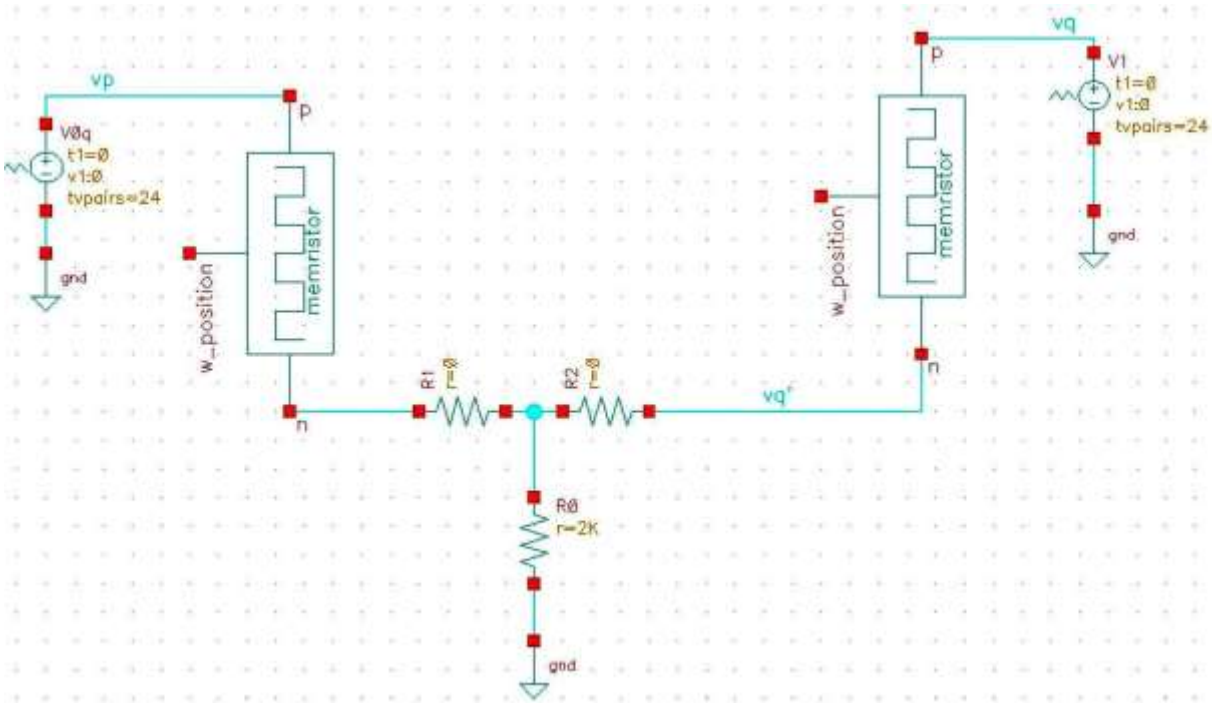


Figure 4.2: Schematic of IMPLY-GATE in virtuoso.

Fig. 4.2 shows the schematic of IMPLY basic gate generated in cadence virtuoso. V_{pwl} of virtuoso is used to generate voltages V_p and V_Q for memristors P and Q respectively and load resistor R_g is chosen as 2kΩ.

For analysis of IMPLY gate, we define some useful parameters-

T_{reset} – Time taken by memristor to come to reset (i.e. 100kΩ) with respect to V_p or V_Q (i.e. time difference between 50% V_p or V_Q and 50% of Memristance of Q (49.5kΩ)).

T_{fall} – For case –first, it is defined as time taken by memristor Q to come to 49.5KΩ from 100kΩ.

Table 4.2-The sequence of voltages that cover all input possibilities for simulation of IMPLY logic gate.

Case number	Time [ns]	V_p	V_Q
-	0-1	0	0
-	1 – 3	V_{reset}	V_{reset}
First	3 – 5	V_{cond}	V_{set}
-	5 – 7	V_{reset}	0
-	7 – 9	0	V_{set}
Second	9 – 11	V_{cond}	V_{set}
-	11 - 13	V_{set}	0
-	13 - 15	0	V_{reset}
Third	15.- 17	V_{cond}	V_{set}
-	17 - 19	V_{set}	0
-	19 - 21	0	V_{set}
Fourth	21 - 23	V_{cond}	V_{set}

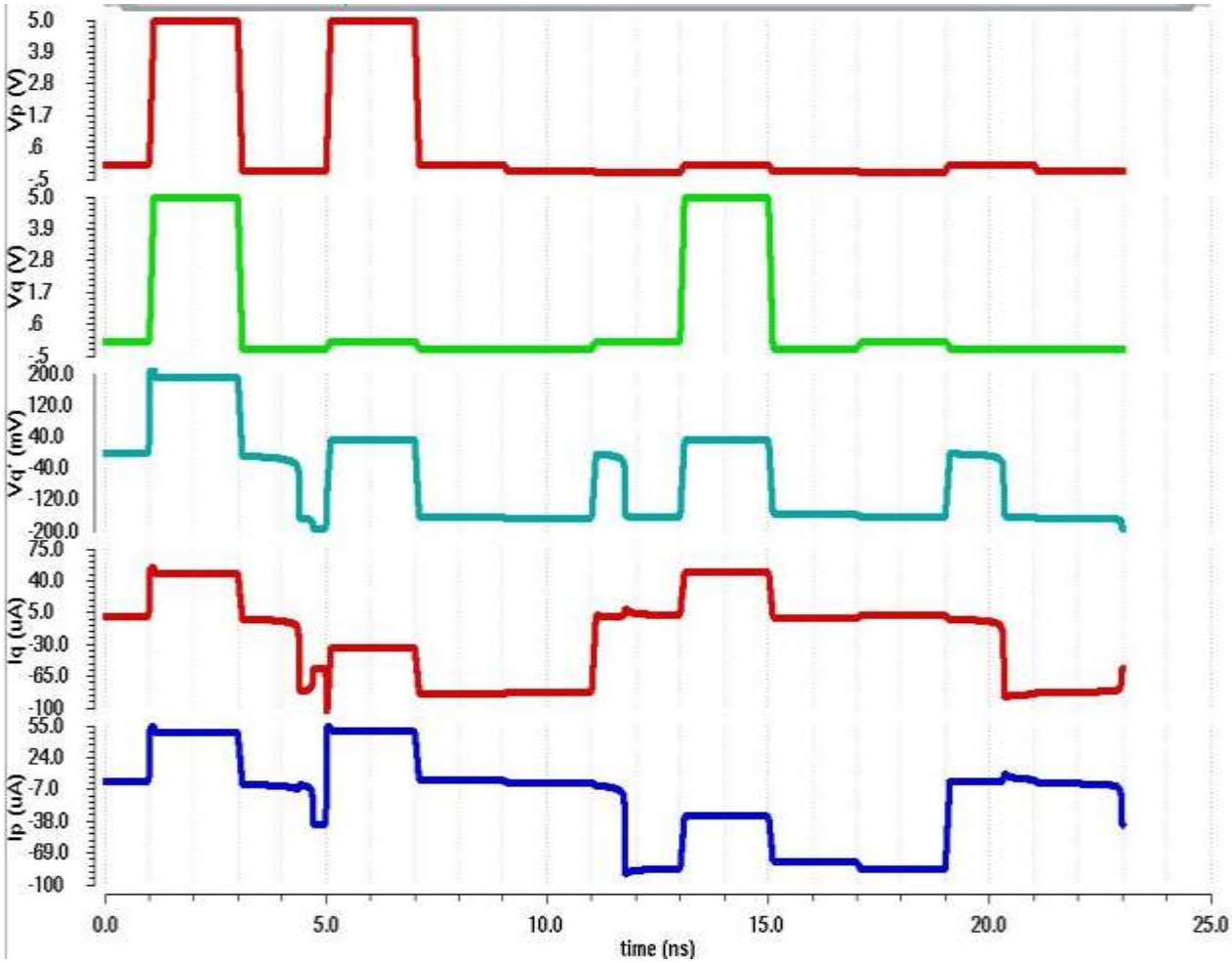


Figure 4.3: Voltages and current variation of IMPLY gate for α=1 without threshold (i_{off} =100fA).

For all the cases voltage needed to reset (V_{reset}) is taken as 5v and rise and fall time for all voltages is taken as 0.1 ns.

For α=1 (linear HP memristor), and parameters defined above for TEAM model IMPLY gate is simulated for V_{cond} = -0.235v, V_{set} = -0.250V. V_{cond}, V_{set} , V_{reset} are chosen according to [9], we have done some adjustments to get full swing.

Fig. 4.4 (a) shows the Variation in memristance of memristor P for load resistance R_g=2kΩ and α=1 without threshold and Fig. 4.4 (b) shows the Variation in memristance of memristor Q for load resistance R_g=2kΩ and α=1 without threshold.

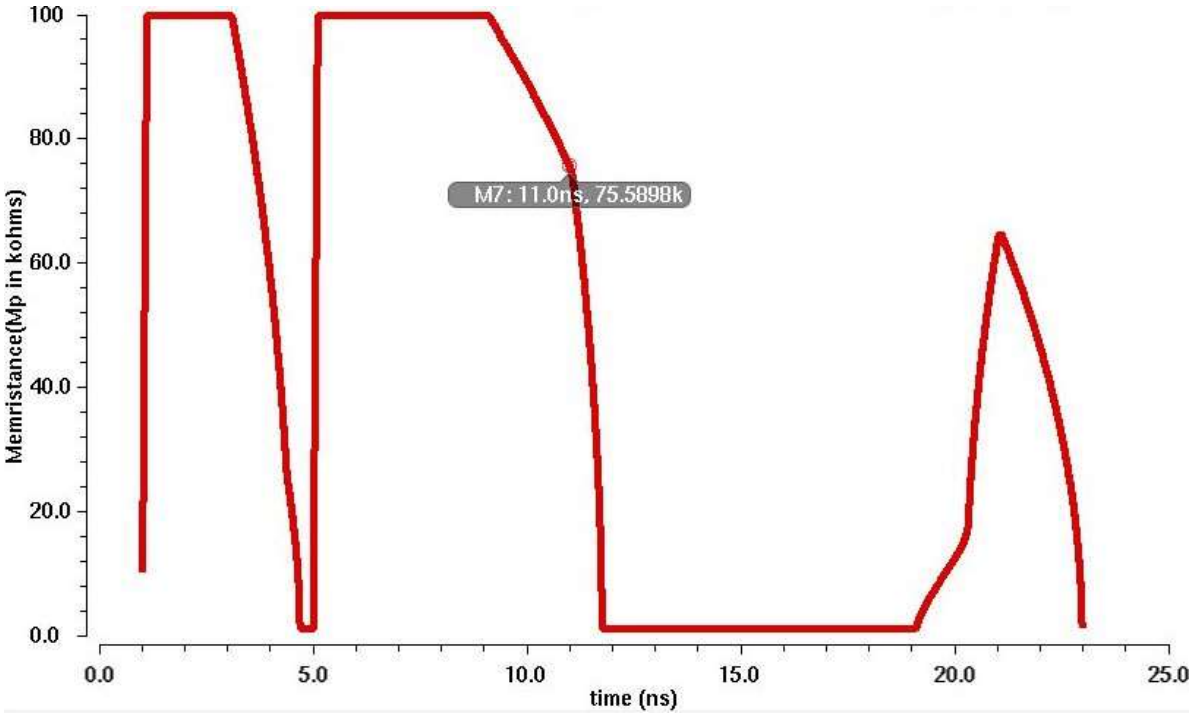


Figure 4.4 (a): Variation in memristance of P for R_g=2kΩ, α=1 without threshold.

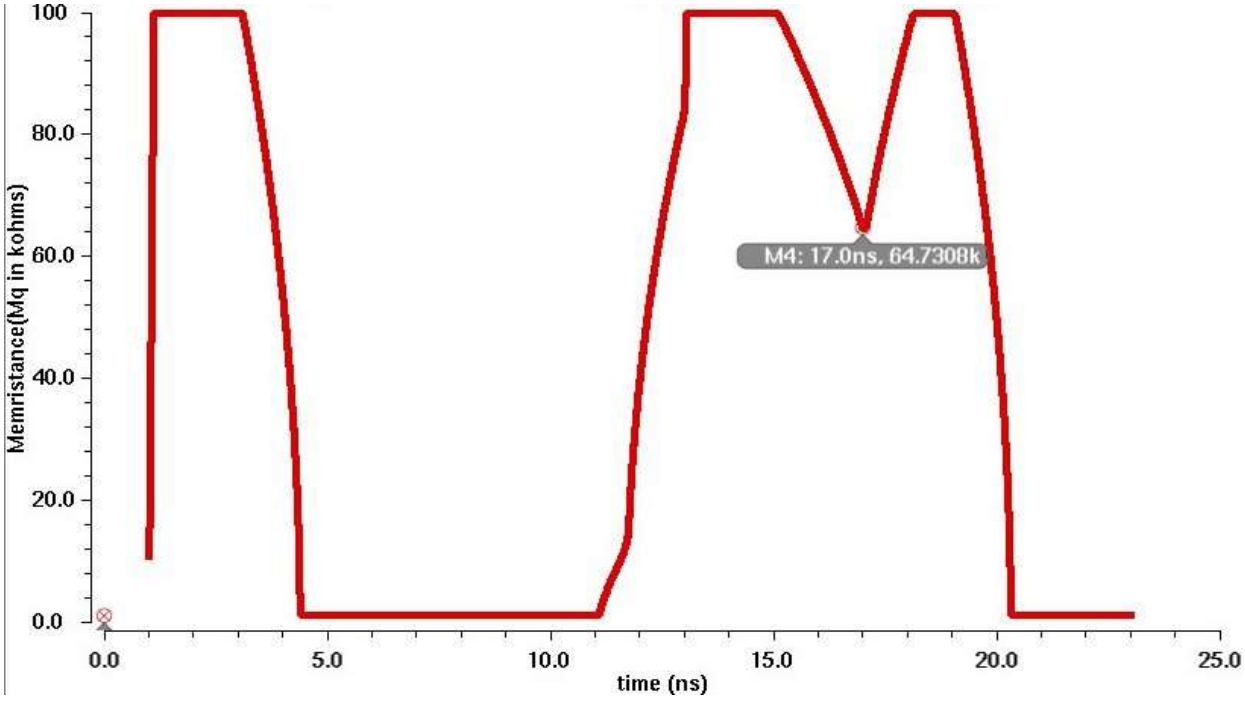


Figure 4.4 (b): Variation in memristance of Q for R_g=2kΩ, α=1 without threshold.

4.2.4 State Drift Problem

Since for case-third, initially the memristance of Q is R_{off} (100KΩ) which corresponds to logic '0'. When we apply the voltages V_{set}, V_{cond} then ideally the logic should remains same (logic '0') but due to some drop across Q, a change in internal state of Q is seen, its resistance tends to drift towards ON switching resistance state (logic '1'). This is called as **state drift.** The output at 17ns should be logic '0' (R_Q=100kΩ ideally) but it is weak logic '0' (memristance of Q at 17ns is lower than that at 15ns). State drift problem is a serious problem and it requires the refreshing of state because repeatedly use for long time may change the logic from logic '0' to logic '1'.

4.2.5 Delay of IMPLY Logic Gate

Since in case-first, memristor requires maximum time to complete logic so it determines the write time or delay time of this IMPLY gate. Because of above two reasons the primarily focus is on case-first and case-third that effect the performance of IMPLY logic gate.

4.2.6 Design of R_g for IMPLY Logic Family

TEAM model is used here and the parameters used here are-

$$\mu v = 1e-14 m^2 v^{-1} s^{-1}, D = 3nm, \text{Ron} = 1\text{k}\,\Omega, \text{Roff} = 100\text{k}\,\Omega, i_{off} = -i_{on} = 100\text{fA},$$

$$\text{k}_{\text{off}} = -\text{k}_{\text{on}} = 0.00000005, \text{dt} = 1\text{e}-12, \alpha = 1$$

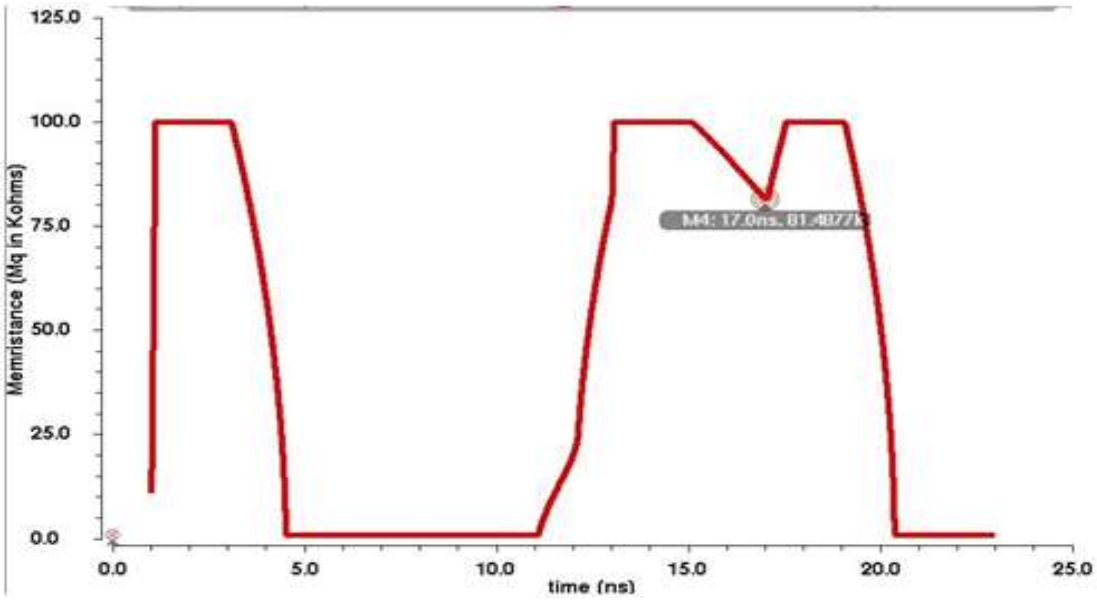


Figure 4.5: Variation in memristance of Q for R_g=5kΩ, α=1 without threshold.

Table 4.3 IMPLY gate analysis for different values of R_g

Resistance R_g(K)Ω	**T_{reset} (Ps)**	**T_{fall} (ns)**	**T_{fall} w.r.t input V_p (ns)**	**T_{fall} w.r.t input V_Q (ns)**	**State drift in Q (for case-third)**
2	6.22	0.9674	1.0104	1.0108	-35.2692%
5	6.74	1.0344	1.0814	1.0818	-18.5123%
10	14.17	1.1465	1.1980	1.9839	-12.005%
15	21.78	1.2650	1.3134	1.3138	-9.6668%

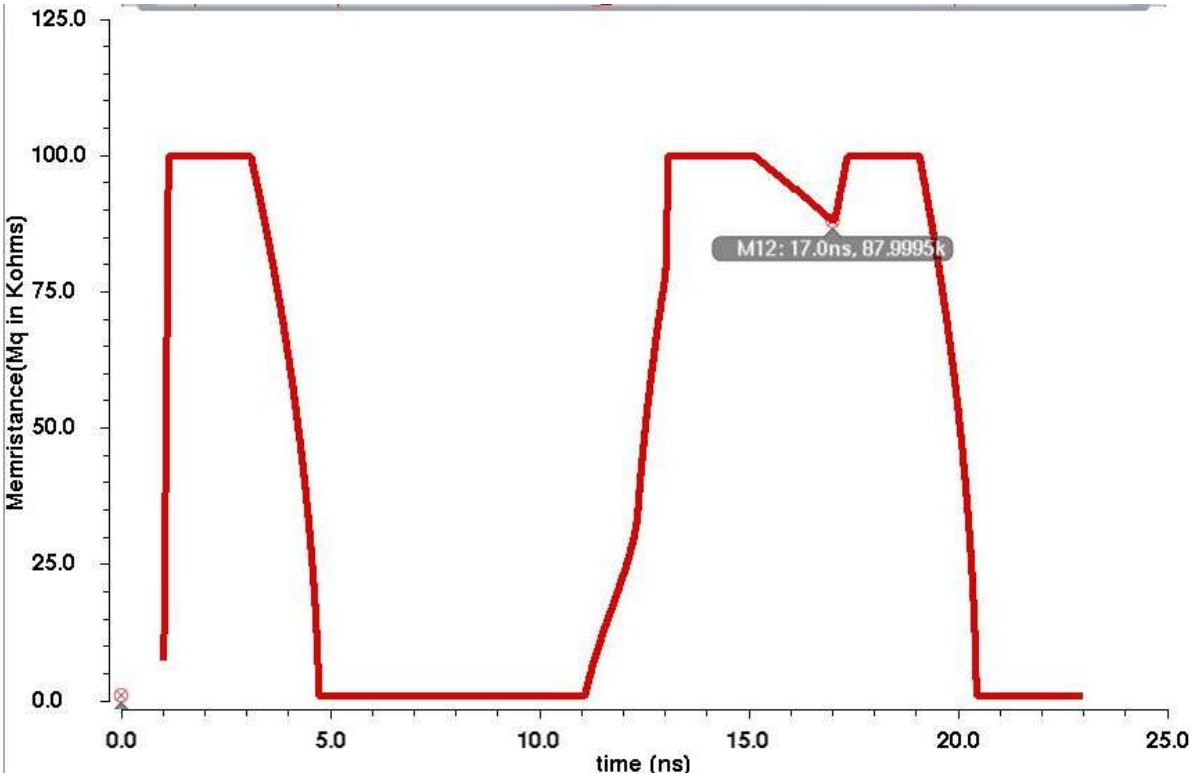


Figure 4.6: Variation in memristance of Q for R_g=10kΩ, α=1 without threshold.

Fig. 4.5, Fig. 4.6, Fig. 4.7 shows the variance in memristance of Q for load reasistances of 5KΩ, 10KΩ and 15KΩ respectively.

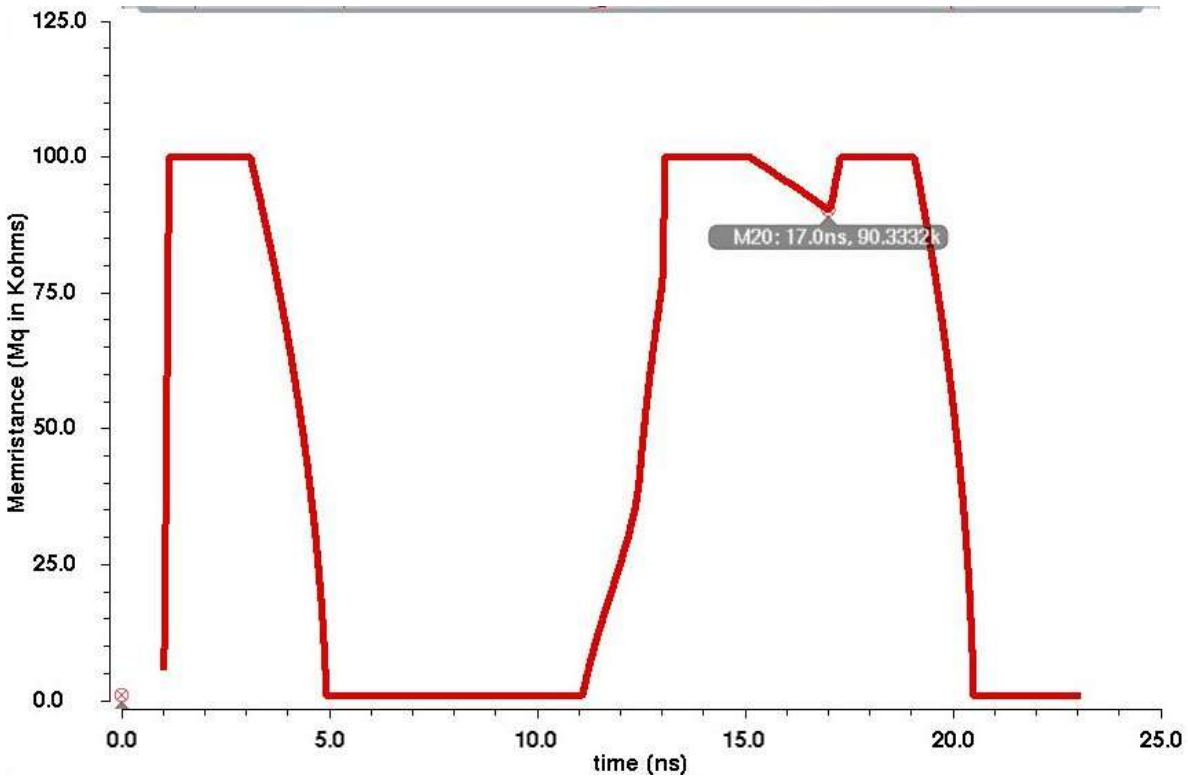


Figure 4.7: Variation in memristance of Q for R_g=15kΩ, α=1 without threshold.

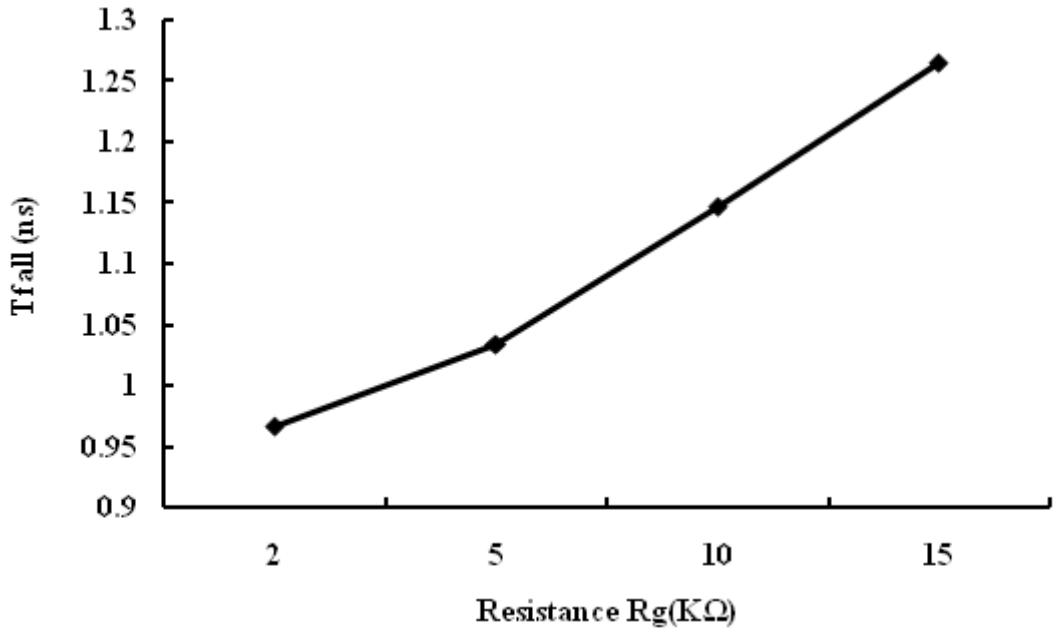


Figure 4.8: Dependence of T_{fall} on R_g.

Fig. 4.8 and Fig. 4.9 reveals that increase in value of R_g results in increase in the write time of IMPLY gate (T_{fall} increases in case-first) which will affect the performance of gate. Increase in R_g also leads to the decrease in state drift in Q of case-third hence increase robustness.

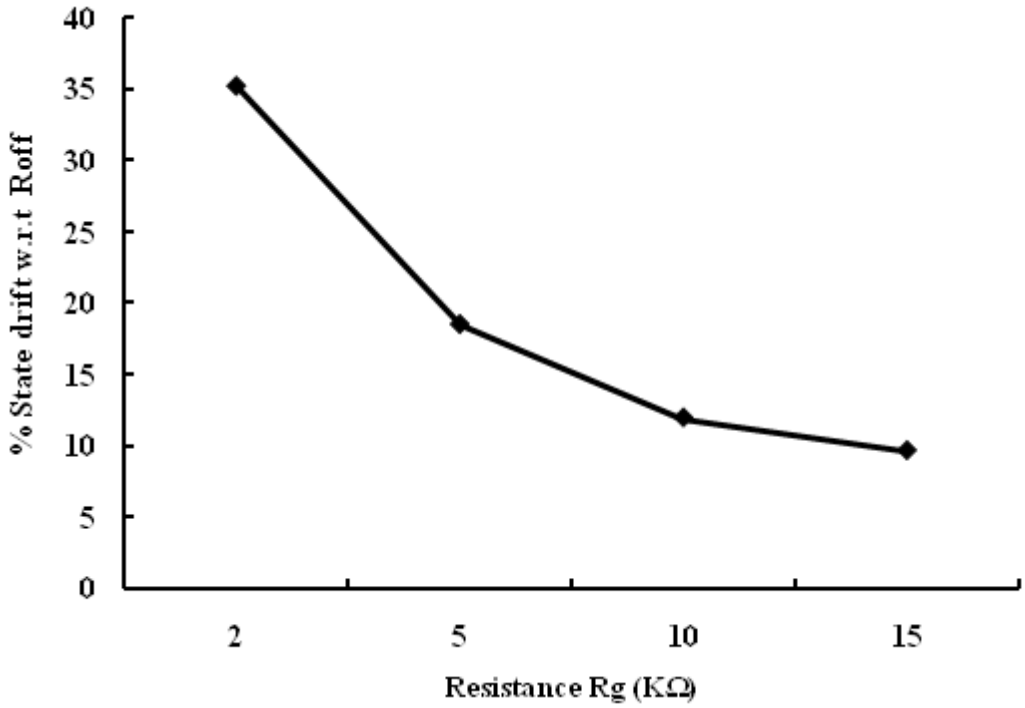


Figure 4.9: Dependence of state drift on $R_{g.}$

4.2.7 Effect of current threshold

TEAM model is used here and the parameters used here are:

$$\mu v = 1e-14 m^2 v^{-1} s^{-1}, D = 3nm, \text{Ron} = 1\text{k}\,\Omega, \text{Roff} = 100\text{k}\,\Omega, i_{off} = -i_{on} = 20\mu\text{A},$$

$$\text{k}_{\text{off}} = -\text{k}_{\text{on}} = 10, \text{dt} = 1\text{e}-12$$

For α=1 (linear HP memristor), and parameters defined above for TEAM model IMPLY gate is simulated for V_{cond} = -1.7v, V_{set} = -2.5v and load resistor R_g is chosen as 2kΩ.

V_{cond} , V_{set} , V_{reset} are chosen according to [9].

$\mathbf{T_{reset}}$in this case is 0.02ns**.**

$\mathbf{T_{fall}}$ observed is 0.315ns; however **no state drift** is seen in Q for case-third.

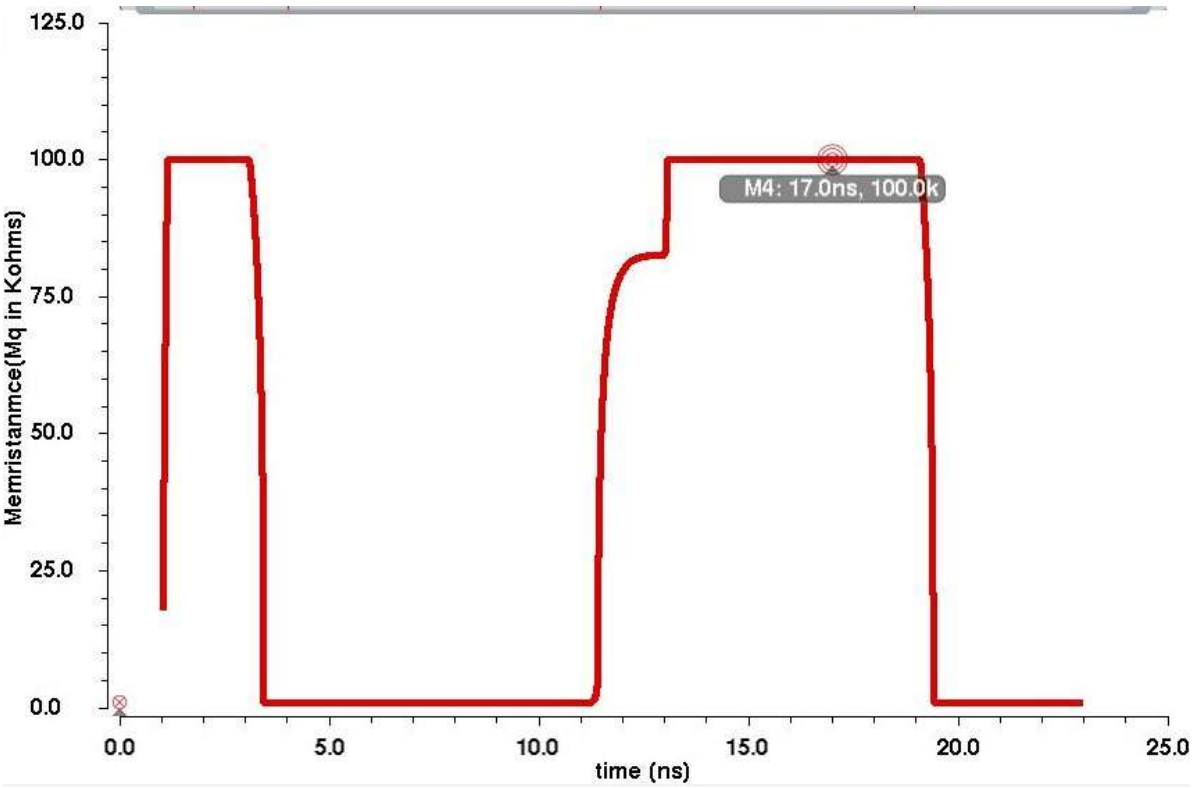


Figure 4.10: Variation in memristance of Q for R_g=2kΩ, α=1 with threshold of 20μA.

Fig. 4.10 shows the Variation in memristance of Q for R_g=2kΩ, α=1 with threshold of 20μA. It is clear from Fig. 4.10 that on increasing the current threshold, the delay of the circuit increases but no state drift problem is observed.

4.2.8 Effect of Non-Linearity

Parameters used here are-

$$\mu v = 1e-14 m^2 v^{-1} s^{-1}, D = 3nm, \text{Ron} = 1\text{k}\,\Omega, \text{Roff} = 100\text{k}\,\Omega, i_{off} = -i_{on} = 5\mu\text{A},$$

$$\text{for } \alpha = 3, \text{k}_{\text{off}} = -\text{k}_{\text{on}} = 0.1, \text{and for } \alpha = 5, \text{k}_{\text{off}} = -\text{k}_{\text{on}} = 0.01$$

Parameters defined above for TEAM model IMPLY gate is simulated for V_{cond} = -1.2v, V_{set} = -1.8v and load resistor R_g is chosen as 2kΩ. Here V_{cond} and V_{set} are chosen according to [9].

Fig. 4.11 shows the variation in memristance of Q for R_g=2kΩ, α=3 with threshold of 5μA and Fig. 4.12 shows variation in memristance of Q for R_g=2kΩ, α=5 with threshold of 5μA

From Fig.4.11 and Fig 4.12 it can be observed that, there is a slight increase in delay of gate on increasing non-linearity but state drift is decreased abruptly.

From Fig. 4.11 for α=3, state drift found is -7.4634%, T_{reset}=0.006ns, T_{fall}=0.44.

From Fig. 4.12 for α=5, no state drift is found, T_{reset}=0.006ns, T_{fall}=0.46.

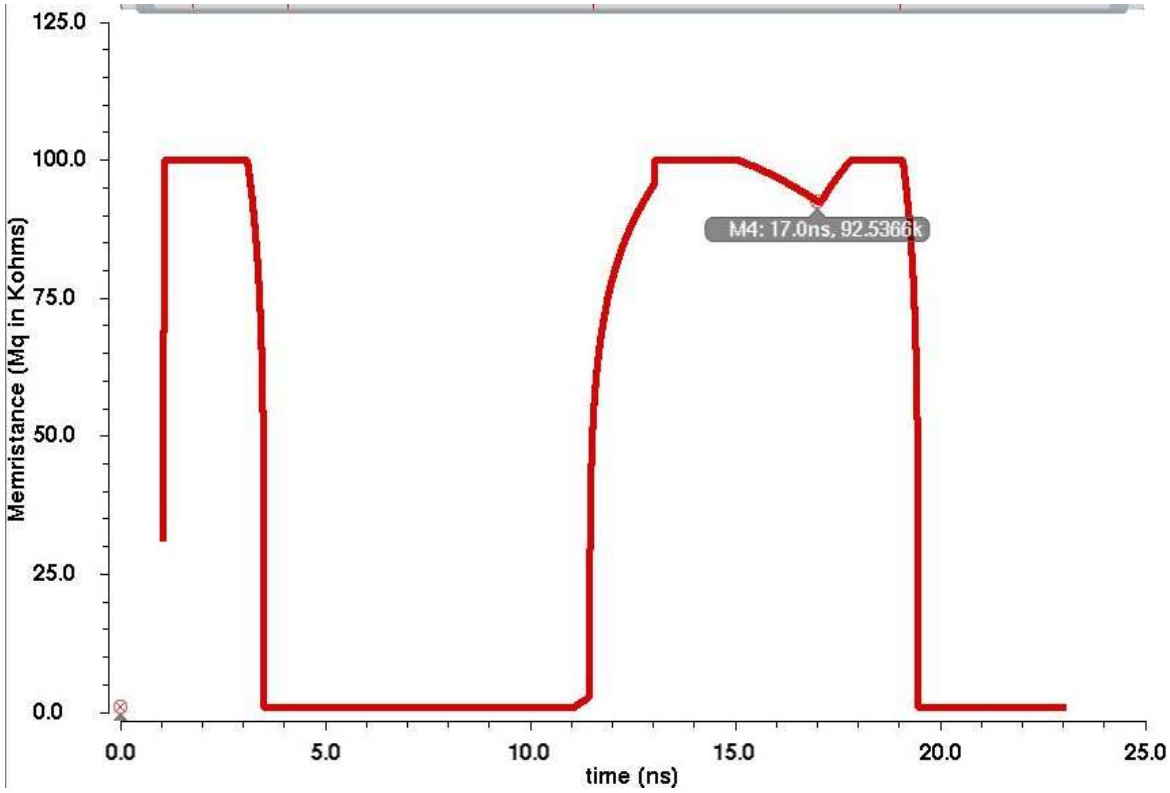


Figure 4.11: Variation in memristance of Q for R_g=2kΩ, α=3 with threshold of 5μA.

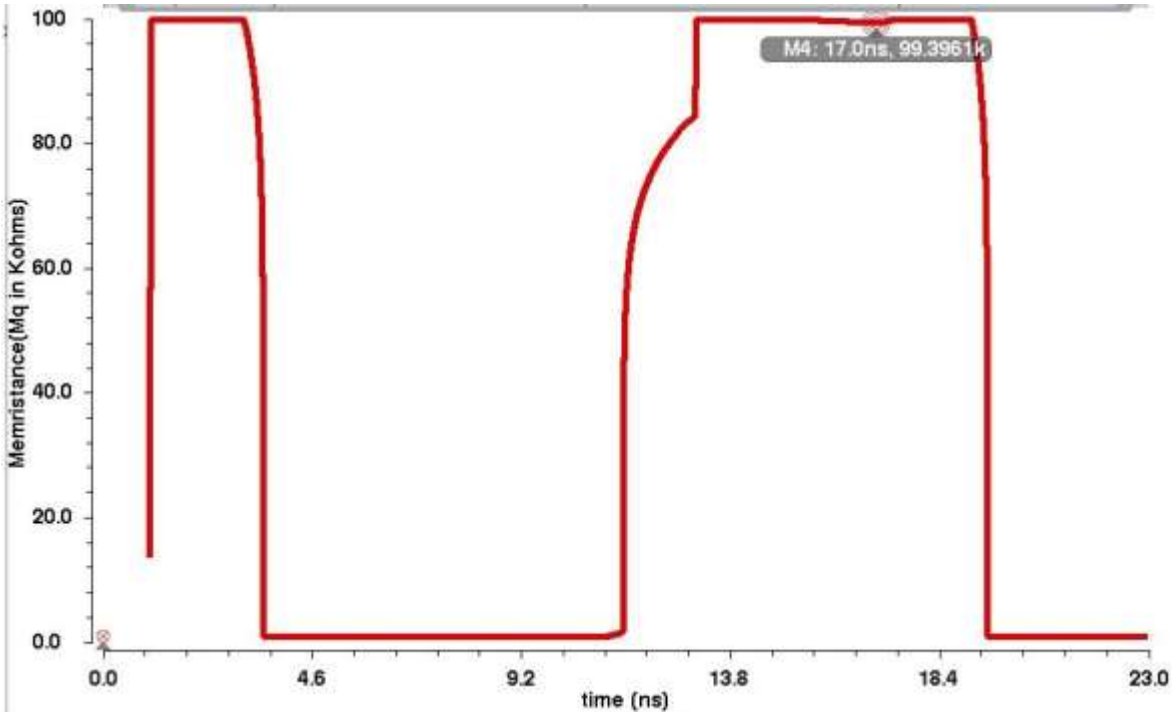


Figure 4.12: Variation in memristance of Q for R_g=2kΩ, α=5 with threshold of 5μA.

It can be observed from the results that, the Linear Memristor suffers more from state-drift problem as compare to non-linear memristor. Adding some practical threshold to this non-linear Memristor is also beneficiary as state drift problem is not observed; also no refreshing

circuit is required. Delay results depends on linearity, applied voltages (V_{cond} and V_{sin}), practical current threshold. Since for different memristors these parameters are different so finding any distinct trend is not possible here.

4.2.9 IMPLY Logic Family

To implement basic gates using IMPLY logic, it is necessary to have knowledge of performing various Boolean operations in this family. Truth tables of various Boolean operations using IMPLY logic are:

1) $\mathbf{A \rightarrow B => B = (\overline{A} + B)}$

A	B	$\overline{A}$	$A \rightarrow B$ =>B
0	0	1	1
0	1	1	1
1	0	0	0
1	1	0	1

2) $\mathbf{A \rightarrow '0' => B = \overline{A}}$

A	B	$\overline{A}$	$A \rightarrow B$ =>B
0	0	1	1
1	0	0	0

3) $\mathbf{'1' \rightarrow B => B = B}$

A	B	$A \rightarrow B$ =>B
1	0	0
1	1	1

(4) $\mathbf{'0' \rightarrow B => B = '0'}$

A	B	$a \rightarrow b$ =>b
1	0	0
1	1	1

Using these, basic IMPLY gate can be implemented as-

1) AND: $\left(\mathbf{PQ} = \left(\left(\mathbf{P} \rightarrow (\mathbf{Q} \rightarrow '\mathbf{0}')\right) \rightarrow '\mathbf{0}'\right)\right)$ **(Required 4 memristors)**

P	Q	$Q \rightarrow '0'$	$P \rightarrow (Q \rightarrow '0')$	$\left(P \rightarrow (Q \rightarrow '0')\right) \rightarrow '0'$	PQ
0	0	1	1	0	0
0	1	0	1	0	0
1	0	1	1	0	0
1	1	0	0	1	1

2) OR: $\left((\mathbf{P} + \mathbf{Q}) = \left((\mathbf{P} \rightarrow '\mathbf{0}') \rightarrow \mathbf{Q}\right)\right)$

P	Q	$P \rightarrow '0'$	$(P \rightarrow '0') \rightarrow Q$	$P + Q$
0	0	1	0	0
0	1	1	1	1
1	0	0	1	1
1	1	0	1	1

3) Duplication the contents of one memristor to another memristor

One extra work Memristor is needed to duplicate contents of Memristor A to M_1.

Duplication of A to M_1 needs 4 steps-

1). False M_1

2). False S

3). A → S

4).$S \rightarrow M_1$

A	M_1	S	$A \rightarrow S$	$S \rightarrow M_1$
0	0	0	1	0
0	0	0	1	0
1	0	0	0	1
1	0	0	0	1

3) BUFFER: $\left((\mathbf{P} \rightarrow {'\mathbf{0}'}) \rightarrow {'\mathbf{0}'}\right)$

P	$\mathbf{p} \rightarrow {'\mathbf{0}'}$	$\left((\mathbf{P} \rightarrow {'\mathbf{0}'}) \rightarrow {'\mathbf{0}'}\right)$
1	**0**	**0**
1	**1**	**1**

4) NOT: $(\overline{\mathbf{p}} = \mathbf{p} \rightarrow {'\mathbf{0}'})$

p	$\mathbf{p} \rightarrow {'\mathbf{0}'}$	$\overline{\mathbf{p}}$
1	**0**	**0**
1	**1**	**1**

6) NAND

Operation steps:

Step-1 L=0

Step-2 $P \rightarrow L$

Step-3 $Q \rightarrow L$

Where L is extra working Memristor (3 memristors are required).

L	P	Q	$P \rightarrow L$ $=> L$	$Q \rightarrow L$ $=> L$
0	**0**	**0**	**1**	**1**
0	**0**	**1**	**1**	**1**
0	**1**	**0**	**0**	**1**
0	**1**	**1**	**0**	**0**

7) XOR

Implementation of XOR in IMPLY logic family is complicated, it needs a total of 13 complicated steps to implement this gate. Operation steps are -

$\text{step} - (1-4)$: Duplicate P to R : False(R) , False(S) , $\text{P} \rightarrow \text{S}$, $\text{S} \rightarrow \text{R}$

$\text{step} - (5-8)$: Duplicate Q to T : False(T) , False(S) , $\text{Q} \rightarrow \text{S}$, $\text{S} \rightarrow \text{T}$

$$\text{step} - 9 : \ \text{Q} \rightarrow \text{R}$$

$$\text{step} - 10 : \ \text{False(S)}$$

$$\text{step} - 11 : \ \text{R} \rightarrow \text{S}$$

$$\text{step} - 12 : \ \text{P} \rightarrow \text{T}$$

$$\text{step} - 13 : \ \text{T} \rightarrow \text{S}$$

Finally result of XOR IMPLY gate is stored in memristor S.

P	Q	Fals e (R)	Fals e (S)	$P \rightarrow S$	$S \rightarrow$ R	Fals e (T)	Fals e (S)	$Q \rightarrow$ S	$S \rightarrow$ T	$Q \rightarrow$ R	Fals e (S)	$R \rightarrow$ S	$P \rightarrow$ T	$T \rightarrow$ S
0	0	0	0	1	0	0	0	1	0	1	0	0	1	0
0	1	0	0	1	0	0	0	0	1	0	0	1	1	1
1	0	0	0	0	1	0	0	1	0	1	0	0	0	1
1	1	0	0	0	1	0	0	0	1	1	0	0	1	0

Thus, two extra work memristors (R and T) and a extra result memristor (S) is needed to Implement XOR gate.

4.3HYBRID CMOS-MEMRISTOR LOGIC FAMILY

In hybrid CMOS-Memristor logic family, voltage decides the logic and memristors are used for computation purpose only. But implementation of AND gate and OR gate with help of memristor is possible in this family, but together with CMOS-inverter we can implement all Boolean operations [65].

4.3.1 Hybrid AND gate

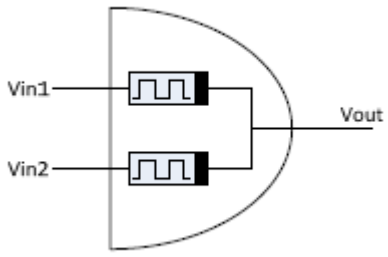


Figure 4.13: Hybrid CMOS-Memristor AND gate.

No voltage drop is seen on both of memristors during the application of identical voltage on both the input terminals and thus whatever input voltage we gave at input same will be replicated at output. When one input voltage is low (logic ‘0’) and other input voltage goes high (logic ‘1’), the current flows from the terminal of memristor corresponds to logic ‘1’ to the terminal of memristor corresponds to logic ‘0’ (from high to low voltage) and thus due to

the polarity of memristors in AND gate circuit, memristance of the memristor which is at high voltage node increases (becomes R_{off}) because current flow out of the black strip through that memristor and thus by voltage dividing rule we have-

$$V_{out} = V_{high} \cdot \left(\frac{R_{on}}{R_{on} + R_{off}} \right) \approx 0$$

4.2.2 Hybrid OR gate:

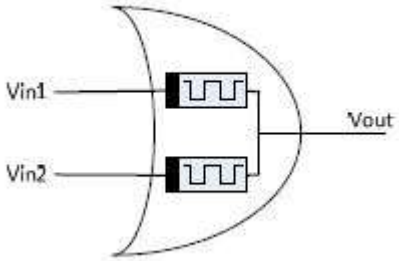


Figure 4.14: Hybrid CMOS-Memristor OR gate.

Operation of hybrid OR gate is similar to that of hybrid AND gate but the main difference is polarities of memristors as shown in Fig. 4.14. On application of identical voltages on both input terminals, no voltage drop is seen on both of memristors and thus whatever input voltage we gave at input same will be replicated at output.

When one input voltage is low (logic '0') and other input voltage goes high (logic '1'), then due to change in polarities of memristors, the high memristance (R_{off}) is observed near low voltage area and vice versa. Thus by voltage dividing rule we have-

$$V_{out} = V_{high} \cdot \left(\frac{R_{off}}{R_{on} + R_{off}} \right) \approx V_{high}$$

4.3.3 Simulation results:

For this TEAM model is used and this model is simulated in Cadence Virtuoso tool. The parameters used are-

$$\mu_v = 1e-14 m^2 v^{-1} s^{-1}, D = 3nm, R_{on} = 1K\Omega, R_{off} = 100K\Omega, dt = 1e-12, i_{off} = -i_{on} = 100fA, k_{off} = -k_{on} = 0.00000005$$

In transient analysis in virtuoso, minimum step is chosen as 1e-12. Output node remains floating and working voltages for these hybrid gates is chosen as 4v.

4.3.3.1 Hybrid CMOS-Memristor OR gate simulation:

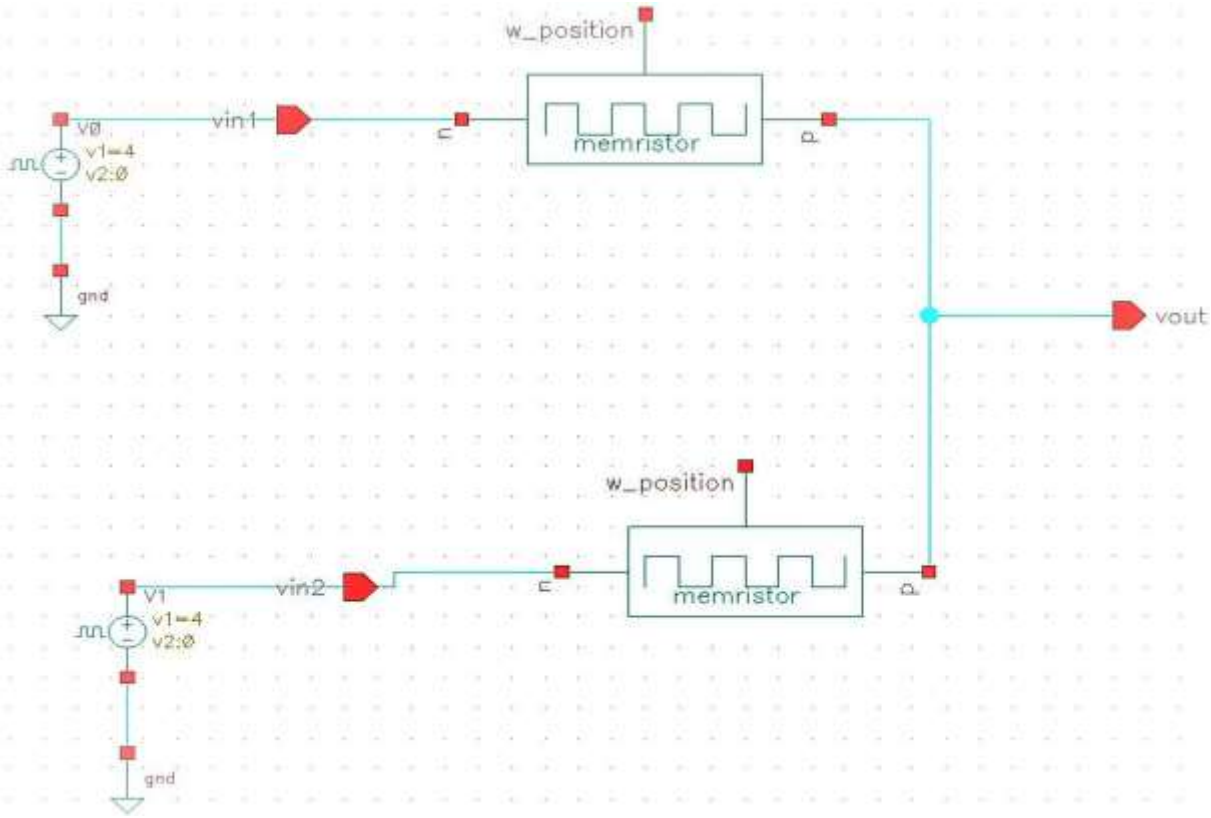


Figure 4.15: Schematic of hybrid OR gate.

Fig. 4.15 shows the schematic of hybrid OR gate and for this gate we assigned a symbol so that we can use it in future. The symbol is shown in Fig. 4.16

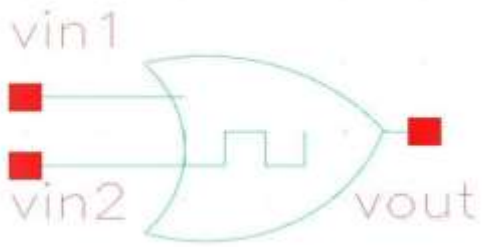


Figure 4.16: Symbol of hybrid OR gate.

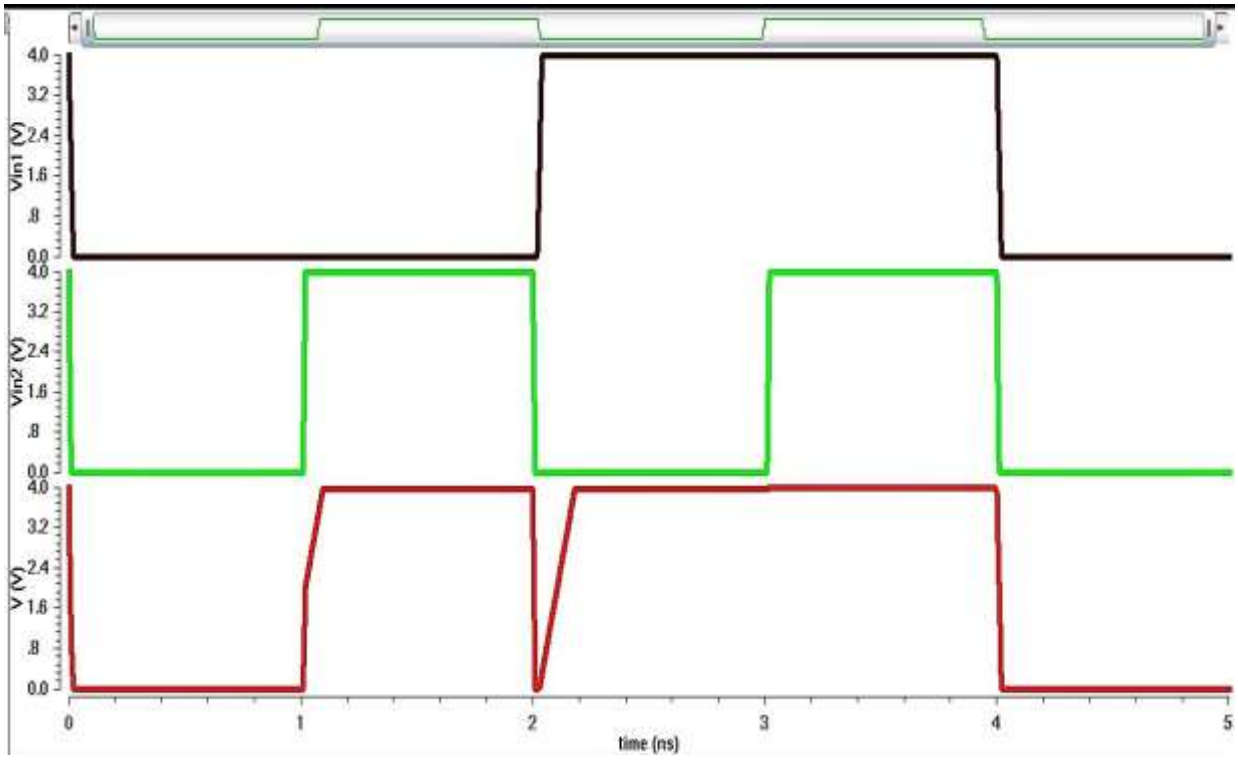


Figure 4.17: Simulation results of hybrid or gate.

4.3.3.2 Hybrid CMOS-Memristor AND gate simulation:

Hybrid CMOS-Memristor AND gate is designed as-

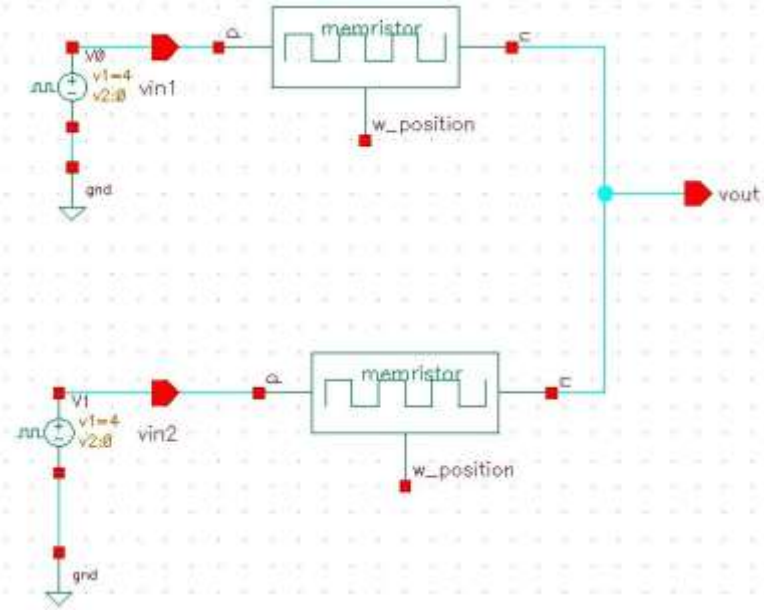


Figure 4.18: schematic of hybrid AND gate.

Fig. 4.18 shows the schematic of hybrid AND gate and for this gate we assigned a symbol so that we can use it in future. The symbol is shown in Fig. 4.19

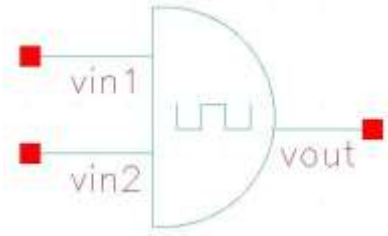


Figure 4.19: Symbol of hybrid AND gate.

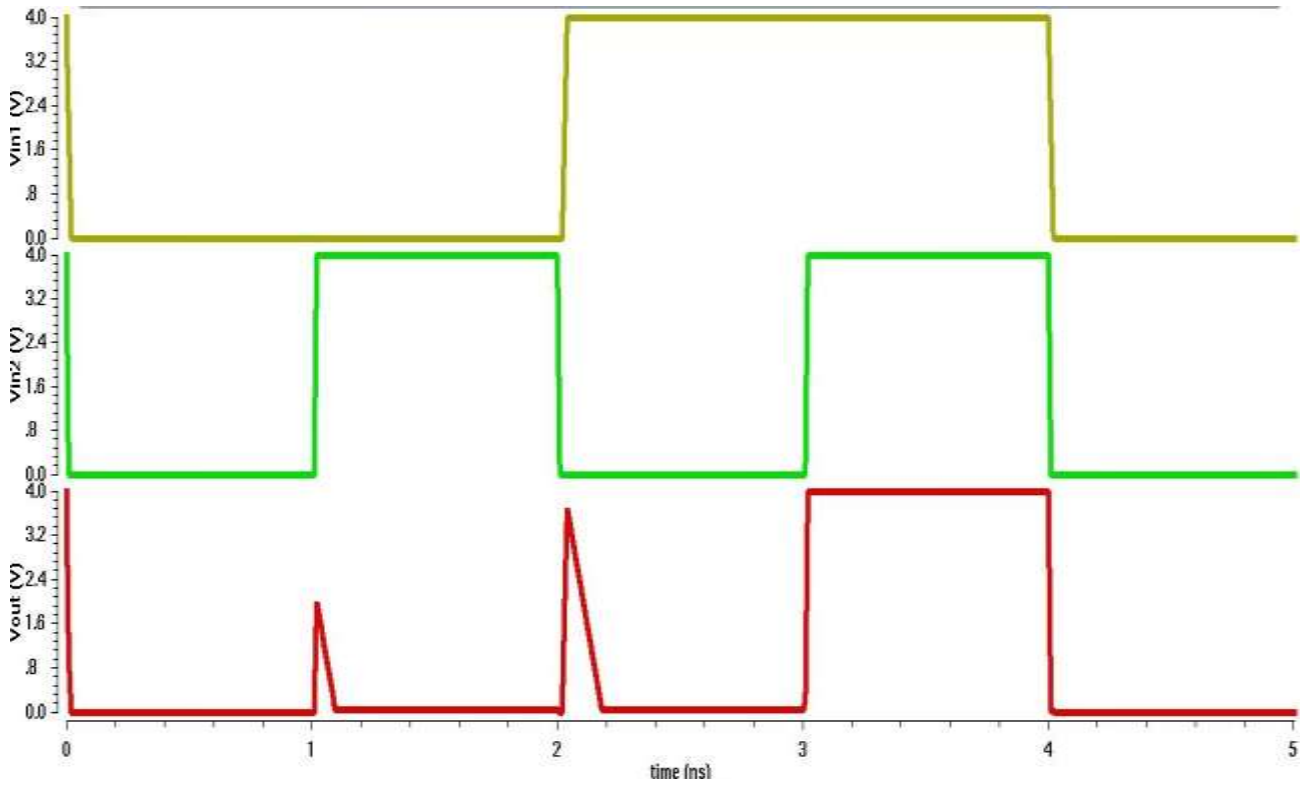


Figure 4.20: Simulation results of hybrid AND gate.

Fig. 4.20 shows the simulation results of AND and OR gate. It is observed that results even if change in voltages at input does not call for output change the output voltage is not always stable because a output voltage is experienced from the node which is connected to memristor having low resistance (R_{on}),thus having the possibility of switching values for different inputs. Thus these gates are producing **"dynamic hazards",** so there is a problem if we sample the output shortly as soon as the input changes and thus we have to wait for a small propagation time. Thus these hazards affect delay constraints of any logic circuits that are implemented with hybrid logic family.

4.3.3.3 CMOS inverter

As discussed above, we need a CMOS inverter to implement all logic operations in this logic family. The design parameters are -

width of NMOS (Wn) = 0.84µm, width of PMOS (Wp) = 1.8µm, channel length (L) = 0.18µm

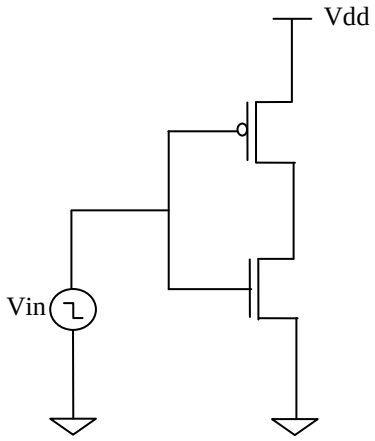


Figure 4.21(a): CMOS inverter

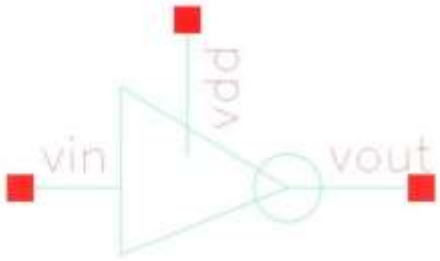


Figure 4.21(b): Inverter symbol

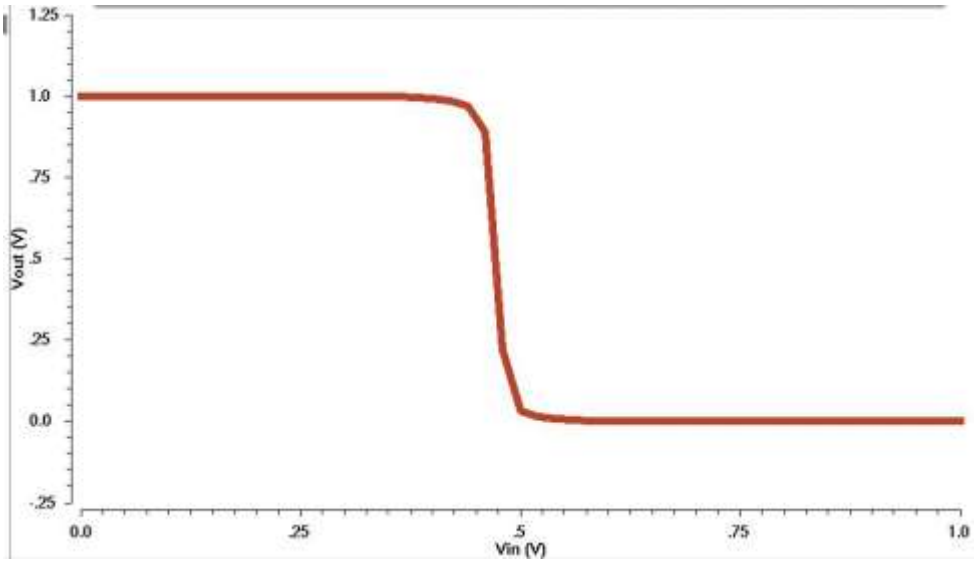


Figure 4.21(c): Voltage transfer curve of CMOS inverter

CMOS-inverter, symbol and its corresponding voltage transfer curve are shown in Fig. 4.20(a), 4.20(b) and 4.20(c) respectively.

4.3.3.4 Hybrid CMOS-Memristor XOR gate

To implement XOR gate, previously implemented hybrid AND gate, hybrid OR gate and CMOS inverter are used.

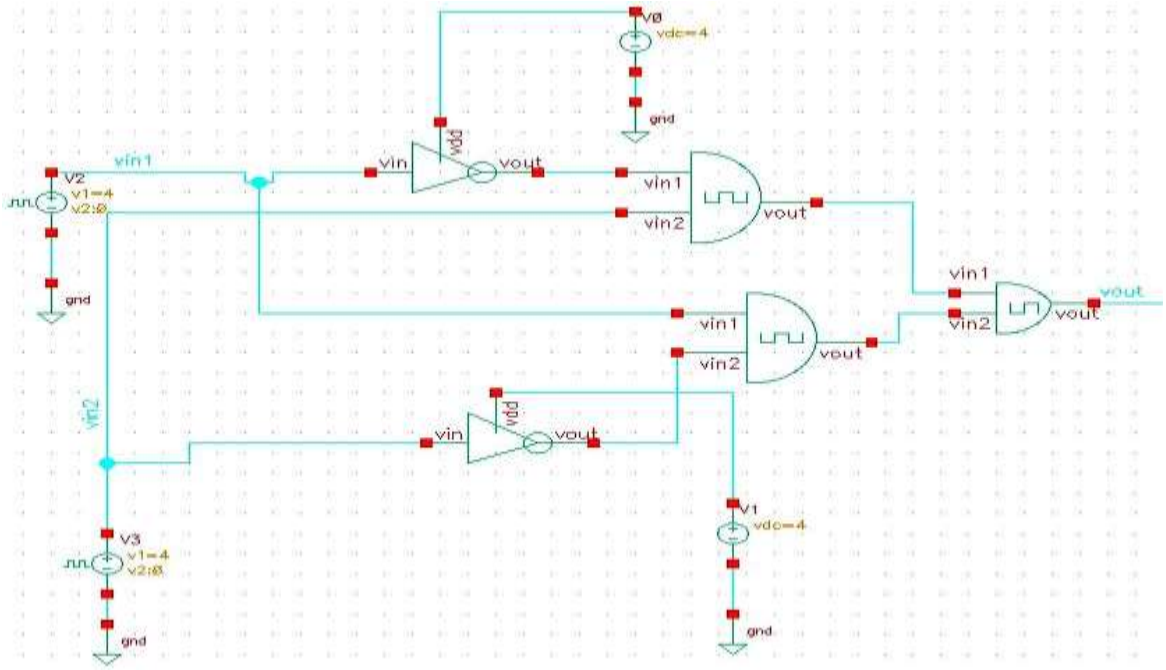


Figure 4.22: (a) Schematic of XOR gate.

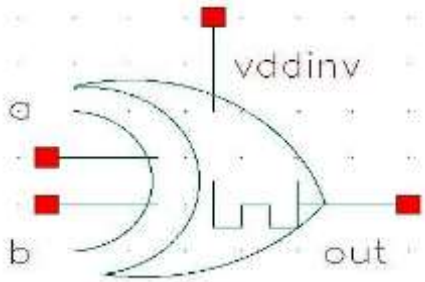


Figure 4.22(b): Symbol of XOR gate.

From simulation of hybrid XOR gate, shown in Fig.4.22(c), an important problem of this logic family comes into picture. Here after settling a large difference is seen between output voltages and applied input voltages (voltage at output is degraded by 33.665% that is instead of 4v we get 2.6534v at output) because here output of one gate is the input to another gate so the current that flows through two memristors of one gate are different and thus there is a possibility that the smaller current is below the current threshold of memristor so memristor will switch partially which results into voltage degradation at output and can fail logic.

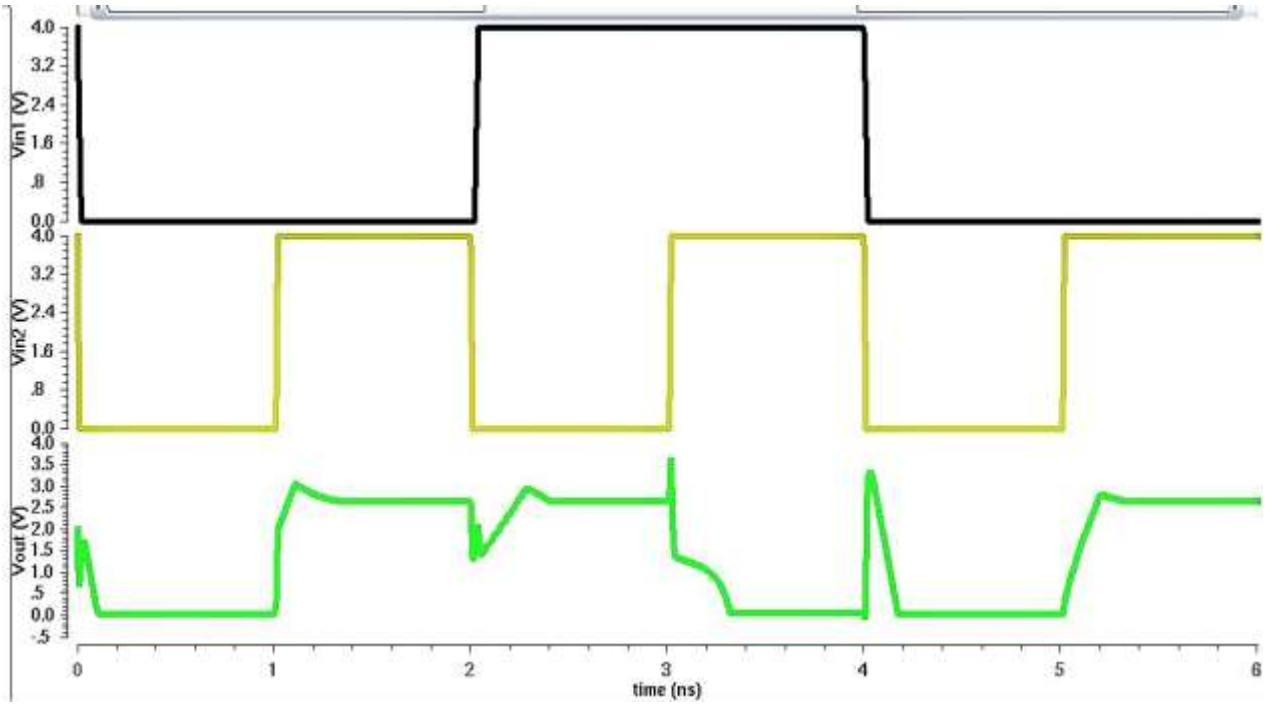


Figure 4.22(c): Simulation results of hybrid XOR gate.

To avoid voltage degradation problem, one possible approach is to increase high logic voltage to ensure that all the currents that flow in the circuit are greater than the current threshold of memristor, so the memristors having low current threshold are beneficiary than high current threshold memristors because low current threshold memristors requires less voltage to operate. Application of large voltage is dangerous for CMOS-inverter and it may cause transistor breakdown [61] also increase power dissipation.

Since the problem is mainly depends on parameters of memristor and structure of circuit. Another approach is to amplify the signal avoiding leakage of current and restore signal, this can be done by using buffer or CMOS-inverter between every two gates. Usage of large number of buffers requires large number of connections between memristor and CMOS (between metal and silicon), thus a large number of vias are needed which will consume more area, so minimum number of buffers or CMOS-inverters should be used to maintain correct output logic. Implementation of hybrid XOR gate (buffer inserted after each stage) and corresponding simulation results are shown in Fig. 4.22(a) and 4.22(b).

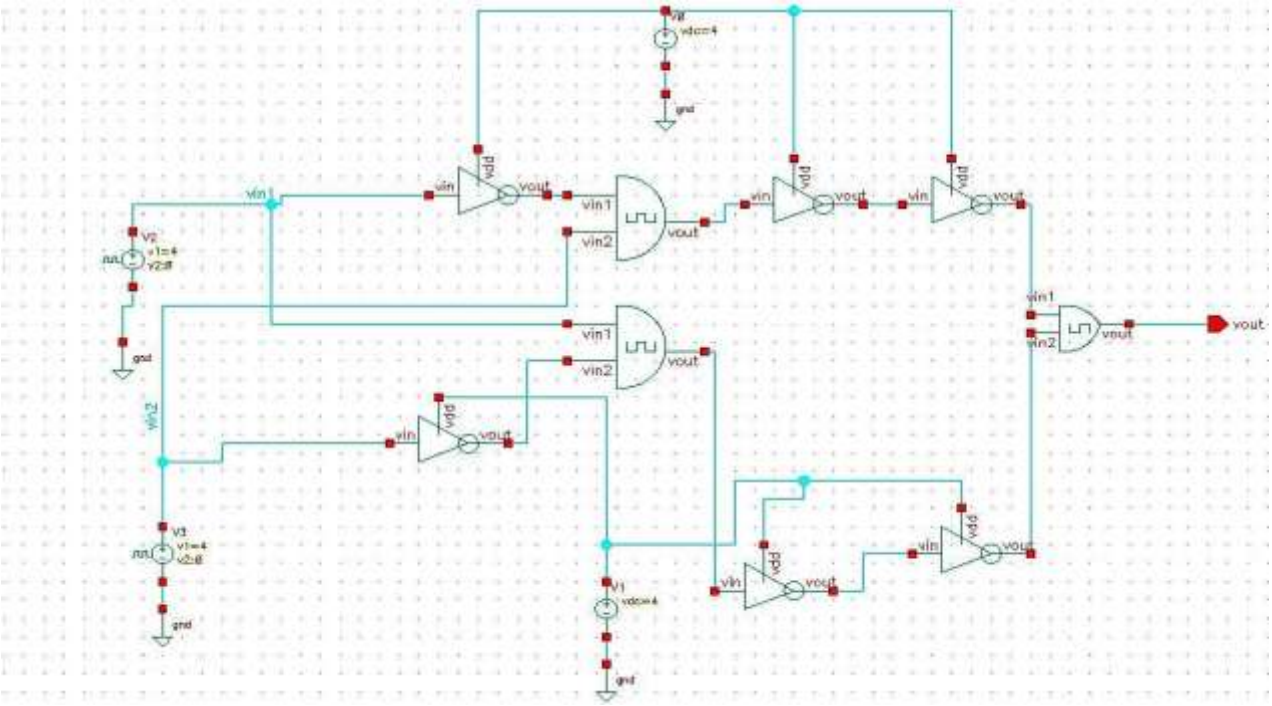


Figure 4.23(a): Schematic of hybrid XOR gate (with buffer inserted between each stage).

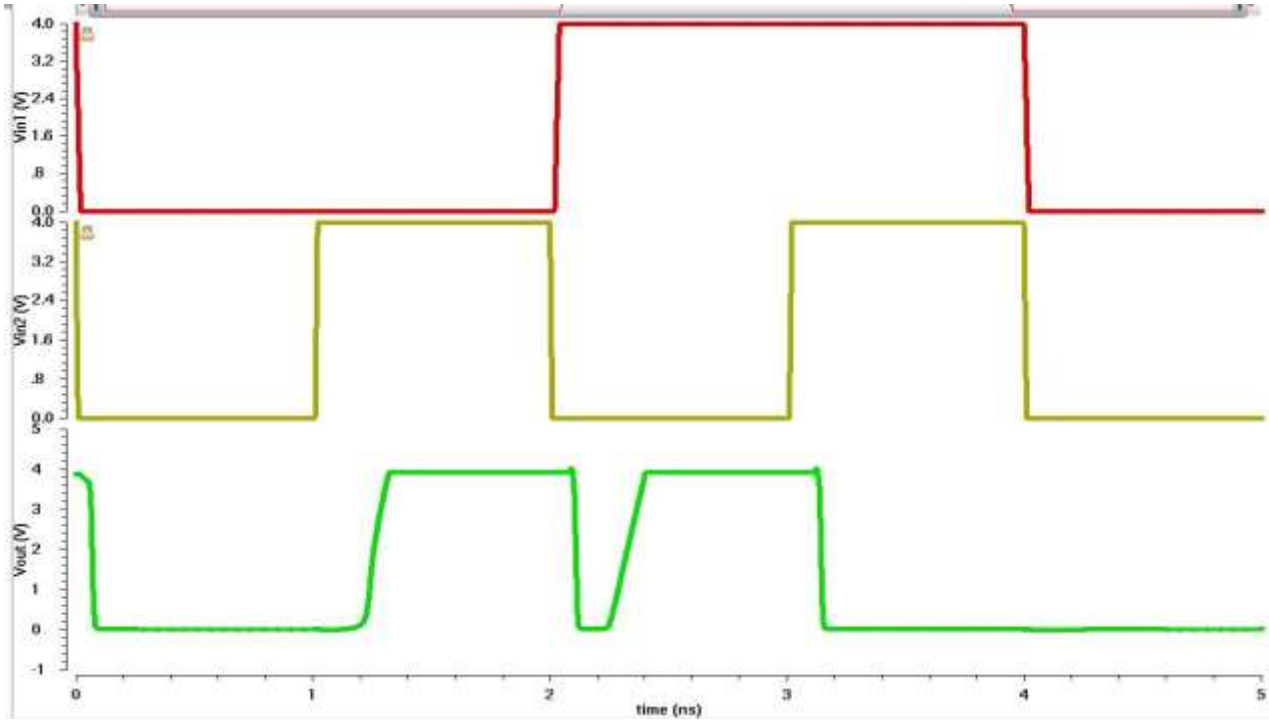


Figure 4.23(b): Simulation results of hybrid XOR gate (with buffer inserted between each stage).

4.3.3.5 Half adder based on Hybrid CMOS-Memristor logic family

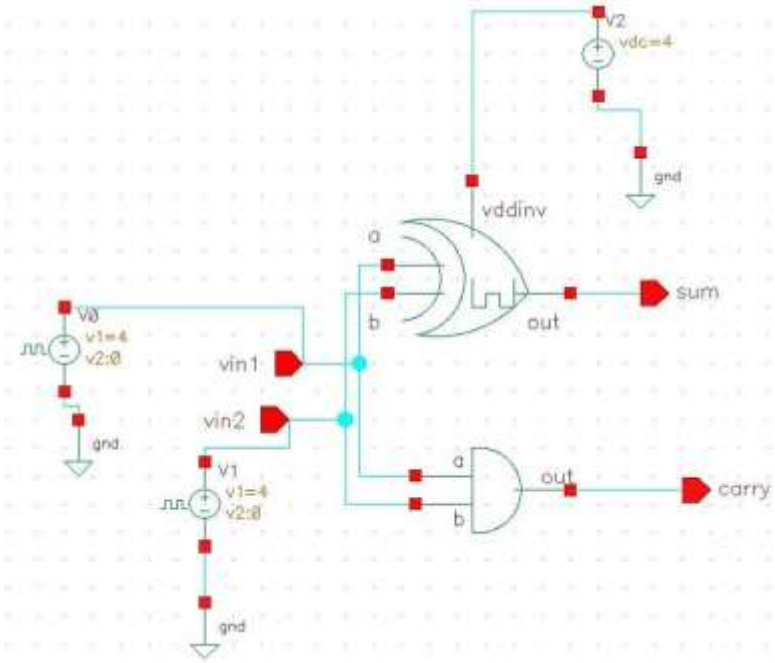


Figure 4.24(a): Schematic of half adder.

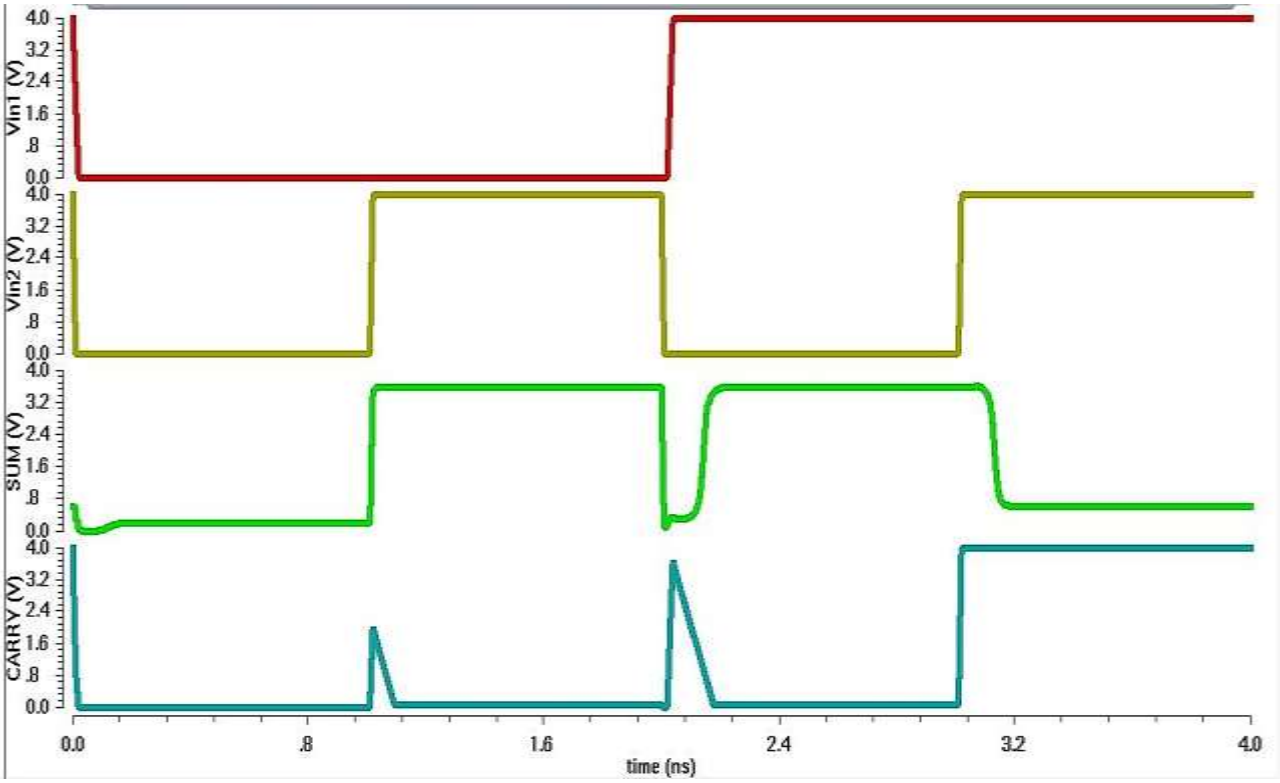


Figure 4.24(b): Simulation results of half adder.

Mehri Teimoori in [14] proposed a new way to design the full hybrid logic family using combination of 1 CMOS-inverter and 4 memristors. This structure provides the output of OR,

AND, XOR gates at the same time which can be used to implement complex circuits where area and power dissipation are the major design constraints. Using this design structure, we can design 1-bit full adder using 4 mosfet transistos and 10 memristors instead of 8 mosfet transistors and 18 memristors presented in [12].

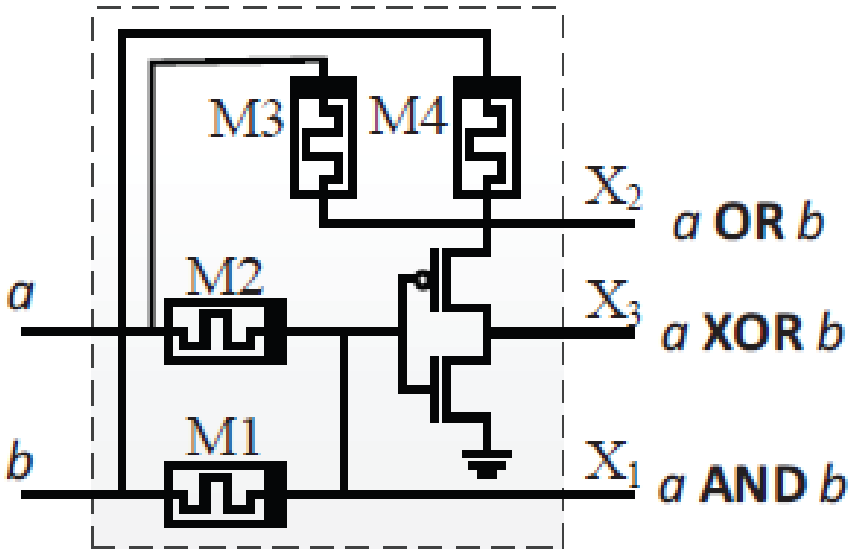


Figure 4.25: Proposed novel MRL universal gate in [69].

In Fig. 4.24, X_1 gives AND gate output, X_2 gives OR gate output. When any one of the two inputs (a or b) is logic zero, then X_1 is at low voltage level thus NMOS transistor gets OFF where as PMOS transistor gets ON and thus voltage of X_2 (high logic voltage) gets tranferred to X_3.

When both inputs are in high logical state then NMOS transistor gets ON where as PMOS transistor gets OFF and thus output X_3 pulled down to low voltage level by NMOS transistor.

When both inputs are in low logical state then X_2 is in low logical state and NMOS transistor gets OFF where as PMOS transistor gets ON and thus output X_3 pulled down to low voltage level by PMOS transistor.Thus we get XOR gate at output X_3.

The design of full adder using design methedology presented in [13] requires 18 memristors and 8 transistors while design of full adder using universal gate presented in [69] requires 10 memristors and 4 transistors. It requires only one power supply for full design of full adder and save approximately 50 % area as compare to [13]. However this design also suffers from voltage degradation problem which can be eliminated by inserting buffers between two stages.

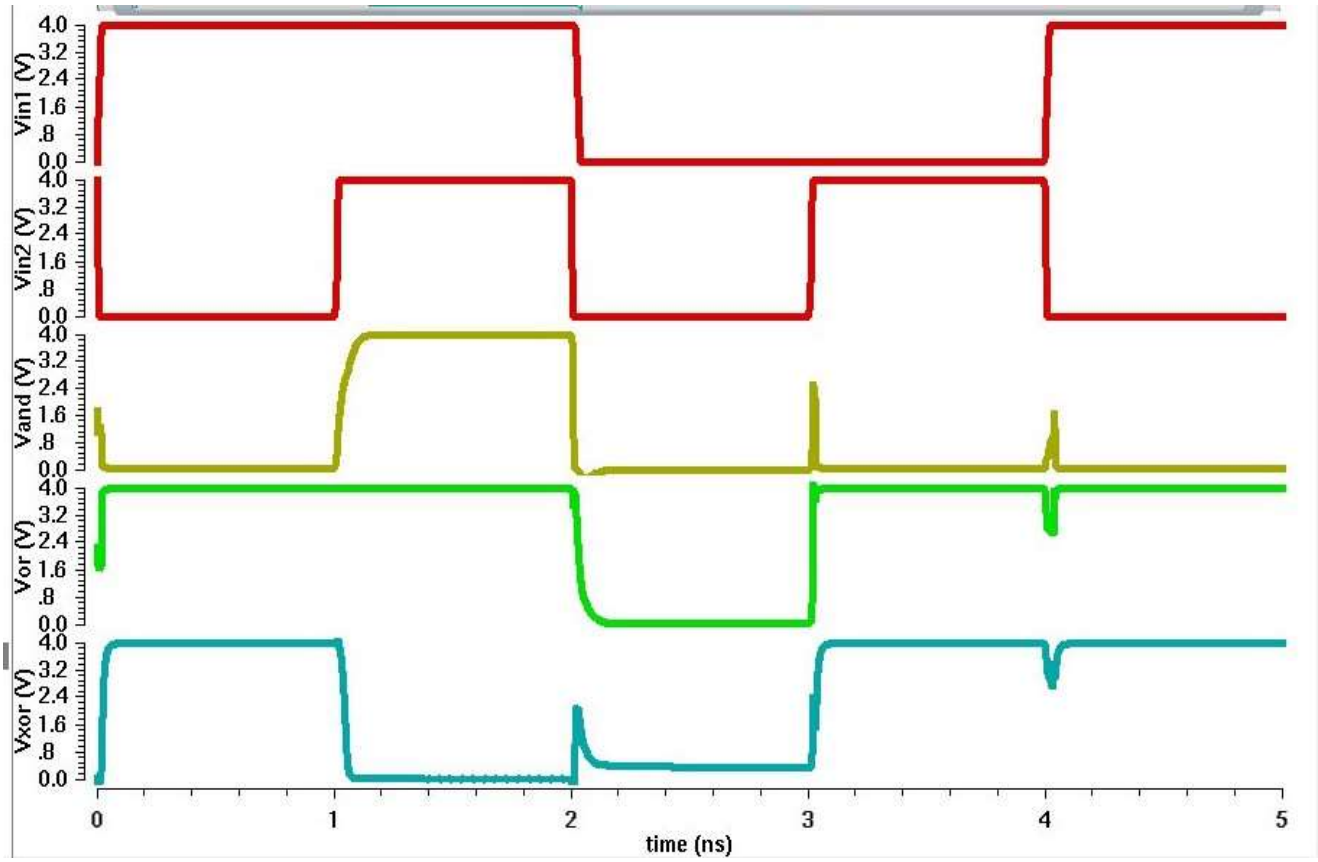


Figure 4.26: Simulation results of universal MRL gate proposed in [69].

CHAPTER

5

A DESIGN APPROACH TO IMPLEMENT AND, OR AND NOT GATES USING MEMRISTOR

5.1 INTRODUCTION

In [10, 11, 12], a design methodology for designing IMPLY gates was presented. Implementation of AND, NOT and OR gates requires a large number of sequential steps, time consuming and also suffers from state drift problem.

In [13], a design methodology for designing MRL (hybrid CMOS-Memristor logic family) based AND, OR gates was discussed, but there is a need of CMOS inverter to implement all Boolean operations also the logic cannot be stored, as the logic is in form of voltage so we can't use this design in memories.

An idea to design the AND, OR and Not gates based on memristor is proposed in 5.2 and proposed AND, OR and NOT gates with their simulation results are presented in 5.3, 5.4 and 5.5 respectively.

5.2 DESIGN APPROACH

An idea to design the AND, OR and Not gates based on Memristor is presented. Like IMPLY logic family the logic is stored with in memory. The inputs are in voltage form whereas output is the memristance of the output memristor which decides the logic. High resistance at output (R_{off}) is considered as logic '0' where as low resistance at output (R_{on}) is considered as logic '1'. Proposed AND gate is very much similar basic IMPLY gate structure (P→Q) except load resistance R_g is replaced by a memristor having high edge resistance (R_{on} and R_{off}) as compare to edge resistances of P and Q.

Proposed OR gate structure is similar to that of proposed AND gate structure except the polarity of input memristors are reversed.

5.3 PROPOSED AND GATE

It consists of two input memristors A and B which are connected to inputs V_{in1} and V_{in2} and one output Memristor C decides the logic. The edge resistances of A and B are negligible as compare to that of edge resistances of Memristor C. Before using this And gate, the output memristor should always be initialized to high resistance state (logic '0').

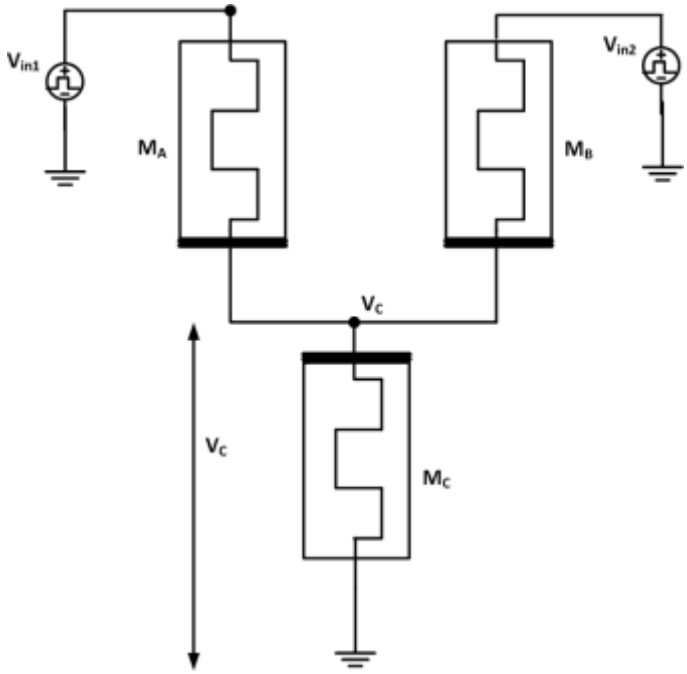


Figure 5.1(a): Proposed AND gate circuit.

- **Case-1:** For $V_{in1} = V_{in2} = 0v$, the voltage at the center node V_c is zero and at the beginning of operation, as the memristor is initialized to R_{off} so its resistance remains unchanged and thus we have logic '0' at the output.

- **Case-2:** For $V_{in1} = 4v$, $V_{in2} = 0v$ then because the highest edge resistance of memristors A and B is always lower than that of lowest edge resistance of memristor C, so always most of the current flows from A to B and because of proposed structure, after some time memristor A reaches to its high resistance state (850Ω) and memristor B to its low

  resistance state (10Ω). Since memristor B and memristor C are connected in parallel, the equivalent resistance is always less than lowest resistance of B, so most of the voltage drop come across A and we have negligible voltage drop across memristor C which is not sufficient to change the state of memristor C and thus we have logic '0' at the output.

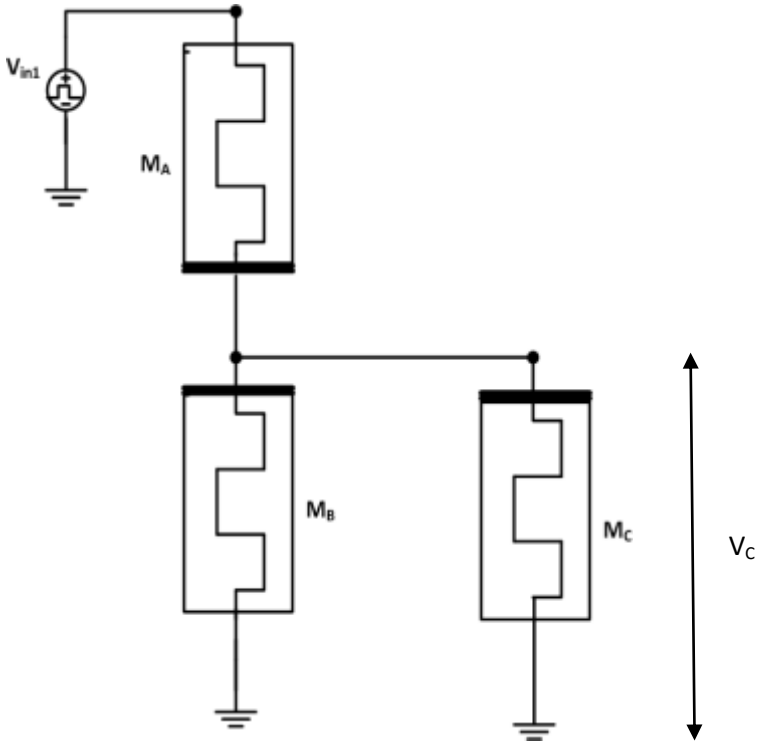


Figure 5.1(b): Study of case-2 of proposed AND gate.

- **Case-3:** This case is similar to case-2, when V_{in1} =0v, V_{in2} = 4v then always most of the current flows from B to A and thus similar to case -2, most of the voltage drop come across B and we have negligible voltage drop across memristor C which is not sufficient to change the state of memristor C and thus we have logic '0' at the output.

- **Case-4:** For V_{in1} = V_{in2} = 4v , the voltage at the centre node V_c is 4v and this voltage is more than sufficient to change the resistance state of output memristor and thus logic '1' at the output is obtained.

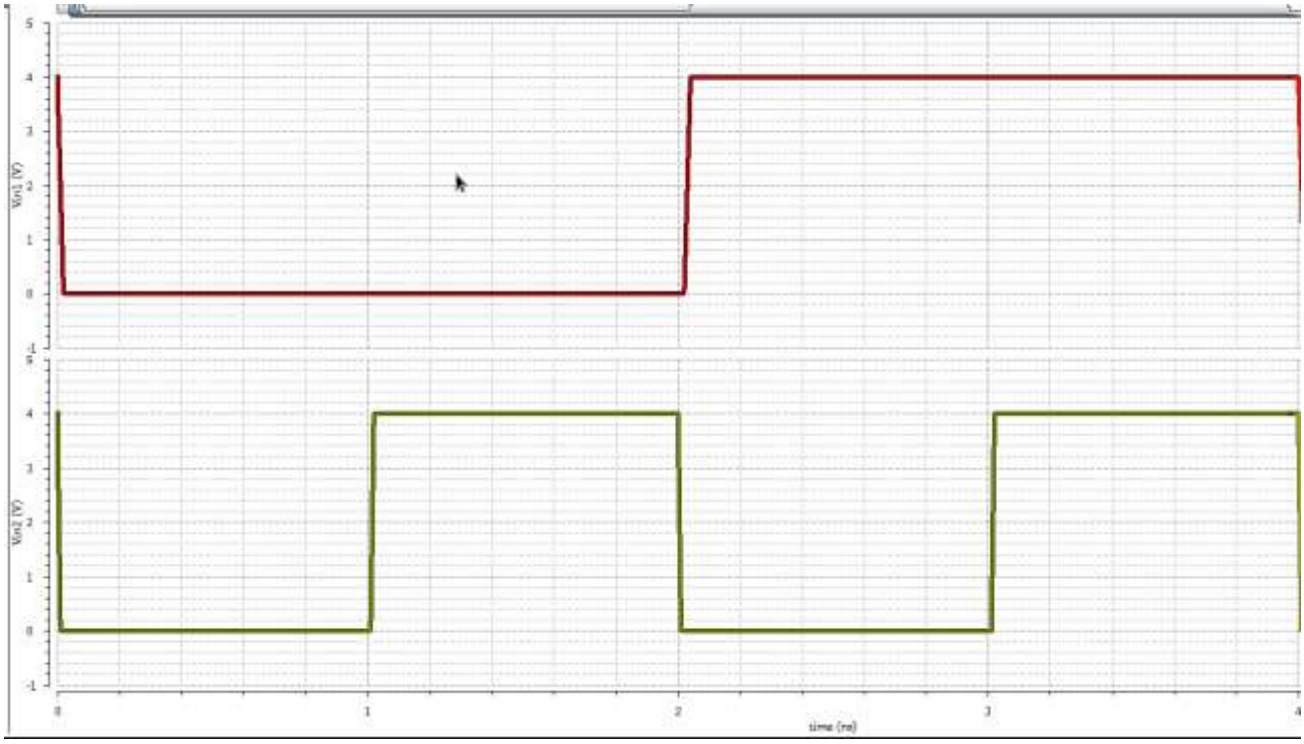


Figure 5.2(a): Input of proposed AND gate

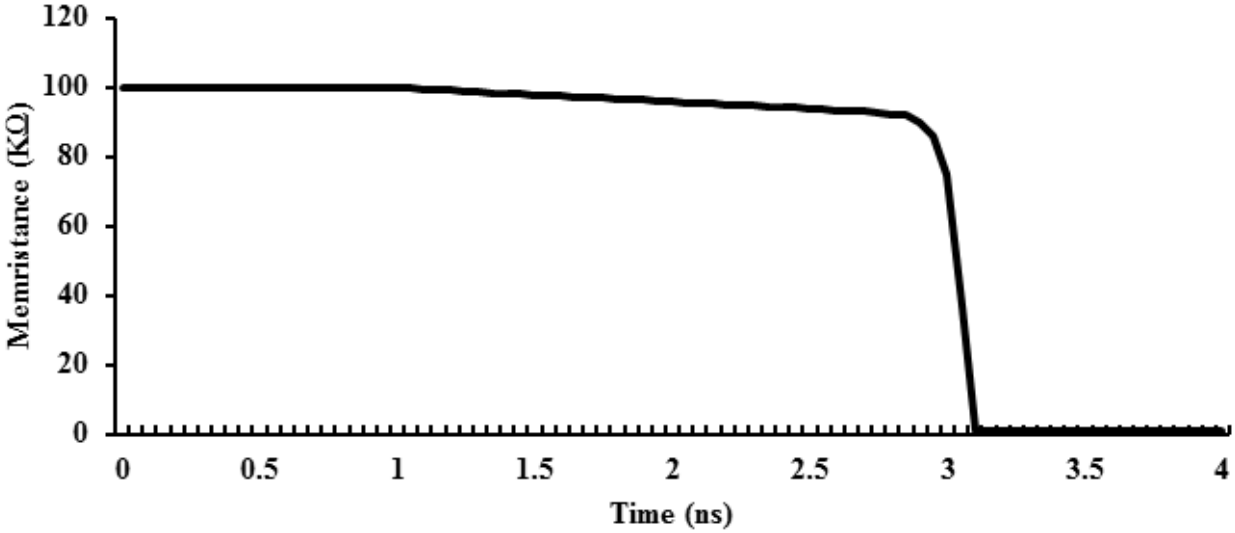


Figure 5.2(b): Output of proposed AND gate.

Fig. 5.2 shows the simulation results of proposed AND gate. It is clear from figure that for case-1, the memristance of memristor C is 100 KΩ (perfect logic '0') but for case-2 and case -3,output is also logic '0' but the memristance for case-2 and case-3 are 95.8KΩ and 90 KΩ because of some flow of current through memristor C .

5.4 PROPOSED OR GATE

Proposed OR gate structure is similar to that of proposed AND gate structure except the polarity of input memristors are reversed. Similar to AND gate, before using this OR gate, the output memristor should always be initialized to high resistance state (logic '0').

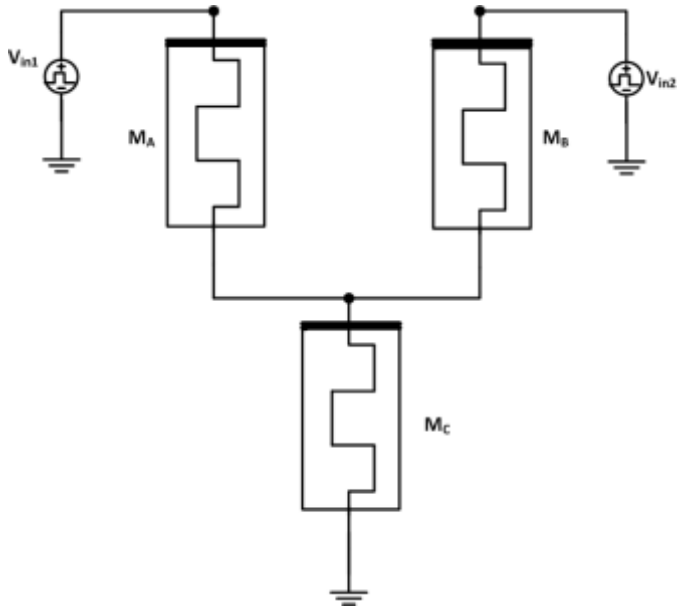


Figure 5.3(a): Proposed OR gate circuit.

- **Case-1:** For $V_{in1} = V_{in2} = 0v$, the voltage at the centre node V_c is zero and at the beginning of operation, as the memristor is initialized to R_{off} so its resistance remains unchanged and thus we have logic '0' at the output.

- **Case-2:** For $V_{in1} = 4v$, $V_{in2} = 0v$ then because the highest edge resistance of memristors A and B is always lower than that of lowest edge resistance of memristor C, always most of the current flows from A to B and because of proposed structure. After some time memristor A reaches to its low resistance state (10Ω) and memristor B to its low resistance state (850Ω). Since memristor B and memristor C are connected in parallel, the equivalent resistance is slightly less than the highest edge resistance of B and thus most of the voltage drop come across and this voltage is more than sufficient to change the resistance state of output memristor and thus we have logic '1' at the output as the memristance of output memristor C reaches to its low resistance state (1kΩ).

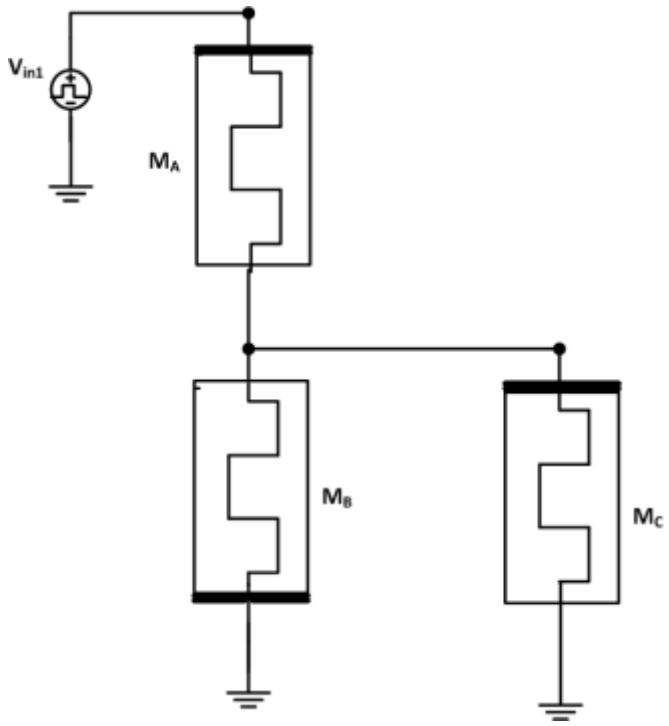


Figure 5.3(b): Study of case-2 of proposed OR gate.

- **Case-3:** This case is similar to case-2, when V_{in1} =0v, V_{in2} = 4v then always most of the current flows from B to A and thus similar to case -2, most of the voltage drop come across C and thus we have logic '1' at the output .

- **Case-**4: For $V_{in1} = V_{in2}$ = 4v, the voltage at the centre node V_c is 4v and thus we have logic '1' at the output.

Fig. 5.4 shows the simulation results of proposed OR gate. It is clear from figure that for case-1, the memristance of memristor C is 100 KΩ (perfect logic '0') but for case-2 and case -3 and case -4, the memristance of output memristor C is 1 KΩ (logic '1').

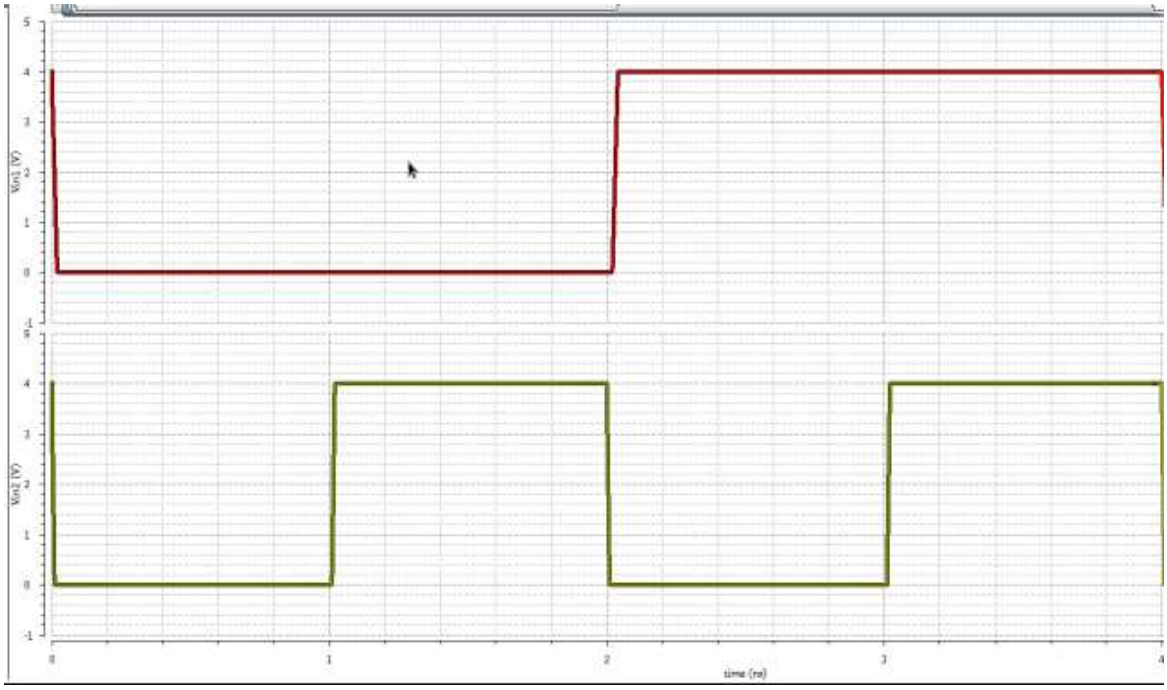


Figure 5.4(a): Input of proposed OR gate.

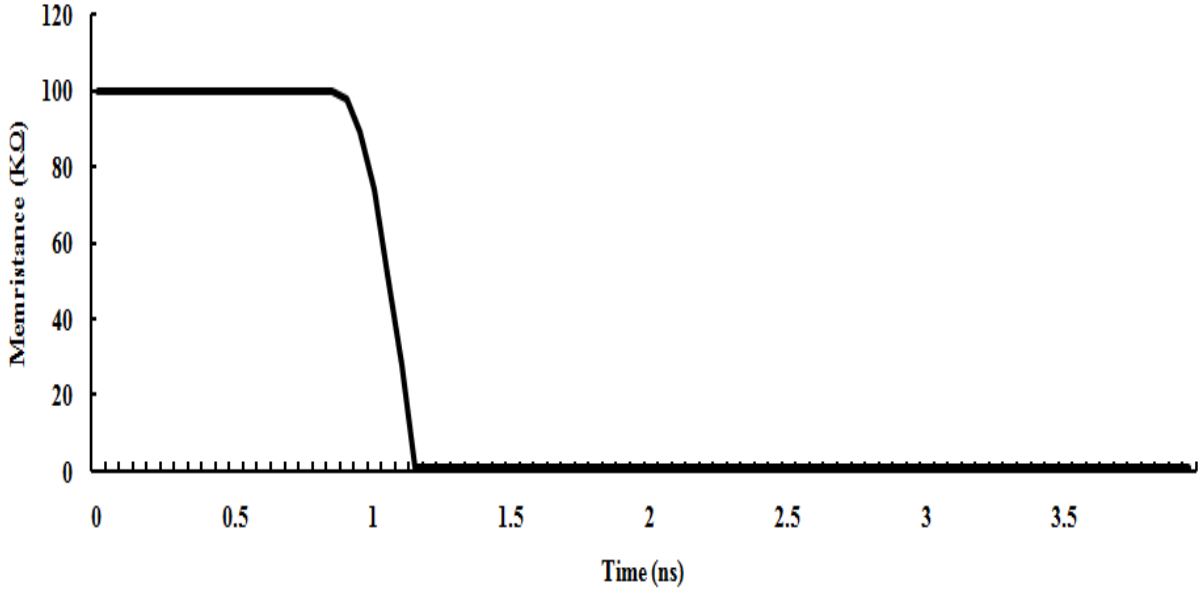


Figure 5.4(b): Output of proposed OR gate.

5.5 PROPOSED NOT GATE

It consists of only one memristor P which acts both as input and output memristor. Before operation, it should be initialized to low resistance state (R_{on}).Figure 5.5 shows the proposed NOT gate and Fig. 5.6 shows the simulation results of proposed not gate.

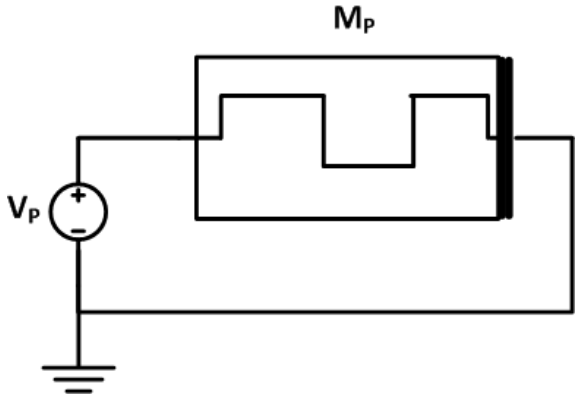


Figure 5.5: Proposed NOT gate.

- **Case-1:** When V_p = 0v, since there is no voltage drop across P so it retains its previous resistance R_{on} (logic 1).

- **Case-**2: When V_p = 4v, there is a voltage drop across P which is sufficient to change its state thus after some time, we have logic '0' at output.

It can be seen from Fig. 5.6, that for case-1, the memristance of memristor P is 1KΩ (logic '1') but for case-2 it rises to 100 KΩ (logic '1').

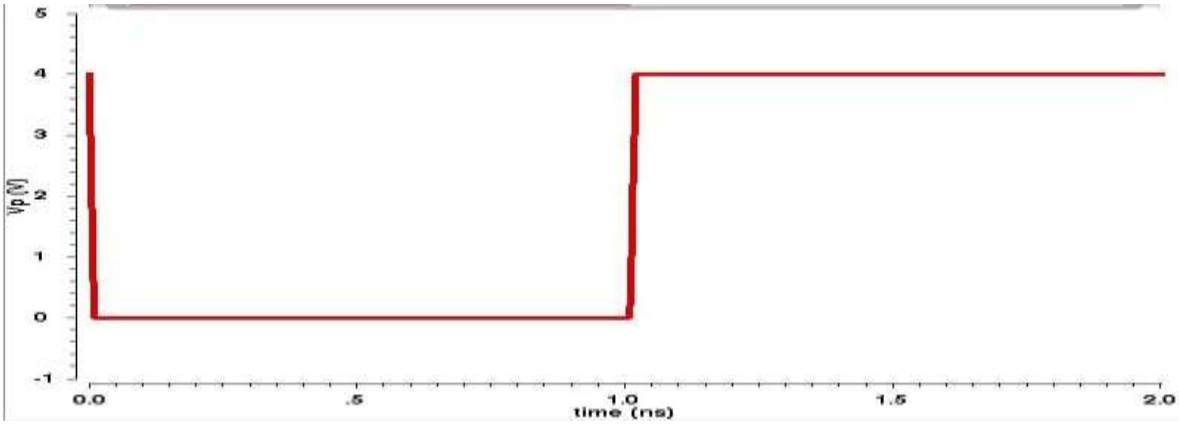


Figure 5.6(a): Input given to of proposed not gate.

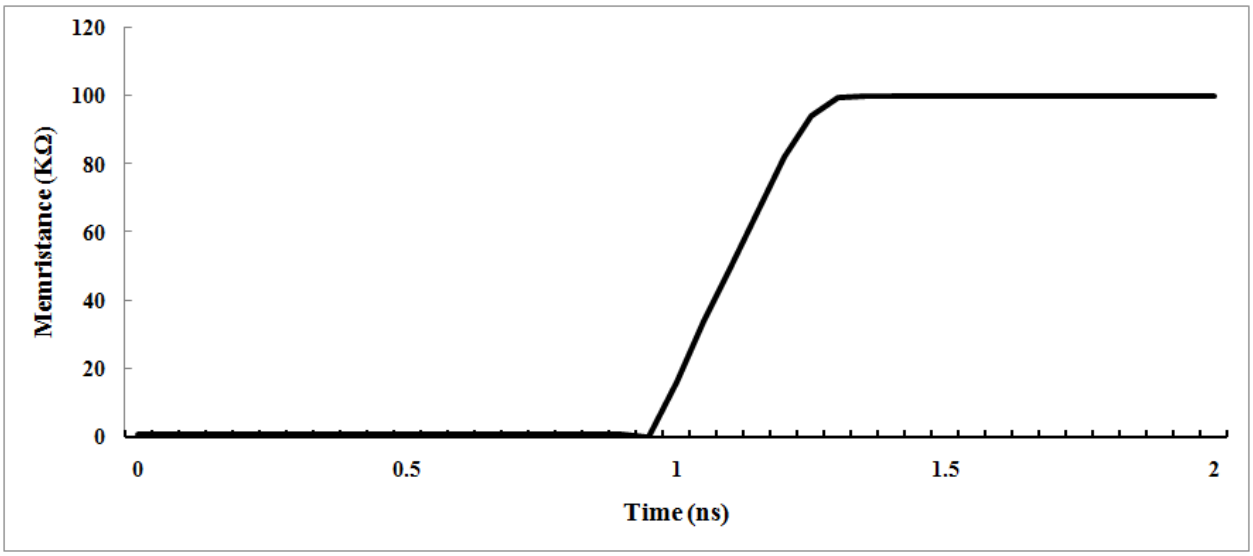


Figure 5.6(b): Output of the proposed not gate.

5.6 CONCLUSION

Design of AND, OR and NOT gate is proposed is this chapter. However, these models need an extra controller circuitry to initialize output memristor. Nevertheless simulation results seem quite satisfactory.

CHAPTER

6

A COMPARATIVE ANALYSIS OF MEMRISTOR BASED LOGIC FAMILIES

6.1 INTRODUCTION

A comparative study of memristor based logic families is presented in this chapter, shown in Table no - 6.1.

6.2 COMPARATIVE ANALYSIS

The outcomes of thesis are presented below:

6.2.1 Speed analysis:

- Generally the speed is –

  Hybrid CMOS > Proposed design > IMPLY

- Since in case of hybrid CMOS and proposed design, we get output in only one clock cycle. But IMPLY logic is sequential in nature and conduct its calculations in different time intervals, so we can use fast clock and thus integration with fast architectures is possible.
- As IMPLY is sequential in nature and logic is within memory so there is no need of extra registers to introduce it in pipeline structures.

6.2.2 Area analysis:

- As the memristors are smaller in size compared to registers and MOSFET transistors, therefore the order of the area of various families is:

  Proposed design < IMPLY < hybrid CMOS

- However proposed design and IMPLY need extra controller circuitry to initialize memristors which increase area.

Table 6.1: A comparative analysis of memristor based logic families

		Proposed design	Hybrid CMOS [13]	IMPLY design [12]
Speed		Average	Fastest	Slowest
Area reqired		Minimum	Maximum	Average
Type of logic		Logic within memory	Voltage decides logic, memristors used for computation only	Logic within memory
Effect of initial value of Memristance		Initial value of memristance affects logic operations.	Initial value of memristance does not affect logic operations but affect timings of gate.	Initial value of memristance affects logic operations.
Fundamental Boolean function		AND, OR, NOT	P IMPLY Q	With inverter, we can implement any Boolean function
Number of Operation steps	**OR**	1	3	1
	AND	1	4	1
	NOT	1	2	1 (NOT gate is implemented using NMOS and PMOS)
Number of Memristors, transistors	**NOT**	1 memristor	2 memristors + 1 register	2 memristors
	AND	3 memristors	4 memristors + 1 register	2 memristors

and registers.	**OR**	3 memristors	3 memristors + 1 register	1 NMOS and 1 PMOS
Controller required		YES	YES	NO
Power consumption		Minimum	Average	Maximum
Complexity in operation		Average	Maximum	Minimum

6.2.3 Power Analysis

By [12, 13] and under the assumption that Memristor consume less power than resistor and MOSFET transistor, the order of power consumption is:

Proposed design < IMPLY < Hybrid CMOS

6.3 CONCLUSION

- As compare to IMPLY, Hybrid CMOS needs high working voltages so the linear memristor having low current threshold will consume less power.
- In case of IMPLY logic, power depends on the memristor linearity and current threshold so we are not able to find distinct trend but to avoid state drift problem, a non-linear memristor with high current threshold is preferable.
- In Hybrid CMOS, increase in current threshold (for fast operation and less dynamic hazards) results in the need of more buffers between two stages thus increase area, memristor with no current threshold provides best trade of between area, power consumption and timings.

CHAPTER

7

CONCLUSION AND FUTURE SCOPE

7.1 CONCLUSION

In this thesis, we examined three ways to implement logic with the use of memristors in which both kinds of logic design approaches (logic within memory and CMOS-memristor integration) are covered. As the research is in its early stage, so obviously many questions are there regarding design methodology. In this thesis, feasibility of logic and factors effecting logic with memristor is successfully analyzed. An approach to design AND, OR and NOT gate is also proposed. Major outcomes are:

- The type of memristor chosen has a little effect on feasibility of logic, as compared to type of logic family chosen.
- Hybrid CMOS can be fastest if we use high current threshold memristor, but they become less power efficient. Integration ofmemristors with CMOS, forces them to use at a particular voltage which will affect both timings and power.
- Proposed design provides the best tradeoff between timings, area and power consumption.

7.2 FUTURE SCOPE

The behavior of memristor to memorize the recent value, when we cut off the power supply makes it a suitable candidate to be used for memory applications. It can be also used for implementation of logics. From many years ago, we are performing all logic operations using CMOS design methodology. In the early stages of research, it was predicted that we cannot perform all Boolean operations using memristor but now we can implement any Boolean operation using memristors. This gives us a hope to use memristor not only for memory but also for CPU purpose. At this time we have an idea of using memristor in CPU architecture by integrating MOSFET transistors with memristors but in near future there is a possibility that even these transistors can be replaced by combination of memristors and the same chip can be used for both memory and computation purpose looks like neural brain, so in future

there is a possibility of having the architecture that compute like human brain rather than Von-Neumann architectures.

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