Testing and Measurement of Operational Amplifier

Dissertation submitted towards the partial fulfillment of requirement

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Submitted by

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DECLARATION

I hereby declare that the dissertation entitled "Testing and Measurement of Operational Amplifier" is an authentic record of my study carried out as partial requirement for the award of degree of M.Tech. (VLSI Design) at Thapar University, Patiala, under the supervision of Dr. Alpana Agarwal, Associate Professor, ECED and refers other researcher's work which are duly listed in the reference section.

The matter embodied in this thesis has not been submitted for award of any other degree at this or any other university.

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Abstract

Today, the operational amplifier is the most important analog device which is being used in almost all the electronic system. Every electronic system has its own requirement. So it is very necessary to measure the specification of the Op-Amp before using it in the respective application.

The present work, proposes a servo Op-Amp based test circuit for the measurement of the performance parameters of the Op-Amp. An extra Op-Amp is added in the feedback loop which is acting as an attenuator. By doing this it is possible to completely reject any input signal feed-through from the feedback loop. So an extra Op-Amp completely decouples the output from the input. Simulations of the test circuit are performed using a spice based simulator MULTSIM. TLV2772CP, a CMOS based Op-Amp is used as the device under test. Verification of the simulated results is being done by the using a measurement setup on the bread board in the laboratory and the results are compared with the data sheet of the DUT.

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Abbreviations

OPAMP	Operational Amplifier
DUT	Device Under Test
CMOS	Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
IC	Integrated Circuit
ATE	Automatic Test Equipment
CMRR	Common Mode Rejection Ratio
PSRR	Power Supply Rejection Ratio
VCVS	Voltage Controlled Voltage Circuit
CM	Common Mode
NG	Noise Gain
OBT	Oscillation based Test
POBT	Predictive Oscillation based Test
PQOBT	Predictive Quassi Oscillation based Test
DOBT	Direct Oscillation based Test
OTA	Operational Trans-Conductance Amplifier
SPICE	Simulation Program with Integrated Circuit Emphasis
GBW	Gain Bandwidth Product

Motivation

The classical operational amplifier has become, since its invention, a comer stone for the analog designers. Every electronic system contains the operational amplifier. The Op-Amp characteristics are defined by some of its specifications like open loop gain, input offset voltage, input bias current, common mode rejection ratio, power supply rejection ratio. But measuring the specifications is a challenging task. For an example, if we go by the definition of the open loop gain, the ratio of the output voltage to the input voltage in open loop configuration is called open loop gain. But for high precision Op-Amp having gain 10^6, the input voltage required is on micro volts. At such a small level of the input voltage noise will play a significant role and can add to the input voltage to give incorrect results of the open loop gain. Moreover the Op-Amp will saturate with slight variation in the input voltage which is very difficult to measure. So it is always preferable to measure the open loop gain in the close loop configurations. There exists different kind of test circuits to measure the specifications of the Op-Amp. Moreover, as the technology is advancing day by day the “time to market” of the integrated circuits is an important parameter for the IC designers and it is very important to complete the manufacturing process of the IC in the desired time. The time to market can be reduced by the reducing the test time. So there is a need of the test circuits which can measure the important specifications on a single test circuit and reduce the test time.

CHAPTER-1
INTRODUCTION

Applying the physical principles so that we are able to design the new devices from which the humanity can be benefited is called the engineering. But without measurement one cannot understand the physical principles. It is a common saying that the physics is the science that measures the reality.

The integrated-circuit operational amplifier is the most widely used linear circuit in the design and construction of electronic system. There are many specification of the op-amp like open loop voltage gain, input offset voltage, common mode rejection ratio (CMRR), power supply rejection ratio (PSRR) etc. The measurement of the specification of the op-amp is a challenging task. For example, ideally the open loop voltage gain of the operational amplifier should be infinite but practically it is as large as 200,000. Open loop voltage gain of such operational amplifier cannot be measured in open loop configuration because for such a large gain input voltages required is of the order of micro volts. At such small voltages other non-linear effects like noise also affects the measured value. So open loop voltage gain is measured in closed loop configuration.

1.1 TEST ENGINEER

Without defining the test engineer we cannot understand how does the test procedure of testing a device under test (DUT) works [1]. Here along with the test engineer it is important to understand the role of Design engineers, Product engineers & System engineers. Each profession has its own set of tasks and responsibilities.

The production of a new product can begins in any one of two ways. It may be the case when a customer demanding the product with its own specifications or an organization wants to produce a device according to the market need. In both cases, systems engineers have an important role to play by deciding the technical specification of the new product so that it will meet the requirement of the customer. The system engineers generally perform the responsibility of deciding specification of the product while the other can design the new device and ensures its release within stipulated time.

Once the system engineers have done their job that is defining the technical requirements then it is the job of the design engineer to develop the corresponding integrated circuit. The new design must meet the requirement of the customer. Unfortunately, some times the new IC is not according to the required specifications. It may be due to the defects while fabricating the IC or it may be due to the bad design of the design engineer. Whatever the case may be faults must be removed from the IC.

The hardware and the software used to test the DUT via automated test equipment (ATE) is generated by the test engineer. The ATE is directed by the software to apply various inputs to record the response of the DUT. The relays are used to attach the test hardware to the DUT. On the basis of the recorded response, test engineer whether the IC is good or bad. After passing the test DUT can be shipped to the customer.

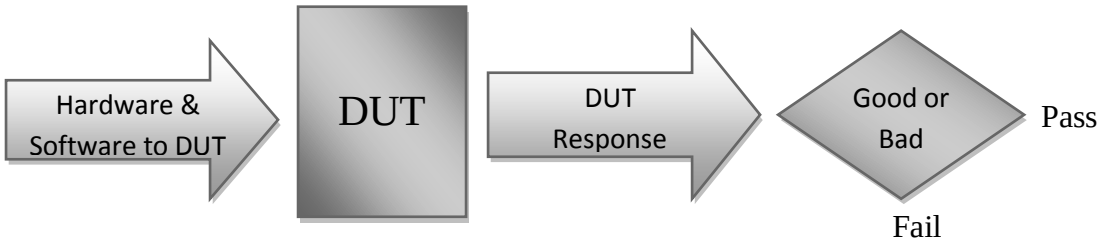

Figure-1.1 DUT response verification [1]

It is the responsibility of the test engineer to reduce the cost of the testing. It can be done by reducing the test time. The product engineer is also responsible to reduce the test cost. But the primary role of product engineer is related to the production of the new IC. The product engineer is the one who will help to identify the tester software defects, deign defects, process defects, and tester hardware defects and then helps to correct them.

1.2 THE IDEAL MODEL

To understand the basic behavior of the op-amp, it is necessary to consider it ideal. From practical point of view, ideal op-amp acts like an ideal VCVS (voltage controlled voltage source). Following are the characteristics [2] of the ideal op-amp:

1) There is no current at the input terminals of the op-amp that is I_p and I_n is zero. This means that the input resistance is infinite.
2) The output resistance is zero.
3) Open loop voltage gain is infinite.
4) Input offset voltage is zero.

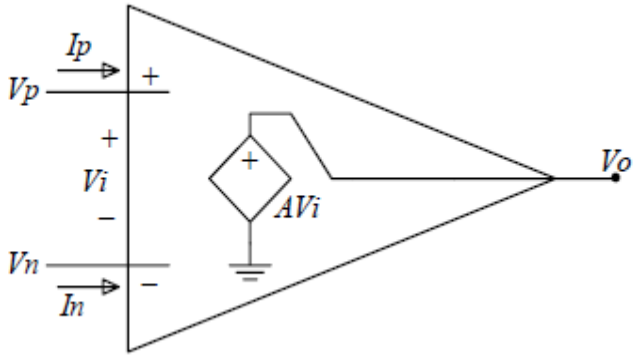

Figure-1.2 The ideal op-amp [2]

On summarizing we can say that:

$$I_p = I_n = 0 \quad \ldots (1)$$

$$R_i \to \infty$$

$$R_o = 0$$

$$A \to \infty$$

The output of the op-amp is given by the equation:

$$V_O = AV_i \quad \ldots (2)$$

Where, $V_O \rightarrow$ Output voltage of op-amp

$V_i \rightarrow$ Differential input voltage *i.e.* difference between non inverting and inverting input terminals

$A \rightarrow$ Open loop voltage gain

Some of the attributes of ideal op-amp are infinite Common Mode Rejection Ratio, infinite Power Supply Rejection Ratio and infinite bandwidth.

1.3 THE NON-IDEAL (REAL) OP-AMP

The characteristics of real op amp [2] are more complicated, of course. The inputs each have a dc current source (I_B) connected to them. A series dc voltage source (V_{OS}) appears in series with one input. Impedance (Z_{IN} diff) appears in between the inputs, and another (Z_{INCM}) appears between input and ground. These impedance usually consist resistance and capacitance in parallel, and the finite Z_{CM} will introduce errors due to common-mode input voltages.

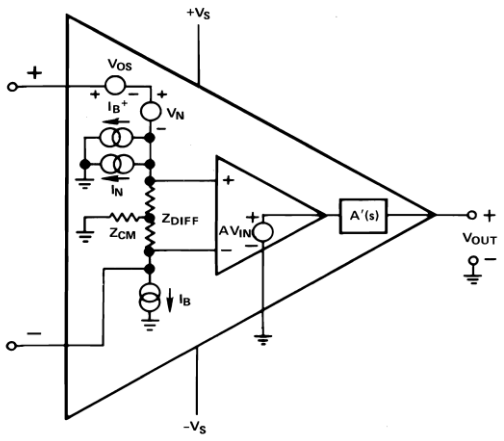

Figure-1.3 The real op amp [2]

There are two additional input error sources. In addition, the dc voltage and current sources representing the noise components (V_N, I_N) must be included in the model. The "A" term defining open loop voltage gain is finite and varies with frequency in a real amplifier. It is also obvious that the output voltage and the current capabilities of a real op amp are bounded. The real amplifier can be modeled as shown in fig.1.3.

The comparison of output and input voltage of the op-amp can be represented by the voltage transfer curve of the op-amp as shown on fig.1.4. The offset voltage is assumed to be zero.

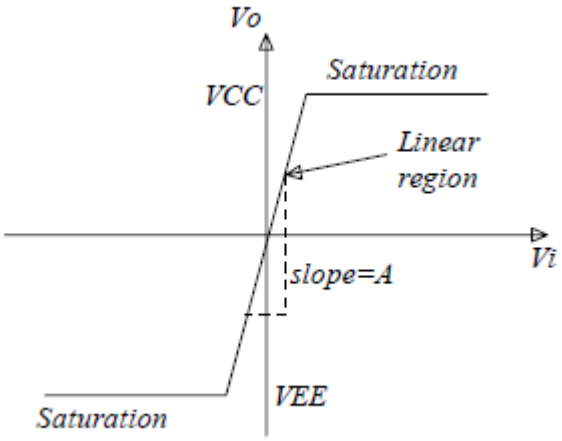

Figure-1.4 Voltage transfer curve of op-amp [3]

1.4 NEAGATIVE FEEDBACK IN OP-AMP

Negative feedback circuit can be obtained by connecting the inverting terminal of the op-amp to the output terminal of the op-amp. The two most fundamental negative feedback op-amp configurations are inverting amplifier and non-inverting amplifier.

1.4.1 Inverting Amplifier

If the input voltage signal is applied to the inverting input terminal of the op-amp then it is called inverting amplifier [3]. Input is applied through a resistance R1 and another resistance R2 is acting as a feedback resistance. The gain of this inverting amplifier can be found by using nodal analysis and virtual ground concept and is given by:

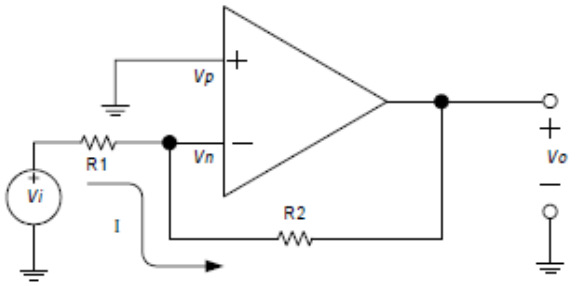

Figure-1.5 Inverting amplifier [3]

$$A_{CL} = -\frac{R_2}{R_1} \quad \ldots(3)$$

Where, the A_{CL} is closed loop gain. Output of the inverting amplifier is out of phase to the input.

1.4.2 Non-Inverting Amplifier

If the input voltage signal is applied to the non-inverting input terminal of the op-amp then it is called non-inverting amplifier [3]. Input voltage signal is directly connected to the non-inverting terminal. Feedback is still through the resistance R2. The gain of this inverting amplifier can be found by using nodal analysis and virtual ground concept and is given by:

$$A_{CL} = 1 + \frac{R_2}{R_1} \quad \ldots (4)$$

Where, the A_{CL} is closed loop gain. Output of the non-inverting amplifier is in phase to the input.

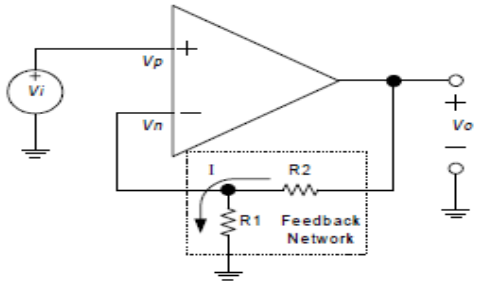

Figure-1.6 The non-inverting amplifier [3]

1.5 SPECIFICATIONS OF THE OP-AMP

The various op-amp specifications [4] are:

- Input offset voltage
- Bias current
- Open loop voltage gain
- Common mode rejection ratio
- Power supply rejection ratio
- Slew rate
- Settling time
- Gain bandwidth product

1.5.1 Offset Voltage

If both inputs of an op-amp are at zero volts or at the same voltages, the output of the op-amp should be zero. But, there exists a voltage at the output and that voltage is

known as the output offset voltage. This is because the difference between both the inputs of the op-amp is not zero. But practically, a small difference between the input terminals exists even when both the inputs are grounded or attached at same voltages. The presence of this error voltage is due to the mismatching between transistors in the internal circuit of the op-amp.

Typically input offset voltage V_{OS} can be defined as the negative of the voltage that must be applied at the input so that the output voltage is zero as shown in fig.1.7. The output offset voltage is the product of the input offset voltage and the dc gain of the circuit. For example if there is a amplifier having output offset voltage of 100 mV and the gain of the amplifier is 100 V/V then the input offset voltage is 1 mV.

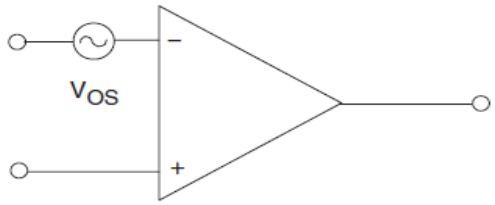

Figure-1.7 Op-amp input offset voltage [4]

1.5.2 Input Bias Current

According to the ideal characteristics of the op-amp there is no current at the input terminals of an op amp. Practically, this is not true and there exist small input current trough each of its terminals and known as input bias currents, I_{B+} and I_{B-} as shown in fig.1.8.

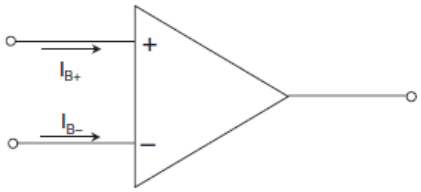

Figure-1.8 Op-amp input bias current [4]

In the data sheet of each op-amp I_B (input bias current) and I_{OS} (input offset current) is given. Input bias current is the average of two currents I_{B+} & I_{B-} and input offset current is the modulus of difference between the two currents I_{B+} & I_{B-}:

$$I_B = \frac{I_{B+} + I_{B-}}{2} \quad \ldots (5)$$

$$I_{OS} = |I_{B+} - I_{B-}| \quad \ldots (6)$$

When an Op-Amp is attached in a circuit then the bias current flows through the external impedances attached and produce an error voltage at the inputs which leads to the output offset voltage due to the bias current. For example, if op-amp is attached in a non-inverting unity gain buffer configuration having source impedance of 100 kΩ and the bias current of 100 nA then it will introduce a 10 mV output offset voltage due to the bias current.

1.5.3 Open-Loop Voltage Gain

As mentioned earlier op-amps have very high value of open-loop voltage gain generally referred as A_{OL} or A_V. Typically this value can vary between 100,000 to 1,000,000. It is illustrated in the fig.1.2. The gain can be defined by the equation (2) and can be calculated from the ratio of the output voltage to the differential input voltage as given by the following equation:

$$A = \frac{V_O}{V_i} \quad \ldots (7)$$

Where, $A \rightarrow$ Open loop voltage gain

$V_O \rightarrow$ Output voltage of op-amp

$V_i \rightarrow$ Differential input voltage *i.e.* difference between non inverting and inverting input terminals

Op-amps having both low and high open loop voltage gain exist. But, Op-Amps with low gain are not suitable in which high accuracy is required. Also open-loop gain varies with respect to the temperature. It can also vary from one device to another, so op-amp should have high gain for accuracy.

From basics of negative feedback, the high accuracy is maintained by high dc open-loop gain. The equation for the closed loop gain having a finite gain error is:

$$A_{CL} = \frac{1}{\alpha}\left[\frac{1}{1 + \frac{1}{A_{OL}\alpha}}\right] \quad \ldots (8)$$

Here, A_N (noise gain) = $1/\alpha$.

This equation can be written as:

$$A_{CL} = \frac{A_N}{1 + \frac{A_N}{A_{OL}}} \quad \ldots (9)$$

Where, Noise gain (NG) = Ideal closed loop gain = $\frac{1}{\alpha}$

Actual close loop gain is given by the equation:

$$A_{CL} = \frac{1}{\alpha}\left[\frac{1}{1 + \frac{1}{A_{OL}\alpha}}\right] = \frac{A_N}{1 + \frac{A_N}{A_{OL}}} \quad \ldots (10)$$

1.5.4 Common-Mode Rejection Ratio

The usefulness of the op-amp can be derived from the fact that how accurately and how much it can amplify the difference between applied input voltages. So, if the input voltages to both the terminals are changed in a way that the differential input is unchanged the output of the op-amp should not change. But the output voltage changes which is not desired. Input common to both the terminals such as noise should be rejected. Infect the ideal op-amp is the op-amp which can completely reject the CM (common mode) signals that's why they have infinite CMRR (common mode rejection ratio). The equation of the output voltage having both differential input voltage V_D and the common mode voltage V_{CM} can be written as:

$$V_O = A_D V_D + A_{CM} V_{CM} \quad \ldots (11)$$

Where, A_D → Differential voltage gain

A_{CM} → Common mode voltage gain

Ideally, A_{CM} should be zero and practically it should be as low as possible. The ability of the op-amp to reject the common mode changes is known as Common Mode Rejection Ratio, CMRR. CMRR can be defined as the ratio of the differential voltage gain to the common mode voltage gain [5] and is given by the equation:

$$\text{CMRR} = 20\log_{10}\left|\frac{\text{Differential voltage gain}}{\text{Common mode voltage gain}}\right| = 20\log_{10}\left|\frac{A_D}{A_{CM}}\right| \quad \ldots (12)$$

1.5.5 Power Supply Rejection Ratio

Ideally, the behavior of the op-amp should be independent to the power supply used that is if the power supply of the op-amp is changed the output voltage should not

change. Practically there is a change at the output voltage on changing the power supply this change is measured by a factor known as Power Supply Rejection Ratio, PSRR.

PSRR is defined as the ratio of the change in the power supply to the respective change at output voltage [5]. Due to any change in the power supply bias voltage changes which can lead to change in the offset voltage. So the PSRR is given by the equation:

$$\mathrm{PSRR} = 20\log_{10}\left|\frac{\Delta V_{\mathrm{Supply}\ \pm}}{\Delta V_{\mathrm{Offset}}}\right| = 20\log_{10}\left|\frac{\Delta V_{\mathrm{Supply}\ \pm}}{\Delta V_{\mathrm{Output}}} * A_V\right| \quad \ldots(13)$$

Where, $\Delta V_{\mathrm{Supply}\ \pm}$ → power supplies (both positive and negative) are changed symmetrically

$\Delta V_{\mathrm{Output}}$ → Change at output voltage

A_V → Close loop gain

1.5.6 Slew Rate

There are many applications which may require the output should change quickly from one level to another level, slew rate is an important parameter for those applications. The slew rate [4] can be defined as the maximum output voltage change per unit time as given by the equation:

$$\mathrm{SR} = \left.\frac{dV_0}{dt}\right|_{\max} \quad \ldots(14)$$

Slew rate can be measured by applying a step input to the Op-Amp connecting in the non-inverting buffer configuration. It is expressed in volts per second typically in V/ms or V/us. If a device has a slew rate of 1V/us, it means that the output voltage changes by 1V in 1us when an ideal step input is applied to the device. Slew rate may be different for negative and positive going transition. Slew rate should be as high as possible.

1.5.7 Settling Time

Settling time is defined as the time elapsed from the instance of the application of an ideal step input to the time at which the close loop amplifier output has entered into a

specified error band. The output must remain in that error band and should be symmetrical about the final value. Settling time is the summation of the propagation delay, the time for the output voltage to slew near to the final value, the time for the recovery from the overload condition due to slewing and finally the time required to settle within in the specified error band as shown in the fig.1.9.

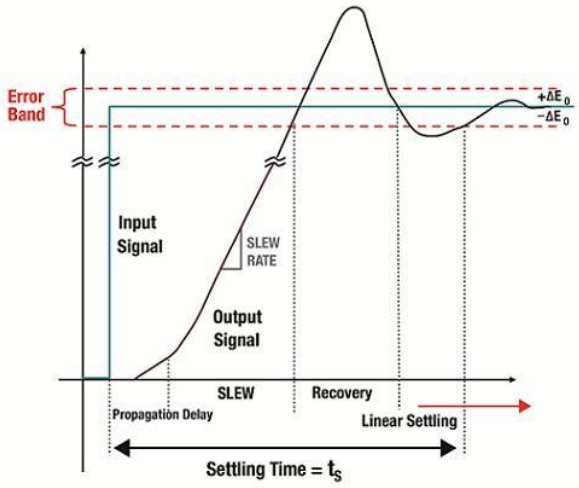

Figure-1.9 Settling time [4]

1.5.8 Gain Bandwidth Product

Gain bandwidth product (GBW) is defined as product of the gain and the bandwidth at which the bandwidth is measured. When the voltage gain is equal to 1, the GBW is known as the unity gain bandwidth product of the operational amplifier. The gain bandwidth product defines the op-amp gain behavior with respect to the frequency.

2

CHAPTER-2
LITERATURE REVIEW

Abundant literature exists on the measurement techniques of the specifications of the op-amp. Literature survey is divided in to four sections:

1. Oscillation based test methodologies.
2. Servo op-amp based test methodologies.
3. Self loop based test methodologies.
4. Neural network based test methodologies.

2.1 OSCILLATION BASED TEST METHODOLOGIES

In the oscillation based testing [6] there is no need of vectors to test the mixed signal and analog integrated circuits and this is a low cost technique. According to the previous research, OBT is generally used for the fault detection but later it is used for calculating the performance parameters of the DUT [6] - [10].

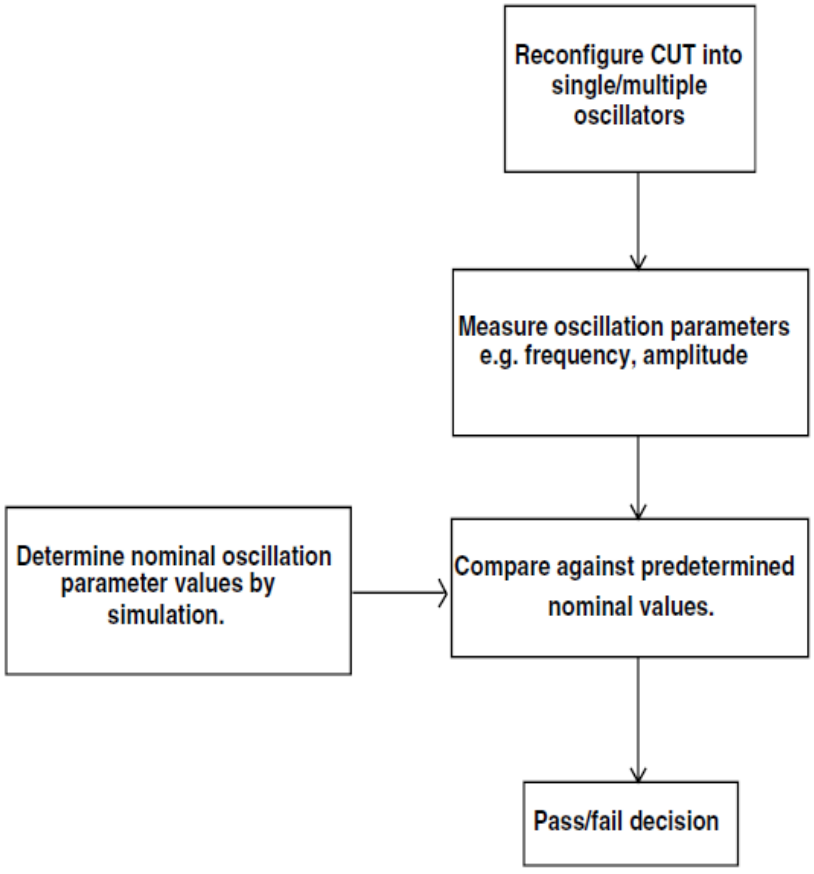

Figure-2.1 Traditional OBT methodology [6]

The traditional OBT procedure can be understood by the flow chart given in fig.2.1 and can be explained as:

1. The DUT is set to the oscillation mode using feedback. Feedback path may consist of non linear elements.
2. Oscillation parameter like amplitude limits and frequency of oscillation are calculated.
3. The DUT may be tested for different kinds of oscillation topologies to get accurate values for the oscillation parameters.
4. The measured and calculated values are compared with their nominal values. On the basis of comparison, decision can be made whether the DUT is good or bad.

The various papers using this method are discussed below.

2.1.1 A. Raghunathan, J. A. Abraham, "Prediction of analog performance parameters using oscillation based test," ***Proceedings. 22nd IEEE VLSI Test Symposium,*** **pp.377-382, April 2004.**

The main disadvantages of the OBT are discussed below:

1. The OBT is a less accurate method.
2. The nominal values used for comparison are not well defined.
3. OBT is used for fault detection not for finding the parameters of the DUT.

The above said disadvantages are overcome by the predictive oscillation based test (POBT) methodology is discussed in this paper [6]. The technique is self explanatory from the flow chart given in fig.2.2.

So the POBT increased the effectiveness of the OBT. There is no need of test stimulus. For verification purposes this technique is applied to the benchmark circuit of continuous time sate variable filter.

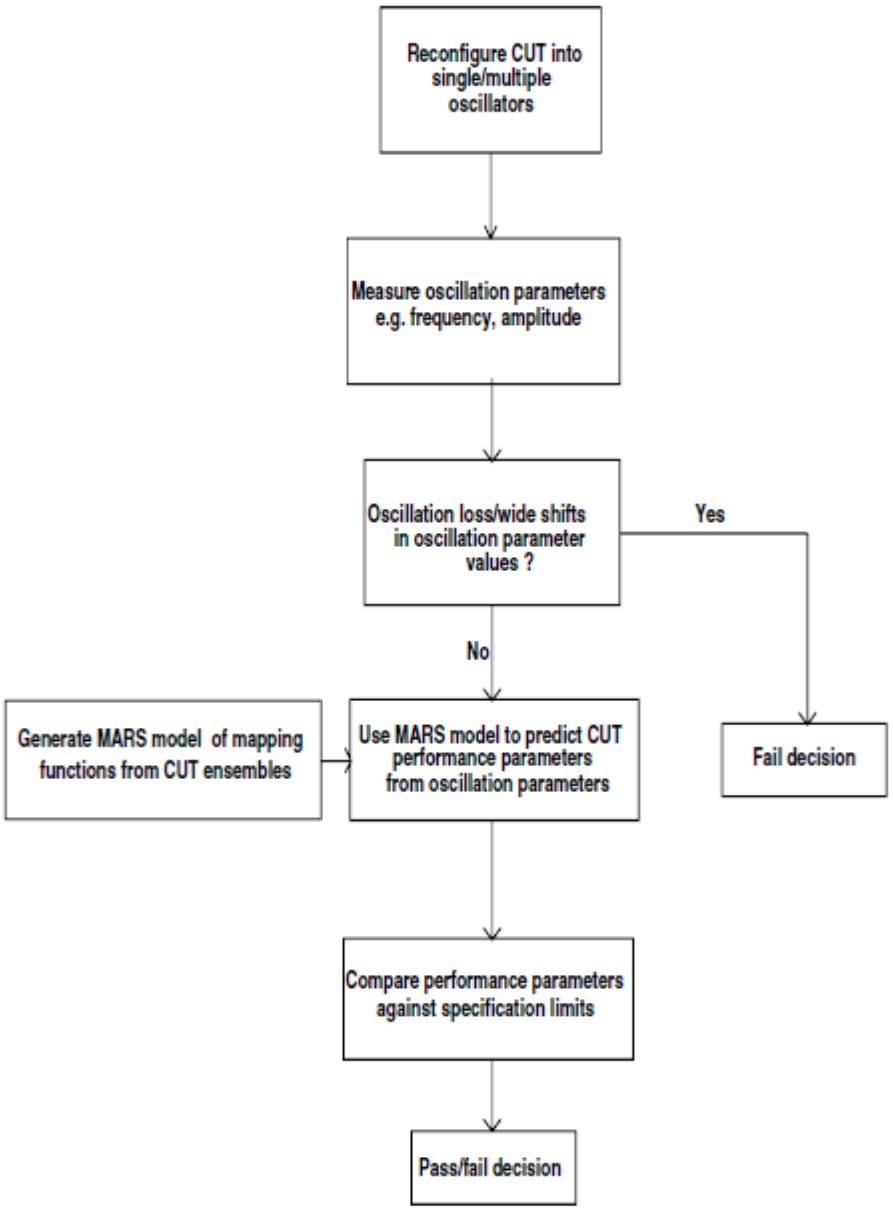

Figure-2.2 Predictive oscillation based test (POBT) methodology [6]

2.1.2 K. Suenaga, E. Isern, R. Picos, S.Bota, M. Roca, E. Garcia-Moreno, "Application of predictive oscillation-based test to a CMOS op-amp," *IEEE Trans. Instrum. Meas.*, vol. IM-59(8):2076–82, 2010.

In this paper [7] the POBT method is combined with the supply current monitoring to purpose a new method. The results obtained are excellent for measured performance parameters (like bandwidth, dc gain and slew rate) of the CMOS op-amp.

The main problem with the POBT is that it is quite a difficult task to set the DUT in the critical oscillation condition. The feedback network should be such that it can build the oscillation within a short duration of transient time. But this may lead to the

oscillations which are controlled by saturation of the circuit at power supply voltage. So the efficiency of performance can be reduced.

To overcome this problem the POBT is combined with supply current monitoring. The measurement setup is given in the fig.2.3.

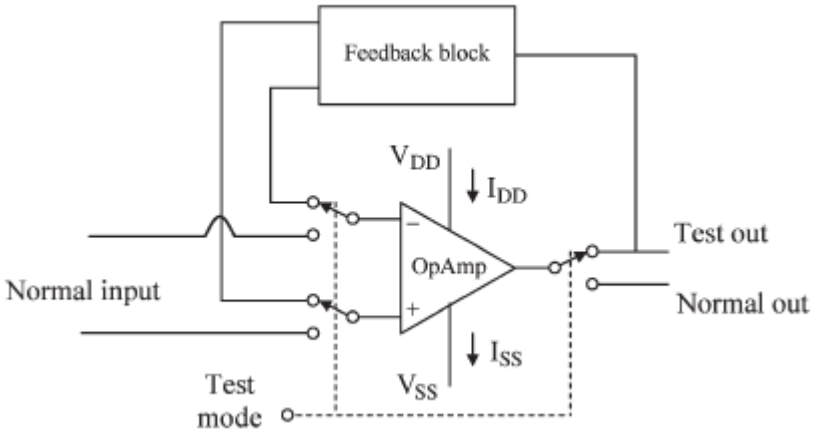

Figure-2.3 OBT strategy applied to an Op-Amp [7]

Oscillation parameters (like amplitude and frequency of oscillation) are the function of the internal parameters of the DUT as well as the external component used in the circuit. Later the comparison of the nominal values with the oscillation parameters are done as explained in the POBT.

2.1.3 R. Picos., Font-Rossello, J. Garcia-Moreno, E. Teruel, A. E., "Fast and accurate estimation of gain and unity-gain bandwidth of the op-amp," ***Electronics Circuits and Systems (ICECS), 19th IEEE International Conference On Digital Object Identifier*****: 10.1109/ICECS.2012.6463500.**

To increase the efficiency of the performance parameters Picos and Rossello [8] proposed a direct oscillation based test (DOBT) methodology to measure the parameters of the op-amp. According to the DOBT methodology it is not necessary to set the DUT in the critical oscillation condition which is itself a difficult task. DUT can be configured in the marginally saturated oscillations. Later the quiescent response can be sampled and analyzed to estimate the circuit performance parameters. This technique is more roust to parameter variation. The measurement setup is shown in the fig.2.4.

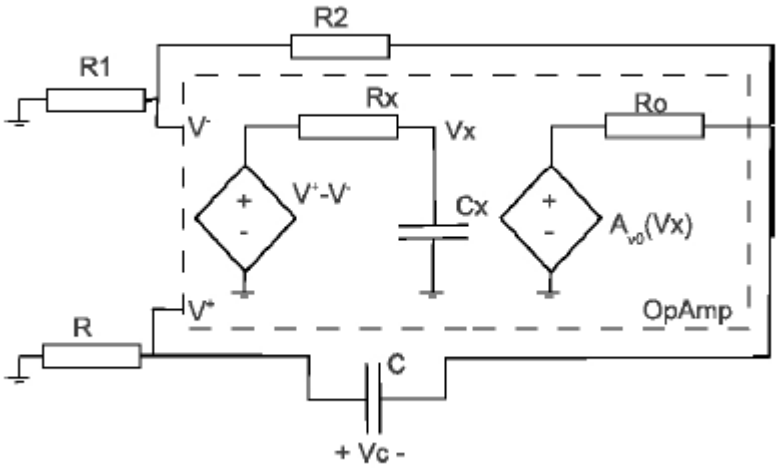

Figure-2.4 Oscillator circuit with the first order operational model [8]

Here they have shown the model of the op-amp having dc gain of A_{vo}, output resistance R_o and R_x & C_x as the position of the first pole. Other method to improve the efficiency of performance parameter is explained by Raghunaathan and Chatterjee [9] using quassi oscillation test (PQOBT) methodology.

2.1.4 B. K. Sharma, "Oscillation based test method of parameterization of open loop op-amp and its authentication," *International Journal of Electronics and Communication (AEU)*, vol. 68, NO. 7, pp- 595-601, July 2014.

This paper [10] uses the OBT technique by placing the DUT in the close loop sate variable filter as shown in fig.2.5.

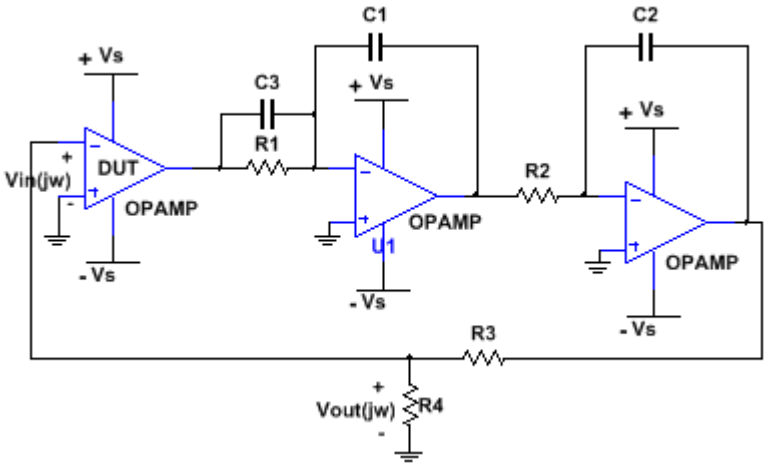

Figure-2.5 Modified state variable filter with dominant pole compensated by a zero [10]

The first stage that is the DUT itself is in the open loop configuration. In the second and third stage integrator are used. To make the system Linear, a zero $w_Z = \frac{1}{R_1 C_3}$ is introduced to compensate the effect of the effect of the dominant pole w_p of the DUT. Loop gain is adjusted by introducing the resistances as the attenuator in the feedback path.

When Vin(jw) is equal to the Vout(jw), the introduced zero has completely compensate the effect of the dominant pole of the DUT. At that oscillatory frequency Barkhausen criteria is fulfilled and oscillation frequency is given by:

$$w_{osc} = \sqrt{\frac{A_{VO} R_4}{R_1 R_2 C_1 C_2 (R_3 + R_4)}} \quad \ldots . (15)$$

2.2 SERVO OP-AMP BASED TEST METHODOLOGIES

In this type of methodology a servo op-amp is used in measurement circuits. The various papers using this methodology are discussed below.

2.2.1 K. Higuchi and H. Shintani, "New measurement methods of dominant pole-type operational amplifier parameters," *IEEE Trans. Ind. Electron*., vol. IE-34, pp. 357–365, June 1987.

Every integrated circuit is provided with a data sheet which is given by the manufacturer. In these data sheets various specifications of the device are given. Generally in all the applications the operating conditions of the device is not same as those of the given in the data sheets. So the designers should know about the performance of the device under different operating conditions and the tolerance of the device must be known.

According to this paper various other methods which are already presented to measure the characteristics of the op-amp are time consuming cumbersome and since they need wide range measurement including voltage, current, frequency, offset current and so on. There are few parameters of the op-amp which are enough to explain the characteristics of the op-amp so that the designer can measure what they need according to their application requirement. These few parameters are the dominant

pole frequency f_C, transition frequency f_T, open loop gain, input offset voltage, input bias current and so on.

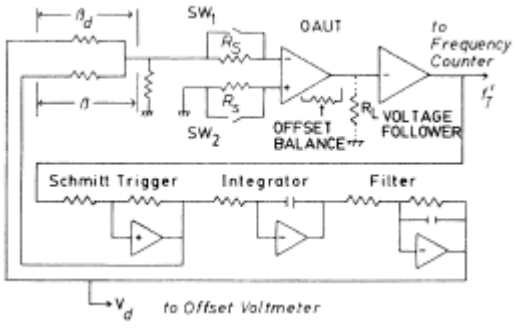

Figure-2.6a Measurement circuit for f_T [11]

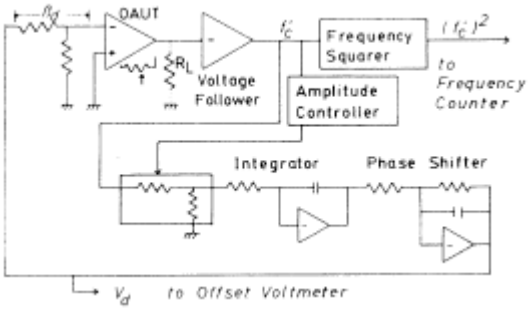

Figure-2.6b Measurement circuit for f_C [11]

In this paper [11], a new technique of measurement for the above said parameters is presented for the dominant pole type op-amp. The circuit used for the measurement of f_T and f_C are shown in the figure-2.6a and figure-2.6b. The open loop gain of the DUT can be measured by using the circuit shown in the fig.2.7.

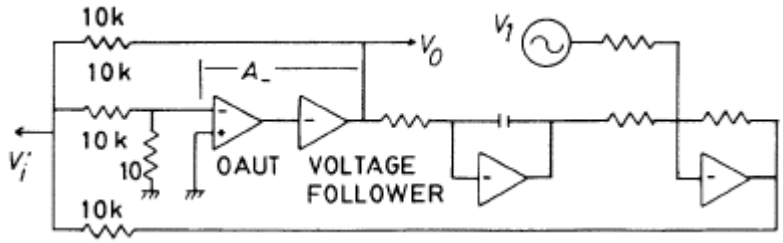

Figure-2.7 Measurement circuit for open loop gain [11]

The open loop gain is given by the equation:

$$A = 10^3 * \frac{V_0}{V_i} \quad \ldots (16)$$

2.2.2 M. E. Brinson and D. J. Faulkner, "New approaches to measurement of operational amplifier common-mode rejection ratio in the frequency domain," *Proc. Inst. Elect. Eng., Circuits Devices Syst.*, vol. 142, no. 4, pp. 247–253, 1995.

In this paper [16] CMRR of the DUT is measured for the four different kinds of the test circuits. The complete analysis of how differential and common mode input resistance and input capacitances affecting the circuit has been shown.

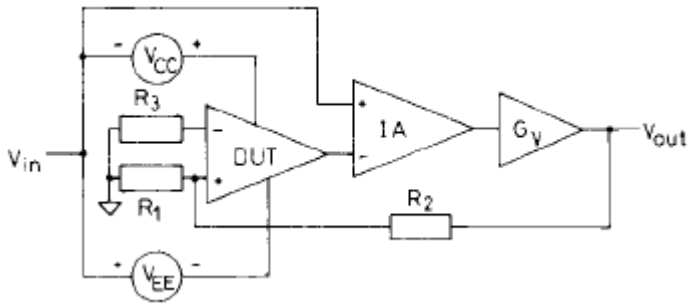

Figure-2.8 Power supply servo test circuit [16]

The comparison of the results of all four techniques is provided. Improvement on some of already existing test circuit is also shown. One of the test circuit named power supply servo test circuit is shown in the fig.2.8.

2.2.3 G. Giustolisi, G. Palmisano, and G. Palumbo, "CMRR frequency response of CMOS operational transconductance amplifiers," *IEEE Trans. Instrum. Meas.*, vol. 49, pp. 137–143, Feb. 2000

In this paper [17] the analysis of CMRR for the operational trans-conductance amplifier OTA has been carried out. The analysis of four different kinds of OTA's is provided and the comparison of the simulated and the calculated values has been shown. The analysis provides us the equations of the CMRR which are functions of different parameters and those equations can help us to design the high accuracy integrated circuits.

The conclusion derived in this paper tells us that CMRR is affected by the two poles and those poles are due to the zeros of the common mode gain.

2.3 SELF LOOP BASED TEST METHODOLOGIES

In this type of methodology only single op-amp that is the DUT itself is used along with other external components like resistances and capacitances in the feedback path. That means there is no servo op-amp in the measurement circuit. However, in the feedback path an Op-Amp can be used. Various papers using this type of methodology are discussed below.

2.3.1 W. M. C. Sansen, M. Steyaert, and P. J. V. Vandeloo, "Measurement of operational amplifier characteristics in the frequency domain," *IEEE Trans. Instrum*. Meas., vol. IM-34, pp. 59–64, Feb. 1985

The op-amp is used very commonly in almost all linear integrated circuit applications. Generally it is assumed that the op-amp to be ideal in most of the designs. For an example, it is assumed that the gain of the op-amp is very high. But this assumption is true only at low frequencies. However, at high frequencies the gain of the op-amp is decreased so that it can be conditionally stable. To sort out this problem various kind of the phase compensation techniques are used.

In this paper [18], the small signal analysis of the already used test circuits has been presented. According to the small signal analysis, at low frequencies output impedance has no influence on the open loop gain but at high frequencies the output impedance becomes significant and reduces the gain. So the measurement techniques are affected by the output impedance of the op-amp.

To overcome the above said problem a new test circuit has been presented as shown in the fig.2.9. Due to output impedance the input signal is feed through via the feedback resistance. To eliminate this buffer is used in the feedback as shown in the fig.2.9. A fit routine is also developed in this method by using that various parameters like open loop gain, phase margin, unity gain bandwidth, common mode rejection ratio and power supply rejection ratio can be measured.

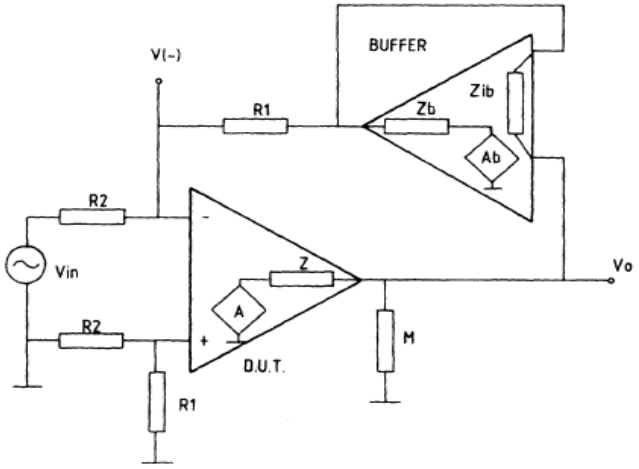

Figure-2.9 Test circuit with buffer [18]

2.3.2 R. Pintelon, G. Vandersteen, L. DeLocht, Y. Rolain, and J. Schoukens, "Experimental characterization of operational amplifiers: A system

identification approach—Part I: Theory and simulations," ***IEEE Trans. Instrum. Meas.*****, vol. 53, June 2004.**

In this paper a system identification approach is presented for the modeling of the linear op-amp characteristics. This paper is presented in two parts [19] – [20] part-1 and part-2.

PART-1: In part-1 of the series of the two papers a simple method of measurement is proposed that can simultaneously measure the type of the non linearity (odd or/and even degrees of distortion), op-amp characteristics and the level of non linear distortion. Part-1 tells us about the implementation of theory on to the simulations and the modeling approach.

The proposed circuit is shown in the fig.2.10. It is a kind of matched resistor based circuit. In this method [19], periodic random excitation signals are being used. The advantage of periodic random excitation signals is that they can provide us the level of the non linearity, the class (odd or even), the noise level and the frequency response function in one single measurement. By averaging the frequency response function of the different periodic random excitation signals the variance can be measured which gives us the estimated parameter value.

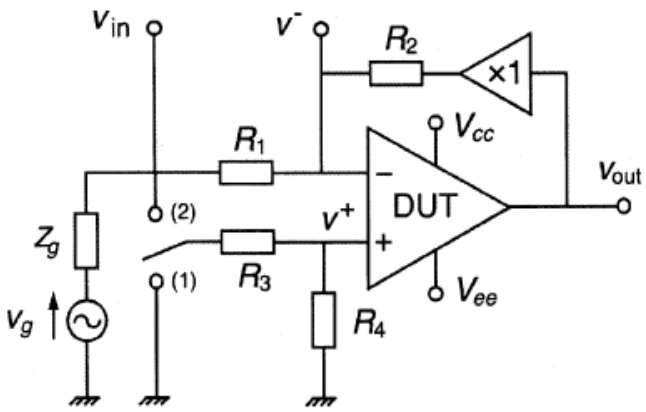

Figure-2.10 Basic scheme for measuring the characteristics of an op-amp [19]

Two kind of measurement techniques are given n this paper. The first one makes use of the single phase realization and the second one uses the multiple phase realizations. First technique is useful only for open loop gain and the second technique is useful for open loop gain, CMRR, PSRR.

PART-2: Part-2 [20] tells us about the implementation of the theory on the real measurements and the calibration of the measurement setup. Three extra ideal buffers having infinite input impedance and zero output impedance are used on the measurement probes as shown in the fig.2.11. The various parameters can be measured as:

1. Open loop gain can be measured when $v_g \neq 0$ and switch at position-1.
2. CMRR can be measured when $v_g \neq 0$ and switch at position-2.
3. PSRR can be measured when $v_g = 0$ and switch at position-2.

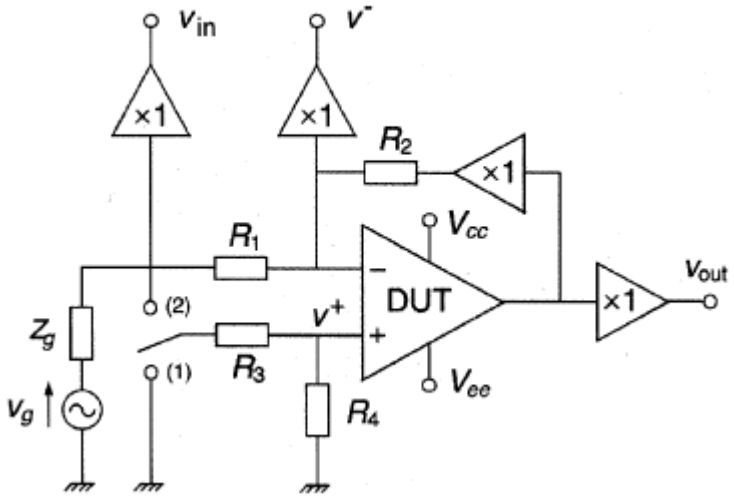

Figure-2.11 Actual measurement setup for the characteristics of an op-amp [20]

2.3.3 R. Pallás areny,J. G.webster, "Common mode rejection ratio in differential amplifiers," *IEEE Trans. Instrum. Meas.*, vol. 40, pp. 669–676, June 1991.

Areney and Webster [21] have given the CMRR of the differential amplifier using a single op-amp and instrumentation amplifier using three operational amplifiers. The circuit for the differential amplifier is as shown in fig.2.12.

The op-amp here is considered to be non-ideal so the equation of the output is:

$$V_O = A_{CM}\frac{(V_b' + V_a')}{2} + A_{OL}(V_b' - V_a') \quad \ldots(17)$$

$$V_O = G_C V_C + G_D V_D \quad \ldots(18)$$

G_D and G_C are the functions of external resistances, A_{OL} & A_{CM} and can be calculated which will give the value of the CMRR by the equation:

$$\text{CMRR} = \frac{G_D}{G_C} \qquad \ldots (19)$$

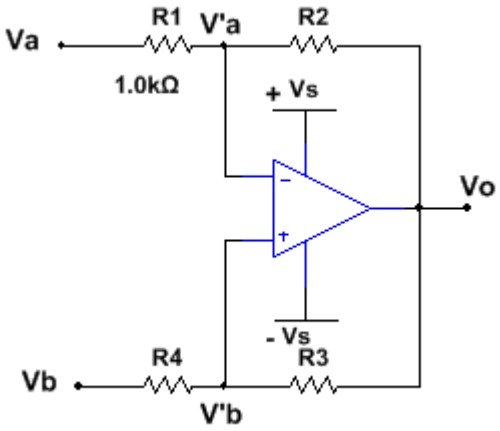

Figure-2.12 Measurement setup for CMRR [21]

2.3.4 Jian Zhou and Jin Liu, "On the measurement of common-mode rejection ratio," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 52, NO. 1, January 2005.

In this paper [22], the CMRR is calculated for several existing test circuits. Comparison of the results between these used test setups and the definition of the CMRR is carried out and the discrepancies are highlighted. Advantages and disadvantages of the existing test circuit have been told. A new test circuit has been proposed for the measurement of the CMRR as shown in the fig.2.13.

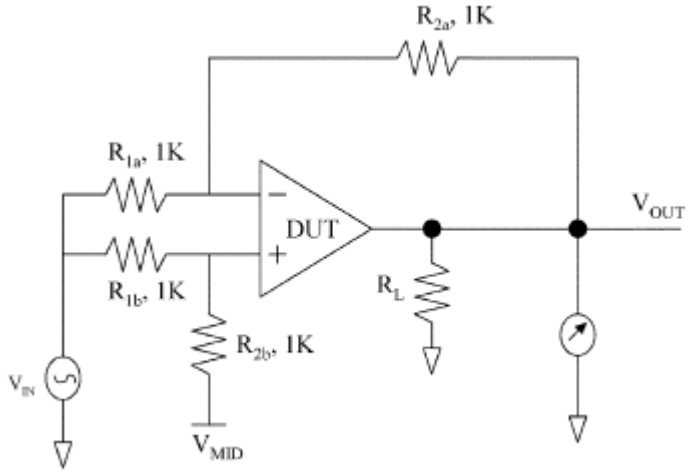

Figure-2.13 Matched resistor measurement setup for CMRR [22]

Resistor R_{1a} & R_{1b} are matched and resistor R_{2a} & R_{2b} is matched. V_{MID} is connected to ground for the simplicity.

2.4 NEURAL NETWORK BASED TEST METHODOLOGIES

Neural network models are used for the synthesis of the analog circuits. The one of the main advantage using this technique is that they are very fast and reasonably accurate and they are completely automated.

2.4.1 G. Wolfe and R. Vemuri, "Extraction and use of neural network models in automated synthesis of operational amplifiers," ***IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,*** **vol. 22, no. 2, Februray 2003.**
Particularly in this paper [24], the neural network based technique is used to create models (which are fast and accurate) for estimating the parameters of CMOS op-amp. Genetic algorithm based system is used for demonstrating the accuracy and efficiency of the performance models.

For the purpose of validation the performance parameters that are estimated by using this technique are compared with the results of the circuits that are simulated using SPICE. The main drawback of this technique is that it requires a large number of samples and as the number of parameters increasing the samples are increasing exponentially.

Performance parameters describing the functionality of the Op-Amp are calculated from the ac and the transient simulations of the corresponding circuit topology. The transistor sizes of the Op-Amp are varied and for many combinations of these varied values, training and the validation data sets are created using SPICE simulations. By using the training data set a neural network model is developed. The Op-Amp or the DUT is synthesized by using a genetic algorithm. The neural network model developed above is used to estimate the performance parameters. Then the above calculated performance parameters are compared with those calculated directly from simulations using the validation data set. The whole process is an iteration based process.

3

CHAPTER-3
MEASUREMENT USING SELF TEST LOOP

The complete analysis and methodology and then the results are discussed for the self loop test circuit [26].

3.1 ANALYSIS AND METHODOLOGY

Where engineers once needed only a single circuit to thoroughly test all DC characteristics of an op-amp today's op-amp have far better specification that require several circuit configuration. Here, the self test loop topology as shown in fig.3.1 is discussed, which is widely used to measure the open loop gain of the DUT. The open loop gain is simulated using the SPICE.

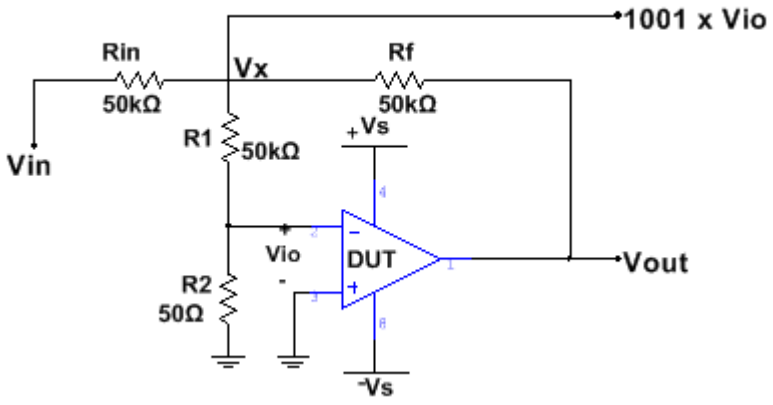

Figure-3.1 Two-op-amp test loop [16]

Open Loop DC Voltage Gain, A_{OL}

A_{OL} is defined as the ratio of the output voltage to the difference between the input voltages. For the measurement of A_{OL}, the output behavior of the DUT should be known in advance. According to the ideal characteristics of the op-amp the output voltage of the op-amp should swing from the minimum value of the power supply voltage to the maximum value of the power supply voltage. But practically this is not true. The output swing voltage is less than the power supply. So it is necessary to measure the output swing voltage for the measurement of the A_{OL}.

Assume that the output voltage swings from the V_{OUT} (neg) to V_{OUT} (pos). If the output voltage of the test circuit is set to V_{OUT} (pos) by varying the applied input voltage then the voltage at the input of the DUT will be V_{IN} (pos) + V_{OS}. The V_{OS} is the input offset voltage required to bring the output voltage of DUT to zero and the V_{IN} (pos) is the small component of the applied input voltage required to drive the output voltage of the DUT to V_{OUT} (pos).

Similarly, if the output voltage of the DUT is set to V_{OUT} (neg) then the value of the voltage at the input of the DUT will be V_{IN} (neg) +V_{OS}. V_{IN} (pos) - V_{IN} (neg) is the differential input voltage for the full scale output voltage. The complete method to measure the A_{OL} is given below:

1. For the test procedure the load is attached to the DUT.

2. V_{IN} is forced to derive the output of the DUT to the measured value of V_{OUT} (pos).

3. V_X (1) is measured, which is: 1001*(V_{OS} + V_{IN} (pos)). Therefore V_{IN} (pos) is given by:

$$V_{IN}(\text{pos}) = \left(\frac{V_X(1)}{1001}\right) - V_{OS} \quad \ldots(20)$$

4. V_{IN} is forced to derive the output of the DUT to the measured value of V_{OUT} (neg).

5. V_X (2) is measured, which is: 1001 * (V_{OS} + V_{IN} (neg)). Therefore V_{IN} (neg) is given by:

$$V_{IN}(\text{neg}) = \left(\frac{V_X(2)}{1001}\right) - V_{OS} \quad \ldots(21)$$

6. A_{OL} is calculated as:

$$A_{OL} = 20 * \log\left(\frac{V_{OUT}(\text{pos}) - V_{OUT}(\text{neg})}{V_{IN}(\text{pos}) - V_{IN}(\text{neg})}\right) \quad \ldots(22)$$

7. By substituting the values measured for $V_{IN}(pos)$ and $V_{IN}(neg)$, A_{OL} can be written as:

$$A_{OL} = 20 * \log\left(\frac{V_{OUT}(pos) - V_{OUT}(neg)}{\left(\frac{V_X(1)}{1001}\right) - V_{OS} - \left(\left(\frac{V_X(2)}{1001}\right) - V_{OS}\right)}\right) \quad \ldots(23)$$

8. It can be noted that V_{OS} drops out of the equation and A_{OL} can be written as:

$$A_{OL} = 20 * \log\left(\frac{V_{OUT}(pos) - V_{OUT}(neg)}{\left(\frac{V_X(1)}{1001}\right) - \left(\frac{V_X(2)}{1001}\right)}\right) \quad \ldots(24)$$

Hence, gain is calculated.

To calculate open loop voltage gain, self test loop as in fig.3.1 is used. Simulations are performed using SPICE via the computer aided design tool MULTISIM. U741 and TLV2772CP models of op-amp are used in MULTISIM to perform various simulations to calculate open loop gain. U741 is an integrated circuit (IC) of bipolar junction transistor (BJT) op-amp where as TLV2772CP is an IC of complementary metal oxide semiconductor (CMOS) op-amp.

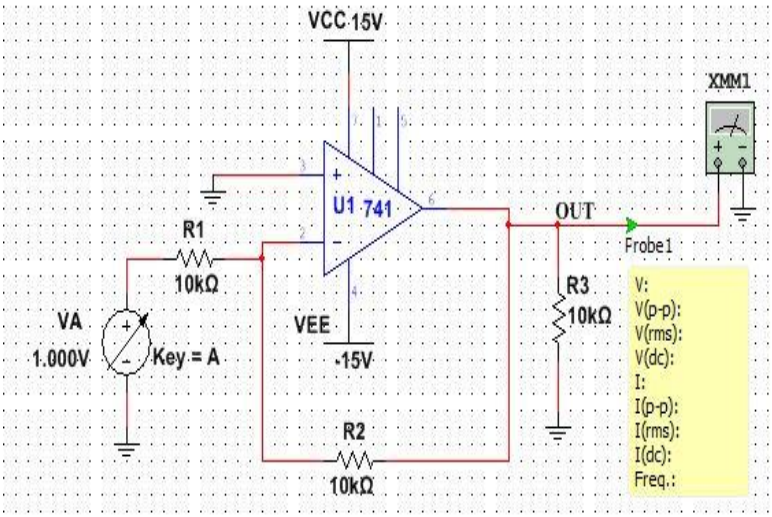

Figure-3.2a Voltage swing measurement for U741

To calculate open loop voltage gain voltage swing is required. This is obtained by connecting DUT in the negative feedback configuration. The circuit simulated on MULTISIM for the maximum output voltage V_{OUT} (pos) and minimum output

voltage V_{OUT} (neg) of U741 and TLV2772CP is shown in fig.3.2a and fig.3.2b respectively.

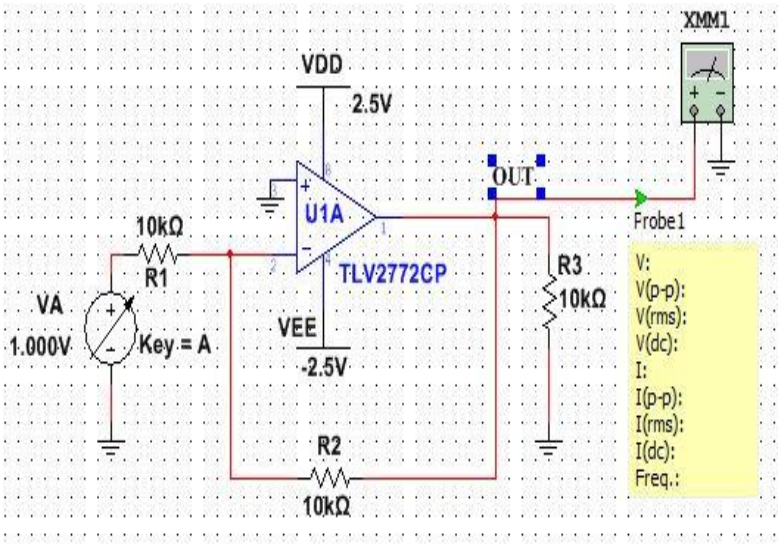

Figure-3.2b Voltage swing measurement for TLV2772CP

The input voltage V_{IN} is set for the measured value of maximum output voltage V_{OUT} (pos). For that input voltage, the voltage at node x that is V_X (1) is measured by simulating the self test loop circuit shown in fig.3.3a. Similarly the input voltage V_{IN} is set for the measured value of minimum output voltage V_{OUT} (neg) and for that V_{IN} voltage at node x V_X (2) is measured. Open loop voltage gain is measured by the using the equation (24).

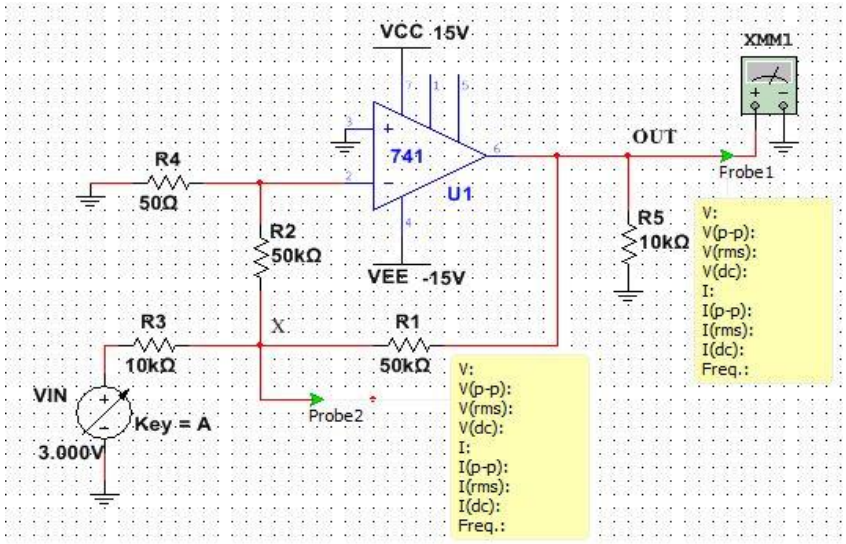

Figure-3.3a Self test loop for BJT based Op-Amp

Self loop test circuit used for TLV2772CP is shown in fig.3.3b. The value of 50Ω resistance is changed to 500Ω because large voltage drop is required at non-inverting input terminal of operational amplifier to drive it in positive and negative saturation. The input voltage V_{IN} is set for the measured value V_{OUT} (pos). For that input voltage, the voltage at node x that is $V_X(1)$ is measured by simulating the self test loop circuit shown in fig.3.3b. Similarly the input voltage V_{IN} is set for the measured value of minimum output voltage V_{OUT} (neg) and for that V_{IN} voltage at node x V_X (2) is measured.

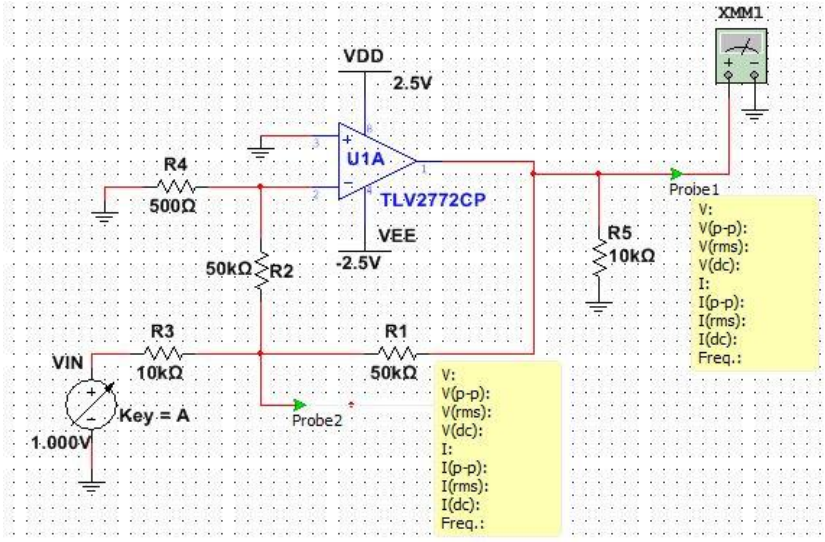

Figure-3.3b Self test loop for CMOS based Op-Amp

The equation of V_X for this circuit is also changed due to change in the ratio of the resistances R2 and R4. The equations of $V_X(1)$ and $V_X(2)$ for these new ratios are given below:

$$V_X(1) = 101 * \left(V_{OS} + V_{IN}(pos)\right) \quad \ldots(25)$$

$$V_X(2) = 101 * \left(V_{OS} + V_{IN}(neg)\right) \quad \ldots(26)$$

The value of open loop voltage gain is calculated by using equation written below:

$$A_{OL} = 20 * \log\left(\frac{V_{OUT}(pos) - V_{OUT}(neg)}{\left(\frac{V_X(1)}{101}\right) - V_{OS} - \left(\left(\frac{V_X(2)}{101}\right) - V_{OS}\right)}\right) \quad \ldots(27)$$

3.2 RESULTS AND DISCUSSIONS

In this the results for the voltage swing and open loop dc gain is shown. Comparison between the simulated and the values taken from data sheet has been done.

3.2.1 Voltage Swing

Maximum output voltage V_{OUT} (pos) and minimum output voltage V_{OUT} (neg) for U741 and TLV2772CP is obtained by simulating the circuit shown in fig.3.2a and 3.2b respectively. The plots are shown below in fig.3.4a and 3.4b. The measured values are shown in Table-3.1.

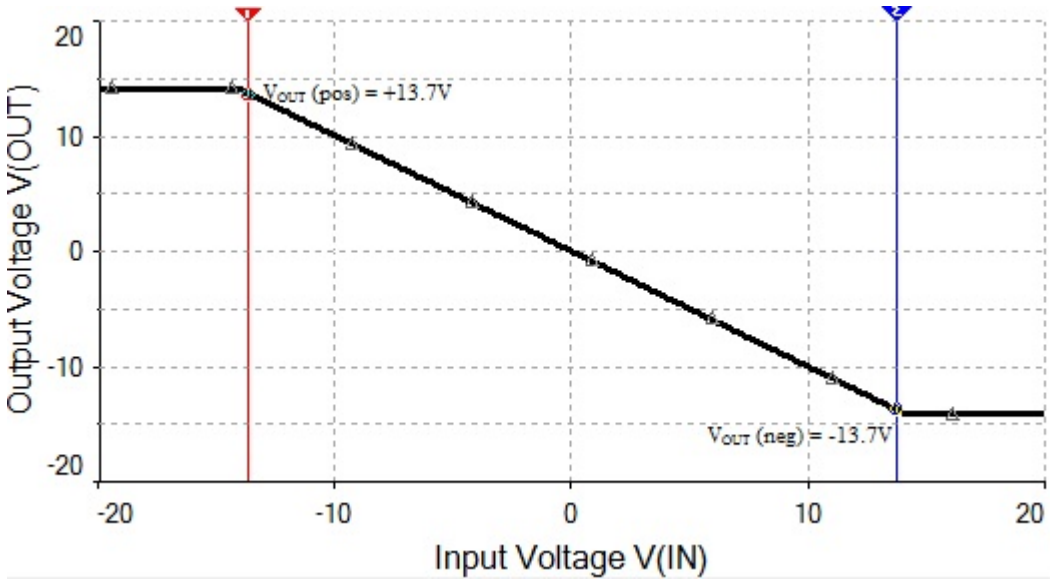

Figure-3.4a Voltage swing of U741

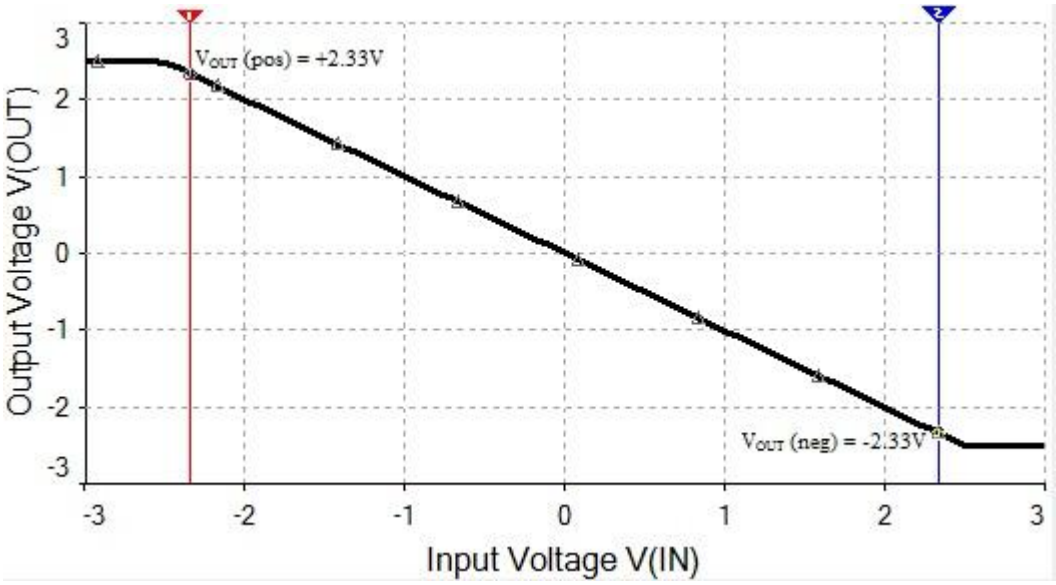

Figure-3.4b Voltage swing of TLV2772CP

Table-3.1 Maximum and Minimum Output Voltages

parameters	U741	TLV2772CP
V_{OUT} (pos)	+13.7	+2.33
V_{OUT} (neg)	-13.7	-2.33

3.2.2 Open Loop dc Gain

The values of V_X (1) and V_X (2) are obtained by simulating the self test loop circuit for U741 and TLV2772CP shown in fig.3.3a and 3.3b respectively. The plots are shown below in fig.3.5a and 3.5b. The measured values are shown in Table-3.2.

The DC open loop gain A_{OL} for U741 can be calculated by using the values from Table-3.1 & Table-3.2 in the equation (24) as shown:

$$A_{OL} = \frac{V_{OUT}(pos) - V_{OUT}(neg)}{\left(\frac{V_X(1)}{1001}\right) - \left(\frac{V_X(2)}{1001}\right)} \quad \ldots(28)$$

$$A_{OL} = \frac{13.7 - (-13.7)}{\frac{0.963}{1001} - \frac{1.10}{1001}} \quad \ldots(29)$$

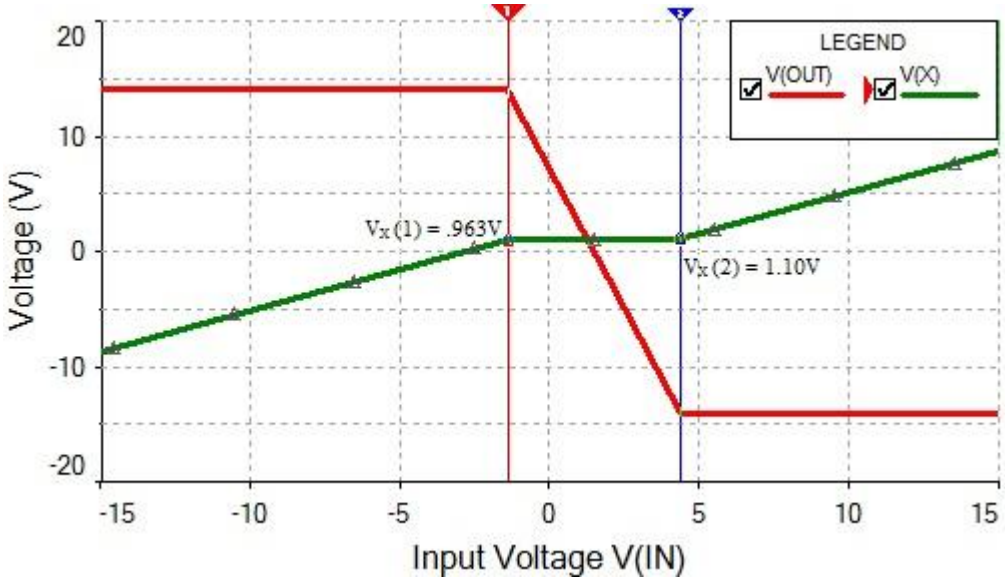

Figure-3.5a Voltage at Node x that is V_X for U741

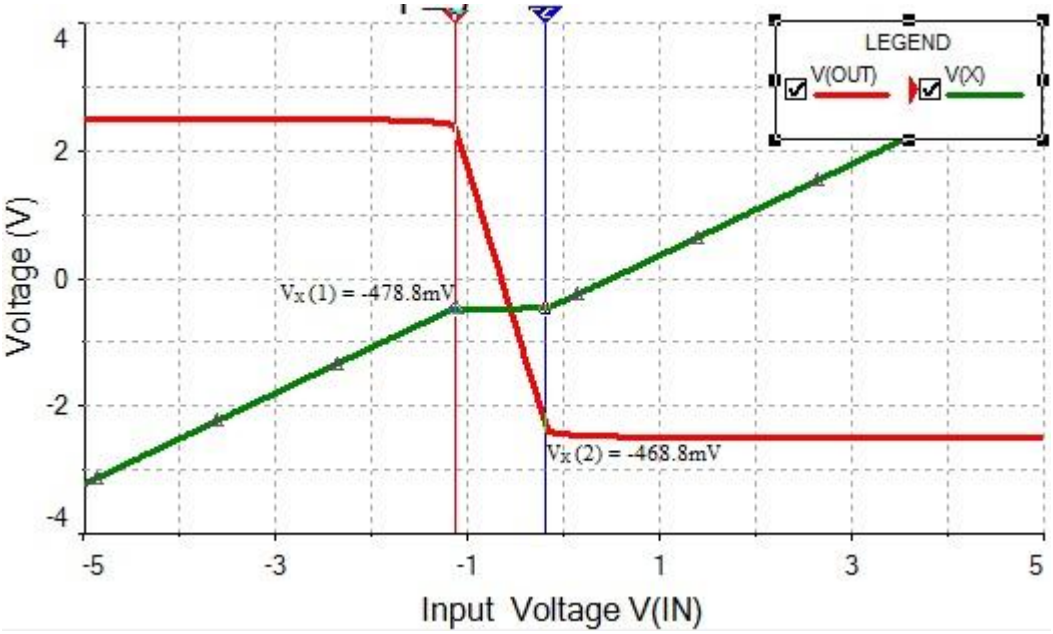

Figure-3.5b Voltage at Node x that is V_X for TLV2772CP

Table-3.2 Voltages at Node x that is V_X

Parameters	U741	TLV2772CP
$V_X(1)$	+0.963V	-478.8mV
$V_X(2)$	+1.10V	-468.8mV

$$A_{OL} = -195{,}000 \quad \ldots.(30)$$

The DC open loop gain A_{OL} for TLV2772CP can be calculated by using the values from Table-1 & Table-2 in the equation (27). The equation (27) and can be written as:

$$A_{OL} = \frac{V_{OUT}(pos) - V_{OUT}(neg)}{\left(\frac{V_X(1)}{101}\right) - \left(\frac{V_X(2)}{101}\right)} \quad \ldots(31)$$

$$A_{OL} = \frac{2.33 - (-2.33)}{\frac{-0.473}{101} - \frac{-0.468}{101}} \quad \ldots(32)$$

$$A_{OL} = -23{,}530 \quad \ldots(33)$$

The comparison of the electrical parameters calculated from simulations and the parameters from the datasheet of both U741 and TLV2772CP is shown in Table-3.3.

Table-3.3 Comparison of electrical parameters

Electrical parameters	U741 Power supply ±15 R_L=10K		TLV2772CP Power supply ±2.5 R_L=10K	
	Values from datasheet	Values from simulations	Values from datasheet	Values from simulations
Maximum and minimum output voltages	±14v	±13.7v	±2.4v	±2.33v
Open loop gain	(50-200)v/mv	195v/mv	(20-380)v/mv	23.5v/mv

CHAPTER-4

MEASUREMENT USING SERVO OP-AMP

4.1 METHODOLOGY

In this chapter, the two Op-Amp based test loop or the servo op-amp based test methodology is used to calculate the open loop gain, CMRR and PSRR. An improved circuit is also proposed to measure the open loop gain, CMRR and PSRR and comparison between the results of the old and the proposed circuit is shown.

4.1.1 Open loop dc gain (A_{OL}) measurement

Open loop gain, A_{OL} is defined as the ratio of the output voltage to the difference between the input voltages. The gain of the operational amplifiers is very large order of 10^6. If the gain of the op-amp is measured in the open loop configuration, the input voltage needed will be in order of micro-volts. At such a small input level there can be errors due to the stray currents, pickup or the seedback effect. The input voltage may change due to these errors so the open loop gain cannot be measured directly. That is why; it is preferable to measure the gain in close loop configurations.

The basic servo op-amp based test circuit [27] used for measurement is shown in the fig.4.1. The non-inverting input of the servo amplifier is attached to the loop voltage (V1 in the fig.4.1). If the loop voltage is set at a particular voltage then the servo op-amp will try to make the other input (inverting terminal of servo op-amp) to the same voltage by varying its output.

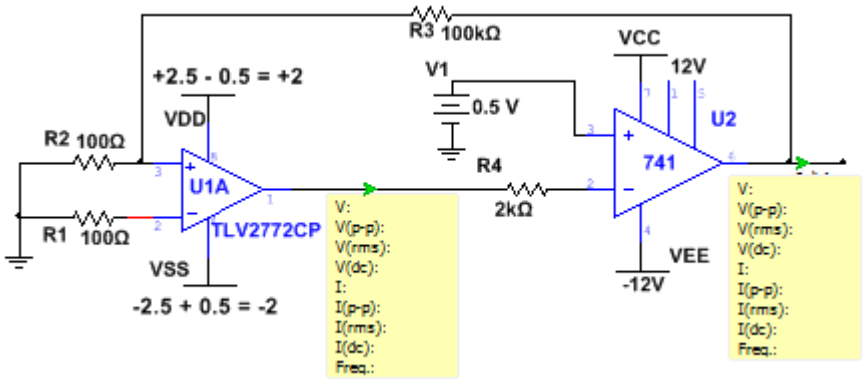

Figure-4.1 A_{OL} using Servo op-amp based test circuit [28]

This property can be used to calculate the open loop gain of the DUT. If the change at the output voltage is known in advance then by measuring the change at the input of the DUT for the known change at output, gain can be obtained by dividing the change at output to the change at input. Following are the steps to calculate gain:

- Loop voltage (V1) is fixed at 0.5V then the output of the DUT, V_{OUT} (1) will be 0.5V.
- Measure the output voltage $V_{O\ servo}(1)$ of the servo op-amp.
- Again the loop voltage (V1) is fixed at 1.5V then the output of the DUT V_{OUT} (2) will be 1.5V.
- Again measure the output voltage $V_{O\ servo}(2)$ of the servo op-amp.
- Open loop voltage gain is given by the equation:

$$A_{OL} = \frac{V_{OUT}(2) - V_{OUT}(1)}{V_{IND}^{+}(2) - V_{IND}^{+}(1)} \quad \ldots(34)$$

  Where, V_{IND}^{+} → is the voltage at non-inverting terminal of the DUT.

- Relation between the output of the servo amplifier and the input voltage of the DUT is given by:

$$V_{IND}^{+} = V_{O\ servo} * \frac{100}{100 + 100k} \approx \frac{V_{O\ servo}}{1000} \quad \ldots(35)$$

- By using equation (35) in equation (34) A_{OL} can be written:

$$A_{OL} = \frac{V_{OUT}(2) - V_{OUT}(1)}{\frac{V_{O\ servo}(2)}{1000} - \frac{V_{O\ servo}(1)}{1000}} \quad \ldots(36)$$

- Finally gain can be written as:

$$A_{OL} = \frac{V_{OUT}(2) - V_{OUT}(1)}{\left(V_{O\ servo}(2) - V_{O\ servo}(1)\right) * \alpha} \quad \ldots(37)$$

  Where, α → Attenuation factor

  V_{OUT} → Voltage at the output of the DUT

  $V_{O\ servo}$ → Voltage at the output of the servo op-amp

The basic servo Op-amp based methodology has a drawback that is the input voltage is feedthrough via the feedback to the output which is affecting the measurement. This can be overcome, if we can decouple the output from the input. A new circuit is proposed for the measurement of gain as shown in the fig.4.2.

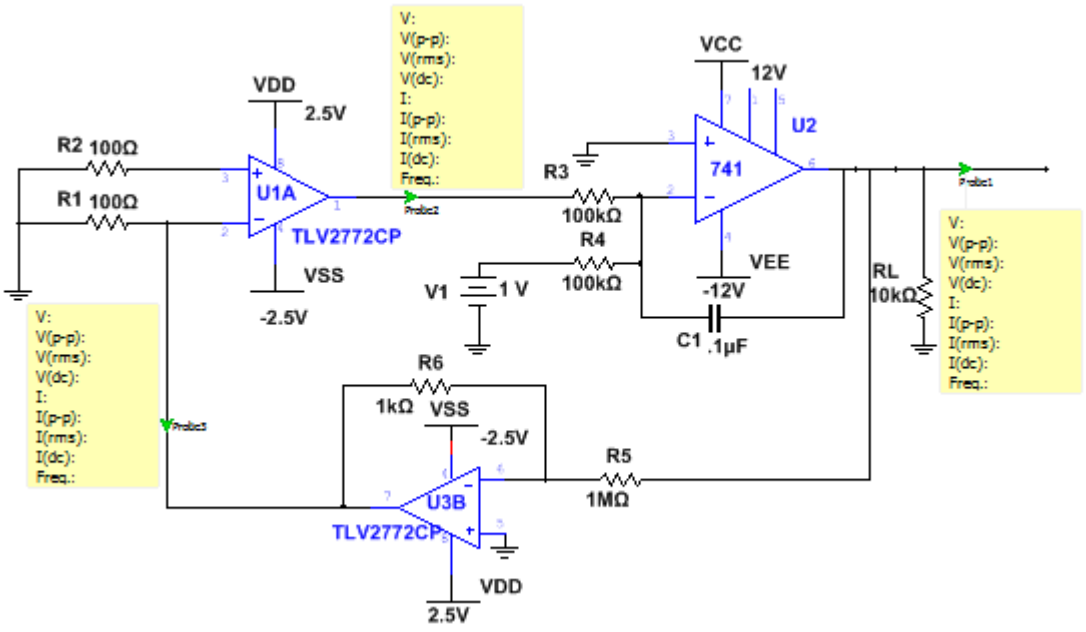

Figure-4.2 Proposed circuit for gain measurement

In the proposed circuit the servo op-amp is used as an inverting integrator. For the dc input voltage, capacitor will behave like an open circuit. So the integrator will act as open loop for dc input. However, the resistance at the input and the capacitance in the feedback limit the bandwidth of the integrator to few hundred of hertz. So the output of the DUT will be completely amplified by the full dc gain of the servo op-amp. In the global feedback loop, the resistive or passive attenuator is replaced by an active attenuator as shown in the fig.4.2. This will completely decouple the output of the servo amplifier from the input of the DUT. Open loop gain can be measured in the same way as stated above. The attenuation factor for the proposed circuit is fixed to 1/1000.

4.1.2 DC common mode rejection ratio (CMRR) measurement

CMRR can be defined as the ratio of the differential voltage gain to the common mode voltage gain. CMRR is measured by using the basic servo op-amp based test circuit [29] as shown in fig.4.3.

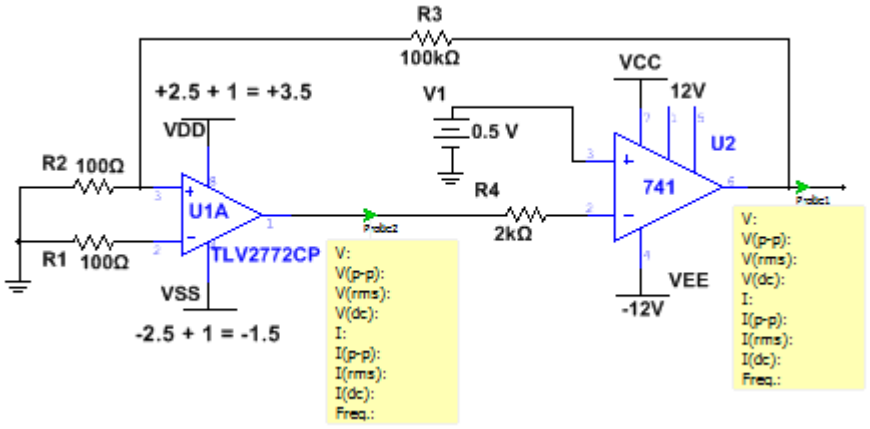

Figure-4.3 CMRR using Servo op-amp based test circuit [29]

The CMRR can be calculated from the measured values of the differential and common mode voltage gains.

$$\text{CMRR} = 20\log_{10}\left|\frac{\text{Differential voltage gain}}{\text{Common mode voltage gain}}\right| = 20\log_{10}\left|\frac{A_D}{A_{CM}}\right| \quad \ldots(38)$$

$$\text{CMRR} = \left|\frac{V_O/V_{id}}{V_O/V_{in\ CM}}\right| = \left|\frac{V_{in\ CM}}{V_{id}}\right| \quad \ldots(39)$$

$$\text{CMRR} = \left|\frac{\Delta V_{in\ CM}}{\Delta V_{in\ OS}}\right| \quad \ldots(40)$$

Where, $\Delta V_{in\ CM}$ → Change in the common mode voltage

$\Delta V_{in\ OS}$ → Change in the input offset voltage

So CMRR can be defined as the inverse ratio of the change of input offset voltage due to change in common mode voltage. Change in the common mode is equivalent to the change in power supply in the common or same direction. Firstly, the offset voltage is measured at power supply of $\pm$2.5. Now the offset voltage is measured when the power supplies are moved up by +1V *i.e.* +3.5 & -1.5, so that the total power supply remains the same as 5V (+3.5 – (-1.5)). But, the common mode voltage is changed by 1V. CMRR is also measured using the proposed circuit as shown in fig.4.4.

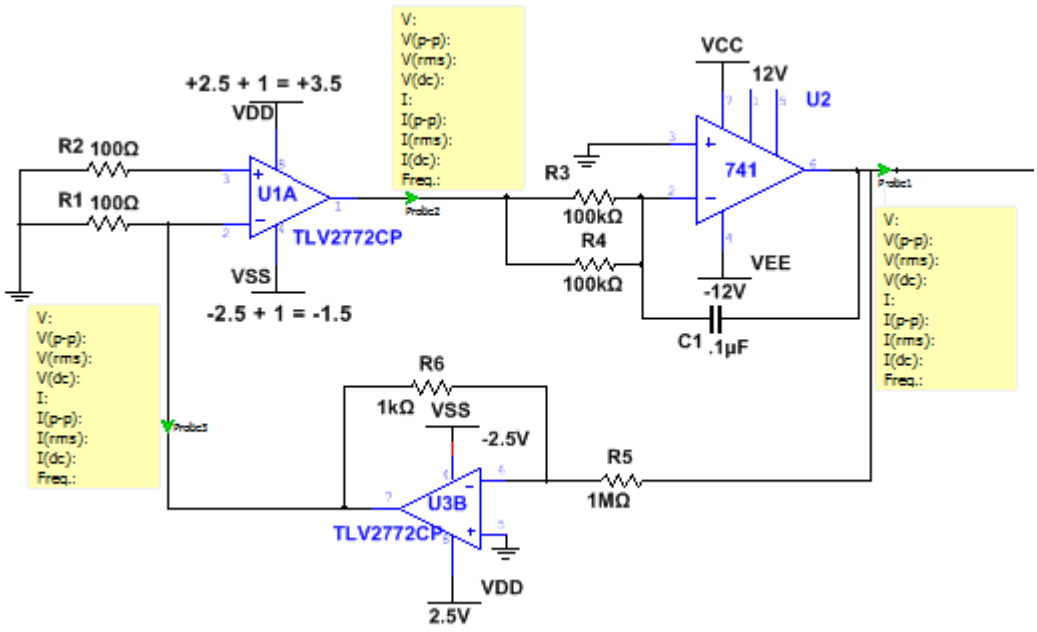

Figure-4.4 Proposed circuit for CMRR measurement

Following are the steps to measure the CMRR:

- Power supply voltage is fixed at +2.5 & -2.5.
- Measure the voltage at the input of the DUT which is equal to $V_{in\ OS}$ (1).
- Supply voltage is moved up by +1V *i.e.* +3.5 & -1.5.
- Again measure the voltage at the input of the DUT which is equal to $V_{in\ OS}$ (2).
- CMRR can be calculated from equation (40) and can be written as:

$$\text{CMRR} = \left|\frac{\text{Change in common mode voltage}}{V_{in\ OS}(2) - V_{in\ OS}(1)}\right| = \left|\frac{1\text{V}}{V_{in\ OS}(2) - V_{in\ OS}(1)}\right| \ldots (41)$$

Where, $V_{in\ OS}$ → is the offset voltage at the input of the DUT

4.1.3 DC power supply rejection ratio (PSRR) measurement

PSRR is defined as the ratio of the change in the power supply to the respective change at output voltage. PSRR is measured by using the basic servo op-amp based test circuit [29] as shown in fig.4.5.

The power supplies are changed from ± 2.5 to ± 2. So that the total power supply is changed by 1V (5V-4V) but the common mode voltage is not affected. PSRR is also measured from the proposed circuit as shown in fig.4.6.

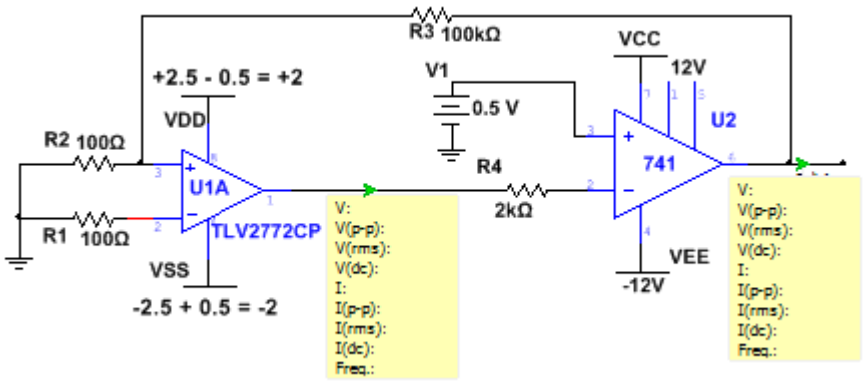

Figure-4.5 PSRR using Servo op-amp based test circuit [29]

In the proposed circuit the output is decoupled from the input of the DUT by using an attenuator so that there cannot be any input signal feed-through from the feedback to the output. The attenuator is implemented by using a CMOS Op-Amp. PSRR is given by the equation:

$$\mathrm{PSRR} = 20\log_{10}\left|\frac{\Delta V_{\mathrm{Supply}\ \pm}}{\Delta V_{\mathrm{Offset}}}\right| \qquad \ldots(42)$$

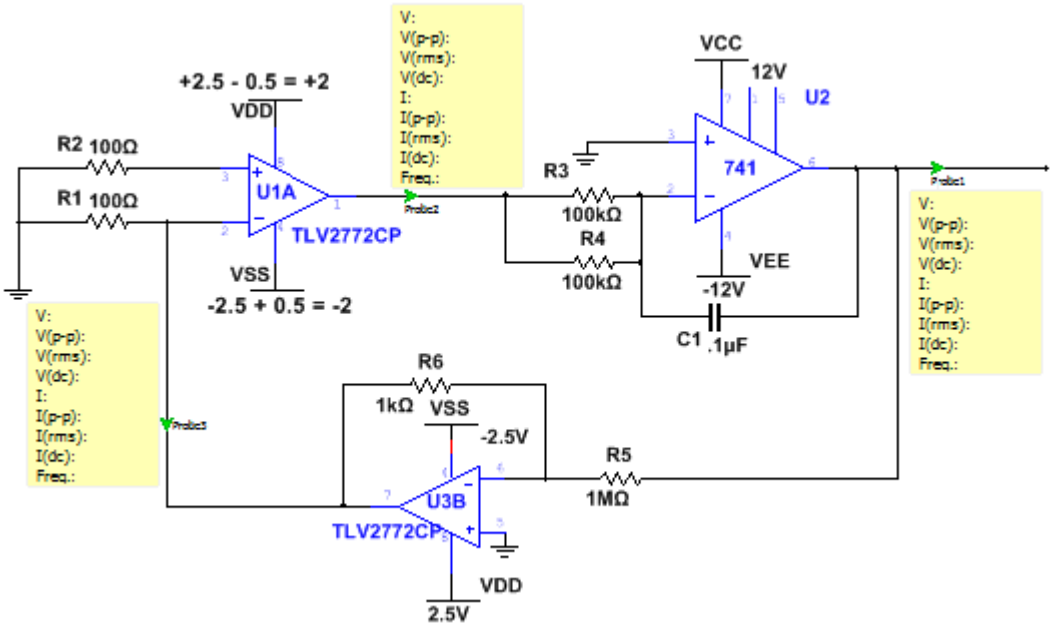

Figure-4.6 Proposed circuit for PSRR measurement

Following are the steps to measure PSRR:

- Power supply voltage is fixed at +2.5 & -2.5.
- Measure the voltage at the input of the DUT which is equal to $V_{in\,OS}$ (1).

- Supply voltage is changed from +2.5 & -2.5 to +2 & -2.
- Again measure the voltage at the input of the DUT which is equal to $V_{in\ OS}(2)$.
- PSRR can be calculated using equation 42 and is given by:

$$\text{PSRR} = \left|\frac{\text{Change in power supply voltage}}{V_{in\ OS}(2) - V_{in\ OS}(1)}\right| = \left|\frac{1V}{V_{in\ OS}(2) - V_{in\ OS}(1)}\right| \ldots (43)$$

Where, $V_{in\ OS}$ → is the offset voltage at the input of the DUT.

4.2 RESULTS AND DISCUSSIONS

Again TLV2772CP (CMOS based Op-Amp) is used as the DUT. Servo Op-Amp should have the power supply voltage greater than the power supply of the DUT. This is because of the reason that the maximum and minimum output voltage of the DUT lie in the range of the power supplies of the servo Op-Amp. To serve this purpose U741 is used which have the power supply of the $\pm$12V, greater than the power supply of $\pm$2.5V of the DUT. The Op-Amp working as an attenuator should have the output voltage in the range of the power supply of the DUT; TLV2772CP is used to serve this purpose.

4.2.1 Simulated results

Simulations are performed using SPICE via computer aided design tool MULTISIM. The values of DC open loop gain, DC CMRR and DC PSRR for both the basic servo op-amp based test circuit and the proposed circuit is calculated by using the equation (37), (41) and (43) respectively. The final results are shown in the Table-4.1.

Table-4.1 Simulated results for A_{OL}, CMRR and PSRR

Electrical Parameter	Basic servo op-amp bsed test circuit	Proposed test circuit
Open loop gain	97	99
CMRR	86.14	89
PSRR	83.6	89.9

4.2.2 Measured results on bread board

The results are verified by performing the testing on actual bread board as shown in fig. 4.7 and fig.4.8. Care must be taken while measuring the parameters on actual

bread board. Power supply must be constant throughout the measurement and should not be greater than the maximum given power supply. Digital multimeter with high precision should be used.

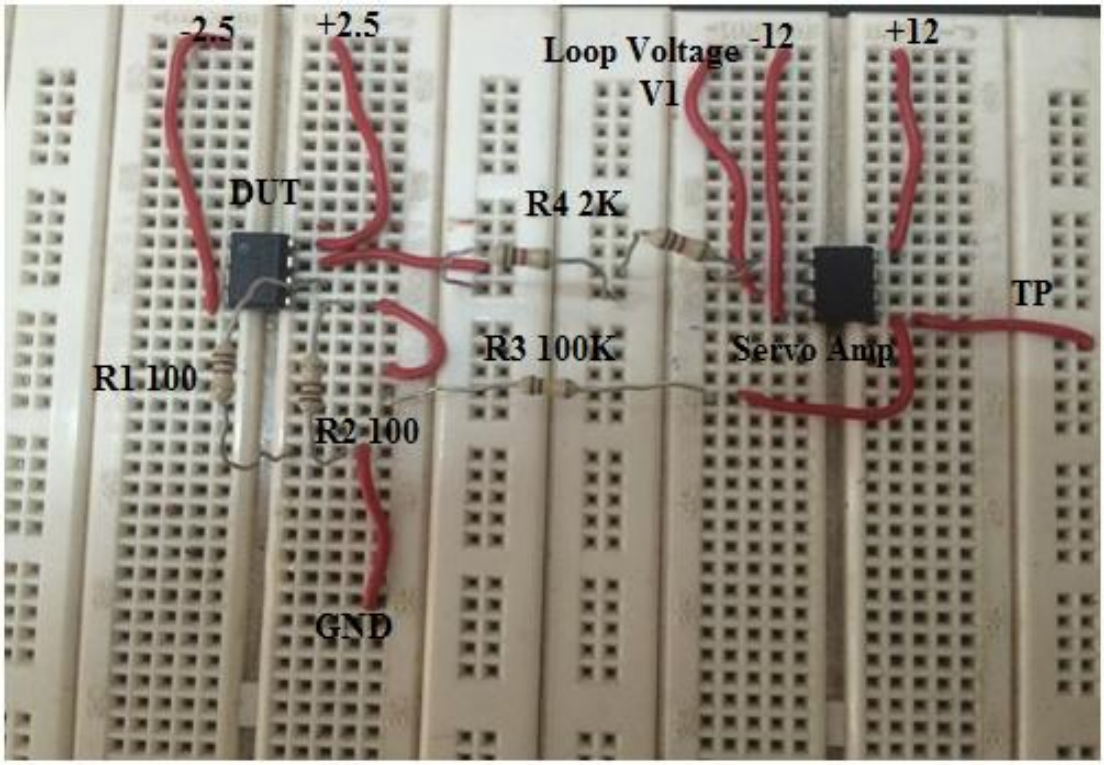

Figure-4.7 Measurement setup for servo op-amp based circuit

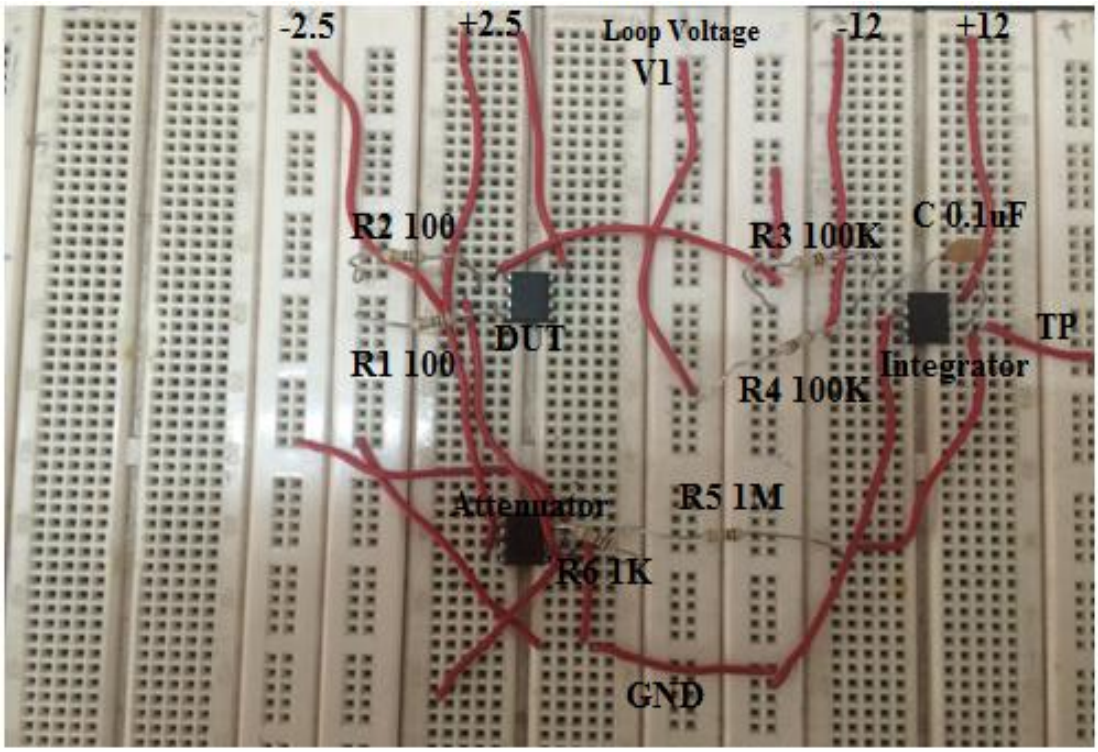

Figure-4.8 Measurement setup for the proposed circuit

The final comparison of the electrical parameters (open loop dc gain, DC CMRR & DC PSRR) is shown in theTable-4.2. The measured and the simulated values for the basic servo Op-Amp based circuit and the proposed circuit is compared with those taken from the data sheet.

Table-4.2 Comparison of electrical parameters

Electrical parameter	Data sheet Values (dB)	Basic servo op-amp bsed test circuit		Proposed test Circuit	
		Simulated values(dB)	Measured values(dB)	Simulated values(dB)	Measured values(dB)
Open loop gain	86-113	97	99.7	99	109.69
CMRR	60-96	86.14	88.63	89	91
PSRR	64-97	83.6	84.29	89.9	93.97

CHAPTER-5
CONCLUSION AND FUTURE SCOPE

Conclusion

In the present work, first open loop dc gain is measured by self test loop circuit so that one can know how to measure gain in close loop configurations. The circuit is simulated using MULTISIM which is a SPICE based simulator. Simulations are performed for the UA741 (a BJT based Op-Amp) and the TLV2772CP (a CMOS based Op-Amp) as the DUTs. Thereafter the simulated results of the open loop dc gain are compared for both DUTs.

Next, the dc specifications of the Op-Amp are measured using a servo Op-Amp based test circuit. Simulations for DC specifications like open loop dc gain, DC CMRR and DC PSRR are performed using SPICE based simulator. Thereafter, a new test circuit is proposed which uses an extra Op-Amp in the feedback loop, which is acting as an active attenuator. This is replacement for the resistive attenuator, which is being used in the basic servo Op-Amp based test circuit. In this way, it is possible to completely decouple the output of the servo Op-Amp from the input of the DUT. Because of this attenuator in the feedback loop it is possible to completely reject the influence of the feed through of any input signal via the feedback loop for measuring the DC specifications of the Op-Amp.

The new proposed circuit is simulated for the open loop dc gain, DC CMRR and DC PSRR using SPICE and the results of the existing and improved circuit are compared. At last to verify the simulated results, the measurements are performed on the actual measurement setup in the laboratory. Care must be taken while measuring the specifications on the bread board. For the measurement purpose TLV2772CP is used as the DUT. Measured values for both the circuits (servo Op-amp based test circuit & the new proposed circuit) are compared with the values taken from the data sheet of the DUT.

Future scope

In the present work, open loop dc gain, DC CMRR and DC PSRR are measured using the proposed circuit. The other important specifications like slew rate, gain bandwidth, ac common mode rejection ratio and ac power supply rejection ratio can be measured. In the new proposed test circuit the complexity is increased due to the extra Op-Amp. Results may get affected due to offset voltage of the added Op-Amp. In future steps can be taken to mitigate the above mentioned flaws such that the test circuit can be used in the more efficient way.

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APPENDIX

Macromodel and subcircuit of TLV2772CP

```
* TLV2772 operational amplifier "macromodel" subcircuit
* created using Parts release 8.0 on 12/12/97 at 10:08
* Parts is a MicroSim product.
*
* connections:   non-inverting input
*                | inverting input
*                | | positive power supply
*                | | | negative power supply
*                | | | | output
*                | | | | |
.subckt TLV2772  1 2 3 4 5
*
  c1   11 12 2.8868E-12
  c2    6  7 10.000E-12
  css  10 99 2.6302E-12
  dc    5 53 dy
  de   54  5 dy
  dlp  90 91 dx
  dln  92 90 dx
  dp    4  3 dx
  egnd 99  0 poly(2) (3,0) (4,0) 0 .5 .5
  fb    7 99 poly(5) vb vc ve vlp vln 0 15.513E6 -1E3 1E3 16E6 -16E6
  ga    6  0 11 12 188.50E-6
  gcm   0  6 10 99 9.4472E-9
  iss   3 10 dc 145.50E-6
```

```
 hlim 90  0 vlim 1K
 j1   11  2 10 jx1
 j2   12  1 10 jx2
 r2    6  9 100.00E3
 rd1   4 11 5.3052E3
 rd2   4 12 5.3052E3
 ro1   8  5 17.140
 ro2   7 99 17.140
 rp    3  4 4.5455E3
 rss  10 99 1.3746E6
 vb    9  0 dc 0
 vc    3 53 dc .82001
 ve   54  4 dc .82001
 vlim  7  8 dc 0
 vlp  91  0 dc 47
 vln   0 92 dc 47
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model jx1 PJF(Is=2.2500E-12 Beta=244.20E-6 Vto=-.99765)
.model jx2 PJF(Is=1.7500E-12 Beta=244.20E-6 Vto=-1.002350)
.ends
```

Macromodel and subcircuit of U741

```
.SUBCKT 741 1 2 3 4 5
* EWB Version 4 - 5 Terminal Opamp Model
* nodes: 3=+ 2=- 1=out 5=V+ 4=V-
* VCC= 15 VEE= -15 CC= 3e-011 A= 200000 RI= 2e+006
* RO= 75 VOS= 0.001 IOS= 2e-008 IBS= 8e-008
* VSW+= 14 VSW-= -14 CMMR= 90
* ISC= 0.025 SR= 0.5 Fu= 1e+006 Pm= 6.09112e-007
```

VC 5 15 DC 1.68573V

VE 12 4 DC 1.68573V

IEE 10 4 DC 1.516e-005A

R1 10 0 10Gohm

R6 11 0 100Kohm

R7 5 4 1Kohm

Rc1 6 5 5305.16ohm

Rc2 5 7 5305.16ohm

Re1 9 10 1839.19ohm

Re2 8 10 1839.19ohm

Ro1 1 14 37.5ohm

Ro2 14 0 37.5ohm

Ree 10 0 1.31926e+007ohm

Rcc 0 13 2.20906e-005ohm

Cee 0 10 1e-012

Cc 14 11 3e-011

C1 6 7 1e-016

GA 11 0 6 7 0.000188496

GC 0 13 1 0 45268.1

GB 14 0 11 0 282.942

GCM 0 11 10 0 5.96075e-009

D1 14 13 Dopamp1

D2 13 14 Dopamp1

D3 1 15 Dopamp2

D4 12 1 Dopamp2

Qt1 6 2 9 Qopamp1

Qt2 7 3 8 Qopamp2

.MODEL Dopamp1 D (Is=7.53769e-014A Rs=0 Cjo=0F Vj=750mV Tt=0s M=0)

.MODEL Dopamp2 D (Is=8e-016A Rs=0 Cjo=0F Vj=750mV Tt=0s M=0)

```
.MODEL Qopamp1 NPN (Is=8e-016A BF=83.3333 BR=960m
+ Rb=0ohm Re=0ohm Rc=0ohm Cjs=0F Cje=0F Cjc=0F
+ Vje=750m Vjc=750m Tf=0 Tr=0 mje=0 mjc=0 VA=50)
.MODEL Qopamp2 NPN (Is=8.30948e-016A BF=107.143 BR=960m
+ Rb=0ohm Re=0ohm Rc=0ohm Cjs=0F Cje=0F Cjc=0F
+ Vje=750m Vjc=750m Tf=0 Tr=0 mje=0 mjc=0 VA=50)
.ENDS
```