Analysis of Breakdown Voltages and Depletion Region width of 3C-SiC Vertical Double Implanted MOSFET using Complementary Error Function Profile In Drift Region

A Thesis submitted in partial fulfilment of the requirements for the award of degree of

MASTER OF TECHNOLOGY

in

VLSI Design & CAD

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June-2009

CERTIFICATE

I hereby certify that the work which is being presented in the thesis entitled **"Analysis of Breakdown Voltages and Depletion Region Width of 3C-SiC Vertical Double Implanted MOSFET using Complementary Error Function Profile in Drift Region"** in partial fulfilment of requirement for award of degree of **Master of Technology** in **VLSI Design & CAD** from **Thapar University**, is an authentic record of my own work carried under the supervision and guidance of **Dr. A.K.Chatterjee**, Professor and Head, Electronics & Communication Engineering department, Thapar University, Patiala.

The matter presented in this thesis has not been submitted in any other university or institute for the award of any other degree.

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ACKNOWLEDGEMENT

I wish to express my special thanks and deepest regards to my Thesis Adviser, **Dr. A. K. Chatterjee**, Professor & Head, Electronics & Communication Engineering Department, for providing me invaluable guidance, suggestions, and support which have helped me to submit this thesis within time.

I take this opportunity to express my gratitude and sincere thanks to **Mrs. Alpana Aggarwal**, Assistant Professor, Electronics & Communication Engineering Department, for their valuable advice and suggestion and for providing me the opportunity to complete my thesis work simultaneously.

I would also like to thank all the staff members of Electronics & Communication Engineering Department for providing me all the facilities required for the completion of this work.

I wish to thank all my classmates for their time to time suggestions and cooperation. Finally it is the support, encouragement and good wishes of my parents and other family members without which I would not have been able to complete my thesis.

I thank and owe my deepest regards to all of them and all others who have helped me directly or indirectly.

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ABSTRACT

It is increasingly recognized that semiconductor based electronics that can function at temperatures higher than 1500^0C without external cooling cold greatly benefit a variety of important applications, especially in the automotive, aerospace, and energy production industries The fact that wide band gap semiconductors are capable of electronic functionality at much higher temperatures than silicon has partially fuelled their development, particularly in the case of SiC. 3C-SiC is a potentially useful material for high temperature devices because of its refractory nature, high thermal conductivity, wide band gap(2.2eV) and high electron mobility comparable to that of Si.

The present work aims at the design of high breakdown voltage 10kV 3C-SiC Double Implanted Metal Oxide Semiconductor Field effect transistor (DIMOSFET) with complementary error function doping profile in drift region. Firstly, the device equation for calculating breakdown voltages (Punch through and Avalanche both) is derived. After that the Drift region depletion width is calculated at doping concentration $N_d = 1\times10^{15}/cm^3$ for different breakdown voltages from 1 to 10kV.

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CHAPTER 1

INTRODUCTION

Silicon carbide is an emerging technology for extreme environment electronics applications. This chapter discusses the background and motivation behind the 3C-SiC vertical double implanted MOSFET and also various applications of SiC technology.

1.1 BACKGROUND

Silicon carbide (SiC) based semiconductor electronic devices and circuits are presently being developed for use in high-temperature, high-power and high-radiation conditions under which conventional semiconductors cannot adequately perform [1].

Thermal oxidation of SiC produces a layer of SiO_2 on the surface while the carbon atoms from the SiC form CO, which escapes as gas. Thus, it is possible to make all devices found in silicon IC technology in SiC, including high quality, stable MOS transistors and MOS integrated circuits. Wide band gap semiconductors examples are: gallium nitride (GaN, E_G=3.4eV), aluminum nitride (AlN, EG= 6.2eV) and silicon carbide (SiC, EG between 2.2-3.25 eV depending on the polytype used). SiC is so thermally stable that dopant impurities cannot be diffused at any reasonable temperature. SiC is the only compound semiconductor which can be thermally oxidised to form a high quality native oxide (SiO_2). Although SiC offers substantial advantages over silicon, it is still immature as a semiconductor material. The main limitations of the technology are in the area of crystal growth.

In 1955, a laboratory simulation process for growing SiC crystals was developed by J. A. Lely [2]. In the Lely process, the nucleation of individual crystals are uncontrolled and the resulting crystals are randomly sized hexagonal-shaped a SiC platelets. In 1978, Tairov and Tsvetkov introduced the growth of SiC single crystal by the vapour transport process [2]. In 1983, Ziegler introduced the modified sublimation process for growing SiC single crystal.

In 1987, a research group under R. F. Davis at North Carolina State University (NCSU) announced a modification to the original Lely sublimation process [2]. In this modified process, single large crystal is grown and this crystal consists of a single polytype. In this process, a charge of polycrystalline SiC is heated in a graphite crucible containing argon at 200 Pascal. In 1987, the students from the NCSU group founded a small company,

Cree Research, to produce silicon carbide commercially [2]. Single crystal SiC forms in the hexagonal lattice, with alternating hexagonal planes of silicon and carbon atoms. Each silicon atom bonds to four nearest-neighbouring carbon atoms and each carbon atom is attached to four nearest-neighbouring silicon atoms.

Doping of silicon carbide can be done during epitaxial layer growth or after crystal growth by ion implantation. Ion-implantation is normally used because of lower quality of doped semiconductor due to crystal damages created during ion bombardment than doped epilayers. The first step in making silicon carbide semiconductor devices is to grow the epitaxial layer using chemical vapour deposition (CVD). The silicon carbide epilayers are produced in the CVD process by thermally decomposing silicon and carbon source gases (called precursors) onto boule-derived SiC substrates. The SiC lattice consists of alternating planes of silicon and carbon atoms. The stacking sequence of these planes defines different polytypes of the material identified by the repeating distance of the stacking sequence (e.g. 3C, 4H & 6H). The lattice constant in the basal plane is virtually identical for all polytypes, but important electrical properties such as band gap energy, electron mobility and critical field differ significantly between the polytypes [3]. The electrical properties are changed by adding impurities. The control over the impurity addition in CVD SiC epilayers is very limited. This leads to difficulties over the control of unintentional impurities, which makes it difficult to achieve the desired epilayer thickness. The other method of doping silicon carbide is selective doping after epitaxial layer formation. The selective doping is accomplished by ion implantation; the diffusion coefficients of aluminium and nitrogen are so low that diffusion in silicon carbide is impossible. Diffusion in SiC at high temperatures produces significant surface damage. Successful fabrication of implanted layers in SiC depends on the proper choice of implant anneal conditions. Implant activation typically requires annealing at temperatures between 1000^0C and 1700^0C. Chemical etching is impractical owing to the high chemical stability of SiC and selective etching is accomplished by reactive ion etching (RIE) using fluorinated gases.

1.2 MOTIVATION

1.2.1 Need of SiC

SiC offers several application opportunities including

- High voltage and High power applications such as industrial motors, locomotives, and power supplies requiring high-voltage switches.

- High-temperature sensor applications for aircraft engines, oil drilling, and automotive electronics, including controlling fuel efficiency and emissions.
- SiC offers the benefit of eliminating expensive cooling systems needed in industrial equipment common to factories worldwide.

1.2.1.1 Need of 3C-SiC

The 3C-SiC is a promising material for MOSFET devices because of high channel mobility due to lower density of interface states compared to 4H-SiC. Poor performance of 6H-SiC and 4H-SiC MOSFETs is related to the interface states located in the band gap close to the conduction band edge limiting the transport of electrons in the channel [4]. Due to the smaller band gap of 3C-SiC, the interface states observed in 6H-SiC and 4H-SiC are located in the conduction band and have no effect on the transport properties of the channel. Channel mobility 75 to 260 cm^2/Vs have been reported. The 3C-SiC polytype has lower critical electric field value due to the lower band gap. It means that the drift region doping corresponding to a given blocking voltage will be lower compared to the hexagonal 4H- and 6H-SiC polytypes. That the specific junction capacitance will be lower in the 3C-SiC devices as compared to the 4H-SiC and 6H-SiC ones. This is an advantage for the high speed MOSFETs. Considering all of the above and given large-area substrates of good quality, 3C-SiC may well be the material of choice for medium voltage (600 V to 1200 V) MOSFETs.

1.2.2 Need of Vertical DIMOSFET

- The channel length of the vertical MOS transistor is not defined by lithography. This means no requirements for post-optical lithography techniques such as x-ray, extreme ultra-violet, electron projection lithography, ion projection lithography or direct write e-beam which are possibly prohibitively expensive.
- Vertical MOS transistors are easily made with both front gate and back gate which doubles the channel width per transistor area. This leads to an increase of packing density of at least a factor of four as compared to horizontal transistors. One step further, is the use of very narrow pillars with the gate surrounding the entire pillar. This way, fully depleted transistors can be produced which have all the advantages of SOI transistors.

- Vertical MOSFET prevents short channel effects from dominating the transistor by adding processes that are not easily realised in horizontal transistors, such as a polysilicon source to reduce parasitic bipolar effects or a dielectric pocket to reduce drain induced barrier lowering (dibl).

1.2.3 3C-SiC DIMOSFET with complementary error function profile

The 3C-SiC is a promising material for MOSFET devices because of high channel mobility due to lower density of interface states compared with 4H-SiC. The doping profile for 3C-SiC vertical DIMOSFET for high breakdown voltage use complementary error function profile. The profile can be generated by ion-implantation from the drain end of the device, so that the projected range is close to the drain end of the device.

1.3 APPLICATIONS

Silicon carbide has a clear place in society today, yet it has only one major commercial application today, which basically is materials or, more specifically, substrates for LED applications. The military has had SiC on its radar screen for many years for radar applications, electronic warfare, more electric airplanes, more electric ships, more electric combat vehicles. The biggest application for SiC technology is the high-power and high temperature electronics market [5].

1.4 ORGANIZATION OF THESIS WORK

An **Introduction** to the concept of SiC technology and vertical DIMOSFET with complementary error function profile is presented in chapter 1.

Chapter Two starts with explaining the SiC technology, its polytypes (3C, 4H, 6H etc), properties and its applications.

Chapter Three presents start with explaining Power MOSFETs, its types, properties and applications.

Chapter Four presents the derivation of the device equation for 3C-SiC vertical DIMOSFET using complementary error function profile.

Chapter Five presents the calculations of breakdown voltages (punch through and avalanche) and depletion region width for the device using complementary error function profile and comparison with uniform doping profile.

Chapter Six, includes conclusion has been analyzed further improvement, which is possible.

CHAPTER 2

SiC TECHNOLOGY

2.1 FUNDAMENTAL SiC MATERIAL PROPERTIES

SiC offers significant advantages for power electronics applications such as lamp ballasts, motor controls, medical electronics, automotive electronics, high-density high-frequency power supplies and smart-power application-specific integrated circuits. quality native oxide for use as an insulator in electronic devices. Silicon carbide can resist high field strengths and offers better heat conducting capacity than copper at room temperature. Due to high thermal conductivity and high breakdown electric field strength, SiC can be used at high temperature, high voltage, high frequency and high power applications. This chapter briefly surveys the SiC semiconductor electronics technology. In particular, the differences between SiC electronics technology and well-known silicon VLSI technology are highlighted. Projected performance benefits of SiC electronics are highlighted for several large-scale applications. Key crystal growth and device-fabrication issues that presently limit the performance and capability of high temperature and/or high power SiC electronics are identified [6].

The arrangement of Si and C atoms in SiC can be described as a covalently bonded tetrahedral, as shown in Figure 2.1(a). In order to maintain the tetrahedral geometry of the lattice, each successive bilayer can be placed in one of only three positions with respect to the underlying plane. These three different positions are commonly denoted by A, B, and C as shown in Figure2.1 (b). The bilayer arrangement scheme, although permitting a large number of polytypes, restricts the polytypes to phases having either cubic, hexagonal, or rhombohedral symmetries. The probability of occurrence of different polytypes depends on temperature. Among the many polytypes, 3C-SiC and 6H-SiC have a higher probability of occurrence.

Generally 3C-SiC is stable in the low-temperature region below 1800^0C, and 6H-SiC is stable in the higher temperature region above 1800^0C. Although 4H-SiC also sometimes occurs in the high temperature region, the probability is very lower compared to 6H-SiC. Each polytype has unique electrical and physical properties. Silicon carbide has been

regarded as a wide band gap semiconductor material for visible light- emitting devices, since electro luminescence was observed for the first time in 1907, and a light emitting diode was fabricated for the first time in 1923[7]. However, the stable characteristics of SiC have caused difficulty in producing high quality layers and large single crystal growth, and thus the development of semiconductor technology in SiC has been delayed. However a wide range of devices have already been demonstrated, including: Bipolar Junction Transistor (BJT), Insulated Gate Bipolar Transistor (IGFET), MESFET, JFET, p-n Junction and Schottky diodes.

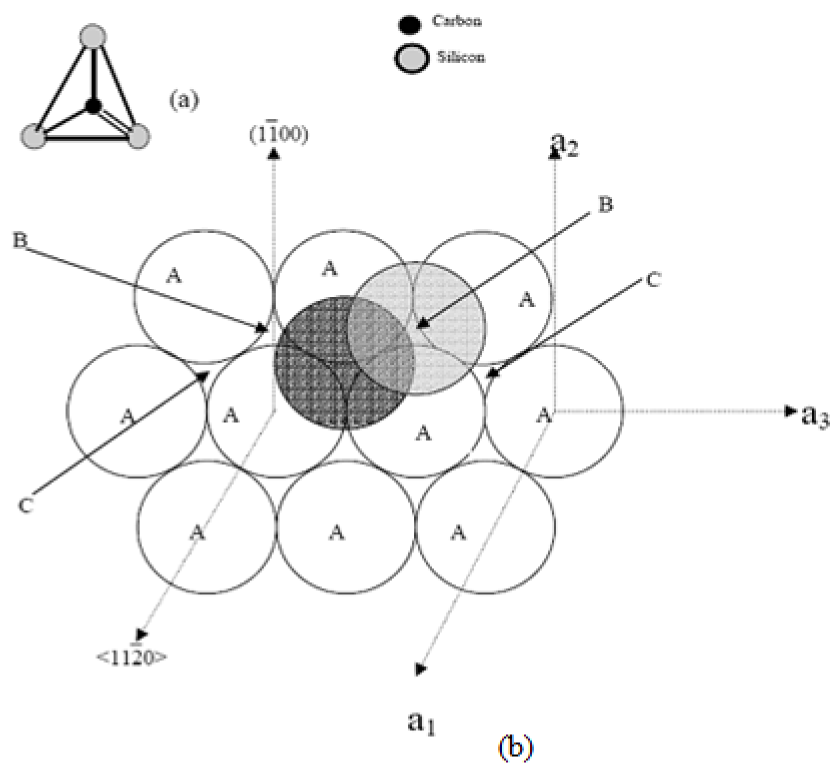

Figure2.1 Schematic of (a)Tetrahedral atomic arrangement of Carbon and Silicon atoms in SiC (b) Close packed plane showing three possible stacking sites [7].

Silicon carbide is a new material, and the processes involved are different to those of silicon, and some of the process steps are still in their infancy. SiC is a very hard material and almost inert, which makes SiC processing problematical. Implantation of dopants is difficult to perform, especially p-type, and the etch rate is slow. Schottky and Ohmic contacts are now fairly well developed processes in SiC. SiC epitaxial layer growth is also well established, and bulk wafers with an epitaxial layer structure are supplied from wafer manufacturers. Hence, the etching of structures in epitaxial layers is the most

common method for the manufacture of SiC devices. SiC has SiO_2 as its naturally occurring oxide, although the quality of the oxide layer reported is not as good as for silicon, suffering from both low surface mobility and low breakdown strength. This is large drawback for MOSFET devices which would be very promising for high-temperature electronic devices. However, much research is focused on this particular area and the quality is constantly increasing [8].

2.1.1 Transport Properties

A large part of this work has been devoted to discovering reliable transport parameters for different SiC polytypes, mainly 4H-SiC. For reliable and efficient device performance, analysis of transport parameters is required. Published measurements are the main source of information used in the tuning process of the transport models. The immature nature of silicon carbide, and lack of measurements for many transport properties, implies that the available set of transport parameters is incomplete.

2.1.1.1 Mobility

The mobility defines that how easily the electrons and holes can be moved in an electric field. Due to random scattering within the crystal, the velocity does not increase with constant acceleration as in a vacuum. The electron velocity rather quickly reaches an equilibrium mean-velocity proportional to the mobility and the electric field.

The mobility in SiC is somewhat lower than for silicon and much lower than in high-mobility materials, such as GaAs. The low mobility in SiC devices is compensated by operation at larger electric fields taking advantage of the higher carrier velocity. To some extent the mobility can be described using the same models as those used for silicon. The parameters for the mobility models are collected from measurements for a temperature dependent mobility model [9].

2.1.1.2 Saturation Velocity

At high electric fields the velocity ceases to be proportional to the electric field, due to increased scattering. The velocity saturates at v_{sat}, which for SiC is approximately twice the value for silicon. A high saturation velocity allows faster devices with shorter switching times.

2.1.1.3 Band Gap

The band gap is a forbidden zone in the energy spectra for a crystal. Without a band-gap the crystal is a metal, and with a large band-gap the crystal is an insulator. A

semiconductor has a band-gap up to a few eV. For some traditional semiconductors the band gaps are: 1.11 eV for Si, 0.7 eV for Ge, and 1.4 eV for GaAs.

Many of the favourable transport parameters in SiC are related to the large band-gap, which is of the order of 3 eV. For such a large band gap the intrinsic carrier concentration is negligible at temperatures up to 600^0C. The intrinsic carrier concentration is responsible for the thermal noise, and also partly responsible for the leakage current, which are both very small in large band-gap materials. The minimum energy required to create an electron-hole pair is equal to the band-gap that in SiC falls within the 3 eV range corresponding to a photon with wavelength close to 400 nm. SiC devices are thus also insensitive to the main part of the visible spectrum, making SiC suitable as a detector material for UV radiation with minimal noise from the visible background [19].

2.1.2 Critical Electric Field

For high electric fields the carrier energy is increasing and as the energy exceeds the band-gap, the probability of an impact ionization event increases. In an impact-ionization event the carrier knocks out one electron from the valence-band, creating an electron-hole pair (EHP). As the energy must be conserved, the energy for the incident carrier is reduced by the band gap energy plus the initial energy for the created electron and hole. The critical electric field is related to the impact ionization rate, which increases as the carrier energy exceeds the band-gap. Due to the large band- gap the critical electric field is thus about 10 times higher in SiC than for small band-gap materials, such as Si and GaAs. With high E_{crit} devices can be much smaller for the same voltage, alternatively operate at much higher voltages.

2.1.3 Thermal Conductivity

The thermal conductivity for SiC is close to copper. Thermal conductivity is a quality that is very important in power semiconductor devices in order to transport the heat in the device.

For high power devices the thermal effects constitute one of the main limiting factor of the performance. One of SiC´s competitors is gallium nitride (GaN), which is a material with similar properties to those of SiC but which are less mature. One drawback of gallium nitride is the even lower thermal conductivity than silicon (1.3 W/cmK). However, gallium nitride is often grown on SiC substrates, with its better thermal conductivity. Nevertheless, the GaN-SiC interface has lower thermal conductivity than GaN itself which leads to a degradation of the performance.

2.1.4 Surface Mobility

The surface mobility describes the transport in the inversion layer of a MOSFET device and is critical for device performance. Pioneering experiments have given very poor values for the surface mobility in SiC devices in the range of 10 cm^2/Vs [6]. The low mobility is related to the high defect density in the oxide-semiconductor interface and doubts about SiC MOSFETs as commercial devices have been expressed in many quarters. The mobility is presently reaching values above 150 cm^2/Vs [8] and commercial MOSFETs are expected to appear in the market shortly.

2.1.5 Impact Ionization

For high-power devices the impact ionization process is very important for accurate predictions of the high power performance. Many of the pioneering measurements reported a positive temperature coefficient of the impact ionization coefficient. As the impact ionization heats the lattice, such behaviour would further increase the impact ionization. This would be a very serious problem, causing local hot spots, unstable operation and thermal runaway, destroying the device. In later measurements the impact ionization coefficient shows a negative temperature dependency and thus the positive sign presented previously was mainly contributed to by the presence of deep levels in the samples used.

The SiC lattice consists of alternating planes of silicon and carbon atoms, and the stacking sequence of these planes defines different polytypes of the material identified by the repeating distance of the stacking sequence (e.g. 3C, 4H & 6H). Silicon carbide occurs in many different crystal structures, called polytypes. Despite the fact that all SiC polytypes chemically consist of 50% carbon atoms covalently bonded with 50% silicon atoms, each SiC polytype has its own distinct set of electrical semiconductor properties. While there are over 100 known polytypes of SiC, only a few are commonly grown in a reproducible form acceptable for use as an electronic semiconductor. The most common polytypes of SiC presently being developed for electronics are 3C-SiC, 4H-SiC, and 6H-SiC. 3C-SiC, also referred to as ß-SiC, is the only form of SiC with a cubic crystal lattice structure. The non-cubic polytypes of SiC are sometimes ambiguously referred to as a 2H-SiC. 4H-SiC and 6H-SiC are only two of many possible SiC polytypes with hexagonal crystal structure. Similarly, 15R-SiC is the most common of many possible SiC polytypes with a rhombohedral crystal structure. Because some important electrical device properties are non-isotropic with respect to crystal orientation, lattice site, and

surface polarity, some further understanding of SiC crystal structure and terminology is necessary. Different polytypes of SiC are actually composed of different stacking sequences of Si-C bilayers (also called Si-C double layers), where each single Si-C bilayer can simplistically be viewed as a planar sheet of silicon atoms coupled with a planar sheet of carbon atoms.

The breakdown field in SiC is about 8 times higher than in silicon. This is important for high-voltage power switching transistors. For example, a device of a given size in SiC will have a blocking voltage 8 times higher than the same device in silicon. Moreover, the on-resistance of the SiC device will be about 100 times lower than the silicon device [9].

Table 2.1 Comparison of electronic properties of SiC with Si, GaAs and GaN [2]

	Si	**GaAs**	**GaN**	**6H-SiC**	**4H-SiC**	**3C-SiC**
Bandgap(eV)	1.1	1.142	3.39	3	3.26	2.2
Breakdown field @ 10^{17} cm^{-3}(MV/cm)	0.6	0.6	3.3	3.2	3.0	1.5
Electron Mobility @ $10^{16}cm^{-3}(cm^2/V\text{-}s)$	1100	6000	1000	370	800	750
Hole mobility @ 10^{16} $cm^{-3}(cm^2/V\text{-}s)$	420	320	200	90	115	40
Saturation electron drift velocity (cm/s)	10^7	10^7	2.5×10^7	2×10^7	2×10^7	2×10^7
Intrinsic concentration, n_i (cm^{-3})	1.5×10^{10}	1.9×10^{-10}	2.1×10^6	2.3×10^{-6}	8.2×10^{-9}	6.9
Thermal conductivity	1.5	0.55	1.3	4.9	4.9	5

Because the band-gap of SiC is so much wider than silicon as shown in Table 2.1, thermal generation of electron-hole pairs is many orders of magnitude lower at any given temperature. This makes it possible to build “dynamic” memories (DRAMs) in SiC that only need to be refreshed about once every 100 years at room temperature. It is possible to operate SiC devices at temperatures as high as 650^0C without degradation in electrical performance.

2.2 SIC CRYSTALLOGRAPHY-IMPORTANT POLYTYPES AND DEFINITIONS

2.2.1 SiC Polytypes

Silicon carbide exists in hundreds of different polytypes, the most common being 3C-SiC, 4H-SiC and 6H-SiC. Furthermore, islands of 15R-SiC can be found on 4H-SiC and 6H-SiC wafers and small crystals of 2H-SiC have been grown. The digit in the name is the number of double layers (one Si and one C layer) in the primitive lattice cell; the character gives the type of crystal symmetry. H stands for hexagonal, C for cubic and R for rhombohedral. A schematic view of some of the different SiC polytypes is presented in Fig.2.2. In the hexagonal structure a clear distinction exists between the different directions in the lattice. The direction parallel to the central axis in the hexagonal structure is called the crystal axis, or c-axis. In commercially available wafers the c-axis is normally oriented perpendicular to the surface, usually being a few degrees off axis. The transport parameters for the most common SiC polytypes, together with some other semiconductors, are presented in Table 2.1[2].

2.2.1.1 6H-SiC

6H-SiC has a large anisotropy due to the long repetition length in the crystallographic lattice. The mobility in the direction perpendicular to the c- axis (commonly parallel to the surface) is four times greater than in the c- axis direction. Compared with Si the mobility in 6H-SiC is about 25% in the direction perpendicular to the c-axis, and 7% in the direction parallel to it.

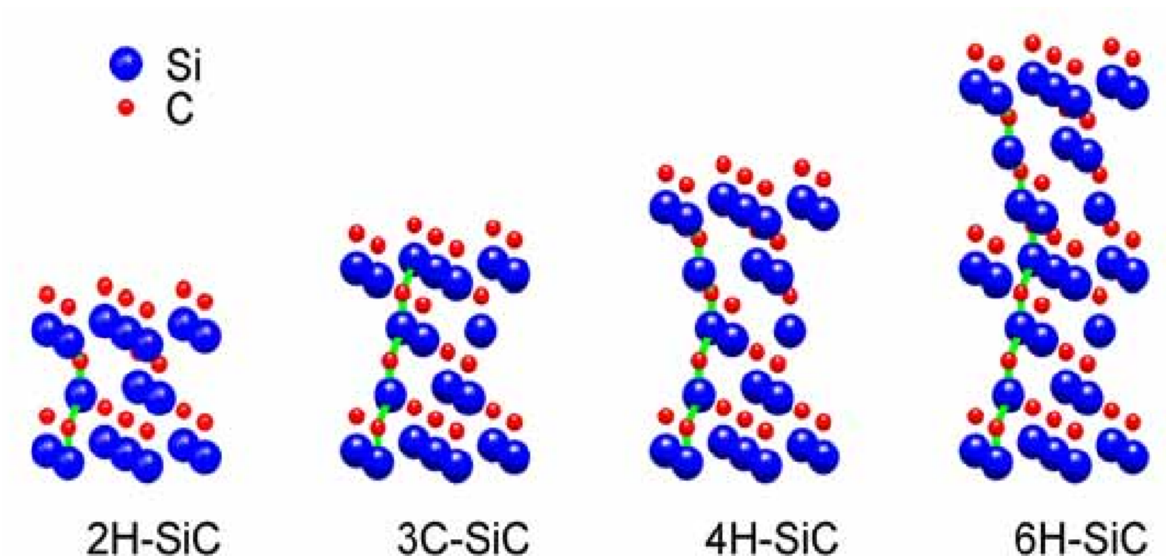

Figure2.2. Schematic Structure for some Different SiC Polytypes [5]

The saturation velocity for 6H-SiC is 2×10^7 cm/s in the direction perpendicular to the c-axis, but only 0.6×10^7 cm/s in the direction parallel to it.

2.2.1.2 4H-SiC

The low-field mobility for 4H-SiC is about half that of silicon with a small anisotropy (20% higher in the direction parallel to the c-axis). The anisotropy in 4H-SiC depends on the electric field, and at high electric fields the saturation velocity is 20% lower in the c-axis direction.

4H-SiC and 6H-SiC are the most mature polytypes and they are the ones which have been characterized most thoroughly. The transport properties are better for 4H-SiC and, at present, this polytype forms the basis for most of the commercial products [8].

2.2.1.3 3C-SiC

3C-SiC has an advantage as it is able to be grown on silicon substrates, however at the moment with reduced quality. It allows the possibility of integration of 3C-SiC devices with silicon technology on the same chip in future. Another advantage is that 3C-SiC does not suffer from stacking faults growth, as these tend to grow towards 3C-SiC. 3C-SiC has larger electron mobility than for 4H-SiC but has reduced hole mobility. The main disadvantages when compared to other polytypes are the lower band-gap and breakdown field and the advantage of replacing existing silicon devices is strongly reduced [8].

2.2.1.4 15R-SiC

15R-SiC is very complex, namely 15 atomic layers ordered in a rhombohedral structure. A few years ago, much attention was focused on 15R-SiC, owing to improved experimental MOSFET performance when compared to the other polytypes [5]. These devices have been manufactured on 4H-SiC or 6H-SiC, where pieces of 15R-SiC were found. Mono-crystalline 15R- SiC wafers are however not a reality in the near future.

2.2.1.5 2H-SiC

2H-SiC is not a commercially available substrate, but small mono-crystalline pieces have been grown. The performance perpendicular to the c-axis direction is similar to 4H-SiC, but the mobility is better in the parallel to the c axis direction (similar to silicon) [5].

2.3 APPLICATIONS AND BENEFITS OF SiC ELECTRONICS

Two most beneficial advantages that SiC-based electronics offer are in the areas of high-temperature device operation and high-power device operation. The specific SiC device

physics that enables high temperature and high power capabilities will be examined first, followed by several examples of revolutionary system-level performance improvements these enhanced capabilities enable.

2.3.1 High Temperature Device Operation

The wide band gap energy and low intrinsic carrier concentration of SiC allows maintaining semiconductor behaviour at much higher temperatures than silicon, which in turn permits SiC semiconductor device functionality at much higher temperatures than silicon. Semiconductor electronic devices function in the temperature range where intrinsic carriers are negligible so that conductivity is controlled by intentionally introduced dopant impurities. Furthermore, the intrinsic carrier concentration n_i is a fundamental prefactor to well-known equations governing undesired junction reverse bias leakage currents. As temperature increases, intrinsic carriers increase exponentially so that undesired leakage currents grow unacceptably large, and eventually at still higher temperatures, the semiconductor device operation is overcome by uncontrolled conductivity as intrinsic carriers exceed intentional device doping [11, 12]. Depending upon specific device design, the intrinsic carrier concentration of silicon generally confines silicon device operation to junction temperatures less than 300^0C. SiC's much smaller intrinsic carrier concentration theoretically permits device operation at junction temperatures exceeding 800^0C, and 600^0C SiC device operation has been experimentally demonstrated on a variety of SiC devices.

2.3.2 High Power Device Operation

The high breakdown field and high thermal conductivity of SiC coupled with high operational junction temperatures theoretically permit extremely high power densities and efficiencies to be realized in SiC devices. Figures 2.3 and 2.4 demonstrate the theoretical advantage of SiC's high breakdown field compared to silicon in shrinking the drift-region and associated parasitic on-state resistance of 3000 V rated unipolar power MOSFET device. The high breakdown field of SiC relative to silicon enables the blocking voltage region to be roughly 10 times thinner and 10 times heavier-doped, permitting a roughly 100 fold decrease in the dominant blocking region (N-Drift Region) resistance R_D of Figure 2.3 for the SiC device relative to an identically rated 3000V silicon power MOSFET [8]. Significant energy losses in many silicon high-power system circuits, particularly hard- switching motor drive and power conversion circuits, arises from semiconductor switching energy loss. While the physics of semiconductor device

switching loss are discussed in detail elsewhere, switching energy loss is often a function of the turn-off time of the semiconductor switching device, generally defined as the time lapse between when a turn-off bias is applied to the time that the device actually cuts off most current flow. The faster a device turns off, the smaller its energy loss in a switched power conversion circuit. SiC's high breakdown field and wide energy band gap enable much faster power switching than is possible in comparably volt-amp rated silicon power-switching devices. Therefore, SiC-based power converters could operate at higher switching frequencies with much greater efficiency (i.e., less switching energy loss).

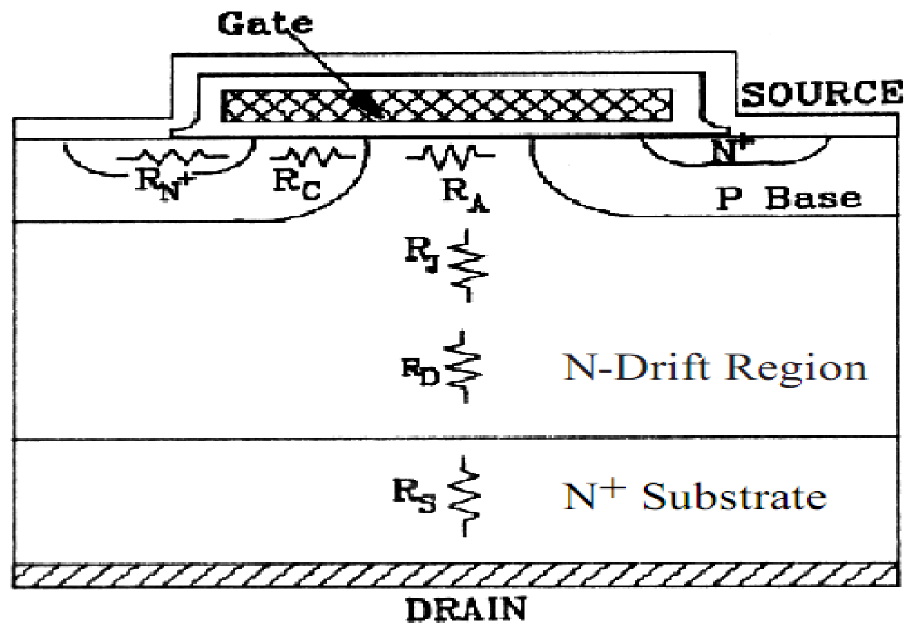

Figure2.3 Cross-section of power MOSFET structure showing various internal resistances [8].

Higher switching frequency in power converters is highly desirable because it permits use of proportionally smaller capacitors, inductors, and transformers, which in turn can greatly reduce overall system size and weight. The resistance R_D of the N-Drift Region is the dominant resistance in high-voltage power devices [8]. While SiC's smaller on-resistance and faster switching helps minimize energy loss and heat generation, SiC's higher thermal conductivity enables more efficient removal of waste heat energy from the active device. By increasing temperature difference between the device and the cooling ambient, SiC's ability to operate at high junction temperatures permits much more efficient cooling to take place. Heat sinks and other device-cooling hardware (i.e., fan cooling, liquid cooling, air conditioning, etc.) typically needed to keep high-power devices from overheating can be made much smaller or even eliminated.

The high breakdown field of SiC relative to silicon (Table2.1) enables the blocking voltage region (N-Drift Region in Figure 2.3) to be roughly 10 times thinner and 10 times heavier-doped, permitting a roughly 100 fold increase in on-state current density for the 3000 V SiC devices relative to 3000 V silicon devices.

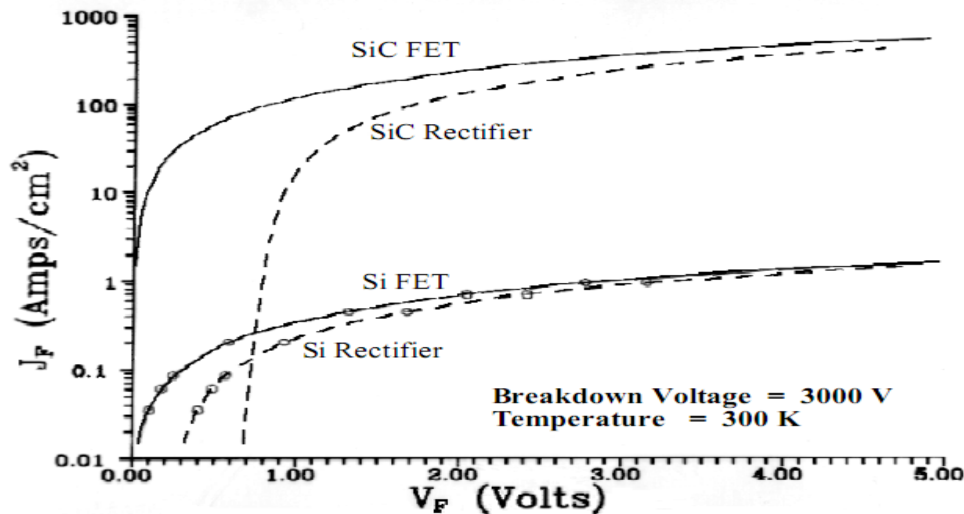

Figure2.4 Simulated forward conduction characteristics of ideal Si and SiC 3000 V power MOSFET's and Schottky rectifiers [12]

While the preceding discussion focused on high-power switching for power conversion, many of the same arguments can be applied to devices used to generate and amplify RF signals used in radar and communications applications. In particular, the high breakdown voltage and high thermal conductivity coupled with high carrier saturation velocity allow SiC microwave devices to handle much higher power densities than their silicon or GaAs RF counterparts, despite SiC's disadvantage in low-field carrier mobility.

2.4 SiC SEMICONDCUTOR CRYSTAL GROWTH

A brief historical examination quickly shows that serious shortcomings in SiC semiconductor material manufacturability and quality have greatly hindered the development of SiC semiconductor electronics. From a simple point of view, SiC electronics development has followed the general rule that a solid-state electronic device can only be as good as the semiconductor material from which it is made.

Many semiconductor materials can be melted and reproducibly recrystallized into large single-crystals with the aid of a seed crystal, such as in the Czochralski method employed in the manufacture of almost all silicon wafers, enabling reasonably large wafers to be mass produced. However, because SiC sublimes instead of melting at reasonably

attainable pressures, SiC cannot be grown by conventional melt-growth techniques. This prevented the realization of SiC crystals suitable for mass production until the late 1980's. sublimate limits the size of the SiC crystals. A modified bulk growth process, called modified sublimation, has been developed and is the preferred means to produce single crystal SiC wafers. In this method, a single crystal seed and polycrystalline SiC source container are placed in close proximity to each other in a container. The polycrystalline source container is heated to about 2400^{0}C in argon at reduced pressure (~200Pascal). The seed crystal is maintained at a temperature of 2200^{0}C, and geometry of the reactor is such that a temperature gradient of 10K cm^{-1} to 20 K cm^{-1} is maintained along the reactor walls. Under these conditions, sublimation of the polycrystalline source and subsequent nucleation and crystallization on the single crystal seed layer occur at growth rates of up to 4 mm h^{-1} [12].The modified method is currently used to produce commercial grade 4H-SiC. Limited progress has been made in producing 3C-SiC substrates in the laboratory using 3C-SiC seeds grown by chemical vapour deposition (CVD) on Si wafers. Difficulties in producing 3C-SiC wafers by sublimation method may be due to the high temperatures used in the sublimation method, which promote the crystallisation of hexagonal and rhombohedral polytypes. Polycrystalline SiC wafers can be fabricated using sintered pressed powders or using CVD.

2.4.1 Historical Lack Of SiC Wafers

Most of silicon carbide's superior intrinsic electrical properties have been known for decades. At the genesis of the semiconductor electronics era, SiC was considered an early transistor material candidate along with germanium and silicon. However, reproducible wafers of reasonable consistency, size, quality, and availability are a prerequisite for commercial mass-production of semiconductor electronics. Many semiconductor materials can be melted and reproducibly recrystallized into large single-crystals with the aid of a seed crystal, such as in the Czochralski method employed in the manufacture of almost all silicon wafers, enabling reasonably large wafers to be mass-produced [6]. SiC sublimes instead of melting at reasonably attainable pressures, therefore SiC cannot be grown by conventional melt-growth techniques. This prevented the realization of SiC crystals suitable for mass production until the late 1980's. Prior to 1980, experimental SiC electronic devices were confined to small (typically ~ 1 cm^2); irregularly shaped SiC crystal platelets grown as a by-product of the Acheson process for manufacturing industrial abrasives (e.g., sandpaper) or by the Lely process [6]. In the Lely process, SiC

sublimed from polycrystalline SiC powder at temperatures near 2500^{0}C are randomly condensed on the walls of a cavity forming small-hexagonally shaped platelets. While these small, non-reproducible crystals permitted some basic SiC electronics research, they were clearly not suitable for semiconductor mass production. As such, silicon became the dominant semiconductor fuelling the solid-state technology revolution, while interest in SiC-based microelectronics was limited.

2.5 DIFFERENT SILLICON CARBIDE DEVICES

Silicon carbide has several unique properties that can lead to enhanced performance in device. These properties include higher breakdown field, wider band gap, lower thermal generation rate, and lower intrinsic carrier concentration.

2.5.1 Silicon Carbide IMPATT Diode

Silicon carbide is an ideal semiconductor for the fabrication of high-power microwave devices due to its high breakdown field. One device, in particular, that benefit from the high breakdown field of SiC is the IMPact ionization Avalanche Transit-Time (IMPATT) diode oscillator.

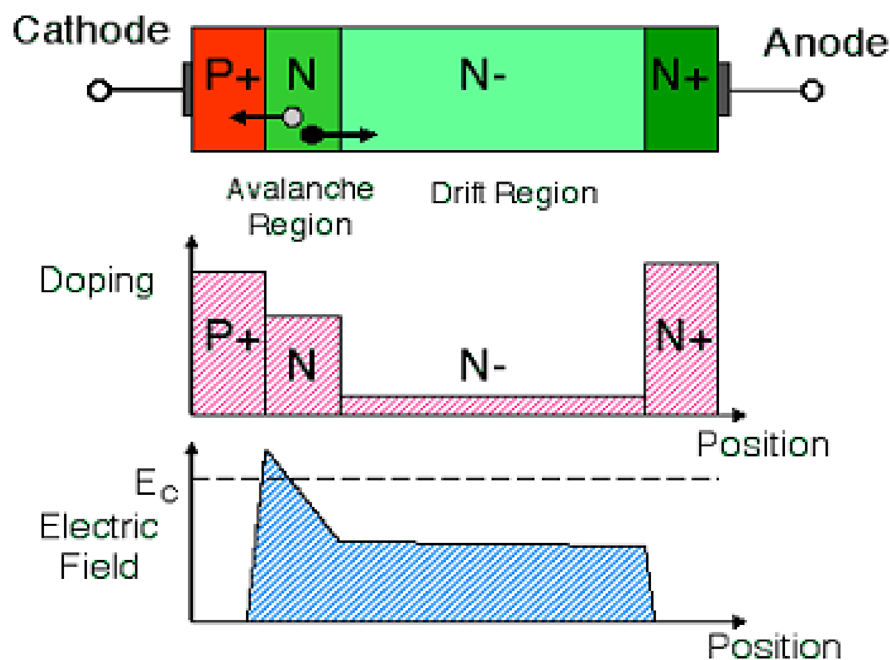

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Figure2.5 Cross section of a SiC IMPATT diode [27]

IMPATT diodes deliver the highest RF power of any semiconductor microwave oscillator, and are used to produce carrier signals for microwave transmission systems, particularly airborne and ground-based radar. Depending upon the design, IMPATT

diodes can operate from few GHz to few hundred GHz. The power-frequency product (p f2) of an IMPATT diode scales as the square of the critical field for avalanche breakdown times the electron saturation drift velocity. Hole-electron pairs are created at the point of highest electric field (the "Avalanche Region"). Holes are swept into the cathode, but electrons drift toward the anode, inducing a displacement current in the external circuit as they drift.

Figure 2.5 shows the build up of microwave oscillations in the diode current and voltage when the diode is embedded in a resonant cavity and biased at breakdown.

2.5.2 Charge Coupled Devices

Charge coupled devices (CCDs) are linear shift registers formed by a series of closely-spaced MOS plates on the surface of a semiconductor. Application of bias voltages to the MOS plates results in the creation of localized potential wells in the semiconductor under each plate. Charge packets can be confined in the potential wells and shifted along the surface under the influence of appropriate clocking waveforms applied to the gates. Silicon CCDs are widely used as image sensors, particularly in digital still cameras and hand-held video cameras. SiC is of interest as a specialized image sensor because its wide band gap makes it transparent to visible light, resulting in an ultraviolet (UV) sensor which is virtually blind to solar radiation. Such a sensor has applications in aerospace research, UV astronomy and in military systems. In this structure, the source and drain junctions and the buried n-type channel are formed by nitrogen ion implantation and the implants are activated by high temperature annealing. The gate oxide is thermally grown using the optimized conditions identified in MOS investigations. Then deposit a layer of polysilicon for the first-level gates and dope the poly with phosphorus. The polysilicon is patterned by reactive ion etching and oxidized to form a passivation layer. A second layer of polysilicon is then deposited and doped to form the second-level gates.

2.5.3 Silicon Carbide Non-volatile Memory Devices

6H silicon carbide is a single-crystal semi conducting material with a band gap of 3.0 eV. This wide band gap results in an extremely low value for the intrinsic carrier concentration in room temperature, about 16 orders of magnitude lower than silicon. Since thermal generation scales directly with the intrinsic carrier concentration, leakage currents in SiC are negligible [14].

2.5.4 Digital CMOS Integrated Circuits in 6H-SiC

CMOS technology is attractive for digital logic because it offers low power consumption, full rail-to-rail output swing, and greater noise margins than NMOS circuits. CMOS also provides active current sources for linear applications. Development of CMOS technology in SiC is expected to provide low power, high temperature circuits as well as reliable control circuitry for smart power integrated circuits. Process utilized an implanted n-well and deposited oxides, but due to other processing problems the PMOSFETs exhibited a very high threshold voltage. Implanted p-well and thermally grown oxide is used to fabricate this device. The fabrication sequence is as follows:

1. P-wells are formed on n-type epilayers doped at $8x10^{15}cm^{-3}$ by boron implantation. Al and N are then implanted through polysilicon masks to form P+ and N+ source/drain regions, respectively.

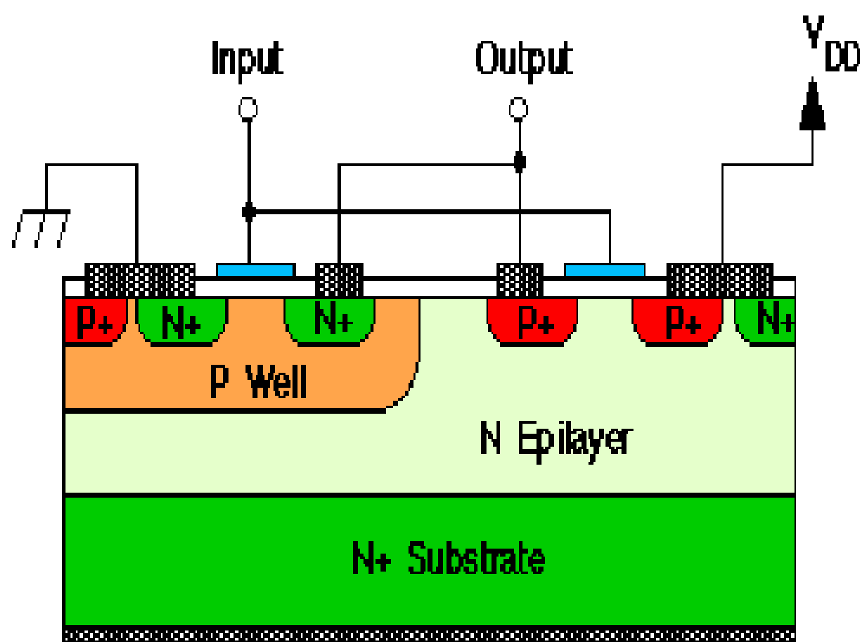

Figure 2.6 Cross section of a CMOS inverter in the implanted p-well process [2].

2. NMOSFETs are formed on p-wells while the PMOSFETs are formed on n-type epilayers. Implants are annealed at $160^{0}C$ for 40 minutes in argon, followed by an $115^{0}C$, 2 hour wet oxidation to form a 40 nm gate oxide layer.
3. Polysilicon is then deposited and patterned to form the gates. Al-Ni is used for p-type ohmic contacts and Ni for n-type contacts. A silicon oxynitride layer is deposited as an inter-metallic dielectric.
4. Vias are opened and interconnect metal is deposited and patterned.

2.5.5 Power MOSFETs

The breakdown electric field of SiC is approximately 8 times higher than silicon. This makes it possible to design power switching devices having correspondingly higher blocking voltages than their silicon counter parts. More importantly, the specific on-resistance (i.e. resistance-area product) of a power device scales inversely as the cube of the breakdown field, so the on-resistance of SiC power MOSFETs are 100-200 times lower than comparable devices in silicon [14].

2.5.6 Schottky Barrier Diodes

Schottky barrier diodes (SBD's) are attractive as power rectifiers because they do not store minority carriers in the on-state, and therefore can be switched off quickly with negligible reverse current. It is widely felt that SBD's will be the first SiC power devices to go into commercial production. The fabricated SBD's on 4H-SiC that exhibit blocking voltages of 1720 V.

CHAPTER 3

POWER MOSFETS

An increasing demand for high-voltage, high-power electronic devices and the fact that traditional silicon technology has come close to its theoretical limits in high power applications gave birth to a new era of power electronics—an era of wide bandgap semiconductors. Initial poor quality and extremely high cost of new materials made the transition between silicon and wider bandgap semiconductors like SiC and GaN very gradual; however, we are now witnessing dramatic improvements in these areas. The most significant success has been made in the field of SiC power rectifiers. Multi kilovolt 4H-SiC PiN and merged pin Schottky (MPS) diodes able to conduct hundreds of amperes of forward current were reported and 1200V, 6A Schottky diodes were introduced commercially in 2003. A dramatic improvement was also made in the field of high-power SiC switching devices. In the mid-1990s, SiC MOS transistors were projected to replace their silicon analogues in high voltage applications. Even the recently introduced Cool MOS transistor, which was expected to breathe new life into power silicon MOS technology, is unable to exceed the theoretical potential of SiC devices in this field. In this chapter, we will provide a short historic review of SiC power MOSFET development, which will help the reader estimate the speed of SiC MOS developments, and evaluate future trends in this area [5].

As with Si power MOSFET development, researchers quickly realized that success would not be rapid, but would take focused, carefully planned efforts to optimize the inversion channel mobility, device structure, and reliability. Simply copying design and process approaches from silicon technology would not lead to desired results. First of all, many of the technological processes from the silicon industry are not applicable to SiC because of different material properties. Secondly the poor interface quality between the gate oxide and SiC bulk material suppresses channel mobility to values at least an order of magnitude lower than bulk mobility. These difficulties required new design solutions to minimize the channel resistance without compromising the other components of the device on-resistance. The right choice of material polytype, crystal orientation, gate dielectric, and method of gate formation dramatically improves the device performance.

This chapter includes different design and technological approaches directed to overcome challenges in achieving the perfect device.

The power MOSFET was the first commercially successful unipolar switch developed using silicon technology. Once the issues related to the metal-oxide-semiconductor interface had been resolved for CMOS technology. In order to reduce cost, the channel in these devices was created by the double diffusion (or DMOS) process. In the DMOS process, the P-base and N^+ source regions are formed by ion implantations masked by a common edge defined by a refractory polysilicon gate electrode. A drive-in cycle is used after each ion implantation step to move the P-N junction in the lateral direction under the gate electrode. The separation between the N^+/P base junction and the P-base/N-drift junction under the gate electrode defines the channel. Consequently, the channel length can be reduced to sub-micron dimensions without the need for high resolution lithography. This approach served the industry quite well from the 1970s into the 1990s with planar power MOSFETs still available for power electronic applications. In the 1990s, the industry borrowed the trench technology originally developed for DRAMs to introduce the UMOSFET structure for commercial applications [13]. This was important for the reduction of the channel and JFET components in the MOSFET structure designed for lower (< 30 volts) voltage applications. In silicon power MOSFETs, the on-resistance becomes dominated by the resistance of the drift region when the breakdown voltage exceeds 200 volts. At high breakdown voltages, the specific on- resistance for these devices becomes greater than 10^{-2} Ohm-cm^2.

The much lower resistance of the drift region in silicon carbide should enable development of power MOSFETs with very high breakdown voltages. These devices offer not only fast switching speed but also superior safe operating area when compared to high voltage silicon IGBTs. This allows reduction of both the switching loss and conduction loss components in power circuits. Unfortunately, the power MOSFET structures developed in silicon cannot be directly utilized to form high performance silicon carbide devices. Firstly, the lack of significant diffusion of dopants in silicon carbide prevents the use of the silicon DMOS process. Secondly, a high electric field occurs in the gate oxide of the silicon carbide MOSFET exceeding its rupture strength leading to catastrophic failure of devices in the blocking mode at high voltages. Thirdly, when compared with silicon, the smaller band offset between the conduction band of silicon carbide and silicon dioxide can produce injection of hot carriers into the oxide leading to instability during operation. In addition, the quality of the oxide-semiconductor

interface for silicon carbide must be improved to allow good control over the threshold voltage and the channel mobility [16].

Power MOSFET can be classified under the following headings:

- Double implanted or DIMOSFET
- UMOSFET
- Lateral or LDMOSFET

3.1 SiC UMOSFET

The classical U-groove n-channel power MOSFET transistor (UMOSFET) in SiC is a vertical device, which comprises epitaxially grown thick n- drift region and p-type base region. N+ source and p+ body contact regions can be either epitaxially grown or implanted. Dry plasma etch is used to form a trench, and a thin dielectric layer is then thermally grown or deposited followed by metal or polysilicon gate deposition to define a vertical MOS channel. A simplified cross section of n-channel UMOSFET is shown in Figure 3.1.

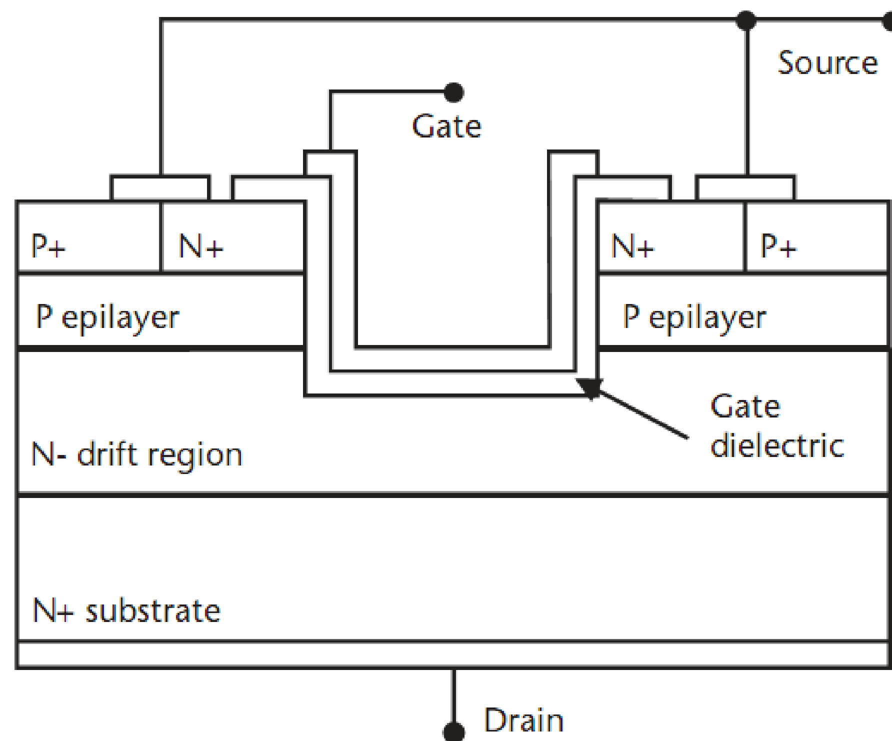

Figure 3.1 Schematic cross section of a classical UMOSFET [5].

UMOSFETs are attractive because the base and source regions are formed epitaxially without the need for ion implantation and associated high temperature annealing. In UMOSFETs, the MOS channel is formed on the sidewalls of trenches created by reactive ion etching.

SiC UMOSFET has two serious problems:

1. A high electric field occurs in the gate oxide caused by higher electric fields in the SiC drift region. This problem occurs at the trench corners leading to catastrophic failure of the gate oxide at higher drain voltages, thus restricting the maximum operating voltage to less than 40% of ideal breakdown voltage.
2. The low inversion layer mobility along the trench sidewalls results in high specific on resistance, which nullifies the advantage of low drift region in SiC. By 1995, UMOSFET fabricated on the carbon face of SiC had achieved the breakdown voltage of about 260V.

Potentially, 4H-SiC UMOS transistor structure offers several advantages over other design solutions as follows:

- ➢ Vertical configuration, where the absence of JFET region allows for taking maximum advantage from excellent blocking/conductive properties of the SiC drift layer.
- ➢ Relatively simple structure that can be made using self-aligned fabrication process resulting in a significant increase of channel packing density.
- ➢ The doping profiles in the entire device structure can be realized by epitaxial growth.

One of the most important issues preventing commercialization of power SiC MOSFETs so far is MOS channel resistance that results from the extremely low inversion channel mobility in 4H-SiC. This problem may become especially significant in the case of 4H-SiC UMOSFET, where the oxide-semiconductor interface is severely damaged by plasma etch when the trenches are formed. In general, there are two major approaches to minimize the channel component of on-resistance:

• Improve channel mobility.

• Increase channel packing density.

Increasing channel packing density can be achieved either by use of high-precision lithography or/and by implementing self-aligned fabrication process. Due to today's low production volume of power SiC switches, use of expensive photo lithographic equipment may not be economically feasible. On the other hand, unlike double diffused MOSFET (DMOS) configuration, SiC UMOS transistor structure is ideally suitable for self-aligned fabrication processes that can be adopted from the silicon industry. For example, scaling down a pitch width from today's 15 µm to 1 µm is very realistic. Such increase in the channel packing density would be equivalent to a 15-fold increase in inversion channel mobility, which may not be feasible in the near future. Another benefit that can be realized from down scaling the pitch width is the reduction of the electric field in the gate

oxide. It has been shown that by closely spacing the UMOS trenches, the electric field enhancement at the trench corners can be partially eliminated, which allows the use of thinner and heavier doped drift region. So the increase in the packing density is a powerful tool to reduce the overall resistance of the UMOS structure. One of the potential benefits of SiC UMOSFET, low cost and easy to manufacture device structure.

3.2 Double implanted MOSFET

Power switching devices are reaching the upper limits imposed by low breakdown field of silicon, and high breakdown voltage can be achieved only by using a semiconductor with a higher breakdown field. SiC is unique among compound semiconductors since its native oxide is SiO_2, the same oxide as of silicon. This means that power devices used in silicon can all be fabricated in SiC. Here we will discuss double implanted MOS (DMOS) as shown in Figure3.2. DMOS transistors are common in silicon power device technology where the p-base and n+ source regions are formed by diffusion of impurities through a common mask opening. However, impurity diffusion is impractical in SiC because of the very low diffusion coefficients at any temperature. The Purdue group fabricated the first DMOS transistors in SiC using ion implantation to introduce dopants for the p-base and the n+ source. The implanted DMOSFET requires that separate masks be used to define the p-base and the n+ source. The construction is a vertical structure with a drift layer built on a highly conductive n+ layer. The n-drift region is designed to give the forward blocking capabilities (Figure 3.2). The forward blocking capability is achieved by the pn junction between p-base region and n-drift region [5].

In power MOSFET, the blocking voltage is supported across the drift layer, and thus the drift- region resistance is considered to be the minimum possible theoretical limit for the on-resistance of a MOSFET. For an ideal DIMOSFET, the resistances associated with the n+ source, the n-channel, the accumulation region and the n+ substrate are assumed to be negligible and the specific on-resistance of the power MOSFET is determined by the drift region only. This assumption is not accurate at lower breakdown voltages where the drift region resistance R_D is comparable to the other resistive components and these resistances should be included in calculating Ron-sp. However, at higher break- down voltages, R_D is significantly higher than other resistances and R_{on-sp} can be approximated by R_D. The details of the device structure are shown in Figure3.2.

During the device operation, a fixed potential to the p-base region is established by connecting it to the source metal by the break in the n+ source region.

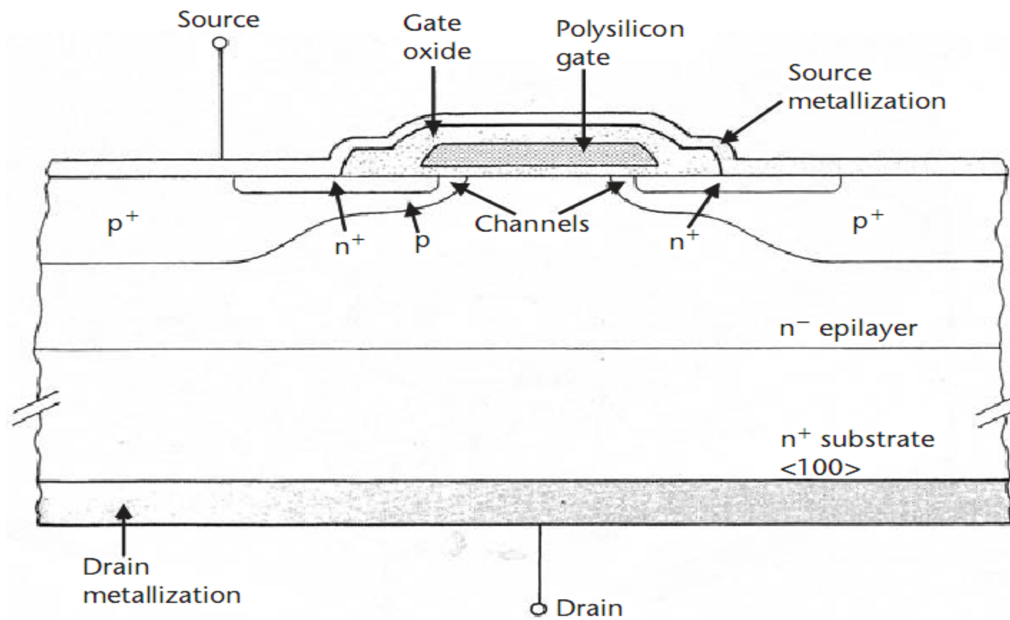

Figure 3.2 Schematic illustration of classical VDMOS transistor [5].

By short-circuiting the gate to the source and applying a positive bias to the drain, the p-base/n-drift region junction becomes reverse-biased and this junction supports the drain voltage by the extension of depletion layer on both sides.

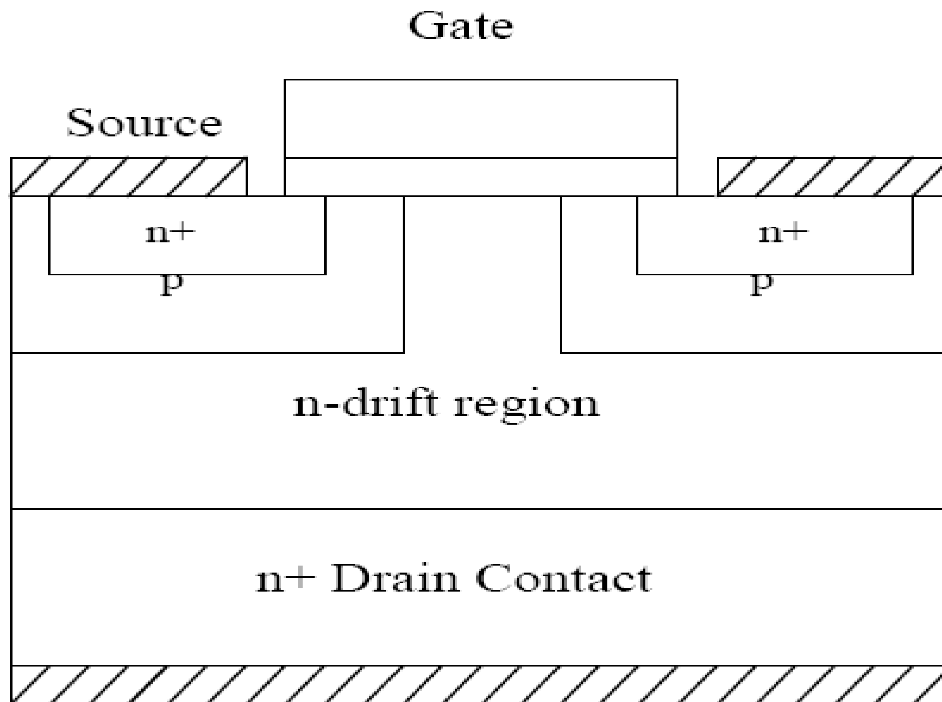

Figure 3.3 Structure of DIMOSFET [18]

However, due to the higher doping level of the p-base layer, the depletion layer extends primarily into the n-drift region. On applying the positive bias to the gate electrode, the conductive path between the n+ source region and the n-drift region is formed.

The application of positive drain voltage results in a current flow between drain and source through the n-drift region and conductive channel. The conductivity of the channel is modulated by the gate bias voltage and the current flow is determined by the resistance of various resistive components [18].

In a power MOSFET, the blocking voltage appears across the drift layer and so the drift-region resistance is considered to be the minimum possible theoretical value for the on-resistance of a MOSFET. For an ideal DIMOSFET, the resistances associated with the n+ source, the n-channel, the accumulation region and the n+ substrate are usually neglected and the specific on-resistance of the power MOSFET is determined by the drift region alone.

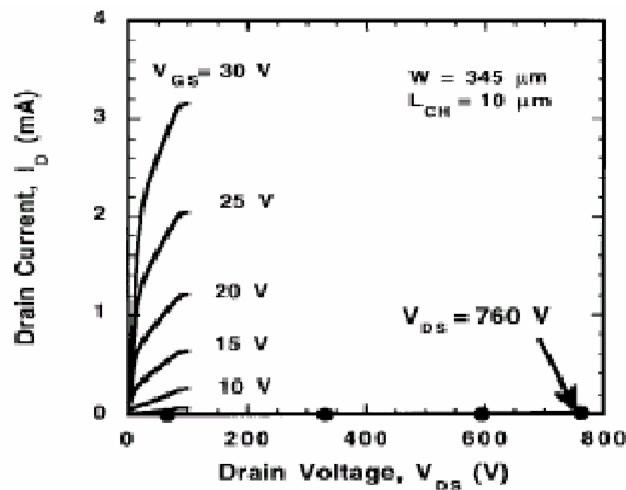

Figure 3.4 (V-I) characteristics of DIMOSFET [12]

SiC DIMOSFETs have been fabricated with the blocking voltage of 760V. To obtain the blocking voltage greater than 760 V for 6H-SiC depends on the drift region thickness, doping level, specific on-resistance and electric field strength. By adjusting all these parameters we propose to get the blocking voltage greater than 760V. The safe operating area of MOSFET is divided into three regions: (i) maximum permissible drain current, (ii) maximum power dissipation limit, and (iii) maximum drain source voltage limit. The safe operating area of MOSFET does not contain any second breakdown as seen in the BJT. This is because of the majority carriers present in the MOSFET.

3.3 Lateral MOSFET

Before the advent of power devices of SiC, MOSFETs and thyristors had been fabricated as vertical structures with the substrate acting as an anode. In the off state, the voltage was blocked by a reverse-biased pn junction. To achieve high blocking voltage, the drift region should be lightly doped and thick. For a given device thickness, there was a maximum possible blocking voltage regardless of doping. For SiC lateral MOSFETs with a 10 μm drift region, the maximum possible voltage is 1600V. To overcome the limitations of vertical-type MOSFETs, lateral- type MOSFET is used. The structure of lateral DMOSFET is as shown in Figure 3.5. It can be observed that the insulating substrate is of SiC. In the blocking state, the depletion layer spreads mainly into the lightly-doped drift region. Once the depletion region reaches the insulating substrate, it continues spreading toward the drain. Here, the maximum voltage is not limited by the thickness of the layer. Figure3.6 shows the current voltage characteristics of lateral DMOSFET. From the characteristics, it is observed that the device withstands a maximum drain voltage of 2.6kV. One can say that the device should be implemented laterally rather than vertically because there is no necessity for an increase of surface area required for the device.

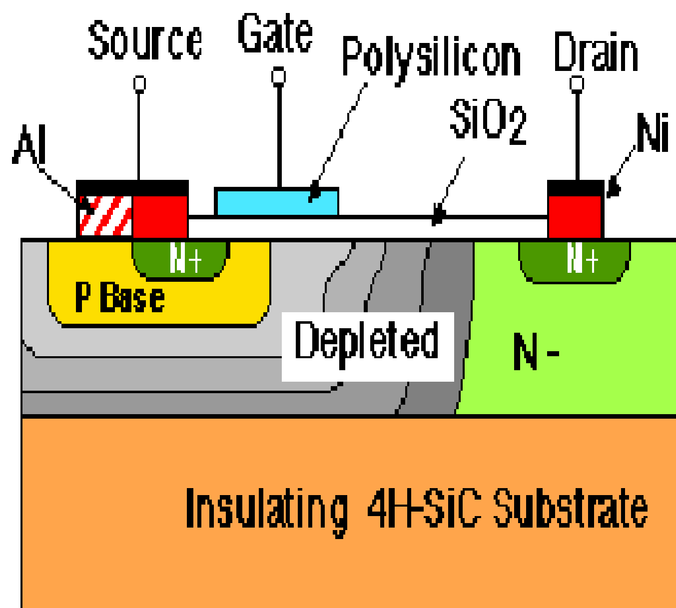

Figure 3.5. Cross section of lateral MOSFET [19]

As in the case of vertical devices, the drift region component of the total LDMOS' specific on-resistance depends on its dimensions and doping concentration.

To reduce this component while maintaining the same blocking capability, a junction-isolation RESURF (REduced SURface Field) technology can be used. The RESURF effect is the result of the depletion region in the lateral n-type drift layer being generated by both the vertical and lateral p-n junctions. This yields a reduction of the electric field peaks that occur at the surface, leading to a considerable increase in the blocking voltage.

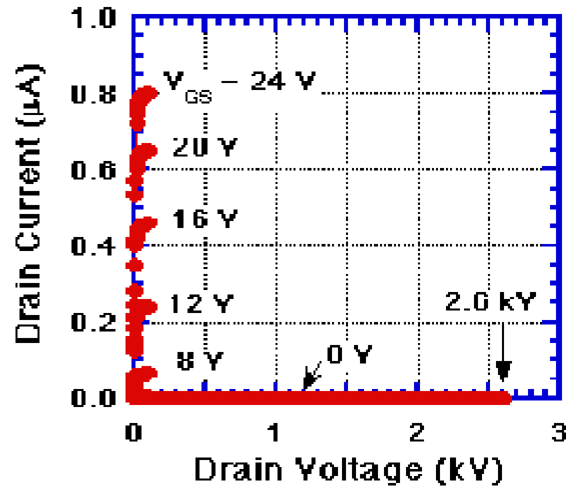

Figure 3.6 (V-I) Characteristics of lateral DMOSFET at room temperature [19]

The closest to the market power SiC MOSFET structures are vertical 4H-SiC DMOS-like transistors, which are now under intense investigation by leading SiC device developers. Increasing channel packing density by implementing self-aligned fabrication processes and advanced layout solutions in conjunction with sophisticated gate oxide growth/annealing techniques will help to overcome such traditional issues for SiC MOSFETs as inversion channel mobility and gate oxide reliability.

Significant progress has been achieved recently in the development of a power LDMOS for smart power electronics. Due to its high inversion channel mobility (several times higher than that in 4H-SiC)and relatively high electron mobility, 6H-SiC has appeared to be an excellent building material for lateral MOS devices such as LDMOS. The higher inversion channel mobility in 6H-SiC compared with that in 4H-SiC results from almost an order of magnitude lower interface state density than in 4H-SiC due to its higher conduction band offset to SiO. In general, the high value of the conduction band offset with related issues such as inversion channel mobility and gate oxide reliability renewed interest in alternative polytypes to 4H-SiC and 6H- SiC such as 3C-SiC and 15R-SiC. These polytypes also exhibit high operating electric field and high bulk electron mobility, which makes them very attractive for future SiC MOSFET development. So far, high-

quality 3C-SiC and 15R-SiC substrates are not commercially available; however, potential advantages of these polytypes as building materials for SiC MOS devices may induce future efforts toward their commercial bulk growth.

CHAPTER.4

ANALYSIS OF 3C-SiC VERTICAL DOUBLE IMPLANTED MOSFET USING COMPLEMENTARY ERROR FUNCTION PROFILE

The 3C-SiC is a promising material for MOSFET devices because of high channel mobility due to lower density of interface states compared to 4H-SiC. Poor performance of 6H-SiC and 4H-SiC MOSFETs is related to the interface states located in the band gap close to the conduction band edge limiting the transport of electrons in the channel. Due to the smaller band gap of 3C-SiC, the interface states observed in 6H-SiC and 4H-SiC are located in the conduction band and have no effect on the transport properties of the channel. The 3C-SiC polytype has lower critical electric field value due to the lower band gap. It means that the drift region doping corresponding to a given blocking voltage will be lower compared to the hexagonal 4H-SiC and 6H-SiC polytypes. This also means that the specific junction capacitance will be lower in the 3C-SiC devices as compared to the 4H-SiC and 6H-SiC ones. This is an advantage from the point of view of high speed MOSFETs.

The 3C-SiC DIMOSFET need for high breakdown voltage analysis has a complementary profile as its impurity content in the drift region. The profile can be generated by ion-implantation from the drain end of the device, so that the projected R_P is close to the drain end of the device. The impurity concentration decays upwards from R_P as we approach the source. The mathematical analysis for evaluation the effective impurity concentration (N_{eff}) has been evaluated by integrating the complementary function error profile over the length of the drift region.

4.1 Basic Structure of 3C-SiC DIMOSFET

When operating the device, the p-base region is connected to the source metal by a break in the N^+ source region and a fixed potential is given to the p-base region. The gate and source are short circuited and a positive bias is applied to the drain. The p-base and N-drift region form a reverse biased p-n junction and this junction supports the drain voltage across the junction depletion region. Since the p-region is more heavily doped than the N-drift region, the depletion region is wider in the drift region than the p-base region. Then for a positive bias applied to the gate, an inversion channel is generated on top of p-region which allows an electron current to flow from N^+ source. At the edge of the p-base region

and N-drift region near the surface and beneath the gate an accumulation layer is forward. This provides a second conducting path for the electron current which then enters the N-drift region and eventually flows to the drain. Between the accumulation and drift regions there exists an in-built n-channel JFET which has its own channel resistance.

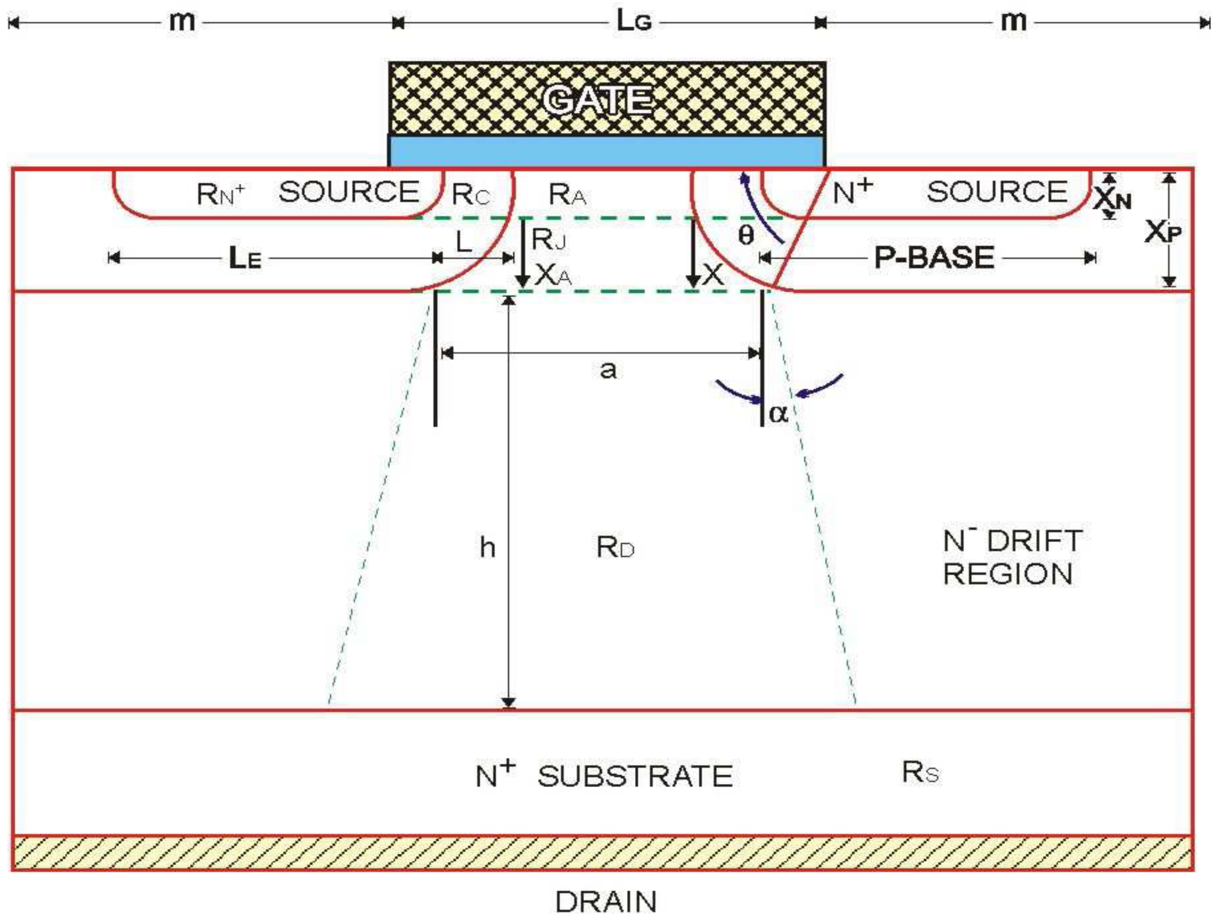

Figure4.1 Basic Structure of DIMOSFET [18]

The specific on resistance of the device $R_{on\text{-}sp}$ is given by

$$R_{on\text{-}sp} = R_{N+} + R_C + R_A + R_J + R_D + R_S \quad (4.1)$$

Where,

R_{N+} is the contribution from the N^+ source region,

R_C is the channel resistance,

R_A is the accumulation layer resistance,

R_J is the resistance of the JFET pinch off region,

R_D is the drift region resistance and,

R_S is the substrate resistance

These components are shown in Figure 4.1 and the unit of $R_{on\text{-}sp}$ is $\Omega\text{-}Cm^2$. The blocking voltage is supported across the drift layer and serves as the minimum possible theoretical

limit for the on resistance of a power MOSFET. Also at high applied voltages, resistance of the device is approximately equal to R_D as all other terms on the RHS of eq. (4.1) are negligible as compared to R_D and so, $R_{on\text{-}sp} \approx R_D$. At lower values of V_B or smaller drain bias, equation (4.1) will have to be evaluated as considering all components on the RHS of that equation. This is because all of them are comparable to each other at these values of drain voltages, i.e. $V_{DS} \ll V_B$.

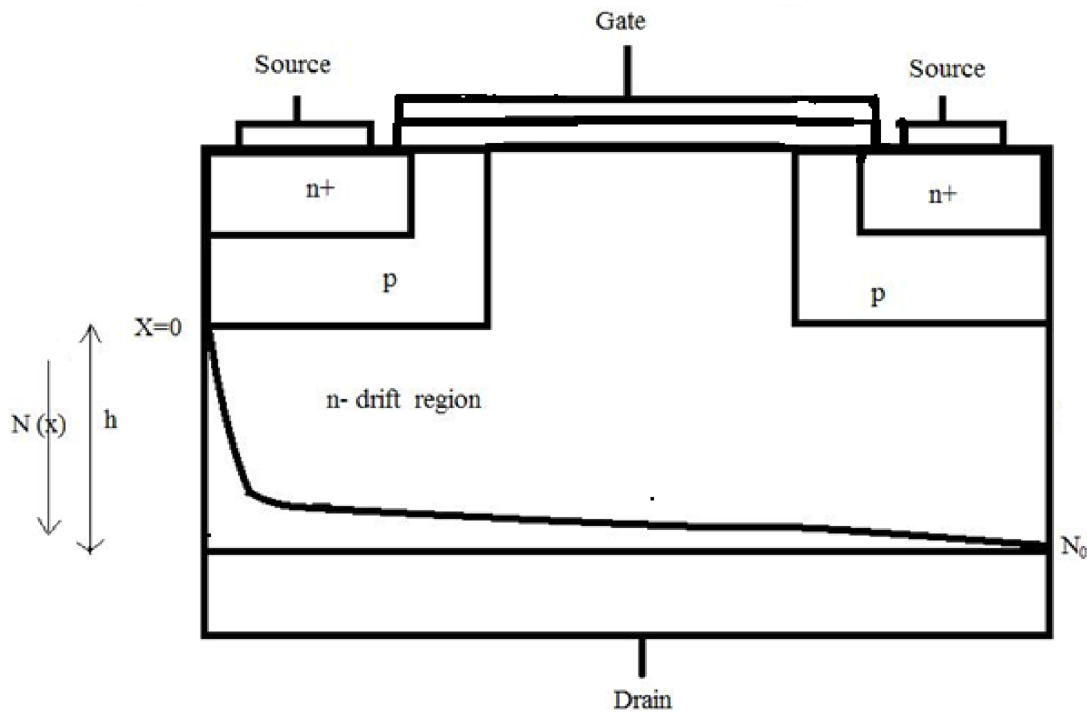

Figure4.2 Structure of DIMOSFET using Complementary error function profile

Structure of DIMOSFET using complementary error function profile is shown in figure 4.2. Suppose carrier concentration is N_0 at x=0 in the complementary function type of doping profile. Carrier concentration,

$$N(x) = N_0\,(erfc(h-x)) \tag{4.2}$$

Where erfc is complementary error function, h is the distance between source and drain of DIMOSFET.

$$erfc(h-x) = 1 - erf\,(h-x) \tag{4.3}$$

or,

$$erfc(h-x) = 1 - \frac{2}{\sqrt{\pi}}\left[(h-x) - \frac{(h-x)^3}{3\times 1!} + \ldots\ldots\ldots\right] \tag{4.4}$$

4.2 BASIC DEVICE EQUATIONS

Using Poisson's Equation,

$$-\frac{\partial^2 V}{\partial x^2} = \frac{\rho}{\varepsilon} \tag{4.5}$$

Where $\mathcal{E}$ is permittivity of semiconductor, ρ is electric charge density and V is potential developed in drift region.

We know,

$$\rho = eN(x) \tag{4.6}$$

Where N(x) is the doping distribution

Put equation (4.4) into (4.3)

$$-\frac{\partial^2 V}{\partial x^2} = \frac{eN(x)}{\varepsilon} \tag{4.7}$$

Put equation (4.2) into (4.7),

$$-\frac{\partial^2 V}{\partial x^2} = \frac{eN_0(erfc(h-x))}{\varepsilon} \tag{4.8}$$

From Equation (4.5) and (4.8),

$$-\frac{\partial^2 V}{\partial x^2} = \frac{eN_0}{\varepsilon}[1 - \frac{2}{\sqrt{\pi}}\{(h-x) - \frac{(h-x)^3}{3\times 1\ !} + \ldots\ldots\}] \tag{4.9}$$

After expanding $(h-x)^3$,

$$-\frac{\partial^2 V}{\partial x^2} = \frac{eN_0}{\varepsilon}[1 - \frac{2}{\sqrt{\pi}}\left\{(h-x) - \frac{1}{3}(h^3 - x^3 - 3xh^2 + 3x^2h)\right\} \tag{4.10}$$

Integrate equation (4.10),

$$-\frac{\partial V}{\partial x} = \frac{eN_0}{\varepsilon}\left[x - \frac{2}{\sqrt{\pi}}\left\{\left(hx - \frac{x^2}{2}\right) - \frac{1}{3}\left(h^3x - \frac{x^4}{4} - \frac{3x^2h^2}{2} + \frac{3x^3h}{3}\right)\right\}\right] + C1 \tag{4.11}$$

We know,

$$-\frac{\partial V}{\partial x} = E \tag{4.12}$$

Where E is the electric field developed in drift region of DIMOSFET.

Using Boundary condition,

At x=h, E=0 (4.13)

From Equation (4.11), (4.12) and (4.13),

We get,

$$C1 = -\frac{eN_0}{\varepsilon}[h - \frac{2}{\sqrt{\pi}}\left\{\frac{h^2}{2} - \frac{1}{3}\left(\frac{h^4}{4}\right)\right\}] \quad (4.14)$$

Putting Equation (4.14) into (4.12)

$$-\frac{\partial V}{\partial x} = \frac{eN_0}{\varepsilon}\left[x - \frac{2}{\sqrt{\pi}}\left\{\left(hx - \frac{x^2}{2}\right) - \frac{1}{3}\left(h^3x - \frac{x^4}{4} - \frac{3x^2h^2}{2} + \frac{3x^3h}{3}\right)\right\}\right] - \frac{eN_0}{\varepsilon}[h - \frac{2}{\sqrt{\pi}}\left\{\frac{h^2}{2} - \frac{1}{3}\left(\frac{h^4}{4}\right)\right\}]$$

(4.15)

After integrating equation (4.15)

$$-V = \frac{eN_0}{\varepsilon}\left[\frac{x^2}{2} - \frac{2}{\sqrt{\pi}}\left\{\frac{x^2}{2}h - \frac{x^3}{6} - \frac{1}{3}\left(\frac{x^2}{2}h^3 - \frac{x^5}{20} - \frac{x^3}{2}h^2 + \frac{x^4}{4}h\right)\right\}\right] - \frac{eN_0}{\varepsilon}\left[hx - \frac{2}{\sqrt{\pi}}\left\{\frac{x}{2}h^2 - \frac{x}{12}h^4\right\}\right] + C2$$

(4.16)

Using boundary condition:

{At x = 0, V = 0}

From boundary condition, we get

C2 = 0

Now equation (4.16) becomes:

$$-V = \frac{eN_0}{\varepsilon}\left[\frac{x^2}{2} - \frac{2}{\sqrt{\pi}}\left\{\frac{x^2}{2}h - \frac{x^3}{6} - \frac{1}{3}\left(\frac{x^2}{2}h^3 - \frac{x^5}{20} - \frac{x^3}{2}h^2 + \frac{x^4}{4}h\right)\right\}\right] - \frac{eN_0}{\varepsilon}\left[hx - \frac{2}{\sqrt{\pi}}\left\{\frac{x}{2}h^2 - \frac{x}{12}h^4\right\}\right]$$

(4.17)

From Boundary conditions,

{At x = w, V = Vbi}

Where w is depletion region width and Vbi is built in potential.

Put x=w in equation (4.16)

$$-V_{bi} = \frac{eN_0}{\varepsilon}\left[\frac{w^2}{2} - \frac{2}{\sqrt{\pi}}\left\{\frac{w^2}{2}h - \frac{w^3}{6} - \frac{1}{3}\left(\frac{w^2}{2}h^3 - \frac{w^5}{20} - \frac{w^3}{2}h^2 + \frac{w^4}{4}h\right)\right\}\right] - \frac{eN0}{\varepsilon}\left[hw - \frac{2}{\sqrt{\pi}}\left\{\frac{w}{2}h^2 - \frac{w}{12}h^4\right\}\right]$$

(4.18)

After solving equation (4.18), we get

$$V_{bi} = \frac{eN_0}{\varepsilon}\left[\frac{w^5}{30\sqrt{\pi}} - \frac{w^4 h}{6\sqrt{\pi}} + w^3\left\{\frac{h^2}{3\sqrt{\pi}} - \frac{1}{3\sqrt{\pi}}\right\} - w^2\left\{\frac{1}{2} - \frac{h}{\sqrt{\pi}} + \frac{1}{3\sqrt{\pi}}h^3\right\} + w\left\{h - \frac{1}{2}h^2 + \frac{h^4}{6\sqrt{\pi}}\right\}\right]$$

(4.19)

Rearranging equation (4.19), we get

$$\frac{V_{bi}\varepsilon}{eN_0} = \left[\frac{w^5}{30\sqrt{\pi}} - \frac{w^4 h}{6\sqrt{\pi}} + w^3\left\{\frac{h^2}{3\sqrt{\pi}} - \frac{1}{3\sqrt{\pi}}\right\} - w^2\left\{\frac{1}{2} - \frac{h}{\sqrt{\pi}} + \frac{1}{3\sqrt{\pi}}h^3\right\} + w\left\{h - \frac{1}{2}h^2 + \frac{h^4}{6\sqrt{\pi}}\right\}\right]$$

(4.20)

In Reverse bias, Equation (4.20) reduces to –

$$\frac{(V_R+V_{bi})\varepsilon}{eN_0} = \left[\frac{w^5}{30\sqrt{\pi}} - \frac{w^4 h}{6\sqrt{\pi}} + w^3\left\{\frac{h^2}{3\sqrt{\pi}} - \frac{1}{3\sqrt{\pi}}\right\} - w^2\left\{\frac{1}{2} - \frac{h}{\sqrt{\pi}} + \frac{1}{3\sqrt{\pi}}h^3\right\} + w\left\{h - \frac{1}{2}h^2 + \frac{h^4}{6\sqrt{\pi}}\right\}\right]$$

(4.21)

In reverse bias condition,

$$V_R >>> Vbi$$

So equation (4.21) reduces to,

$$\frac{V_R\varepsilon}{eN_0} = \left[\frac{w^5}{30\sqrt{\pi}} - \frac{w^4 h}{6\sqrt{\pi}} + w^3\left\{\frac{h^2}{3\sqrt{\pi}} - \frac{1}{3\sqrt{\pi}}\right\} - w^2\left\{\frac{1}{2} - \frac{h}{\sqrt{\pi}} + \frac{1}{3\sqrt{\pi}}h^3\right\} + w\left\{h - \frac{1}{2}h^2 + \frac{h^4}{6\sqrt{\pi}}\right\}\right]$$

(4.22)

At the breakdown point,

$$V_R = V_B \tag{4.23}$$

Where V_B is the breakdown voltage

$$\frac{V_B \varepsilon}{e N_0} = [\frac{w^5}{30\sqrt{\pi}} - \frac{w^4 h}{6\sqrt{\pi}} + w^3 \left\{\frac{h^2}{3\sqrt{\pi}} - \frac{1}{3\sqrt{\pi}}\right\} - w^2 \left\{\frac{1}{2} - \frac{h}{\sqrt{\pi}} + \frac{1}{3\sqrt{\pi}} h^3\right\} + w \left\{h - \frac{1}{2} h^2 + \frac{h^4}{6\sqrt{\pi}}\right\}] \tag{4.24}$$

$$\text{Impurity gradient } \alpha = \frac{dN}{dx} \tag{4.25}$$

From Equation (4.2)

$$\alpha = \frac{d(N_0 \operatorname{erfc}(h-x))}{dx} \tag{4.26}$$

Put value of erfc(h-x) from equation (4.4) in to this equation (4.26) and neglecting higher order terms

$$\alpha = \frac{2}{\sqrt{\pi}} N_0 \tag{4.27}$$

Critical Electric field is Electric field developed at breakdown point. The value of critical electric field

$$E_c = 1.95 \times 10^4 \times N_0^{0.131} \tag{4.28}$$

The breakdown voltage VB for uniform doping profile can be calculated from the equation,

$$V_B = (E_c W)/2 \tag{4.29}$$

CHAPTER.5

CALCULATION AND RESULTS

In calculating the Breakdown voltage, we have used the following parameters with the value quoted against each of them:

Doping concentration $N_0 = 1\times10^{15}$ /cm^3

Permittivity of free space$\mathcal{E}_0 = 8.85\times10^{-14}$ $(\Omega\text{-cm})^{-1}$sec

Permittivity of SiC semiconductor $\mathcal{E}_s = 9.7\ \mathcal{E}_0$

Electron charge e=1.6×10^{-19} coulomb

Let us suppose, punch through breakdown voltage V_B = 10 kV,

We know that for punch through breakdown, Depletion region width is equal to maximum height between source and drain, or we can say,

$$w=h$$

Put this condition in to equation (4.24)

$$\frac{V_B\varepsilon}{eN_0} = [\frac{h^5}{30\sqrt{\pi}} - \frac{h^5}{6\sqrt{\pi}} + h^3\left\{\frac{h^2}{3\sqrt{\pi}} - \frac{1}{3\sqrt{\pi}}\right\} - h^2\left\{\frac{1}{2} - \frac{h}{\sqrt{\pi}} + \frac{1}{3\sqrt{\pi}}h^3\right\} + h\left\{h - \frac{1}{2}h^2 + \frac{h^4}{6\sqrt{\pi}}\right\}] \quad (5.1)$$

After simplifying this equation,

$$5.36\times10^{-5} = 0.018806h^5 - 0.18806h^3 + 0.5h^2 \quad (5.2)$$

After solving it, we get,

h= 103.78 μm.

So we should take minimum height of source and drain 103.78μm.

Now take Breakdown voltage V_B= 1 kV, the value of depletion region width can be calculated from equation (4.24)

$$5.36\times10^{-6} = [\frac{w^5}{30\sqrt{\pi}} - \frac{w^4}{6\sqrt{\pi}}h + w^3\left\{\frac{h^2}{3\sqrt{\pi}} - \frac{1}{3\sqrt{\pi}}\right\} - w^2\left\{\frac{1}{2} - \frac{h}{\sqrt{\pi}} + \frac{1}{3\sqrt{\pi}}h^3\right\} + w\left\{h - \frac{1}{2}h^2 + \frac{h^4}{6\sqrt{\pi}}\right\}] \quad (5.3)$$

Put value of h into this equation,

$$5.36\times10^{-6} = 0.0188w^5 - 0.000968w^4 - 0.188w^3 - 0.4942w^2 + 0.0102w \quad (5.4)$$

After solving this equation we get,

$$w = 5.5\mu m \quad (5.5)$$

Breakdown voltage for uniform doping profile, $V_{AB} = \frac{1}{2} wEc$ (5.6)

So for w = 5.5 μm,

$V_{AB} = 0.5$ kV.

Now take Breakdown voltage $V_B = 2$ kV, the value of depletion region width can be calculated from equation (4.24)

$$10.72 \times 10^{-6} = \left[\frac{w^5}{30\sqrt{\pi}} - \frac{w^4}{6\sqrt{\pi}}h + w^3\left\{\frac{h^2}{3\sqrt{\pi}} - \frac{1}{3\sqrt{\pi}}\right\} - w^2\left\{\frac{1}{2} - \frac{h}{\sqrt{\pi}} + \frac{1}{3\sqrt{\pi}}h^3\right\} + w\left\{h - \frac{1}{2}h^2 + \frac{h^4}{6\sqrt{\pi}}\right\}\right]$$

Put value of h into this equation

$$5.36 \times 10^{-6} = 0.0188w^5 - 0.00097w^4 - 0.188w^3 - 0.4942w^2 + 0.0102w$$

After solving this equation we get,

$$w = 11.5\mu m \quad (5.7)$$

So for w = 11.5 μm

$V_{AB} = 1$ kV.

Now take Breakdown voltage $V_B = 3$ kV, the value of depletion region width can be calculated from equation (4.24),

$$5.36 \times 10^{-6} = \left[\frac{w^5}{30\sqrt{\pi}} - \frac{w^4}{6\sqrt{\pi}}h + w^3\left\{\frac{h^2}{3\sqrt{\pi}} - \frac{1}{3\sqrt{\pi}}\right\} - w^2\left\{\frac{1}{2} - \frac{h}{\sqrt{\pi}} + \frac{1}{3\sqrt{\pi}}h^3\right\} + w\left\{h - \frac{1}{2}h^2 + \frac{h^4}{6\sqrt{\pi}}\right\}\right]$$

(5.8)

Put value of h into this equation

$$16.08 \times 10^{-6} = 0.0188w^5 - 0.00097w^4 - 0.188w^3 - 0.4942w^2 + 0.0102w \quad (5.9)$$

After solving this equation we get,

$$w = 17.5\mu m$$

$V_{AB} = 1.5$kV.

Similarly, for $V_B = 4$kV,

$$w = 24.5\mu m$$

$V_{AB} = 2.2$kV.

For V_B= 5kV,

$$w = 32.3\mu m$$

V_{AB} = 3.0 kV.

For V_B = 6kV,

$$w=40.2\ \mu m$$

V_{AB} = 3.5 kV.

For V_B= 7kV,

$$w = 50.4\ \mu m$$

V_{AB} = 4.4 kV.

For V_B=8kV,

$$w= 62.6\ \mu m$$

V_{AB} = 5.5 kV.

For V_B=9kV

$$w= 80.7\ \mu m$$

V_{AB} = 7.12 kV.

For V_B = 10 kV

$$w= 103.78\ \mu m$$

V_{AB} = 9.16 kV.

Effective doping concentration,

$$N_{eff} = \frac{2N_0}{\sqrt{\pi}}\left\{\frac{\sqrt{\pi}}{2} - \frac{h}{2}\right\} \tag{5.10}$$

Critical Electric field Ec = $1.95\times10^4\times (N_{eff})^{(0.131)}$ V/cm

$$E_c = 1.8\times10^6\ V/cm$$

Table 5.1 Variation of depletion region width with Breakdown voltage

S.N.	Breakdown Voltage(V)	Depletion region width (w)(μm)	$V_{AB} = 0.5 \times w\times E_c$(kV)
1	1000	5.5	0.5
2	2000	11.5	1.0
3	3000	17.5	1.5
4	4000	24.5	2.2
5	5000	32.3	3.0

6	6000	40.2	3.5
7	7000	50.4	4.4
8	8000	62.6	5.5
9	9000	80.7	7.12
10	10000	103.7	9.16

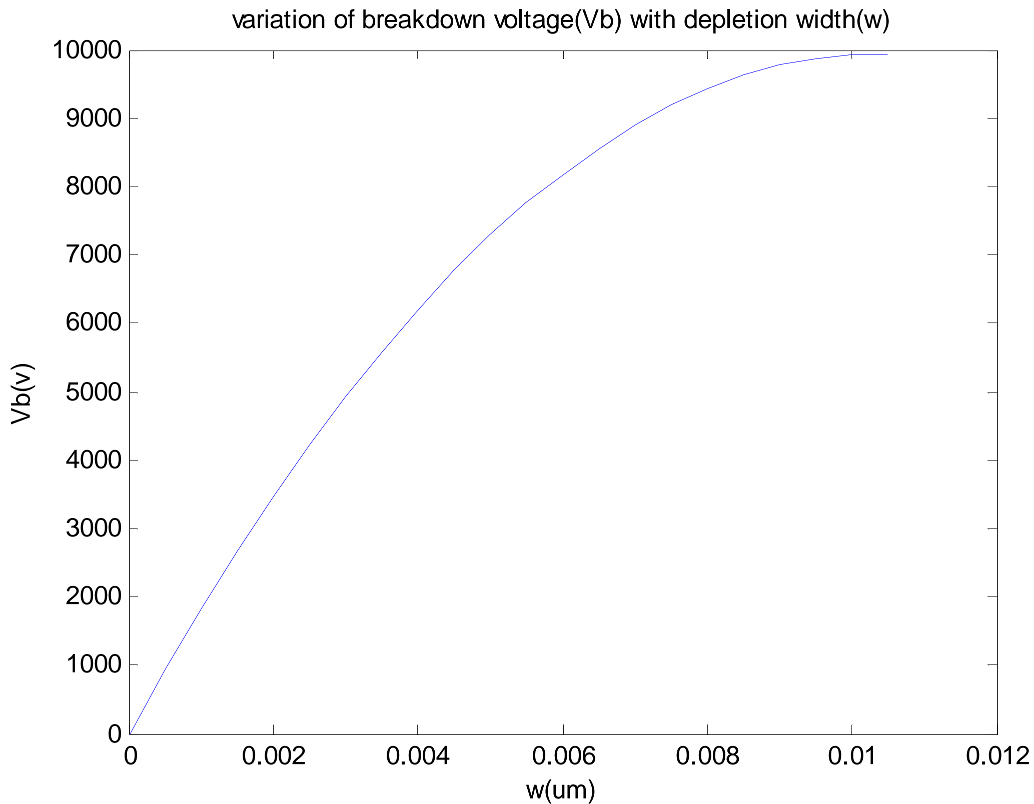

Figure 5.1 Plot of breakdown voltage with variation of depletion width

5.1 Calculation of depletion region width with different value of h:

For h= 100 µm

From equation (4.24)

$$\frac{V_B \varepsilon}{eN_0} = [\frac{w^5}{30\sqrt{\pi}} - \frac{w^4}{6\sqrt{\pi}}h + w^3\left\{\frac{h^2}{3\sqrt{\pi}} - \frac{1}{3\sqrt{\pi}}\right\} - w^2\left\{\frac{1}{2} - \frac{h}{\sqrt{\pi}} + \frac{1}{3\sqrt{\pi}}h^3\right\} + w\left\{h - \frac{1}{2}h^2 + \frac{h^4}{6\sqrt{\pi}}\right\}]$$

Put value of h into this equation,

$$\frac{V_B \varepsilon}{eN_0} = 0.018806w^5 - 9.4 \times 10^{-4}w^4 - 0.18804w^3 - 0.4943w^2$$

$$+9.9 \times 10^{-3} w \tag{5.11}$$

Put V_B=1kV, and solve the equation (5.6),

w = 5.56 µm

Similarly for V_B = 2 kV, w = 11.4 µm,

For V_B = 3kV, w = 17.83 µm,

For V_B = 4kV, w = 24.7 µm,

For V_B = 5kV, w = 32.27 µm,

For V_B =6kV, w=40.81 µm,

For V_B = 7kV, w = 50.81 µm

For V_B = 8kV, w = 63.48 µm

For V_B = 9kV, w = 84.45 µm

For h= 200 µm

From equation (4.24)

$$\frac{V_B \varepsilon}{e N_0} = [\frac{w^5}{30\sqrt{\pi}} - \frac{w^4 h}{6\sqrt{\pi}} + w^3 \left\{\frac{h^2}{3\sqrt{\pi}} - \frac{1}{3\sqrt{\pi}}\right\} - w^2 \left\{\frac{1}{2} - \frac{h}{\sqrt{\pi}} + \frac{1}{3\sqrt{\pi}} h^3\right\} + w\left\{h - \frac{1}{2}h^2 + \frac{h^4}{6\sqrt{\pi}}\right\}]$$

Put value of h into this equation,

$$\frac{V_B \varepsilon}{e N_0} = 0.018806w^5 - 1.8806 \times 10^{-3} w^4 - 0.18794w^3 - 0.4888w^2 + 0.01977w \tag{5.12}$$

Put V_B=1kV, and solve the equation (5.7),

w = 2.729 µm

Similarly for V_B = 2 kV, w = 5.49 µm,

For V_B = 3kV, w = 8.30 µm,

For V_B = 4kV, w = 11.15 µm,

For V_B = 5kV, w = 14.04 µm,

For V_B =6kV, w=16.98 µm,

For V_B = 7kV, w = 19.96 µm,

For V_B = 8kV, w = 22.98 µm,

For V_B = 9kV, w = 26.08 µm,

For V_B = 10kV, w = 29.22µm.

For h= 300 μm

From equation (4.24)

$$\frac{V_B \varepsilon}{eN_0} = [\frac{w^5}{30\sqrt{\pi}} - \frac{w^4}{6\sqrt{\pi}} h + w^3 \left\{\frac{h^2}{3\sqrt{\pi}} - \frac{1}{3\sqrt{\pi}}\right\} - w^2 \left\{\frac{1}{2} - \frac{h}{\sqrt{\pi}} + \frac{1}{3\sqrt{\pi}} h^3\right\} + w\left\{h - \frac{1}{2}h^2 + \frac{h^4}{6\sqrt{\pi}}\right\}]$$

Put value of h into this equation,

$$\frac{V_B \varepsilon}{eN_0} = 0.018806w^5 - 2.8 \times 10^{-3} w^4 - 0.18789w^3 - 0.48308w^2 + 0.029429w \quad (5.13)$$

Put $V_B = 1$kV, and solve the equation (5.8),

w = 1.8 μm

Similarly for $V_B = 2$ kV, w = 3.657 μm,

For $V_B = 3$kV, w = 5.5023 μm,

For $V_B = 4$kV, w = 7.3589μm,

For $V_B = 5$kV, w = 9.227μm,

For $V_B =6$kV, w=11.1075 μm,

For $V_B = 7$kV, w = 12.99 μm,

For $V_B = 8$kV, w = 14.904 μm,

For $V_B = 9$kV, w = 16.821 μm,

For $V_B = 10$kV, w = 18.75 μm.

For h= 350 μm

From equation (4.24)

$$\frac{V_B \varepsilon}{eN_0} = [\frac{w^5}{30\sqrt{\pi}} - \frac{w^4}{6\sqrt{\pi}} h + w^3 \left\{\frac{h^2}{3\sqrt{\pi}} - \frac{1}{3\sqrt{\pi}}\right\} - w^2 \left\{\frac{1}{2} - \frac{h}{\sqrt{\pi}} + \frac{1}{3\sqrt{\pi}} h^3\right\} + w\left\{h - \frac{1}{2}h^2 + \frac{h^4}{6\sqrt{\pi}}\right\}]$$

Put value of h into this equation,

$$\frac{V_B \varepsilon}{eN_0} = 0.018806w^5 - 32.91 \times 10^{-4} w^4 - 0.18783w^3 - 0.48025w^2 + 0.0343w \quad (5.14)$$

Put V_B=1kV, and solve the equation (5.9),

w = 1.52 μm

Similarly for V_B = 2 kV, w = 3.12 µm,

For V_B = 3kV, w = 4.71 µm,

For V_B = 4kV, w = 6.306 µm,

For V_B = 5kV, w = 7.90 µm,

For V_B =6kV, w = 9.50 µm,

For V_B = 7kV, w = 11.11 µm,

For V_B = 8kV, w = 12.72 µm,

For V_B = 9kV, w = 14.35 µm,

For V_B = 10kV, w = 15.98 µm

For h= 400 µm

From equation (4.24)

$$\frac{V_B \varepsilon}{eN_0} = \left[\frac{w^5}{30\sqrt{\pi}} - \frac{w^4}{6\sqrt{\pi}} h + w^3 \left\{\frac{h^2}{3\sqrt{\pi}} - \frac{1}{3\sqrt{\pi}}\right\} - w^2 \left\{\frac{1}{2} - \frac{h}{\sqrt{\pi}} + \frac{1}{3\sqrt{\pi}} h^3\right\} + w\left\{h - \frac{1}{2}h^2 + \frac{h^4}{6\sqrt{\pi}}\right\}\right]$$

Put value of h into this equation,

$$\frac{V_B \varepsilon}{eN_0} = 0.018806w^5 - 37.61 \times 10^{-4} w^4 - 0.18776w^3 - 0.47744w^2 + 0.03909w \qquad (5.15)$$

Put V_B=1kV, and solve the equation (5.9),

w = 1.373 µm

Similarly for V_B = 2 kV, w = 2.7511 µm,

For V_B = 3kV, w = 4.133 µm,

For V_B = 4kV, w = 5.521 µm,

For V_B = 5kV, w = 6.913 µm,

For V_B =6kV, w = 8.310 µm,

For V_B = 7kV, w = 9.771 µm,

For V_B = 8kV, w = 11.11 µm,

For V_B = 9kV, w = 12.53 µm,

For V_B = 10kV, w = 13.947 µm

Table 5.2 Variation of breakdown voltage with depletion region width (w) for different values of h

S.N.	V_B(V)	h = 100 μm w(μm)	h = 200 μm w(μm)	h = 300 μm w(μm)	h = 350 μm w(μm)	h = 400 μm w(μm)
1	1000	5.56	2.72	1.8	1.52	1.37
2	2000	11.4	5.49	3.65	3.12	2.75
3	3000	17.83	8.30	5.50	4.71	4.13
4	4000	24.71	11.15	7.36	6.31	5.52
5	5000	32.27	14.04	9.23	7.90	6.91
6	6000	40.81	16.98	11.11	9.50	8.31
7	7000	50.81	19.96	12.99	11.11	9.71
8	8000	63.48	22.99	14.91	12.72	11.11
9	9000	84.45	26.08	16.82	14.35	12.53
10	10000		29.22	18.75	15.98	13.97

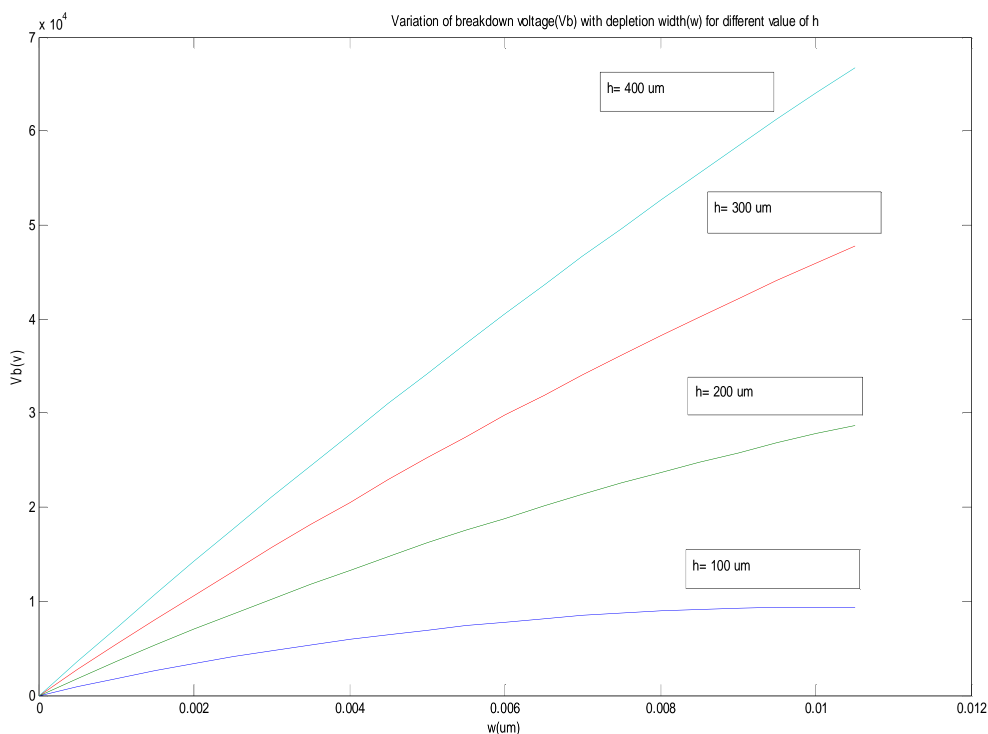

Figure 5.2 Plot of breakdown voltage with variation of depletion width for different value of height (h).

Table 5.3 Variation of breakdown voltage with depletion region width (w) for different value of doping level

S.N.	Depletion region width(w)(µm)	Breakdown voltage(Vb)(V) N0(1*10^14)	Breakdown voltage(Vb)(V) N0(1*10^15)	Breakdown voltage(Vb)(V) N0(1*10^16)
1	0.0001	19.36	193.62	1936.29
2	0.0011	202.86	2028.67	20286.70
3	0.0016	287.71	2877.19	28771.90
4	0.0021	367.97	3679.75	36797.51
5	0.0031	514.70	5147.08	51470.82
6	0.0041	643.08	6430.87	64308.77
7	0.0051	753.13	7531.34	75313.41
8	0.0061	844.86	8448.68	84486.87
9	0.0071	918.31	9183.12	91831.24
10	0.0081	973.48	9734.86	97348.63
11	0.0091	1010.41	10104.11	101041.14
12	0.0101	1029.10	10291.08	102910.87

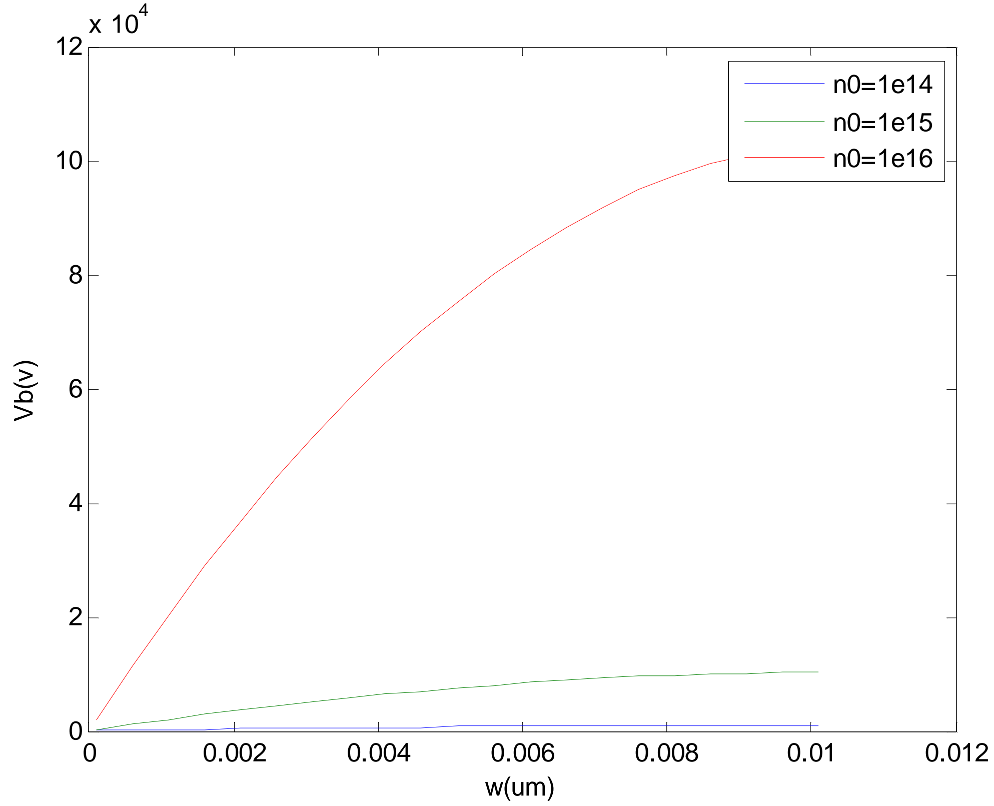

Figure 5.3 Plot of breakdown voltage with depletion region width for different doping level (N_0)

Table 5.4 Variation of breakdown voltage with height (h) for w=95µm

S.N.	**Height(h)(µm)**	**Breakdown voltage(V)**
1	100	9320.9028
2	150	18097.2177
3	200	26823.9577
4	250	35501.1291
5	300	44128.7409

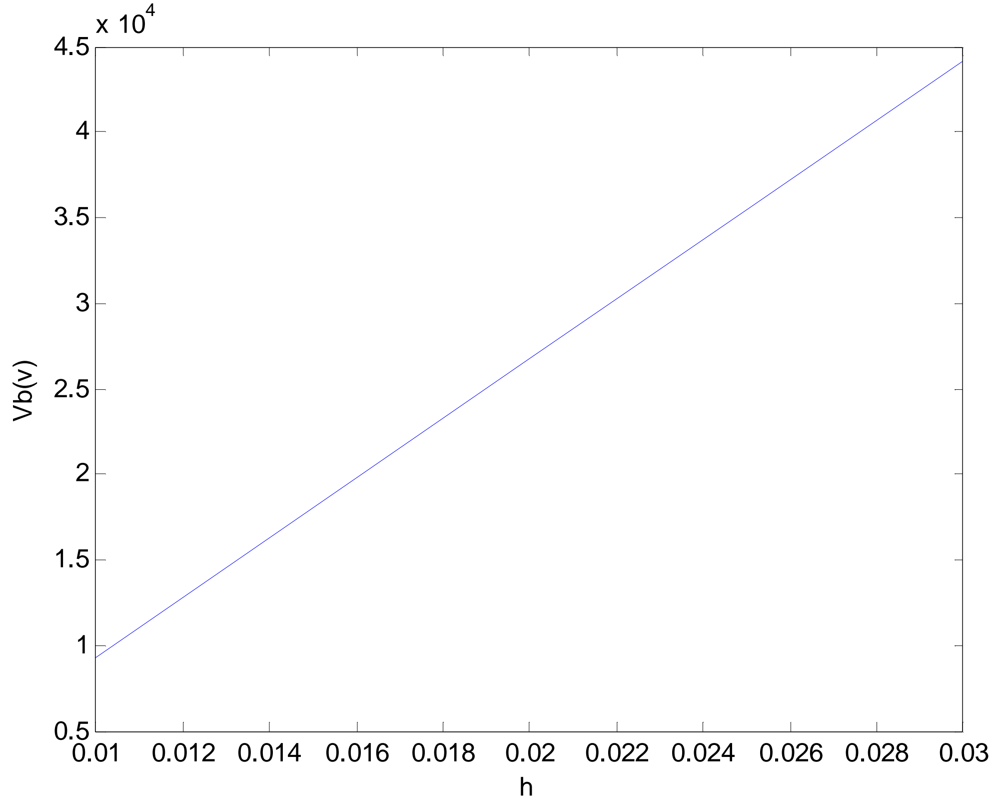

Figure 5.4 Variation of breakdown voltage with height (h)

Table 5.5 Variation of breakdown voltage with different doping level (N_0)

S.N.	**N_0(/cm^3)**	**For h=100µm Breakdown voltage(V)**	**For h=200 µm Breakdown voltage(V)**	**For h=300 µm Breakdown voltage(V)**
1	1e14	924.20	2581.92	4220.85
2	1e15	10152.80	28363.47	46367.81
3	1e16	96867.41	270614.66	442393.20
4	1e17	924207.61	2581922.2	4220853.50

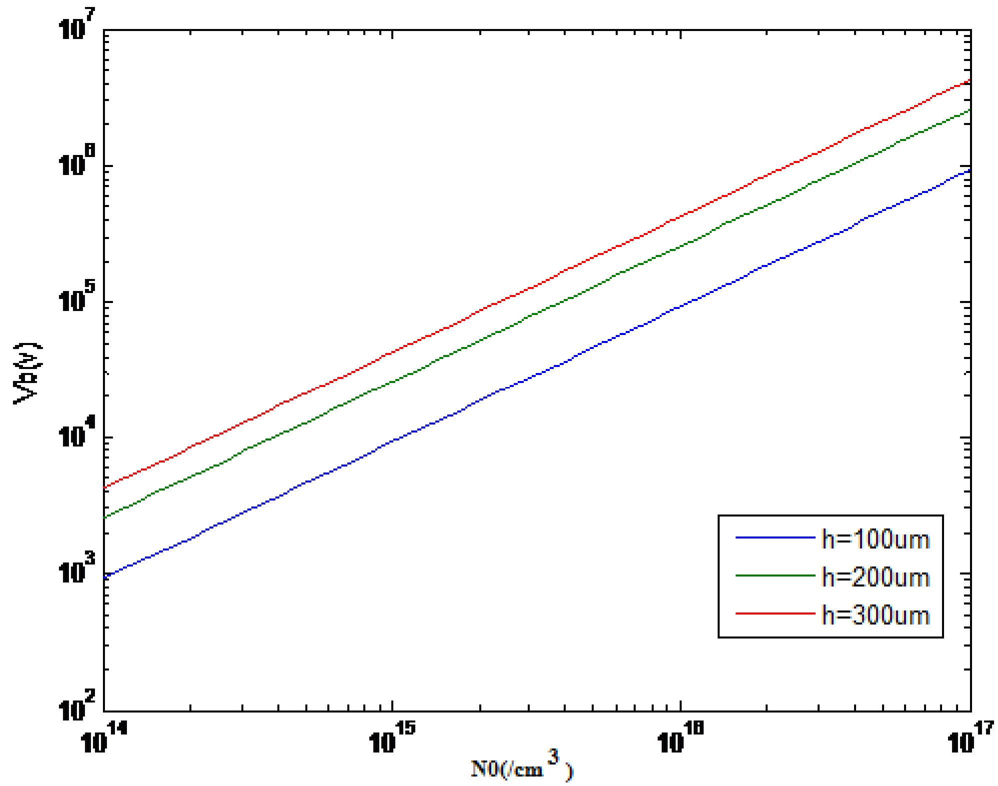

Figure 5.5 Plot of variation of breakdown voltage with different doping levels (N_0)

Table 5.6 Variation of breakdown voltage (Vb) with drift region height (h) for different value of doping level (N_0)

S.N.	**Height(h) (µm)**	**Breakdown Voltage(Vb)(V) for Doping level (N_0)(1e14/cm^3)**	**Breakdown Voltage(Vb)(V) for Doping level (N_0)(1e15/cm^3)**	**Breakdown Voltage(Vb)(V) for Doping level (N_0)(1e16/cm^3)**
1	100	924.20	9242.07	92420.76
2	200	2581.92	25819.22	258192.22
3	300	4220.85	42208.53	422085.35

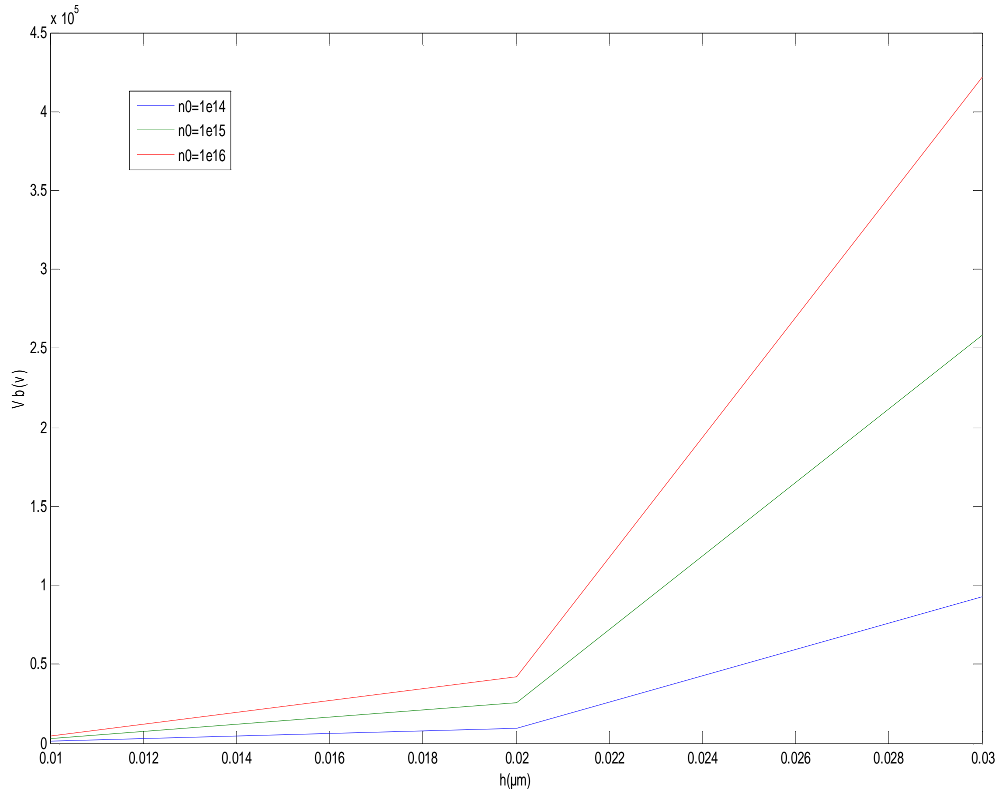

Figure 5.6 Plot of variation of breakdown voltage with drift region height (h) for different value of doping level

CHAPTER 6

CONCLUSION AND FUTURE WORK

The equation for breakdown voltage for 3C-SiC Vertical DIMOSFET, using Complementary error function doping profile in drift region, was derived. Equation showed that the value of Breakdown voltage depends on height (h) of drift region and doping level. For different values of height (h), breakdown voltages (Punch through and Avalanche) and its corresponding depletion region width was calculated and was plotted in Figure 5.2. For the drift region height h=103µm, $N_{eff} = 1\times10^{15}$ cm^{-3}, the punch through breakdown voltage was found to be 10kv and at the same point Avalanche breakdown voltage was 9.2kV. Hence, Avalanche breakdown will occur before punch through. For different value of doping level, the breakdown voltage was calculated and plotted in Figure 5.3. It was seen from Figure 5.4 that by with increase in drift region height, Breakdown voltage was found to increases.

For the same height, breakdown voltage for other doping profiles like uniform, linearly graded could be calculated and could be compared with the complementary error function profile results given in this work. For larger drift region height, depletion region width is very small even for higher breakdown voltages and it could be improved further.

REFERENCES

[1] Md Hasanuzzaman, Syed K. Islam, Leon M. Tolbert, Burak Ozpineci , "Design, Modeling, Testing, And Spice Parameter Extraction Of Dimos Transistor In 4h-Silicon Carbide" , (26 May 2005).

[2] Munish Vashishath and Ashoke K. Chatterjee, "Recent trends in silicon carbide device research", Mj. Int. J. Sci. Tech. 2008, 2(03), 444-470.

[3] S. Sridevan, P. K. Mclarty, and B. J. Baliga, "On the presence of aluminum in thermally grown oxides on 6H-silicon carbide power MOSFETs", IEEE Electron Device Lett., 1996, 71, 136- 138.

[4] Mietek Bakowski, Adolf Schöner, Per Ericsson, Helena Strömberg, Hiroyuki Nagasawa,and Masayuki Abe, "Development of 3C-SiC MOSFETs", Journal of Telecommunication and information Technology,2/2007.

[5] Stephen E. Saddow, Anant Agarwal, "Advances in Silicon Carbide Processing and Applications".

[6] Philip G. Neudeck , "SiC TECHNOLOGY (1998)", NASA Lewis Research Center.

[7] Akira Itoh, Hiroyuki Matsunami, "Critical reviews in solid state and Materials Sciences", 22(2) (1997)111-197.

[8] Kent Bertilsson, "Simulation and Optimization of SiC Field Effect Transistors".

[9] M. Roschke, F. Schwiertz, "Electron mobility Models for 4H, 6H, and 3C SiC", IEEE trans. Elec. Dev. Vol. 48, No. 7, 2001, pp1442-1447.

[10] V. Dimitrev, S. Trendakova, N. Kuznetsov, N. Savkina, A. Andreev, M. Rastegaeva, M. Mynbaeva, A. Morozov, "Large area silicon carbide devices fabricated on SiC wafers with reduced micropipe density", Mtrl. Sci. and Eng. B61-62, 1999, pp. 446-449.

[11] Sze, S. M., Physics of Semiconductor Devices, 2nd. edition, Wiley-Interscience, New York.

[12] Bhatnagar, M. and Baliga, B. J., “Comparison of 6H-SiC, 3C-SiC, and Si” for v Proceedings of the IEEE, 82, 1112, 1994. Power Devices, IEEE Transactions on Electron Devices, 40, 645, 1993.

[13] Baliga, B. J., “Modern Power Devices”, 1st, John Wiley & Sons, Inc., New York, 1987.

[14] W.Xie, J.A.Cooper, Jr., M.R.Melloch, J.W.Palmour and C.H.Carter, Jr.,"A Vertically Integrated Bipolar Storage Cell in 6H Silicon Carbide for Nonvolatile Memory Applications, "IEEE Electron Device Lett., 15,212(1994).

[15] http://www.ecn.purdue.edu/WBG/SiC Data Bank, Introduction, Basic Studies, Device Research: From the Purdue’s Wide Band Gap Semiconductor Device Research in Electrical and Computer Department, America.

[16] B.Jayant Baliga, “Silicon Carbide power devices”, World Scientific publication.

[17] Baliga, B. J., Prospects For Development of SiC Power Devices, Silicon Carbide and Related Materials 1995, Institute of Physics Conference Series, 142, Nakashima, S. Matsunami, H., Yoshida, S. and Harima, H., Eds., IOP Publishing, Bristol, United Kingdom, 1996.

[18] Munish Vashishath and Dr. A. K. Chatterjee, “Theoretical analysis and design of double implanted MOSFET on 6H silicon carbide wafer for low power dissipation and large breakdown voltage”, Mj. Int. J. Sci. Tech. 2008, 2(02), 308-319.

[19] J.Spits, M.R.Melloch, J.A.Cooper, Jr. And M.A.Capano,"High-Voltage (2.6kV) Lateral DMOSFETs in 4H-SiC," IEEE Electron Device Lett., 19,100(1998).

[20] J.N.Shenoy, M.R.Melloch, and J.A.Cooper, Jr., “High-Voltage Double-Implanted MOS Power Transistors in 6H-SiC,” IEEE Device Research Conf., Santa Barbara, CA, June 24-26 , 1996.

[21] J.N.Shenoy, J.A.Cooper,Jr., and M.R.Melloch, “High-Voltage Double-Implanted Power MOSFETs in 6H-SiC,”IEEE Electron Device Lett.,18,93(1997).

[22] D. J. Larkin, P. G. Neudeck, J. A. Powell, and L. G. Matus, 5th Int. Conf. On Silicon Carbide and Related Matls, Washington, DC, USA, 1993; Inst. Phys. Conf. Ser. No. 137 (1994) 51.

[23] E. Janzen, 6th Int. Conf. on Silicon Carbide and Related Matls., Kyoto, Japan,1995.

[24] T. Kimoto, A. Itoh, H. Matsunami, T. Nakata, and M. Watanabe, J. Elec. Matls.,(1995).

[25] C. Weitzel, J. Palmour, C. Carter, K. Moore, K. Nordquist, S. Allen, C. Thero, and M. Bhatnagar, “Silicon carbide high-power devices”, IEEE Trans. Electron Devices, 1996, 43, 1732-1741.

[26] S.C.Sunand, J.D.Pulmmer, “Modeling of the on-resistance of LDMOS, VDMOS, and VMOS power transistors,” IEEE Transaction on Electron Devices, vol.27, pp.356-367, 1980.

[27] L.Yuan, M.R.Melloch, J.A.Cooper and K.J.Webb, "Silicon Carbide IMPATT Oscillators for High-Power Microwave and Millimeter-Wave Generation, "IEEE Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, Ithaca, NY,August7-9,2000.