TO STUDY THE DESIGN AND ANALYSIS OF OPERATIONAL AMPLIFIER

Thesis submitted towards the partial fulfilment of the requirements for the award of degree of

Master of Technology

In

VLSI Design

Submitted by

Soumen Chatterjee

Roll. No. 601361027

Under the supervision of

Dr. Mayank Kumar Rai

Assistant Professor, ECED

Department of Electronics & Communication Engineering

Thapar University, Patiala

INDIA

June, 2015

DECLARATION

I hereby declare that the work which is being presented in the thesis entitled, **"To study the design and analysis of operational amplifiers"** in partial fulfillment of the requirement for the award of degree of M.Tech (VLSI Design) at Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Dr. Mayank Kumar Rai, Assistant Professor, ECED.

The matter presented in this thesis has not been submitted in any other University/ Institute for the award of my degree.

Date: 23/6/15

Soumen Chatterjee

Enroll. No. 601361027

It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

Date: 23/6/15

Dr. Mayank Kumar Rai

Assistant Professor

ECED, Thapar University

Counter signed by:

Dr. Sanjay Sharma

Professor & Head

ECED, Thapar University

Patiala- 147004

Dr. S. S. Bhatia

Dean of Academic Affairs

Thapar University

Patiala- 147004

ACKNOWLEDGEMENT

I take this opportunity to express my profound sense of gratitude and respect to all those who helped me through the duration of this thesis. I would have never succeeded in completing my task without the cooperation, encouragement and help provided to me by various people. Words are often too less to reveal one's deep regards. I acknowledge with gratitude and humility my indebtedness to **Dr. Mayank kumar Rai, Assistant Professor**, Electronics and Communication Engineering Department, Thapar University, Patiala, under whose guidance I had the privilege to complete this thesis. I wish to express my deep gratitude towards him for providing individual guidance and support throughout the thesis work.

I convey my sincere thanks to **HEAD OF THE DEPARTMENT, Dr. Sanjay Sharma** as well as **PG Coordinator, Dr. Amit Kohli** Associate Professor, **Programme Coordinator, Dr. Anil Arora** Assistant Professor**,** Electronics and Communication Engineering Department, entire faculty and staff of Electronics and Communication Engineering Department for their encouragement and cooperation.

My greatest thanks to all who wished me success especially my parents and other family members and friends without whom I would not have been able to complete my thesis work.

I thank and own my deepest regards to all of them and all others who have helped me directly or indirectly.

Date: **SOUMEN CHATTERJEE**

(601361027)

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LIST OF ABBREVIATIONS AND SYMBOLS

Symbol	Quantity	Units
Vi	Input voltage	V
Vo/Vout	Output voltage	V
ωu/Wu	Unity gain frequency	$Time^{-1}$
Ve	Error voltage	Volts
t	Time	Corresponding unit of time
S	Laplace domain	-
jω	ω-plane, jω is the Y axis	Radians
Vtest	Input voltage test signal	V
Vreturn	Return at given terminal for input Vtest provided	V
Gm	Trans-conductance	Ω^{-1}
Ao	Open loop DC gain	Db.
Go	Output admittance	Ω^{-1}
Gds	Drain to source conductance	Ω^{-1}
µn	Mobility of electron	$cm^2/V - sec$
Zo	AC impedance	Z∟Ɵ
Rds	Drain to source resistance	Ω
Cgd	Gate to drain capacitance of MOS transistor	f
Cgs	Gate to source capacitance	f
Cdb	Drain to bulk capacitance	f
Ios	Offset current	A
Cox	Normalized oxide capacitance	f/m^2
CMRR	Common mode rejection ratio	Db.
Cl	Load capacitance	f
Id	Drain Current	A
L	Channel length	µm
W	Channel Width	µm
PSRR	Power supply rejection ratio	Db.
Vtn	Threshold voltage of n-type MOS transistor	V
Vtp	Threshold voltage of n-type MOS transistor	V
Vcm	Common mode input voltage	V
Vdd	Power supply	V
VDSAT	Drain to source voltage	V
Vgs	Gate to source voltage of n-type	V
Vsg	Gate to source voltage of p-type	V

ABSTRACT

Operational Amplifiers (op-amps) have been in use for a long time. They are very versatile. They have the performance levels which are closed to ideal.

As a part of the thesis work, a two stage fully differential telescopic operational amplifier and a two stage fully differential folded cascode operational amplifier have been designed and compared at 180 nm technology node. Here the unity gain frequency and the slew rate of both the amplifiers are maintained same. Such an effort is made so as to bring about a comparison of their various parameters viz. voltage gain, phase margin, common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), output swing and power consumption. The following parameters of the telescopic two stage amplifier were found to be superior as compared to its folded cascade counterpart viz. voltage gain, CMRR, PSRR and low power applications. Whereas the folded cascode two stage gives better results in terms of bandwidth and output swing limit.

Keywords: Operational Amplifier, Telescopic, Folded Cascode, Output Swing.

CHAPTER 1

INTRODUCTION

In this chapter the background and motivation behind the two stage fully differential operational amplifier is discussed. It also consists of various applications of the above mentioned amplifier.

1.1 Background

With the advancement of IC process technologies, modern electronic system requirements and the circuit integration economics, constrains are imposed which have created new challenges in the field of analog circuit design. The demand for lower voltage analog circuit designs is created due to the advancement of CMOS process technologies and the increasing popularity of battery powered mobile electronic systems. Both the analog and digital circuitry systems are now forcefully integrated onto a single die so as to reduce the system costs. Such an integration is bringing about a detrimental impact upon the analog circuit performance. Both the peak SNR and the dynamic range of an analog circuit gets degraded due to the reduction in the power supply voltage. Further degradation in the analog performance happens due to the integration of analog circuitry and the noisy digital circuitry on the same die. This degradation actually occurs due to noise injection through a common power supply and/or power distribution network, the die substrate and/or capacitive coupling between conductors.

In order to enable higher performance in the processing of analog signals in today’s environment, various analog design methodologies and techniques have been devised on the electronic components. Operational amplifiers are one of such components. First coming to the purpose of designing the amplifier with two stages. The two stage operational amplifier has huge number of practical applications where the requirement of high gain-bandwidth product and low output power dissipation are inevitable. The high voltage gain is obtained by the product of the gains of two individual stages which are associated to one another by means of compensation capacitor or the Miller Capacitor and a nulling resistor. The Miller Capacitor plays a dominating role in pole splitting the dominant and the non-dominant poles so as to increase the bandwidth and stability of the amplifier at the cost of increased propagation delay and greater power consumption. The nulling resistor nullifies a right-half plane (RHP) zero to a considerable extent which is created unwantedly by the Miller Capacitor. The two stages of the amplifier are designed considering that the voltage gain of the first stage is much higher as compared to that of the second stage so that the power dissipation at the output resistance is minimalistic. The low voltage gain of the second stage design is ensured by making a DC current of lesser magnitude to flow through it. The high gain of the two stages combined, can somewhat be realized with a single stage operational amplifier as well but in that case the bandwidth and output power dissipated across a load resistor would be very poor. To obtain a combination of high gain-bandwidth product and low output power dissipation, the two stage operational amplifier is preferred to single stage operational amplifier.

For reduction of the problems associated with reduction in signal swings and noise coupling the fully differential operational amplifier has found its usage in the areas of analog signal processing. The maximum signal swing of the circuit gets effectively doubled on account of usage of the fully differential design technique. Moreover, all external noise sources which brings about an influence on both signal paths of a balanced differential system in the same way, are rejected. This favorable situation happens in case of a fully differential system because here the signal of interest happens to be the difference between the signals of the two signal paths. Hence any noise which is common to both signal paths will be cancelled out with one another. The same justification applies to the reduction of total harmonic distortion caused in the circuit due to the presence of its non-linear elements.

Operational amplifiers (“op-amps”) happens to be one of the most important constituents of many analog circuit designs. It is a DC-coupled high gain electronic voltage amplifier with a differential input and usually a single ended output. In this configuration the op-amp produces an output potential relative to the ground which is much greater than the potential difference between its input terminals.

Op-amp usage had their origins in analog computers, where they were used to do mathematical operations in many linear, non-linear and frequency dependent circuits. Due to the versatile nature of an op-amp as a building block it has gained its popularity. On account of the negative feedback, the characteristics of an op-amp circuit, input and output impedance, its gain, bandwidth etc. are determined by the external components and have very little dependency on temperature coefficients and manufacturing variations in the op-amp itself.

Among the currently used electronic devices, op-amps are one of the most widely used. It finds its usage in a vast array of consumer, industrial and scientific devices. Many standard op-amps which have a moderate production volume, cost only a few cents however some integrated or hybrid op-amps with special performance specifications may cost over $100 US and are manufactured in small quantities. Op-amps may be packed as components, or used as elements of more complex integrated circuits. They are used as a fundamental building block in many circuit designs where the high input impedance, high gain, high bandwidth, low output impedance and fast settling time of the op-amps are utilized. They also find usage in several analog circuits such as switched-capacitor filters, pipelined and sigma-delta A/D converters, sample and hold amplifiers etc. They are also critical in analog sampled data circuits, such as switched capacitors and modulators. The high speed op-amps are also used in video amplifiers. The wide-band op-amps operating in megahertz range also finds its usage in fiber optic applications which require analog drivers and receivers.

In recent years, expectation to achieve a high gain, unity gain band-width and fast settling time exists due to the advancements in CMOS analog-digital converters (ADC). Moreover IC op-amps have characteristics that closely approach the assumed ideal. Also, op-amp circuits work at performance levels that are quite close to those predicted theoretically. In the literature, many researchers have suggested techniques to improve the different parameters of op amps such as bandwidth, gain, stability, impedance etc.

1.2 **Some of applications of Fully Differential Operational Amplifier**

- Used in digitally programmable Voltage gain amplifier.
- Can be used as pipelined ADC stage.
- In main stage of CMOS ADC.
- In switched-capacitor filter.
- Audio Systems and RF modulators.
- In Delta Sigma Modulator and many more.

1.3 MOTIVATION

As the supply voltage and the channel length of transistors is being scaled down the design of high-accuracy analogue circuits is becoming a difficult task. The operational amplifiers with best performance are required by most of these kind of circuits. Analog designers are continuously working towards the trade-off solutions between gain, input/output swings, speed, power dissipation and noise. The telescopic cascode, folded cascode, two stage or gain boosting schemes are the principle topologies of the op-amps. In order to increase the open loop gain without using cascode devices and without adding cascade stages, op-amps with active cascade circuits are used. In this procedure the high speed circuits with a reduced transistor count can be obtained.

1.4 Organization of Thesis

Introduction to operational amplifiers, fully differential design and applications of the fully differential structure.

Chapter two consists of the literature survey of some of the work carried in the field of operational amplifiers.

Chapter three consists of the block level analysis of op-amps.

Chapter four consists of a detailed transistor level analysis of the differential structure. This structure is discussed in such a great depth as the application of all the concepts discussed can be applied to any higher level of op-amps.

Chapter five starts with fundamentals of fully differential op-amps, its necessity and basic architecture of two stage op-amps. It also consists of design procedure of single stage differential structure, fully differential two stage telescopic op-amps and fully differential folded cascode op-amps and as a part of the thesis work the entire implementation details of the last two designs mentioned above.

Chapter six presents the simulation results of the designed amplifiers and the comparison of the results of the two implemented designs as mentioned in chapter five.

Chapter seven concludes the present work and suggests some of the future scope of improvement.

CHAPTER 2

LITERATURE SURVEY

In this section some of the research work that is carried out by various research scholars is presented. It also includes the recent trends of research that is done in this field.

In [1] J. Mahattannakul has designed a two-stage CMOS op-amp employing current buffer. Only one non-dominant real pole gets generated in design procedure that has been proposed. A flat closed loop frequency response is obtained. In comparison to [2], a compensation capacitor of smaller value is proposed. The procedure of design rely on pole-zero cancellation. As the pole-zero doublet is placed much higher than the non-dominant pole hence the proposed design procedure is less sensitive to the exactness of calculation.

In [2] G. Palmisano *et al.* does the compensation with a current buffer rather than nullifying resistor or voltage buffer. It is justified that the input of the current buffer has a constrain of low input impedance which has to be met to achieve frequency compensation as there exists formation of complex conjugate pole pairs in closed loop transfer function. The current buffer helps in achieving a high gain bandwidth product as compared to voltage buffer or the nullifying resistor. The designing of the op-amp is carried out using current buffer based technique and a rise of gain bandwidth product is obtained by 18%. The simulations are performed on 2µm CMOS process. The power dissipation in case of resistor was 590 µ Watt, in case of voltage buffer 630 µ Watt and in case of current buffer based technique it was 790 u Watt. The circuit designed using the current buffer based technique improves the low frequency power supply rejection ratio and the amplifier gain.

In [3] J. Mahattannakul *et al.* discusses about obtaining a balance between the noise compensation and power consumption by applying techniques by the help of which the coupling capacitor value can be made much smaller. Actually by the Miller compensation technique the value of capacitance is virtually increased, and since its value can be varied, one can always make adjustments to adjust a compromise between power consumption and noise as the smaller its value becomes, more its effects falls on the lower level of frequency due to which it brings about instability in the system.

In [4] B. K. Ahuja developed an improved frequency compensation technique for the op-amps with a brief review of the existing techniques. A CMOS implementation of the above mentioned technique is done and experimental results that show considerable high frequency power supply rejection improvement over the existing techniques by approximately -30 to -35 Db. at PSRR at 100 KHz is presented. Furthermore for a particular size of compensation capacitor the technique provides extended capacitive drive.

In [5] B. Y. Kamath *et al.* explore the effect of pole-zero pairs on the frequency response and settling time of the op-amps using analytical techniques and computer simulations. It is shown that severe degradation in settling time with minor changes in frequency response of the amplifier occurs due to frequency doublets in the transfer function. Both the pole-zero spacing and the frequency has dependency on the effect of poles. Its effect is reduced by reducing the spacing of the pole zero doublet. Even if the mismatch in pole-zero frequency is as small as 8% can cause a significant increase in settling time. There is a high degree of complexity of doublet frequency upon the settling time. The influence of frequency doublets on the op-amp can be predicted by the simple formulae derived in this paper.

In [6] Wen-Whe Sue *et al.* have discussed the design of a folded-cascode op amp. For stability compensation, the output capacitance is used and simply design appropriate width-to-length ratio to as increase the limitation on output swing of the conventional folded-cascode configuration. The designed op amp obtains a 4.7K open-loop DC gain with 1 Mhz. unity-gain bandwidth.

In [7] T. Lehmann *et al.* designed a trans-conductance cascode amplifier in a standard CMOS process which has a gain of 69 Db. and a bandwidth of 2 MHz and a compatible input output voltage level of 1-V power supply. This is done by a novel current driven bulk (CDB) technique, in which the threshold voltage of MOST is reduced by forcing a constant current though the transistor bulk terminal. A poor initial high frequency is obtained by these drain-bulk capacitance but compensation can be done by the usage of cascodes or by using additional circuits in the CDB structure.

In [8] Zushu Yan *et al.* presents the idea of effectively minimizing the physical size of the compensation capacitor which improves the slew rate of the amplifier with no extra power consumption and a useful LHP zero is created that enhances stability. A capacitor multiplier (CM) is introduced so as a feasible alternative for better area and power efficiency. The embedded CM does not require any extra biasing circuit nor extra power consumption. Here the driving capability of the two stage amplifier is also enhanced by the incorporation of current buffer based Miller compensation with more sophisticated Capacitor multipliers. Here the work is carried out for 35-μm CMOS process.

In [9] G. Blakiewicz discusses a frequency compensation technique for improving the PSRR for two stage op-amp is presented. Such a technique is mostly applied to most known two stage op-amps for continuous time filtering applications. The proposed op-amp has a better gain-bandwidth product and a better power supply rejection ratio (PSSR). It requires several times less on-chip area. The entire work of fabrication is carried out using 35-μm process technology.

In [10] D. Grasso *et al.* use the reversed nested Miller compensation with nulling resistor (RNMCNR) and reversed active feedback frequency compensation (RAFFC) as the two frequency compensation schemes for three-stage operational trans-conductance amplifiers in this paper. The techniques are especially useful for heavy capacitive loads which are based on the basic RNMC and are seen to be inherently advantageous over traditional compensation strategies. Moreover, the implementation is done without entailing extra transistors which saves circuit complexity and power consumption. The design procedure is well defined where phase margin happens to the main design parameter. The verification of the effectiveness of the techniques is done by the fabrication of the two amplifiers in a standard 0.5-μm CMOS process. Experimental measurements and theoretical analysis are found to agree to one another to a considerable extent. The small signal and the large signal amplification performances are seen to improve considerably. Finally, the non-reversed counterparts' topologies are compared to the proposed solution, where the latter is seen to be superior.

In [11] K. N. Leung *et al.* reanalyzed frequency-compensation strategies of single, two and three stage amplifiers based on Miller pole splitting and pole–zero cancellation. The analysis also includes the discussion of pros and cons of the various techniques as well their design requirements. Inclusions of the assumptions made, stability criteria, transfer functions, important design issues and bandwidths of almost all reported topologies are done. In order to improve the published topologies several proposed methods are provided. In order to verify the analysis and to prove the effectiveness of the proposed methods simulations and experimental results are also provided. Design procedures are proposed to improve nested Miller compensation (NMC) and nested Gm-C compensation (NGCC), nested miller compensated with nulling resistor (NMCNR), and NMC with feed-forward Gm stage (NMCF) and for its verification experimental results are provided. In addition damping factor controlled (DFCFC) is introduced which is seen to have much better frequency and transient performances than the other published topologies for driving large capacitive loads. Finally, the robustness of the studied topologies are also discussed.

In [12] A. D. Grasso *et al.* compares the possible Miller approaches by utilizing an analytical figure of merit on the basis of a tradeoff between gain-bandwidth product, load capacitance, and total trans-conductance for a given value of phase margin. The validation through simulations are also performed to display the accuracy of the comparison. An analytical comparison method originally developed for three-stage amplifiers, was applied to two-stage amplifier frequency compensation topologies. Here comparison are basically done for the main optimized Miller compensation approaches based on nulling resistor, voltage buffer, and current buffer/amplifier. The results of comparison shows that for moderate capacitive loads the current amplifier is the best option whereas for that for higher capacitive loads the voltage buffer is a better choice. The proposed comparison has no dependency on the technology adopted and enables the better understanding of the real advantages of a particular frequency compensation topology under different design constraints. Better speed performance is seen to be provided by a two-stage Miller amplifier than a single stage implementation with the same load capacitance and total quiescent current. Several transistors and additional bias circuits are required to implement the current amplifier but reduction of output swing of the amplifier is avoided as it happens in the case of voltage buffer. Apart from the above obtained results it is also seen that the circuit with voltage buffer and with nulling resistor are affected by the pole zero doublet which arise from process tolerances and hence poor high frequency PSRR is obtained as compared to the current buffer counterpart.

In [13] G. A. Rincon-Mora presents a technique whereby multiplication is effectively performed for the compensating capacitor of an internally compensated linear regulator, Miller-compensated two-stage amplifier. Due to the increased capacitance with a current-mode multiplier the circuit occupy less silicon area and to more effectively drive capacitive loads. The higher integration is enabled due to the enhanced Miller-compensation technique which is readily applicable to any process technology. The technique proposed works well in feedback configuration. Experimentally, the integrated linear regulator (fabricated in a 1-μm biCMOS process technology) proved to be stable for a wide variety of loading conditions. By the usage of modified Miller-compensating scheme a linear regulator is designed and fabricated. The enhancement of the voltage-mode multiplying effects of Miller compensation is done by a current-mode capacitor multiplier. The designed circuit is seen to deteriorate the input offset voltage which is reduced with careful design and layout. Moreover in high-frequency applications, care must be taken about the placement of the LHP introduced by the circuit as a low LHP zero degrades phase margin. By controlling the trans-conductance of the diode-connected device the zero is manipulated. The diode connected device may get turned off during an event of fast load transient and this degrades overall recovery time. The above mentioned negative effect can be removed by placing an additional current source in parallel to the above mentioned device.

The concept is proved to be valid by the simulations and the experimental results. The fabricated IC is stable for load currents of up to 200 mA, ESR of up to 3 Ω, and load capacitors ranging from 1.5-nF to 21 μF. The above results are obtained by using a low compensation capacitor as compared to standard Miller compensation technique. The above mentioned technique reduces the overhead in terms of silicon area which reduces the overall cost. Moreover the technique also applies to the compensation of feedback networks.

In [14] W. Aloisi *et al.* propose a novel and simple design approach for the frequency compensation of a two-stage amplifier exploiting a current buffer/amplifier. The procedure has been profitably applied to a class-AB two-stage CMOS operational trans-conductance amplifier, with a 100 pF load. Using a 1.3 pF, 0.6 pF and 250-fF compensation capacitor alternatively three compensation networks were designed. Moreover, it is also demonstrated that the adopted compensation topology provides an improvement in terms of power supply rejection ratio. Simulations carried out show that experimental data are in agreement with the expected data. The design technique incorporates Miller compensation strategy and is seen to bring about an improvement in the PSRR. Experimental data also shows that the value of compensation capacitor can be reduced greatly. The only demerit of the circuit is its poor noise performance.

In [15] K. N. Leung *et al.* presents a novel damping-factor-control frequency compensation (DFCFC) technique with detailed theoretical analysis. The compensation strategy improves frequency response, transient response and PSRR for amplifiers especially when large capacitive loads are driven by it. The value of compensation capacitors used are generally small hence can be integrated in commercial CMOS processes. Two capacitive loads of value (100 and 1000) pF are driven by the amplifiers using DFCFC and nested Miller compensation (NMC) using a 0.8-μm CMOS process with Vtn = 0.72 V and Vtp = -0.75 V. In case of DFCFC based amplifier driving a 1000 pF load with integrated compensation capacitor, gain-bandwidth product of 1 MHz, phase margin of 51˚, slew rate of 0.33 V/μs, settling time of 3.54-μs and a power consumption of 426-μW are obtained. In case of DFCFC based amplifier, the frequency and the transient response are comparatively better than the NMC amplifier by one order of magnitude with a very less increase in power consumption.

In [16] Loikkannen M. *et al.* presents a simple circuit for the improvement of mid-band PSRR of a gain boosted class AB amplifier. The advantage of the bias network and narrow gain boosting amplifier bandwidth is taken. Experimental results show that mid-band PSRR is improved by more than 20 Db. at a frequency of 100 KHz.

In [17] Loikkannen M. *et al.* presents a two stage Miller compensated class AB amplifier where single ended class AB is used as control for exact setting of the output stage quiescent and minimum currents. The PSRR also get boosted by the used controlling technique. It is experimentally shown that the mid-band PSRR improves by more than 20 Db. by the used design as compared to popular symmetrical class AB amplifiers with similar bandwidth.

In [18] P.A. Gowri Sankar *et al.* presents a two-stage dual-path fully differential topology based on Improved Recycling Folded Cascode (IRFC) where (IRFC) based first stage provides a moderate DC gain and the dual path push pull type output stage increases the unity gain band-width and slew rate while keeping the power consumption low.

In [19] Hamed Aminzadeh *et al.* presents the design of two stage operational amplifier with carbon nanotube field-effect transistor (CNFET) as a promising candidate for future electronic devices which produces remarkable results as compared to existing CMOS based counterpart, where both designed on 32 nm technology.

In [20] Siddharth Malhotra *et al.* puts up a comparative analysis on power consumption for two stage cascode compensation and Miller compensated counterpart on 0.25μm technology and finally concluded that of the two types the cascode compensated operational amplifier is more efficient.

CHAPTER 3

ANALYSIS OF OPERATIONAL AMPLIFIERS AT A BLOCK LEVEL.

In this part of the thesis work the analysis of Operational Amplifiers at block level is presented. The below figure is that of an amplifier. It has a constant DC input Vi (say) and it generates an output Vo (say) where Vo = K × Vi where K is the "desired gain".

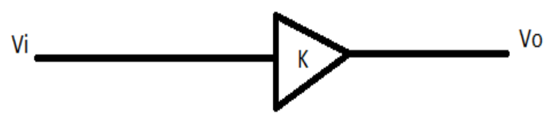


Figure 3.1 Amplifier with a forward gain K.

The above amplifier must be realized using negative feedback. Using feedback it means that the current output must be looked at and it must be compared with the desired output and based on the comparison of result the output is controlled so that it becomes appropriate value. In a general sense it looks as below.

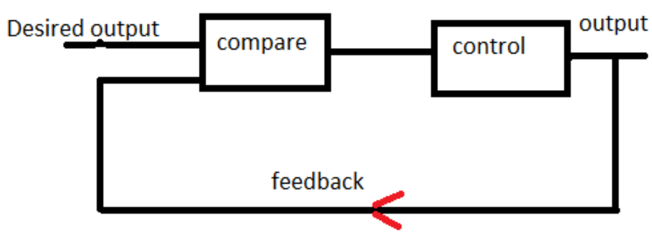


Figure 3.2 Feedback network of an amplifier.

In "compare" block the difference of the desired output and the current output is taken i.e. the error signal is generated which is then integrated in the "control" block and finally the output signal is generated to track the current output.

If analogy of the system is done with a vehicle in the following way. Here the desired and actual outputs are compared to compute the error and finally control the output in the direction that reduces the error. The integrator stops working if and only if the input error = 0, i.e. desired speed equals the actual speed. Hence the negative feedback amplifier is made by using the same method. The actual output (Vo) is compared to the desired output (K × Vi). The error (K × Vi - Vo) is measured. Now here there is a flaw, K × Vi is not obtained at output, then there was no need to build the amplifier, so instead of trying for (K × Vi - Vo), Vi - Vo/k is obtained by bringing Vo/K from output to input and then generating the error signal and then integrating it in the direction of reduction of error and finally tracking the desired output. Thus the representation is as below:-

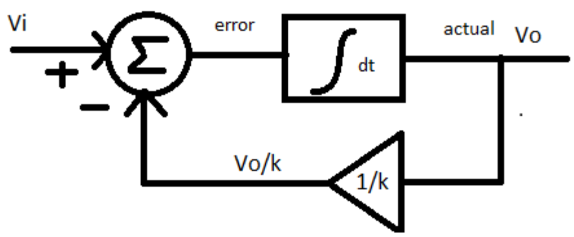


Figure 3.3 Circuit with the feedback factor of 1/K.

Here Vo/K can be obtained by the help of resistive divider network as below:-

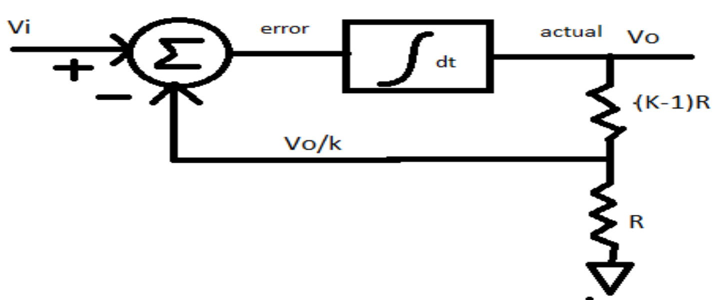


Figure 3.4 Resistive divider feedback network.

Thus the two essential components of the negative feedback system are:-

- Sense the input and compute the error.
- Integrate the error to drive the output.

The integrator is used to make the error equal to 0. The reason for implementing such a design is, obtaining Vo/K is easier to implement as compared to K × Vi. If the integrator is looked at more closely, it is observed that there is input voltage at the input of integrator and output voltage at the end of integrator. Thus the integrator must have the dimension of frequency ("ωu"). Hence the equation is:-

$$Vo = \omega u \times \int Ve.dt \qquad (3.1)$$

Where ωu is the unity gain frequency of the device and Ve is the error voltage. So if Ve is constant, output will increase like a ramp with a constant slope in relation with the constant ωu and Ve. So if error is small, output will rise slowly and ωu defines the rate of integration. So the nature in which Vo varies with time is given below.

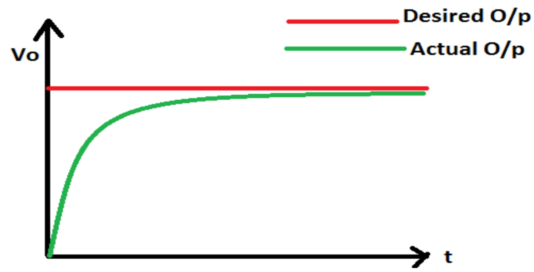


Figure 3.5 Plot showing desired output and final output.

Important Design criteria: - When told about reaching the steady state in a given time it is determined by the speed of integration of the amplifier.

3.1 Step Response of negative feedback amplifier:-

The figure below represents the step response of a negative feedback amplifier.

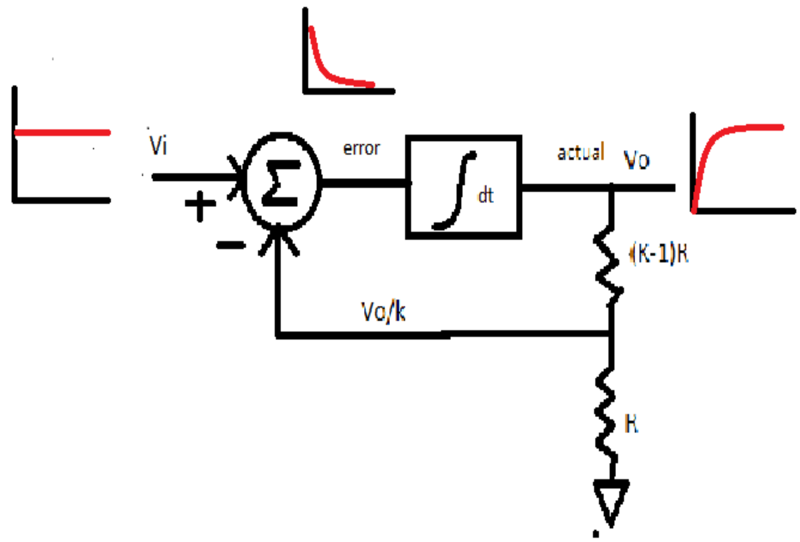


Figure 3.6 Step response of a negative feedback amplifier.

Thus the natures of input, error and output are as below:-

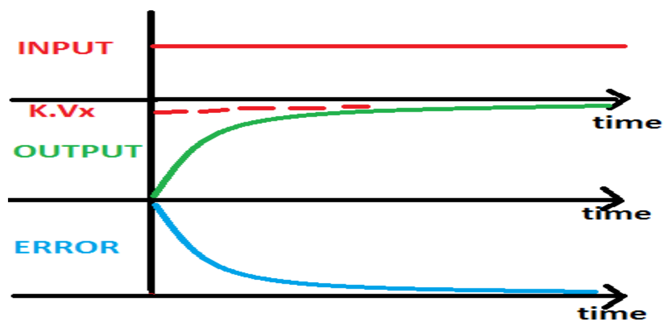


Figure 3.7 Natures of input, output and error are represented.

It can be verified by solving the equation:-

$$\text{Vo} = \omega\text{u} \times \int_{0\,sec.}^{t\,sec.} \left(Vi - \frac{Vo}{K}\right) \times dt \qquad (3.2)$$

$$\Rightarrow \frac{dVo}{dt} = \omega\text{u} \times (\text{Vi-Vo/K}). \qquad (3.3)$$

Solving it for the given limits gives

$$\text{Vo} = \text{K} \times \text{Vi} \times (1 - e^{(\omega u/K)} \times t) + \text{V(0)} \times e^{(-\omega u/K)} \times t \qquad (3.4)$$

Since V(0) {initial voltage = 0 Volts here} and ($K/_{\omega u}$) is the time constant of the amplifier. It can also be seen that after 5 time constants the system reaches 99% of the steady state value. To reduce the energy of error, ωu must be increased and obtaining higher and higher value of ωu is more challenging.

3.2 Response of amplifier to Sinusoidal Input:-

If the integrator is modelled as the system then the system response is expressed as below.

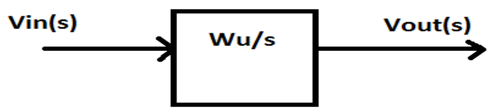


Figure 3.8 Integrator modelled as a system.

$$\text{Thus } \frac{Vout(S)}{Vin(S)} = \frac{\omega u}{(j\omega)} = \text{H}(j\omega). \quad (3.5)$$

Where H(jω) represents system response.

If co-sinusoidal input is applied to the above system then the system responds as below in figure 3.9. Similar kind of response is observed for sinusoidal input.

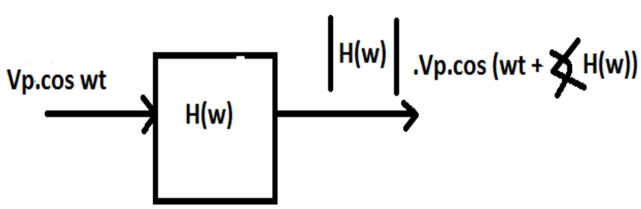


Figure 3.9 Response of amplifier to co-sinusoidal input.

In the above shown figure │H(jω)│ represents the magnitude of output and <H(jω) represents the phase shift at output. The response of the system indicates the contribution of the system in generating the gain and phase lag at the output.

The Bode Plot of the above system is represented in the following way.

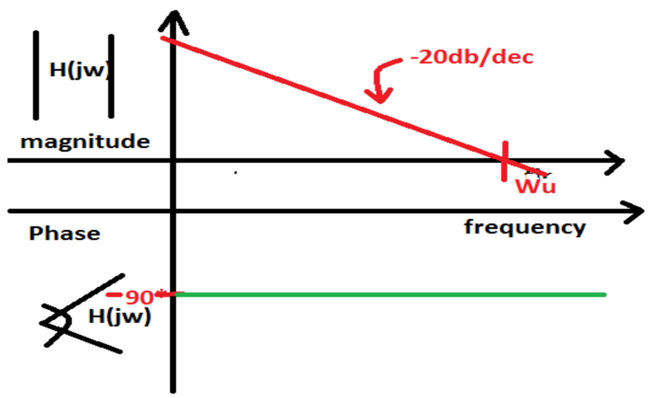


Figure 3.10 Bode Plot of system shown in figure 3.9 where w (omega in radians).

Thus at ω=ωu, the magnitude of transfer function reaches unity, thus ωu is the unity gain frequency of the integrator. It is to be noted that the X-axis of Bode Plot is in Log scale "0" frequency cannot be represented on a log scale but the frequency can be reduced as much as required. For the integrator the magnitude will be higher and higher for lower frequency.

For a given unity gain frequency in case of step input, ωu determines the rate at which Vo reaches the steady state and in case of sinusoidal input ωu is the frequency at which response is unity. Thus if a sinusoidal input is applied to an integrator output will be sinusoidal as shown below:-

$$\left(\frac{(Vi - {}^{Vo}/_{K})}{{}^{\omega u}/_{S}}\right) \times ({}^{\omega u}/_{S}) = \text{Vo} \tag{3.6}$$

$$\Rightarrow \text{Vi} \times {}^{\omega u}/_{S} = \text{Vo} \times \left(({}^{\omega u}/_{KS}) + 1\right) \tag{3.7}$$

$$\Rightarrow \frac{Vo}{Vi} = \frac{{}^{\omega u}/_{S}}{\left(({}^{\omega u}/_{KS}) + 1\right)} \times \frac{{}^{KS}/_{\omega u}}{{}^{KS}/_{\omega u}} \tag{3.8}$$

$$\Rightarrow \text{Hence } \frac{Vo}{Vi} = \frac{K}{(1 + S[{}^{K}/_{\omega u}])} = \text{H(s)} \tag{3.9}$$

Thus H(0) = K and Pole location is at $(-\ {}^{\omega u}/_{K})$ in time domain. The polar plot of the above system is as below.

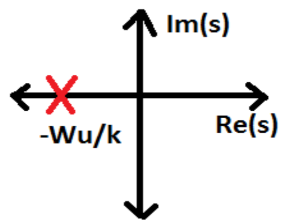


Figure 3.11 Pole location of system represented in figure 3.9.

Thus a single pole exists at Left Half of S plane which makes the system stable and hence there exist exponential decay in time domain.

3.3 Negative feedback amplifier transfer function:-

$$H(s) = K/ (1+K.s/Wu) \tag{3.10}$$

$$H(S) = K\Big/\left(1 + S \times \left(K/\omega u\right)\right) \tag{3.11}$$

$$H(j\omega) = K\Big/\left(1 + \left(j\omega K/\omega u\right)\right) \tag{3.12}$$

$$|H(j\omega)| = \frac{K}{\sqrt{(1+(K^2 \times \omega^2/\omega u^2))}} \tag{3.13}$$

$$\text{For } \omega >> (\omega u/K) \quad |H(j\omega)| = \omega u/\omega \tag{3.14}$$

$$<H(j\omega) = -\tan^{-1}(K \times \omega/\omega u) \qquad \text{and } <H(j\omega) = -90^{o} \tag{3.15}$$

Thus at high frequency the system gain becomes independent of gain K and the output voltage is out of phase of the input.

Thus the Bode Plot as below:-

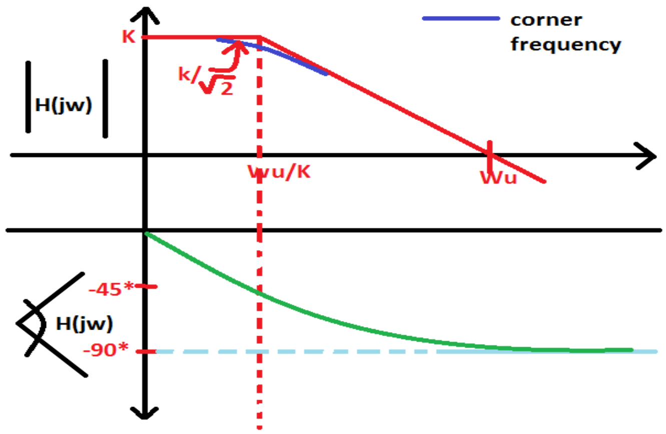


Figure 3.12 Bode plot of first order negative feedback amplifier w.r.t. frequency in radians.

In the above figures the Bode Plot of first order negative feedback amplifier is shown with the above one representing the magnitude plot and the below one representing the phase plot. At ω << $\omega u/K$, i.e. at low frequency, phase lag very is small and the system gain is close to K. At ω >> $\omega u/K$, phase lag becomes -90˚. At higher frequency it rolls off at $-20\ db/decade$. The proper behavior of the amplifier is seen to be, what the amplifier has up to a gain of K, till its frequency < $\omega u/K$. Thus this amplifier is used for sinusoids whose frequency are well below $\omega u/K$, which is called the bandwidth. Bandwidth simply means usable range of frequency. For this system the product of $\omega u/K$and Gain of the system at -3db bandwidth is $(K/\sqrt{2})$.

Apart from this, one important point about the first order negative feedback amplifier is that for a higher gain the time to reach steady state is also higher. Below diagram shows the following situation:-

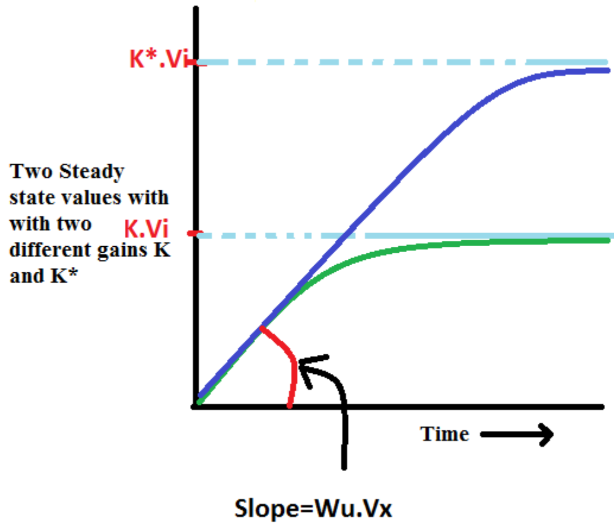


Figure 3.13 Shows two system responses with different values gains K* and K respectively w.r.t. time.

In case of the higher gain of K* as compared to that of K, both the curves start with the same slope but the former system requires a greater value of time to reach steady state. One important observation about the above plot is that at an initial stage, Vo ramps up faster as compared to that of the later stages. The reason for such a phenomenon is, at step input t=0, Vo = 0, thus error voltage (Ve) is very high so Vo ramps up at a faster rate initially, when Vo increases, the fed-back voltage increases thus the error decreases hence the rate of integration of the amplifier reduces and thus Vo finally ramps up to K × Vi (desired value of Voltage) at a reduced rate.

It is observed that $\omega u/K$ seems to appear almost in all expressions, to analyze its importance one of the crucial quantities of the negative feedback system is the loop gain. In the analysis of loop gain, let a certain quantity be injected to a system say ("Vtest") and what comes back say ("Vreturn")**,** as in below figure**.**

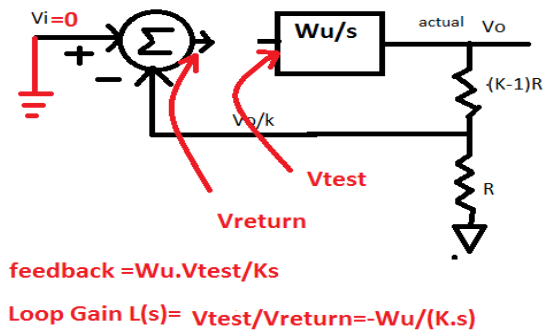


Figure 3.14 Determination of loop gain for a negative feedback amplifier.

Thus the Bode Plot of above system can be represented as below.

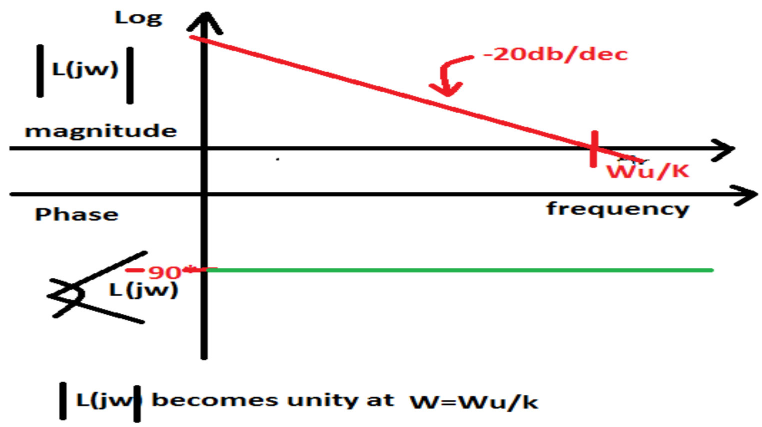


Figure 3.15 Magnitude and phase plot of the system in figure 3.14.

For a feedback system it is not sufficient for connection to come from output to input but a significant amount of signal must come back and what comes back is decided by loop gain. From the given plot it is clear that for ω << $(\omega u/K)$ the feedback quantity is large and beyond that it becomes inexistent. So from analysis of transfer function the amplifier is usable for the frequency below $(\omega u/K)$. Thus the graphical representation of the above system is as below:-

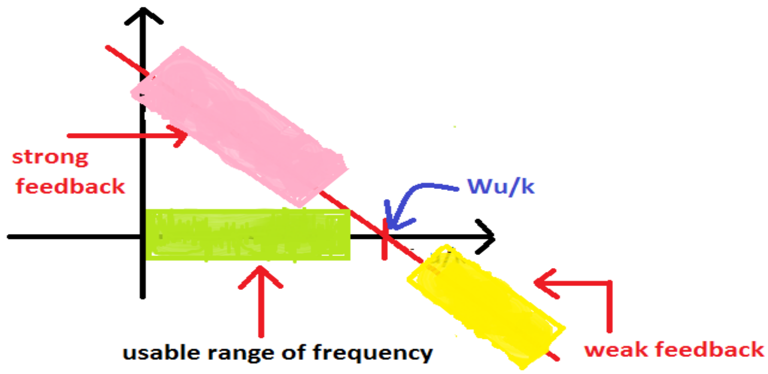


Figure 3.16 Graphical representation of a negative feedback amplifier.

The unity loop gain frequency (ωu, loop) is the frequency at which |L(jω)| = 1 divides regions of ideal and non-ideal behavior as it divides where there is strong and weak feedback.

The negative feedback amplifier concept is so useful that people have put a lot of effort to put the difference part and the integrator part together into a single block known as operational amplifier (op-amp).

3.4 Operational Amplifier (Op-amp)

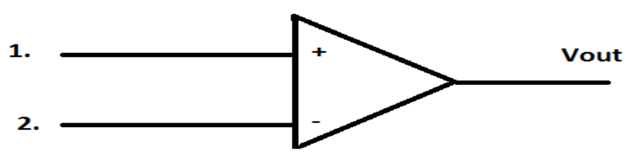


Figure 3.17 Symbol of op-amp.

In the above system there are two input voltages in terminals 1 and 2, the op-amp first finds the difference of the two inputs and then integrates the value of error. Using the above system the negative feedback amplifier can be made as shown in below figure.

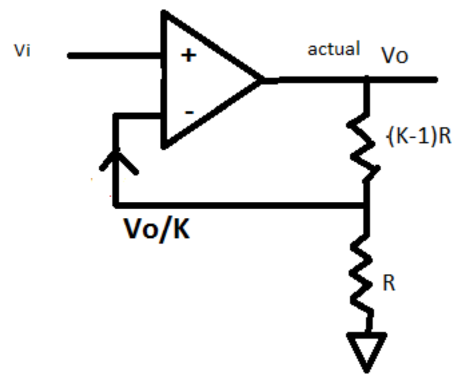


Figure 3.18 Op-amp with negative feedback.

The above is a classical non-inverting amplifier. The DC gain is positive. Now there is also a concept of ideal op-amp in which if the unity gain frequency of the op-amp (ωu) is increased unlimitedly the bandwidth goes on increasing indefinitely, i.e. the transfer function will not have any "S" terms in it, and it will be simply equal to K. Hence at an infinite value of ωu, gives the bandwidth at infinity and the op-amp shows ideal behavior for all frequencies. Thus for any frequency Vo = K × Vi implies at (-) ve terminal Vo/K = Vi and the difference between will be equal to zero. Thus the op-amp with negative feedback is shown in the below figure:-

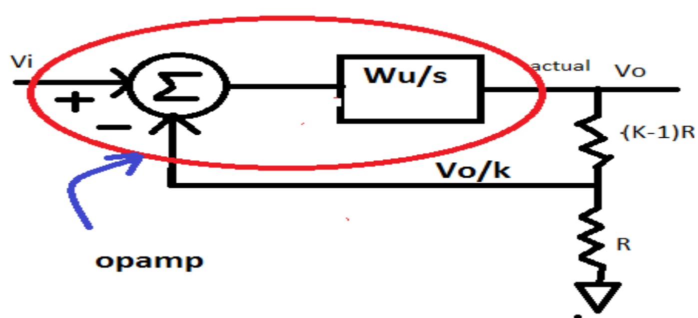


Figure 3.19 Discrete components of op-amp with negative feedback.

3.4.1 Integrator Realization of an op-amp:-

Among the basic resistor (R), inductor (L), capacitor (C), only L and C give integral values. The capacitor integrates current to give voltage (Ic = C × $\frac{dV}{dT}$) where Ic is the current through the capacitor and $\frac{dV}{dT}$ is the rate of change of voltage across the capacitor. The inductor integrates voltage to give current (Vl=L× $\frac{dI}{dT}$) where Vl is the voltage across the inductor and $\frac{dI}{dT}$ is the rate of change of current through it. Now in case of integrated circuits the component requirements is small and inductors being bulky cannot be used hence capacitors are the only choice. Thus the work of integrating action by the capacitor is shown below.

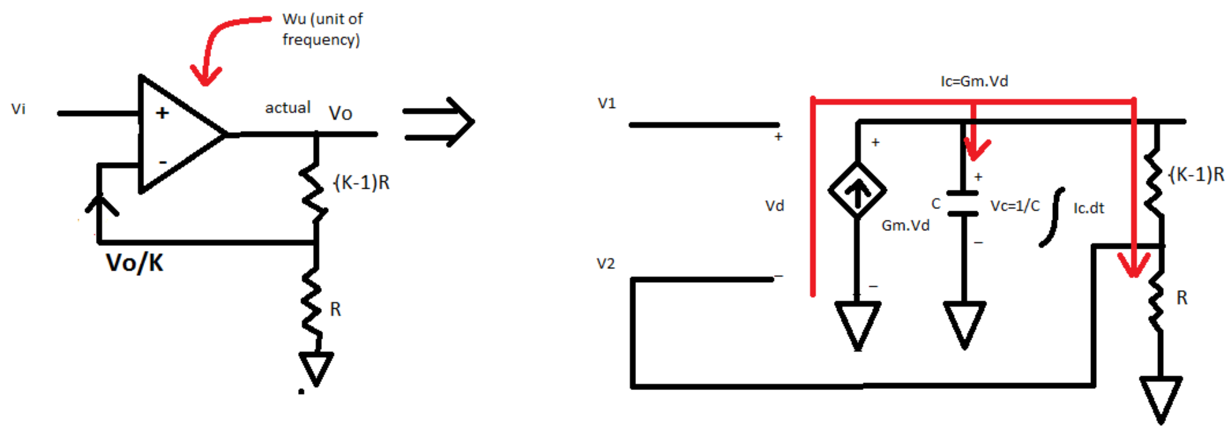


Figure 3.20 Internal structure of op-amp with feedback without buffer.

Now by the design as shown in the above the purpose of the integrator is ruined. It is because a part of the current goes into the resistor apart from the capacitor i.e. it doesn't all go through the capacitor. So in order not to have this, there is a need to have a voltage buffer as shown below with input impedance as infinite:-

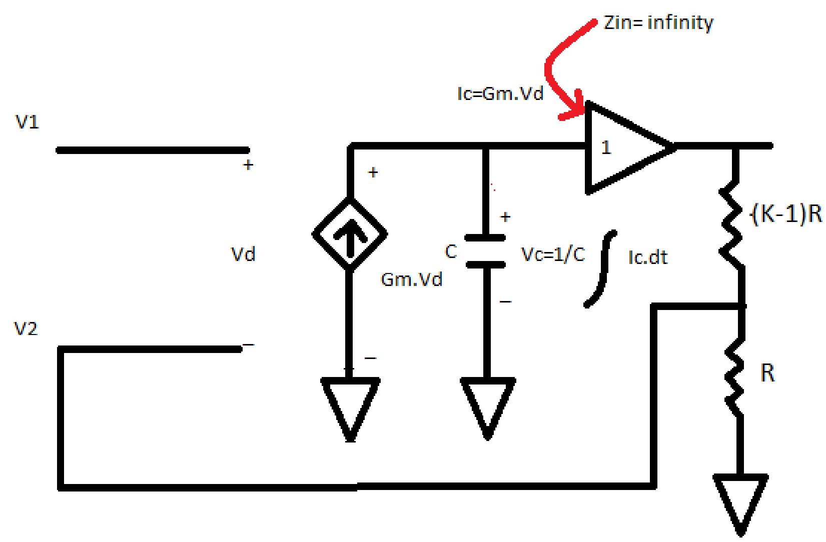


Figure 3.21 Internal structure of op-amp with feedback with voltage buffer.

3.4.2 Delay and stability Analysis of op-amp:-

By the above circuit, op-amps can be made but in the process, non-idealities would come up and there are ways to combat them. Let the first non-ideal parameter that is to be considered is delay.

When $Vo/K$is compared to Vi, there can exist a delay in the circuit. This delay is in terms of parasitic capacitances. This delay makes desired output to be compared with a delayed version of the actual feedback. If the delay is present in acceptable limits then its ok, or else it might bring about heavy ringing or even instability (sustained oscillations), i.e. the target can never be reached. Delay can appear in any part of the system. It can appear in the integrator due to implementation of the integrator or it can appear in the feedback. It doesn't matter where it is, the delay is the same. By quantitative analysis of feedback with delay it would be possible to be able to limit ringing. As of now let the delay be assumed in the feedback path as shown in the below block.

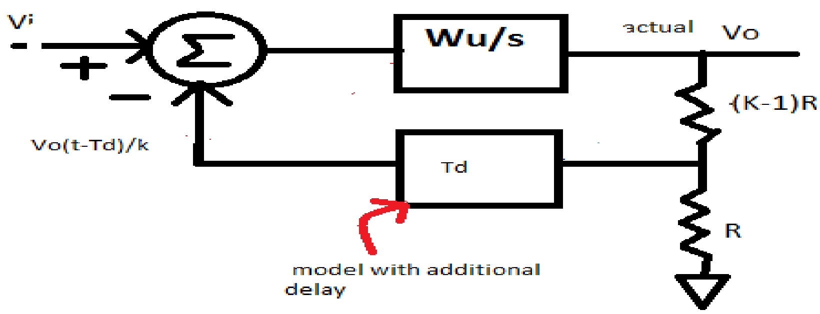


Figure 3.22 Showing the Delay Model.

In the op-amp it is seen that there is a requirement of voltage controlled current source (VCCS) after the differential stage. In "Analog IC." the VCCS is represented by a different symbol. The symbol is represented as below with other important features:-

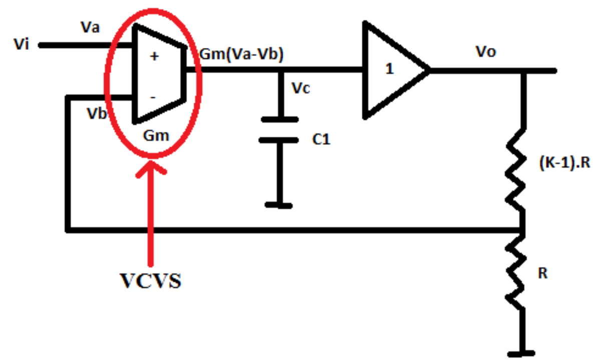


Figure 3.23 VCCS being used in an amplifier.

The above diagram represents an op-amp realization, Gm refers to the trans-conductance of the op-amp. In the op-amp there are general possibilities because of which there is delay in the circuit. The delay is due to the parasitic capacitances that occur at the below locations:-

1. Voltage Buffer - Ideally this has a transfer function (TF) of "1". But in reality it appears as below:-

$$\frac{(1+S/Z1)\ldots\ldots\ldots}{(1+S/P1)\ldots\ldots\ldots} \qquad (3.16)$$

Now the exact TF depends upon the details of the circuit used to implement the buffer where the numerator represent the zeroes and the denominator represent the poles of the system.

2. Trans-conductor - Ideally trans-conductance has the transfer function as Gm = $\frac{Iout(S)}{(Va(S)-Vb(S))}$. But in reality it appears as as below:-

$$Gm \times \frac{(1+S/Z1)\ldots\ldots\ldots}{(1+S/P1)\ldots\ldots\ldots}. \tag{3.17}$$

3. Voltage divider network - Ideally its value is 1/K, but practically its transfer function appear as below:-

$$\frac{(1/K)}{1+(K-1)/K \times S \times Cp \times R}. \tag{3.18}$$

Below is its diagrammatic representation.

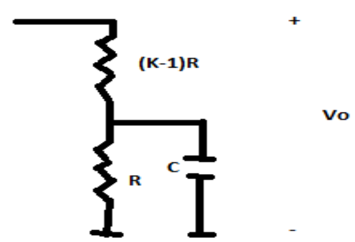


Figure 3.24 Voltage divider network.

In the equation of transfer function of voltage divider network, the denominator has terms that contain a pole. Thus the transfer function of a voltage divider is $(1/K) \times [1/(1+S/P2)]$ where P2 indicates a pole. If S×Cp×R (mentioned in equation 3.18) >> 1, then at high frequency the pole becomes $[(1/(S \times Cp)]$. Thus in voltage divider there exists a pole and the pole acts as a delay. So in general there can be additional poles and zeroes in the transfer function. The poles and zeroes come at inside the integrator and the divider but they can clubbed into the poles and zeroes in the feedback path as below:-

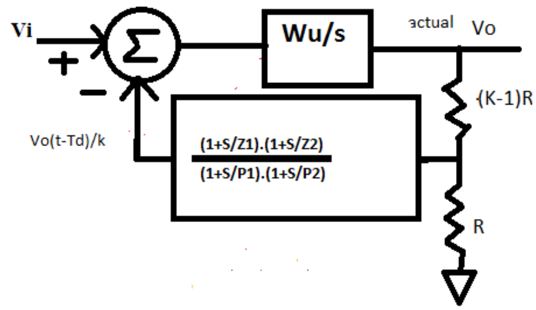


Figure 3.25 System with poles and zeros clubbed in feedback path.

Now the poles and zeroes can be modeled in the forward path, their effect is the same. For the sake of convenience here it is modelled in forward path as below:-

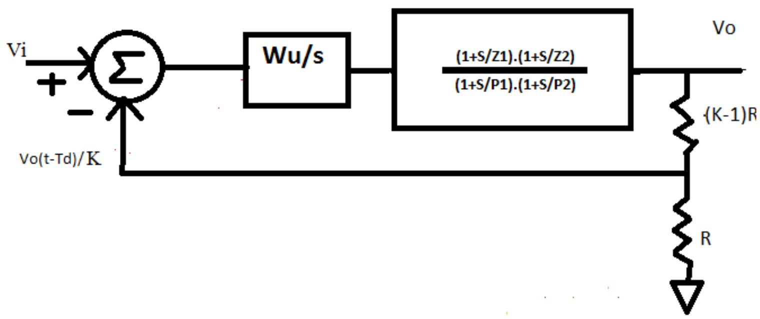


Figure 3.26 System with poles and zeros clubbed in feed-forward path.

First let it be assumed that there exists a single extra pole in the forward path, then it would be assumed for two extra poles in the forward path and then conclusion would be drawn for multiple poles and zeroes in the forward path.

First the analysis of a system with a single extra pole is presented. Below diagram represents the same.

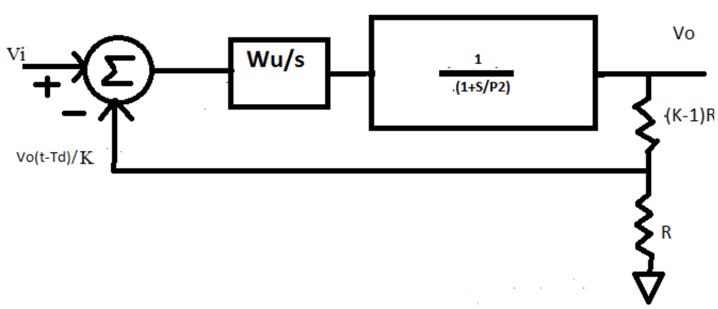


Figure 3.27 System with single extra pole.

The expression of Vo(S) is as below.

$$\text{Vo(S)} = [\text{Vi(S)} - (Vo(S)/K) \times (\omega u/S) \times (1/1 + S/P2)] \tag{3.19}$$

On simplification below given expression is obtained.

$$\frac{Vo(S)}{Vin(S)} = \text{K} \times [\frac{1}{(1+(S \times K/\omega u) + (S^2 \times {}^{K}/_{(\omega u \times P2)}))}] \tag{3.20}$$

In the above expression K is the ideal gain of the amplifier and the remaining symbols have usual meanings. Thus on rearranging the above expression in the form of 2nd order system, the final expression is obtained as below.

$$\frac{Vo(S)}{Vin(S)} = \text{K} \times [\frac{\omega u \times P2/K}{S^2 + (S \times P2) + ({}^{\omega u \times P2}/_{K})}] \tag{3.21}$$

The 2nd order system characterized by its natural frequency (ωn) and damping factor called zeta (ξ). Hence the expression of ωn and ξ is as given below.

$$\omega n = \sqrt{({}^{\omega u \times P2}/_{K})} \tag{3.22}$$

$$\xi = 0.5 \times \sqrt{(\frac{P2}{{}^{\omega u}/_{K}})} \tag{3.23}$$

If the value of ωn and ξ of second order negative feedback system are known, statements about its step response can be made. The below plot represents the system response for various values of ξ.

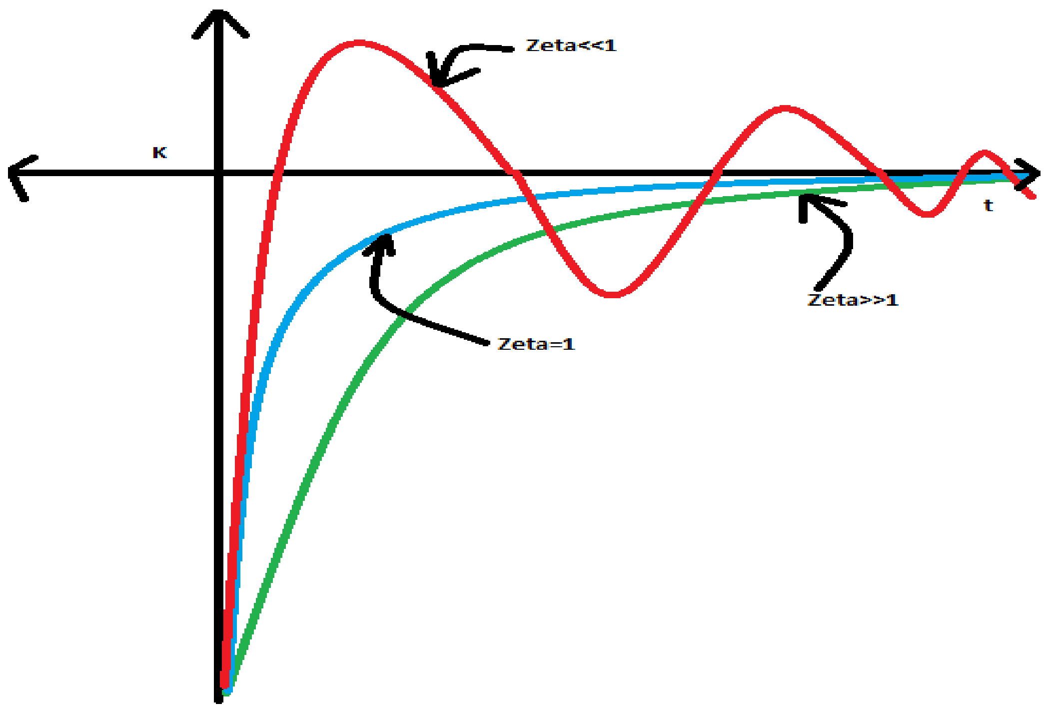


Figure 3.28 System response for the various values of zeta (ξ).

For ξ << 1, it is an under damped system. Here the system reaches steady state but with a lot of oscillations. For ξ = 1, it is critical damped situation. Here the time at which the system reaches the steady state would be minimum. For ξ >> 1 it is the over-damped situation when the system is slow and sluggish.

As far as the system is concerned a critically damped response is desired or a little underdamped with a little overshoot is tolerable. Thus the permissible parasitic poles to generate such a damping so that ξ = 1 is obtained as below.

$$\xi = 0.5 \times \sqrt{\left(\frac{P2}{\omega u/K}\right)} = 1 \tag{3.24}$$

$$\Rightarrow \quad P2 = 4 \times \left(\omega u/K\right). \tag{3.25}$$

Hence it is found that the expression of the second order transfer function is unconditionally stable. But for P2 << 4 × $(\omega u/K)$ a severely underdamped response is obtained. In case of first and second order systems if the open loop forward path is stable then under all cases the closed loop systems are stable. But for third order systems the stability is not unconditional hence it is really very important to find out the condition under which the system the system is stable. Same technique of analysis can be applied to higher order systems as well. Let a third order system be considered as below.

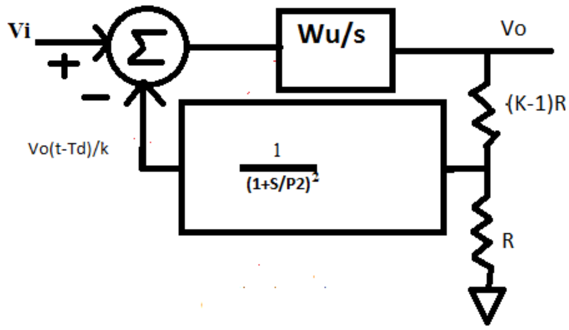


Figure 3.29 System with two extra poles.

The below expression is that of the loop gain L(S) of a third order system.

$$L(S) = \left(\frac{\omega u/K}{S}\right) \times \left(\frac{1}{(1+S/P2)^2}\right). \tag{3.26}$$

The magnitude of L(S) is expressed as $|L(j\omega)|$.

$$|L(j\omega)| = \frac{\omega u/K}{\omega \times (1+(\omega/P2))^2}. \tag{3.27}$$

The phase angle of L(S) is expressed as below.

$$<L(j\omega) = -\pi/2 - 2\tan^{-1}(\omega/P2). \tag{3.28}$$

$$\text{Hence at } \omega = 0, <L(j\omega) = -\pi/2 \text{ and } \omega = \text{infinite}, <L(j\omega) = -(3\pi/2). \tag{3.29}$$

For the analysis of the above system let the below Nyquist Plot be observed.

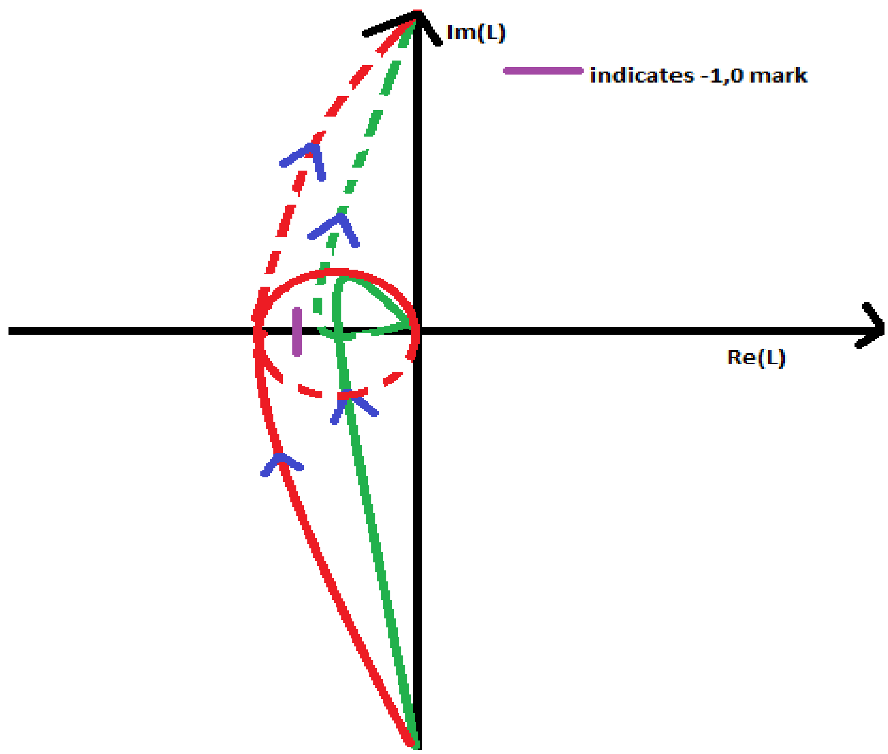


Figure 3.30 Indicating a Nyquist Plot.

It is to be observed that for the red colored curve the system shown in figure 3.30, it encloses the (-1, j0) mark of X – axis for which P2 is very small and for the green curve the system does not encircle the (-1, j0) mark of the same axis and thus for the green colored curve the system is unstable. Hence such a situation gives rise to a condition known as conditional stability. Thus for higher order systems care must be taken about stability and Nyquist Plot is one of the best possible ways.

One more important point is, if there is an extra pole P2 then in long run the response gets shifted as compared to ideal response and the horizontal shift is (1/P2). If there are two parasitic poles the actual response gets shifted as compared to the ideal response by 2/P2. In fact if multiple pole exist then with each pole a delay of (1/that pole) is contributed. Thus the plots of such systems are shown below:-

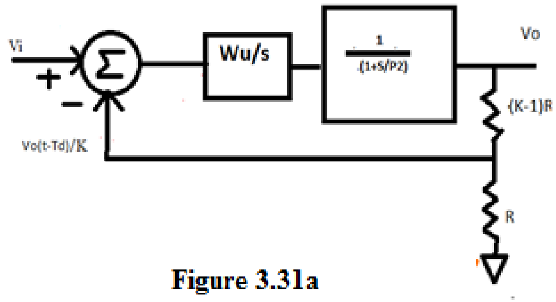


Figure 3.31a

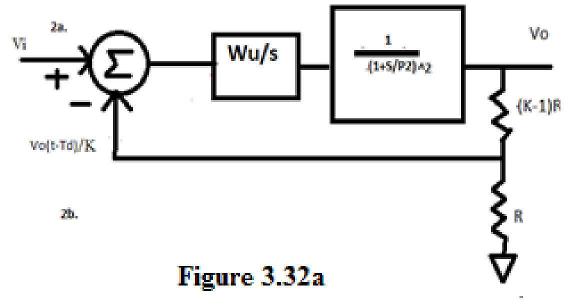


Figure 3.32a

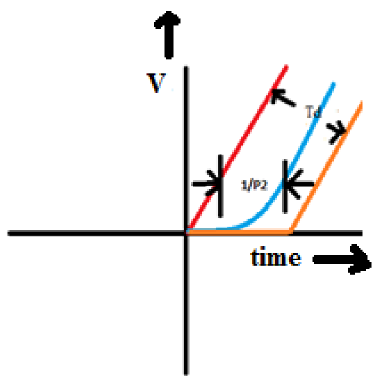


Figure 3.31b

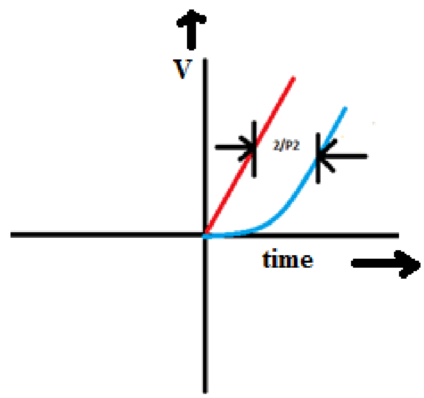


Figure 3.32b

Figure 3.31 (a) System with two poles. Figure 3.32 (a) System with three poles. Figure 3.31 (b) Indicates the relation of pole and delay for the system in figure 3.31 (a). Figure 3.32 (b) Indicates the relation of pole and delay for the system in figure 3.32 (a).

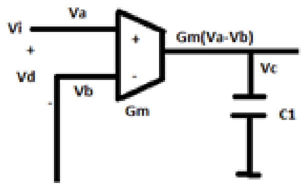
Thus a pole P2 is exactly similar to a delay of (1/P2).One thing exists as difference for system with pole and system with delay is with a single extra pole P2 ,the system is unconditionally stable .There can be ringing in system but there cannot be sustained oscillations. Now when there are multiple extra poles this can no longer be the case. Thus tabulating the results, in the below table:-

Table 4.1 Indicates the transfer functions of various ordered of systems and the limits up to which the respective systems are stable.

Parasitic poles	Loop gain	Remarks
No parasitic poles	$\omega u/K/_S = \omega u,\ loop/_S$	Never unstable.
One parasitic pole	$(\omega u,\ loop/_S) \times (\frac{1}{1+(S/P2)})$	Never unstable but can be underdamped if P2 < $\omega u,\ loop$.
Two parasitic poles	$(\omega u,\ loop/_S) \times (\frac{1}{1+(S/P2)})^2$	Unstable for P2 < 0.5 × $\omega u,\ loop$.
Three parasitic poles	$(\omega u,\ loop/_S) \times (\frac{1}{1+(S/P2)})^3$	Unstable for P2 < 1.13 × $\omega u,\ loop$.
Four parasitic poles	$(\omega u,\ loop/_S) \times (\frac{1}{1+(S/P2)})4$	Unstable for P2 < 1.76 × $\omega u,\ loop$.

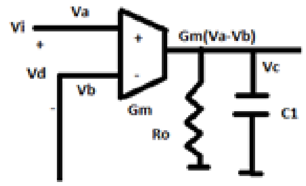
So to summarize an extra pole is like a delay and with delay one can have ringing in the system and if delay increases a lot one can have instability i.e. the system can give output without input. It can be thought as gain being equal to infinity at some particular frequency or the pole being at Right Hand Side of S plane. The same analysis of stability can be shown with Bode and Nyquist Plots. From the Bode plot of second order system under the situation of critical damping the value of Phase Margin is 76^0. The phase margin of $(60\text{-}70)^0$ are good.

The effect of non-ideality in op-amp as below:-



(Vo/Vd) = Gm/SC
Hence a pole at origin

Figure 3.33a



Vo/Vd = Gm/(SC + 1/Ro)
= GmRo/(1 + SCRo)
Here pole at LHS of S plane

Figure 3.34 a

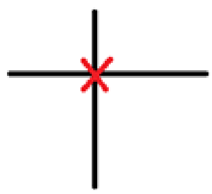


Figure 3.33 b

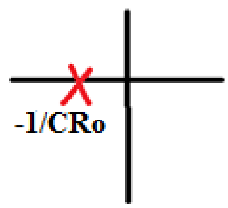


Figure 3.34b

Figure 3.33 a Shows the ideal single stage op-amp and its pole location is shown in Figure 3.33b. Figure 3.34 a Shows the effect of non-ideality on op-amp and its pole location is shown in Figure 3.34b.

At high frequency the impedance of capacitor is much low so most current passes through the short circuited capacitor but at low frequency the capacitor acts as open circuit and thus the current passes through Ro.

Bandwidth of the system for which the gain is unity is as below:-

$$\left| \frac{Gm}{(j\omega C + (1/Ro))} \right| = 1 \qquad (3.30)$$

On solving the above expression

$$\omega^2 = (Gm/C)^2 - (1/CR)^2 \qquad (3.31)$$

As long as $(1/CR) << (Gm/C)$ the unity gain frequency is (Gm/C) and this case applies for any op-amp.

To implement an op-amp there is a requirement of a VCCS, a capacitor and a buffer is also used at the output so as not to disturb the current flowing through the capacitor due to the load. Problem in a VCVS is that it has a finite output resistance and there exists a steady state error even for DC, the output will not settle to K times the input but will settle to something lesser than K times the input known as the steady state error or the DC error. Equivalently it can be thought of as the op-amp with a finite gain Gm × Ro i.e. (Ao) and thus pole moves from origin to ($-\omega u/Ao$) and finally result of this is a finite dc loop gain as Ao/K or a relative error in degree = (K/Ao).Thus apart from obtaining a high value of ωu which put constrains on Gm and C it is also required to make sure that whatever circuit is chosen to design Gm it must have a high value of Ro. More the accuracy is needed, higher must be the value of Ao. Thus care is taken so that the op-amp has a high DC gain.

3.4.3 DC open loop gain of op-amp:-

The DC loop gain is the product of DC gain and feedback network which results in the requirement of more and more complicated topologies. In order to increase the DC gain of the op-amp, there is a requirement of two stage amplifier. Below diagram shows the two stage operational amplifier.

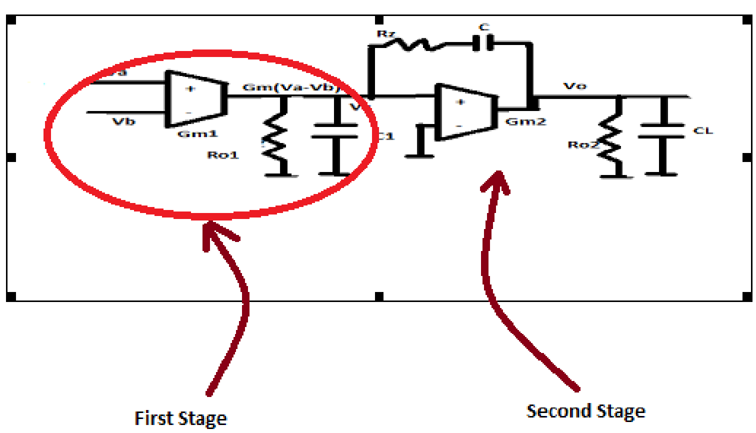


Figure 3.35 A two stage Miller Compensated op-amp.

Below diagram shows the single stage amplifier.

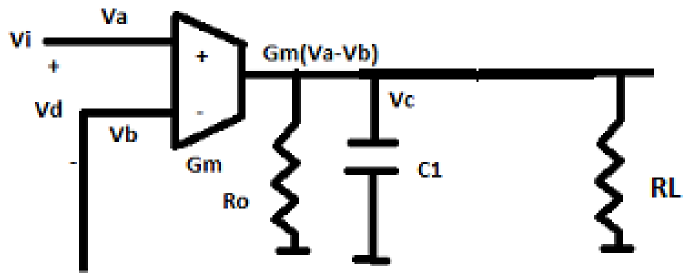


Figure 3.36 A single stage op-amp.

The purpose for adoption of two stage amplifier over a single stage amplifier are as below:-

- The DC gain is not good as compared to the two stage amplifier as in two stage there is a product of two gains.

- The power dissipation is much more in the single stage as in single stage if DC gain is required to be increased then the value of Ro must be improved and its combined effect with the load resistor, it brings about more power dissipation across the load resistor but in case of two stage the increase in gain is established in the first stage and a moderate gain is obtained in the second stage, this actually reduces power dissipation across the load resistor.

3.4.4 Miller compensation capacitance:-

Now let the Miller Capacitance be analyzed and let its effect be seen on the circuit. Below is the amplifier with the Miller Capacitor "C".

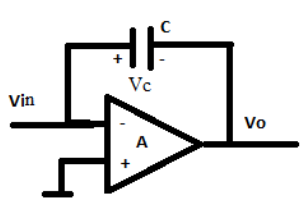


Figure 3.37 Circuit connected in the form of Miller Compensated Technique.

$$Vo = -A \times Vin. \quad (3.32)$$

In above equation "A" is the forward path gain of the amplifier shown in figure 3.37. Applying KVL over the amplifier above, + Vin – Vc - Vo = 0. Now putting the value of Vo from equation 3.32 above the below expression is obtained.

$$Vc = (A+1) \times Vin \quad (3.33)$$

Thus the voltage across the capacitor with the given polarity becomes Vc = (A+1) × Vin hence the capacitor would draw a current of (A+1) × Vin × SC where SC is the value of admittance through the capacitor. So in the block it appears as below:-

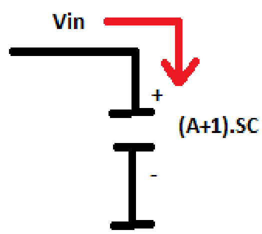


Figure 3.38 Shows an increase in Virtual Capacitance.

So the above is the Miller effect. If a capacitor is applied from the input to output of the amplifier, it appears to have a much larger value i.e. the product of (1+gain (A)) and Capacitance value. And this capacitor is sometimes called Miller Multiplier Capacitor. Now the second stage of the DC amplifier has a gain of Gm2 × Ro2, now considering Go2 as the conductance of Ro2, the input capacitance almost looks like $((Gm2/Go2) + 1)$ × C. Now let the consequences of placing the second stage (Miller Compensated CCVS) in the circuit be observed. For that let the below figure be observed:-

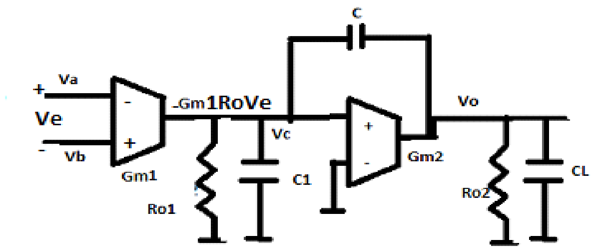


Figure 3.39 Represents a two stage op-amp.

Now let the Cramer's Rule be applied to find the Voltage gain of the above circuit as below:

$$\begin{bmatrix} S(C1+C)+Go1 & -SC \\ Gm2-SC & S(Cl+C)+Go2 \end{bmatrix} \times \begin{bmatrix} V1 \\ V0 \end{bmatrix} = \begin{bmatrix} -Gm.Ve \\ 0 \end{bmatrix} \quad (3.34)$$

$$\Rightarrow \frac{\begin{bmatrix} S(C1+C)+Go1 & -Gm1.Ve \\ Gm2-SC & 0 \end{bmatrix}}{\begin{bmatrix} S(C1+C)+Go1 & -SC \\ Gm2-SC & S(Cl+C)+Go2 \end{bmatrix}} \quad (3.35)$$

Thus Voltage gain:-

$$\frac{Vo}{Ve} = \frac{Gm1(Gm2-SC)}{S^2(C1C+CCL+CLC1)+S(C(Gm2+Go2+Go1)+C1Go2+C2Go1)+Go1Go2} \quad (3.36)$$

Thus DC Gain due to two stage as below:-

$$\frac{Gm1Gm2}{Go1Go2}. \quad (3.37)$$

Thus the above design has 2 poles at (left hand plane) and 1(right hand plane) zero. Here the right hand plane zero brings about a phase lag into the system. First the reason of occurrence of the right hand plane zero is found and then its nullification is taken care of. Below figure indicated the direction of current in second stage of Miller Compensation technique.

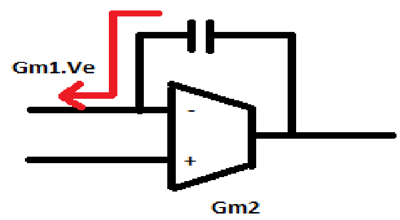


Figure 3.40 Indicating the direction of current in second stage of Miller Compensated Technique.

The current Gm1 × Ve supplied by first trans-conductor is passed through CCVS of the second stage. Gm1Ve will pass through the capacitor and it causes a voltage drop of $(Gm1/SC)$ × Ve. This is the exact voltage that is required, but this is not the actual voltage that appears as Vo. The actual voltage Vo is equal to the sum of the voltage across the capacitor and the voltage between Vx (voltage at the mentioned terminal in figure 3.41) and ground and this will have a voltage that is equal to the current through the trans-conductor divided by the trans conductance value of second stage, that is Gm2 when assumed that there is no loading effect at output. Thus the current Gm1 × Ve passes through the capacitor and comes out of the trans-conductor only when the voltage drop developed across the capacitor is greater than the Vx. For the entire analysis of the given paragraph the figure below can be referred.

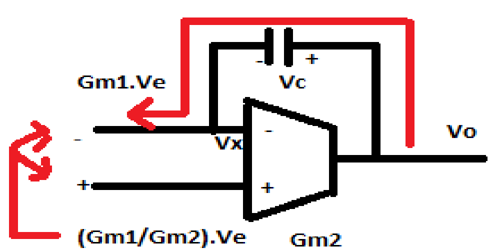


Figure 3.41 Represents current direction and Voltage drops in the second stage of Miller Compensated Technique.

Thus the expression of total Voltage is as below:-

$$Vo = Gm1 \times Ve \times [(1/SC) - (1/Gm2)]. \tag{3.38}$$

$$\Rightarrow \; Vo = Gm1 \times Ve \times ((Gm2 - SC)/Gm2 \times SC). \tag{3.39}$$

Thus in the above expression it is found that a right hand zero is introduced on the S plane. Now to remove this right hand plane zero, a resistor (Rz(let)) is introduced along with the capacitor, whose value is (+1/Gm2) and thus the RHP zero gets removed as in the figure below:-

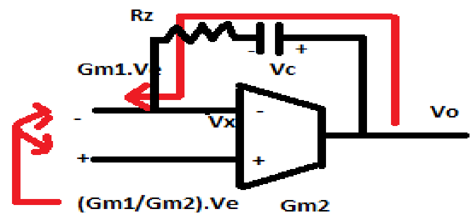


Figure 3.42 Represents a situation of compensation of an Right Hand Plane zero by resistor (Rz).

Thus the expression becomes as is mentioned below:-

$$Vo = Gm1 \times Ve \times [(1/SC) - 1/Gm2 + 1/Gm2]. \tag{3.40}$$

Hence removing the right hand plane zero.

The effect of introducing Rz is that it introduces a pole at high frequency (which can also be shown) whose effect is much less than the right hand plane zero but this action cannot be overdone as the insignificant pole might become significant and in fact cancel out the nullification process that is carried out to cancel out the right hand plane zero.

One more advantage of introducing Miller Compensation capacitor is pole splitting. Actually the second stage of amplification introduces a pole due to non-idealities and if this pole happens to be within the unity gain frequency of the system then it is going to make the system unstable. Now due to this Miller Compensation the pole that is produced due to the non-idealities moves to a higher frequency and thus allowing the system to continue its functionality in a stable manner.

The features of two stage operational amplifier are as follows:-

1. Using a capacitive trans-impedance second stage results in a better op-amp.

2. DC gain is the product of two stage gain.

3. Two stage miller op-amp has 2 poles and a RHP zero.

4. First stage of the output pole at a low frequency due to Miller effect.

5. Second stage output pole at a high frequency due to feedback around second amplifier.

Now so as to improve the DC gain, the above process can be built for three or four or even five stages when there is a requirement of a very high gain but the problem is ωu, loop5> ωu, loop4> ωu, loop3> ωu, loop2> ωu, loop1 must be maintained where ωu, loop is unity gain frequency of the system with feedback loop and the above situation constrains the ωu, loop1 which happens to be the ωu, loop of the system, as there is always a limit up to which highest value of ωu, loop can go. The below diagram represents the three stage Nested Miller op-amp:-

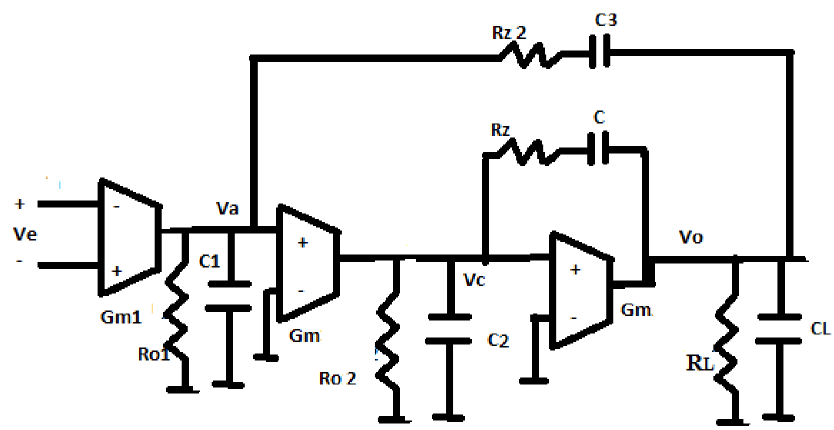


Figure 3.43 Three stage Miller Compensated.

3.4.5 Feed-forward compensated op-amp:-

Now an alternative to the above situation is a feed-forward compensated op-amp. Below design represents the same:-

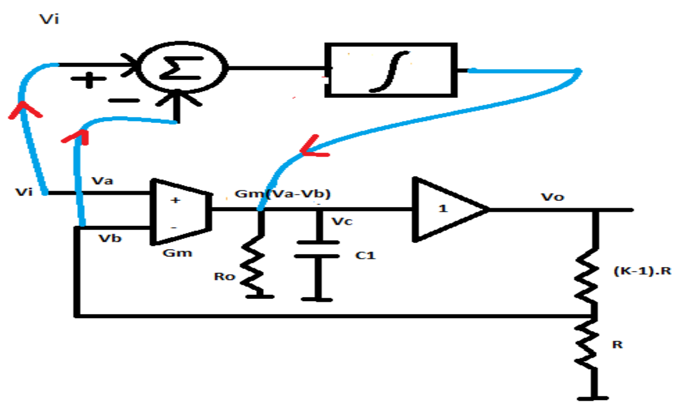


Figure 3.44 Feed-forward compensated op-amp.

In the above system, when the response has reached steady state with a steady state error existing between desired output and actual output, then the difference is computed and then it is made sure that across Ro potential is generated due to the current output of the integrator and not the current output due to trans-conductor. The integration that happens in the top stage happens very slowly and starts only when Vo has reached steady state due to the lower amplifier. The greatest advantage of this amplifier is that this amplifier can even reduce the steady state error to zero.

The following feed-forward amplifier can be implemented by the one as below by two stage compensation:-

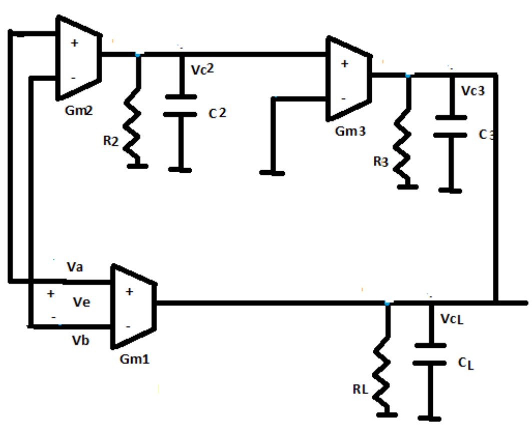


Figure 3.45 Representation of two stage feed-forward compensated op-amp.

Now let a second order Transfer Function of the two stage feed-forward compensated transfer function be obtained (reference to figure3.45) be looked upon and its stability be analyzed. Thus the transfer function is as below:-

$$\frac{Gm1}{Gl+SCl} + \frac{Gm2 \times Gm3}{(Go2+SC2) \times (Gl+SCl)} \quad (3.41)$$

$$\Rightarrow \frac{Gm1 \times (Go2+SC2)+(Gm2 \times Gm3)}{(Go2+SC2) \times (Gl+SCl)} \quad (3.42)$$

$$\Rightarrow \text{Ao} \times \frac{(1+ S/_{Z})}{(1+ S/_{P1}) \times (1+ S/_{P2})} \quad (3.43)$$

In the above expression the term $\frac{Gm1}{Gl+SCl}$ is due to the first stage and the term $\frac{Gm2 \times Gm3}{(Go2+SC2) \times (Gl+SCl)}$ is due to the second stage of the amplifier shown in figure 3.45 where Gl is the reciprocal of RL and Go2 is the reciprocal of R2.

So if the Bode Plot of the above transfer function is drawn, it appears as below:-

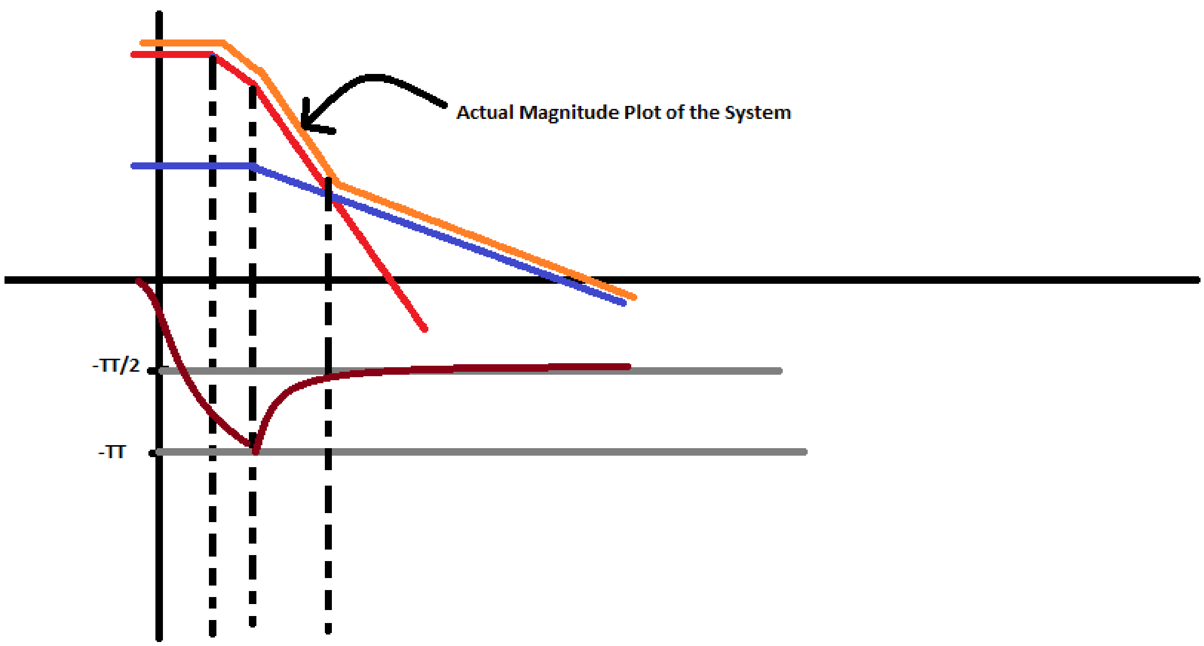
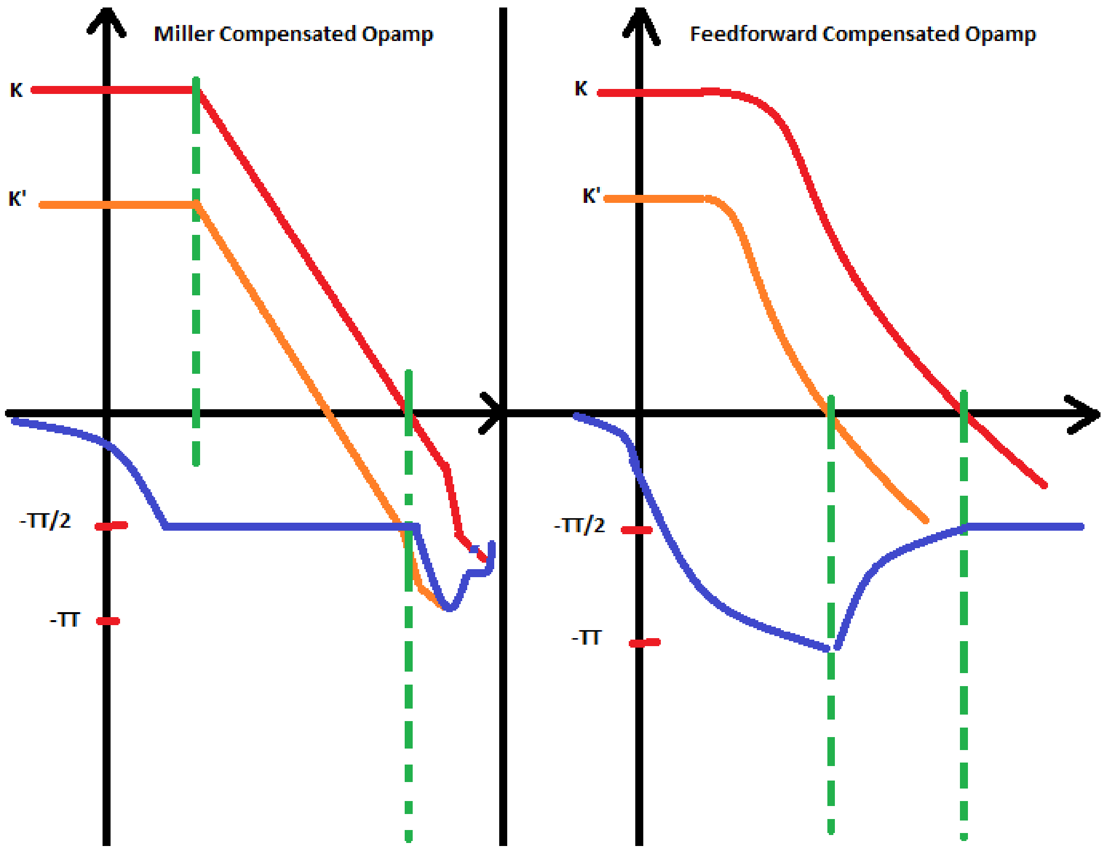


Figure 3.46 Bode Plot for two stage feed-forward compensated op-amp.

In the figure 3.46, the above plot indicates the magnitude plot and the lower one indicates the phase plot. So now if stability curves which compares about the stability of Miller Compensation technique and feed-forward compensation techniques are drawn then following findings are obtained.

3.4.6 Comparison between Miller compensated and feed-forward compensated op-amp.



Figures 3.47 Bode plots of Miller Compensated and feed-forward compensated op-amps respectively (comparison).

The above two plots indicate the responses (Bode Plots) of two different types of amplifiers. Both systems are found to be stable when the gain is K. But at K' Miller Compensated op-amp is found to be stable whereas the feed-forward compensated amplifier is found to be unstable.

Only one advantage of Miller Compensation over the feed-forward compensation technique is that a Miller Compensated circuit is an unconditionally stable circuit but the feed-forward compensated is a conditionally stable circuit. Else there are only positive aspects of feed-forward compensated circuits. They are as follows:-

1. They have a higher bandwidth.

2. Will consume less power.

3. Always give accurate results as far as reaching steady state is concerned.

But as far as the problem of less stability condition is concerned it can be solved in case when the system gain is given. Most commercial op-amps that are available in the market are Miller Compensated ones.

3.4.7 Some data sheet contents of op-amps:-

As of now the last thing about op-amps is what one finds in the data sheet of op-amps. They are as below:-

1. DC gain.

2. AC magnitude and Phase response.

3. Slew Rate.

4. Offset and noise voltages.

5. Other limits: maximum supply voltages, maximum load current etc.

The above specifications are general where there may be single and multistage op-amps.

Hence the block level analysis of op-amps are completed. The transistor level analysis is carried out in next chapter.

CHAPTER 4

ANALYSIS OF OPERATIONAL AMPLIFIERS AT A TRANSISTOR LEVEL.

In this section, most of the important analysis till a basic single stage differential amplifier with a current mirror load is discussed at transistor level. The reason to consider it to a great depth as it forms the basis of the op-amp design.

4.1 Analysis of circuit topology:-

For an op-amp there is a need for a circuit topology which would amplify the difference between the input voltages. There is a need to have a high dc gain, in fact infinite. Below diagram represents the same.

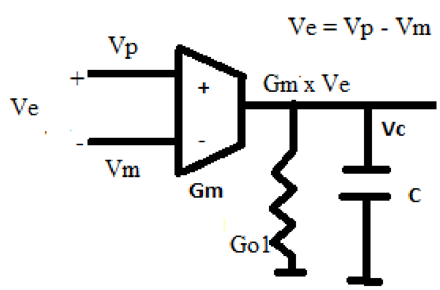


Figure 4.1 Single stage differential pair.

In the above op-amp shown, ideally $(Gm/Go1)$ = infinite, where Gm is the trans-conductance and Go1 is the admittance of the shown resistance of the trans-conductor. Thus there is a requirement of designing the amplifier that has a very large gain. Now starting with the basic amplifier that is known, are common source (CS), common gate (CG) and common drain (CD) amplifiers. First the common drain amplifier is ruled out as it has a voltage gain equal to 1. As for the op-amp, there is a need of a high gain and high input impedance hence it requires a common source amplifier. The CS amplifier amplifies difference between two input voltages as shown in below figure.

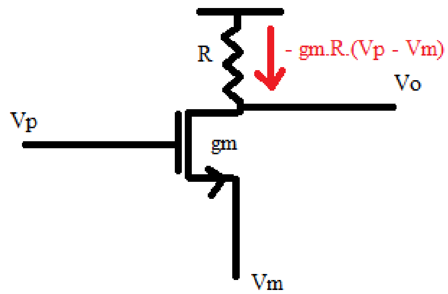


Figure 4.2 Basic CS amplifier showing its capacity to take the difference of two input voltages into consideration.

In the above figure Vp and Vm happens to be input voltages that are applied to the gate and source terminals respectively. The CS amplifier amplifies the difference between Vp and Vm and generates a proportional current gm × R × (Vp - Vm).

Now let the analysis of what is seen by Vp and Vm respectively are carried out independently. For its analysis below figures must be observed.

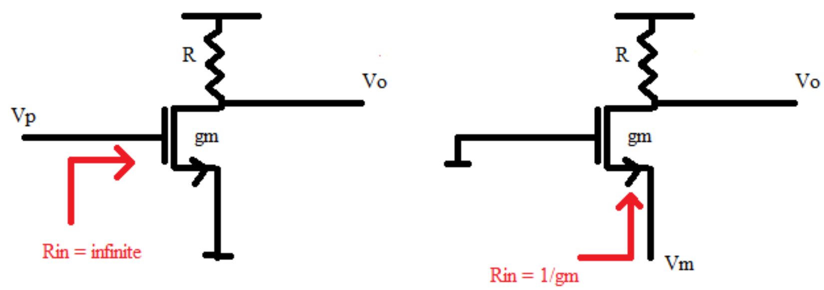


Figure 4.3 Shows the nature input impedance as seen by inputs Vp and Vm respectively.

In the above figures, the CS amplifier when seen from input Vp, the input impedance appears to be very large whereas when seen from input Vm, the input impedance appears to be very low. Such a situation is undesirable as the requirement is to sense the difference between input and feedback without disturbing the negative feedback system. Hence there is a requirement of a voltage buffer at the source terminal of unity gain value which would prevent the adverse effect of presence of any heavy load at the source terminal over the input gate. Hence the system represented as below:-

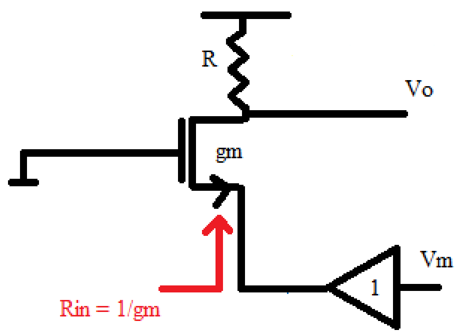


Figure 4.4 Shows CS amplifier with voltage buffer at source terminal.

As it is known that the basic voltage buffer happens to be the common drain amplifier or the source follower as shown below:-

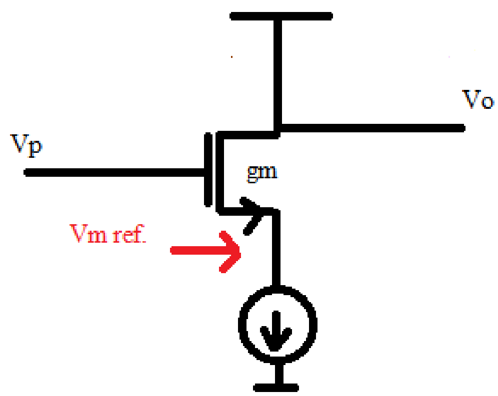


Figure 4.5 Shows a CD amplifier.

The CD amplifier can be used in conjunction with the CS amplifier which can enhance the difference between the two input voltages. In the figure 4.5 the point where Vm reference is obtained is marked as Vm ref. The circuit would be as below:-

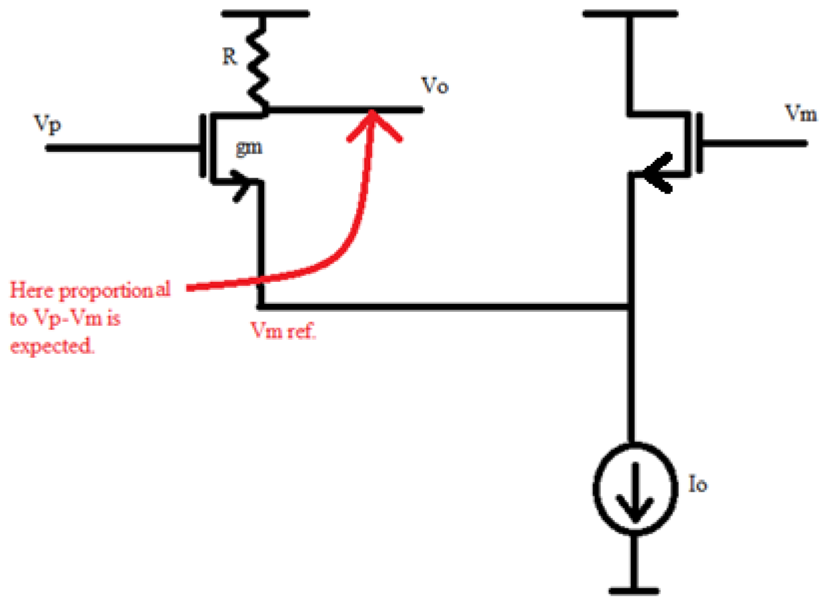


Figure 4.6 CS and CD amplifiers in conjunction with one another to develop a difference of two input voltages.

Thus the above design looks as below:

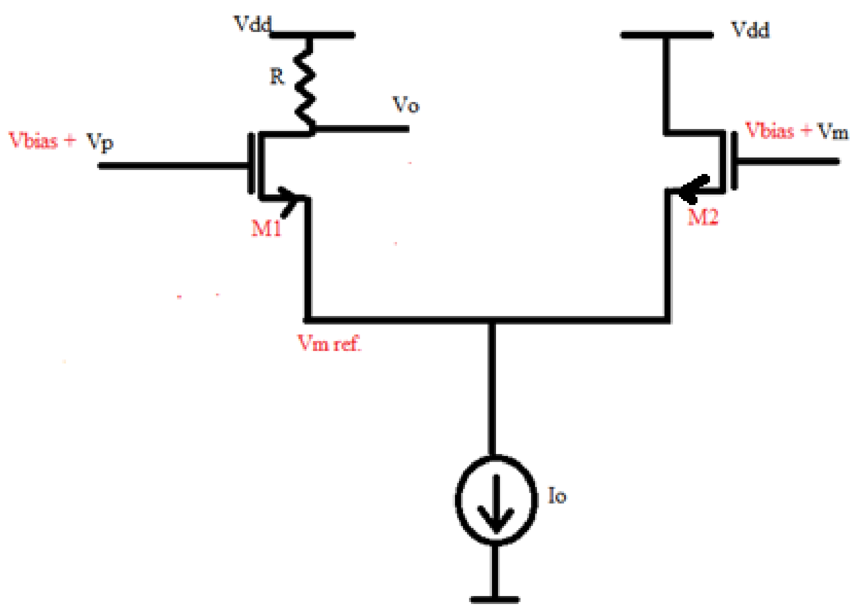


Figure 4.7 CS and CD amplifiers joined to obtain the difference of Vp and Vm.

In the above representations Vp and Vm are really small voltages so on both sides input bias is applied to both transistors named as Vbias. In all analysis it is assumed that there is no drain to source conductance i.e. no (Gds) and the transistors are simply represented by Gm. As of now the body effect of the transistors are also ignored.

At first let the quiescent condition or the operating point be determined. At quiescent condition both Vp and Vm are zero, Vbias is only present at both the input terminals and gate to source voltage Vgs of both transistors M1 and M2 as shown in figure 4.7 are equal. Now the basic assumption for the analysis is that all transistors are in saturation region. For a better analysis let the below figure be considered.

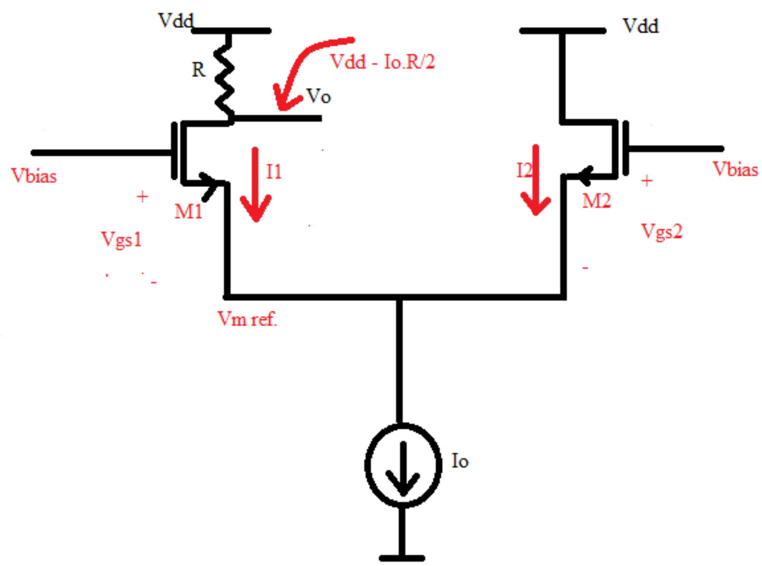


Figure 4.8 Showing the various voltage drops and the currents through various branches in the structure.

In the above figure I1 and I2 are equal as Vgs1 and Vgs2 are equal where I1 and I2 are the currents flowing through transistors M1 and M2 respectively. It was initially assumed that there is no influence of Gds in the circuit thus drain to source voltage Vds has no influence on it and sum of I1 and I2 equals Io and each of I1 and I2 equals Io/2. It was also assumed that the transistors are in saturation because the trans-conductance of transistors are highest in saturation region and the influence of Gds is lowest hence saturation is preferred to as the region of operation of the transistors. Thus the quiescent operating region is fixed. Now at the given operating point the transistors M1 and M2 will have some trans-conductance, let it be called Gm1. Thus the small signal picture of the amplifier is as below:-

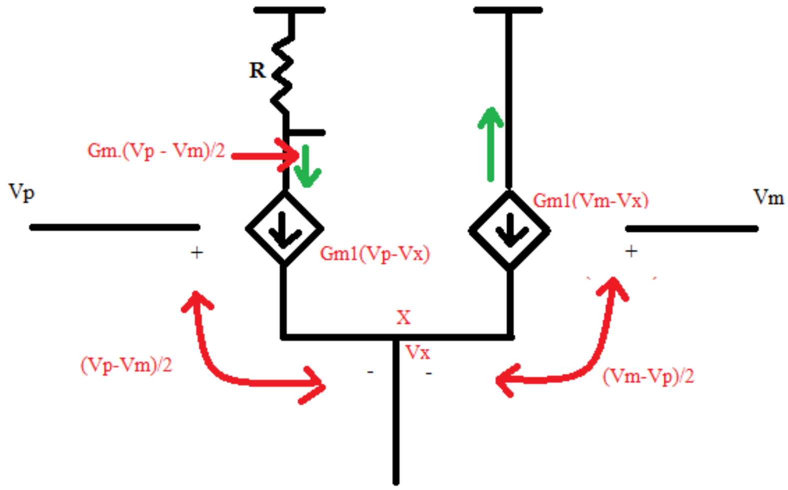


Figure 4.9 Small signal picture of input difference stage.

The node X as shown in figure 4.9 is assumed to have a voltage of Vx. Thus the value of net current at node X is [Gm1 × (Vp - Vx)] + [Gm1 × (Vm - Vx)] = 0. Hence

$$\mathrm{Vx} = \frac{(Vp+Vm)}{2} \tag{4.1}$$

Thus the incremental current in M1 is same as incremental current in M2 in other direction. So as expected, a small signal current is obtained that is proportional to (Vp - Vm) which flows through load resistance R and has a output voltage Gm.R.(Vp-Vm)/2.

In the original CS amplifier, the case where Vp was applied to gate and Vm was applied to source, an incremental current of Gm × (Vp - Vm) was expected and the important thing was that source was driven by an imperfect buffer. The buffer's output impedance was not zero but equal to $(1/Gm)$ of that transistor. Now in case of CS amplifier its source is not exactly at ground but connected to ground through a small resistance $(1/Gm)$, thus the gain from Vp to output changes and also as far as the buffer is concerned, it is not terminated by a very high impedance. It is terminated by $(1/Gm)$. So Vm does not appear at source of M2 with a gain of"1", in fact it appears with a gain of "1/2" as $(Vp - Vm)/2$ is obtained. Hence the output voltage obtained is Gm.(R/2).(Vp - Vm). But that is perfectly fine as the output current is proportional to (Vp - Vm) and that was actually wanted. Thus the expression of total voltage at output is as below:-

$$[\text{Vdd} - {}^{Io.R}/_{2}] + [-\text{Gm} \times ({}^{R}/_{2}) \times (\text{Vp} - \text{Vm})]. \tag{4.2}$$

Hence the small signal output voltage is the amplified version of (Vp - Vm). Thus the amplifier with all the voltage values shown are presented below:-

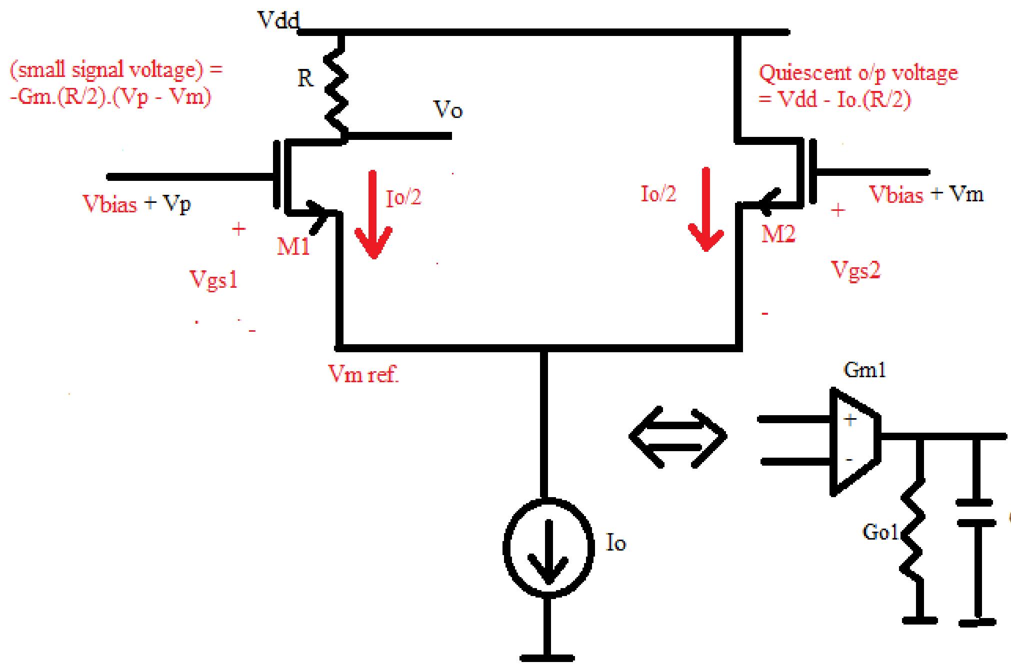


Figure 4.10 Shows voltages developed by the amplifier and also represented with some output conductance and a connected capacitor.

Ideally there would be no output conductance Go1 but there is a need of some output resistance to bias the circuit which results in a DC gain of $(Gm1/Go1)$ which is nothing but $(Gm1.\,R/2)$, where R is the reciprocal of Go1. So if the circuit in figure 4.10 is observed, it is symmetrical w.r.t. M1 and M2 but not symmetrical as a whole as resistance is seen to be connected to the drain of M1 and not to that of M2 but the quiescent condition is symmetrical and thus R can be connected to M2 as well. The below figure shows the same.

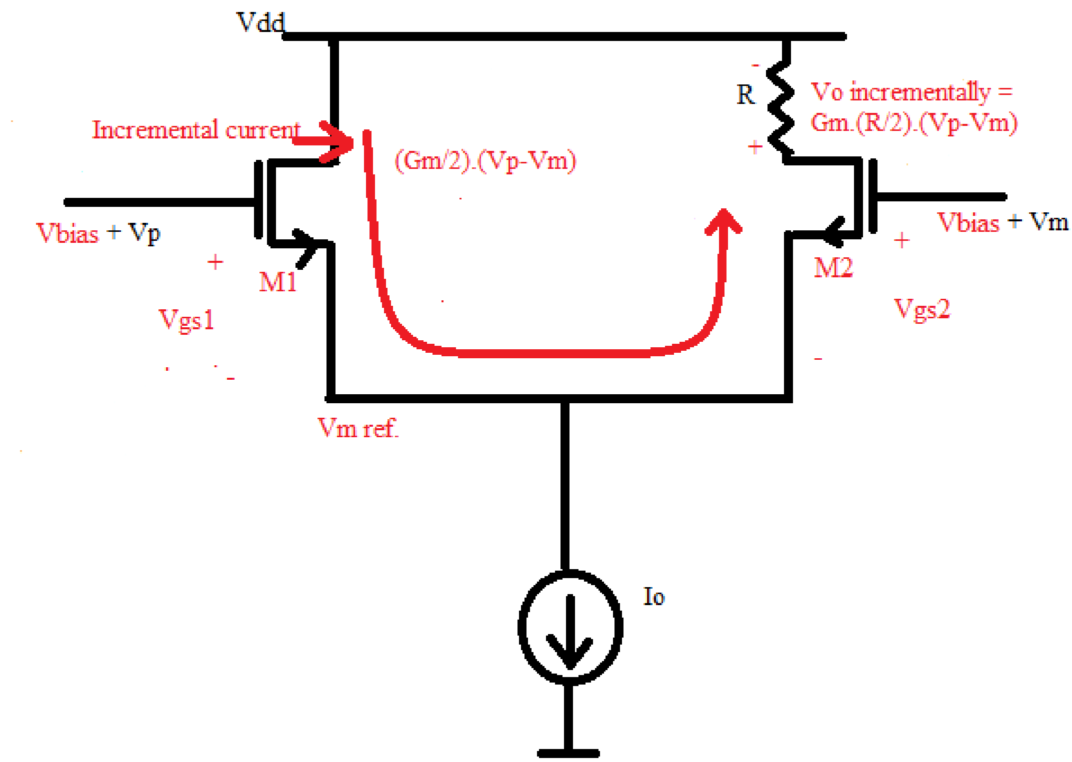


Figure 4.11 Shows the symmetrical circuit of figure 4.10.

It is like interchanging of Vp and Vm and obtaining a gain of Gm.($R/2$) instead of - Gm.($R/2$). Thus in order to make the circuit symmetrical the following can be done as indicated in below figure:-

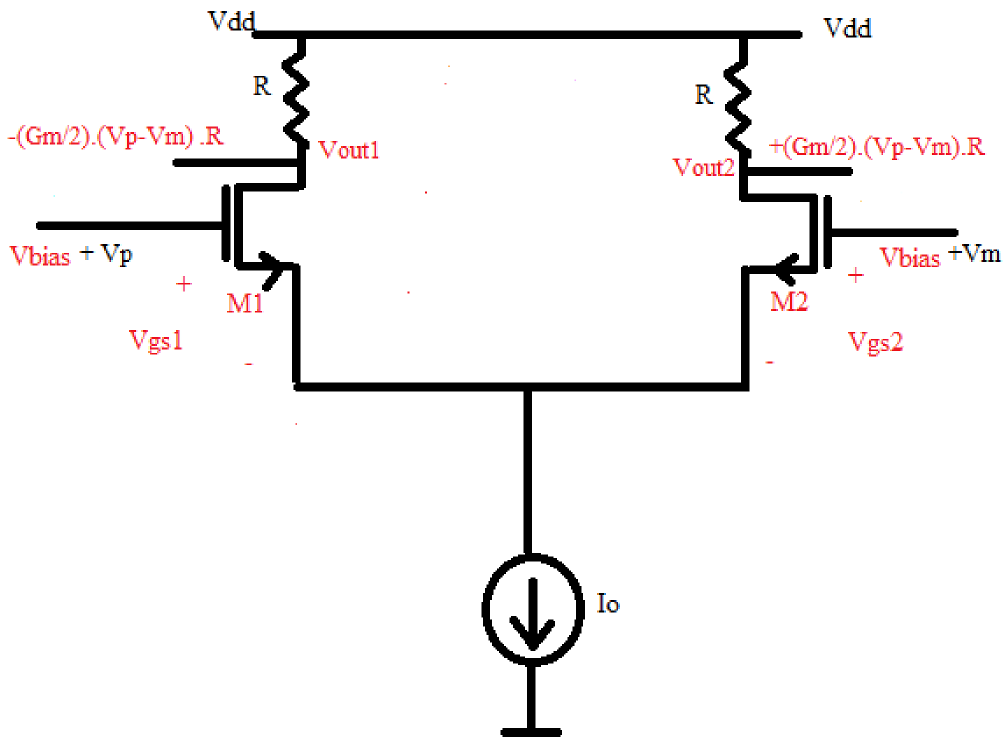


Figure 4.12 Symmetrical structured amplifier.

In the above figure 4.12, if the difference between the terminals Vout1 and Vout2 is considered then Gm × R × (Vp-Vm) is obtained. So the requirement to obtain some output related to the difference between Vp and Vm has given the above circuit. The way it was started was with a CS amplifier as it is the only known thing which could give an appreciable gain and amplifies the difference between gate and source. So one of the voltage sources was connected to gate terminal and the other voltage source was connected to the source terminal but the impedance looking into the source was very low. Thus instead of connecting it directly, it was connected through a source follower. The whole circuit was put up with two transistors M1 and M2 respectively and current in two transistors are related to the difference of Vp and Vm. Now this current can be integrated in a capacitor and for biasing reasons there is also a requirement of a resistor. Thus the discussed circuit forms the first stage of the circuit which is the differential pair.

4.2 Differential pair formation:-

Now the complete symmetrical circuit that was put up last where the resistance was placed at the drain of both the transistors would be discussed. Its diagram is shown below:-

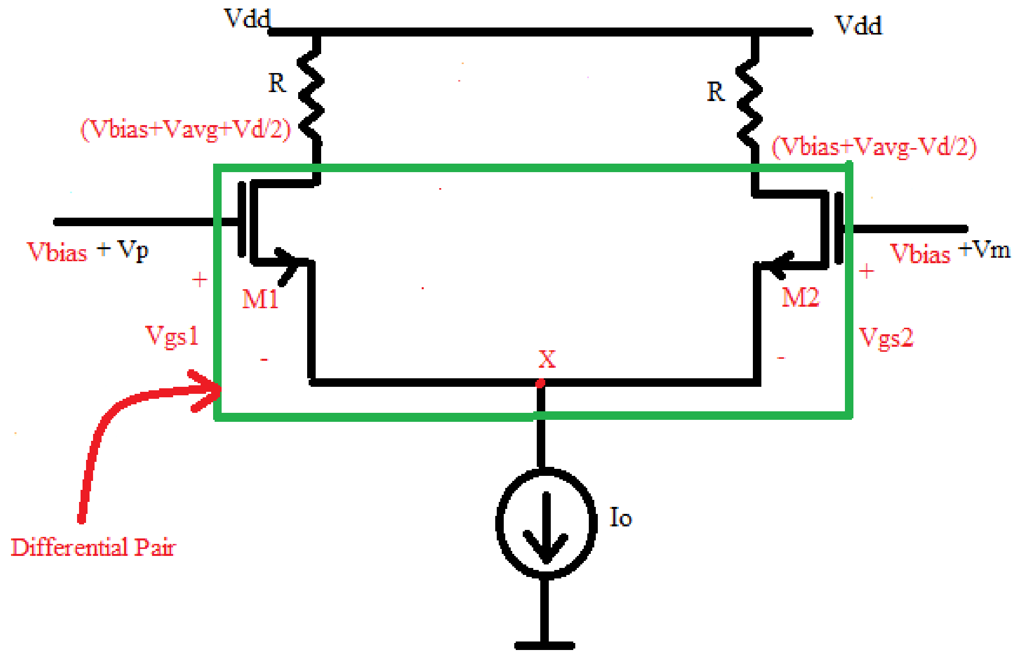


Figure 4.13 Symmetrically loaded differential pair.

In the above figure node X is called a tail node and the current source Io is called a tail current source. For the above drawn differential pair both the large signal and small signal analysis is required to be done. The drain to source voltage Vds of the two transistors is zero and the ideal current source Io does the biasing of the two transistors.

Vp and Vm are expressed as an average voltage value of the following form as expressed as below:-

$$\text{Vavg} = \frac{Vp+Vm}{2} \pm \frac{Vp-Vm}{2}. \tag{4.3}$$

Where $\frac{Vp+Vm}{2}$ is the common mode voltage and $\frac{Vp-Vm}{2}$ is the differential voltage. It is very obvious that common mode voltage has no influence on the circuit when the current sources are ideal but they do have otherwise. As of now Vavg is ignored and thus +Vd/2 is considered as an input on right side and –Vd/2 is considered as an input on the left side.

4.2.1 Large Signal Analysis of Differential Pair:-

The below diagram could be useful for the analysis of differential pair.

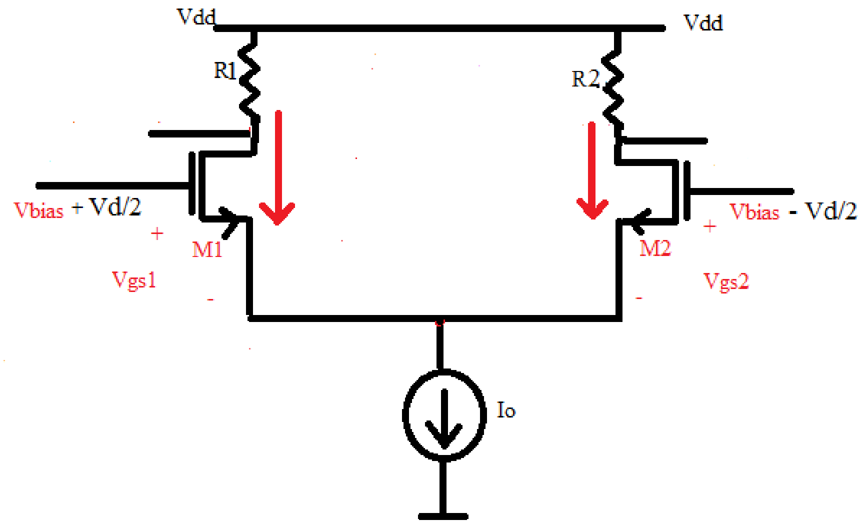


Figure 4.14 Schematic of Differential Pair.

The above schematic of differential amplifier would be useful for large signal analysis. In above if Vd/2 is positive then gate to source voltage (Vgs) of M1 is more than Vgs of M2 so I1 will be more than I2 and similarly when Vd/2 is negative then Vgs of M1 will be less than that of M2 and I1 will be less than I2 as represented in figure 4.14. Now when Vd is zero, then both I1 and I2 equals Io/2. Below plot shows I1 and I2 as a function of Vd.

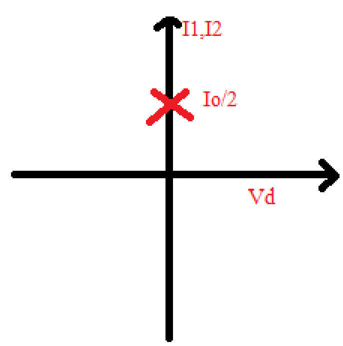


Figure 4.15 Location of Io/2.

Now for a small value of Vd, deviation happens to a small extent in operating point so the small signal analysis holds. Thus the incremental currents are as, current in M1 is $(I1/2) + (gm/2) \times (Vp - Vm)$ and that in M2 is $(I1/2) - (gm/2) \times (Vp - Vm)$. Now for small value of Vd, there would be straight lines at point $Io/2$ with a slope of $Gm/2$ or - $Gm/2$ depending upon whether I1 or I2 is talked about at Vd = 0. At Vd very large, as Vd increases Vgs of M1 goes on increasing and at some point it would become so large that the current corresponding to that voltage becomes Io. It is already known that in quiescent condition M1 draws a current of $Io/2$ and as Vgs is increased, it will increase from $Io/2$ and at some point current in transistor M1 becomes equal to Io. So obviously current in M2 becomes equal to 0. Thus the transistor M2 goes in cut-off and for any increase in Vd beyond this point transistor M2 cannot have a current that is less than zero. So it will continue to have a current of 0 and transistor M1 will continue to have a current of Io. The above phenomenon will happen when Vgs of M1 is such that the entire current Io travels through M1. Thus the overdrive at quiescent condition of M1 and M2 is Vt + $\sqrt{\frac{2 \times {}^{Io}/_{2}}{un \times Cox \times ({}^{W}/_{L})}}$. The quiescent condition at which all of Io is going through M1 is Vt + $\sqrt{\frac{2 \times Io}{un \times Cox \times ({}^{W}/_{L})}}$. When M1 is carrying Io it means that the value of Vd is increased such that current in M1 just reaches Io and current in M2 just reaches 0. So when current in M2 just reaches 0, its Vgs just reaches Vt. Thus the difference between these two transistors is Vd = $\sqrt{\frac{2 \times Io}{un \times Cox \times ({}^{W}/_{L})}}$. Where µn is the mobility of electrons, Cox is the oxide capacitance and $({}^{W}/_{L})$ is the ratio of width to length of a MOS transistor. The below diagram represents the above phenomenon.

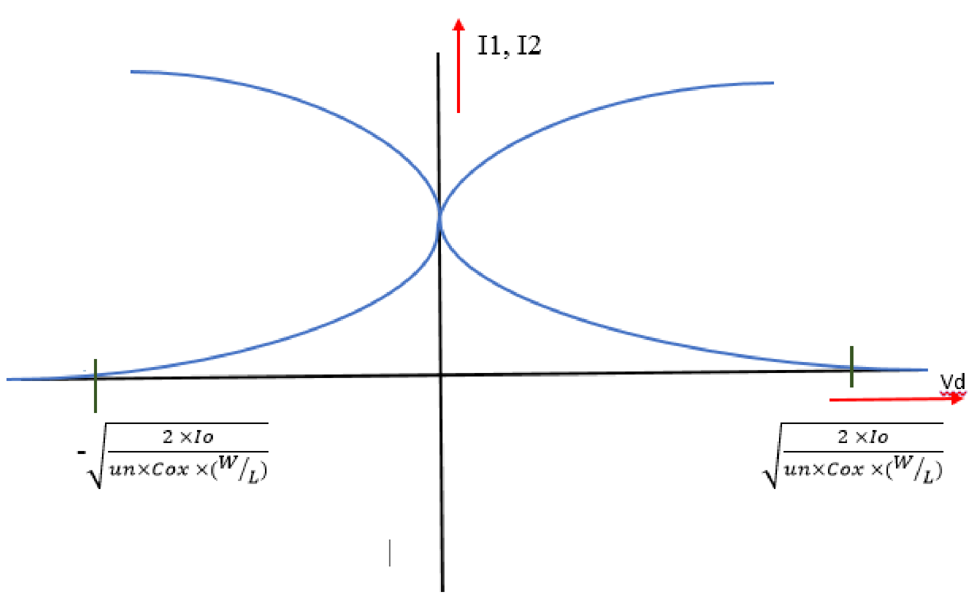


Figure 4.16 Represents tail current vs. differential input curve.

Thus at a voltage of $\sqrt{\frac{2 \times Io}{un \times Cox \times (W/_L)}}$ current in M1 will be Io and that in M2 will be 0. The circuit is symmetrical and hence at a voltage of - $\sqrt{\frac{2 \times Io}{un \times Cox \times (W/_L)}}$ current at M2 reaches Io and that in M1 will be 0. When the differential pair is operated with small differential voltage then currents are linearly related to difference. In fact the differential pair is designed as a means of having some current that responds to the difference between two voltages and also presents a very high impedance to both the voltage sources. When the difference voltage Vd becomes very large, the circuit starts becoming non-linear like any other circuit and for a large enough Vd the currents in the transistors become constant. All of the tail current will flow through M1 or M2 and the other transistor will carry zero current. It is important to know the linear range at which the differential pair operates. In an op-amp it is good to know that when the current gets saturated and it enters the slew rate. Now for the above analysis the below circuit must be looked at:-

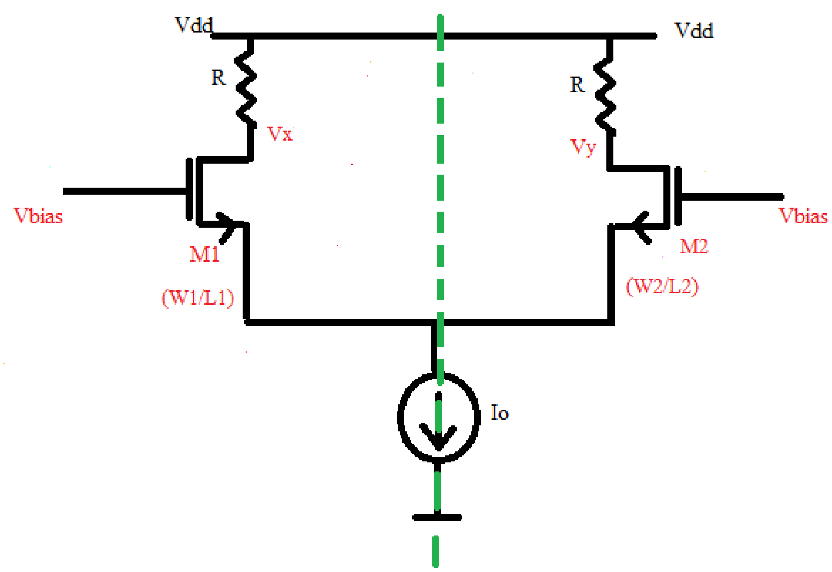


Figure 4.17 Represents the symmetrical structure of differential amplifier.

In the above figure it is assumed that the circuit is symmetrical about the indicated line of symmetry and the transistors are identical w.r.t. their (W/L) ratio i.e. M1 is equal to M2. Before it is transformed into an op-amp some important behavior of the circuit must be analyzed which includes the large signal and the small signal analysis. Now due to symmetrical nature of the above circuit if equal incremental voltages are applied to both the input terminals (common mode input) then Vx and Vy as shown in figure 4.17 would be generated which would be equal in nature. To do an in-depth analysis of the symmetry the below diagram must be considered which shows a network which is same on both the sides.

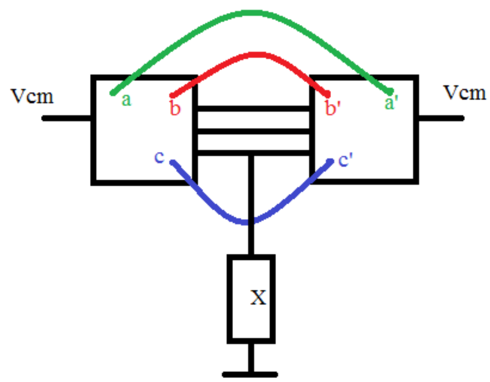


Figure 4.18 Represents symmetrical circuit with two identical networks.

Now both the networks of the circuit has equal number of nodes and equal inputs are applied on two sides. They together must be fixed to the ground and it is done by a component X. Now equivalence of components are shown by equivalent colors. As indicated in figure 4.17 that Vx is equal to Vy. Now in that case the corresponding nodes can be connected together by means of wires where the corresponding points have same potentials and no current would flow through the wires connecting them respectively. So the circuit is not disturbed anyway. Thus nothing changes due to the connection and the below change can be done.

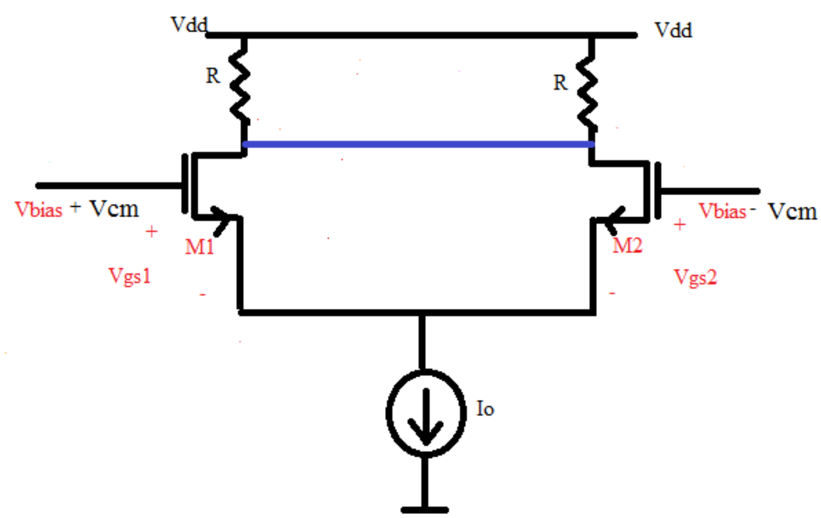


Figure 4.19 Showing the connection of similar points in a differential pair.

So the above modification significantly simplifies the circuit for the sake of analysis. Thus due to the above modification the two resistors and the two MOSFETS are seen to be parallel respectively. When it is said that two MOSFETS are parallel, it means that all its corresponding terminals are connected to each other (i.e. its two gates, its two drains, its two sources and its two bulks respectively). Thus the circuit in figure 4.19 can be converted into a single circuit with a single transistor as shown below:-

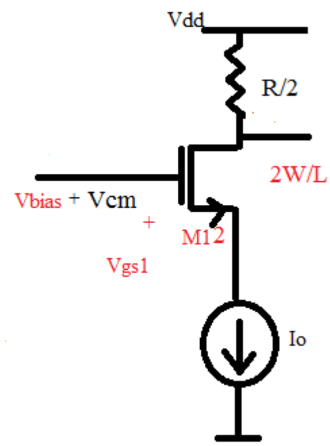


Figure 4.20 Single circuit for a differential pair.

Thus it is seen that where there were pairs of components, now there is only a single component for the two resistors and for two MOS transistors. It is also seen that the component along the central line of the circuit (here it is Io) will remain as it is. Thus the number of components in the new circuit will be little more than the half of the original circuit. Hence it brings about simplification in analysis. The newly formed circuit is called "Common Mode Equivalent Circuit". The common mode equivalent circuit is also called a common mode half circuit. Now let anti-symmetric inputs be considered on two symmetric sides of the circuit as is shown below:-

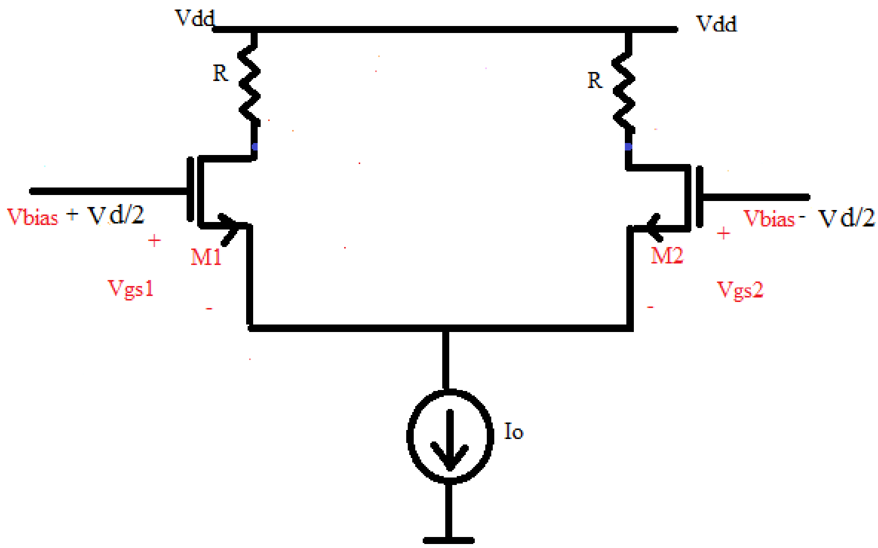


Figure 4.21 Differential Pair with anti-symmetric excitations.

Now considering the small signal equivalent of the above circuit. The reason for considering the small signal circuit of figure 4.21 is the small signal equivalent is linear. The below figure represents the small signal equivalent of the figure 4.21.

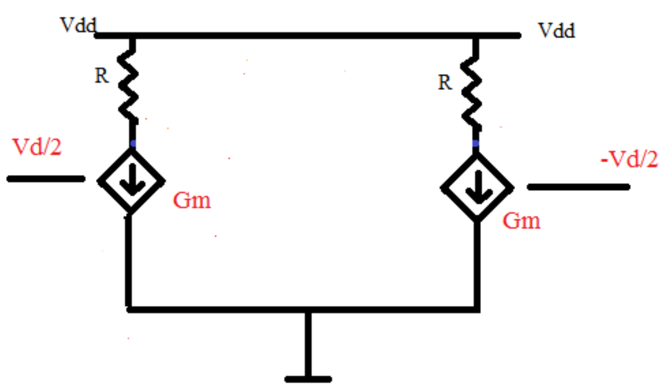


Figure 4.22 Small signal equivalent of differential pair with anti-symmetric excitation inputs.

Now let it be imagined that that there are two linear circuits which are exactly symmetrical with some nodes connected between them and containing some components and one input on each side. The components are linear and the excitations are anti-symmetric. Let the below circuit be considered.

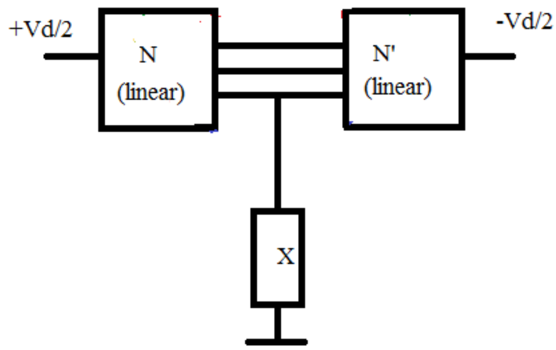


Figure 4.23 Symmetric system with anti-symmetric excitations.

Due to the property of linearity and symmetry, the linear and symmetric system with anti-symmetric excitations generates a zero volt along the line of symmetry. Applying this concept on differential pair as shown in the below figure:-

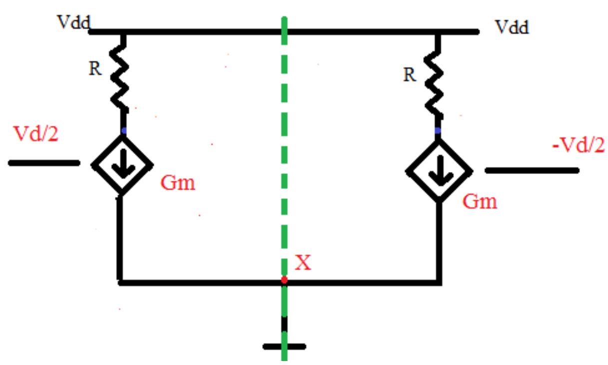


Figure 4.24 Small signal equivalent of a differential pair showing the axis of symmetry.

In the above figure due to the previously presented explanation the voltage at node X is 0 volts. This concept can be used to simplify the circuits. Thus due to linearity and symmetry, if voltage in a network at a point is Vw corresponding to the voltage in the other symmetrical circuit at the corresponding point is –Vw. To analyze the explanation below circuit can be referred.

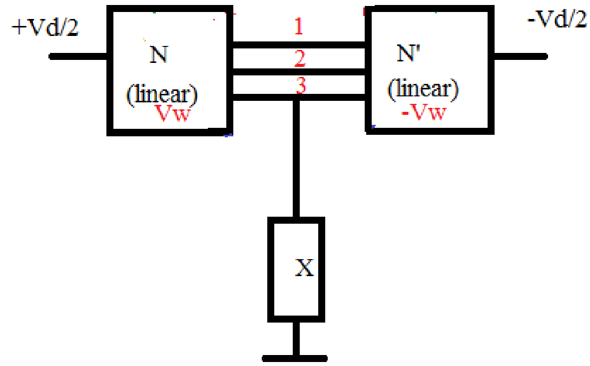


Figure 4.25 Symmetric system with anti-symmetric excitations showing the numbered network lines.

Thus the entire network need not be analyzed, by setting the network lines (1, 2, 3) in the above shown figure to zero analysis can be only on one half of the circuit and whatever voltages are present on the positive half of the circuit will be negated and the solution is obtained. Thus whatever is obtained as Vw on one side, -Vw is obtained on the other side. Thus in a differential pair analysis can be done on one side to obtain the required equations and the same can be applied to the other side of the differential pair with a negative sign. Below figure shows the same thing.

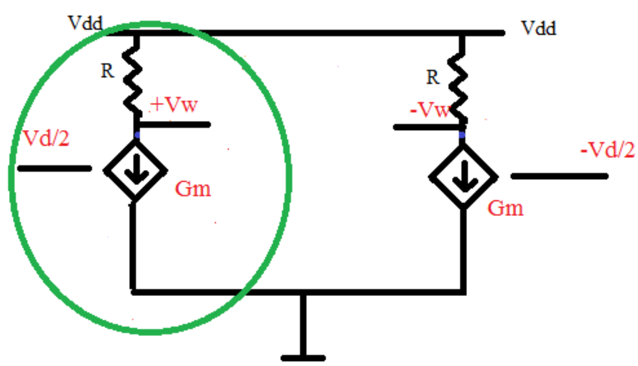


Figure 4.26 Shows that analysis can be done on encircled part and same can be applied on other side with a negated sign.

So with differential half circuit, analysis can be done only on one half of the differential circuit as shown below and the result of analysis can be put on the entire circuit.

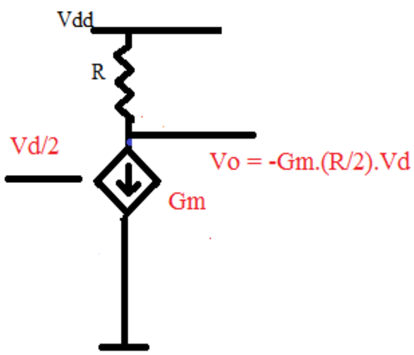


Figure 4.27 a Showing differential Half Circuit

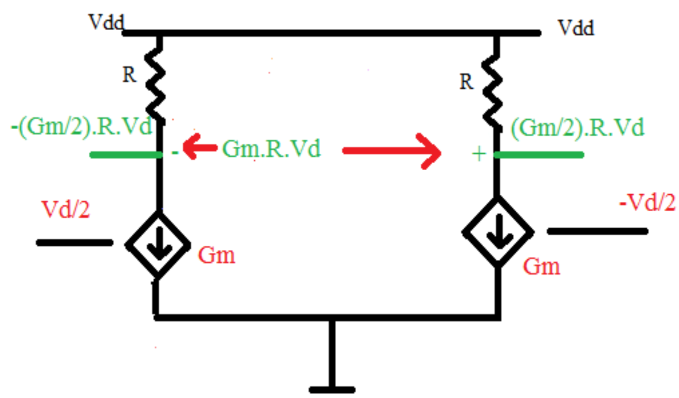


Figure 4.27 b Applying the concept of differental half circuit on differential pair.

The above circuit is known as differential half circuit just like the common mode half circuit. It reduces the number of components and makes the analysis much easier. These circuits are very useful when there are symmetric circuits with symmetric or anti-symmetric inputs. This analysis makes the circuits much simpler and this simplicity is much more useful when there are bigger and bigger circuits.

Now let the common mode equivalent circuit is again looked at as shown below.

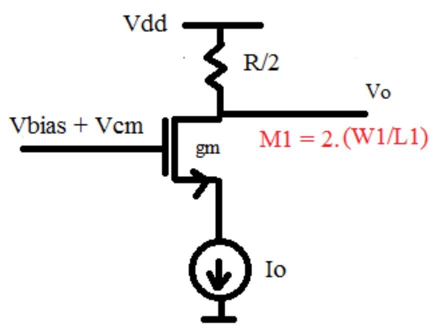


Figure 4.28 Common mode equivalent circuit of the differential pair.

Now it is very obvious that the common mode input voltage Vcm has no effect on the output voltage as the current Io has to flow into the source and also out of the drain. So the output voltage Vo is Vdd – Io × $(R/2)$ which is independent of input voltage. Thus the circuit does not respond to common mode inputs. Thus the common mode gain of an ideal differential pair is zero. As it was seen earlier that the expressions of common mode voltage ($\frac{Vp+Vm}{2}$) and the differential mode voltages ($\frac{Vp-Vm}{2}$) were developed and said that common mode voltage had no effect when the current sources are ideal is verified now and it is already seen the differential pair responding to differential mode voltage. Now instead of an ideal current source let a real current source be placed and then let it be analyzed. Since the current source was ideal thus the current through the combined load resistance is Io. Now in reality the current source is not ideal, it will have some finite output resistance as shown below:-

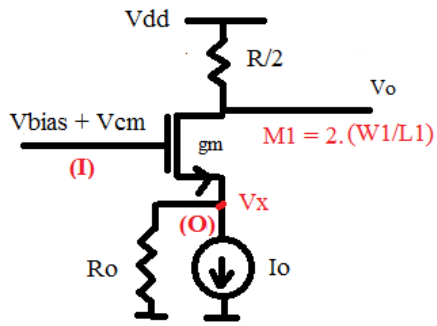


Figure 4.29 Source follower circuit with I as input and O as output with real current source.

Now as the increment voltage Vcm is applied, voltage at node Vx as shown in above figure increases. In fact if the circuit is thought of with "I" as input and "O" as output the circuit is a source follower. The quiescent voltage at Vx at Vcm = 0, is Vbias –Vgs (M1). The value of the above equation is as below:-

$$\text{Vbias - Vt - }\sqrt{\frac{2 \times {Io}/{2}}{un \times Cox \times ({W}/{L})}} + \text{Vcm} \qquad (4.4)$$

In the above equation each transistor can be thought of carrying a current $Io/2$ or a combined transistor carrying a current Io. When some increment Vcm is applied, there will be some increment in source voltage, the voltage across current source. Now as the circuit is a source follower, the increment is the input. From the previous knowledge it is known that at output the voltage is not exactly what is at input but is attenuated. Thus the total current going into the source of transistor was Io will change to (Io + Vcm/Ro) and similarly the quiescent output voltage was (Vdd – Io × (R/2)) will also change to (Vdd – Io × (R/2) + $({Vcm}/{Ro})$ × $({R}/{2})$). Thus practically the common mode input has no effect on output. Thus the common mode output is Vcm × $(R/2Ro)$ and thus the common mode gain is $(R/2Ro)$.

To analyze the common mode gain and differential mode gain below diagram must be looked at:-

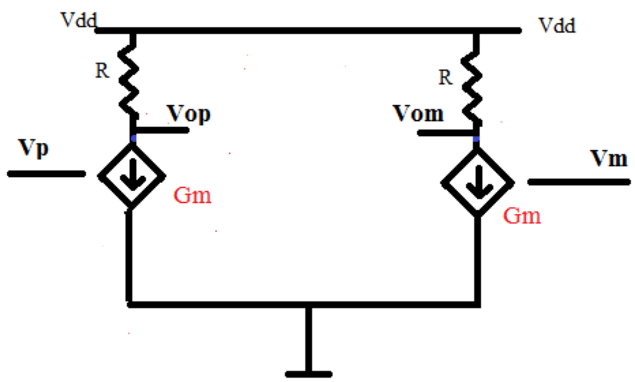


Figure 4.30 Differential pair showing the inputs and outputs of the system.

The differential gain is obtained as $\frac{Vop-Vom}{Vp-Vm}$ and the common mode gain is $\frac{(Vop+Vom)/_2}{(Vp+Vm)/2}$ from the above figure. When the same input is applied to the two sides, i.e. a common mode input is applied, then the outputs will also be the same as each other. So the average value is same as individual output voltages. Thus the common mode rejection ratio (CMRR) which is nothing but the ratio of differential gain to the common mode gain which is equal to $\frac{Gm \times R}{R/_{2Ro}}$ = 2 × Gm × Ro. Thus it is seen that the output resistance predominantly depends upon the output resistance of tail current source. Thus in order to improve the CMRR the resistance of tail current source must be improved. Now the above is the dc analysis, in many case the AC common mode gain analysis is also very important. In that case, the formula will exactly be the same except the resistance Ro will be replaced by an AC impedance Zo. Thus to improve the CMRR the value of Zo must be improved at all frequencies.

The purpose of concerning about common mode and differential mode inputs is explained as below. Suppose there is a pair of signal Vp and Vm. Instead of thinking the signals individually as Vp and Vm it must be thought as below:-

$$Vp = \frac{Vp+Vm}{2} + \frac{Vp-Vm}{2}. \quad (4.5)$$

$$Vm = \frac{Vp+Vm}{2} - \frac{Vp-Vm}{2}. \quad (4.6)$$

Where common mode voltage Vcm = $\frac{Vp+Vm}{2}$ and differential mode voltage Vd = $\frac{Vp-Vm}{2}$. It is preferred to think in the above way rather than thinking about Vp and Vm directly. Usually the circuit designers wish their circuits to respond to differential signal and not respond to common mode signal. Hence the signals are differentiated between differential mode and common mode. There are also alternative cases when the circuits respond to common mode and not to differential mode. Thus it is preferred to think Vp and Vm as common mode and differential mode rather than singly as functionally they make more sense.

Now a trial can be given to design an op-amp with a differential amplifier. The below circuits represent the same:-

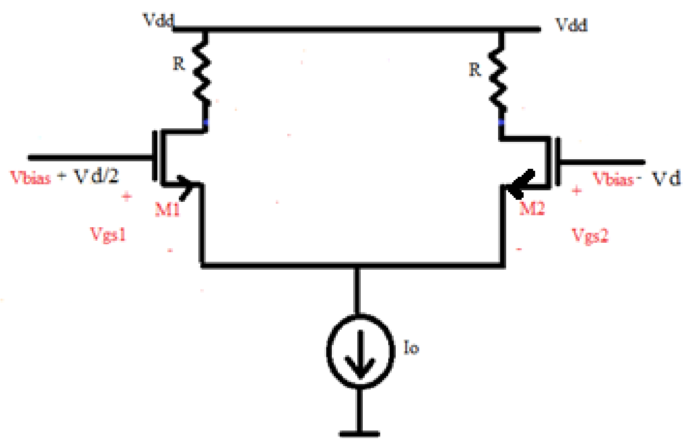


Figure 4.31a Represents a differential amplifier.

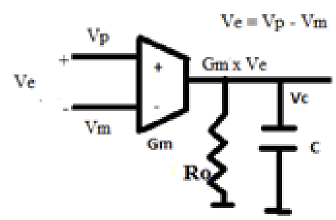


Figure 4.31b Represents an op-amp designed with a differential pair .

Thus whatever trans-conductance the op-amp is made, it will have a resistance Ro which is desired to make it maximized so as to improve the CMRR. In the circuit, the incremental current in the transistor is equivalent to the difference in the voltages. The circuit that is designed also has an output resistance, now the way the circuit is designed is completely symmetrical. So here one of the outputs can be considered and the other side can be ignored. So let's say that output can be taken from one side and it can be passed through the capacitor as shown in the below figure.

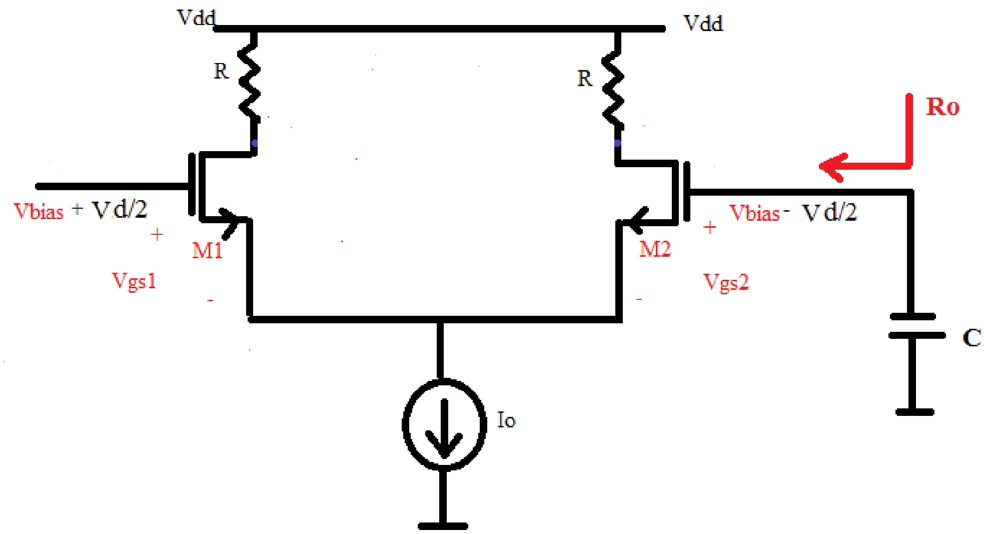


Figure 4.32 Differential pair with an output capacitor.

Now in the above figure it is also wanted that output resistance Ro is very large while looking at the given arrow mark. In the above figure $\frac{Vo}{Vd} = \frac{Gm \times R}{2}$. Now to increase the gain value, the value of R must be increased but if the value of R is increased, the DC drop across R will also increase as it is (Io × $R/_2$). Hence for that the supply voltage must be raised so as to keep all transistors in saturation. The above situation cannot be applied to real circuits as in real circuits there is always a limitation of supply voltage. Thus this way is not a good way to increase the DC gain and by this process better op-amps cannot be designed. So there is a need to replace the resistance value which will look like a very high value of resistance but it won't demand a high potential drop. It is known that an active load i.e. using a MOS transistor as a current source is a very common way of obtaining a very high incremental resistance while keeping the voltage drop across it to a limited value. This is a very common way of simulating very high incremental resistance and the voltage drop across this is not related to resistance value but it is related to (Vgs - Vt) of the transistor, where Vgs is the gate to source voltage of the MOS transistors and Vt is the threshold voltage. So the next structure that can be formed is as below:-

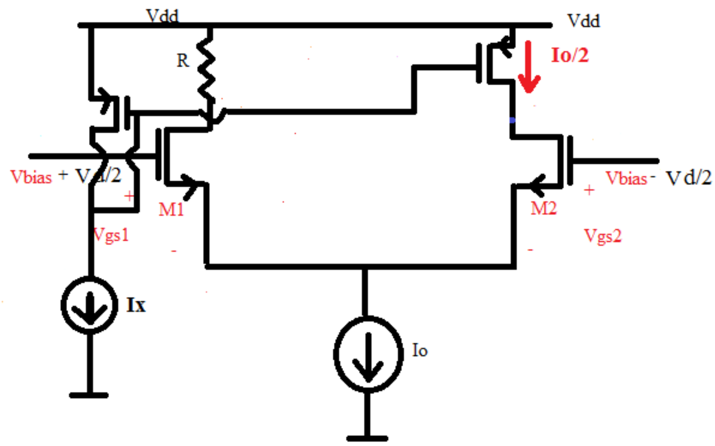


Figure 4.33 New structure to form differential pair to reduce power consumption.

Now the above structure also seems to be wasteful as there is an extra bias branch of Ix. So in order to bring about a corrective to the above design below design is taken up which is known as differential pair with a current mirror load. Below is the design for it:-

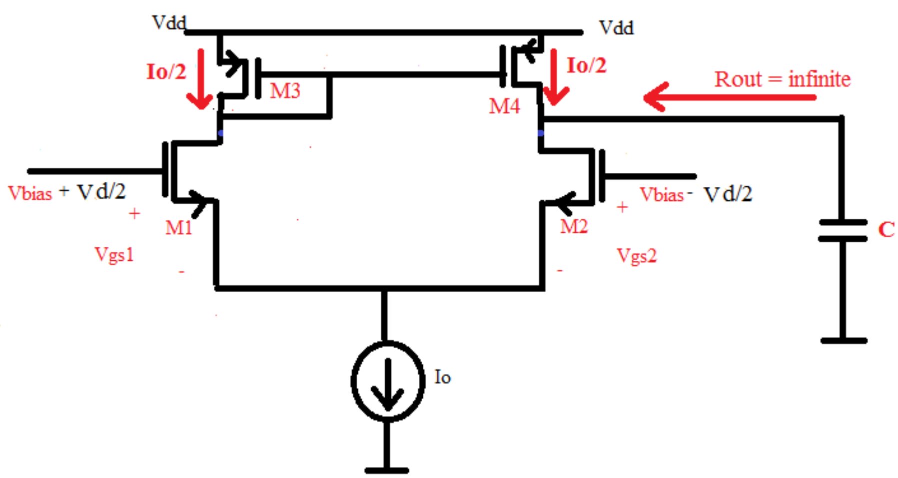


Figure 4.34 Differential pair with current mirror load.

Thus in the above figure, due to symmetry in the quiescent condition the currents in both the branches will be $Io/2$. Thus the currents in the circuit will get mirrored in the current mirror. All transistors are assumed to be in saturation region. If it is assumed that transistors have infinite drain to source resistance Rds then the incremental resistance looking into the differential pair is infinite. As Rds tends to infinite thus Rout tends to infinite. That will be the ideal case of the trans-conductor when the Rout is infinite and the op-amp behaves like an ideal integrator. In reality the transistors will have some Gds and it is needed to analyze the effect of that. But the above topology can be useful because it gives a very high output resistance as high as the value of Rds can possibly be and it converts the input difference voltage into current and drives the output. Now when Rds tends to be infinite, the currents in each transistor are identical and that value is Gm × ($^{Vd}/_{2}$). When Rds doesn't turn out to be infinite, then the analysis becomes a bit critical. The above circuit is non-symmetrical as M3, M4 transistors are not connected symmetrically. Hence the concept of half differential circuit cannot be applied directly.

4.2.2 Analysis of differential pair with active load:-

Below diagram indicates a differential pair with an active load. For the above mentioned analysis, let the below diagram be considered.

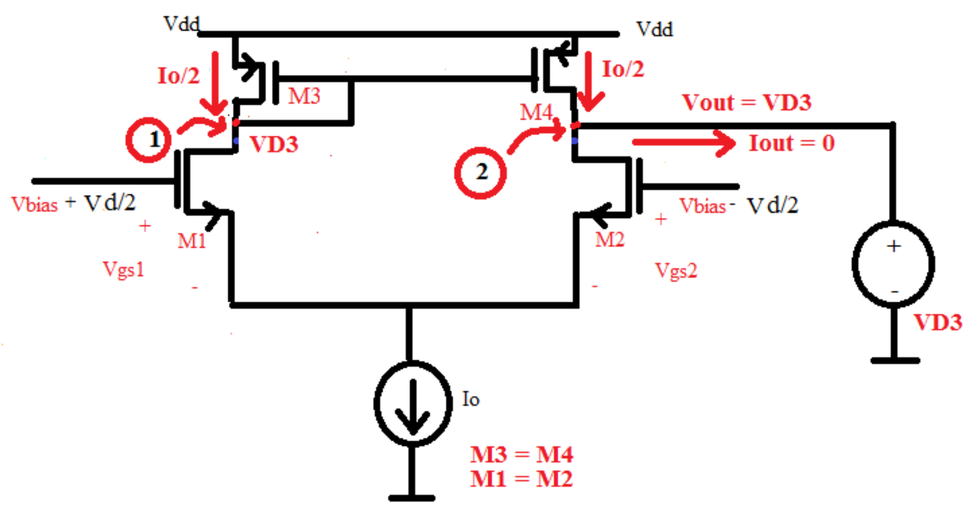


Figure 4.35 Differential pair with active load and with external bias.

First of all, let it be started with quiescent condition i.e. with Vbias only applied to two sides and a tail current Io and the corresponding transistors are exactly identical. In this case mismatch is not assumed but the transistors are perfectly matched. Now let the analysis of output voltage be done. Under quiescent condition Vout at '2' is exactly equal to Vout at '1' as labeled in figure 4.35. So Vout is equal to VD3. The easiest way to prove it, can be explained in the following way. Let it be assumed that Vout at '2' is greater than VD3 at terminal '1'. Under quiescent condition Vgs2 is equal to Vgs1 and Vgs3 is equal to Vgs4. Now if two transistors have same Vgs and if their currents are different, the only reason for them to be different is their Vds are different. Thus at Vout '2' greater than VD3 '1' implies VDS2 is greater than VDS1 which implies IM2 (current through transistor M2) is greater than IM1 (current through transistor M1). For transistors M3 and M4 case same condition applies, i.e. Vsd3 (voltage from source to drain of transistor M3) is greater than Vsd4 (voltage from source to drain of transistor M4) which implies IM1 is greater than IM2. So clearly the above situations are contradictory. So the only solution that happens to be correct is Vout at terminal '2' is equal to VD3 at terminal '1'. This situation means that the above circuit is perfectly symmetrical and transistors are in saturation. Now this implies that if a voltage source is connected at Vout terminal such that its value is VD3 = (Vdd – Vsg3) at a current of Io/2 where Vsg3 at a current Io/2 is (Vt + $\sqrt{\frac{2 \times Io/2}{un \times Cox \times (W/L)}}$). So if a voltage source of value VD3 is connected in the circuit then nothing in the circuit changes and Iout is equal to 0 as the current balance is between M2, M4 and M1, M3 respectively and hence nothing flows into the voltage source. But the output is now incrementally short circuited and this fact would be exploited to do the buffer analysis of the differential pair.

Now analysis would be carried out for the situation when R1 ≠ R2 as shown in the below figure:-

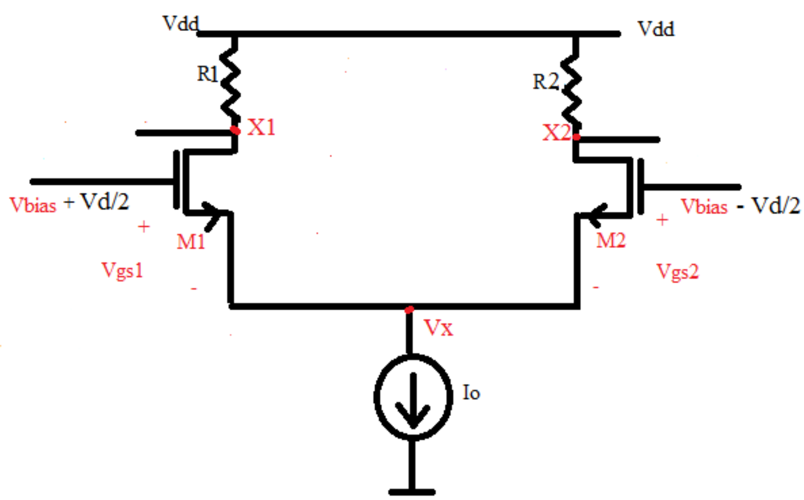


Figure 4.36 Differential pair with varying load resistors R1 and R2.

Remark: Here it is assumed Io to be ideal but in reality it will have some output resistance but to analyze everything with finite resistance at current source is very complicated, it results in complicated expressions without resulting in much insight.

Here it was seen that when common mode input was applied output was not affected if the current source was ideal but it was affected if the current source had some finite output resistance. So for all other analysis the current source would be considered to be ideal. When the resistances were equal the analysis was simplified because it is already known that incrementally the tail node was at zero volts. When the circuit is symmetric with anti-symmetric excitation the tail node is at line of symmetry and its increment is zero and this considerably simplified the analysis as if tail node voltage is zero volts. Then the incremental Vgs across M1 is + $Vd/2$ and that of M2 is – $Vd/2$ and just by inspection the currents and output voltages can be found out. Thus in figure 4.36 with R1 = R2, the output voltage at X1 would be (- Gm × R × $^{Vd}/_{2}$) and at X2 it will be (Gm × R × $^{Vd}/_{2}$). Now if R1 ≠ R2, this is no longer true. So the tail node voltage Vx as shown in above figure is found out first at R1 ≠ R2. Once Vx is known, currents in M1 and M2 can be determined and the expression of output voltage can be written as well.

First let the small signal equivalent of circuit of the circuit be drawn as shown below:-

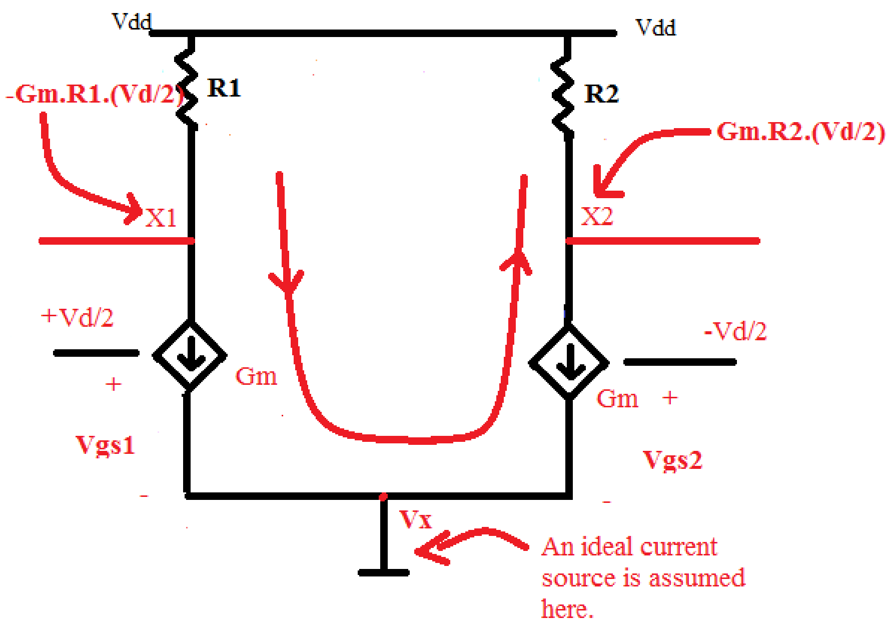


Figure 4.37 Small signal equivalent of differential pair with constant current source with R1 ≠ R2.

The transistors in the above figure are considered without any output resistance and it is also assumed that their Gm are identical. Under this situation let the value of Vx be found out. When nodal analysis is applied at Vx, (Gm × Vgs1) has to be equal to (- Gm × Vgs2), i.e. current in both branches are equal. When (+ $Vd/2$) and (-$Vd/2$) are applied as inputs, then even the circuit is asymmetrical and if Gds1 is 0 (compulsorily) then Vx is equal to 0V. Thus in the above situation the results can be written by inspection alone i.e. Vgs1 = + $Vd/2$ and Vgs2 = - $Vd/2$. So the output voltage at X1 and X2 are (- Gm × R1 × ${}^{Vd}/_{2}$) and (+ Gm × R2 × ${}^{Vd}/_{2}$) respectively.

Now considering the situation when Gds of transistors ≠ 0 (as in reality), mismatch in R1 and R2 exists and anti-symmetric excitations are considered as shown in below figure:-

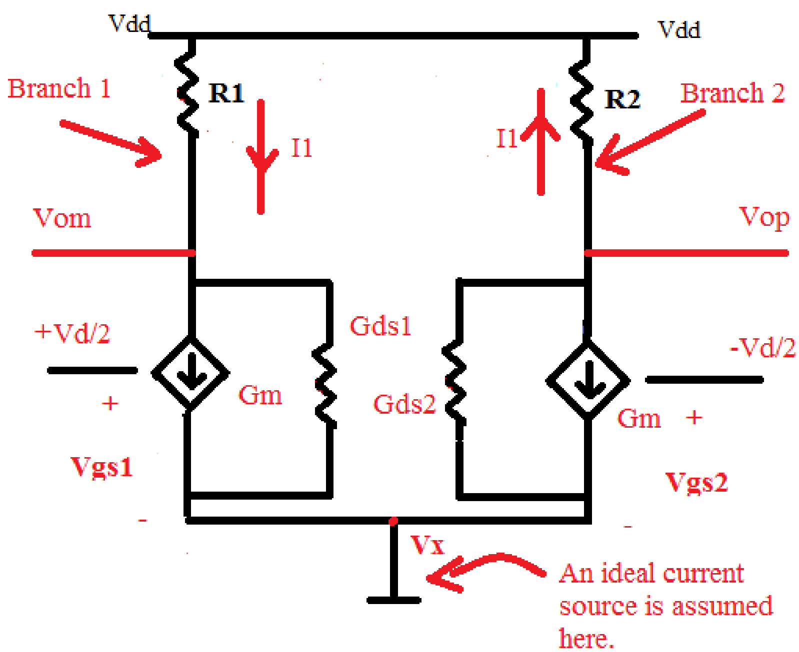


Figure 4.38 Small signal analysis with R1, R2 mismatch, finite Gds (Gds1 = Gds2) and anti-symmetric excitations.

For the above differential system, anti-symmetric excitations are considered. R1 and R2 are considered to be not equal with a finite non-zero Gds. Let the current in branch ‘1’ be I1, now the same current has to flow through branch ’2’ i.e. I1 in the upward direction. Now since the currents in R1 and R2 are I1 in opposite directions, thus

$$- \frac{Vom}{R1} = \frac{Vop}{R2} = \text{I1} \quad (4.7)$$

$$\frac{Vom}{R1} + (\text{Vom - Vx}) \times \text{Gds1} + (\frac{Vd}{2} - Vx) \times \text{Gm1} = 0 \quad (4.8)$$

$$\frac{Vop}{R2} + (\text{Vom - Vx}) \times \text{Gds1} + (-\frac{Vd}{2} - Vx) \times \text{Gm1} = 0 \quad (4.9)$$

Thus it is seen that there are three equations above and three unknowns (Vom, Vop and Vx). The above three equations must be solved to determine the three unknowns and finally the solution of Vx is obtained as below:-

$$\text{Vx} = \frac{Vd}{2} \times \frac{Gm1}{(Gm1+Gds1)} \times \frac{Gds1 \times (R2-R1)}{1+Gds1 \times (R2+R1)}. \quad (4.10)$$

The above is just a solution of linear simultaneous equations. The analysis of the solution is presented as below:-

1. At R1 = R2, Vx = 0 [i.e. if R1 = R2, the voltage at tail node is equal to zero].
2. If Gds1 = 0, the expression also becomes 0.
3. Tail node ≠ 0 if R1 ≠ R2 and Gds1 (a significantly large number). Thus in the expression there is :-
   a) $Vd/2$ [a input applied to each side].
   b) $\frac{Gm1}{Gm1+Gds1}$ (here it is expected that Gm >> Gds) in transistors so that $(\frac{Gm1}{Gm1+Gds1}) \approx 1$.
   c) $\frac{Gds1 \times (R2-R1)}{1+Gds1 \times (R2+R1)}$ here nothing can be concluded as the relative values of Gds1, R1 and R2 are unknown.

Thus from the above it can be concluded:-

- Vx = 0, if R1 = R2 or Gds1 = 0.
- Vx ≈ 0 if │Gds1 × R2│, │Gds1 × R1│ << 1 => Rds1 >> R1 and R2.
  Thus if load resistances are much smaller than output resistances of the transistor then even if the circuit is asymmetrical i.e. (R1 ≠ R2), the value $\frac{Gds1 \times (R2-R1)}{1+Gds1 \times (R2+R1)}$ will be very small because eventually the numerator would be $(^{R2}/_{Rds1}) - (^{R1}/_{Rds1})$. So if each of the values in numerator is small then the difference would also be small.
- Vx ≠ 0, if R1 and R2 are comparable to Rds1. So if R1 is significantly different from R2 and comparable to Rds1, then there is a significant voltage swing at tail node.

The reason for interest in Vx = 0 is, the analysis becomes much simpler. From the above the focus is now shifted to the analysis of differential pair with asymmetrical current mirrored load.

4.2.3 Differential pair with asymmetrical current mirror load:-

Below diagram represents the same:-

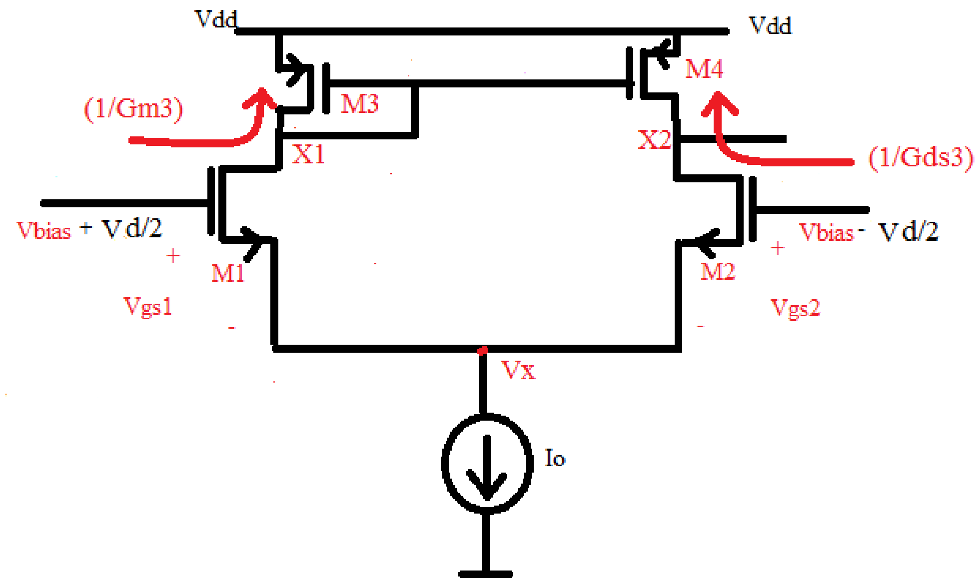


Figure 4.39 Differential pair with varying current mirrored loads.

As the small signal resistance looking up at M3 is $(1/Gm3)$, whereas the small signal resistance looking up into M4 in saturation will be $(1/Gds4)$. Thus $(1/Gds4)$ = $(1/Gds3)$. Thus the loads are $(1/Gm3)$ and $(1/Gds3)$ are very different from each other.

$(1/Gm3)$ << Rds1 but $(1/Gds3)$ not necessarily less than Rds1, it could be of same order or higher. $(1/Gds3)$ = Rds3 ≈ Rds1. Thus in the above circuit clearly Vx (tail node voltage ≠ 0) so it makes quite difficult to analyze and if the Rds of all transistors are put together and then analyzed then it would be very messy and hence no insight can be obtained from the circuit. So instead a trick would be used. From the previous analysis, it was already known that a voltage source could be put at X2 as shown in the above figure, VD3 such that VD3 = Vdd –Vsd3 at a current of $Io/2$. Let that terminating voltage source be called as Vterm. If this is done, nothing would change as voltage at terminal X2 (quiescent output voltage) is equal to Vterm and thus can be connected. Now the change that is brought about due to such a connection is in the value of incremental resistance at output i.e. the parallel combination of what is contributed by M4 and the voltage source and that is obviously zero as it is the output impedance across an ideal voltage source. In this particular case the resistance looking up at M3 is (1/Gm3) and the resistance looking up at M4 is zero and both are much smaller than Rds1 and thus safely it can be assumed that Vx = 0. Hence the voltage source (of certain value was connected at output). Let the below figure be observed for its analysis.

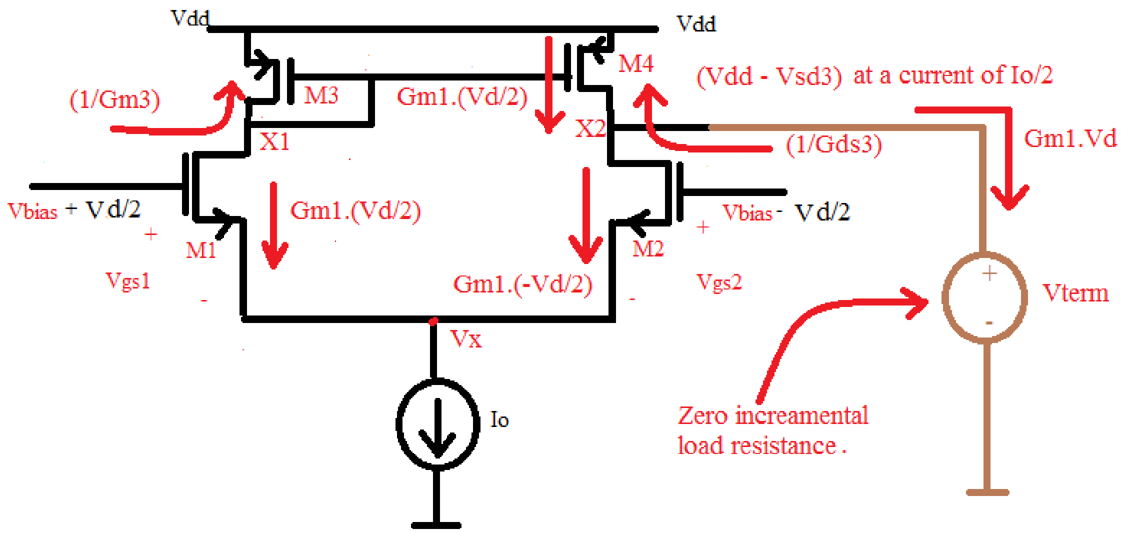


Figure 4.40 Differential pair with varying current mirrored loads showing various values of currents, voltages and resistances at various important nodes.

Now let it be analyzed that how the above feature would be useful. Let's say that it is required to calculate the voltage gain (Gm × Ro). It can be done in different ways. One way is, it can be directly be calculated or alternatively, first the current output is calculated i.e. the output of trans-conductor, i.e. the current that is going towards the voltage source and the output resistance can be calculated separately and the two can be multiplied. This view point is any how useful as the op-amp can be thought as the trans-conductor, i.e. it takes in the input voltage and converts it into a current and passes it through a capacitor. Here the current that is flowing into the voltage source must be computed. For that also, the above viewpoint is useful since if the voltage source is connected to the output and though the circuit is asymmetrical, the two load resistances will be so small that the tail node voltage can safely assumed to be zero. So under the above condition Vx ≈ 0 and thus the analysis becomes very easy. In the quiescent condition Io/2 is flowing in both branches and when an increment Vd/2 is applied, the increment in tail current is almost equal to zero. Thus the incremental current in branch '1' is (Gm1 × $^{Vd}/_{2}$) and that in branch '2' is (- Gm1 × $^{Vd}/_{2}$) i.e. currents in both branches are oppositely directed. Thus the incremental current flows through M3 and comes out of M4. Here the approximation technique is used where M3, M4 is a current mirror, it turns out that it is not a perfect current mirror because of output resistances Rds3 and Rds4 but it is assumed to be a perfect current mirror. So through M4 the current is (Gm1 × Vd/2) in the given direction as in figure 4.40. Thus the total current flowing into the voltage source

Vterm is Gm1 × Vd, where Gm1 is the trans-conductance of M1 or M2 in quiescent condition. The expression of output current is very simple but for that a fact have to be used that Vx is approximately equal to zero. So this differential pair with a current mirror works like a trans-conductor whose trans-conductance Gm is nothing but Gm1 (trans-conductance of transistors M1, M2) which forms the differential pair. Now that the trans-conductance is calculated, the output resistance must also be calculated. It is already known that the DC gain of the op-amp will be the trans-conductance times the output resistance which is a very important quantity as it determines the output error. Now if the transistors didn't have any output resistance it would be an ideal trans-conductor. The DC gain would be infinite. As it is known that this is not the case, so it must be computed. Now for calculating the output resistance at M4, the small signal equivalent of the differential pair must be looked at. The below figure represents the small signal equivalent of the differential pair with a current mirror load.

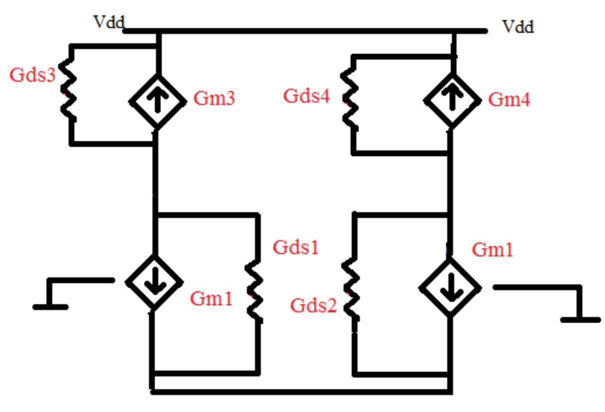


Figure 4.41 Small signal equivalent of a differential pair with a current mirror load.

As the operating pints of M1 and M2 are identical, they will have same trans-conductance and output conductance as in figure 4.41 similarly same thing happens for M3 and M4 respectively. Either an incremental voltage can be applied and incremental current is found out or vice-versa. It is assumed that the given differential amplifier is terminated by Vterm as below and to that an incremental test voltage is applied say Vtest. The below figure is shown below:-

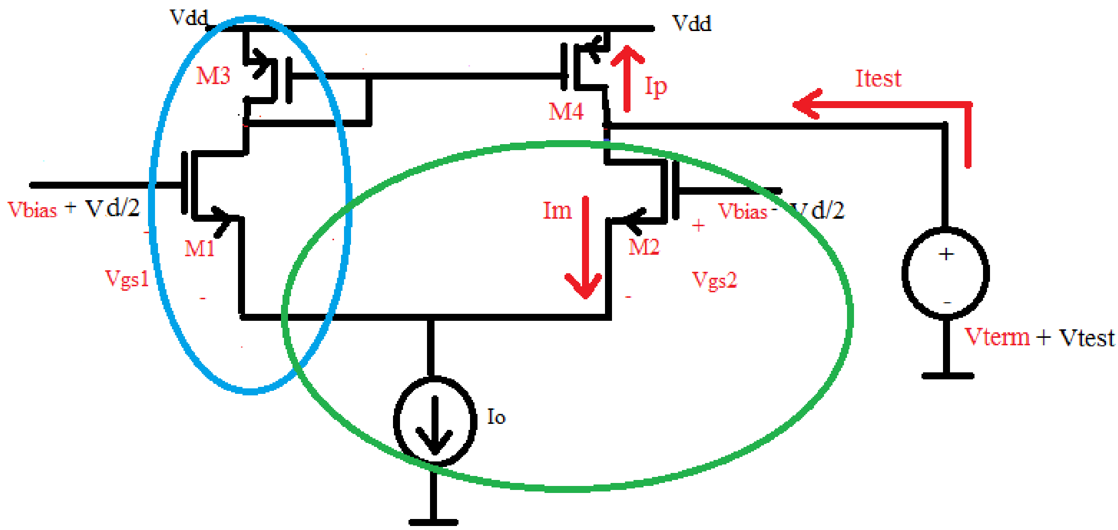


Figure 4.42 Differential Pair with applied Vtest.

Here it is needed to find out the incremental test current Itest. From previous analysis it is known that if Vterm alone is applied then current alone in Itest path is zero. Vtest will give some test current in the circuit. The circuit above is asymmetrical as well as the excitations so none of half differential concepts can be applied. Itest consists of two parts, one of which goes into M2 and other goes into M4. The current values are found separately and they are added to find the output conductance or output resistance. In order to do this, some results from prior knowledge must be used. They are the input and output resistance of source follower or common gate amplifier. So first of all, let that part of the differential pair be considered which is encircled in blue color. The gate of M1 is at fixed voltage and the drain is loaded by a diode connected transistor. Let the below figure be looked at for the analysis of the same:-

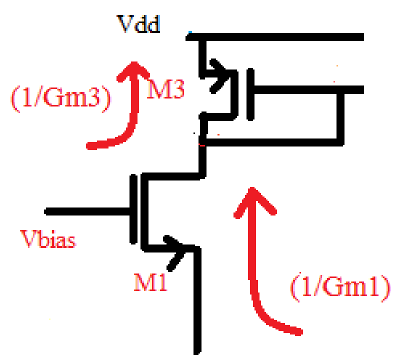


Figure 4.43 Part of the differential pair showing that gate terminal of M1 biased with a fixed voltage and the drain loaded by a diode connected load.

Now M1 can be thought of as a common gate amplifier loaded by a relatively small resistance, i.e. the resistance Rds of M1. The resistance looking in M1 at given arrow mark is approximately (1/Gm1) which is something that is known. The above statement is not unconditionally true, if load resistance increases a lot then (1/Gm1) will also increase. Now as the value of load resistance is relatively small so looking into source of M1, the value of resistance is less i.e. (1/Gm1). So the circuit above has a resistance of (1/Gm1). Now it is important to find out the amount of current that goes up M4 and the amount of current goes to M2. Let them be called as Ip and Im as shown in figure 4.42 i.e. currents going into PMOS and NMOS respectively.

Now to find out Im, it is required to see what the circuit looks like looking down towards M2 as indicated by the encircling green color in figure 4.42. Let the below figure be considered for the analysis of the same:-

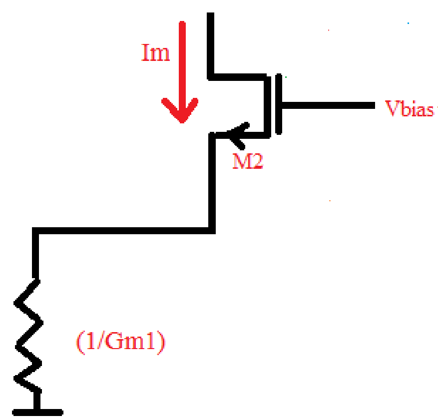


Figure 4.44 Appearance of M2 when it is looked down towards M2.

It appears that M2's source is complicatedly connected, but it is already known from previous analysis that its value is (1/Gm1). Looking into red arrow mark it is seen that the circuit appears as a common gate amplifier. The output resistance of a common gate amplifier will be (Gm1 × Rds1 × Rs + Rds1 +Rs) where Rds1 is the output resistance of the CG amplifier M2 and Rs is the resistance connected to the source of CG transistor as shown in figure 4.44. Now on substituting the terms, the following expression is obtained Gm1 × Rds1 × 1/Gm1 + Rds1 + 1/Gm1. On simplification 2 × Rds1 + (1/Gm1) is obtained, where (1/Gm << Rds). Thus (1/Gm) can safely be neglected, resulting in a value of 2 × Rds1. The complete representation is shown below:-

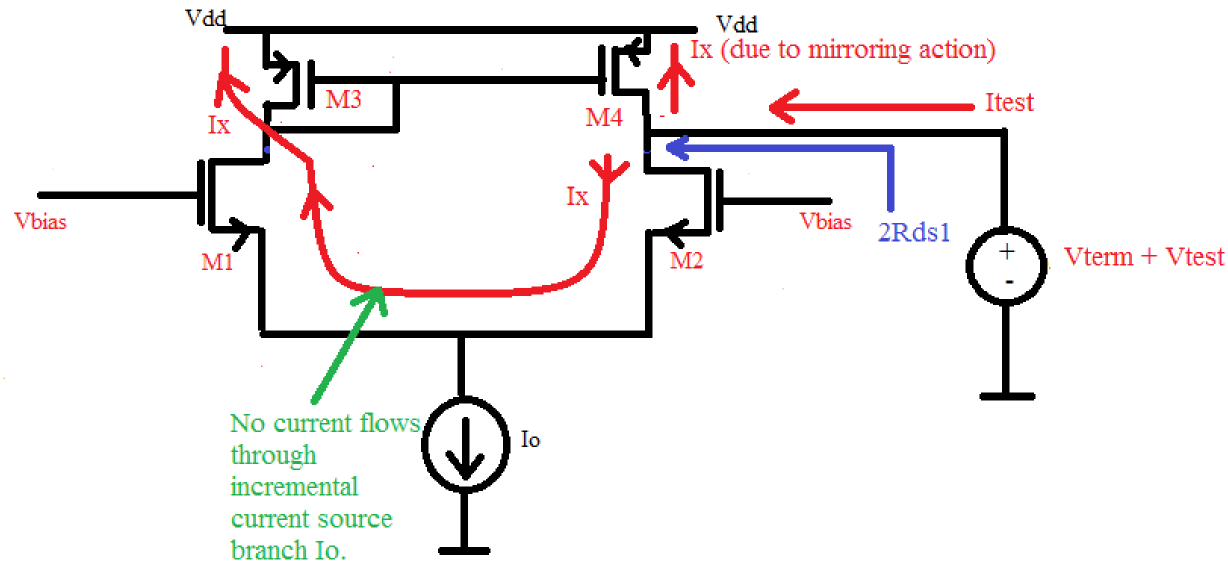


Figure 4.45 Differential pair with current mirror load showing output resistance and current due to mirroring action.

Thus if Vtest is applied at the given location, current that flows in M2 is as below:-

$$\text{Im} = \frac{Vtest}{2 \times Rds1} = \text{Vtest} \times \frac{Gds1}{2} \text{ where Gds1 is the conductance of transistor M1.} \quad (4.11)$$

For determination of Ip as shown in figure 4.42, the increment Vtest is applied at the given location and that appears across output resistance of M4. So, Ip will have a component due to output resistance of M4 (let it be called as Gds3 as a reciprocal of Rds3 of M3 and M3 being equal to M4). So Ip = Vtest × Gds3 + Ix of M4 (as marked in figure 4.45). Thus the final expression of Ip is as below:-

$$\text{Ip} = \text{Vtest} \times \text{Gds3} + \text{Vtest} \times (\text{Gds1}/2). \quad (4.12)$$

$$\text{Itest} = \text{Ip} + \text{In}. \quad (4.13)$$

$$\text{Itest} = \text{Vtest} \times [(\text{Gds3} + \text{Gds1}/2) + \text{Gds1}/2] \quad (4.14)$$

$$\Rightarrow \text{Vtest} \times (\text{Gds1} + \text{Gds3}). \quad (4.15)$$

$$\text{Rout} = \frac{1}{Gds1+Gds3} = (\text{Rds1} \,//\, \text{Rds3}). \quad (4.16)$$

So the differential pair with a current mirror load can be represented by a trans-conductance (Gm) where Gm is the Gm of the NMOS transistor and the output resistance is parallel combination of

PMOS and NMOS transistor. The above situation can be represented by the below figure:-

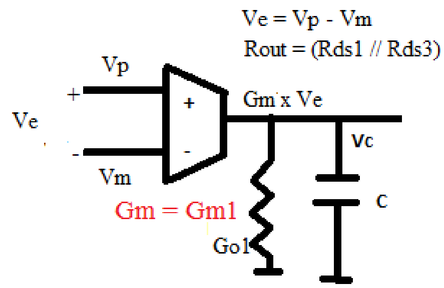


Figure 4.46 Single stage trans-conductor where trans-conductance (Gm) of trans-conductor is equal to the Gm1.

So to above trans-conductor, if a capacitor C is attached as shown in the above figure, the op-amp of unity gain frequency (Gm1/C) and a DC gain of Gm × Rout = Gm1 × (Rds1 // Rds3).

The above is the basic op-amp circuit that works exactly as anticipated. The model is that of a trans-conductance in parallel with an output resistance and the DC gain that is obtained is that of a single transistor i.e. (Gm × Rds) as the DC gain of the whole op-amp. The above is known as the single stage op-amp which is the simplest of all op-amps. Thus the above op-amp can be used in the following way as shown in the below figure:-

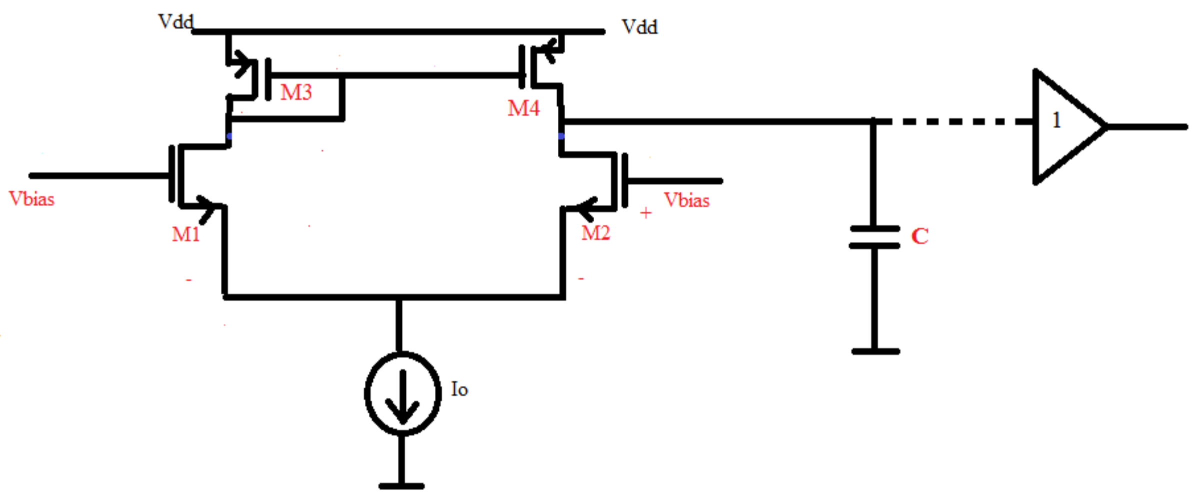


Figure 4.47 Simplest op-amp.

The above figure shows the simplest op-amp which has a unity gain frequency of Gm1/C and its DC gain is Gm1 × (Rds1 // Rds3). The above circuit seems to have 1 pole whose pole location is not at origin but the pole will be at $\frac{Gds1+Gds3}{C}$ in the LHS of the S-plane. The above speculation is not true as none of the parasitic capacitances are included in the op-amp. The parasitic capacitances must be included as it introduces a certain number of poles and zeroes in the system which might affect the stability of the system. Hence all parasitic capacitances must be included and the stability can be judged.

4.2.4 Analysis of parasitic capacitances:-

In general there are parasitic capacitance everywhere in the circuit. The guideline here is Cgd << Cgs so Cgd can be neglected. So now putting the capacitance together as shown in below figure.

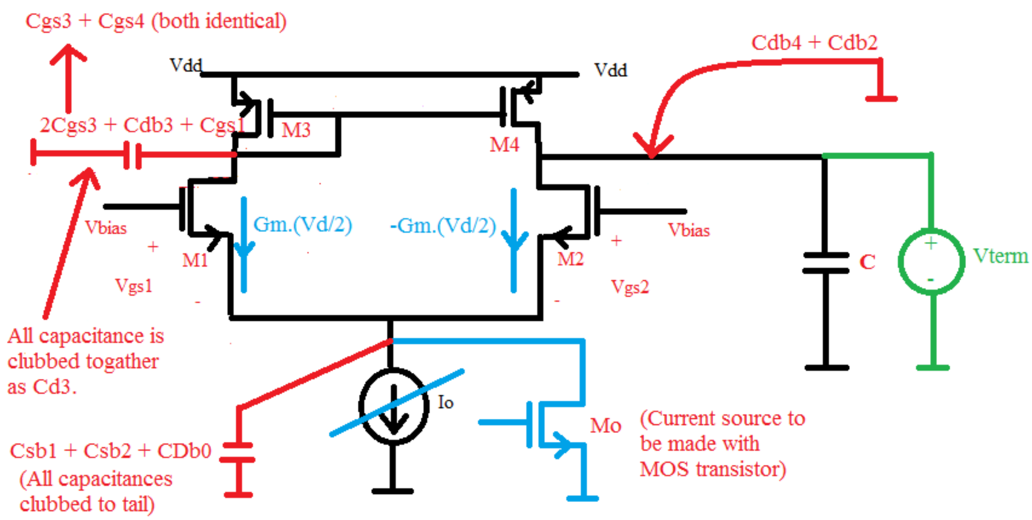


Figure 4.48 Differential pair with all the capacitances shown.

As before the output is terminated with an ideal voltage source, so that a simplified result can be deduced that the voltage at tail node is approximately zero volts. The difference between earlier analysis and now is that earlier the circuit was frequency independent and now the circuit will be frequency dependent. As seen earlier that Vterm = Vdd – Vsd3, so that no output current flows in quiescent condition. Now if (+Vd/2) and (-Vd/2) are applied at both the input sides (at M1 and M2 gates), Vx ≈ 0. If the incremental voltage at tail is zero, the current through parasitic capacitance across M0 transistor is 0. So now analysis would be done for ± Vd/2 by ignoring the flow of current across in parasitic capacitance across M0 transistor. All that is now needed is to find out the effect of Cd3. As Vx = 0, currents in two branch transistors are (± Gm × Vd/2), with (− Gm

× Vd/2) flowing into the voltage source as it presents the short circuit path. So all of this current has to go into the voltage source as the voltage source presents a short circuit. Gm × Vd/2 gets mirrored through M3 to M4, now there is an additional capacitance Cd3 so it must be seen that what happens to it. Finally the current coming out of M4 will get added to the output. Previously all of (Gm × Vd/2) came out from M4 and it got added to output current, now some part of it will go into Cd3 and the remaining part will get added to M4. So now the current mirror is only put as shown in below figure:-

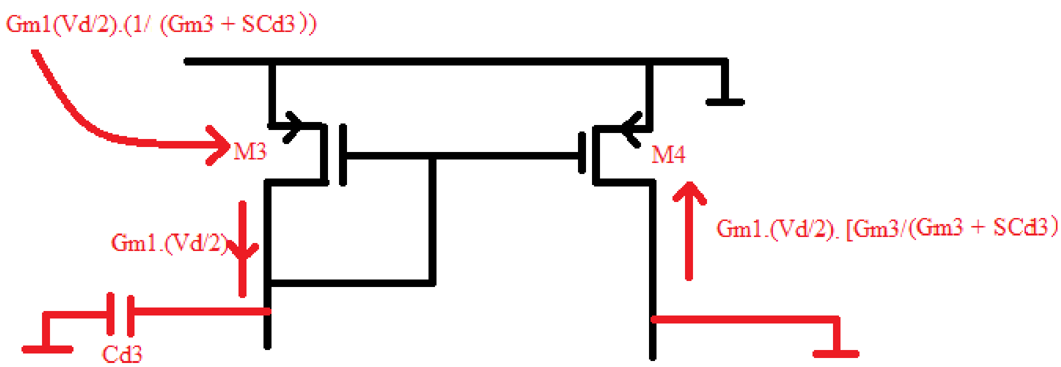


Figure 4.49 Magnitude of currents flowing in the current mirror part under the influence of various capacitances.

The circuit above is terminated by a short circuit as there exists a Vterm on the right hand side. Here Gds3 is neglected as Gds3 << Gm3. Now at DC, the expression Gm1 × (Vd/2) × ($\frac{Gm3}{Gm3+SCd3}$) is Gm1 × (Vd/2) which was assumed during the past analysis. At high frequencies more and more currents from M1 goes into the capacitor, so at a very high frequency, no current is mirrored. Thus the complete circuit of the differential pair is shown below.

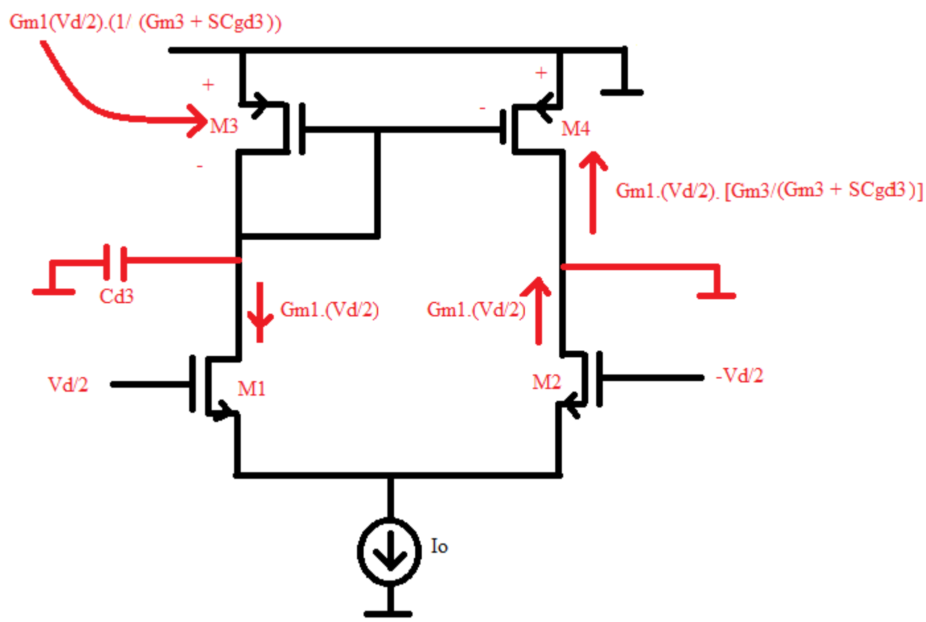


Figure 4.50 Differential pair with all currents at high frequency.

Thus the total current flowing out:-

$$\text{Gm1} \times (\frac{Vd}{2}) \times [\frac{Gm3}{Gm3+SCd3}] + \text{Gm1} \times (\frac{Vd}{2}) \tag{4.17}$$

$$= \text{Gm1} \times (\frac{Vd}{2}) \times (\frac{2Gm3+SCd3}{gm3+SCd3}) \tag{4.18}$$

$$= \text{Gm1} \times \text{Vd} \times [\frac{1+(SCd3/2.Gm3)}{1+(SCd3/Gm3)}] \tag{4.19}$$

It turns out that the trans-conductor of the basic amplifier which is a differential pair with a current mirror load has a pole and a zero. The pole is at (– Gm3/Gd3) on the left hand plane and zero at twice that frequency.

Now there are two paths from input to the output. The output consists of two halves of current, one through M1 and the other through M2 i.e. the drain currents of M1 and M2 gets added up. The drain current of M2 directly goes to the output (unaffected by high frequency). The drain current of M1 goes into a current mirror, but the current mirroring is imperfect at high frequencies because of parasitic capacitance Cd3. Because of this at a high frequency all the current goes into the parasitic capacitances and nothing is mirrored. Only the current in M2 goes to the output and that is very obvious from the expression as well. As in low frequency the trans-conductance is Gm1 and at very high frequency it will be Gm1/2, i.e. the current contributed by M2 only will go to the output. So in the middle somewhere there is a zero and a pole and this will modify the frequency response to some extent and one can see that the pole is at lower frequency than the zero. Thus there is a net phase lag in the overall trans-conductance or trans-admittance. Thus trans-admittance expression is obtained as below:-

$$\text{Ym(S)} = \text{Gm} \times [\frac{1+(SCd3/2.Gm3)}{1+(SCd3/Gm3)}] \tag{4.20}$$

It is already known that the output current from the op-amp goes into the impedance which consists of an output resistance and an integrating capacitance. The output conductance (Go), is Go = Gds3 +Gds1. Thus the transfer function of the op-amp is as below:-

$$\frac{V0}{Vd} = \frac{Ym(S)}{Gds3+Gds1+SC}. \tag{4.21}$$

Thus there is a dominant pole due to the integrating capacitor and there is a non-dominant pole and zero due to current mirroring.

Note: With parasitic pole and so on, the point where magnitude plot crosses the unity gain frequency is not exactly Gm1/C but if it is assumed that parasitic affects happen beyond this as it is usually seen for stability, the unity gain frequency can be assumed to be Gm1/C. For stability, it is best to have the parasitic pole and zero beyond unity gain frequency (assuming that the op-amp is in unity feedback, otherwise the unity loop gain frequency of whatever feedback loop that exists instead of unity gain frequency). The system is unconditionally stable as the phase lag never reaches 180˚.

4.3 Single stage op-amp: Offset

As seen in the differential pair, transistors M1, M2 and M3, M4 must be identical respectively, but there will be a mismatch between them. So appropriate sources are added to the circuit that will represent the mismatch, find the output and from there calculate the offset. Input referred offset is the useful referred offset in the op-amp. It is that input voltage for which the output will be zero. Now as before, while calculating the DC gain and so on, the output voltage was not calculated directly. Instead, the output current going into the voltage source was calculated, multiplied that by whatever impedance connected at output to get the voltage. Similarly here also same approach will be followed as doing this is much easier than calculating the output voltage.

Now here, offsets will not be symmetrically injected into the circuit, the circuit analysis will become very complicated, so during this analysis the extremely small values like that of Gds of transistors are neglected to reduce the complications of the circuit. To simplify the calculations, only the threshold voltage mismatch of the MOS transistors is only considered. Now as seen previously that if the inputs are identical and there is a terminating voltage [Vterm = Vdd – Vsg3], then the current flowing into the voltage source [Vterm] is zero. Now due to mismatches in transistors this current will be non-zero which means that if there is a trans-conductor with offset and if 0 Volt is applied at input there will be some current called the offset current. Below figure represents the same.

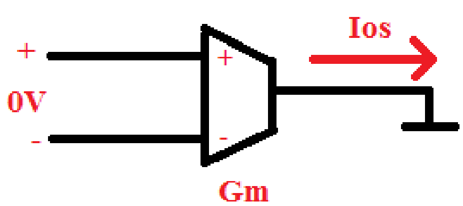


Figure 4.51 (a) Shows the offset current due to the transconductor.

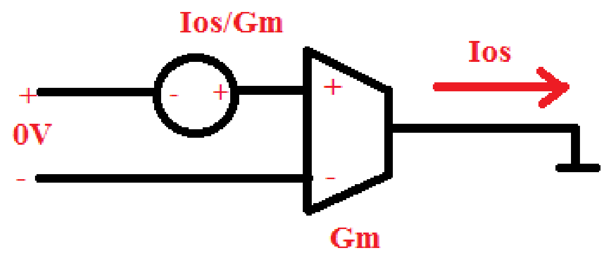


Figure 4.51 (b) Shows the representation of offset at the input due to the transconductor.

Representation of equivalence of figure 4.51 (a) is required which is done in figure 4.51 (b) where the noise of the trans-conductor is represented by $\frac{Ios}{Gm}$ referred at input. So as before at first the output current of the trans-conductor is calculated then divided by the trans-conductance of the circuit gives the input referred offset. So here there will be two mismatches, which are as below:-

- Between M3 and M4.
- Between M1 and M2.

To represent the threshold voltage mismatch between M1 and M2, a voltage source in series is added to the gate terminal as shown below:-

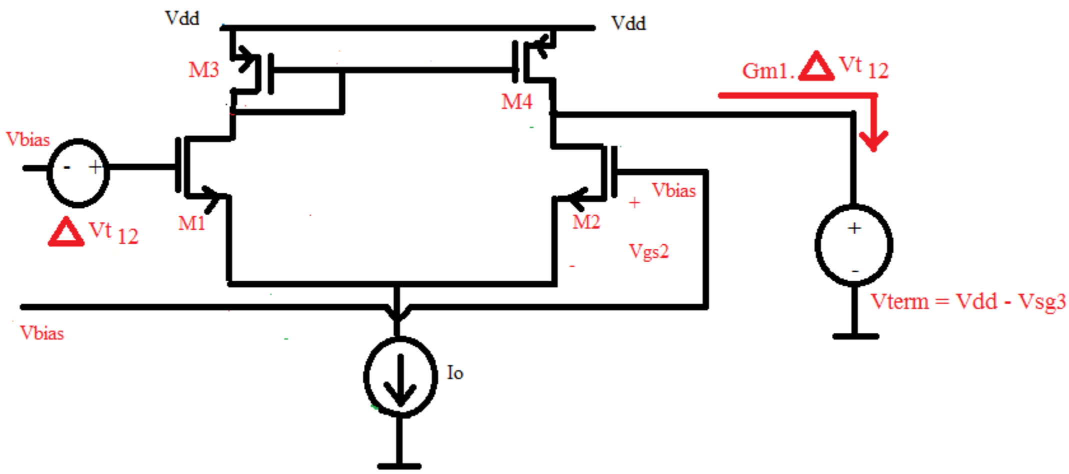


Figure 4.52 Differential pair with a mismatch existing between M1 and M2 represented as a threshold mismatch at the input gate terminal.

Any change in threshold voltage (Vt) can be represented as a change in gate source voltage (Vgs). So the mismatch threshold voltage between M1 and M2 represent equivalently as mismatch in Vgs between M1 and M2. Let it be called as ΔVt_{12}. As with noise the polarity is not important as it is a random quantity, finally the deviation or the variance of this quantity is calculated. Now the analysis of output current due to introduced ΔVt_{12} is done. Now the output current is $Gm1\times \Delta Vt_{12}$. Now this is a very common feature, usually there is some input signal applied to some transistors, any offset due to the input transistors will directly affect the circuit. This is more obvious when the input referred noise is calculated. The offset between M3 and M4 must also have to be calculated. Finally both the effects of noise analysis must be added up together. When the analysis of ΔVt_{34} is carried out, ΔVt_{12} is considered to be zero. Below diagram represents the mismatch between M3 and M4.

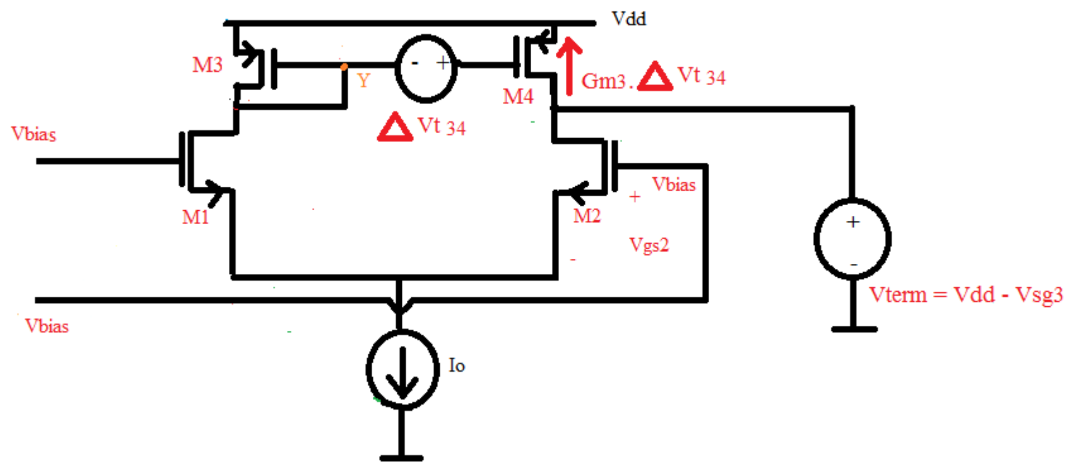


Figure 4.53 Differential pair with a mismatch between M3 and M4.

For the above analysis $\Delta Vt_{12} = 0$ as M1 and M2 are at zero input (apart from Vbias) and it is also assumed that the transistors do not have any Gds so the currents in M1 and M2 will also be 0. Thus the incremental voltage at Y is 0. Thus the small signal Vgs4 = ΔVt_{34}. Thus the incremental current in M4 will be Gm3 × ΔVt_{34} at Gm3 = Gm4 and the current will go into the terminating voltage. Thus the total output current due to source noise is Gm1 × ΔVt_{12} - Gm3 × ΔVt_{34}. The negative sign is only because of the way the polarity is chosen and it does not have any significance. Both the mismatches are put in order to obtain the value of current that is to be obtained at the output. Hence the offset current Ios is Gm1 × ΔVt_{12} - Gm3 × ΔVt_{34}. If this offset voltage is required to be referred to as the input referred offset voltage which is equivalent to $Ios/Gm1$.

$$Vos = \Delta Vt_{12} - \frac{Gm3}{Gm1} \times \Delta Vt_{34}. \quad (4.22)$$

This is meant by offset of input differential pair that appears directly as input offset. Thus the mean square value of offset or standard deviation of offset represented as 'σ' is as below:-

$$\sigma\, Vos^2 = \sigma\, \Delta Vt_{12}^2 - \left(\frac{Gm3}{Gm1}\right)^2 \times \sigma\, \Delta Vt_{34}^2. \quad (4.23)$$

$$\sigma\, Vos = \sqrt{\sigma\, \Delta Vt_{12}^2 - \left(\frac{Gm3}{Gm1}\right)^2 \times \sigma\, \Delta Vt_{34}^2}. \quad (4.24)$$

The effect of M1 and M2 simply cannot be avoided and the effect of M3 and M4 i.e. the offset between them is multiplied by the ratio ($Gm3/Gm1$). Now if the value of Gm3 is small and that of Gm1 is large then on dividing Gm3 by Gm1 the value will become negligible. Now the way to think about this is, that the input transistors M1, M2 convert the input voltage to a current. The load transistors M3 and M4 will add an offset current of their own which is proportional to Gm3 × ΔV_{t34}. When referred to the input that will get divided by Gm1. So if the offset current of the load devices is made small and is added to large values of trans-conductance of the input device then the effective offset due to load at the input will be small. So there is a room to reduce the offset of load but as far as the offset of the input is concerned, nothing can be done about it as it appears directly at the input. The only way to reduce that is to increase the area of the device. So by making the input devices bigger and bigger the offset can be reduced. And if it is desired to make the overall offset small, the input devices must be made as large as possible and the load devices as small as possible.

4.4 Single stage op-amp: Noise.

So while calculating the noise of the entire op-amp, the noise contributed by each transistor must be added. The transfer function from every noise source to the output is evaluated and finally all of them are added up in an uncorrelated way to get the output noise spectral density divided that by $Gm1^2$ to get the input noise spectral noise density. Thus both the noise sources from current source transistors and the current mirror are added. Below diagram represents the single stage differential op-amp.

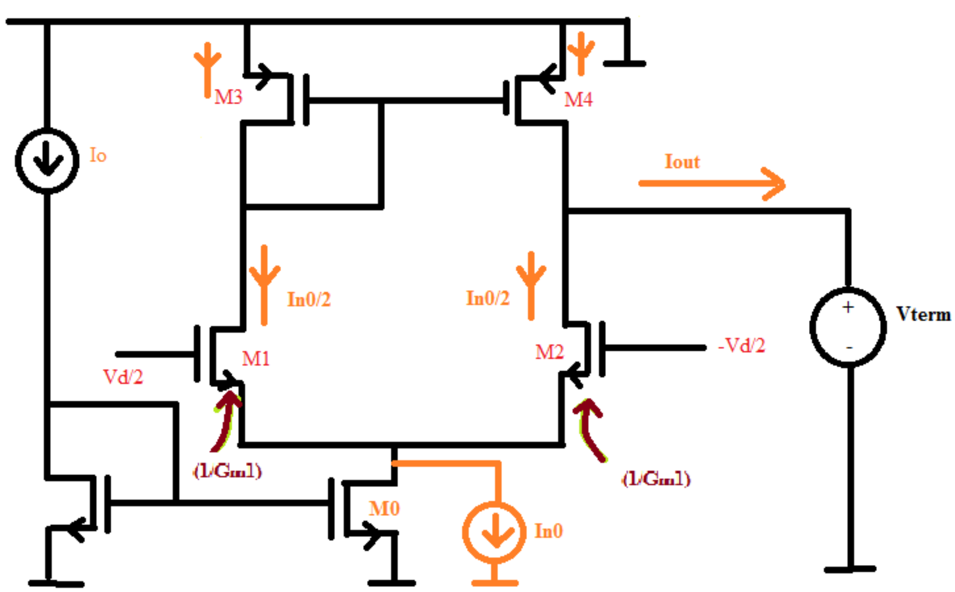


Figure 4.54 Single stage op-amp showing the noise currents in the branches.

Under quiescent condition of course Iout = 0. Let a current Ino [i.e. due to Mo] is added. If there is a current Ino due to Mo, there would be an incremental current in both M1 and M2. Now let it be analyzed that how much that current would be. The impedance looking up at M1 is $(1/Gm1)$ as the drain is relatively loaded by a low resistance, the impedance looking up in M2 is also $(1/Gm1)$ as its drain is loaded by a short circuit which is also a small resistance. So the current due to Mo, divides equally among M1 and M2 hence there is a current of Ino/2 flowing through both transistors M1 and M2 respectively. Thus Iout due to noise current in Mo is zero as [through M4 and M2 the value is 0]. Now this is a general result, if some current is injected in common-mode node [tail node of an op-amp], the effect will be zero as the current will symmetrically get divided between M1 and M2 and mirrored in M3 and M4 and net effect will be zero. So the noise of current source transistor will not appear at the output of op-amp. Let the design in figure 4.54 be reconsidered once again and let the noise due to M3 and M4 be calculated for that let the below diagram be considered.

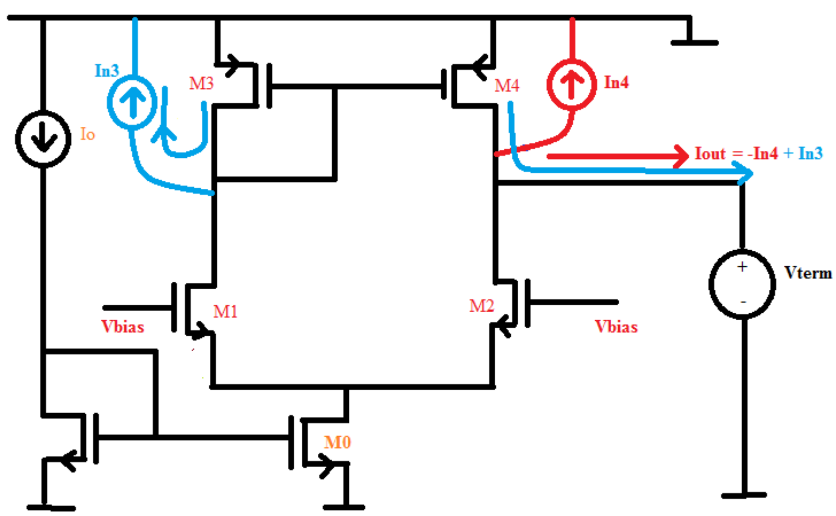


Figure 4.55 Single stage op-amp showing noise currents due to M3 and M4.

In4 represents noise due to M4 and in small signal it is grounded as it is connected to Vterm, which is zero in small signal analysis as it is a constant source. So all of the current from current source In4 simply goes to the ground. So the effect of noise current due to M4 i.e. I4 appears at Iout. With the polarity that is chosen, it happens to be –In4. If the noise current due to M3 is looked at, the impedance due to M1 is infinite and the Gds of M1 is zero. So the current In3 is simply drawn out of transistor M3. Now M3 and M4 form a current mirror so the same current appear at M4 and the same current goes into terminating voltage source (Vterm) as that has zero impedance. So In3 also appears directly at output. Now the noise currents due to M1 and M2 must be calculated. Let the noise current in M1 be calculated. For the above analysis let the below figure be considered.

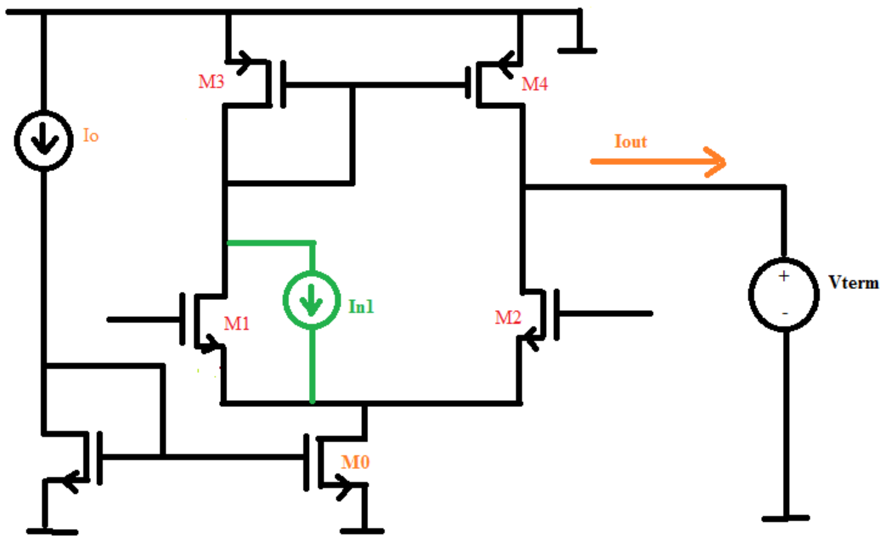


Figure 4.56 Single stage op-amp showing the noise source due to transistor M1.

Now the earlier noise had one of the terminals grounded, here the noise is connected between drain and source of M1, so the analysis can be bit more calculated. But there is also a neat trick that makes the analysis very easy. In any circuit, let's say there is a current source between A and B. It can be replaced by a series combination of two current sources of exactly the same value as shown in the below figure.

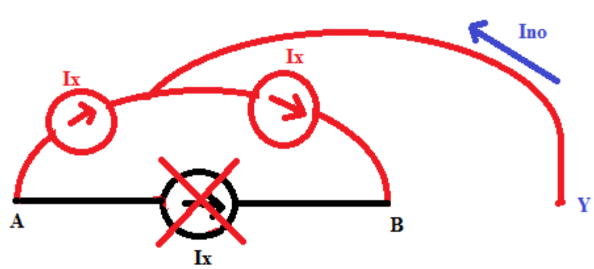


Figure 4.57 A current source being replaced by a series combination of two current sources of exactly same value.

In the above figure KCL is satisfied and nothing changes in the nodes A and B. Now if the in between node is taken and is joined to some other node again as shown in above figure it will not affect the circuit because Ix near points A and B are identical and the current flowing from Y will be zero. So in the above figure due to the external connection from any arbitrary point Y neither affects KCL nor the circuit. Now this is a very convenient thing when the analysis with floating current sources i.e. current sources connected between two nodes and neither of it is grounded. Such a situation in many cases would simplify things. In above situation the most important thing is that the two current sources must be identical. The representation of the above scenario is seen in the figure below:-

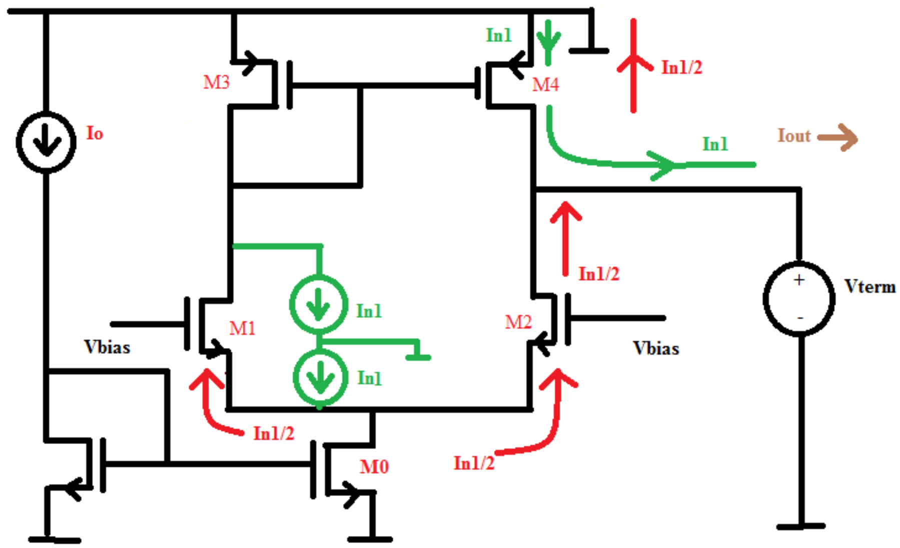


Figure 4.58 Representation of a single noise source of amplifier in figure 4.56 with two identical noise sources for its analysis.

The middle of two noise sources as shown in the above figure is connected to the ground and the analysis of the two sources are carried out separately. No further analysis is required as the analysis of upper In1 of the two sources of In1 is similar to that what was done for M3 in figure 4.55. The lower In1 is similar to the analysis of In0. Due to In1, all of it will flow through M3 and get mirrored through M4. Due to lower In1, it will split into In1/2 towards M1 and M2 respectively exactly as discussed for noise of M0 and whatever goes through M1 also goes through M3 and gets mirrored in M4. Thus there is a net current of In1/2 in M4 and a net current of In1/2 in M2. Thus the total current coming out as Iout is In1. Hence the noise current of In1 appears at output. Now in a similar way noise of M2 can be analyzed and it turns out that exactly the same thing happens and all the noise of M2 exactly appears at the output. Thus the output current will be the sum of all the device currents which is as given below:-

$$Iout = In1 - In2 + In3 - In4. \quad (4.25)$$

The tail device does not contribute anything. It will contribute equal currents at the two halves and the currents get cancelled out. Thus the total noise spectral density (Siout) which happens to be the sum of all spectral densities (Sin1, 2, 3, 4) which are related to each other as below:-

$$Siout = Sin1 + Sin2 + Sin3 + Sin4. \quad (4.26)$$

$$\frac{8}{3} KT\ (Gm1 + Gm1 + Gm3 + Gm3). \quad (4.27)$$

$$\frac{16}{3} KT\ (Gm1 + Gm3). \quad (4.28)$$

Where Gm1 is proportional to both of M1 and M2 and Gm2 is proportional to both of M3 and M4.

$$Svin = \frac{Siout}{Gm1^2} = \frac{16}{3} KT \times \left(\frac{1}{Gm1} + \frac{Gm3}{Gm1^2}\right) = \frac{16}{3} \frac{KT}{Gm1} \times \left(1 + \frac{Gm3}{Gm1}\right) \quad (4.29)$$

The expression $Svin = \frac{Siout}{Gm1^2}$ comes up from the past analysis where an output current was represented by an equivalent input voltage as ${Iout}/{Gm1}$.

So the above expression numbered as (4.29) is that for input voltage noise spectral density. The frequency dependencies and so on are ignored as it is not so important with noise and it leads to messy and cumbersome expressions. If it is desired to calculate the frequency dependency of input and output noise spectral density, a simulator is used. But the above expression is good for wide variety of calculations to estimate the noise. By this the noise analysis of a single stage op-amp comes to an end.

4.4.1 Analysis of optimization of offset, noise reduction:-

Offset related to mismatch in input differential pair and load expressed as $\sigma Vos^2 = \sigma \Delta Vt_{12}^2 - (\frac{Gm3}{Gm1})^2 \times \sigma \Delta Vt_{34}^2$ can be reduced by increasing the size of the transistor. Contribution from M34 mismatch can be reduced by reducing Gm3. Now let's say that Gm3 is desired to reduce alone and Gm1 is not desired to make it affected (in fact the differential pair is not desired to make it affected) i.e. the tail current and the differential pair is kept as it was before. The only way to do that was to increase VDSAT3, as Gm3 = $\frac{2 \times {}^{I0}/_{2}}{VDSAT3}$ where VDSAT3 is the saturation voltage of the transistor M3. Increase in VDSAT3 means that it will reduce the swing limit. So this is a very common trade-off that is seen. Some parameters are required to improve and it ends up adversely affecting some other parameter. To reduce the total offset, the size of all transistors must be increased. So to reduce the offset voltage by a factor of 2, the area of all transistors must be reduced by 4. The bad consequence of this is, the value of parasitic capacitances increases. This results in movement of non-dominant pole and zero towards the unity gain frequency and this reduces the speed of op-amp, and the stability. To maintain the stability to same value the unity gain frequency must be reduced. If there is a larger delay in the system, then only way to stabilize it, is to slow down the integrator. Again if it is desired to optimize the offset, the op-amp becomes slower. Thus it is needed to iterate many times to arrive at the final design.

Now let the noise that was calculated earlier be looked at. It was thermal noise. Input referred noise that was calculated earlier was $\frac{16}{3}\frac{KT}{Gm1} \times (1 + \frac{Gm3}{Gm1})$. The loads' contribution to noise can be reduced only by reducing Gm3 (noise scaling or impedance scaling), which can be done by increasing the VDSAT3 of those transistors. But if it is done so, then it adversely affects swing limits. Now if the noise is reduced by increasing Gm1 of the involved transistors, then it ends up with a larger power dissipation i.e. with the doubling of the widths of all transistors in the circuit, the currents everywhere will double and trans-conductance will double and the input noise spectral density will go down but this will increase the power dissipation. The above explanations can be explained in the following way:-

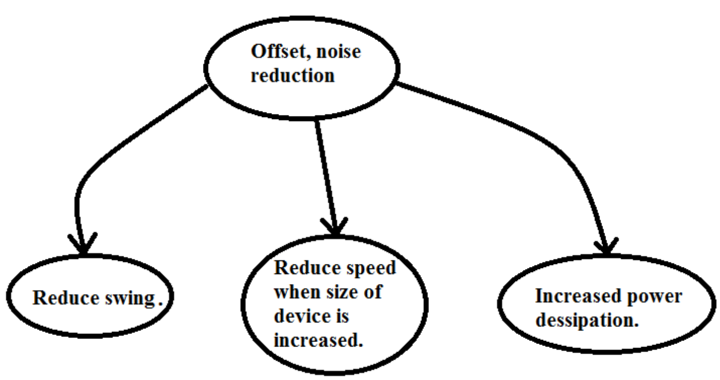


Figure 4.59 Effect of offset and noise reduction.

4.5 Slew rate:-

One more important that must be looked at is the slew rate of the op-amp. It is the maximum rate of change of output which can be illustrated by the below circuit. Let it be imagined that the circuit has reached steady state with Vbias at input and Vbias at output as shown below:-

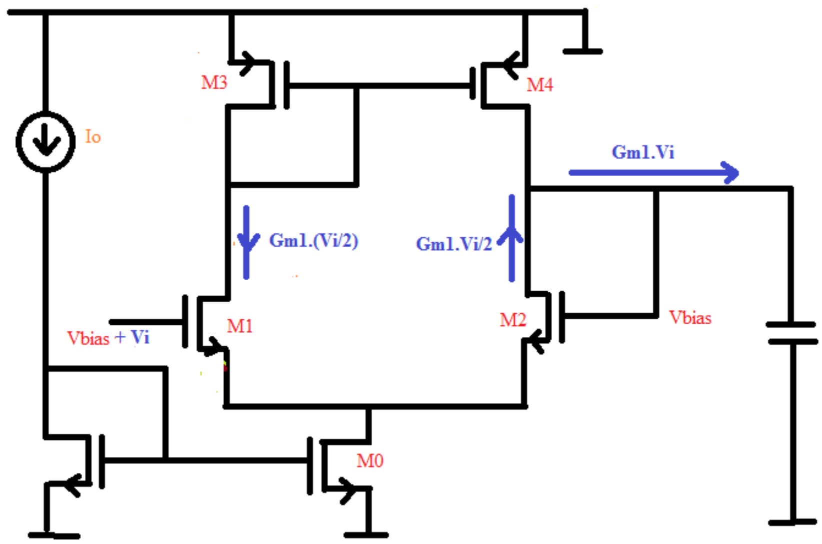


Figure 4.60 Obtaining the slew rate of the op-amp.

Let a small step input (Vi) be applied to the input. As soon as the input step is applied the current in M1 is increased by Gm1 × $(\frac{Vi}{2})$. The capacitor still holds the initial voltage so the output voltage does not change. It is like applying the step Vi to the differential pair or a step current of Gm1 × $(\frac{Vi}{2})$ in transistor M1 and Gm1 × $(\frac{Vi}{2})$ in other transistor in opposite direction. So a total current of Gm1 × Vi flows into the capacitor. So at the output, it will start rising at Gm1 × $(\frac{Vi}{C})$. This is exactly what is expected from the op-amp. If there is an op-amp with an unity gain frequency ωu and if a unit step input is applied to it, the slope of the output of the op-amp would be ωu. If a step of Vi input is applied to it, the slope of the output of the op-amp would be ωu × Vi. Let's say if the magnitude of Vi is kept on increasing, i.e. the steps that are applied are larger and larger then the currents in transistors also goes on increasing but with opposite signs. Soon a stage will be reached when the input step will become greater than saturation voltage of the differential pair which is nothing but the overdrive voltage required by M1 to carry current Io. There is some voltage beyond which all of Io flows through M1 and nothing flows through M2. So the current through the capacitor is Io as is flowing in M1, which will be mirrored in M4 and then finally flow into the capacitor. So there is a maximum change of output of + Io/C when a positive step is applied. In this particular circuit, when a negative step is applied, current in M1 will reduce and again if a large negative step is applied current in M1 will reduce and eventually it becomes zero and current in M2 will become Io and that will be drawn out of the capacitor. So the maximum rate of change in negative direction will also the same value. It will be - Io/C. But practically the slew rates on the positive and negative sides are different.

4.6 Increasing DC gain:-

The DC gain of single stage differential amplifier with current mirror load is limited. A way to increase the DC gain is to reduce the output conductance or increase the output resistance. The way to increase the output resistance, is by using a current buffer or a common gate amplifier after that. To increase the output conductance contributed by each of differential pair and the current mirror load, current buffers can be used with each of them as both of them are nothing but current sources.

Let the below transistor be looked at, from the direction as shown with arrow mark and let it be biased with some voltage Vgs1 and let it be called as M1.

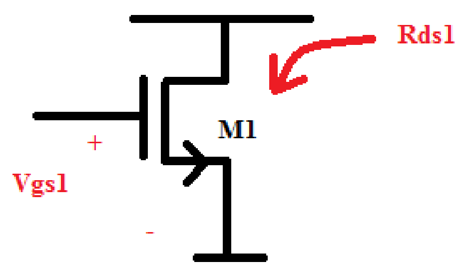


Figure 4.61 Transistor with bias Vgs1 and output resistance Rds1.

As with the direction given for the above transistor, the output resistance is Rds1 or a conductance of Gds1. Let a common gate amplifier is applied on the top of it and then its output resistance is observed as shown in the below figure:-

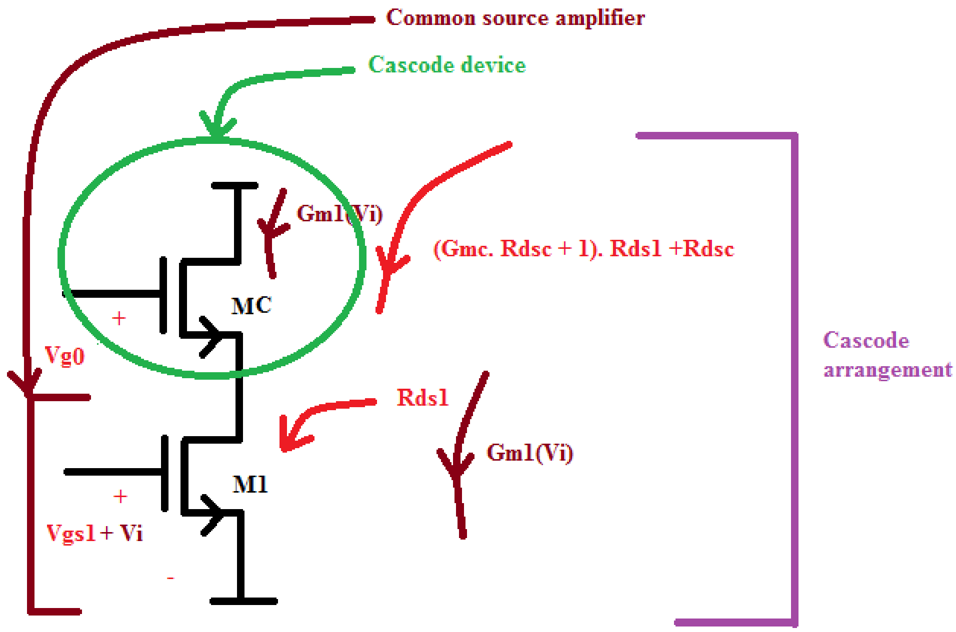


Figure 4.62 Shows a CG amplifier cascoded with a CS amplifier to increase the overall output impedance.

In the above figure, if a voltage source Vi is applied in the mentioned location, it would give a current of Gm1 × Vi. The same current appears when the circuit is looked from above the cascode structure but the output impedance while looking from the same location appears to be (Gmc × Rdsc + 1) × Rds1 +Rdsc i.e. sum of both the output impedances where Gmc is the trans-conductance of transistor Mc and Rdsc is the output impedance of the transistor MC. Thus the dominant contributor to the output resistance is (Gmc × Rdsc × Rds1) and that increases the output resistance to the considerable extent. Thus the above is a very common technique to increase the output impedance of current sources. The upper transistor is called the cascode device and the total arrangement is called cascode arrangement. The lower transistor is shown to be a common source amplifier in the above figure but it need not be so. This design procedure can be used for both the differential pair and the current mirror to design the op-amp which has much higher gain. Now the advantage with this is, the magnitude of output resistance can be increased drastically without increasing the length of transistors. Increasing transistor length would slow down the circuit whereas this does not appreciably change the circuit. Now these cascodes can widely be used in integrated circuits. Let it be started with a current mirror which can be used as a current source. If there is a current source Io, the output current nominally is also Io in the other branch as shown in the figure below:-

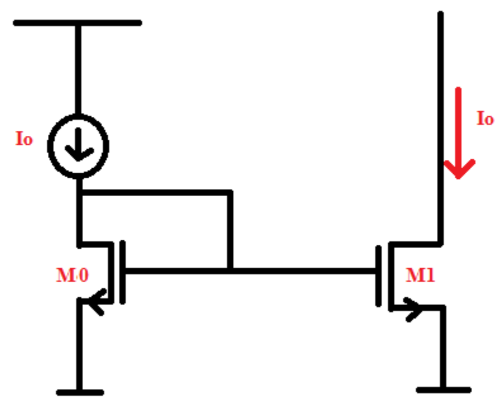


Figure 4.63 Current mirror.

Now let the above shown current be terminated by a voltage source as shown in the figure below:-

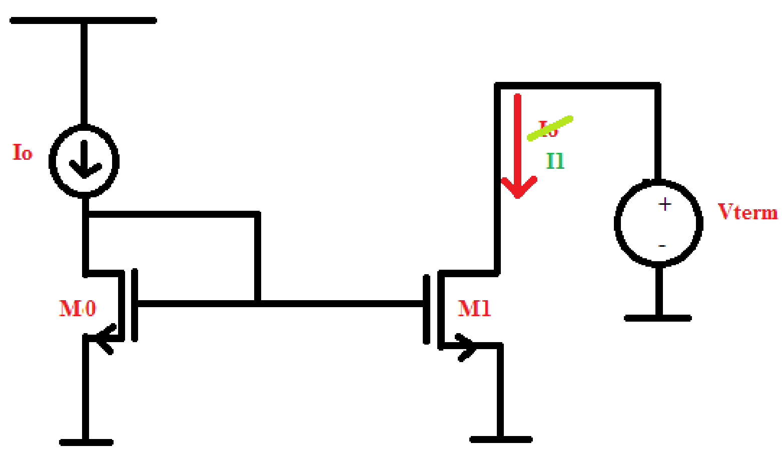


Figure 4.64 Output of a current mirror ending with a voltage source.

In the above circuit shown the output current Io also get influenced by drain source voltage of the transistors M0 and M1 as they could be different and the current I1 becomes equal to as below:-

$$I1 = Io \times \left(\frac{1+ \lambda Vds1}{1+ \lambda Vds0}\right) \quad (4.31)$$

In the above equation λ is the channel length modulation factor of the transistor and Vds is its drain to source voltage. It is also seen that Vds1 is equal to Vterm in above figure so I1 = Io × $\left(\frac{1+ \lambda Vterm}{1+ \lambda Vds0}\right)$. Thus if the terminating voltage changes, the current I1 also changes as well. Now this situation is undesirable, if the output is desired to be closer to ideal current source, the current source must have a higher output incremental output resistance. In-fact the current source must be ideally infinite. This can be done by placing a common gate structure on top of it as shown in the below figure.

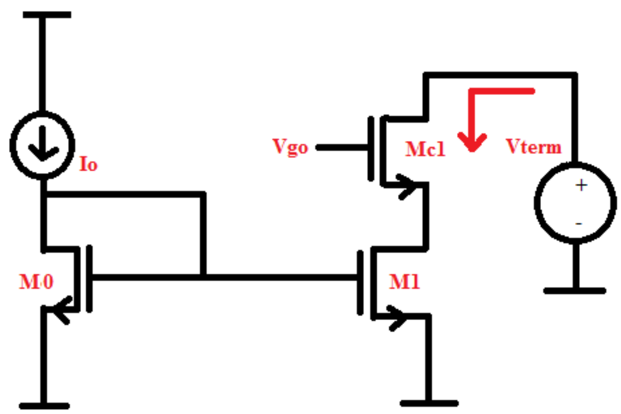


Figure 4.65 Increasing output impedance of a current mirror by placing a common gate structure on top of it.

Now the output current will not be significantly affected by Vterm. So the above is a better current source but uncertainty still exists as the current I1 is still related to Vds of M1 and M0. The above is a better current source as I1 is not significantly by Vterm but it is not equal to I0. To obtain an equivalence of I1 and I0, Vds of M1 and that of M0 must be equal. Then the two currents would be exactly equal. This can be achieved in the below mentioned way:-

In a diode connected arrangement, the current Id is subtracted from desired current Io and applying negative feedback to the transistor as shown in the below circuit.

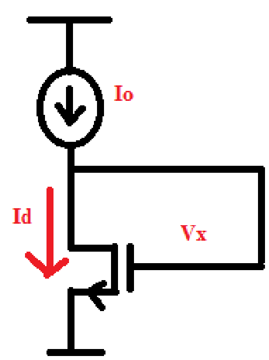


Figure 4.66 Diode connected load.

If the voltage at node Vx increases, the current Id increases and that tends to lower Vx and finally the circuit reaches equilibrium when Id becomes exactly equal to Io. Now let a cascode transistor is put on top of it as shown in the below figure:-

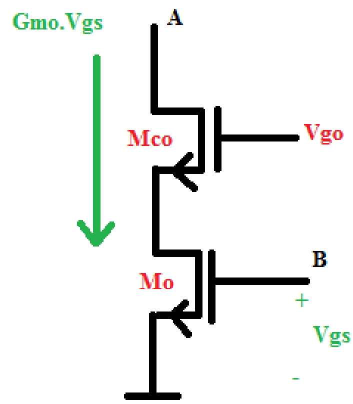


Figure 4.67 Cascoded structure to illustrate high gain.

If the behavior between points A and B is looked at to find its response to incremental Vgs as shown in above figure it is seen that there will be an increment Gm0 × Vgs as was obtained in case of figure 4.62. The only difference is Mc0 transistor will improve the output impedance of the above circuit. The same circuit can be used in a feedback network as shown below and the previous given analysis of high gain and negative feedback of diode connected arrangement can be applied to it. The negative feedback concept actually improves the swing limits of the amplifier.

4.7 High swing generation:-

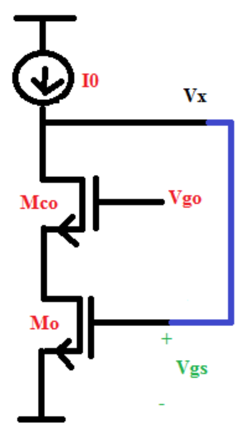


Figure 4.68 Cascode structure with negetive feedback.

Thus the complete circuit in a differential pair is as below which is known as high swing cascode current mirror:-

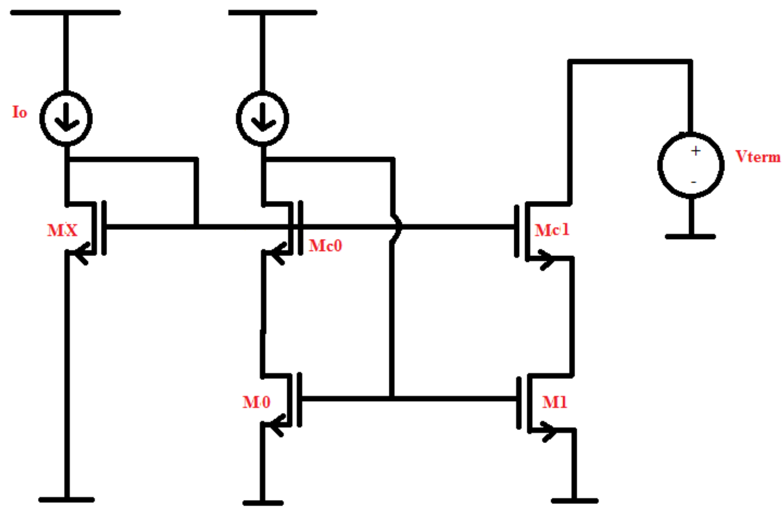


Figure 4.69 Schematic of high swing cascode current mirror.

An alternative biasing scheme for the above design so as to reduce the number of constant current sources is shown below. It also works on the concept of high gain and high swing.

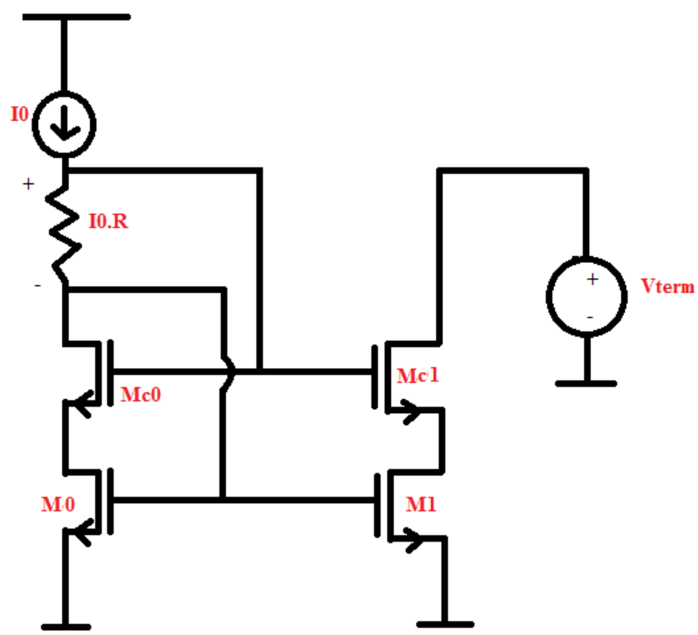


Figure 4.70 High swing cascode current mirror with a reduced number of constant current sources.

By the above discussion almost the entire analysis of a differential pair structure is covered. The reason for discussing the differential pair in such a great detail as the concepts that are discussed about the differential pair in transistor level can be applied to analysis of any higher level of op-amp structure. The basic idea of analysis of higher level of op-amps is already presented in chapter 3 at block level. Moreover the design procedure pertaining to higher level op-amps at the transistor level and their large signal analysis i.e. their biasing scheme are discussed in the upcoming chapter namely design procedure of operational amplifiers.

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CHAPTER 5

DESIGN PROCEDURE OF OPERATIONAL AMPLIFIERS.

Before going directly into the topic two important ideas are required to be presented. They are as follows:-

- Fundamentals of Ideal Fully Differential Op-Amp.
- Basic architecture of Two Stage Op-amp.

5.1 Fundamentals of Ideal Fully Differential Op-Amp.

There are two input signals in an op-amp Vi1 and Vi2, and two output signals, Vo1 and Vo2 as shown in figure 5.1. On both the input and output side of the system, the signal of interest happens to be the difference between them respectively. The respective difference between the input side and the output side are called differential mode input and differential-mode output, or V_{iDM} and VoDM. If the system is balanced with balanced inputs, the input and output signals can be called as common mode, or average voltage, ViCM and VoCM, respectively as shown in figure 5.2. If the common mode voltage is set to analog ground then the following relation holds: V1 = -V2.

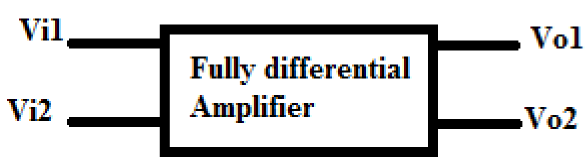

Figure 5.1 Fully differential op-amp with input and output terminals shown.

There are 4 gain parameters of interest. Differential mode gain A_{DD} relates the differential output signal, Vo_{DM}, and the differential input signal, Vi_{DM}.

$$V_{i1} = Vicm + \frac{1}{2}Vidm \qquad V_{i2} = Vicm - \frac{1}{2}Vidm \tag{5.1}$$

$$V_{o1} = Vocm + \frac{1}{2}Vodm \qquad V_{o2} = Vocm - \frac{1}{2}Vodm \tag{5.2}$$

$$Vidm = V_{i1} - V_{i2} \qquad Vicm = \frac{1}{2}[V_{i1} - V_{i2}] \tag{5.3}$$

$$Vodm = V_{O1} - V_{O2} \qquad Vocm = \frac{1}{2}[V_{O1} - V_{O2}] \tag{5.4}$$

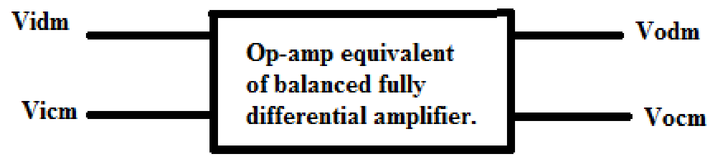

Figure 5.2 Balanced fully differential op-amp with input and output terminals.

5.1.1 Need of Differential Output Op-Amp.

This section discusses about the requirement of fully differential op-amp. The basic necessity of fully differential operational amplifier are as follows:

- Increase in signal swing.
- Cancellation of common mode signals including clock feed through.
- Even-order harmonics get cancelled.
- Common mode output voltage stabilization. Common mode voltage must be small else it may cause poor definition of common mode output voltage.

5.2Basic architecture of Two Stage Op-amp.

The basic two-stage CMOS op-amp is presented in this section. CMOS op-amps are integral parts in various analog and mixed-signal circuits and systems. Due to the simplicity of structure and its robustness the two stage CMOS op-amp has found its usage. Various electrical characteristics such as slew rate, common mode range, gain-bandwidth, offset, output swing etc. are considered while designing op-amps. Moreover, the frequency compensation is essential for closed loop stability as the op-amps are designed to be worked in a negative feedback mode. In order to achieve required amount of stability by the op-amp which is measured by phase margin the other important parameters are compromised, especially the voltage gain. Hence a good frequency compensation strategy and design procedure is a must for designing op-amps that meets all specifications.

Figure 5.3 Block diagram of basic op-amp [21]

Figure 5.3 above shows three stages from which a classic op-amp is made, i.e. its third stage, the buffer stage is ignored. A high gain differential amplifier forms the first stage. The dominant pole of the system is caused due to this stage. The second stage which has a moderate gain is met by the common source amplifier. The third stage is basically a unity gain source follower and forms the third stage [22].

Note: As a part of the thesis work, a design methodology of a two stage fully differential telescopic operational amplifier is discussed in detail. Similar analysis is carried out for the two stage folded cascode operational amplifier and results are compared at 180 nm technology node. Here effort is made to make the unity gain frequency and the slew rate same of both the respective two stage amplifiers. The purpose of such an effort is to carry out a comparison of various parameters viz. voltage gain, phase margin, common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), output swing and power consumption. It has been observed that the two stage telescopic amplifier gives better results in terms of voltage gain, CMRR, PSRR as compared to folded cascade counter-part. Whereas the folded cascode two stage gives better results in terms of bandwidth and output swing limit. Furthermore, it is also seen that the two stage telescopic amplifier is more suitable for low power applications.

5.3 Basic design procedure of a current source

The design procedural discussion of two stage operational amplifier, necessarily involves the prior importance being given to its first stage. It consists of a voltage to current converter. Since current is the output of first stage hence it is called a current source. It ideally converts the difference of two input voltages into a proportional current with certain practical constrains. It consists of a simple differential pair with a current mirror load. Let below diagrams be considered.

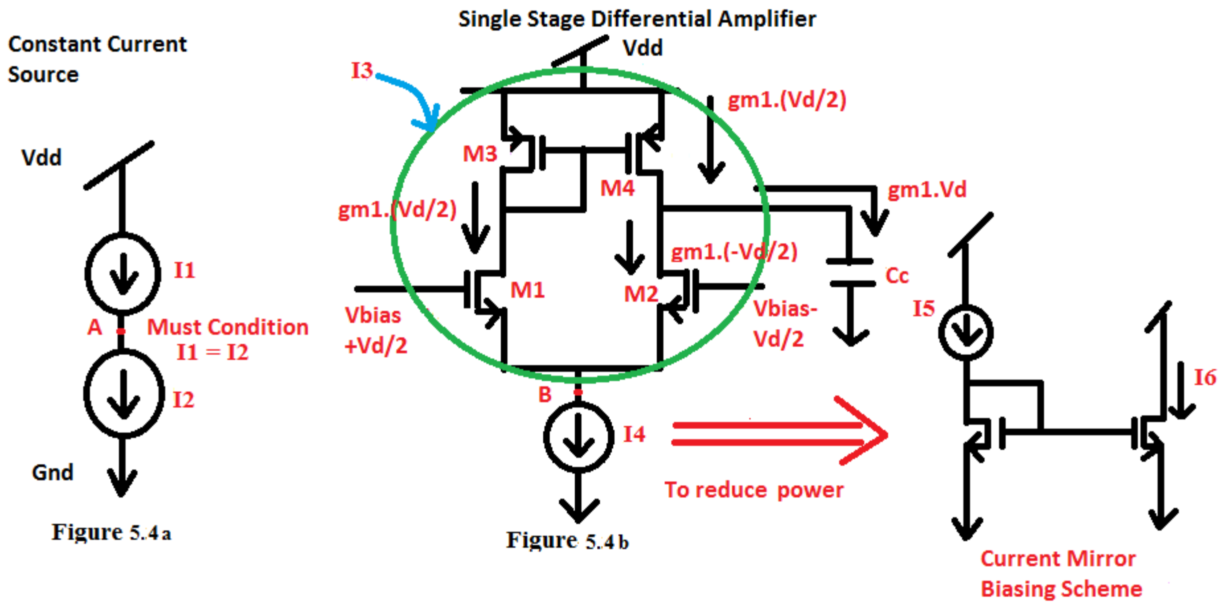

Figure 5.4 a Two independent series connected current sources.

Figure 5.4 b Single ended single stage differential amplifier.

Figure 5.4 a shows two independent series connected current sources named I1 and I2. According to Kirchhoff's Law, to make the circuit stable, I1 must be equal to I2 at point A else, there is a large number of oscillations or instability in the circuit. Same concept applies to design circuit labeled as 5.4 b. Its two independent current sources namely I3 and I4 must be approximately equal, both directed in the same direction at point B. Thus I3 carries equal currents of approximately I3/2 in each of its half differential parts consisting of MOS transistors. To decide the saturation voltage across the MOS transistors, output voltage swing and voltage gain requirements from the amplifier are required to be considered. Power consumption reduction can be achieved by designing I4 with current mirror circuit as in figure 5.4 b. An output AC current of gm1.Vd is also seen in above figure, where gm1 is the trans-conductance of transistors M1, M2 and ±Vd/2 is the input AC voltage signal applied to the gates of M1 and M2 respectively.

5.4 Design process of a fully differential two stage telescopic op-amp.

Below figure represents the design of the mentioned amplifier.

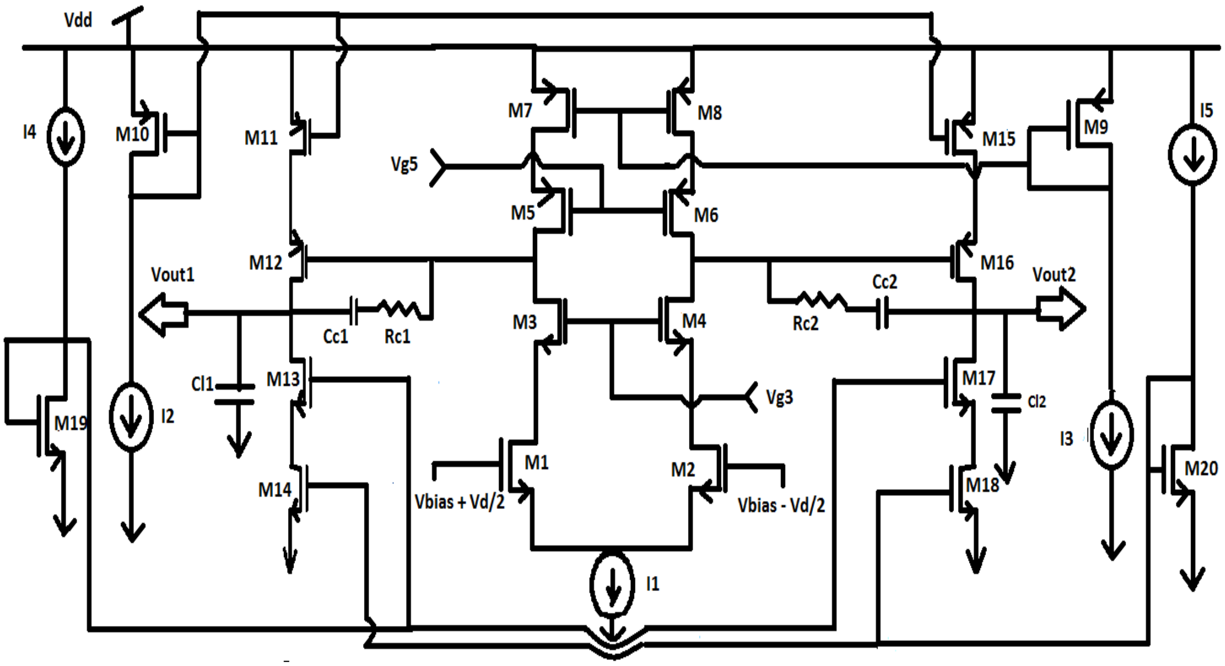

Figure 5.5 Two stage fully differential telescopic amplifier.

In above figure transistors M1 - M8 and the current source I1 forms the first stage which are biased with various sources. M3, M4 forms the cascode devices of differential pair M1 and M2. M7, M8, M5 and M6 forms the PMOS cascoded, current mirrored and constant voltage source biased loads respectively. Owing to the constant current source I1 as in figure 5.5 the amplifier can accommodate a greater space for a higher voltage swing as compared to that when implemented using a current mirrored tail current source as the voltage drop requirement across a constant current source is comparatively less. But the power consumption in this case would be higher.

Let the below expressions be considered.

$$\text{VOM} = 2 \times [\text{VDD}-(|\text{VOD1}| + |\text{VOD3}| + |\text{VOD5}| + |\text{VOD7}| + \text{VCCS})] \tag{5.5}$$

$$\text{A0} \approx \text{GM1} \times [(\text{GM3.RO3.RO1}) \,||\, (\text{GM5.RO5.RO7})] \tag{5.6}$$

$$\text{GM} = \sqrt{(2 \times K \times (W/L)\ \times IDSAT)} \tag{5.7}$$

$$\text{W/L of all transistors} = \frac{(2 \times IDSAT)}{(K \times Vov^2)} \tag{5.8}$$

Here the expression VOM is the output voltage swing of the first stage of the amplifier [22]. VDD is the supply voltage, VOD are the overdrive voltages of the respective MOS transistors and VCCS is the voltage across the constant current source I1. Let the following voltage drops be considered.

VDD = 1.8V, VOD1 = VOD3 = 0.120V, VOD5 = VOD7 = 0.225V and VCCS = 0.210V. The purpose of considering different voltage levels for different types of MOS transistors is explained later. Thus VOM = 2 × (1.8-0.9) = 1.8V. Hence the output bias voltage is adjusted at 2 × (|VOD1|+ |VOD3|+ VCCS) which is equal to 0.9V which is exactly between the rail to rail voltages of 1.8V so as to generate the maximum output swing. The expression A0 is the DC voltage gain [22] of the first stage of the designed amplifier, GM, RO, VOV, IDSAT are the trans-conductance, output resistance, overdrive voltages and saturation drain to source current of the transistors respectively and K is the product of mobility of holes or electrons and the oxide capacitance of a MOS transistor.

After the overdrive voltages are adjusted, consideration must be given to A0. It involves the parallel combination of NMOS and PMOS transistors of the first stage hence for a high voltage gain their W/L values must be comparable. The mobility of electrons are much higher than that of the holes hence to make the W/L values of both the MOS types comparable, the VOD of PMOS transistors are kept considerably greater than that of the NMOS transistors as discussed earlier. Characteristics below shows the nature of output swing of first stage of the designed amplifier with a constant tail current source whose voltage drop is neglected here as it can be of minimum value.

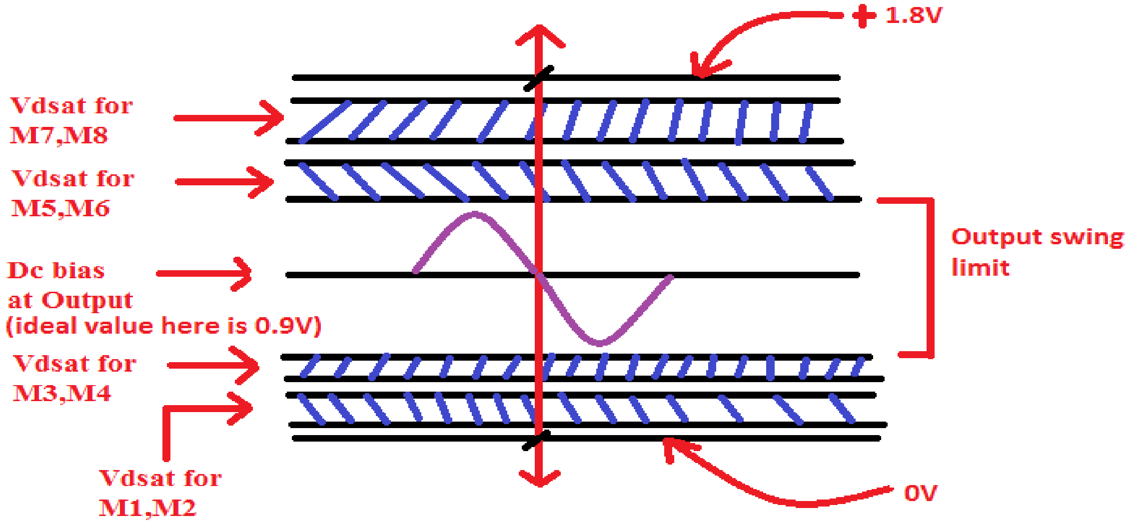

Figure 5.6 Output swing characteristics of a single stage telescopic amplifier.

As shown in above figure that there are all total four levels of saturation voltages to be adjusted. Two levels above and two levels below the output DC value. The voltage gain must be well within the area kept vacant for the output swing. The biasing adjustment details are mentioned in the design steps table (Table 5.1). The DC level at output must be between Vg3 and Vg5 voltage levels.

As discussed before, about the VOD of the NMOS and the PMOS devices, [21] presents the idea of maintaining the VOD of the MOS transistors at different voltage levels. In this design certain values of VOD and VCCS were already considered. But practically the voltage drops across them turned out to be M7, M8 = 348mV, M5, M6 = 820mV, M3, M4 = 143mV and M1, M2 = 435mV and hence only 50mV remains from 1.8V to get adjusted across the constant current source I1. Now to convert I1 to an NMOS transistor with a current mirror bias and given specifications of $IDSAT$ and VOD it requires a large W/L value which produces a large propagation delay hence collapses the circuit. Thus to convert effectively, the actual VOD of the MOS transistors involved in the differential and the PMOS cascoded loads must be reduced which in turn reduces the gain of the amplifier or an amplifier with a lesser slew rate can be designed. The design was initially started with a constant tail current source for both the amplifiers, to maintain same slew rates. Hence accomplishing the first stage design of the telescopic amplifier.

After the first stage is designed, the second stage is cascaded with the first stage by means of Miller Capacitor and the nulling resistor labeled as Cc1, Cc2, Rc1 and Rc2 respectively. Here transistors M11- M14 and M15 - M18 constitute the respective half differential parts of the second stage as shown in figure 5.5. Cl1, Cl2 forms the load capacitors. One design constrain is M12 and M16 cannot be of high W/L value as they tend to push M5 and M6 respectively to linear regions. The plot below shows the input and the output variations of the fully differential two stage telescopic operational amplifier with respect to time for a ±1.25mV, 50 KHz sinusoidal input.

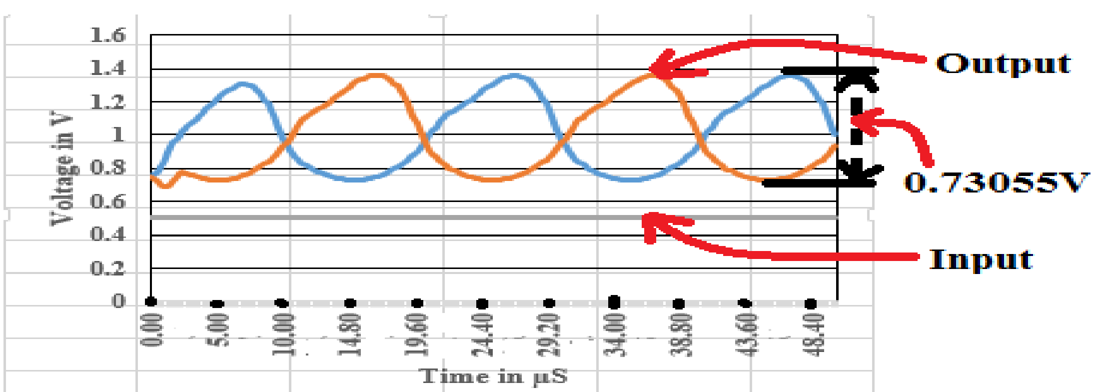

Figure 5.7 Input and output characteristics of the two stage fully differential telescopic amplifier.

The values of Cc1, Cc2, Rc1, Rc2, Cl1 and Cl2 are adjusted observing that the output response indicated in figure 5.7 above, has minimum distortion.

Design steps of two stage fully differential telescopic operational amplifier.

Table 5.1 Design steps of two stage telescopic amplifier

Step 1	*fixing of overdrive voltages from the below equation.* VOM = 2 × [VDD – (|VOD1|+ |VOD3|+ |VOD5|+ |VOD7|+ VCCS)]
Step 2	(W/L)1,2,3,4 = $\frac{2 \times I1/2}{\mu nCox(VoD^2)}$
Step 3	(W/L)5,6,7,8 = $\frac{2 \times I1/2}{\mu pCox(VoD^2)}$
Step 4	*determination of all bias voltages V and bias currents I* VBIAS = VDSSAT + VTN, VG3 = VBIAS - VTN + (VGS3 at I1/2), VG5 = VDD -VSDSAT - (VSG5 at I1/2), VG3 – VTN < VOUT 1,2 < VG5 + |VTP| and I fully differential second stage << I fully differential first stage
Step 5	$\frac{I3}{(W/L)9} = \frac{I1}{(W/L)7+(W/L)8}$
Step 6	(W/L)12,16 = $\frac{IDSAT\ HALF\ DIFF.\ SECOND\ STAGE \times \left(\frac{W}{L}\right)5{,}6}{I1/2}$
Step 7	(W/L)14,18 = $\frac{IDSAT\ HALF\ DIFF.\ SECOND\ STAGE \times \left(\frac{W}{L}\right)1{,}2}{IDSAT\ HALF\ DIFF.\ FIRST\ STAGE}$
Step 8	(W/L)11,15 = $\frac{IDSAT\ HALF\ DIFF.\ SECOND\ STAGE \times \left(\frac{W}{L}\right)7{,}8}{I1/2}$
Step 9	(W/L)13,17 = $\frac{IDSAT\ HALF\ DIFF.\ SECOND\ STAGE \times \left(\frac{W}{L}\right)3{,}4}{I1/2}$
Step 10	$\frac{I2}{(W/L)10} = \frac{IDSAT\ FULL\ DIFF.\ SECOND\ STAGE}{(W/L)11+(W/L)15}$
Step 11	$\frac{I4}{(W/L)19} = \frac{IDSAT\ FULL\ DIFF.\ SECOND\ STAGE}{(W/L)13+(W/L)17}$
Step 12	$\frac{I5}{(W/L)20} = \frac{IDSAT\ FULL\ DIFF.\ SECOND\ STAGE}{(W/L)14+(W/L)18}$
Step 13	Rc1, Rc2, Cc1, Cc2, Cl1, Cl2 are adjusted as mentioned earlier.

VDSSAT is the drain to saturation voltage of an NMOS transistor, VSDSAT is the source to drain voltage of a PMOS transistor. VTN and VTP are the threshold voltages of the NMOS and PMOS transistors respectively. VGS and VSG are the respective gate to source voltage of an NMOS transistor and the source to gate voltage of a PMOS. Others have same meanings as indicated in fig. 5.5 above.

The specifications of all the components used in the above circuit are in below table.

Table 5.2 Specifications of the two stage telescopic amplifier.

VDD = 1.8V	VBIAS = 0.5V	VG3= 0.638V	VG5= 1V	
I1=3mA	I2=6.7µA	I3=411 µA	I4=195 µA	I5=77µA
Rc1=Rc2= 0.5KΩ	Cc1 = Cc2 =15pF	Cl1 = Cl2 = 10pF		
M(1,2,3,4)= 120µm/0.18 µm	M(12,16) = 32µm/0.18 µm			
M(5,6,7,8)= 148µm/0.18 µm	M(13,17) = 12µm/0.18 µm			
M(9) = 16.2µm/0.18 µm	M(14,18) = 4µm/0.18 µm			
M(10) = 2.5µm/0.18 µm	M(19) = 2.1186µm/0.18 µm			
M(11,15) = 42µm/0.18 µm	M(20)= 125µm/0.18 µm			

In above table all transistors used, are in saturation. AC gain obtained here is 1267.3. Input AC signal ± Vd/2 = ± 1.25mV sinusoidal applied at the gates of M1 and M2 respectively.

5.5 Design process of a two stage fully differential folded cascode op-amp.

Below figure represents the design of the mentioned amplifier.

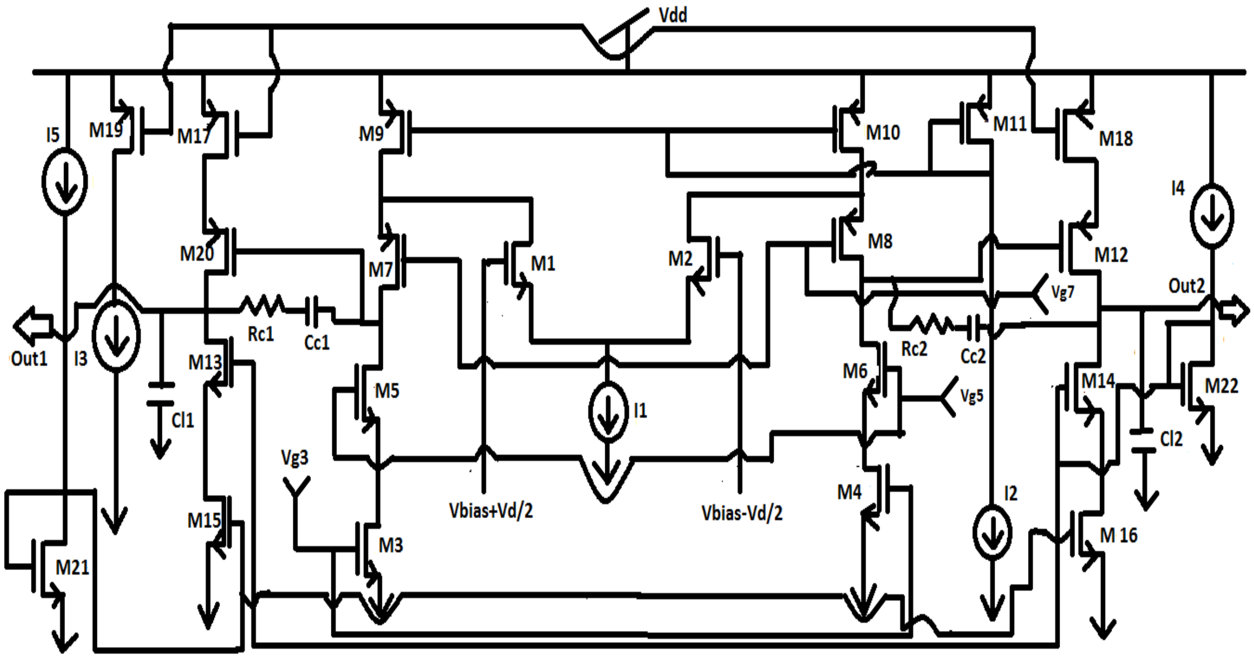

Figure 5.8 Two stage fully differential folded cascode operational amplifier.

Here transistors M1 - M10 and I1 forms the first stage which are biased with various sources as shown in figure 5.8 above.

Let the below expressions be considered.

$$VOM = 2 \times [VDD – (|VOD3|+ |VOD5|+ |VOD7|+ |VOD9|)] \tag{5.9}$$

$$A0 \approx GM1\times \{[GM3.RO3. (RO1 \| RO5)] \| [GM7.RO7.RO9]\} \tag{5.10}$$

Here the expressions VOM and A0 are also the output voltage swing and the voltage gain of first stage of the amplifier [2]. Remaining symbols have usual meanings as earlier. VOM and A0 are adjusted in a similar fashion as explained earlier in case of the previous amplifier. But here the design style is different. M9 and M10 here are current source devices [23] biased with a current mirror, which were not present in the telescopic type. M7 and M8 are the cascode devices of the differential pair M1 and M2 respectively. M3 - M6 forms the NMOS cascoded constant voltage source biased loads. M9 and M10 has large W/L values, each to produce a biasing current which is at least equal to the value of I1 in figure 5.8. Optimally both the biasing currents and the tail current are equal. M7 and M8 also has large W/L values to make sure that the current flowing through each of half differential parts of the differential sub-circuit region must not be greater than half of the current of I1. The W/L values of the remaining M3 - M6 are decided based on the equivalence of current flowing through them and that of M7 or M8. Apart from IDSAT and VOV adjustments that still remains unused in the rail to rail value, among M3, M4, M5 and M6, care must be taken that the transistors are designed with the maximum W/L. The W/L values of M3 and M5 must be comparable to one another. In a folded cascode first stage, the W/L values of the PMOS are greater in order to that of NMOS hence the amplifier has lesser voltage gain as compared to that of telescopic structure. The remaining aspects of the design, for e.g. adjustment of biasing voltage etc. remains same in both the types. Hence accomplishing the first stage design.

The second stage design process is same as the earlier discussed. Cc1, Cc2, Rc1, Rc2, Cl1 and Cl2 are adjusted in a similar fashion observing figure 5.9 below for minimum distortion. Hence the design of fully differential two stage folded cascode operational amplifier is accomplished.

Design steps of two stage fully differential folded cascode operational amplifier.

Table 5.3. Design steps of two stage folded cascode amplifier

Step 1	*fixing of overdrive voltages from the below equation.* VOM = 2 × [VDD – (|VOD3|+ |VOD5|+ |VOD7|+ |VOD9|)]
Step 2	(W/L)9,10 = $\frac{2 \times I1}{\mu pCox(VOD9{,}10^2)}$
Step 3	(W/L)7,8 = $\frac{2 \times I1/2}{\mu pCox(VOD7{,}8^2)}$
Step 4	(W/L)5,6 = $\frac{2 \times I1/2}{\mu nCox(VOD5{,}6^2)}$
Step 5	(W/L)3,4 = $\frac{2 \times I1/2}{\mu nCox(VOD3{,}4^2)}$
Step 6	(W/L)1,2 = $\frac{2 \times I1/2}{\mu nCox(VOD1{,}2^2)}$
Similarly all other biasing voltages, currents and other components are adjusted as the other designed amplifier.	

The specifications of all the components used in the above circuit are in below table.

Table 5.4 Specifications of the two stage folded cascode amplifier

VDD=1.8V	VG7=0.95V	VG5=0.638V	VG3=0.5V	VBIAS=0.5V
I1=3mA	I2=594µA	I3=6.7µA	I4=77µA	I5=195µA
RC1 = RC2 = 0.5KΩ	Cc1 = Cc2 = 15 pF	Cl1 = Cl2 = 10 pF		
M(1, 2) = 160µm/0.18µm	M(13, 14) = 12µm/0.18µm			
M(3, 4) = 152µm/0.18µm	M(15, 16) = 4µm/0.18µm			
M(5, 6) = 120µm/0.18µm	M(17, 18) = 42µm/0.18µm			
M(7, 8,9,10) = 1300µm/0.18µm	M(19) = 3.2µm/0.18µm			
M(11) = 1µm/0.18µm	M(21) = 15µm/0.18µm			
M(12, 20) = 32µm/0.18µm	M(22) = 2.1186µm/0.18µm			

In above table all transistors used are in saturation. AC gain obtained here is 224.46. Input AC signal ± Vd/2 = ± 1.25 mV sinusoidal applied at the gates of M1 and M2 respectively.

The plot below shows the input and the output variations of the fully differential two stage folded cascode operational amplifier with respect to time for a ±1.25mV, 50 KHz sinusoidal input.

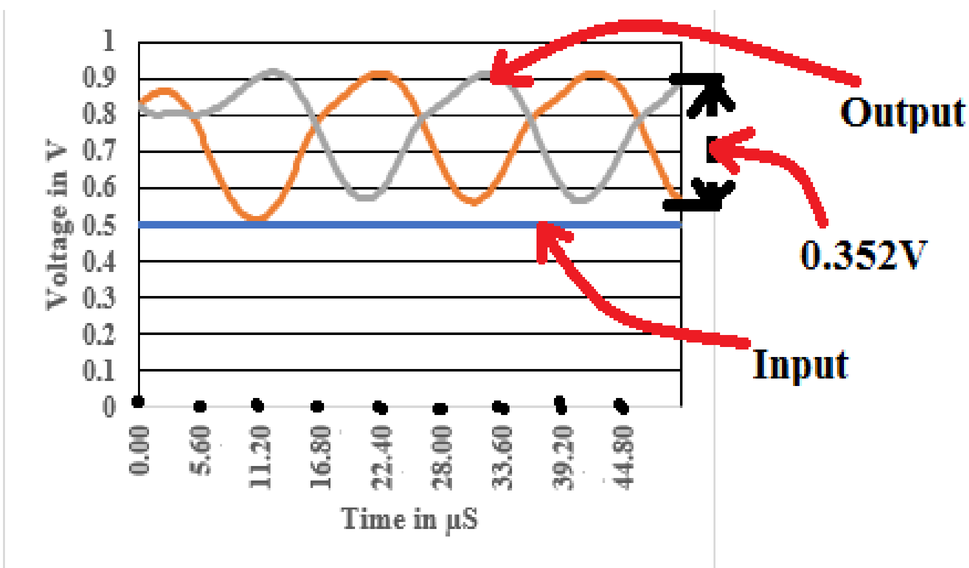

Figure 5.9 Input and output characteristics of the two stage fully differential folded cascode amplifier.

5.6 Frequency compensation consideration

In both the systems a real pole, a complex conjugate pole pair and a real zero forms before the region of unity gain frequencies of respective amplifiers. The formation of complex conjugate pole pair before the unity gain frequency region for both the amplifiers makes them less stable in a certain band of frequency. Many researchers have contributed in the development of frequency compensation strategy. In [1] it is justified that the problems related to instability in certain band of frequency can be resolved by making damping factor greater than 1 which is done by the proper adjustment of complex conjugate pole pairs which in turn is achieved by a different design style for frequency compensation. In [2] and [4] different designing approaches are revealed for frequency compensation as well. In [3] a design style is introduced where noise-power balancing in terms of frequency compensation and consumed power is efficiently achieved. Moreover in [24] a current buffer based approach is discussed which is designed in conjunction with Miller Compensation technique so as to overcome the band of instability problem.

CHAPTER 6

SIMULATION RESULTS AND THEIR COMPARISON

Results are obtained in terms of gain, phase margin, CMRR, PSRR and output swing through simulation at 180 nm technology node. These results are shown in next subsections.

6.1 Gain vs. Frequency

The below is the gain vs. frequency plot of the fully differential telescopic structure.

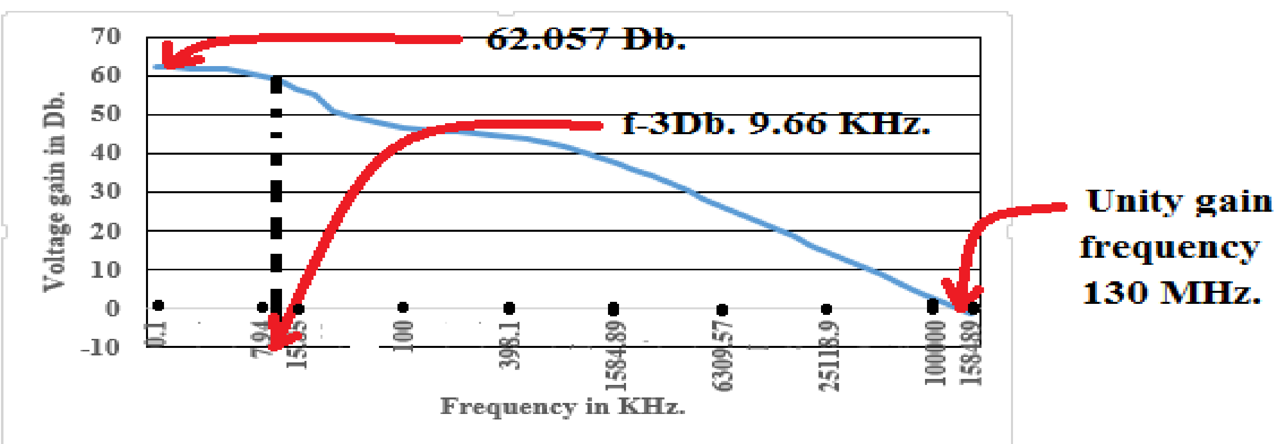

Figure 6.1 Gain vs. frequency plot of the two stage fully differential telescopic structure.

Below is the gain vs. frequency plot of the folded casode type.

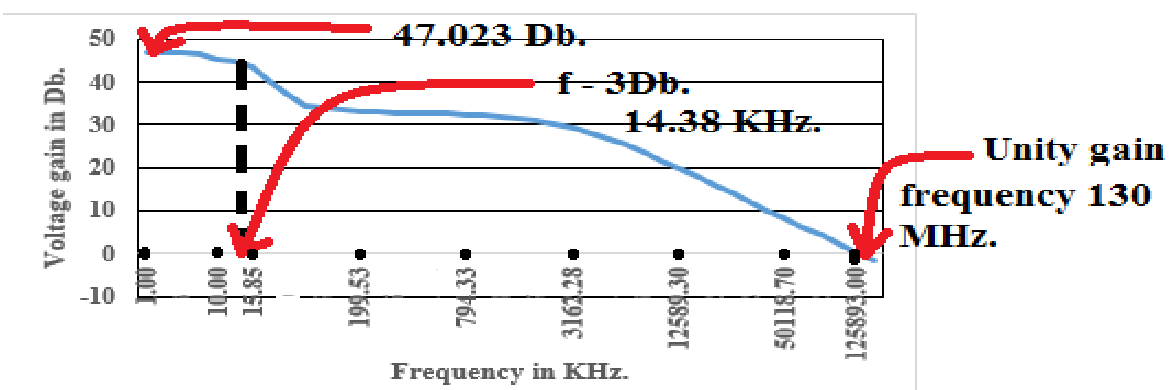

Figure 6.2 Gain vs. frequency plot of the two stage fully differential folded cascode structure.

Figure 6.1 shows that the gain of the designed system is 62.057 Db. and location of first dominant pole is 9.66 KHz and figure 6.2 shows the gain to be 47.023 Db. for the other design style and location of its dominant pole is at 14.38 KHz and both the amplifiers are seen to be maintained at a unity gain frequency of 130 MHz.

6.2 Phase Plot

Below shown the phase response of a fully differential telescopic operational amplifier.

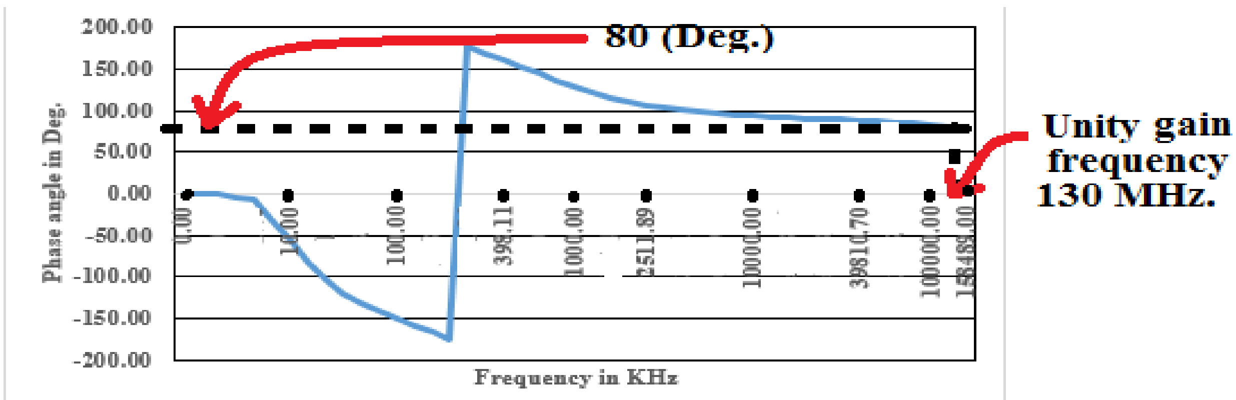

Figure 6.3 Phase response of a fully differential two stage telescopic operational amplifier.

Below shown the phase response of a fully differential folded cascode operational amplifier.

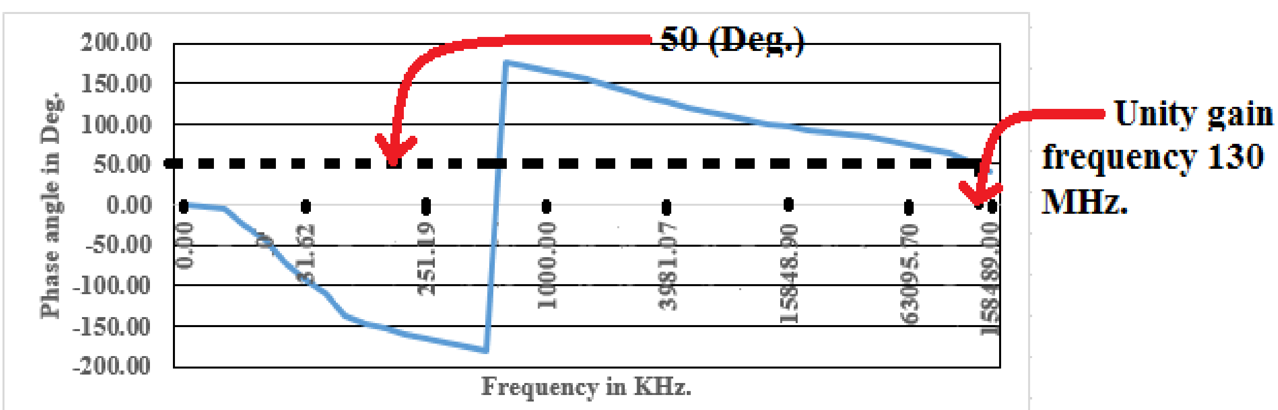

Figure 6.4 Phase response of a fully differential folded cascade operational amplifier.

Figure 6.3 enables to interpret that the phase margin of the designed system is 100° and that of the other corresponding to figure 6.4, turns out to be 130°. Both systems are seen to be perfectly stable as a whole but with constrains at certain frequency band for both the amplifiers as seen in the above figures 6.3 and 6.4 respectively. Both can more be optimized in terms of speed of response and stability if the frequency compensation strategy is handled more efficiently.

6.3 CMRR or common mode rejection ratio

CMRR of the telescopic amplifier designed, is obtained as below.

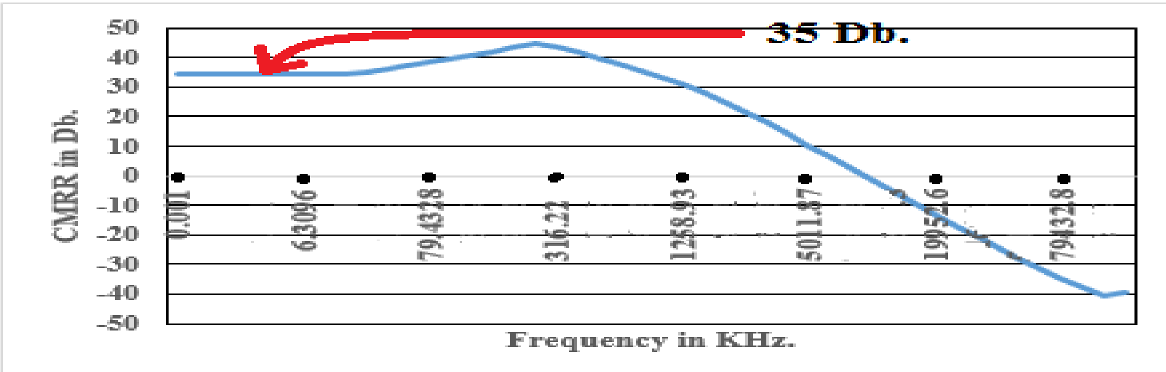

Figure 6.5 CMRR of the two stage fully differential telescopic operational amplifier

The CMRR of the folded cascode amplifier designed, is obtained as below.

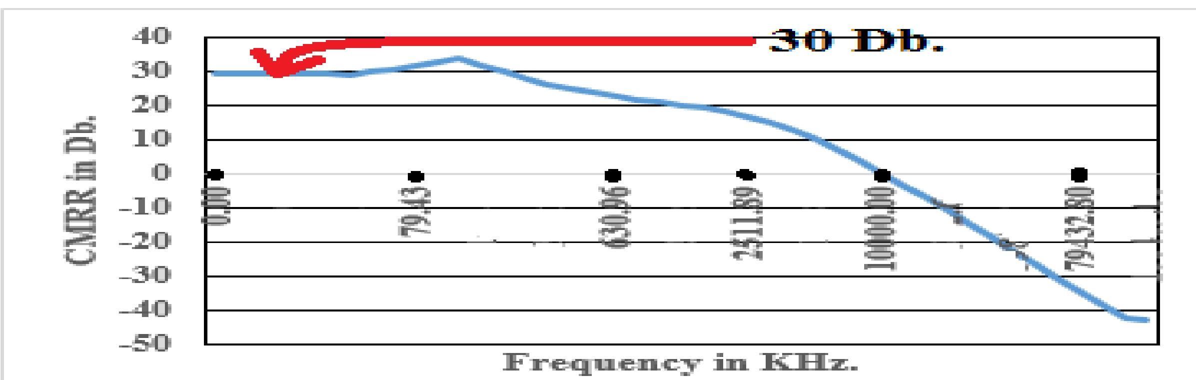

Figure 6.6 CMRR of the two stage fully differential folded cascode operational amplifier

Figure 6.5 shows that the CMRR of the designed system is 35 Db. whereas in figure 6.6 it is seen that the CMRR of the other design style is 30Db.

6.4 PSRR or power supply rejection ratio

The PSRR of the two stage telescopic amplifier designed, is as below.

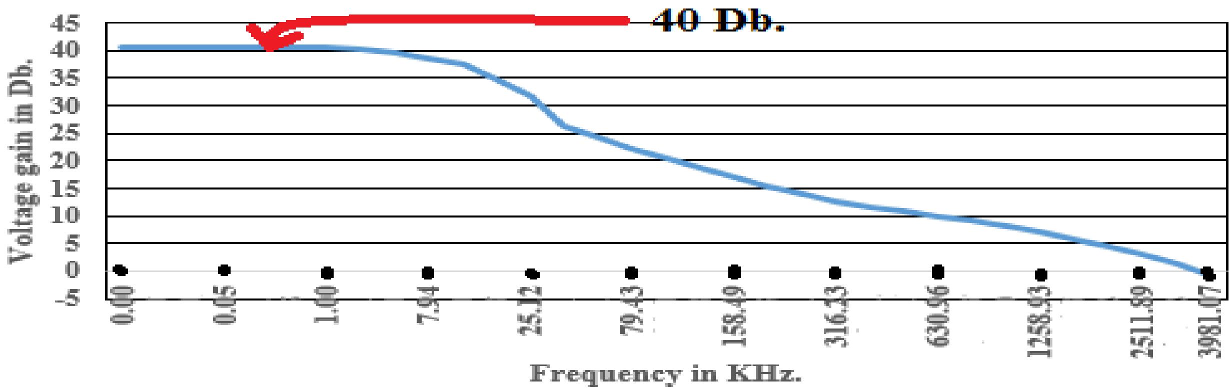

Figure 6.7 PSRR of the two stage fully differential telescopic operational amplifier

The PSRR of the two stage folded cascode amplifier designed, is as below.

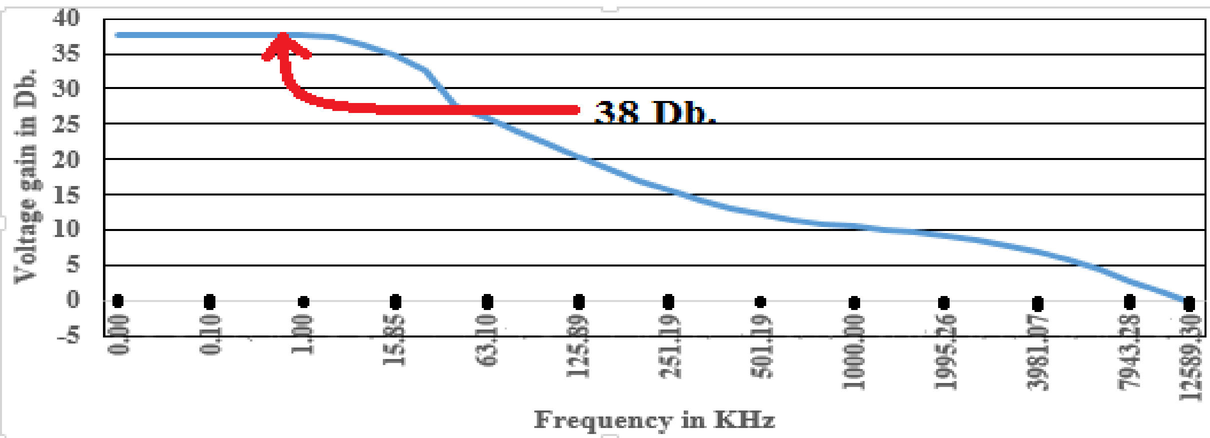

Figure 6.8 PSRR of the two stage fully differential folded cascode operational amplifier

Figure 6.7 shows the PSRR of the designed amplifier is 40.78 Db. whereas figure 6.8 shows that of the other is 38 Db.

6.5 Output voltage swing

The maximum output voltage swing for the two stage telescopic amplifier is shown below in figure 6.9 to be 0.9422V for an input voltage of ± 5mV sinusoidal voltage of frequency 50 KHz. Beyond this input amplitude, the output clips away at peaks.

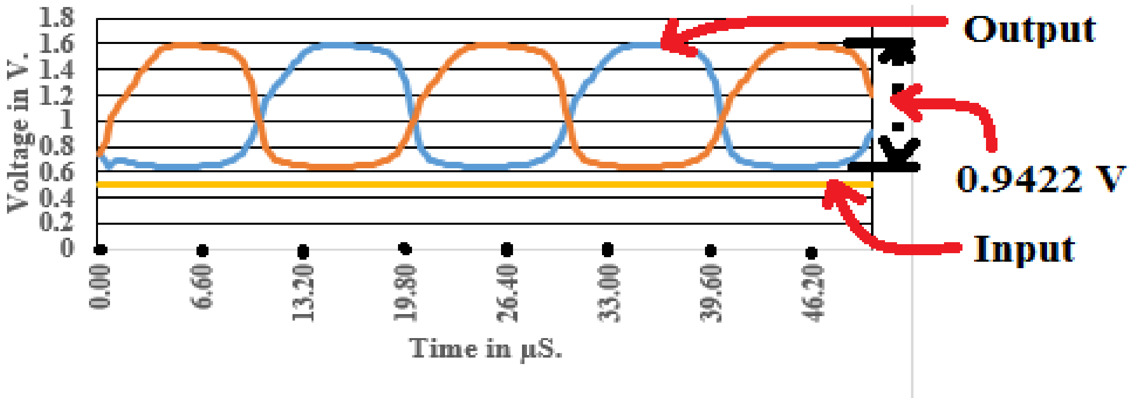

Figure 6.9 Maximum output characteristics of the two stage fully differential telescopic operational amplifier.

The maximum output voltage swing for a two stage folded cascode operational amplifier is shown below.

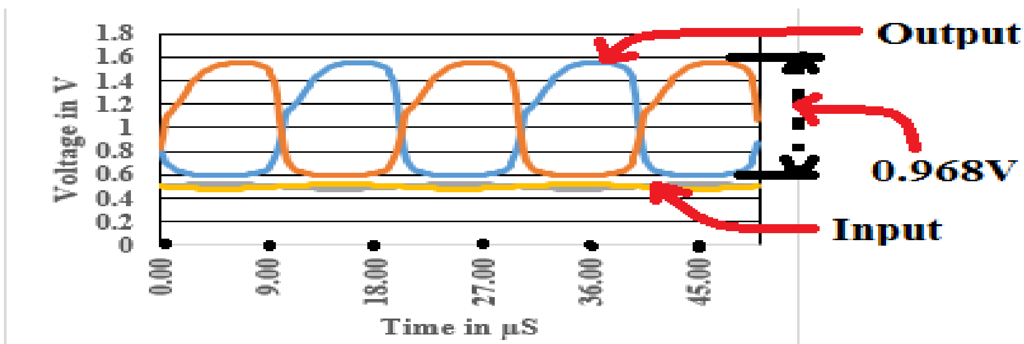

Figure 6.10 Max. output characteristics of the two stage fully differential folded cascode operational amplifier.

The above figure shows the maximum output swing at 0.968V for an input voltage of ± 20mV sinusoidal voltage of frequency 50 KHz. Beyond this input amplitude, output gets clipped away at peaks.

6.6 Minimum differential Input

For the two stage telescopic amplifier designed, the distortion at output starts at an input signal lesser than ± .04µV for a frequency of 50 KHz whereas for that of the other designed type it starts for signals lesser than just ± .3µV for the same frequency which can be verified experimentally from the above two design. Such an advantageous feature of telescopic type amplifier is obtained due to its high CMRR.

6.7 Power consumption

As seen in design style of folded cascode amplifier that it requires a pair of current source transistors of very high W/L value which were not present in the telescopic type hence for same components used, the power consumption in case of folded cascode is higher than the other.

Thus after obtaining the simulation results and the analysis of the above two stage amplifiers, a comparison of them is established. Below chart represents the same in a tabular form.

Table 6.1 Comparison of obtained results of two stage telescopic amplifier and two stage folded cascade amplifier.

Parameters	Two Stage Telescopic	Two Stage Folded Cascode
Voltage gain in Db.	62.057	47.023
Bandwidth in KHz.	9.66	14.38
Phase margin in degrees.	100	130
CMRR in Db.	35	30
PSRR in Db.	40.78	38
Max. output swing in V	0.9422	0.968
Max. differential input in mV	± 5	± 20
Min. differential input in µV	± 0.04	± 0.3
Power consumption comparison	Less	more

Table 6.2 Process parameters [25].

Parameters	NMOS	PMOS
$\mu[cm^2/Vsec]$	181	23
Vt[V]	0.3692	-0.25399
Tox[nm]	0.65	0.67

CHAPTER 7

CONCLUSION AND FUTURE SCOPE OF WORK

7.1 Conclusion

A comparative analysis between two stage fully differential telescopic operational amplifier and two stage fully differential folded cascode operational amplifier has been performed. It has been observed that the telescopic amplifier has higher gain whereas, the folded cascode amplifier has greater bandwidth. It is also seen that the telescopic amplifier is comparatively better in terms of common mode noise and power supply noise. The folded cascode amplifier has comparatively a higher output swing limit. The folded cascode amplifier is a better choice when differential input signals of moderate amplitudes are required to be amplified i.e. the input in the range of few mV. The telescopic amplifier is a better choice when differential input signals of very less magnitude are required to be amplified i.e. the input in the range of few µV. Finally the telescopic amplifier is also a better choice for low power applications.

7.2 Future scope of work

The two stage amplifiers designed do have certain limitations and they do have scope of improvement. Some of the future scope of work are as follows:-

- Removal of the glitch from the phase plots which indicates a small region instability in case of both the two stage designed amplifiers by the usage of an efficient frequency compensation strategy.
- While fabricating the circuit there would be mismatch in the similar transistors which should be taken care by the Common Mode Feedback Circuit.
- The Layout of the transistors are yet to be drawn.
- For both the Fully Differential Two Stage Op-amps the power consumption is relatively high as both of them are designed using Constant Current Sources of 3mA, instead they must be designed using current mirrors.

- Many other parameters which are present in a standard data sheet of an op-amp are required to be found out.
- The compensation resistors are to be replaced with MOS transistors operating in linear region so as to reduce the power consumption.

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