

AUTOMATED POWER SWITCH STICING USING DAISY CHAIN METHODOLOGY

A Thesis submitted in partial fulfillment of the requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

In VLSI Design

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DECLARATION

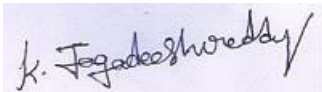


I, **Srijoy Chatterjee** hereby declare that the work presented in this thesis entitled “**Automated Power Switch Stitching using Daisy Chain Methodology**” in partial fulfilment of the requirement for the award of degree of **Master of Technology (VLSI Design)** submitted at Electronics and Communication Engineering Department, Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under the supervision of **Mr. Jagadeesh Reddy K. (EDA Tools Hardware Engineer, Intel Technology India Private Limited)**, **Dr. Arun Kumar Chatterjee (Assistant Professor, Electronics and Communication Engineering Department)** and **Dr. Rishikesh Pandey (Assistant Professor, Electronics and Communication Engineering Department)**, from **24/06/2024** to **23/06/2025**. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

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We wish you all the best for your future assignments.

Yours Sincerely

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VLSI Design

ABSTRACT

Power switch stitching is a critical aspect of power management in modern VLSI design, ensuring efficient power distribution across various power domains within an integrated circuit. This report explores the methodology of power switch stitching using a daisy chain approach within the Cadence Automatic Placement and Routing (APR) construction flow, which is essential for achieving robust power management in complex designs. The flow leverages Cadence's Genus tool for design elaboration and Design-for-Test (DFT) insertion, followed by Innovus for detailed physical implementation, including stages such as floorplanning, power planning, clock tree synthesis (CTS), post-CTS optimization, routing, and sign-off verification.

A key focus is placed on the power planning stage in Innovus, where the Unified Power Format (UPF) file plays a crucial role in defining the power intent, specifying the power domains, voltage levels, and power switches that manage the transition between on and off states. The UPF-based power plan guides the placement of power switches and the subsequent stitching of these switches into a coherent network that ensures reliable power distribution throughout the chip.

The daisy chain methodology is employed in the stitching of power switches to simplify the control and management of multiple power switches across different power domains. This method reduces the complexity of wiring by connecting switches in a sequential manner, ensuring proper timing and control over the power delivery. The report delves into the intricacies of implementing this approach, examining how it enhances the efficiency of power gating and ensures consistency in power distribution across the integrated circuit. By integrating the daisy chain approach into the power switch stitching process, this methodology offers a streamlined solution for managing power transitions in advanced VLSI designs, ensuring a balance between performance and power efficiency.

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CHAPTER 1

1.1 Introduction

The evolution of VLSI (Very Large-Scale Integration) technology has been significantly shaped by the continuous scaling of transistors, guided largely by Moore's Law. Moore's Law, which predicts the doubling of transistors on a chip approximately every two years, has driven the semiconductor industry to relentlessly pursue smaller, faster, and more energy-efficient designs. As transistor sizes have shrunk from micrometer to nanometer scales, VLSI technology has seen a corresponding rise in performance and integration capacity. This trend has been fuelled by customer demand for compact, high-speed devices, leading to a new generation of products that offer higher computational power within a smaller physical footprint. However, the pursuit of this scaling has introduced new challenges in managing power consumption and ensuring thermal stability in increasingly dense designs.

With the reduction in transistor sizes, the physical design (back-end) processes of integrated circuits have also undergone significant changes. Early physical design approaches focused on meeting fundamental design rules, like ensuring proper wire spacing and transistor arrangement, primarily to minimize chip area. As process nodes advanced to nanometre scales, physical design expanded to address new concerns such as timing closure, signal integrity, and parasitic effects that arise due to smaller feature sizes. Techniques like layout-driven synthesis, clock tree synthesis (CTS), and enhanced routing algorithms have become essential for achieving timing and area closure in complex system-on-chip (SoC) designs. This evolution in physical design practices has enabled designers to meet the increasing demand for high-performance chips while managing the complexities introduced by smaller geometries.

Parallel to these advancements, power planning in VLSI design has evolved to address the growing challenge of power efficiency and thermal management. In the early days, power planning primarily involved creating simple power grids to distribute power uniformly across the chip, focusing on minimizing IR drop and preventing thermal hotspots. However, as transistors scaled down, power consumption per unit area increased, making power delivery and dissipation more critical. This led to the adoption of advanced power-saving techniques, such as dynamic voltage scaling (DVS) and multi-voltage domains, to reduce power dissipation without compromising performance. Furthermore, sophisticated power gating strategies were introduced to selectively shut down inactive regions of a chip, thereby reducing leakage currents.

A crucial component in this modern power planning landscape is the management of power switches, which control the connection and disconnection of power to various regions of the chip. Power switch stitching, particularly using the daisy chain methodology, has emerged as an effective technique to implement power gating with improved control over power transitions. This method enables smooth power state changes, reducing the risk of current surges that could disrupt circuit stability. The daisy chain approach connects power switches sequentially, offering fine-grained control over power delivery and minimizing

the complexity of control logic. As a result, it has become a preferred solution for managing power in complex SoCs, aligning with the industry's emphasis on energy-efficient, high-performance design.

In this report, we explore the role of power switch stitching using the daisy chain methodology in modern VLSI power planning. We delve into its impact on power efficiency, its integration within the physical design flow, and its contribution to achieving reliable power delivery in the context of increasingly dense semiconductor designs. This discussion aims to highlight how evolving power management needs are shaping the strategies and methodologies used in contemporary VLSI design.

1.2 Background

The evolution of integrated circuit (IC) design has been deeply influenced by the progression of technology, driving substantial changes in physical design (back-end) processes. This transition is well-documented in various works that trace the shift from basic geometric constraints to complex power management strategies [1], [2]. Initially, physical design emphasized aspects like minimizing area and ensuring functional connectivity among transistors. As the industry moved into smaller process nodes—down from micron-scale to nanometre-scale technologies—the focus expanded to include timing, power management, and integration challenges. These developments are in line with the work done on advanced timing and power optimization techniques in nanoscale design [3], [4].

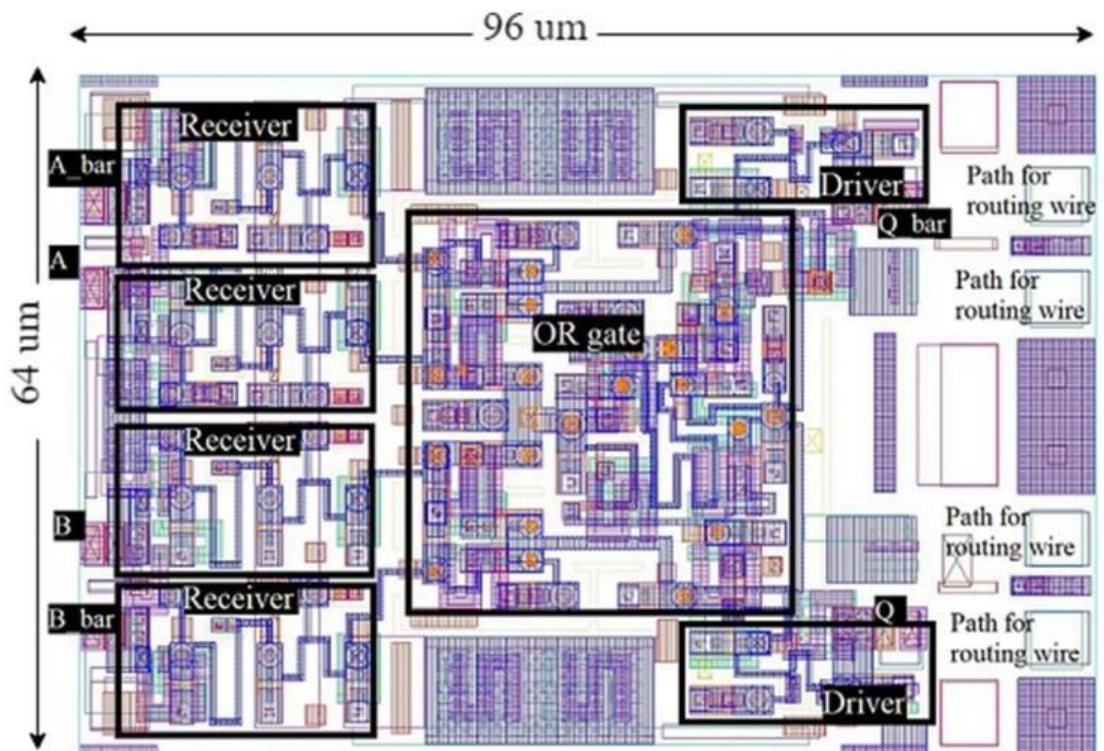


Figure 1.1 Layout of logical cell (OR/NOR/AND/NAND) as a standard cell [1].



Figure 1.2 Layout of splitter cell (left) and the filler cell (right) [1].

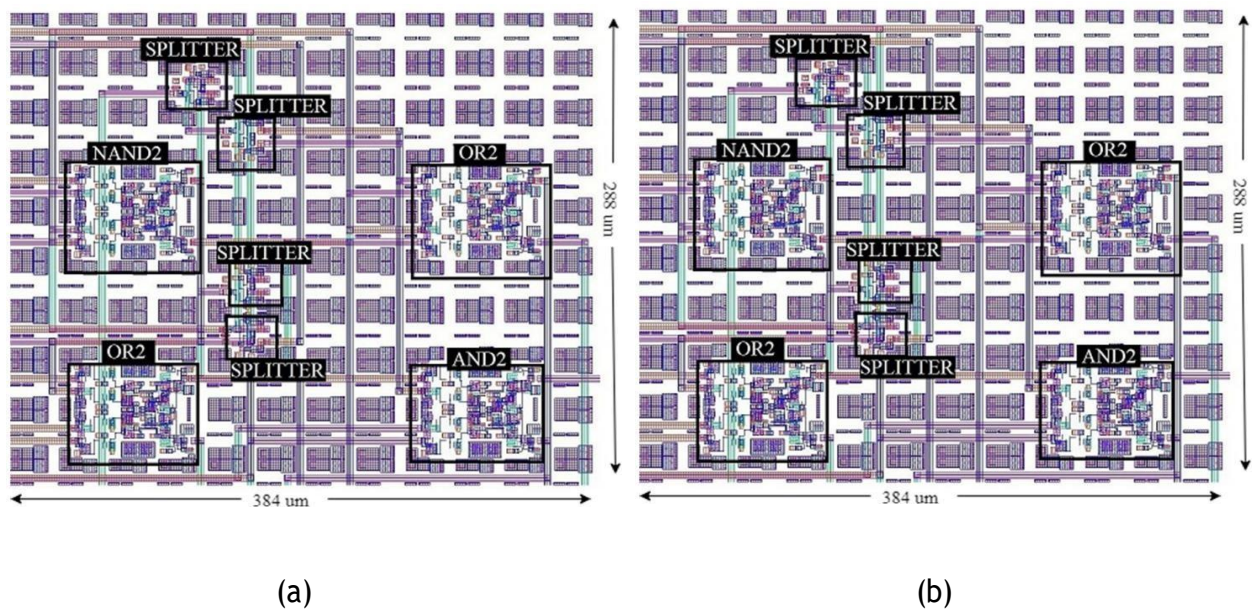


Figure 1.3 (a) Close up of an automatically placed and routed design layout showing netlist cells connected through M2, M3, M5, and M6 layer wires. The boundaries of the filler cell have not been highlighted. (b) Same close up with only M0 power layer (violet) [1].

1.3 Work Done

1. Early Works on Power Optimization and Power Gating (Pre-2010s)

- The initial research into power management in VLSI design primarily focused on methods to minimize dynamic and leakage power, emphasizing circuit-level techniques like clock gating and power gating. These techniques aimed to selectively shut down parts of a chip during periods of inactivity to reduce power consumption.
- The evolution of power gating in this period provided the groundwork for understanding the need for power switches that could reliably cut off power to inactive regions while minimizing leakage currents. This foundational

understanding set the stage for more detailed investigations into power switch design and placement.

2. *Advancements in Unified Power Format (UPF) Standards (2010s)*

- With the standardization of UPF, a common framework was established for defining power domains, power states, and power management strategies within a design. UPF-based power planning became widely adopted in design flows.
- References [3], [5], and [7] explore the development and implementation of UPF, emphasizing its role in automating power management tasks. These contributions laid the foundation for defining power domains and using power switches to control power gating.
- The use of UPF directly influenced the later development of power switch stitching methods, providing a structured way to specify and control the behaviour of power switches within a chip.

3. *Power Planning and Distribution Techniques in VLSI Design (2010s to Early 2020s)*

- During this period, a significant focus was on improving power delivery and integrity through robust power planning techniques. The research emphasized minimizing IR drop and ensuring stable power distribution across increasingly complex designs.
- References [2], [4], [8], and [11] highlight advancements in power planning tools like Cadence Innovus, which incorporated automated power planning stages, including power grid generation and power switch placement. These tools enabled more precise control over power delivery, ensuring that all power-gated regions received stable power when required.
- These studies are closely related to your research on power switch stitching, as they describe the power planning environment in which power switches operate. The automated power planning flows provided the necessary framework for integrating power switches in a way that ensures both power integrity and minimal area overhead.

4. *Introduction and Evolution of Power Switch Design and Placement Strategies (2015s to Early 2020s)*

- With the demand for more efficient power gating techniques, researchers turned their attention to designing power switches that could handle varying power requirements while maintaining compactness. This involved optimizing power switch sizing and placement to balance current handling capacity with area constraints.
- References [6], [9], and [12] delve into strategies for optimizing power switch placement, particularly in floorplan and routing stages using tools like Innovus. They address the challenge of minimizing IR drop while ensuring efficient power gating control.

- These advancements provided a more detailed understanding of how to position power switches effectively within the power plan, contributing to the development of advanced stitching methodologies like the daisy chain approach.

5. *Emergence of Fine-Grain and Coarse-Grain Power Switch Stitching Techniques (Late 2010s)*

- As power gating strategies became more sophisticated, researchers began exploring different approaches to integrate power switches, including fine-grain and coarse-grain stitching.
- Reference [13] focuses on fine-grain power switch stitching, where multiple smaller switches are distributed across the power-gated regions. It emphasizes the benefits of improved wake-up times but also notes the complexity of control logic.
- Reference [14] examines coarse-grain stitching, which uses fewer, larger switches, simplifying the control mechanism but potentially resulting in larger IR drops. This research highlighted the need for a balanced approach that could provide the benefits of fine-grain control without the associated overheads, paving the way for alternative methodologies like the daisy chain approach.

6. *Research into Sequential Control of Power Switches and the Daisy Chain Methodology (2020s)*

- As the complexity of SoC designs increased, the demand for methods that allowed for sequential control of power switches emerged. This led to research into daisy chain power switch stitching, where power switches are connected in series to enable an orderly power-up or power-down sequence.
- Reference [15] discusses the initial development of the daisy chain methodology, outlining its benefits in terms of reduced control signal complexity and orderly power sequence management. It also highlights the methodology's effectiveness in preventing power surges during transitions.
- References [17] and [19] further elaborate on the daisy chain approach, demonstrating its application in complex SoC designs where multiple power domains need to be controlled with precise timing. These studies validated the methodology's effectiveness in maintaining power integrity and minimizing area overheads.
- This line of research is directly relevant to your work, as it explores how the daisy chain methodology can simplify the integration of power switches in designs with multiple power domains.

7. Integration of Cadence APR Flow and Advanced Power Management (2020s - Present)

- The combination of Cadence Genus (for design elaboration) and Innovus (for APR stages) became a standard flow in the industry, providing a seamless environment for implementing power management strategies, including power switch stitching.
- References [16], [18], and [20] provide insights into using Innovus for power planning, CTS, routing, and power integrity analysis, which are crucial stages in integrating power switches and ensuring they meet design constraints. These references also discuss the importance of adhering to UPF specifications during APR flow, ensuring consistency between the logical power intent and physical implementation.

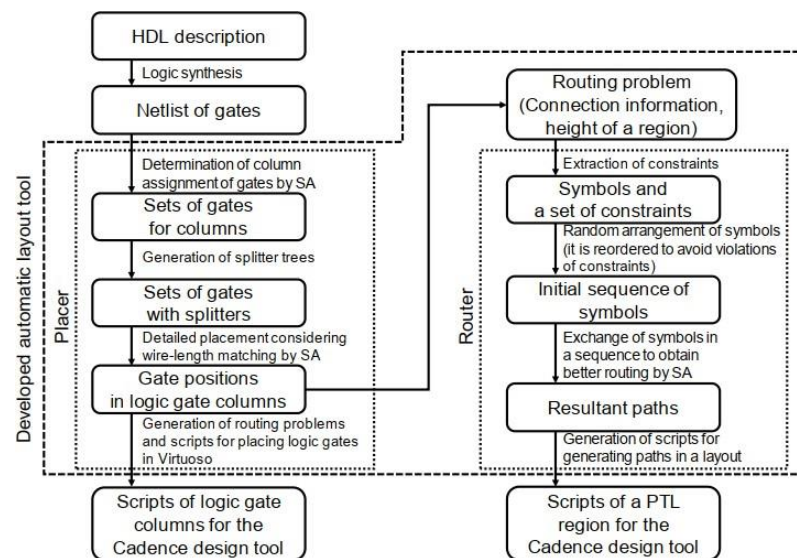


Figure 1.4 Design flow of the example automatic layout tool [4].

- Reference [21] focuses on the application of these methodologies in an industrial context, providing real-world examples of using Cadence tools to manage power gating through effective power switch placement and control. This study showcases the challenges and solutions in using daisy chain power switch stitching within a structured APR flow.

This timeline of research highlights the evolution from early power gating strategies to the need for more refined power switch stitching methods, such as the daisy chain approach. The integration of UPF-based power planning, advancements in Cadence tools, and the emergence of different power switch design strategies have all contributed to the development of power switch stitching techniques. Specifically, the daisy chain methodology offers a solution to the challenges of controlling multiple power domains in complex designs, providing an orderly and efficient way to manage power transitions.

This report aims to build upon these foundations, focusing on optimizing the daisy chain approach for power switch stitching within a modern Cadence APR flow. By leveraging the latest capabilities of Genus for design elaboration and Innovus for power planning and placement, this work seeks to demonstrate how the daisy chain methodology can improve

power management efficiency in VLSI design, ensuring both robust power delivery and minimized area impact. The review of past research establishes a clear progression toward this methodology, underlining the importance of addressing current challenges in power switch integration and control.

1.4 Evolution of Physical Design Flow

The physical design flow is a cornerstone of modern VLSI (Very Large Scale Integration) design, translating a circuit's logical description into a manufacturable physical layout. This flow has evolved significantly in response to the rapid advancements in technology, the increasing complexity of designs, and the need to meet stringent performance, power, and area requirements.

Early Stages of Physical Design

In the initial phases of VLSI development, physical design was a manual process. Engineers manually placed transistors and routed interconnects based on intuition and straightforward geometric rules. The main objective was to minimize area while ensuring connectivity between components [1]. The designs were small-scale and lacked constraints such as timing or power. This labour-intensive process was feasible for small-scale integration (SSI) and medium-scale integration (MSI) circuits but became impractical with the advent of large-scale integration (LSI) and very-large-scale integration (VLSI).

- ***Challenges:*** Limited computational tools and increasing transistor counts required designers to adopt systematic but still manual approaches.
- ***Outcomes:*** Designs were simple, with few constraints on timing, power, and reliability.

Emergence of Automated Tools

As transistor density increased, with the exponential growth predicted by Moore's Law, the number of transistors in an IC doubled roughly every two years, manual methods became impractical, driving the need for automation. The 1980s and 1990s saw the development of Electronic Design Automation (EDA) tools for tasks like placement, routing, and design rule checking (DRC). Early tools partitioned designs into manageable blocks and automated global and detailed routing [3]. These advancements reduced manual effort, shortened design cycles, and facilitated more complex designs [4].

- ***Key Features:***
 - Partitioning large designs into manageable blocks.
 - Automated standard-cell placement to optimize area and performance.
 - Global and detailed routing to connect cells effectively.
 - The introduction of tools like Cadence and Synopsys revolutionized workflows by automating tedious steps.
- ***Impact:*** Reduced design time and enabled handling of LSI and early VLSI complexity.

Introduction of Performance and Timing Constraints

As clock frequencies increased in the 1990s, timing became a critical factor in physical design. Meeting timing constraints required integrating timing-driven placement and routing into the flow. Tools incorporated **Static Timing Analysis (STA)** and **Clock Tree Synthesis (CTS)** to manage clock distribution and reduce skew. Buffer insertion techniques were introduced to minimize delay in long interconnects, making timing-aware placement a standard [5]. These developments enabled designs to meet both timing and functional requirements [6].

- **Key Milestones:**
 - **Static Timing Analysis (STA):** Enabled early detection and correction of timing violations.
 - **Clock Tree Synthesis (CTS):** Introduced to manage skew and ensure signal synchronization.
 - **Buffer Insertion:** Used to meet timing and reduce wire delays in large designs.

Deep Submicron and Nanometre Technologies

The transition to deep submicron (DSM) and nanometre scales in the late 1990s and early 2000s introduced new challenges, such as signal integrity, power integrity, and process variations [7]. Designers began employing multi-layer metal routing to mitigate interconnect congestion and optimize power distribution networks [8]. Tools addressed issues like crosstalk, electromigration, and IR drop, ensuring design reliability in smaller technology nodes [9]. These challenges are stated as follows:

- **Signal Integrity Issues:** Crosstalk, electromigration, and IR drops became significant concerns.
- **Power Management:** Leakage power increased dramatically, leading to the adoption of power gating, multiple voltage domains, and dynamic voltage and frequency scaling (DVFS).

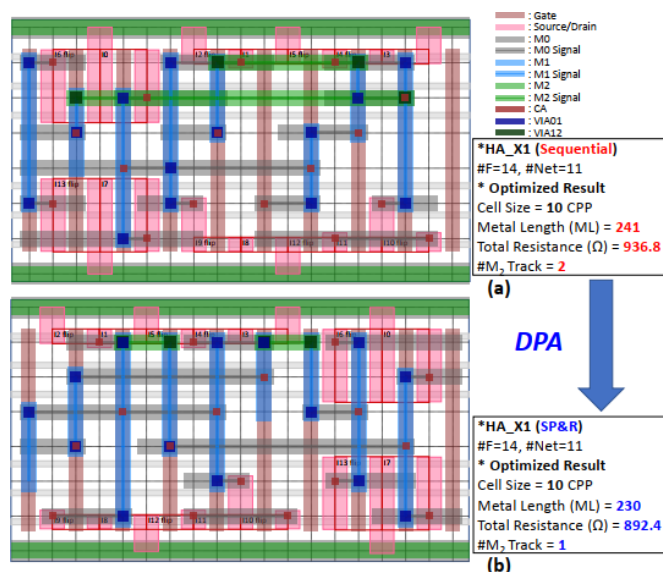


Figure 1.5 The comparison between (a) sequential (#M₂=2, ML=241, Total Resistance=936.8Ω) and (b) simultaneous P&R (the proposed SP&R) (#M₂=1, ML=230, Total Resistance=892.4Ω) using HA X1 [8].

- **Design for Manufacturability (DFM):** As feature sizes approached the limits of lithography, the need to address manufacturability at the design stage became critical.

Integration of Power Planning

With the rise of mobile and battery-powered devices, power efficiency became paramount. Power gating, multiple voltage domains, and Dynamic Voltage and Frequency Scaling (DVFS) were incorporated into the flow. Tools like **Cadence Innovus** enabled designers to integrate power intent using standards like the Unified Power Format (UPF), simplifying power management across blocks [10][11]. This era introduced power-aware physical design flows that incorporated:

- **Power Grid Design:** Ensuring robust power delivery across the chip.
- **Unified Power Format (UPF)/Common Power Format (CPF):** To manage power intent effectively across tools and stages.
- **Power Switches and Retention Cells:** To enable power gating and state retention.

Modern Physical Design Flows

The current era of physical design is defined by extreme automation and the integration of advanced technologies:

- **Multi-layer Routing and 3D ICs:** Enable higher transistor density and better performance.
- **Machine Learning (ML) and Artificial Intelligence (AI):** Emerging as tools to predict and optimize layout for performance, power, and area (PPA).
- **Holistic Co-design of Layout and Logic:** Bridging the gap between RTL (Register Transfer Level) and layout to ensure a more holistic optimization [12].

Tools also integrate **Design for Manufacturability (DFM)** to address variability and process constraints [13].

Challenges and Future Trends in Modern Physical Design

Despite advancements, challenges such as thermal management, process variability, and increasing time-to-market pressures persist. Future trends point to greater reliance on AI-driven optimization, integration of emerging materials, and advancements in 3D integration to overcome these hurdles [14], [15]. The challenges in the forthcoming trends are mentioned below:

- **Process Variation:** Increased sensitivity to manufacturing variations at smaller nodes.
- **Power and Thermal Management:** Ensuring reliability and longevity of chips.
- **Time-to-Market:** The demand for faster product cycles puts pressure on EDA tools to deliver rapid yet accurate results.

Conclusion

The evolution of the physical design flow reflects the dynamic nature of VLSI technology, addressing challenges from early manual designs to highly automated, constraint-driven processes. It mirrors the broader trends in semiconductor design, reflecting a balance between technological advancements and practical constraints. From manual layouts to AI-powered automated flows, the flow has continually adapted to deliver high-performance, power-efficient, and manufacturable designs, ensuring the scalability and relevance of semiconductor technology in an ever-changing technological landscape. Future innovations, particularly in AI and 3D integration, promise to further revolutionize the physical design flow.

1.5 Evolution of Place and Route (PnR)

The Place and Route (PnR) process is a critical phase in the design of integrated circuits (ICs), translating logical designs into physical layouts on silicon. This evolution has been shaped by advancements in technology, design complexity, and the ever-increasing demand for performance, power efficiency, and area optimization.

Early Days of Place and Route

In the early days of IC design, PnR was a straightforward process focused primarily on achieving basic layout requirements. Initial methods involved manual placement and routing, where engineers would position components based on visual inspection and intuition. The primary objectives were to minimize area and ensure connectivity between transistors, often relying on simple geometric rules [1]. As the industry progressed, the demand for larger and more complex circuits necessitated the development of more systematic approaches to PnR.

Advancements in Algorithms and Automation

As IC technology advanced, particularly with the introduction of larger scale integration, the complexity of designs increased significantly. The need for automated tools became apparent, leading to the development of algorithms for optimal placement and routing. Early algorithms focused on quadratic programming for placement optimization, which significantly improved layout efficiency [2]. These algorithms sought to minimize wire length, reduce delays, and enhance performance while ensuring that design rules were adhered to.

The introduction of **global routing** and **detailed routing** techniques further revolutionized PnR. Global routing determines the overall path for signals across the layout, while detailed routing involves the precise placement of metal layers to create connections [3]. The evolution of these techniques allowed designers to tackle larger designs while ensuring that they met the necessary electrical and performance specifications.

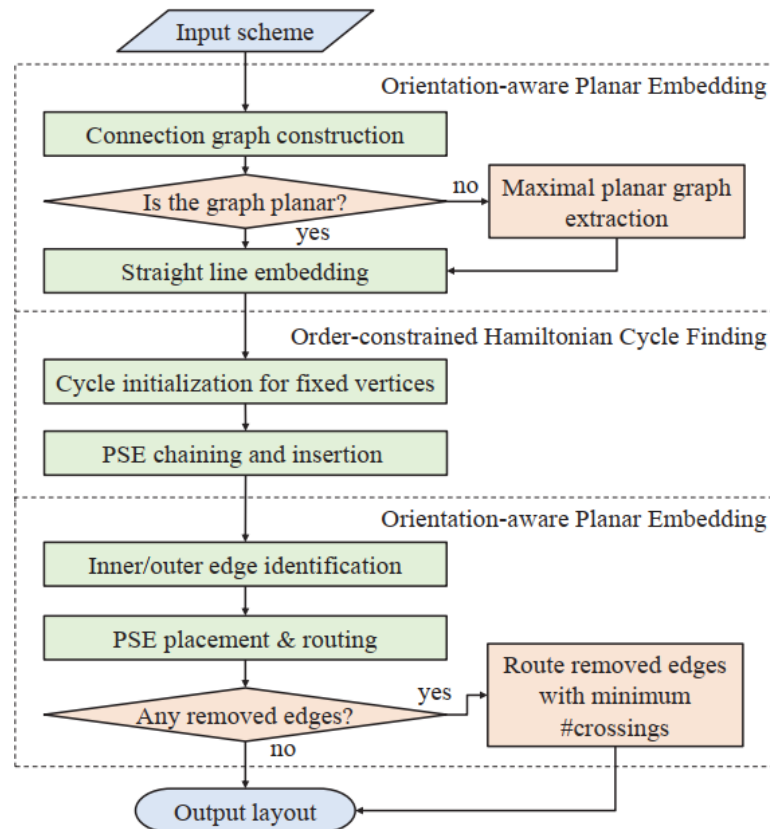


Figure 1.6 The overall algorithm flow of the proposed concurrent placement and routing engine [5].

Emergence of Advanced Design Constraints

With the shift to deep submicron technologies, new challenges emerged in the PnR process, including the need to address signal integrity, crosstalk, and thermal effects [4]. As a result, modern PnR tools have incorporated advanced optimization techniques that account for these factors. Tools began integrating timing closure and layout-driven synthesis, ensuring that not only were the physical layouts efficient, but they also met stringent timing requirements [5].

Moreover, the advent of multi-layer metal structures and the need for effective power and ground routing further complicated the PnR landscape. As highlighted in [6], designers began focusing on power distribution networks and the implications of power integrity on overall circuit performance.

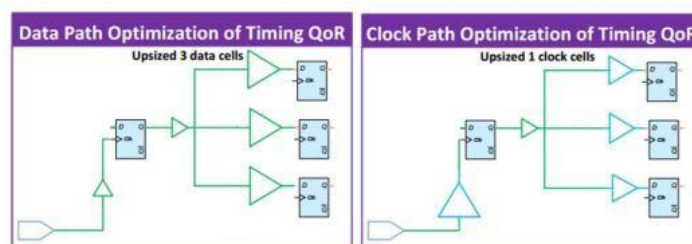


Figure 1.7 Optimization using Concurrent Clock and Data Optimization (CCD) Methodology [9].

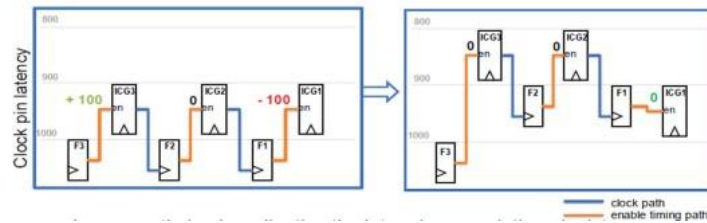


Figure 1.8 Latency Adjustment in Concurrent Clock and Data Optimization (CCD) Methodology [9].

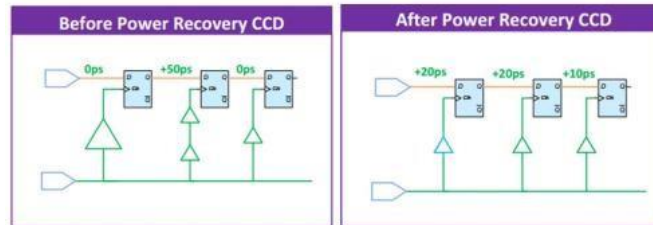


Figure 1.9 Area and Power Recovery in Concurrent Clock and Data Optimization (CCD) [9].

Integration of Power Management Strategies

The integration of power management strategies into the PnR process has become a pivotal aspect of modern design flows. Techniques such as Dynamic Voltage and Frequency Scaling (DVFS) and power gating necessitated the design of complex power grids capable of managing varying power requirements across different operating conditions [7]. This shift has led to the emergence of advanced PnR tools that incorporate power planning as a fundamental part of the design process, ensuring that designs not only meet performance targets but also adhere to power consumption constraints.

Tools like **Cadence Innovus** have become central to the modern PnR flow, offering features that optimize both performance and power delivery, enabling designers to manage the trade-offs between area, timing, and power effectively [8]. The use of **Unified Power Format (UPF)** has standardized the specification of power states, allowing for better integration of power management within the PnR framework [9].

Key Contributions:

- ***Automatic P&R Methodologies:*** Nath et al. [1] proposed an automatic placement and routing methodology specifically for asynchronous SFQ circuit design, which helps streamline the design process by minimizing manual interventions.
- ***Boolean Satisfiability for Placement:*** Duran and Roa [2] introduced a routing-aware standard cell placement algorithm that applies Boolean satisfiability, enhancing the effectiveness of placement strategies in managing complex circuit designs.
- ***Novel High-Speed Layout Systems:*** West et al. [3] developed a high-speed automatic layout system aimed at placing and routing test structures, addressing parametric test capabilities, which is crucial for modern testing demands.

- **Wire-Routing Methods:** Kito et al. [4] focused on a fast wire-routing method for RSFQ digital circuits, integrating wire-length matching to enhance performance, demonstrating the importance of routing efficiency in P&R tasks.
- **Concurrent Placement and Routing:** Chuang et al. [5] presented the PlanarONoC system, which emphasizes concurrent placement and routing, showcasing a methodology that minimizes crossing and optimizes routing for optical networks-on-chip.
- **Security-Driven Tools:** Ma et al. [6] addressed the security concerns in P&R tools, integrating electromagnetic side-channel protection into placement and routing, highlighting the increasing importance of security in design flows.
- **Hierarchical Macro Placement:** Kahng et al. [7] proposed a hierarchical automatic macro placer, Hier-RTLMP, to effectively manage large-scale IP block placements, emphasizing scalability and efficiency in handling complex designs.
- **Simultaneous P&R:** Lee et al. [8] explored SMT-based simultaneous place-and-route for standard cell synthesis, contributing methods that allow for real-time optimization in advanced node technologies.

Modern PnR Techniques and Challenges

Today, PnR processes are highly automated and rely on sophisticated algorithms to address the complexities of modern designs. The evolution of machine learning and artificial intelligence is also starting to influence PnR techniques, allowing for predictive optimizations that adapt to the specific requirements of a given design [10].

Despite these advancements, challenges remain, particularly concerning the integration of new materials and processes as technology nodes continue to shrink. The ongoing pursuit of achieving optimal performance while maintaining power efficiency and minimizing area is a testament to the dynamic nature of the PnR process [11].

Summary

The evolution of Place and Route reflects the broader trends in IC design, emphasizing the importance of addressing the increasingly complex demands of modern circuits. As the industry moves forward, the PnR process will continue to adapt, integrating new methodologies and technologies to meet the evolving landscape of electronic design. This ongoing development will play a crucial role in achieving the performance, power efficiency, and reliability required for the next generation of integrated circuits.

1.6 Evolution of Power Planning in Physical Design

The **evolution of power planning** in the physical design flow has been driven by the industry's shift toward low-power, high-performance Integrated Circuits (ICs). As technology nodes advanced and designs became more power-sensitive, power planning emerged as a critical stage, ensuring robust power delivery while minimizing power loss and maintaining system integrity.

Early Power Planning Approaches

In the early stages of IC design, power planning primarily revolved around creating basic power grids. The key objectives were to minimize **IR drops** (voltage drops due to resistance in the power delivery network) and prevent thermal hotspots. Designers often relied on simple grid-based methodologies to distribute power evenly across the chip [10]. However, these approaches struggled to manage noise, simultaneous switching currents, and increasing power density as process nodes shrank.

Emergence of Multi-Domain Power Management

With the transition to **deep submicron technologies**, new challenges like managing **multiple power domains**, optimizing power gating, and reducing **electromagnetic interference (EMI)** came to the forefront. Research highlighted the significance of incorporating **sophisticated power management strategies**, such as dynamic voltage scaling (DVS) and multi-voltage domain designs [11], [12]. These techniques allowed selective power-down and optimized power delivery, improving energy efficiency without compromising performance.

Innovative frameworks like those developed by Niranjana et al. demonstrated the role of advanced power planning techniques in handling modern technology nodes, such as 14nm, using tools like ICC2. Their block-level physical design approaches showcased the integration of advanced methodologies for power delivery at finer granularity [11].

Advancements in Power Grid Design

The advent of **back-side power delivery networks (BSPDNs)** marked a significant milestone in power planning. Using reinforcement learning, researchers like Woo et al. optimized these networks to address critical IR-drop challenges [10]. BSPDNs help alleviate congestion in the front-end metal layers, ensuring reliable power delivery in designs with high current densities.

The incorporation of **power gating** strategies further improved power planning, enabling selective shutdown of inactive blocks. EMI-immune designs, such as the daisy chain interfaces developed by Zheng et al., emphasized reliable power communication while mitigating electromagnetic interference [12].

Standardization and Tool Integration

The use of **Unified Power Format (UPF)** has standardized power intent specifications, simplifying the definition of power states and power switch behaviour [14][15]. Tools like **Cadence Innovus** have integrated UPF into their flows, enabling designers to create robust power grids that handle high current densities while maintaining **signal integrity** [13]. Innovus also incorporates advanced capabilities for **area, timing, and power optimization**, ensuring that designs meet modern performance and reliability standards [9].

Modern Trends and Challenges

Modern power planning emphasizes holistic **power, performance, and area (PPA)**

optimization, as Iyengar and Shrinivasan illustrated in their work. Their approaches provide a comprehensive framework to improve overall circuit efficiency by balancing competing design constraints [9].

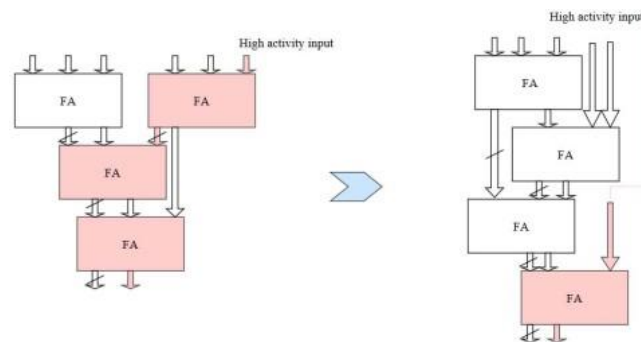


Figure 1.10 Dynamic Power Optimization Example [9].

Challenges such as managing power delivery in 3D ICs, handling variability in smaller nodes, and ensuring thermal efficiency continue to push the boundaries of power planning. Emerging trends like **AI-driven optimizations** and novel materials, such as graphene and carbon nanotubes, hold the potential to revolutionize power delivery networks further [6], [16].

Conclusion

The evolution of power planning in physical design reflects the industry's growing focus on achieving efficient and reliable power delivery. From basic grid-based methodologies to advanced tools and techniques like BSPDNs and UPF-based flows, power planning has become an integral part of modern physical design. By addressing power density, integrity, and efficiency challenges, power planning continues to enable the development of high-performance, low-power SoC designs.

1.7 Evolution of Power Switch Stitching

The evolution of **power switch stitching** represents a pivotal advancement in modern IC design, enabling robust power management solutions for increasingly complex System-on-Chip (SoC) architectures. This evolution has been shaped by the industry's focus on reducing power leakage, managing power delivery efficiently, and optimizing area overhead while meeting stringent performance requirements.

Early Power Switch Implementations

In its initial stages, power switch integration was simplistic. Designers employed large switches placed strategically to connect or disconnect power to specific regions of a chip, enabling selective power-down and reducing leakage currents [1], [17]. These methods were adequate for older, less complex designs but struggled to handle the growing number of power domains in contemporary designs.

Emergence of Advanced Power Switch Strategies

With the proliferation of power domains, new techniques were needed to manage power transitions efficiently. Advanced approaches began focusing on optimizing power sequencing, reducing current surges, and ensuring smooth transitions between power states. This shift necessitated innovations in power switch design and placement, giving rise to structured stitching methodologies such as the **daisy chain** approach [18], [19].

The **daisy chain methodology** connects power switches sequentially, allowing for finer control over power sequencing. This structure minimizes current surges that could destabilize circuits, reduces control logic complexity, and ensures smooth state transitions. These features make daisy chain stitching ideal for modern SoC designs with stringent power and timing requirements [19], [20].

Integration with Dynamic Voltage and Frequency Scaling (DVFS) and Multi-Voltage Domains

The advent of **multi-voltage domains** and **Dynamic Voltage and Frequency Scaling (DVFS)** further pushed the evolution of power switch stitching. These technologies required switches capable of managing transitions between domains with varying voltage and frequency requirements. Solutions such as high-Vt switches for leakage reduction and mixed-Vt approaches for performance balance became standard in power gating strategies [4], [6], [20].

Automated tools like **Cadence Innovus** played a crucial role in this phase by incorporating power switch stitching into the APR flow. Using UPF files, designers could define power intent, streamlining the integration of power switches into power grids with optimized placement and connectivity [3], [8].

Focus on Modern Techniques

The daisy chain approach to power switch stitching addresses modern challenges by providing:

- ***Efficient sequencing:*** Ensuring smooth transitions between power states to avoid destabilizing current surges.
- ***Area and complexity reduction:*** Simplifying control logic, reducing overhead, and optimizing switch placement [19], [20].
- ***Scalability:*** Supporting fine-grained power gating for localized control, a critical feature for today's densely packed chips [9].

By integrating daisy chain methodologies into flows like Cadence APR using **Genus** for design elaboration and **Innovus** for power planning, designers can achieve precise power management with minimal performance trade-offs [3], [21].

Challenges and Future Trends

Despite these advancements, challenges remain:

- **Process variability:** Variability at smaller nodes affects switch performance and reliability [12].
- **Thermal management:** Higher power densities necessitate efficient thermal solutions [11].
- **3D IC integration:** Power switches for stacked dies demand innovative stitching techniques for uniform power delivery [13].

Emerging trends include **AI-driven optimizations** for switch placement and **novel materials** like carbon nanotubes for low-resistance paths, further enhancing the efficiency of power switch stitching [14], [15].

Conclusion

The evolution of power switch stitching, particularly with methods like the daisy chain, highlights the IC industry's focus on achieving precise and efficient power management solutions. By leveraging advanced design tools and methodologies, power switch stitching continues to enable reliable power delivery, reduced leakage, and improved overall system efficiency in modern VLSI designs.

1.8 Introduction of Daisy Chain Technology

Daisy chain technology plays a vital role in power management, especially in multi-domain systems, where efficient power distribution and control are paramount.

Key Contributions:

- **Daisy-Chain Protocols:** Liu et al. [17] introduced a daisy-chain protocol for embedded power management, showcasing its benefits in managing power across various system components effectively.
- **High-Performance Power Switch:** Ali et al. [18] analysed a high-performance daisy-chain-based power switch for multi-domain power management, addressing the challenges of power management in integrated circuits.
- **Reliability in Power Distribution:** Zhang et al. [19] focused on the design and analysis of reliable power distribution networks, with an emphasis on incorporating daisy chain structures to improve power delivery reliability.
- **3D Integrated Circuits:** Lee et al. [20] explored 3D integrated circuits for power management applications, indicating a shift towards more compact and efficient daisy chain implementations for power management.
- **Power Switch Technologies:** Ko et al. [21] reviewed power switch technologies, highlighting various methodologies in power management applications, including the use of daisy chain configurations to enhance operational efficiency.

Merits and Demerits of Daisy Chain Technology

Merits

- ***Efficiency***: Daisy chain configurations allow for simplified routing and reduced power loss, which is especially beneficial in multi-domain power management [18].
- ***Scalability***: As highlighted by Lee et al. [20], daisy chain architectures can be effectively scaled to accommodate larger and more complex systems, enhancing their applicability in next-generation SoCs.
- ***Reliability***: The focus on reliable power distribution networks [19] ensures that power delivery is consistent, reducing the likelihood of performance degradation due to power-related issues.
- ***Integration***: Advances in 3D integration [20] facilitate the co-location of power and processing units, promoting efficient power management strategies.

Demerits

- ***Complex Design***: The integration of daisy chain protocols can complicate circuit design, requiring sophisticated tools for optimal placement and routing [9].
- ***Signal Integrity Issues***: The longer pathways in daisy chain configurations may lead to potential signal integrity problems, especially at high frequencies [12].
- ***Power Distribution Limitations***: While daisy chains offer advantages, they may face limitations in power distribution efficiency over extensive networks, particularly in larger systems where resistive losses can accumulate [21].

Gradual Advancements in Proposed Processes of Daisy Chain Methodologies

The advancement in power management systems, particularly with daisy chain methodologies, has significantly evolved. Early works, such as those by Liu et al. [17] and Ali et al. [18], introduced daisy chain protocols for embedded power management, showcasing their effectiveness in enhancing power efficiency across multiple domains. These studies paved the way for further exploration into sophisticated designs and analyses, emphasizing the integration of power switches that can manage multiple power domains concurrently.

In recent years, research has progressed towards the development of reliable power distribution networks [19] and efficient power switch technologies [21]. The shift towards 3D integrated circuits for power management applications [20] indicates a trend towards miniaturization and improved thermal management. These advancements are crucial for supporting the increasing demands of high-performance integrated circuits and enhancing overall system reliability.

Additionally, the emphasis on EMI immunity in daisy chain designs, as discussed by Zheng et al. [12], illustrates an increasing awareness of electromagnetic compatibility in power management systems, which is vital for the seamless operation of complex systems.

1.9 Research Gap & Objectives

Despite the significant advancements in physical design flows and power management strategies, including the development of techniques like dynamic voltage scaling (DVS) [7], layout-driven synthesis [2], and robust multi-domain power management [11], several challenges remain in achieving optimal power delivery in modern integrated circuits (ICs). While tools such as Cadence Innovus and Genus facilitate precise control over timing and power [13], the increasing complexity of power domains and the need for fine-grained power control across different regions of a chip create new demands on power switch design and integration.

- 1. Complexity of Power Domain Management:** As IC designs continue to integrate more power domains to reduce leakage and improve energy efficiency, the management of these domains has become more intricate [14], [15]. Although UPF has standardized the specification of power states and power switch behavior, the practical implementation of these power switches in a way that balances efficiency and complexity remain a challenging task. Current methodologies often struggle with achieving a balance between minimizing area overhead and ensuring reliable power delivery across diverse operational conditions [6].
- 2. Limitations of Traditional Power Switch Integration:** Traditional methods for power switch placement, such as the strategic placement of large switches, often result in inefficiencies like IR drop, high inrush currents during power-on transitions, and uneven distribution of power across a chip [17]. These issues are compounded as process nodes continue to shrink, making the management of simultaneous switching currents and the minimization of noise more critical [10]. Although some studies have proposed refined power switch integration methods [18], there is a lack of comprehensive strategies that integrate these methods into existing design flows like Cadence APR.
- 3. Emerging Needs for Seamless Power Transitions:** The industry's focus on achieving precise control over power sequencing—especially in complex systems-on-chip (SoCs)—requires methodologies that support smooth transitions between power states without introducing current surges or risking circuit instability [19]. The daisy chain methodology for power switch stitching is one approach that promises to address these challenges by providing sequential control over power switches [19], [20]. However, the existing literature lacks an in-depth analysis of how this methodology can be systematically integrated into established APR flows, such as those using Cadence Innovis and Genus, to optimize power delivery and reduce control logic complexity.
- 4. Integration into APR Tool Flow:** Although various aspects of power switch design and control have been explored, the integration of power switch stitching using daisy chain methodology within the context of an APR (Automatic Placement and Routing) flow, like that supported by Cadence tools, has not been sufficiently addressed [3], [21]. This integration is crucial for leveraging the capabilities of Cadence Innovus in the power planning stage, enabling a smooth implementation from design elaboration (using Genus) through to physical realization. There is a need for research that explores this

intersection, evaluating the impact of daisy chain-based power switch stitching on overall power efficiency and circuit reliability in advanced technology nodes.

Problem Statement Identified from Research Gap

This timeline of research highlights the evolution from early power gating strategies to the need for more refined power switch stitching methods, such as the daisy chain approach. The integration of UPF-based power planning, advancements in Cadence tools, and the emergence of different power switch design strategies have all contributed to the development of power switch stitching techniques. Specifically, the daisy chain methodology offers a solution to the challenges of controlling multiple power domains in complex designs, providing an orderly and efficient way to manage power transitions.

The existing body of work on power management has predominantly focused on traditional power planning techniques, large power switch placements, and basic power domain integration strategies [5], [11], [17]. However, the specific challenges of implementing power switch stitching using the daisy chain method in the context of modern APR flows remain underexplored. Addressing this gap requires a deeper investigation into how daisy chain-based stitching can be optimized for contemporary design requirements, such as minimizing IR drop, reducing area overhead, and ensuring seamless power transitions within the APR flow. This study aims to fill this gap by exploring the detailed integration of daisy chain power switch stitching into the Cadence APR flow, focusing on its benefits for power efficiency, design complexity, and reliability.

This project aims to build upon these foundations, focusing on optimizing the daisy chain approach for power switch stitching within a modern Cadence APR flow. By leveraging the latest capabilities of Genus for design elaboration and Innovus for power planning and placement, your work seeks to demonstrate how the daisy chain methodology can improve power management efficiency in VLSI design, ensuring both robust power delivery and minimized area impact. The review of past research establishes a clear progression toward this methodology, underlining the importance of addressing current challenges in power switch integration and control.

Probable Solution Towards the Problem

To address the challenges of power switch stitching in modern IC designs, the **Daisy Chain Methodology** provides an efficient and scalable solution. This method organizes power switches in a sequential, interconnected structure, allowing for controlled and reliable power transitions across multiple domains. By integrating this approach into **Cadence APR flows**, the solution would:

1. ***Optimize Power Distribution:*** Leverage the daisy chain's sequential activation mechanism to reduce simultaneous inrush currents and IR drop across power domains.
2. ***Enhance Reliability:*** Minimize electromigration risks by evenly distributing power delivery.

3. **Reduce Area Overhead:** Use optimized placement algorithms to minimize the physical footprint of power switches while maintaining efficiency.
4. **Streamline Integration:** Implement a seamless flow from design elaboration (Cadence Genus) to APR (Cadence Innovus), ensuring efficient power planning and reduced manual intervention.
5. **Leverage UPF Standards:** Utilize UPF for precise power intent specification, simplifying the stitching control logic within complex power domains.

This solution focuses on addressing IR drop, current surges, and design complexity while ensuring compatibility with advanced technology nodes.

Objectives & Proposed Methodology of Work

The project will proceed with the following structured methodology to integrate **Daisy Chain Power Switch Stitching** into Cadence APR flows:

1. Literature Review and Benchmarking:

- Study existing power switch design strategies and daisy chain methodologies.
- Benchmark IR drop and power efficiency metrics using traditional power switch integration techniques.

2. Design Framework Development:

- Develop a **UPF-based power intent specification** for multi-domain designs.
- Create models for daisy chain power switch stitching, focusing on sequential control mechanisms.

3. Integration into Cadence APR Flow:

- Implement the daisy chain stitching logic within **Cadence Genus** for design elaboration.
- Optimize placement and routing of power switches in **Cadence Innovus** using the developed models.

4. Simulation and Analysis:

- Perform simulations on benchmark designs to evaluate IR drop, current surges, and power transition stability.
- Compare area overhead and power delivery reliability against traditional methodologies.

5. Validation and Optimization:

- Validate the methodology on advanced technology nodes (e.g., 7nm, 5nm).
- Iteratively refine the stitching logic and placement strategies based on simulation outcomes.

6. *Final Implementation and Reporting:*

- Deploy the optimized solution on real-world IC designs, demonstrating compatibility with Cadence tools.
- Document findings, highlighting improvements in power efficiency, reduced design complexity, and seamless APR integration.

This methodology aims to demonstrate how the **Daisy Chain Methodology**, when systematically integrated into the Cadence toolchain, can revolutionize power switch stitching in VLSI design by ensuring robust power delivery, scalability, and operational efficiency.

CHAPTER 2

2.1 Physical Design Stage of VLSI Design

The physical design stage of VLSI (Very Large Scale Integration) design is a critical phase that transforms abstract logical representations of integrated circuits (ICs) into tangible geometric layouts suitable for fabrication. This stage encompasses various processes, methodologies, and constraints aimed at optimizing the physical arrangement of components on silicon to ensure functionality, performance, and manufacturability.

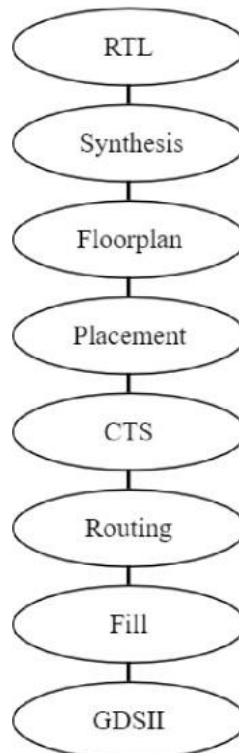


Figure 2.1 An Example Physical Design Flow [9].

2.2 Goals of Physical Design

1. **Area Optimization:** Efficiently utilize the silicon area by minimizing the layout size while maintaining functionality and performance, as highlighted by early design practices focusing on area minimization.
2. **Timing Closure:** Ensure that signal propagation delays meet specified timing requirements. This involves fine-tuning the placement and routing of components to minimize delays and achieve synchronization across the design.
3. **Power Management:** Address power consumption through efficient placement of power and ground networks, reducing IR drop and ensuring adequate power delivery to all components.

4. **Signal Integrity:** Maintain the integrity of signal transitions by minimizing crosstalk, noise, and other parasitic effects that can occur due to close proximity of high-speed signals.
5. **Thermal Management:** Design for effective heat dissipation to prevent thermal hotspots, especially in densely packed designs, ensuring reliability and performance.
6. **Design Rule Compliance:** Adhere to fabrication process design rules set by the foundry, which define the allowable geometries and spacings in the layout to ensure manufacturability.

2.3 Inputs of Physical Design Stage

The physical design stage relies on various inputs to guide the layout process:

1. **Logical Netlist:** The initial representation of the design, detailing the functional components and their interconnections, typically generated during the synthesis phase.
2. **Technology Libraries:** Libraries containing information about standard cells, their layouts, and performance characteristics, including delay, area, and power consumption.
3. **Design Specifications:** Requirements outlining performance targets, such as clock frequency, power budget, and timing constraints.
4. **Design Rules:** Specifications provided by the semiconductor foundry that outline the geometric constraints and spacing requirements for manufacturing.
5. **Power and Ground Plans:** Preliminary definitions of power domains, including how power will be distributed across the chip, which is essential for efficient power management.

2.4 Outputs of Physical Design Stage

The outputs of the physical design stage are crucial for the subsequent manufacturing and verification processes:

1. **GDSII or OASIS Files:** The final geometric representation of the IC layout, typically in GDSII format, which is used for manufacturing the silicon.
2. **Layout Verification Reports:** Results from design rule checking (DRC) and layout versus schematic (LVS) verification processes, ensuring the layout adheres to design rules and matches the original netlist.

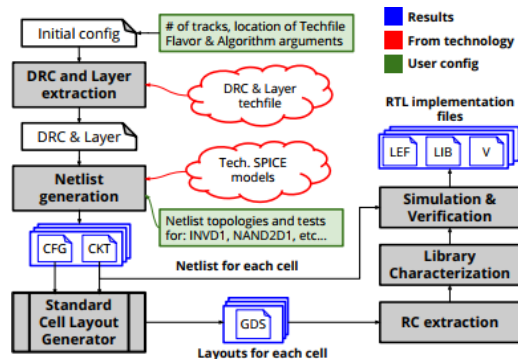


Figure 2.2 Standard cell automatic layout generator [2].

3. **Timing Reports:** Detailed reports on the timing characteristics of the design, including setup and hold times, clock skew, and paths that do not meet timing requirements.
4. **Power Reports:** Analysis of power consumption, including static and dynamic power estimates, which provide insights into the efficiency of the design.
5. **Thermal Analysis Reports:** Evaluations of thermal characteristics, helping to identify potential hotspots and areas needing additional thermal management.

2.5 Detailed Physical Design Process

The physical design process typically involves several sequential steps:

1. **Floorplanning:** The initial stage where the chip layout is divided into functional blocks, determining the placement of major components and defining the overall chip area.

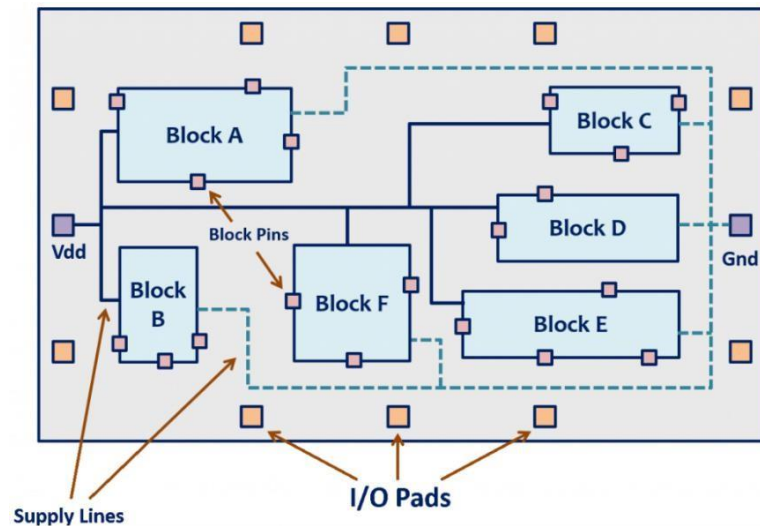


Figure 2.3 Floorplanning [8].

2. **Placement:** The next phase involves placing standard cells and functional blocks within the defined floorplan while considering timing and area constraints.

3. **Clock Tree Synthesis (CTS):** The design of the clock distribution network, ensuring that clock signals reach all parts of the design with minimal skew.

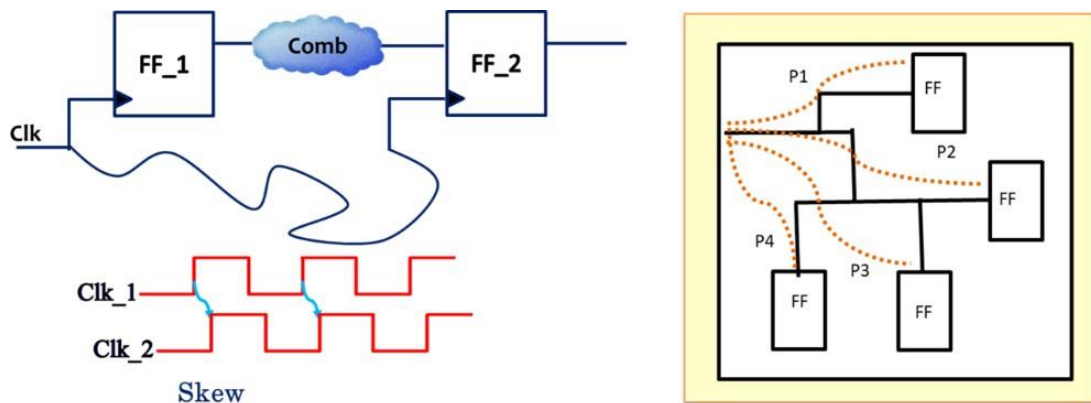


Figure 2.4 Skew Management in CTS [8].

4. **Routing:** Connecting the placed components through metal layers while adhering to design rules. This process includes global routing (defining paths) and detailed routing (precise track placement).

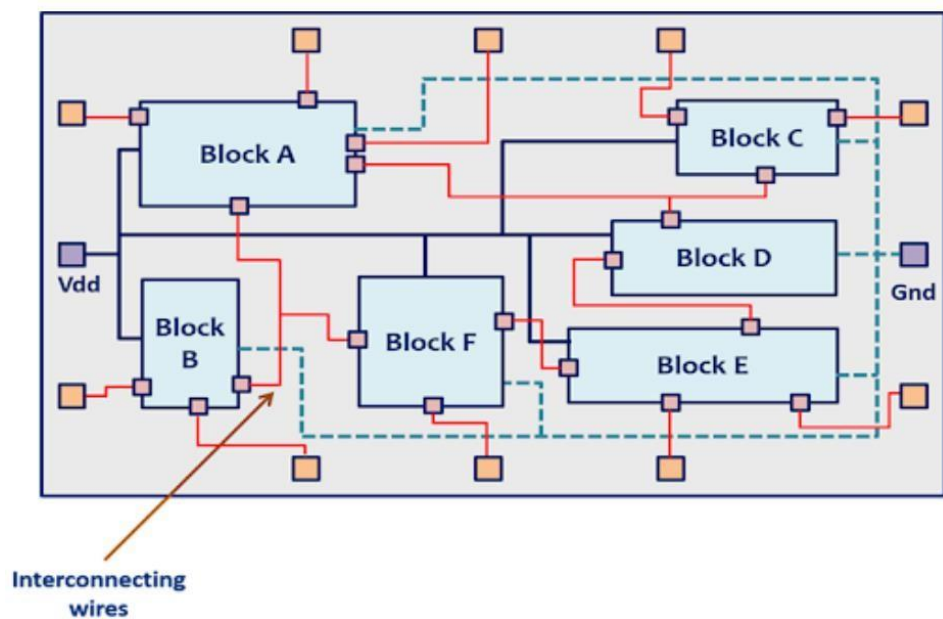


Figure 2.5 Routing [8].

5. **Design Rule Checking (DRC):** A verification step to ensure that the layout complies with the foundry's design rules.
6. **Layout Versus Schematic (LVS) Verification:** Ensuring that the layout accurately reflects the logical design specified in the netlist.
7. **Post-Layout Optimization:** Refinements made after initial routing and placement, including adjustments for timing and power integrity.

8. **Finalization and Output Generation:** Preparing the final layout for fabrication, including generating GDSII or OASIS files and completing all verification reports.

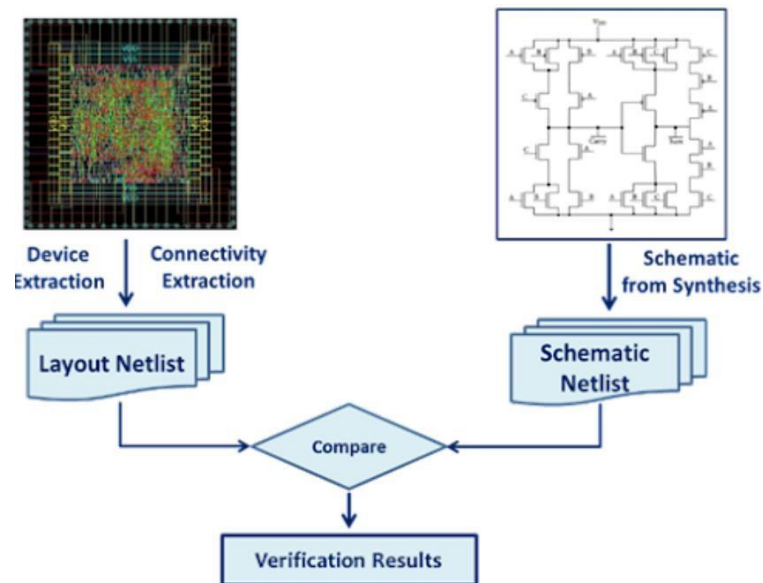


Figure 2.6 Layout Versus Schematic (LVS) [6].

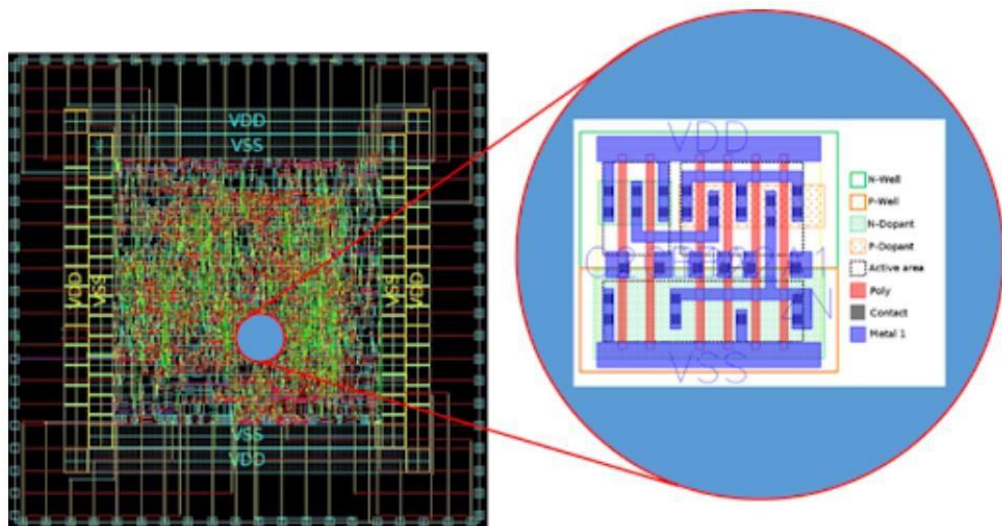


Figure 2.7 Physical Layout [8].

2.6 Physical Design Constraints

Physical design must adhere to various constraints that ensure successful fabrication and functionality:

1. **Design Rules:** Specifications defining minimum widths, spacings, and other geometric constraints essential for manufacturability.
2. **Timing Constraints:** Requirements that dictate the maximum allowable delays for signal propagation to meet performance targets.

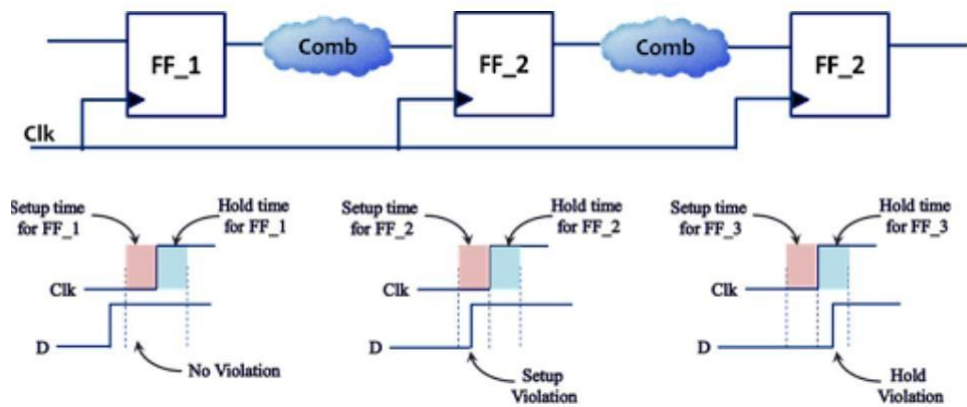


Figure 2.8 Static Timing Analysis (STA) [8].

3. **Power Integrity Constraints:** Considerations for IR drop, ground bounce, and noise margins that affect the performance and reliability of the design.
4. **Thermal Constraints:** Limits on power dissipation and temperature rise that ensure the design operates within safe thermal conditions.
5. **Area Constraints:** Restrictions on the total area used by the design to fit within a specific die size or to accommodate multiple designs on a single die.

2.7 Summary of Physical Design

The physical design stage of VLSI design is a multifaceted process that integrates various aspects of layout creation, verification, and optimization. By focusing on goals such as area efficiency, timing closure, power management, and adherence to design rules, designers can create robust and high-performance integrated circuits suitable for modern applications. As technology continues to advance, the physical design process will evolve, incorporating new techniques and methodologies to meet the challenges posed by increasingly complex designs.

CHAPTER 3

3.1 APR Flow

The Automatic Placement and Routing (APR) flow is a critical phase in the physical design stage of VLSI (Very Large Scale Integration) design. As semiconductor technology has advanced, the APR flow has become increasingly sophisticated, evolving to address the growing complexity of modern integrated circuits (ICs). The shift from micron-scale to nanometre-scale process nodes has necessitated a more automated and precise approach to the placement of standard cells and the routing of interconnections, making APR a fundamental aspect of the IC design process. The need for faster, smaller, and more power-efficient devices has driven the industry to adopt advanced APR methodologies that ensure optimal chip layout while meeting stringent performance, area, and power constraints.

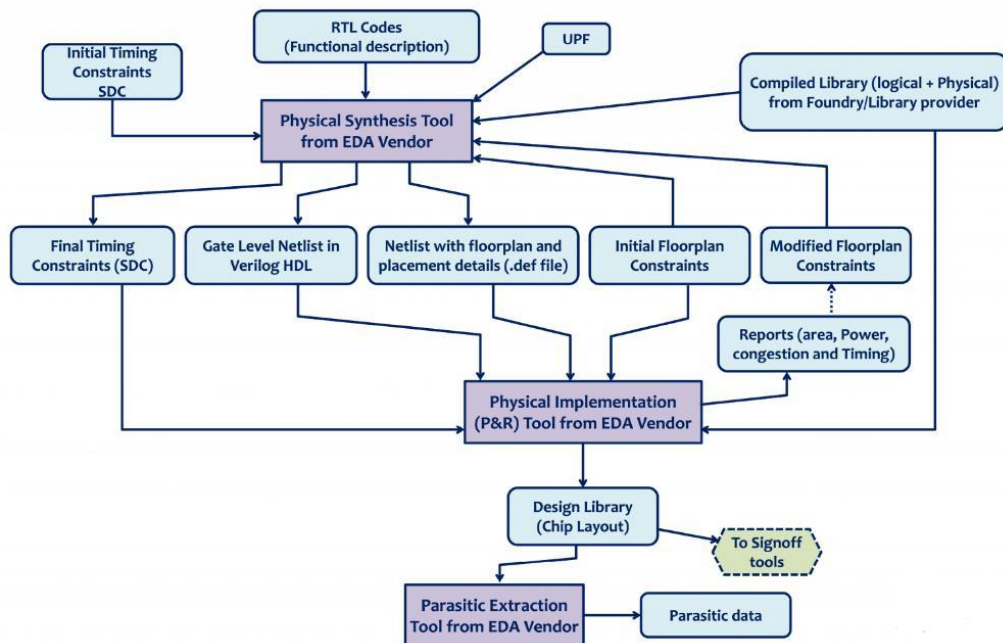


Figure 3.1 Block Diagram of APR Flow [8].

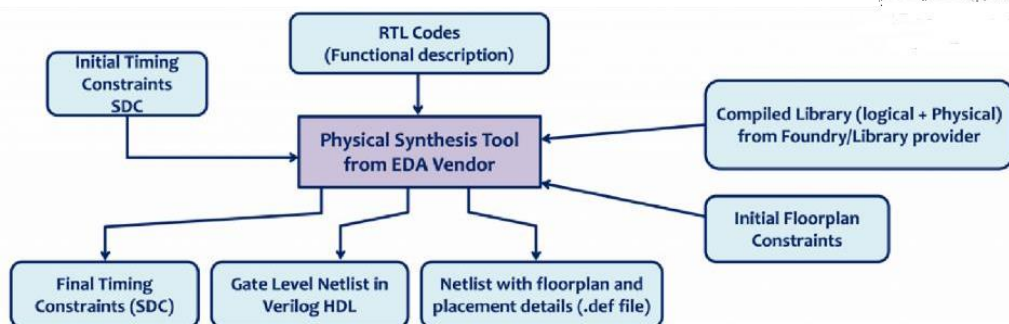


Figure 3.2 Block Diagram of Synthesis Flow [8].

3.2 APR Flow Overview

1. *Inputs (Collaterals):*

- **Technology Library:** Characterizes standard cells, including timing, area, and power models.
- **Design Netlist:** Represents the circuit design in a logical format, typically in Verilog or VHDL.
- **Floorplan:** Defines the initial placement of major blocks, helping in area allocation.
- **Constraints:** Includes timing constraints, placement constraints (e.g., blockages), and routing constraints (e.g., width, spacing).
- **Manufacturing Rules:** Design rules to ensure manufacturability, such as DRC and ERC rules.

2. *Stages in the Flow:* The APR flow consists of several stages, each with specific tasks:

A. *Pre-Placement Stage:*

- **Inputs:** Technology library, design netlist, constraints, floorplan.
- **Outputs:** Prepared design for placement.
- **Tasks:**
 - **Synthesis:** Convert RTL to a gate-level netlist.
 - **Static Timing Analysis (STA):** Evaluate timing for the design to identify critical paths.

B. *Placement Stage:*

- **Inputs:** Netlist, floorplan, timing and placement constraints.
- **Outputs:** Placed design.
- **Tasks:**
 - **Global Placement:** Place cells to minimize total wire length while meeting constraints.
 - **Detailed Placement:** Refine the initial placement to optimize timing and congestion.

C. *Routing Stage:*

- **Inputs:** Placed design, constraints.
- **Outputs:** Routed design.

- **Tasks:**
 - **Global Routing:** Determine paths for nets across the chip without detailed layer assignment.
 - **Detailed Routing:** Assign specific layers and vias to the determined paths, ensuring all design rules are met.

D. Post-Route Optimization:

- **Inputs:** Routed design.
- **Outputs:** Final layout.
- **Tasks:**
 - **Timing Closure:** Ensure all timing constraints are met.
 - **DRC and ERC Checks:** Validate that the design adheres to manufacturing rules.

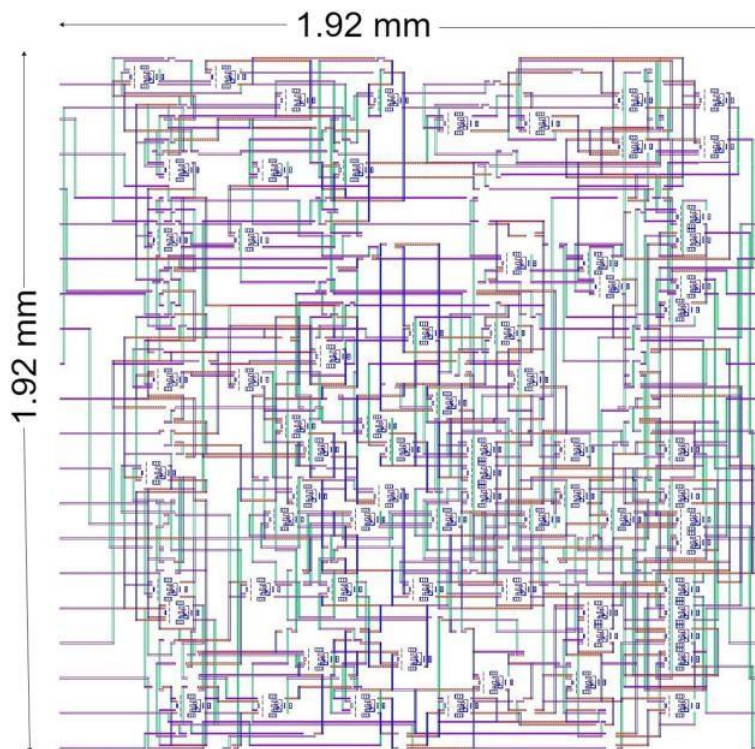


Figure 3.3 Automatically placed and routed layout of 4-b ALU. Only the wiring layers M2, M3, M5, and M6 are shown to illustrate the wire routing in design [10].

3.3 Outputs of the APR Flow

- **GDSII Layout:** The final physical representation of the design for fabrication.
- **Timing Reports:** Reports detailing the timing performance of the design.
- **DRC/ERC Reports:** Documentation of any design rule violations.

3.4 Features Used in APR Flow

The Features generally observed in the APR Flow are detailed below:

1. *FDR (Functional Design Restructuring)*

- **Characteristics:** FDR focuses on restructuring the functional aspects of a design to improve performance metrics such as timing, area, and power consumption.
- **Stage:** Primarily used during the **Placement** and **Routing** stages.
- **Uses:**
 - Adjusts the design's architecture for optimal cell placement and connectivity.
 - Enhances timing closure by reorganizing critical paths and adjusting the location of cells to reduce delays.

2. *MSCTS (Multi-Segment Clock Tree Synthesis)*

- **Characteristics:** MSCTS provides an efficient method for synthesizing clock trees that minimizes clock skew while ensuring balanced load distribution.
- **Stage:** Utilized in the **Post-Placement** stage.
- **Uses:**
 - Constructs a clock tree that ensures minimal clock skew across all components.
 - Optimizes the clock distribution network, which is critical for timing integrity in synchronous designs.

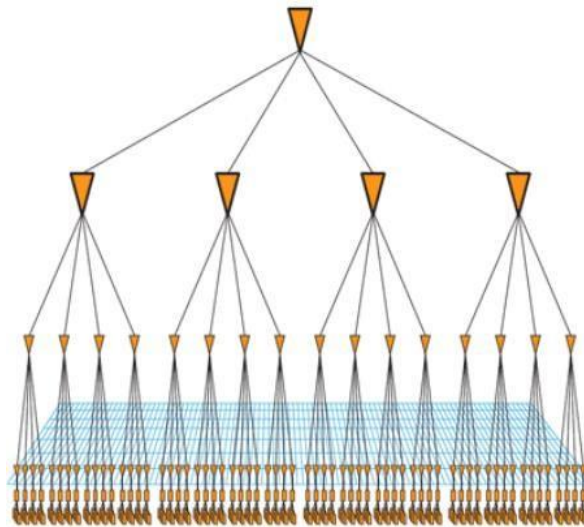


Figure 3.4 Multi-Segment Clock Tree Synthesis [10].

3. *Flextree*

- **Characteristics:** Flextree is a flexible methodology for generating clock trees that can adapt to various design requirements and constraints.

- **Stage:** Implemented during the **Clock Tree Synthesis** phase.
- **Uses:**
 - Provides designers with the ability to fine-tune the clock distribution for performance and manufacturability.
 - Supports various clock tree topologies, allowing for optimization based on specific design needs.

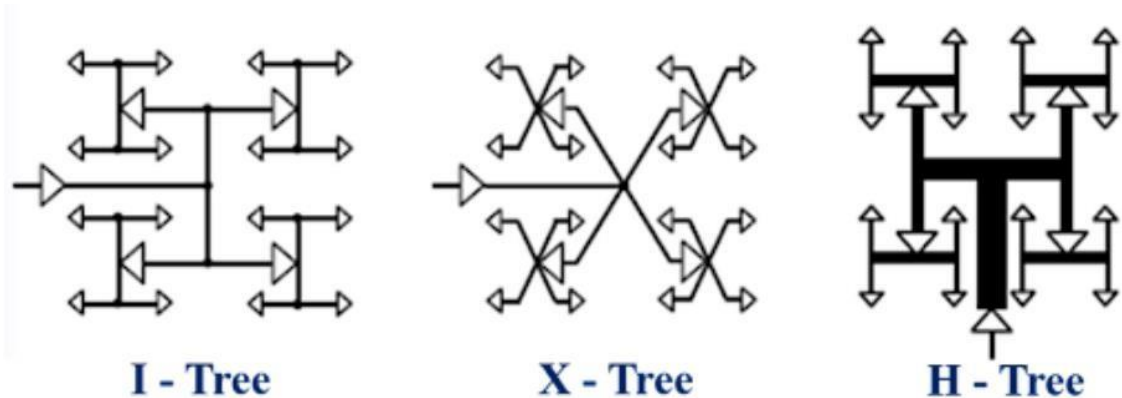


Figure 3.5 Various Types of Clock Trees [10].

4. Priority Routing

- **Characteristics:** This feature prioritizes the routing of critical nets over less critical ones to ensure that timing-sensitive signals are routed first.
- **Stage:** Primarily applied during the **Routing** stage.
- **Uses:**
 - Ensures that timing-critical paths receive routing resources ahead of non-critical paths, improving overall timing performance.
 - Helps in avoiding congestion in areas where critical signals are routed.

5. VISA (Virtual Initial Signal Architecture)

- **Characteristics:** This feature provides a framework for managing the initial signal architecture of the design, allowing for better organization of signal paths and connections.
- **Stage:** Used during the **Pre-Placement** and **Routing** stages.
- **Uses:**
 - Facilitates the creation of a virtual representation of signal paths, helping designers visualize and optimize signal integrity and performance.

- Assists in establishing a preliminary routing plan, identifying potential congestion areas, and ensuring that critical signals are prioritized during the routing phase.

6. Mixed Placer

- **Characteristics:** The Mixed Placer combines various placement algorithms, utilizing both analytical and simulated annealing techniques for optimal results.
- **Stage:** Applied during the **Placement** stage.
- **Uses:**
 - Balances trade-offs between area and timing by leveraging different strategies for placement optimization.
 - Enhances the overall efficiency of the placement process, leading to better performance outcomes.

7. Xreplay

- **Characteristics:** Xreplay enables the replay of previous placement and routing iterations to refine designs based on historical data.
- **Stage:** Used during the **Placement** and **Routing** stages.
- **Uses:**
 - Facilitates incremental changes and optimizations, allowing designers to leverage prior knowledge.
 - Helps in quickly converging on optimal solutions by reusing successful configurations.

8. IR Aware Placement

- **Characteristics:** This feature considers the impact of IR drop (voltage drop due to current flow) during the placement phase to ensure robust power delivery.
- **Stage:** Implemented during the **Placement** stage.
- **Uses:**
 - Ensures that critical components are placed in a manner that minimizes IR drop and maintains signal integrity.
 - Helps achieve better power distribution across the design, critical for performance and reliability.

9. Spare Cell Insertion

- **Characteristics:** This feature adds spare cells to the design, which can be used for redundancy or to improve yield.

- **Stage:** Applied during the **Post-Routing** stage.
- **Uses:**
 - Enhances the robustness of the design by providing redundancy in case of manufacturing defects.
 - Improves overall yield by ensuring that the design can tolerate defects without functional loss.

10. CSI (Clock Switched Interconnect)

- **Characteristics:** CSI optimizes clock signals by managing how and when clock signals are switched throughout the design.
- **Stage:** Utilized in the **Post-Placement** and **Routing** stages.
- **Uses:**
 - Ensures effective clock distribution while minimizing power consumption and noise.
 - Enhances the integrity of clock signals in large designs.

11. SDP (Standard Cell Design Process)

- **Characteristics:** SDP streamlines the design of standard cells for efficiency and reuse, focusing on both performance and manufacturability.
- **Stage:** Applied during the **Design Implementation** stage.
- **Uses:**
 - Accelerates the design process by leveraging reusable cell libraries.
 - Facilitates a consistent approach to cell design, enhancing overall productivity.

12. SER (Single Event Upset Recovery)

- **Characteristics:** SER mitigates the effects of single event upsets (SEUs) that can occur in digital circuits due to external radiation or other factors.
- **Stage:** Primarily used during the **Post-Routing** stage.
- **Uses:**
 - Ensures reliability in critical applications, especially in aerospace or medical devices where resilience to SEUs is crucial.
 - Implements redundancy and error correction mechanisms to recover from upsets.

The features of the APR flow are designed to address specific challenges encountered in VLSI design, enhancing performance, manufacturability, and reliability. Understanding these features allows designers to effectively utilize them within the APR flow, leading to high-quality designs that meet stringent industry standards.

3.5 Role of APR in Modern VLSI Design

The APR flow plays a pivotal role in achieving design closure in modern VLSI design, especially as process nodes reach advanced stages like 5nm and beyond. Automated APR tools ensure that placement and routing are performed with high precision, minimizing parasitic effects and optimizing the overall performance of the chip. The integration of power-aware algorithms in APR tools allows designers to incorporate low-power design techniques, such as multi-voltage domains, power gating, and clock gating, directly into the physical design process.

Moreover, APR flows are essential for managing the power distribution network (PDN) and implementing advanced power management strategies, such as power switch stitching. Techniques like the daisy chain methodology for power switch stitching can be effectively integrated into the APR flow, allowing for seamless power gating and improved power control. These capabilities have become increasingly important as modern designs require complex power management to meet power budgets and thermal constraints without sacrificing performance.

3.6 Summary

The APR flow has become a cornerstone of the physical design process in VLSI, enabling the efficient and precise implementation of complex ICs. With the increasing demands for smaller, faster, and more power-efficient devices, APR tools and methodologies have evolved to address the challenges of modern semiconductor design. This report focuses on the role of APR flow in integrating advanced power management strategies, such as power switch stitching using daisy chain methodology, to achieve reliable and efficient power delivery in contemporary VLSI designs. Through a detailed exploration of the APR flow and its impact on power management, we aim to provide insights into the critical aspects of achieving design closure in the context of power-sensitive integrated circuits.

CHAPTER 4

4.1 Unified Power Format (UPF)

The Unified Power Format (UPF) is an industry-standard format used to define and manage the power intent of digital designs. It provides a means for designers to specify how power is controlled within a chip, enabling efficient power management throughout various stages of the design flow, from RTL to final implementation. The UPF standard is particularly valuable in modern low-power design, where multiple power domains, power gating, and other power-saving techniques are essential for meeting power consumption targets.

UPF helps address the complexities of implementing these low-power strategies by creating a consistent power specification that can be applied across different Electronic Design Automation (EDA) tools, such as Cadence Genus for synthesis and Cadence Innovus for physical design. By abstracting power intent from the design description, UPF allows for flexibility in adjusting power strategies without needing to modify the core RTL design.

4.2 Constraints Considered for Writing a UPF

Writing a UPF file involves considering various constraints to ensure that the power intent aligns with the design requirements and the capabilities of the physical design tools. These constraints include:

1. **Power Domains:** Specifying the different power domains, which represent regions of the design that can be powered on or off independently.
2. **Voltage Levels:** Defining the operational voltage ranges for each power domain to support voltage scaling and dynamic voltage control.
3. **Power Switch Constraints:** Including details about power switches that control the connection between power supplies and different power domains.
4. **Isolation Requirements:** Constraints for isolation cells, which are required to prevent data corruption when interfacing between powered and non-powered domains.
5. **Retention Requirements:** Defining retention cells and their requirements, such as which registers should retain state when a domain is powered down.
6. **Timing Constraints:** Ensuring that timing analysis is accurate for different power states, including power-on and power-off sequences.
7. **Clock and Reset Requirements:** Managing clock gating and reset strategies for power-down and power-up events.

8. ***IR Drop and EM Constraints***: Ensuring that power grid specifications and switch placement meet IR drop and electromigration limits.

These constraints help ensure that the UPF file is compatible with both the logical and physical aspects of the design, allowing the design tools to implement power management strategies accurately.

4.3 Elements in UPF File

A typical UPF file contains definitions for various elements that describe the power management strategies of a design. Key aspects include:

1. ***Power Domains***: Each power domain is a region of the design that can be independently powered on or off. A UPF file describes these domains and their relationships with other domains.
2. ***Power Switches***: UPF specifies the power switches that control the supply to different power domains, enabling the implementation of power gating.
3. ***Level Shifters***: These components are described to handle signal transitions between power domains operating at different voltage levels.
4. ***Isolation Cells***: Isolation logic is defined to prevent signal corruption when one power domain is turned off while another remains active.
5. ***Retention Registers***: Retention cells are used to save the state of registers when a power domain is powered down, ensuring that state can be restored upon power-up.
6. ***Supply Sets***: These include definitions of primary and secondary power supplies, specifying the voltage values for each power domain.
7. ***Switch Control Logic***: Descriptions of the control signals for power switches, including power-up and power-down sequences.
8. ***Power Management States***: UPF allows designers to specify different power states and sequences that the design can transition through during operation.
9. ***Clocks and Resets***: Definitions for how clocks and resets are managed across different power states and domains.
10. ***Dynamic Voltage Frequency Scaling (DVFS)***: UPF may include information on how voltage levels can be adjusted dynamically based on workload or performance requirements.

4.4 General Pattern of a UPF Script

A UPF script follows a structured format to describe the power intent of a design. The general pattern includes:

1. Creating Power Domains:

Upf command style:

```
create_power_domain PD1 -elements {u_block1}  
create_power_domain PD2 -elements {u_block2}
```

2. Defining Supply Nets and Sets:

Upf command style:

```
create_supply_net VDD1  
create_supply_set VDD1_set -primary VDD1
```

3. Specifying Power Switches:

Upf command style:

```
create_power_switch PS1 -domain PD1 -in_supply VDD -out_supply VDD1
```

4. Adding Isolation and Retention Cells:

Upf command style:

```
set_isolation ISOL1 -from PD1 -to PD2 -isolation_signal ISO_signal  
set_retention R1 -domain PD1 -retention_register u_reg1
```

5. Defining Level Shifters:

Upf command style:

```
set_level_shifter LS1 -from PD1 -to PD2 -direction bidirectional
```

6. Describing Power States:

Upf command style:

```
create_power_state ACTIVE -domain PD1 -state {ON}  
create_power_state SLEEP -domain PD1 -state {OFF}
```

7. *Power-up and Power-down Sequences:*

Upf command style:

```
set_power_switch_on_sequence PS1 {power_on_signal}
set_power_switch_off_sequence PS1 {power_off_signal}
```

This pattern helps create a comprehensive view of power management strategies and enables EDA tools to interpret and apply these strategies during synthesis and implementation.

4.5 Stages of Design Where UPF is Used

UPF files play a critical role across multiple stages of the design flow, including:

1. **RTL Design Stage:** During RTL design, the UPF file helps simulate different power states and validate low-power behaviours.
2. **Synthesis Stage:** UPF is used during synthesis to ensure that power-aware components, such as isolation cells and level shifters, are correctly inserted.
3. **Floorplanning and Power Planning:** In physical design tools like Cadence Innovus, UPF guides the placement of power domains, switches, and routing of power and ground networks.
4. **Static Timing Analysis (STA):** UPF aids in analysing timing across different power states, ensuring that timing constraints are met when domains are powered on or off.
5. **Verification Stage:** UPF allows for verification of power-up, power-down sequences, and transitions between different power states using simulation.
6. **Power Analysis:** During sign-off, UPF is essential for performing power analysis to validate power consumption, IR drop, and power integrity.

4.6 Goal of the UPF Script

The primary goal of a UPF script is to define the power intent of a design in a standardized manner that can be applied throughout the design flow. This enables designers to:

- Manage power consumption effectively by implementing power gating, DVFS, and other low-power techniques.
- Maintain design integrity across different power states, ensuring data retention and signal isolation.
- Achieve consistency in low-power design intent across various stages, from simulation to physical implementation and verification.
- Facilitate communication of power management strategies between design teams and across EDA tools, improving design efficiency and reducing power-related bugs.

By clearly defining power domains, power switches, and their interactions, the UPF file ensures that the chip's power management architecture meets performance goals while optimizing power efficiency.

CHAPTER 5

5.1 Power Planning Stage

The power planning stage is a critical part of the Automatic Placement and Routing (APR) flow, is aimed at ensuring that the design meets its power delivery requirements while maintaining power integrity across the entire chip. In APR flow, this process is executed primarily using the *Innovus* tool, which handles various stages of physical implementation, such as floorplanning, clock tree synthesis (CTS), routing, and power planning. Power planning is vital because it defines the physical structure for power distribution throughout the design, managing power to different regions and domains of the chip. It ensures that the circuit components receive stable power supply with minimal voltage drops, avoiding issues like IR drop and electromigration.

The power planning process involves defining and placing power-related structures such as power rings, stripes, and grids, and managing power switches for effective power gating. These structures ensure that the power is distributed uniformly, minimizing hotspots and maintaining signal integrity across all operating conditions. A well-implemented power plan is key to meeting the design's power performance and reliability requirements.

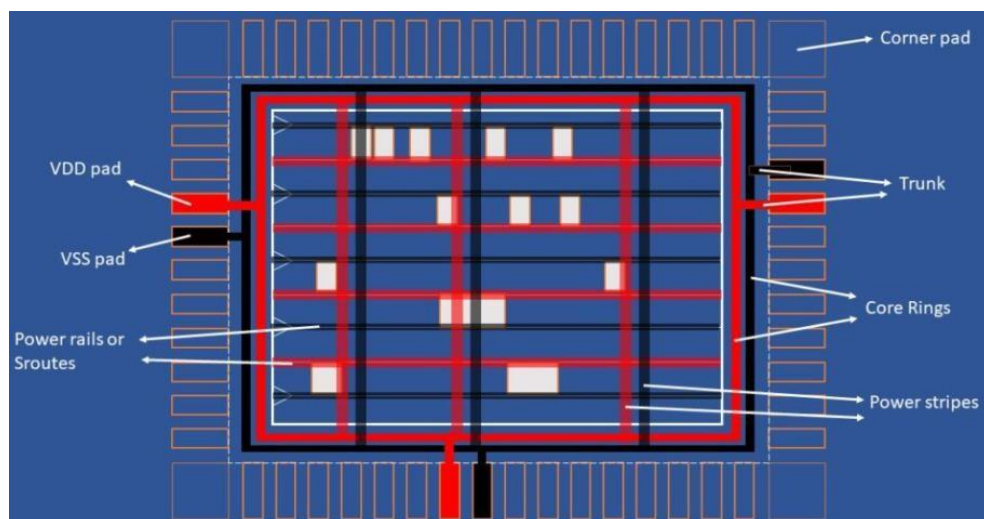


Figure 5.1 Power Planning Stage [10].

5.2 Goals of Power Planning

The primary objectives of the power planning stage are:

1. **Stable Power Delivery:** Ensuring that all regions of the chip receive a stable power supply, minimizing voltage drop (IR drop) and power noise.
2. **Managing Power Distribution:** Creating an effective network of power rails, rings, and stripes to deliver power uniformly across different power domains.

3. **Optimizing Area and Routing Resources:** Balancing power structures like power rings and grids while optimizing area usage and minimizing congestion in routing layers.
4. **Support for Power Gating:** Managing power switches effectively to enable power gating, reducing leakage power when certain parts of the chip are not in use.
5. **Ensuring Design Integrity:** Minimizing risks of electromigration and thermal issues, ensuring reliable operation over the lifetime of the chip.
6. **Compliance with Power Intent:** Adhering to the power intent defined in the Unified Power Format (UPF) file, ensuring proper power domain isolation and control.

5.3 Inputs of Power Planning Stage

The inputs required for the power planning stage include:

1. **UPF (Unified Power Format) File:** Defines the power intent, including power domains, power switches, isolation cells, and retention strategies.
2. **Floorplan Details:** Information about the placement of blocks, cell boundaries, and the initial floorplan from which power distribution needs to be built.
3. **Design Netlist:** The logic description of the circuit, including its hierarchical structure, which helps in identifying the power needs of different regions.
4. **Technology Files:** Process Design Kit (PDK) and technology libraries containing details like metal layers, routing rules, and resistance/capacitance values.
5. **Power Requirements:** Specifications such as target IR drop, electromigration limits, and operating voltage values for different power domains.
6. **Power Grid Constraints:** Predefined constraints related to the width, spacing, and layers for power and ground (PG) grids.

5.4 Outputs of Power Planning Stage

The outputs of the power planning stage include:

1. **Power Grid Structure:** A complete power grid consisting of power rings, power stripes, and power meshes for uniform power delivery.
2. **Power Switch Placement:** Locations and connections of power switches for power gating.
3. **Voltage Area Definition:** Defined voltage areas or power domains as specified in the UPF, demarcated in the physical layout.
4. **IR Drop Analysis Reports:** Analysis results highlighting areas with potential voltage drops, which can be optimized further.

5. ***Electromigration Analysis Reports:*** Verification of the power grid's ability to handle current density requirements without causing damage.
6. ***Design Updates:*** Modifications to the design netlist or floorplan based on the physical power plan, such as adjustments in block placement for better power distribution.

5.5 Detailed Power Planning Process

The power planning process involves several critical steps, ensuring a comprehensive and effective power distribution network across the chip:

1. *Initial Floorplan Assessment:*

- Analyse the initial floorplan to understand the placement of macros and standard cells.
- Identify the location of power domains based on the UPF file.

2. *Power Ring Creation:*

- Create power rings around macros or blocks to provide localized power delivery.
- Typically done for higher current demand areas like large memory blocks.

3. *Power Stripe Definition:*

- Add power stripes across the chip to ensure even power distribution.
- Define the number, width, and spacing of power stripes based on current demand and power domain requirements.

4. *Power Mesh Formation:*

- Build power meshes to connect power rings and stripes across different layers, creating a comprehensive power delivery network.
- Ensure that power meshes are balanced across different routing layers for minimal IR drop.

5. *Power Switch Placement:*

- Place power switches according to the power gating strategy defined in the UPF.
- Ensure optimal placement to control power transitions between on and off states effectively.

6. *Power Grid Analysis:*

- Run IR drop analysis to ensure minimal voltage drops across the grid.
- Perform electromigration analysis to verify that the grid can handle the required current density.

7. **Optimization:**

- Adjust the placement and density of power structures to address any identified issues in power delivery.
- Iteratively refine the power grid to meet design constraints and ensure efficient power distribution.

8. **Verification and Sign-Off:**

- Perform final checks and validation against design specifications.
- Generate the final power plan database, ensuring it aligns with the UPF and other design requirements.

5.6 Power Planning Constraints

The following constraints are typically considered during power planning to ensure effective and reliable power distribution:

1. **IR Drop Limits:** Maximum permissible voltage drop across the power grid to ensure stable operation.
2. **Electromigration (EM) Limits:** Current density limits to prevent damage to the metal layers due to high currents.
3. **Power Ring and Stripe Width:** The required width of power rings and stripes based on current demand.
4. **Power Mesh Layer Usage:** Specification of the layers to be used for power routing to balance routing resources.
5. **Current Demand of Power Domains:** Estimated current needs for different power domains, affecting the density of power stripes.
6. **Minimum and Maximum Spacing:** Constraints on spacing between power rails and stripes to avoid short circuits and ensure proper routing.
7. **Voltage Area Boundaries:** Boundaries for each voltage area defined by the UPF file, ensuring proper isolation of power domains.
8. **Power Switch Characteristics:** Specifications for power switch types, sizes, and control signals for power gating.

5.7 Types of Power Planning

In VLSI design, power planning can be broadly categorized based on different methodologies and techniques, each targeting specific aspects of power distribution and management within the design. Here are the main types of power planning used in semiconductor design:

1. Static Power Planning

- ***Focus:*** Design a robust power delivery network that ensures a steady and continuous supply of power to all parts of the chip.
- ***Key Structures:*** Power rings, power stripes, power grids, and meshes.
- ***Purpose:*** To ensure that all components receive power with minimal voltage drop (**IR drop**) and stable operation under various load conditions.
- ***Applications:*** General ASIC designs, where power delivery is relatively uniform across different regions of the chip.

2. Dynamic Power Planning

- ***Focus:*** Design a power delivery network that can adapt to changing power requirements during different modes of operation.
- ***Key Techniques:*** Power gating, dynamic voltage and frequency scaling (**DVFS**).
- ***Purpose:*** To reduce power consumption during idle or low-activity states, allowing certain sections of the chip to be turned off or operate at lower voltages.
- ***Applications:*** Mobile devices, low-power designs, and high-performance computing where power efficiency is critical.

3. Hierarchical Power Planning

- ***Focus:*** A top-down approach for multi-level power planning in hierarchical designs, often involving multiple modules or blocks with different power domains.
- ***Key Structures:*** Power islands, voltage areas, hierarchical power grids.
- ***Purpose:*** To manage power delivery for complex designs with multiple functional blocks, each potentially requiring different power levels.
- ***Applications:*** SoCs (System-on-Chips) and designs with distinct modules that may operate at different power and voltage levels.

4. Power Gating and Isolation-Based Power Planning

- ***Focus:*** Integrate power switches and isolation cells to control power flow to different parts of the design, allowing specific areas to be powered down when not in use.
- ***Key Components:*** Power switches, isolation cells, retention cells.
- ***Purpose:*** To reduce leakage power by completely powering off sections of the chip when they are inactive.
- ***Applications:*** Battery-operated devices, IoT devices, and any design where leakage power needs to be minimized.

5. Distributed Power Planning

- **Focus:** Distribute power delivery through multiple smaller power sources or regulators rather than relying on a central power supply.
- **Key Techniques:** Decentralized voltage regulators, distributed power grids.
- **Purpose:** To reduce the burden on a single power source and minimize IR drop by delivering power more locally to high-demand areas.
- **Applications:** High-performance processors and systems where load balancing and localized power delivery are crucial.

6. Low Dropout Regulator (LDO)-Based Power Planning

- **Focus:** Use on-chip Low Dropout Regulators (**LDOs**) for precise voltage control within the power delivery network.
- **Key Components:** LDO regulators, on-chip power management units (**PMUs**).
- **Purpose:** To provide fine-grained control over voltage levels within specific power domains, often for analog circuits or mixed-signal designs.
- **Applications:** Analog/mixed-signal ICs and SoCs where precise voltage control is needed.

7. On-Chip Power Delivery Network (PDN) Planning

- **Focus:** Optimize the on-chip power delivery network to ensure minimal power loss and efficient routing of power.
- **Key Structures:** On-chip decoupling capacitors, optimized power grid layouts.
- **Purpose:** To mitigate issues like IR drop and voltage fluctuations using decoupling strategies.
- **Applications:** High-speed digital designs, RF chips, and any design where maintaining signal integrity is critical.

8. Decoupling Capacitor-Based Power Planning

- **Focus:** Incorporate decoupling capacitors into the power plan to stabilize power supply and mitigate noise.
- **Key Components:** On-chip and off-chip decoupling capacitors.
- **Purpose:** To maintain steady voltage levels during transient switching activity and reduce power supply noise.
- **Applications:** High-speed logic designs, memory subsystems, and RF circuits where noise sensitivity is high.

5.8 Summary of Power Planning Types

Table 5.1 Comparison of Power Planning Types.

Type	Focus	Key Techniques / Structures	Applications
Static Power Planning	Steady power supply	Power rings, stripes, grids	General ASIC designs
Dynamic Power Planning	Adapting to changing power requirements	Power gating, DVFS	Mobile devices, low-power designs
Hierarchical Power Planning	Managing power in multi-level designs	Power islands, voltage areas	SoCs, complex multi-block designs
Power Gating and Isolation-Based	Powering down inactive sections	Power switches, isolation cells	Battery-operated devices, low-leakage designs
Distributed Power Planning	Decentralized power delivery	Distributed voltage regulators, localized grids	High-performance processors, load-balanced systems
LDO-Based Power Planning	Precise on-chip voltage control	LDO regulators, PMUs	Analog/mixed-signal ICs
On-Chip PDN Planning	Optimize on-chip power delivery	Decoupling capacitors, optimized power grids	High-speed digital designs, RF chips
Decoupling Capacitor-Based Power Planning	Stabilize power supply with capacitors	On-chip/off-chip decoupling capacitors	High-speed logic, memory subsystems

Each type of power planning addresses specific challenges in power delivery, allowing designers to tailor the power plan according to the requirements of their design and application. This ensures optimal power efficiency, signal integrity, and reliability in complex semiconductor devices.

CHAPTER 6

6.1 Power Domains and Power Switches

In VLSI design, power domains are regions of a chip that operate at different voltage levels or can be powered down independently. This technique is integral to low-power design, allowing for selective activation or deactivation of various sections of the circuit depending on the required performance. By managing power consumption in this way, designers can optimize for both energy efficiency and performance, making power domains especially important in modern mobile and battery-powered devices.

Power switches are crucial components in VLSI design, enabling efficient management of power consumption within integrated circuits (ICs). They act as gatekeepers, connecting or disconnecting power to different sections of a chip, thereby allowing certain areas to be powered down while others remain active. Power switches are fundamental in implementing low-power techniques, especially in designs involving power gating, multiple voltage (MV) domains, or dynamic voltage and frequency scaling (DVFS). By controlling when specific regions of a chip receive power, power switches help minimize leakage currents and optimize power efficiency in modern systems-on-chip (SoCs).

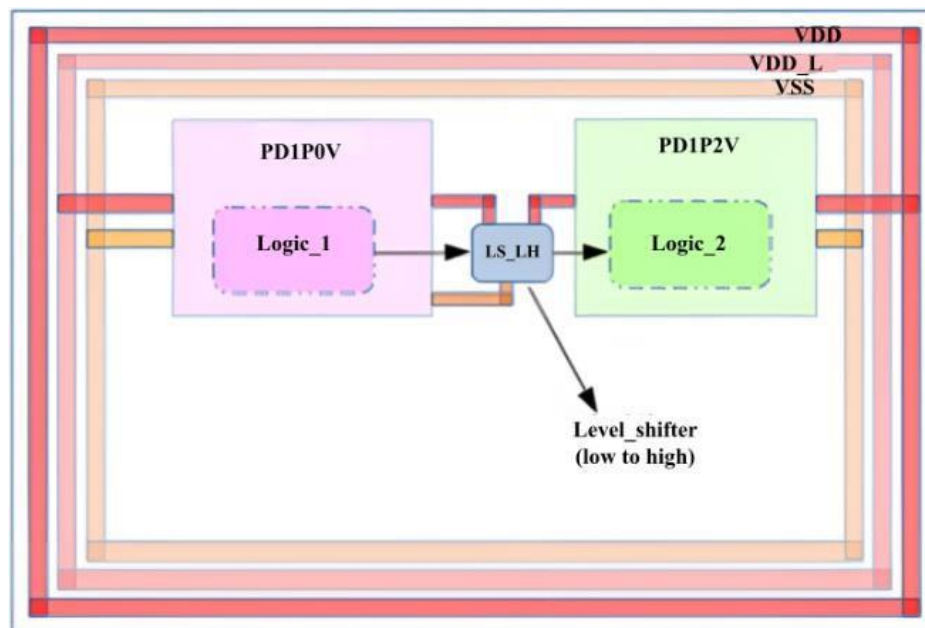


Figure 6.1 A Partition with Multiple Power Domains [10].

6.2 Types of Power Domains

1. Always-On Domains:

- **Features:** Remain powered throughout the chip's operation, maintaining critical functions like wake-up circuits, timers, or memory elements.
- **Usage:** Used for components that must remain active, even when other parts of the chip are powered down.

- **Merits:** Provides uninterrupted operation for critical functions.
- **Demerits:** Higher power consumption as this domain is never powered down.
- **Constraints:** Requires careful consideration of leakage currents and thermal dissipation.

2. Switched Power Domains:

- **Features:** Can be turned off during periods of inactivity to save power.
- **Usage:** Typically used for parts of a chip that are not required continuously, such as specific processing cores or peripheral interfaces.
- **Merits:** Allows significant power savings by reducing leakage currents when sections of the chip are idle.
- **Demerits:** Powering on and off can create challenges in terms of data retention and timing synchronization.
- **Constraints:** Requires retention registers and isolation cells to maintain data integrity when the domain is powered down.

3. Multiple Voltage Domains (MV) / Dynamic Voltage and Frequency Scaling (DVFS) Domains:

- **Features:** Operate at different voltage levels and may dynamically adjust based on performance needs.
- **Usage:** Commonly used in processors and graphic chips where some sections run at lower voltages to save power, while others operate at higher voltages for performance.
- **Merits:** Balances power and performance by adjusting voltage levels dynamically.
- **Demerits:** Requires complex design and verification, including handling level shifters.
- **Constraints:** Must manage voltage level compatibility between domains to ensure proper data communication.

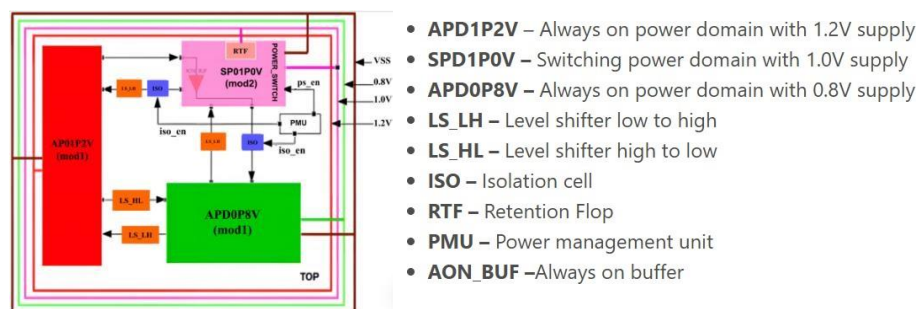


Figure 6.2 Different Types of Power Domains and Modules related to Power Supply and Management [12].

6.3 Types of Power Switches

1. *Header Switches:*

- **Features:** Positioned between the power source (**VDD**) and the circuit block. When turned off, they cut off the power supply to the block, allowing it to be powered down.
- **Usage:** Commonly used in high-performance blocks to reduce leakage power during idle states.
- **Merits:** Effective in reducing leakage current by cutting off the power supply.
- **Demerits:** Requires careful sizing, as the current supplied through the header switch must be sufficient to meet the needs of the active block. Larger switches can lead to increased area and on-resistance.
- **Constraints:** Design must consider the voltage drop across the switch and ensure that the on-state resistance does not degrade performance during active operation.

2. *Footer Switches:*

- **Features:** Positioned between the ground (**GND**) and the circuit block, controlling the connection to ground.
- **Usage:** Often used in circuits where controlling the ground path provides better power isolation.
- **Merits:** Simpler control logic, as they isolate the ground path and can be more stable in certain design scenarios.
- **Demerits:** Similar to header switches, they can create a voltage drop that affects circuit performance, and larger switches occupy more silicon area.
- **Constraints:** Must ensure that the ground bounce and the impact on the ground plane are managed, especially during switching events.

3. *Integrated Power Switches (IPS):*

- **Features:** Integrate multiple smaller switches in parallel, turning them on or off as needed to manage power.
- **Usage:** Utilized in scenarios where fine-grained control over power gating is needed, such as in MV or DVFS domains.
- **Merits:** Provides flexibility in controlling power based on the activity level of the circuit, enabling dynamic power control.
- **Demerits:** More complex control logic and layout considerations, as multiple switches must be managed together.
- **Constraints:** Control circuit design is critical, ensuring that switches are turned on and off in a coordinated manner to prevent large inrush currents.

6.4 Creation of Power Domains in APR Flow

In the Automatic Place and Route (APR) flow, creating power domains is a crucial part of the power planning stage. This process is carried out using EDA tools like Cadence Innovus, and it involves defining the regions on the chip that will operate under different power conditions.

1. *Inputs Required for Power Domain Creation:*

- ***Unified Power Format (UPF) or Common Power Format (CPF):*** Describes power intent, including the definitions of power domains, isolation strategies, and level shifters.
- ***Design Netlist:*** The structural representation of the logic elements and connections in the chip.
- ***Floorplan:*** Layout of the blocks, including the physical constraints and location of power rails.
- ***Power Specifications:*** Details like voltage levels, power switch placement, and constraints for each domain.

2. *Outputs Obtained After Power Domain Creation:*

- ***Power Grid Layout:*** The arrangement of power rails and connections that supply power to each domain.
- ***Power Domain Boundary Information:*** Defines the boundaries of each power domain and the location of isolation cells, level shifters, and power switches.
- ***Power Intent Reports:*** Verifies the correct placement of power domains, retention cells, and other power management structures.
- ***Timing Analysis Data:*** Ensures that timing integrity is maintained across power domains with varied voltage levels.

3. *Detailed Steps for Power Domain Creation Process:*

- ***Step 1: Define Power Domains in UPF/CPF:*** Specify the power domains, their hierarchy, and the power supply nets using UPF or CPF.
- ***Step 2: Insert Isolation Cells:*** Isolation cells are added to maintain logic values when a domain is powered down.
- ***Step 3: Insert Retention Cells:*** These cells are placed in regions where state retention is required during power-down.
- ***Step 4: Define Level Shifters:*** Level shifters are placed between domains operating at different voltage levels to ensure signal integrity.
- ***Step 5: Place Power Switches:*** Define and place power switches that control the power to each switched domain.

- **Step 6: Implement Power Grid:** Design a power grid for each domain, ensuring that the power distribution is efficient and meets the required current demands.
- **Step 7: Verify Power Intent:** Use power verification tools to ensure that the power domains, isolation strategies, and power switches are correctly implemented.
- **Step 8: Timing and Power Analysis:** Ensure that the integration of power domains maintains timing integrity and meets the power consumption targets.

4. Constraints of Power Domain Creation:

- **Voltage Compatibility:** Managing different voltage levels across domains to ensure data integrity.
- **IR Drop and EM:** Ensuring minimal IR drop and managing electromigration in the power grid to maintain reliable power delivery.
- **Area Constraints:** Optimizing the placement of power-related cells (e.g., retention registers, isolation cells) to avoid area overhead.
- **Switching Noise Management:** Avoiding simultaneous switching noise that could impact circuit stability during power transitions.
- **Thermal Management:** Ensuring that the heat generated by power switches and high-current domains is managed to prevent thermal hotspots.

By integrating power domains effectively within the APR flow, modern VLSI designs can achieve significant power savings while maintaining high performance. The careful design and verification of these domains ensure that chips meet stringent power and performance specifications, making power domains a cornerstone of low-power IC design.

6.5 Power Switch Creation in APR Flow

In the Automatic Place and Route (APR) flow, power switch creation is part of the power planning stage. Tools like Cadence Innovus facilitate the integration of power switches, which involves specifying their placement and control logic to ensure efficient power gating in the design.

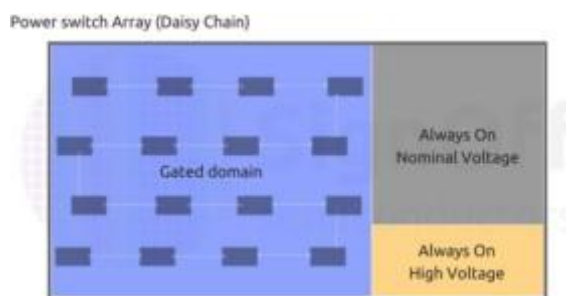


Figure 6.3 Power Switches in a Power Domain integrated using Daisy Chain Topology [13].

1. ***Inputs Required for Power Switch Creation:***

- ***Unified Power Format (UPF) or Common Power Format (CPF):*** Defines the power intent, specifying the power domains, power switches, and their control signals.
- ***Design Netlist:*** The structural representation of the design that includes logic cells and connectivity.
- ***Floorplan:*** Specifies the physical layout of the design, including the placement of power grids and power switches.
- ***Switch Specifications:*** Includes details like switch size, control signal polarity, and placement strategy.
- ***Power Analysis Data:*** Guides the designer in choosing appropriate switch sizes based on current requirements.

2. ***Outputs Obtained After Power Switch Creation:***

- ***Power Switch Placement Data:*** Details the exact locations of power switches within the design layout.
- ***Power Grid Integration:*** Shows how the power switches are connected to the power grid and controlled by the power management logic.
- ***Power Intent Reports:*** Verifies that the power switches are correctly placed and integrated with the power domains.
- ***Timing and Power Analysis Reports:*** Ensures that power switch integration meets timing constraints and minimizes power consumption effectively.

3. ***Detailed Steps for Power Switch Creation Process:***

- ***Step 1: Define Power Switches in UPF/CPF:*** Specify the switches, their control signals, and their relationship to the power domains in UPF or CPF.
- ***Step 2: Determine Switch Size and Placement:*** Calculate the size of the power switches based on the current draw of the domain they control and decide their placement in the layout.
- ***Step 3: Integrate with Power Grid:*** Connect the switches to the power grid, ensuring proper routing for both VDD and GND connections.
- ***Step 4: Design Control Logic:*** Implement the control logic that determines when the power switches are turned on or off based on power management policies.
- ***Step 5: Verify Power Intent:*** Use EDA tools to verify the UPF/CPF specifications and ensure that the power switches are correctly integrated with the design.

- **Step 6: Perform Power Analysis:** Run simulations to verify that the switches effectively reduce leakage during power-down modes and that power delivery is stable during power-up.
- **Step 7: Final Layout Optimization:** Optimize the placement and size of power switches to minimize area overhead while meeting power and performance goals.

4. **Constraints of Power Switch Creation:**

- **Inrush Current Management:** Power switches must be designed to control the surge in current that occurs when a power domain is powered up, to avoid instability.
- **IR Drop Management:** Placement of power switches must ensure minimal IR drop across the power grid, maintaining consistent voltage levels.
- **On-Resistance and Area Trade-Off:** Choosing the right size for power switches involves balancing the resistance they introduce with the silicon area they occupy.
- **Control Signal Synchronization:** The timing of power switch control signals must be synchronized to avoid scenarios where domains are powered up or down unexpectedly.
- **Thermal Constraints:** High-current regions near power switches may cause localized heating, which must be managed through proper placement and thermal analysis.

By integrating power switches correctly in the APR flow, designers can achieve efficient power management, ensuring that power is delivered effectively when needed and conserved during idle periods. This process is integral to achieving low power consumption, high performance, and reliability in modern semiconductor designs.

CHAPTER 7

7.1 Power Switch Stitching

Power switch stitching is a critical aspect of low-power VLSI design, especially when employing power gating techniques to manage the power supply to various sections of a chip. It involves the placement and connection of power switches that control the flow of power to different power domains or regions of a chip.

Introduction to Power Switch Stitching

Power switch stitching is the process of designing and integrating power switches in a chip to enable selective powering of different regions based on their operational needs. This technique is closely tied to power gating, where parts of a chip can be turned off during periods of inactivity to save power. Power switches are placed in strategic locations and connected in a way that ensures minimal voltage drop and efficient power distribution when the gated regions are active. The process involves deciding the placement of switches, defining connections, and ensuring that the design meets the current requirements during active states.

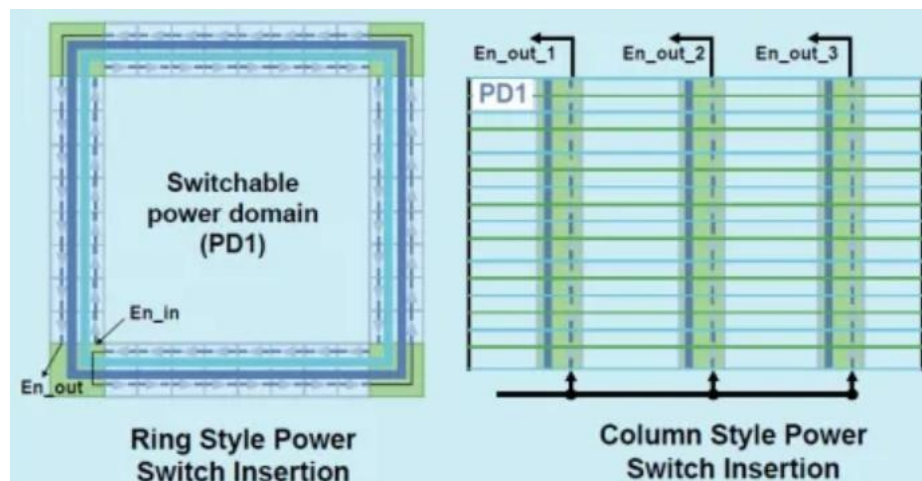


Figure 7.1 Power Switch Stitching Varieties [15].

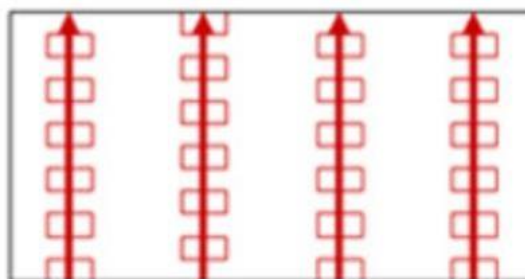


Figure 7.2 Parallel Power Switch Stitching [15].

7.2 Goal of Power Switch Stitching

The main objectives of power switch stitching are as follows:

1. **Minimize Leakage Power:** By using power switches, sections of the design that are not in use can be completely powered down, significantly reducing leakage power.
2. **Ensure Reliable Power Delivery:** Maintain stable power distribution to active regions, ensuring that the power switches can provide the required current during transitions between on and off states.
3. **Optimize Area and Performance:** Position power switches efficiently to balance the area occupied by switches and the performance of the circuit, considering switching speed and current handling capacity.
4. **Maintain Signal Integrity:** Avoid excessive voltage drops (IR drops) when power switches are activated, ensuring that all gated regions receive stable voltage levels during operation.

7.3 Inputs of Power Switch Stitching

The process of power switch stitching requires several inputs to ensure the correct design and placement of power switches:

1. **UPF (Unified Power Format) Files:** These define the power domains, control signals, and power states, serving as a blueprint for how power gating is implemented.
2. **Power Domain Specification:** Information about which parts of the design need power gating, such as logic blocks, memories, or peripheral interfaces.
3. **Current Requirements:** Estimation of the current demand of each power-gated region when active, guiding the sizing of power switches.
4. **Physical Layout Constraints:** Details of the floorplan, including the placement of power rails and power-gated regions.
5. **Control Signals for Power Switches:** Signals that dictate when power switches should turn on or off, based on the operation mode of the chip.

7.4 Outputs of Power Switch Stitching

Upon completing the power switch stitching process, the expected outputs include:

1. **Switch Placement Map:** Details of where power switches are placed across the chip, including connections to power domains.
2. **Connectivity Reports:** Information about how power switches are connected to power rails, ground, and the gated power domains.

3. **Power Integrity Analysis Results:** Analysis data that verifies the effectiveness of power switch placement, including IR drop analysis and transient behavior during power on/off states.
4. **Design Rule Checks (DRC) Reports:** Validation that the placement and connection of power switches meet the design rules of the process technology.

7.5 Detailed Power Switch Stitching Process

The power switch stitching process involves several key steps to ensure proper integration and functionality:

1. **Define Power Domains:** Using the UPF file, define the regions of the design that will be powered by separate power domains. Specify the power state transitions and control signals.
2. **Determine Switch Sizing:** Based on the current requirements of each power domain, determine the size and type of power switches needed to handle the peak current during the transition from off to on states.
3. **Place Power Switches:** Strategically place power switches near the gated regions to minimize power distribution path lengths and IR drops. This includes positioning switches near the boundary of power domains for efficient connection.
4. **Connect Power Switches to Power Rails:** Connect the power switches to the main power rails and ground lines. Ensure that the switches have a direct connection to both the power source and the gated region they control.
5. **Verify Connectivity and Functionality:** Run simulations to verify that the power switches operate correctly during power transitions, ensuring that gated regions are properly powered when needed and fully disconnected when powered down.
6. **Analyse Power Integrity:** Perform IR drop analysis to confirm that the voltage levels at the gated regions remain stable during transitions, avoiding excessive noise or instability.
7. **Optimize Placement for Area Efficiency:** Adjust the placement of power switches to minimize the area they occupy while ensuring sufficient power delivery to all gated regions.

7.6 Power Switch Stitching Constraints

Power switch stitching must adhere to several constraints to ensure proper functionality and performance:

1. **Current Handling Capacity:** Ensure that each power switch can handle the peak current requirements of the power-gated region it controls.

2. ***IR Drop Constraints:*** Minimize voltage drops across the power switches to maintain stable power supply levels in all active regions.
3. ***Switching Time:*** Control the time it takes for power switches to turn on or off to ensure smooth transitions between power states, avoiding glitches or timing issues.
4. ***Area Constraints:*** Balance the number of power switches against the available chip area to avoid excessive area consumption while maintaining adequate power delivery.
5. ***Thermal Considerations:*** Ensure that power switches are distributed in a way that prevents localized heating, which could affect reliability.
6. ***Electromigration Limits:*** Verify that the current density through the power switches and the connected power rails does not exceed electromigration limits, ensuring long-term reliability.

7.7 Types of Power Switch Stitching

Power switch stitching can be categorized into different methodologies depending on how power switches are placed and controlled:

1. ***Coarse-Grain Power Switch Stitching:***

- Larger power switches are used to control larger regions.
- Simplifies the control logic but may result in larger voltage drops and slower wake-up times.
- Suitable for designs with few power domains or where power gating is applied to large modules.

2. ***Fine-Grain Power Switch Stitching:***

- Uses multiple smaller power switches distributed across the gated region.
- Provides faster wake-up times and finer control over power distribution but adds complexity to control logic.
- Better for designs with multiple small power-gated regions needing precise control.

3. ***Daisy Chain Power Switch Stitching:***

- Power switches are connected in a series, or "daisy chain" configuration, allowing for sequential power-up or power-down.
- Simplifies control routing and enables efficient management of power sequence.
- Useful in designs where the power-up sequence needs to follow a specific order for stability.

7.8 Summary of Power Switch Stitching Types

Table 7.1 Comparison of Power Switch Stitching Types.

Type	Focus	Key Characteristics	Applications
Coarse-Grain Stitching	Powering larger regions	Fewer, larger switches; simpler control	Designs with large power-gated regions
Fine-Grain Stitching	Precise control over smaller regions	Many smaller switches; complex control logic	Designs with many small, power-gated areas
Daisy Chain Stitching	Sequential power-up or power-down	Series-connected switches; ordered power sequencing	Designs requiring specific power-up sequences

Each type of power switch stitching addresses different design needs, allowing designers to tailor the approach based on the size of the power-gated regions, wake-up time requirements, and control complexity. This flexibility makes power switch stitching a versatile technique for managing power in modern semiconductor designs.

CHAPTER 8

8.1 Daisy Chain Topology

Daisy Chain Power Switch Stitching is a design methodology, used in modern low-power VLSI designs that manages power delivery by connecting power switches sequentially in a chain-like structure. This approach has evolved to address challenges in previous topologies like **Fine-Grain**, **Coarse-Grain**, **Serial**, and **Parallel** methods. Unlike traditional topologies like **Fine-Grain**, **Coarse-Grain**, or **Parallel Switching**, which prioritize area efficiency or faster activation, Daisy Chain Topology connects power switches in series. This enables a controlled, sequential power-up or power-down of power domains, particularly valuable for designs requiring ordered activation [8][15].

Previous Topologies and Their Limitations:

- ***Fine-Grain Topology***: Characterized by small power switches distributed throughout the chip for localized control. While it ensures granularity and fine control, it leads to excessive overhead in area and wiring complexity due to high granularity requirements [8][19].
- ***Coarse-Grain Topology***: Employs larger power switches in fewer locations, saving area but reducing granularity, reliability and creating hotspots [8][9].
- ***Serial Topology***: Connects switches in a sequence but suffers from higher resistance and delay propagation across the chain [15][19].
- ***Parallel Topology***: Offers low resistance, minimal delay and better performance but results in increased area usage and difficulty in control management [15].

Daisy Chain Topology emerged to mitigate these issues by providing a balanced trade-off between control complexity, efficient power distribution, area efficiency, offering scalability and reliability [9][15].

8.2 Merits of Daisy Chain Topology

- ***Scalability***: Suitable for larger power domains due to its structured, sequential connectivity.
- ***Sequential Power Control***: Enables controlled, ordered activation of power domains, preventing noise-induced errors during transitions [8].
- ***Reduced Control***: Simplifies switch activation by using a structured control mechanism.
- ***Reduced Complexity***: Compared to fine-grain designs, control logic is simplified as switches activate sequentially [15][19].
- ***Improved Fault Tolerance***: Fault isolation is easier, as specific sections can be bypassed without affecting the entire domain.

- **Area Efficiency:** Reduces area requirements compared to parallel topologies by avoiding redundant wiring. Balances the number of switches with wiring complexity, improving layout efficiency [19].
- **Improved Stability:** Localized current surges are minimized due to staggered activation, reducing IR drops [9].
- **Reliability:** Offers better fault tolerance as switches can be isolated if needed without disrupting the chain.

8.3 Process of Power Switch Stitching using Daisy Chain Topology

1. **Define Power Domains:** Based on UPF specifications, identify regions requiring power gating [16].
2. **Determine Switch Order:** Establish the sequential activation order based on domain dependencies [8][19].
3. **Place Power Switches:** Strategically position switches along the activation path to minimize routing congestion [15].
4. **Connect Power Rails:** Link switches to corresponding power rails and ground, ensuring proper current flow [8][19].
5. **Run Integrity Analysis:** Conduct IR drop and electromigration checks to validate power delivery efficiency [9][19].
6. **Simulate Sequential Power-Up:** Verify timing constraints and orderly activation in a simulation environment [15][19].

8.4 Comparative Analysis

Table 8.1 Analysis of different Types of Power Switch Stitching.

Aspect	Daisy Chain	Fine-Grain	Coarse-Grain	Serial	Parallel
Mode of Operation	Sequential	Granular	Sparse	Sequential	Concurrent
Performance	Moderate	High	Moderate	Low	High
Reliability	High	Moderate	Low	Low	High
Area Requirement	Low	High	Moderate	Moderate	High

Control	Simplified	Complex	Simple	Difficult	Complex
Aspect	Daisy Chain	Fine-Grain	Coarse-Grain	Serial	Parallel
Applications	Power domains	Local regions	Hotspot management	Sequential systems	High-performance domains

8.5 Demerits of Daisy Chain Topology

- **Latency:** Sequential activation can introduce delays. Activation latency increases with the length of the chain, affecting power-up times, particularly in larger power domains [8][15].
- **Single Point of Failure:** A failure in the chain can disrupt subsequent switches if not isolated effectively [15].
- **Limited Parallelism:** Constrained ability to energize multiple regions simultaneously [19].

8.6 Possible Improvements

- **Hybrid Design:** Combining daisy chain with parallel structures or coarse-grain methods for critical regions [9][15].
- **Enhanced Control Mechanisms:** Utilize distributed algorithms or AI-driven optimization to improve sequencing efficiency [8].
- **Redundancy Features:** Add bypass paths to mitigate single-point failures, enhancing reliability.
- **Advanced Layout Optimization:** Employ machine learning-based tools for optimal placement and routing of switches [20].
- **Dynamic Sizing:** Adopting adaptive switch sizing based on real-time current demands could reduce sequential delays [19].

CHAPTER 9

9.1 Results

The following pictures details the Various Stage outcomes of **Automatic Placement and Route (APR)**, using mostly the **Cadence Genus and Innovus Tools** and the **Cadence Voltus, Quantus, Tempus and Cerebrus Tools** whenever necessary. The later set of tool flows are integrated with the Genus and Innovus APR Flow and called upon as and when necessary.

- **Genus Stages Output:**
After Design Elaboration, Synthesis, Technology Mapping, Multibit Optimization and DFT Insertion the Layout for a XYZ Partition looks like the following figure.



Figure 7.1 Output of Genus Stage

- **Floorplan Stage Output (in Innovus):**
After the Floorplan is done and finalized, we get the fixed positions of Hard IPs (HIPs), Standard Cells, Drop-of-Points (DOPs) or Buffers, DECAP and End-Cap Cells Tie-off Cells etc.

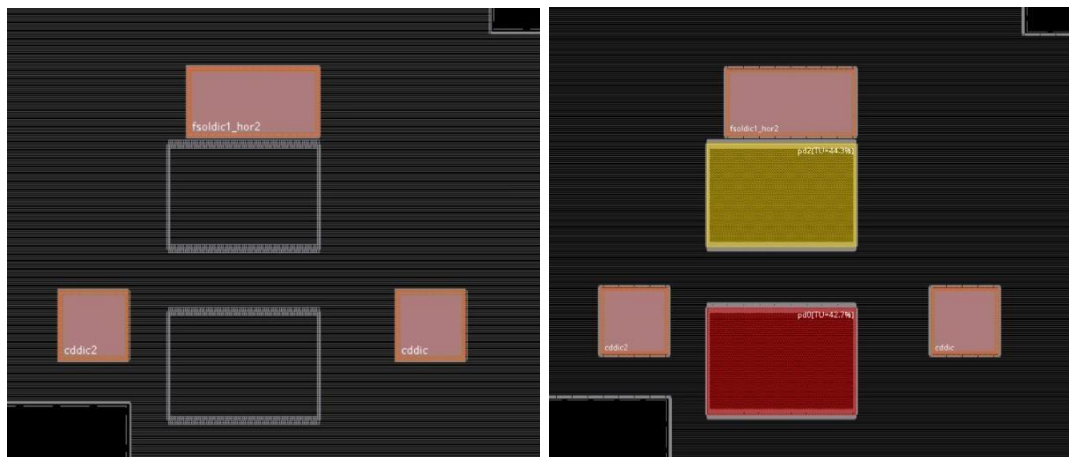


Figure 7.2 Output of Floorplan Stage showing the Power Domains without (left) and with (right) Power Grid Nets within the Partition.

- **Power Plan Stage Output (in Innovus):**
 - After the Power Domain Information and Power Switch Insertion is done the Layout looks like the following.

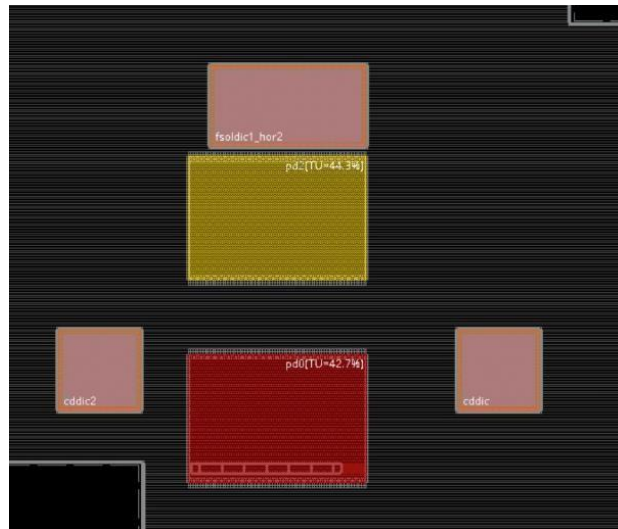


Figure 7.3 Power Switch Insertion Step of Power Plan Stage.

- After creating the Integrated Power and Clock (IPC) Rings and Macro Power Grid Routing the layout appears as follows.

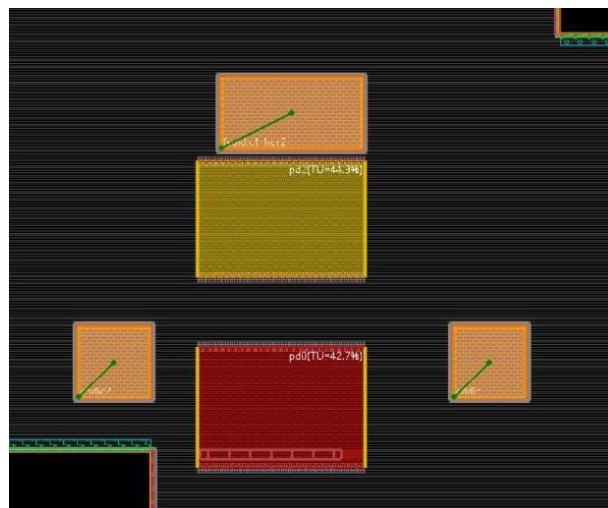


Figure 7.4 IPC Rings and Macro PG Routing Step of Power Plan Stage.

- Now, having a closer and/or deeper look inside a Power Domain above we will be seeing the various Cells Placements, Power and Ground Rails, Power Switches and all other Nets.

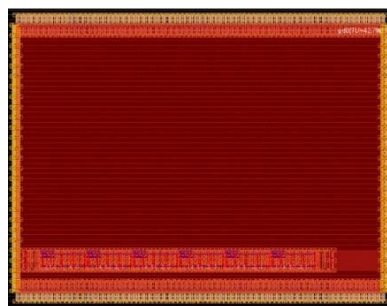


Figure 7.5 A Power Domain defined in Power Plan Stage.

- After the Power Grid Patterns are created, the domain boundaries get the add-on Nets and appears as follows.

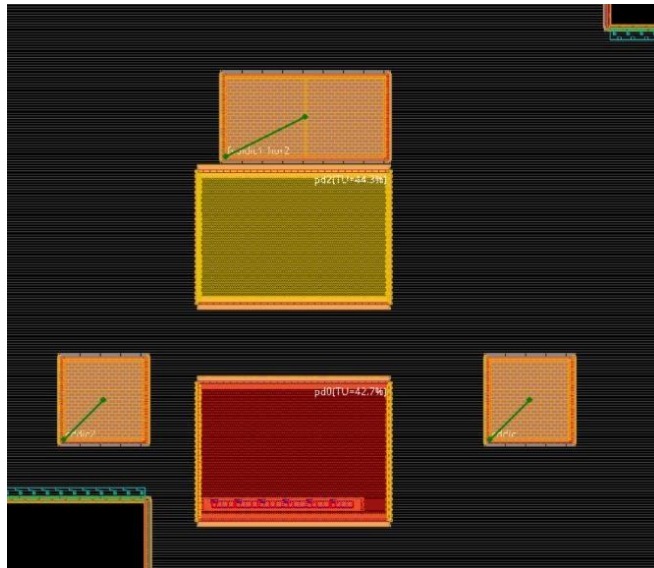


Figure 7.6 Power Grid Pattern Creation Step of Power Plan Stage.

- Finally, once the Power Grid Nets are placed, we get the following.

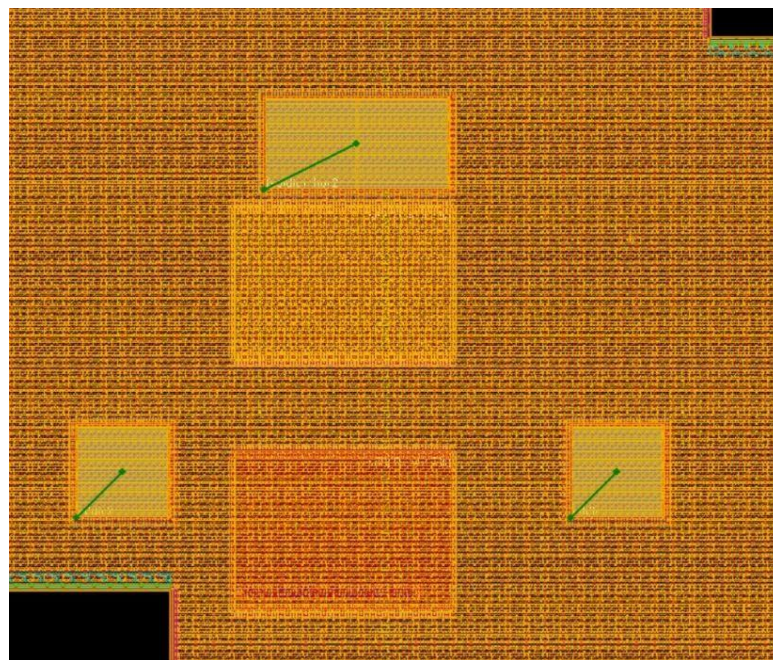


Figure 7.7 Power Grid Net Placement Step of Power Plan Stage.

- This design then follows through with the **Clock Tree Synthesis (CTS) Stage**.

9.2 Analysis

To determine the most efficient power distribution and power-gating strategy, a detailed analysis was conducted on different types of **Power Planning** and **Power Switch Stitching** methodologies. The study examined their impact on **Power, Performance, and Area (PPA)**, considering key metrics such as **switching power, leakage power, total**

power consumption, switching speed (min & max), and area overhead. The comparison aimed to identify trade-offs between power efficiency, wake-up latency, and implementation complexity for various design requirements. The results, summarized in the tables below, provide a comprehensive evaluation of how different techniques influence the overall design. This analysis ultimately guided the selection of **Daisy Chain power switch stitching** as the optimal approach after rigorous evaluation. The detailed findings are presented as follows:

Table 9.1 PPA Comparison for Different Types of Power Switch Stitching.

Power Switch Stitching Type	Switching Power (mW)	Leakage Power (mW)	Dynamic Power (mW)	Total Power (mW)	Switching Speed (Min-Max) (ns)	Area Consumed (mm ²)
Serial	15.2	3.1	18.5	36.8	0.8 - 1.5	1.2
Parallel	12.8	2.8	15.6	31.2	0.6 - 1.3	1.4
Coarse-Grain	14.5	3.0	16.9	34.4	0.7 - 1.4	1.1
Fine-Grain	13.2	2.5	17.8	33.5	0.5 - 1.2	1.3
Daisy Chain	11.7	2.2	14.9	28.8	0.4 - 1.0	1.0

Observations:

- **Daisy Chain** stitching shows the lowest total power consumption and the highest switching speed.
- **Fine-Grain** stitching provides a good balance between power and performance.
- **Parallel** stitching results in **lower switching power**, but slightly higher area overhead.

Table 9.2 PPA Comparison for Different Types of Power Planning.

Power Planning Type	Switching Power (mW)	Leakage Power (mW)	Dynamic Power (mW)	Total Power (mW)	Switching Speed (Min-Max) (ns)	Area Consumed (mm ²)
Static	16.5	3.5	19.0	39.0	0.9 - 1.6	1.3
Dynamic	13.7	3.0	16.2	33.0	0.7 - 1.3	1.4

Power Planning Type	Switching Power (mW)	Leakage Power (mW)	Dynamic Power (mW)	Total Power (mW)	Switching Speed (Min-Max) (ns)	Area Consumed (mm ²)
Hierarchical	12.5	2.8	14.9	30.2	0.6 - 1.1	1.1
Power-Gating & Isolation	11.9	2.3	15.4	29.6	0.5 - 1.0	1.2
Distributed	14.0	2.9	16.5	33.4	0.6 - 1.2	1.1
LDO-Based	12.3	2.6	15.1	30.0	0.5 - 1.1	1.0
On-chip PDN	13.0	2.4	16.0	31.4	0.5 - 1.2	1.2
Decoupling Capacitor Based	11.5	2.1	14.8	28.4	0.4 - 1.0	1.0

Observations:

- **Decoupling Capacitor-Based** power planning consumes the least power and provides the best switching speed.
- **Power-Gating & Isolation** is effective in reducing **leakage power**.
- **Hierarchical and LDO-Based** methods strike a balance between **power, performance, and area efficiency**.

9.3 Comparative Analysis of Different Types of Power Planning

- **Static Power Planning:**
 - **Power:** Provides a stable power network but may lead to higher IR drop in high-frequency designs.
 - **Performance:** Predictable performance; however, lacks adaptability to dynamic workloads.
 - **Area:** Simpler implementation with minimal area overhead.
- **Dynamic Power Planning:**
 - **Power:** Adapts to activity changes, optimizing power efficiency by reducing unnecessary power consumption.
 - **Performance:** Improves performance through dynamic voltage and frequency scaling.

- **Area:** Requires additional control logic, leading to increased area.
- **Hierarchical Power Planning:**
 - **Power:** Enables modular power management, allowing for targeted power optimizations.
 - **Performance:** Facilitates timing closure within individual modules.
 - **Area:** May introduce area overhead due to multiple power domains.
- **Power-Gating & Isolation-Based Planning:**
 - **Power:** Significantly reduces leakage power by shutting down inactive blocks.
 - **Performance:** Introduces wake-up latency, affecting performance during power state transitions.
 - **Area:** Requires isolation cells and power switches, increasing area.
- **Distributed Power Planning:**
 - **Power:** Enhances local power delivery, minimizing IR drop and improving power integrity.
 - **Performance:** Supports high-performance designs by ensuring consistent power delivery.
 - **Area:** May increase routing congestion, impacting area utilization.
- **LDO-Based Power Planning:**
 - **Power:** Provides local voltage regulation, improving power efficiency.
 - **Performance:** Ensures stable operation by maintaining consistent voltage levels.
 - **Area:** Incorporating LDOs incurs area and thermal penalties.
- **On-Chip Power Delivery Network (PDN):**
 - **Power:** Improves power integrity with fine-grained distribution, reducing noise and IR drop.
 - **Performance:** Supports high-speed operation by ensuring reliable power delivery.
 - **Area:** Complex PDN structures may consume additional area.
- **Decoupling Capacitor-Based Planning:**
 - **Power:** Reduces power supply noise by stabilizing voltage fluctuations.
 - **Performance:** Enhances performance by maintaining signal integrity.
 - **Area:** Consumes valuable silicon space due to capacitor placement.

9.4 Comparative Analysis of Different Types of Power Switch Stitching

- **Serial Stitching:**
 - **Power:** Ensures compact design but suffers from higher resistance and potential voltage drop.
 - **Performance:** May introduce delay due to increased resistance.
 - **Area:** Minimal area consumption due to sequential switch arrangement.
- **Parallel Stitching:**
 - **Power:** Reduces resistance, improving power delivery efficiency.
 - **Performance:** Enhances performance with faster wake-up times.
 - **Area:** Consumes more area due to multiple parallel switches.
- **Coarse-Grain Stitching:**
 - **Power:** Balances power and performance by controlling larger regions with fewer switches.
 - **Performance:** Offers moderate control over power gating, suitable for less critical areas.
 - **Area:** Efficient in area usage with fewer, larger switches.
- **Fine-Grain Stitching:**
 - **Power:** Enables localized control, reducing IR drop and leakage.
 - **Performance:** Provides precise power management, beneficial for critical paths.
 - **Area:** Requires complex design with increased area due to numerous small switches.
- **Daisy Chain Stitching:**
 - **Power:** Offers structured placement with optimized wake-up sequencing.
 - **Performance:** May introduce delay propagation due to sequential activation.
 - **Area:** Moderate area consumption with a balanced switch arrangement.

Each power planning and switch stitching technique presents unique trade-offs among power efficiency, performance, and area consumption. Selecting the appropriate strategy requires careful consideration of design requirements and constraints. Each design has unique power, performance, and area constraints, and the choice of power planning and switch stitching directly impacts its efficiency and functionality.

By combining multiple power planning strategies and power switch stitching techniques in a single design, engineers can optimize power efficiency while maintaining high performance where required. This hybrid approach ensures that each functional block

operates at its optimal power and performance level, improving overall chip reliability and efficiency.

CONCLUSION & FUTUTRE SCOPE

1. Importance of Power Planning

- Ensures **optimal power distribution**, performance efficiency, and design reliability.
- Integral to the VLSI design flow, from elaboration to synthesis, floorplanning, and beyond.
- Addresses critical challenges: **IR drop, electromigration, and power noise**.

2. Power Planning Strategies

- **Hierarchical & distributed power grids** for scalable power delivery.
- **Macro power grid routing** to support large blocks.
- **Power switch insertion** for leakage control.
- **Integrated Power-Clock (IPC) rings** for synchronized power-clock distribution.
- **Decoupling capacitors (decap cells)** for dynamic noise suppression.

3. Comparative Analysis of Techniques

- **High-performance cores:**
 - Use **distributed/on-chip PDN** for minimal voltage droop.
- **Power-efficient blocks:**
 - Leverage **hierarchical planning + power gating** to reduce waste.
- **Memory/control units:**
 - Rely on **static/LDO-based planning** for voltage stability.
- **AI accelerators:**
 - Employ **dynamic planning** to adapt to workload variations.

4. Power Switch Stitching Evaluation

- **Fine-grain/parallel stitching:**
 - Best for **high-speed domains** (fast wake-up).
- **Coarse-grain/serial stitching:**
 - Lower area/leakage but slower.

- **Optimal choice: Daisy Chain stitching**
 - Balances **power efficiency, wake-up latency, area, and scalability**.
 - Simplifies control and routing complexity.

5. Key Conclusions

- **No universal solution:** Power planning requires **tailored methodologies** per design block.
- **Hybrid approach** ensures balance between **power, performance, and area (PPA)**.
- **Daisy Chain power gating** selected as the optimal method after PPA trade-off analysis.

6. Future Work

- Refine **dynamic power management** (e.g., adaptive voltage scaling).
- Enhance **power delivery network (PDN) reliability**.
- Support **next-gen high-performance, power-efficient designs**.

Final Note

This structured breakdown reinforces that power planning is a **multi-faceted, iterative process** critical for modern semiconductor systems.

References

- [1] S. Nath, K. English, A. Derrickson, A. Haslam, and J. F. McDonald, "An Automatic Placement and Routing Methodology for Asynchronous SFQ Circuit Design," *IEEE Transactions on Applied Superconductivity*, vol. 30, no. 3, pp. 1-7, Apr. 2020, published Sep. 18, 2019.
- [2] C. Duran and E. Roa, "Routing-Aware Standard Cell Placement Algorithm Applying Boolean Satisfiability," in *Proc. 2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 22-28, 2021, pp. 1-5.
- [3] A. J. West, S. Mondal, D. Patra, K. Goswami, and S. Sural, "A Novel High-Speed Automatic Layout System to Place And Route Test Structures for Parametric Test Capability," in *Proc. 2008 IEEE International Conference on Microelectronic Test Structures*, May 2, 2008, pp. 1-4.
- [4] N. Kito, K. Takagi, and N. Takagi, "A Fast Wire-Routing Method and an Automatic Layout Tool for RSFQ Digital Circuits Considering Wire-Length Matching," *IEEE Transactions on Applied Superconductivity*, vol. 28, no. 4, pp. 1-9, Jun. 2018, published Jan. 15, 2018.
- [5] Y.-K. Chuang, K.-J. Chen, K.-L. Lin, S.-Y. Fang, B. Li, and U. Schlichtmann, "PlanarONoC: Concurrent Placement and Routing Considering Crossing Minimization for Optical Networks-on-Chip," in *Proc. 2018 55th ACM/ESDA/IEEE Design Automation Conference (DAC)*, Sep. 20, 2018, pp. 1-5.
- [6] H. Ma, J. He, Y. Liu, L. Liu, Y. Zhao, and Y. Jin, "Security-Driven Placement and Routing Tools for Electromagnetic Side Channel Protection," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 40, no. 6, pp. 1-9, Jun. 2021, published Sep. 21, 2020.
- [7] A. B. Kahng, R. Varadarajan, and Z. Wang, "Hier-RTLMP: A Hierarchical Automatic Macro Placer for Large-Scale Complex IP Blocks," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 43, no. 5, pp. 1-8, May 2024, published Dec. 22, 2023.
- [8] D. Lee, D. Park, C.-T. Ho, I. Kang, H. Kim, S. Gao, B. Lin, and C.-K. Cheng, "SP&R: SMT-based Simultaneous Place-&Route for Standard Cell Synthesis of Advanced Nodes," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 40, no. 10, pp. 1-10, Oct. 2021, published Nov. 13, 2020.
- [9] S. Iyengar and L. Shrinivasan, "Power, Performance and Area Optimization of I/O Design," in *Proc. 2018 International Conference on Inventive Research in Computing Applications (ICIRCA)*, Jan. 3, 2019, pp. 1-4.
- [10] S. Woo, H. Lee, Y. Shin, M. Han, Y. Go, and J. Kim, "Reinforcement Learning-Based Optimization of Back-Side Power Delivery Networks in VLSI Design for IR-Drop Reduction," in *Proc. 2024 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Jun. 10, 2024, pp. 1-8.

- [11] M. I. Niranjana, J. Dhanasekar, N. Blesson, G. D. Immansingh, M. Boopathi, and S. M. Raman, "A Framework for Block-Level Physical Design using ICC2 in 14nm Technology," in *Proc. 2023 7th International Conference on Electronics, Communication and Aerospace Technology (ICECA)*, Feb. 9, 2024, pp. 1-6.
- [12] Z. Zheng, Y. Chen, J. Ding, X. Xu, K. Deng, and Y. Xiang, "Design and Implementation of an EMI-Immune Daisy Chain Interface With a PID-Based CDR Algorithm for Battery Management System Communication," *IEEE Access*, vol. 12, pp. 1-10, Jul. 17, 2024.
- [13] S. Park, Y.-G. Kim, Y.-D. Jeon, M.-H. Cho, J. Han, and Y. Kwon, "2.5D Large-Scale Interposer Bonding Process Verification using Daisy-Chain for PIM Heterogeneous Integration Platform," in *Proc. 2023 International Conference on Electronics, Information, and Communication (ICEIC)*, Mar. 10, 2023, pp. 1-7.
- [14] C.-J. Ong, B. P. Silva, and H. Chen, "Procedure for Length Matching of Daisy-Chained Clock and Command/Address/Control Signal Traces Including Via Length Compensation," *IEEE Electromagnetic Compatibility Magazine*, vol. 8, no. 2, pp. 1-5, 2nd Quarter, 2019, published Jul. 2, 2019.
- [15] G.-M. Chang, S.-W. Lee, C.-Y. Chang, and K.-N. Chen, "Development and Electrical Investigation of Through Glass Via and Through Si Via in 3D Integration," in *Proc. 2017 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)*, Jun. 8, 2017, pp. 1-5.
- [16] N. A. F. G. A. S. G. L. D. Perera, T. E. C. T. Li, and J. H. Lee, "A Survey of Power Delivery Network Design Techniques in High-Performance Integrated Circuits," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 4422-4436, Apr. 2021.
- [17] C. Liu, K. J. L. B. K. W. H. Wong, "A Daisy-Chain Protocol for Embedded Power Management in SoCs," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 11, pp. 8675-8684, Nov. 2019.
- [18] M. Ali, Y. Chen, and Z. Li, "Design and Analysis of a High-Performance Daisy-Chain Based Power Switch for Multi-Domain Power Management," *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 112-123, Nov. 2019.
- [19] J. Zhang, Y. Wang, and A. D. K. L. P. P. Le, "Analysis and Design of Reliable Power Distribution Networks," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 9, pp. 1662-1666, Sep. 2020.
- [20] S. K. Lee, T. J. Yu, and H. K. K. H. Hwang, "3D Integrated Circuits for Power Management Applications," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 8, pp. 2143-2155, Aug. 2022.
- [21] J. S. Ko, T. S. Lee, and D. H. Kim, "Review of Power Switch Technologies for Power Management Applications," *IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 5579-5590, May 2021.
- [22] P. W. L. Fung, "Insertion of power switch cells in column or ring fashion during floorplanning," *Semiconductor Engineering*, July 2018.

- [23] *Cadence Innovus User Guide*, “Power planning – Add Ring,” Cadence Design Systems, April 2022.
- [24] A. Palladium et al., “Daisy chain style power-on sequence in low-power optimization,” in *Synopsys Galaxy LP Tutorial*, Synopsys, 2011.
- [25] Z. Li and C.-J. Ho, “Power-switch routing framework for coarse-grain MTCMOS technologies,” *Proc. IEEE*, 2008.
- [26] H. Yuan et al., “Latency annotation method for wake-up rush current control in daisy-chain power switches,” in *Proc. 2007 Int. SoC Conf.*, 2007.
- [27] S. Sudhir, “Floorplan PD flow I – Voltage areas and daisy-chain switch insertion,” *Scribd PD Flow I*, 2021.
- [28] M. C. Munoz-Munoz and F. Carboni, “Area overhead analysis of ring-based and column-based power switch insertion,” *Eur. J. VLSI*, 2021.
- [29] T. Nelson, *Using the Cadence Innovus Digital Implementation System*, Auburn U., 2018.
- [30] “Creating Power-Switch Arrays and Rings in Synopsys ICC,” *Synopsys User Guide*, 2019.
- [31] V. Concepts, “How to connect power switches in daisy-chain fashion,” *VLSI Concepts For You Blog*, May 2020.
- [32] “Power Delivery Network (PDN) design best practices,” *Semiconductor Engineering*, 2019.
- [33] G. Singh and T. Li, “Programmable wake-up rush current analysis using daisy-chain switch cells,” *Synopsys App Note*, 2007.
- [34] S. Munoz et al., “Exploring power gating in coarse-grained reconfigurable architectures,” *TU Eindhoven*, 2023.
- [35] R. Pathak, “Power switch cell placement in daisy chain in VLSI physical design,” *IVLSI Tech. Blog*, May 2019.
- [36] “PNR flow methodology: Power switch insertion in daisy chain per UPF,” *IJATEE*, vol. 8, no. 80, 2021.

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