STUDY THE PERFORMANCE ANALYSIS OF CARBON NANOTUBE AS A VLSI INTERCONNECT

Thesis submitted in the partial fulfillment of requirement for the award of degree of

Master of Technology

in

VLSI Design

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<u>DECLARATION</u>

I, Anup Kumar, hereby certify that the work which is being presented in this thesis entitled "Study the Performance Analysis of Carbon Nanotube as a VLSI Interconnect" by me in partial fulfilment of the requirements for the award of degree of Master of Technology in VLSI Design from Thapar University (Deemed University), Patiala, is an authentic record of my own work carried out under the supervision of Mr. Mayank Kumar Rai.

The matter presented in this thesis has not been submitted in any other University / Institute for the award of any other degree.

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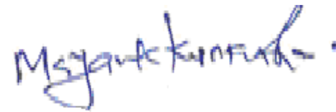
It is certified that the above statement made by the student is correct to the best of my knowledge and belief.



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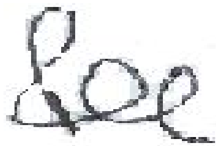

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ACKNOWLEDGEMENT

First of all, I would like to express my gratitude to **Mr. Mayank Kumar Rai, Assistant Professor,** Electronics and Communication Engineering Department, Thapar University, Patiala for his patient guidance and support throughout the work. I am truly very fortunate to have the opportunity to work with him. I found this guidance to be extremely valuable.

I am also thankful to **Dr. Rajesh Khanna, Professor & Head,** Electronics and Communication Engineering Department, entire faculty and staff of the department and the friends who devoted their valuable time and helped me in all possible ways towards successful completion of this work.

Lastly, I would like to thank my grandparents and parents for their years of unyielding love for constant support and encouragement. They have always wanted the best for me and I admire their determination and sacrifice.

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ABSTRACT

Interconnect delay is a major factor determining the performance of VLSI circuits. As technology scaled down interconnects delay dominates the gate delay.

In deep submicron meter VLSI technologies, it has become increasingly difficult for conventional copper based electrical interconnect to satisfy the design requirements of delay, power and bandwidth.

Promising candidate to solve this problem is carbon nanotube(CNT). CNTs are susceptible to electromigration problems that plague the copper interconnect. Due to high thermal conductivity and large current carrying capacity CNTs are preferred over copper as VLSI future interconnect.

In this thesis Performance of CNT and copper has been studied with equivalent circuit model of CNT and Copper at 32nm technology node. Using this model, the performance of CNT-bundle interconnects (at local, intermediate and global levels) is compared to copper wires. It is shown that CNT bundles gives better results at semiglobal and global length of interconnects whereas copper interconnect gives better result at local length of interconnects.

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ABBREVIATION

CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nanotube
EDA	Electronic Design Automation
IC	Integrated Circuit
ITRS	International Technology Road Map for Semiconductors
MFP	Mean Free Path
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MWCNT	Multi Wall Carbon Nanotube
RLC	Resistance, capacitance and Inductance
SPICE	Simulation Program with Integrated Circuit Emphasis
SWCNT	Single wall carbon nanotube
VLSI	Very large scale integration

CHAPTER1

INTRODUCTION

Interconnects means the wires that link together transistors, circuits, cell, modules and system as well. It controls timing, power, noise, design functionality and reliability. It mainly provides power delivery paths, clock delivery paths and signal delivery paths. Power delivery path distribute power to every element in the system and provides appropriate return paths, clock delivery paths deliver global or local clocks to storage elements, and signal delivery paths provide the communication capability among circuit modules. For multiple- processor system, a more complicated interconnect network referred to as a network on chip.

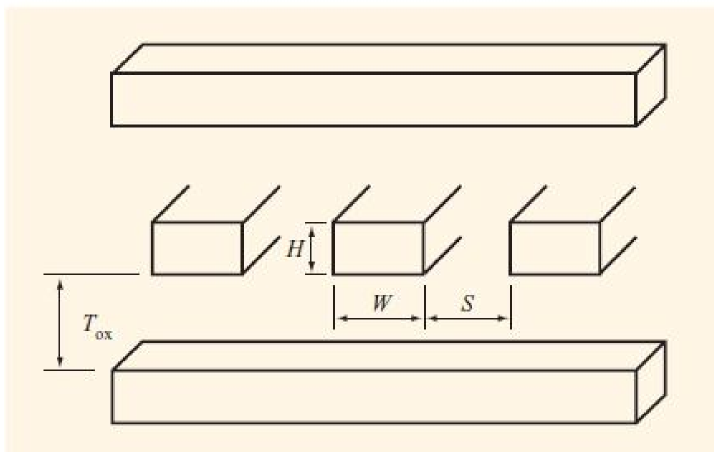

Fig 1.1 Physical representation of interconnect system [1]

Interconnects play a major role in deep submicron technologies such as 90nm and below. While gate delay dominated interconnect delay in earlier technologies, it is no longer the case and delays associated with interconnects are becoming increasingly important. This is because in deep submicron technologies interconnect can no longer be seen as simple resistor but the associated parasitic such as capacitance and inductance also need to be considered [1]. Thus any signal propagating through such interconnect can be expected to be delayed. The parasitic effects introduced by the interconnects display scaling behaviour that differs from the active devices such as transistors, and they tend to gain in importance as device dimensions are reduced and circuit speed is increased. In fact, they

start to dominate some of the relevant matrices of digital integrated circuits such as speed, energy consumption and reliability.

The semiconductor industry has been fuelled by enhancements in integrated circuit density and performance, resulting in information revolution for over four decades and is expected to continue in future. The periodic improvement in density and performance improves as gate length, gate dielectric thickness and junction depth are scaled. Scaled chip interconnect suffers from increased resistance due to increase in conductor cross sectional area and may also suffer from increased capacitance if metal height is not reduced with conductor spacing. As operating frequencies goes on increases parasitic inductive effects must also be considered. Thus interconnect parasitic play an increasingly important role in overall chip performance as feature size scaled.

The increase in integration density and chip area results in the total increase in wire length per unit area and decrease in interconnect pitch (sum of space between two interconnects and width of one interconnect). As feature size will continue to scale down enforces an increase in impurity concentration and scaling down of supply and threshold voltage to maintain the electric fields in the device. As the supply voltage is scaled, the interconnect dimensions must also reduced to take advantage of feature size scaling. Hence due to increase in complexity and functionality the chip size growth increases and scaling results in rapid increase of capacitance and resistance of interconnect wires. The interconnect effects like the rising RC delay of on-chip wiring, noise considerations such as crosstalk and delay unpredictability, uncertainty due to process variations, reliability concerns due to rising current densities and oxide electric fields, and increasing power dissipation are becoming increasingly prominent in deep submicron and nanometer as technology scaling trend continues, interconnect parasitic play dominant role in determining chip performance and functionality.

To improve the propagation speed, delay, power consumption, silicon area, and cost characteristics the feature size of ICs has been reduced. Semiconductor technologies with feature size of several tens of nanometer are currently in use. These interconnects distribute robust and reliable power and ground; clock; data and address; and other control signals. Distributing these signals in such a high speed, high-complexity environment, is a challenging task. As technology scaling trend continues, interconnect parasitic play dominant role in determining chip performance and functionality. The performance of a high-speed chip is highly dependent on

interconnects which connect different macro cells within a very large-scale integrated (VLSI) chip.

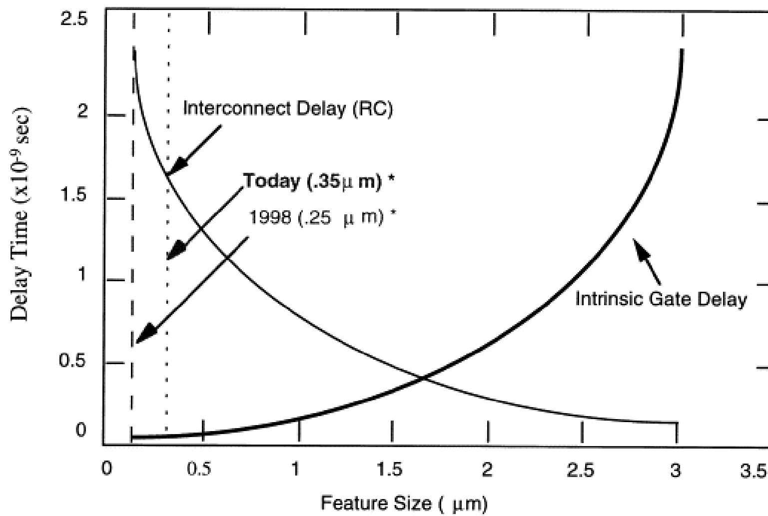

Fig1.2 Interconnect delay dominates gate delay in sub-micron technologies [2]

1.1 Interconnect delay

Historically, interconnect delay was considered to be electrically negligible. Currently interconnections are becoming a major concern in high performance ICs and the RC delay due to interconnect is the key factor in determining the performance of a chip. The resistance of wires increases rapidly as chip size grows larger and minimum feature size reduces.

The interconnect delay can be estimated by the *RC* delay product of interconnect line resistance, *R*, and the parasitic capacitance C coupling interconnect to adjacent lines and underlying Si substrate. Resistive parasitic may cause an IR drop such that noise margins are reduced and the performance of logic circuits is deteriorated. The combination of resistive and capacitive parasitic induces RC delays of signals and clocks, which may severely impact on the performance of logic circuits. Hence the reduction of RC delays is an important issue for designing high performance logic circuits.

1.2 Buffer insertion

The delay of a wire is a quadratic function of its length. Hence, to reduce the propagation delay of a long wire, we need to break up the quadratic relationship associated with the

length. To achieve this subdivide the long wire into many segments and then to insert a buffer between two segments so that the propagation delay of resulting long wire becomes a linear function of the number of segments. The design approach based on this idea is referred to as buffer insertion.

1.3 Interconnection scaling effects:

Scaling of widths and spacing has caused the metal interconnections to start dominating the IC's performance, reliability and signal integrity. The increasing resistance values of the on chip interconnections lead to larger voltage drops and the increasing mutual capacitance values cause more cross-talk, while the combination leads to larger signal propagation delays. At 1GHz, the required signal rise and fall times should be less than 50ps to perform some computational tasks within the available 1ns time frame. Even on-chip wires then cause interference with other modules. For such signal edges, line lengths of 3mm and above become critical and require transmission line modelling.

There are several approaches to reduce the negative effects of scaled interconnections. One is to reduce the capacitance and resistance and other is insert repeaters in between interconnects. The signal propagation delay over a metal wire is proportional to square of length of interconnects, the use of repeaters, however reduces the propagation delay for global signal wires, this may reduces the propagation delay by more than a factor of two.

1.4 Aluminium interconnect

For several semiconductor technology generations, aluminium was used as the on-chip interconnect metal and silicon-di-oxide as the inter- and intra-level insulator. With rapid scaling of feature size to deep submicron levels, the signal delay caused by interconnect became increasingly significant compared to the delay caused by the gate and thus affecting the circuit's reliability. As per ITRS predictions, for nanometer size gate lengths the interconnections will decide the communication speed of a VLSI chip [3]. The interconnect delay is mostly affected by resistive and capacitive parasitic. For decreasing the resistive part of the RC delay, various alternatives to aluminium were considered in early 1990s. For metallic conductors with electrical resistivity lower than aluminium, the options were targeted to silver, copper, and gold. Although gold has high resistance to electromigration but shows a little improvement in resistivity. Furthermore, adding to its

demerit gold creates deep levels in the band gap due to diffusion in silicon and thus affects electronic properties of a device. Similarly, silver with the lowest resistivity creates deep levels in the silicon band gap and diffuses in SiO_2 vigorously. Copper with close to half the resistivity (1.7mVcm) compared to Al/0.5 percent Cu alloys (3.0mVcm) and with electromigration of the order of ten times better appeared to be most appropriate material for VLSI interconnect [4]. Copper has a higher melting point (1,357 K) than aluminium (933K), which gives copper the advantage over aluminium in electromigration and stress migration. The typical VLSI application temperature range (1,373 K) is about 40 percent of the aluminium melting point and 27.4 percent of the copper melting point. This suggests that mass transport (copper diffusion) in copper is generally slower than that in aluminium at room temperature. Recently, copper is widely used on chip interconnect for advanced ICs.

1.5 Copper interconnects

Copper interconnects offer better reliability than aluminium interconnects. Regarding electromigration, copper interconnects can carry a much higher current than their aluminium counterparts for the same lifetime and similar end-of-life failure rates. In addition to having lower electrical resistivity than aluminium interconnects, copper interconnects have a higher resistance to electromigration. Copper has a higher melting point (1357 K) than aluminium (933 K), which gives copper the advantage over aluminium in stress migration.

It was realized in early 2000, that even copper is not able to fulfil the demands of high-speed interconnects. The requirement of lower resistance and higher bandwidth is the major concern in interconnects design with the increase in the integration density of the complementary metal-oxide-semiconductor and higher clock frequency. To accommodate more interconnects in a chip the cross-sectional dimensions are being reduced rapidly, resulting in dimensions reaching to the order of the mean free path of electrons (~40nm Cu at room temperature). Furthermore, the resistivity of copper interconnects is increasing rapidly under the effects of enhanced grain and surface scattering; larger interconnect length; and higher frequency operation.

Owing to the decreasing thermal conductivity of low-k dielectrics and increasing current density in concise dimension interconnect; the rising Cu resistivity also poses a reliability concern due to Joule heating. The increased heating stimulates electromigration induced

hillocks and voids. One key constraint in the conventional scaling of silicon VLSI is the high interconnect-related power dissipation per unit area. Thus, researchers require serious alteration in copper interconnect technology because copper interconnect is limited by skin effect, dispersion, signal degradation, power dissipation, and electromagnetic interference at higher frequency.

1.6 Interconnect Challenges in VLSI Circuits

As interconnect feature sizes shrink, copper resistivity increases due to surface and grain boundary scatterings and also surface roughness. Furthermore, wires, especially power and ground lines are becoming more and more vulnerable to electromigration because of rapid increases in current densities. The resistance of copper interconnects, with cross-sectional dimensions of the order of the mean free path of electrons in current and imminent technologies, is increasing rapidly under the combined effects of enhanced grain boundary scattering, surface scattering and the presence of the highly resistive diffusion barrier layer. The steep rise in parasitic resistance of copper interconnects poses serious challenges for interconnect delay and for interconnect reliability; hence it has a significant impact on the performance and reliability of VLSI circuits. In order to alleviate such problems, changes in the material used for on-chip interconnections have been sought even in earlier technology generations, for example the transition from aluminum to copper some years back.

Carbon nanotubes (CNTs) exhibit a ballistic flow of electrons with electron mean free paths of several micrometers, and are capable of conducting very large current densities. They are therefore proposed as potential candidates for signal and power interconnections. Because of their extremely desirable properties of high mechanical and thermal stability, high thermal conductivity and large current carrying capacity, CNTs have aroused a lot of research interest in their applicability as VLSI interconnects of the future. Depending on their chirality (the direction along which the graphene sheets are rolled up), CNTs demonstrate either metallic or semiconducting properties.

1.7 Future Interconnects

Some problems persist like crosstalk, skin effect, signal degradation and crosstalk induced propagation delay while working at high frequencies [5]. Electrons transmitted

through metal wires have an information carrying capacity limited by the resistance and capacitance of the cable and the terminating electronic circuits. To overcome such problems, VLSI designers gear up with certain methods and materials, which will be of eminent use in upcoming days, promising ones are carbon nanotube interconnects. Carbon nanotubes exhibit a ballistic flow of electrons with electron mean-free paths of several micrometers, and are therefore capable of conducting very large current densities. Moreover, they posses larger lifetime and less power dissipation as compared to copper interconnect.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

The propagation delay of interconnects is a major factor to determine the performance of VLSI circuits, because the RC time constant of interconnects increase very rapidly as chip and interconnect dimensions are scaled aggressively. To reduce interconnect time delay, properly scaled multilevel conductors, repeaters, cascaded drivers is used and various delay models which yields the optimum cross sectional interconnect dimensions and repeaters configuration that can reduce interconnect time delays by more than an order magnitude. The model proposed [6], a straightforward approach was used to scale interconnect dimensions by the same factor as transistor dimensions. Thus the delay time of local interconnect remained same but the transistor delay decreased by factor 1/S.

To prevent excessive time delay multilevel metal interconnects are essential. Thus all of long distance communication can be accomplished by low resistive metal layers and the cross sectional dimensions of the upper layers can be adjusted to obtain minimum interconnect delay. Multilevel metal can decrease the chip dimensions, and thus further improve the performance.

2.2 Scaling

Analytical expression developed to relate the time delay to various element of technology. Empirical expressions [6] to predict the trends of technological elements as a function of chronological time had been developed. Calculations of time delay of interconnection shows that as the chip area is increased and other device related dimensions are decreased the interconnection time delay becomes significant compared to the device time delay and in extreme cases dominates the chip performance.

During calculation following equation is obtained:

$$\tau = 2*0.89\rho\epsilon_0 K_{ox} \frac{L^2}{WH}\left(\frac{W}{X_{ox}} + \frac{H}{L_s}\right) \quad (2.1)$$

From the above equation we can see that the delay of a wire is a quadratic function of its length. It means that doubling the length of the wire quadruples its delay.

Voltage scaling has been used for reducing power dissipation of interconnects. An undesired effect observed due to voltage scaling is increase in propagation delay [5]. Thus a trade-off lies in between power dissipation and propagation delay with voltage scaling. However, voltage scaling can result in overall reduction of power delay product. It is found that irrespective of interconnect length and technology node, an optimized voltage scaling reduces normalized crosstalk level.

2.3 Delay Models

The Elmore Delay Model is well known as an analytical model for interconnect delays estimation. The popularity of the Elmore delay model is mainly due to the existence of simple tractable formula for the delay [7] making the calculation if the circuit delays highly efficient even in large circuits. No formula for delay calculation has been determined for RLC trees that maintain all characteristics of the Elmore delay model [8]. The absence of an equivalent delay model for RLC trees is primarily due to fact that the Elmore delay model does not cover non monotone response, which can occur in RLC circuit.

Accurate calculation of propagation delay in VLSI interconnects is critical to the design of high speed systems, and transmission line. Elmore delay has been widely used as an analytical estimate of interconnect delays in the performance driven synthesis. However this model cannot be applied to estimate the delay of interconnect lines with ramp input source because it is independent of rise time of input ramp signal. A new analytical model [9] is developed which is based on first and second moments of interconnect transfer function when the input is a ramp signal with finite rise time. This model gives the accurate analytical delay estimate for distributed RLC interconnects under ramp input.

With fast switching speeds and large interconnect trees, the resistance and inductance of interconnect has a dominant impact on logic gate delay. A new Π-model for distributed RC and RLC interconnects to estimate the driving point admittance at the output of a CMOS gate with the help of this model [10] gate delay efficiently computed. Parameters are depended on the total interconnect tree resistance and capacitance at the output of the

gate. That model was useful for iterative optimization of performance-driven routing or for estimation of gate delay and rise times in high level synthesis.

2.4 Repeater Insertion:

Signal propagation on long resistive interconnect lines is a function of the product of the line resistance and capacitance, commonly known as the RC delay. Since both the resistance and capacitance show a linear increase with length, that means the delay increases quadratically with length. Because interconnections have become smaller in cross section and longer in length with each succeeding generation of CMOS technology. Bakoglu [11] presented an analysis based on characterizing the repeater with an input capacitance and an output resistance which was one of the pioneering works in this area.

Friedman in [12] use Sakurai's alpha power model to include the effect of velocity saturation in short channel devices and present an analysis which models inductance in the interconnect for the first time . In Sakurai alpha power law MOS model [13] carrier velocity saturation effect is introduced which is eminent in short channel MOSFET's. This model is an extension of Shockley's square law MOS model in saturation. Using this model, closed form expressions are derived for the delay, the short circuit power, and transition voltage of CMOS inverters.

In large chips, the propagation delay of the data and clock signals can limit performance due to long resistive interconnect. The insertion of repeaters alleviate the quadratic increase in propagation delay with interconnect length while decreasing power dissipation by reducing the short circuit current [14]. The Sakurai alpha power law model is applied to the problem of repeaters to produce design expressions for determining the optimum number of uniformly sized repeaters to be inserted along a resistive interconnect line for reduced delay. For a wide variety of typical RC loads, this analytical repeater model exhibits a maximum error of 16% as compared to a dynamic circuit simulator. The advantage of uniformly sized repeaters versus tapered buffer repeaters is also investigated using the repeater model[12].It is shown that uniform repeaters remain advantageous over tapered buffers and tapered buffer repeaters even with relatively small resistive RC loads.

Another expression based on alpha power law model is introduced [15] for propagation delay of CMOS gate driving a distributed RLC line. It is shown that the error in the

propagation delay if inductance is neglected then interconnect is treated as a distributed RC line can be over 30% for present on chip interconnect. It is also shown that the traditional quadratic dependence of propagation delay on the length of the interconnect for RC lines approaches a linear dependence as inductance effect increases, which is expected to have a profound effect on traditional design methodologies. This model is applied to the problem of repeater insertion in RLC interconnect. Closed form solutions are presented for inserting repeaters into RLC lines that are highly accurate with respect to numerical solution. Thus importance of inductance in high performance VLSI design methodologies will increase as technologies scale.

2.5 Parasitic effects on Interconnects

Semiconductor technologies with feature sizes of several tens of nanometers are currently in development. Distributing robust and reliable power, ground, clock, data, address and other control signals through interconnects in such a high speed, high complexity environment, is a challenging task.

Wide wires are frequently encountered in global and semiglobal interconnect in upper metal layers. These wires are low resistive lines that can exhibit significant inductive effect. Due to presence of these inductive effects interconnects are modelled as distributed RLC transmission lines [5]. These RLC transmission line when running parallel to each other have capacitive and inductive coupling which makes the design of interconnects even more important in terms of crosstalk. In a modern interconnect design, interconnects in adjacent metal layers are kept orthogonal to each other. This is done to reduce crosstalk as far as possible. But with growing interconnect density and reduced chip size, even the non –adjacent interconnects exhibit significant coupling effects are significantly dependent on length of interconnects, distance between them, transition time of the input and the pattern of input.

The inductance of interconnect wire significantly plays a major role in on-chip circuit performance [16]. The inductive and capacitive coupling are more effective when interconnects line run parallel for a long distance and they are quite close each other. The reliability and performance of the circuit is affected by these parasitic.

The mutual inductance depends on flux linkages due to change in current in another wire. The mutual inductance induces current on the victim line and the direction of current follows lenz's law. The mutual capacitance passes current through it that flows in both directions on the victim line.

The coupling capacitance is limited to adjacent neighbours and to adjacent layers in multilayer structure. However, the mutual inductance is not limited to adjacent wires and layers and it exists among all parallel wires. These parasitic leads to crosstalk noise, propagation delay and power dissipation which affect the signal integrity and degrade the performance of the circuit.

Crosstalk is the coupling of energy from one wire to another via coupling parasitic. It adversely affects the circuit operating at high frequencies. It induces glitch fault and delay fault. Glitch fault occurs when the victim line is intended to be stable state and a noise pulse on the net occurs. It induced overshoot and undershoot which leads to false switching and creates logic errors [18]. Delay fault occurs when both aggressor and victim lines have simultaneous transition.

2.6 Interconnect materials

For several semiconductor technology generations, aluminum was used as the on-chip interconnect metal and silicon-di-oxide (SiO_2) as the inter- and intra-level insulator [18].With rapid scaling of feature size to deep submicron levels, the signal delay caused by the interconnect became increasingly significant compared to the delay caused by the gate and thus affecting the circuit's reliability. For decreasing the resistive part of the RC delay, various alternatives to aluminum were considered in early 1990s.

For metallic conductors with electrical resistivity lower than aluminum, the options were targeted to silver, copper, and gold. Although gold has high resistance to electromigration but shows a little improvement in resistivity. Furthermore, adding to its demerit gold creates deep levels in the band gap due to diffusion in silicon and thus affects electronic properties of a device [19]. Copper with close to half the resistivity (1.7mVcm) compared to Al/0.5 percent Cu alloys (3.0mVcm) and with electromigration of the order of ten times better appeared to be most appropriate material for VLSI interconnect. Although

copper also creates deep levels in the silicon band gap, but several materials that can act as diffusion barrier for copper were found.

To prevent copper from diffusing into transistors, it must be encapsulated in a barrier film, usually a derivative of tantalum or titanium. Adding to its merit, copper has a higher melting point (1,357 K) than aluminum (933K), which gives copper the advantage over aluminum in electromigration and stress migration as well.

It was realized in early 2000, that even copper is not able to fulfill the demands of high-speed interconnects. The requirement of lower resistance and higher bandwidth is the major concern in interconnects design with the increase in the integration density of the complementary metal-oxide-semiconductor and higher clock frequency. To accommodate more interconnects in a chip the cross-sectional dimensions are being reduced rapidly, resulting in dimensions reaching to the order of the mean free path of electrons in copper material. Consequently, the effect of surface scattering and grain boundary scattering increases and hence increases the resistivity as the width decreases and degrades the performance copper as an interconnect.

The dimensions of Cu interconnect are scaled with technologies advanced and its resistivity increases due to surface and grain boundary scatterings significantly, as discussed above. Therefore, its performance as interconnect is degraded and conflicts with the high performance requirement, such as high current density, low interconnect delay of advanced integrated circuits. In contrast, metallic carbon nanotube has long mean free path (several micrometers) and can carry extremely high current densities (103 higher than Cu wires). It has been proposed to be possible candidate of the interconnection material for future IC technology [22].

2.7 Future interconnect

The performance and power dissipation of integrated circuits (IC) are largely affected by interconnects. Carbon nanotubes, which are rolls of one-atom thick carbon sheets, show great potential in addressing some of the major interconnect challenges in future generations of technology, when copper conductivity will degrade substantially because of size effects. The fascinating properties of carbon nanotubes include very large current

conduction capacity, large electron mean free paths, high mechanical strength, and stability [23].

Carbon nanotubes (CNTs) are a recently discovered form of carbon, which can be thought of as a rolled-up sheet of hexagonal ordered graphite formed to give a seamless cylinder. They can be 0.4–100 nm in diameter with lengths up to 1 mm. Several single-walled nanotubes (SWCNTs) can be concentrically nested inside each other forming so-called multi-walled carbon nanotubes (MWCNTs). Due to the variety of extraordinary properties exhibited by carbon nanotubes, a large number of possible applications have been proposed. In particular, the high current carrying capacity and mechanical stability of metallic nanotubes indicates applications in microelectronic interconnects whereas the reasonably large band gap of narrow single-walled nanotubes suggests their use as nanoscale transistor elements. Further, due to the small radius of curvature at the tips of the nanotubes, they are ideally suited to low-voltage field emission devices such as flat-panel displays [21].

An SWCN (single walled carbon nanotube) is very close to a one-dimensional (1-D) system of electrons that gives rise to many unique electrical and thermal properties. Since electrons can move in 1-D only, the phase space for scattering in nanotubes is very limited; electrons can be scattered only backward [20]. The mean free path (MFP) in high quality nanotubes, therefore, is in the micrometer range. This is in contrast to a three-dimensional (3-D) metallic wire in which electrons can be backscattered by a series of small- angle scatterings, and MFPs are in the range of a few tens of nanometers. Carbon nanotubes have the potential of being used as both transistors and interconnects as, depending on their chirality, they can be either metallic or semiconductor.

Electrons in CNT flow without scattering over long nanotube lengths, enabling them to carry high currents wit essentially no heating. Whereas, electrons in copper travel only 40-50nm before they scatter. Due to strong sp^2 bonding, carbon nanotubes are much less susceptible to electromigration (EM) problems that plague copper interconnects and can carry extremely high current densities of the order of $10^9 A/cm^2$. Copper interconnects on the other hand have a current capacity of ~10^6 A/cm^2 due to elctromigration [24]. Because of their extremely desirable properties of high mechanical and thermal stability, high

thermal conductivity and large current carrying capacity CNTs are preferred over copper as VLSI future interconnects.

This is also observed that the impedance parameters at the equivalent circuit also depend on CNT diameter and how much delay and power dissipation in CNT bundle interconnect is controlled by constituent tube diameter can be found in [40].

An over view of the exploratory research on CNT as possible VLSI interconnect is presented by [25]. The problem of continuing with copper interconnects in highly scaled technologies of future are briefly discussed. The works carried out in finding an alternative solution indicates that the CNT based interconnects have the potential to replace copper in future. The SWCNT bundle is most desirable form of CNT based interconnect provided all constituent CNTs of the bundle are metallic. The SWCNT has been studied extensively and it is found that isolated tube diameter plays an important role in determining delay and power dissipation. Another parameter of importance is the interconnect length. It is observed that both SWCNT and MWCNT perform better than copper in the semi-global and global levels of interconnect length. At local level performance of copper interconnects is better. In brief, the analyses and simulations reported by various authors show that if a CNT technology compatible with present form of IC technology can be developed, then it will be possible to partially or wholly replace copper interconnect by CNT based interconnect.

CHAPTER 3

INTERCONNECT PARASITIC

3.1 Introduction

Interconnect refers to the metal wires that make electrical connections between the transistor on die. Aluminium and copper are commonly used as interconnect metals. Interconnect has attracted increasing attention over the past few years because of its growing influence on the overall performance of integrated circuit. This has come about by the scaling of device dimensions coupled with the trend to larger die sizes. Currently microprocessor contain about 1Km of interconnect for every square centimeter of die area. Interconnect introduces parasitic capacitances, resistances and inductances that can degrade the overall performance significantly. The interconnect capacitances present considerable loading to circuits, increasing the propagation delays and switching dissipation. The trend toward larger die sizes has also necessitated the use of longer interconnects on the chip. In such long interconnects, the parasitic resistance must be considered as well as capacitance. Then the associated RC delays further degrade the overall circuit performance. In some cases interconnects can be so long that they must be treated as lossy RLC transmission lines rather than RC networks.

3.2 Transmission line Effect

Usually, when a wire is longer than 1/10 wavelength of the signal frequency component that is transmitted, neglecting the wave nature of the signal propagated on it will result in obvious error in analysis. The wave nature of the signal presents a spatial variation of signal amplitude across interconnect due to a phase difference. Such a line is electrically long and needs to be modeled as a transmission line. When a wire is a transmission line, the signals that propagate on it behave as traveling waves. As the traveling waves see discontinuities on the line, reflection waves will occur.

The discontinuity of a transmission line is defined as any change in impedance of the line. A few of the basic discontinuities are series inductance, shunt capacitance, capacitive

loads, impedance steps, and unmatched terminations. They are introduced by physical changes of the signal paths such as vias, wire bends, stubs, wire crossovers, bonding wires, package pins, connectors, and non-ideal receivers.

3.3 Interconnect Delay Model

The interconnect delay model in VLSI has been improved as technology is scaling. In early VLSI design, interconnects were modeled as a lumped capacitive load for gates. It ignored resistance of wires. As feature sizes decrease, wire resistance increases, invalidating this approximation. The resistance of interconnects can be taken into account by approximating the distributed RC structure using a lumped RC tree. One of the most popular RC delay models is based on the Elmore time constant [7].

The RC tree model is inadequate to accurately model delay, because RC models cannot model higher-order under-damped systems. A second or higher order RLC model of the interconnect can provide significant improvements over the accuracy of a first-order RC delay model, since RLC trees and higher order transfer functions may have oscillatory output voltages, and are thus able to predict increased delays due to settling times of interconnect waveforms.

3.4 Types of interconnects:

Interconnects can be global, semi global or local. In general, local interconnects are the first, or lowest, level of interconnects. They usually connect gates, sources and drains in MOS technology, and emitters, bases, and collectors in bipolar technology. They generally consist of very thin lines and used for very short interconnects at the device level.

- **Semi global** interconnects provides the connectivity between large modules and input/output circuitry. They are generally wider and taller than local interconnects in order to provide lower resistance. They provide clock and signal distribution within a functional block with typical lengths up to 3 to 4mm.

- **Global interconnects** provides clock, power and long distance communication between functional blocks and deliver ground to all functions. They occupy the

top one or two layers, and they are longer than 4mm as long as half the chip parameter.

- **Local interconnects** can afford to have higher resistivity than global interconnects since they do not travel very long distances. But they must also be able to withstand higher processing temperatures. Global interconnects travel over large distances, between different devices and different parts of the circuit, and therefore are always low resistant metals.

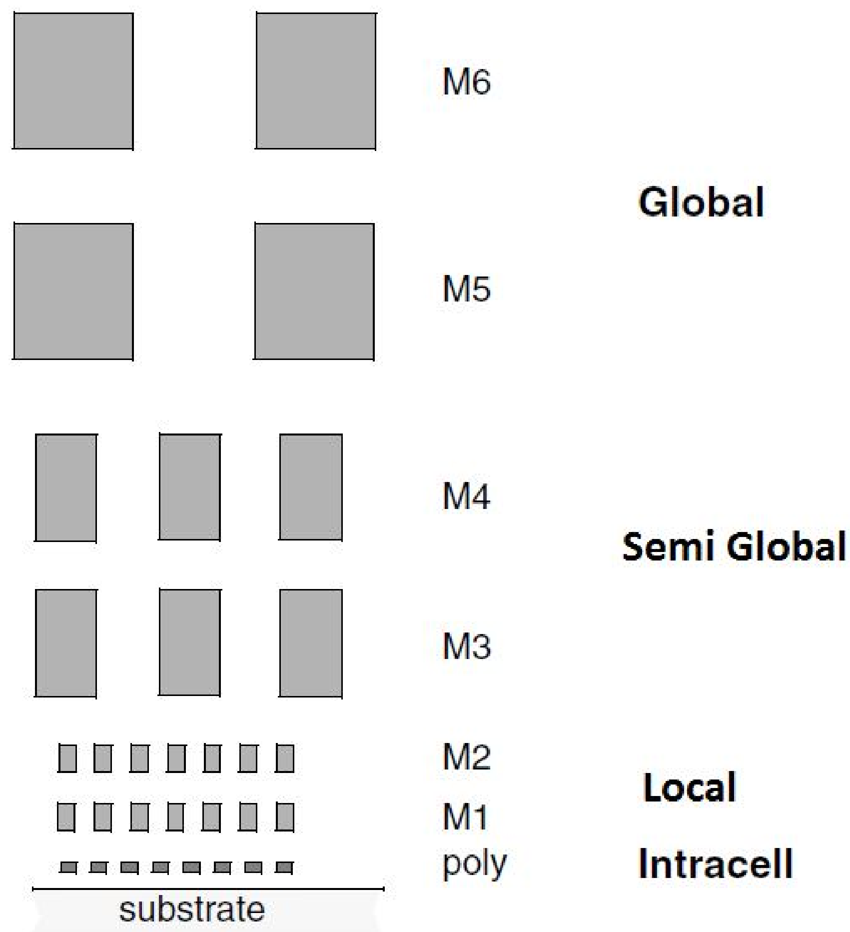

Fig. 3.1 Interconnect hierarchy of 0.25µm CMOS process [26]

Parasitic cause an increase in propagation delay, increase energy dissipation and affect the power distribution, introduce extra noise sources, which affect reliability of the circuit.

3.5 Parasitic of interconnects

Interconnect introduces capacitive, resistive and inductive parasites. All three have multiple effects on the circuit behaviour. Interconnect parasites cause an increase in propagation delay, increase energy dissipation and affect the power distribution, introduce extra noise sources, which affect reliability of the circuit.

3.5.1 Capacitive Parasitic

The capacitance is the most important parasitic introduces by interconnect wires. Some of the capacitance appears between interconnect and ground. Another component appears between wires on a single level and is called interwire capacitance. There are also capacitances between interconnect and wires on other levels, the interlevel capacitance.

An unwanted coupling from a neighbouring signal wire to a network node introduces an interference that is generally called cross talk. The resulting disturbance acts as a noise source and can lead to hard-to-trace intermittent errors, since the injected noise depends upon the transient value of the other signals routed in the neighbourhood. In integrated circuits, this inter signal coupling can be both capacitive and inductive. Capacitive cross talk is the dominant effect at current switching speeds, although inductive coupling forms a major concern in the design of the input-output circuitry of mixed-signal circuits.

A crosstalk induces glitch occurs when the victim line is intended to be stable state and noise pulse on the net occurs. It induced overshoot and undershoot generated at circuit node can cause false switching and creates a logic error. It induced delay when the aggressor and victim lines have simultaneous transitions. It may cause chip failure. How it takes place we can see with the help of following diagram.

Assume that the inputs to the three parallel wires X, Y and Z experience simultaneous transitions. Wire Y (called the victim wire) switches in a direction that is opposite to the transitions of its neighbouring signals, X and Z. The coupling capacitances experiences a voltage swing that is double the signal swing, and thus represent an effective capacitive load that is twice as large as C_C. It has major impact on the propagation delay of the circuit.

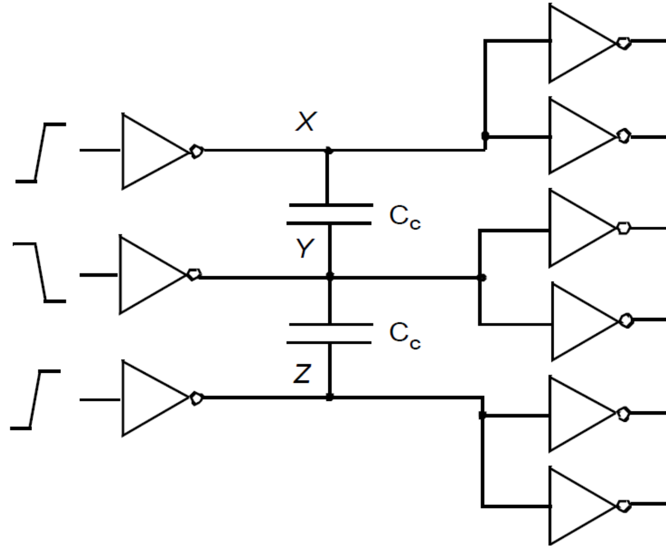

Fig. 3.2 Impact of crosstalk on propagation delay [26]

3.5.2 Resistive parasitic

Current flowing through a resistive wire results in an ohmic voltage drop that degrades the signal levels. This is especially important in the power distribution network, where current levels can easily reach amperes. Beyond causing a reliability risk, IR drops on the supply network also impact the performance of the system. A small drop in the supply voltage may cause a significant increase in delay. The resistance of a wire is proportional to its length *L* and inversely proportional to its cross-section *A*.

At very high frequencies however, an additional phenomenon called the skin effect comes into play such that the resistance becomes frequency-dependent. High-frequency currents tend to flow primarily on the surface of a conductor with the current density falling off exponentially with depth into the conductor. The skin depth [26] is defined as the depth where the current falls off to a value of e^{-1} of its nominal value, and is given by with *f* the frequency of the signal and m the permeability of the surrounding dielectric. For Aluminium at 1 GHz, the skin depth is equal to 2.6 mm.

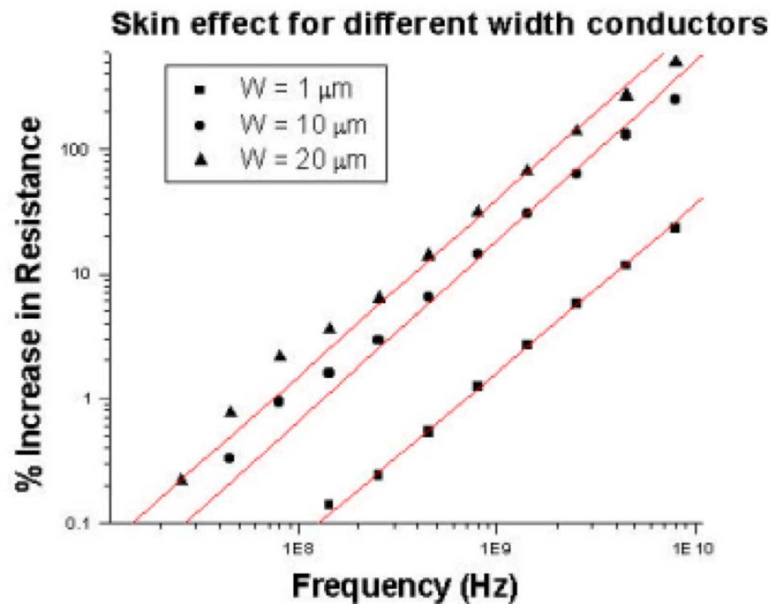

Fig. 3.3 Skin-effect induced increases in resistance as a function of frequency and wire width. All simulations were performed for a wire thickness inductance [26].

3.5.3 Inductive Parasitic

Besides having a parasitic resistance and capacitance, interconnect wires also exhibit an inductive parasitic. An important source of parasitic inductance is introduced by the bonding wires and chip packages. Even for intermediate-speed CMOS designs, the current through the input-output connections can experience fast transitions that cause voltage drops as well as ringing and overshooting, phenomena not found in *RC* circuits. At higher switching speeds, wave propagation and transmission line effects can come into the picture. During each switching action, a transient current is sourced from (or sunk into) the supply rails to charge (or discharge) the circuit capacitances. Change in the transient current creates a voltage difference between the external and internal supply voltages. This situation is especially severe at the output pads, where the driving of the large external capacitances generates large current surges. The deviations on the internal supply voltages affect the logic levels and result in reduced noise margins.

As the interconnect lines run parallel for a long distance and they are quite close to each other, this leads to significant coupling. The mutual inductance depends on flux linkage due to change in current in another wire. The value of mutual inductance between two

lines depends on the value of inductance of each line, their separation, the strength of current and its rate change.

The mutual inductance induces current on the victim line and the direction of the current follows Lenz's law. The mutual inductance is not limited to adjacent wires and layers and it exists among all parallel wires. It leads to propagation delay and power dissipation which affects the signal integrity and degrade the performance of the circuit [26].

Yet with the adoption of low-resistive interconnect materials and the increase of switching frequencies to the super GHz range, inductance starts to play a role even on a chip. Consequences of on-chip inductance include ringing and overshoot effects, reflections of signals due to impedance mismatch, inductive coupling between lines, and switching noise due to $L\frac{di}{dt}$ voltage drops. The inductance of a section of a circuit can always be evaluated with the aid of its definition, which states that a changing current passing through an inductor generates a voltage drop.

3.6 Scaling in interconnect

For larger circuits, the time delays associated with the interconnections can play a significant role in determining the performance of the circuit. As the minimum feature size is made smaller, the area of cross section of the interconnection also reduces. At the same time, a higher integration level allows the chip area to increase, causing the length of the interconnections to increase. The net effect of this scaling of interconnections is reflected into an appreciable *RC* time delay. For a very large chip with extremely small geometries, the time delay associated with interconnections could become an appreciable portion of the total time delay, and hence the circuit performance could no longer be decided by the device performance. The time delay associated with the interconnections is dependent upon two factors; the resistance of the interconnections and capacitance controlled by dielectric media.

For local interconnects, length also shrinks as technology node. Therefore, the net result is that the time delay for local interconnects stays approximately constant according to the scaling scheme [6]. However, for global interconnects as the technology progresses, the length of the global interconnects usually increases rather than shrinks. This is because

the chip area of each new technology generation usually keeps increasing forcing the global interconnects to increase in length to connect up all the areas of devices. The average length of the longest global interconnects in a circuit can be approximated by [6]:

$$L_{max} = \frac{\sqrt{A}}{2} \quad (3.1)$$

Where A is the chip area and L_{max} is the maximum length of global interconnects. From this equation it can be seen that interconnect delay is based on the global interconnect because as the length increases, parasitic capacitance and resistance also increases and hence delay increases. So scaling of global interconnect is more important as compared to local interconnect. So in the following scaling table global interconnect is scaled by Sc (where Sc < 1) local interconnect is scaled by factor S (where s > 1) and constant wire length is scaled by factor 1. The average length of these long wires is proportional to the die size (or complexity) of the circuit. An interesting trend is that while transistor dimensions have continued to shrink over the last decades, the chip sizes hence actually increased gradually over the same period. So while we have to study the scaling behaviour of the wire length.

Table 3.1 Scaling of Interconnect [6]

Interconnection Parameter	Scaling Factor(S)
Long distance interconnection dimensions H, W, Ls	1/S
Long distance interconnection dimensions L_{max}	Sc
Line resistance $R = L_{max}/WH$	S^2Sc
Line capacitance $C_{OX} = K_{OX}\varepsilon_0 LmaxW/X_{OX}$	Sc
Interelectrode capacitance $C_I = K_{OX}\ \varepsilon_0 L_{max}H/Ls$	Sc
Line response Time RC	S^2Sc^2
Line voltage drop IR	SSc
Line current Density	S

Where X_{OX} and K_{OX} are the SiO_2 thickness and dielectric constant, ϵ_0 is the permittivity of free space. Ls is the separation between two interconnects. H, L and W are the length, height and width of interconnects.

3.7 Delay Estimation

The time delay associated with the interconnection is dependent upon two parameters; the resistance and the capacitance associated with the interconnections. The resistance of an interconnection line of length, width W, thickness If, and resistivity ρ is given by

$$R = \frac{\rho L}{WH} \quad (3.2)$$

Assuming a parallel-plate capacitance model, the capacitance between the interconnection and the silicon substrate is given by:

$$C_{ox} = K_{ox}\varepsilon_{ox} \frac{WL}{Xox} \quad (3.3)$$

Where X_{OX} and K_{OX} are the SiO_2 thickness and dielectric constant, respectively, and εo is the permittivity of free space. The capacitance between the two adjacent interconnections separated by a distance of *Ls* is given by

$$C_I = K_{ox}\varepsilon_{ox} \frac{HL}{Ls} \quad (3.4)$$

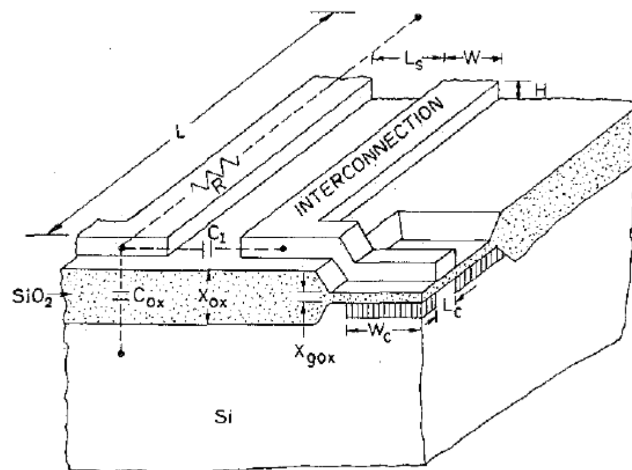

Fig. 3.4 Parasitic associated with interconnects [6].

Where it has been assumed that the dielectric between them is SiO_2. The total line capacitance is given by

$$C_T = 2(C_{OX} + C_I) \tag{3.5}$$

The time it takes the output to reach from 10% to 90% of its final value, defined as rise time τ, is 0.89 RC. It will be used as a figure of merit for interconnects line [6].

$$\tau = RC_T \tag{3.6}$$

From equation the value delay is given by following equation:

$$\tau = 2{*}0.89\rho\epsilon_0 K_{OX}\frac{L^2}{WH}\left(\frac{W}{X_{OX}} + \frac{H}{L_S}\right) \tag{3.7}$$

So from the above equation we can see that the delay of a wire is a quadratic function of its length. It means that doubling the length of the wire quadruples its delay.

3.8 Insertion of repeaters

In large chips the propagation delay of the data and clock signals is limited due to long resistive interconnect. Repeater insertion is a well-known design technique to reduce the delay required to propagate a signal along a line. The proper insertion of repeaters alleviates the quadratic increase in propagation delay with interconnects length while decreasing power dissipation by reducing short circuit current. These repeaters are inserted within different types of common resistive interconnect structures. We can say Repeater insertion is a technique for reducing the time delay associated with long wire lines in integrated circuits. The technique involves the division of long wire interconnect into smaller sections and inserting a repeater between each new pair of short wire. It can be done by inserting a buffer at the beginning and at the end of the interconnect line to improve the delay and slew rate of the signal.

It is the propagation delay when buffer is not inserted in interconnects. By breaking a long interconnect into n smaller lines the propagation delay of each is reduced quaderatically [6].

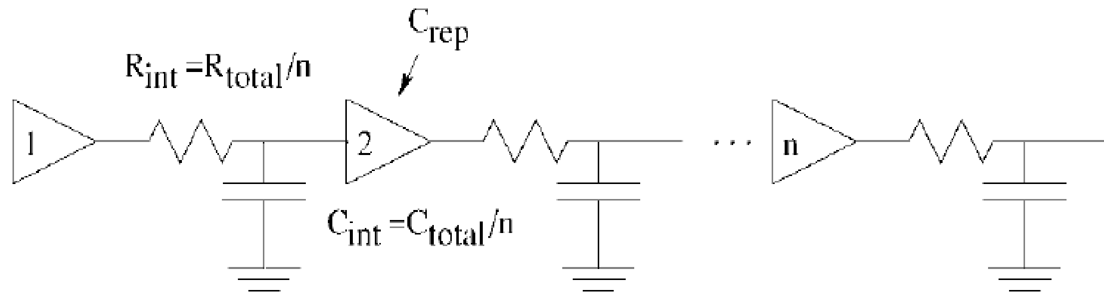

Fig. 3.5 n equal sized CMOS inverting repeaters driving an RC load [12]

There exists an optimal length of wire segment between the repeaters. We call this the critical length. So inserting repeaters to reduce the delay of a wire only makes sense when the wire is at least two times longer than critical length.

If the number of repeater is too small, the delay due to interconnect will dominate. If the number of repeater is too large, the repeater delay dominates. So the optimal number of repeaters that minimizes the overall delay must be considered. The advantage of repeater insertion is reducing the coupled noise from adjacent interconnects.

3.9 Copper interconnect

For several decades aluminium was used as the on chip interconnects metal and SiO_2 as insulator in between interconnects. Due to rapid scaling in die size the signal delay caused by interconnects become increasingly significant as compared to the delay caused by the gate. The interconnect delay is worse affected by capacitive and resistive parasitic. In earlier decades various alternatives to aluminium were considered, among them silver, copper and gold were considered, so that resistive part of RC delay can be decreased by using low resistive metals as compared to aluminium (bulk resistivity 2.65µΩcm). Gold leads to deep levels in the silicon band gap and diffuses in SiO_2 and affects electronic properties of device. Gold (bulk resistivity 2.4µΩcm) also has high resistance to electro migration but due to above demerit it was not preferred [27]. Although silver (bulk resistivity 1.6µµcm) has the lowest resistivity among them but due to low melting point and low resistance to electro migration so it was not preferred.

Copper with close to half resistivity (1.7µΩcm) compared to aluminium alloy (3.0µΩcm) and with electro migration of the order of ten times better appeared to be the most

appropriate for the VLSI interconnect. Copper has higher melting point (1357K) as compared to aluminium (933K) which gives copper the advantage over aluminium in electro migration and stress migration as well. The typical VLSI application temperature range (~373K) is about 40 percent of the aluminium at room temperature. Although copper also creates deep levels in silicon band gap, but several materials that can act as diffusion barrier for copper were found. To prevent copper from diffusing into transistors, it must be encapsulated in a barrier film, usually a derivative of titanium. So copper is widely used as on chip interconnect for advanced ICs.

Since copper film has almost 35% lower bulk resistivity than aluminium. It is expected that the number of interconnecting lines with copper will be less than the number required with aluminium. It has been estimated that a reduction of almost 40% in the RC time constant can be achieved by using copper rather than aluminium. In other words we can say that the speed of circuit will be faster with copper interconnects compared to aluminium interconnects.

3.9.1 Electro migration

Electro migration is the result of momentum transfer from the electrons to the ions which make up the lattice of the interconnect metal. In aluminium (Al), electro migration is a grain boundary diffusion phenomenon whereas in copper (Cu) it is a surface diffusion phenomenon, because of the damascene structure. As the line-widths become comparable to the grain size, the electrical, mechanical and physical characteristics of the metal lines can no longer retain the properties of the bulk material. In addition to that, metallic lines experience very high current densities, which lead to reliability issues like, electromigration, void formation, hillock formation, track thinning, and stress as shown in following figure. Generally electron migration is the forced mass transport in electrical conductor due to momentum exchange between the large flux of conduction electrons (electron winds) and diffusing metal atoms [28].

3.9.2 Grain boundary effect

As the width of the interconnecting Copper line decreases, it shows a long distribution of grain size, and a short distance between scattering barriers. As a result, the effective

resistivity of the Copper line increases due to the scattering from the sidewall and from the grain boundary. Copper electrical resistivity proportional to the grain boundary area per unit volume and smaller the grain size gives rise to larger numbers of grain boundaries per unit volume. The grain boundaries impose additional resistance on the total grain resistance.

3.9.3 Drawbacks of copper interconnect

In last decade it was found that even copper is not able to fulfil the demands of high speed interconnects. The requirement of lower resistance and higher bandwidth is the major concern in interconnects design with the increase in integration density of devices and higher operating clock frequency. The cross sectional area reduced rapidly to accommodate more interconnects in a chip, resulting in dimensions reaching to the order of the mean free path of electrons. The resistivity of copper interconnects is increasing rapidly under the effects of enhanced grain boundary effect, electromogration and surface scattering, larger interconnect length and higher operating frequency.

Increase in wire resistance due to scaling has caused more voltage drop and power consumption at constant voltage through wires. However, it is expected that the use of superconducting wires for global interconnects might be a possible avenue for reliable performance of global interconnects in the near future.

Thus alteration in copper interconnect technology is required because copper interconnect is limited by skin effect, dispersion, signal degradation, power dissipation and electromagnetic interference at high frequency. Electron transmitted through metal wires has an information carrying capacity limited by the resistance and capacitance of the cable and the terminating electronic circuits. So to overcome such problem we are in search of methods and materials, which will be of eminent use in upcoming days, promising one are CNTs (carbon nanotubes). Research activities in this field shows that metallic carbon nanotube (CNT) is a potential candidate for next generation of interconnect.

CNTs (carbon nanotubes) exhibit a ballistic flow (the chance of scattering event will be low and most of the electron will transported without scattering) of electron mean free paths of several micrometers and therefore capable of conducting very large current

densities. They will possess larger life lifetime compares to copper interconnect. It is believed that CNT shall outperform copper interconnects in near future.

3.10 Introduction to Carbon Nanotube

Carbon nanotube (CNT) is hollow cylinders of graphite sheets with nanometer radius and length ranging from hundreds of nanometers to microns even milimeters. They can be looked at as quasi one dimensional crystal with translational periodicity along the tube axis. There are infinitely many ways to roll a sheet into a cylinder, resulting in different diameters and microscopic structures of the tubes. These are defined by chiral angle, the angle of hexagon helix around the tube axis. They usually come in a variety of forms, including single wall and multi wall, semiconducting and metallic, bundles, networks or isolated, and in a broad distribution of chiralities.

CNTs are fullerene-related structures that consist of graphene cylinders closed at either end with caps containing pentagonal rings. One can get both the ends closed, or one end open, or even both ends open. They can be classified into single walled (SWNT) or multi walled nanotube (MWNT), and each has its advantage or disadvantage depending upon the application in which it is to be used. Single-walled nanotubes are a single sheet of graphite rolled into a cylindrical form. They differ from MWNT in the sense that all of their atoms form single covalently bound network. Single walled nanotubes can further be classified into armchair, zigzag, or chiral structures depending on their wrapping angle. MWNT consist of many concentric cylinders, one inside the other and different walls or layers have interactions with each other.

SWNT consist of singular graphene cylindrical walls with diameters ranging between 1 and 2nm. MWNTs have thicker walls, consisting of several coaxial graphene cylinders separated by spacing (0.34nm) that is closer to interlayer distance in graphite. The outer diameters of MWNTs range between 2 and 25nm and the inner hollows range from ~1 to 8nm.

Table 3.2- Comparison between SWNT and MWNT [29]

Sr.No	SWNT	MWNT
1	Single layer of graphene.	Multiple layer of graphene.
2	Catalyst is required for synthesis.	Can be produced without catalyst.
3	Bulk synthesis is difficult as it requires proper control over growth and atmospheric condition.	Bulk synthesis is easy.
4	Purity is poor.	Purity is high.
5	A chance of defect is more during fictionalization.	A chance of defect is less but once occurred it's difficult to improve.
6	It can be easily twisted and are more pliable.	It cannot be easily twisted.

3.11 Structure of Carbon nanotube

A tube made of a single graphite layer rolled up into a hollow cylinder is called a single walled nanotube (SWNT); a tube comprising several, concentrically arranged cylinders are referred to as a multiwall tube (MWNT). Single wall nanotubes are produced by laser ablation, high pressure CO conversion. Single walled tubes form hexagonal-packed bundles during growth process. The wall to wall distance between two tubes is in the same range as the interlayer distance in graphite ($3.41A^0$). Multiwall nanotubes have similar lengths to single-walled tubes, but much larger diameters. Their inner and outer diameters are around 5 and 100nm, respectively. Because the microscopic structure of carbon nanotubes is closely related to grapheme, the tubes are usually labelled in terms of grapheme lattice vectors.

The way the graphene sheet is rolled determines the fundamental properties of carbon nanotube. There are many possible ways to roll up a graphene sheet into a cylinder with the hexagons to be completed. The roll up vector is termed as chiral vector(C) and is defined as $na_1 + ma_2$, where a_1 and a_2 are the basis vector the graphene lattice; n and m are

the so called chiral indices. By using unit vectors a_1 and a_2 with chiral indices n and m, geometric parameters of carbon nanotube can be defined.

Carbon nanotubes have very high aspect ratios are essentially all surface are. The two main aspects of nanotubes that determine their electrical properties are diameter and chirality. If the nanotube is envisioned as rolled graphite sheet, the tube's chirality is determined by how the sheet attaches to itself. The chiral vector C represents where the graphite sheet attaches to itself to form the nanotube. The vector is directed along the circumference of the tube and normal to its axis. The magnitude of the vector is equal to the diameter of the tube, while its direction indicates its chirality. Carbon nanotubes have three distinct categories classifying their chirality: armchair, zigzag and chiral tubes. Tubes are also classified as being either metallic or semi conducting. All armchair tubes, described by n = m, are metallic. Zig-zag tubes, described by m=0, are metallic if n is a multiple of three. The condition for a nanotube to be conducting can be stated as the difference between n and m must be a multiple of three or zero. The conditions for the nanotubes to be metallic are equivalent to the chiral vector intersecting the points were valence and conduction bands in the first brillouin zone of the equivalent graphite sheet are degenerate and therefore no band gap occurs. For the tubes having a band gap, the band gap is inversely proportional to the diameter of the tube [31].

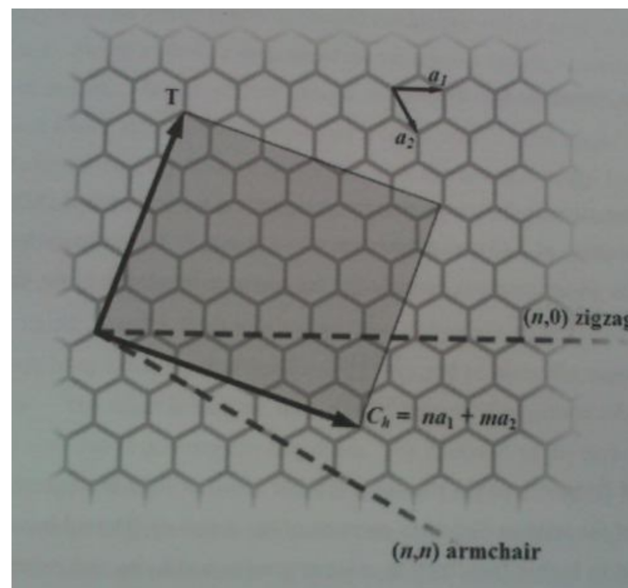

Fig. 3.6 Illustration of chiral vector C in terms of vector a_1 and a_2 [42]

In order to describe such a fundamental characteristic of the nanotube, two vectors, C and T. C is the vector that defines the circumference on the surface of the tube connecting two equivalent carbon atom and T is translation vector that aligned along the cylindrical axis. It will be more clear from the above diagram.

The chiral angle is used to separate carbon nanotube into three classes differentiated by their electronic properties: armchair ($n = m$, $\theta = 30^0$), Zig-zag ($m = 0$, $n>0$, $= 0^0$) and chiral ($0 < |m|<n$, $0< \theta<30^0$). Armchair carbon nanotubes are metallic (a degenerate semiconductor with zero band gap). Zig-zag and chiral nanotubes can be semiconductor depend on their band gap.

3.12 Electronics Property of carbon nanotube:

The most exciting of nanotube properties relates to its electronic band structure. CNTs can be metallic or semiconducting, depending on their helicity and diameter. The armchair tubes are always metallic, whereas the zigzag and chiral tubes can be either metallic or semiconducting.

The electronic conduction process in nanotubes is quantum confined, because, in the radial direction, the electrons are confines in the singular plane of the graphene sheet. The conduction process occurs in armchair (metallic) tubes through gapless modes because the valance and conduction bands always cross each other at Fermi energy for a certain wave vector. In most of the chiral tubes, where the unit cell contains a large number of atoms, the one-dimensional band structure shows an opening of the gap at Fermi energy and, hence has semiconducting properties. When the diameter of the tubes increases, the band gap (which varies inversely with the tube diameter) tends to zero, yielding a zero-gap semiconductor that is essentially equivalent to the planar graphene sheet. Hence, in a MWNT, the electronic structure of the smallest inner tubes is superimposed by several outer, larger planar graphene like tubes.

The electronic properties of the nanotube depend on the diameter and the direction in which the sheet has been rolled up. Some nanotubes are metals with high electrical conductivity, while others are semiconductors with relatively large band gaps. Because of the interaction between different layers of multi-walled carbon nanotubes, it is difficult to

predict their electronic nature. The interlayer interaction is expected in MWNTs but they show no electronic-scattering behavior. These tubes carry such high current density that it

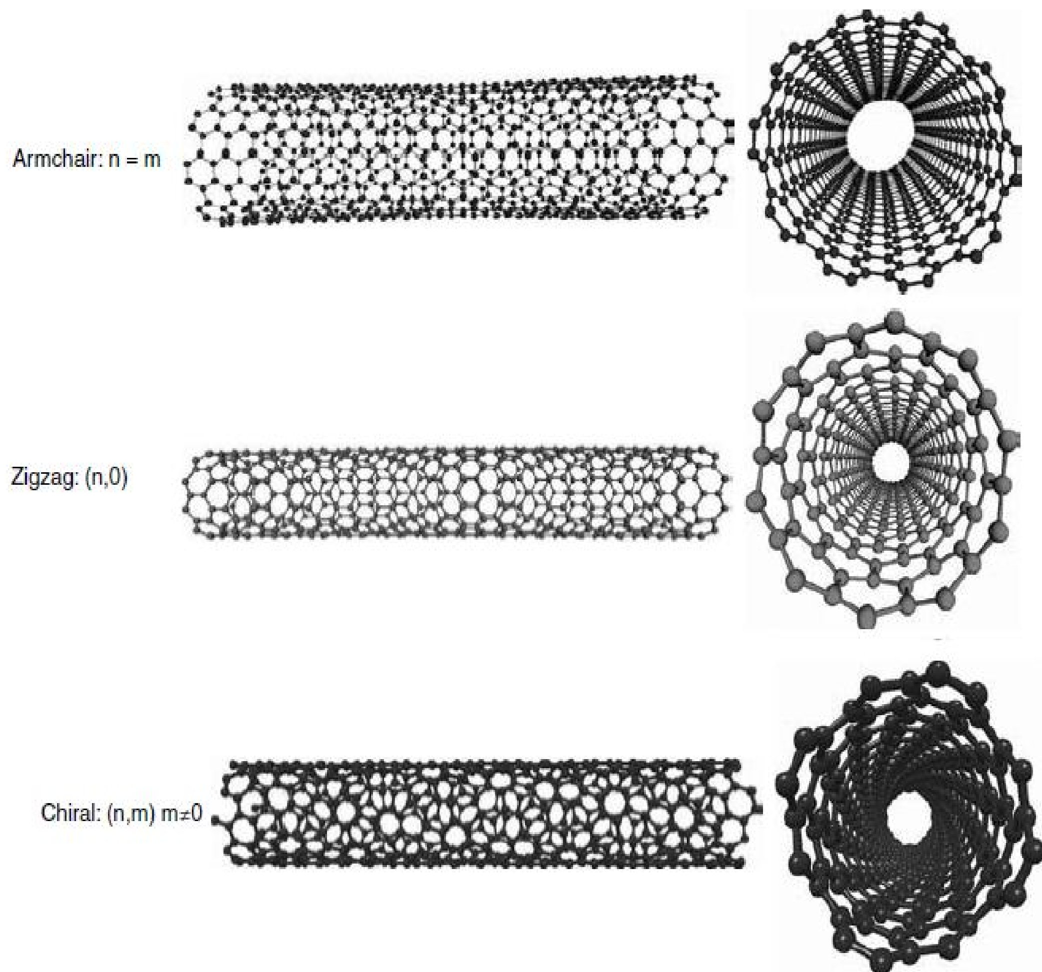

Fig. 3.7 By rolling a graphite sheet in different directions, two typical nanotubes can be obtained: zigzag (n, 0), armchair (m, m) and chiral (n, m) where n>m>0 by definition [30].

should heat the nanotube to its vaporization temperature. But electrons are thought to be strongly de-coupled from the lattice and, hence the heat is not transferred to the lattice.

3.13 Ballistic flow in CNT

Ideally any perfect metal tube should be a ballistic conductor. In the ballistic conductor, the resistance is independent of the length of the conductor. In other words, all electrons that are injected at one end of the tube should reach the other end without a single electron being lost [29]. The electronic transport is ballistic when the length of the

conductor is smaller than the electronic mean free path. On the other hand, diffusive conductors follow ohm’s law and, hence, depend upon the length of the conductor.

In the band structure of metal carbon nanotubes, there are two distinct linear bands in contrast to single band in normal metals. One band is formed by bonding molecular orbitals and another one is formed by anti-bonding molecular orbitals, and the electrons move in opposite directions in these two bands. Thus it is very unlikely that the electron moving in one direction will change direction as then it has to move to another band i.e. another molecular orbital for changing direction. This keeps them moving in a single direction, and that means no scattering and, hence ballistic nature.

Basic electrical properties of semiconducting carbon nanotubes change when they are places inside a magnetic field. The band gap of semiconducting nanotubes narrowed down steadily in the presence of a strong magnetic force. It is anticipated that at very high magnetic fields, the band gap may even disappear completely and the nanotubes can become a metal [29].

3.14 Synthesis of carbon nanotube:

Carbon nanotube synthesis is the method of production used to create carbon nanotubes. They are essentially constructed of a lattice work sheet of graphite that is rolled into a cylindrical shape It can occur naturally through flame synthesis, the most common methods of used in modern science include laser ablation, arc discharge and chemical vapour deposition.

Synthesis of carbon nanotube can be done the following ways

1. Arc discharge method
2. Chemical vapour deposition
3. Laser ablation (vaporization).

A brief introduction to the above process is given in the following table.

Table 3.3 Summary and comparison of the three most common methods of synthesis used for the preparation of carbon nanotubes [29].

Method	**Arc discharge method**	**Chemical Vapour deposition**	**Laser ablation**
MWNT	Short tubes with inner diameters of 1-3nm and outer diameters of approximately 10nm	Long tubes with diameters ranging from 10-240nm	Technique is too much expensive. MWNT synthesis is possible.
Production	Can easily produce SWNTs and MWNTs. SWNTs have few structural defects.	Easiest to scale up to an industrial production; long length , simple process, SWNT diameter controllable	Primarily SWNTs, with good diameter control and few defects.
Conclusion	Tubes tend to be short with random sizes and directions; often needs a lot of purification.	CNTs are usually MWNTs and often riddled with defects.	Costly technique, because it requires expensive lasers and high power requirement.

CHAPTER 4

EQUIVALENT CIRCUIT MODEL OF CARBON NANOTUBE AND COPPER AS INTERCONNECT

4.1 Introduction

The analysis of copper and one dimensional CNT bundle as interconnects for VLSI circuit is done in the chapter. A model is developed to calculate equivalent circuit parameters for a CNT bundle and copper based on interconnect geometry. Using this model, the performance of CNT bundle interconnects at global, local and intermediate level is compared to copper wires. It is shown that CNT bundles can outperform copper for long intermediate and global interconnects, and can be engineered to compete with copper for local level interconnects.

For analytical model equivalent resistance, capacitance and inductance is calculated using equations (given below) for CNT bundle and copper interconnects. On the basis of these parasitic analytical model is designed. Delay is determined at global, local and intermediate level for CNT bundle and compared with copper. This delay analysis is done using Tanner EDA tools in which simulation is done with the equivalent circuit SPICE files.

4.2 Equivalent Circuit model of Copper interconnect

The winbond TSM model [33] is for top global layer interconnect lines with coupling above one ground. According to the model, the thickness of the interconnect is t, the width of CNT bundle is w, and h is the height of the interconnect above the ground. The spacing between the interconnect S is assumed to be equal to the interconnect width, i.e. S = W in figure 4.1.

4.2.1 Equivalent resistance

Based on this model, the resistance of a CNT bundle of length L is given by following equation where ρ is the resistivity of copper,

$$R = \frac{\rho l}{wt} \tag{4.1}$$

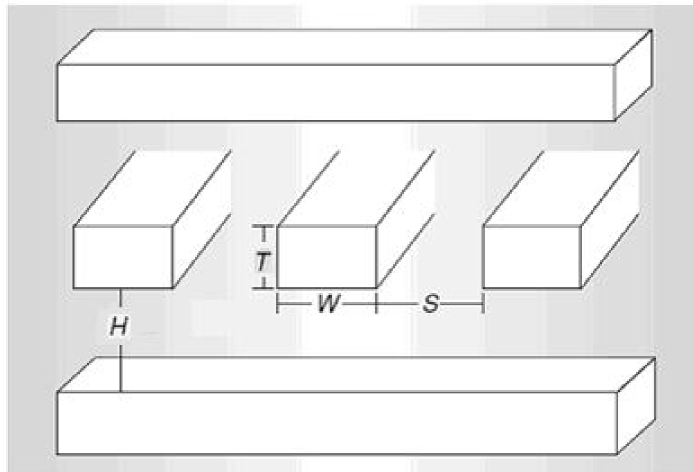

Fig. 4.1 Geometry of Global Interconnect [32]

4.2.2 Equivalent Capacitance

The total effective capacitance of the copper interconnect is given by

$$C_g = \varepsilon\left[\frac{w}{h} + \left\{2.22\left(\frac{s}{s+0.7h}\right)^{3.19}\right\} + \left\{1.17\left(\frac{s}{s+1.51h}\right)^{0.76}\left(\frac{t}{t+4.53h}\right)^{0.12}\right\}\right] \tag{4.2}$$

Where ε_o is the dielectric permittivity; and ε_r is the relative dielectric permittivity of copper

$\varepsilon = \varepsilon_r \times 8.86 \times 10^{-12}$

Thickness t is determined by $t = 3 \times W$ (width of interconnect)

4.2.3 Equivalent Inductance

Inductance associated with copper interconnect is given by the following expression:

$$L_s = \frac{\mu_o l}{2\pi}\left[ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{0.22(w+t)}{l}\right] \tag{4.3}$$

Whereas mutual inductance M is given by the following expressions

$$M = \frac{\mu_o l}{2\pi}\left[ln\left(\frac{2l}{d}\right) - 1 + \frac{d}{l}\right] \tag{4.4}$$

Where μ_o is the permeability and given as $\mu_o = 4\pi \times 10^{-7}$

Due to high density of interconnect the pitch (space in between interconnects) s is assumed equal to the w width of interconnect i.e. s = w. Hence the distance between layers of interconnect d is assumed to be equal to the twice the interconnect width.

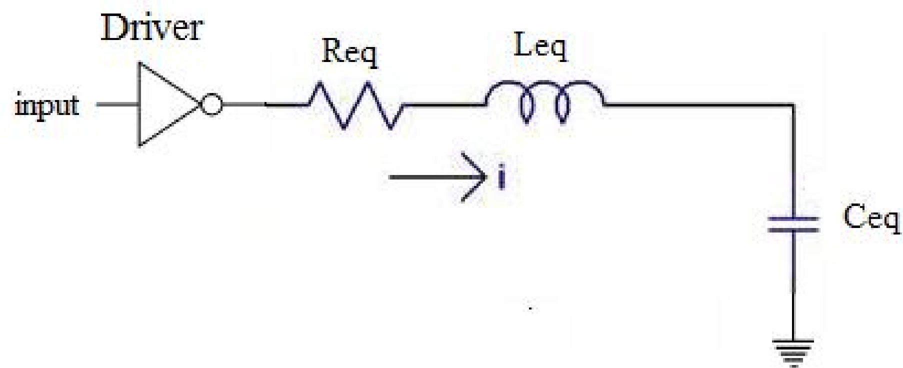

Fig. 4.2 Equivalent Circuit model of copper interconnect

4.3 Equivalent Circuit Model for Carbon nanotube

The interconnect behavior of carbon nanotube is described by the transmission line with an RLC model as shown in following figure. Equivalent circuit model of isolated single walled carbon nanotube (SWCNT) is used for simulation because it is more convenient than Multiwall carbon nanotube (MWCNT). This model is taken from Luttinger Liquid Theory proposed by PJ Burke [34]. The model and its component are explained in the following subsection.

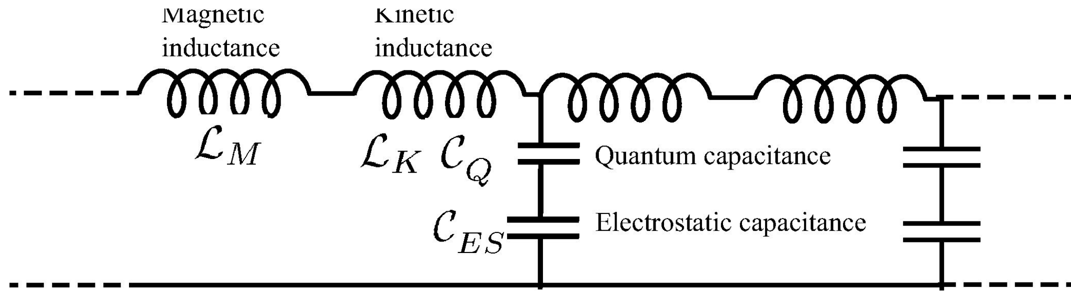

Fig. 4.3 Luttinger theory model [34]

4.3.1 Resistance of Isolated SWCNT

The diffusive component R was not modeled and was taken in ballistic limit. In such case, intrinsic impedance (also called contact or quantum resistance) is given by h/e^2 where e is the electronic charge and h is the planks constant.

In CNTs, the quantization is in circumferential direction due to its ultra small diameter. This causes large energy spacing between 1-D sub-bands. Therefore when an electron jumps from a 3-D metal contact to a 1-D system like CNT it sees only two sub bands near its Fermi energy. These two sub bands are present due to the orbital degeneracy. As the conductance quantum for each sub band is e^2/h, therefore an electron will see combined conductance of $2e^2/h$. In addition to this each sub band can accommodate two electrons of different spins.

Due to spin degeneracy and sublattice degeneracy of electrons each nanotube has four conducting channels in parallel. Therefore the total conductance will be $4e^2/h$ or 155µS. In resistance terms this corresponds to 6.5kΩ. Hence, the minimum resistance that an electron will see when it enters a nanotube is 6.5kΩ; this is independent of nanotube length or chirality. Resistance is given by the following expression

$$R_F = \frac{h}{4e^2} \tag{4.5}$$

This is the fundamental resistance associated with a SWCNT that cannot be avoided. As shown in following figure this fundamental resistance (R_F) is equally divided between the two contacts on either side of the nanotube.

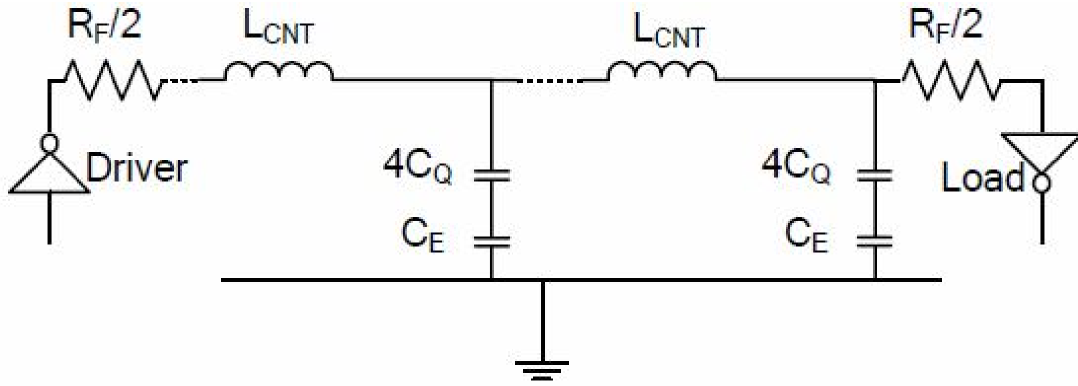

Fig. 4.4 Equivalent circuit model for an isolated SWCNT [25]

The mean free path of electrons (the distance across which no scattering occurs) in a CNT is typically 1μm [35.]. For CNT lengths less than 1μm, electron transport is essentially ballistic within the nanotube and the resistance is independent of length (6.45 KΩ). However, for lengths greater than the mean free path, resistance increases with length [36], where L_0 is the mean free path and L is the length of the CNT. Hence resistance of CNT is given by

$$R_{CNT} = \left(\frac{h}{4e^2}\right)\frac{L}{L_0} \qquad (4.6)$$

4.3.2 Capacitance of Isolated SWCNT

The capacitance of a CNT arises from two sources. The electrostatic capacitance (C_E) is calculated by treating the CNT as a thin wire, with diameter '*d*', placed a distance '*y*' away from a ground plane. The quantity d and y is shown in the following figure.

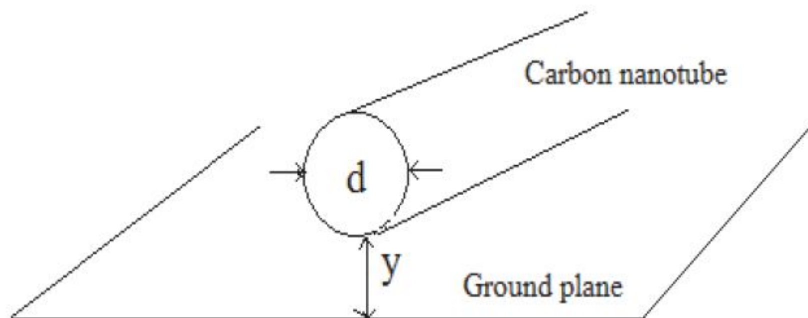

Fig. 4.5 Carbon nanotube with diameter 'd' and, distance 'y' below it [37]

This is the intrinsic plate capacitance of an isolated CNT.

$$C_E = \frac{2\pi\epsilon}{\left(\frac{y}{d}\right)} \qquad (4.7)$$

The quantum capacitance (C_Q) accounts for the quantum electrostatic energy stored in the nanotube when it carries current. Due to the Pauli Exclusion Principle, it is only possible to add electrons into the nanotube at an available quantum state above the Fermi energy level. By equating this energy to an effective capacitance, the expression for the quantum capacitance (per unit length) is obtained as shown in Equation 4.8 [9], where h is the Planck's constant and v_f is the Fermi velocity. For a carbon nanotube ($v_f \approx 8x10^5$m/s), C_Q≈100aF/um [34].

$$C_Q = \frac{2e^2}{hv_F} \qquad (4.8)$$

As a CNT has four conducting channels as described in the previous sub-section, the effective quantum capacitance resulting from four parallel capacitances C_Q is given by $4C_Q$. The same effective charge resides on both these capacitances (C_E and $4C_Q$) when the CNT carries current, as is true for any two capacitances in series. Hence these capacitances appear in series in the effective circuit model.

4.3.3 Inductance of an Isolated SWCNT

The inductance associated with an isolated SWCNT can be calculated from the magnetic field of an isolated current carrying wire some distance away from a ground plane**.** In addition to this magnetic inductance (L_M), the kinetic inductance is calculated in [9] by equating the kinetic energy stored in each conducting channel of the CNT to an effective inductance. The four parallel conducting channels in a CNT give rise to an effective kinetic inductance of $L_K/4$. The expressions for L_M and L_K are shown in Equation 4.9 below.

$$L_M = \frac{\mu}{2\pi}\ln\left(\frac{y}{d}\right) \qquad (4.9)$$

$$L_K = \left(\frac{h}{2e^2 v_F}\right) \quad (4.10)$$

For d=1 nm and y=1 um, L_M (per unit length) evaluates to ≈1.4 pH/um. On the other hand, L_K (per unit length) for a CNT evaluates to 16 nH/um. However, the kinetic inductance (L_K) in is derived considering no potential drop along the nanotube; hence it must be treated with care. Since $L_K >> L_M$, the inclusion of L_K can have a significant impact on the delay model for interconnects. In the light of experimental evidence of potential drop appearing along the length of a nanotube, L_K is excluded from the calculations in this work. The large inductive effects expected due to L_K are not observed up to frequencies as high as 10 GHz and the high frequency response is effectively damped by the nanotube resistance.

4.4 Equivalent Circuit Parameters for a Bundle of SWCNTs

A CNT-bundle interconnect is assumed to be composed of hexagonally packed identical metallic single-walled carbon nanotubes. Each CNT is surrounded by six immediate neighbors, their centers uniformly separated by a distance'sʼ. The densely packed structure with's' ='d' (CNT diameter), shown in Fig. 4.6, will lead to best interconnect performance.

The expressions to calculate the number of CNTs in the bundle are shown in following equations where n_H is the number of "rows" in the interconnect bundle, n_W is the number of "columns" n_{CNT} is the total number of CNTs and $\lfloor y \rfloor$ denotes the largest integer less than or equal to '*y*'.

Number of rows in interconnect bundle is given by

$$n_W = \left\lfloor \frac{w-d}{s} \right\rfloor \quad (4.11)$$

Number of columns in interconnect bundle is given by

$$n_H = \left\lfloor \frac{h-d}{(\sqrt{3}/2)s} \right\rfloor + 1 \quad (4.12)$$

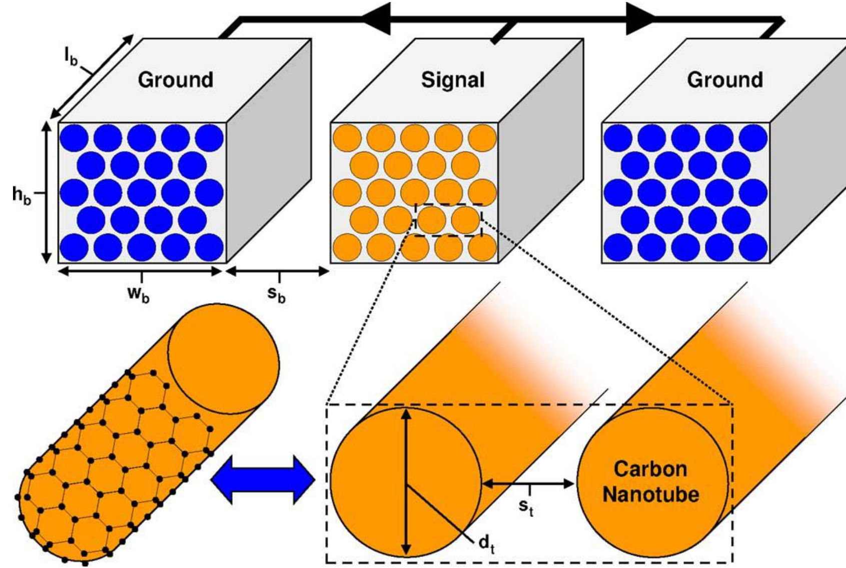

Fig. 4.6 SWCNT bundle interconnect geometric parameters and circuit model [38]

Therefore number of CNT used in the interconnect bundle is given by the following equation.

If number of rows nH in the CNT bundle is even, the number of CNT used is given by

$$n_{\mathrm{CNT}} = n_{\mathrm{W}} n_{\mathrm{H}} - \frac{n_{\mathrm{H}}}{2} \qquad (4.13)$$

If number of rows nH in the CNT bundle is odd, the number of CNT used is given by

$$n_{\mathrm{CNT}} = n_{\mathrm{W}} n_{\mathrm{H}} - \frac{n_{\mathrm{H}} - 1}{2} \qquad (4.14)$$

4.4.1 Resistance of CNT bundle:

In order to calculate the effective resistance of a CNT bundle, it is assumed that all CNTs packed into the interconnect structure are metallic and conducting. The CNT-bundle resistance is then given by following Equation, where $R_{isolated}$ is the resistance of an isolated CNT and n_{CNT} is the total number of CNTs forming the bundle.

$$R_{bundle} = \frac{R_{isolated}}{n_{CNT}} \qquad (4.15)$$

4.4.2 Capacitance of CNT bundle:

The total electrostatic capacitance of the bundle is given by the sum of the contribution from each of these CNTs.

$$C_E^{bundle} = 2C_{\mathrm{En}} + \frac{n_{\mathrm{W}}-2}{2}C_{\mathrm{Ef}} + \frac{3(n_{\mathrm{H}}-2)}{5}C_{\mathrm{En}} \quad (4.16)$$

Where C_{En} and C_{Ef} are the intrinsic plate capacitances calculated for an isolated CNT over a ground plane.

C_{En} is calculated assuming the ground plane to be at a distance equal to the separation distance 's'from the adjacent interconnect.

$$C_{\mathrm{En}} = \frac{2\pi\epsilon}{ln\left(\frac{s}{d}\right)} \quad (4.17)$$

C_{Ef} is calculated assuming the ground plane to be at a distance equal to the separation distance 's+w' from the "far" adjacent interconnect.

$$C_{\mathrm{Ef}} = \frac{2\pi\epsilon}{ln\left(\frac{s+w}{d}\right)} \quad (4.18)$$

The effective quantum capacitance of the bundle is the sum of the individual quantum capacitances. C_Q^{CNT} is the quantum capacitance of an isolated CNT and n_{CNT} is the total number of CNTs forming the bundle.

Quantum capacitance of the bundle is given by the following expression:

$$C_Q^{bundle} = C_Q^{CNT} . n_{\mathrm{CNT}} \quad (4.19)$$

The effective capacitance (C_{bundle}) of the series combination of a quantum and electrostatic capacitance is given by

$$\frac{1}{C_{bundle}} = \frac{1}{C_Q^{bundle}} + \frac{1}{C_E^{bundle}} \quad (4.20)$$

4.4.3 Inductance of CNT Bundle

The inductance of a *CNT bundle* is given by the parallel combination of the inductances corresponding to each CNT forming the bundle where L_{CNT} is the (magnetic) inductance of an isolated SWCNT.

$$L_{bundle} = \frac{L^{CNT}}{n_{CNT}} \tag{4.21}$$

CHAPTER 5

COMPARATIVE STUDY OF VARIATION IN PARASITIC ON DELAY AND POWER DISSIPATION OF COPPER AND CNT

5.1 Introduction

On the basis of parasitic explained with equations in previous chapter the equivalent resistance, capacitance and inductance of copper and CNT bundle is determined. With variation in length and width of interconnect, variation in resistance, capacitance and inductance of global, semiglobal and local interconnect is observed with the help of graph.

5.2 Parameters used for calculation

Table 5.1 ITRS 2005 based parameters for calculation [3]

Parameters	CNT/Copper
Technology	32 nm
Length of global interconnect	1mm
Length of semiglobal interconnect	700µm and 400µm
Length of Local interconnect local	100µm and 50µm
Width of interconnect	48 nm
Aspect Ratio	3
ILD thickness t_{OX}	110.4 nm
K_{ILD}	2.25
Diameter	1 nm
Pitch of interconnect	1 nm

5.3 Parasitic variation with change in width of SWCNT bundle interconnect

a) Variation of Resistance with change in width and MFP of CNT bundle interconnect. Here length of interconnect is 1mm and MFP is mean free path.

Table 5.2 CNT resistance with change in mean free path and width of interconnect.

Width(nm)	MFP(0.6μm)	MFP(0.8μm)	MFP(1μm)	MFP(1.2μm)	MFP(1.4μm)	MFP(1.6μm)
48	1397.13 Ω	1047.85 Ω	838.28 Ω	698.56 Ω	598.77 Ω	522.3 Ω
72	614.32 Ω	460.74 Ω	368.59 Ω	307.16 Ω	263.28 Ω	229.6 Ω
96	343.74 Ω	257.805 Ω	206.244Ω	171.87 Ω	147.317 Ω	128.5 Ω
120	219.29 Ω	164.4714 Ω	131.57 Ω	109.64 Ω	93.98 Ω	81.9 Ω
144	151.66 Ω	113.747 Ω	90.99 Ω	75.831 Ω	64.998 Ω	56.7 Ω

On the basis of above data following graph is drawn

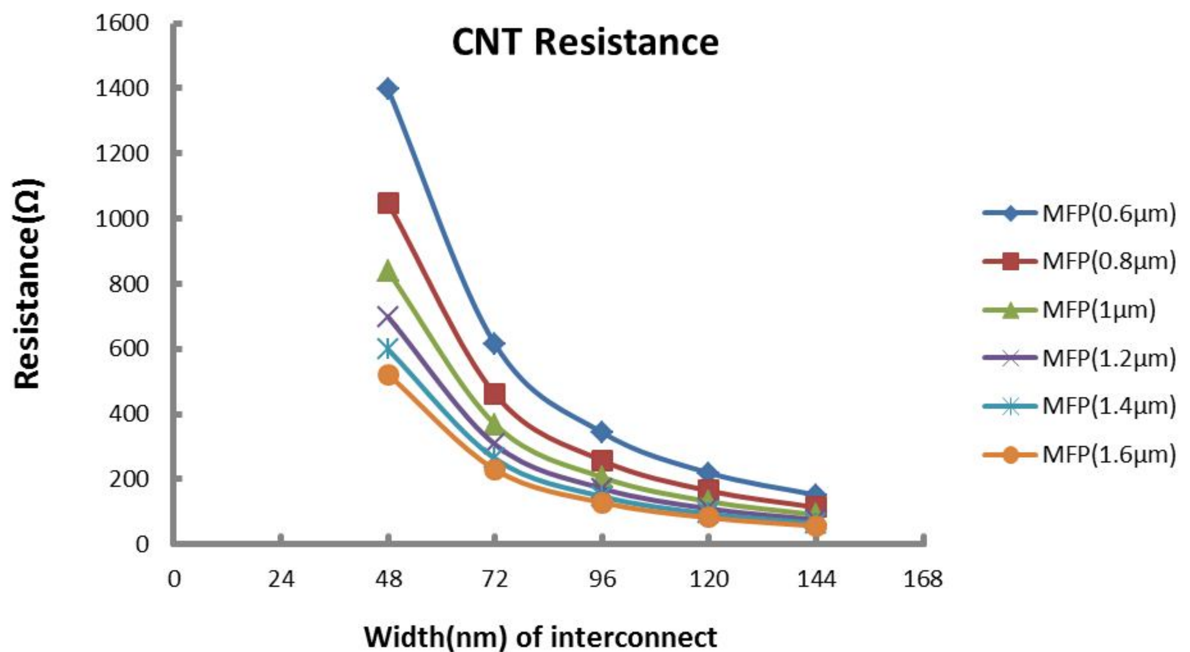

Fig. 5.1 CNT bundle resistance versus mean free path and width of interconnect at 32nm technology.

With increase in width of interconnect the number of rows used in CNT bundle increases from equation 4.11 and hence number of rows used is CNT bundle increases from

equation 4.13. R_{bundle} inversly propotional to the n_{CNT} from equation 4.11 and hence from above fig 5.1, with increase in width of interconnect resistance of CNT bundle decreases.

From equation 4.6 we can see that resistance of CNT bundle is inversely proportional to the mean free path and hence with increase in mean free path resistance of CNT bundle decreases.

b) Variation of capacitance with change in width of interconnect. Here length of interconnect is 1mm.

Table 5.3 CNT bundle Capacitance versus width of interconnect

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Width(nm)	Capacitance(pF)
48	3.59
72	5.2
96	6.505
120	7.83
144	9.1

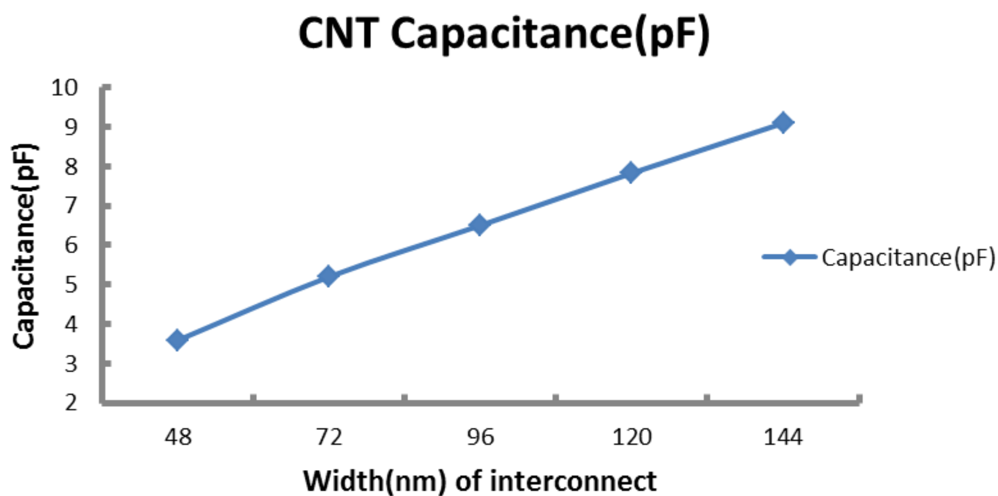


Fig. 5.2 CNT bundle capacitance versus width of interconnect at 32nm technology.

With increase in width n_{CNT} increases from equation 4.13 and 4.11 and hence from equation 4.19 we can see that quantum capacitance is directly proportional to nCNT and hence capacitance increases. From equation 4.16 and 4.17 we can see that capacitance is independent on free mean path. With variation in mean free path capacitance will remain same. So in above fig 5.2, with increase in width of interconnect capacitance increases.

c) Variation of inductance of CNT bundle with change in width of interconnects. Here length of interconnect is 1mm.

Table 5.4 CNT bundle Inductance versus width of interconnect

Width(nm)	Inductance(fH)
48	121.88
72	53.59
96	29.9
120	19.13
144	13.2

From fig 5.3, we can observe that with increase in width of interconnect inductance of CNT bundle decreases. Due to increase in width n_{CNT} increases and hence inductance will decrease from equation 4.21. Inductance of CNT bundle is also independent on mean free path from equation 4.9 and 4.10 and hence with increase in mean free path inductance will remain same.

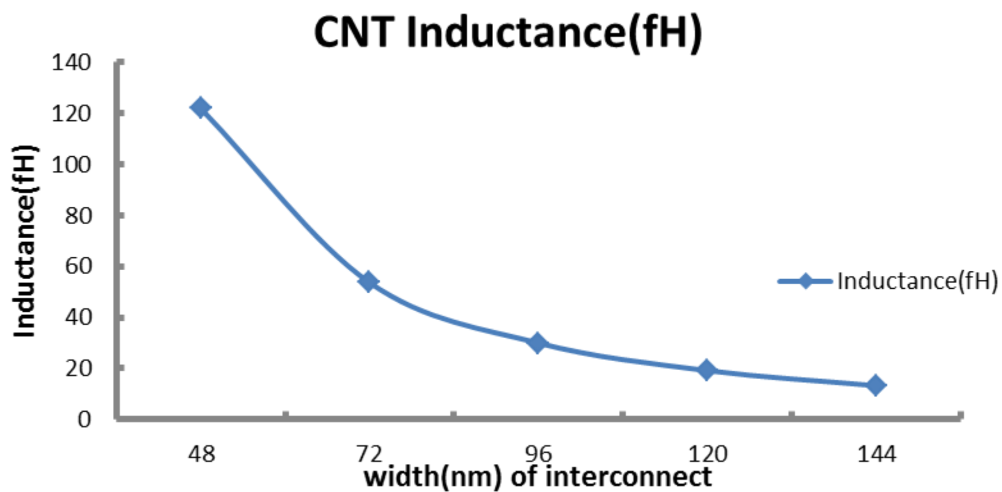


Fig. 5.3 CNT bundle inductance versus width of interconnect at 32nm technology.

5.4 Parasitic variation with change in width of copper interconnect

a) Variation of Resistance with change in width of interconnect. Here length of interconnect is 1mm.

Table 5.5 Copper resistance vs width of interconnect

Width(nm)	Resistance(Ω)
48	5092
72	2263.27
96	1273.148
120	814.8
144	565.84

From equation 4.1 we can see that Resistance of copper interconnect is inversely proportional to width of interconnect and hence from the following fig 5.4, with increase in width of interconnect resistance of copper decreases.

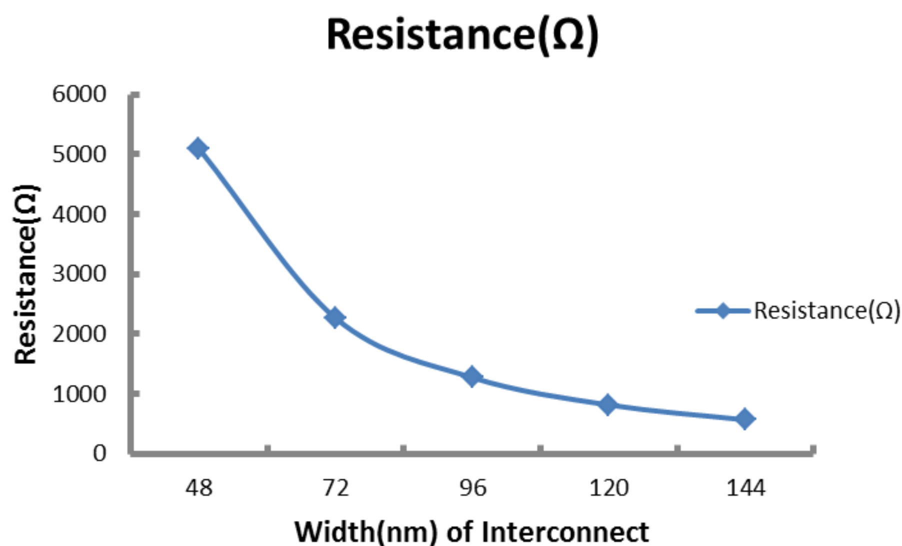


Fig. 5.4 Copper resistance versus width of interconnect at 32nm technology.

b) Variation of capacitance with change in width of interconnect. Here length of interconnect is 1mm.

Table 5.6 Copper capacitance vs width of interconnect

Width(nm)	capacitance(fF)
48	16.8
72	19
96	22.7
120	26.3
144	29.5

Capacitance increases with increase in width of interconnect. From equation 4.2 capacitance is directly proportional to the width of interconnect so this effect appears in fig 5.5, with increase in width of interconnect capacitance is also increases.

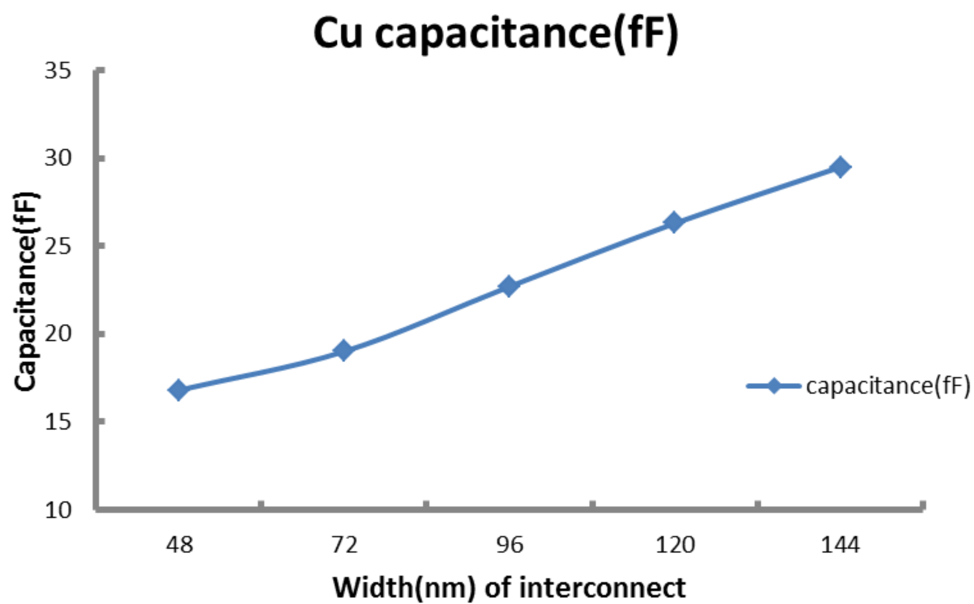


Fig. 5.5 Copper capacitance versus width of interconnect at 32nm technology.

c) Variation of inductance of copper with change in width of interconnect. Here length of interconnect is 1mm.

Table 5.7 Copper inductance vs width of interconnect

Width(nm)	Inductance(nH)
48	1.94
72	1.85
96	1.803
120	1.75
144	1.72

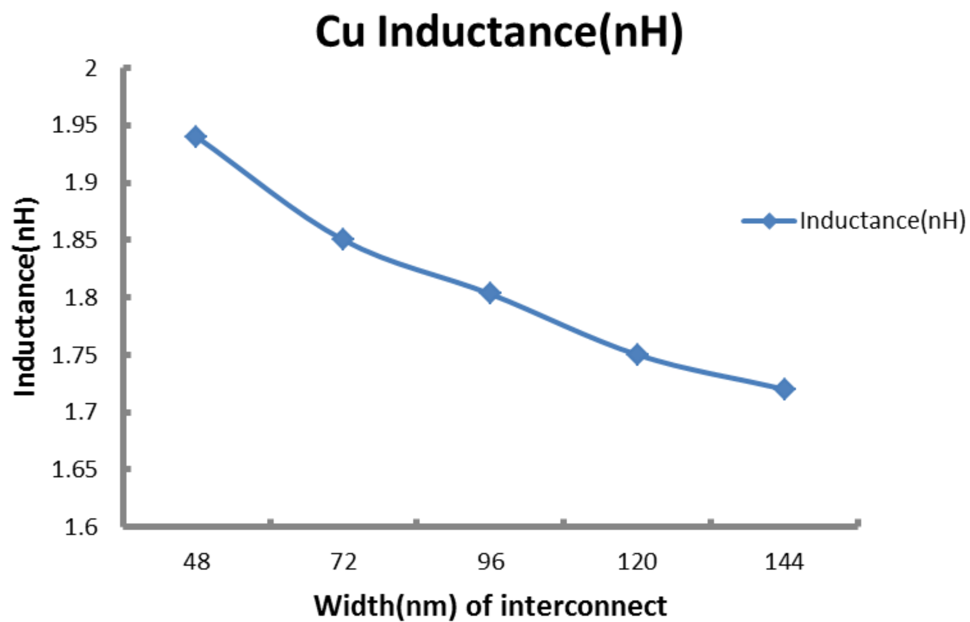


Fig. 5.6 Copper inductance versus width of interconnect at 32nm technology

From equation 4.3 inductance of copper is inversly propotional to the width of interconnect and with increase in width of interconnect inductance decreases. It is more clear form the fig 5.6.

5.5 Parasitic variation with change in length of SWCNT Bundle Interconnect

a) Variation of Resistance of CNT bundle with change in length of interconnect.

Table5.8 CNT bundle resistance with variation in mean free path and length of interconnect.

Length(μm)	MFP(0.6μm)	MFP(0.8μm)	MFP(1μm)	MFP(1.2μm)	MFP(1.4μm)	MFP(1.6μm)
50	69.85 Ω	52.39 Ω	41.91 Ω	34.92 Ω	29.93 Ω	26.115 Ω
100	139.713 Ω	104.78 Ω	83.8 Ω	69.85 Ω	59.87 Ω	52.23 Ω
400	558.85 Ω	419.14 Ω	335.312 Ω	279.4275 Ω	239.509 Ω	208.92 Ω
700	977.99 Ω	733.495 Ω	586.796 Ω	488.992 Ω	419.139 Ω	365.61 Ω
1000	1397.13 Ω	1047.85 Ω	838.28 Ω	698.56 Ω	598.77 Ω	522.3 Ω

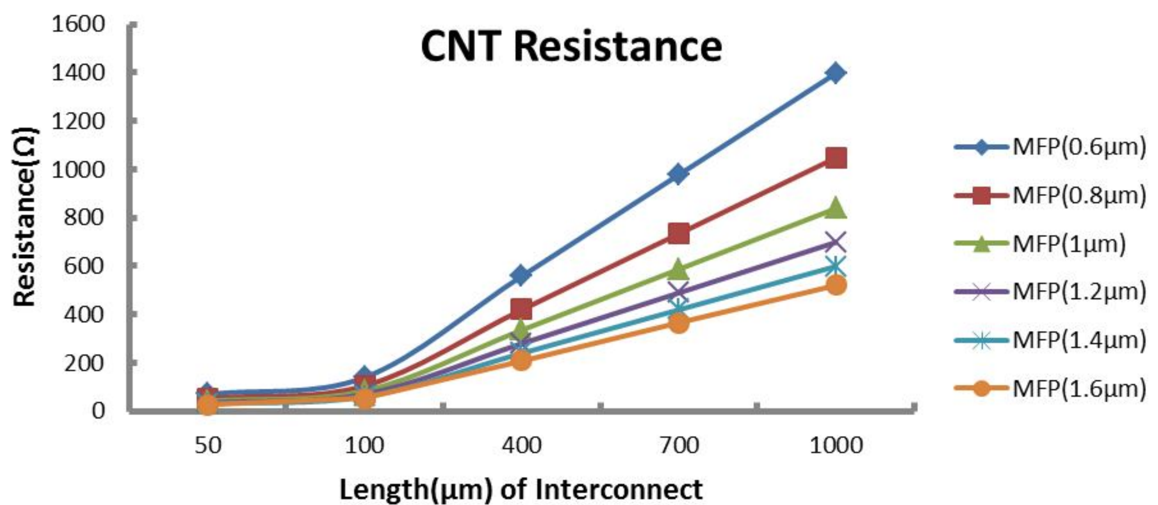


Fig. 5.7 CNT bundle resistance versus mean free path and length of interconnect at 32nm technology.

From equation 4.6 R_{CNT} is directly proportional to the length of interconnect and inversely proportional to the mean free path of CNT bundle. So in fig 5.7, with increase in length

resistance increases and with increase in mean free path of CNT bundle, resistance decreases.

b) Variation of inductance of CNT bundle with change in width of interconnect.

Table 5.9 CNT inductance versus length of interconnect

Length(μm)	Inductance(fH)
50	6.094
100	12.18
400	48.75
700	85.316
1000	121.88

Inductance is modeled as distributed parameter. So inductance is dependent on length of interconnect. So in the following fig 5.8, inductance is increases with increase in width of interconnect.

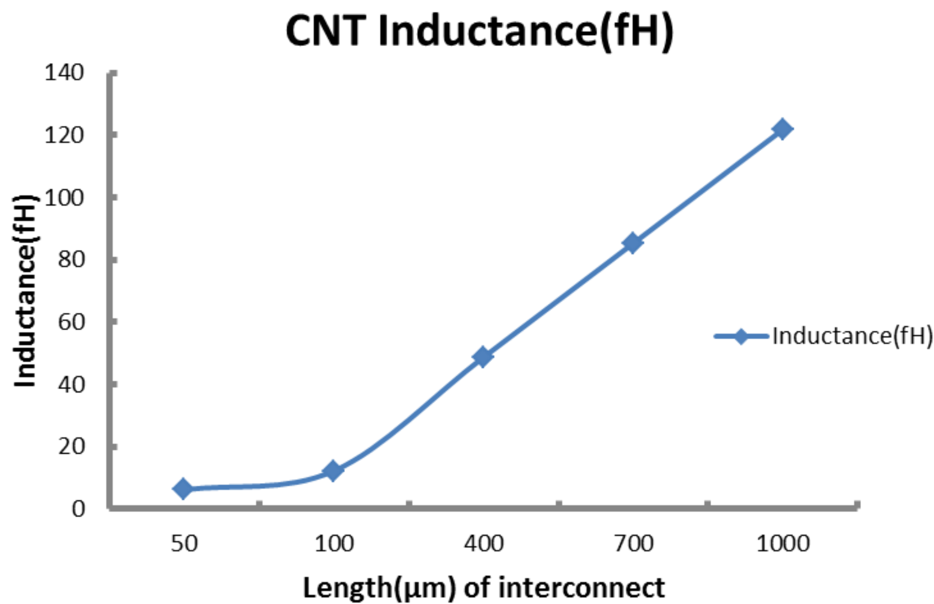


Fig. 5.8 CNT bundle inductance versus length of interconnect at 32nm technology.

c) Variation of capacitance of CNT bundle with change in width of interconnect.

Table 5.10 CNT bundle inductance and length of interconnect

Length(μm)	Capacitance(pF)
50	0.19293
100	0.38594
400	1.539
700	2.513
1000	3.59

As inductance of CNT bundle, capacitance is also modeled as distributed parameter. So capacitance is also dependent on length of interconnect. So in fig 5.9, with increase in length capacitance of CNT bundle also increases.

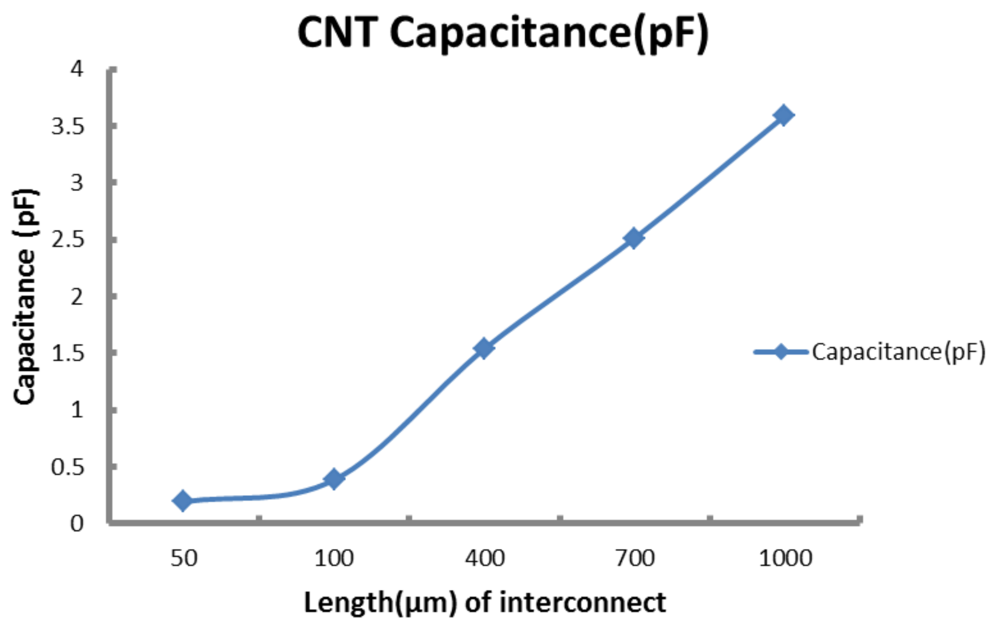


*Fig. 5.9 CNT bundle capacitance versus length of interconnect at 32nm technology***.**

5.6 Parasitic variation with change in length of copper interconnect

a) Variation of Resistance with change in length of interconnect *at 32nm technology*.

Table 5.11 Copper resistance and length of interconnect

Length(μm)	Resistance(Ω)
50	254.62
100	509.25
400	2037.03
700	3564.8
1000	5092.5

In equation 4.1 resistance of copper interconnect is directly proportional to the length of interconnect. So variation in length of interconnects leads to variation in resistance. So in fig 5.10, with increase in length of interconnect resistance of copper interconnect increases.

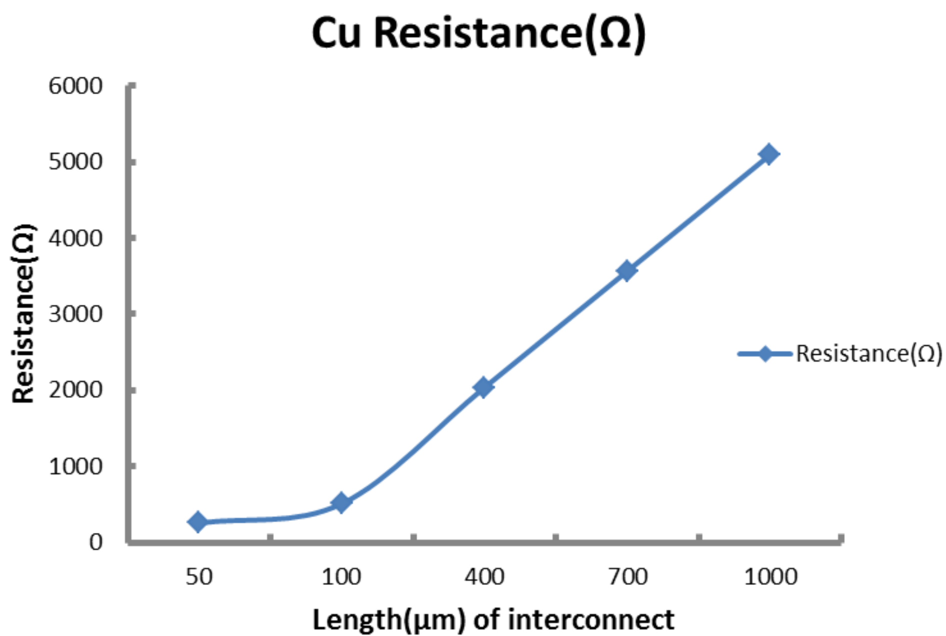


Fig. 5.10 Variation of copper resistance with length of interconnect at 32nm technology.

b) Variation of capacitance with change in length of interconnect

Table 5.12 Copper capacitance and length of interconnect

Length(μm)	capacitance(fF)
50	0.84
100	1.68
400	6.72
700	11.76
1000	16.8

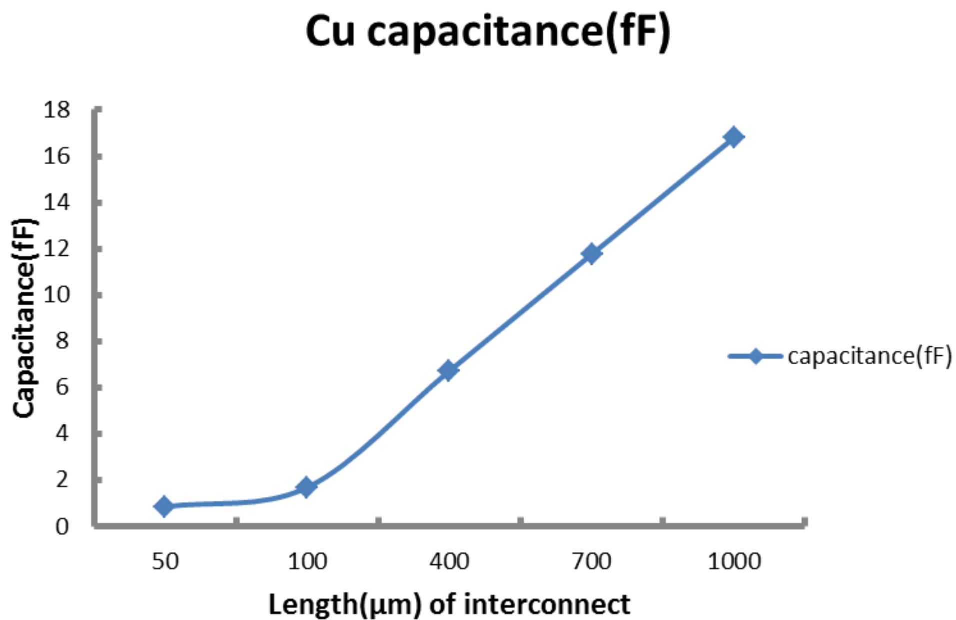


Fig 5.11 Variation in copper capacitance with length of interconnect at 32nm technology.

Capacitance of copper interconnect is modeled as distributed parameter, so with change in length capacitance also changes. So in fig5.11 with increase in length of interconnect capacitance also increases.

c) Variation of inductance with change in length of interconnect

Table 5.13 Copper inductance and length of interconnect

Length(μm)	Inductance(pH)
50	67.5
100	148
400	704
700	1310
1000	1940.4

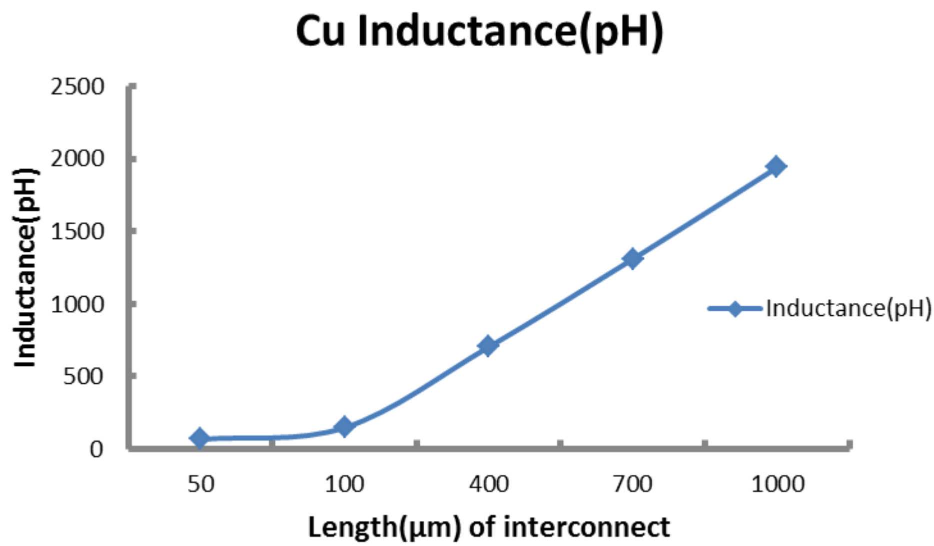


Fig. 5.12 Copper inductance versus length of interconnect at 32nm technology.

From equation 4.3 inductance is directly dependent on length of copper interconnect. So with increase in length of interconnect inductance of copper interconnect also increases.

5.7 Delay analysis

On the basis of above parasitic of CNT bundle and Copper interconnect delay is determined by using these parasitic as a load to CMOS inverter. Parasitic values are determined by using above equation of equivalent resistance, capacitance and inductance of Bundled CNT and copper interconnect. With the help of Tanner EDA tool these parasitic are used as a load to CMOS inverter. By performing transient analysis by Tanner EDA tool at 32nm technology at 0.1GHz frequency, delay is determined for bundled CNT and copper interconnect.

5.7.1 Simulation Parameters

Table 5.14 ITRS 2005 based parameters for simulation [3]

Parameters	CNT/Copper
Technology	32 nm
V_{DD}	0.9 V
Length of interconnect(L)	1mm(global)
Width of interconnect(W)	48 nm
Aspect Ratio	3
ILD thickness t_{OX}	110.4 nm
K_{ILD}	2.25
Load Capacitance	1 pF
Operating Frequency	0.1 GHz

5.7.2 Delay analysis for Local Interconnect

For Local interconnect the length of interconnect 50µm and 100µm are taken. The width of interconnect is taken as 48 nm. Resistance, capacitance and inductance of CNT bundle and copper interconnect is calculated using equation in chapter5.These parasitic used as load for CMOS inverter and delay is calculated by transient analysis at frequency 0.1GHz using Tanner EDA Tool.

At local interconnect capacitance is dominates over resistance. Due to closely placed at local interconnect the distance between interconnect reduces and leads to rise in the capacitance. SWCNT can conduct orders of magnitude larger current densities compared to copper. SWCNT bundle offer a significant reduction in lateral capacitance.

Delay of CNT bundle at different mean free path and copper interconnect is following.

a) Delay for CNT bundle length of interconnect = 50µm

Table5.15 Delay of CNT bundle with variation in mean free path and aspect ratio (W/L) of driver

W/L)	MFP1(0.6µm)	MFP2(.8µm)	MFP3(1µm)	MFP4(1.2µm)	MFP5(1.4µm)	MFP6(1.6µm)
20	1.965 ns	1.94 ns	1.93 ns	1.92 ns	1.915 ns	1.895 ns
30	1.35 ns	1.32 ns	1.315 ns	1.31 ns	1.3 ns	1.845 ns
40	1.085 ns	1.06 ns	1.045 ns	0.78 ns	1.025 ns	0.99 ns
50	0.905 ns	0.885 ns	0.875 ns	0.865 ns	0.86 ns	0.835 ns
60	0.835 ns	0.815 ns	0.795 ns	0.785 ns	0.78 ns	0.75 ns
70	0.77 ns	0.74 ns	0.72 ns	0.715 ns	0.7 ns	0.665

b) Delay for Copper interconnect

Table 5.16 Delay of copper versus W/L Driver

(W/L)	delay(ns)
20	2.315
30	1.745
40	1.452
50	1.295
60	1.185
70	1.09

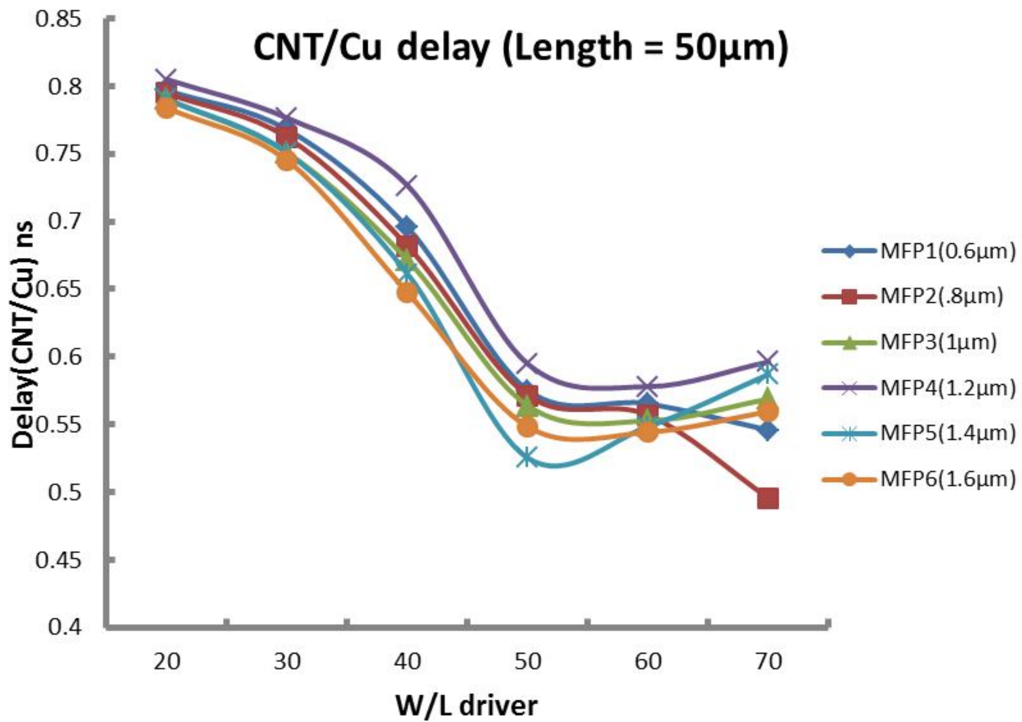


Fig.5.13 Normalized delay versus W/L ratio as a functionality MFP(length 50µm) at 32nm technology.

c) Delay for CNT bundle length of interconnect = 100µm

Table5.17 Delay of CNT bundle with variation in MFP and aspect ratio (W/L) of driver

W/L)	MFP1(0.6µm)	MFP2(.8µm)	MFP3(1µm)	MFP4(1.2µm)	MFP5(1.4µm)	MFP6(1.6µm)
20	1.965 ns	1.94 ns	1.93 ns	1.92 ns	1.915 ns	1.895 ns
30	1.35 ns	1.32 ns	1.315 ns	1.31 ns	1.3 ns	1.845 ns
40	1.085 ns	1.06 ns	1.045 ns	0.78 ns	1.025 ns	0.99 ns
50	0.905 ns	0.885 ns	0.875 ns	0.865 ns	0.86 ns	0.835 ns
60	0.835 ns	0.815 ns	0.795 ns	0.785 ns	0.78 ns	0.75 ns
70	0.77 ns	0.74 ns	0.72 ns	0.715 ns	0.7 ns	0.665 ns

- Delay for copper interconnect

Table5.18 Delay of copper interconnect with variation in aspect ratio(W/L) driver.

(W/L)	delay(ns)
20	2.68
30	2.405
40	2.32
50	2.08
60	1.985
70	1.905

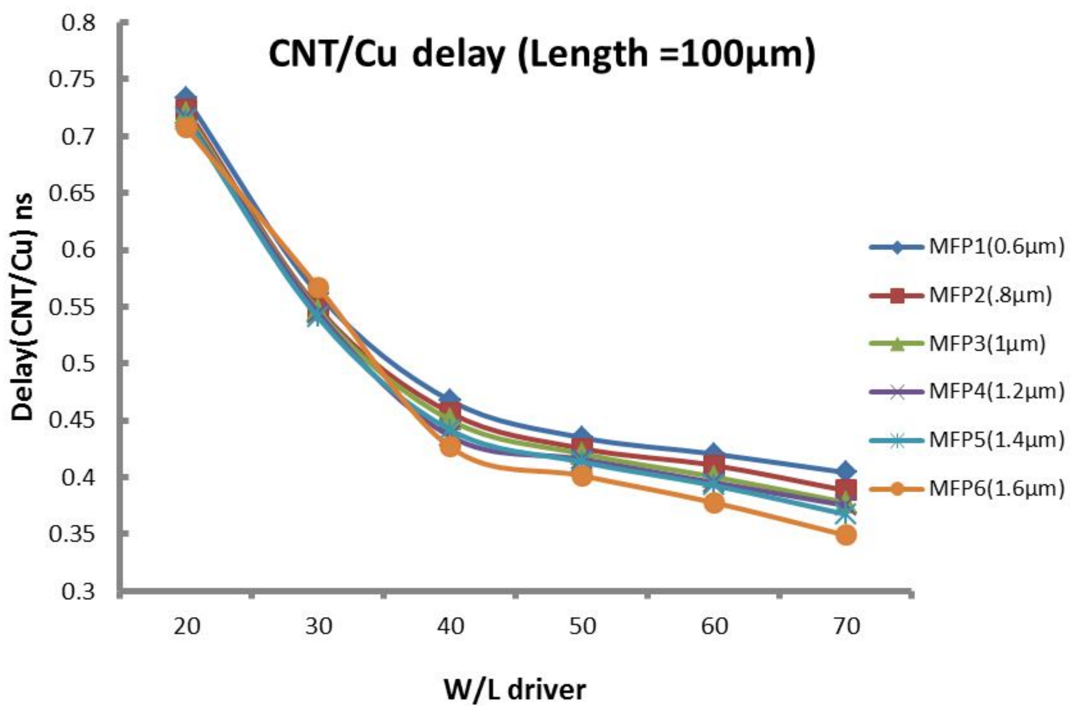


Fig.5.14 Normalized delay versus W/L ratio as a functionality MFP(length 100µm) at 32nm technology.

At local interconnect contact resistance of CNT bunle dominates. From the fig 5.13 and 5.14 we can see that with increase in mean free path the performance of delay is iproved

as compared to the copper interconnect. As the aspect ratio of driver increases SWCNT bundle gives the improved performance in delay over copper interconnect. Whereas in copper interconnect with increase in W/L ratio the parasitics increases and hence increaes the delay.

5.7.3 Delay analysis for Semiglobal Interconnect

SWCNT bundle can replace the copper wires at the semiglobal level and improve their latency because of their small resistivity. Semiglobal interconnects are less sensitive to contact resistance.

For Local interconnect the length of interconnect 400µm and 700µm are taken. The width of interconnect is taken as 48 nm.

- Delay for CNT bundle length of interconnect = 400µm

Table5.19 Variation in delay with change in MFP and W/L of driver

(w/L)	MFP1(0.6µm)	MFP2(.8µm)	MFP3(1µm)	MFP4(1.2µm)	MFP5(1.4µm)	MFP6(1.6µm)
20	1.94 ns	1.91 ns	1.89 ns	1.895 ns	1.905 ns	1.855 ns
30	1.31 ns	1.295 ns	1.225 ns	1.245 ns	1.225 ns	1.215 ns
40	1.02 ns	0.93 ns	0.98 ns	0.96 ns	0.945 ns	0.925 ns
50	0.875 ns	0.695 ns	0.8 ns	0.785 ns	0.775 ns	0.745 ns
60	0.745 ns	0.705 ns	0.705 ns	0.675 ns	0.66 ns	0.71 ns
70	0.675 ns	0.745 ns	0.605 ns	0.58 ns	0.55 ns	0.545 ns

- Delay for Copper interconnect

Table5.20 Variation in delay of copper interconnect with change in aspect ratio (W/L) of driver.

(W/L)	delay(ns)
20	2.315
30	1.745
40	1.452
50	1.295
60	1.185
70	1.09

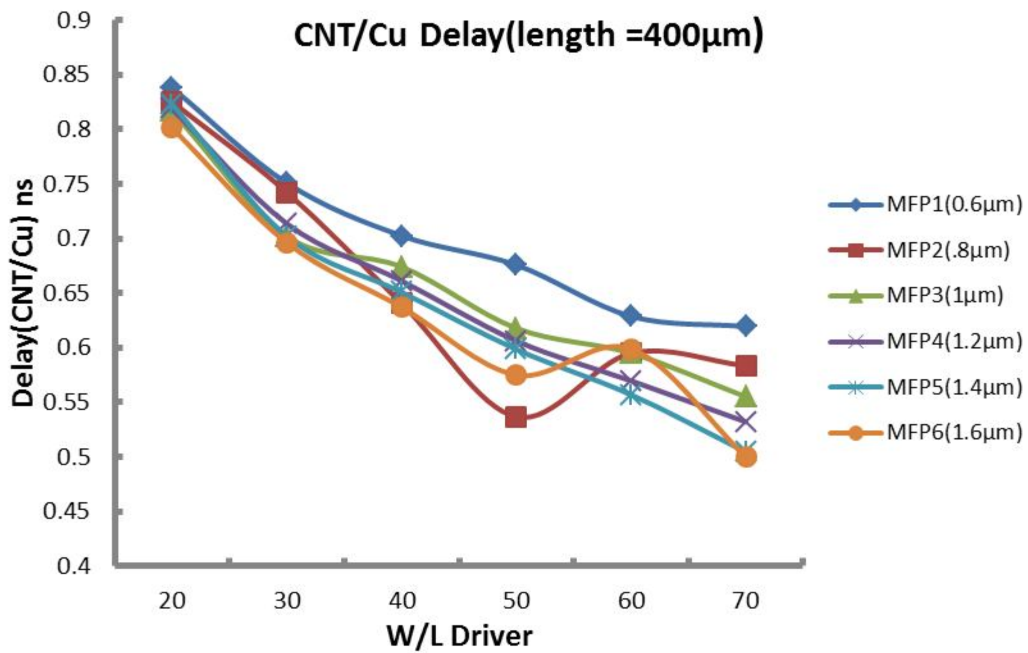


Fig.5.15 Normalized delay versus W/L ratio as a functionality MFP(length 400µm) at 32nm technology.

- Delay for CNT bundle length of interconnect = 700µm

Table5.21 Delay of CNT bundle with variation in MFP at different W/L of driver.

(W/L)	MFP1(0.6µm)	MFP2(.8µm)	MFP3(1µm)	MFP4(1.2µm)	MFP5(1.4µm)	MFP6(1.6µm)
20	2.31 ns	2.19 ns	2.04 ns	2.095 ns	2.07 ns	2.145 ns
30	2.14 ns	1.61 ns	1.535 ns	1.48ns	1.34 ns	1.43 ns
40	1.365 ns	1.25 ns	1.22 ns	1.355 ns	1.135 ns	1.125 ns
50	1.14 ns	1.095 ns	0.995 ns	0.955 ns	0.915 ns	0.92 ns
60	1.005 ns	0.925 ns	0.87 ns	0.835 ns	0.8 ns	0.845 ns
70	0.935 ns	0.835 ns	0.81 ns	0.73 ns	0.715 ns	0.71 ns

- Delay for Copper interconnect

*Table5.22 Delay of copper interconnect at different WL of driver for semiglobal (*700µm) *interconnect*

W/L	delay(ns)
20	2.315
30	1.745
40	1.452
50	1.295
60	1.185
70	1.09

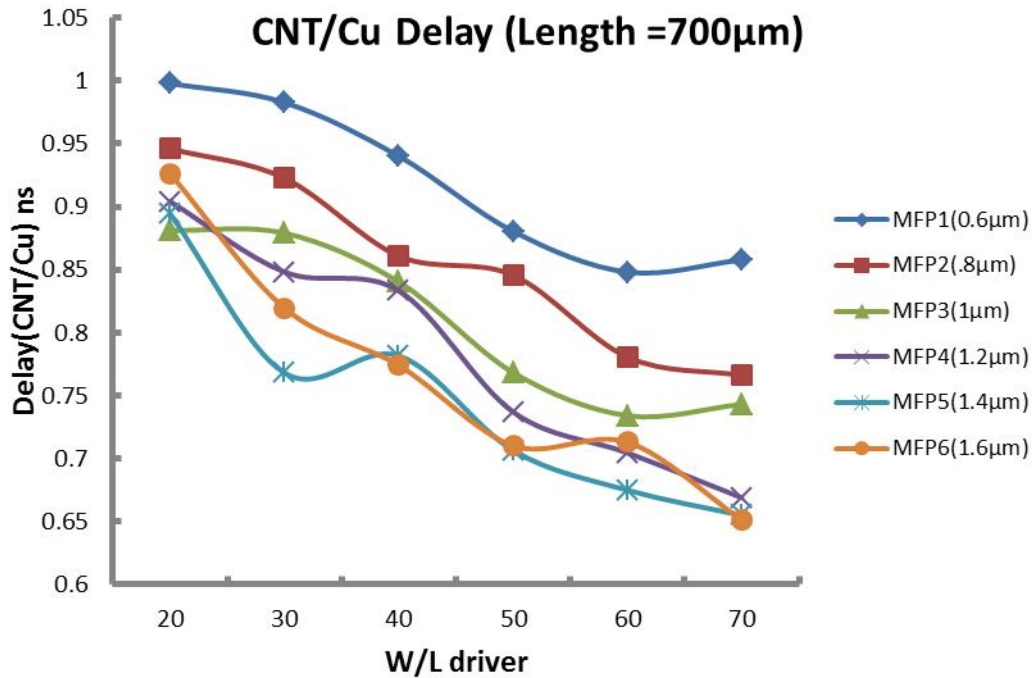


Fig.5.16 Normalized delay versus W/L ratio as a functionality MFP(length 700µm) at 32nm technology.

From fig 5.15 and 5.16 we can see that MFP and density of SWCNT bundle are the key parameters that determine the performance improvement. The improvement in delay that SWCNT bundle offer is shown in fig 5.15 and 5.16.

5.7.4 Delay analysis for Global Interconnect

Since global interconnects normally have large cross-sectional dimensions. Due to this density of CNT in bundle increases and leads to large reduction in resistance and it leads to highly reduction in delay. It is shown in the following figure.

Width of interconnect is 48nm and length of interconnect is 1mm.Number of repeaters used for the analysis is 8.

a) Delay for CNT bundle

Table5.23 Delay of CNT bundle at different MFP and W/L for Driver for Global interconnect.

(W/L)	MFP1(0.6μm)	MFP2(.8μm)	MFP3(1μm)	MFP4(1.2μm)	MFP5(1.4μm)	MFP6(1.6μm)
20	2.5 ns	2.5 ns	2.37 ns	2.33 ns	2.31 ns	2.29 ns
30	1.735 ns	1.605 ns	1.53 ns	1.5 ns	1.495 ns	1.49 ns
40	1.38 ns	1.325 ns	1.24 ns	1.175 ns	1.15 ns	1.15 ns
50	1.175 ns	1.11 ns	1.025 ns	0.985 ns	0.975 ns	0.97 ns
60	1.06 ns	0.97 ns	0.895 ns	0.87 ns	0.83 ns	0.825 ns
70	0.975 ns	0.875 ns	0.82 ns	0.74 ns	0.735 ns	0.73 ns

b) Delay for copper interconnect

Table 5.24 Delay for copper interconnect with change in W/L of driver for global interconnect.

(W/L)	delay(ns)
20	2.42
30	1.94
40	1.935
50	1.855
60	1.715
70	1.72

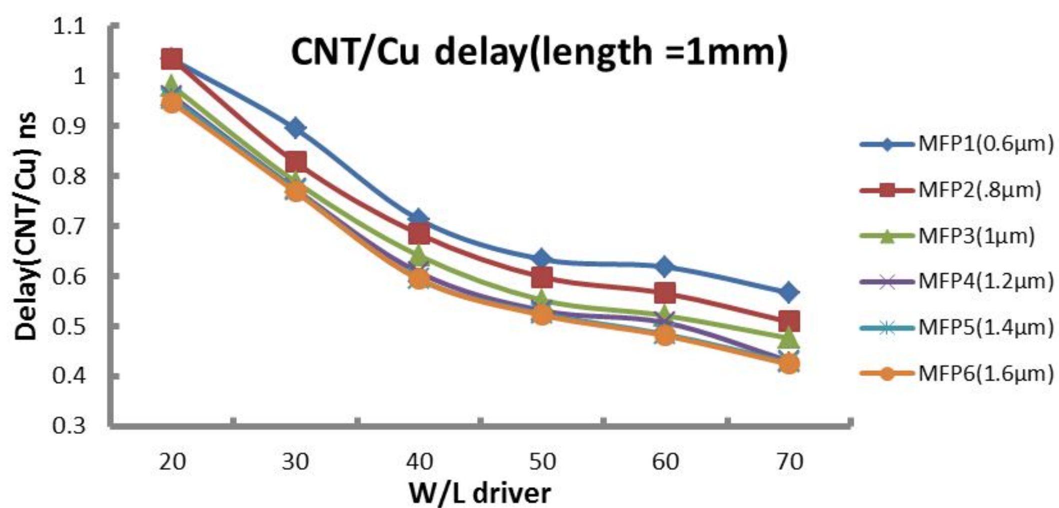


Fig.5.17 Normalized delay versus W/L ratio as functionality MFP for global interconnect.

5.8 Power analysis of Interconnect

The power dissipation of logic circuits comprises static and dynamic components. Static power dissipation is due to the leakage current of reverse-biased junctions, subthreshold current etc. Dynamic power dissipation is caused by a short circuit as well as the currents that charge and discharge loading capacitors [43]. Dynamic power dissipation includes two components: the power consumed by short circuit current and the power consumed by the transistors during charging and discharging loading capacitors.

Charging and discharging power dissipation is proportional to square of supply voltage and linearly proportional to both loading capacitance and operating frequency. Whereas short circuit power dissipation is proportional to the rise time and fall times of the input signal.

So dynamic power is given by the expressions.

$$P = C_l VDD^2 fp \qquad (5.1)$$

Where C_l is load capacitance, VDD is supply and f_p is the operating frequency.

So dynamic power can be lowered by reducing the capacitance C. Therefore at different level local, semiglobal and global interconnect, power dissipation of SWCNT bundle and copper interconnect is calculated and compared at different MFP and variation in W/L of driver.

5.8.1 Power dissipation at global interconnect

At global interconnect area of interconnect increase. Number of SWCNT in bundle increases, hence equivalent resistance and inductance of the interconnect reduces. It leads to low power dissipation at global interconnect as compared to copper interconnect in which with increase in area all the parasitic (capacitance, inductance and capacitance) increases.

Table5.25 Power of bundle SWCNT with different MFP and W/L of driver for global interconnect.

W/L)	MFP1(0.6µm)	MFP2(.8µm)	MFP3(1µm)	MFP4(1.2µm)	MFP5(1.4µm)	MFP6(1.6µm)
20	0.3409mW	0.3431 mW	0.343 mW	0.34 mW	0.3445 mW	0.346 mW
30	0.415 mW	0.421 mW	0.427 mW	0.4273 mW	0.4292 mW	0.4379 mW
40	0.4941 mW	0.50024 mW	0.5018 mW	0.5018 mW	0.5188 mW	0.4984 mW
50	0.51225 mW	0.5105 mW	0.5134 mW	0.5147 mW	0.5133 mW	0.5152 mW
60	0.5627 mW	0.5681 mW	0.5677 mW	0.567 mW	0.5682 mW	0.5591 mW
70	0.5894 mW	0.5827 mW	0.576 mW	0.574 mW	0.5731 mW	0.5662 mW

Table 5.26 Power of copper interconnect at different W/L of driver

W/L)	power(mW)
20	0.1274
30	0.162
40	0.16229
50	0.175
60	0.1855
70	0.1995

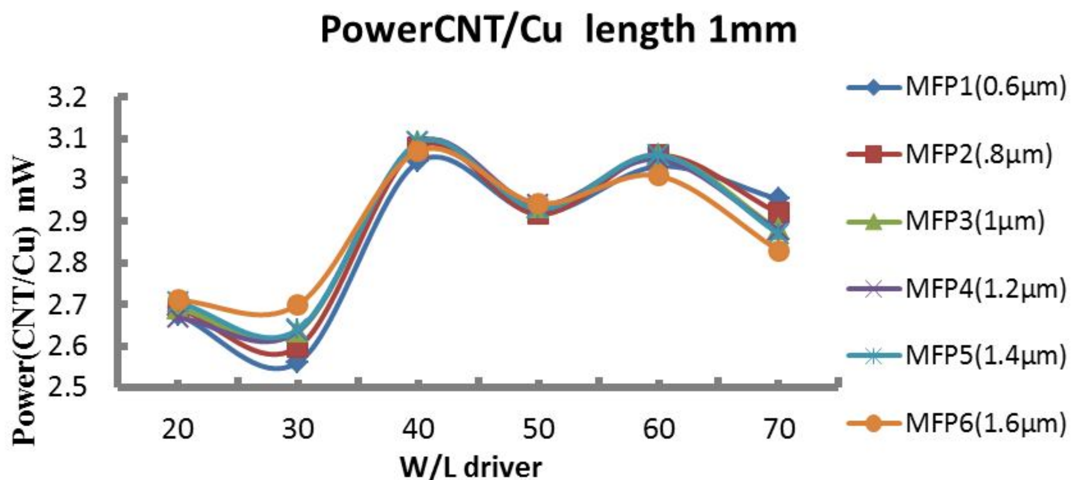


Fig .5.18 Normalized power versus W/L ratio as fuctionality MFP for global interconnect.

5.8.2 Power dissipation at semiglobal interconnect

At semiglobal interconnect effective resistance is independent on SWCNT bundle contact resistance hence effective resistance is smaller than the equivalent resistance of copper interconnect from fig 5.8 and fig 5.10. It leads to lower power dissipation as compared to copper interconnect. With increase in mean free path power performance is improved as compared to copper inteconnect. It is shown in the following figure.

Table 5.27 Power of bundle SWCNT with variation in MFP and W/L of driver for semiglobal inteconnect (400μm).

W/L)	MFP1(0.6μm)	MFP2(.8μm)	MFP3(1μm)	MFP4(1.2μm)	MFP5(1.4μm)	MFP6(1.6μm)
20	0.251 mW	0.252 mW	0.252 mW	0.2253 mW	0.253 mW	0.254 mW
30	0.2904 mW	0.289 mW	0.289 mW	0.289 mW	0.289 mW	0.29 mW
40	0.3051 mW	0.305 mW	0.304 mW	0.304 mW	0.303 mW	0.3011 mW
50	0.306 mW	0.301 mW	0.2996 mW	0.3009 mW	0.299 mW	0.2914 mW
60	0.3088 mW	0.309 mW	0.3048 mW	0.287 mW	0.286 mW	0.304 mW
70	0.31732 mW	0.287 mW	0.2772 mW	0.275 mW	0.274 mW	0.288 mW

Table 5.28 Power of copper interconnect with variation in W/L of driver for semiglobal interconect (400μm).

W/L)	power(mW)
20	0.1324
30	0.1506
40	0.162
50	0.1738
60	0.183
70	0.1941

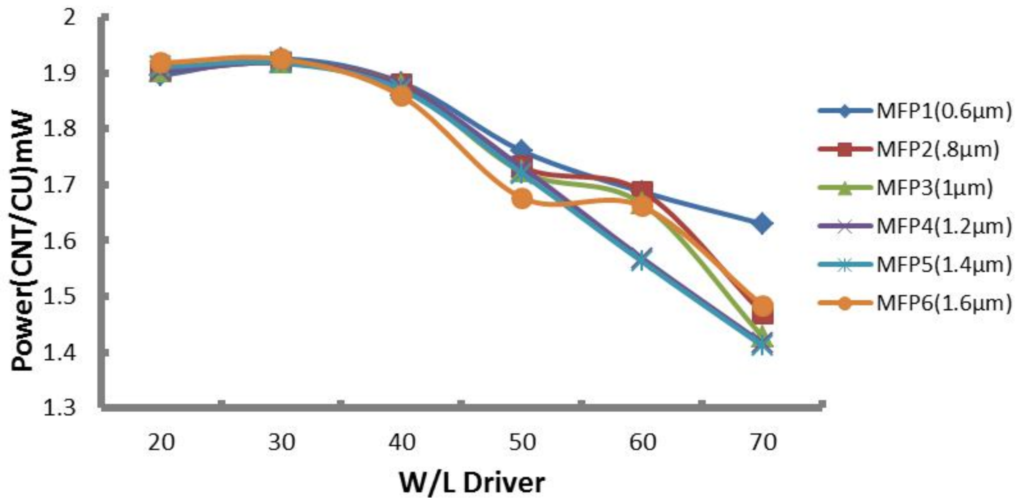


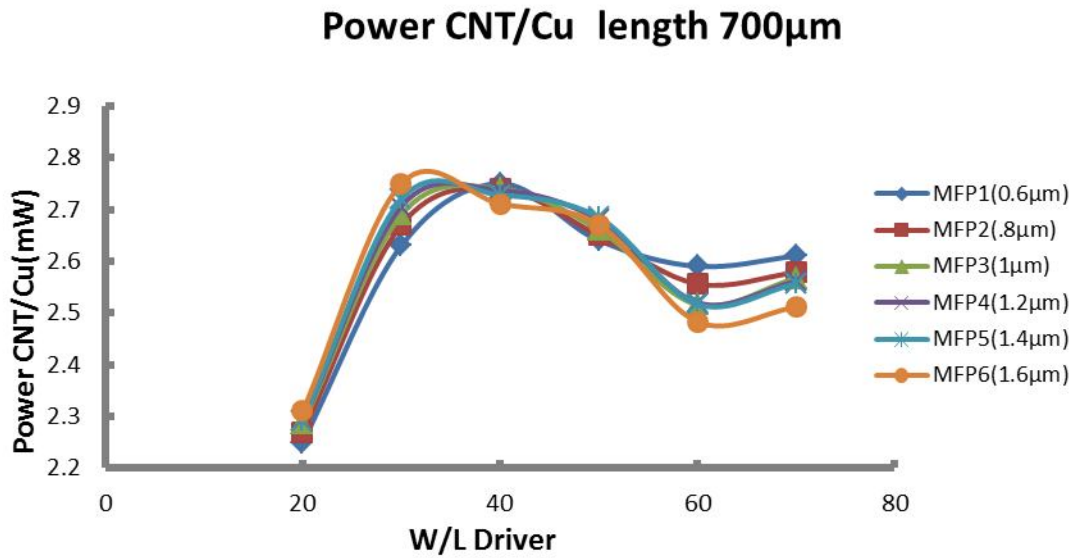
Fig.5.19 Normalized power versus W/L ratio as a functionality MFP for semiglobal interconnect(400µm).

Table 5.29 Power of bundle SWCNT with different MFP and W/L of driver for semiglobal interconnect(700µm).

W/L)	MFP1(0.6µm)	MFP2(.8µm)	MFP3(1µm)	MFP4(1.2µm)	MFP5(1.4µm)	MFP6(1.6µm)
20	0.283 mW	0.285 mW	0.287 mW	0.288 mW	0.288 mW	0.291 mW
30	0.377 mW	0.382 mW	0.385 mW	0.387 mW	0.389 mW	0.394 mW
40	0.429 mW	0.428 mW	0.427 mW	0.427 mW	0.4257 mW	0.423 mW
50	0.436 mW	0.438 mW	0.439 mW	0.443 mW	0.443 mW	0.4407 mW
60	0.459 mW	0.452 mW	0.445 mW	0.446 mW	0.445 mW	0.439 mW
70	0.462 mW	0.4559 mW	0.454 mW	0.4529 mW	0.452 mW	0.444 mW

Table 5.29 Power of copper interconnect with variation in W/L of driver for semiglobal interconnect(700µm)

W/L)	power(mW)
20	0.1256
30	0.143
40	0.156
50	0.16498
60	0.1768
70	0.1768



Fi

g 5.20 Normalized power versus W/L ratio as a functionality MFP(700µm).

5.8.3 Power dissipation at local interconnect

At local interconnect resistance increases due to contact resistance increases. The length of local layer interconnects is about 1 micron, which is within the mean free path of electron in SWCNT. SWCNT bundle with such length can achieve ballistic transport, thus no scattering resistance and leads to reduction in power dissipation as compared to copper interconnect.

Table 5.30 Power of bundle SWCNT at different MFP and W/L of driver for local interconnect(100µm)

W/L)	MFP1(0.6µm)	MFP2(.8µm)	MFP3(1µm)	MFP4(1.2µm)	MFP5(1.4µm)	MFP6(1.6µm)
20	0.143 mW	0.1439 mW	0.144 mW	0.144 mW	0.144 mW	0.144 mW
30	0.1417 mW	0.1417 mW	0.1417 mW	0.1417 mW	0.1417 mW	0.1416 mW
40	0.1357 mW	0.1352 mW	0.1349 mW	0.1347 mW	0.1346 mW	0.1339 mW
50	0.1318 mW	0.1311 mW	0.1305 mW	0.13012 mW	0.1298 mW	0.128 mW
60	0.1294 mW	0.127 mW	0.1265 mW	0.1259 mW	0.1254 mW	0.1236 mW
70	0.127 mW	0.1263 mW	0.1256 mW	0.1251 mW	0.1247 mW	0.1233 mW

Table 5.31 Power of copper interconnect with variation in W/L of driver for local interconnect(100μm)

W/L)	power(mW)
20	0.105
30	0.1187
40	0.1159
50	0.119
60	0.1223
70	0.1225

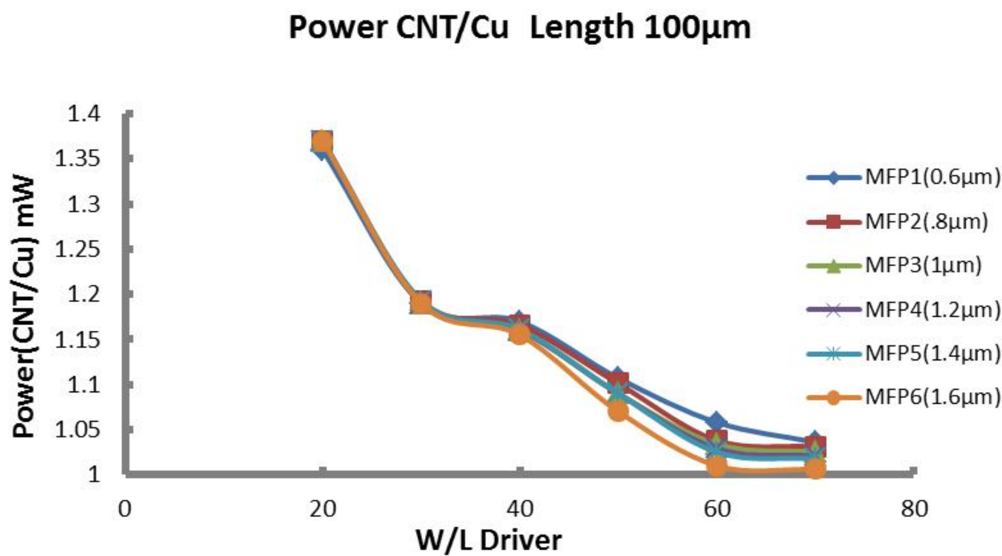


Fig.5.21 Normalized power versus W/L ratio as a functionality of MFP local interconnect(100μm).

Table 5.32 Power of bundle SWCNT at different MFP and W/L of driver for local interconnect(50μm)

W/L)	MFP1(0.6μm)	MFP2(.8μm)	MFP3(1μm)	MFP4(1.2μm)	MFP5(1.4μm)	MFP6(6μm)
20	0.126 mW	0.1216 mW	0.126 mW	0.1257 mW	0.126 mW	0.1264 mW
30	0.127 mW	0.1277 mW	0.1277 mW	0.127 mW	0.1277 mW	0.127 mW
40	0.1226 mW	0.1224 mW	0.1222 mW	0.105 mW	0.12208 mW	0.1217 mW
50	0.116 mW	0.1156 mW	0.115 mW	0.1171 mW	0.1149 mW	0.1142 mW
60	0.1136 mW	0.1129 mW	0.125 mW	0.1149 mW	0.112 mW	0.111 mW
70	0.1126 mW	0.1194 mW	0.1114 mW	0.1141 mW	0.1109 mW	0.109 mW

Table 5.33 Power of copper interconnect with variation in W/L of driver for local interconnect(50µm)

W/L)	power(mW)
20	0.109
30	0.1137
40	0.148
50	0.1162
60	0.1178
70	0.1196

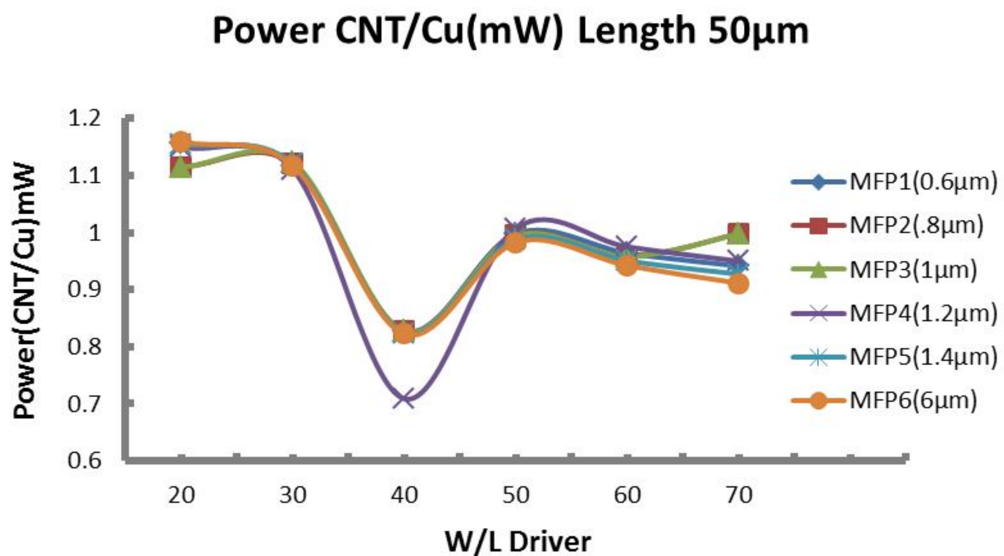


Fig.5.22 Normalized power versus W/L ratio as a fuctionality MFP(length 50µm).

CHAPTER 6

RESULT AND DISCUSSIONS

The resistance, inductance and capacitance of the π-RLC equivalent circuit can be obtained by appropriate use of expression available in [39]. The equivalent circuit of an interconnect of a CNT bundle is used to SPICE simulate signal propagation down SWCNT- interconnect at 32nm technology node. Simulation is also carried out for copper interconnects of same technology and clock speed (0.1GHz). For simulation purpose copper interconnect is modeled by a π equivalent circuit [40].

For both SWCNT and copper interconnect 90% delay and Power has been experienced from the SPICE simulation result. Predictive Technology model [41] has been used for the CMOS driver. Copper interconnect delay and power dissipation are used to normalized corresponding SWCNT interconnect propagation delay and power dissipation.

The normalized quantities are thus relative measures of CNT interconnect delay and power dissipation with respect to those of copper interconnect.

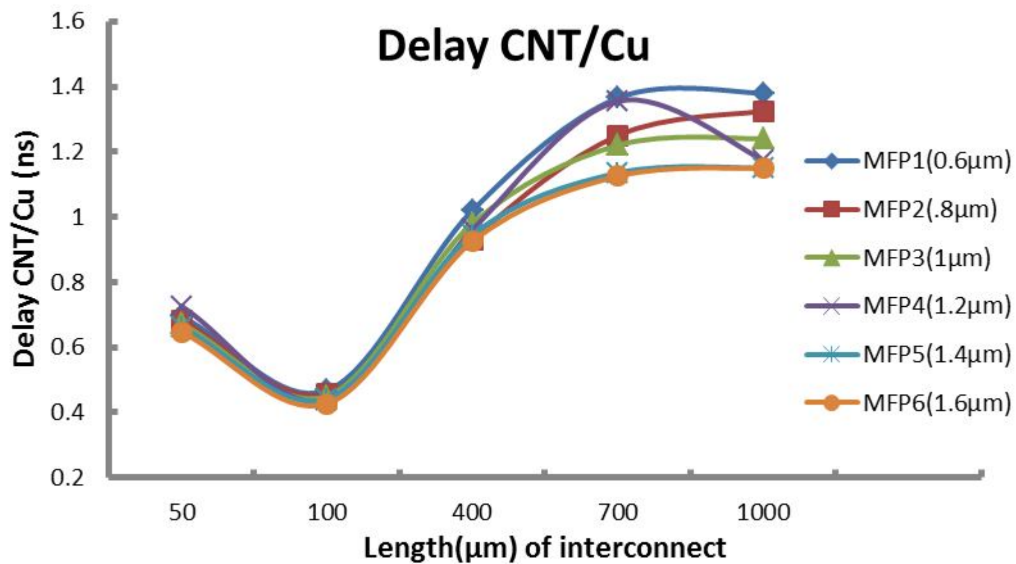


Fig 6.1 Normalized delay versus length of interconnect as a functionality MFP.

Fig6.1 reveals that normalized delay increases with increase in interconnect length whereas graph also reflect that normalized delay increases with decrease in MFP because MFP is inversely proportional to the resistance.

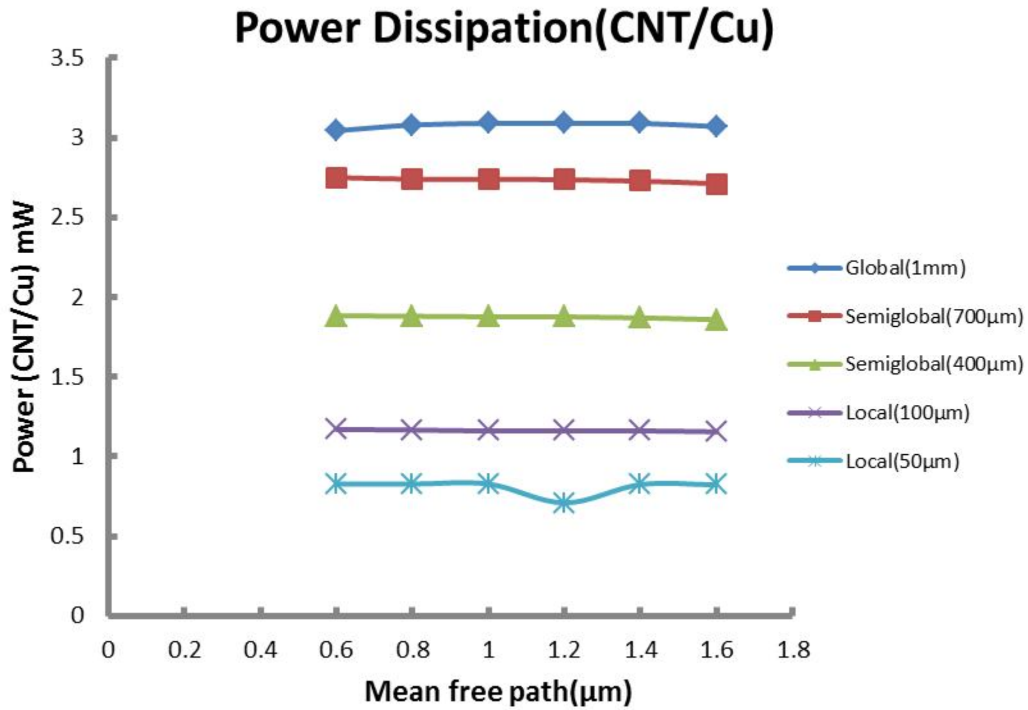


Fig.6.2 Normalized power dissipation of bundled SWCNT and Cu at global, semiglobal and local interconnect at different mean free path.

Fig5.2, shows that the normalized power versus W/L ratio of driver transistor as a function of interconnect length. This graph reveal that power ratio is almost constant for a different aspect ratio but we got higher power dissipation at global length of interconnect.

CHAPTER 7

SUMMARY

The influence of mean free path (MFP), interconnect width and aspect ratio of driver transistor on SWCNT bundle interconnect is critically examined in this thesis. Spice simulation is used to compare SWCNT interconnect delay and power output with copper interconnect at 32nm Technology node.

The result shows that tube MFP and driver aspect ratio can control SWCNT interconnect delay and power. This can also be utilized to improve power dissipation.

The analysis shows that delay is appreciably increased by decrease in tube MFP and increase in length of interconnects.

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APPENDIX

A.1 PTM Level 54 Model

This model is used in simulation of equivalent circuit model of bundle SWCNT and copper interconnect using SPICE coding.

.model nmos nmos level = 54

```
+version = 4.0       binunit = 1         paramchk= 1         mobmod  = 0
+capmod  = 2         igcmod  = 1         igbmod  = 1         geomod  = 1
+diomod  = 1         rdsmod  = 0         rbodymod= 1         rgatemod= 1
+permod  = 1         acnqsmod= 0         trnqsmod= 0
+tnom    = 27        toxe    = 6.5e-010  toxp    = 4e-010    toxm    = 6.5e-010
+dtox    = 2.5e-010  epsrox  = 3.9       wint    = 5e-009    lint    = 1.35e-009
+ll      = 0         wl      = 0         lln     = 1         wln     = 1
+lw      = 0         ww      = 0         lwn     = 1         wwn     = 1
+lwl     = 0         wwl     = 0         xpart   = 0         toxref  = 6.5e-010
xl      = -9e-9
+dlcig   = 1.35e-009
+vth0    = 0.3692    k1      = 0.2       k2      = 0         k3      = 0
+k3b     = 0         w0      = 2.5e-006  dvt0    = 1         dvt1    = 2
+dvt2    = 0         dvt0w   = 0         dvt1w   = 0         dvt2w   = 0
+dsub    = 0.078     minv    = 0.05      voffl   = 0         dvtp0   = 1e-011
+dvtp1   = 0.1       lpe0    = 0         lpeb    = 0         xj      = 7.2e-009
+ngate   = 1e+023    ndep    = 1.2e+019  nsd     = 2e+020    phin    = 0
+cdsc    = 0         cdscb   = 0         cdscd   = 0         cit     = 0
+voff    = -0.13     nfactor = 2.3       eta0    = 0.0045    etab    = 0
+vfb     = -1.058    u0      = 0.0181    ua      = -5e-010   ub      = 1.7e-018
+uc      = 0         vsat    = 200000    a0      = 1         ags     = 0
+a1      = 0         a2      = 1         b0      = 0         b1      = 0
+keta    = 0.04      dwg     = 0         dwb     = 0         pclm    = 0.06
+pdiblc1 = 0.001     pdiblc2 = 0.001     pdiblcb = -0.005    drout   = 0.5
+pvag    = 1e-020    delta   = 0.01      pscbe1  = 2.0e+009  pscbe2  = 1e-007
+fprout  = 0.2       pdits   = 0.01      pditsd  = 0.23      pditsl  = 2300000
+rsh     = 5         rdsw    = 60        rsw     = 30        rdw     = 30
+rdswmin = 0         rdwmin  = 0         rswmin  = 0         prwg    = 0
+prwb    = 0         wr      = 1         alpha0  = 0.074     alpha1  = 0.005
+beta0   = 30        agidl   = 0.0002    bgidl   = 2.1e+009  cgidl   = 0.0002
+egidl   = 0.8       aigbacc = 0.012     bigbacc = 0.0028    cigbacc = 0.002
+nigbacc = 1         aigbinv = 0.014     bigbinv = 0.004     cigbinv = 0.004
+eigbinv = 1.1       nigbinv = 3         aigc    = 0.0213    bigc    = 0.0025889
+cigc    = 0.002     aigsd   = 0.0213    bigsd   = 0.0025889 cigsd   = 0.002
+nigc    = 1         poxedge = 1         pigcd   = 1         ntox    = 1
+xrcrg1  = 12        xrcrg2  = 5
+cgso    = 7e-011    cgdo    = 7e-011    cgbo    = 0         cgdl    = 7.5e-013
+cgsl    = 7.5e-013  clc     = 1e-007    cle     = 0.6       cf      = 1.1e-010
+ckappas = 0.6       ckappad = 0.6       vfbcv   = -1        acde    = 1
```

```
+moin    = 15          noff    = 1            voffcv  = 0
+kt1     = -0.154      kt1l    = 0            kt2     = 0.022        ute     = -1.1
+ua1     = 1e-009      ub1     = -1e-018      uc1     = -5.6e-011    prt     = 0
+at      = 33000
+fnoimod = 1           tnoimod = 0            noia    = 6.25e+041    noib    = 3.125e+026
+noic    = 8.75e+009   em      = 41000000     af      = 1            ef      = 1
+kf      = 0           tnoia   = 1.5          tnoib   = 3.5          ntnoi   = 1
+jss     = 1.2e-006    jsws    = 2.4e-013     jswgs   = 2.4e-013     njs     = 1
+ijthsfwd= 0.1         ijthsrev= 0.1          bvs     = 10           xjbvs   = 1
+jsd     = 1.2e-006    jswd    = 2.4e-013     jswgd   = 2.4e-013     xjbvd   = 1
+pbs     = 1           cjs     = 0.0018       mjs     = 0.5          pbsws   = 1
+cjsws   = 1.2e-010    mjsws   = 0.33         cjswgs  = 2.1e-010     cjd     = 0.0018
+cjswd   = 1.2e-010    mjswd   = 0.33         pbswgd  = 1            cjswgd  = 2.1e-010
+mjswgd  = 0.33        tpb     = 0            tcj     = 0            tpbsw   = 0
+tcjsw   = 0           tpbswg  = 0            tcjswg  = 0            xtis    = 3
+dmcg    = 0           dmci    = 0            dmdg    = 0            dmcgt   = 0
+dwj     = 0           xgw     = 0            xgl     = 0
+rshg    = 0.4         gbmin   = 1e-010       rbpb    = 5            rbpd    = 15
+rbps    = 15          rbdb    = 15           rbsb    = 15           ngcon   = 1
```

.model pmos pmos level = 54

```
+version = 4.0         binunit = 1            paramchk= 1            mobmod  = 0
+capmod  = 2           igcmod  = 1            igbmod  = 1            geomod  = 1
+diomod  = 1           rdsmod  = 0            rbodymod= 1            rgatemod= 1
+permod  = 1           acnqsmod= 0            trnqsmod= 0
+tnom    = 27          toxe    = 6.7e-010     toxp    = 4e-010       toxm    = 6.7e-010
+dtox    = 2.7e-010    epsrox  = 3.9          wint    = 5e-009       lint    = 1.35e-009
+ll      = 0           wl      = 0            lln     = 1            wln     = 1
+lw      = 0           ww      = 0            lwn     = 1            wwn     = 1
+lwl     = 0           wwl     = 0            xpart   = 0            toxref  = 6.7e-010
xl       = -9e-9
+dlcig   = 1.35e-009
+vth0    = -0.25399    k1      = 0.2          k2      = -0.01        k3      = 0
+k3b     = 0           w0      = 2.5e-006     dvt0    = 1            dvt1    = 2
+dvt2    = -0.032      dvt0w   = 0            dvt1w   = 0            dvt2w   = 0
+dsub    = 0.1         minv    = 0.05         voffl   = 0            dvtp0   = 1e-011
+dvtp1   = 0.05        lpe0    = 0            lpeb    = 0            xj      = 7.2e-009
+ngate   = 1e+023      ndep    = 4.4e+018     nsd     = 2e+020       phin    = 0
+cdsc    = 0           cdscb   = 0            cdscd   = 0            cit     = 0
+voff    = -0.13       nfactor = 2.3          eta0    = 0.0037       etab    = 0
+vfb     = -1.058      u0      = 0.0023       ua      = -5e-010      ub      = 1.6e-018
+uc      = 0           vsat    = 78000        a0      = 1            ags     = 1e-020
+a1      = 0           a2      = 1            b0      = 0            b1      = 0
+keta    = -0.047      dwg     = 0            dwb     = 0            pclm    = 0.1
+pdiblc1 = 0.001       pdiblc2 = 0.001        pdiblcb = 3.4e-008     drout   = 0.6
+pvag    = 1e-020      delta   = 0.01         pscbe1  = 2e+009       pscbe2  = 9.58e-007
+fprout  = 0.2         pdits   = 0.08         pditsd  = 0.23         pditsl  = 2300000
+rsh     = 5           rdsw    = 60           rsw     = 30           rdw     = 30
+rdswmin = 0           rdwmin  = 0            rswmin  = 0            prwg    = 0
```

```
+prwb    = 0           wr      = 1            alpha0  = 0.074        alpha1  = 0.005
+beta0   = 30          agidl   = 0.0002       bgidl   = 2.1e+009     cgidl   = 0.0002
+egidl   = 0.8         aigbacc = 0.012        bigbacc = 0.0028       cigbacc = 0.002
+nigbacc = 1           aigbinv = 0.014        bigbinv = 0.004        cigbinv = 0.004
+eigbinv = 1.1         nigbinv = 3            aigc    = 0.012731     bigc    = 0.00115
+cigc    = 0.0008      aigsd   = 0.012731     bigsd   = 0.00115      cigsd   = 0.0008
+nigc    = 1           poxedge = 1            pigcd   = 1            ntox    = 1
+xrcrg1  = 12          xrcrg2  = 5
+cgso    = 7e-011      cgdo    = 7e-011       cgbo    = 0            cgdl    = 3e-011
+cgsl    = 3e-011      clc     = 1e-007       cle     = 0.6          cf      = 1.1e-010
+ckappas = 0.6         ckappad = 0.6          vfbcv   = -1           acde    = 1
+moin    = 15          noff    = 1            voffcv  = 0
+kt1     = -0.14       kt1l    = 0            kt2     = 0.022        ute     = -1.1
+ua1     = 1e-009      ub1     = -1e-018      uc1     = -5.6e-011    prt     = 0
+at      = 33000
+fnoimod = 1           tnoimod = 0            noia    = 6.25e+041    noib    = 3.125e+026
+noic    = 8.75e+009   em      = 41000000     af      = 1            ef      = 1
+kf      = 0           tnoia   = 1.5          tnoib   = 3.5          ntnoi   = 1
+jss     = 2e-007      jsws    = 4e-013       jswgs   = 4e-013       njs     = 1
+ijthsfwd= 0.1         ijthsrev= 0.1          bvs     = 10           xjbvs   = 1
+jsd     = 2e-007      jswd    = 4e-013       jswgd   = 4e-013       xjbvd   = 1
+pbs     = 1           cjs     = 0.0015       mjs     = 0.5          pbsws   = 1
+cjsws   = 9.4e-011    mjsws   = 0.33         cjswgs  = 2e-010       cjd     = 0.0015
+cjswd   = 9.4e-011    mjswd   = 0.33         pbswgd  = 1            cjswgd  = 2e-010
+mjswgd  = 0.33        tpb     = 0            tcj     = 0            tpbsw   = 0
+tcjsw   = 0           tpbswg  = 0            tcjswg  = 0            xtis    = 3
+dmcg    = 0           dmdg    = 0            dmcgt   = 0            xgw     = 0
+xgl     = 0
+rshg    = 0.1         gbmin   = 1e-012       rbpb    = 50           rbpd    = 50
+rbps    = 50          rbdb    = 50           rbsb    = 50           ngcon   = 1
```

A.2 SPICE Coding for Global interconnect.

For global interconnect number of repeaters are 8 and operating frequency is 0.1GHz

```
MMOSFET_N_1 N_1 In Gnd Gnd NMOS L=32n W=640n AD=51.2f PD=1.44u
AS=51.2f PS=1.44u
MMOSFET_N_2 N_6 N_3 Gnd Gnd NMOS L=32n W=640n AD=51.2f PD=1.44u
AS=51.2f PS=1.44u
MMOSFET_N_3 N_7 N_4 Gnd Gnd NMOS L=32n W=640n AD=51.2f PD=1.44u
AS=51.2f PS=1.44u
MMOSFET_N_4 N_10 N_9 Gnd Gnd NMOS L=32n W=640n AD=51.2f PD=1.44u
AS=51.2f PS=1.44u
MMOSFET_N_5 N_13 N_12 Gnd Gnd NMOS L=32n W=640n AD=51.2f PD=1.44u
AS=51.2f PS=1.44u
MMOSFET_N_6 N_16 N_15 Gnd Gnd NMOS L=32n W=640n AD=51.2f PD=1.44u
AS=51.2f PS=1.44u
MMOSFET_N_7 N_19 N_18 Gnd Gnd NMOS L=32n W=640n AD=51.2f PD=1.44u
AS=51.2f PS=1.44u
```

MMOSFET_N_8 N_22 N_21 Gnd Gnd NMOS L=32n W=640n AD=51.2f PD=1.44u AS=51.2f PS=1.44u
MMOSFET_N_9 N_25 N_24 Gnd Gnd NMOS L=32n W=640n AD=51.2f PD=1.44u AS=51.2f PS=1.44u
****
MMOSFET_P_1 N_1 In Vdd Vdd PMOS L=32n W=1920n AD=.15p PD=4u AS=.15p PS=4u
MMOSFET_P_2 N_6 N_3 Vdd Vdd PMOS L=32n W=1920n AD=.15p PD=4u AS=.15p PS=4u
MMOSFET_P_3 N_7 N_4 Vdd Vdd PMOS L=32n W=1920n AD=.15p PD=4u AS=.15p PS=4u
MMOSFET_P_4 N_10 N_9 Vdd Vdd PMOS L=32n W=1920n AD=.15p PD=4u AS=.15p PS=4u
MMOSFET_P_5 N_13 N_12 Vdd Vdd PMOS L=32n W=1920n AD=.15p PD=4u AS=.15p PS=4u
MMOSFET_P_6 N_16 N_15 Vdd Vdd PMOS L=32n W=1920n AD=.15p PD=4u AS=.15p PS=4u
MMOSFET_P_7 N_19 N_18 Vdd Vdd PMOS L=32n W=1920n AD=.15p PD=4u AS=.15p PS=4u
MMOSFET_P_8 N_22 N_21 Vdd Vdd PMOS L=32n W=1920n AD=.15p PD=4u AS=.15p PS=4u
MMOSFET_P_9 N_25 N_24 Vdd Vdd PMOS L=32n W=1920n AD=.15p PD=4u AS=.15p PS=4u
****
LInductor_1 N_2 N_3 13.54p
LInductor_2 N_5 N_4 13.54p
LInductor_3 N_8 N_9 13.54p
LInductor_4 N_11 N_12 13.54p
LInductor_5 N_14 N_15 13.54p
LInductor_6 N_17 N_18 13.54p
LInductor_7 N_20 N_21 13.54p
LInductor_8 N_23 N_24 13.54p
LInductor_9 N_26 Out 13.54p
****
RResistor_1 N_1 N_2 58.03 TC=0.0, 0.0
RResistor_2 N_6 N_5 58.03 TC=0.0, 0.0
RResistor_3 N_7 N_8 58.03 TC=0.0, 0.0
RResistor_4 N_10 N_11 58.03 TC=0.0, 0.0
RResistor_5 N_13 N_14 58.03 TC=0.0, 0.0
RResistor_6 N_16 N_17 58.03 TC=0.0, 0.0

RResistor_7 N_19 N_20 58.03 TC=0.0, 0.0
RResistor_8 N_22 N_23 58.03 TC=0.0, 0.0
RResistor_9 N_25 N_26 58.03 TC=0.0, 0.0
****
CCapacitor_1 N_3 Gnd 398.8f
CCapacitor_2 N_4 Gnd 398.8f
CCapacitor_3 N_9 Gnd 398.8f
CCapacitor_4 N_12 Gnd 398.8f
CCapacitor_5 N_15 Gnd 398.8f
CCapacitor_6 N_18 Gnd 398.8f
CCapacitor_7 N_21 Gnd 398.8f
CCapacitor_8 N_24 Gnd 398.8f
CCapacitor_9 Out Gnd 398.8f
CCapacitor_10 Out Gnd 1p

********* Simulation Settings - Additional SPICE commands *********
Vdd Vdd Gnd 0.9v
VIn In Gnd PULSE (0 0.9 0 1n 1n 4n 10n)
.power Vdd 1n 8n
.Tran 1n 40ns
.print v(Out) V(In)
********* Simulation Settings - Additional SPICE commands *********
.end

A.3 SPICE coding for Semiglobal Interconnect

For semiglobal interconnect number of repeaters are 6 and operating frequency is 0.1GHz
MMOSFET_N_1 N_1 In Gnd Gnd NMOS L=32n W=2240n AD=179.2f PD=4.64u AS=179.2f PS=4.64u
MMOSFET_N_2 N_5 N_2 Gnd Gnd NMOS L=32n W=2240n AD=179.2f PD=4.64u AS=179.2f PS=4.64u
MMOSFET_N_3 N_8 N_6 Gnd Gnd NMOS L=32n W=2240n AD=179.2f PD=4.64u AS=179.2f PS=4.64u
MMOSFET_N_4 N_11 N_9 Gnd Gnd NMOS L=32n W=2240n AD=179.2f PD=4.64u AS=179.2f PS=4.64u
MMOSFET_N_5 N_14 N_12 Gnd Gnd NMOS L=32n W=2240n AD=179.2f PD=4.64u AS=179.2f PS=4.64u
MMOSFET_N_6 N_17 N_15 Gnd Gnd NMOS L=32n W=2240n AD=179.2f PD=4.64u AS=179.2f PS=4.64u
MMOSFET_N_7 N_20 N_18 Gnd Gnd NMOS L=32n W=2240n AD=179.2f PD=4.64u AS=179.2f PS=4.64u

****
***
MMOSFET_P_1 N_1 In Vdd Vdd PMOS L=32n W=6720n AD=537.6f PD=13.6u AS=537.6f PS=13.6u
MMOSFET_P_2 N_5 N_2 Vdd Vdd PMOS L=32n W=6720n AD=537.6f PD=13.6u AS=537.6f PS=13.6u
MMOSFET_P_3 N_8 N_6 Vdd Vdd PMOS L=32n W=6720n AD=537.6f PD=13.6u AS=537.6f PS=13.68u
MMOSFET_P_4 N_11 N_9 Vdd Vdd PMOS L=32n W=6720n AD=537.6f PD=13.6u AS=537.6f PS=13.6u
MMOSFET_P_5 N_14 N_12 Vdd Vdd PMOS L=32n W=6720n AD=537.6f PD=13.6u AS=537.6f PS=13.6u
MMOSFET_P_6 N_17 N_15 Vdd Vdd PMOS L=32n W=6720n AD=537.6f PD=13.6u AS=537.6f PS=13.6u
MMOSFET_P_7 N_20 N_18 Vdd Vdd PMOS L=32n W=6720n AD=537.6f PD=13.6u AS=537.6f PS=13.6u
****
***
CCapacitor_1 N_2 Gnd 384.2f
CCapacitor_2 N_6 Gnd 384.2f
CCapacitor_3 N_9 Gnd 384.2f
CCapacitor_4 N_12 Gnd 384.2f
CCapacitor_5 N_15 Gnd 384.2f
CCapacitor_6 N_18 Gnd 384.2f
CCapacitor_7 Out Gnd 384.2f
CCapacitor_8 Out Gnd 1p
****
***
LInductor_1 N_3 N_2 12.188f
LInductor_2 N_4 N_6 12.188f
LInductor_3 N_7 N_9 12.188f
LInductor_4 N_10 N_12 12.188f
LInductor_5 N_13 N_15 12.188f
LInductor_6 N_16 N_18 12.188f
LInductor_7 N_19 Out 12.188f
****
***
RResistor_1 N_1 N_3 52.23 TC=0.0, 0.0
RResistor_2 N_5 N_4 52.23 TC=0.0, 0.0
RResistor_3 N_8 N_7 52.23 TC=0.0, 0.0
RResistor_4 N_11 N_10 52.23 TC=0.0, 0.0
RResistor_5 N_14 N_13 52.23 TC=0.0, 0.0
RResistor_6 N_17 N_16 52.23 TC=0.0, 0.0

RResistor_7 N_20 N_19 52.23 TC=0.0, 0.0

********* Simulation Settings - Additional SPICE commands *********
Vdd Vdd Gnd 0.9v
VIn In Gnd PULSE (0 0.9 0 1n 1n 4n 10n)
.power Vdd 1n 8n
.Tran 1n 40ns
.print v(Out) V(In)
********* Simulation Settings - Additional SPICE commands *********

********* Simulation Settings - Additional SPICE commands *********

.end

A.3 SPICE coding for Local Interconnect

For local interconnects number of repeaters are 2 and operating frequency is 0.1GHz.
MMOSFET_N_1 N_1 In Gnd Gnd NMOS L=32n W=2240n AD=153.6f PD=4.64u AS=179.2f PS=4.64u
MMOSFET_N_2 N_6 N_3 Gnd Gnd NMOS L=32n W=2240n AD=153.6f PD=4.64u AS=179.2f PS=4.64u
MMOSFET_N_3 N_8 N_4 Gnd Gnd NMOS L=32n W=2240n AD=153.6f PD=4.64u AS=179.2f PS=4.64u
****

MMOSFET_P_1 Vdd In N_1 Vdd PMOS L=32n W=6720n AD=537.6f PD=13.6u AS=537.6f PS=13.6u
MMOSFET_P_2 Vdd N_3 N_6 Vdd PMOS L=32n W=6720n AD=537.6f PD=13.6u AS=537.6f PS=13.6u
MMOSFET_P_3 Vdd N_4 N_8 Vdd PMOS L=32n W=6720n AD=537.6f PD=13.6u AS=537.6f PS=13.6u
****
LInductor_1 N_1 N_2 2.03f
LInductor_2 N_6 N_5 2.03f
LInductor_3 N_8 N_7 2.03f
****
CCapacitor_1 N_3 Gnd 64.31f
CCapacitor_2 N_4 Gnd 64.31f
CCapacitor_3 Out Gnd 64.31f

```
CCapacitor_4 Out Gnd 1p
*************************************************************************
***
RResistor_1 N_2 N_3 8.705 TC=0.0, 0.0
RResistor_2 N_5 N_4 8.705 TC=0.0, 0.0
RResistor_3 N_7 Out 8.705 TC=0.0, 0.0
********* Simulation Settings - Additional SPICE commands *********
Vdd Vdd Gnd 0.9v
VIn In Gnd PULSE (0 0.9 0 1n 1n 4n 10n)
.power Vdd 1n 8n
.Tran 1n 40ns
.print v(Out) V(In)
********* Simulation Settings - Additional SPICE commands *********
.end
```