“The Effect of Intercalation Doping on the Performance of Multi-Layer Graphene Nano Ribbons as VLSI Interconnects for Deep-Submicron technology nodes”

Dissertation submitted towards the partial fulfillment of requirement for the award of degree of

Master of Technology
In
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DECLARATION

I hereby declare that the work which is being presented in the dissertation titled **"The Effect of Intercalation Doping on the Performance of Multi-Layer Graphene Nano Ribbons as VLSI interconnects for Deep-submicron technology nodes"** in the partial fulfillment of the requirement for the award of the degree of Master of Technology in VLSI Design submitted in Electronics and Communication Engineering Department of Thapar University, Patiala is an authentic record of my study carried out as under guidance of **Dr.Karamjit Singh Sandha** (Assistant Professor, ECED) during 2014-2016.

Date: 15/7/16
Place: Patiala

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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The study has indeed helped me to explore knowledge and avenues related to my topic and I am sure this will help me in my future.

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ABSTRACT

Performance of deep micron and sub-micron circuits is deeply impacted by the interconnect due to reduced pitch size. With the reduction of technology below 45nm, the resistivity of copper increases drastically. The surface grain boundary scattering and electro-migration problem causes serious degradation in performance of copper as interconnect material.

With the invention of graphene, GNR's are the major contenders of replacing copper as a VLSI interconnect. In this dissertation, the applicability of MLGNR as interconnect material is studied. With the advantage of relatively easy manufacturing of GNR's when compared with copper and retaining high mean free path and thermal stability makes it a dominant contender for interconnect material. The impact of Fermi energy on the propagation delay and power dissipation is studied. The increase in Fermi energy is the direct impact of increasing doping in MLGNR interconnects. With the addition of suitable dopant atoms the Fermi energy of GNR interconnects increases. This result in reduced parasitic components involved with interconnects material. This decrease in RLC parameters directly causes reduce delay and power dissipation of MLGNR interconnects. The results obtained by varying Fermi energy of MLGNR are also compared with copper interconnects. The obtained results shows improvement in performance of graphene ribbons with increased doping

The variation of delay and power dissipation of MLGNR is also discussed by varying the technology node. A suitable number of repeaters are inserted to obtain the performance analysis of GNR interconnects .As the scaling continues, the delay as well as power of MLGNR increases. The performance variation between copper and MLGNR interconnect is observed at higher global interconnect lengths. Thus MLGNR with suitable Fermi energy has a potential to replace copper at global interconnect lengths.

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LIST OF ACRONYMS

GNR	Graphene Nano Ribbons
CNT	Carbon Nano Tube
SLGNR	Single-Layer Graphene Nano Ribbons
MLGNR	Single-Layer Graphene Nano Ribbons
ESC	Equivalent Single Conductor
MFP	Mean free path
DIL	Driver Interconnect Load
VLSI	Very Large Scale Integration
SWCNT	Single Wall Carbon Nano Tube
MWCNT	Multi Wall Carbon Nano Tube
ITRS	International Technology Roadmap for Semiconductors
PDP	Power Delay Product

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CHAPTER 1

INTRODUCTION

1.1 Motivation

A VLSI interconnect is a thin film of conducting material which provide electrical connection between different nodes of the circuit. The function of interconnect is to provide electrical connection between different blocks in the circuit [1]. Power and clock to all the blocks are also provided by interconnect. On the basis of length of interconnects, it can be divided into three parts i.e. local, intermediate and global interconnects. Local interconnects consist of very small lines, connecting gates and transistors inside a functional block. They consist of only a few transistors and make first and second metal layers. Intermediate interconnects are wider and longer than local interconnects. These are made longer so that it can provide lower resistance. Intermediate are used for clock distribution within a length of 3- 4 nm. The back end of line is shown in Figure 1.1 which shows local, intermediate and global levels [2]. Global interconnects are used for clock and power distribution and make top few layers.

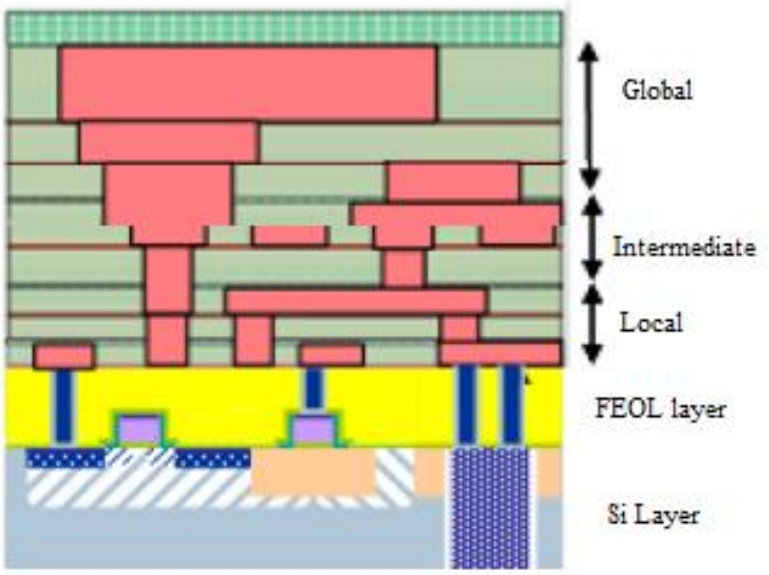

Figure 1.1 Schematic showing the hierarchy of metal levels for distribution of interconnects [2]

In a modern VLSI technology, the interconnection between various components on the chip has become complex task. With the miniaturization of transistors, the interconnect dimensions and the device packing are also reduced [3].Earlier aluminum was used as a interconnect material. This was because of good conductivity and better adherence with silicon. At higher integration level, the problem with aluminum is electro migration problem whereas copper has high current carrying capacity and is immune to electro migration problem up to certain extent. Therefore a one-time transition from aluminum to copper is made. The current interconnect material (Cu) has a lot of problems as scaling continues. Improvement in new technology also resulted in reduction of feature size. The resistivity of copper interconnect increases very sharply when the dimensions are of the order of mean free path. This is due to the surface roughness and grain boundary scattering. The result is increase in propagation delay, electro migration and power dissipation. Various interconnect materials are shown in Figure 1.2

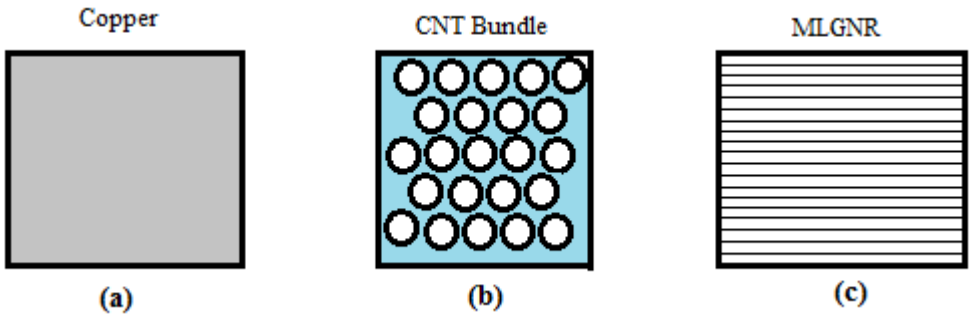

Figure 1.2 Resistance structures a) copper interconnect b) CNT-bundle c) MLGNR [3]

Graphene is considered as potential candidates for replacing copper as VLSI interconnect. Graphene is a two dimensional mono-atomic allotrope of carbon [3]. The unique properties of graphene like electrical, thermal and mechanical properties makes it a potential candidate for interconnect as well as fabricating transistors. Graphene can sustain higher current density approximately three times as that of copper [3]. Electrons in graphene can travel longer distance without scattering, thus having longer mean free path when compared with copper [4-5]. There are two current research topics which have the potential to replace copper as VLSI interconnect, these are CNT and GNR. Carbon nanotubes (CNTs) are

graphene sheets rolled up into cylinders with diameter of the order of a nanometer. On the basis of number of shells

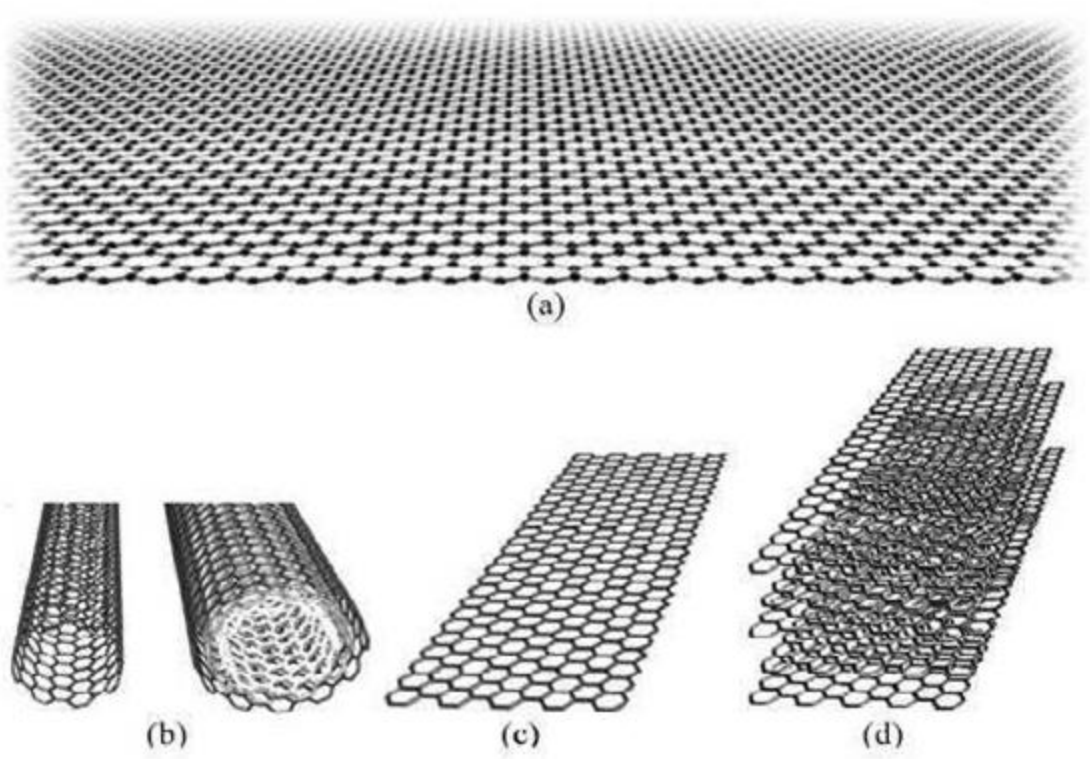

Figure 1.3 Geometries of graphene a) sheet of graphene b) CNT c) SLGNR d) MLGNR. [5]

The geometries of various structures of graphene is shown in Figure 1.3.The various types of interconnect models are shown. Figure 1.3(a) shows the geometries of graphene through which various interconnect models are made. Figure 1.3(b) shows the carbon nano tubes which are in the form of cylindrical shape. The CNT may be single walled or multi walled depending upon structure. Figure 1.3(c) shows the single layer GNR, but because of higher resistance of SLGNR, it cannot be used in interconnect applications. Figure 1.3(d) shows the MLGNR interconnect which has the potential to replace copper as interconnect. GNR's are the unrolled version of carbon nano tubes. In a simple way, single layer GNR's are unrolled version of Single Wall CNT whereas MLGNR are the unrolled version of MWCNT interconnect. The suitable doping along with layer spacing is must for better performance. Also edge defects in MLGNR due to manufacturing small GNR is also a big problem. The

various geometries of graphene have the potential to replace copper as interconnect whether it is a multi-wall carbon nano tubes or multi-layer graphene nano ribbons.

1.2 Introduction of copper interconnect

Since the invention of integrated circuits, aluminium and silicon dioxide were the interconnect material and insulated material respectively. The industry has done a one-time transition from aluminium to copper interconnect. As the feature size increased, the electro migration problem in aluminium is increased. When compared with aluminium, copper is a lot better option for interconnect applications. The most important benefit of copper when compared with aluminium is that copper has lower resistivity. The use of low resistivity in copper and immunity to electro migration causes reduction in propagation delay and power dissipation in integrated circuits. The speed of integrated circuit is determined by the efficiency of transistor to switch between Vcc to ground. The speed limit of transistor is decided by the propagation delay. With the reduction of technology, the delay of transistor reduces but the propagation delay of interconnect is not reducing at the same pace. The propagation delay is determined by the time constant of the circuit. The time constant is further dependent on resistive and capacitive components. RC time constant can be reduced by reducing the resistivity of material or by using low permittivity material. Copper has lower resistivity as compared to aluminium and provides an improvement of 40% reduction in resistivity. So this reduction in resistivity causes reduction of propagation delay, since resistance of copper is proportional to the resistivity and propagation delay of copper is proportional to the resistance of copper. The propagation delay can be further reduced by combining the reduction in resistivity and proper selection of dielectric material. Other major advantage of copper over aluminium is better thermal conductivity. It has been experimentally observed that copper is 100 times immune to electro migration when compared with aluminium. Electro migration causes damage to the atoms due to higher current density resulting in breakdown of material. There are other benefits of using copper, including the improvement in routing. The number of metal layers was also reduced by using copper as interconnect material. As the scaling trend continues, the performance of copper as interconnect is reduced. With the manufacturing of 2-D graphene and better lithography techniques, graphene based interconnect materials can replace copper as interconnect.

1.3 Analysis of copper as a VLSI interconnect

In copper interconnects, CMOS is used to drive an interconnect load. The model of copper as interconnect is shown in Figure 1.4. The ratio of NMOS and PMOS are selected according to the ITRS standards. Other parameters like power supply are also taken from IRTS 2013 [2]. The interconnect load, driven by the CMOS inverter can be evaluated by the transmission line model. The interconnect load can be further broken into the passive components. The suitable number of repeaters must also be inserted to reduce the propagation delay of interconnect at the cost of increasing the power dissipation.

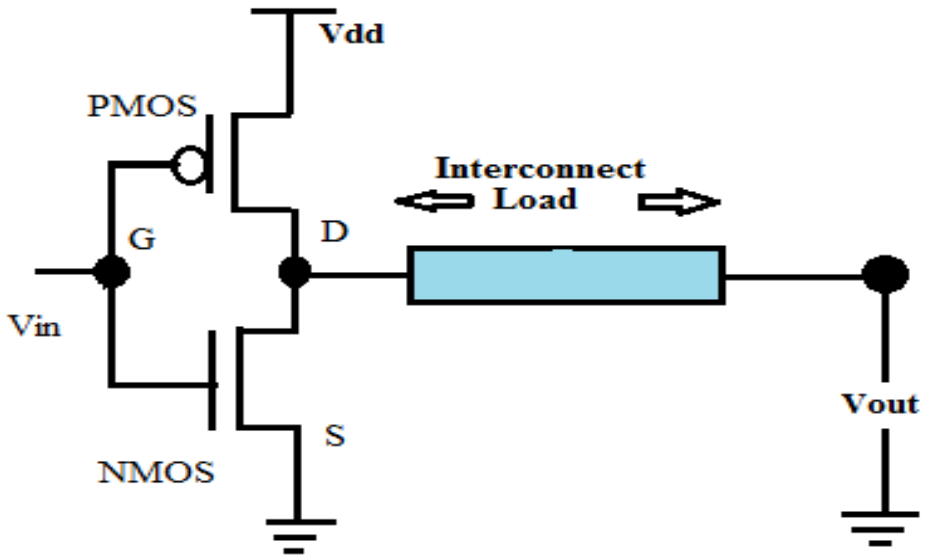

Figure 1.4 CMOS driving an interconnect load

1.3.1 Modeling of copper interconnect

The modeling of a global interconnect is mainly regarded as a major problem in designing of high speed designing. This issue has been discussed in a number of recent researches, and a lot of optimization techniques have been developed. For a different technology nodes, the interconnect thickness ‘t’, the height of the metal layer from the substrate ‘h’, the width ‘w’ and spacing between the signal and ground line ‘s’ are the main variables used in the designing and optimization of global interconnect.

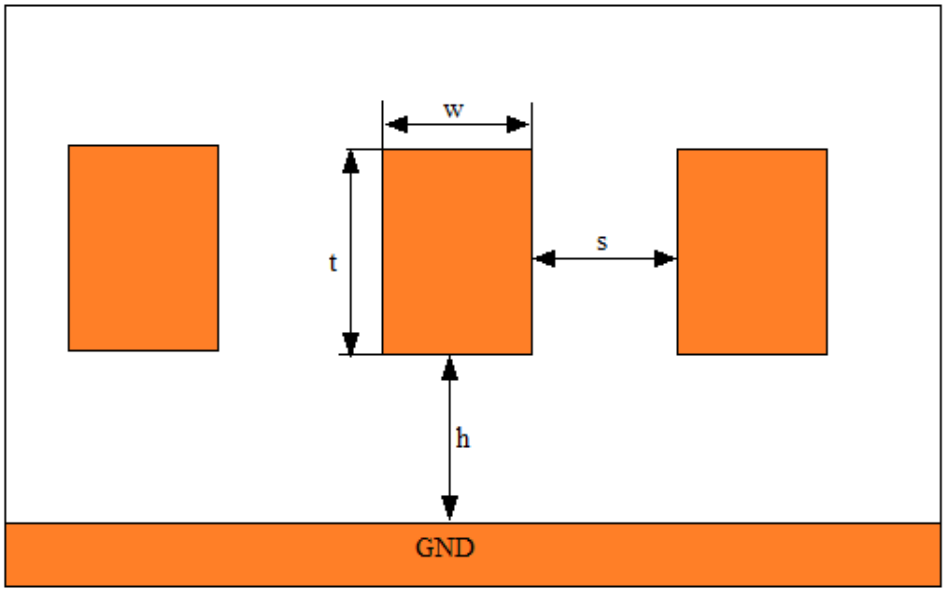

Figure 1.5 Cross-section of global interconnect [20].

The cross section of global interconnect is shown in Figure 1.5. The height, width, spacing and thickness of interconnect are technology dependent and changes with the variation in technology node. These values are taken from the International Technology Roadmap for Semiconductors (ITRS) 2013 [2].Based on these dimensions the interconnect load can be modeled into transmission line. The parasitic components of a interconnect load i.e resistance, capacitance and inductance are calculated accordingly. After calculation of these values, the propagation delay of copper and power dissipation are calculated according to SPICE simulations. The technology variation causes the changes in parasitic components of transmission line. As a result the impact is imposed on propagation delay and power dissipation of copper interconnect

Resistance (*R*) of copper interconnect:

$$R = \frac{\rho . l}{w . t} \tag{1.1}$$

Where ρ =is the resistivity of copper

l= length of interconnect

w= width of interconnect

t= thickness of interconnect

Inductance (*L*) of copper interconnect:

In a rectangular conductor the inductance is produced due to the changing of current in the wire. In this a magnetic-field is created due to the change in current flow which induces a voltage, thus producing an inductance called self-inductance and is given by the equation 1.2. In copper , there exists another type of inductance called mutual inductance. This inductance is due to the magnetic coupling between different layers of interconnect and is given by equation 1.3

$$L = \frac{\mu_0 . l}{2\pi}\left[\ln\left(\frac{2l}{w+t}\right)+\frac{1}{2}+\frac{0.22(w+t}{l}\right] \quad (1.2)$$

$$M = \frac{\mu_0 . l}{2\pi}\left[\ln\left(\frac{2l}{h}\right)-1+\frac{h}{l}\right] \quad (1.3)$$

Capacitance (*C*) of copper interconnect:

The interconnect line is considered as a conducting plate which is parallel to the ground plane, acting as another plate. The capacitance induced due to these parallel plates is called parallel plate capacitance and is given by equation 1.15. The thickness of interconnect is quite noticeable and produce another type of capacitance called fringing capacitance. The equation 1.15 contains both fringing and parallel plate capacitance.

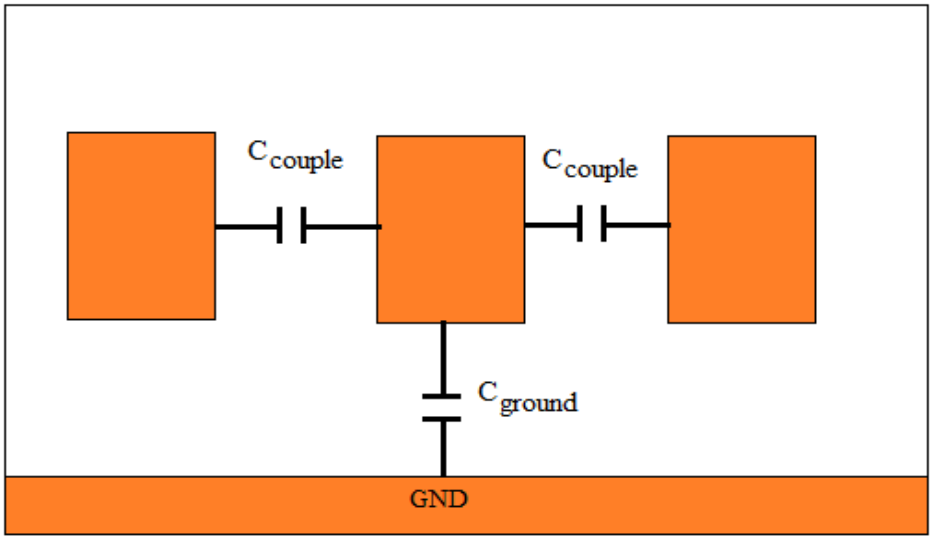

Figure 1.6 various Capacitance in copper interconnect [20]

The coupling capacitance is produced due to the interaction of different layers of copper and is given by equation 1.6.

C_t =total capacitance of wire

$$C_t = C_g + 2C_C \tag{1.4}$$

$$C_g = \in \left[\frac{w}{h} + 0.22 \left(\frac{s}{s+0.70h} \right)^{3.19} + 1.17 \left(\frac{s}{s+1.51h} \right)^{0.76} \cdot \left(\frac{t}{t+4.53h} \right)^{0.12} \right] \tag{1.5}$$

C_g =area and fringe flux to the underlying plane

$$C_c = \in \left[1.14 \frac{t}{s} \left(\frac{h}{h+2.06s} \right)^{0.09} + 0.74 \left(\frac{w}{w+1.59s} \right)^{1.14} + 1.16 \left(\frac{w}{w+1.87s} \right)^{0.16} \cdot \left(\frac{h}{h+0.98s} \right)^{1.18} \right] \tag{1.6}$$

C_c=coupling capacitance

h= Height of metal layer from the substrate

s = Spacing between the signal and ground line

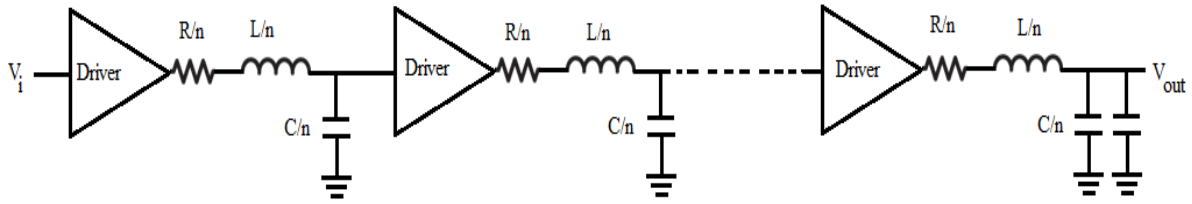

Figure 1.7 Copper interconnect with repeaters and R, L and C parameters

By inserting proper number of repeaters and calculating RLC values, proper delay estimation can be done. As the technology reduces, the problem in copper being used as a interconnect increases. There is a drastic increase propagation delay and power dissipation of copper interconnects. The RLC equations are taken from predictive technology models [20]. These equations are used for calculating RLC parameters .Figure1.7 shows the model used for simulation. The value of n depends on technology node and appropriate power delay product achieved. The number of repeaters can vary from 3 to 9 depending upon the technology node.

1.4 Graphene Nano Ribbon interconnects

Introduction

Graphene is a flat two-dimensional (2D) single atomic layer sheet of carbon atoms. These atoms are packed into a honeycomb lattice. Graphene is made in the form of ribbons to use it as a VLSI interconnect material. GNR are the unrolled version of CNT and were extracted in 2004 and soon after that, it is proposed as a potential candidate for use as interconnect. Earlier it was believed that 2D structures are unstable and cannot exist but after the discovery of graphene a lot of research work started on graphene based interconnects to replace copper. Graphene shows excellent properties which makes it a potential candidate. Graphene shows good electronic and thermal properties which are similar to that of CNT. The atomic bonding in carbon is the strongest bond among different elements, resulting in graphene to be immune to electro migration problem.

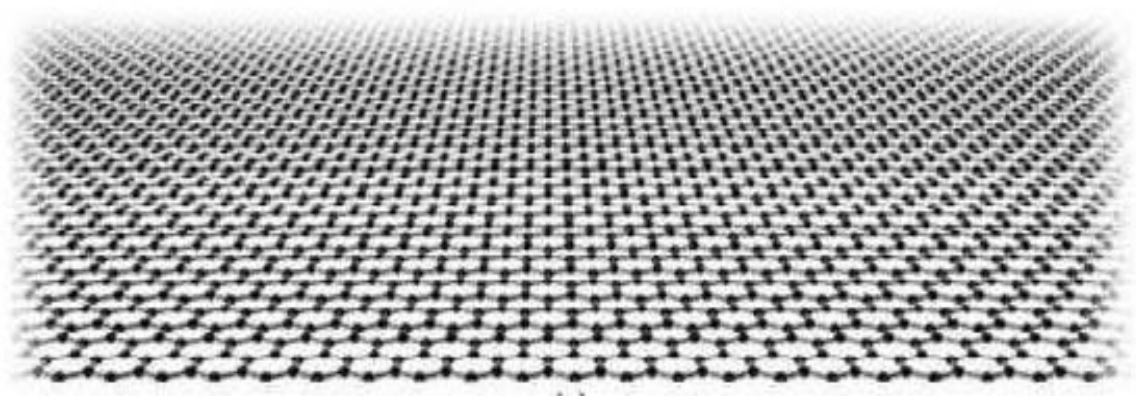

Figure 1.8 a sheet of graphene nano ribbon [4]

Graphene can handle a large magnitude of current densities. The sheet of graphene nano robbon is shown in Figure 1.8.These sheets are the unrolled version of carbon nano tubes. GNR shares most of their properties with carbon nano tubes. The major advantage of GNR over carbon nano tubes is the straight forward fabrication process. The mean free path of GNR is also large when compared with copper. It is a semiconductor with zero band gap energy and share properties with CNT. Good quality graphene has the mean free path of the order of 1 to 5 microns [6].

1.4.1 Classification of GNR Interconnects

GNR's can be classified as armchair (ac) or zigzag (zz) as shown in Figure 1.9.Graphene can be metallic or semiconducting. Zigzag GNR's are always metallic while the armchair GNR can be metallic or semiconducting depending upon the number of hexagonal rings present across the width of GNR. [7] In ac-GNR's if number of rings (N) is 3p-1 or 3p+2 then ac-GNR is metallic and if N= 3p or 3p+1 is satisfied then ac-GNR is semiconducting.

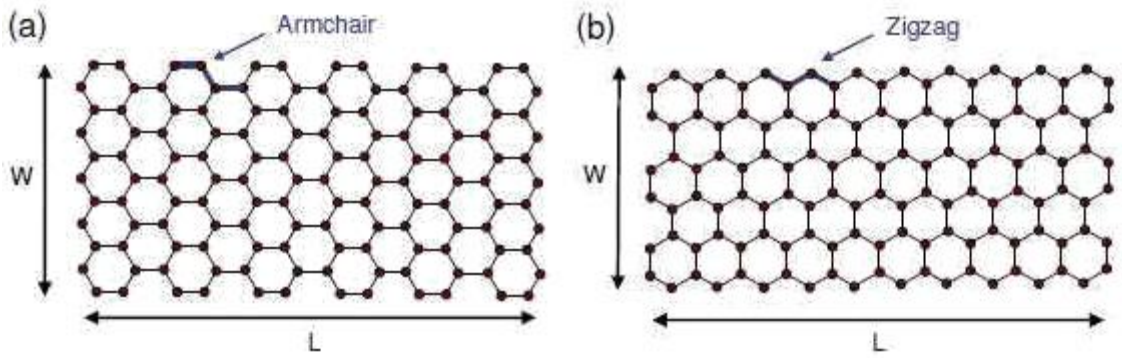

Figure 1.9 Types of GNR a) armchair b) zigzag [6]

Depending upon the number of layers stacked, GNR's can also be classified as single-layer GNR (SLGNR) or multi-layer GNR (MLGNR) as shown in Figure 1.10 and Figure 1.11.Single layer GNR, as the name depicts consists of one layer placed at the distance d from the ground. As such single layer GNR is of no use. The resistance of SLGNR is very high so MLGNR is preferred because of their reduced resistance [8].The resistance of single layer GNR is of the order of kilo ohms. In MLGNR, the interaction between different layers is weak and is governed by van der Waals forces. Therefore, the characteristics of multi-layer graphene are expected to be similar to that of graphene. Figure1.5 shows the un-doped multi-layer GNR. The number of layers depends upon the thickness and the spacing between each layer.

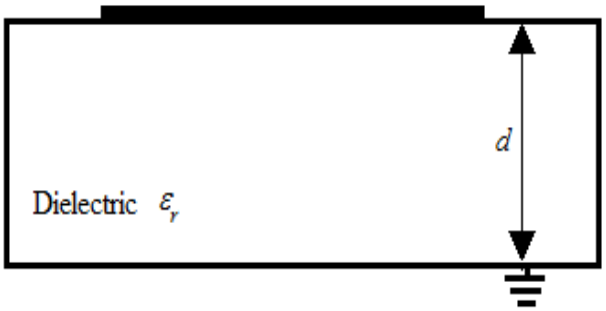

Figure 1.10 Single-layer GNR interconnect [15]

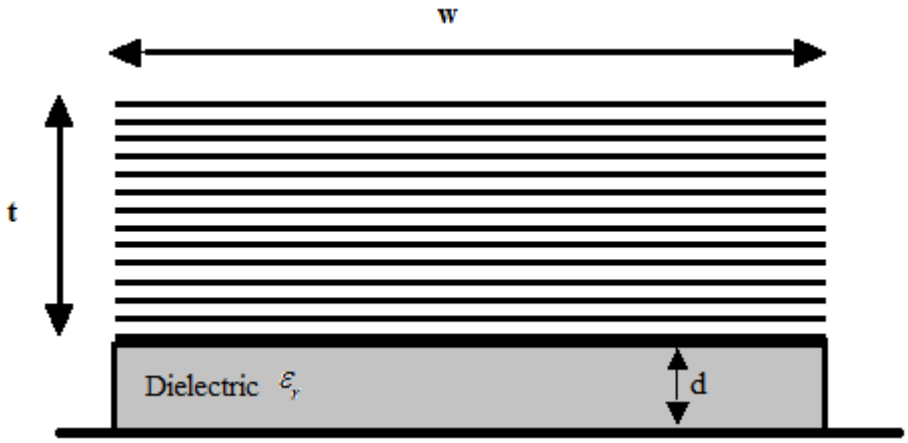

Figure 1.11 Multi-layers GNR interconnects [15]

A MLGNR is placed above the ground by distance d as shown in Figure 1.11. W and t are the width and the thickness. ε_r is the permittivity of the medium between the ground and the bottommost layer of GNR. The total number of layers is dependent on the *t* and interlayer distance (δ). The parameter δ is assumed to be 0.575 nm and 0.34 nm for doped and neutral MLGNR.

1.4.2 Single Layer GNR interconnects

Single layer graphene nano-ribbons are shown in Figure 1.10, placed above the ground by distance d. Single layer GNR are the basic building block of multi-layer GNR interconnects. The resistance of single layer GNR is very high and so it cannot be used without any modification in the design. The equivalent RLC model of SLGNR is very important for understanding various parameters. The equivalent RLC model is shown in Figure 1.6 Consisting of various resistors, capacitors and inductors. The contact which is due to the

imperfect connection between interconnect and the device is ignored in future calculation because there is not so much accurate data available

1.4.3 Equivalent RLC model of Single Layer GNR interconnects

Single layer RLC model is used to derive the ESC model of the MLGNR, so it is very important to understand the various parameters affecting the performance.

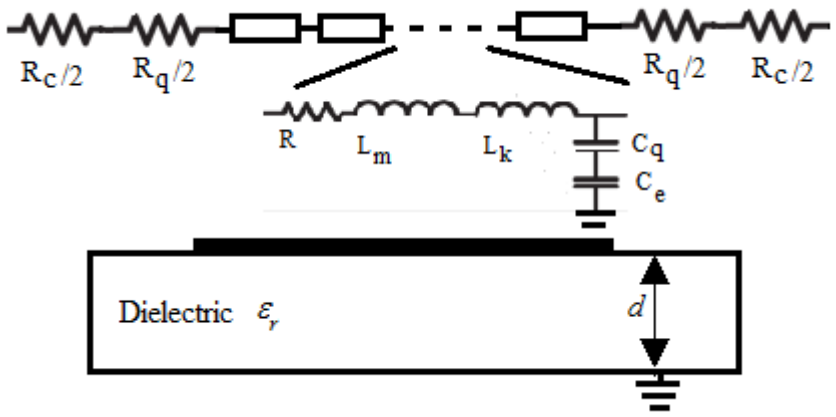

Figure 1.12 Equivalent RLC model of SLGNR interconnects [15].

The R_C is the contact resistance which is due to the imperfect contact between transistors and interconnects. Typical value of contact resistance is 3.2KΩ [9]. R_Q is the quantum resistance and its value is 12.9 KΩ for one channel SLGNR. The quantum capacitance arises due to the quantum energy stored in the carrier. Electrostatic capacitance exists due to the parallel conducting path differentiated by dielectric. The detailed formulae will be discussed in MLGNR where the difference is only between number of channels and number of layers [10]. The SLGNR is of no use because of the higher resistance and inductances involved, so practically we can use MLGNR as Interconnect material.

1.4.4 Multi-Layer GNR interconnects

MLGNR is the stacking of number of layers of SLGNR. Multi-layering of GNR helps to increase the number of conducting paths that can reduce the resistance per unit length of interconnects. In MLGNR, the interaction between different layers is weak and governed by van der wal forces. Also the mean free path and the conductance is reduced by stacking the

number of single layer GNR's. [11] This is due to the inter-sheet electron hoping. So to overcome certain limitations intercalation doping is used.

In intercalation doping, one dopant layer is added between pair of graphene sheets. By using this technique the conductivity of MLGNR is increased drastically. It has been proposed that the conductivity of doped MLGNR is increased up to 30 times when compared with un-doped MLGNR.

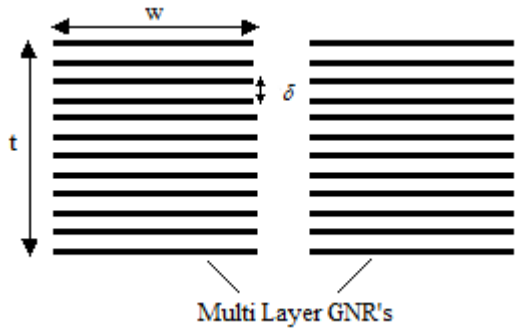

Figure 1.13Un-doped MLGNR interconnects [4]

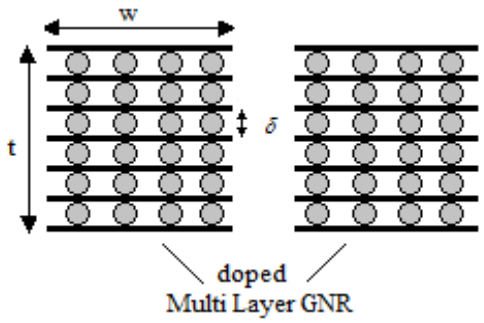

Figure 1.14 Intercalation doped MLGNR interconnects [4]

The structure of un-doped MLGNR interconnect is shown in Figure 1.13.The un-doped MLGNR have thickness t and width w.The spacing between two layers is called inter-layer spacing denoted by δ.Figure 1.14 shows the intercalation doped MLGNR interconnect. In this structure a dopant atom is inserted between two layers of GNR. Due to this insertion of dopant atom, the inter-layer spacing between adjacent atoms is increased. As a result of this increase in spacing, the number of layers in a particular thickness MLGNR decreases. The typical value of δ for un-doped MLGNR is 0.34nm whereas for doped MLGNR it is observed as 0.575nm [4] Intercalation can also increase the mean free path of electron

1.5 Thesis organization

The dissertation is divided into six chapters keeping the performance comparison between copper and MLGNR interconnects in terms of propagation delay and power dissipation at various technology nodes. All aspects of copper and GNR are discussed in detail.

Chapter 1 contains the introduction of various interconnects materials. The detailed theory of GNR and its various structures is explained. The type of material as well as its basic structure and physical properties are discussed.

Chapter 2 contains literature survey related to the topics. In order to understand the thesis , the first step is to study the information available about related topic. Various research papers and letters on the related topic are studied well.

Chapter 3 introduces the research gaps found in the literature survey. According to these research gaps, the objectives of thesis are selected.

Chapter 4 covers the proposed methodology for objectives. It contains the DIL load and various mathematical equations which are used to analyze the performance of GRaphene Nano Ribbons as interconnect material**.** The method to solve the mathematical equation and simulate the MLGNR to obtain propagation delay and power dissipation is studied**.**

Chapter 5 discusses the results based on proposed methodology. The delay and power dissipation of MLGNR at various technology node and interconnect length is studied. The detailed analysis of copper is done and a comparison is performed between MLGNR and copper. Also the comparison between different fermi levels of MLGNR is done in the form of propagation delay and power dissipation.

Chapter 6 contains the conclusion and future scope of MLGNR as a interconnect material. According to obtained results , the applicability of MLGNR in interconnect applications and its potential to replace copper as VLSI interconnect is studied.

CHAPTER 2

LITERATURE REVIEW

Effect of Scaling of Interconnections on the Time Delay of VLSI Circuits [1]

Krishna C. Saraswat and Farrokh Mohammadi

The effect of scaling on time constant RC has been studied. Different mathematical formulae are proposed in terms of feature size and it has been concluded that more work should be done on the conductivity of interconnect because it can effectively reduce the resistance and as a result the time constant of the interconnect RC is also improved. The list of future work to be done is summarized which includes resistivity, high thermal stability and immune to electro migration problem which is major concern in copper interconnect. Materials like poly silicon, aluminum, as a candidate for replacing copper was also compared.

On the Modeling of Resistance in Graphene Nano ribbon (GNR) for Future Interconnect Applications [3]

T. Ragheb and Y. Massoud

In this paper, the MLGNR structure and the effect of stacking layer model is used to perform comparison of MLGNR CNR and copper interconnect. The result obtained clearly shows the replacement of copper and carbon nano tubes interconnects at width less than 15nm. So for high packaging requirements, GNR can replace both copper as well as carbon nano tubes.

Modeling, Analysis, and Design of Graphene Nano-Ribbons Interconnects [5]

C. Xu, H. Li, and K. Banerjee

A study on conductance and RLC model is done in this paper. The conductance model of GNR is obtained using landauer formula. The conductance of GNR is also compared with other interconnect materials i.e. copper, CNT, W (tungsten). The effect of intercalation doping is also taken into account. There are several problems in GNR like these have edge scattering phenomenon which reduces the effective mean free path. The inter-sheet hopping which is due to the layering also reduces the conductivity per layer. It is shown that the in plane conductivity of GNR can be increased by 100 times with the intercalation doping. This

is done by placing of one dopant layer between each adjacent pair of graphene layers. This cause increment in the carrier density which is mainly due to charge transfer and causes further increase in the mean free path due to increased inter layer spacing between different ribbons. The delay ratio of GNR is compared with copper and it is concluded that the intercalation doping and also the specular edges (p> 0.8) are necessary to make MLGNR comparable to copper and CNT.

Carbon Nano material's for Next-Generation Interconnects and Passives: Physics, Status, and Prospects [6]

H.Li, C. Xu, N. Srivastava, and K. Banerjee

In this paper, relative study is analyzed between CNT and GNR. Different models are compared. Single walled carbon nano tubes, double walled carbon nano tubes and multi walled carbon nano tubes are compared with copper. It is found that all of these can outperform copper as VLSI interconnects. For GNR to compete with copper and CNT as a VLSI interconnect intercalation doping is required because the conductivity of un-doped GNR is very much less as compared to doped GNR. The future scope of on chip capacitors and inductors is also discussed here due of reduced skin effect. For the circuits operating at very high frequencies the CNT are the promising candidate because of very high kinetic inductance. CNT based capacitors were mathematically developed and the solved capacitance density is up to three times that of normal silicon dioxide dielectric.

Conductance modeling for graphene nano ribbon (GNR) interconnects [7]

A. Naeemi and J. D. Meindl

The physical model for the conductance model of GNR is obtained taking into account Fermi level, width, chirality and the various type of scattering phenomenon's. Resistance per unit length vs width (in nm) is .Study reveals that below 8nm GNR's offer smaller resistance as compared with copper. Thus metallic GNR's can outperform copper at 8nm or lower level at unity aspect ratio. For wider GNR's (W>100nm) Increasing the Fermi level increases the conductance which is not the case with smaller width. Contact resistance of GNR is not taken into account in this model because of less experimental and theoretical data available.

Compact Physics-Based Circuit Models for Graphene Nano ribbon Interconnects [8]

A. Naeemi and J. Meindl

In this paper the effect of edge roughness which is due to the manufacturing problem is discussed. The resistance comparison is done and the impact of edge roughness on the resistivity of GNR is compared. It has been concluded that there is a need to manufacture small width GNR with smooth edges. Edge roughness has major impact on the resistivity of GNR and thus increases the propagation delay. Therefore better fabrication techniques are required for replacing copper.

Graphene nano-ribbon (GNR) interconnects: A genuine contender or a delusive dream [9]

C. Xu, H. Li, and K. Banerjee

The delay analysis and the conductance of GNR are modeled and the values of resistance, capacitance and inductances are derived. The components of distributed capacitance are similar to CNT i.e. electrostatic inductances and quantum capacitances. Similarly the distributed inductance has magnetic inductance and kinetic inductance. A comparison is made in between GNR and other interconnects material at different technological nodes. Beyond 22nm SWCNT are best while all the GNR's are not better than copper for both global and local interconnects. Also the impact of intercalation doping is studied and is found that by increasing intercalation doping conductivity is increased significantly. The result of this paper is that multilayer metallic GNR have the properties comparable to copper and can replace the same at local interconnects.

Number of Conducting Channels for Armchair and Zig-Zag Graphene Nano ribbon Interconnects [10]

Antonio Maffucci and Giovanni Miano

In this paper the kinetic inductance and the quantum capacitances are expressed in terms of number of conducting channels. The exact variation of number of conducting channels along with the width is studied and it is concluded that the number of conducting channels derived in the theory is much overestimated when compared with the actual results. This is analyzed by taking the exact distribution of the energy spectrum and the velocity of the conduction

electrons. The calculation of number of layers is very important. The numbers of channels of GNR are also very much dependent on the width, Fermi energy and temperature. The exact analysis is important since impedance parameters are very much dependent on these calculations. A simple but very accurate technique is used to calculate the number of layers of graphene as well as conducting channels in GNR. It is also concluded that the number of conducting channels and number of layers has been over estimated in ac GNRs and highly overestimated in zz GNR.

Resistivity of Graphene Nanoribbon Interconnects [11]

Raghunath Murali, Kevin Brenner, Yinxiao Yang, Thomas Beck, and James D. Meindl

This paper represents the first experimental results to replace copper with narrow graphene nano ribbons as VLSI interconnects. Graphene nano ribbons were manufactured and compared with copper in terms of 3-D resistivity. The average GNR resistivity was calculated higher than that of Cu resistivity with the feature size between 18 nm and 52 nm. Resistivity's of individual GNR were calculated from the MLGNR and it was found that the best GNR with appropriate width have the resistivity similar to that of copper interconnect for similar dimensions. The analysis of scattering mechanisms were limited by the edge and grain boundary problems

Comparative Study on Multilayer Graphene Nano ribbon (MLGNR) Interconnects [12]

Wen-Sheng Zhao and Wen-Yan Yin

In this paper, equivalent models for multi-layer GNR is studied and using RLC impedance parameters , propagation delay, power dissipation of interconnect and power delay product are studied. The geometry of multi-layer GNR is shown in Figure 1.6 and the equivalent RLC model is shown in Figure 1.10, where Rc is the contact resistance, R_Q is the quantum resistance and R_s the resistance due to various scattering phenomenon's. A table is prepared comprising different number of layers at different interconnect length. It has been observed that with the increase in length of interconnect delay and power dissipation of the circuit is increased. The lowest propagation delay and highest power dissipation is obtained for higher number of layers in multi later graphene nano ribbons interconnect.

Chemically derived, ultra smooth graphene nano ribbon semiconductors [13]

M. Poljak and K. L. Wang

In this paper, the mobility of graphene nano ribbons is calculated by variations with various types of defect. It has been concluded that the mobility in poor graphene nano ribbons reduced by large extent as the width of graphene is reduced when compared to ideal devices. It is concluded that both the ideal graphene nano ribbons and GNR with various edge defects possesses continuously decreasing electron mobility and there is a drastic change when graphene nano ribbon width is reduced. The electron mobility variation range increases from 100% up to 960% as W is reduced from 4.80 nm to 1.10 nm.

Stability analysis in graphene nanoribbon interconnects. [14]

S. H. Nasiri,Md. K. M. Farshi, and R. Faez

This paper represents the analytical model for calculation of number of channels and number of layers of graphene nano ribbon interconnects. The complex equation of number of channels of MLGNR is solved by iteration and simplified formula is obtained by curve fitting tools. Liquid helium, nitrogen and room temperature were also considered. It has been found that the accuracy of obtained result is with 1% of the exact formula. The number of channels depends on width, Fermi and temperature was calculated. The only variation in the formula with temperature is the value of coefficients. At zero Fermi level, different mathematical equation is developed.

Analytical Time Domain Models of MLGNR Interconnects [15]

Atul K. Nishad and Rohit Sharma

In this paper, analytical time domain model for MLGNR is proposed. The comparison of performance of SC-MLGNR is done with TC-MLGNR. The motivation behind this work is the simple fabrication and reduced complexity as compared to SC-MLGNR in TC-MLGNR. The equivalent model is prepared for comparing TC-MLGNR and SC-MLGNR. In TC-MLGNR there is a metallic contact only with the first layer of graphene while in SC-MLGNR the metallic contact is with all layers. The equivalent resistance of SC-MLGNR is less than TC-MLGNR. The performance of TC-MLGNR can be improved by increasing the interlayer conductance. the interlayer conductance can be increased by increasing the Fermi

level. The Fermi level is further increased by doping process. With sufficient doping ,the conductivity of TC-MLGNR can be made comparable with SC-MLGNR and at reduced with , TC-MLGNR can replace SC-MLGNR , thus reducing the complex fabrication required for SC-MLGNR. Results indicate that TC-MLGNR can replace copper and optical interconnects.

Circuit Modeling of MLGNR Interconnects. [16]

Yuan Fang, Wen-Sheng Zhao and Wen-Yan Yin

In this paper, circuit modeling of single as well as MLGNR is done. The impact of capacitive and inductive coupling is carefully calculated. The delay ratio of copper with MLGNR is calculated. The impact of contact resistance on delay of MLGNR interconnect is studied theoretically and it is concluded that there is a variation of only 3% by including contact resistance. This is very crude approximation considering contact resistance of 200K.

Compact Formulae for Number of Conduction Channels in GNR's [17]

S.H. Nasiri, R. Faez, and Md. K. Moravvej-Farshi

In this letter, a compact formula is derived for calculating the number of channels in different types of graphene nano ribbons. The simplified equation of number of channels is represented in the form of Fermi energy and width of MLGNR interconnects. The data fitting tool is used to calculate the constants at various temperatures. The obtained formula has a high accuracy with a variation of 1%.The number of channels can be obtained at three temperatures 300k, 77k and 4.2k.

Performance Improvement in SC-MLGNRs Interconnects Using Interlayer Dielectric Insertion [18]

Atul Kumar Nishad and Rohit verma

In this paper, the impact of dielectric layer insertion on propagation delay, power dissipation and bandwidth of GNR is studied. The results show that by inserting dielectric layer, the performance of MLGNR is increased. The reduction in both delay and power dissipation is observed along with improvement in bandwidth.

CHAPTER 3

RESEARCH GAPS

The work present in the literature shows that the resistivity of copper increases drastically as the technology scales down below 45nm. This is because when the feature size become close to mean free path of copper (45nm), its performance as VLSI interconnect degrades. So, in deep submicron region there is a need to replace copper interconnects. GNR interconnects have the potential to outperform the copper and replace it for future interconnects applications. The impact of Fermi energy on the delay and power dissipation of MLGNR is not analyzed in the literature. The impact on delay and power dissipation will be considered at different technology nodes and lengths.

3.1 Objectives

1. To propose the equivalent impedance model for GNR which includes the effect of gap of two adjacent layers of GNR.
2. To analyze the effect of Fermi energy on the impedance parameters of graphene nano ribbons for different technology nodes.
3. To study the impact of Fermi energy on propagation delay and power dissipation of MLGNR interconnects.
4. To compare the results obtained from above objective with copper interconnect.

CHAPTER 4

PROPOSED METHODOLOGY

The multi-layer GNR interconnect is modeled into equivalent single conductor model. The RLC components of the associated layer are calculated using mathematical equations. The equations are solved in MATLAB and simulated in T-SPICE.

4.1 Equivalent RLC model of MLGNR interconnects

The layers of GNR are placed at distance d from ground. The permittivity of medium is $\in$ and thickness of GNR layers is t. W is the width of interconnect line and δ is the spacing between different layers. The number of layers is given by equation 4.1.

$$N_{layers} = 1 + \left[\frac{t}{\delta} \right] \tag{4.1}$$

The number of channels per layer (N_{ch}) is given by equation 4.2. This is very important parameter for calculating parasitic components. This equation can be further simplified into equation 4.3. The efficiency of equation 4.3 is very high and at the same time easy to calculate even with calculator.

$$N_{ch} = \sum_{i=1}^{N_c} \left[1 + e^{\frac{(E_i - E_f)}{kT}} \right]^{-1} + \sum_{i=1}^{N_v} \left[1 + e^{\frac{(E_i + E_f)}{kT}} \right]^{-1} \tag{4.2}$$

Now we will analyze the values on the basis of number of contact layers and number of channels. The above equation depends on Fermi energy, ribbon width as well as temperature and is complicated. We can use approximate of above equation obtained by data fitting tools. The modified equation is

$$N_{ch}(W,E_F)=\begin{Bmatrix}(a_0+a_1.W+a_2.W^2+a_3.E_F+a_4.W.E_F+a_5.E_F{}^2)....E_F>0\\(b_0+b_1.W+b_2.W^2)....E_F=0\end{Bmatrix} \quad (4.3)$$

Using the above equation, the number of channels in a layer of GNR can be easily calculated. It is observed that with the increase in width and Fermi level, the number of channels increases.

Table 4.1.Fitting parameters for number of channels at E_F >0 [17]

Parameter	Temperature(300K)			Unit
	Zigzag	Armchair-Metallic	Armchair-semiconducting	
$a_0(X10^{-2})$	124.4	4.148	-49.38	-
$a_1(X10^{-3})$	-16.96	-0.4644	3.207	nm^{-1}
$a_2(X10^{-6})$	75.17	-15.78	5.714	nm^{-2}
a_3	-5.031	-0.3067	0.5501	eV^{-1}
a_4	1.225	1.201	1.194	$(nm\text{-}eV)^{-1}$
a_5	5.122	0.3724	-0.2755	eV^{-2}

Table 4.2.Fitting parameters for number of channels at E_F = 0 [17]

Parameter	Temperature(300K)			Unit
	Zigzag	Armchair-Metallic	Armchair-semiconducting	
b_0	1.94	0.806	-0.322	-
$b_1(X10^{-3})$	0.297	19.86	38.99	nm^{-1}
$b_2(X10^{-5})$	22.9	14.8	2.535	nm^{-2}

Using the above equation, the number of channels in a layer of GNR can be easily calculated. It is observed that with the increase in width and Fermi level, the number of channels increases. The equivalent model of MLGNR is shown in Figure consisting of contact and quantum resistance, quantum and equivalent capacitance, magnetic and kinetic inductance and last is mutual inductance and capacitances. The model used for the analysis of MLGNR is shown in Figure 1.16.R1 consists of contact resistance and quantum resistance. The typical value of contact resistance is in the range of $1k\Omega$ to $20k\Omega$. The impact of contact resistance

on propagation delay and power on MLGNR is very small and can be ignored. The distributed network is used for evaluating the performance of interconnect line driven by CMOS inverter. The parasitic components shown in the Driver interconnect load are per unit length. The load is also replaced by the capacitor with value ranging from 1fF to 10fF.

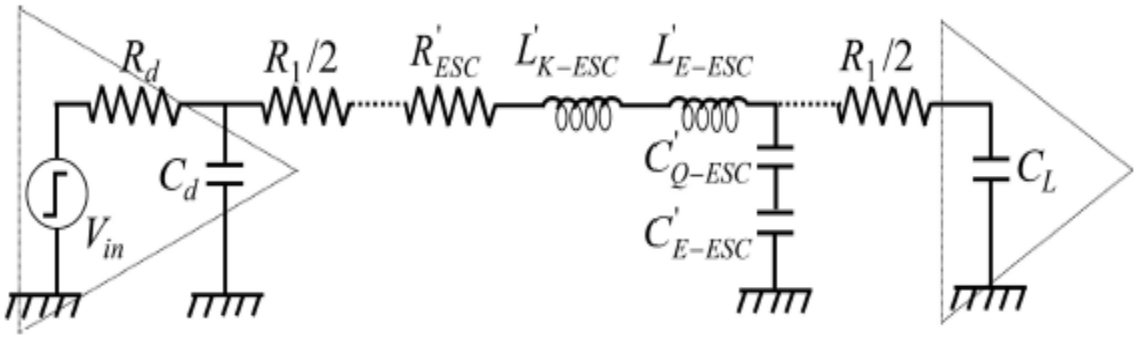

Figure 4.1 DIL load of MLGNR Interconnect [21]

Resistance of MLGNR:

Depending upon the fabrication process the contact resistance of MLGNR involved is in the range of 1-20kΩ.With every conductor there exists a quantum resistance which is due to the confinement of charges carriers. The quantum resistance is given by

$$R_q = \frac{h}{2.e^2.N_{ch}} \tag{4.4}$$

For global interconnects, the resistance is impacted by the scattering defects and edge defects causing increase in resistance commonly known as scattering resistance. Due to the scattering defects and edge defects, the mean free path of MLGNR reduces. The scattering resistance is given by

$$R_s = \frac{h}{2.e^2.N_{ch}.\lambda_{eff}} \tag{4.5}$$

Matthiessen's rule can be used to calculate the effective mean free path of MLGNR. It is given by

$$\frac{1}{\lambda_{eff}} = \frac{1}{\lambda_d} + \frac{1}{\lambda_n} \tag{4.5}$$

Where δ is the mean free path due to edge roughness and it dominates at smaller interconnect lengths. λ_d is the mean free path due to scattering phenomenon's including optical and acoustic phonon scattering. The value of λ_d is taken as 419nm while that of λ_n is ignored because of small impact at global interconnect levels.

Inductance (L) of MLGNR interconnect:

$$L_k = \frac{h}{4.e^2.N_{ch}.v_f.N_{layers}} \tag{4.6}$$

$$L_e = \frac{\mu_0.\mu_r.d}{w} \tag{4.7}$$

There are two type of inductance involved in interconnect modeling, these are kinetic inductance and magnetic inductance. The kinetic inductance represents the kinetic energy of electrons represented by equation 4.6 while the magnetic inductance provides the energy stored in magnetic field. The magnetic inductance is shown in equation 4.7

Capacitance(C) of MLGNR interconnect:

$$C_q = \frac{4.e^2.N_{ch}.N_{layers}}{h.v_f} \tag{4.8}$$

$$C_e = \frac{\in_0 \in_r w}{d} \tag{4.9}$$

There are two types of capacitors involved; these are quantum capacitance and electrostatic capacitance. The equation 4.8 shows quantum capacitance and equation 4.9 shows electrostatic capacitance. The quantum capacitance is due to the density of electronic states whereas the electrostatic capacitance is due to the coupling between different layers of GNR.The equivalent parasitic components are given by

$$R'_{ESC} = \frac{R_q}{N_{layers}} \tag{4.10}$$

$$L'_{ESC} = L_K + L_e \tag{4.11}$$

$$\frac{1}{C'_{ESC}} = \frac{1}{C_q} + \frac{1}{C_e} \tag{4.12}$$

The equivalents RLC as shown in equation 4.10-4.12 are per unit length and varies by varying the length of interconnect. To calculate equivalent parasitic in transmission line model, the values obtained from these equations must be multiplied with the length of interconnect. The magnetic inductance of MLGNR is very small compared with that if kinetic inductance therefore the overall inductance is due to the kinetic inductance. so from equation 4.11 , it is clear that for simplicity we can neglect magnetic inductance.

The equivalent RLC components are calculated by multiplying equations 4.10-4.12 by length of interconnect.

$$R_{ESC} = R'_{ESC}.l \tag{4.13}$$

$$L_{ESC} = L'_{ESC}.l \tag{4.14}$$

$$C_{ESC} = C'_{ESC}.l \tag{4.15}$$

The values obtained by equations 4.13-4.15 are lumped and cannot be used directly. A suitable number of repeaters are used in analysis of graphene ribbons as interconnect. The number of repeaters is varied and optimum numbers of repeaters are obtained by simulations. The RLC components are divided by number of repeaters used. The result of adding number of repeaters is reduced propagation delay at a cost of increased space and power dissipation of the circuit. The obtained results of resistance are in the order of few kilo-ohms whereas the inductance is in nH and capacitance is in pF. The load capacitance can be used in the range of 1fF-10fF. In this dissertation, a load capacitance of 10fF is taken.

CHAPTER 5

RESULTS

To do the performance analysis of MLGNR as a VLSI interconnects; first we need to calculate the delay of copper interconnects. The values of passive components are calculated using predictive technology models and simulations are performed on tanner. The DIL model as shown in Figure 5.1 is used for calculating propagation delay and power dissipation of copper at various technology nodes.

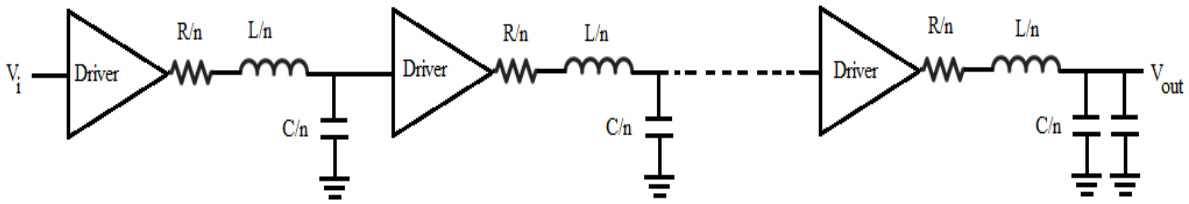

Figure 5.1 Distributed Interconnect model for copper [21]

Table 5.1 ITRS 2013 based simulation parameter for global interconnect [2]

Parameters	**32nm node**	**22nm node**	**16nm node**
Width(nm)	40	28	18
Thickness (nm)	120	84	54
Aspect ratio	3	3	3
Oxide Thickness(nm)	93.6	65.5	40
Power supply (V)	0.9	0.8	0.7
Dielectric constant	2.77	2.59	2.31
Copper resistivity (ρ)	3.66	3.42	5.69

Table 5.2 RLC parameters, delay and power of copper at 16 nm technology node

Length (um)	Resistance (kΩ)	Inductance (nH)	Capacitance (fF)	Propagation delay(ns)	Power Dissipation (uW)
100	3.547	0.17	20.4491	1.14	2.16
200	6.097	0.368	40.89	1.46	2.65
300	8.639	0.576	61.347	1.80	3.152
400	11.186	0.792	81.79	2.18	3.643
500	13.732	1.012	102.25	2.58	4.142
600	16.278	1.236	122.69	3.04	4.64
700	18.825	1.464	143.14	3.52	5.1416
800	21.370	1.695	163.59	4.02	5.64
900	23.917	1.928	184	4.53	6.135
1000	26.463	2.163	204.491	5.12	6.6388

Table 5.3 RLC parameters, delay and power of copper at 22 nm technology node

Length (um)	Resistance (kΩ)	Inductance (nH)	Capacitance (fF)	Propagation delay(ns)	Power Dissipation(uW)
100	1.936	0.159	24.9947	0.376	3.657
200	2.871	0.347	49.98	0.475	4.44
300	3.806	0.545	74.98	0.587	5.24
400	4.742	0.749	100	0.705	6.03
500	5.677	0.959	125	0.833	6.82
600	6.613	1.173	150	0.970	7.608
700	7.548	1.39	175	1.12	8.398
800	8.483	1.61	200	1.27	9.19
900	9.419	1.833	225	1.44	9.98
1000	10.354	2.058	250	1.62	10.789

Table 5.4 RLC parameters, delay and power of copper at 32 nm technology node

Length (um)	Resistance (kΩ)	Inductance (nH)	Capacitance (fF)	Propagation delay(ns)	Power Dissipation(uW)
100	1.458	0.152	26.7318	0.159	6.2
200	1.916	0.332	53.4636	0.209	7.324
300	2.375	0.475	80.1954	0.256	8.418
400	2.833	0.721	106.927	0.310	9.535
500	3.292	0.924	133.659	0.367	1.06
600	3.750	1.13	160.3908	0.423	1.174
700	4.208	1.34	188	0.487	1.284
800	4.666	1.553	214	0.549	1.387
900	5.125	1.769	241	0.617	1.49
1000	5.583	1.986	268	0.690	1.600

Results are also obtained at different technology node. International Technology Roadmap for Semiconductor 2013 is used to calculate RLC parameters as shown in table 5.1. After calculating resistance, capacitance and inductance the values of propagation delay and power dissipation are shown in table 5.2. As the length increases the propagation delay and power dissipation increases. This is because of increase in RLC parameters with the increase in length.

It is observed from the table 5.2-5.4; as the technology node decreases the delay of interconnect at global level increases substantially. This is because of the increase in RLC of copper interconnect and delay is proportional to these parasitic components. The achievement of reducing technology node is reduction in power dissipation of interconnect.

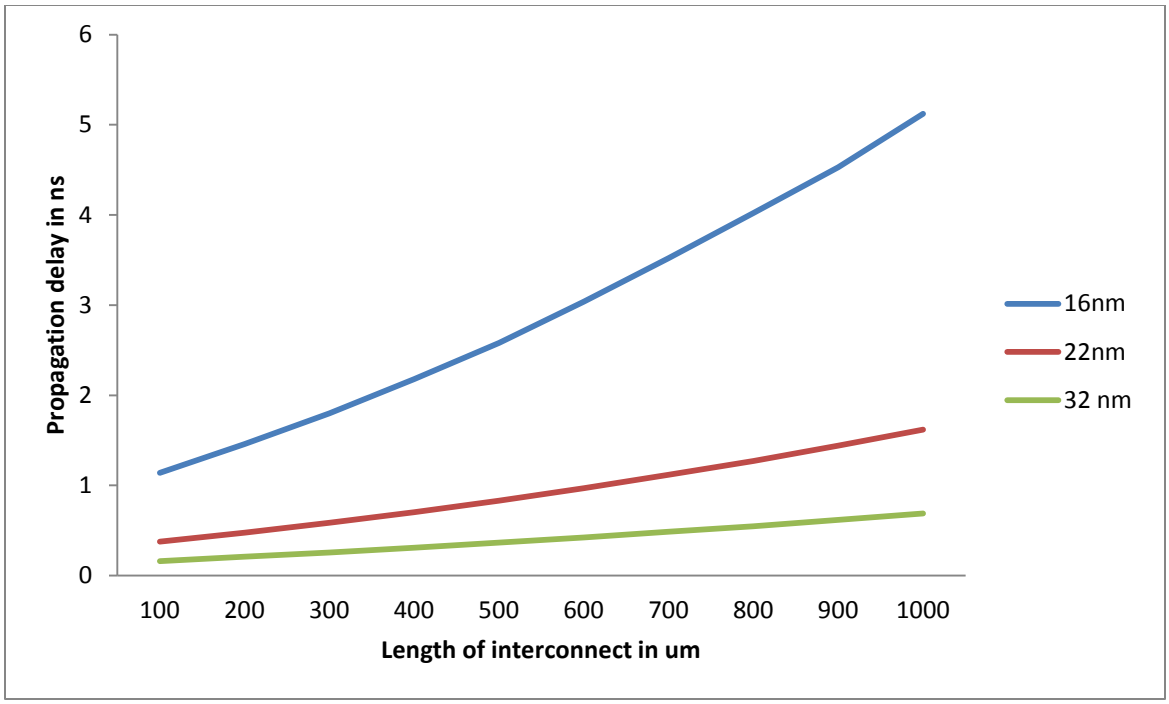

Figure 5.2 Propagation delay of copper interconnect at different technology nodes

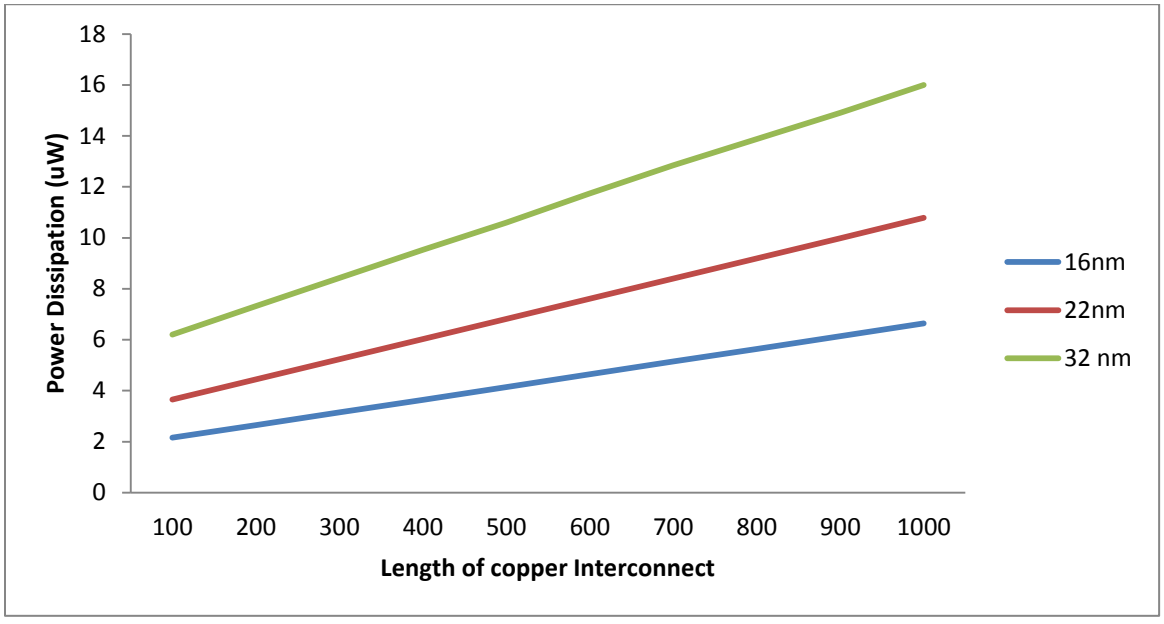

Figure 5.3 Power dissipation of copper interconnect at different technology node

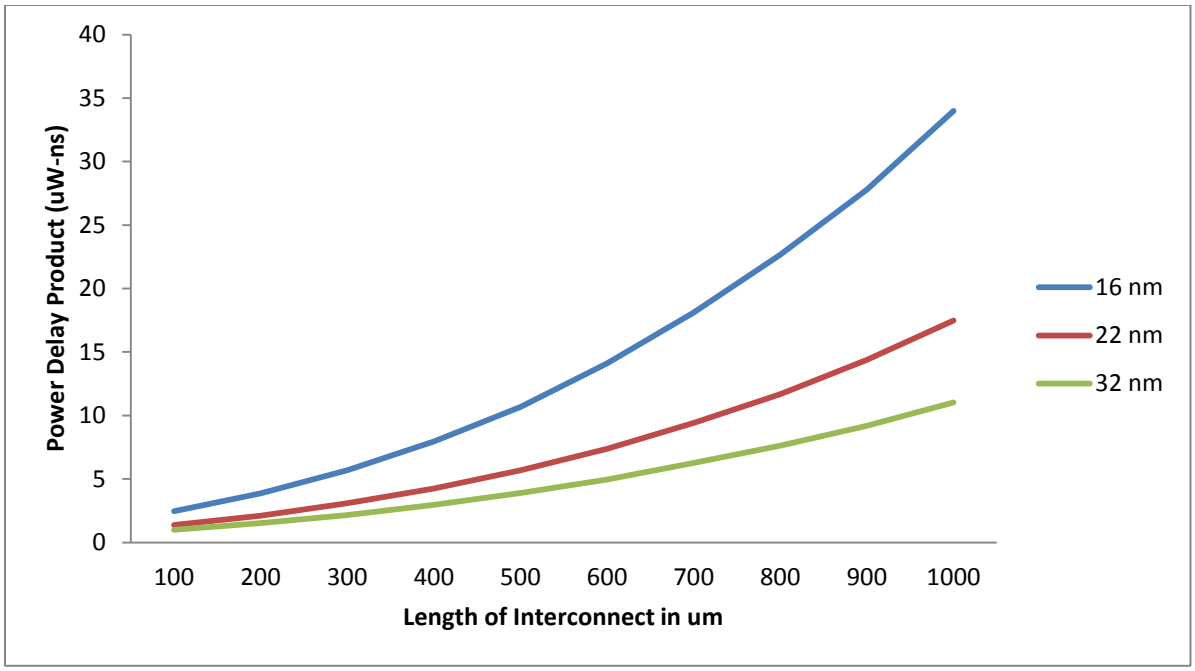

Figure 5.4 PDP of copper at different technology nodes

Table 5.5 PDP of copper wrt to different lengths at different technology nodes

Length of interconnect (um)	**Power delay product at 16 nm (uW-ns)**	**Power delay product at 22 nm (uW-ns)**	**Power delay product at 32 nm (uW-ns)**
100	2.4624	1.375032	0.9858
200	3.869	2.109	1.530716
300	5.6736	3.07588	2.155008
400	7.94174	4.25115	2.95585
500	10.68636	5.68106	3.8902
600	14.1056	7.37976	4.96602
700	18.09843	9.40576	6.25308
800	22.6728	11.6713	7.61463
900	27.79155	14.3712	9.1933
1000	33.99066	17.47818	11.04

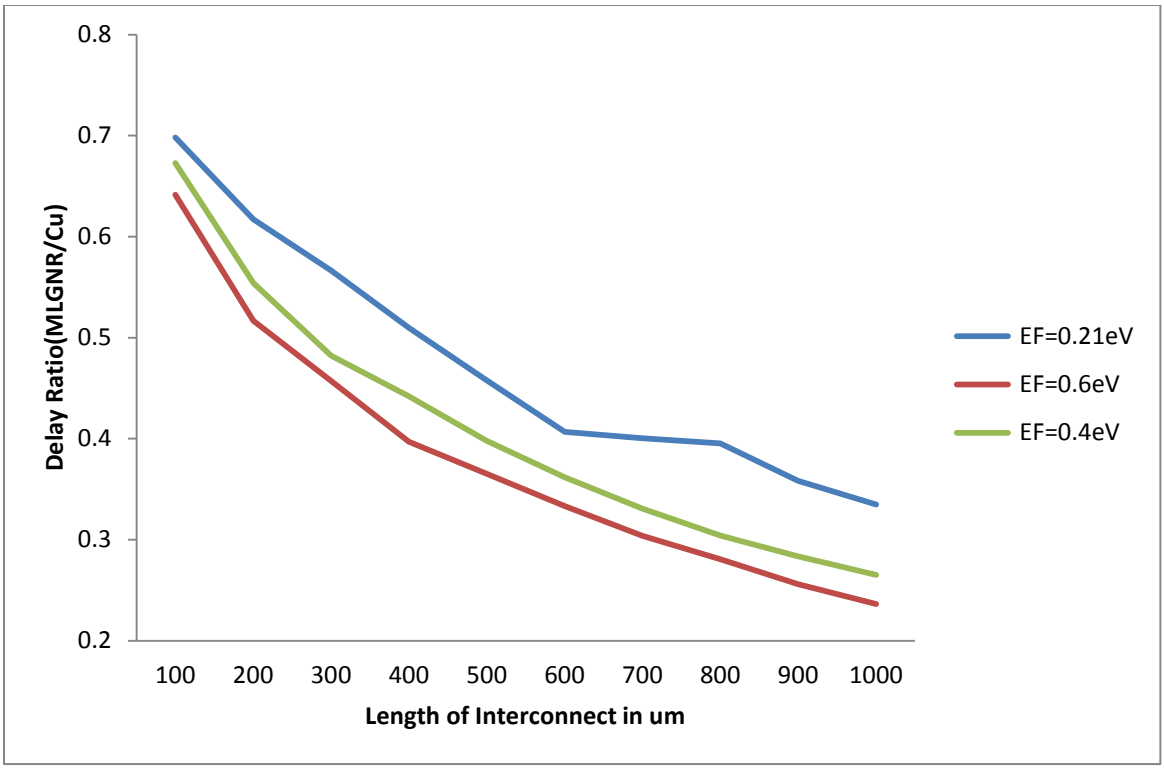

Figure 5.5 Propagation delay ratio of MLGNR/Cu vs. interconnect length at 32nm technology node

Table 5.6 Propagation delay ratio at different interconnect lengths 32nm

Length of Interconnect (um)	**Propagation delay(ns) EF=0.21eV**	**Propagation delay(ns) EF=0.6eV**	**Propagation delay(ns) EF=0.4**
100	0.69811321	0.64150943	0.672955975
200	0.61722488	0.51674641	0.554114833
300	0.56640625	0.45703125	0.481992188
400	0.50967742	0.39677419	0.441935484
500	0.45776567	0.36512262	0.397820163
600	0.40661939	0.33333333	0.361702128
700	0.40041068	0.30390144	0.330595483
800	0.39526412	0.28051002	0.304189435
900	0.35818476	0.2560778	0.28363047
1000	0.33478261	0.23623188	0.265217391

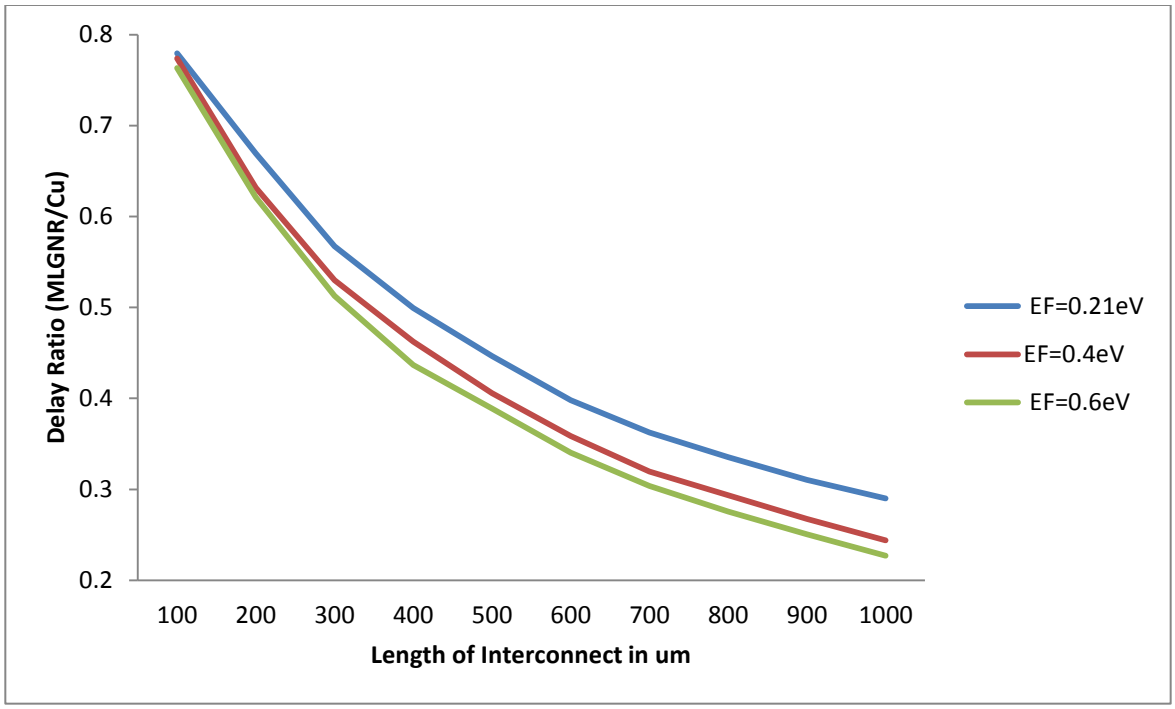

Figure 5.6 Propagation delay ratio of MLGNR/Cu vs interconnect length at 22nm technology

Table 5.7 Propagation delay ratio at different interconnect lengths 22nm

Length of Interconnect (um)	**Propagation delay(ns) EF=0.21eV**	**Propagation delay(ns) EF=0.4eV**	**Propagation delay(ns) EF=0.6**
100	0.77925532	0.77393617	0.763297872
200	0.66947368	0.63157895	0.621052632
300	0.56729131	0.52981261	0.512776831
400	0.49929078	0.46241135	0.436879433
500	0.44657863	0.4057623	0.388955582
600	0.39793814	0.35876289	0.340206186
700	0.3625	0.31964286	0.303571429
800	0.33543307	0.29370079	0.275590551
900	0.31041667	0.26736111	0.250694444
1000	0.29012346	0.24382716	0.227160494

The similar simulations are performed on 22 nm technology node. The comparison of Table 5.3 and 5.4 shows that at 1000um and Fermi level of 0.6eV there is a reduction of 4% on propagation delay ratio.

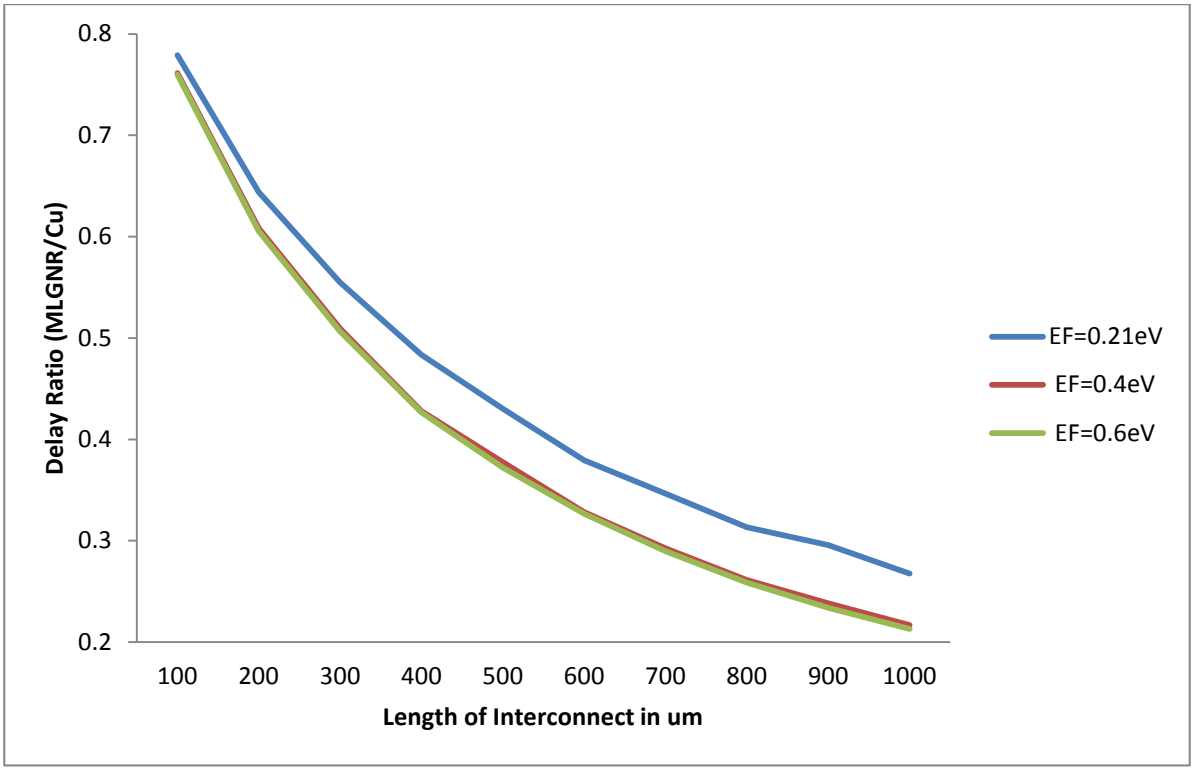

Figure 5.7 Propagation delay ratio of MLGNR/Cu vs interconnect length at 16 nm

With the increase in length of interconnect, the propagation delay ratio reduces. This is due to the fact that the RLC components of GNR are not strongly dependent on length of interconnect as compared with copper. The doping effect causes reduction in parasitic components and increase in mean free path resulting in improved performance of MLGNR at global levels. The effect of varying Fermi level at 16nm technology node reduces as shown in Figure 5.7. This is because of the reason that at l6 nm node and below the impact of Fermi energy on RLC parameters reduces

Table 5.8 Propagation delay ratio at different interconnect lengths 16nm

Length of interconnect (um)	Propagation delay(ns) EF=0.21eV	Propagation delay(ns) EF=0.4eV	Propagation delay(ns) EF=0.6
100	0.77894737	0.76140351	0.759649123
200	0.64383562	0.60821918	0.605479452
300	0.555	0.50944444	0.506666667
400	0.48348624	0.42798165	0.426605505
500	0.43023256	0.37751938	0.372093023
600	0.37927632	0.32828947	0.326644737
700	0.34659091	0.29261364	0.289772727
800	0.31343284	0.26119403	0.258706468
900	0.29580574	0.2384106	0.233995585
1000	0.26757813	0.21679688	0.212890625

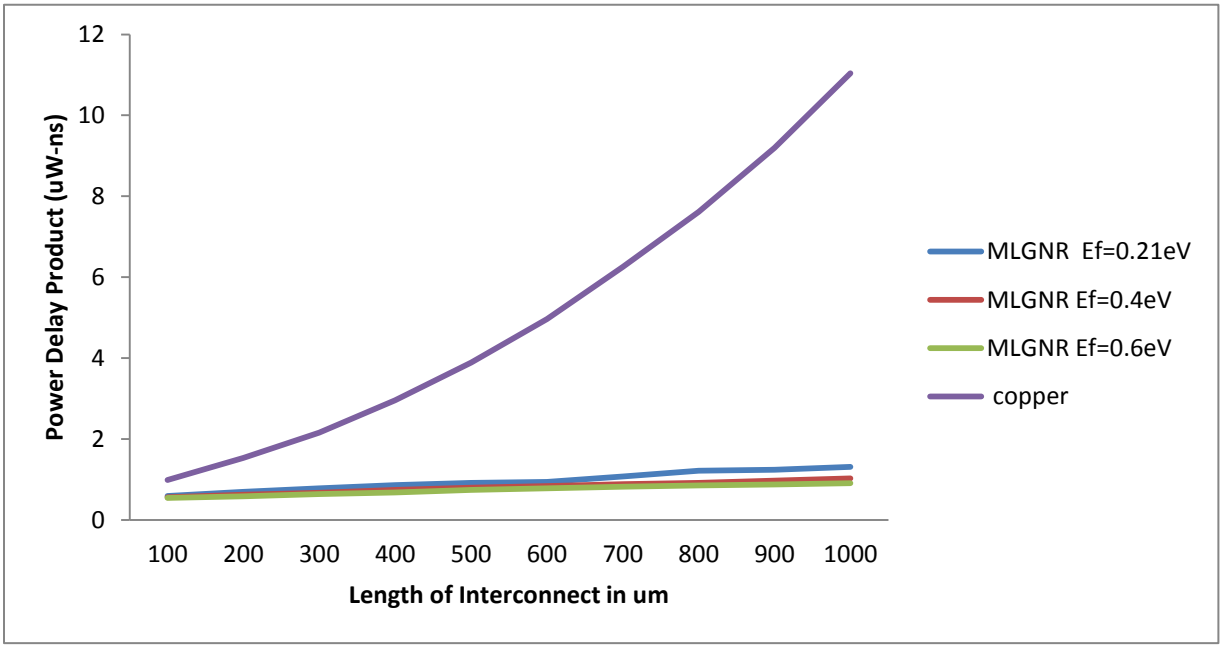

Figure 5.8 Power delay product of MLGNR and copper vs interconnect length at 32nm technology node

Table 5.9 Power delay product of MLGNR and copper vs interconnect length at 32nm technology node

Length of interconnect (um)	PDP of MLGNR at Ef=0.21	PDP of MLGNR at Ef=0.4	PDP of MLGNR at Ef=0.6	PDP of copper
100	0.59163	0.560336	0.5406	0.9858
200	0.693375	0.62271037	0.5778	1.530716
300	0.783	0.6675399	0.634725	2.155008
400	0.85636	0.742677	0.6758	2.95585
500	0.91392	0.794094	0.736464	3.8902
600	0.94084	0.832626	0.777051	4.96602
700	1.070745	0.878577	0.815776	6.25308
800	1.21086	0.914325	0.849002	7.61463
900	1.24202	0.970375	0.875952	9.1933
1000	1.30746	1.027911	0.907421	11.04

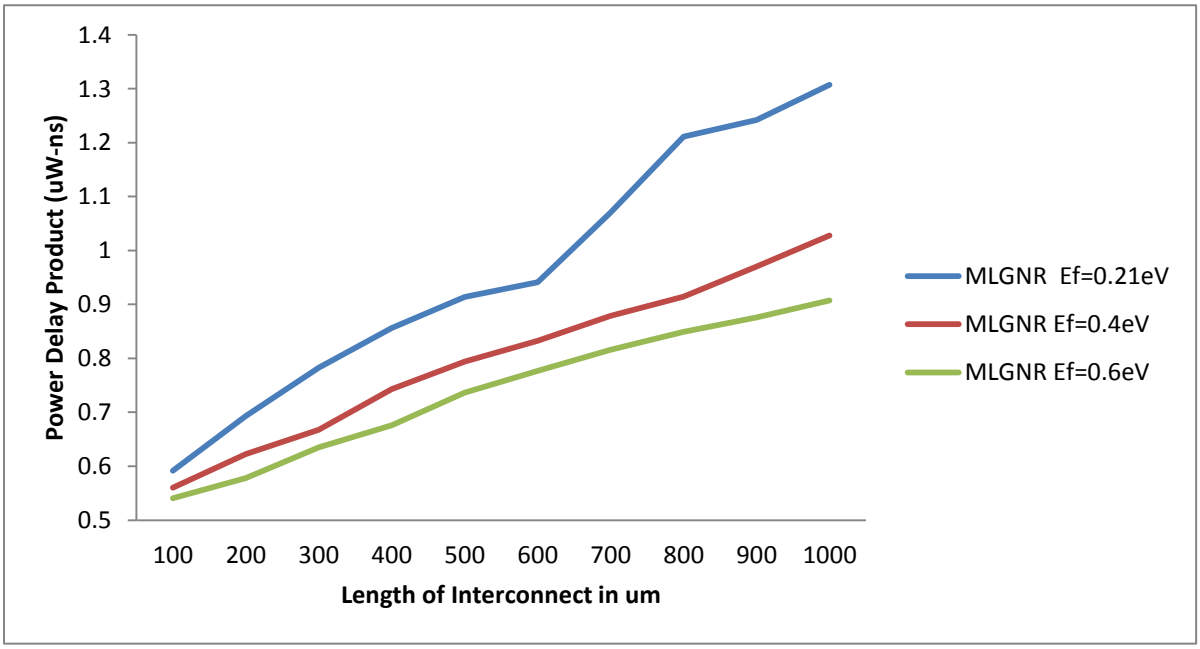

Figure 5.9 Power delay product of MLGNR at different Fermi levels vs interconnect length at 32nm technology node

The power delay product comparison of MLGNR and copper is performed in Figure 5.8. with the increase in length , there is substantial increase in propagation delay of copper. This is due to the quadratic relation of propagation delay with copper. In MLGNR, there is a smaller impact of length on propagation delay of GNR. Due to this, the variation between power delay product of MLGNR and copper is huge as shown in Figure 5.8.The variation of power delay product between different doped MLGNR is shown in Figure 5.9. The obtained results show the reduced PDP at higher Fermi levels. Table 5.10 contains the exact values of PDP at different Fermi levels. The higher percentage change is also observed at higher interconnect lengths.

Table 5.10 Power delay product of MLGNR at different Fermi levels vs. interconnect length at 32nm technology node

Length of interconnect (um)	**PDP of MLGNR at Ef=0.21**	**PDP of MLGNR at Ef=0.4**	**PDP of MLGNR at Ef=0.6**
100	0.59163	0.560336	0.5406
200	0.693375	0.62271037	0.5778
300	0.783	0.6675399	0.634725
400	0.85636	0.742677	0.6758
500	0.91392	0.794094	0.736464
600	0.94084	0.832626	0.777051
700	1.070745	0.878577	0.815776
800	1.21086	0.914325	0.849002
900	1.24202	0.970375	0.875952
1000	1.30746	1.027911	0.907421

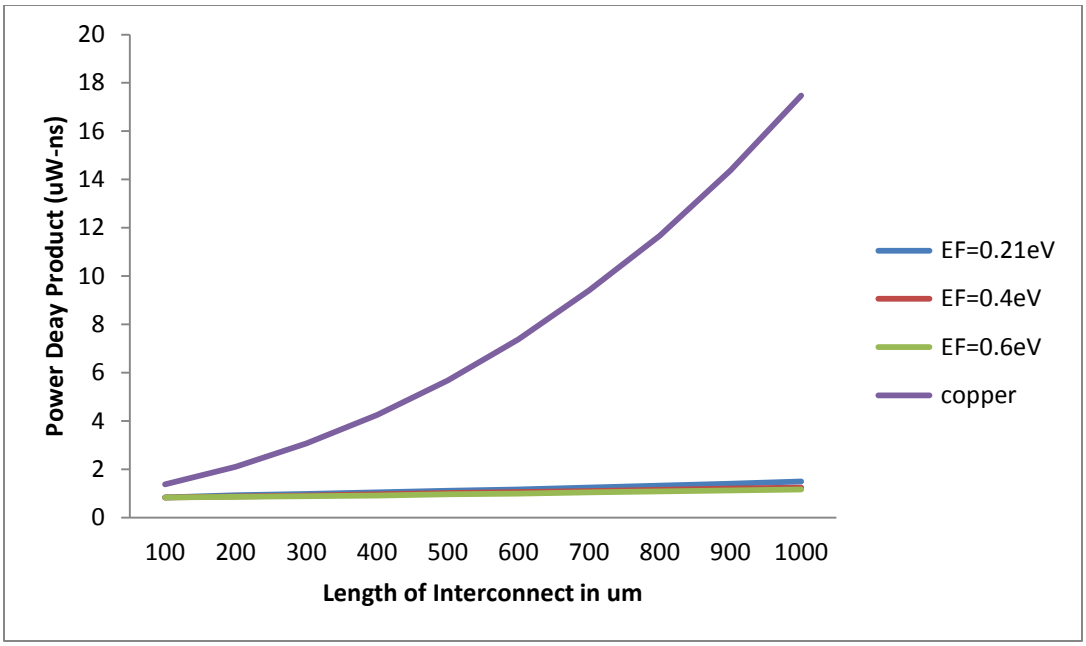

Figure 5.10 Power delay product of MLGNR and copper vs interconnect length at 22nm

Table 5.11 Power delay product of MLGNR and copper vs interconnect length at 22nm technology node

Length of interconnect (um)	**power delay product EF=0.21eV**	**power delay product EF=0.4eV**	**power delay product EF=0.6**	**power delay product copper**
100	0.84091	0.839826	0.82943	1.375032
200	0.92856	0.8763	0.86081	2.109
300	0.98568	0.914651	0.890358	3.07588
400	1.04896	0.974088	0.91784	4.25115
500	1.116	1.020422	0.972	5.68106
600	1.170738	1.0588596	0.9999	7.37976
700	1.247638	1.098702	1.0438	9.40576
800	1.32699	1.158538	1.08955	11.6713
900	1.402239	1.203895	1.129569	14.3712
1000	1.49742	1.24978	1.162512	17.47818

With the increase in Fermi energy, the propagation delay of MLGNR reduces because of reduction in RLC parameters. The impact observed on power is very small and is almost similar, so the power delay product increases almost similarly as compared with propagation delay as shown in Figure 5.9

The power delay product comparison of MLGNR and copper at 22nm is performed in Figure 5.10. With the increase in length, there is substantial increase in propagation delay of copper. This is due to the quadratic relation of propagation delay with copper. In MLGNR, there is a smaller impact of length on propagation delay of GNR. Due to this, the variation between power delay product of MLGNR and copper is huge as shown in Figure 5.10.

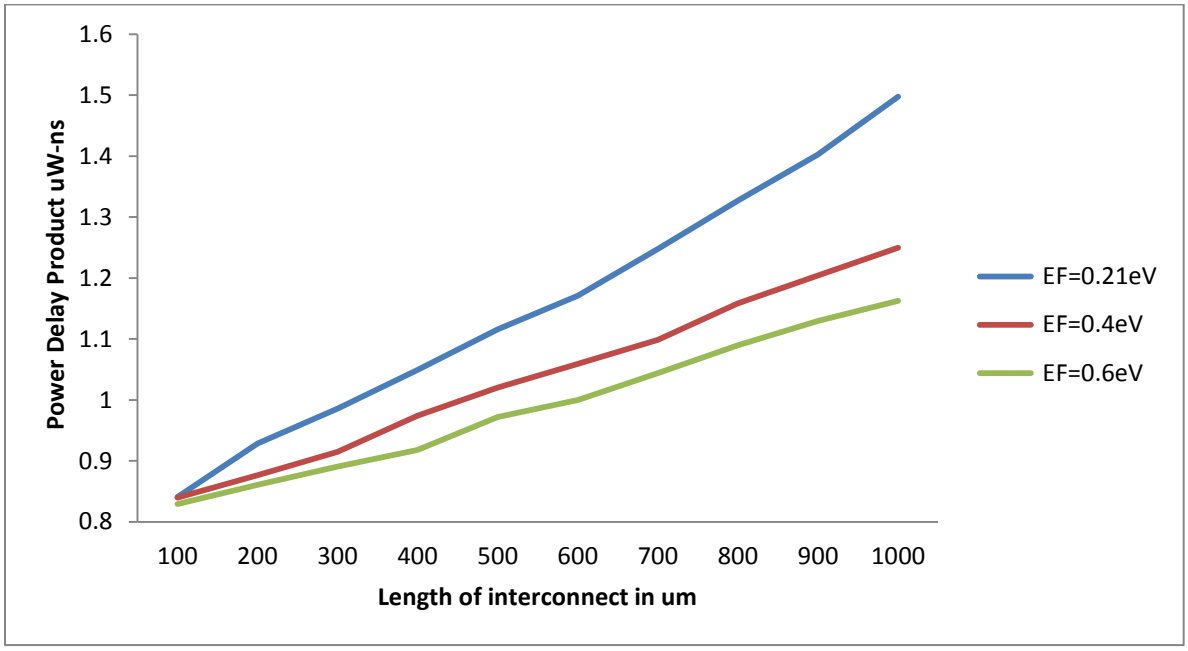

Figure 5.11 Power delay product of MLGNR at different Fermi levels vs interconnect length at 22nm technology node

Table 5.12 Power delay product of MLGNR at different Fermi levels vs interconnect length at 22nm technology node

Length of interconnect (um)	**power delay product EF=0.21eV**	**power delay product EF=0.4eV**	**power delay product EF=0.6**
100	0.84091	0.839826	0.82943
200	0.92856	0.8763	0.86081
300	0.98568	0.914651	0.890358
400	1.04896	0.974088	0.91784
500	1.116	1.020422	0.972
600	1.170738	1.0588596	0.9999
700	1.247638	1.098702	1.0438
800	1.32699	1.158538	1.08955
900	1.402239	1.203895	1.129569
1000	1.49742	1.24978	1.162512

With the increase in Fermi energy, the propagation delay of MLGNR reduces because of reduction in RLC parameters. The impact observed on power is very small and is almost similar, so the power delay product increases almost similarly as compared with propagation delay as shown in Figure 5.11. When compared with higher technology node, the power delay product is high with the deciding parameter as propagation delay. Table 5.12 shows the PDP of MLGNR at 22nm node. As the length of interconnect increases the percentage difference between different Fermi levels also increases. The PDP variation between different doped MLGNR and copper is very high as shown in Figure 5.12.The doped multi-layer GNR shows much better PDP at higher interconnect lengths when compared with copper. The results follows almost linear trend in MLGNR whereas in copper interconnects, there is quadratic increase in power delay product.

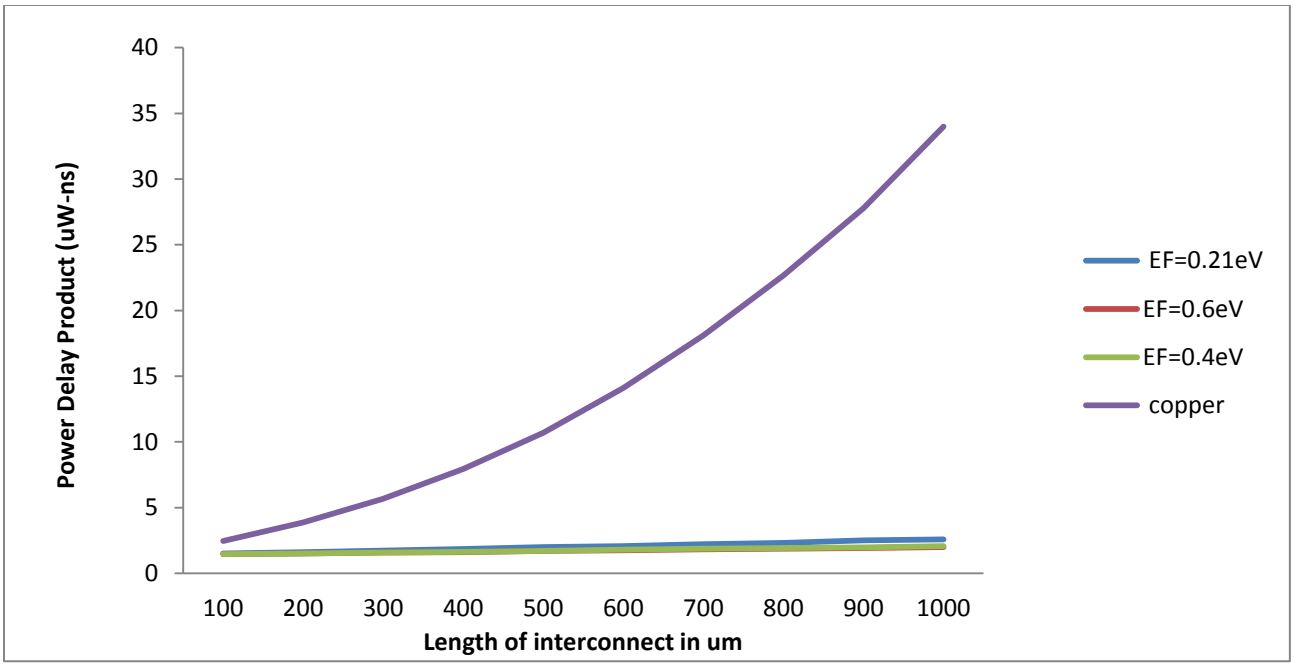

Figure 5.12 Power delay product of MLGNR and copper vs interconnect length at 16nm technology node

Table 5.13 Power delay product of MLGNR and copper vs interconnect length at 16nm technology node

Length of interconnect in um	**power delay product EF=0.21eV**	**power delay product EF=0.6eV**	**power delay product EF=0.4eV**	**power Delay product copper**
100	1.50072	1.461712	1.466138	2.4624
200	1.61116	1.50516	1.515176	3.869
300	1.72827	1.569904	1.5817728	5.6736
400	1.846608	1.610358	1.6368	7.94174
500	1.99467	1.691838	1.71168	10.68636
600	2.074247	1.747498	1.7921664	14.1056
700	2.22162	1.81795	1.86201	18.098432
800	2.3184	1.86165	1.91984	22.6728
900	2.49776	1.92888	1.9769	27.79155
1000	2.58245	2.00133	2.06446	33.990656

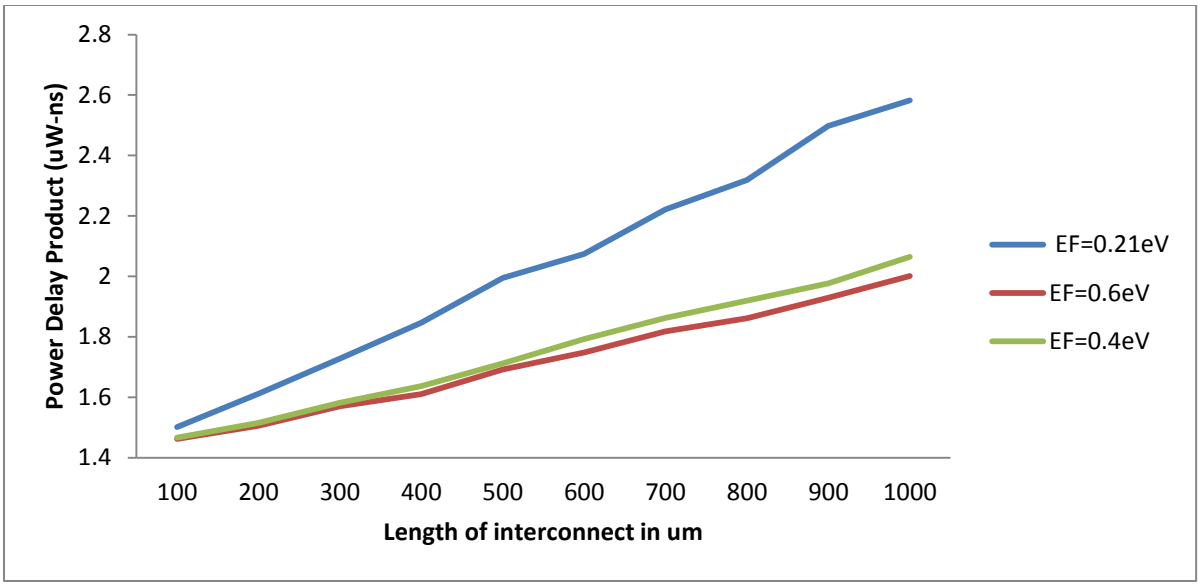

Figure 5.13 PDP of MLGNR at different Fermi levels vs interconnect length at 16nm technology node

The highest variation in power delay product between MLGNR and copper is observed at 16nm technology node. This is due to the higher power dissipation and propagation delay difference.

Table 5.14 PDP of MLGNR at different Fermi levels vs. interconnect length at 16nm technology node

Length (um)	**PDP EF=0.21eV**	**PDP EF=0.6eV**	**PDP EF=0.4eV**
100	1.50072	1.461712	1.466138
200	1.61116	1.50516	1.515176
300	1.72827	1.569904	1.5817728
400	1.846608	1.610358	1.6368
500	1.99467	1.691838	1.71168
600	2.074247	1.747498	1.7921664
700	2.22162	1.81795	1.86201
800	2.3184	1.86165	1.91984
900	2.49776	1.92888	1.9769
1000	2.58245	2.00133	2.06446

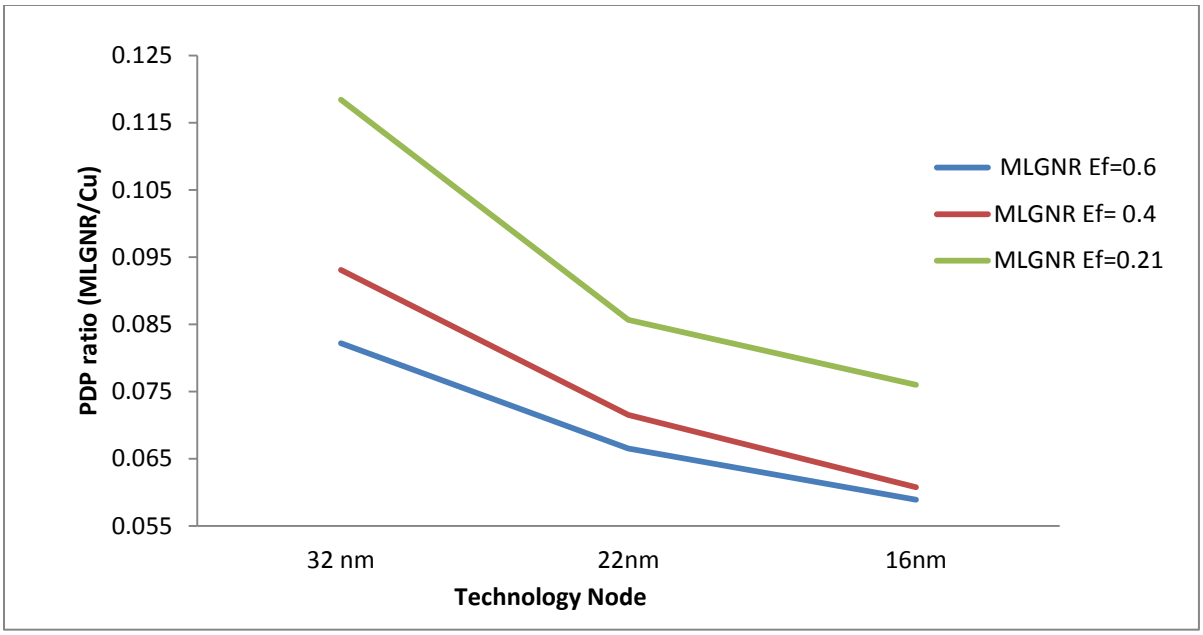

Figure 5.14 Power Delay product ratio (MLGNR/Cu) at different technology nodes

	32 nm	**22nm**	**16nm**
MLGNR Ef=0.6	0.082193931	0.066512188	0.058878828
MLGNR Ef= 0.4	0.09310788	0.071505157	0.060736103
MLGNR Ef=0.21	0.118429348	0.08567368	0.075975292

Table 5.15 Power Delay product ratio (MLGNR/Cu) at different technology nodes

With the reduction in technology node, the difference between power delay product of MLGNR and copper increases. This is due to the fact that with decrease in technology node the impact on power and delay in copper is very high. The impact on MLGNR is not observed at the same rate. Since in copper square law dependence is observed with RLC parameters, the power delay product of copper is higher at smaller technology nodes. Due to this reason, there is reduction in power delay product ratio of MLGNR/Cu. Figure 5.14 shows the trend of power delay product at different technology node and different fermi levels. The values are calculated at 1000um interconnect length.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

In this dissertation, a DIL load is used to analyze the performance of MLGNR interconnect at different Fermi levels. The impedance parameters are calculated using mathematical equations to compute the interconnect performance metrics. The delay and power dissipation of MLGNR by varying doping is calculated. It is observed that the increase in Fermi energy reduces the propagation delay as well as power dissipation of MLGNR interconnects. By inserting dopant atoms higher mean free path can be obtained.

Increasing the Fermi energy of the MLGNR interconnect improves the interconnect performance. The effect of doping and variation in Fermi energy is studied. The impedance parameters at different technology node 16nm, 22nm, 32nm for GNR are calculated with the help of MATLAB. The obtained impedance parameters are then used to calculate the delay and power dissipation at various technology nodes. Both copper and MLGNR calculations are performed and compared with each other. The result shows that the MLGNR interconnect with suitable doping exhibits improved delay and power dissipation. It has been observed that the MLGNR interconnect can replace copper at higher interconnect lengths.

The impact of variation in technology node is also analyzed. The simulations are performed at 32nm , 22nm ,16 nm and ITRS 2013 simulation parameters are used. With the reduction in technology the variation in performance of MLGNR is observed. The result shows that with the increase in length of interconnect the performance of doped MLGNR improves and exhibits the potential to replace copper as a VLSI interconnect.

The effect of edge roughness on propagation delay and power dissipation is ignored in the analysis. At intermediate and higher GNR width, the combined effect of Fermi energy and edge roughness has to be done. More effective MLGNR fabrication techniques needed to be developed so that edge defect issues can be eliminated.

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