Thesis

On

"Low Power & Process Variation Resistant SRAM Design Using Process Tracking & VTCMOS"

Submitted towards the partial fulfillment of requirement for the award of degree of

Master of Technology

In

VLSI Design

Submitted by:

Tanuj Sharma

Roll No: 601461030

Under the guidance of:

Mr. Arun Kumar Chatterjee

Assistant Professor

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

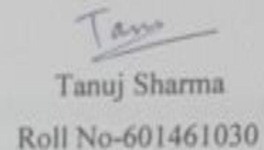
THAPAR UNIVERSITY

(Established under the section 3 of UGC Act, 1956)

PATIALA – 147004 (PUNJAB)

DECLARATION

I hereby declare that the dissertation titled **"Low Power & Process Variation Resistant SRAM Design Using Process Tracking & VTCMOS"** in the partial fulfillment of the requirement for the award of degree of Master of Technology in VLSI DESIGN submitted in Electronics and Communication Engineering Department of Thapar University, Patiala is an authentic record of my study carried out as under the guidance of **Mr. Arun Kumar Chatterjee** (Assistant Professor, ECED) during 2014-2016.



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Roll No-601461030

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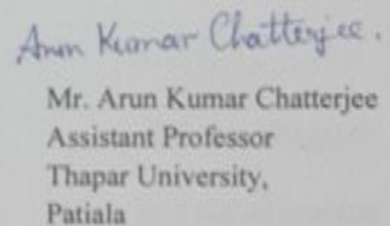
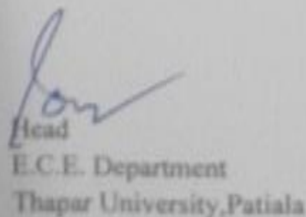


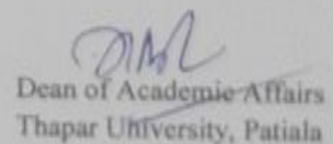
Date: 15/07/2016

Mr. Arun Kumar Chatterjee
Assistant Professor
Thapar University,
Patiala

Counter signed by:



Head
E.C.E. Department
Thapar University,Patiala



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Thapar University, Patiala

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TANUJ SHARMA

Roll No. 601461030

ABSTRACT

In the light of exponentially increasing number of microprocessor based devices like smartphones, tablets, laptops and Internet of Things (IoT) devices, reducing power consumption of portable device is major area of interest. Static Random Access Memory (SRAM) is an integral part of a System On Chip(SOC) and consumes a significant area on the die. Thus reducing power consumption is an indispensable part of SRAM design for portable devices. Another concern for SRAM design is increased process variability in deep sub-micron technology. Process variations not only make SRAM functionally fail in form of read/write errors but also leads to increased power dissipation in faster process corners.

This thesis presents the concept of dynamically identifying the operating process condition of the integrated circuit and implement the corrective measures by using Variable Threshold Complementary Metal Oxide Semiconductor (VTCMOS) scheme to 6-Transistor SRAM (6TSRAM) cell. A ring oscillator is used as process sensor that operates at a frequency which is characteristic of a particular process corner. A digital circuit called process decoder has been designed which reads the operating process corner from the process sensor. It identifies the process corner of the SRAM cell and generates a control signal which is fed to the voltage control block. The voltage control block provides the body bias voltage for the NMOS transistors of the SRAM cell. This setup results in reduced power dissipation and enhanced resistance to process variations.

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LIST OF ACRONYMS

CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical-mechanical polishing
DIBL	Drain-Induced Barrier Lowering
DRAM	Dynamic Random Access Memory
EUV	Extreme Ultra Violet
LER	Line Edge Roughness
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NBTI	Negative Bias Temperature Instability
NMOS	N-channel Metal Oxide Semiconductor
OPC	Optimal Proximity Correct
PCB	Printed Circuit Board
PMOS	P-channel Metal Oxide Semiconductor
RDF	Random Dopant Fluctuation
SOC	System on chip
SRAF	Sub-Resolution Assist Features
SRAM	Static Random Access Memory
VLSI	Very Large Scale Integration

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CHAPTER 1

INTRODUCTION

SRAM (Static Random Access Memory) is a volatile memory that uses two back to back inverters to store data. SRAM is implemented at transistor level where 6T SRAM (SRAM using 6 transistors) is the most widely used SRAM basic cell. SRAM is widely used in microprocessors as cache memory which serves as a faster alternative to main data memory for the program being executed. SRAM is generally fabricated using the standard CMOS (Complementary Metal Oxide Semiconductor) process. This allows SRAM to be directly integrated on the same die on which logic circuit resides unlike DRAM(Dynamic Random Access Memory) which requires a special fabrication process and is generally integrated at package or PCB(Printed Circuit Board) level. However SRAM requires significantly more area as compared to DRAM which can be created by using a single transistor and a capacitor. Area requirements of SRAM depends on the fabrication node and SRAM size. With continued process scaling, SRAM is now being on smaller process nodes then before but have also grown in area thanks to high performance computation requirements. Also scaling brings its own adverse effects which makes SRAM design challenging to achieve enhanced speed, power, area and reliability .

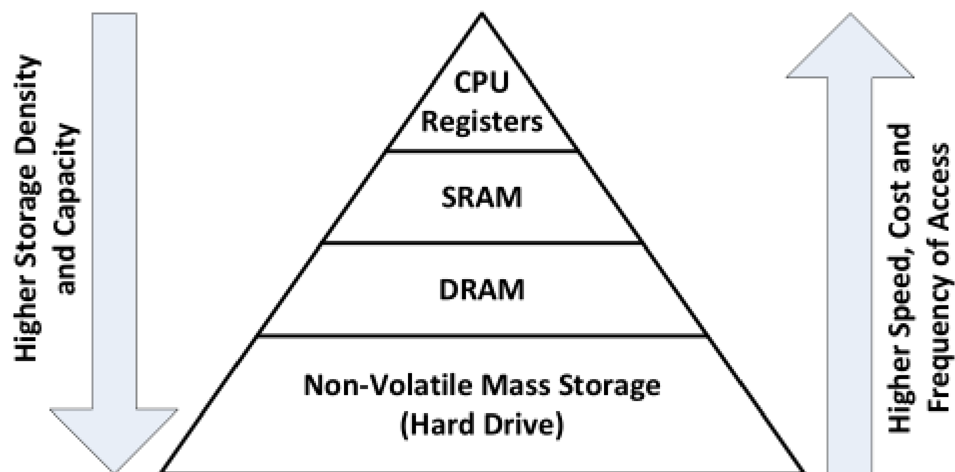

Figure 1.1 Typical processor memory hierarchy

SRAM is a standard requirement in the typical hierarchy of Computer system organization where it sits between the CPU registers and main memory(DRAM) as a compromise compared to CPU register in terms of speed but much frugal in terms of area. DRAM on the other hand provides main chunk of the usable data memory that measure up in gigabytes where as SRAM is typically in megabytes. But because of nature of DRAM and off chip location, it cannot compare in terms of latency and speed.

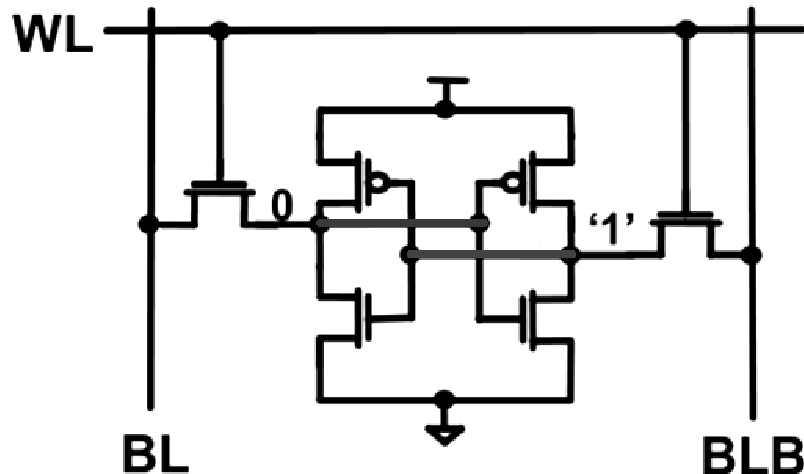

Figure 1.2 6TSRAM Cell

SRAM is static because once it is programmed to store a '1' or '0', it effectively holds its state without the use of any refreshing procedure like in case of DRAM. Use of two back to back CMOS inverters ensure that data stored at both the storage nodes is retained by virtue of positive feedback of CMOS inverter. These cross coupled inverters are further mated with two access transistors that allow data to be read or written at these nodes. These access transistors are controlled by a control signal, Wordline (WL) that is asserted whenever a read/write operation is to be performed. Data to be written or read is routed through Bitline (BL) and its complementary version (BLB).For a write operation, bitline is loaded with a V_{dd}('1') or Gnd ('0') and Complementary bitline with its inverse. Once the Wordline is turned on, storage nodes of the SRAM are forced by the bitlines to change to required state by charging or discharging via the access transistors. For a read operation, each of the bitlines are precharged to V_{dd}. Once the Wordline is turned on, one

of the bitlines connected to the storage node storing a ‘0’ is discharged to some extent. This fall in voltage as compared to the other bitline is sensed by a differential amplifier(often called sense amplifier) and is conveyed as hard ‘1’ or ‘0’.

1.1 SRAM Array Architecture

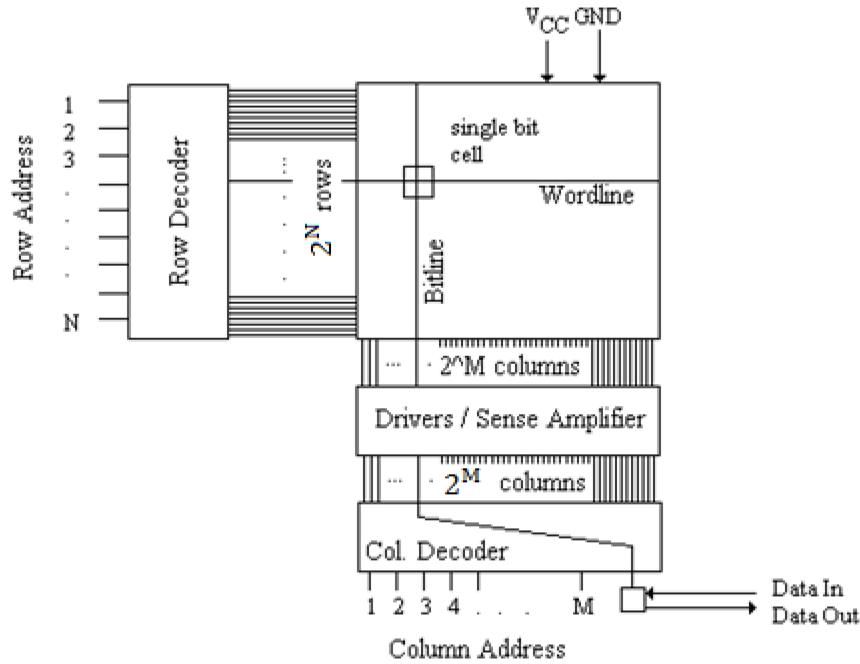

Figure 1.3 SRAM architecture

A typical SRAM is arranged into a array as shown in figure 1.3. Array comprises of 1 bit SRAM cells arranged into a two dimensional array. To access a particular cell in array, we need both the address of the row and column of the cell. Once row and column addresses are fed to the respective decoders, the corresponding address line is asserted while rest of the lines are low. A N x M SRAM array has 2^N horizontal wordlines and 2^M column vertical bitline pairs. A single high wordline activates the entire row and read/write operation can be performed on any one the columns in this row. The column decoder is responsible for choosing the required column. In case of read operation, read may be performed on the entire row and route the required bit to “Data Out” by using the column address. Sense amplifiers are used to convert drop in voltage in bitlines to hard

coded bit. For write operation, driver only activates the required bitline and loads the "Data In" to the bitline (and its complementary to bitline bar). The array is generally organized to operate at a word at a time, so a 8K x 1byte SRAM will operate at 1byte (8 bits) at a time.

1.2 6TSRAM Cell Sizing

For proper operation of 6TSRAM cell, it is necessary to properly choose the size of the transistors used in 6TSRAM cell. We examine the sizing required in both read and write operation of 6TSRAM cell.

Read operation

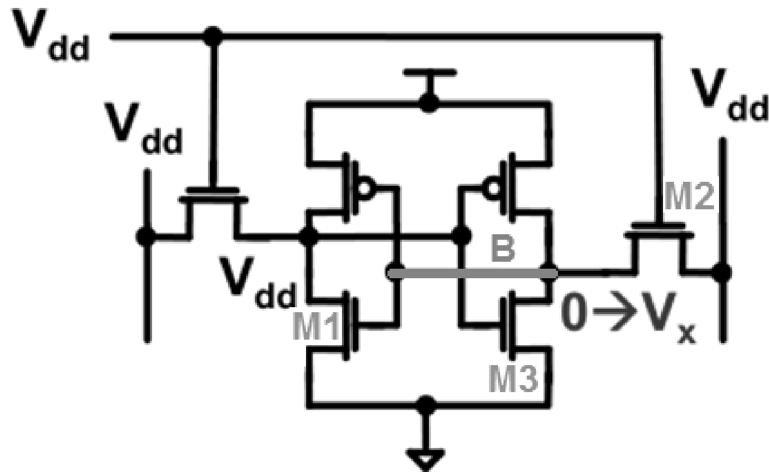

Figure 1.4 SRAM in read configuration

During read operation, let us say node B is at 0V.When wordline is asserted after charging the bitlines to V_{dd}, a path is created between the bitline (right), M2,M3 and ground. This is a voltage divider configuration where the voltage at node B (V_x) is a function of resistance of M2 & M3. For non-destructive read, we need the V_x to be lower as compared to the threshold voltage, else it will turn on M1, which will lead to flipping of the state of the cell. So to achieve a low V_x, we need the M3's resistance to be low as compared to M2's. So, M3's width should be higher than M2's that is Access transistor should be weaker than pull down transistor considering read after both state '1' & '0'.

Write operation

During write operation, bitlines are charged differentially. In the figure above, the cell currently stores ‘0’(V_A is at ground & V_B is at V_{dd}). For writing a ‘1’ to the cell, BL & BLB is charged to ‘1’ and ‘0’ respectively and wordline is asserted . Now there are

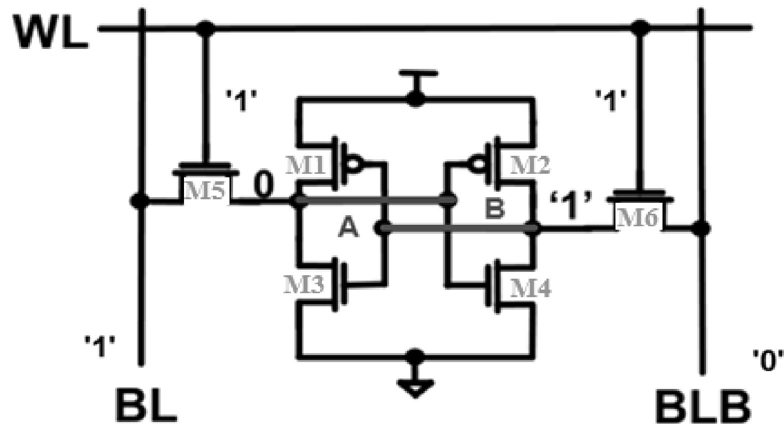

Figure 1.5 SRAM in write configuration

two paths possible in the cell. One is through BL, M5, M3 and ground and another one is through V_{dd}, M2,M6 and BLB. Examining the second path, since we need the cell to flip, it is desirable to have a V_B less than V_t to turn off M3 and trigger cell state change. So, we need M2’s resistance to be higher than M6, or M6 should be stronger than M2. Similarly, we need M5 stronger than M3. But this relation contradicts with what is required for read operation, so we only honor the first relation that is M6 > M2. This concludes that Access transistor should be stronger than the pull up considering write operation for ‘1’ to ‘0’ and vice-versa.

Final Sizing

Combining the sizing for both the read & write conditions, the end result we get is as follows:

1. Access transistor width > Pull-down transistor width (for Write)
2. Access transistor width < Pull-up transistor width (for Read)

1.3 Power Dissipation

Power dissipation of 6TSRAM is mainly registered during read & write operations, only leakage power can be registered at hold state. Main source of power dissipation is dynamic & short circuit power that occurs during state switching (write operation) and discharging of bitlines (read operation). All the transistors contribute to power consumption and there sizing play important part. Larger is the transistor, more is the power consumption. So, proper sizing though necessary for the proper functionality, leads to increased to power consumption as compared to a minimum sized transistor 6TSRAM cell.

1.4 Process Variation

The continued miniaturization and increase in functionality of the modern electronics is the result of continuous shrinking of transistor scaling. An electronic device like smartphone that combines processor system and communication radios is possible because of the System on chip (SOC) revolution that integrates hundreds of millions of transistors in a few hundred millimeters-square of area. A single transistor is built of number of atoms where dimensions of a transistor can be described in nanometers. Moore's Law[1] is key driver to semiconductor industry's success which has kept the cost of fabricating a chip of more functionality at reduced area at same or reduced price.

In 1965, Gordon Moore predicted that transistor density would increase by twice every 18 months. The result of device scaling is reduced area and cost. But designers often pack more functional and performance enhancements to boost the consumer appeal which leads to sales at every generation of a product. However this doesn't translate to a challenge less endeavor once we begin scaling to sub 100 nm process node. Process variability is major hurdle to uniform and regular characteristics of a fabricated device.

Process variation is not a new phenomenon. Often called as process tolerance, it is a standard feature of most industrial processes. However in most of the cases, it is often possible to achieve a very low level of variance which is acceptable for its application. However semiconductor industry has always suffered from process related variations which were mostly due to imperfect fabrication techniques that result in sub-optimal

yields and operating margins. But the situation has only deteriorated due to the fact that at current process nodes, we are working at dimensions that are comparable to size of a molecule or atom. Even presence or absence of a single molecule may lead to variation which cannot be controlled even by using state of the art fabrication techniques. The result of high process variations ultimately means poor yields where dies operating in the specified tolerance range are only accepted while rest the discarded. Dies that are functional but are too fast which overshoots the total design power or too slow that leads to performance failures are also considered to be scrap. Thus process variation is not just a concern for process engineers but also circuit designers and design architects that needs to be concerned of this issue.

1.5 Sources of variation

Figure 1.6 shows the entire cross section of a CMOS technology to view the layers used in integrated circuit layout. Each fabrication process requires a number of process steps. For example, the well implant requires deposition or thermal growth of oxide, application of photoresist, lithographical patterning the photoresist, etching away of exposed photoresist to get the required pattern, implanting the required material and then finally removing the oxide and photoresist.

This entire process for each well. For formation of shallow trench isolation and other interconnect layers, additional polishing steps are required to achieve a uniform surface on which other layers can be fabricated. Modern chipsets require over 100 individual processes to fully fabricate the entire die.

These process steps can be : 1) lithography, 2) etching, 3) ion implantation , and 4) chemical-mechanical polishing (CMP). Each of these processes define the transistor and interconnect characteristics. Variations in lithography, etching and CMP causes variance in transistor behavior and physical dimensions of vias and interconnects. Ion implantation directly effects the structure at molecular level which causes variance in concentration of dopant material.

1. Twin-well Implants
2. Shallow Trench Isolation
3. Gate Structure
4. Lightly Doped Drain Implants
5. Sidewall Spacer
6. Source/Drain Implants
7. Contact Formation
8. Local Interconnect
9. Interlayer Dielectric to Via-1
10. First Metal Layer
11. Second ILD to Via-2
12. Second Metal Layer to Via-3
13. Metal-3 to Pad Etch
14. Parametric Testing

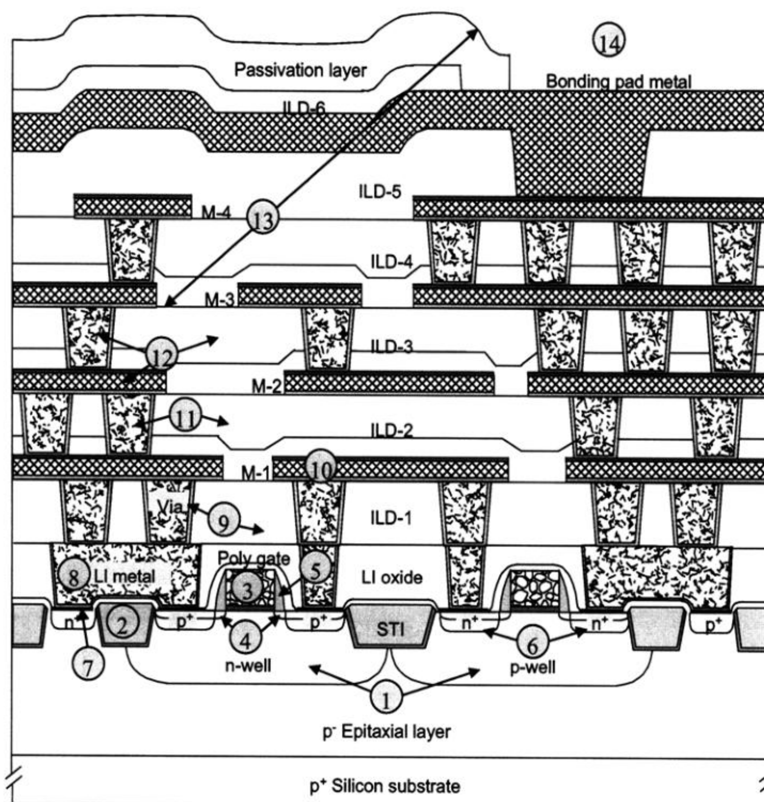

Figure 1.6 Cross-sectional view of a CMOS integrated circuit with major steps needed for fabrication [2]

As process node keeps on shrinking, process variations become increasingly difficult to tackle due to decreasing resolution of lithography, line edge imperfections, random dopant concentration fluctuations and variable oxide thickness. In the following sections, we discuss the before mentioned sources of variation in detail.

1.5.1 Lithography

Lithography is process of exposing a light sensitive material to obtain a particular pattern on a semiconductor surface. The light sensitive material is called photoresist. The wavelength of the electromagnetic wave used to define the feature has been scaling for a long time so as to achieve the required resolution of shrinking process node. However it was not possible to scale down after 193nm wavelength which was used at 180nm process node. This resulted to a number of lithography related variations due lens

imperfections, masking mistakes, non-uniform radiation, and non-uniform photo-resist. This also led to system wide line width variations[3]. A number of techniques were used like Optimal Proximity Correction (OPC), Sub-Resolution Assist Features (SRAF) and phase-shifted mask lithography to compensate for 193nm wavelength. Another area of concern are random variations in line edges called as line edge roughness(LER) which as shown in figure 1.7, results in local line width variations.

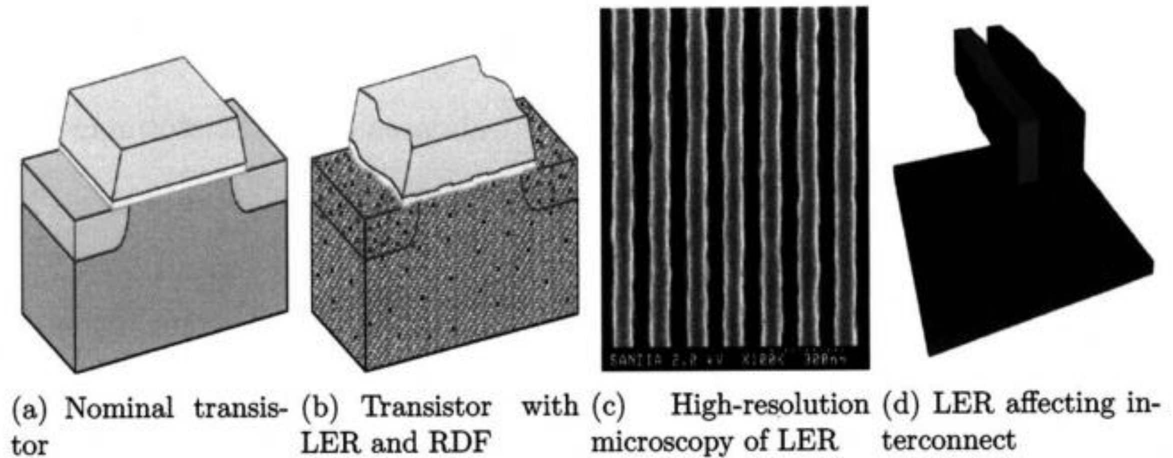

Figure 1.7 Line Edge Roughness [4]

Immersion lithography is often used commercially to achieve a higher resolution of the exposing radiation by immersing the entire setup in water or other liquid to achieve a higher convex nature of the lens system. EUV(Extreme Ultra Violet) allows for sub 193nm, but is still not commercially viable.

1.5.2 Etching

After lithographic process, etching is used to remove the exposed portion of material(in case of positive photoresist). This may be polysilicon in case of transistor gate or insulator like SiO_2 in case of interconnect. Variations in fabrication environmental variables like temperature, pressure, RF power and gas concentration leads to process variations.

1.5.3 Ion implantation

Creation of transistors involves doping with ions to define the nature of the material: n-type or p-type. Ion implantation is technique where these ions are accelerated to high velocity and allowed to penetrate into the target substrate for doping. This also involves heating the wafer which activates the lattice and ensures that dopants are properly trapped in substitution sites.

Variations in ion implantation can occur due to process conditions like implant energy and dose, angle of penetration and temperature. In sub-micron technology nodes, device features are so small that only a few hundred of maximum number of dopant atoms are required for the channel region (beneath the gate). Due to small number of atoms, variation in dopant atoms quantity and even arrangement is a cause for variation. This method of variations called Random Dopant Fluctuation(RDF) and was introduced by Keyes[5].In the figure 1.8 below, the dopant ions are visible in ion implant simulation for transistor. It is easy to visualise how changing the number of dopant atoms or there position can change the transistor characteristics. This only worsens with finer process nodes where the channel region volume only decreases along with dopant count and associated variations.

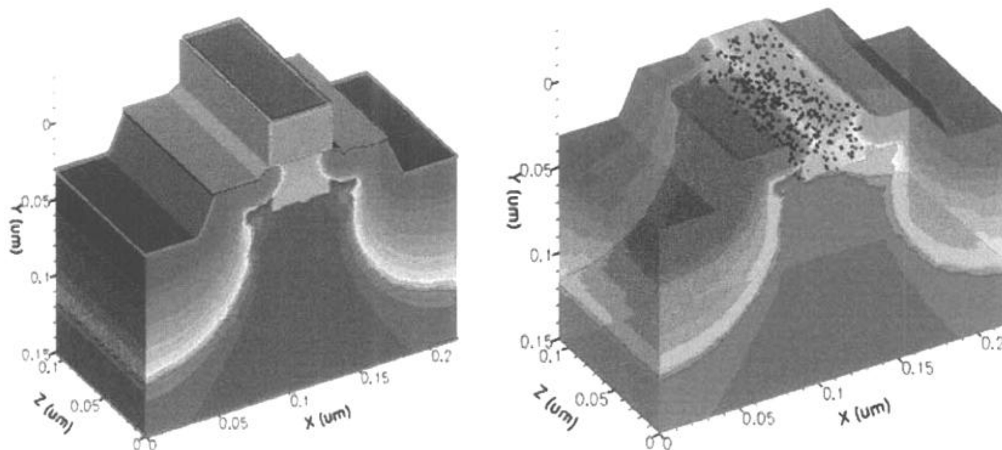

Figure 1.8 Simulation of Random Dopant Fluctuation (RDF) [6]

1.5.4 Chemical-Mechanical Polishing (CMP)

CMP is used to obtain a regular and smooth surface on which other fabrication steps may be performed. Decreasing resolution of modern lithography requires ultra smooth surfaces where even a disturbance of nanometers may cause a problem.CMP however itself introduces variations. CMP involves actions that involves parameters like down force, rpm and conditioning of pad and also temperature which finally affect the feature generated. The major effect of CMP, as shown in fig 1.9, where copper interconnects are dished and interlayer dielectrics eroded affecting copper interconnect height.

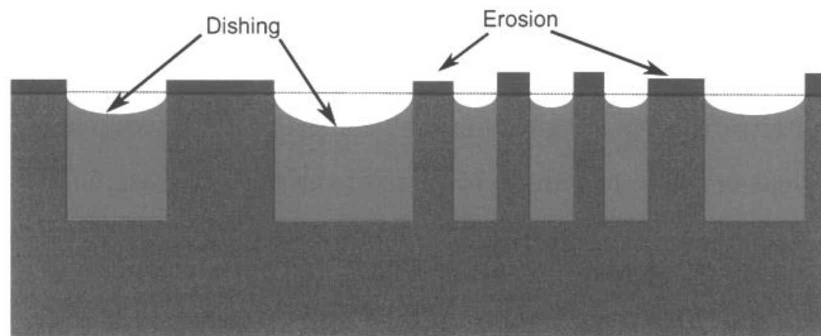

Figure 1.9 Dishing of copper and erosion of dielectric in CMP

Several strategies are used for mitigation of CMP variations. Many of the solutions involves improved process control methods that use feedback from the process itself to guide when polish should end [7].Automated mitigation strategies are used to manipulate pattern densities to reduce design susceptibility to CMP caused variation.

1.6 Impact on transistor parameters

Each of the variation discussed above leads to variation in electrical parameters of transistor and interconnects. In a typical integrated circuit, a transistor either charges or discharges a capacitive load. Current through the transistor is a function of mobility(u), oxide capacitance(C_{ox}),dimensions of transistor(length(L) and width(W)) and threshold voltage(V_t).Further time required to charge or discharge now depends on capacitive load(C_{load}),voltage applied(V_{dd}) and current through transistor(I_D).

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_T)^2 \quad (1.1)$$

$$t_d = \frac{C_{load} \quad V_{DD}}{I_D} \tag{1.2}$$

Variation in any of these parameters directly lead to change in the time required for charging or discharging of load capacitor. Typically in a digital CMOS circuit PMOS is used to charge the capacitor to V_{dd} while NMOS is used to discharge the capacitor to ground. Because of difference in fabrication techniques for NMOS and PMOS, it is very much possible to get more variation in one and less in another leading to asymmetric drive of charging and discharging of capacitors. The table below gives an idea which parameters are affected by which respective fabrication technique.

Table 1.1 Transistor Parameters and their respective variation source

Transistor Parameter	Fabrication process
μ	Ion implantation, gate oxidation
C_{ox}	Lithography, etch
W,L	Gate oxidation
V_T	Ion implantation, diffusion

1.6.1 Mobility

Mobility is defined as the tendency of a charge carrier(electron or hole) to travel through a semiconductor material under the influence of a electric field. Mathematically mobility is defined as

$$\mu_{n,p} = \frac{q\ \tau_c}{2m_{n,p}} \tag{1.3}$$

where q is the electronic charge, τ_c is the mean free time between carrier collisions, and $m_{n,p}$ is the effective mass of either an electron (n) or hole (p). Mobility often is a function if doping concentration as shown in figure 1.10 since doping concentration determines the mean free time between collisions. In modern processes, stress engineering is used to create stress in the lattice structure of p-type material to

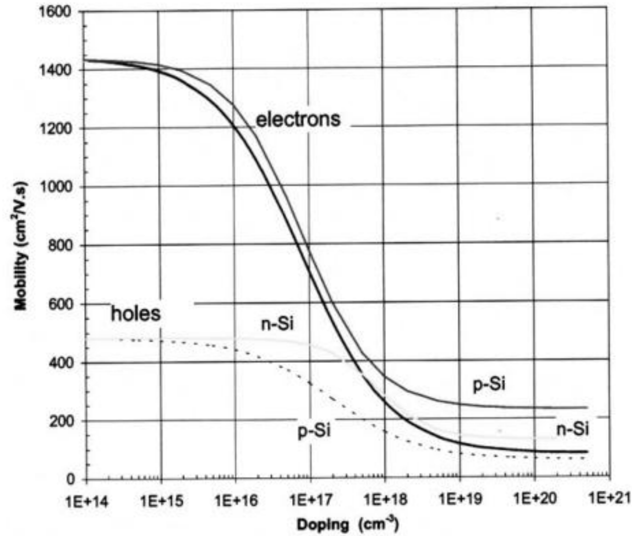

Figure 1.10 Mobility vs Doping concentration

increase its mobility. This compensates for the otherwise lower mobility offered by p-type material and related slower performance. Mobility improvements of over 10% has been achieved by use of advanced strain engineering [8].

However unintentional strain may also occur due STI proximity that can cause intra die mobility variations of the order of a few % depending on transistor location with respect to STI edge [9]. Recent characterization of mobility in advanced processes indicates quite large variations of 21% and also because of intrinsic fluctuations in process of intentional stresses [10].

1.6.2 Oxide capacitance

Oxide capacitance is the developed between poly-Si or metal gate and inverted surface in the channel region separated by oxide layer. The oxide capacitance is a function of oxide thickness and dielectic constant of oxide insulator.

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad (1.4)$$

Gate oxidation process is pretty well controlled step and dry oxidation is often used to obtain a slow and high quality oxide. However with gate oxide thickness in modern sub-micron devices reaching a paltry few nanometres, this means that oxide layer is now only

few number of atoms thick. For SiO_2 gate oxide, variations are about 20% that is single monolayer of atoms[11].Moreover oxide thickness also reduces the barrier to Fowler-Nordheim tunnelling and exponentially boosts gate leakage current. To tackle this problem, Intel has started using high k dielectric oxides like hafnium oxide to keep oxide thickness but also maintaining oxide capacitance and gate control. This allows for thicker oxides that considerably suffers less from thickness variability. But variability still occurs in interfacial oxide of high-K stacks.[12]

1.6.3 Transistor Dimension(W,L)

Width and length are directly responsible for current through the transistor according to equation 1.1. Length of the transistor is the technological parameter that has been scaled down every generation since the inception of semiconductor industry. Except for circuits that use a very narrow width comparable to the length, length is main parameter to watch out for process variation. Since the sub 180nm process nodes are patterned by 193nm wavelength light, which leads to major loss in resolution, variation in length is significant. Any variation in length directly leads to change in current through transistor according to equation 1.1, thus reflecting a change in time to charge/discharge a capacitive load. ITRS projections for length variability in 2003 was 10% but increased to 12% in 2007 and is only expected to increase in coming next generation processes.

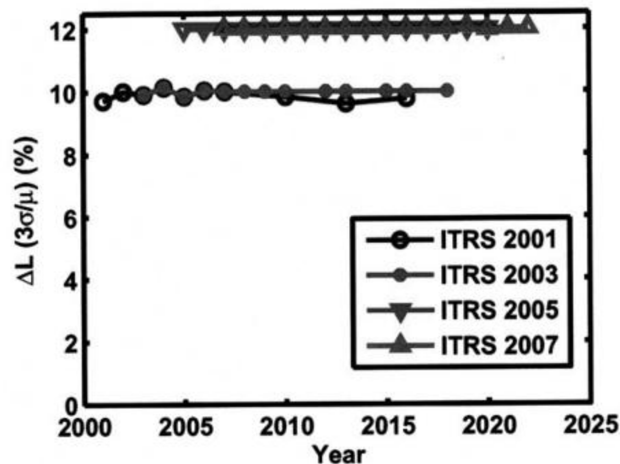

Fig 1.11 ITRS Projection for Channel length variation [13,14,15,16]

Normally V_t is a not a function of length of transistor but for deep sub-micron process nodes, DIBL(Drain-Induced Barrier Lowering) results in V_t lowering. This further brings in another form of variation in form of boosted transistor through current and reduced time to charge or discharge the transistor.

1.6.4 Threshold Voltage

The threshold voltage of a MOSFET is minimum gate to source voltage that results in formation of channel and significant flow to current from drain to source terminal. In a ideal long channel MOSFET, the threshold voltage is function of doping concentration and oxide capacitance where flatband voltage and Fermi potential are dependent on only doping concentration and γ is dependent on both doping concentration and oxide capacitance. In short channel. For short channel devices, Vt is also a function of channel length, junction depths and stresses.

$$V_{T_0} = V_{FB} + 2.\phi_{F_p} + \gamma.\sqrt{2.\phi_{F_p} + V_{SB}} \qquad (1.5)$$

Owning to this susceptibility and the intrinsic random variability of RDF, V_t is one of the most difficult to control parameters, with variations of over 30%. A lot of research has been done on V_t variations. Pelgrom et al.[17] observed that Vt variation is a function of area of device. As scaling shrinks the device dimensions as well as area, control over V_t has become more and more difficult. As the value of V_t has scaled with smaller process node, variations has become more prominent. For a minimum size transistor in a 45nm process node, variation in V_t is about 20%.

1.7 PVT Variations

Process, Voltage & Temperature (PVT) variations is often used as combined metric to simulate the effects of process variations, power rail fluctuations & temperature variations. Like process variations, statistical information is required on voltage & temperature variations so that the same can be reproduced during simulations to verify

the functionality of the circuit. Voltage variations are generally due to voltage drop along the interconnect lines and other interference like capacitive coupling. Temperature is generally is a function of ambient temperature & IR drop of the integrated circuits, which is a major concern in densely packed modern process nodes.

1.8 Effect on process variation on SRAM

Process variations can cause SRAM cell to fail from functioning properly as the above discussed effects can change the effective resistance of MOS used in SRAM cell that alters the transistor sizing and render the SRAM to fail in one or more ways discussed below.

1) Read failure: Read failure occurs when data stored in SRAM cell gets flipped during read operation. This failure depends upon the voltage V_{read} that appears at the storage node while reading it. If a storage node storing '0' gets charged to a voltage V_{read} greater than the trip point of inverter, this may trigger a state change in the cell. So, it is required to keep the V_{read} as low as possible to minimise the probability of read failure.

2) Write failure: Write failure occurs when a write operation fails to change the state of SRAM cell. This occurs when the voltage at the storage node('1'),called V_{write}, fails to discharge below the trip point of inverter.

3) Access failure: Access failure occurs when the voltage difference developed between the bitlines is less than the minimum requirement for the sense amplifier to work properly. This lead to incorrect sensing. This occurs due to insufficient current flowing through the access transistors, which is required to discharge the bitline.

4) Hold failure: Destruction of SRAM state due to lower supply voltage in standby/sleep state is called an hold failure. However , if standby/sleep is not incorporated in memory architecture, than hold failure probability is almost zero.

CHAPTER 2

LITERATURE SURVEY

2.1 Effect of process variations on SRAM

Process variations occurs because of lack of control over various parameters during actual silicon fabrication like doping concentration, inaccurate lithography leading to length and width variations and other reasons discussed in Chapter 1. One of the outcomes of process variations in terms of electrical parameters is change in current through a MOSFET affecting its relative strength. In case of global variation, there is a possibility of huge variations at die-level. This variation is often modeled as threshold voltage shift as a decrease or increase in threshold voltage as it directly relates to change in current through a transistor or rather its effective resistance.

Global variation usually effects the entire die similarly. So, a global process variation affects all the transistors of a die by a random threshold voltage shift. The maximum threshold voltage shift is often defined by process corners of a technology node, which are extreme corner cases possible after statistical sampling of the actual silicon. These results are then made available as model files which can be run on EDA to simulate the behavior of circuit under these extreme but possible process variations. So if a circuit is able to successfully simulate under process corners, we can be assured about the success of all real life silicon conditions. FF represents fast NMOS and fast PMOS, FS represents fast NMOS and slow PMOS & similarly for SF & SS. TT is the typical corner which is the ideal corner. A process state (in actual silicon) should be a state which is bounded by the 4 process corners that is FF, FS, SF & SS and should be ideally close to the TT corner (Figure 2.1).

Since we have already discussed how important transistor sizing is for proper working of SRAM cell, it is easy to see how process variations hurt 6TSRAM functionality and power consumption. The effect of process variations on SRAM can be modeled as change in effective width of transistors in 6TSRAM cell. This basically means that sizing

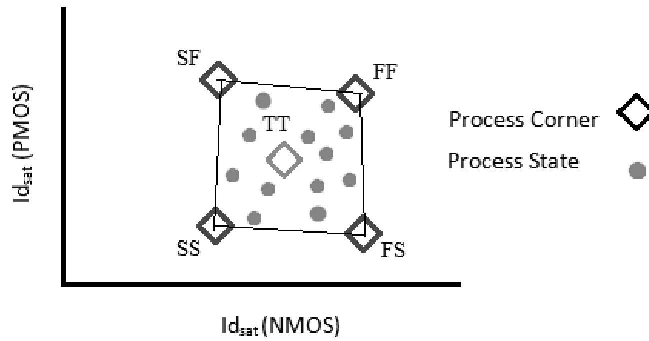

Figure 2.1 Process Corners & States

of the transistors is now directly affected by process variations. This can lead to read/write failures if the sizing requirements are not met. Also, faster corners if doesn't throw any read/write failure, definitely leads to higher consumption.

Process variations lead to SRAM parametric failures in following ways[19]:

1) Read failure: Read failure occurs when access transistors become stronger as compared to the driver NMOS. This can occur in case of a process variation where NMOS are fast(negative V_t shift) and PMOS are slow(positive V_t shift) or any other variation which makes NMOS relatively faster as compared to PMOS. This causes V_{read} to cross the trip point of inverter and cause read failure.

2) Write failure: Write failure occurs when the access transistors are not strong enough to flip the state of the SRAM cell. This can happen when NMOS access transistors are slow due to process variations as compared to PMOS drivers and NMOS drivers. This prevents the V_{write} to fall below V_{trip} which is necessary to disturb the current state and flip the state of the cell eventually.

3) Access failure: Access failures are also because of same reason as that of write failure. If access transistors are weak, they fail to discharge the bitlines to minimum required voltage difference within the read cycle window. This results in false read operation as sense amplifier output is wrong.

4) Hold failure: Hold failures are generally due to excessive leakage currents through the NMOS & PMOS drivers. So a negative V_t shift would result into more leakage current, meaning higher probability of hold failure at reduced V_{dd}.

2.2 Alternate SRAM cell design

6T SRAM suffers from poor read noise margins and doesn't fare well in presence of process variations as well as other voltage and temperature variations together called as PVT (Process, Voltage & Temperature) variations. A lot of research has been on alternate SRAM cell design that improve SRAM cell characteristics. Most of the improvements involve using additional transistors and modifying the way read and write operation is performed.

2.2.1 7T SRAM

Ramy et. al [20] uses a extra transistor between cross coupled transistors to get a 7T SRAM cell. The purpose of this extra transistor that acts like a pass transistor is to make or break the feedback between the invertors. During the read operation, "W" signal is kept high to emulate a normal 6T SRAM cell. However it is during the write operation, role of N5 comes into play. N5 is turned off which results into breaking of positive feedback between the inverters. Now only BL_bar is used for write operation which makes it single ended write operation but the usual dual-ended read operation. BL_bar is loaded with the complimentary of the data to be written and N3 is turned on. Node Q2 charges/discharges to reflect the data on the BL_bar. Q now gets charges/discharges to the compliment of Q2 and similarly occurs for Q_bar node. Once all these node are stable, N5 can be turned off. Turning off N5 should not be dramatic as it connects the nodes Q2 & Q_bar which are actually supposed to store the same voltage. So, write operation is completed successfully just by using a single bitline. This leads to major saving of upto 49% during write operation but at the cost of area increase of 17.5%.

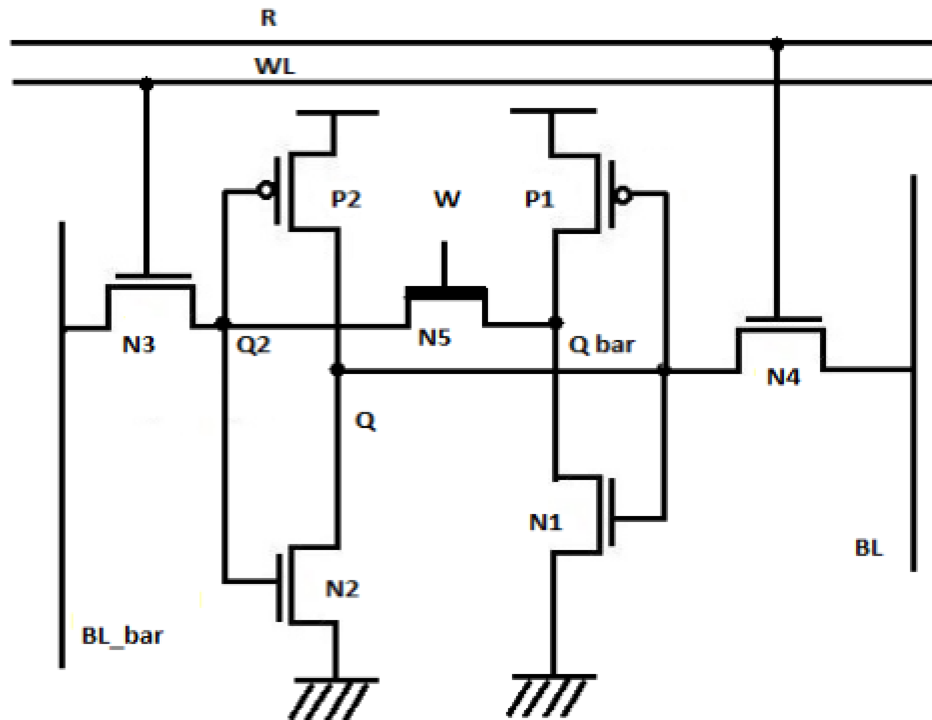

Figure 2.2 7TSRAM cell [20]

2.2.2 8T SRAM

The main reason for poor read noise margins in SRAM cell is due to the fact that read operation draws significant current out of the storage nodes which lowers the Vread and may even lead to read failure(undesired flipping of memory state) if Vread is low enough. This problem can be circumvented by using a alternate arrangement as shown in figure 2.2 as proposed by L.Chang in [21]. This design uses single ended different bitlines for read and write operation.For write operation, the write_word_line is loaded with the data to be written and then M5 is turned on to force the node Q to change. Once node Q is changed, this effect propagates to Q_bar as well.So its similar to conventional 6TSRAM write operation only with the exception of single-ended nature. However, read operation is completely changed. The Q-bar is used to sense the state of the cell but it only drives the gate terminal of the next transistors and the current via the storage nodes

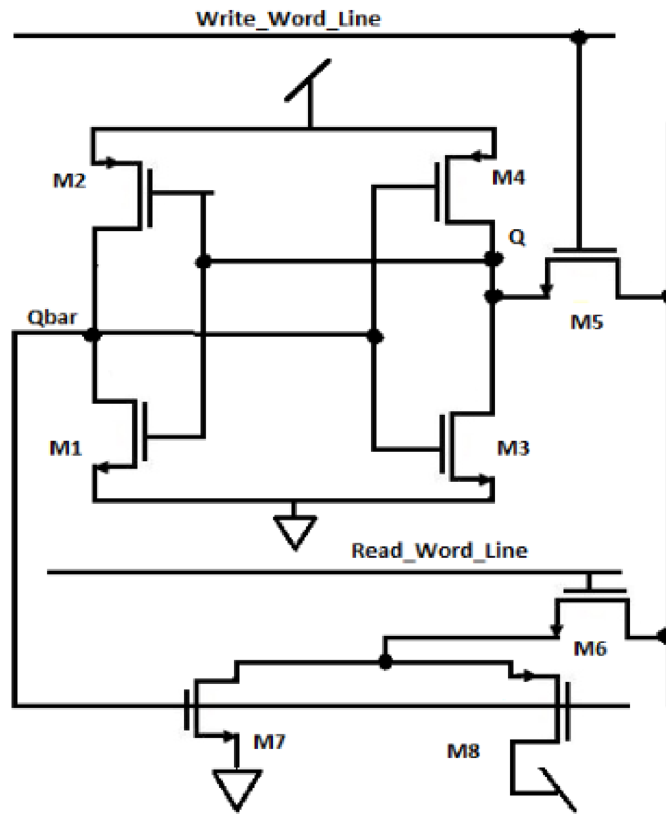

Figure 2.3 8TSRAM cell [21]

are is almost negligible save for the gate leakage currents. If cell stores state ‘1’ that is Qbar is ‘0’ which turns on M8(PMOS) but turns off M7. So when Read_word_line is asserted, a conducting path is created between V_{dd} and bitline.Since bitline is already precharged to V_{dd}, we see no difference in voltage at the bitline. Altenatively, if cell state is ‘0’, bitline is connected to ground which leads to discharging of the bitline. Another noteworthy addition to the read operating could be use of $V_{dd}/2$ precharging which will easily double the voltage swing for read ‘1’ and read ‘0’, easing the sense amplifier.8T SRAM however suffers from slow write due to asymmetrical write operation using a single bitline. Morever, 8T cell takes 30% more area as compared to conventional 6T SRAM cell.

2.2.3 9T SRAM

9T SRAM circuit[22] improves upon the previously discussed 8T SRAM by using same differential bitlines for both read/write operation but uses dedicated paths for read and write. The write operation is same as conventional 6T SRAM by using two differential bitlines. But the read operation uses 3 transistors to reflect the changes back to the same bitlines. NMOS N5 is turned on whenever Node1(State) is high which automatically implies that N6 is turned off as Node2(State compliment) is low. So when RD is turned high, a path is created between bitline BL and ground N5 & N7.This allows the BL to take a voltage drop at BL while BLB remains at precharged level. Similar operation occurs when cell state is zero where BLB takes a voltage drop. This makes the cell architecture compatible with the 6T SRAM cell save for the additional requirement of routing WR & RD signals to the cell instead of Wordline(WL) signal.

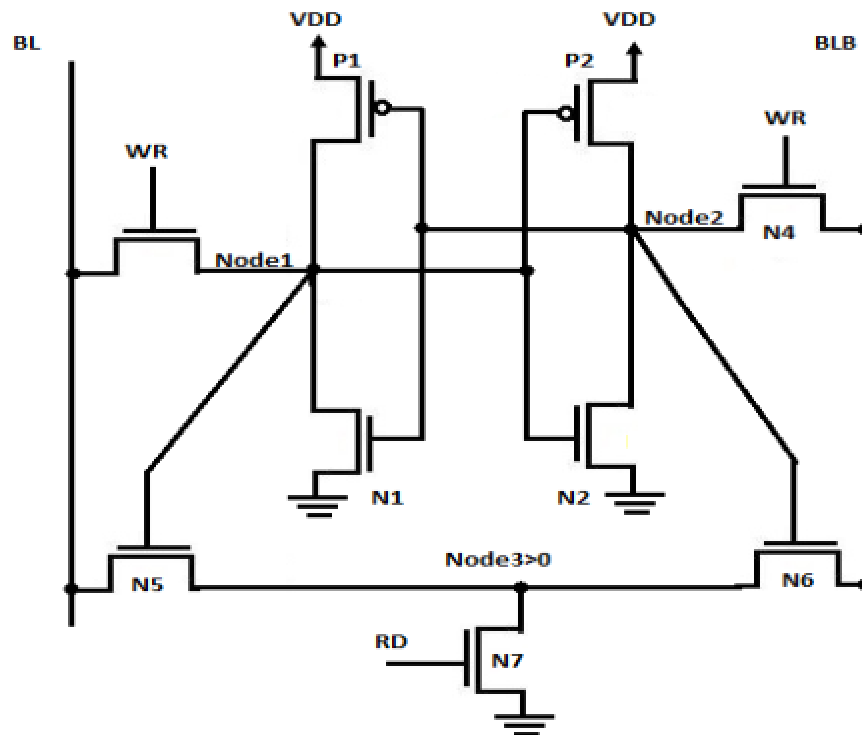

Figure 2.4 9TSRAM cell [22]

Though the above mentioned SRAM cell designs have better noise margins as compared to 6TSRAM, they are also not immune from process variations. So they will continue to

have degraded noise margins & fluctuating power at process corners. Moreover, since more number of transistors are employed the power dissipation goes high as well.

2.3 Process sensors

Process sensors the circuits which are capable of identifying the current process condition of the silicon. Process sensors can be analog or digital. Analog sensors generally compare a current parameter to a reference current source. Digital sensors, on the other hand, are delay based, where a counter is used to measure the time elapsed between two time events.

1. SRAM based Analog Sensor
2. Digital sensors

2.3.1 SRAM based Analog Sensors

Process sensors aimed at sensing the operating condition of SRAM cell generally use a test SRAM cell or the entire SRAM array to measure current in a particular branch of the circuit and compare it to a reference current source.

Hassan et. al [23] uses the circuit in figure 2.5 circuit is used to sense the active threshold voltage of the operating PMOS. The equations explaining the behavior are given below. A similar complimentary circuit is used to sense threshold voltage of NMOS.

Nildari et. al [24] uses a technique where circuit doesn't measure threshold voltage or process state. It directly measures the noise margin which can be determined by taking the difference between V_{read} and V_{trip} .(Figure 2.6) The sensing cell consists of two half-cells where the left one is configured to measure trip voltage of inverter and right one measures V_{trip} . Both these voltages are then fed to PMOS P0 which generates current I_{sensor} which is compared to a reference I_{ref} . The comparator then generates a voltage (or digital output in this case) which is used to measure the read noise margin.

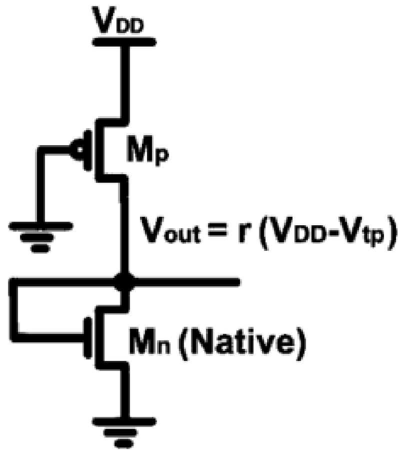

Figure 2.5 V_{tp} sensor [23]

$$V_{out} = V_{tn} + r.\left[V_{DD} - V_{tp}\right] \quad (2.1)$$

$$V_{out} \sim r.\left[V_{DD} - V_{tp}\right] \quad (2.2)$$

$$where \quad r = \left(\frac{k_p . \frac{W_p}{L_p}}{k_n . \frac{W_n}{L_n}}\right)^{\frac{1}{\alpha}} \quad (2.3)$$

Another method of measuring process state is by measuring leakage current through SRAM array[25]. If leakage current is high, it indicates a faster corner which means lower Vt corner. The circuit in figure 2.7 uses two reference current sources, which means the operating leakage current can be lower than first one, greater than the second one or lie between them, thus resolving into 3 regions of operation.

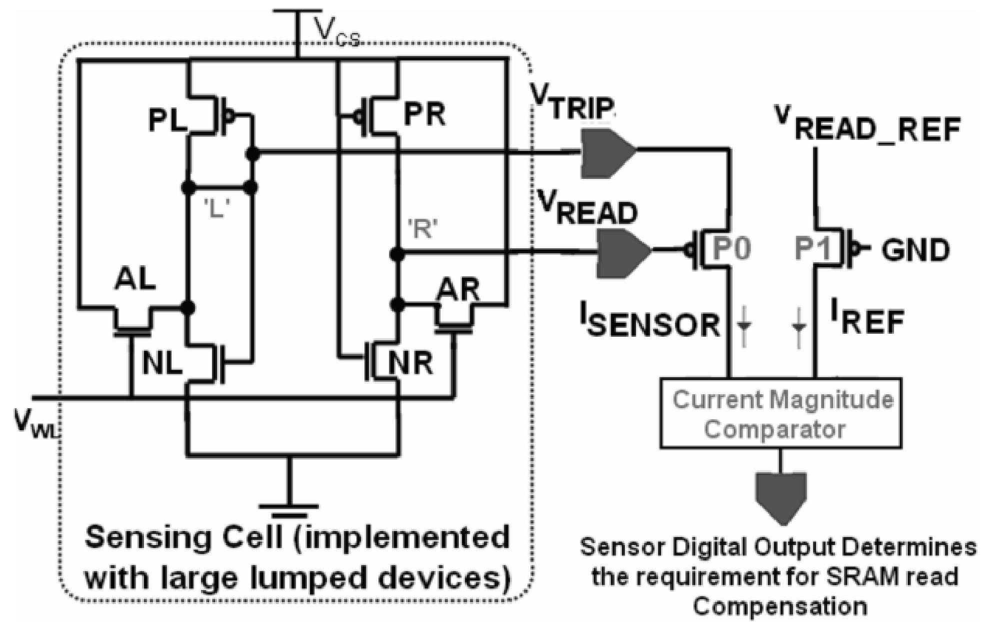

Figure 2.6 Read noise margin based process sensor [24]

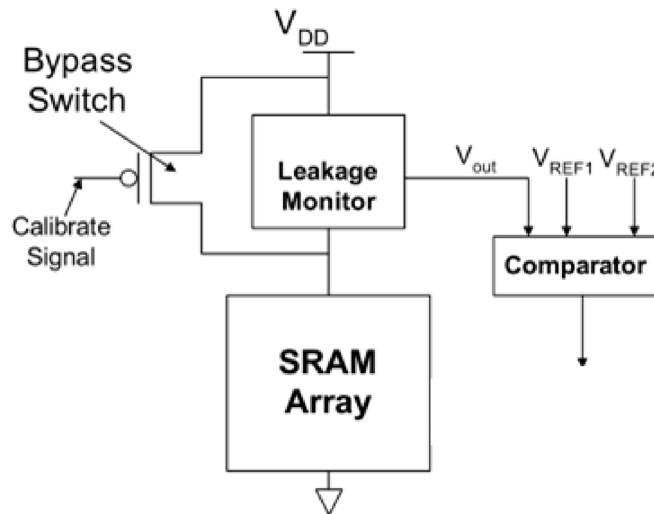

Figure 2.7 Leakage current based process sensor [25]

2.3.2 Digital Sensors

Digital sensors employ combinational and sequential circuits to count and compare delay based parameter. They don't need any current comparators, reference sources or amplifier and can be built by using logic gates and flip-flops.

Figure 2.8 Inverter chain based process sensor [25]

A 60 stage inverter chain is used by [25] to identify the operating process state. Let us say, at t=0, a input to the inverter chain goes high from a initial low level. The same rise in voltage is reflected at the output after some time(due to even number of inverters). This change in level can be monitored by a digital controller which runs a counter as long as the rise in voltage is not detected at the output. This counter value gives a good estimate about the process state. Higher the value of the counter, faster is the corner.

Ming-Hung Chang et. al [26] has proposed process, voltage and temperature sensors that are used for implementation of DVFS(dynamic voltage frequency scaling) system. Process and voltage is sensed by a combined sensor called process-voltage (PV) sensor. It consists of 31 stage ring oscillator(along with a NAND gate and enable control signal) whose characteristics are highly process and voltage dependent. PMOS and NMOS characteristics vary with change in process conditions. Temperature also leads to variation but variations are far more subtle to be observed as compared to change in process and voltage. The author uses low threshold transistors for inverters used in ring oscillator. The ring oscillator output is fed to a counter to count the number of pulses in a given time period. A 9 bit counter is used to detect the process conditions and temperature. PV[8:4] is used for detecting changes in process(while enable is high). The sensor resolves SS,TT and FF corners are measured at 7,11 and 16 values of PV[8:4] respectively.

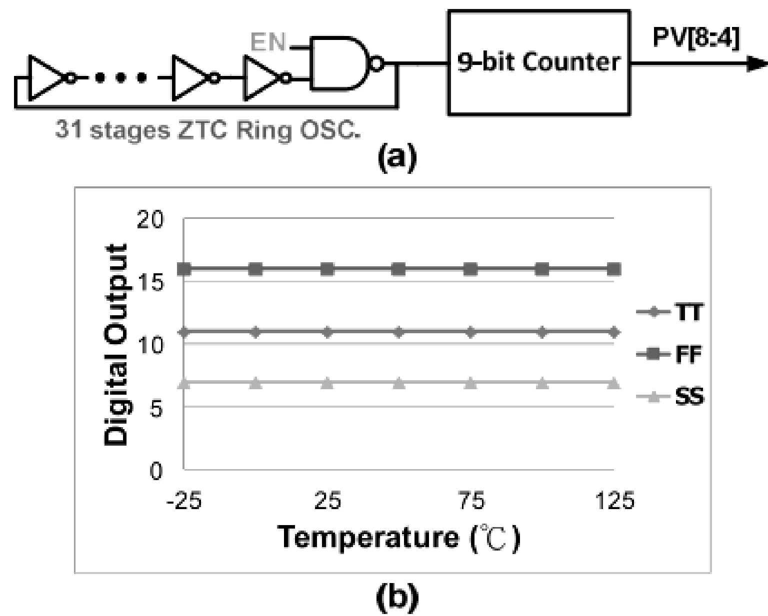

Figure 2.9 Ring Oscillator based process sensor [26]

[25] uses two methods to identify process corner & subsequently apply body bias, by monitoring of leakage current & by measuring delay in a inverter chain. Both the methods are compared & it is found that delay monitoring method is more robust & scalable and is preferable for large arrays.

2.4 VTCMOS

Variable threshold CMOS (VTCMOS) is method of applying multiple voltages to body terminal of a MOS to manipulate the effective threshold voltage of the transistor. To implement VTCMOS, a bias circuit is used to feed the required bias to the transistor's body terminal. In active mode, where circuit is required to operate normally, a zero body bias is applied. In standby or sleep mode, a high reverse body bias is applied to suppress leakage currents. Moreover, a little forward body bias can be used to speed up the circuit which also reduces short channel effects. But implementing VTCMOS adds to the overall area due to routing of the body voltage lines.

Once a process sensor has identified the operating process sensor of the silicon, the circuit needs to dynamically set the body bias to compensate for the process corner. The actual circuit operates in a particular process state that is bound by the process corners. Since there are infinite process states possible, it is necessary to divide the entire sample space into logical regions. Once the operating region has been identified, required body bias can be applied to counter the effects of process variations.

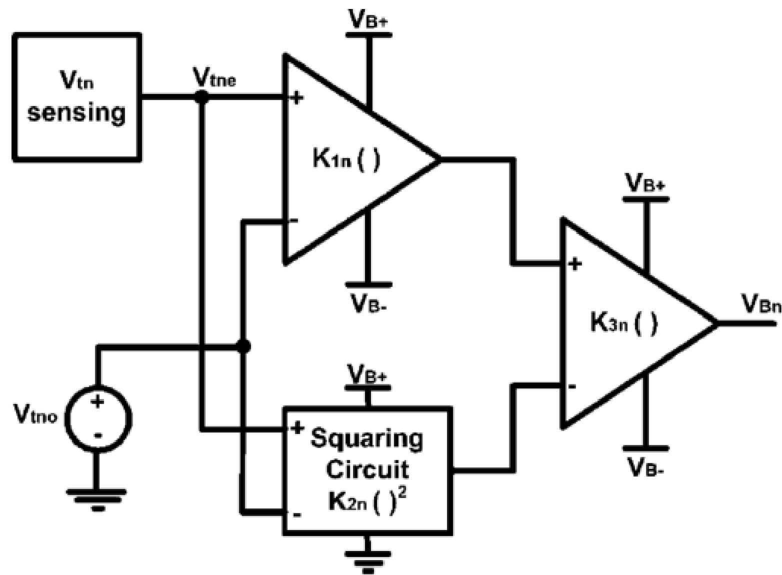

Figure 2.10 Analog adaptive body bias [23]

[23] uses a Vt sensing circuit as discussed in section 2.3.1 and uses the setup in figure 2.10 to implement adaptive body biasing. It involves use of differential amplifiers and squaring circuits to finally feed V_{Bn} to 6TSRAM.

Saibal et. al [19] has done comprehensive analysis of body bias technique in fixing the parametric variations due to intra and inter die variations in silicon. Parametric failures are defined as functional SRAM errors such as read, write, access, and hold failures. Using body biasing alters the threshold voltage of a transistor and can be used as method of repairing the variation incurred due to process variation. Applying a forward bias to the body terminal(FBB) reduces the effective V_t of NMOS transistor whereas a reverse body bias(RBB) increases the V_t of a transistor. The author proposes the use of body bias

only to NMOS transistors of the 6T SRAM & analyses the effect of body biasing on parametric failures as follows:

1) Read failure: Read failure occurs because of a strong NMOS access transistors. So using RBB increases the threshold voltage of the access transistor which makes it weaker. This reduces the V_{read} which reduces the chances of read failure. Moreover it increases trip point of inverter thus increasing gap between V_{read} and trip point of inverter.

2) Write failure: Write failures occur due to slow access transistors as compared to pull up and pull down transistors. Using FBB decreases Vt of NMOS transistors. So access transistors are stronger, which increases write current through them and reduces write time which directly leads to reduction in write failure probability. Though trip point of inverter increases, but its effect is not as prominent.

3) Access failure: Access failures are due to weak access transistors that due not provide enough current to discharge the bitline sufficient for the sense amplifier to obtain the correct output. So, FBB significantly reduces access failure probability.

4) Hold failure: Hold failure generally occurs only when V_{DD} is scaled down to a voltage, let us say V_{DDmin}. Using RBB reduces probability of read failure as it reduces leakage current which in turn allows for a lower V_{DDmin} without any hold failures.

The entire process variations set is divided into 3 regions based on inter-die shift(IDS): $IDS < -75mV$, $IDS > 75mV$ & $-75mV < IDS < 75mV$. The first region requires RBB to decrease effective V_t, similarly second region requires FBB and third one requires no effort that is ZBB. For process sensing use of ring oscillator or leakage current monitor is suggested but the paper doesn't discuss the implementation. The proposed circuit leads to a yield improvement of up to 25%.

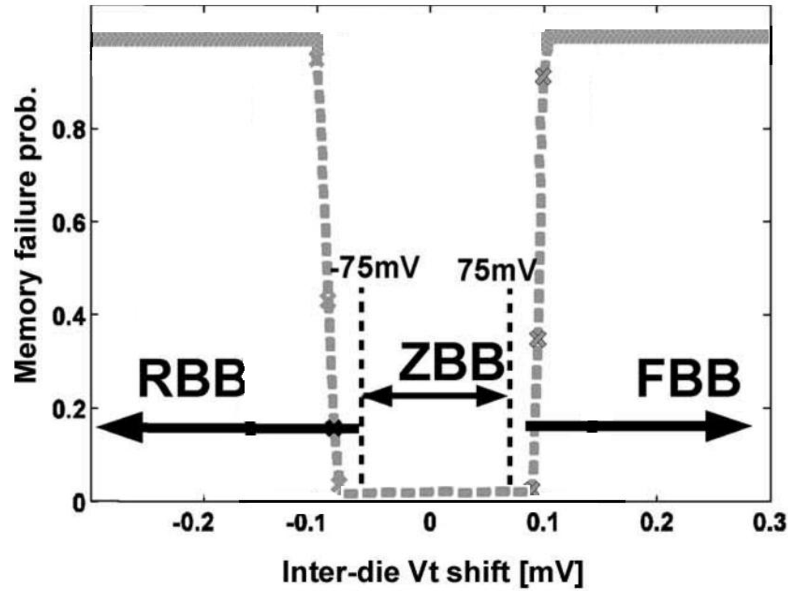

Figure 2.11 Regions specifying V_t shift for body biasing [19]

2.5 Research Gaps

Most of the work done in adaptive body biasing for SRAM is aimed at improving yield and reducing read/write failures [23,24,25] which are in fact inter-related. If the wafer has a die that exhibits read/write failures, it is discarded and thus brings down the yield. So theoretically if there is not a single read/write failure involved die in a wafer, yield is 100% but in real life there are other reasons for decreasing yield.

However process variations not only effect the functionality of SRAM but power consumption as well. Power dissipation at faster process corner is always more than the typical process corner. So, in a modern deep sub-micron process node, probability of operating near the process corners is very high, which means a lot of extra power is dissipated(at faster corners) and read/write errors occur.

Objectives of Thesis

Objective of the thesis is to design a low power & process resistant 6TSRAM circuit using active process tracking which can be used as a potential alternative to conventional 6TSRAM array.

2.6 Methodology

The aim of proposed circuit is to dynamically vary the body bias applied to NMOS transistors of 6TSRAM cell to compensate for the reduced resistance to PVT variations and increased power dissipation at process corners. SRAM cell used in this design deliberately uses under-sized transistors, which is just sufficient to pass the typical corner. The process sensor (ring oscillator) along with Process Decoder identifies the operating process corner of the die and generates the required body bias to correct the threshold voltage of NMOS transistors in 6TSRAM cell to ultimately control power dissipation and allow enhanced resistance to PVT variations in spite of using almost minimum sized transistors in SRAM cell.

CHAPTER 3

DESIGN OF PROCESS ADAPTIVE 6TSRAM

The proposed circuit, Process Adaptive 6TSRAM (PA6TSRAM), comprises of following sub-circuits:

1. SRAM cell
2. Process Sensor
3. Process Decoder (to generate control signals)
4. Voltage Control Block (for VTCMOS)

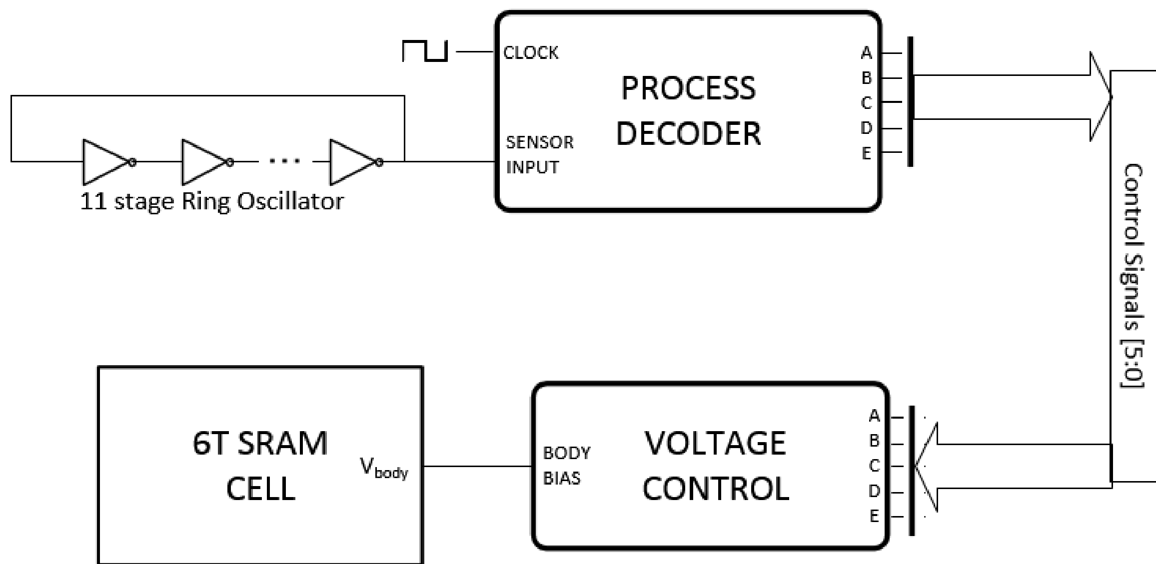

Figure 3.1 PA6TSRAM Architecture

3.1 SRAM cell

The base 6TSRAM cell used for the proposed circuit is a minimum possible sized SRAM cell with a $V_{dd}/2$ bitline pre-charging as compared to conventional V_{dd} pre-charging. The benefit of using $V_{dd}/2$ pre-charging is reduced probability of read failure due to the fact

that the storage node being read now theoretically charges/discharges by $V_{dd}/2$ as compared to V_{dd} in conventional SRAM, which makes it almost immune to read failures[10]. It passes all process corners, but SF and SS corners(without body biasing), which throw write failure, due to weak access transistors at these corners. The motive behind using inadequate sizing is to reduce power and area, as the body biasing will provide the V_t shift required for proper operation. The pull-ups and pull-downs are sized at minimum possible 400nm/180nm while Access transistors are sized at 600nm/180nm to allow write operation at 1GHz. This base cell is mated with process tracking and compensation circuit as in figure 3.1.

3.2 Process Sensor

This circuit uses a ring oscillator as a process sensitive test circuit. A ring oscillator consists of odd number of stages of back to back connected inverters that acts like oscillator running at a particular frequency. This frequency is a function of the delay of the inverter used in the ring oscillator which depends upon the size of PMOS and NMOS, node capacitance, number of inverters and most interestingly the process state. Any variation in the process state shifts the frequency of the ring oscillator considerably. For the proposed circuit, 11 stage ring oscillator is used.

A particular process state now maps to a unique frequency. The variation in frequency is directly proportional to the proximity between two process state under comparison. For example, moving from FF corner to SS corner gives maximum frequency shift while moving from a FF to FS gives a lesser extent of frequency shift.

3.3 Process Decoder

The process decoder consists of the logic responsible for converting ring oscillator frequency into respective control signals that drive the Voltage block. Since frequency of the ring oscillator is now a measurable parameter that varies with process state, its measurement can be done. One of the easiest ways of measuring frequency of a periodic waveform is by counting the number of pulses in a given fixed time. The circuit is implemented by Verilog module in mixed signal simulation that can be readily

synthesized for transistor level implementation. The digital block basically serve two purposes. One is counting of the pulses that is achieved by triggering a counter on every positive edge of the ring oscillator output. The counting starts as soon as the clock goes high. The clock has a time period of 300ns with 50% duty cycle .The counter counts as long as clock is high and when it falls, the value of the counter is passed to the combinational decoder that implements the strategy required for power saving at FF,FS process corners and improving V_{read} (with neighboring process states) while allowing the SF,SS process corners (with neighboring process states) to pass gracefully that would otherwise encounter write failure. At every positive edge of the clock, the counter resets itself so that it can count again in next cycle. Combinational decoder then maps the counter value to the required control signals for driving the VTCMOS voltage control block. The 6 bit counter ranges from the slowest (least frequency) at the SS corner to fastest (max frequency) at FF corner. At the mean point lies the TT corner, FS corner lies between the SS and TT while the SF lies between the TT and FF corners.

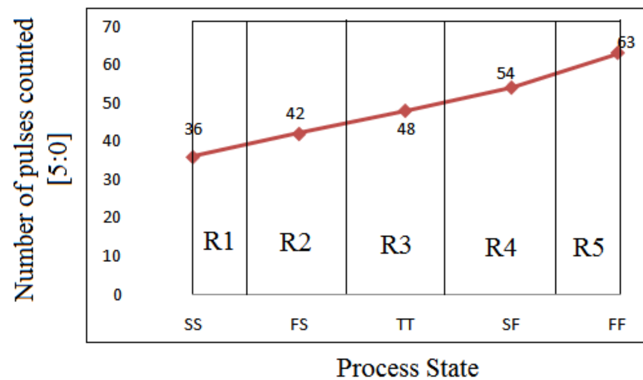

Figure 3.2 Counter value against Process state

Figure 3.2 shows the number of pulses counted against the process state. For purpose of mapping the counter value to the VTCMOS block, we partition the entire range of process states into five regions labeled as R1 to R5. Here each region corresponds to the process corner it contains. An actual piece of silicon is supposed to operate in one the these five regions, ideally at the TT corner.

Table 3.1 Output frequency & counter state at different process corners

Process Corner	Output Frequency (MHz)	No. of pulses counted
FF	423	63
FS	276	42
SF	360	54
SS	235	36
TT	321	48

The process decoder after identifying the region, maps it on 5-bit wide control signal lane (A,B,C,D,E). Only one control signal is high at a time and thus conveys the information the regarding the current operating process region. For example, if operating region is R5, then $[ABCDE]=[10000]_2$. Verilog code used to implement Process decoder is given in Appendix.

3.4 Voltage Control Block

The Voltage Control Block is responsible for generating the appropriate body bias voltage for the 6TSRAM cell which is function of the control signals ABCDE.

Table 3.2 Adaptive Body Bias Logic

Region	**Associated corner**	**Control Signal [ABCDE]**	**Action required**	**V_{body} (in V)**
R1	TT	00001	None	0
R2	FF	10000	Save power	-1
R3	FS	01000	Save power	-1
R4	SF	00100	Speed up circuit	+0.5
R5	SS	00010	Speed up circuit	+0.5

Region R1 requires no action as the base 6TSRAM cell works well without any change in body bias voltage of the cell. Regions R2 & R3 are fast regions where the silicon has a negative V_t shift which makes the NMOS faster. Reverse biasing the body terminal of

NMOS transistors will compensate for the process variation and also provide major power savings. Reverse body bias of -1V is applied in this region. Regions R3 & R4 are slow regions where the slow NMOS can be compensated by applying a forward bias of 0.5V to body terminals of NMOS . This should treat the write failures due to weak access transistors.

Voltage control block is implemented using five transmission gates that are controlled by control signals ABCDE. The outputs of all transmission gates are electrically shorted in a wired OR logic.

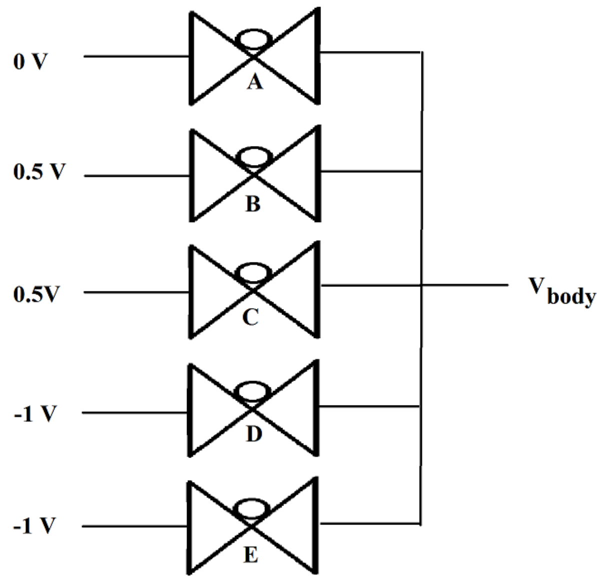

Figure 3.3 Voltage source selector

CHAPTER 4

SIMULATION RESULTS

The simulation results are divided into two parts:

1. Basic 6TSRAM cell
2. Process Adaptive 6TSRAM cell (PA6TSRAM)

4.1 Basic 6TSRAM cell

The simulation circuit used for 6T SRAM cell is shown in figure 4.1. The two NMOS pass transistors are controlled by signal wordline "WL". Both the pass transistors are connected to differential bitline signals BITLINE+ AND BITLINE-. The bitlines are loaded with capacitive loads which are a function of the array size of the entire SRAM memory.

Figure 4.1 6TSRAM with the peripheral circuitry

For reading & writing into the bitline, each of the bitline is connected to 2 transmission gates(TG); one for feeding the bit that is to be written into the memory cell and other for reading the current state of the memory cell. TGATE T1 and T3 when turned on by the signal READ provides differential voltage across READ+ and READ-, which can then be fed to a sense amplifier which ramps up the voltage to full scale V_{dd} or ground depending upon the signal DELTA=(READ+) - (READ-) is positive or negative. As the size of array increases, signal delta decreases and requires a more sensitive sense amplifier. Transmission gates T2 & T4 when turned On by the signal WRITE, accepts complimentary signals on the bitlines. Input to bitlines is provided by signals input to BITLINE+ "IP+"and input to BITLINE- "IP-". If IP+=1 & IP- =0, then memory cell stores logic 1 and vice-versa. It is required to precharge the bitlines for read operation, so PMOS Q1 & Q2 are used for that purpose. When PRECHARGE signal is ON, both the bitlines are charged to $V_{dd}/2$ that is 0.9V.

4.1.1 Signals used in simulation circuit

Table 4.1 Signals in Simulation circuit

WORDLINE	WL	Enables access to the internal memory state
WRITE	WR	Enables write operation
READ	RD	Enables read operation
PRECHARGE	PR	Precharges the bitlines to $V_{dd}/2$ [Active Low]
INPUT DATA+	IP+	Carries the bit to be written
INPUT DATA-	IP-	Carries the complementary of the bit to be written
STATE+	Q+	The bit stored in memory cell
STATE-	Q-	Complementary of the bit stored in memory cell
BITLINE+	BL+	Positive Bitline
BITLINE-	BL-	Negative Bitline
READ+	R+	Value read off the BL+
READ-	R-	Value read off the BL-
(R+) – (R-)	DELTA	Potential difference b/w R+/-

4.1.2 Specifications & Results

Table 4.2 Specifications

Process Node	180 nm GPDK
Supply Voltage	1.8V
Precharge Voltage	0.9V
Temperature	27 C
Bitline Cap	1 pF
Pull-up NMOS width	600 nm
Pull-down PMOS width	400 nm
Access NMOS width	800 nm

Table 4.3 Performance Parameters

Access Time (Read/Write)	1 ns/500 ps
Clock Cycle	500 ps
Write Data Rate	2 Gbps
Read Data Rate	1 Gbps
Peak Power	300 µW
Avg Power*	93 µW
Differential Output [(R+) – (R-)]	+640 mV / -300 mV

Write operation requires one clock cycle while read operation requires two clock cycles. In the 1st cycle, pre-charging is done and in 2nd clock cycle, read/write operation is performed. Thus each micro-operation is performed at a rate of 2GHz .

*Avg Power is calculated over process of initialising the Simulation circuit by Write '1' operation, then read '1' operation, Write '0' operation, then read '0' operation and finally Write '1' operation

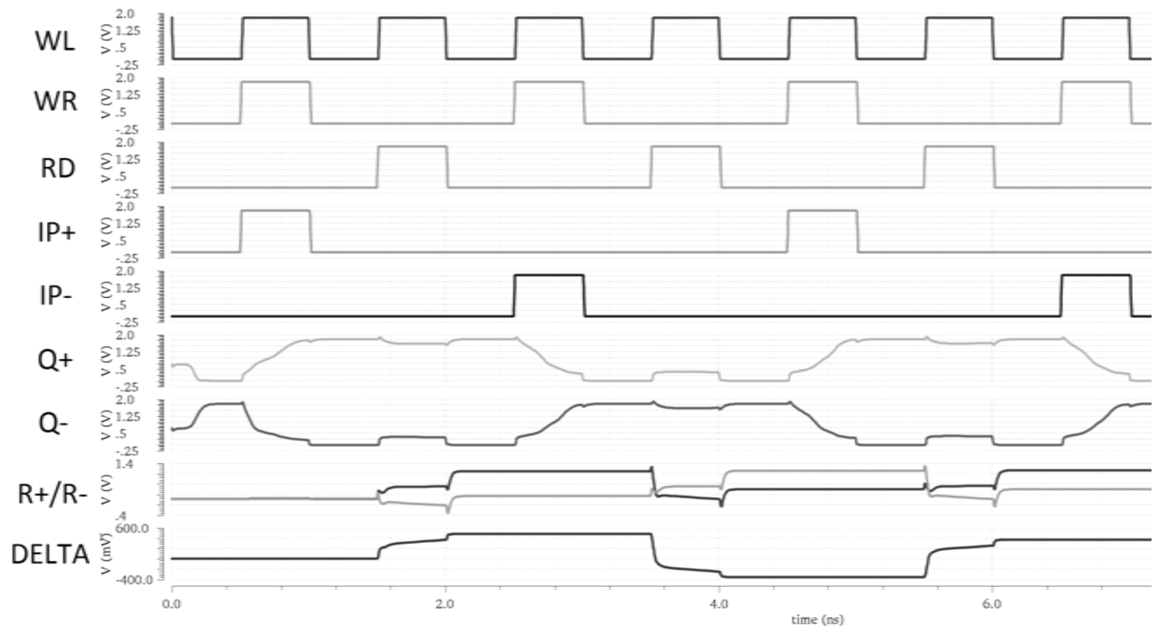

Figure 4.2 6TSRAM simulation showing read & write operations

4.2 PA6TSRAM

The following section contains simulation results of PA6TSRAM and its comparison with PS6TSRAM.

4.2.1 SRAM cell

PA6TSRAM cell is compared to properly sized SRAM cell (PS6TSRAM) and their sizing is described in Table 4.7.

Table 4.4 6TSRAM sizing

	PS6TSRAM	PA6TSRAM
NMOS Driver(nm)	600	400
PMOS Driver(nm)	400	400
NMOS Access (nm)	800	600

4.2.2 Process sensor

PA6TSRAM uses a 11 stage ring oscillator as a process sensor. The base inverter used in the ring oscillator is made up of minimum sized transistors that is 400 nm/180 nm for both PMOS and NMOS. Since NMOS is much stronger as compared to PMOS due to mobility difference, the duty cycle of the oscillator is less than 50% as NMOS quickly discharges the output as compared to PMOS so output stays at low level for more time.

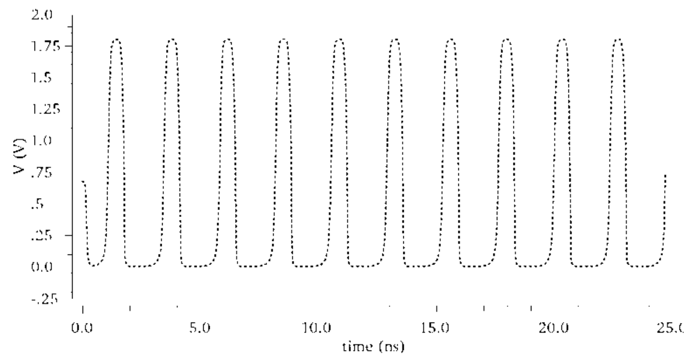

Figure 4.3 Ring oscillator output

4.2.3 Process Decoder

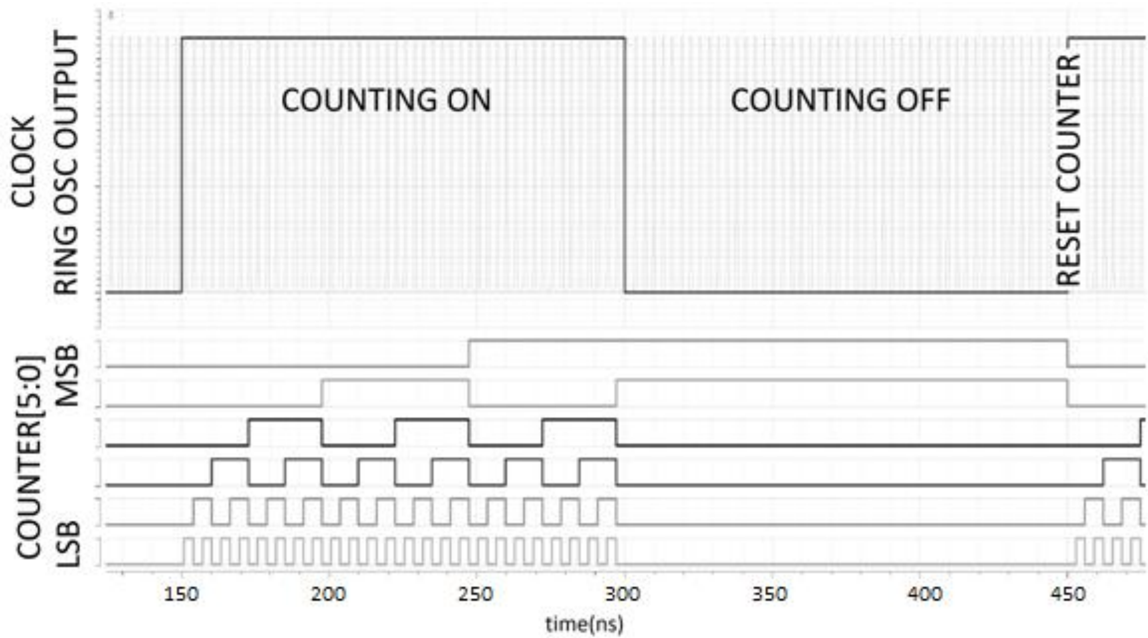

Figure 4.4 Process decoder showing clock, ring oscillator output(in background of clock signal) & counter state

The process decoder is designed in Verilog and imported as an AMS module in the test schematic. The counter starts counting when clock turns high. The 6 bit counter stops counting as clock goes low and holds the value of counter for entire low level of clock. During this period, the combinational portion of decoder becomes active and drives the control signal lane – ABCDE.

4.3 Comparison Simulations

Both the SRAM cells were subjected to Write ‘1’, Read '1', Write ‘0’ & Read '0' cycles with each Read cycle preceded by $V_{dd}/2$ bit line precharge. Each cycle was 500 ps long translating to maximum write data rate of 2 Gbps and read rate of 1Gbps.

4.3.1 Process Corner Simulations

Corner simulations have been done at 27ºC and power dissipation is logged for each process corner. All cases are verified for read/write failure and no failure has been found in PS6TSRAM and PA6TSRAM(Fig. 4.5).

Table 4.5 Power Dissipation

Region of operation	PS6TSRAM Average Power (µW)	PS6TSRAM Peak Power (µW)	AD6TSRAM Average Power (µW)	AD6TSRAM Peak Power (µW)
R1 | TT	93	300	74	235
R2 | FF	112	406	77	243
R3 | FS	85	343	60	204
R4 | SF	98	242	78	220
R5 | SS	78	215	64	200

Table 4.6 Power Reduction

Region of operation	Average Power Reduction (in %)	Peak Power Reduction (in %)
R1 | TT	20.4	21.6
R2 | FF	31.25	40.2
R3 | FS	29.4	40.5
R4 | SF	20.4	9
R5 | SS	17.9	6.9

Significant power savings are visible in TT,FF and FS corners while minor savings are seen in SS and SF corners(Table 4.5, 4.6). It is expected as major emphasis is to reduce power at faster corners .Hence maximum power saving is observed at FF and FS corners in both average and peak power consumption. TT corner, though is not eligible for any assist from VTCMOS, still shows power saving due to use of smaller transistors as compared to PS6TSRAM.

Slow process corners were prone to write failures, as discussed before, but use of forward body biasing compensates for the slow NMOS and hence both SS & SF corners shows no failure. As visible from the figure 4.5, PA6TSRAM cell shows a lower V_{read} for all the corners as compared to base PS6TSRAM cell due to body biasing. FF,FS corners (PS6TSRAM) show significant degradation due to faster access NMOSs as compared to driver transistors.

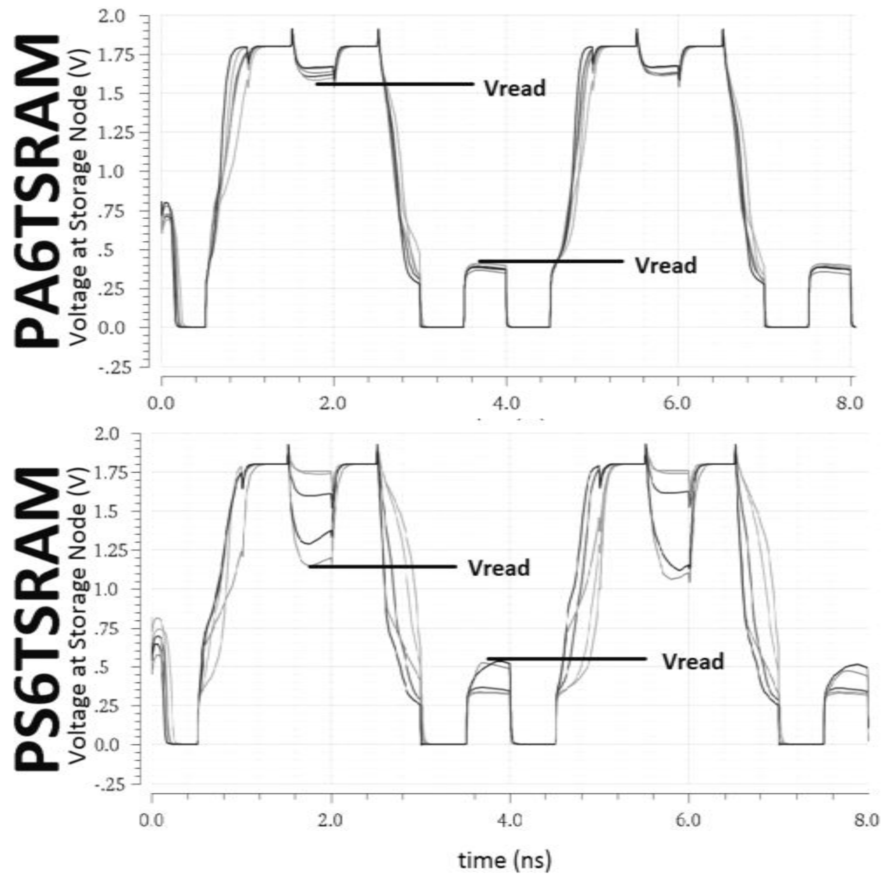

Figure 4.5 Process Corner Simulation of Write ‘1’, Read '1', Write ‘0’ & Read '0' cycle.

4.3.2 Monte Carlo Simulations

2000 point Monte Carlo simulation was performed to check resistance to process variations and mismatching. The results shown in figure 4.6 indicate failure free operations of both the circuits except difference in V_{read}.

Table 4.7 Power Dissipation in Monte Carlo Simulations

	Average Power (μW)		
	PS6TSRAM	PA6TSRAM	% reduction
Mean	92	72	21.7
Maximum (4σ)	96	81	15.6
Minimum (4σ)	87	63	38.0

Power dissipation was measured for all iterations of Monte Carlo simulations and it shows reduction in mean, minimum and maximum power consumed within 4σ standard deviation.

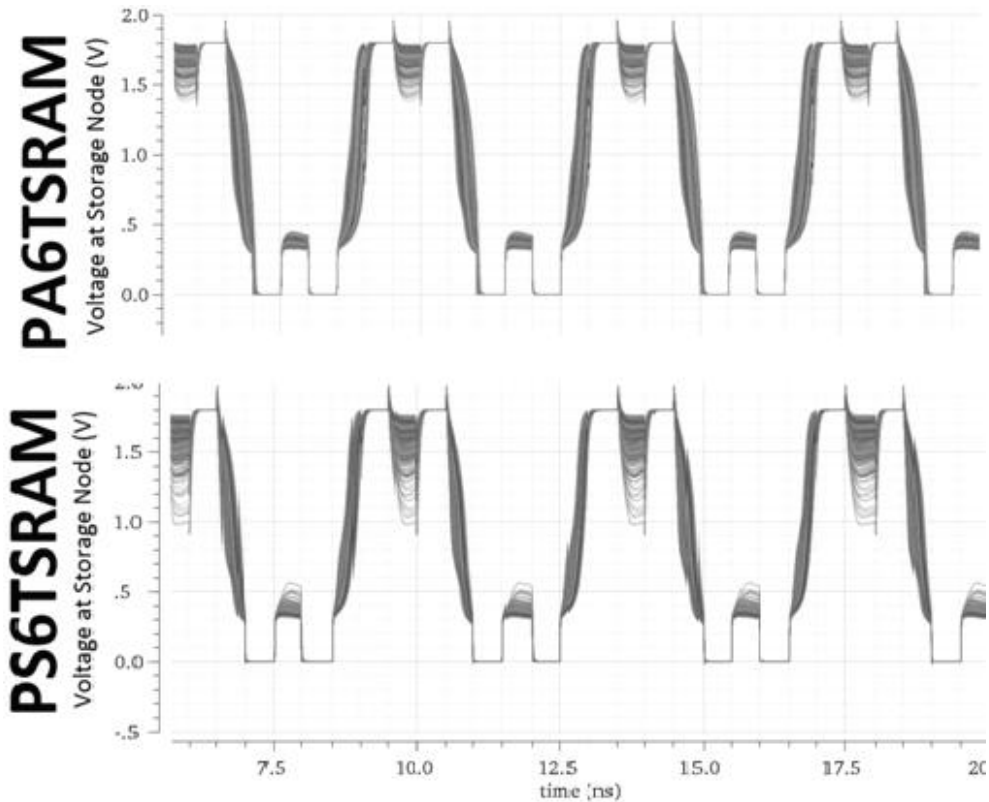

Figure 4.6 Monte Carlo simulation of Write ‘1’, Read '1', Write ‘0’ & Read '0' cycle

4.3.3 Width variance corner simulation

To check the resistance of PA6TSRAM cell to process variations, a corner simulation was set up to vary width of all transistors in the 6TSRAM cell by ±15%(Fig. 4.7). This helps to recreate both local & global process variations that are much more harsh as compared to the one employed in Monte Carlo Simulation. PA6TSRAM comes out with zero failures while PS6TSRAM cell failed at 49 out of 650 corners.

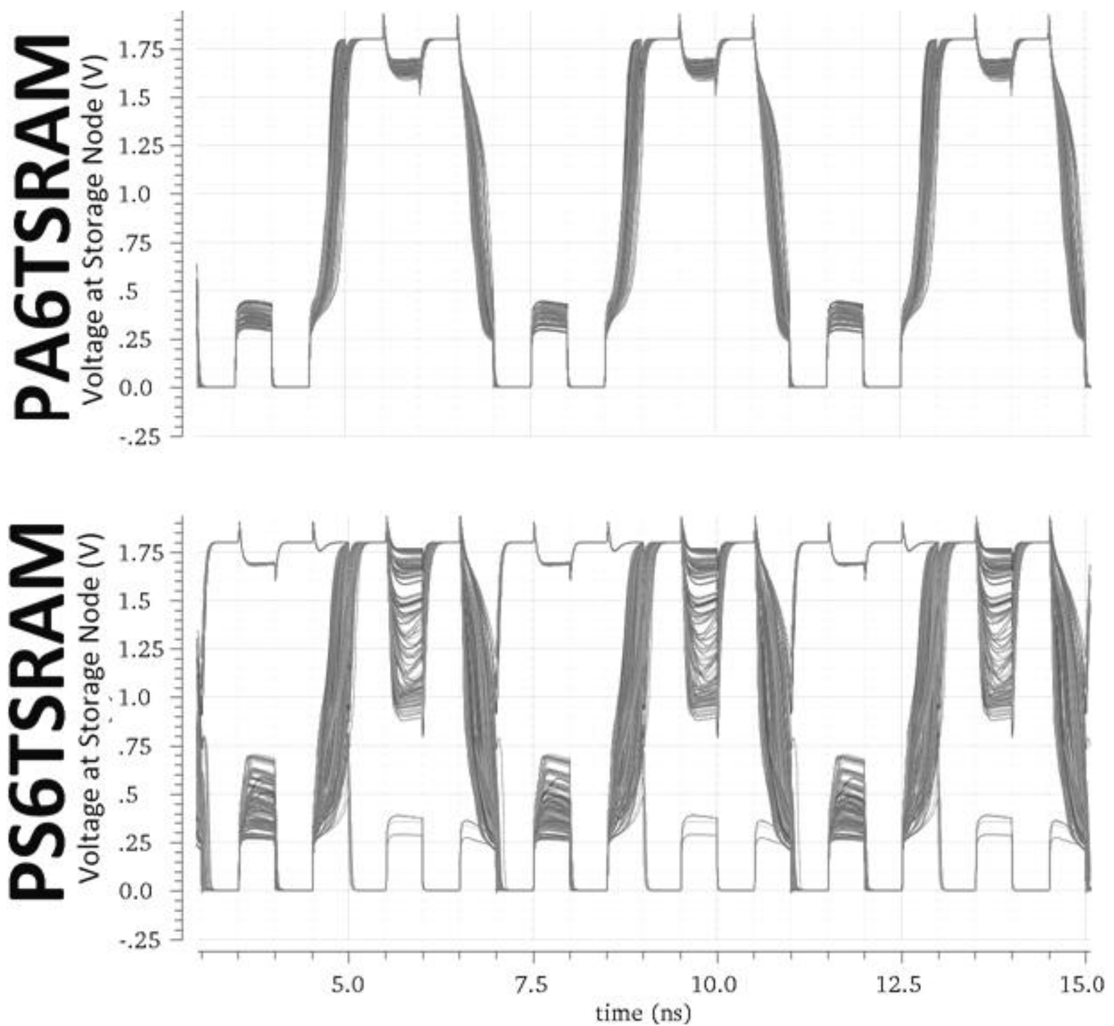

Figure 4.7 Width variance corner simulation of Write ‘1’, Read '1', Write ‘0’ & Read '0' cycle

4.3.4 PVT corner simulation

SRAM cells are subjected to PVT corner simulations. The variations are V_{dd} ± 10%, temperature varying from -20ºC to +80ºC and all process corners(Figure 4.8). PA6TSRAM clears all the combinations possible but PS6TSRAM fails on three corners (eg SS,1.62V,80 ºC) out of 45 corners.

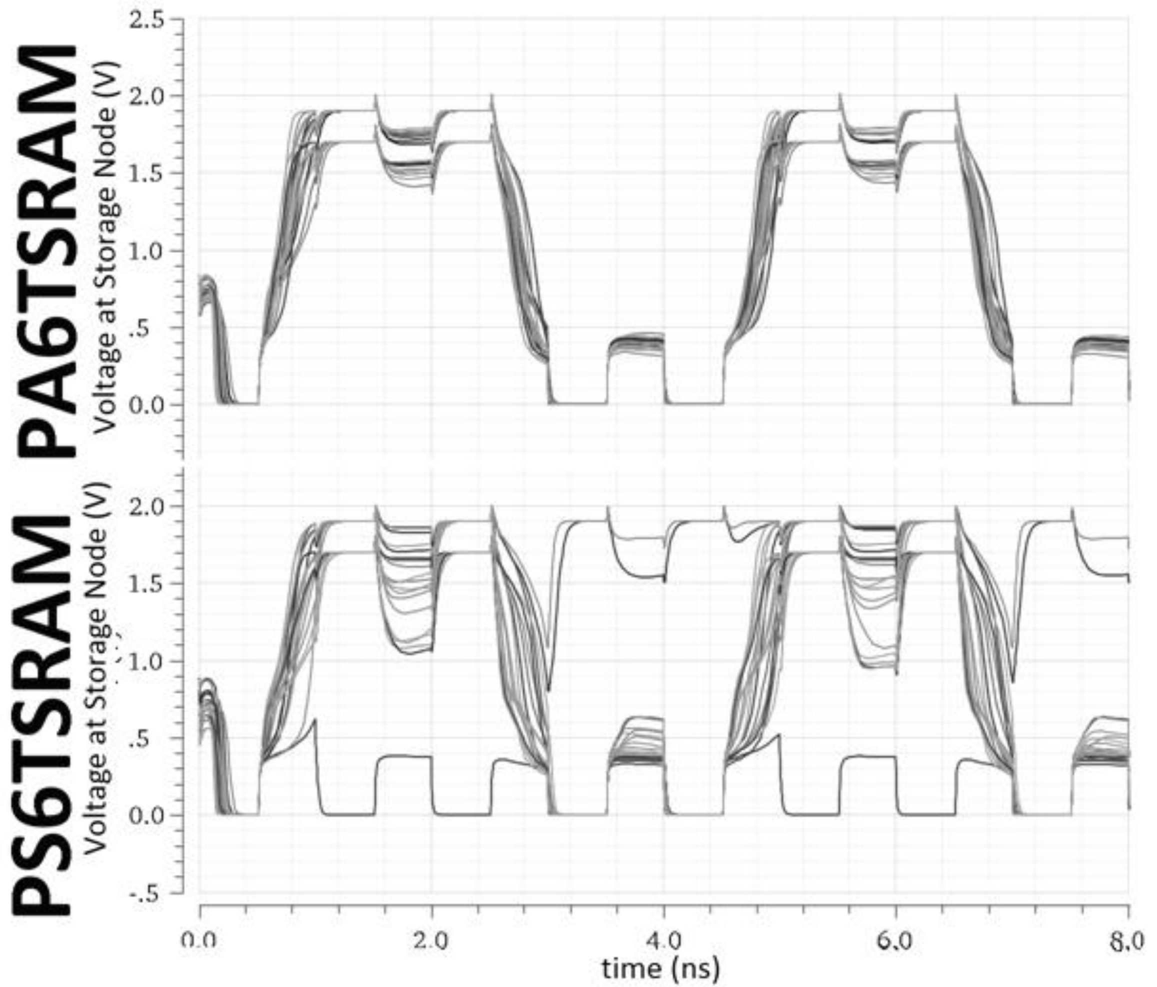

Figure 4.8 PVT corner simulation of Write '1', Read '1', Write '0' & Read '0' cycle

CHAPTER 5

CONCLUSION AND FUTURE PROSPECTS

5.1 Concluding Remarks

PA6TSRAM allows us to use 6TSRAM even at finer process nodes and bring in the benefits of lower power dissipation & improved resistance to process variations. Saving in power dissipation of upto 40% has been achieved in PA6TSRAM using VTCMOS. The effectiveness of this scheme becomes more relevant as process variation increases, that is, the probability of the circuit to operate at a typical process corner decreases and is redistributed to other farther process corners. But even at typical process corner, use of minimum sized transistors results in 20% power savings. All of these advantages make this scheme a viable alternative to basic 6TSRAM at deep sub-micron nodes.

5.2 Future Prospects

The scheme used for dividing the process sample space into operating regions can be further refined where high probability process areas (near typical process corner) can be allocated more number of regions as compared to low probability process corners. This will optimize the circuit for low average power dissipation & increased resistance to process variations.

APPENDIX

A.1. Verilog HDL code for Process Decoder

```
module veri4(ro,clk,cnt, A,B,C,D,E);
input ro,clk;
output A,B,C,D,E;
output reg [5:0] cnt;

reg a1,b1,c1,d1,e1;
assign A=a1;
assign B=b1;
assign C=c1;
assign D=d1;
assign E=e1;

always @(posedge ro) begin
        if(clk==1)
            cnt=cnt+1;
end

always @(clk,cnt) begin

        if(clk==0)
          begin
                if ( (cnt<40) && (cnt>34) ) begin a1=1; b1=0; c1=0; d1=0; e1=0; end
            else if ( (cnt<46) && (cnt>39) ) begin a1=0; b1=1; c1=0; d1=0; e1=0; end
             else if ( (cnt<52) && (cnt>45) ) begin a1=0; b1=0; c1=0; d1=0; e1=1; end
             else if ( (cnt<60) && (cnt>51) ) begin a1=0; b1=0; c1=1; d1=0; e1=0; end
             else if ( (cnt<65) && (cnt>59) ) begin a1=0; b1=0; c1=0; d1=1; e1=0; end
           end
end

always @ (posedge clk)  cnt=6'b000000;

endmodule
```

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