Thesis

On

"Design of class-AB level shifted flipped voltage follower cell"

Submitted towards the partial fulfillment of requirement for the award of degree of

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In

VLSI Design

Submitted by:

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DECLARATION

I, Caffey hereby declare that the work presented in this thesis entitled "**Design of class-AB level shifted flipped voltage follower cell**" in partial fulfillment of the requirement for the award of degree of Master of Technology in VLSI Design submitted at Electronics and Communication Engineering Department, Thapar University, Patiala is an authentic record of work carried out under supervision of **Dr. Rishikesh Pandey**, Assistant Professor, ECED, Thapar University from 2015 to 2017. The matter presented in this thesis has not been submitted either in part or full to any other university or institute for the award of any other degree.

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It is certified that the above statement made by the candidate is correct to the best of my knowledge and belief.

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ABSTRACT

The low-voltage/low-power techniques are used as an integral part of the design process for any modern electronic device. To achieve downscaled supply voltage and a resultant low-power operation, an extensive research of such techniques is required. Flipped voltage follower (FVF) is an analog cell that can operate under low supply voltage environment and consumes less power and can be used for designing the analog circuits. With the advantages offered by it, it has presented itself as a promising substitute of other conventional low-voltage/low-power techniques.

The research work includes designing of class-AB level shifted flipped voltage follower (LSVFVF). The level shifter is used to increase the swing of flipped voltage follower. In the proposed circuit bulk-driven MOSFET is used as a current source which improves the sourcing capability and symmetrical slew rate for class-AB operation. The circuit has input/output swing of 1.01 V/0.809 V, wide bandwidth of 750.92 MHz and low output resistance of 106.78 Ω. The applications of the proposed circuit as current sensing cell and differential structure using LSVFVF cell are also presented. The proposed circuits have been designed and simulated in Cadence Virtuoso Analog Design Environment using BSIM3V3 180 nm CMOS technology. The comparison of the proposed LSVFVF with flipped voltage follower cells available in literature shows that the proposed LSVFVF can be used in designing of analog circuits.

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LIST OF ACRONYMS

LV	Low-Voltage
LP	Low-Power
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
FVF	Flipped Voltage Follower
RFID	Radio Frequency Identification
FGMOS	Floating Gate MOSFETs
DC	Direct Current
MIFG	Multi Input Floating Gate
VF	Voltage Follower
DFVF	Differential Flipped Voltage Follower
FVFCS	Flipped Voltage Follower Current Sensor
TL	Translinear Loop
CFDP	Complimentary Flipped Differential Pair
QFG	Quasi Floating Gate
OTA	Operational Transconductance Amplifier
ADC	Analog to Digital Converter
LDO	Low Drop Out
DTMOS	Dynamic Threshold MOS

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CHAPTER 1

INTRODUCTION

Nowadays, design strategies for electronic devices are aimed at achieving higher portability. The need of portability in the devices places restriction on size and power consumption of the battery [1]. If the device needs frequent charging of the battery, consumers will not buy that device and device will exit early from the market. So, the reduction in power consumption is important to maximize the run time of batteries with minimum size and weight allocated to batteries. With the reduction in supply voltages, power consumption can be reduced.

The low-voltage/low-power (LV/LP) techniques are used during the design process to achieve low supply voltage operation which results in low power dissipation [2]. Over the past few years, there has been an increase in the number of portable devices that offer long lasting battery lifetime. Keeping this in mind it can be inferred that various LV/LP techniques are already prevalent in the market. The LV/LP design techniques for low supply voltage operation of analog circuits are sub-threshold MOSFETs [1-6], bulk-driven MOSFETs [1-3, 5-7], self-cascode structures [1-3, 5], floating gate MOSFETs [1-3, 8-9]. However, with scaling down of technology a constant improvement in these techniques is in demand. Flipped voltage follower (FVF) cell overcomes the limitations of the previously mentioned techniques and can operate under low supply voltage [10, 11].

In this chapter conventional LV/LP techniques are discussed. The motivation behind the research work is also presented followed by organization of thesis.

1.1 CONVENTIONAL LV/LP TECHNIQUES

To increase the portability in electronic equipment market, electronic devices are designed to operate at low supply voltage and consume less power. The LV/LP techniques are developed to increase the portability are discussed as follows:

1.1.1 Sub-Threshold MOSFETs

In this technique, the MOSFETs operate in sub-threshold or weak inversion region for gate-to-source voltages (V_{GS}) less than the threshold voltage (V_T). The drain current in this region is due to the diffusion of minority charge carriers because circuits make use of supply voltages less than the threshold voltages of the device [2]. The conduction in the sub-threshold region was considered as a current leakage and was undesirable [12]. However, it has gained prominence as an ultra-low power technique over the past few years.

The reduced supply voltage decreases the power consumption of circuit. The advantage of sub-threshold operation is reduced input-referred noise contribution as compared with the saturation-region. There are various limitations also on the use of sub-threshold MOSFETs. The frequency response of sub-threshold circuits is poor because of the usage of sub-threshold currents. To obtain high gain the device width has to be increased and this limits the speed of operation of the sub-threshold circuits. The sub-threshold approach is best suited for low performance applications, such as RFID tags and wireless sensor nodes, where speed of operation may be compromised.

1.1.2 Bulk - Driven MOSFETs

In MOSFETs the biasing current through its drain is required to perform any signal processing task. In conventional MOSFETs this biasing current flows when gate voltage more than threshold voltage is applied. In bulk-driven MOSFETs, input voltage is applied at bulk terminal and the gate terminal is connected to fixed biasing voltage which helps in forming the conducting channel between source and drain of MOSFET. Due to the availability of this channel the device operates in the depletion-mode. The channel width gets modulated according to the input voltage applied at the bulk terminal and the voltage may be zero, positive or negative. This voltage does not need to overcome the threshold voltage and thus bulk-driven MOSFET can work under low supply voltage [1-3].

The transconductance of bulk-driven MOSFET is smaller than conventional MOSFET. Isolation of bulk terminal is required in bulk-driven technique [5-7]. During fabrication to have isolated bulk terminals different wells are required. This increases the area consumed and results in high capacitance. Therefore, the frequency response is also degraded.

1.1.3 Self - Cascode structures

With the downscaling of CMOS technology, it is possible to utilize the advantages of high density circuits and systems. But with scaling, output impedence decreases due to channel length modulation. This results in low gain of the circuits. To improve the gain, output impedence of the circuits should be increased. The cascoding technique increases the output impedence and thus improves the gain. A limitation associated with cascoding of MOSFETs is the decreased output signal swing. Self-cascoding technique overcomes the limitation of conventional cascoding technique [1-3, 5].

The output impedance can be improved by choosing threshold voltages of first transistor greater than that of second transistor. This can be achieved by multiple threshold technology, which is very expensive.

1.1.4 Floating Gate MOSFETs

The Floating Gate MOSFET (FGMOS), otherwise similar to a conventional MOS transistor, has an additional gate called the floating gate. In FGMOS the polysilicon gate is surrounded by an insulating oxide layer on all sides and is electrically isolated from the rest of the device. As there is no DC path to ground for this polysilicon gate, leaving it floating. The signal inputs are applied to the transistor through an insulating oxide layer deposited on top of the polysilicon layer and connected to polysilicon layer capacitively [1-3]. This oxide layer forms the control gate. When multiple inputs are applied, it is called multi-input floating gate MOSFET (MIFG MOSFET) [8].

Due to the programmability of the threshold voltage of FGMOS devices it can be used in low voltage designs [8, 9]. The problem with the use of FGMOS is charge gets trapped at the floating gate during fabrication. So, FGMOS cannot be fabricated using conventional technology and this increases the cost. The trapped charge also results in large DC offsets. The other disadvantage is FGMOS devices offers low gain because of low output impedence.

1.1.5 Flipped Voltage Follower

The voltage follower (VF) is used to transfer the voltage from the circuit having high output impedence to the circuit having low input impedence. It avoids loading effect. Voltage Follower must have high input impedance, low output impedance, unity voltage gain.

The output impedence of voltage follower is not low enough. To decrease the output impedence, transconductance can be increased. The transconductance can be increased by increasing the aspect ratio of transistor. But this is not acceptable in deep submicron technologies, since the main aim is to reduce the transistor size. Also, the power dissipation will increase with increment in aspect ratio [13]. The current sinking capability of voltage follower is poor due to biasing current source and voltage gain is also less than unity [13].

A modified form of voltage follower known as flipped voltage follower has improved characterstics as it can operate under low supply voltage environment and has low output impedence compared to voltage follower. FVF has large current sinking capability due to the low impedance at the output node [13, 14]. Also, the gain of flipped voltage follower can be altered by scaling aspect ratio of MOSFETs [15]. It is a cascode amplifier with shunt feedback and is called as flipped because it is biased at the drain side. FVF operating at low supply voltage can be used in designing differential pair circuits [16], amplifiers [16] and filters [17]. However, the conventional FVF has limited input/output swing and asymmetrical slew rate (class-A operation) [13]. Several class-AB modifications of the flipped voltage

follower cell have been presented in the literature, which offers different electrical features i.e. large input/output swing and symmetrical slew rate [18-23].

1.2 MOTIVATION

In portable electronic equipment market, to have longer shelf life of batteries, analog and mixed mode electronic devices require designing of analog circuits to operate at low supply voltage levels [2]. The analog circuits are decomposed into several sub circuits which can be called as analog cells. These analog cells are designed to operate at low-voltage, which further reduces the power dissipation of the analog circuit [3]. The low-voltage/low-power analog circuits can be designed by using flipped voltage follower cell (FVF) as an analog cell [10, 11]. FVF being a relatively new LV/LP technique has not been discussed as much in literature as the other prevalent methodologies. FVF offers advantages of low supply voltages, low power dissipation and hence increased device portability. Therefore with further research in this domain this technique will effectively replace the other LV/LP techniques that suffer from significant drawbacks.

Therefore, the motivation behind the research work recorded in this report was to design class-AB flipped voltage follower as a LV/LP analog cell. A comparison of performance parameters of proposed class-AB FVF with FVFs available in literature is done to observe advantages offered by proposed cell.

1.3 ORGANIZATION OF THE THESIS

The organization of thesis is as follows:

Chapter 1 introduces the LV/LP techniques and described advantages offered by flipped voltage follower over the other LV/ LP techniques.

Chapter 2 presents a brief description of the research that has been reported in literature in the field of FVF based analog circuits.

Chapter 3 describes the proposed class-AB level shifted flipped voltage follower and its applications.

Chapter 4 addresses the simulation results of the proposed circuits. The results have been compared with the similar circuits available in literature.

Chapter 5 concludes the report while also mentioning the future possibilities to carry forward the research in this domain.

CHAPTER 2

LITERATURE SURVEY

The chapter discusses the research work which has been carried out on the flipped voltage follower (FVF) cell reported by various authors in the recent years. A succinct review based on the study of papers is as follows:

FVF cell used for designing low-voltage/low-power analog circuits has been identified in [10] which overcome the limitations of conventional source follower. FVF cell operates at low- voltage and can also provide class-AB behaviour. A large variety of applications based on the way the cell is employed such as current mirrors, differential pairs and transconductance operational amplifiers are also discussed.

Torralba *et al.* [24] presented CMOS class-AB buffer which operates under low-power conditions and maintains high slew rate. The class-AB buffer is implemented using differential FVF (DFVF) but it has limited input swing. The input swing is increased by adding DC level shifter in the proposed circuit and by constructing buffer with only PMOS DFVF.

A high speed current sensor based on FVF (FVFCS) used for testing of mixed signal circuits is proposed in [25]. FVFCS has low supply voltage requirement, very low input impedence and can sink large currents. The high gain and high bandwidth is achieved using FVFCS.

FVF based MOS translinear loops (TL) operating at low voltage is reported in [26]. In the conventional low-voltage TL techniques, loop transistors operate in weak inversion region resulting in poor matching characterstics. But, in the proposed technique square law of MOS transistors is exploited in strong inversion and saturation region which overcomes the limitation of conventional techniques. FVF create a low impedence node where the controlled DC reference voltage can be established for the TL loop. The proposed technique can be used to build either static nonlinear computational circuits or dynamic linear and nonlinear circuits. The circuit implementing the square root of input current using MOS TL loop with FVF is also presented.

Lopez-Martin *et al.* [27] presented a current conveyor based on low-voltage/low-power FVF cell. FVF provides it high input impedence, low output impedence, accurate copying of voltage, high speed for a given current consumption. The simulation results show that the proposed current conveyor is better in terms of bandwidth, supply voltage and power consumption as compared to conventional current conveyors. The application demonstrated is universal biquadratic filter which is designed using three CCII+ blocks.

The op-amp with a complimentary flipped differential pair (CFDP) at the input stage is introduced in [16]. The rail-to-rail op-amp operation is achieved using CFDP. The supply voltage requirement is decreased by two drain-source saturation voltages as compare to op-amp with complimentary conventional differential pair. The constant transconductance gain is maintained in the proposed circuit with the use of control circuit based on flipped differential pair.

Angulo *et al*. [18] has modified the conventional voltage follower (VF) and introduced a voltage follower with class-AB operation with no additional power dissipation. The circuit has been designed using quasi-floating gate (QFG) technique. A comparison between the proposed VF and conventional VF has also been reported in which it is observed that QFG based VF offers lower total harmonic distortion and improvement in terms of slew rate and bandwidth as compare to conventional VF.

The flipped voltage follower providing class-AB operation is reported in [19]. The folded version of the proposed circuit to increase the voltage swing has also been presented. The circuits need few extra devices and small increase in power dissipation compared to other class-A and class-AB modifications of FVF cell but have improved sinking and sourcing capability at the output stage. The output voltage is maintained consistently constant with respect to input.

Fayomi [28] suggested FVF based fully differential sample-and-hold circuit. The fully differential operational transconductance amplifier (OTA) is developed using the proposed sample-and-hold circuit, where FVF is used as differential pair at the input stage. The use of FVF at the input stage enables a psuedodifferential class-AB operation and supply power required for the operation of OTA is reduced. The clock signal doubler is used to overcome the limitation of input sampling switches due to low-voltage supply. The applications such as

pipelined, flash and successive approximation ADCs can be designed using the proposed circuit.

The FVF based single-transistor-control low-drop-out (LDO) regulator is discussed in [29]. The proposed LDO is stable for different output capacitors, equivalent series resistances and load currents and offers more stability than conventional LDO. It is discussed that proposed LDO is also stable when there is no output capacitor. The loop bandwidth of the proposed regulator is high for both with capacitor and without capacitor at the output.

Haga and Kale [20] introduced a bulk driven flipped voltage follower. In the proposed circuit, replica-biased bulk-driven MOSFET is used for the input device to remove the DC level shift. Because of class-A type, it has poor sinking capability and cannot drive large loads at high speed. The proposed circuit is modified to class-AB type to overcome the problem of class-A type circuit. The modification improves the sinking capability at the output and the circuit offers advantages in terms of low-power consumption and high-power driving capability. To attain a virtual short between input and output, input current and input capacitance should not be large.

A class-AB buffer which is modified version of flipped voltage follower is proposed in [21]. A comparison between the standard buffer (class-A and class-AB type), conventional FVF buffer (class-A and class-AB type) and proposed class-AB FVF buffer is reported. The proposed buffer has higher slew rate and less setting time than class-A conventional FVF buffer. It offers higher bandwidth, low output impedence, higher linearity than standard class-AB buffers. The proposed FVF shows improvement in output swing compared to standard class-AB buffer and conventional FVF buffer (class-A and class-AB type).

Blakiewicz [30] presented an improved version of FVF and low-dropout voltage regulator as an application of FVF is also presented. The conventional FVF has poor stability for large capacitive loads and poor time response to the output current changing from low to high value. The proposed FVF overcomes the limitation of conventional FVF with small increase in the complexity of circuit and offers better frequency and time responses.

The current comparator circuit is designed using FVF with voltage at the output in [31]. The comparator circuit required small area and less propagation delay. The circuit has rail-to-rail output swing and fast rise and fall time.

Dingcyhan [14] described three different class-A voltage followers. Two of them are conventional source follower and flipped voltage follower. The third voltage follower is the proposed circuit which is the level shifted version of flipped voltage follower. The level shifter technique increases the input and output voltage swing. The proposed circuit offers wide bandwidth and low output resistance. The various performance parameters of the three circuits and compared and proposed follower is found to be suitable for low voltage applications.

FVF based current mirror (FVF) current mirror using Dynamic Threshold MOS (DTMOS) technique is presented in [32]. The supply voltage and threshold voltage is lowered due to the use of body effect. Three different structures have been reported to show the effect of DTMOS technique in conventional FVF current mirror and one of them is found to be suitable for low-voltage applications. But the fabrication of DTMOS is difficult.

Haga [33] presented a voltage follower that operates at low supply voltage. The quasi-floating gate (QFG) and bulk-driven technique are used in the proposed circuit which allows the circuit to operate under low supply voltage environment.

A capacitor-free low-dropout voltage regulator based on FVF which uses digital detecting technique is proposed in [34]. This technique replaced large capacitors and resistors used for transient coupling. The digital detection circuit consumes less power and is small. In the proposed circuit slew rate has been increased at the gate of power transistor by detecting the dynamic changes inside the circuit. Load-transient recovery time is decreased and fast-transient response is obtained.

Molinar-Solis et al. [22] presented a bulk-driven configuration of flipped voltage follower. The proposed circuit does not need any additional devices and is a modified version of conventional FVF where current source is replaced by bulk-driven transistor to achieve class-AB operation. A symmetrical slew rate and increased current sourcing capability is achieved with the use of proposed circuit.

FVF based voltage adder is reported in [35]. The adder is used as a basic building block to design analog multiplier. The biasing and signalling of multiplier has been done by using four such adders. The percentage of distortion is less due to the presence of undesired harmonics. The application of the proposed circuit as a amplitude modulator has also been presented.

Centurelli et al. [23] proposed class-AB flipped voltage follower. The proposed topology is similar to [21], but to avoid an additional pole, common-gate auxiliary amplifier is used. The resulting circuit shows linear behaviour for large signal swings and better frequency response, enables faster settling time, consumes less power and has improved phase margin.

CHAPTER 3

PROPOSED CLASS-AB LEVEL SHIFTED FLIPPED VOLTAGE FOLLOWER CELL

In this chapter level shifted version of flipped voltage follower (LSVFVF) is proposed. Section 3.1 discusses description of the proposed circuit. Analysis of the circuit is presented in section 3.2. In section 3.3 applications of proposed LSVFVF are discussed.

3.1 CIRCUIT DESCRIPTION

The conventional FVF and proposed level shifted version of conventional FVF cell (LSVFVF) are shown in Figures 3.1 and 3.2, respectively. The constant current source I_B used for biasing in the conventional FVF cell is implemented by transistor M_3 with its bulk terminal connected to drain end as an adaptable current source in the proposed circuit. The input (V_{IN}) is applied at the gate terminal and output (V_O) is drawn from the source terminal of transistor M_2. In the feedback path, transistor M_4 connected between the gate of transistor M_1 and drain of transistor M_2 is used as a level shifter. The bias voltage (V_{BIAS}) at gate terminal of transistor M_3 adjusts gate-source voltage of transistor M_3 (V_{GSM3}) and it results in constant bias current in the branch M_1-M_3. The voltage variations at node 'X' are transferred to node 'Y' through transistor M_4. Consider, if input voltage (V_{IN}) increases sharply causing decrement in voltages V_X and V_Y. The decrement in voltage V_X increases the source-bulk voltage of transistor M_3 (V_{SBM3}) that allows transistor M_3 to provide a higher current, which results very large sourcing current in capacitive load C_L. The decrement in voltage V_Y reduces the gate-source voltage (V_{GSM1}) which turns off transistor M_1. Further, when input voltage (V_{IN}) decreases, the voltages V_X and V_Y increases. This increases the current in transistor M_1, resulting in a large sinking output current in capacitive load C_L. In Figure 3.2, the dotted line is used when body effect is not considered for the transistor M_2.

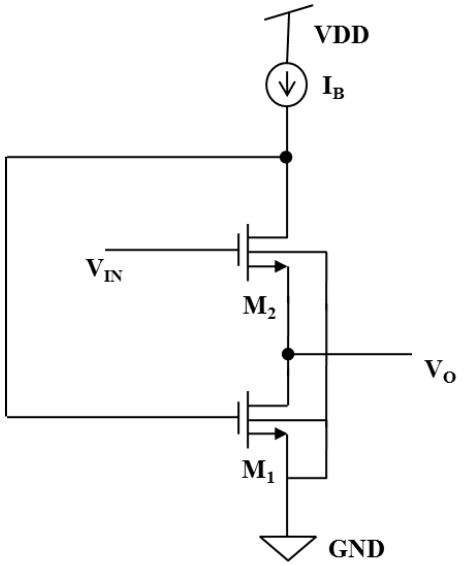

Figure 3.1 Conventional FVF [13]

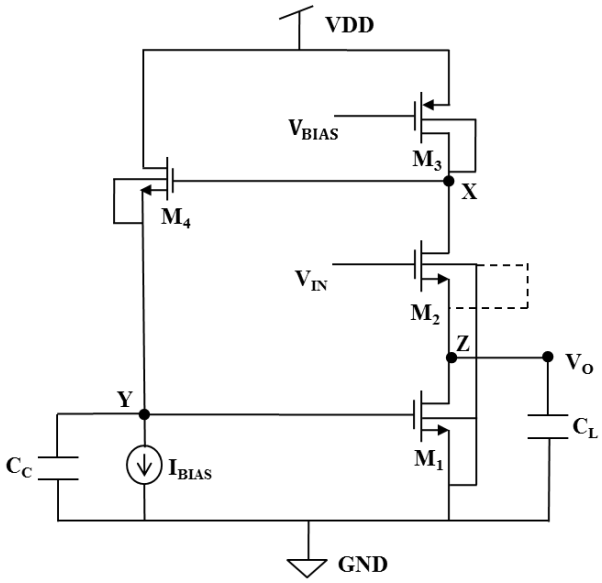

Figure 3.2 Proposed Level shifted version of class-AB FVF (LSVFVF)

3.2 ANALYSIS OF LSVFVF

3.2.1 DC Analysis

DC analysis is performed by assuming the circuit under DC equilibrium conditions. As transistor M_3 used as a current source it is kept in the saturation region. To keep transistors M_1, M_2 and M_4 in saturation region, their drain-source voltages must follow the condition given as

$$V_{DSM1,2,4} \geq V_{DSsatM1,2,4} \text{ and } V_{DSsatM1,2,4} = V_{GSM1,2,4} - V_T \quad (3.1)$$

where V_T is the threshold voltage.

Using equation (3.1), the boundary condition for output voltage (V_O) can be obtained as

$$V_O \leq V_X - V_{DSsatM2} \quad (3.2)$$

$$V_O \geq V_{DSsatM1} + V_Y - V_{GSM1} \quad (3.3)$$

Using equations (3.2) and (3.3), the output voltage (V_O) is bounded as

$$V_{DSsatM1} + V_Y - V_{GSM1} \leq V_O \leq V_X - V_{DSsatM2} \quad (3.4)$$

Using equation (3.1), the drain-source voltage of transistor M_4 in saturation condition can be written as

$$V_{DSsatM4} = V_X - V_Y - V_{TM4} \quad (3.5)$$

Using equations (3.4) and (3.5), swing at the output node (V_{OSW}) is calculated as

$$V_{OSW} = V_{DSsatM4} + V_{TM4} + V_{GSM1} - V_{DSsatM1} - V_{DSsatM2} \quad (3.6)$$

From equation (3.6), it is clear that swing at the output node can be increased if $V_{DSsatM1, 2}$ is as small as possible. To lower the value $V_{DSsatM1, 2}$, the gate-source voltages of $M_{1, 2}$ ($V_{GSM1, 2}$) should be minimum, but it must follow the condition ($V_{GS} > V_T + \eta kT/q$ where η is in the range $1 \leq \eta \leq 3$ and kT/q is the thermal voltage at room temperature $\approx$ 26mV) given in [36] to avoid weak inversion region. For the worst case η =3 has been chosen for the design of the proposed circuit and hence, the minimum value of $V_{GS} - V_T$ has been obtained as 100 mV.

Using equations (3.1) and (3.5), the upper bound for input voltage (V_{IN}) is given as

$$V_{IN} \leq V_{GSM4} + V_{DSsatM1} + V_{TM1} + V_{TM2} \quad (3.7)$$

The lower bound for input voltage (V_{IN}) is given as

$$V_{IN} \geq V_O + V_{TM2} \text{ or } V_{IN} \geq V_{DSsatM1} + V_{TM2} \quad (3.8)$$

where $V_{DSM1} = V_O \geq V_{DSsatM1}$

Using equations (3.7) and (3.8), the boundary condition for input voltage (V_{IN}) can be written as

$$V_{DSsatM1} + V_{TM2} \leq V_{IN} \leq V_{GSM4} + V_{DSsatM1} + V_{TM1} + V_{TM2} \quad (3.9)$$

The swing at the input node (V_{ISW}) is calculated as

$$V_{ISW} = V_{GSM4} + V_{TM1} \quad (3.10)$$

Due to body effect, threshold voltage of transistor M_2 is considered as $V_{TM2} \approx 1.2\ V_{ToM2}$ [22]. The minimum power supply voltage requirement of the proposed circuit can be calculated as

$$V_{DD(min)} = V_{DSsatM1} + V_{TM1} + V_{TM2} \quad (3.11)$$

3.2.2 AC analysis

AC analysis of the proposed circuit is performed and the small signal gain (A_V), output resistance (r_o') and open loop gain (A_{OL}) are calculated by using small signal model of the proposed circuit.

3.2.2.1 *Gain (A_V)*

The small signal model of the proposed LSVFVF is shown in Figure 3.3.The gain (A_V) of the LSVFVF can be calculated by applying KCL at node D_{M1} as

$$g_{mM2}\,(V_{in} - V_o) - g_{mbM2}\,V_o + \frac{V_{GM4} - V_o}{r_{oM2}} = g_{mM1}\,g_{mM4}\,V_{GSM4}\,r_{oM4} + \frac{V_o}{r_{oM1}} + \frac{V_o}{R_D} \qquad (3.12)$$

where $g_{mM1,\,2\,,4}$ are the transconductances of transistors $M_{1,\,2,\,4}$, g_{mbM2} is the transconductance due to body effect of transistor M_2 and r_{oM4} is the output resistance of transistor M_4.

Substituting the value of $V_{GSM4} = \frac{V_{GM4}}{1+g_{mM4}r_{oM4}}$ in equation (3.12), we get

$$g_{mM2}V_{in} + V_{GM4}\left(\frac{1}{r_{oM2}} - \frac{g_{mM1}g_{mM4}r_{oM4}}{1+g_{mM4}r_{oM4}}\right) = V_o\left(\frac{1}{r_{oM1}} + \frac{1}{r_{oM2}} + \frac{1}{R_D} + g_{mM2} + g_{mbM2}\right) \qquad (3.13)$$

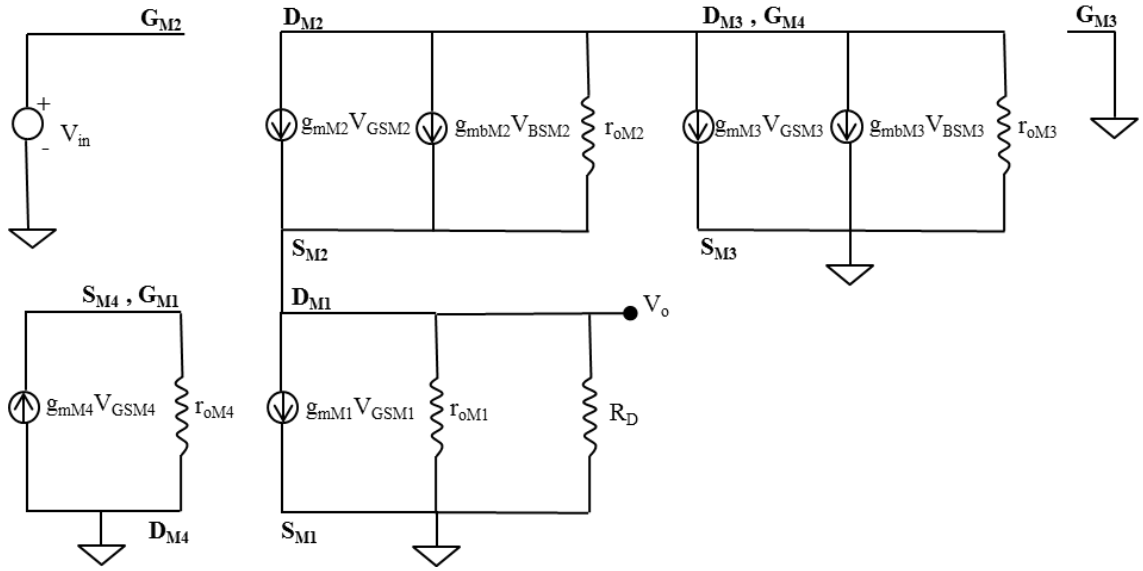

Figure 3.3 Small signal model of proposed LSVFVF

Using approximation $g_m r_o >> 1$, equation (3.13) is modified as

$$g_{mM2}V_{in} + V_{GM4}\left(-\frac{g_{mM1}g_{mM4}r_{oM4}}{1+g_{mM4}r_{oM4}}\right) = V_o\left(\frac{1}{R_D} + g_{mM2} + g_{mbM2}\right) \qquad (3.14)$$

Now, Applying KCL at node D_{M3}, we get

$$g_{mM2}\,(V_{in} - V_o) - g_{mbM2}\,V_o + \frac{V_{GM4} - V_o}{r_{oM2}} = -g_{mbM3}\,V_{GM4} - \frac{V_{GM4}}{r_{oM3}} \qquad (3.15)$$

Using approximation $g_m r_o >> 1$, equation (3.15) is modified as

$$V_{GM4} = \frac{V_o\,(g_{mM2}+g_{mbM2})-V_{in}\,g_{mM2}}{g_{mbM3}} \quad (3.16)$$

Using equations (3.14) and (3.16), the gain of LSVFVF circuit is given as

$$A_V = \frac{V_o}{V_{in}} = \frac{g_{mM2}}{(g_{mM2}+g_{mbM2})} \quad (3.17)$$

3.2.2.2 *Output resistance (r_o')*

The output resistance (r_o') of the proposed LSVFVF is calculated by assuming that the gate terminal of transistor M_2 is connected at ground potential and a voltage source (V_o) is connected at the output terminal, which supplies current I_o in Figure 3.3.

Applying KCL at node D_{M1}, we get:

$$g_{mM2}\,(-V_o) - g_{mbM2}\,V_o + \frac{V_{GM4}-V_o}{r_{oM2}} = g_{mM1}\,g_{mM4}\,V_{GSM4}\,r_{oM4} + \frac{V_o}{r_{oM1}} + I_o \quad (3.18)$$

Substituting the value of $V_{GSM4} = \frac{V_{GM4}}{1+g_{mM4}r_{oM4}}$, equation (3.18) can be written as

$$V_o\left(g_{mM2} + g_{mbM2} + \frac{1}{r_{oM1}} + \frac{1}{r_{oM2}}\right) = I_o - V_{GM4}\left(\frac{1}{r_{oM2}} - \frac{g_{mM1}g_{mM4}r_{oM4}}{1+g_{mM4}r_{oM4}}\right) \quad (3.19)$$

Using approximation $g_m r_o >> 1$, equation (3.19) is modified as

$$V_o(g_{mM2} + g_{mbM2}) = I_o - V_{GM4}\left(-\frac{g_{mM1}g_{mM4}r_{oM4}}{1+g_{mM4}r_{oM4}}\right) \quad (3.20)$$

Now, Applying KCL at node D_{M3}, we get

$$g_{mM2}\,(-V_o) - g_{mbM2}\,V_o + \frac{V_{GM4}-V_o}{r_{oM2}} = -g_{mbM3}\,V_{GM4} - \frac{V_{GM4}}{r_{oM3}} \quad (3.21)$$

Assuming $g_m r_o >> 1$, equation (3.21) is modified as

$$V_{GM4} = \frac{V_o\,(g_{mM2}+g_{mbM2})}{g_{mbM3}} \quad (3.22)$$

Using equations (3.20) and (3.22), the output resistance is given as

$$r_o' = \frac{g_{mbM3}(1+g_{M4}r_{oM4})}{(g_{M2}+g_{mbM2})(g_{M1}g_{M4}r_{oM4}+g_{mbM3}+g_{mbM3}g_{M4}r_{oM4})} \quad (3.23)$$

3.2.2.3 *Open loop voltage gain (A_{OL})*

To calculate the open loop voltage gain (A_{OL}) the small signal model is redrawn as shown in Figure 3.4, where input voltage source V_Y is connected at the gate terminal of transistor M_1 and open loop voltage is taken at the drain of transistor M_2 (V_X).

Applying KCL at node D_{M1}, we get

$$g_{mM2}\,(-V_R) - g_{mbM2}\,V_R + \frac{V_X-V_R}{r_{oM2}} = g_{mM1}\,V_Y + \frac{V_R}{r_{oM1}} \quad (3.24)$$

Using approximation $g_m r_o >> 1$, equation (3.24) is modified as

$$\frac{V_R}{V_Y} = -\left(\frac{g_{mM1}}{g_{mM2}+g_{mbM2}}\right) \quad (3.25)$$

Applying KCL at node D_{M3}, we get

$$g_{mM2}(-V_R) - g_{mbM2}V_R + \frac{V_X - V_R}{r_{oM2}} = -g_{mbM3}V_X - \frac{V_X}{r_{oM3}} \quad (3.26)$$

Using approximation $g_m r_o >> 1$, equation (3.26) is simplified as

$$\frac{V_R}{V_X} = \frac{g_{mbM3}}{g_{mM2}+g_{mbM2}} \quad (3.27)$$

Hence, using equations (3.25) and (3.27) open loop gain (A_{OL}) can be written as

$$|A_{OL}| = \frac{g_{mM1}}{g_{mbM3}} \quad (3.28)$$

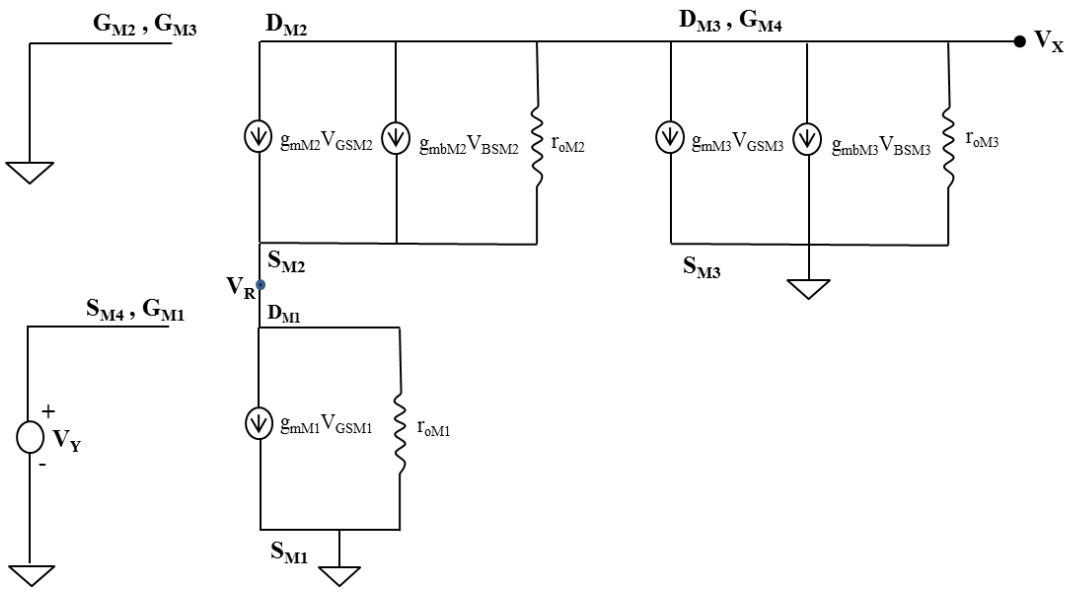

Figure 3.4 Small signal model of proposed LSVFVF to calculate open loop voltage gain

Suppose body and source of M_2 are at the same potential (shown in the Figure 3.1 using dotted line) then V_{SB}=0. Substituting g_{mbM2}=0 in equations (3.17), (3.23) and (3.28), the gain (A_V), output resistance (r_o') and open loop voltage gain (A_{OL}) are modified as

$$A_V = \frac{V_o}{V_{in}} = \frac{g_{mM2}}{g_{mM2}} = 1 \quad (3.29)$$

$$r_o' = \frac{g_{mbM3}(1+g_{M4}r_{oM4})}{g_{M2}(g_{M1}g_{M4}r_{oM4}+g_{mbM3}+g_{mbM3}g_{M4}r_{oM4})} \quad (3.30)$$

$$|A_{OL}| = \frac{g_{mM1}}{g_{mbM3}} \quad (3.31)$$

3.2.3 Stability analysis

The two poles of the proposed circuit at nodes ‘X’ and ‘Z’ are given as

$$w_X = g_{mbM3}/C_X \quad (3.32)$$

$$w_Z = g_{mM2}/C_L \quad (3.33)$$

where C_X includes the parasitic capacitances due to transistor M_4 and compensation capacitor C_C and C_L is the load capacitance.

For small capacitive loads i.e. $C_L \leq 20$ pF, pole at node 'X' (w_X) is dominant and pole at node 'Z' (w_Z) is non-dominant. Using equations (3.28) and (3.32), the gain bandwidth product (GBW) is given as

$$GBW = g_{mM1}/C_X \tag{3.34}$$

The condition $w_Z \geq GBW$ ensures the phase margin of atleast 45° [2]. Using equations (3.33) and (3.34), stability condition can be derived as

$$C_L \leq (g_{mM2}/g_{mM1})C_x \tag{3.35}$$

Now, for large capacitive loads i.e. $C_L \geq 20$ pF, pole at node 'Z' (w_Z) is dominant and pole at node 'X' (w_X) is non-dominant. Using equations (3.28) and (3.33), the gain bandwidth product (GBW) is given as

$$GBW = (g_{mM1}g_{mM2})/(g_{mbM3}C_L) \tag{3.36}$$

Using equations (3.32) and (3.36), stability condition can be derived as

$$C_L \geq (g_{mM1}g_{mM2}/g_{mbM3}^2)C_x \tag{3.37}$$

For the proposed circuit we have considered the value of C_L less than 20 pF which ensure the stability condition given in equation (3.35).

3.3 APPLICATIONS OF PROPOSED LSVFVF

3.3.1 Current sensor based on proposed LSVFVF

Current sensing cell shown in Figure 3.5 is realized using proposed LSVFVF. All the transistors are biased in the saturation region. The input current (I_{IN}) is applied at node 'Z' and this node is called as current sensing node. The impedence at node 'Z' is low due to the presence of shunt feedback. Therefore, the voltage at current sensing node does not change and it can source large variations in input current. The LSVFVF transfers the input current variations at node 'Z' to voltage variations at node 'Y'. The input current is replicated by transistor M_5 using voltage at node 'Y'.

The output current (I_O) is measured at drain of transistor M_5. The relation between output and input current is obtained as

$$I_O = I_{IN} + I_B \tag{3.38}$$

where I_B is the current flowing through the bulk-driven transistor M_3.

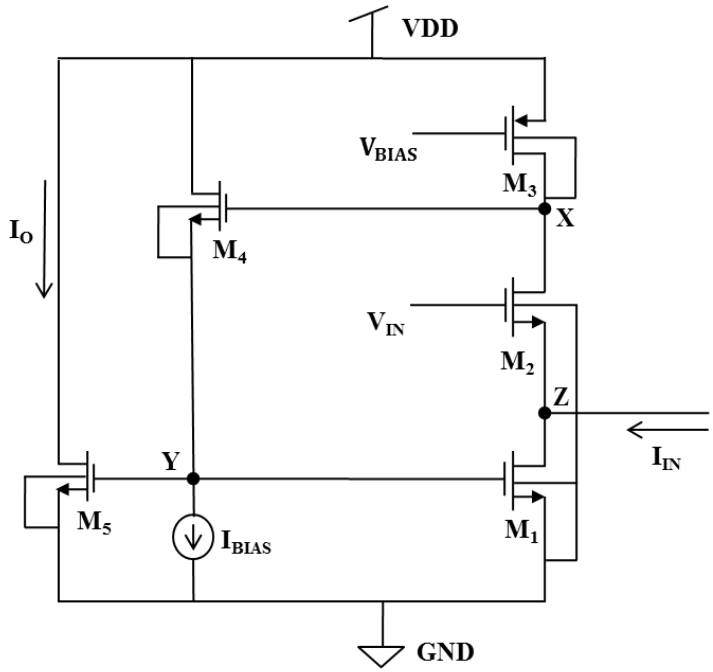

Figure 3.5 Current sensor based on proposed LSVFVF

3.3.2 Differential structure using proposed LSVFVF

The differential structure using proposed LSVFVF cell shown in Figure 3.6 is realized by adding the source terminal of transistor M_5 at node 'Z' operating in saturation region. The output impedence is low due to shunt feedback at node 'Z'. Therefore, for large currents flowing through transistor M_5, the voltage at node 'Z' remains constant. The bias voltage (V_B) and input voltage (V_{IN}) are applied at gates of transistors M_5 and M_2, respectively.

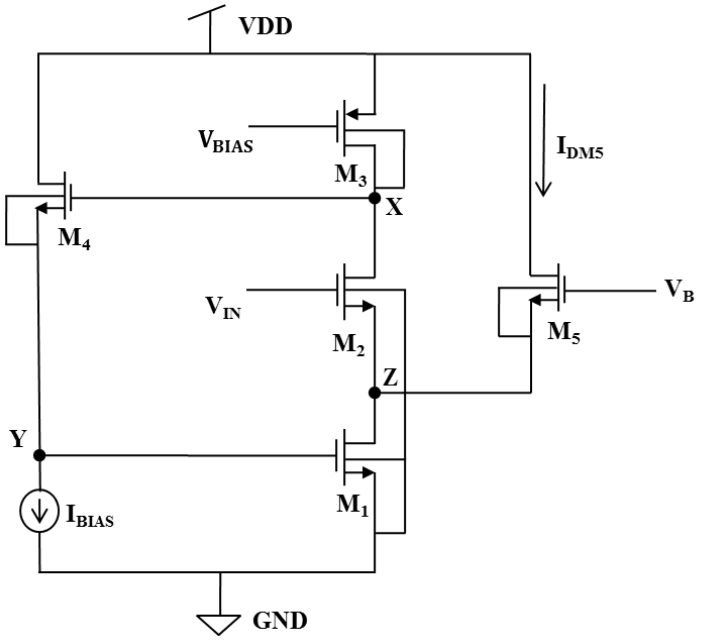

Figure 3.6 Differential structure using proposed LSVFVF

If $V_{IN} = V_B$ and aspect ratios of both the transistors are equal then the drain currents flowing through the transistors M_2 and M_5 are given as

$$I_{DM2} = I_{DM5} = I_B \quad (3.39)$$

where I_B is the current flowing through the bulk-driven transistor M_3.

If $V_{IN} \neq V_B$ then difference of voltages $(V_{IN} - V_B)$ generates current variations in transistor M_5 and the increase in current follows the MOS square law.

The characteristic of differential structure using proposed LSVFVF cell is that the output is available as both current through transistor M_5 and voltage at node 'X' and output current can be larger than biasing current I_B.

CHAPTER 4

SIMULATION RESULTS

The proposed circuit is designed and simulated in Cadence Virtuoso Analog Design Environment using BSIM3V3 180 nm CMOS technology.

Using the drain current equation of saturation region, the voltages $V_{DSsatM1}$, $V_{DSsatM2}$ and $V_{DSsatM4}$ are obtained as 82 mV, 88mV and 83 mV respectively. But in section 3.2.1, we have already discussed that the minimum value of V_{DSsat} should be atleast 100 mV. Therefore, $V_{DSsatM1,2,4}$ = 100 mV has been chosen for the design of proposed circuit. Due to body effect, the threshold voltage of transistor M_2 (V_{ToM2}) is obtained as 0.585 V and without body effect the threshold voltage of transistor M_2 (V_{TM2}) is obtained as 0.48 V. Therefore the value of V_{TM2} is obtained as 1.2 times $V_{ToM2,}$ which we have already considered in section 3.2.1. The minimum value of the required supply voltage is calculated using equation (3.11) as 1.175 V and hence, 1.2 V is decided to use as a supply voltage for the proposed circuit. Using equations (3.6) and (3.10), the output swing (V_{OSW}) and input swing (V_{ISW}) are calculated as 0.96 V and 1.06 V respectively. Also, the small signal gain is calculated as 0.805 using equation (3.17).

The DC transfer characterstics of the proposed circuit is shown in Figure 4.1 for the input voltage (V_{IN}) in the range of $0 \leq V_{IN} \leq 3$ V. From Figure 4.1, the output voltage swing (V_{OSW}) and the input voltage swing (V_{ISW}) are observed as 0.80 V and 1.01 V, respectively. The value of V_{OSW} and V_{ISW} show good agreement with the calculated values. The DC transfer characterstics of the proposed circuit without body effect is shown in Figure 4.2. From Figure 4.2, the output voltage swing (V_{OSW}) and the input voltage swing (V_{ISW}) are observed as 0.826 V and 0.84 V, respectively. Figure 4.3 shows the DC transfer characterstics of the circuit when I_{BIAS} is replaced by MOSFET. From Figure 4.3, the output voltage swing (V_{OSW}) and the input voltage swing (V_{ISW}) are observed as 0.820 V and 1.028 V, respectively.

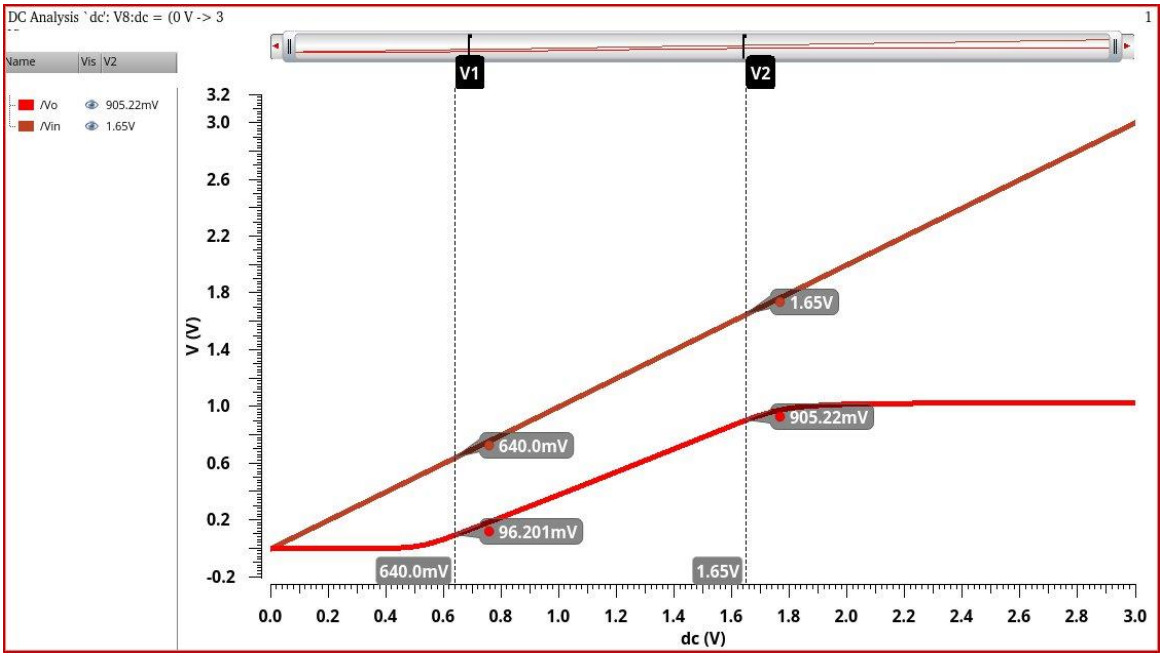

Figure 4.1 DC transfer characterstics of proposed LSVFVF (with body effect)

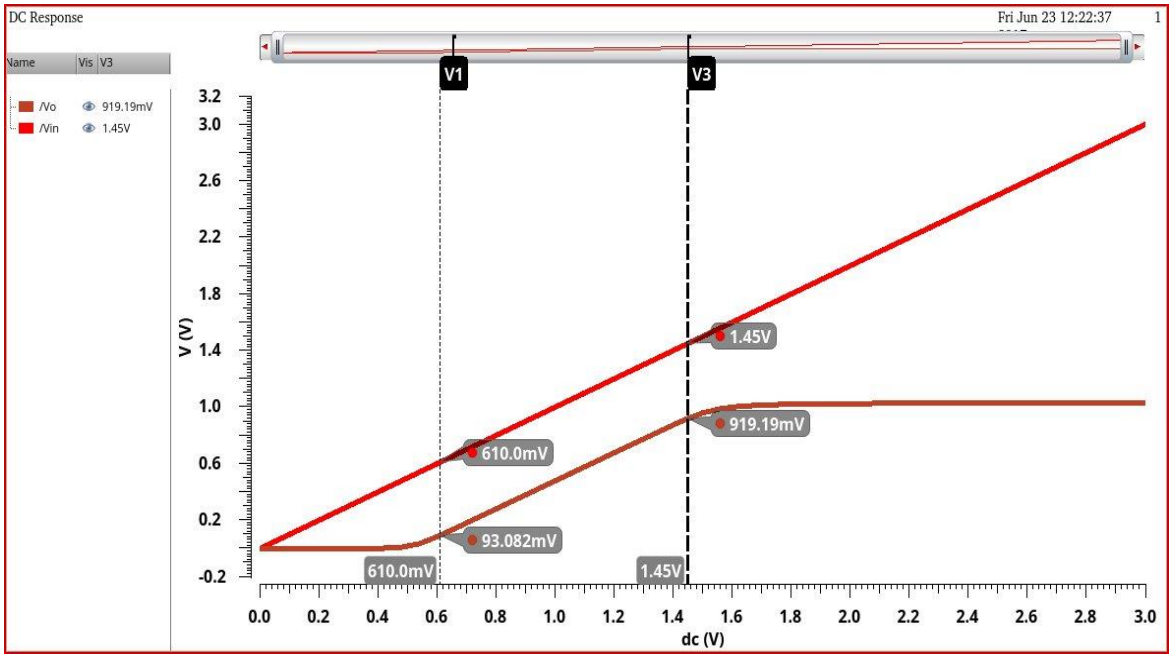

Figure 4.2 DC transfer characterstics of proposed LSVFVF (without body effect)

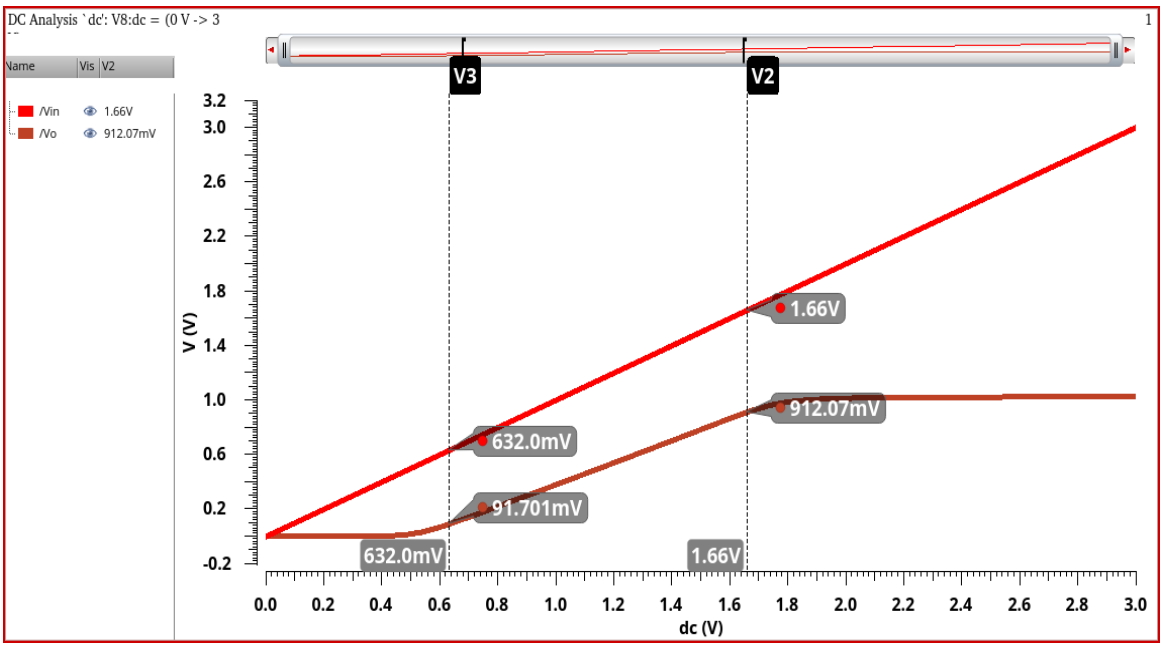

Figure 4.3 DC transfer characterstics of proposed LSVFVF (I_{BIAS} is replaced by MOSFET)

The AC analysis of the proposed circuit has been performed with small signal AC magnitude of 300 mV with dc offset voltage of 1 V. From the frequency response shown in Figure 4.4, the small signal gain (Av) is observed as 0.80 and the bandwidth is 750.92 MHz for C_L=1pF. The frequency response of the proposed circuit without body effect is shown in Figure 4.5. From the plot, the small signal gain (Av) and the bandwidth are obtained as 0.99 and 685.97 MHz, respectively for C_L=1pF. The values of small signal gain with body effect and without body effect show a good agreement with the calculated values. The frequency response of the proposed circuit when I_{BIAS} is replaced by MOSFET is shown in Figure 4.6. From the plot, the small signal gain (Av) and the bandwidth are obtained as 0.8 and 490.60 MHz, respectively for C_L=1pF.

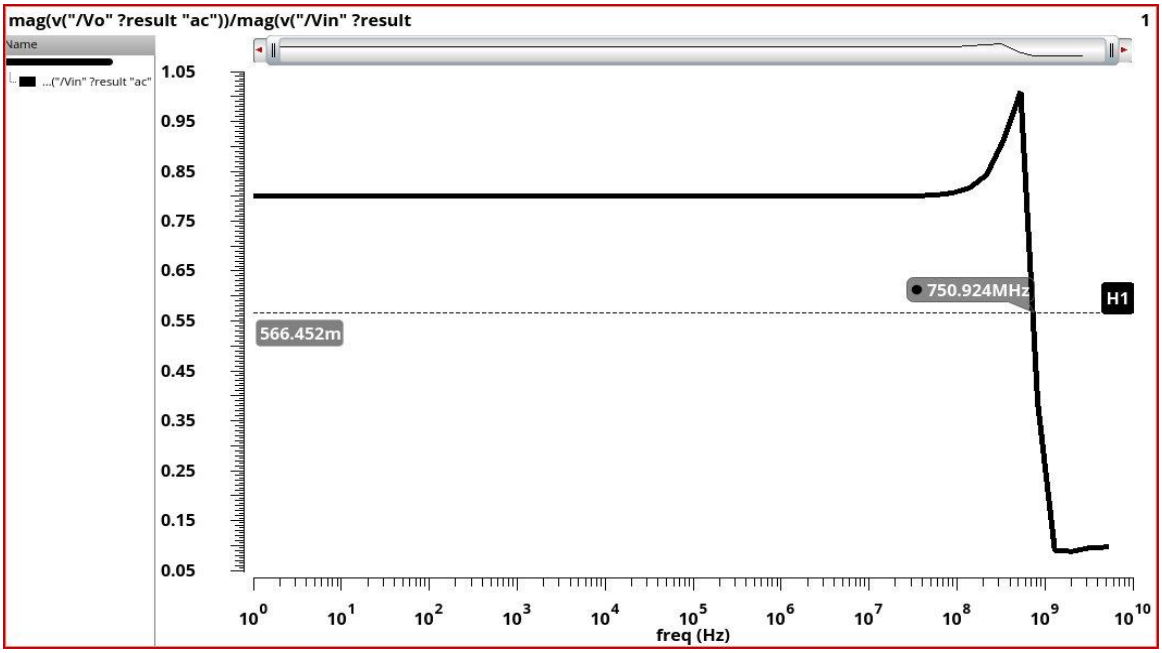

Figure 4.4 Frequency response of proposed LSVFVF (with body effect)

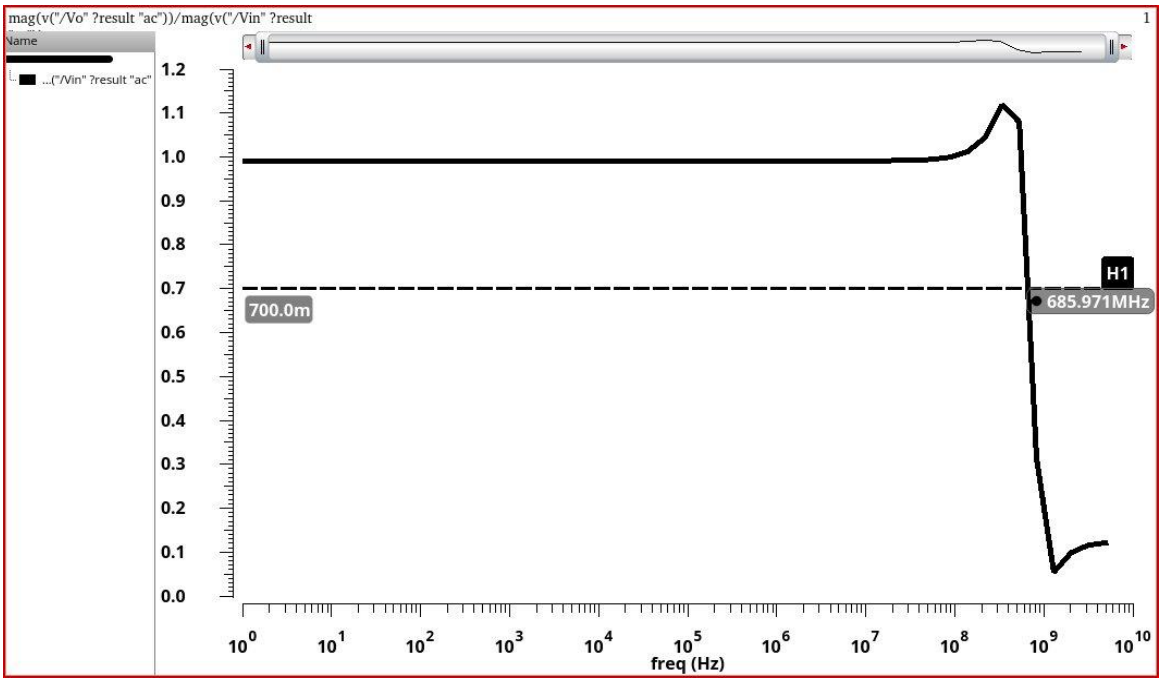

Figure 4.5 Frequency response of proposed LSVFVF (without body effect)

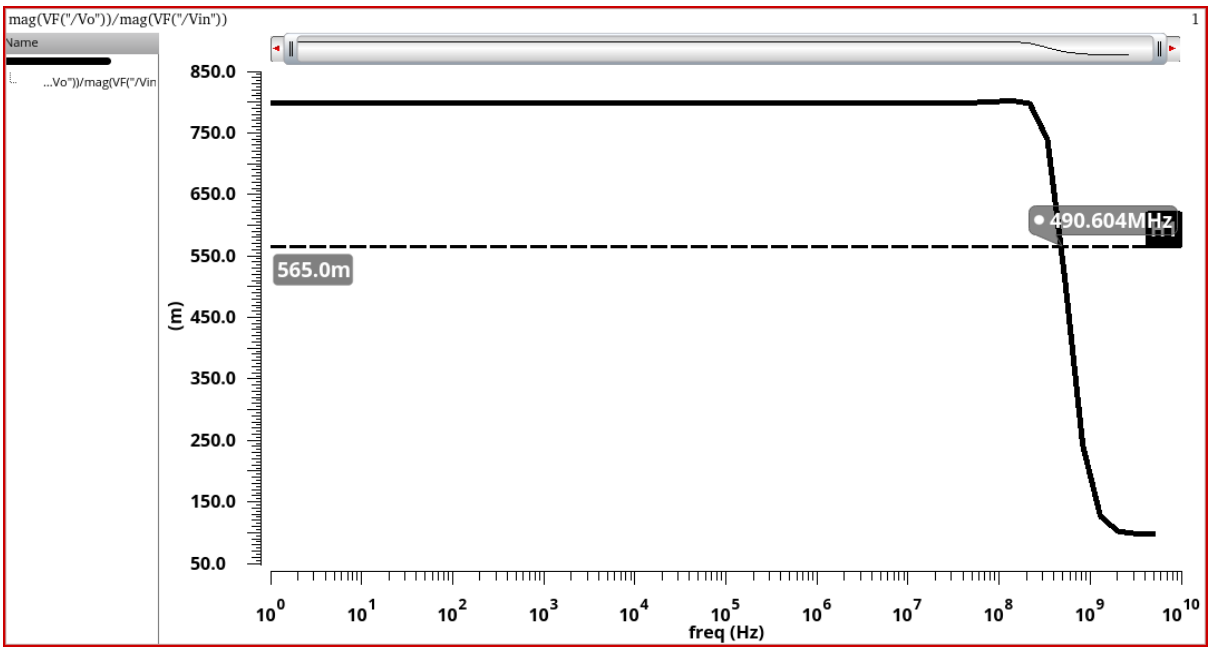

Figure 4.6 Frequency response of proposed LSVFVF (I_{BIAS} is replaced by MOSFET)

Figure 4.7 shows the transient response of the proposed circuit for which a square input pulse of 300 mV (Vpeak) with offset voltage of 1 V at 1MHz is applied. The load capacitance (C_L) is selected as 15 pF. From Figure 4.7, it is observed that output voltage (Vo) exactly follows the input voltage (V_{IN}). The symmetrical slew rate is calculated as SR^+ = 31.58 V/µsec and SR^- = 27.9 V/µsec whereas asymmetrical slew rate of conventional FVF is $SR^+ = I_B/C_L \approx 4.33$ V/µsec. Figure 4.8 shows the sourcing and sinking output current capability and the sourcing and sinking capabilities on rising and falling transitions of input signal are observed as 15.2 I_B and 6.9 I_B respectively. Figures 4.9 and 4.10 show the transient response and the current sourcing and sinking capabilities on rising and falling transitions of input signal of the proposed circuit without body effect, respectively for capacitive load C_L=1pF. The transient response and the current sourcing and sinking capabilities on rising and falling transitions of input signal of the proposed circuit when I_{BIAS} is replaced by MOSFET for capacitive load C_L=15pF are shown in Figures 4.11 and 4.12, respectively.

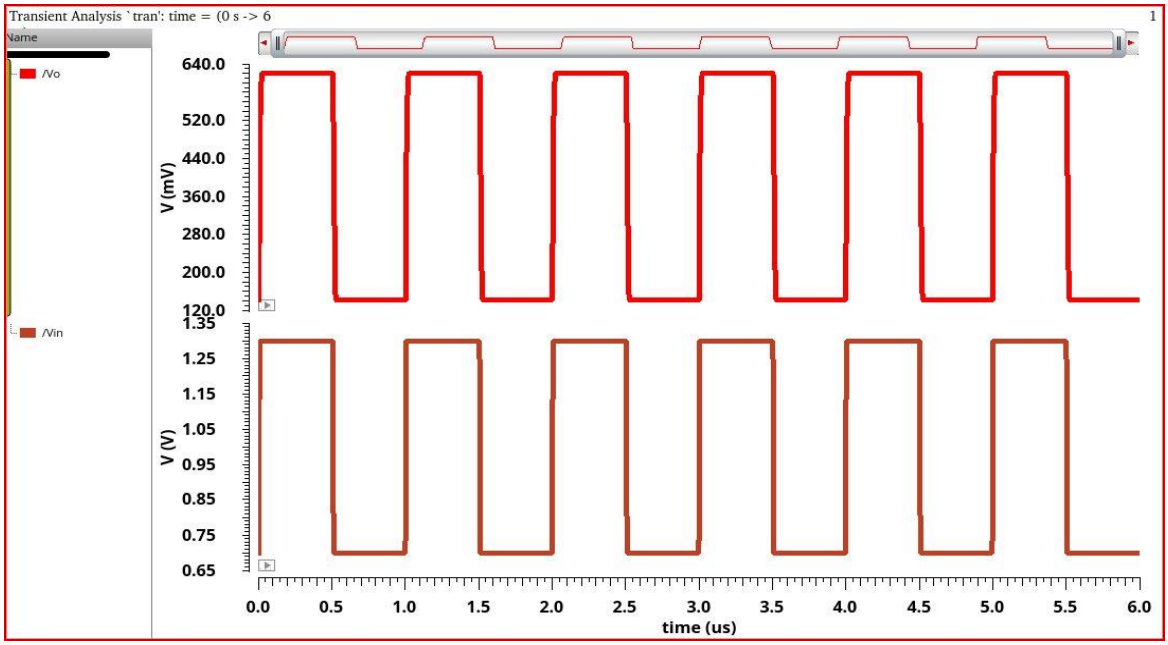

Figure 4.7 Transient response of proposed LSVFVF (with body effect)

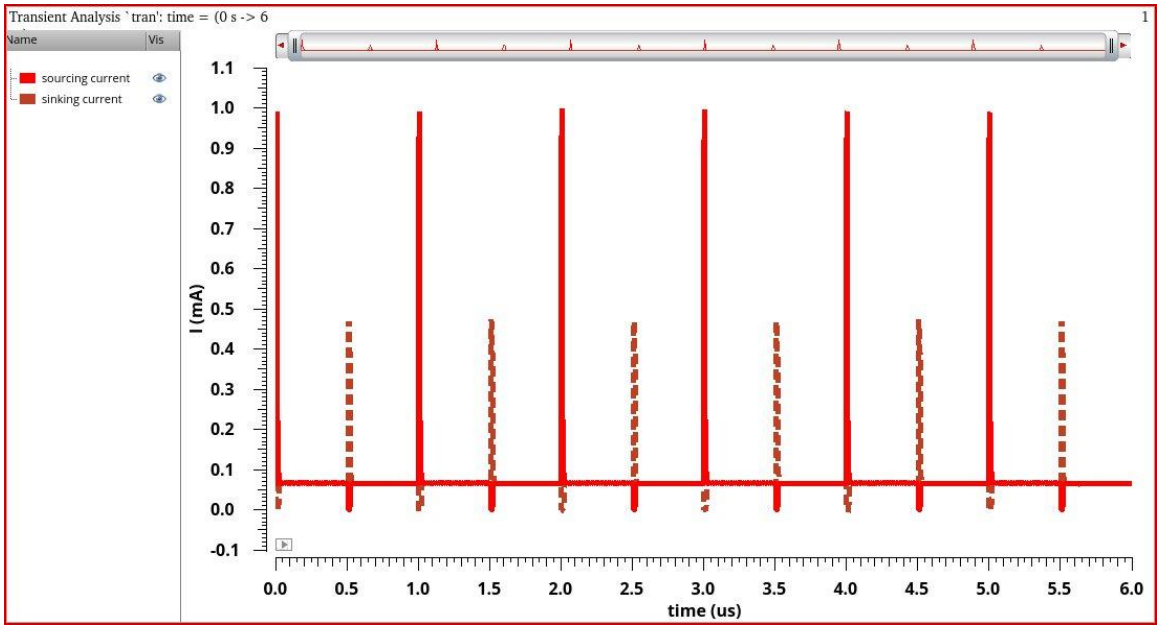

Figure 4.8 Sourcing and sinking output current capability (with body effect) for capacitive load C_L=15pF

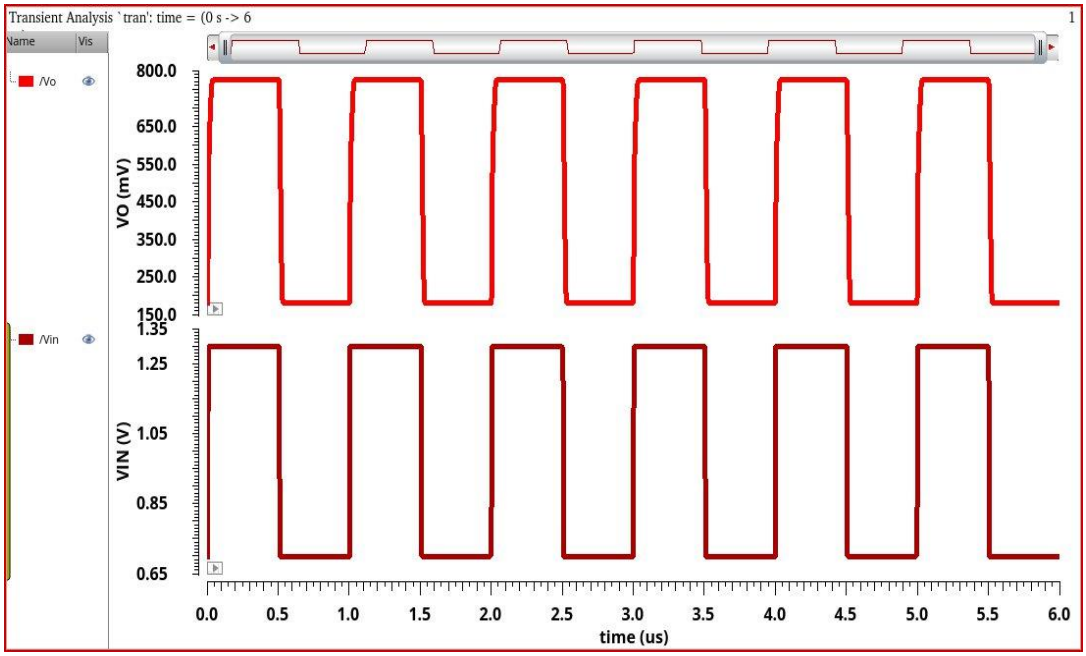

Figure 4.9 Transient response of proposed LSVFVF (without body effect)

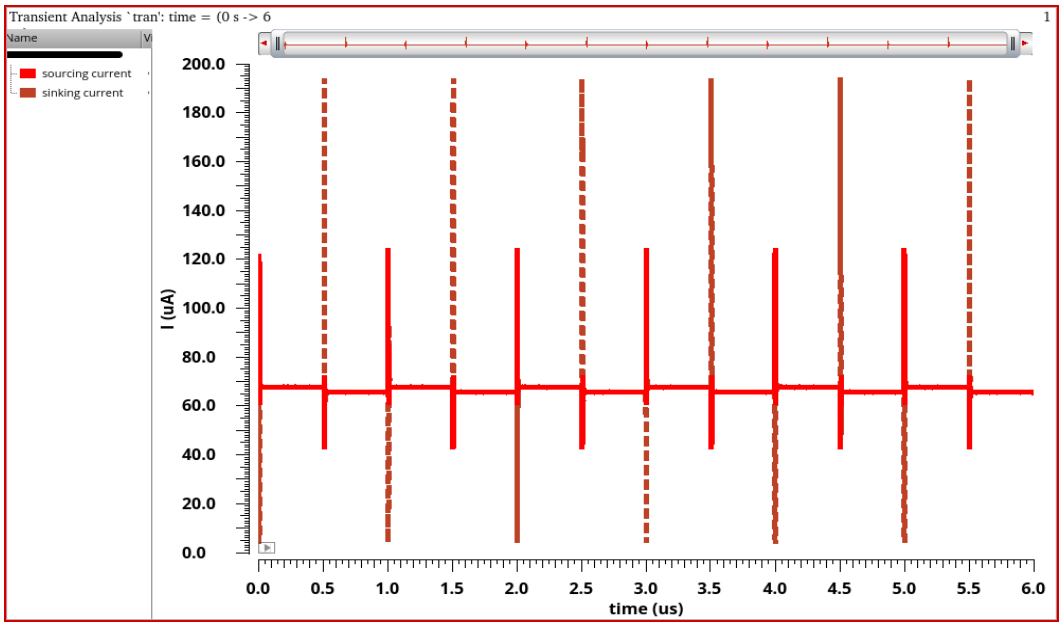

Figure 4.10 Sourcing and sinking output current capability (without body effect) for capacitive load C_L=1pF

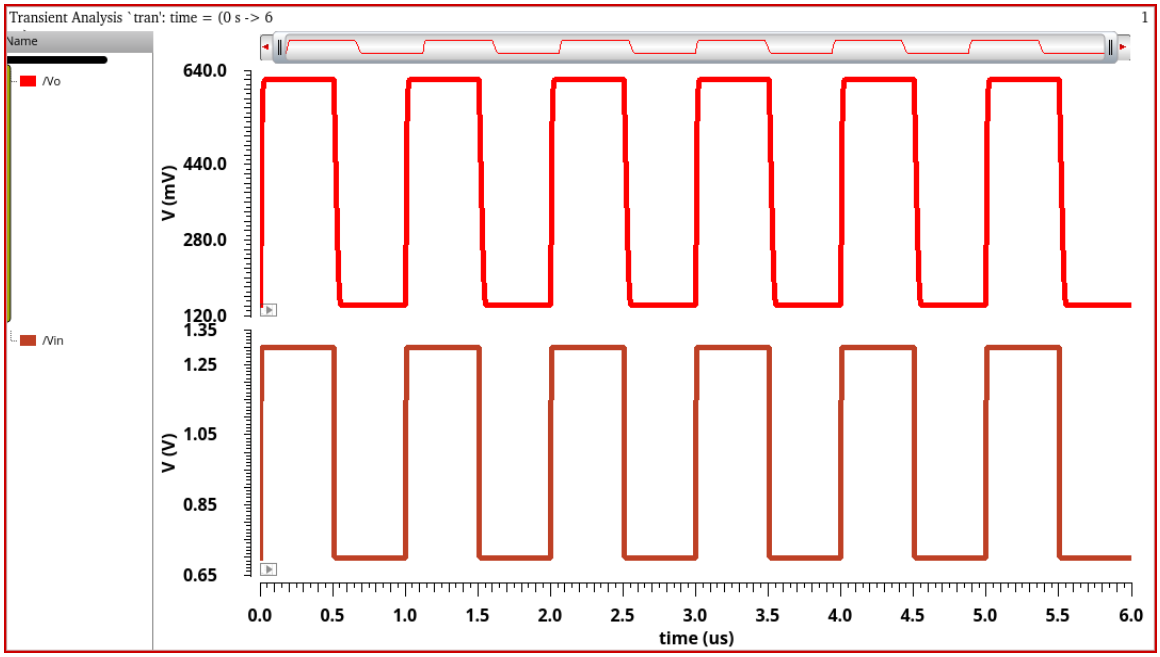

Figure 4.11 Transient response of proposed LSVFVF (I_{BIAS} is replaced by MOSFET)

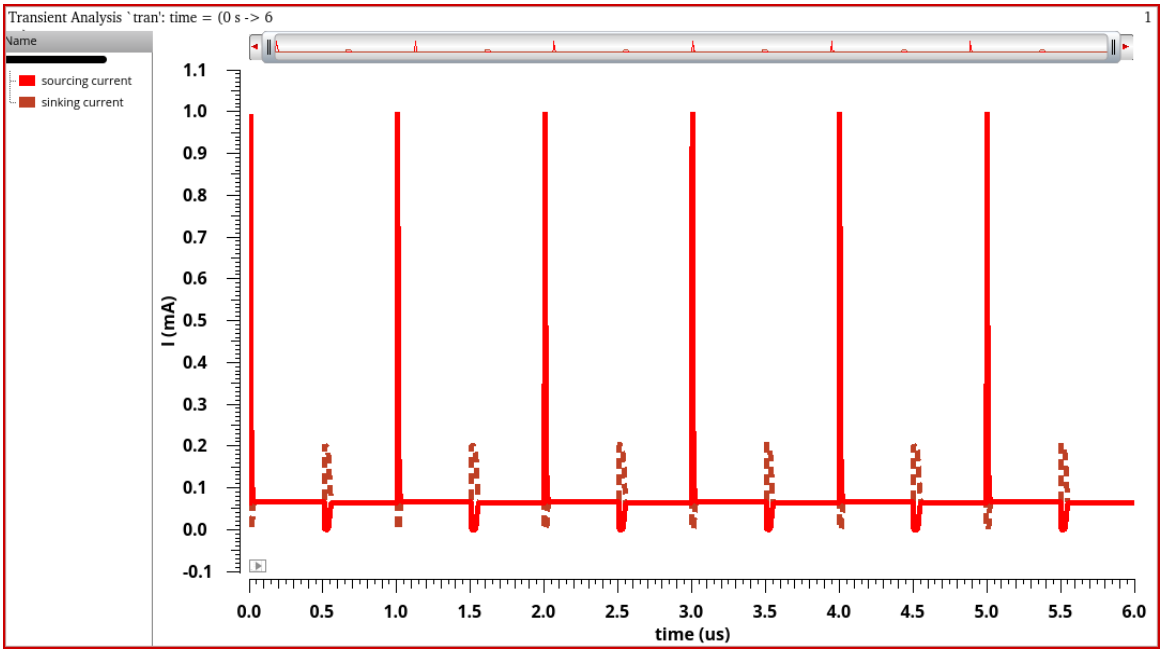

Figure 4.12 Sourcing and sinking output current capability (I_{BIAS} is replaced by MOSFET) for capacitive load C_L=15pF

To estimate the total harmonic distortion (THD) of the proposed circuit a sinusoidal wave of 600 mVpp with dc offset voltage of 1 V is applied at the input terminal. The percentage of THD for various frequencies is plotted in Figure 4.13 and it is observed that the THD of the proposed circuit is less than 2% upto 4.4 MHz.

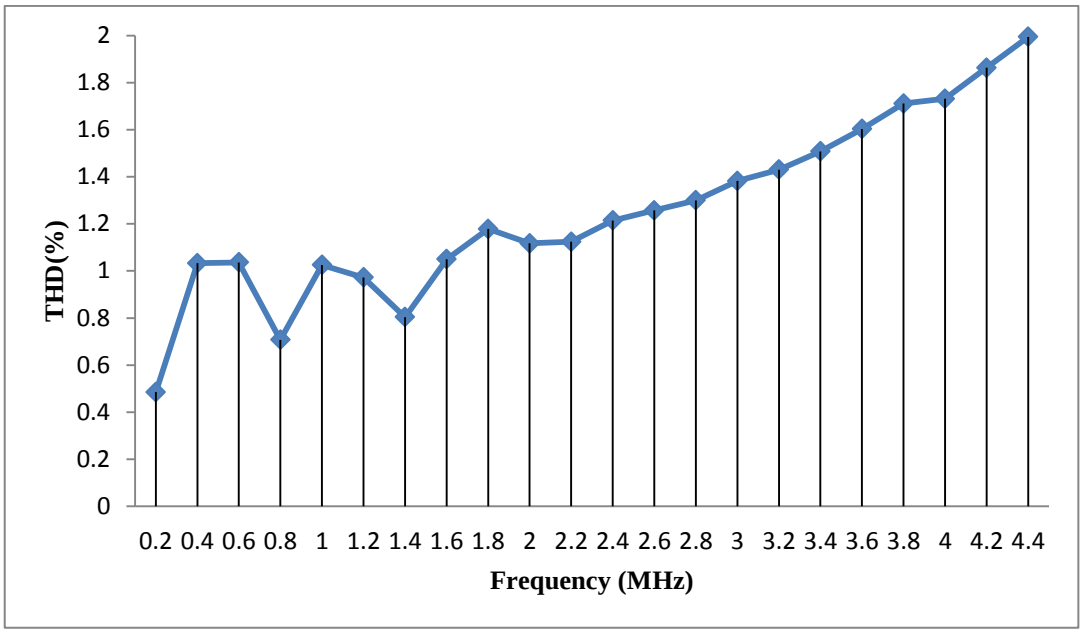

Figure 4.13 Variation of THD (%) with Frequency (MHz)

The corner analysis is performed to measure the circuit performance when there are extreme variations in process, voltage and temperature values. If all the variations produce acceptable results then there is largest possible yield of the circuit. The circuit is observed at five corners to check the circuit's performance under extreme conditions: typical NMOS typical PMOS (TT), slow NMOS slow PMOS (SS), slow NMOS fast PMOS (SF), fast NMOS slow PMOS (FS), fast NMOS fast PMOS (FF). Since, the chances of the circuit failure are maximum at these process corners, the designers must account for process variations in their designs.

The corner analysis of the proposed circuit is done with temperature and supply voltage as design variables. During simulation, the lowest supply voltage (VDD−10% of VDD) with highest temperature (125°C) is applied for SS corner and the highest supply voltage (VDD+10% of VDD) with lowest temperature (−55°C) is applied for FF corner. The process corners to obtain the simulation results for the proposed LSVFVF are listed in Table 4.1

Table 4.1 Corners Table

Corners	Supply voltage (VDD)	Temperature (°C)
TT	1.2	27
SS	1.08	125
SF	1.2	27
FS	1.2	27
FF	1.32	-55

The simulated DC transfer characterstics and frequency response of proposed LSVFVF for different process corners (TT, FF, SS, SF and FS) are shown in Figures 4.14 and 4.15 respectively.

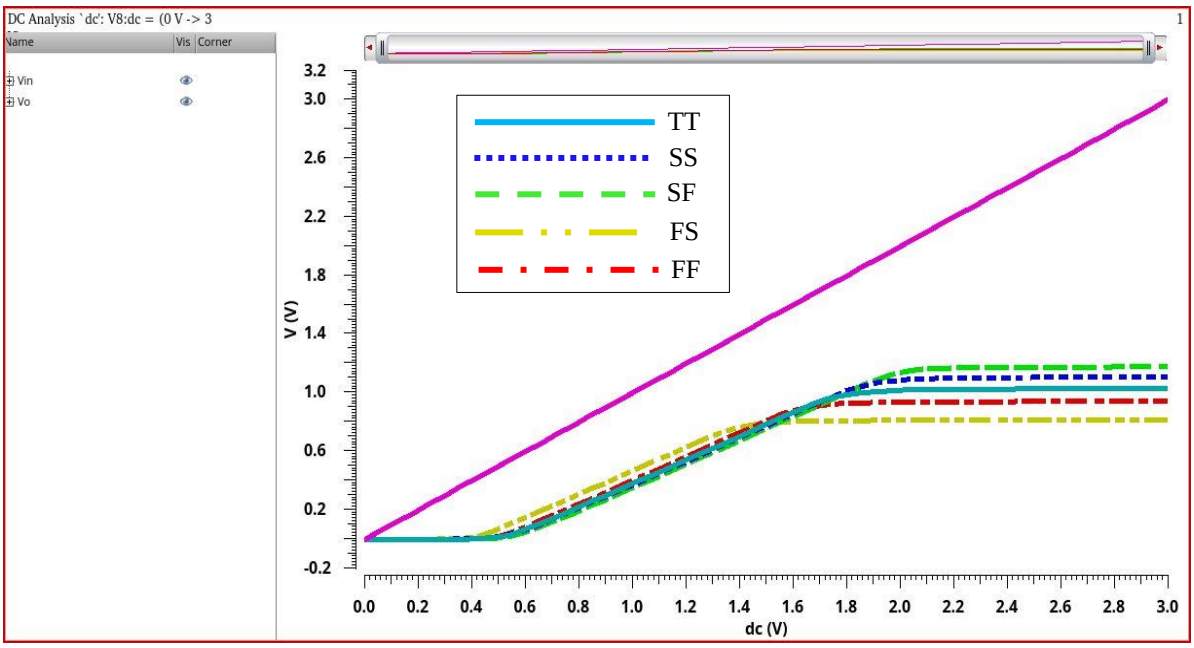

Figure 4.14 DC transfer characterstics of proposed LSVFVF for different process corners

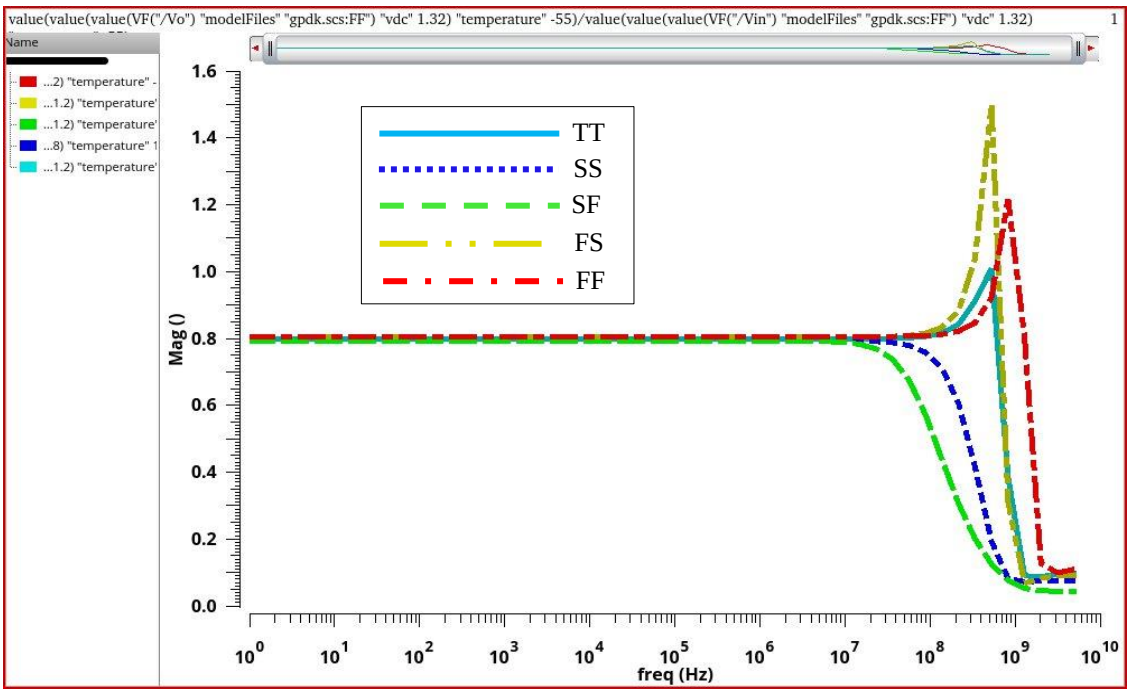

Figure 4.15 Frequency response of proposed LSVFVF for different process corners for C_L=1pF

The various performance parameters i.e. input swing, output swing, gain and bandwidth for different process corners are tabulated in Table 4.2. From Table 4.2, it is evident that the proposed LSVFVF operates at all the corners within the acceptable range.

Table 4.2 Performance parameters of the proposed LSVFVF for different process corners

Corners → Parameters ↓	TT	SS	SF	FS	FF
Input Swing	1.01 V	1.1 V	1.25V	0.8 V	0.88V
Output Swing	0.80 V	0.864 V	0.99 V	0.631 V	0.716 V
Gain	0.800	0.794	0.794	0.805	0.807
Bandwidth(C_L=1pF)	750.92MHz	249.13MHz	93.90MHz	772.79MHz	1.56GHz

Table 4.3 compares the performance parameters of proposed LSVFVF with FVF cells available in literature considering the body effect. It has been observed that the proposed LSVFVF has higher input/output swing, wider bandwidth and lower output resistance than similar FVF cell available in literature [22]. The gain, slew rate, power dissipation and sourcing capability of the proposed LSVFVF are also improved. In the proposed LSVFVF when I_{BIAS} is replaced by MOSFET then also large input/output swing, low output resistance and large current sourcing capability is achieved.

Table 4.3 Comparison of proposed LSVFVF with FVF cell available in literature

Parameters	Class- AB FVF [22]	Proposed LSVFVF	Proposed LSVFVF (I_{BIAS} is replaced by MOSFET)
Input Swing	0.534	1.01 V	1.028 V
Output Swing	0.353	0.809 V	0.820 V
Gain	0.78	0.80	0.80
Bandwidth (for C_L=1pF)	200 MHz	750.92 MHz	490.60 MHz
Output resistance	220 Ω	106 Ω	138 Ω
Bias current (I_B)	40 µA	65 µA	65 µA
SR+ (for C_L=15pF)	29 V/µs	31.58 V/µs	31.48 V/µs
SR- (for C_L=15pF)	27 V/µs	27.9 V/µs	12.18 V/µs
Sourcing current (for C_L=15pF)	11 I_B	15.2 I_B	15.38 I_B
Sinking current (for C_L=15pF)	10.4 I_B	6.9 I_B	3 I_B

Table 4.4 presents the comparison of proposed LSVFVF with similar FVF cells available in literature (when body effect is not considered). It is observed from Table 4.4 that the maximum gain, maximum input/output swing and minimum output resistance is achieved in case of proposed LSVFVF. The proposed LSVFVF has higher symmetrical slew rate.

Table 4.4 Comparison of proposed LSVFVF with FVFs (without body effect) available in literature

Parameters ↓	Conventional FVF [23]	Class- AB FVF [21]	Class- AB FVF [23]	FVF using level shifter [14]	Proposed LSVFVF
Input Swing	----	----	----	0.5 V	0.84 V
Output Swing	----	----	----	0.5 V	0.826 V
Gain	0.9	0.95	0.95	0.97	0.99
Bandwidth (for C_L=1pF)	260 MHz	200 MHz	170 MHz	1150 MHz	685.97 MHz
Output resistance	730 Ω	760 Ω	1.15 k Ω	193 Ω	144 Ω
Bias current (I_B)	7.4 µA	9.8 µA	8.3 µA	----	65 µA
SR+ (for C_L=1pF)	7.4 V/µs	----	42 V/µs	----	116.6 V/µs
SR- (for C_L=1pF)	145 V/µs	----	50 V/µs	----	120.5 V/µs
Sourcing current (for C_L=1pF)	1.08 I_B	----	20.48 I_B	----	1.87 I_B
Sinking current (for C_L=1pF)	28.37 I_B	----	9.63 I_B	----	2.89 I_B
Power Dissipation (for C_L=1pF)	9 µW	11 µW	10 µW	52 µW	24 µW

The DC transfer characterstics of LSVFVF based current sensor is shown in Figure 4.16 for the input current (I_{IN}) in the range of $0 \leq I_{IN} \leq 50$ µA. From Figure 4.16, it is observed that the output current (I_O) follows the input current (I_{IN}) with dc offset current ($I_B = 65\mu A$).

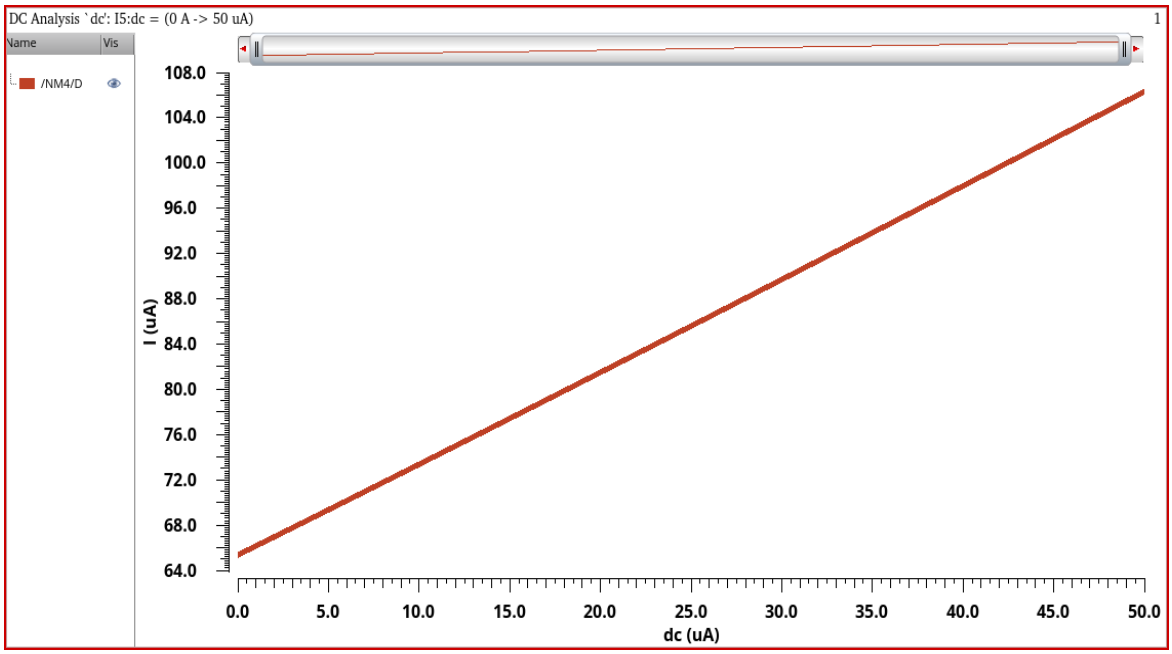

Figure 4.16 DC transfer characterstics of current sensor based on proposed LSVFVFCS

The DC transfer characterstics of differential structure using proposed LSVFVF is shown in Figure 4.17. From Figure 4.17 it is observed that the current through transistor M_5 (I_{DM5}) increases with the increase in ($V_{IN} - V_B$) following the MOS square law.

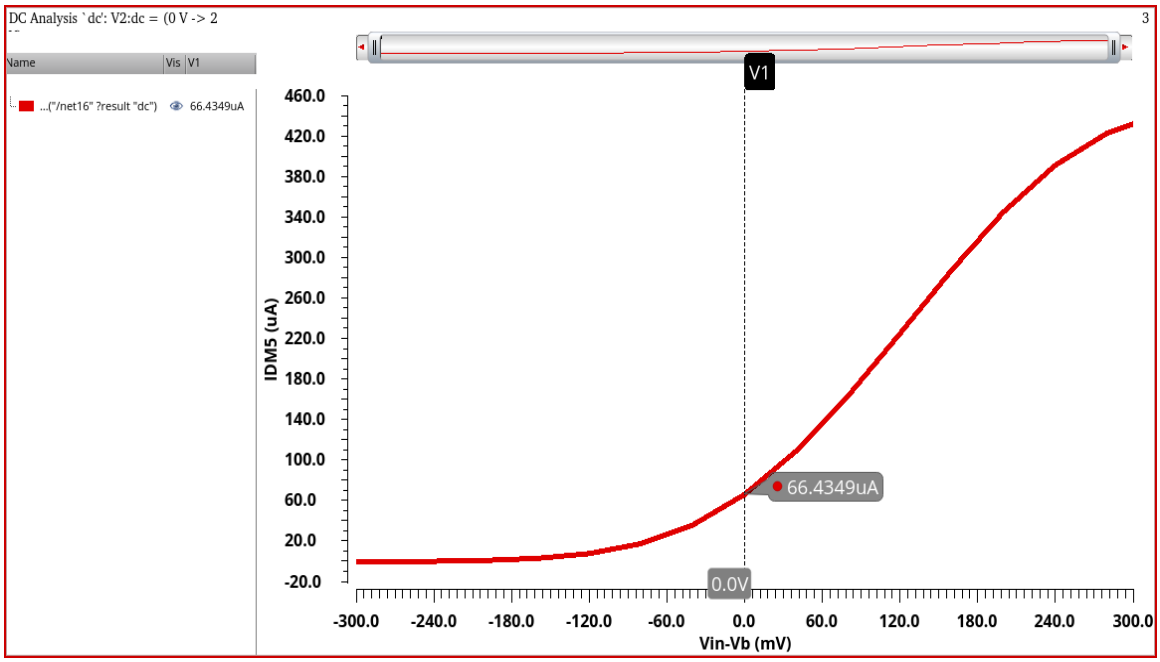

Figure 4.17 DC transfer characterstics of differential structure of proposed LSVFVF

CHAPTER 5

CONCLUSION AND FUTURE SCOPE

5.1 Conclusion

The research work in the thesis presents class-AB level shifted version of conventional flipped voltage follower (LSVFVF). The LSVFVF has higher input and output swing because of level shifter circuit and increased current sourcing capability and symmetrical slew rate for class-AB operation because of bulk-driven MOSFET used as a current source. The current sensing cell and differential structure using LSVFVF cell are also presented as an application of LSVFVF. The proposed circuits are simulated in Cadence Virtuoso Analog Design Environment using BSIM3V3 180 nm CMOS technology. Based on the comparison with the flipped voltage follower cell available in literature, it is concluded that the LSVFVF has wide bandwidth and low output resistance. The process corner analysis shows that the proposed circuit can work under extreme conditions of the design space. The proposed LSVFVF has high gain and is thus capable of handling large signal swings.

5.2 Future Scope

The research work in the thesis proposes LSVFVF that can be used as an analog basic building cell in the designing of various analog circuits such as current conveyors, current mirrors, operational amplifiers, multipliers, adders, filters, low-dropout regulators etc.

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APPENDIX A

Model file of NMOS

Generic PDK BSIM3V3 Spectre nmos1.scs

model nmos1_int bsim3v3

type=n lmin=0.18e-6 lmax=0.501e-6 wmin=0.4e-6 wmax=10.001e-6 minr=1e-60 tnom=25
+version=3.1 tox=toxn xj=1.6e-7 nch=3.9e+17 lln=1 lwn=1 wln=1 wwn=1 lint=1e-8 ll=0
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+dxwn dwg=0 dwb=0 ldif=9e-8 hdif=hdifn rsh=6.8rd=0 rs=0 vth0=0.48 dvthn lvth0=1.18e-8
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+k2=0.03 lk2=-2.01e-8 wk2=6.03e-10 pk2=5.87e-16 k3=0 dvt0=0 dvt1=0 dvt2=0 dvt0w=0
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+pub=-5.53e-32 uc=7.19e-11 luc=1.46e-17 wuc=-3.71e-19 puc=-1.43e-23 rdsw=170
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+ppdiblc2=5.71e-16 pdiblcb=0.01 drout=0 pscbe1=4e+08 pscbe2=1e-6 pvag=0 delta=0.01
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+pub1=2.31e-31 uc1=1.07e-10 luc1=-1.73e-17 wuc1=-1.51e-16 puc1=3.17e-23 kt1l=0 prt=0
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+6 jsw=1.6e-11 n=1 xti=3 capmod=2 nqsmod=0 xpart=1 cf=0 tlev=1 tlevc=1 dlc=3e-9
+noimod=2 noia=5.0e+19 noib=4.0e3 noic=-4.0e-13 em=3.0e+07 ef=0.883

Model file of PMOS

Generic PDK BSIM3V3 Spectre pmos1.scs

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