DESIGN AND ANALYSIS OF A 14-BIT LOW POWER SAR ADC

A Thesis submitted in partial fulfilment of the requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

in

VLSI Design

Submitted By

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JULY, 2019

DECLARATION

I, hereby declare that the dissertation titled **"Design and analysis of a 14-bit low power SAR ADC"** in the partial fulfillment of the requirement for degree of Master of Technology in VLSI DESIGN submitted in Electronics and Communication Engineering Department of Thapar Institute of Engineering and Technology, Patiala is an authentic record of my study carried out as under the guidance of **DR. Alpana Agarwal** (Associate Professor, ECED) during 2017-2019.

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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ABSTRACT

Now a days most of communicating system require wireless signal that is in digital form but at the same time if talking about real world all systems output analogues in nature, due to this reason firstly to communicate with real world analog signal convert into digital signal. For this system first requirement is speed. This fact leads to designer or researcher to proposed and implement analog to digital converter. Successive approximation ADC is accepted for reasonable rapid conservation with fine resolution. This present work explains the 14-bit SAR ADC with sampling frequency 20MHz. This present work mainly focused on the digital to analog converter block of SAR ADC for high speed and resolving coupling effect of device. Proposed design simulated in cadence virtuoso analog design environment and analog mixed signal (AMS) in 180nm CMOS technology. It has been designed for sampling frequency 20MHz to achieve high resolution for 14- bit successive approximation register ADC. Supply voltage for this design is 1.8V caters effective number of bit is 13.86.

AKNOWLDEGEMENT

First of all, I would like to express my gratitude to Dr. Alpana Agarwal, Associate Professor, Electronics and Communication Engineering Department, Thapar institute of engineering and technology, Patiala for her patient guidance and support throughout this report. I am truly very fortunate to have the opportunity to work with her. I found this guidance to be extremely valuable.

I am also thankful to Dr. Alpana Agarwal, Head of the Department (ECED) for providing us adequate environment in carrying the work.

I am also thankful to Dr. Anil Arora, Program Coordinator, Electronics and Communication Engineering Department, for the motivation and inspiration and that triggered me for the work. I would also like to thank my friends who have more or less contributed to the preparation of this report. I will be always indebted to them.

Last but not the least, I would like to thank my parents for their years of unyielding love and encourage. They have always wanted the best for me and I admire their determination and sacrifice.

Swati Lamoria

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LIST OF ACRONYMS

IC	Integrated Circuit
ADC	Analog to digital converter
FFT	Fast Fourier Transform
INL	Integral Non Linearity
DNL	Differential Non Linearity
SNR	Signal To Noise Ratio
SNDR	Signal To Noise Distortion Ratio
SNFR	Spurious Free Dynamic Range
THD	Total Harmonic Distortion
ENOB	Effective Number Of Bits
SHA	Sample And Hold Circuit
DAC	Digital To Analog Converter
AMS	Analog Mix Signaling
CMOS	Complementary Metal Oxide Semiconductor
PMOS	Positive Metal Oxide Semiconductor
NMOS	Negative Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SAR	Successive Approximation Register
MSB	Most Significant Bit
LSB	Least Significant Bit
RMS	Root Mean Square
RF	Radio Frequency
WLAN	Wireless Local Area Network
PDP	Power Delay Product
FOM	Figure Of Merit
VCO	Voltage Control Oscillator
ICMR	Input Common Mode Rejection Ratio
EOC	End Of Conversion
DC	Direct Current

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CHAPTER 1
INTRODUCTION

1.1 BACKGROUND

For portable and battery operated system, low power is significant parameter with growing technology and scaling of device. To diminish the power dissipation either low supply voltage is used that degrades the performance of the circuit or change capacitor value that is somewhat depends on the size of the device. With cutting in supply voltage, the value of threshold voltage should cutback. According to the Moore's law, as technology scales down it does not affect dynamic power but static power dissipation is affected. With scaling[1]. Due to this reason with more number of CMOS circuits power abandonment is crucial factor in design aspects. The digital integrated circuits are more beneficial than analog integrated circuits in the shattered in market with newly featherweight compact devices [2]. The target Digital IC design is to escalate the density of circuit, the logical precision and placing of circuitry therefore the clock signals is routed accurately though analog integrated circuit designs more convoluted and expensive as compare the digital IC design to reconcile the analogous achievement constraints. Further, upgrading in wireless technology, recently digital signal processing is evolved as wireless world came into picture.

A vast range of communication needs wireless systems that works upon digital signals but in day to day life, outputs of all systems are analogous in nature causing a demand to convert analog signals to digital signals so as to communicate with the real world. To inherit a good platform in digital side, analog design can be rebuilt in digital format.

1.2 SAR ADC ARCHITECTURE

Successive approximation analog to digital converter (SAR ADC) is most commonly used type ADC and it is very suitable for the general purpose application. Like portable device, data acquisition and industrial control. The main advantages of SAR ADC are low power utilization, high resolution and more accurate. Form factor of SAR ADC is small.

As a results all these benefit , SAR ADC usually merge with other large function. Lower sampling rate is main disadvantage for this SAR architecture. In this overall system accuracy is limited by the main block like comparator and digital to analog converter

By the name signify, the SAR ADC mostly follow the binary search algorithm. And for several MHz the internal circuit may be running at same time.

There are many innovation for executing the SAR ADC, the basic architecture of SAR ADC is little bit simple. Basic architecture consists four major block:-

- **Sample and Hold** : - it is hold and sample the value of signal with respect to clock signal.

- **SAR Register** :- it is called successive approximation register in which N-bit shift register that is used binary search algorithm method with every clock cycle
- **DAC** :- it stands for digital to analog converter that convert digital code into analog value.
- **Comparator**:- basically it is compare two analog signal and give the output response in the terms of logic high and logic low(1 or 0).

SAR ADC basic block diagram:

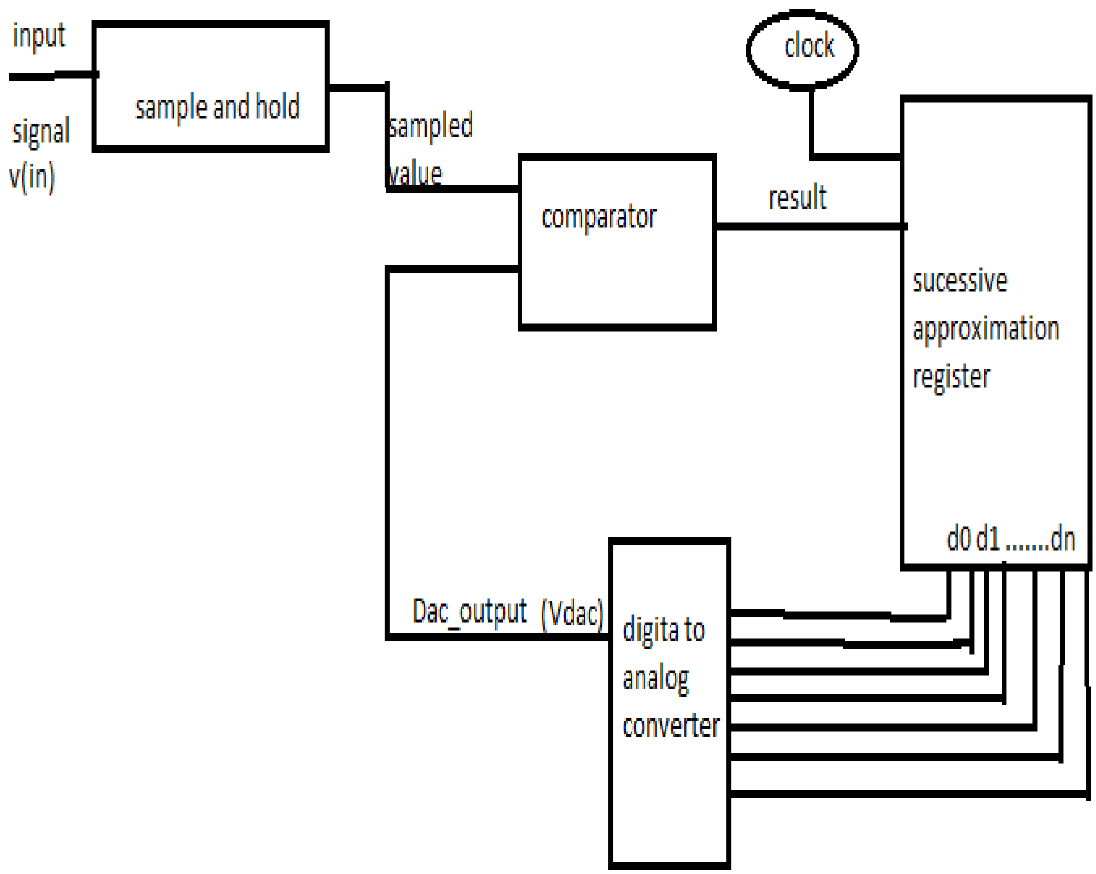

Figure 0.1 Basic block diagram of SAR ADC

The input voltage is taken with clock signal for applying the binary search algorithm. SAR register consist the N-bit register that with first cycle MSB bit is set to 1. This impose the digital to analog converter output (V_{DAC}) at V_{REF} /2, where V_{REF} is refer the reference voltage that is contribute in ADCs.

To understand the working of SAR ADC firstly the input voltage is compare with the digital to analog output signal that is input of the comparator and after that the comparator compare both the signal and give the response on terms of logic high and logic low (0 or1). According to the comparator response the

MSB is decided 1 or 0. For conversion of SAR ADC N number of clock cycle is required. And this N express the number of bits.

This analogy is used to determine if input voltage (V_{IN}) is more than or less than DAC output (V_{DAC}). Now firstly take an assumption if input voltage is greater the DAC voltage, the comparator output goes to logic high (or 1) and N bit register MSB is constant at logic high. Vice versa , if input voltage V_{IN} is less than the DAC voltage (V_{DAC}) then comparator again compare both the values and reset the MSB at zero logic. After that SAR logic shifted on the next bit, And set the bit at logic high. further comparison continue till the last bit is set or reset. The N-bit array go on all step down to the last bit. This process conclude , that the conservation is completely finished and the N bit is obtain in digital form.

Now let's take a example for 4 bit SAR ADC in the first clock cycle voltage of digital to analog converter is set to half of by reference voltage setting the code to 1000, next the input voltage is compared to half of the reference voltage ($V_{REF}/2$) and after that based on the confining result, Most significant bit (MSB) is decided. If $V_{IN} > V_{REF}/2$ then the value of MSB bit will be unchanged and will continue at one, or else the MSB is reset to zero. So MSB (*D3*) remains at 1. Input voltage of digital to analog converter (DAC) is set on 1100 in next clock cycle and repeatedly V_{IN} is correlated to 3vref/4. *D2* hold its value since $V_{IN} > 3V_{REF}/4$. As the next bit the DAC input is set to 1110. In the next comparison, *D1* is zero since $V_{IN} < 7V_{REF}/8$ and lastly for defining least significant bit (LSB), input of the digital to analog converter set on 1101. *D0* is 1 because $V_{IN} > 13V_{REF}/16$. Thus, the analog input is transformed to the digital signal 1101 in four clock cycles.

It is very necessary the performance of the ADC is figured out before its use. By using some performance Metrics. For any kind of ADC the performance metrics along with pipeline ADC classify in the two group one is static and another dynamic.

1.3 ADC DESIGNE PARAMETER METRICS

1.3.1 Static Performance Metrics:-

Using DC signal, low frequency signal and ramp signal the static performance can be determine. These parameter consist of offset value, gain, differential non linearity and integral non linearity. All these aspect examined using ADC's input-output attributes. These are:

1.3.1.1 Sample Condition:

Nyquist criterion, states that " frequency of sampling signal is larger or equal to twice of input signal frequency so that the attained discrete spectra can be fully recovered from the input signal. In figure 1.2 sample conditions is describe.

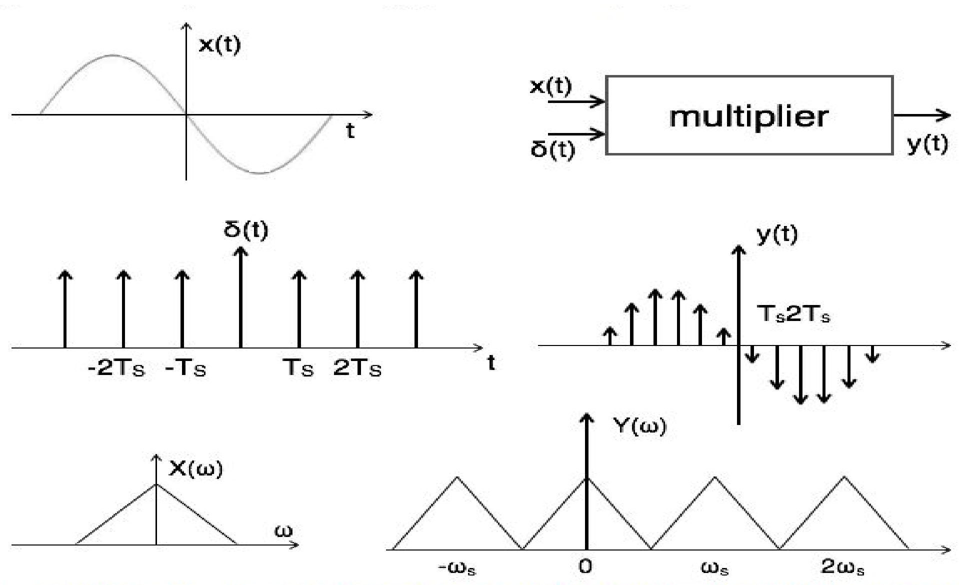

Figure 0.2 Sampling condition for analog signal

In another way, when different frequency appears in frequency domain, it leads to a problem known as aliasing.

Aliasing condition when fs > 2fm

Aliasing is an impact that originator for the different signals to become indistinguishable when it sampled.in other way we can say it is also point out the distortion or misinterpretation that results while signal is restore from samples is not same as original signal. In figure 1.3 oversampling is known as aliasing.

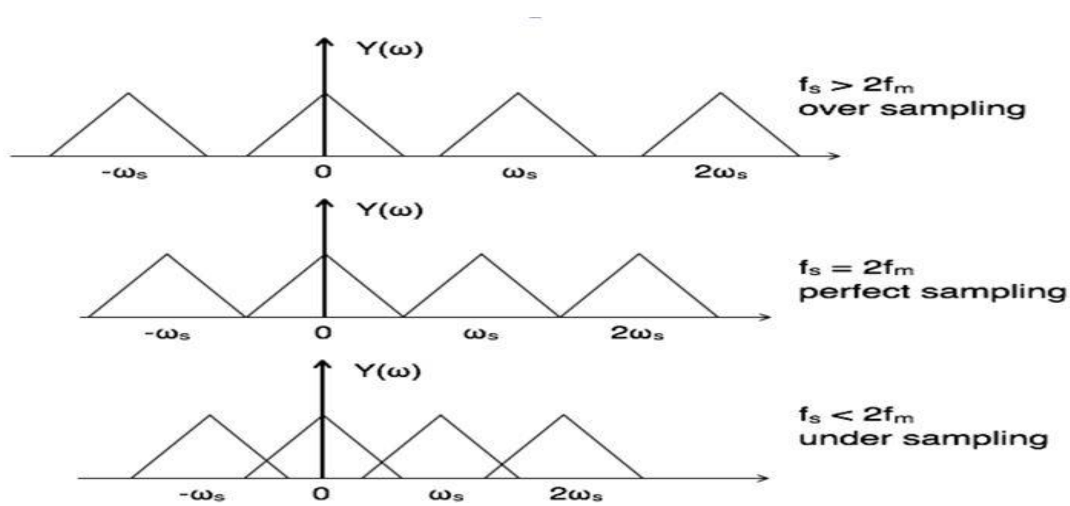

Figure 1.3 Aliasing condition for signal

1.3.1.2 Quantization Error:

In an ideal converter quantization process is introduce an permanent error. Moreover the sampling time is constant and fixed and no extra error introduce. Quantization error introduced by the procedure of the quantization. Ideally, value of analog input signal can be superlative of ½ of least significant bit away from the adjacent digital code.as a result 0.5 of LSB is the quantization error.

To determine the relationship between the quantization step q_s and input signal $v_{in.}$ Quantization step is computed by a signal is quantized in how many number of step. No of quantization step is indicate in no. of bits (here n is no of bits).

In figure 1.4 the amplitude level (A_k) of a quantized signal is shown. A signal $A_k+\alpha$ is perfectly quantized within level of A_k considering the value of α is enclosed by $-{q_s}/{2} < \alpha < {q_s}/{2}$. Quantization error never be superior to an amplitude level equal to $\pm < {q_s}/{2}$.signals that's to some extent larger then $A_k + {q_s}/{2}$ are quantized A_{k+1} next quantization level.

The probability error function demonstrate that there no correlation between sampling frequency and signal frequency.

RMS quantization error represent as:

$$E(\alpha^2) = \frac{1}{q_s}\int_{-\frac{1}{q_s}}^{\frac{1}{q_s}} \alpha^2 d\alpha$$

Here E(.) shows statistical expectation. With some assumptions the average value of quantization error is zero.

After solving integral, the quantization error represented as quantization error voltage e_{qns}^2. The quantization error voltage $e_{qns}^2 = E(\alpha^2)$ can be expressed by:

$$e_{qns}^2 = \frac{1}{12} q_s^2$$

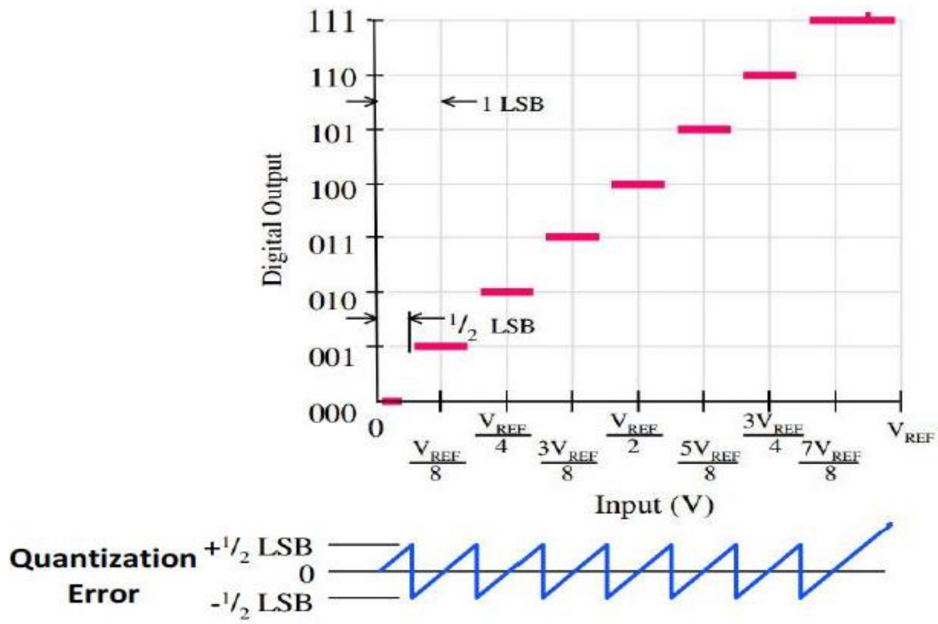

Figure 1.4 Quantization error for ideal ADC

1.3.1.3 Offset Error:

In an ideal case an input voltage of (LSB) / 2 will cause the first transition in output but practically the first transition takes place at a different voltage. Offset error is define by the difference of above two input transition voltages as shown in fig. 1.5

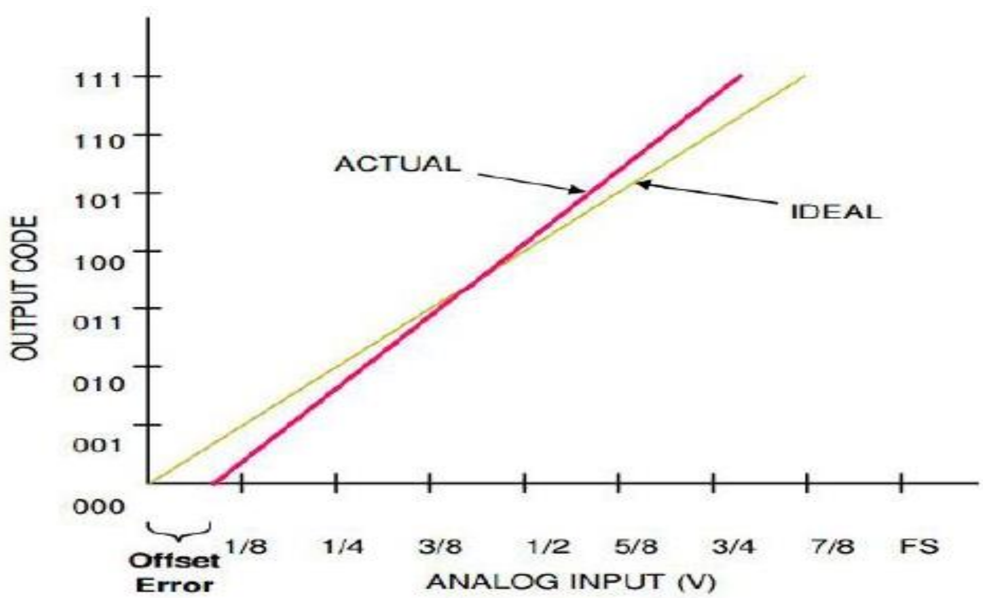

Figure 1.5 Offset error In transfer function of ADC

If the practical value of voltage at which first changeover takes place is more than the ideal voltage then it is called as positive offset error. If the practical voltage at which first transition takes place is less than the ideal voltage then it is called as negative offset error. The difference between the practical full scale transition value (last transition value) and ideal full scale transition value is recognize as full scale offset error as shown in figure1.6

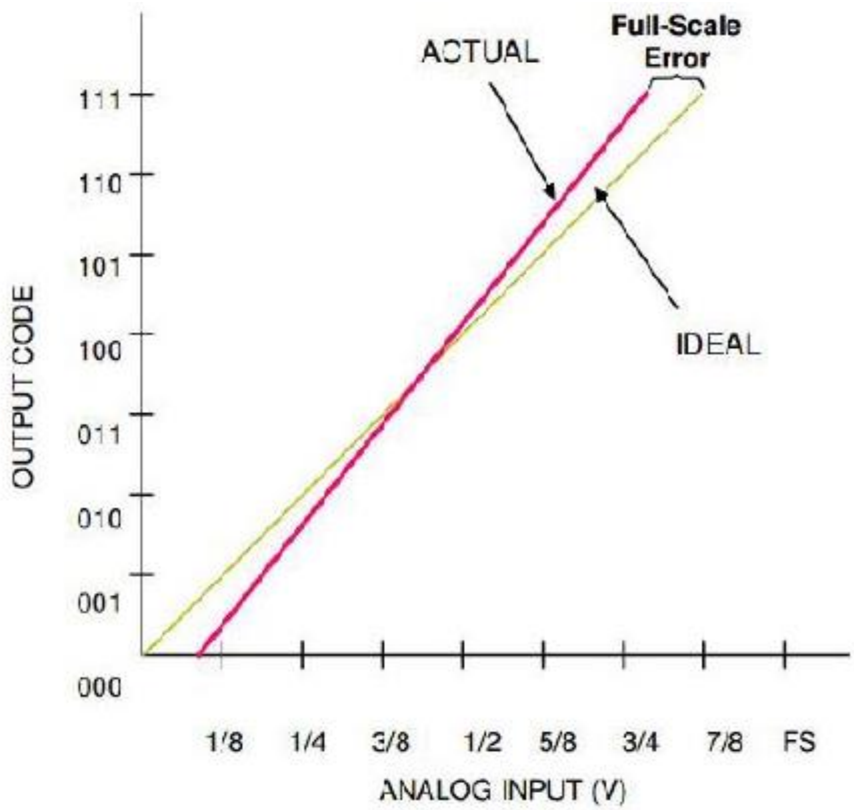

Figure 1.6 Full scale offset error in ideal ADC

Reason of occurrence of full scale error is because of presence of offset error, which can be eliminated easily as it is constant. Presence of slope error in input-output characteristics also leads to full scale error.

1.3.1.4 Gain Error:

The difference of both the slopes of practical and ideal transfer function is referred to as gain error.

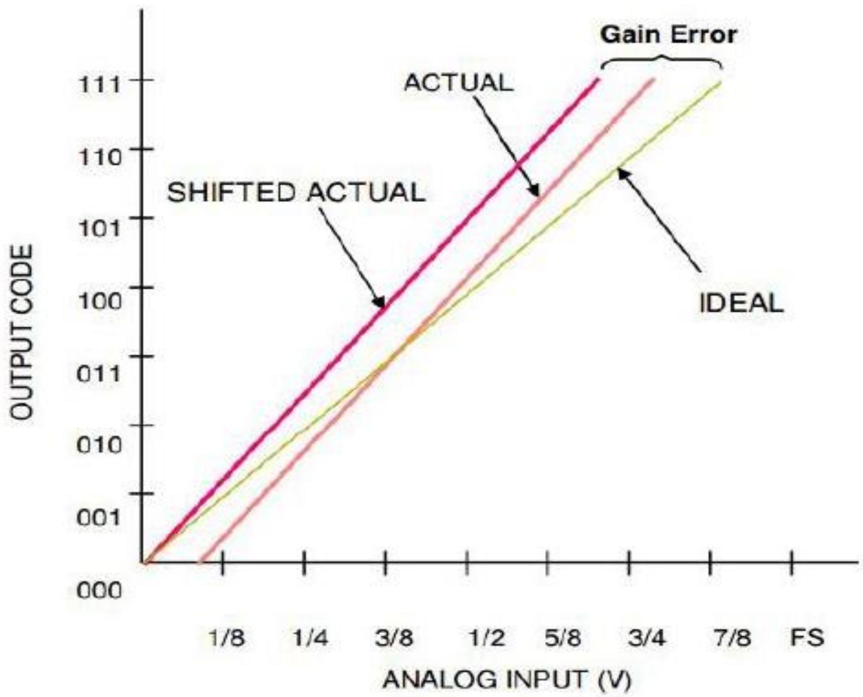

Figure 1.7 Gain Error for ADC

Gain error = full scale offset error - offset error value

To calculate gain error transfer function can be adjusted to make offset error during first transition zero then , Gain error = full scale offset error

1.3.1.5 Non Linearity Error:

In ADC these are of two types

a) Differential error b) Integral error

- **Differential error**: Differential non-linearity depicts step size error. For ideal converter, the transitions in output code happens accurate after each count/LSB and transfer function characteristics step size in ideal stair case should be one LSB. But step size in case of practical converter is not equal to 1 LSB/count. Differential error/ non linearity is the difference between ideal and practical step sizes. As shown in fig 1.8 with change in input from 1500 mv to 2500 mv the digital output level does not change in practical case, but ideally it change, This is referred to as missing code as shown. In figure. 1.8

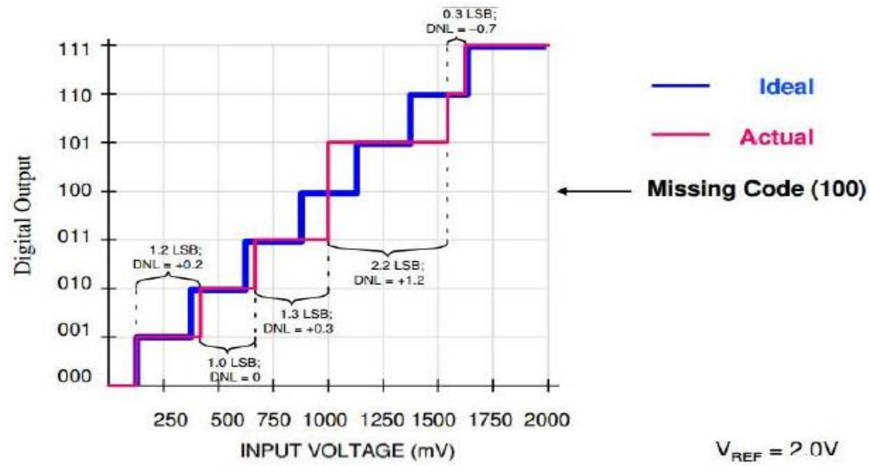

Figure 1.8 Differential error with missing code in ADC

- **Integral non linearity /error**: when transfer function is deviated from ideal linear function leads to integral non linearity which is shown in figure 1.9. integral non linearity shows bow in the transfer function curve. Offset error value and gain error value Quantization error, are not contained in INL. The integral linearity for the ADC is determined by the size of differential non linearity.

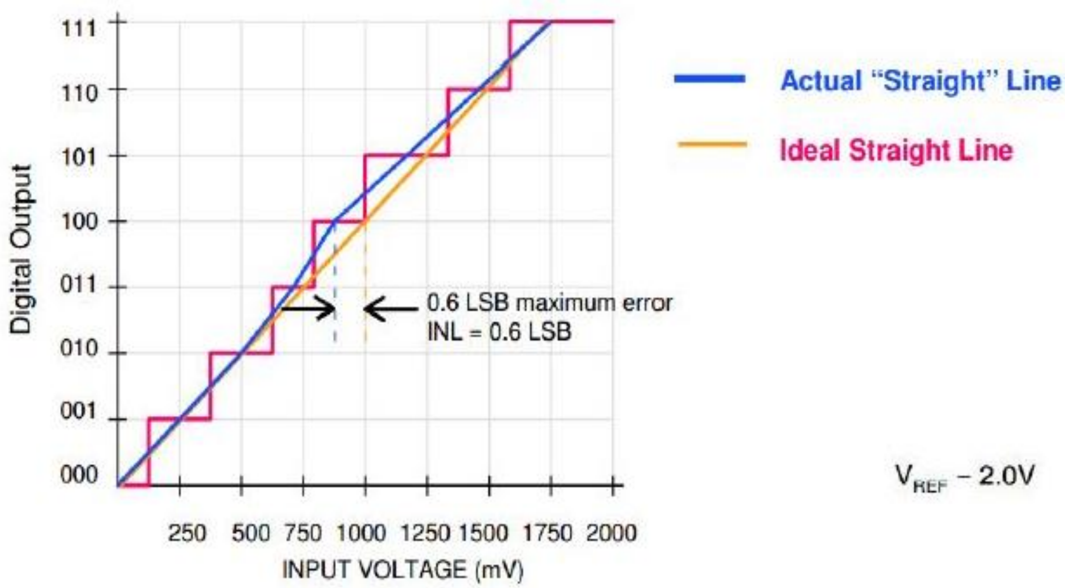

Figure 1.9 Integral non linearity in ADC

- **Total unadjusted error**: It shows worst possible deviation in performance from the ideal performance. It includes all errors such as linearity error, offset error , gain error.

1.3.2 Dynamic Performance Matrices:

Frequency response of an ADC is used for determining ADCs dynamic performance and high frequency signals are required for determining dynamic parameters .The ADC is fed with a high frequency input signal which gives same signals quantized level at the output after that digital output of ADC is converted again . Dynamic parameters of ADC under test are obtained from frequency spectra of the rebuilt high frequency input signal. The parameter under test are in dynamic range are

1.3.2.1 Signal To Noise Ratio (SNR)

SNR is characterized by the ratio of the signal to noise power. With resolution N, maximum achievable SNR (dB) is given by

$$SNR = N \times 6.02 + 1.76\ dB$$

Factors affecting SNR are linearity error, thermal noise, clock jitter these factors leads SNR degradation. In general, SNR is the ratio of the signals power to addition of different noise power. SNR is input signal dependent because with increases in frequency of input signal with jitter increases and when amplitude of input signal is decrease power of the signal is also decrease.

1.3.2.2 Total Harmonic Distortion (THD)

Output spectrum of ADC which is non- ideal includes harmonics at frequency that are multiplex of frequency signal. Total harmonic distortion is define as ratio between total that exist in signal power.

$$THD = \frac{\sum_{k=2}^{l} p(k)}{P(z)}$$

Where m denoted in spectrum how many harmonics are present s the total number of, P(k) denotes kth harmonic power , P(z) is fundamental harmonics power or power of a signal.

1.3.2.3 Spurious Free Dynamic Range (SFDR)

The Harmonics which is present in a signal that are tone occurring in the multiple time of frequency of input. Unwanted tones which occur at the input signal frequency that have non integer behavior are known as spurious frequency. SFDR is define as signal power is divided by the power using by component of any frequency excluding DC component. In denominator presented frequency is tone occurring that may be harmonic frequency or may be spurious frequency.

$$SFDR = \frac{P(z)}{Max(P(Spectrum))}$$

Where P(z) presented power of signal, P(spectrum)represented the other frequency power that appearing at multiple times of signal frequency it may be integers or non - integers.

1.3.2.4 Signal To Noise Distortion Ratio (SNDR Or SINAD)

Covering the effect of noise and distortion by SNDR. So SNDR is define in terms of signal power is divided by the summation of both harmonic and noise power.

$$SNDR = \frac{p(z)}{\sum_{k=2}^{l} p(k) + p(n)}$$

Here P(z) denotes power used by signal signal , P(k) denotes kth harmonic power, P(n) represent the power of noise that is summation of differential non linearity jitter noise and thermal noise.

1.3.2.5 Effective Number Of Bits (ENOB)

Due to non – ideal behavior of ADC ideal resolution of an ADC is differ from real resolution of ADC. When an ADC is under test the real resolution is examine by the parameter which is known as effective number of bits.

$$ENOB(bits) = \frac{SNDR - 1.76}{6.02}$$

1.4 LITERATURE REVIEW

The research work being done in the field of SAR ADC and comparators is reported in the following chapter. A brief description based on the research is as follows.

Pedro M. Figueiredo et al. [3] described the disruption known as kickback noise in the latched comparators. As we know that in flash ADC comparators are used in large numbers according to the determination because of which the reference voltage of the converter gets affected. The kickback noise might alter the transition of voltage. This phenomenon also leads to the degradation of the amplifier in the pipelined stage. This research paper is an effort to propose some new kickback noise reduction techniques by studying existing techniques. The commonly used is the source follower or preamplifier technique, but this technique increases the offset voltage and power consumption. The new techniques being proposed are inserting sampling switches before input differential pair, control on the change of voltage on drains of differential pair and detection only when comparator output is ready etc.

M.B. Guermaz et al. [4] suggested a clocked computer which is based on a switched capacitors by using a two-phase non-overlapping clock for RF WLAN application. This clocked comparator uses decisive feedback stage after the preamplifier stage. Reduction in power consumption is achieved using dynamic latches in place of static latches; this arrangement has buffer also that helps in reducing gain and increasing bandwidth. The advantage of using buffers is that they can also be used as a memorizer circuit, and it is also capable of erasing the memory during pre-change. With the addition of large MOSFET in the preamplifier stage, the offset voltage is decreased, and gain is increased moderately. But this further leads to affect in the conversion speed of comparator. So differential comparator configuration is employed to obtain an offset voltage of 77.3mv, 0.8mw of power consumption and 17.3ns delay

D. Meganathan et al. [5] also suggested an approach for low power pipelined ADC. In this sample, a modified two-stage high gain operational trans conductance amplifier having a wide bandwidth was used and hold amplifier to decrease the thermal noise and power consumption. For this the lower limit of the signal swing of analogue functional block is the supply voltage (1.8V). Due to power-sharing kickback noise dynamic range is increased, and the dynamic power dissipation of the comparator was reduced. By using Bottom plate sampling and bootstrap technique, the Non-linearity error that causes SNDR of 58.72 at 2 MHz and 57.57 dB at a Nyquist frequency is reduced.

Hugues J. Achigui et al. [6] concentrated on comparator depicted in this paper has a differential input stage and flipped voltage follower cell that has high input common mode range and because of this high swing. It is good for current mode applications due to its low input resistance. Improvement in speed is made by adding inverters to the loop, and it is also allowed to the source of large currents. It is equipped with class AB, which helps in improving input resistance and push-pull digital inverter, which, uses class B concept for low voltage. A 1V supply voltage it consumes 30μW power and power delay-delay product (PDP) I/tpis1μA/15ns.

Samaneh Babayan et al. [7] depicted dynamic and double-tailed comparator. Clocked comparators can decide the faster way due to positive feedback in regenerative latch and hence are used in wide 8applications. Some stacked MOS makes the supply voltage to have a proper delay. Since the single current path is where the transistor operated on the triode region and current depend in the common mode input voltage. Conventional double tailed comparator intermediate nodes are discharge and charge during the phase and reset, respectively. During the set phase, it will evaluate the logic according to inputs, this increases the power consumption, and in reset phase nodes are charged up to VDD. The output is affected by mismatching in the controlling transistor. High parasitic capacitance in large-sized transistors further affects the delay. A new double tailed comparator is proposed in the paper that does not require high voltage and to stack up too many MOSFET. Here the size is reduced, which helps to add the MOSFET to the conventional double tailed comparator that further reduces the delay of the circuit. In this Power is saved as compared to the conventional double tail comparator. At 0.8V power supply, average power dissipation (at 500 MHz) = 329μW, worst case delay = 294 ps/dec. And offset (σ_OS) of 7.8mV were observed.

I-Chyn Wey et al. [8] tried to speed up gradation by designing comparator based on CMOS dynamic comparator. Main areas of concern are a reduction in power, less transistor count, and enhancing speed. Main ideas behind this comparator are rearrangement and reordering of transistors. These can also be used as a 0/1 detector, equality and mutual comparator. This approach results in 37.8% less number of transistor count and noise immunity are even better as compared to conventional circuits. Since only two comparators are used in series pull-down delay is reduced, which helps in reducing the delay. Speed was also acerbated by combating 'weak 0' problem in PMOS of pull down the network. In place of it, an NMOS combined with an inverter was used, which resulted in the low power delay product. The suggested 64-bit comparator consumed 0.176 mw power and a delay of 0.38ns.

Ghil-Geun Oh et. al. [9] came up with the simplified ADC that exclude extra blocks from the device like sample and hold circuit, reference ladder etc. Low power is the main factor for the ADC that is useful for many applications. The new clock generator is explained in this to eliminate the sample and hold circuit, that reduces the need for a higher frequency clock. Clock generator made up by delay locked loop also helps in reducing the burden of the clock source. It comes with a conversion rate of 400MS/s with a supply voltage of 2V.

Lei Sun et al. [10] design implementation of Pipelined based SAR ADCs for application of high speed and high resolution. To optimizing the stage resolution have been reported. The single A/D converter like SAR ADC outperform other type of A/D converter considering area and energy efficiency which also limits the speed of conversion this is all due to the binary search algorithm. Using this design methodology author resolves this problem using pipelining with successive approximation register ADC for which increase the conversion speed of SAR ADC and also individual stage is resolved. Speed, area, power consumption and non- linearity of the conventional ADC are improved in this hybrid type of ADC. Author concluded in this design process that under certain cases resolution per stage improves the A/D converter linearity without costing the speed of the op-amps used for residue amplification. Also operational amplifier open loop gain requirements are not affected by pre stage resolution. Some constraints like power consumption of overall circuitry depends on the first stage resolution. Serial decision process is slowed down by pipelining of energy efficient SAR ADC as a result overall conversion rate relies on the first stage resolution and linearity also depends on this stage.

Hyunsoo Ha et al.[11] implemented a design for 13-bit SAR ADC that is represented for sensor interface with ultra- low power. In DAC two identical capacitor array play a role for swapping, capacitor error compensation is achieved. ADC is implemented in 130nm CMOS technology. The ADC power dissipates 1.47uW with 40KS/s sampling frequency with single supply voltage is 0.5V full conversion range is obtain. For this design ENOB is 11.0 bit and FOM is 17.9fJ

Arindam Sanyal et al[12] has reported a design implementation scheme. This scheme is about SAR ADC switching efficiency that can be obtain at 95% decrement in energy of switch or the existing SAR ADC. Power consumption by switch and power absorbed from reference generator, switching power can be calculated. Over the broad range of frequency, higher range of efficiency is maintain by the proposed methodology . Also came into the picture scaling of the device and FOM is 0.14fJ/ conversion.

Taimur Rabuske et al.[13] proposed to design a successive approximate register ADC with principle of charge sharing. In the proposed design author tells that self-calibration leads to cancellation of mismatching of comparator and improvement in the linearity of the A/D converter. For the power supplied to the circuit is 350mv to 600mv for SAR ADC that conclude this proposed circuit is demonstrated at low voltage. The design is used 130nm CMOS technology for 8- bit resolution and the other parameter id given below:

Hokyu Lee et al. [14] gave the idea to use SAR ADC with time-interleaved that shares the resistor array of DAC. By implementing this technique power consumption was reduced by 69% and inter-channel error is compensated by different calibration technique. Fabricated with 65nm technology and consumed 22mW at the supply of 1.2V.

Zbigniew Jaworski et al. [15] proposed a new design of ADC that consist of the resistive ladder, comparator based on MCML with pipelined latch circuit and also innovate encoder block with 2 segment MCML. To enhance the proposed design performance an averaging method is used for interpolations. By using these techniques the number of preamplifiers is reduced and for the advancement in averaging efficiency a connection is used that is triple cross connection. The encoder is able to bear the bubble error.

Muhammad Ahmadi et al.[16] in this design A comparator for SAR ADC with high resolution that are used in the field of low power . power consumption is major design Aspect for SAR ADC that’s the reason this proposed design came into picture. To get the overall performance at low power level the implemented design to find out the theoretical analysis comparator. Firstly mathematical modeling of SAR ADC has to done for accuracy. Power used by per conversion is not same so with the help of mathematical modeling comparison of power is done. Therefore when this problem is optimizes so power budget of comparator among all bits for SAR ADC is distributed. By using simulation of this device result conclude that power saved up to 50% to 60% for 12b or 14 b SAR ADC. Noise allocation problem of comparator solved by using less number of comparator are used in ADC.

Peng Zhu et al.[17] design implementing for Delta sigma ADC with 02- MASH and bandwidth is used by this ADC is 40MHz. In this design the non-linearity cancellation technique in VCO that is based on Delta Sigma ADC is presented. Due to scaling of transistor the recently used CMOS technology arrange the fast switching. That is used for high speed continuous analog to digital converter. For the reason of voltage headroom the CMOS design figure out new design challenge. VCO based ADC that is also time based used for overcome this problem and advantage for this the gate delay is reduced. Inherited non - linear behavior of VCO limits the performance of the ADC. This proposed device is achieve the SNDR is 66.8 dB with 40MHz sampling frequency and power is 4.98mW and FOM is 35FJ/steps

Xinpeng Xing et al.[18] reported a VCO design based on delta sigma ADC. In this design method due to open loop structure and digital building block the device give the high bandwidth and efficient power with robust performance. Cancel distortion and reduction in voltage both schemes are mitigated on VCO Base quantized and non-linarites. Quantized output of the VCO with intrinsic DEM matching for the digital to analog converter cell is relaxed. This proposed design is used 40nm technology and power supply is 0.9 with low power consumption up to 2.7mW.

Long Lim et al.[19] a design implementation for 13 bit SAR ADC which assisted with pipeline ADC for sampling speed 50 MS/s based on fully differential ring amplifier. ADC is reported, which is used 65 nm CMOS technology. The author has been stating that this design introduces a fully differential ring amplifier which maintains the benefits of fast slew rate based on charging high gain and full output swing.

Min kyu kim et al.[20] reported with12-bit SAR ADC that is used low area with low power consumption or single slope ADC for CMOS image sensor. In SAR/SS ADC the quantity of unit capacitors is being decreased to $1/64^{th}$ of the conventional design and power consumption is being decreased by analog circuit sharing among SAR ADC and single slope ADC. For CMOS image sensing single slope ADC is widely used due to its high resolution and small area, but it’s A/D conversion time is large for which there is an alternate solution that is delta sigma, cyclic ADC or SAR ADC can be used in place of SS ADC. Delta sigma ADC and cyclic ADC are the case of low noise and conversion time is less whereas on the other hand it requires high power consuming op-amps. The problem of power consumption in delta sigma ADC and cyclic ADC, VCO is resolved with current source being used which leads to the CIS circuit complexity hence making it not completely useful. When the case of SAR ADC is considered it accompanies conversion time is short and low power consumption while as a limitation it requires larger area to implement capacitor DAC. The formation of hybrid ADC is done with the combination of SAR with single slope ADC such that i the area of SAR and also the conversion time for SS ADC is decreased. This implementation uses 90nm CMOS technology. For high speed application single slope / SAR ADC is used like CMOS image sensors.

Advantages-

1) Analog to digital converter conversion time of SS ADC is decreased. .
2) SAR ADC area is also reduced.
3) Due to sharing of power supply there is low power consumption.

Disadvantage– Non linearity of differential SAR ADC.

Wan Kim et al.[21]reported a certain design which uses a time interleaved that Assisted with asynchronous successive approximation register ADC. Which is suitable architecture in the condition of low power supply . Gain boosting dynamic pre amplifier has been proposed that improve the performance I term of the noise of comparator. To increase the speed of asynchronous decision in the pre amplifier a reference generator is added which is based on self- timing. In the same way a dual mode cock generator has been proposed which is generated the low jitter with fix width of sampling frequency for higher frequency of operation. And if clock is with low quality the frequency is also low. For this design the supply voltage is 0.6V other comparable design circuits. When ENOB is more the 10bit the conversion rate is less it is up to 1MSPs.

SWC operation helps in reducing the size of the logical blocks of the SAD control loop also help to reduce the power consumption. Some techniques like in dynamic comparator the gain boosting technique that is related with noise and also proposed the clock generator with dual mode. At the conservation rate is 10MSPs from which ENOB is 1.04 with figure of merit 6.2fj/ conservation.

Chun-Po Huang et al. [22] reported a design analysis SAR ADCs that were broadly used in portable devices and also in bio medical application for this reason is listed is excellent power efficiency. At the process node specification of optimized high performance SAR ADC is consume time and also hard to find the feasibility at this node. Based on design considerations this design presents a asynchronous SAR ADC sizing methodology in systematic manner. Based on the design the size of tool also executed. With art manual work of the other state is comparable with sizing tools. Due to this reason an efficient and effective searching algorithm of size time is decreased.

Dai Zhang et al.[23] reported a design of 14 bit SAR ADC with sampling speed 10KSPs using in biomedical.. In this design uniform algebra of non–binary weighted capacitive DAC is designed and also helps to achieve increased linearity, a power comparator is designed with bias control method for reduction in power consumption. Additionally error correction logic is implemented in this design.

Wei Hsin Tseng et al.[24] came up with a 12 bit SAR ADC using 28nm CMOS technology for wireless transmitter with assistance of digital slope to be used in cellular applications. This design implementation uses a calibration method to correct the capacitor digital to analog converter and reducing the size of the capacitor to 0.6pf from 3.6pf desired for 12 -bit matching and also power consumption is reduced. Since the capacitor size is decreased area is also reduced and also this design is very compact for mobile applications. The calibration that is proposed here reduces power of the reference generator by 80% capacitor size by 83% and buffer current is 72%. ADC here achieves both low power and high speed by the combination of several features. Above design method reduces duty cycle up to 25% and other features are shown in the table below:

Chun Cheng Liu et.al.[25] reported design implementing using two ADC one is digital slope ADC and another SAR ADC to get high resolution up to 12-bit. A hybrid ADC is also formed with combining digital slope ADC for low noise and SAR ADC for low power. For high energy efficiency SAR ADC is used. Scaling of CMOS technology improves the speed of this A/D converter with growing band of transistor. By using this design the single channel SAR ADC sampling speed can be increased to few MS/s with 8 to 12 bit resolution. This proposed design is used for the wireless communication like LET and WIFI. Comparator

Noise is constrained the SNR of the SAR ADC and limited below 60dB. There is nonlinear trade-off between the power consumption and noise of the comparator. This design technique helps in reducing comparator noise without increasing power consumption. Maximum speed is degraded with the additional bit cycles. In this design process a 12 bit hybrid A/D converter. Which is combination of the two ADC one is 7-bit coarse SAR ADC and second one is digital slope ADC with 0.9 power supply to achieve the sampling speed up to 100MSPs with 0.35mW power consumption. In this proposed design SNDR and SNFR is 64.43dB and 75.42dB respectively achieved by ADC at 100MSPs. A continuous comparator that used in digital slope to measure the signal is detecting zero dynamic crossing. Continuous ramp signal prevent the continuous comparator in mete stable state and provide the constant delay with zero crossing.

. The comparison time is:

$$Tc = V_{IN}/V_{LSB} \cdot$$

$\tau u + T_{\text{Latency}}$

Where: τu is the latency of a delay cell.

T_{latency}: It is the latency that tends zero crossing input to flipping the output. For large-signal conversion the power efficiency of SAR ADC is good, but it have a problem for small signals it suffering from meta stability and noise of comparator. This digital-slope ADC by using the ramping and continuous comparator it will change the signal voltage-domain to a time-domain , and in the end performance of quantization level in the time domain. The low noise of this design is inherited from the dual slope ADC as a result of which it achieves good noise suppression.

Hua Fan et al.[26] reported a design implementation using two way switching method for DAC, for binary-weighted capacitor array SAR ADC, in this design SNR and SFDR of the SAR ADC is improve by averaging and rotating but without using redundancy method. From this methodology static linearity is decreased. And when redundancy method is used with averaging and rotating it is improve the linearity but reduced the SNR. Both method demonstrate the application for 14_bit SAR ADC by Monte-Carlo run.

Wenjuan Guo et al[27] has reported a design for Theory for compressive sensing . It states that to save the power conversion rate of the SAR ADC is reduced. When conversion rate is reduced signal sparsity is exploited. To limiting the overall power consumption previously designed CS require the analog based CS encoder. This proposed design is used fully passive switched _capacitor based CS framework that is directly enclose CS in SAR ADCs. This proposed method is operated in two mode only one is nyquist mode and another CS mode. In CS mode SAR ADC quantized the input for sampling is four times and also reducing the conversion rate, by the method circuit is consume power four time then nyquist mode. So nyquist mode can be considered to be better among the two of them. Technology used in this design is 130nm. At 0.8 supply voltage power consumed by nyquist mode is 19.2uW and in CS mode 5uW at sampling speed is 1MSPs.

Baozhen Chen et al.[31] reported a design implementation based on passive-charge-sharing SAR ADC to get linearity for 16-bit. The reason for poor linearity during on-chip passive charge sharing is unregulated reference voltage is used in bit trail.in this proposed design resolve the poor linearity problem in SAR ADC when it use the passive charge technique. This proposed method is here with one reference capacitor with per bit and small switch that able to highlight reference voltage is depends on the signal is drop when SAR ADC done the conversion and bit weight is set. The ADC to 16-bit linearity is further calibrated by calibration technique.Being proposed here. This proposed design is achieve maximum signal to noise ratio by the sampling on the output of DAC which is produced by capacitor array. In this design the obtainable result is ± 0.8LSB non linearity at the sampling frequency of 1MSPs.

Junbo Shim et al.[32] reported a design implementation on 16-bit amplifier-free second order incremental ADC for sensor applications. Proposed design based on the transfer of charge operation for SAR that used efficient power. This operation is consume dynamic power only.at the place of trans conductance amplifier. Which is utilize high static current in operation. Proposed amplifier thus succeeds in achieving consumption of low power at low frequency. Also on the top of the it the charge redistribution period of capacitor DAC in successive approximation ADC based integrator. That is divide in time interleaving way, capacitor DAC share first and second both integrator.in this proposed design using 180nm technology in fabrication with 0.24uW power consumption at sampling speed is 10KHz. This proposed design is useful for the sensor application which is required low power consumption.

Jian Luo et al.[33] presented a report on designing a low-power with 12-bit and the sampling frequency is 100-MS/s for an asynchronous SAR ADC. Enhancing performance of an ADC there so many technique has been introduced. Reduce the settling time for digital to analog converter With utilization of hardware that is allowed by a capacitor array which is non-binary is maintain. For this array capacitor total capacitance is 394fF. non–linear behavior of a capacitance is resolved by non-linear capacitance correction method, the suggested method describe in this report which is useful for the comparator and a small capacitor is use. Using glitch removal technique for latch output ensured the speed and accuracy of the used comparator design at low power supply. When reported SAR logic is compare with traditional SAR , speed of operation of SAR logic is improved by 75%. Fabrication is done by 40nm technology with 0.9V power supply. And here sampling Rate for this SAR ADC is 100MSPS.power consumption is 2.6mW with 14.6fj/ conversion- step FOM.

Chao Wu et al.[34] presented a report on the pipelined-SAR ADC. It this design speed is improved, sampling rate of 300MSPs is achieved using single channel and with the help of split capacitor.
To minimize the power dissipation calibration method is used.it this design SNDR 63.6 dB at 10MHz input frequency. Achieved power efficiency is 34fJ/conversion speed.

Table 0.1 Comparison of performance of various SAR ADCs

Ref.	power supply (v)	Sampling Frequency(Hz)	Resolution (Bit)	ENOB (Bit)	Power (W)	FOM (fJ/con)	CMOS Technology (nm)	Area mm2
[11]	0.5	40K	13	11	1.47u	17.9	130	-
[13]	0.35	200K	8	6.4	84.7n	5.04	130	-
	0.6	3M	8	6.53	3.44n	12.5	130	
[19]	-	50M	13	11.48	1m	6.9	65	
[23]	-	10k	14	12.5	1.98u	-	-	0.28
[24]	-	104M	12	-	.88m	7.3	28	.003
[25]	0.9	100M	12	10.41	0.35m	-	-	-
[32]	-	10K	16		0.24u	-	180	-
[33]	0.9	100M	12		2.6m	14.6	40	-
[34]	1.2	300M	12	10.27	12.5	34	65	-

CHAPTER 2
COMPARATOR DESIGN

2.1 INTRODUCTION

Now a days in analog world everything is going to be digitalized. So there is requirement to convert analog signal into digital signal. This building block play the important role in all kind of analog to digital converters. For the any comparator power consumption, speed, gain value, offset value are the important parameter so according to accomplishment of parameter we can be choose the comparator design. Basic work of the comparator is compare the input signal voltage with the reference signal voltage and generate the output according to comparison value it will be high or low. Comparator produces the output signal that is not dependent on common mode voltage and equal to the distinctness of two input voltage. If we talk about the basic comparator design the at the positive terminal applied the input voltage (V_{in}) and at the negative terminal we provide the reference voltage (V_{REF}) . So output logic can be at logic high and logic low depends on the comparison of both input voltage and reference voltage. Usually, comparators are difficult to figure out because static comparator has high power consumption and low speed but its offset value is less. And opposite to static comparator the dynamic comparator has low power consumption, high speed, full rail to rail output, and input impedance is also high.

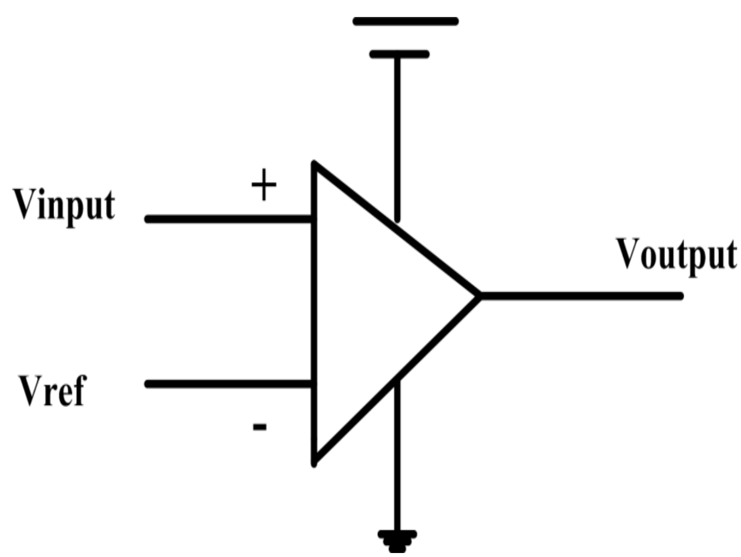

Figure 2.1 Basic Block of Comparator Design

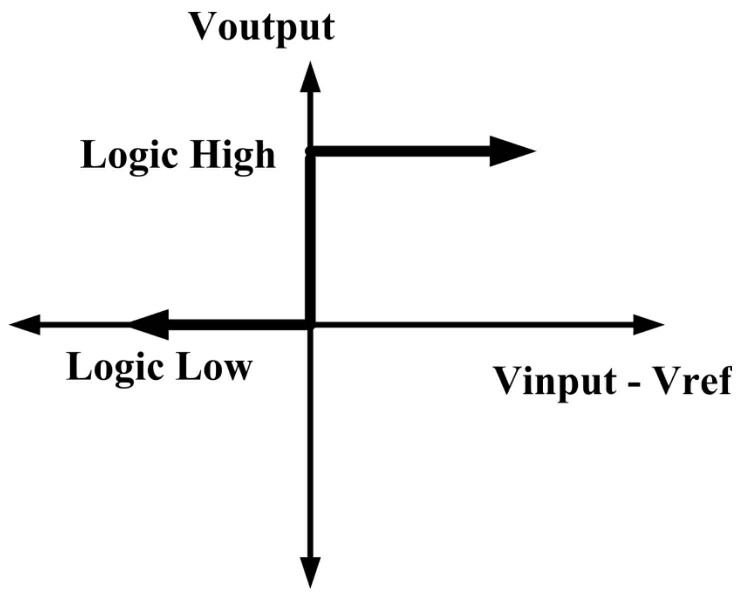

Figure 2.2 Transfer Characteristics of an Ideal Comparator

Mathematically it is define as

If $V_{IN} < V_{REF}$ then output voltage (V_{OUT}) = logic low (or 0)

If $V_{IN} > V_{REF}$ then output voltage (V_{OUT}) = logic high (or 1).

2.1.1 Comparator Characteristics

The term static and dynamic characteristics of the comparator are define according to its performance [28]. Static aspects consist of gain value, noise and resolution bit, and input offset voltage. And dynamic aspects mainly consists of speed and propagation delay. Power consumption is main design factor for comparator.

2.1.1.1 Offset Calculation:

The input offset voltage value of comparator emerge from contradict in same device . so due to is reason the comparator produce random change in output that is reverse of comparator output. Comparator output changes from one logic level to second logic level as early as input difference is zero.

If output does not make any change before difference of input catch out the value of offset voltage. Figure 2.3 shows this difference. Offset voltage cause the problem for the designer as it vary in circuit to circuit randomly and prediction is hard.

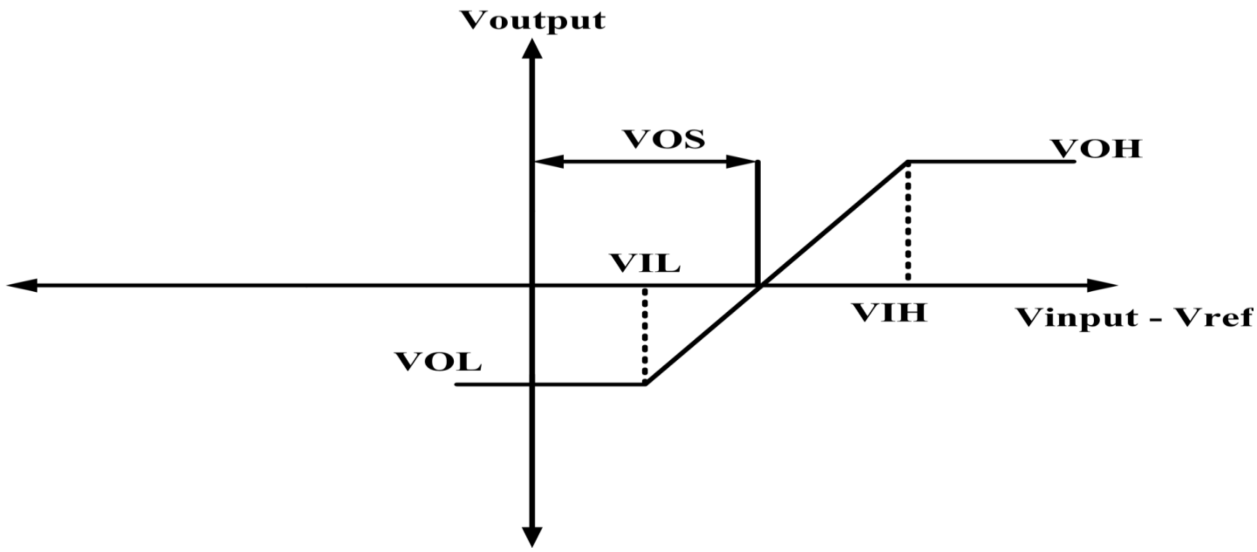

Figure 2.3 Transfer Curve of Comparator Contain Input Offset Value

2.1.1.2 Resolution

In the voltage of the input signal smallest difference is define by comparator that give logic high (1) or low(0) called resolution. The confine factor noise and input offset voltage both are affect the resolution. The minimum of ADC resolution is voltage of least significant bit (V_{LSB}). Comparator able to find out the V_{LSB} .

For N-bit ADC voltage of least significant bit is $\frac{1}{2^N}$.

2.1.1.3 Gain

The gain value is characterized as output value is change when input value is change. Input change denoted by ΔV, where ΔV is tends to zero. Comparator voltage gain is composed by

$$Gain = A_V = lim_{\Delta V \to 0} \frac{V_{oH} - V_{oL}}{\Delta V}$$

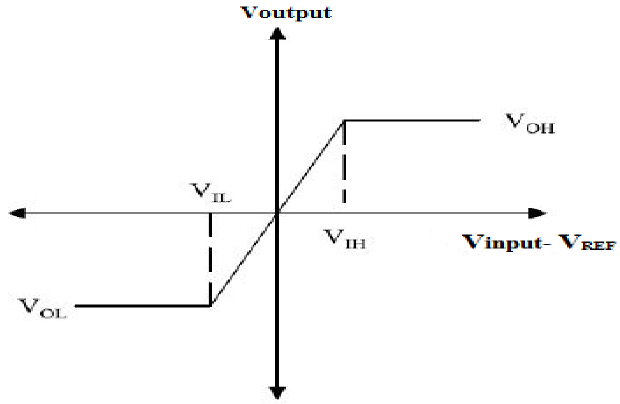

Figure 2.4 Transfer characteristics of comparator with finite gain

Above mention figure 4.5 show the Dc characteristic's practical value that is :

$$A_v = \frac{V_{oH} - V_{oL}}{V_{IH} - V_{IL}}$$

Where: V_{IH} and V_{IL} serve as input voltage difference that is require for the output saturation on its lower limit and upper limit. Also input common mode voltage range (ICMR) for comparator when comparator work properly .

2.1.1.4 Propagation Delay

The basic functionality of comparator is compare values of both the input signal and change the output when one input is larger than another. But at same time output cannot changed , its required some time for changing its value that time so this time known as propagation delay. This delay express the speed of comparator means how much fast the comparator change the response according to change in input value. The delay is present due to internal circuitry because signal inseminate through the internal circuit. Propagation delay also degrade the analog to digital converters performance. It is average time value of the rise time of output edge and fall time of the output edge.

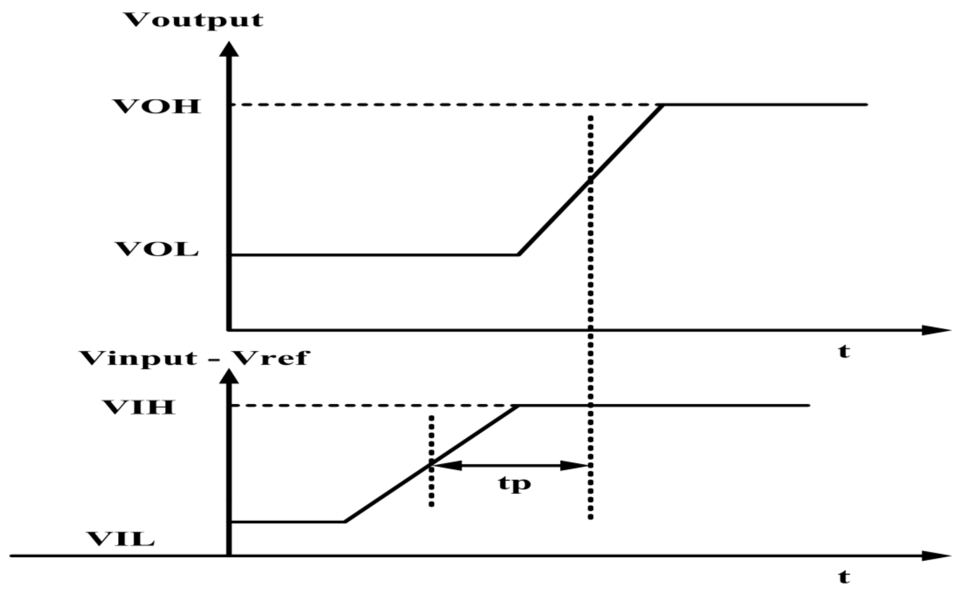

Figure 2.5 Propagation delay of comparator

Rise time propagation delay is defined by progression of the output when it is switch from 10 to 90 % of highest value. Fall time propagation delay is represented by changeover the output when it switch from 90 to 10% of highest value. According to circuit design definition of rise time and fall time is different it could be 30 to 70% or 70 to 30 % .

For the calculation it takes the middle value (50%) point of input –output change. Propagation delay is denoted by t_{pd} and the mathematical representation of delay is:

$$t_{pd} = \frac{T_{Rise\ time} + T_{fall\ time}}{2}$$

Where $T_{Rise\ time}$ is define rising edge value and $T_{Fall\ time}$ is define falling edge value. In clock base circuit like comparator where its propagation delay computed at 50 % changeover at point of output value and clock signal in other word difference between the high output level and low output level ($V_{OH} - V_{OL}$) .

2.1.1.5 Power Dissipation

Power dissipation is main factor for the all type of circuit. Similarly, power dissipated by comparator also critical design specification. Analog circuit consumes more power over the digital circuits. Though, digital MOS base circuit compared with analog MOS Base circuit.

In digital design circuit total power dissipation is specify the summation of the short-circuit power, dynamic power , and leakage power.

Mathematical term used for total power is P_{TOTAL} than is figure out by :

$$P_{TOTAL} = P_{Short_{circuit}} + P_{Dynamic} + P_{Leakage}$$

Dynamic power is also known as the switching power. It is depends on the switching activity of the circuit which arise when capacitor is fully charged or fully discharge. Where short-circuited power is dissipated due to short circuit current which flow through circuit from VDD (supply voltage symbolized by VDD) to ground. Leakage power dissipation when circuit is open and due to external or internal environment or factor some small amount current flow through circuit called leakage power . In ultra-sub micron technology leakage power play a major role. But in 180nm technology it can be neglected so easily. Here we use 180nm technology so we can neglect the leakage power and the main power dissipated due to short- circuit power and dynamic power.

2.2 BASIC DIFFERENTIAL CIRCUIT

In analog integrated design differential configuration amplifier most commonly used building block. Input stage of each operational amplifier is a differential amplifier. For high speed of application BJT differential amplifier is basic amplifier. For example emitter-coupled logic circuit.

Firstly vacuum tube is invented and afterword the basic differential pair was implemented with discrete type bipolar transistor. However, differential pair become very popular in both MOS technology and bipolar technology because in integrated circuit it was advent.

There is two reason behind using the differential pair in fabrication of ICs. First one is matching between both side of circuit performance get affected by of the differential pair. Integrated circuit fabrication able to arrange the matched device whose specification track over broad area of alteration in environmental circumstances. Now second one is differential pair use more number of component as compare to the single end circuit due to its very nature. Opening of huge no of transistor at comparatively low cost is main significant assets of the integrated circuit.

Reason behind using differential pair instead of the single ended circuit. Differential pair is less sensitive in interference and noise as compare to single ended circuit. And second preference is due to is differential configuration allow to bias amplifier and couple amplifier stage well balanced without using coupling capacitor bypass capacitor which is used in discrete circuit amplifier design.

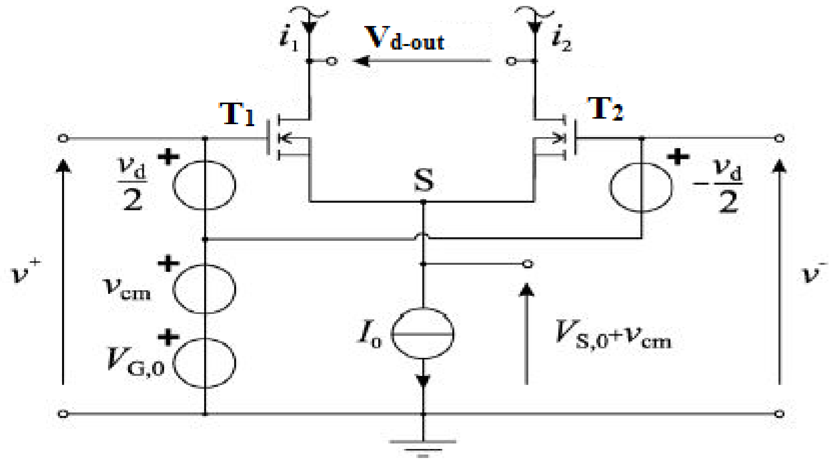

Figure 2.6 The basic MOS differential pair configuration

Differential pair consist of two matched transistor T_1 and T_2 , that's source are connected closely and biased by a constant current source *I*. For this differential pair we take a assumption that its output resistance is infinite and the current source is ideal. As shown in figure both side of drain is connected to positive power supply with resistance R_D. For the any type of load. it is important that the MOSFET does not enter in the triode region. Both transistor T_1 and T_2 are identical. And constant current source is utilize to bias both matched transistor goes in the saturation region. Output current i_1 and i_2 is flowing through transistor T_1 and T_2 . Both transistor not dependent on common mode input voltage.

The CMOS differential pair follows various problem like ICMR, power dissipation, low power supply, output voltage swing. [29-30]. To overcome these problem analog comparator with digital designed based is introduce.[28].

2.3 STRONG ARM DYNAMIC COMPARATOR

Strong arm dynamic latch comparator is broadly use as sense amplifier. A comparator or strong latch containing high sensitivity is known as "Strong Arm ". Strong Arm dynamic latch has become well known with three reasons:

- It is produce full swing output .
- It absorb zero static power.
- Its input mention offset emerge from generally one differential pair.

To get better performance in terms of that is speed and low power , a lot of research have been done in the field of dynamic comparator. This thesis report also used the existing comparator with different transistor sizing to get better resolution and high speed in successive approximation register ADC.

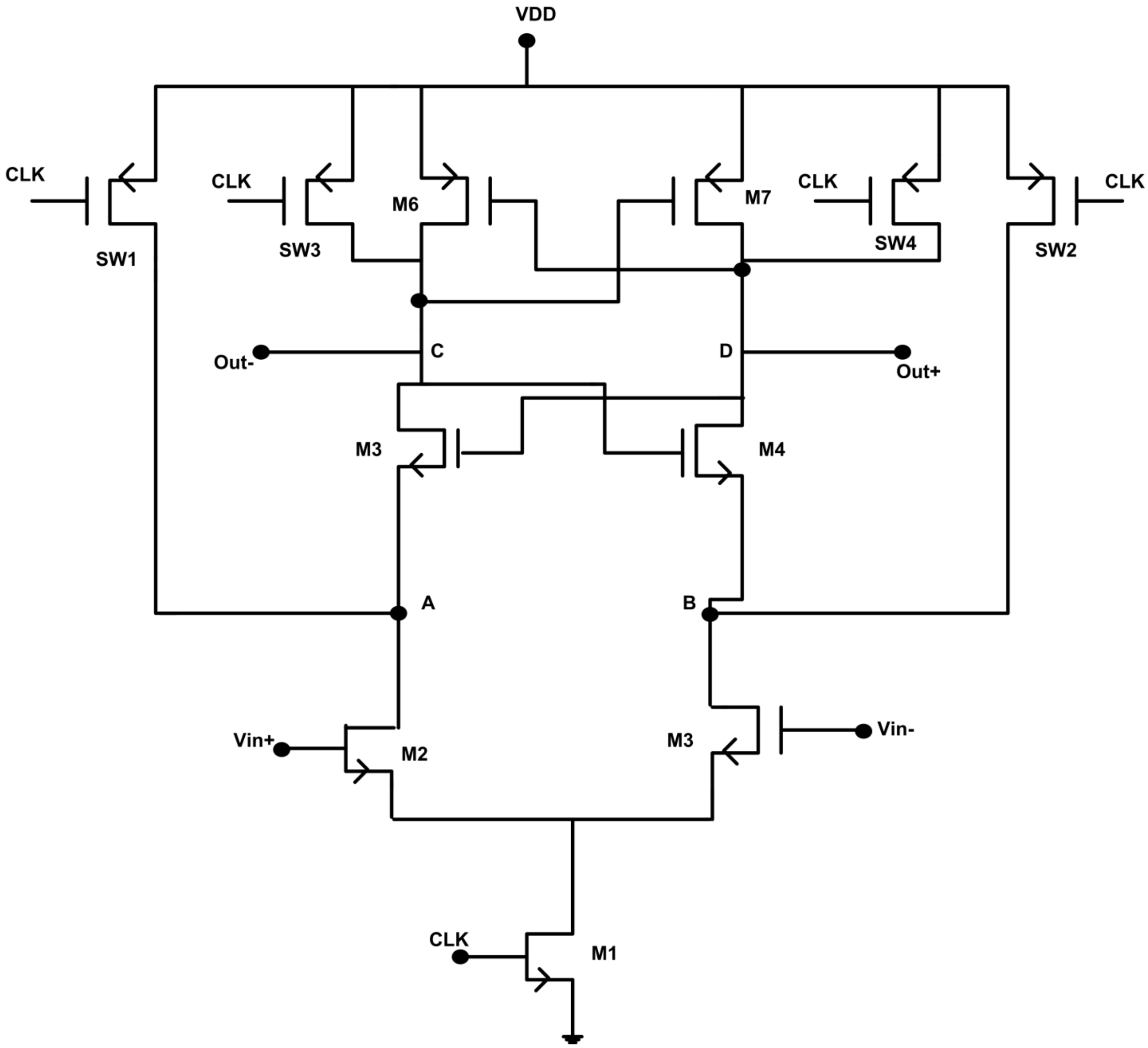

Figure 2.7 Circuit diagram of strong Arm latch comparator

2.3.1 Basic Operation Of Strong Arm Latch Circuit:

This strong arm dynamic comparator contain M1-M2 and M3-M4 two cross coupled pairs, And M5-M6 is one clock based differential pair, SW1-SW4 four precharge switches. The comparator provide full swing output at the node C and D due to Vin – and Vin+ respectively . we explain the operation of comparator in four stage:

First stage when clock is low ; differential pair M5-M6 are in off state so node A,B,C and D are charged up to VDD. And switch SW1-SW4 are turn on and capacitor C_A, C_B ,C_C and C_D, fully charged. The cross coupled pair transistor M1-M2 and M3-M4 are open circuit. When we plot graph between VDD and time V_A and V_B decrease with time and slope of V_A slightly greater the V_B .

In second stage when clock goes high ; than switches SW1-SW4 are turn off and transistor M6-M7 turn on and tracing a differential current in fraction of Vin+ - Vin-. Initially M3-M4 turn off and the differential current flow through C_A and C_B . With allowing $|V_A - V_B|$ to evolve and by chance exceed $|V_{in+} - V_{in-}|$. This stage provides voltage gain, and this stage called amplification mode. Tail current is constant during this time period.so we can conclude that the relation

$$|V_A - V_B| = \left(\frac{gm_{5,6}\,|Vin_+ - Vin_-|}{C_{A,B}}\right) \times t$$

Where : $gm_{5,6}$ is the small signal trans conductance of the comparators transistor M5-M6 , $C_{A,B}$ = C_A= C_B .

While V_A and V_B drop to VDD- V_{thn} , transistor M5-M6(cross coupled NMOS transistor) turn on and these transistor allowed M1-M2 transistors small portion of drain current flow from C and D. comparator run for $(C_{A,B}/I_{CM})V_{thn}$ seconds for amplification mode. Voltage gain for this stage is:

$$A_V = \frac{g_{m5,6} \times V_{thn}}{I_{CM}}$$

Nature of this circuit can be analyzed using third stage. In which the crossed coupled NMOS transistor M3- M4 turn on and differential pair M5-M6 generate two differential current ΔI and -ΔI.

Output voltage V_C and V_D continuously fall till both are not reached at | VDD- V_{thn} | at that point transistor M1= M2 turned on. During this period comparator enter in fourth stage and when we plot the graph between VDD (y-axis) and time (x- axis) the all four node voltage A, B ,C, D and we observe that V_A and V_B decreases with respect to time and also we can see slope of V_A is larger than $V_{\mathbf{B}}$. When we draw a line at both axis where on y-axis we take the point | VDD- V_{thn} | and on x-axis we take time than result is Slope of V_A above the point | VDD- V_{thn} | and slope of $V_{\mathbf{B}}$ below the point **.** and another one is when positive feedback is applied these transistor finally import one output voltage V_C reached out at VDD and another one voltage V_D go down to zero.

In strong arm dynamic comparator used each transistor PMOS and NMOS is play important role. Rather than the transistor M5,M6, M7 remaining transistor also serve useful purpose in device.

Here we can see to neglect the static power drain in fourth stage M3-M4 transistor are in cut off region and a DC path between VDD and ground. Here we applied a differential voltage intending 80mv to 120mv and common mode voltage approximate 600mv-700mv. Clock is applied at transistor M7 according to differential input voltage output voltage V_C fall and V_D rise , M1 transistor turn off , M2 is on working and its gate connected to ground and input V_{in-} is applied to M6 therefore direct path for the current from VDD to ground. M1-M2 ideally retain the output voltage high level VDD. Without these transistor if difference of input is small , CM discharge at C or D would produce a degrade level.

Switch SW1 and SW2 show two performance: a) erase the past phase at node A and B, decreasing offset voltage, and b) at these nodes organize an initial voltage of *V*DD, enabling amplification before transistors *M*5 and *M*6 enter in the triode region. The topology differentiate both points . During the primary amplification switches *SW*3 and *SW*4 precharge *C* and *D* to *V*DD, confirm that *M*1 and *M*6 remain off and the offset negligibly raise. The strong arm dynamic latch for about half of the clock period produce invalid outputs ($V_C = V_D = V$DD) .

For the ensuing logic to describe the outputs correctly, an NAND based RS latch pursue the circuit. Here output of dynamic comparator voltage V_C and V_D is input to the NAND latch and it is produce the output for the SAR ADC terminal result. According these results bit conversion start with clock transition.

The power absorbed by the Strong arm dynamic latch mainly the charging and discharging of the capacitors. therefore roughly power is

$$Power = F_{CLK}\left(2C_{A,B} + C_{C,D}\right)VDD^2$$

Where F_{CLK} is the frequency of the clock , $C_{C,D}$ is output node capacitance and $2C_{A,B}$ capacitor of node A,B and here the factor of 2 used due to charging and discharging of the capacitor in every clock cycle.

This is the conceptual idea of working now discus about the practical aspect then firstly applied the clock at transistor M7 and the clock period is 32ns and positive edge is 1.8V and lower value is zero. Clock is applied at four switch SW1 , SW2, SW3 and SW4. This clock cycle decided by according to the proposed ADC sampling frequency. Here sampling frequency is 31.25MSPS.

At the input terminal of this comparator we applied the digital to analog converter output it is sampled output at positive terminal of the comparator the input is positive sin wave with sampled value and at the negative terminal also applied the sine wave with negative amplitude. Now from above working when negative clock is applied then value of positive sine wave is greater the it is node capacitance is charge and discharge from VDD to ground hence negative input side output is at VDD. But practically it is not give the proper value of VDD, spike occur in output. Produced output not useful for ADC’s due to this reason added the circuitry in comparator that is called latch. It is give exact high and low value (1 or 0) according to input transition. For this producer Transient analysis is done.

Using transient analysis also calculate the delay and power of the comparator. In this at one terminal here applied the DC voltage or we can say V_{CM} 600mv and at second input terminal we applied sine wave with differential voltage 5mv to 600mv. To find out the delay of the comparator we compare the output of the comparator and the plot a graph with the help of the tool and the interpolate the clock at compared value according to ideal value when transition is done output also changed but practically it is not possible so we can see after the clock edge occur extra time taken by the output is called delay. And delay is reduce by increasing the differential voltage of sine wave. Power is also decreasing while increasing the differential voltage.

For the calculation of offset voltage of the comparator at one input terminal V_{CM} applied and at the second terminal a smooth ramp signal is applied. After this we get offset value in mv and to verify the value Monte Carlo simulation has to be done in tool.

CHAPTER 3

DIGITAL TO ANALOG CONVERTER

This chapter explain a detail analysis of digital to analog converter with existing and new proposed design and also discuss about improved parameter. In this section detailed analysis of digital analog converter that explain the proposed design and existing design.

3.1 INTRODUCTION TO DIGITAL TO ANALOG CONVERTER

Digital to analog converter circuit design used to convert digital data into analog value. It can be either current or voltage signal. For DAC resolution is most important design parameter. Resolution is define by using number of bits or step size.

Nyquist Shannon sampling theory states with the help of nyquist criteria and bandwidth sampled data reconstructed in perfect manner. And digital to analog converter can recover sampled data into analog signal precisely. To communicate with real world we required the analog value so if we have any digital data generated from microprocessor, FPGA, ASIC etc. also required the conversion at the end.

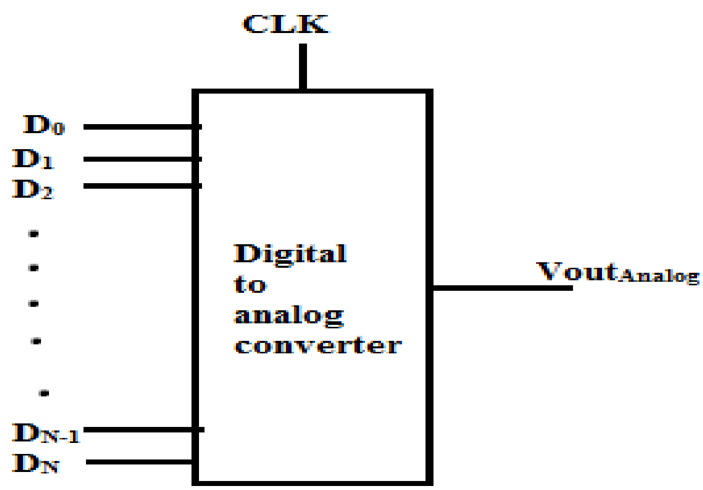

Figure 3.1 Basic block of digital to analog converter

There are so many architecture of digital to analog converter like resistive ladder and capacitive ladder according to required performance of device selection of DAC has to be done.

3.2 EXISTING DESIGN OF SAR ADC:

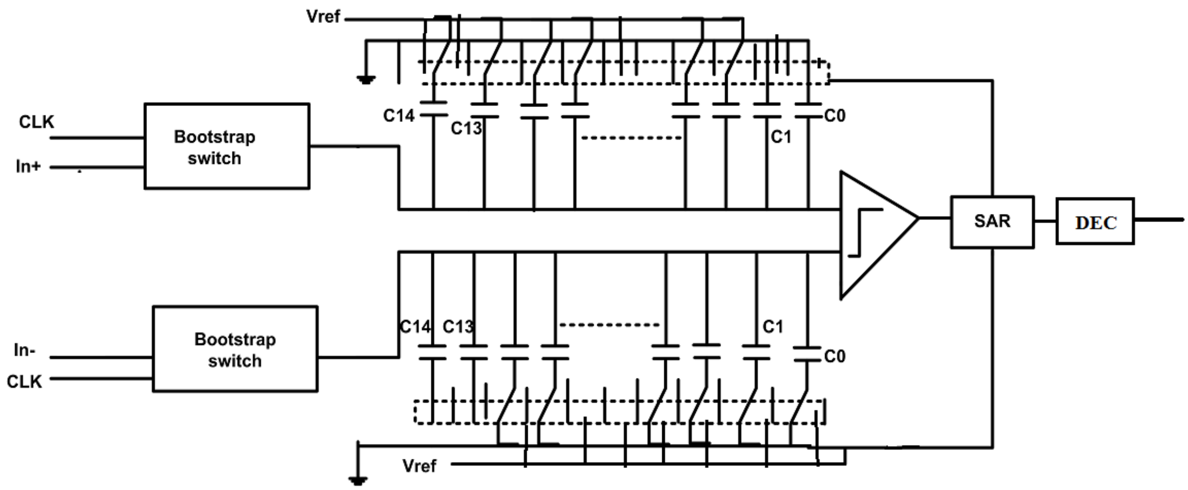

Figure 3.2 Existing design of SAR ADC

Figure 3.2: show the existing design of SAR ADC with 12 bit resolution. In this design SAR ADC has main four block a) SAR register , b) capacitor array , c) Two Stage dynamic comparator and d) digital error correction logic.

This design reported low cost SAR ADC in which two stage dynamic comparator is used. High speed with low noise and power consumption is also low. In two stage dynamic comparator composition of dynamic preamplifier and also used latch circuit. In the working of this comparator common mode voltage is decrease gradually and pre amplifier is used p-type input pair. In this circuitry when clock is high then output of pre amplifier reset to ground and when clock goes low the output is charged up to input voltage .

Here difference of two voltage is transferred by the preamplifier with clocking. Digital error correction logic consist of 10 full adder 10_D-flip flop and two multiplexer. When selection line is high last bit operation is miss and no of total cycle is reduced. Binary scaled method is used in capacitor array network with bootstrap switch but here coupling effect is cause the problem in conservation. Non binary SAR ADC produce more decision level the conventional circuit . Several digital code expressing the same input signal, it means foe different switching result leads to same , so for certain range it does not have give any error.

Comparator start comparison before DAC and the reference voltage is settled. Due to this reason time of bit cycling can be decrease. Conversion time sill can be enhance. According to bit redundancy method, a binary scaled weighting method is proposed without extra hardware circuit and compensative capacitor. Redundant range of MSB is enough to implement this design. To get more wide redundant range, more number of bit weighted from the MSB and added into LSB weighted bit. Comparator noise is also reduce in MSB bit. For the time being settling issue of DAC is ignored then maximum circuit relaxed from noise. The main advantage of this design is power consumption is less.

3.3 PROPOSED DESIGN OF CAPACITOR ARRAY FOR SAR ADC:

In this proposed design circuit a capacitor network serve as both bootstrap switch with cross coupled capacitor and capacitor array. So in this circuit a sample and hold circuit is not required for sampling. Used capacitor array is fully differential with binary weighting method. Figure 3.3 show the block diagram of proposed design.

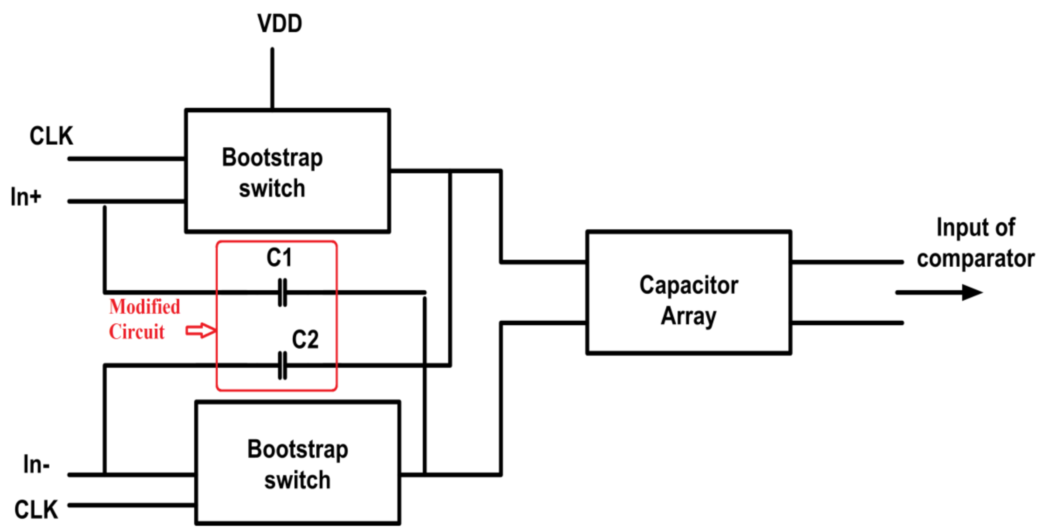

Figure 3.3 Block diagram of proposed DAC network

3.3.1 BOOTSTRAPPING IN SWITCH:

Firstly in CMOS design circuit bootstrapping is used for overcoming threshold voltage drop. In digital circuit output voltage may endure from threshold voltage drop. To reduce threshold voltage drop and get full swing output level and from this technique operating point is also pulled up. The bootstrapping circuit is organization of components knowingly designed to change the input impedance of a circuit. Using a small amount of positive or negative feedback, Usually it is promised to decrease or increase the input impedance in analog circuit design according to requirement. When bootstrapping is applied in circuit a capacitor is connected from output to biased circuit figure 3.3 shown bootstrap based switch which is used in proposed DAC design. In this maintain the switch resistance relatively constant that's why in this proposed design this circuit is used instead of simple switch. Main advantage of this circuit is provide less distorted and full output swing. Bootstrap switch have two mode one is sampling mode and another one is hold mode. In the sampling mode supply voltage is provided than precharged capacitor keeps the transistor turn on and in hold mode transistor turn off and capacitor is charged again. Bootstrap switch is used for analog to digital converter when resolution range is 8 to 12 bit.

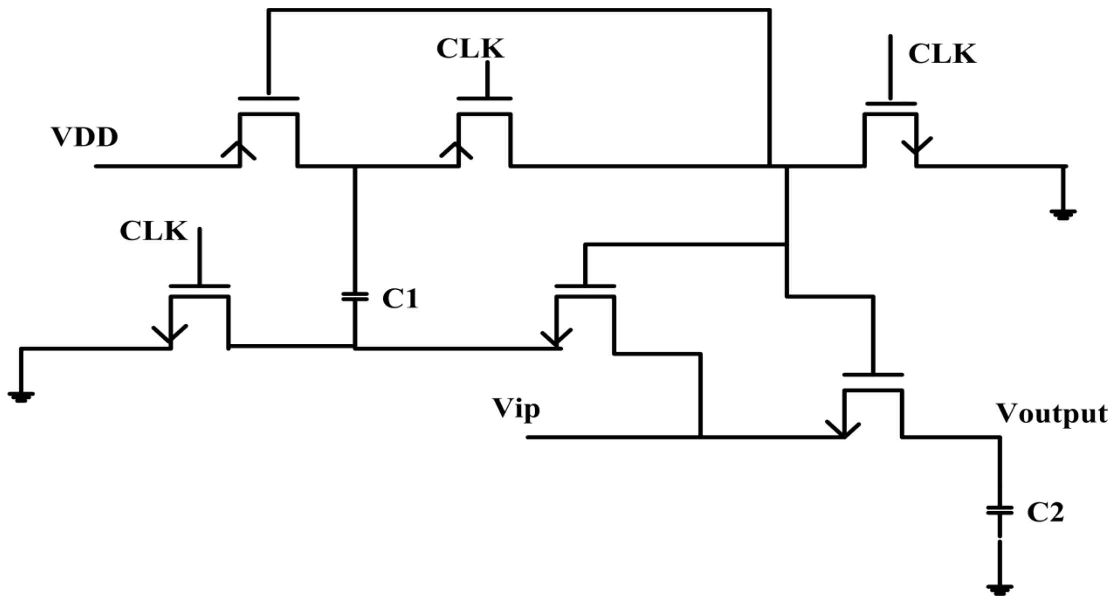

Figure 3.4 Bootstrap switch circuit

After that for above this range it will work but due to coupling effect somewhere it will have cause a problem of full output rail and also compromise with speed so to resolve this problem, cross coupling with bootstrap switch is developed because from previous design we conclude that coupling effect degrade the speed of conversion for ADC. So to overcome this problem two cross coupled capacitor is used which is increase the swing of the sampled output for higher bit resolution. Proposed design is for 14-bit so it is useful. At low frequency parasitic capacitor effect is not bother the output response but if we talk about higher frequency like MHz or GHz the it is cause the problem in design. Due to cross talk harmonic distortion and signal dependent error cause the problem in performance. Because in analog to digital converter multiple signal used to sampled at a time so there is some degree of coupling effect or cross talk due to stray capacitor. Voltage spike across the capacitor due to switching action. This voltage spike cause a problem for next voltage level because it have not that much energy and exponentially dissipate through resistance. To reduce this cross talk device needs settling time and impedance. So a new modification have to be done in design that is cross coupling. Figure:3.3 shows the cross coupling capacitance C_1 and C_2 .

3.3.2 CAPACITOR ARRAY:

Proposed design follow the binary weighting method with bit redundancy. Figure3:4 shows the Proposed design capacitor array of 14-bit which is used binary scale capacitor at the place of original binary capacitor DAC network to arrange the compensative value of voltage. Compensation method MSB bit represent difference of two power number $2^P - 2^Q$ where is MSB bit express as P = N-1. And other bit also represent as sum of two power or one power. In this method extra bit compensation is needed.

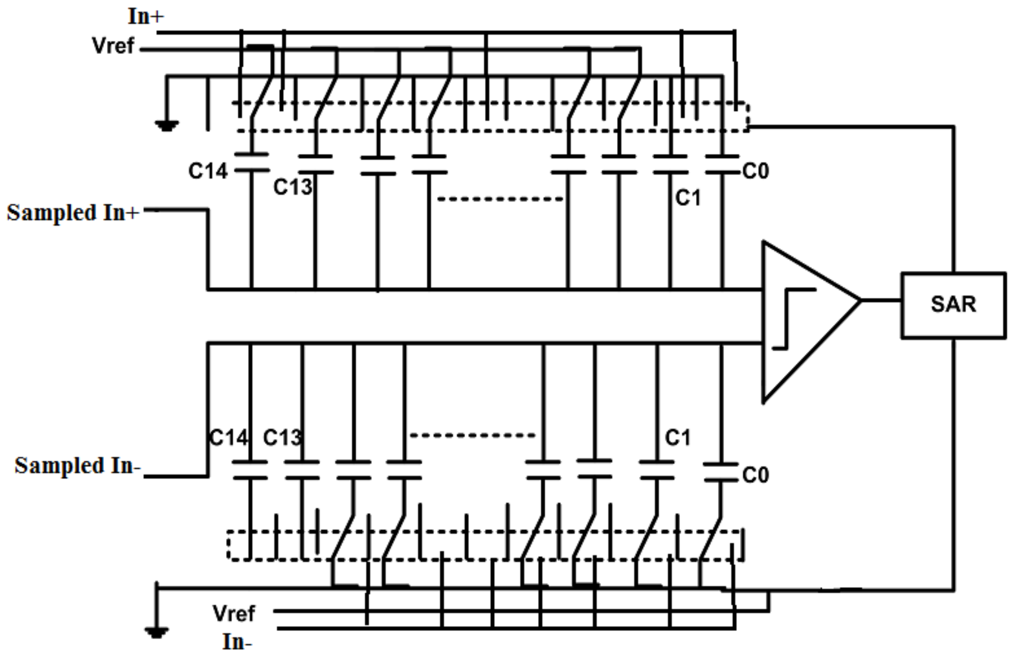

Figure 3.5 Design of proposed 14-bit digital to analog converter

Here digital output expressed as

$$D_{out} = (2^{13} - 2^{7}) \times B_{15} + (2^{12}) \times B_{14} + (2^{11}) \times B_{13} + (2^{10} + 2^{5}) \times B_{12} + (2^{9} + 2^{5}) \times B_{11} + (2^{8} + 2^{4}) \times B_{10} + (2^{7} + 2^{4}) \times B_{9} + (2^{6} + 2^{3}) \times B_{8} + (2^{5} + 2^{3}) \times B_{7} + (2^{4} + 2^{2}) \times B_{6} + (2^{3} + 2^{2}) \times B_{5} + (2^{3}) \times B_{4} + (2^{2} + 2^{1}) \times B_{3} + (2^{2}) \times B_{2} + (2^{1}) \times B_{1} + (2^{0}) \times B_{0}$$

In this design the cross coupled capacitor C_1 and C_2 capacitor value is 30f .

3.4 COMPLETE SAR DESIGNE :

Figure 3.4 show the complete design of SAR ADC in this design at the input of the DAC which is connected to the bootstrap switch a sinusoidal input signal is provided.

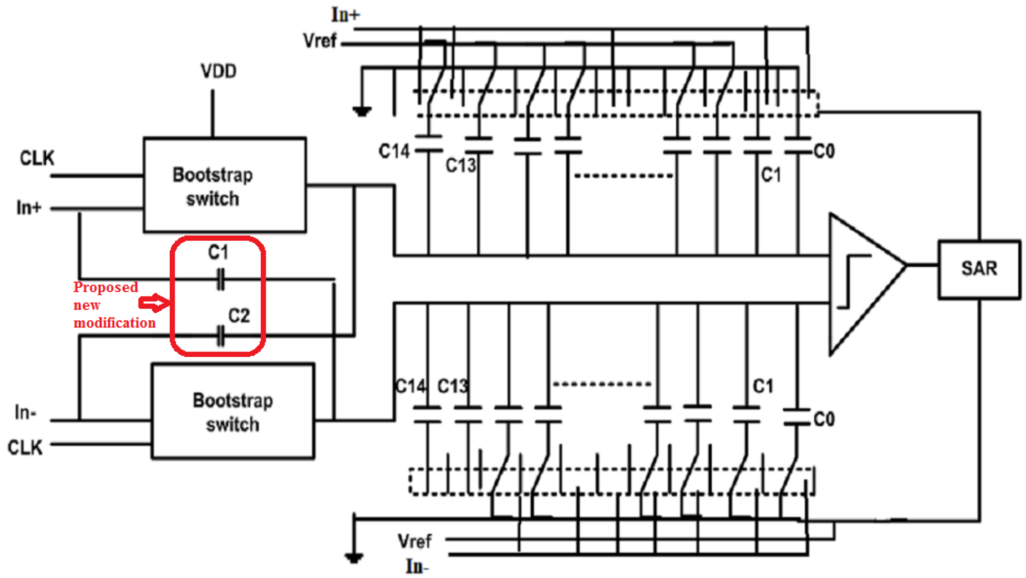

Figure 3.6 Synthesis design of proposed SAR ADC

Figure 3.6 When first clock cycle occur the MSB set to 1 and each bit is connected to capacitor array through switch. DAC produce the sampled output with respect to clock and bit. Produced sampled output is input to strong arm dynamic latch comparator. Then output produced from the comparator is input to the SAR register and according to comparator decision and clock SAR conserve the next cycle and again DAC produce the output and so on. This conservation continue until last bit of SAR is converted. In SAR ADC the total capacitance of DAC network array is 700fF. Sinusoidal input that is provided to DAC network has 200KHz input frequency with 1.8V and sampling frequency is 20MHz. clock is 50ns.

Table 3.1 Comparison Of Performance Parameter With Proposed Design

Parameter	[12]	[19]	[23]	**This Work**
Power supply(VDD)	0.5	-	-	**1.8V**
Sampling frequency(Hz)	40k	50	10k	**20M**
Resolution (Bit)	11	11.35	12.5	**13.86**
Power(uW)	1.47	100	1.98	**5.68**
CMOS Technology(nm)	130	65	65	**180**

CHAPTER 4

EXPERIMENTAL AND SIMULATION RESULT FOR SUCESSIVE APPROXIMATION REGISTER ADC

This chapter explains 14-bit SAR ADC with binary scaled weighting method using cross coupling in bootstrap switch in DAC. SAR ADC basically consist four main block : sample and hold circuit, comparator and digital to analog converter. In this section 14-bit SAR ADC designed using above mention block and also discuss various measured static and dynamic parameter. Different block of SARADC discuss in this section.

4.1 COMPARATOR:

The dynamic comparator compared voltage of the input (V_{IN}) with that is produced by digital to analog converter. If V_{IN} is greater than $V_{REF.}$ The output voltage of the dynamic comparator goes at logic high and when V_{IN} is less than the V_{REF} then the output of the comparator goes at logic low. Hence the comparator generate the output as a string of '0's and '1's that is input to the SAR register and that decide the bit conversion. The strong arm dynamic comparator circuit designed in section 2.4 which is used in SAR ADC. it is designed by using NMOS, PMOS and MOS based latched circuit.

4.1.1 Transient Analysis For Output Response

Figure 4.1 shows the transient analysis of comparator. Strong arm comparator is clock based comparator when at the both input terminal sine wave is applied with 180 degree phase shift. Here clock pulse is with 32ns period 1.8V voltage and rise time ,fall tine ,delay for this pulse is 1ps. and When clock signal is low then all capacitor C_A, C_B, C_C and C_D charged up to VDD and when clock goes high output voltage at ground.

This phenomena also depends on the input voltage also so according to which input is high output shows the transition. Here in first case V_{IN+} (for V_{IN+} is sine wave with offset is 600mV, amplitude is 600mV and frequency is 2.2MHZ) is high then according to this input in figure 4.1 output comp_outN shows the response with respect to clock signal. vise versa when V_{IN-} (where for V_{IN+} is sine wave with offset is 600mV, amplitude is -600mV and frequency is 250KHZ) is high then comp_outP shows the response as VDD and ground.

Here output depends upon the clock so with every clock cycle the output response will be changed that is not as much as fruitful for SAR ADC so here latch circuit is used which is NAND based. Once the output of comparator is produce it will be input to the NAND based SR latch. And that gives the proper logic high and logic low. In figure 4.1 latch_N(V) and latch_P(V) show the latch output.

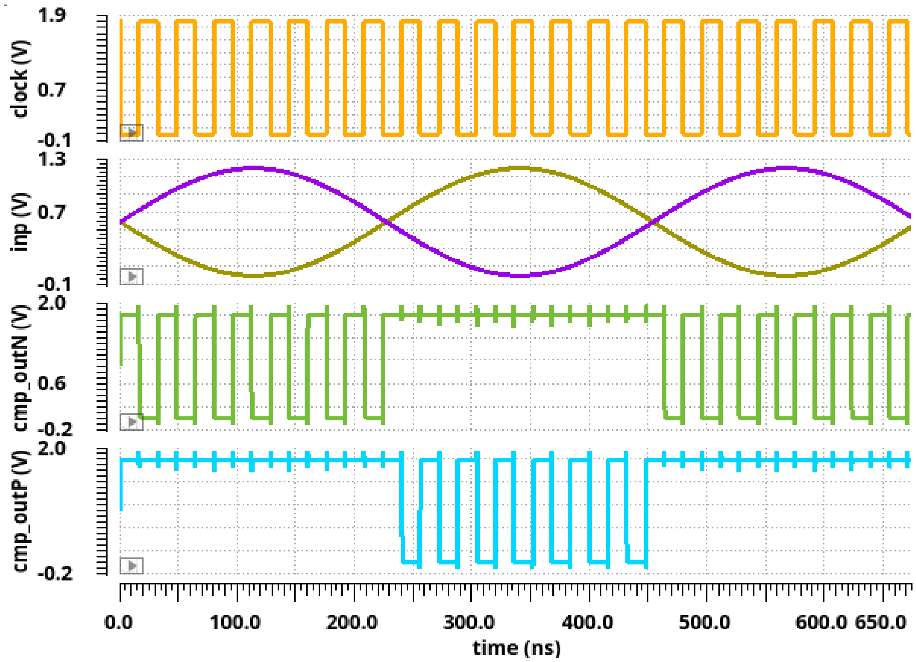

Figure 4.1 Transient analysis of comparator at 20MHz clock frequency

4.1.2 Power And Delay Analysis Of Comparator :

Using transient analysis power and delay calculation has to be done. For delay calculation at the one input terminal common mode voltage is provided and on second input differential voltage is applied and then take difference voltage VDD/2 of both output wave form. After that check output response how much far away from clock edge for example clock pulse width is 25ns and common mode voltage is 600mV and differential voltage is also 600mV at this instant the output voltage difference is occur at 25.33ns the delay is 0.33ns because output is generate at the clock edge ad that is 25ns but output is take 25.33ns so this is called delay. As difference voltage is increase delay of comparator is decrease. Delay shown in figure 4.2.

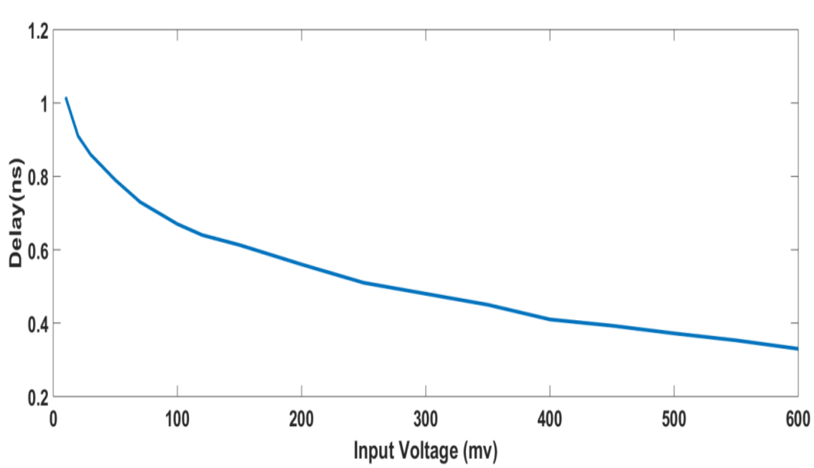

Figure 4.2 Delay analysis comparator at different input voltage

Power consumption is main factor for every device now a days. Figure 4.3 shown when difference voltage is increase power consumption of comparator is decrease.

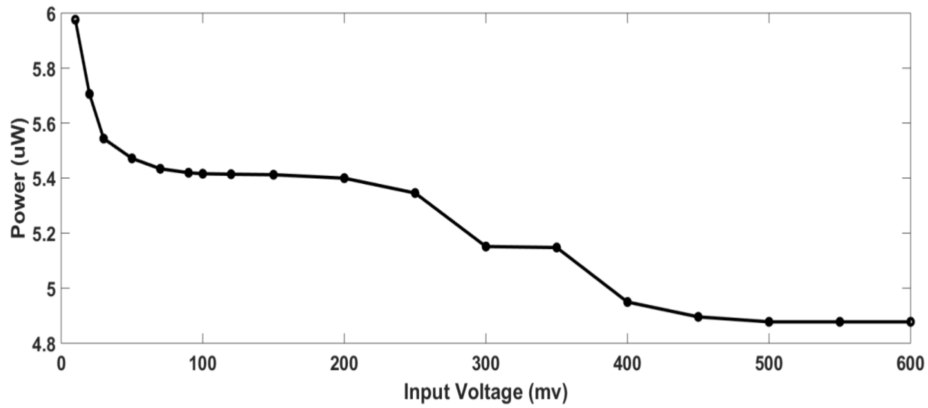

Figure 4.3 Power analysis of comparator at different input voltage

4.1.3 Noise Analysis

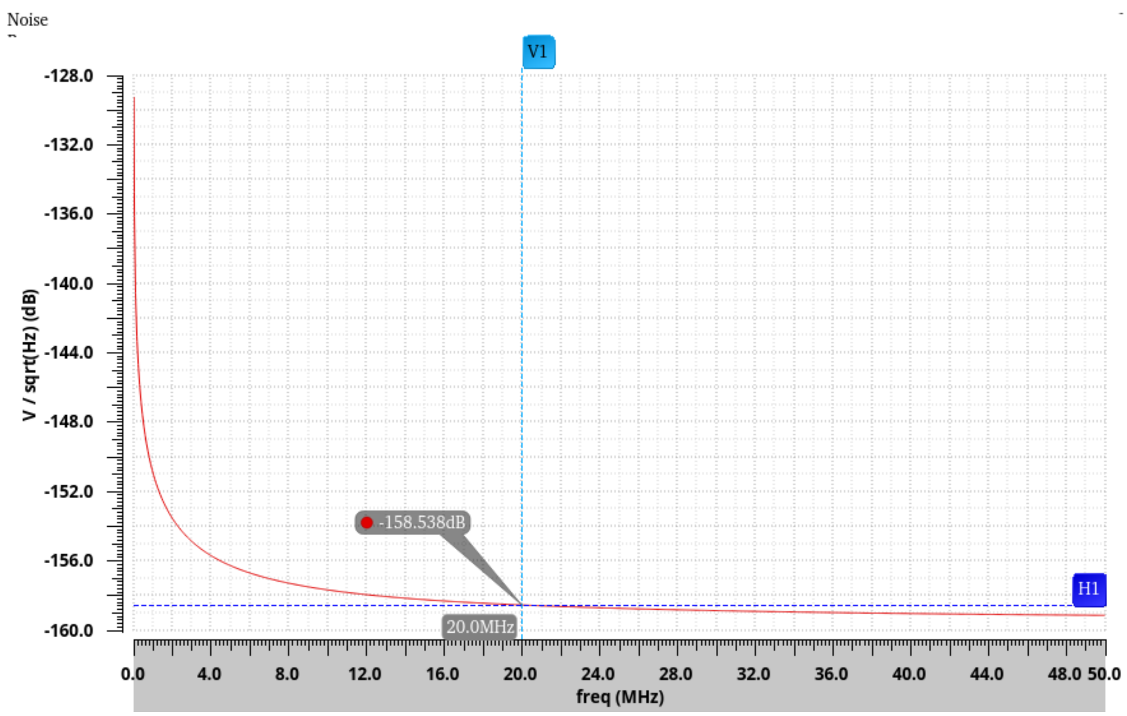

Figure 4.4 Simulation Result Of Comparator Noise At 20mhz Clock Frequency

As shown in figure 4.4 When at the both input terminal sine wave is applied with 600mV offset, ±600mV amplitude and 200KHz frequency the 50ns clock is provided then at the output terminal

-158.538dB noise is present when noise analysis is done I the range 10KHz to 50MHz. with respect to clock noise of comparator is decrease.

4.1.4 Offset of Comparator

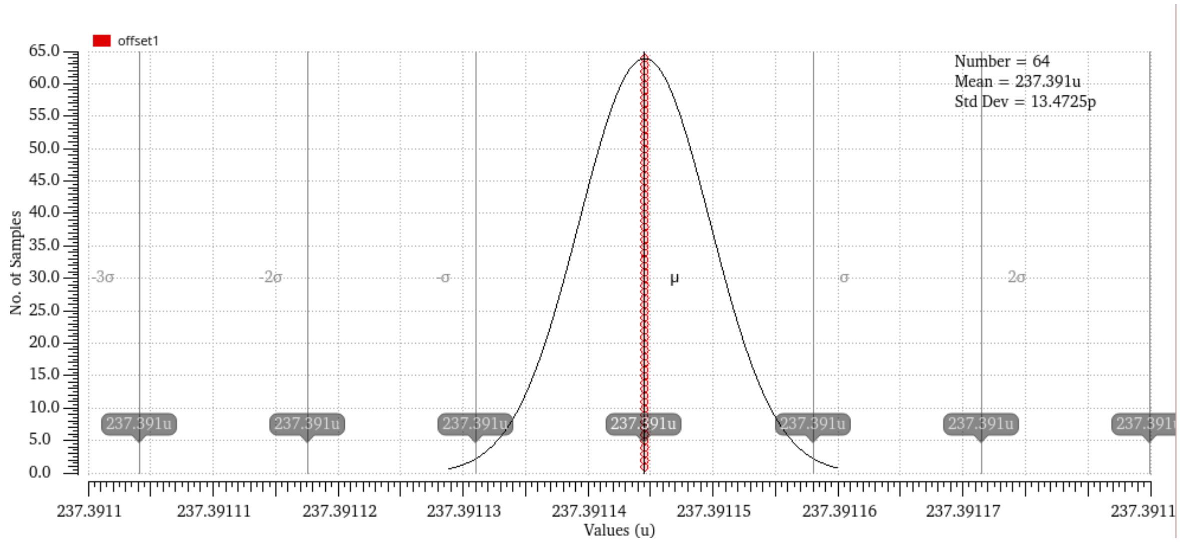

Figure 4.5 Monte Carlo simulation for comparator offset at 64 runs

As shown in the figure 4.5 the Comparator offset voltage is 237.391uV by using transient analysis And Monte Carlo analysis is for verifying the offset value. Low value offset voltage is good for design. In this design scaling of MOS produce this low offset.

4.2 DIGITAL TO ANALOG CONVERTER

Digital to analog converter is based on binary scaled weighting method capacitor array network using bootstrap switching with cross coupling capacitor

4.2.1 Transient Analysis Of Bootstrap Switch

Figure 4.5 shows the transient analysis of bootstrap switch that is sample and hold the input signal with respect to clock. In design of SAR ADC at the input side of DAC a bootstrap switch is used, which increases the performance of ADC.

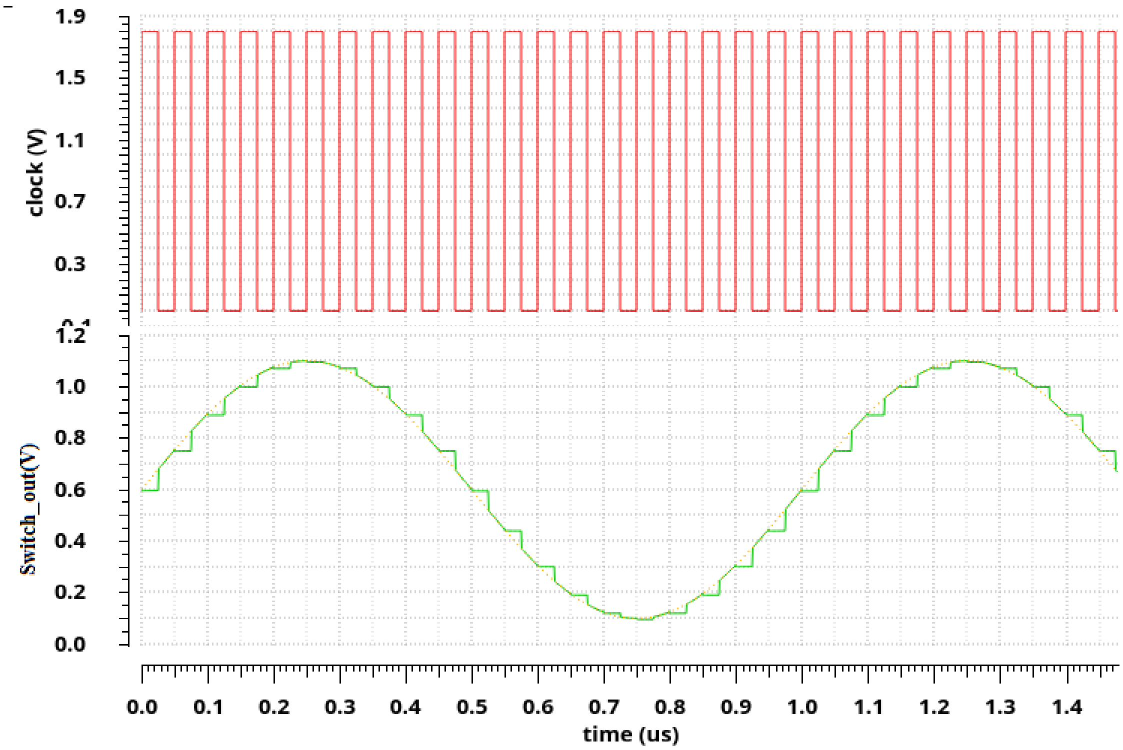

Figure 4.6 Transient Analysis Of Bootstrap Switch At 250khz Input Frequency

4.2.2 Transient Analysis Of Digital To Analog Converter

As shown in figure 4.7 the transient analysis of digital to analog converter with sinusoidal input with 20MHz sampling frequency and 250KHz input frequency. It Also shows the output of comparator which is changing with respect to DAC output.

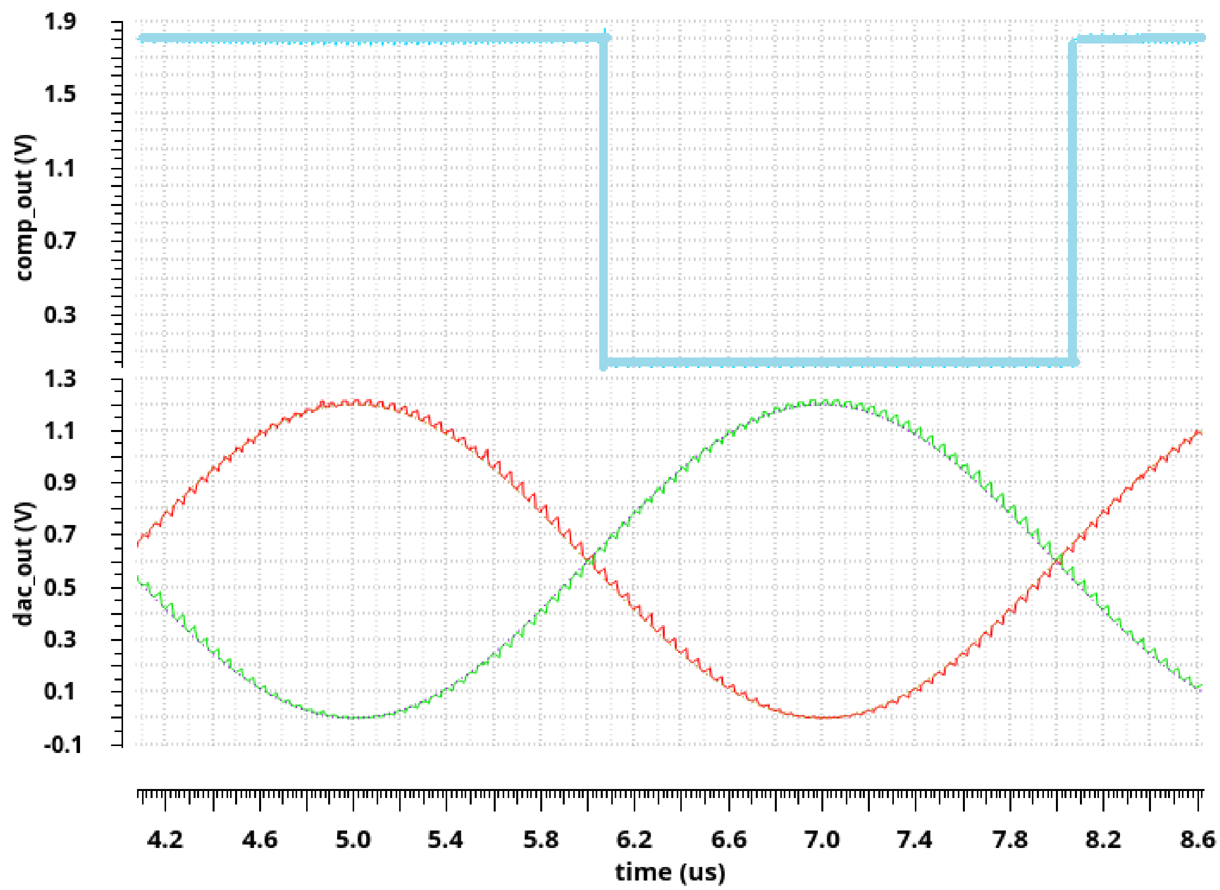

Figure 4.7 Simulation result of digital to analog converter with sinusoidal input at 250KHz frequency

4.3 SAR ADC TOP LEVEL IMPLEMENTATION

SAR register follow the binary search algorithm. The comparator output is input to SAR register and clock is also input to SAR register. When the transient analysis is done the DAC output is input for comparator and comparator produce the response that is input to the SAR register. At first clock is triggered then MSB of SAR set to one and with respect to comparator result next bit is set or reset. This conversion is stop when last bit is set or reset. And End of conservation is 1 then after one clock cycle again EOC is zero all bit reset and conservation start again. Figure 4.6 shows the SAR ADC bit from D13 to D0.

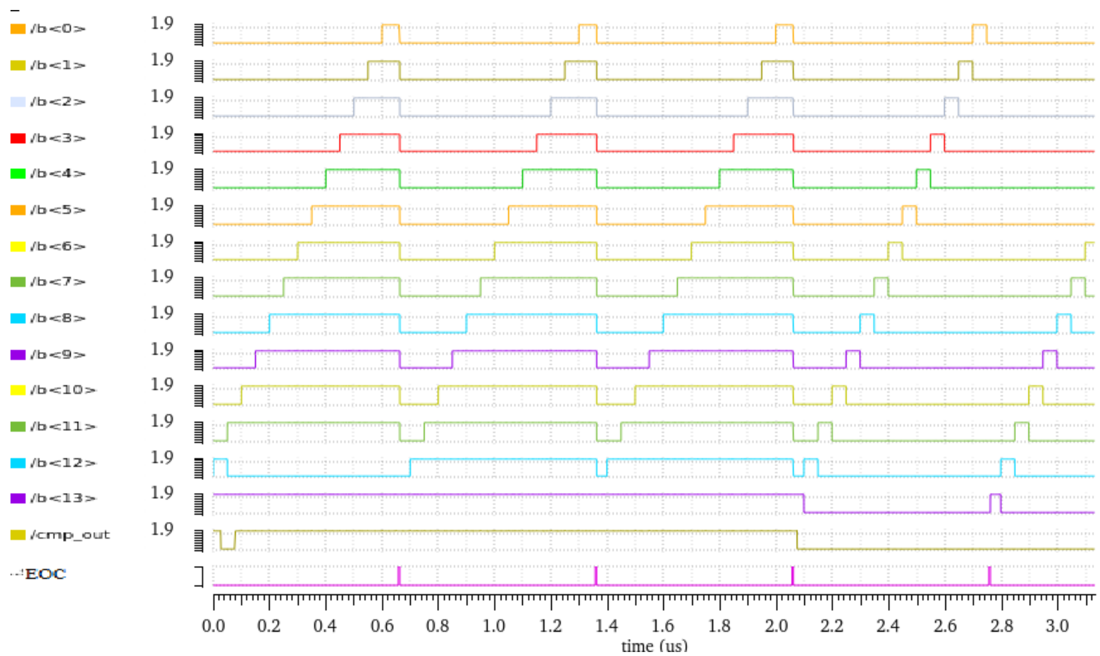

Figure 4.8 Simulation Result Of Proposed 14-Bit SAR ADC At 20mhz Clock Frequency

A differential non-linearity (DNL) error description of equal to and less than 1LSB that is Capability of a monotonic transfer function with no missing codes. Integral non-linearity (INL) is progressive sum of DNL code. The DNL and INL of 14 bit SAR ADC is measured in cadence virtuoso tool is shown in Figure 4.9. The DNL of this proposed 14-bit SAR ADC is +0.116 LSB and figure 4.10 shows the INL is +0.5LSB. The linearity is restricted between 1 LSB.

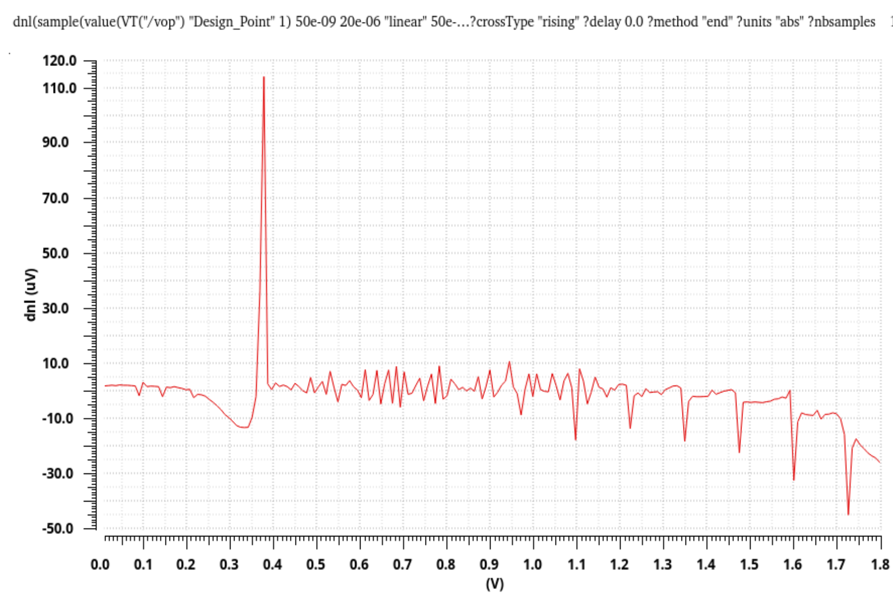

Figure 4.9 Simulation result of DNL for 14-bit SAR ADC

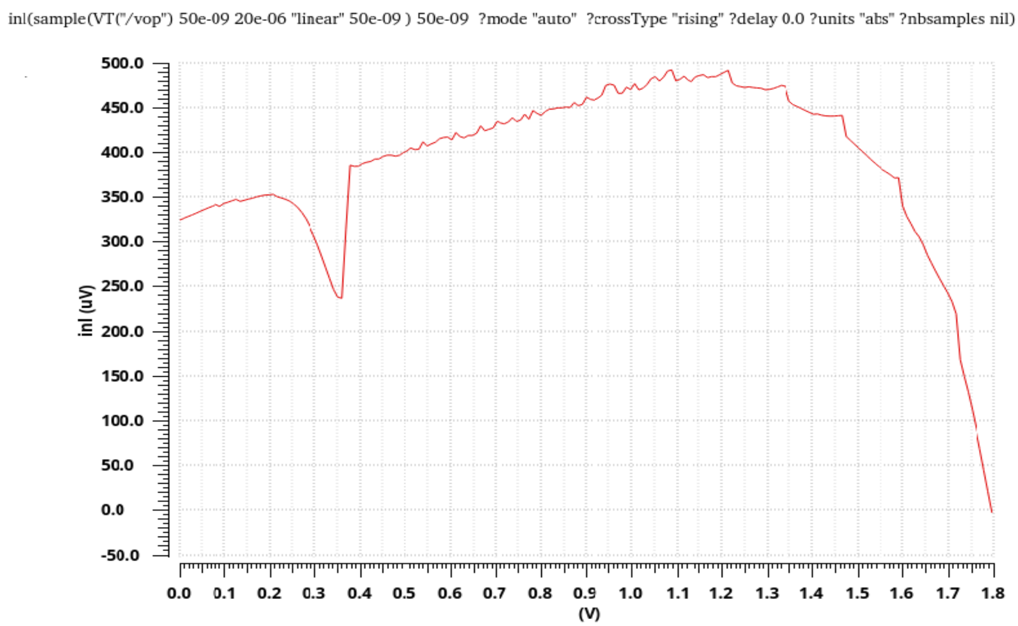

Figure 4.10 simulation result of INL for 14-bit SAR ADC

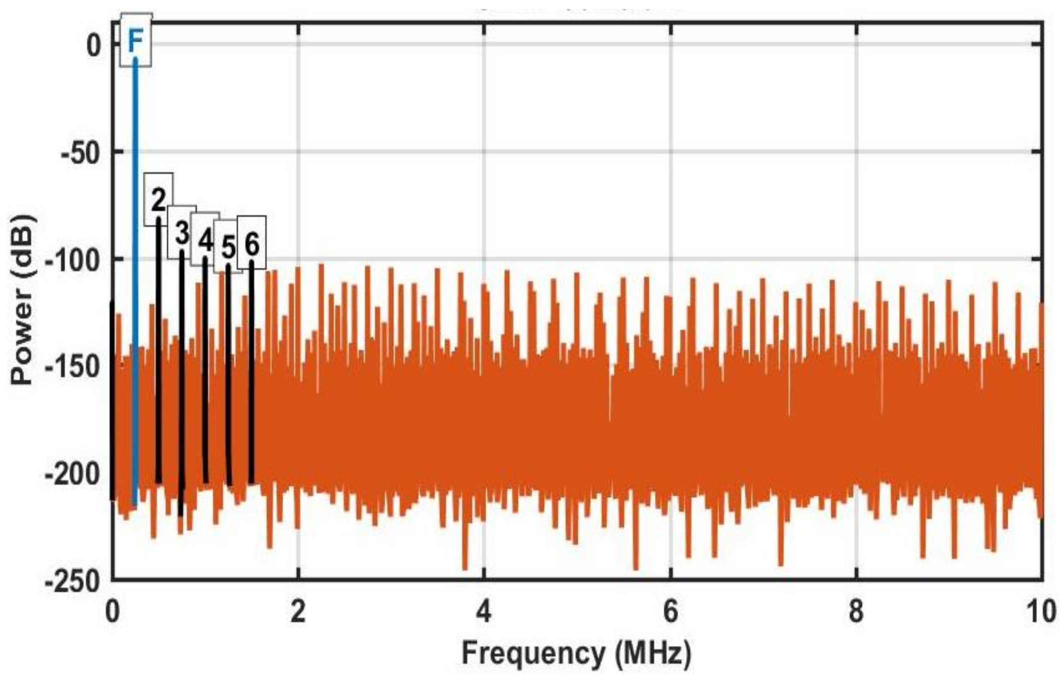

Figure 4.11 FFT of 14-bit SAR ADC with input frequency 250KHz

Using FFT spectrum a signal which is reconstructed by device for the calculation of the dynamic performance for SAR ADC. Figure 4.11 shown above is the reproduced signal spectra for 250KHz frequency of the input signal with sampling frequency 20MHz. The dynamic performance of SAR ADC is shown in Figure 4.6 When 250KHz is the frequency of input signal and 20MHzis clock frequency , the value of ENOB and SNR are obtained in this range is 13.86, 85.20dB, respectively.

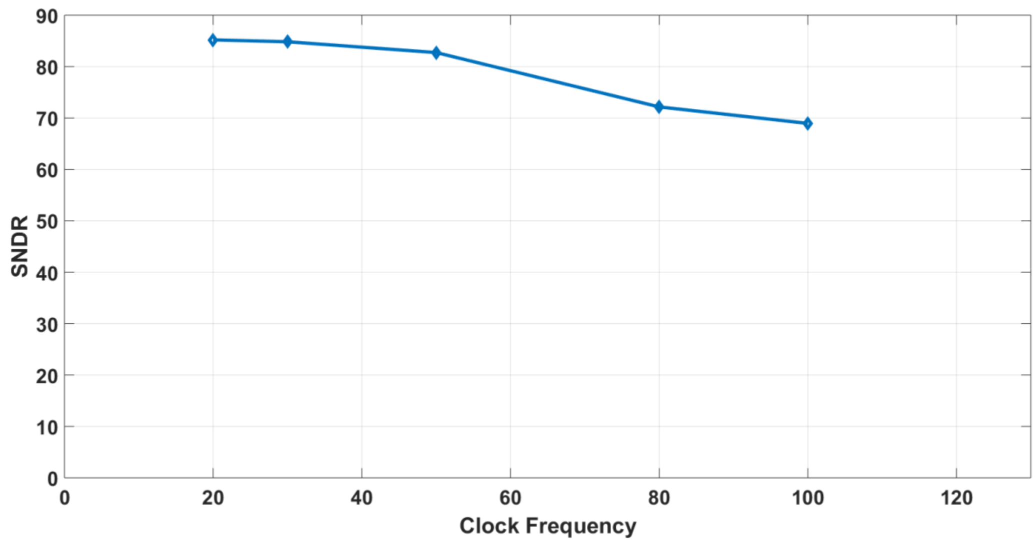

Figure 4.12 Measured dynamic performance(SNDR) for SAR ADC at different clock frequency

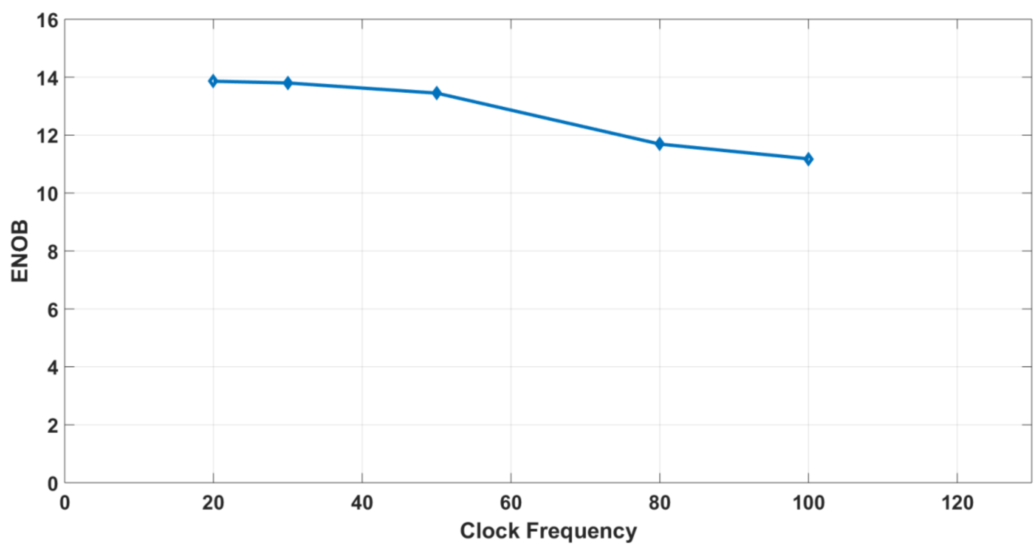

Figure 4.13Measured dynamic performance(ENOB) for SAR ADC at different clock frequency

Dynamic performance for SAR ADC shown in figure 4.12 , figure 4.13 with different clock frequency These parameter express the decrement in performance with clock frequency because SAR ADC speed depends on resolution. As resolution increase clock frequency decrease.

CHAPTER 5

CONCULSION

In present work A 14-bit SAR ADC with low power consumption has been proposed. In this work DAC is based on binary scaled weighting method capacitor array with bootstrap switching using at the input of the DAC with cross coupling capacitor. In this modification speed get enhanced and also reduces the coupling effect. Proposed circuit simulated in 180nm CMOS N-well technology using cadence virtuous tool in analog design environment (ADE) and analog mixed signal (AMS). Power consumption estimated to 5.86uW, ENOB 13.86, DNL and INL is +0.16LSB and +0.5LSB .

5.1 FUTURE SCOPE

Following can be done

- Amid to increase speed, calibration technique may be proposed
- DAC design can be simplified to reduce the area on chip area.

CHAPTER 6

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