LOW VOLTAGE LOW POWER HIGH PERFORMANCE ANALOG C-MOS DESIGN

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Certificate

*This is to certify that the Thesis entitled "**Low Voltage Low Power High Performance CMOS Op-Amp Design**" which is being submitted herewith by Mr. Sushrant Monga (Roll No. 8014105) towards the partial fulfillment for the award of the degree of **Master of Engineering (Electronics & Communication)** of **Thapar Institute of Engineering & Technology (Deemed University), Patiala** is a bonafide work carried by him under my supervision and guidance.*

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Notations and formulas

A few notations and formulas are enumerated below which would be frequently used in this chapter.

$\langle\ \rangle$ ... Not the designer's choice.

V_{tn} ...Threshold Voltage of the n-transistors

V_{tp} ...Threshold Voltage of the n-transistors

V_{GD_M} ... Gate to Drain Voltage of the M'th transistor

$K_{n/p}$ ... process parameter ($\mu A/V^2$)

S ...Aspect ratio $\left(\frac{W}{L}\right)$ of a transistor

v_{onM} ... $v_{GS\_M} - V_{tn/p}$ of the M'th Transistor

v_{ic} ...common mode voltage for the differential-pair

V_n^- / V_n^+ ...Threshold points for the $\sqrt{I_{sn}}$ curve

V_p^- / V_p^+ ...Threshold points for the $\sqrt{I_{sp}}$ curve

I_N ... Current flowing in the n'th transistor

g_{ds} ... Drain to source conductance of a Transistor

$$S = \frac{g_m^{\ 2}}{2 \times I \times k_{n/p}}$$

$$v_{on} = \sqrt{\frac{2 \times I}{k_{n/p} \times S}}$$

$g_{m1}^{\ 2} = 2 \times I \times \beta$ Where $\beta = k_{n/p} \times S$

$g_{ds} = \lambda \times I_{ds}$

INTRODUCTION

1.1 GENERAL

The need for analog circuits that can operate with low power-supply voltage has increased in recent years. Reducing power consumption in portable applications has made lower power supplies increasingly common in systems with large digital content since many portable products operate from alkaline batteries or rechargeable nickel-metal-hydride, nickel-cadmium batteries, the operating supply for these systems is migrating down to 0.9 V for a single battery cell. These decreasing supply voltages often have detrimental effect on analog components in these systems, however. Additionally supply current of amplifier should be minimized to improve the battery life of the product.

We begin our discussion here about an inherently important and popular component 'Op-Amp'. Ideally an Op-Amp has infinite differential voltage gain, infinite input resistance and zero output resistance. In reality an operational amplifier has high open loop gain, high input resistance, low output resistance and high gain bandwidth unusual as an ideal Op-Amp. For most of the application where CMOS Op-Amps are used, an open loop gain of 2000 or more is usually sufficient. V_{out} can be expressed as

$$V_{OUT} = A_V (v_1 - v_2) \qquad \ldots\ldots \quad 1.1$$

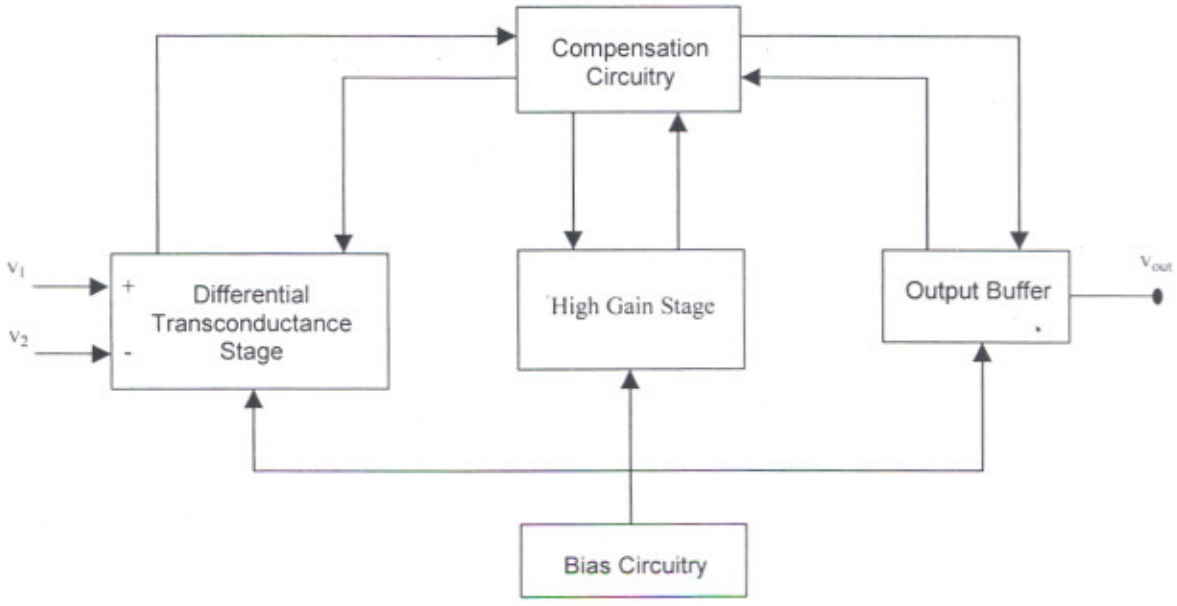


Figure 1.1 Operational Amplifier

A_v is used to designate the open loop differential voltage gain, v_1 and v_2 are input voltages applied to inverting and noninverting terminals. There has to be proper connections to power supply voltages V_{DD} and V_{SS}. Generally these connections are not shown but they are an integral part of biasing of the Op-Amp.

To begin our discussion, we briefly digress the construction of differential Amplifier and then relate the working of low power C-MOS circuits (Op-Amps). Here we start from a scratch and then build on to discuss some of the best prevalent designs. The Op-Amp can be seen as comprised of discrete modules, the first of which is a differential Amplifier which comprises a the input stage of any configurable Op-Amp's architecture.

1.2 The Differential Amplifier

The differential amplifier is one of the more versatile circuits in analog circuit designer also very compatible with integrated-circuit technology and serves as the input stage to op amps. Figure shows a schematic model for a differential amplifier (actually symbol will also be used for the comparator and op amp). Voltages v_1, v_2, and called single-ended voltages. This means that they are defined with respect to ground. The differential-mode input voltage, v_{1D}, of the differential amplifier is defined as the difference between v_1 and v_2. This voltage is defined between two terminals, neither of ground. The common-mode input voltage, v_{1C}, is defined as the average value of v_1 and v_2.

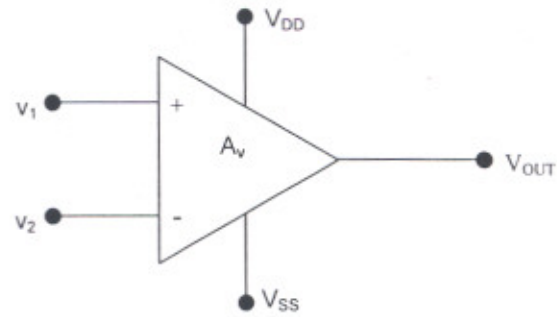


Figure 1.2: Schematic Representation Of Op-Amp

These voltages are given as

$$v_{id} = v_1 - v_2 \qquad \ldots\ldots \quad 1.2$$

and

$$v_{ic} = \frac{v_1 + v_2}{2} \qquad \ldots\ldots \quad 1.3$$

$$v_o = A_{vd}(v_{id}) \pm A_{vc}(v_{ic}) \qquad \ldots\ldots \quad 1.4$$

where A_{VD} is the differential-mode voltage gain and A_{VC} is the common-mode voltage gain. The 've sign preceding the common-mode voltage gain implies that the polarity of this

voltage gain is not known beforehand. In order to assess the behavior of real differential amplifier quantitatively we need to define a few measurable parameters namely:

- CMRR
- ICMR
- A_V (OPEN LOOP VOLTAGE GAIN)
- R_{OUT}, R_{IN}

The objective of the differential amplifier is to amplify only the difference between two different potentials regardless of the common-mode value. Thus, a differential amplifier can be characterized by its common-mode rejection ration (CMRR), which is the ratio of the magnitude of the differential gain of the common-mode gain. An ideal differential amplifier will have a zero value of A_{VC} and therefore an infinite CMRR. In addition, the input common-mode range (ICMR) specifies over what range of common-mode voltages the differential amplifier continues to sense and amplify the differential amplifier is offset voltage. In CMOS differential amplifiers, the most serious effect is the offset voltage. In ideal CMOS differential amplifier when both the inputs are connected together, the output voltage is at a desired quiescent point. In a real differential amplifier, the output-offset voltage is the difference between the actual output voltage and the ideal output voltage when the input terminals are connected together. If this offset voltage is divided by the differential voltage gain of the differential amplifier, then it is called the input offset voltage (V_{OS}). Typically, the input offset voltage of a CMOS differential amplifier is 5-20 mV.

1.2.1 Large-Signal Analysis

Let us begin our analysis of the differential amplifier with the large-signal, that Figure 1.3 shows a CMOS differential amplifier that uses a channel MOSFETs to form a differential amplifier. MI and M2 are biased with a current sink I_{ss} connected sources of M1 and M2. This configuration of M1 and M2 is often called a sources pair. M3 and M4 are an example of how the current sink I_{ss} might be implemented.

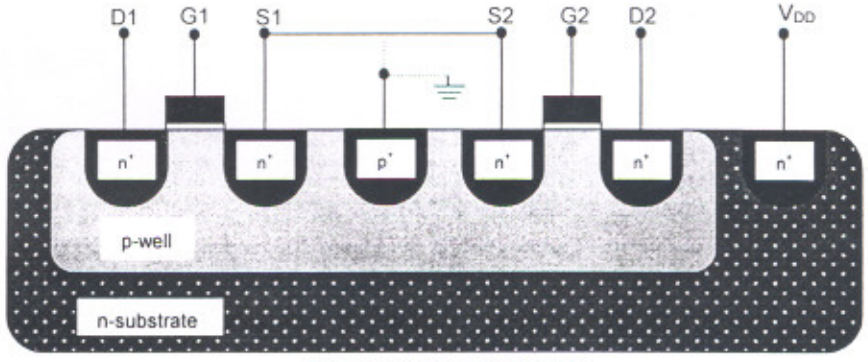


Figure 1.3 P-well Process

Because the sources of M1 and M2 are not connected to ground, the question of connect the bulk arises? The answer depends on the technology. If we assume that the technology is p-well, then the n-channel transistors are fabricated in a p-well as Fig. 1.3 There are two obvious places to connect the bulks of M1 and M2. The first is to connect the bulks to the sources of M1 and M2 or to connect the bulks to the sources of M1 and M2 and let the P-well containing M1 and M2 float. The second is to connect the bulks of M1 and M2 to ground. What difference exists in the two choices? If the p-well is connected to the sources of M1 and M2, then the voltages are not increased because of the reverse-biased bulk-source junction. However the capacitance at the source- coupled point to ground now becomes the entire reverse-biased junction between the p-well and the n-substrate. If the p-well is connected to lowest point available (ground), then the threshold voltages will increase and vary with the common input voltage but the capacitance from the source-coupled point to ground is red the two reverse-biased pn-junctions between the sources of M1 and M2 and the p-well choice depends on the application. Also, note that no such choice exists of the source-coupled pair are p-channel transistors in a p-well technology.

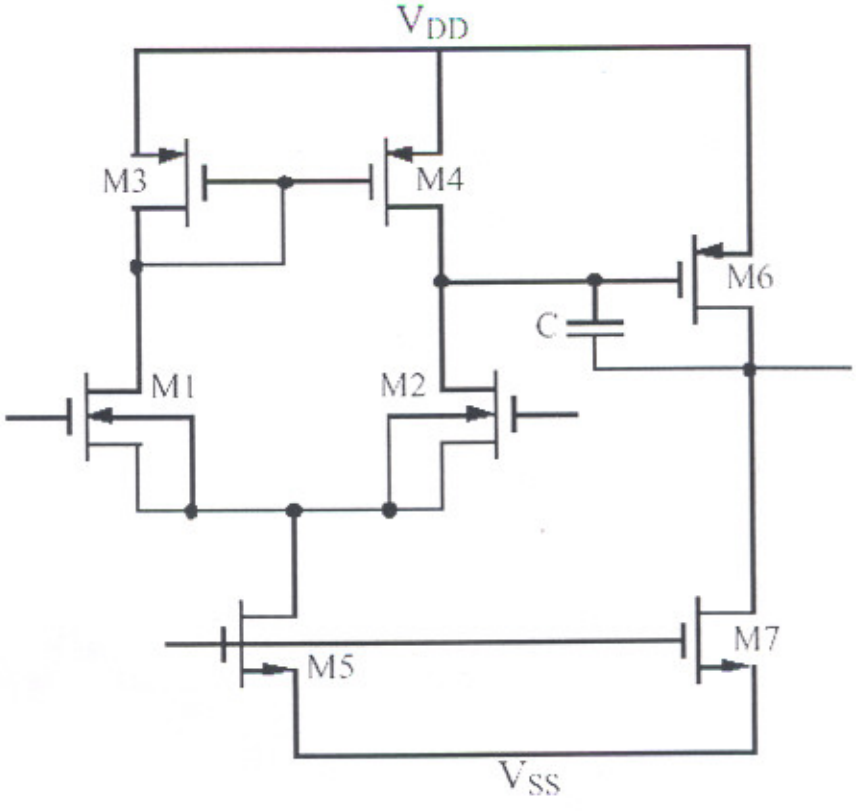


Figure 1.4 A Simple Op-Amp Showing The Differential Amplifier At The Input Stage

The large-signal analysis begins by assuming that M1 and M2 are perfectly match, it is also not necessary for us to define the loads of M1 and M2 to understand the different large-

signal behavior. The large-signal characteristics can be developed by assuming all of the transistors of Fig. 1.4 are always in saturation. This condition is reasonable and illustrates the behavior even when this assumption is not valid. The pertinent relation describing large-signal behavior are given as

$$v_{ID} = v_{GS1} - v_{GS2} = \left(\frac{2i_{D1}}{\beta}\right)^{1/2} - \left(\frac{2i_{D2}}{\beta}\right)^{1/2} \quad \ldots\ldots \quad 1.5$$

and $I_{ss} = i_{D1} + i_{D2}$ 1.6

Substituting Eq. 1.5 into Eq.1.6 and forming a quadratic allows the solution for i_{D1} and i_{D2} as

$$i_{D1} = \frac{I_{SS}}{2} + \frac{I_{SS}}{2}\left(\frac{\beta v_{ID}^2}{I_{SS}} - \frac{\beta^2 v_{ID}^4}{4I^2_{SS}}\right)^{1/2} \quad \ldots\ldots \quad 1.7$$

and

$$i_{D2} = \frac{I_{SS}}{2} + \frac{I_{SS}}{2}\left(\frac{\beta v_{ID}^2}{I_{SS}} - \frac{\beta^2 v_{ID}^4}{4I^2_{SS}}\right)^{1/2} \quad \ldots\ldots \quad 1.8$$

where these relationships are only useful for $v_{ID} < 2\,(I_{SS} / \beta)^{1/2}$. Figure 1.5 shows a plot of the normalized drain current of MI versus the normalized differential input voltage. The dotted portions of the curves are meaningless and are ignored.

The above analysis has resulted in i_{D1} or i_{D2} in terms of the differential input voltage, v_{ID}. It is of interest to determine the slope of this curve, which leads to one definition of transconductance for the differential amplifier. Differentiating Eq. 1.7 respect to v_{ID} and

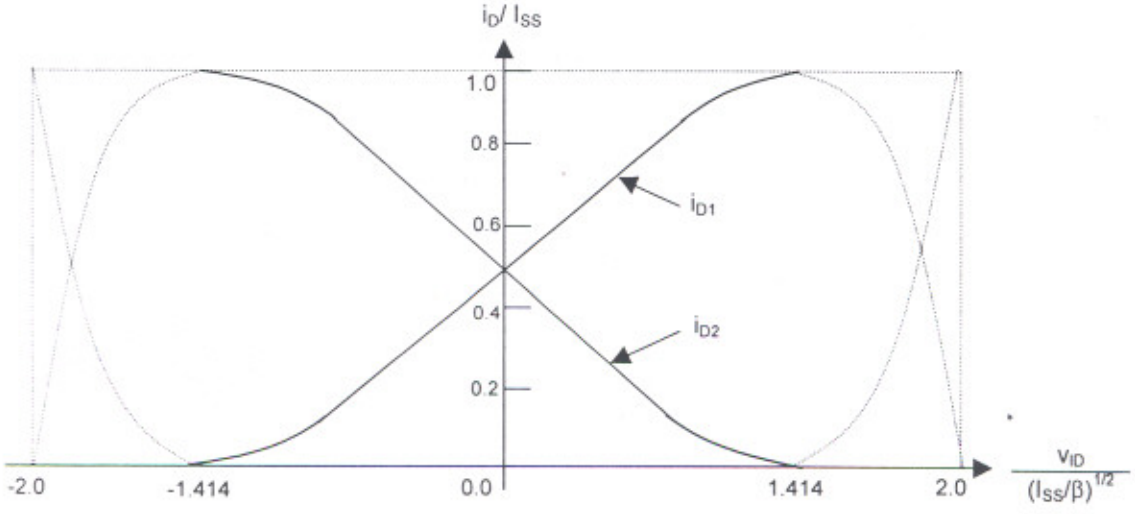


Figure 1.5 Transconductance Vs Differential voltages

setting $V_{ID} = 0$ gives the differential transconductance of the differential amplifier as

$$g_m = \frac{\partial i_{D1}}{\partial v_{ID}}(V_{ID} = 0) = (\beta I_{SS}/4)^{1/2} = \left(\frac{K_1' I_{SS} W_1}{4L_1}\right)^{1/2} \quad \ldots\ldots \quad 1.9.$$

It is interesting to note that as I_{SS} is increased the transconductance also increases. The next step in the large-signal analysis of the CMOS differential amplifier is to example the voltage-transfer curve. This requires inserting a load between the drains of M1 and M2 and the power supply, V_{DD}. We have many choices including resistors, MOS diode or current sources. We will examine some of these choices later; however, for now let us set a widely used load consisting of a p-channel current mirror. Under quiescent conditions (no applied differential signal, i.e., $v_{ID} = 0$ V), the current in M1 and M2 are equal to sum to I_{SS}, the current in the current sink, M5. The current of M1 will determine the current in M3. Ideally, this current will be mirrored in M4. $v_{GS1} = v_{GS2}$ and M1 and M2 are matched, then the currents in M1 and M2 are equal. Thus, the current that M4 sources to M2 should be equal to the current that M2 requires, causing be zero – provided that the load is negligible. In the above analysis, all transistors are assumed to be in saturation.

If these currents are not equal as in the following analysis, we assume that because the external load resistance is infinite that the current flows in the self-resistance of M2 and M3 (due to the channel modulation effect). If $v_{GSI} > v_{GS2}$, then i_{D1} increases with respect to since $I_{SS} = i_{D1} + i_{D2}$. The increase in i_{D1} implies an increase in i_{D3} and i_{D4}. However, this decreases when v_{GS1} is greater than v_{GS2}. Therefore, the only way to establish circuit equilibrium is for i_{OUT} to become positive and v_{OUT} decreases. This configuration provides a simple way by which the differential output signal of the differential amplifier can be converted back to a single-ended signal, that is, one referenced to ac ground. If we assume that the currents in the current mirror are identical, then I_{OUT} can be found by subtracting i_{D2} from i_{D1} for the n-channel differential amplifier of Fig 1.4 Since I_{OUT} a differential output current, we distinguish this transconductance from that of Eq.1.9 by using the notation g_{md}. The differential-in, differential-out transconductance is twice g_m, can be written as

$$g_{md} = \frac{\partial i_{OUT}}{\partial v_{ID}}(V_{ID} = 0) = \left(\frac{K_1' I_{SS} W_1}{L_1}\right)^{1/2} \quad \ldots\ldots \quad 1.10$$

which is exactly equal to the transconductance of the common-source MOSFET if $I_D = I_{ss}/2$. The large signal voltage transfer function for the CMOS differential amplifier of Fig.1.4 with the dashed battery at the output removed is shown in Fig.1.5. The inputs have been applied. The common mode input has been fixed at 2.0 V and the differential input has been swept

from –1 to + 1V. We note that the differential amplifier can be either inverting or non-inverting depending on how the input signal is applied. If $v_{IN} = v_{GS1} - v_{GS2}$ as is the case in Fig., then the voltage gain from v_{IN} to v_{OUT} is non-inverting.

The regions of operation for the pertinent transistors of Fig.1.4 are shown on Fig 1.5. We note that the largest small-signal gain occurs when both M2 and M4 are saturated. M2 is saturated when

$$v_{DS2} \geq v_{GS2} - V_{TN} \rightarrow v_{OUT} - V_{SI} \geq V_{IC} - 0.5v_{ID} - V_{SI} - V_{TN} \rightarrow v_{OUT} \geq V_{IC} - V_{TN} \quad \ldots\ldots \quad 1.11$$

where we have assumed that the region of transition for M2 to close to $v_{ID} = 0$ V. M4 is saturated when

$$v_{SD4} \geq v_{SG4} - |V_{TP}| \rightarrow V_{DD} - v_{OUT} \geq v_{SG4} - |V_{TP}| \rightarrow v_{OUT} \leq v_{DD} - v_{SG4} - |V_{TP}| \quad \ldots\ldots \quad 1.12$$

The regions of operation for M2 and M4 on Fig.1.5 have assumed the W/L values of Fig. 1.4 and $I_{SS} = 100\ \mu A$. The output swing of the differential amplifier of Fig 1.4 could be given by Eq. 1.12 for v_{OUT} (min) and Eq. 1.11 for v_{OUT} (max). Obviously, the output swing exceeds these values as the magnitude of v_{ID} becomes large.

A CMOS differential amplifier that uses p-channel MOSFET devices, M1 and M2, as the differential pair. The circuit operation is identical to that, if the CMOS technology is n-well, then the bulks of the input p-channel MOSFET devices can connect either to V_{DD} or to their sources assuming that M1 and M2 are fabricated in their own n-well that can float. The same considerations hold for capacitance at the source-coupled node as we discussed previously for the differential amplifier using n-channel MOSFETs as the input transistors.

Another important characteristic of a differential amplifier is input common-mode ICMR. The way that the ICMR is found is to set v_{ID} to zero and vary v_{IC} until one of the transistors in the differential amplifier is no longer saturated. We can think of this analysis as connecting the inputs together and sweeping the common-mode input voltage. V_{IC} (max), is found as follows. There are two paths from V_{IC} to V_{DD} that we must examine. The first is from G1 to M1 and M3 to V_{DD}. The second is from G2 through M2 and M4 to V_{DD}. For the first path we can write

$$V_{IC}(\text{max}) = V_{GI}(\text{max}) = V_{DD} - V_{SG3} - V_{DS1} + V_{GS1} \quad \ldots\ldots \quad 1.13$$

The above equation can be rewritten as

$$V_{IC}(\text{max}) = V_{DD} - V_{SG3} - V_{TN1} \quad \ldots\ldots \quad 1.14$$

The second path can be written as

$$V_{IC}(max)' = V_{DD} - V_{DS4}(sat) - V_{DS2} - V_{GS2} = V_{DD}(sat) + V_{TN2} \quad \ldots\ldots \quad 1.15$$

Since the second path allows a higher value of V_{IC} (max), we will select the first path worst-case viewpoint. Thus, the maximum input common-mode voltage for the differential amplifier Fig.1.4 equal to the power supply voltage minus the drop across M3 plus the threshold voltage. If we want to increase the positive limit of V_{IC}, we will need to select a load circuit different from the current mirror.

The lowest input voltage at the gate of M1 (or M2) is found to be

$$V_{IC}(min) = V_{SS} - V_{DS5}(sat) - V_{GS1} = V_{SS} = V_{DS5}(sat) + V_{GS2} \quad \ldots\ldots \quad 1.16$$

We assume that V_{GS1} and V_{GS2} will be equal during changes in the input common age. The value of W_3/L_3 will determine value of V_{IC} (max) while the values of W_1 / L_1 (W_2/L_2) and W_5/L_5 will determine the value of V_{IC} (min). We will use these equations in later chapters to design the W/L values of some of the transistors of the different amplifier.

To design the differential amplifier to meet a specified negative common-mode range, the designer must consider the worst-case V_T spread (specified by the process) and adjust I_{SS} and β_3, to meet the requirements. The worst-case V_T spread affecting positive common-mode range for the configuration of Fig. 1.4 is a high p-channel threshold magnitude ($|V_{T03}|$) and a low n-channel threshold (V_{T01}).

An improvement can be obtained when the substrates of the input devices are connected to ground. This connection results in negative feedback to the sources of the input devices. For example, as the common source node moves positive the substrate bias increases, resulting in an increase in the threshold voltages (V_{T1} and V_{T2}). Equation shows that the positive common-mode range will increase as the magnitude of V_{T1} increases.

1.3 Characterization of Op Amps [1]

In practice, the operational amplifier only approaches the ideal infinite-gain voltage amplifier. Some of its other nonideal characteristics are illustrated in Fig.1.6. The finite differential input impedance is modeled by R_{id} and C_{id}. The output resistance is modeled by R_{out}. The common-mode input resistances are given as resistors of R_{icm} connected from each of the inputs to ground. V_{os} is the input-offset necessary to make the output voltage zero if both of the inputs of the op amp are grounded. I_{os} (not shown is the input-offset current, which is

necessary to make the output voltage zero if the op amp is driven from two identical current sources. Therefore, I_{os} is defined as the magnitude of the difference between the two input-bias currents I_{B1} and I_{B2}. Since the bias currents for a CMOS op amp are approximately zero, the offset current is also zero. The common-mode rejection ratio (CMRR) is modeled by the voltage-controlled voltage source indicated as v CMRR. This source approximately models the effects of the common-mode input signal on the op amp. The two sources designated as e_n^2 and i_n^2 are used to model the Op-Amp noise. These are rms voltage and current noise sources with units of mean-square volts and mean-square amperes, respectively. These noise sources have no polarity and are always assumed to add.

Not all of the nonideal characteristics of the op amp are shown in Fig.1.6. Other pertinent characteristics of the op amp will now be defined. The output voltage can be defined as

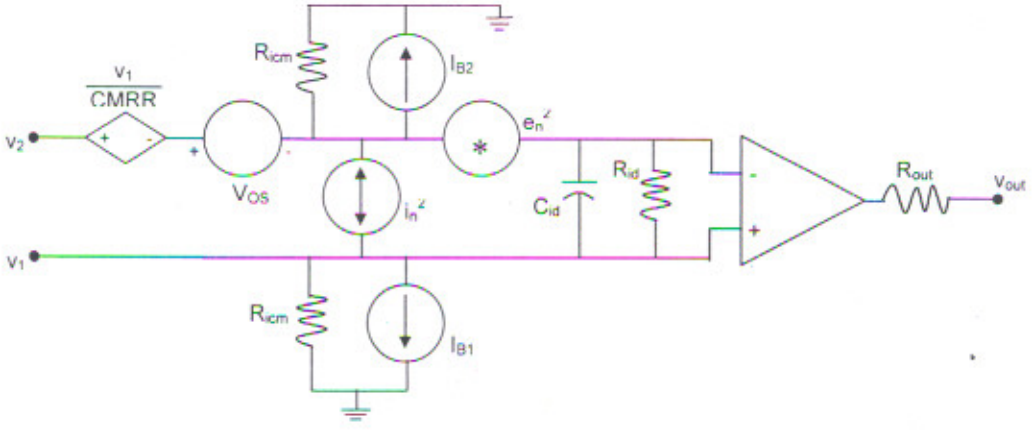


Figure 1.6 A Practical Operational Amplifier

$$v_o(s) = A_{vd}(s)(v_{id}(s)) \pm A_{vc}(s)(v_{ic}(s)) \qquad \ldots\ldots \quad 1.17$$

Where the first term on the right is the differential portion of V_{out} (s) and the second term is the common-mode frequency response is given as A_c(s). A typical frequency response of an Op-Amp is given as

$$A_v(s) = \frac{A_{v0}}{\left(\frac{s}{p_1} - 1\right)\left(\frac{s}{p_2} - 1\right)\left(\frac{s}{p_3} - 1\right)\ldots\ldots} \qquad \ldots\ldots \quad 1.18$$

Where p_1, p_2... are poles of the operational amplifier open-loop transfer function. In general, a pole designated as p_1 can be expressed as

$$p_i = -\omega_i \qquad \ldots\ldots \quad 1.19$$

Where ω_i is the reciprocal time constant or break-frequency of the pole p_i. While the operational amplifier may have zeros, they will be ignored at the present time. A_{vo} or $A_v(0)$ is the gain of the op amp as the frequency approaches zero.

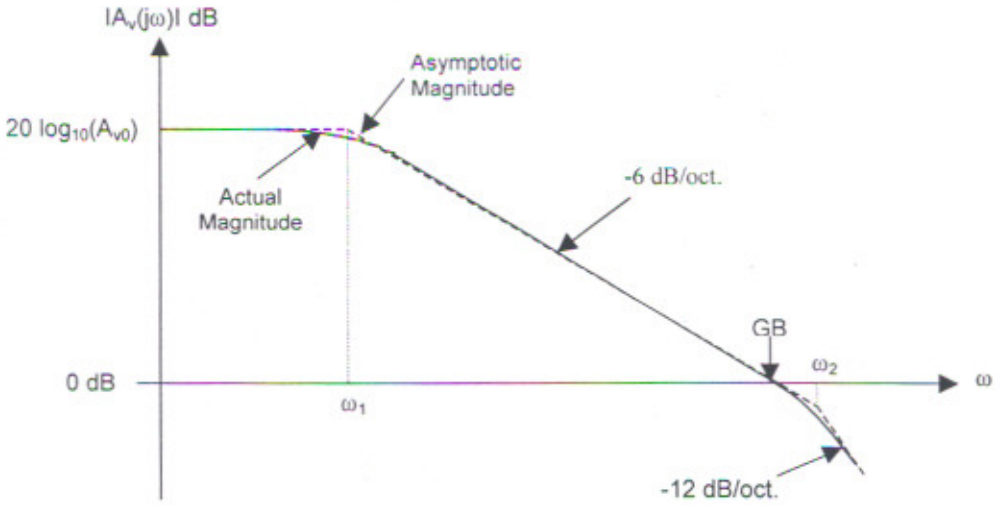


Figure 1.7 Bode Plot of a Simple Uncompensated Op-Amp

Figure 1.7 shows a typical frequency response of the magnitude of $A_v(s)$. In this case we see that w_1 is much lower than the rest of the break-frequencies, causing w_1 to be the dominant influence in the frequency response. The frequency where the – 6 dB/Oct. slope from the dominant pole intersects with the 0db axis is designated as the unity-gain bandwidth, abbreviated GB, of the op amp. Even if the next higher order poles are smaller than GB, we shall still continue to use the unity-gain bandwidth as defined above.

Other nonideal characteristics of the op amp include the power supply rejection ration, PSRR. The PSRR is defined as the product of the ratio of the change in supply voltage to the change in output voltage of the op amp caused by the change in the power supply and the open-loop gain of the op amp. Thus,

$$PSRR = \frac{\Delta V_{DD}}{\Delta V_{OUT}} A_v(s) = \frac{V_o / V_{in}(V_{dd} = 0)}{V_o / V_{dd}(V_{in} = 0)} \qquad \ldots\ldots \quad 1.20$$

An ideal op amp would have an infinite PSRR. The common-mode input range is the voltage range over which the input common-mode signal can vary. Typically, this range is 1-2 V less than V_{DD} and 1-2 more than V_{ss}.

The output of the op amp has several important limits, one of which is the maximum output current sourcing and sinking capability. There is a limited range over which the output voltage can swing while still maintaining high-gain characteristics. The output also has a voltage rate limit called slew rate. The slew rate is generally determined by the maximum current available to charge or discharge a capacitance. Normally, slew rate is not limited by the output, but by the current sourcing/sinking capability of the first stage. The last characteristic of importance in analog sampled-data circuit applications is the settling time.

$$\frac{dV}{dt} = \frac{I}{C} = \text{Slew rate} \qquad \ldots\ldots \quad 1.21$$

This is the time needed for the output of the Op-Amp to reach a final value (to within a predetermined tolerance) when excited by a small signal. This is not to be confused with slew rate, which is a large-signal phenomenon. Many times, the output response of an op amp is a combination of both large and small-signal characteristics. Small-signal settling time can be completely determined from the location of the poles and zeros in the small-signal equivalent circuit, whereas slew rate is determined from the large-signal conditions of the circuit. It is necessary to wait until the amplifier has settled to within a few tenths of a percent of its final value in order to avoid errors in the accuracy of processing analog signals. A longer settling time implies that the rate of processing analog signals must be reduced.

Fortunately, the CMOS op amp does not suffer from all of the nonideal characteristics previously discussed. Because of the extremely high input resistance of the MOS devices both R_{id} and I_{os} (or I_{B1} and I_{B2}) are of no importance. A typical value of R_{id} is in the range of 10^{14} ohms. Also, R_{icm} is extremely large and can be ignored. With the noninverting terminal on ac ground, then all common-mode characteristics are unimportant.

1.4 Classification of Op-Amps

In order to understand the design of CMOS op amps it is worthwhile to examine their classification and categorization. It is encouraging that Op-Amps that we are totally unfamiliar with at this point can be implemented using the previous blocks. We see that the differential amplifier is almost ubiquitous in its use as the input stage. As we have seen previously, amplifiers generally consist of a cascade of voltage-to-current or current-to-voltage converting stages. A voltage-to-current stage is called a transconductance stage and

a current-to-voltage stage is called the load stage. In some cases, it is easier to think of a current-to-current stage, but eventually current will be converted back to voltage.

We discuss two different architectures; the first is the *Two-Stage Op-Amp*. It consists of a cascade of V-I and I-V stages. The first stage consists of a differential amplifier converting the differential input voltage to differential currents. These differential currents are applied to a current- mirror load recovering the differential voltage. This of course is nothing more than the differential voltage amplifier. The second stage consists of a common-source MOSFET converting the second-stage input voltage to current. This transistor is loaded by a current-sink load, which converts the current to voltage at the output. The second stage is also nothing more than the current-sink inverter This two-stage Op-Amp is so widely used that we will call it the classical two-stage Op-Amp; it has both MOSFET and BJT versions.

A second architecture is commonly called *The Folded-Cascode Op Amp*. This architecture was developed in part to improve the input common-mode range and the power-supply rejection of the two-stage op amp. In this particular op amp, it is probably more efficient to consider it as the cascade of a differential transconductance stage with a current stage followed by a cascode current mirror load. One of the advantages of the folded-cascode op amp is that it has a push-pull output. That is, the op amp can actively sink or source current from the load. The output stage of the previous two-stage op amp is Class A, which means that either its sinking or sourcing capability in fixed.

1.5 Design of Op Amps

The design of an op amp can be divided into two distinct design-related activities that are for the most part independent of one another. The first of these activities involves chòosing or creating the basic structure of the op amp. A diagram that describes the interconnection of all of the transistors results. In most cases, this structure does not change throughout the remaining portion of the design, but sometimes certain characteristics of the chosen design must be changed by modifying the structure.

One the structure has been selected, the designer must select de currents and begin to size the transistors and design the compensation circuit. Most of the work involved in completing a design is associated with this, the second activity of the design process. Devices must be properly scaled in order to meet all of the ac and dc requirements imposed on the op amp. Computer circuit simulations, based on hand calculations, are used extensively to aid the designer in this phase.

Before the actual design of an op amp can begin, though, one must set out all of the requirements and boundary conditions that will be used to guide the design. The following list describes many of the items that must be considered.

1.5.1 Boundary Conditions:

1. Process specification (V_T, K^1, C_{ox}, etc.)
2. Supply voltage and range
3. Supply current and range
4. Operating temperature and range

Requirements:

1. Gain
2. Gain Bandwidth
3. Settling time
4. Slew rate
5. Input common-mode range, ICMR
6. Common-mode rejection ratio, CMRR
7. Power-supply rejection ratio, PSRR
8. Output-voltage swing
9. Output resistance
10. Offset
11. Noise
12. Layout area

The compensation method has a large influence on the design of each block. Two basic methods of compensation are suggested by the opposite parallel paths into the compensation block. These two methods, feedback and feed forward, are developed in the following section. The method of compensation is greatly dependent on the number of stages present (differential, second, or buffer stages).

1.5.2 Compensation of Op-Amps

Operational amplifiers are generally used in a negative-feedback configuration. In this way, the relatively high, inaccurate forward gain can be used with feedback to achieve a very accurate transfer function that is a function of the feedback elements only. Figure 1.6 illustrates a general negative-feedback configuration. A(s) is the amplifier gain and will normally be the open-loop, differential voltage gain of the op amp, and F(s) is the transfer function for external feedback from the output of the op amp back to the input. The loop gain of this system will be defined as

$$\text{Loop gain} = L(s) = -A(s)F(s) \qquad \ldots\ldots \quad 1.22$$

Consider a case where the forward gain from V_{in} to V_{out} is to be unity. It is easily shown that if the open-loop gain at dc A(0) is between 1000 and 2000, and F is equal to 1, the forward gain varies from 0.999 to 0.9995. For very high loop gain (due primarily to a high amplifier gain), the forward transfer function V_{out} / V_{in} is accurately controlled by the feedback network. This is the principle applied in using operational amplifiers.

1.5.2.1 Small-Signal Dynamics of a Two-Stage op Amp

It is of primary importance that the signal fed back to the input of the Op-Amp be of such amplitude and phase that is does not continue to regenerate itself around the loop. Should this occur, the result will be either clamping of the output of the amplifier at one of the supply potentials (regeneration at dc), or oscillation (regeneration at some frequency other than dc). The requirement for avoiding this situation can be succinctly stated by the following equation:

$$\left|A(j\omega_{0^\circ})F(j\omega_{0^\circ})\right| = \left|L(j\omega_{0^\circ})\right| < 1 \qquad \ldots\ldots \quad 1.23$$

when $\arg\left[A(j\omega_{0^\circ})F(j\omega_{0^\circ})\right] = 180^\circ$ $\qquad \ldots\ldots \quad 1.24$

If these conditions are met, the feedback system is said to be stable (i.e., sustained oscillation cannot occur). This second relationship given in Eq.1.23 is best illustrated with the use of Bode diagrams. Figure 1.8 shows the response of $\left|A(j\omega_{0^\circ})F(j\omega_{0^\circ})\right|$ and $\arg\left[A(j\omega_{0^\circ})F(j\omega_{0^\circ})\right]$ as a function of frequency. The requirement for stability is that $\left|A(j\omega_{0^\circ})F(j\omega_{0^\circ})\right|$ curve crosses zero dB point before $[-\arg\left[A(j\omega_{0^\circ})F(j\omega_{0^\circ})\right]]$ reaches 0°. A measure of stability is given by the value of phase when $\left|A(j\omega_{0^\circ})F(j\omega_{0^\circ})\right|$ is 0 dB. This measure is called the phase margin.

Now consider the small signal model for an uncompensated Op-Amp. In order to generalize the results the components associated with the first stage have the subscript I and those associated with the second stage have the subscript II. The location for the two poles are given by

$$p_1' = \frac{-1}{R_I C_I} \qquad \ldots\ldots \quad 1.25$$

and

$$p_2' = \frac{-1}{R_{II} C_{II}} \qquad \ldots\ldots \quad 1.26$$

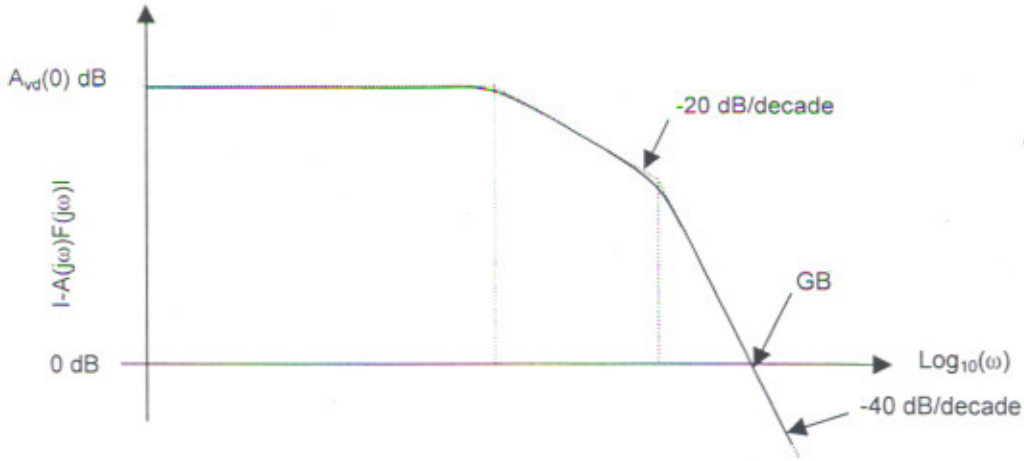


Figure 1.8 Bode Plot for the Two Stage Op-Amp

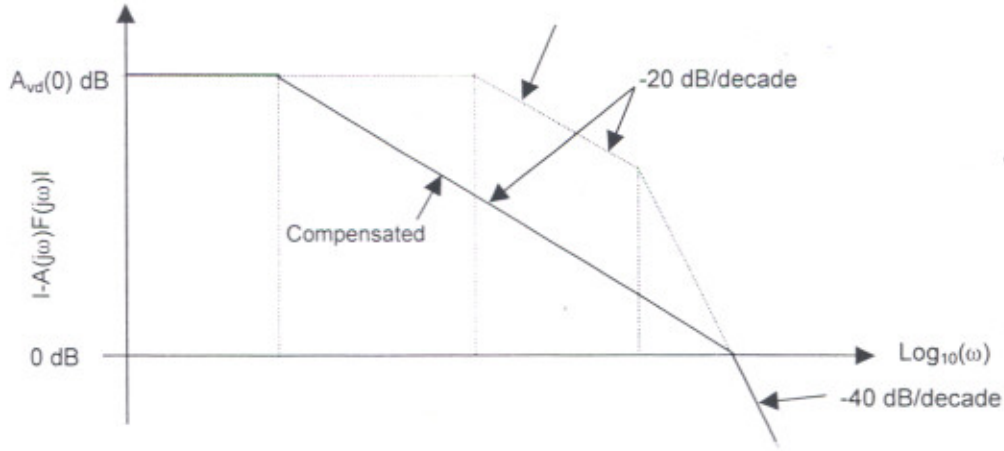


Figure 1.9 Bode Diagram of the Above Amplifier Now Compensated

Here we show a famous compensation technique called as the miller compensation whereby we connect a capacitor from the output of the first stage to the input of the second stage of our generic Op-Amp model. For this, we see that our dominant pole is moved towards the origin and other poles and zeroes move farther away. This helps to increase the phase

margins to somewhere between 45° to 60°, hence increasing the stability of the amplifier. Ideally we should have zero ten times farther than GB and pole to be somewhere between 1.2 to 2.2 times GB in order to have the requisite phase margin as shown above.

As predicted in the forthcoming decades we foresee a steep decline in the power usage as guided by the advancement in VLSI. The shrinking size of a chip thus evolving SOC require whole of the system on the chip including a lot more to memory and interfacing also.

Therefore we are bound to reduce power consumption or either deduce fast and effective ways of cooling the already miniaturized surface of the chip. The applications are even more demanding in further years to come, especially in field of Tele-communications, Mobile Networks Laptops etc.

The lowering of the supply voltage results in a reduced input common-mode range. An op-amp can easily be designed to achieve rail-to-rail output swing with simple class-A or class-AB designs. The key problems lie at the input stage, and the classic two-stage architecture demands to rail-to-rail transconductance function with both constant gm and limiting current, so that unity-gain bandwidth and slew rate are both maintained over the full common-mode input range. Rail-to-rail input stages allow input common-mode signals to vary from the negative to positive supply rails by the use of complementary differential pairs operated in parallel. When the common-mode input signal is near one of the rails, only one of the pairs turns on; the other is cut off. At the middle of the common-mode input range, both the n- and p-pairs are on, and the total transconductance has twice the gm of a single pair, assuming both pairs have the same gm value. Because of this, the total transconductance is not constant across the input common-mode range. This is an undesired phenomenon because it not only results in non-constant gain and variable unity-gain frequency but also degrades the common-mode rejection ratio (CMRR) and causes the slew rate to vary.

Henceforth we discuss techniques of implementing the Micro-power Op-Amps by carefully designing the input differential transconductance stage with the same process technologies. We go on to introduce various *input stages design* and the improvement leading to the current architecture for the present day input stage

Out of the various techniques we would be discussing the low voltage circuits explicitly. Further we will also discuss another method of implementing the Op-Amp with the same process technologies but operated *dynamically*. The dynamic operation also helps in reducing the parasitics inevitable in conventional two-stage architecture.

ROAD TRUDGED

2.1 DEVELOPMENTS TILL NOW

We had started with the design of a two stage CMOS Op-Amp which is probably one of the most widely used CMOS Op-Amp. However there are number of unbuffered applications in which the performance of a two stage Op-Amp is not sufficient. The performance limitations of the conventional two stage Op-Amp are:

- Insufficient gain
- Limited stable bandwidth
- Poor PSRR
- Small ICMR

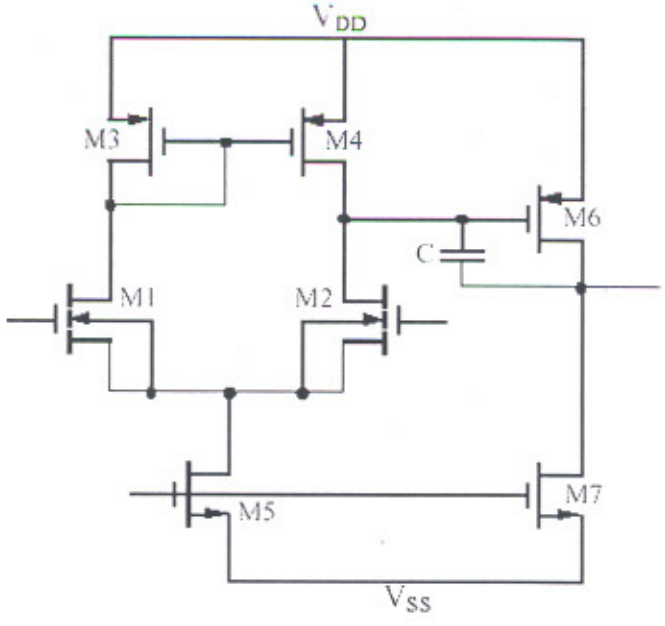


FIGURE 2.1 : Conventional Two Stage

Hence we turn to cascaded Op-Amps which assure enhancement in some of the parameters listed above.

Why Cascode Op-Amps?

- Control the frequency behavior
- Increase PSRR
- Simplifies design

Where is the Cascode Technique Applied?

- First stage -
  - Good noise performance
  - Requires level translation to second stage
  - Requires Miller compensation
- Second stage -
  - Self compensating
  - Reduces the efficiency of the Miller compensation
  - Increases PSRR

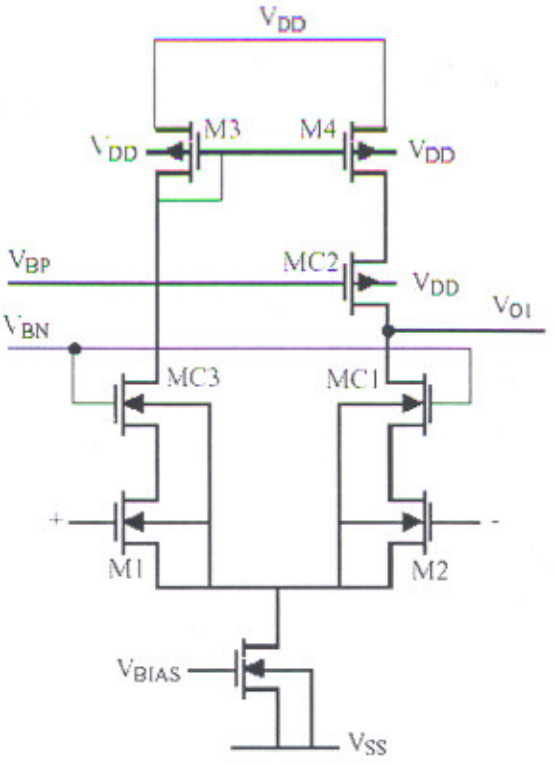


Figure 2.2: Input Stage Of Cascode Differential

2.2 Rail to Rail Input Architectures [3],[4],[5],[6]

Perhaps the most difficult circuit design challenge for the low-voltage operational amplifier is the design of an input stage with a rail-to-rail common-mode voltage range. Much work has been reported on input stages with complementary differential pairs and associated circuit network used to maintain constant transconductance over the input voltage range. However, at low supply voltages, the sum of the common-mode voltage range of the n-channel and p-channel differential pairs may become larger than the available supply voltage, creating a

"dead zone" in the amplifier's common-mode input range, as shown in Fig 2.3. The minimum supply voltage range of an amplifier with a complementary input stage can then be described as

$$V_{SUPPLY} \geq V_{GS(N)} + V_{GS(P)} + 2*V_{DS(SAT)} \quad \ldots\ldots \quad 2.1$$

Where V_{SUPPLY} is the amplifier supply voltage, $V_{GS(N)}$ and $V_{GS(P)}$ are the gate source voltages of the n-channel and p-channel differential pairs, respectively and $V_{DS(SAT)}$ is the saturation voltage of each differential pair's current source bias.

The complementary input architecture also suffers from reduced common-mode rejection as the input control of the amplifier is switched from the p-channel to the n-channel differential pairs. Since the input offset voltages of the n-channel and p-channel differential pairs likely have differential values, the effective input offset voltage of the amplifier may exhibit a discontinuity as the control of the input stage shifts between these differential pairs. This mechanism will degrade the common-mode rejection of the amplifier.

Another rail-to-rail input stage technique utilizes a bulk-driven differential pair for the input stage, which is shown in Fig 2.4. This technique modulates the threshold voltages of the differential pair to generate transconductance (g_m), through not as efficiently as the conventional gate-driven differential pair. For example, the g_m of a bulk-driven differential pair in this CMOS process is approximately 30% of its gate-driven equivalent. Although the bulk-driven differential pair can achieve rail-to-rail common-mode input range at low supply voltages, it suffers from a large voltage-dependent input capacitance due to the junction capacitance, and increased input bias currents at low common-mode input voltages. The input currents can become substantial as the threshold voltage increases, due to the larger source-bulk junction bias. These input currents can become problematic in the amplifier feedback network, especially with the large impedances used in low-power portable applications.

A third rail-to-rail input stage technique utilizes an n-channel depletion-mode differential pair, as shown in Fig 2.5. The differential pair relies upon modulating the source-bulk bias voltage as a function of the input common-mode voltage, which dynamically increases the threshold voltage of the depletion input differential pair. The transistors essentially operate as depletion-mode transistors at low common-mode voltages, where the gate-source voltage (V_{GS}) of the transistors is negative. This allows sufficient bias voltage for the differential pair" bias current source. As the common-mode voltage increases, the threshold voltages of the transistors become more positive, their V_{GS} voltages become positive, and eventually the transistors operate in enhancement mode at common-mode voltages near the positive supply. This maintains the operation of the differential pair transistors in saturation.

A good example of the problem occurs when the amplifier's common-mode voltage is near the negative supply, where the depletion mode voltage is near the negative supply, where the depletion-mode differential pair needs to provide sufficient bias voltage for its bias current source. In weak inversion operation, the V_{GS} voltage is a weak function of the ratio of the drain current and the device aspect ratio. But since the drain current also determines the gm of the differential pair, it may be difficult to find the proper bias point for the circuit in a given process technology.

Further, sufficient back-gate modulation of the threshold voltage is required to generate a sufficiently large threshold voltage shift when the common-mode voltage is at the positive supply. If the increase in V_{GS} due to back-gate effect is too small, the differential pair transistors will not have enough drain-source voltage (V_{DS}) to operate in saturation, and the transconductance of the input stage will decrease at high common-mode voltages. Therefore, the design flexibility for a weak inversion depletion-mode differential pair is small, since the device process parameters of threshold voltage and back-gate modulation factor dictate if the transconductor operates properly over the entire common-mode voltage range.

More design flexibility is available when biasing the depletion-mode differential pair in strong inversion, since the V_{GS} voltage can be designed to offer the correct source voltage to the bias current source when the common-mode voltage is near the negative supply. But since

$$(V_{GS} - V_t) \propto g_M$$

the transconductance of the input stage is determined by this bias point constraint. A large modulation factor to shift the transistor V_{GS} is also still required.

A number of techniques to achieve constant g_m has been proposed. Stabilization of the total g_m over the common-mode range can be tackled by varying the effective tail current in the active differential pair, so that its gm doubles when the other is inactive. A simple way to achieve this is to use a transistor to sense that one of the pairs has lost sufficient gate drive to operate and to divert the unused tail current through a bypass transistor. An alternative technique is to increase the tail current bias on each side by a factor of four and to add additional devices inside each differential pair, which have a width three times that of the active devices. If the square-law operation is valid, gm will double, making up the deficit caused by the inactive pair. In these implementations, the diverting transistor is three times wider than the driving transistor, which causes extra tail current added to the large signal limiting value. Hence slewing value doubles within the common input range. To remedy this, a novel implementation that employs a diverting transistor of the same size as that of the driving transistor has been recently reported. Different from the techniques handling the dc-tail current, a method based on processing signal current has been proposed. There, the

signal currents from the n- and p-pairs are compared, and only the maximum current is selected and processed, keeping the g_m constant. All the above techniques need extra circuitry such as many current mirrors; signal-processing circuits as maximum-selecting circuitry, which requires even more mirrors; or four 1:1 mirrors accompanying the current diverting circuit. All these implementations make the input stage much more complicated and inevitably require more chip area and power consumption compared with the conventional input stage. Furthermore, these techniques often have degraded CMRR.

Here a novel technique to obtain a constant gm as well as to achieve rail-to-rail input and output swings are presented. This paper is organized as follows. Section II presents an analysis of the complementary input stage and introduces the idea of overlapping the transition regions of the tail currents for the n- and p-pairs to achieve constant overall transconductance g_m.

We have seen that all the higher order roots of the polynomial must be greater than the desired value of GB. This places a frequency response limit that is difficult to overcome .to reduce the number of higher order roots, it is necessary to keep the circuitry as simple as possible. One approach that has been used to simplify the circuitry is switched op amps .A switched Op-Amp uses dynamic biasing to simplify the biasing circuitry and therefore reduces the number of higher order roots.

2.3 Dynamic Circuits

Dynamic circuits take advantage of the fact that many applications are synchronously clocked resulting in periods of time where the circuit is not functioning.
We will examine:

- Dynamic or switched resistors
- Dynamically biased amplifiers
- Dynamically biased, push-pull, cascode Op-Amp

Let's talk about the dynamically switched inverting amplifier such a circuit functions only for a limited period of time and must be refreshed. This type of amplifier would be limited to sampled data applications such as switched capacitors circuits.

The dynamically biased inverter establishes the biased conditions during ϕ_2 phase M1 and M2 are connected as two series connected MOS diodes. The source to gate potential of M2 is established on the capacitor C_B. At the same time the offset voltage of the amplifier is

referenced to ground by the capacitor C_{OS}. During the second phase ϕ_1, the input is connected in series with C_{OS}. Thus the voltage applied to the gate of M1 has the DC value superimposed by an AC signal, C_B causes M2 to function as a current source for M1.

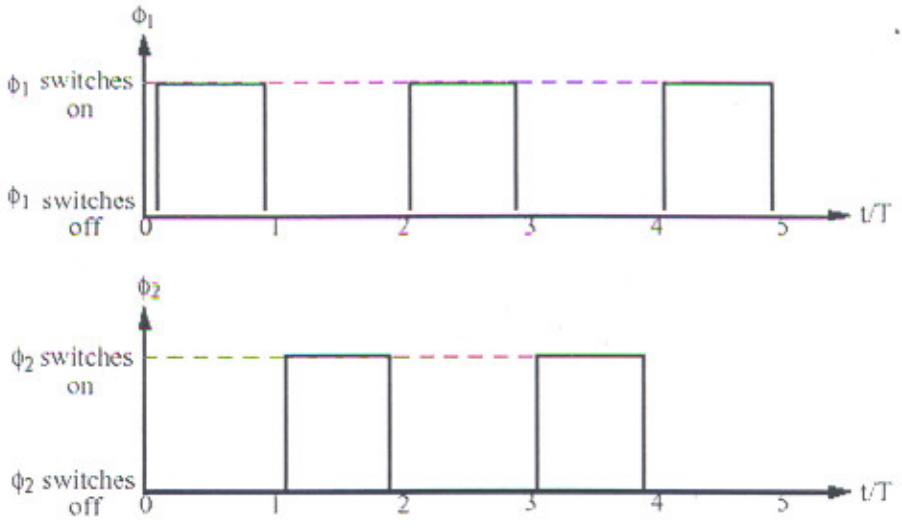
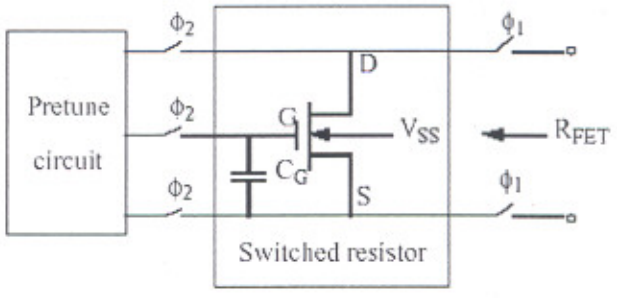


Figure 2.3 : The Two Phases Of Clock



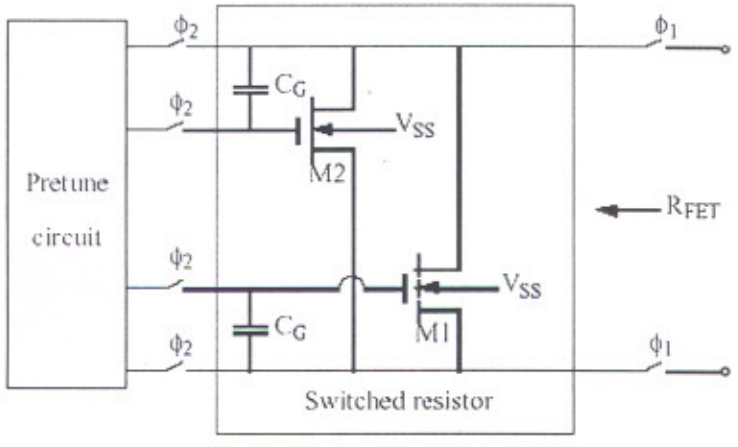


Figure 2.4 A Switched Resistor

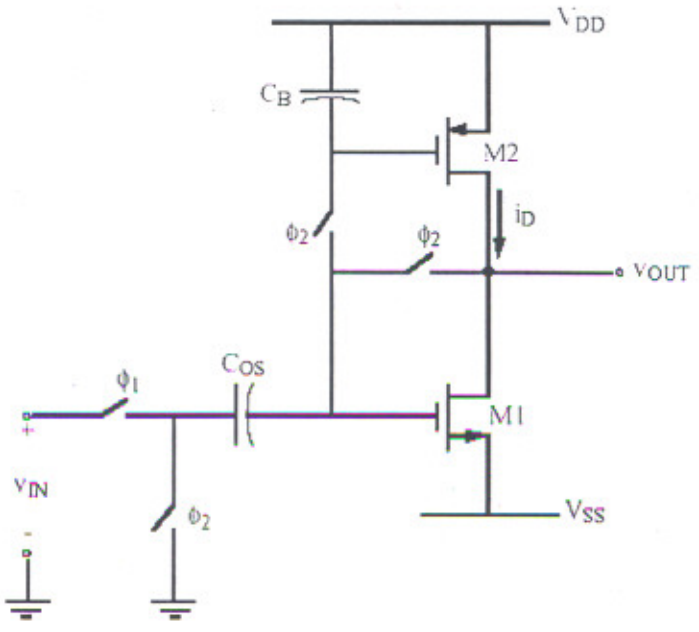


Figure 2.5: Dynamically Biased Inverting Amplifier

The dynamically biased cascode amplifier (refer [1]) is a better example of reducing parasitics by using switched amplifier. The NMOS transistors M1 and M2 and the PMOS transistors M3 and M4 constitute the push-pull cascode output stage. The six switches and the capacitors C1 and C2 represent the differential input stage of the Op-Amp. The NMOS transistors M5 and M6 and the PMOS transistors M7 and M8 generate the bias voltages of the Op-Amp. The channel lengths of M1, M2, M3 and M4 are equal to those of M5, M6, M7 and M8 respectively. When the Op-Amp given below was fabricated using a 1.5μm, n-well, double-poly and double-metal, it was found to have a GB of 127MHz with a load capacitance of 2.2pF. The settling time 10ns for a 5pF load capacitance the PSRR for positive and negative power supplies was 33db at 100 kHz. The ICMR was 1.5 V – 3.5 V for 5V power supply. The power dissipation was 1.6mW. The key to high performance of the circuit was the simplification due to dynamic circuit techniques and clever use of high speed technology.

2.4 Micro-power Op-Amps [1], [6]

In this section, op amps that require minimum power are considered. This type of op amp primarily operates in the weak inversion region. Op amps operating in the weak inversion region have become very useful because they operate not only at low power-supply currents but also at very low power-supply voltages. Our first task in this section is to develop the small-signal equations for transistors operating in weak inversion. These will be applied to

understanding a few basic amplifier architectures that work well using micro-power techniques. The techniques that are introduced in this section to create high current overdrive can be used in strong inversion circuits as well.

2.4.1 Two-Stage Miller Op-Amp Operating in Weak Inversion [5], [6]

First, consider the equations that model the large-signal behavior of transistors operating at very low current densities. Assuming operating in the saturation region, sub-threshold drain current was given in equation as :

$$i_D = \frac{W}{L} I_{D0} \exp\left(\frac{q v_{GS}}{nkT}\right) \quad \ldots\ldots \quad 2.2$$

From this equation, the transconductance can easily be derived as

$$g_m = \frac{I_D}{nkT/q} \quad \ldots\ldots \quad 2.3$$

This result is very interesting in that it shows a linear relationship between transconductance and drain current. Furthermore, the transconductance is independent of device geometry. These two characteristics set the sub-threshold region apart from the strong inversion region, where the relationship between g_m and I_D is a square-law one and also a function of device geometry. In fact, the transconductance of the MOS device operating in the weak inversion region looks very much like that of a bipolar transistor.

Equation shows no dependence of drain current on drain-source voltage. If such were the case, then the device output impedance would be infinite (which is obviously not correct). The dependence of i_D on v_{DS} can be approximated in the same way as it was for the simple strong inversion model, where the drain current is modulated by the term $1 + \lambda v_{DS}$. Note that the weak inversion λ may not necessarily be the same as the extracted from strong inversion measurements. The expression for output resistance in weak inversion is

$$r_0 \cong \frac{1}{\lambda I_v} \quad \ldots\ldots \quad 2.4$$

Like the transconductance, the output resistance is also independent of device aspect ratio, W/L (at constant current). Since λ is a function of channel length, it is the only control the designer has on the gain ($g_m r_o$) of a single stage operating in weak inversion. With these things in mind, consider the simple op amp shown in Fig. The de gain of this amplifier is

$$A_{v0} = g_{m2}g_{m6}\left(\frac{r_{02}r_{04}}{r_{02}+r_{04}}\right)\left(\frac{r_{06}r_{07}}{r_{06}+r_{07}}\right) \quad \ldots\ldots \quad 2.5$$

In terms of device parameters the gain can be expressed as

$$A_{v0} = \frac{1}{n_2 n_6 (kT/q)^2(\lambda_2+\lambda_4)(\lambda_6+\lambda_7)} \quad \ldots\ldots \quad 2.6$$

The gain bandwidth g_{m1}/C is

$$GB = \frac{I_{D1}}{(n_1 kT/q)C} \quad \ldots\ldots \quad 2.7$$

It is interesting to note that while the dc gain of the op amp is independent of I_D, the GB is not. This becomes a limiting factor in the dynamic performance of the op amp operating in weak inversion because the dc current is small and thus the GB is small. The slew rate of this amplifier is

$$SR = \frac{I_{D5}}{C} = 2\frac{I_{D1}}{C} = 2GB\left(n_1\frac{kT}{q}\right) = 2GBn_1V_1 \quad \ldots\ldots \quad 2.8$$

2.4.2 Low Voltage Bias and Load Circuits [3] [4]

In addition to the input stage of an op amp, the biasing and load circuits can become a limit to power-supply reduction. In this section we will consider current mirrors and low-voltage bandgap references that can work down to 1 V. We have seen that the simple current mirror requires a gate-source voltage drop at the input to function properly. This voltage can be as much as 1 V or more depending on the W/L and the current. The minimum power supply would be the voltage plus a saturation voltage of a current source or sink. Consequently, the minimum power supply would be

$$V_{DD}(min) = V_t + 2\,V_{DS}(sat) \quad \ldots\ldots \quad 2.9$$

Or course, this situation becomes worse if cascode current mirrors are used. The minimum input voltage for the self biased cascode current mirror is the same as that of equation2.9. These are two ways of decreasing the voltage required across the input of the current mirror. One is to use bulk-driven devices and the other is to level shift the drain voltage below the gate voltage. We noted above that the bulk-driven MOSFET is normally operated in the depletion region but that it is possible to slightly forward bias the bulk-source junction. Under these conditions, the bulk-driven MOSFET can yield a low-voltage current mirror. A simple current mirror using bulk-driven MOSFET is shown in Fig.2.6. The gates taken to V_{DD} to form

channels in M1 and M2. If the value of I_{IN} is greater than I_{DSS}, then V_{BS} is greater than zero and the current mirror functions as a normal current mirror. In the following material, we would discuss about these various techniques in detail.

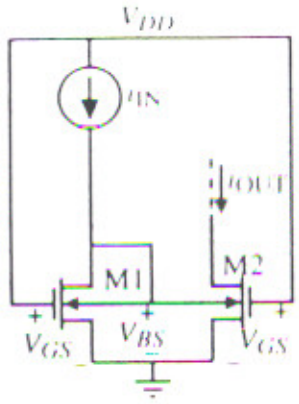


Figure 2.6 Simple Bulk Driven Current Mirror

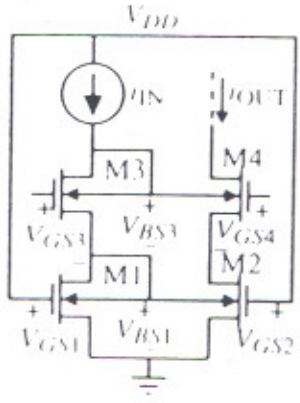


Figure 2.7 Bulk Driven Cascode Current Mirror

HIGH PERFORMANCE ARCHITECTURES

3.1 Constant–g_m Rail-to-Rail CMOS Op-Amp Input Stage with Overlapped Transition Regions

The schematic of a complementary input stage is shown in Fig. 3.1, where M1n, M2n and M1p, M2p constitute the n- and p-type differential input pairs respectively.

The gm of this input stage is constant if the following equation is satisfied:

$$\sqrt{\beta_n I_{sn}} + \sqrt{\beta_p I_{sp}} = const. \qquad \ldots\ldots \quad 3.1$$

where $\beta_n = \beta_n C_{ox} W_n / L_p$, $\beta_p = \beta_p C_{ox} W_p / L_p$, and I_{sn} and I_{sp} are the bias current for the n- and p-pair transistors, respectively. By choosing $\beta_n = \beta_p$, g_m is constant if $\sqrt{I_{sn}} + \sqrt{I_{sp}}$ is constant. Fig 3.1. shows three regions of operation, for I_{sn} and I_{sp}.

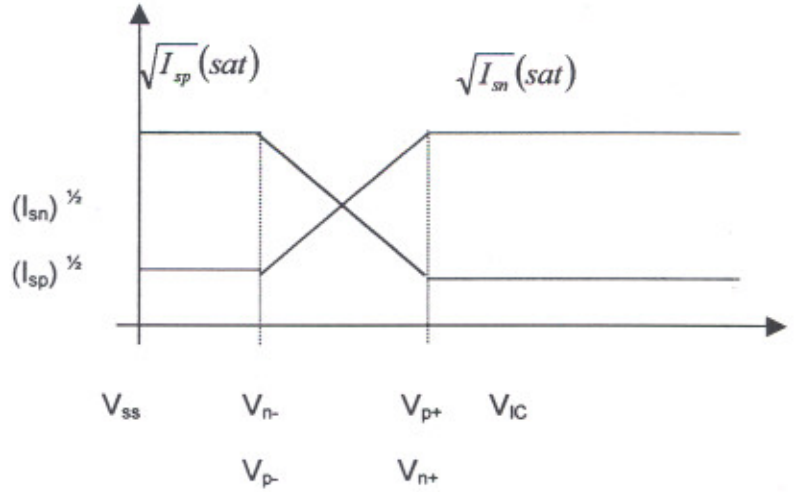


Figure 3.1 Regions Of Operation Of The NP- Differential Pair

The current in each region is described as follows :

cutoff

$$I_{sn} = 0 \qquad \ldots\ldots \quad 3.2$$

$$V_{SS} \le V_{cm} \le V_n$$

Transition

$$I_{sn} = I_{sn}(V_{cm}) \qquad \ldots\ldots \quad 3.3$$

$$V_n < V_{cm} \le V_n^+$$

Saturation

$$I_{sn} = I_{sn0} = \frac{\beta_{MBn}}{2}\left(V_{GSMBn} - V_{ss} - V_{tn}\right)^2 \qquad \ldots\ldots \quad 3.4$$

$$V_n^- \le V_{cm} \le V_{dd}$$

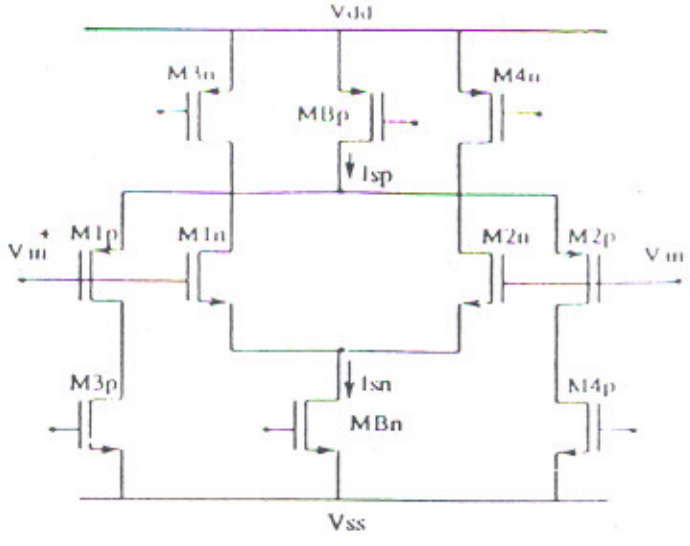


Figure 3.2 Complimentary N-P Differential Input Stage

where I_{sn0} is the saturation current for the n-pair transistors. In the cutoff region, M1n and M2n are in cutoff, MBn is in linear region, and the currents through them are all zero. In the transition region, M1n and M2n are in saturation, and MBn is in the linear region. The voltage V_{DSMBn} is very small when V_{cm} approached V_n and increases with increasing V_{cm} until MBn enters into the saturation region. In the maximum I_{sn} region, as specified by, all three transistors (M1n, M2n and MBn) enter into the saturation region. The subthreshold region between the cutoff and the transition region is not considered here for the sake of simplicity.

The lower boundary of the transition region V_n^- is given by

$$V_n^- = V_{ss} + V_{tn} + V_{DS\text{-}MBn} \qquad \ldots\ldots \quad 3.5$$

The fact that $I_{D\text{-}MBn}$ is almost zero at V_n^- and that $V_{GS\text{-}MBn}$ is always greater than V_{tn} implies that $V_{DS\text{-}MBn}$ must be negligible, so can be approximated by

$$V_n^- \approx V_{ss} + V_{tn} \qquad \ldots\ldots \quad 3.6$$

At the upper boundary of the transition region V_n^+, MBn is at the transition from the linear to the saturation, i.e.,

$$V_{DG\text{-}MBn} = -V_{tn} \quad \ldots\ldots \quad 3.7$$

Since V_{DG_MBn} can be expressed as $V_n^1 - V_{tn} - \sqrt{I_{sn0}/\beta_{MIn}} - V_{G\_MBn}$ can be rewritten as

$$V_n^+ = V_{G\_MBn} + \sqrt{\frac{I_{sn0}}{\beta_{MIn}}} \quad \ldots\ldots \quad 3.8$$

To derive a general expression for I_{sn} in the transition region, consider the following equations :

$$I_{sn} = -\beta_{M1n}(V_{cm} - V_{D\_MBn} - V_{tn})^2 \quad \ldots\ldots \quad 3.9$$

$$I_{sn} = \beta_{MBn}\left(V_{G-MBn} - V_{ss} - V_{tn} - \frac{V_{D\_MBn} - V_{ss}}{2}\right)(V_{D-MBn} - V_{ss})$$

$$\ldots\ldots \quad 3.10$$

To simplify the analysis, we assume $(W/L)_{MBn} = 2\,(W/L)_{Min}$, i.e.

$$\beta_{MBn} = 2\,\beta_{MBn}$$

V_{D_MBn} can be solved from to be

$$V_{D\_MBn} = \frac{V_{cm} + V_{G\_MBn}}{2} - V_n - \frac{1}{2}\sqrt{2\left(-V_{cm} + V_{G\_MBn} - V_{ss}\right)^2 - \left(V_{cm} - V_{G\_MBn}\right)^2}$$

$$\ldots\ldots \quad 3.11$$

Substituting for $V_{D\text{-}MBn}$ from we have shown at the bottom of the page. It can be verified from that I_{sn} is zero for $V_{cm} = V_n^-$ and it is I_{sn0} for $V_{cm} = V_n^+$.

The boundaries of the transition region for the p-pair can be found similarly to be

$$V_p^+ = V_{dd} + V_p \quad \ldots\ldots \quad 3.12$$

$$V_p^- = V_{V\_MBnp} - \sqrt{\frac{I_{sp0}}{\beta_{MBp}}} \quad \ldots\ldots \quad 3.13$$

I_{sp} is shown in at the bottom of the page. One can also easily verify from that I_{sp} is zero for $V_{cm} = V_p^+$, and it is I_{sp0} for $V_{cm} = V_p^-$, where I_{sp0} is the current in the saturation region for the p-pair i.e.,

$$I_{sp0} = (\beta_{MBp}) \times (-V_{G\_MBp} + V_{dd} + V_{tp})^2. \quad \ldots\ldots \quad 3.14$$

It has been observed that as long as β_{MBn} is comparable with β_{MBn}, very similar results to and can be obtained. So we will use these two equations in the following analysis.

$$I_{sn} = \beta_{MBn}\left[\frac{V_{cm} - V_{G-MBn}}{2} + \frac{1}{2} - \frac{1}{2}\sqrt{2\left(-V_{tm} + V_{G\_MBn} - V_{ss}\right)^2 - \left(V_{cm} - V_{G\_MBn}\right)^2}\right]^2 \quad \ldots\ldots \quad 3.15$$

$$I_{sn} = \beta_{MIp}\left[\frac{-V_{cm} - V_{G-MBp}}{2} + \frac{1}{2} - \frac{1}{2}\sqrt{2\left(-V_{tp} + V_{G\_MBp} - V_{dd}\right)^2 - \left(V_{cm} - V_{G\_MBp}\right)^2}\right]^2 \quad \ldots\ldots \quad 3.16$$

Equations 3.15 and 3.16 shows that $\sqrt{I_{sn}}$ is monotonically increasing within the transition region while $\sqrt{I_{sp}}$ is monotonically decreasing. If the transition regions of the n- and p-pairs are properly overlapped, a relatively constantly $\sqrt{I_{sn}} + \sqrt{I_{sp}}$ or gm can be achieved.

By the symmetry between the n- and p-pairs, we can assume that $I_{sp0} = I_{sn0}$, $\beta_{MIp} = \beta_{MIn}$, and $V_{G\_MBp} = -V_{G\_MBn}$. We also assume that $V_{tp} = -V_{tn}$ for simplicity. Recall that the boundaries of the transition regions are as expressed by where V_n^- and V_p^- depend on the dimensions of the transistors of the differential pairs. Let,

$$V_p^- = V_n^- \quad \ldots\ldots \quad 3.17$$

or, equivalently

$$V_p^+ = V_n^+ \quad \ldots\ldots \quad 3.18$$

Which means the transition of the n- and p-pairs are overlapped. As illustrated in Fig, we locate V_p^- exactly at the same position as V_n^- and locate V_n^+ at V_p^+ . Using and we have

$$V_{G\_MBn} + \sqrt{\frac{I_{sn0}}{\beta_{MIn}}} = V_{dd} - |V_{tp}| \quad \ldots\ldots \quad 3.19$$

Therefore

$$\beta_{MIn} = \frac{I_{sn0}}{\left(V_{dd} + V_{tp} - V_{G\_MBn}\right)^2} = \beta_{MIp} \quad \ldots\ldots \quad 3.20$$

which is close to the theoretical value of 12 A/V² verifying our theoretical analysis. The optimal g_m obtained is constant within 9%.

Suppose K_n = 60 μA/V², the aspect ratio of M1n is 1/5. Aspect ratios of the input transistors of the differential pairs are calculated to be less than one for n-pair and close to one for p-

pair. These small β's for the input differential pairs widen and linearize the transition regions where the increasing $\sqrt{I_{sn}}$ and the decreasing $\sqrt{I_{sp}}$ cancel each other, thus yielding a constant g_m. Unfortunately, the small aspect ratios of the differential pairs degrade the noise performance and cause the circuit to be more sensitive to the mismatch between the pair transistors.

3.1.1 Complementary Input Stage with DC Level Shifter

In this section, we present another technique to overlap the transition regions without sacrificing the g_m [3]. From the analysis carried out in the previous section, we know that as long as the two transition regions overlap properly, constant g_m can be obtained. It can be observed from and that β is proportional to the slopes of the curves for the transition region. To obtain overlapped transition regions while preserving the original slope of the curve (i.e. keeping the original large β) in the transition region, a dc level shifter can be introduced to shift the p-transition curve leftward to overlap the n-transition curve as shown in Fig. If the level shifting is too small, gm exceeds the nominal constant value. If the amount of level shifting is too large, g_m drops below the nominal constant value. There is an optimal shift $\Delta V_{optimal}$, which yields a constant gm. The optimal shift can be easily realized using a conventional source follower.

Since, it is difficult to derive an expression for the optimal shift $\Delta V_{optimal}$, the authors [7] have identified the narrow range within which the optimal value for ΔV_{shift} exists. This range can be defined as follows:

$$2V_{G\_MBn} < \Delta V_{optimal} < 2V_{G\_MBn} + \sqrt{\frac{I_{sn0}}{\beta_{M1}}} \qquad \ldots\ldots \quad 3.21$$

3.1.2 Implementation of an Op-Amp with Complementary Input Stage Using DC Level Shifters

Fig. 3.2 shows the op-amp with the dc level shifters in the complementary input stage. The pair of dc level shifters is implemented by two pairs of PMOS source followers MS1 – MS4, as indicated in Fig 3.3. The op-amp consists of three stages : the complementary input stage, the folded cascode stage M21 – M28, and the class AB output stage M30 – M33. Transistors MB1 – MB11 are used to bias the circuit, and their dimensions also determine V_{G_MBn} and V_{G_MBp}, respectively. The folded cascode stage provides high gain while keeping the input and output swing high.

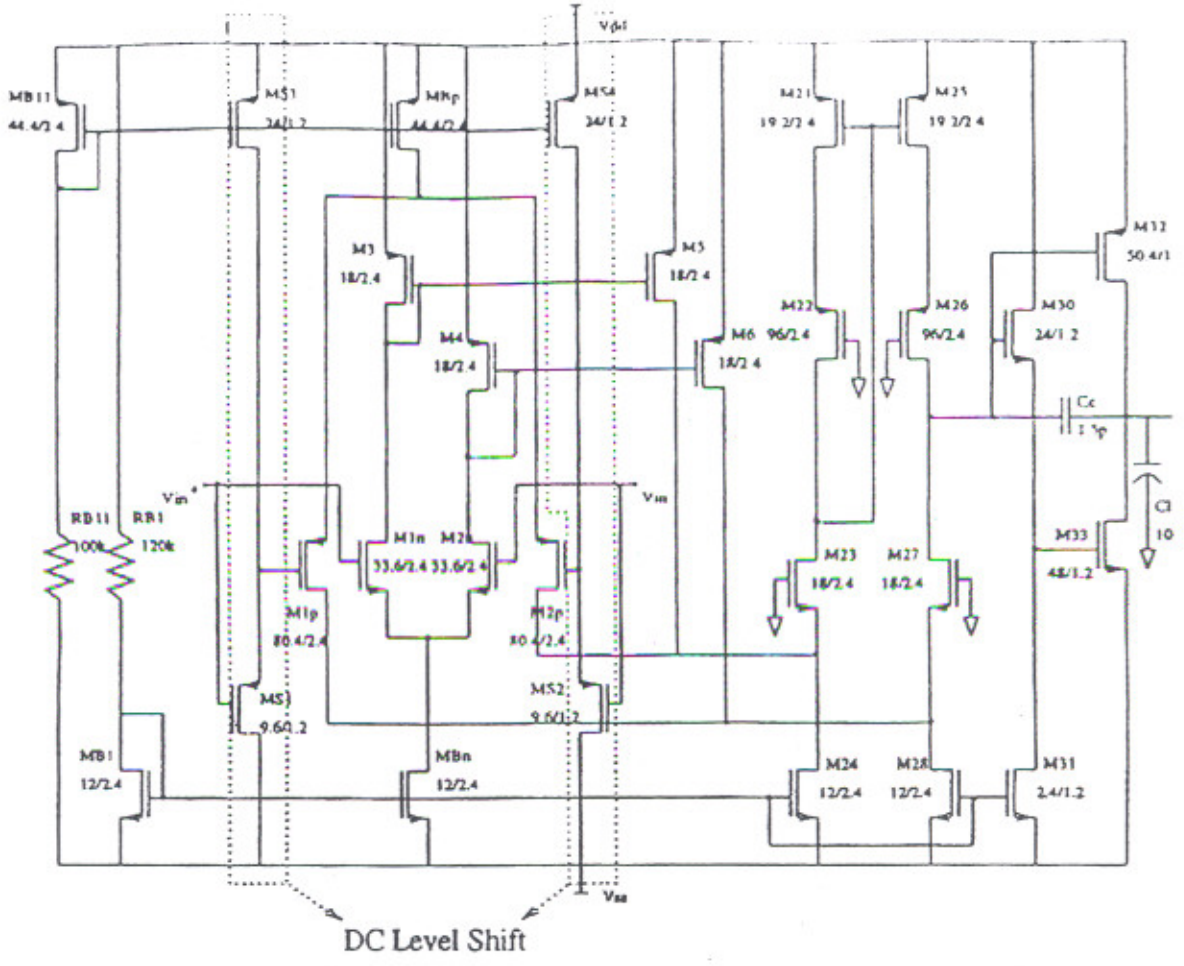


Figure 3.3 Schematic Of An Op-Amp With Level Shifters In The Complimentary Input Stage

The amplitudes and the phases are heavily dependent upon the applied common-mode input voltage V_{cm}, which is varied from rail (-1.5 V) to rail (1.5 V) by a step of 0.1 V. This op-amp is unstable and cannot be compensated due to the varying gm, as we stated in the introduction. In contrast, the frequency responses of the op-amp with level-shifted input stage for the common-mode input voltage V_{cm} varying from rail to rail by a step of 0.1 V. The amplitudes and the phases of the proposed op-amp are almost independent of the applied V_{cm}. It can be observed that by using dc level shifters, the degradation of the CMRR is reduced to 45 dB, compared to 55 dB for the case that uses no level shifters.

3.2 A New Rail-to-Rail Input Stage

The input stage architecture used in this amplifier is shown in Fig. An enhancement, bulk-driven differential pair of p-channel transistors, MP1 and MP2, is used to generate transconductance. However, instead of driving the bulks directly from the inputs, depletion-

mode n-channel transistors MN1 and MN2 are used as source followers to buffer the inputs from the p-channel bulk terminals. MN1 and MN2 also provide a common-mode dependent level-shifting function to the bulk terminals, which minimizes excess bulk currents when the input common-mode voltages are near V_{EE} potentials. The modulated drain currents of MP1 and MP2 are folded into the current summing nodes of the cascode circuit at the sources of MN3 and MN4, with current mirror MP3 and MP4 performing a differential-to-single-ended conversion to the high impedance output node V_{01}.

The use of the deplection-mode source followers MN1 and MN2, in conjunction with the bulk-driven p-channel differential pair MP1 and MP2, allows additional design flexibility to meet the rail-to-rail input requirements of the amplifier. The input depletion-mode source followers may be designed to level-shift the input signal to MP1 and MP2 and their bias current. In fact, MN1 and MN2 can be operated in strong inversion if the process technology and bias point of the circuit dictate. This allows the input circuit architecture to be used over a greater range of threshold voltages and well concentrations for the depletion-mode transistors.

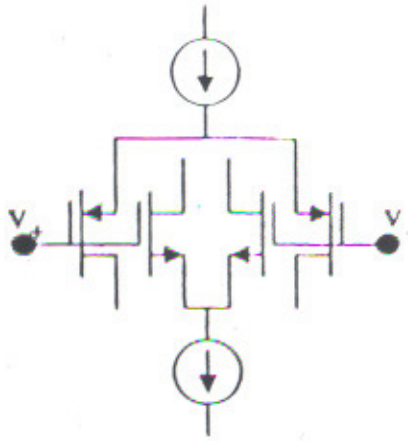


Figure 3.4

The design methodology for input source followers MN1 and MN2 is shown below. The drain current in a MOS transistor operating in weak inversion is given by :

$$I_D = I_{DO} \exp\left(\frac{V_{GS}}{nV_T}\right)\left(\exp\left(\frac{-V_{SB}}{V_T}\right) - \exp\left(\frac{-V_{DB}}{V_T}\right)\right) \qquad \ldots\ldots \quad 3.22$$

where n is the subthreshold slope factor, V_T is the thermal voltage, and I_{DO} is the characteristic current of the device. Solving for V_{GS} gives

$$V_{GS} = nV_T\left(\ln\left(\exp\left(\frac{-V_{SB}}{V_T}\right) - \exp\left(\frac{-V_{DB}}{V_T}\right)\right) - \ln\left(\frac{I_D}{I_{DO}\frac{W}{L}}\right)\right) \qquad \ldots\ldots \quad 3.23$$

which can be further simplified (assuming V_{DB} V_{SB}) to

$$V_{GS} = n V_{SB} + C \qquad \ldots\ldots 3.24$$

Therefore, V_{GS} increases as a linear function of V_{SB}. As V_{SB} increases to the positive supply voltage, the influence of the V_{DB} term may become significant if the threshold voltage modulation due to back gate effect is not sufficiently large (i.e., the transistor's V_{DS} voltage is small). The constant C, which is determined by the bias and aspect ratio of the transistor, can be adjusted to give a desired V_{GS} value when V_{SB} = 0 (VC = 0) to meet biasing requirements, such as for current source I_1 in Fig 3.6. But since the n-channel depletion-mode transistors MN1 and MN2 act as source followers and do not substantially affect the input stage transconductance, the designer has more flexibility in meeting the bias point constraints and target transconductance of the input stage in a given process.

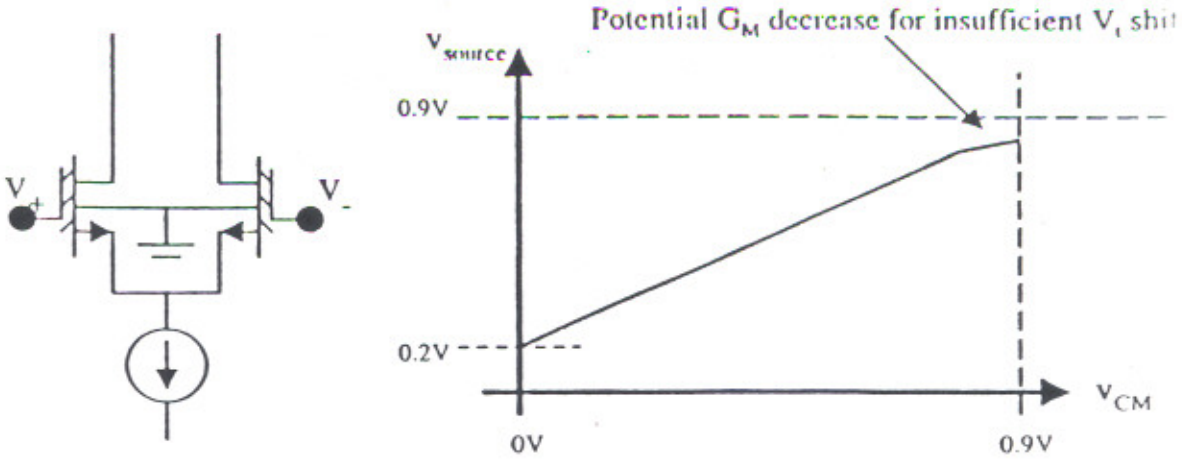


Figure 3.5 Depletion Mode n-channel Differential Transconductor

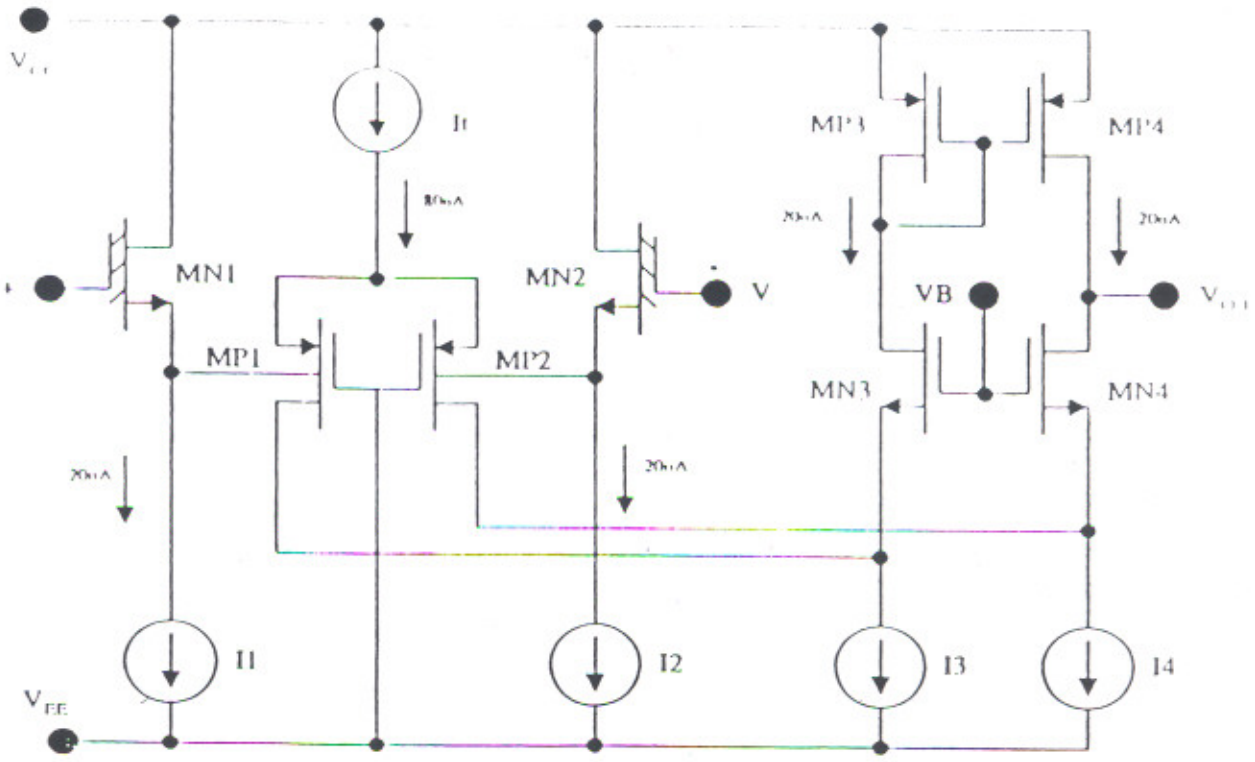


Figure 3.6 New Input Stage

The minimum operating power supply of this input stage to meet rail-to-rail input common-mode requirements is determined by the threshold voltage shift due to back-gate effect in the process. Insufficient threshold voltage modulation decreases the transconductance at common-mode voltages near the positive supply. Since the g_m of input follower transistors MN1 and MN2 decreases when they operate in linear mode. Conversely, the input stage will operate at supply voltages lower than 0.9 V with the common-mode range decreasing below the positive supply.

DESIGN AND ANALYSIS

4.1

4.1.1 Notations and formulas

To accomplish our design we use the theoretical values of the following parameters [1]

K_n ... 60 μA/V²

K_p ... 25 μA/V²

λ ... 0.01 μA/V (for 2μm process)

$|V_{tp}|$ ... 0.64V

V_{tn} ...0.74V

$$S = \frac{g_m^{\ 2}}{2 \times I \times k_{n/p}} \qquad \text{...4.1.1}$$

$$v_{on} = \sqrt{\frac{2 \times I}{k_{n/p} \times S}} \qquad \text{...4.1.2}$$

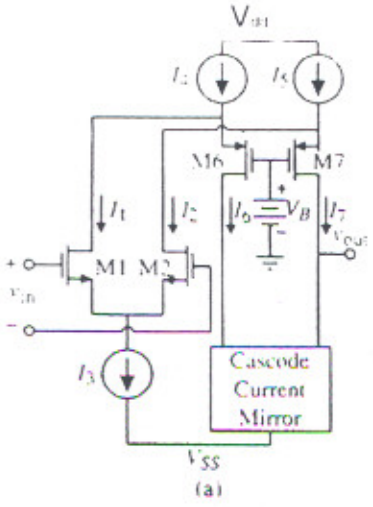
$$g_{m1}^{\ 2} = 2 \times I \times \beta \quad \text{Where } \beta = k_{n/p} \times S \qquad \text{..:4.1.3}$$

$$g_{ds} = \lambda \times I_{ds} \qquad \text{...4.1.4}$$

4.1.2 A Rational Approach to Small Signal Analysis of Op-Amp's

Let us briefly digress about the AC analysis of the folded cascode structure and analogously develop an approximate expression for our parallel transconductance amplifier. To discuss about the gain of the folded cascade amplifier, we assume the matching of the transistors and a symmetric design.

Let's say $g_{m1} = g_{m2}$ as we have symmetrically biased the transistors, same current flowing through the two transistors $I_1 = I_2 = 0.5.I_3$



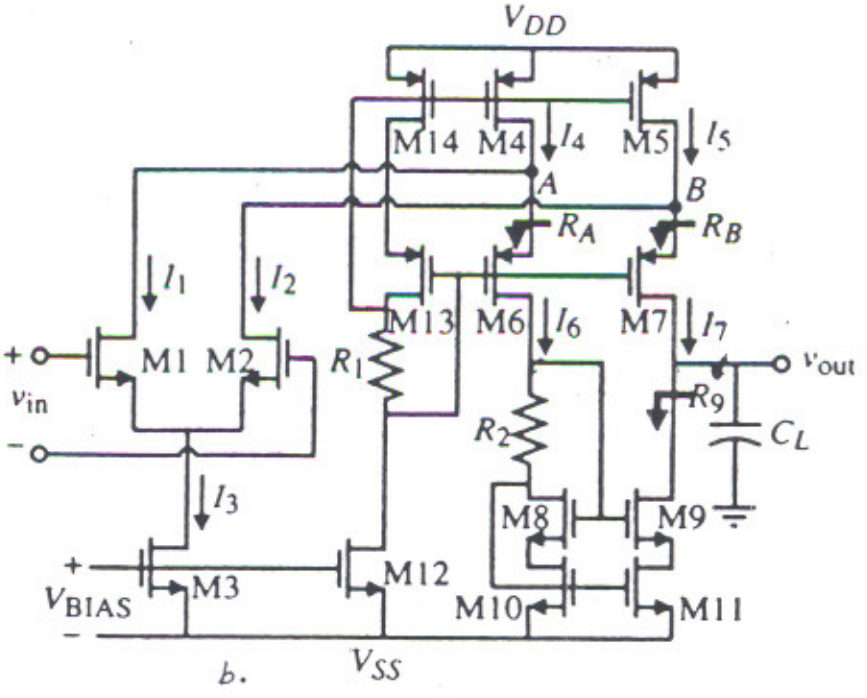


Figure . 4.1 Schematic Of a Folded Cascode Op-Amp

a: BLACK BOX REPRESENTATION

b: COMPLETE SCHEMATIC

Referring to the figure (4.1b)

r_{out} = output resistance of the folded cascode stage.

$r_{out} = r_p \parallel r_n$, ...4.1.5

Where,

r_p denotes the resistance contributed to the output by the p-pair of the transistors namely referring to the figure 4.1 by the resistance looking into the drain of M7, and

r_n denoting the resistance looking into the drain of the n transistor M9 [1]

=> $r_p \cong r_{ds7} \times g_{m7} \times r_{ds5}$ and ...4.1.6

$r_n \cong r_{ds9} \times g_{m9} \times r_{ds11}$

Now just by reasoning we can ascertain the gain in the folded cascade structure as follows: Since application of a potential $v_{in}/2$ at the gate of M_1 produces a current source of $(g_{m1}v_{in})/2$ which is further supplied to the folded-cascode stage and is mirrored by the transistor pairs (M_{10} M_{11}) to the output. Similarly we have for the transistor M_2 a current $(g_{m2}v_{in})/2$ which also reinforces current in the same direction as the earlier source $g_{m1}v_{in}/2$

The total current $((g_{m1}v_{in})/2 + (g_{m2}v_{in})/2)$ flows in the output resistance to produce the output voltage.

$v_{out} \approx (g_{m1}v_{in}/2 + g_{m2}v_{in}/2) . r_{out}$ ...4.1.7

$$Av \approx \left(\frac{g_{m1} + g_{m2}}{2}\right) \times \frac{g_{m7} r_{ds7} r_{ds5} \times g_{m9} r_{ds9} r_{ds11}}{g_{m7} r_{ds7} r_{ds5} + g_{m9} r_{ds9} r_{ds11}} \quad \text{...4.1.8}$$

since we have assumed that $g_{m1} = g_{m2}$

$$Av \approx g_{m1} \times \frac{g_{m7} r_{ds7} r_{ds5} \times g_{m9} r_{ds9} r_{ds11}}{g_{m7} r_{ds7} r_{ds5} + g_{m9} r_{ds9} r_{ds11}} \quad \text{...4.1.9}$$

Working on the same lines for our parallel transconductance stage we have analogously

$r_{out} = r_{p1} \parallel r_{n1}$, where these resistances have been analogously defined

$$r_{p1} \cong r_{ds17} \times g_{m17} \times r_{ds12} \quad \text{...4.1.10}$$

$$r_{n1} = r_{ds7} \times g_{m7} \times \left[r_{ds5} \parallel (r_{ds24} + r_{ds19})\right] \quad \text{...4.1.11}$$

$$A_v \approx g_{m1} \times r_{out} \quad \text{...4.1.12}$$

4.2 SMALL SIGNAL ANALYSIS OF A GENERIC TWO STAGE OP-AMP [1]

The design of the conventional two stage amplifiers presented, the first stage being the differential stage and the second being the inverting amplifier. As in we discuss the most

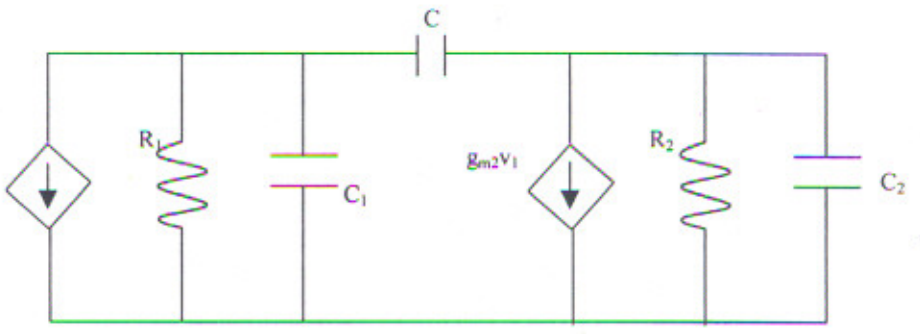


Figure 4.2 : AC model of two stage Op-Amp for small signal analysis

generic case to analyze this configuration .we neglect small capacitances, which do affect less on the dominant poles &zeros and don't significantly alter the bode plot in the gain bandwidth region. To begin our analysis of this configuration we need to specify the

r_i = resistance of the i'th stage ...4.2.1

C_i = capacitance of the i'th stage ...4.2.2

C = Coupling capacitance ...4.2.3

g_{mi} = transconductance of the i'th stage, refer figure4.3 ...4.2.4

To have the nodal analysis we thereby start at the first node ref[1]

$$v_1(sC_1 + sC + g_1) - v_2(sC) + g_{m1}v = 0 \quad ...4.2.5$$

$$v_2(sC_2 + sC + g_2) - v_1(sC) + g_{m2}v_1 = 0 \quad ...4.2.6$$

rearranging the second equation we have $v_1 = - v_2(sC_2 + sC + g_2) / (sC - g_{m2})$

now putting this value of v1 in the first equation we have

$g_{m1}v_{in}$

$$v_2\{(sC_2 + sC + g_2) / (sC - g_{m2})\}.(sC_1 + sC + g_1) - v_2(sC) + g_{m1}v = 0 \quad ...4.2.7$$

Now rearranging the above equation we have

$$v_2 = v_0 = \frac{-v(sC - g_{m2})}{\{(sC_2 + sC + g_2)(sC_1 + sC + g_1) - sC(sC - g_{m2})\}} \quad ...4.2.8$$

Now to analyze the characteristic equation thoroughly

$$(sC_2 + sC + g_2)(sC_1 + sC + g_1) - (sC - g_{m2}).sC = 0$$

$$s^2(C_2C + C_1C + C_1C_2) + s\{ g_1(C_2 + C) + g_2(C_1 + C) + g_{m2}C \} + g_1g_2 = 0$$

...4.2.9

On comparing this with the typical Quadratic Equation

$$1 + as + bs^2 = 0$$

where we can write it as

$\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right) = 0$, where p_1 & p_2 are roots of the Equation

and $p_1 << p_2 \Rightarrow 1/p_1 >> 1/p_2$

$$\Rightarrow \quad 1+\frac{s^2}{p_1p_2}+s\left(\frac{1}{p_1}+\frac{1}{p_2}\right)=0 \qquad \text{...4.2.10}$$

On comparing this Equation with the above we have,

$$\frac{1}{p_1}+\frac{1}{p_2}=\frac{(g_1(C_2+C)+g_2(C_1+C)+g_{m2}C)}{g_1g_2} \qquad \text{...4.2.11}$$

$$\frac{1}{p_1p_2}=\frac{C_2C+C_1C+C_1C_2}{g_1g_2} \qquad \text{... 4.2.12}$$

From the above, we know $\frac{1}{p_2}+\frac{1}{p_2}\approx\frac{1}{p_1}$

$$\Rightarrow \quad p_1 = \frac{g_1 \times g_2}{(g_1(C_2 + C) + g_2(C_1 + C) + g_{m2}C)}$$

And $p_2 = \frac{(g_1(C_2+C)+g_2(C_1+C)+g_{m2}C)}{C_2C+C_1C}$

Now we apply some assumptions to real amplifier as we know while designing we have

$C_2 > C >> C_1$, so putting these approximations below we have

$$p_1 = \frac{g_1 \times g_2}{(g_1C_2 + g_2C + g_{m2}C)} \qquad \text{...4.2.13}$$

$$p_2 = \frac{(g_1C_2 + g_2C + g_{m2}C)}{C_2C} \qquad \text{...4.2.14}$$

knowing that $g_m >> g_i$ we get as follows

$$p_1 = \frac{g_1 \times g_2}{(g_1 C_2 + g_{m2} C)}$$

$$p_2 = \frac{(g_1 C_2 + g_{m2} C)}{C_2 C}$$

=> $$p_1 = \frac{g_1 \times g_2}{g_{m2} C} \quad \text{...4.2.15}$$

$$p_2 = \frac{g_{m2}}{C_2} \quad \text{...4.2.16}$$

and we have $z_1 = \frac{g_{m2}}{C}$ ...4.2.17

So we have formed an equation for the bode plot as follows

$$|A_v| = \frac{K \times \left(1 - \frac{s}{z_1}\right)}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)} \quad \text{...4.2.18}$$

where K is the gain in the GB region as

$$K = \frac{g_{m1} \times g_{m2}}{g_1 \times g_2} \quad \text{...4.2.19}$$

Now to have an appropriate phase margin we have

$$\varphi = -\arctan\left(\frac{\omega_0}{z}\right) - \arctan\left(\frac{\omega_0}{p_1}\right) - \arctan\left(\frac{\omega_0}{p_2}\right) \quad \text{...4.2.20}$$

Where ωo = radian frequency at which $|A_v|$ = 1 i.e the gain bandwidth. To have an phase margin of about 45- 60 degrees to ensure stability we have

$$\varphi = -\arctan\left(\frac{\omega_0}{z}\right) - \arctan\left(\frac{\omega_0}{p_1}\right) - \arctan\left(\frac{\omega_0}{p_2}\right) = 120^\circ \quad \text{...4.2.21}$$

Now suppose we place zero to be far away from the gain BW ω_o From the definition of GBW(Gain Bandwidth) we know $\omega_o = p_1 . K$. Putting this into the above equation we have

$$-120^\circ = -\arctan\left(\frac{1}{10}\right) - \arctan\left(\frac{K}{1}\right) - \arctan\left(\frac{\omega_0}{p_2}\right) \quad \text{...4.2.22}$$

allowing the minimum value of K(min) = 5000V/V

$$-120^{\circ} + \arctan\left(\frac{1}{10}\right) + \arctan\left(\frac{5000}{1}\right) = \arctan\left(\frac{\omega_0}{p_2}\right) \qquad \ldots 4.2.23$$

=> $24.3^{\circ} = \arctan\left(\frac{\omega_0}{p_2}\right)$ taking the tangent of both sides we have $\omega_o / p_2 = 0.4515$

=> $$p_2 = \frac{\omega_0}{0.4515} = 2.214665245 \qquad \ldots 4.2.24$$

from the above relations we enumerate as follows as we have

$$p_2 = \frac{g_{m2}}{C_2} \text{ and } \omega_0 = p_1 \times K = \frac{g_{m1}}{C} \qquad \ldots 4.2.25$$

$$\frac{g_{m2}}{C_2} = 10\frac{g_{m1}}{C}$$

=> $g_{m2} = 10g_{m1}$ ...4.2.26

From equation 5.2.25 and 5.2.26 we have

$$C \geq 0.2124C_2$$

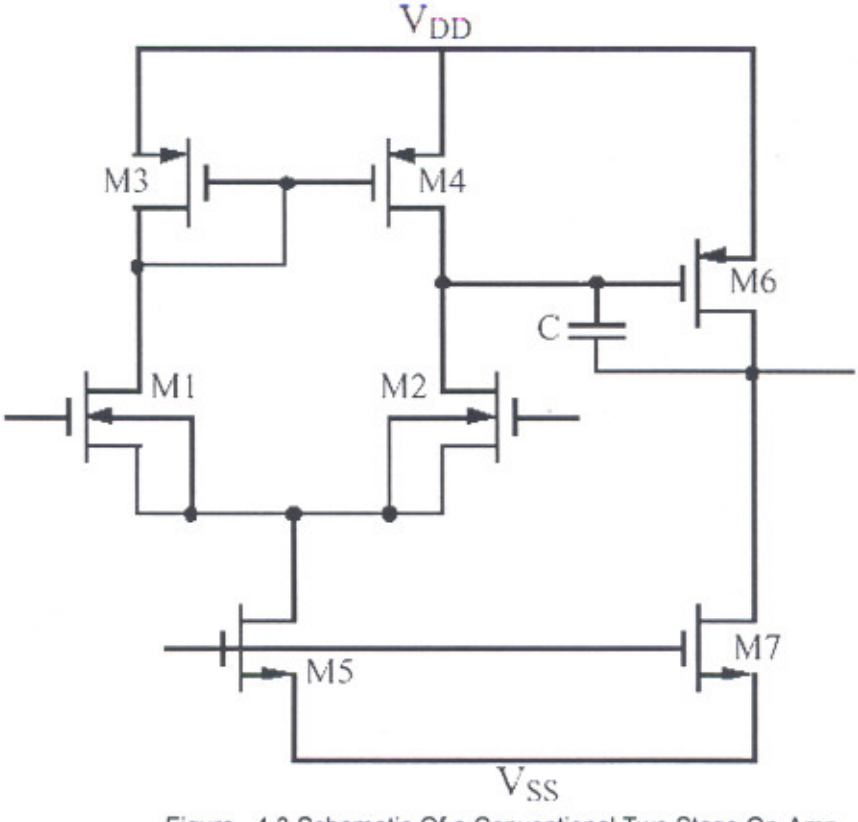


Figure . 4.3 Schematic Of a Conventional Two Stage Op-Amp

4.3 A DESIGN STRATEGY FOR LOW POWER FOR THE TWO STAGE OP-AMP

On the low power side, here's presented the design of the Op-Amp, where we have the constraint that the (power dissipation) P_d < 1 mW. For this section we refer to the figure 4.3

Under $\pm$ 2.5 V power supply this means that I_{total} < 200 μA (total current)

=> $I_5 + I_7$ < 200 μA say I_{total} = 100μA

As we know $$Av = \frac{-g_{m1} \cdot g_{m6}}{g_1 \cdot g_2} \quad \text{...4.3.1}$$

where ,

$g_1 = g_{ds2} + g_{ds4}$, denoting the conductance of source to drain of the respective transistor , similarly $g_1 = g_{ds6} + g_{ds7}$

so as we know [1][6],

$$g_1 = \lambda I_2 + \lambda I_4 \quad \text{...4.3.2}$$

$$g_2 = \lambda I_6 + \lambda I_7$$

since by KCL we get $I_6 = I_7$ and similarly $I_2 = I_4$ we have $g_1 = 2\lambda I_2$ & $g_2 = 2\lambda I_6$

As we know $$A_v = 10.\frac{g_{m1}^{\ 2}}{4 \times \lambda^2 \times i_2 \times i_7} \quad \text{...4.3.3}$$

So, we want $I_5 \cdot I_7$ to be minimum to have an ample amplification

Now, $$I_5 + I_7 = I_{total} \quad \text{...4.3.4}$$

Let $$I_5 \times I_7 = P \quad \text{...4.3.5}$$

$P = (I_{total} - I_7)I_7$ and the maximum P, by applying differential analysis goes for

$$I_5 = I_7 = \frac{I_{total}}{2} \quad \text{...4.3.6}$$

To avoid designing with this value and striving for a higher gain , we choose $I_5 : I_7$: : 60 : 40 as the output resistance of the folded cascode stage would be maximized together with the transconductance of the first stage with a ratio greater than 1:1.

assuming V_{on5} = 0.25 V

=> S_5 > 32 . Let S_5 be 50 so that we have V_{on5} = 0.2 V

Now considering the expression for A_v we have

$$A_v = 5.\frac{g_{m1}^{\ 2}}{\lambda^2 \times i_2 \times i_7} \quad = \quad A_v = 5.\frac{g_{m1}^{\ 2}}{\lambda^2 \times i_5 \times i_7} \quad = \quad A_v = 5.\frac{g_{m1}^{\ 2}}{\lambda^2 \times 60 \times 40}$$

$A_v = 20.833 \times g_{m1}^2$

Say, if we want A_v = 5000 V/V, we have

g_{m1}^2 > 240 (μA/V)^2 => g_{m1} > 15.49 μA/V

So, let us have g_{m1} = 100 μA/V (a fairly modest value) => S_{1n} = 2.666667,

approximating it to 3, we get

g_{m1} = 103.92 μA/V

V_{on1} = 0.577 V

from equation 4.2.26 and 4.1.1, we get

g_{m6} = 10. g_{m1} = 1039.234 μA/V

$$S_6 = \frac{g_{m6}^2}{2 \times k_p \times I_6} \quad \Rightarrow \quad S_6 = 540$$

Now to have a symmetric design we have equal bias for all p transistors

$$\frac{g_{m4}}{S_4} = \frac{g_{m6}}{S_6} \qquad \ldots 4.3.7$$

, on squaring both sides and manipulating the equation for S_4 we get

$$S_4 = \frac{2 \times K_p \times I_4}{\frac{g_{m6}^2}{S_6^2}} = \frac{2 \times 25 \times 30}{\left(\frac{1039.24}{540}\right)^2} = 404.9925 = 405 \text{(approx)}$$

=> V_{on4} = 0.076 V ...4.3.8

From the earlier derived Relations as enumerated above in equation 1.14 & 1.16 we get

v_{ic} (max) = 2.5 - 0.65 + 0.7 - 0.076

= 2.55 - 0.076 = 2.473 V

v_{ic} (min) = - 2.5 + V_{on1} + V_{on5} - V_{in} (max)

= - 2.5 + 0.2 V + 0.577 + 0.75

v_{ic} (min) = - 0.97 V

4.4 DESIGN OF THE FOLDED CASCODE OPERATIONAL AMPLIFIER

The design of the folded cascode amplifier is presented below, it is augmented with an example using the parameters given in the model file. The amplifier has been designed optimizing on the following constraints:

P_d (power dissipation),

ICMR which has been the main concern of this document)

To design the folded cascode amplifier our first concern would be the power dissipation. Let's assume that operating on $\pm 2.5V$ power supply, the power dissipated $P_d \leq 1000\mu W$ (referring to the figure 5.2) , this implies that

$$P_d = 5(I_3 + I_4 + I_{12} + I_{14}) \leq 1000\mu W \quad \ldots 4.4.1$$

$$(I_3 + I_4 + I_{12} + I_{14}) \leq 200\mu A \quad \ldots 4.4.2$$

By the symmetry of design we have $I_{12} = I_{14}$, which implies

$(I_3 + I_4 + 2I_{12}) \leq 200\mu A$, now to have minimum power consumption we have assumed that

$$I_3 = \frac{I_4}{2} \text{ and. By KCL we know } I_3 = I_{15}$$

And we assume currents to be as follows ...4.4.2a

$I_3 = 30\mu A$ => $I_4 = 60\mu A$ and $I_{12} = I_{14}$ =45μA and by the configuration of the Folded cascode we have $I_{11} = I_{10} = I_2 = I_8 = 15\mu A$ ...4.4.2b

so, that we have $I_{total} = 170\mu A$

To have the maximum output range i.e. v_{out}(max/min)= $\pm 2V$ we have

$v_{on14} + v_{on10} < 0.5V$ and similarly ...4.4.3

$v_{on9} + v_{on7} < 0.5V$ ...4.4.4

Choosing on the margin we have $v_{on14} = v_{on10} = 0.25V$ and symmetrically

$v_{on7} = v_{on9} = v_{on2} = v_{on8} = 0.25V$, ...4.4.5

carrying on these lines we have the current from equation 4.4.2 and we get from equation 4.1.2 ,

$S_{2/7/8/9} = 7.586$

$S_{13/11/10} = 18.2163$

To choose maximum ICMR we select the S(aspect ratio) for the M_4 as guided by the constraint $v_{on4} < 0.25V$ $\Rightarrow S_4 = 30.347$

...4.4.6

And since we have from equation 4.4.2a => $S_3 = \frac{30.347}{2}$ ...4.4.6a

Since we are to design on low power still maintaining maximum ICMR we get as follows

$v_{ic}(\min) = v_{ss} + v_{tn}(\max) + v_{on1} + v_{onn4}$ ...4.4.7

Let's assume in a generic sense that as we have $v_{ic}(\min) < -1.25V$

To achieve this we have from the above equation

$v_{on5/6} = 0.26V$ $\Rightarrow S_1 = 14.029$

From the above equation we get

$g_m = 230\frac{\mu A}{V}$

Now to design for the resistances used i.e. R_{67} (used between the nodes 6 and 7) we have, biased the folded cascade stage such as M_{15} is operating at the verge of saturation.

=> $v_{on15} = v_{sd15} = 0.25V$ ...4.4.8

also we want $v_{sg14} = |V_{tp}| + v_{on14}$ ...4.4.9

from equations 4.4.8 and .4.4.9, we get

$v_{on15} = IR_{67}$ => $R_{67} = \frac{v_{on15}}{I_{15}}$ = 8.33K

By assuming the symmetric bias points i.e $v_{on9} = v_{on8} = v_{on7} = v_{on2} = 0.25V$ we get

$R_{78} = \frac{v_{on2}}{I_2}$, R_{78} denoting the resistance between the nodes 7 and 8, further we use equation 4.4.2a to get $R_{78} = 16.66667K$ ...4.4.10

To calculate the ICMR we proceed as

$v_{ic}(\max) = V_{dd} - v_{on12/14} - |V_{tp}|(\max) + V_{tn}(\min)$ ...4.4.11

= $1.5V - 0.25V - 0.642V + 0.7V$ =1.308V

$v_{ic}(\min) = V_{ss} + v_{on5/6} + +V_{tn}(\max) + v_{on4}$ ...4.4.12

= -1.5V + 0.26V + 0.75V +0.25V

= -0.24V

$P_d = 170 \times 3\mu W = 510\mu W$ ...4.4.13

4.5 DESIGN OF THE PARALLEL INPUT CONSTANT TRANSCONDUCTANCE STAGE

Let us design the folded cascode output stage parallel input constant transconductance amplifier. For the analysis we refer to the figure3.2. To start with let us design the parallel transconductance input stage for the n. Stage diff. Amp, we have (refer for Theory -chapter3)

$$V_n^- = V_{ss} + V_{tn} \quad \ldots 4.5.1$$

Now at the saturation, we have $V_{GD\_MBN} = V_{tn}$

$$V_{G\_MBN} - V_{D\_MBN} = V_{tn} \quad \ldots 4.5.2$$

as $I_{sn\,(O)}$ saturation current is flowing

$$V_{GS\_1n} = V_{tn} + V_{on1n} \quad \ldots 4.5.3$$

$$V_{s\_1n} = V_{D\_MBN} \quad \ldots 4.5.4$$

So we have

$$V_{G\_MBN} - V_{tn} = V_{D\_MBN} = V_{s\_1n} \quad \ldots 4.5.5$$

From equation 4.5.3 we have

$$V_{G\_1n} - V_{tn} - V_{on1n} = V_{s\_1n}, \quad \ldots 4.5.6$$

Putting this value in equation 4.5.5 we have

$$V_{G\_In} - V_{tn} - V_{on1n} = V_{G\_MBN} - V_{tn}$$

$$V_{G\_In} = V_{G\_MBN} + V_{on1n} \quad \ldots 4.5.7$$

But at the threshold $V_{G1N} = V_{n+}$

$$V_n^+ = V_{G\_MBN} + V_{on1}$$

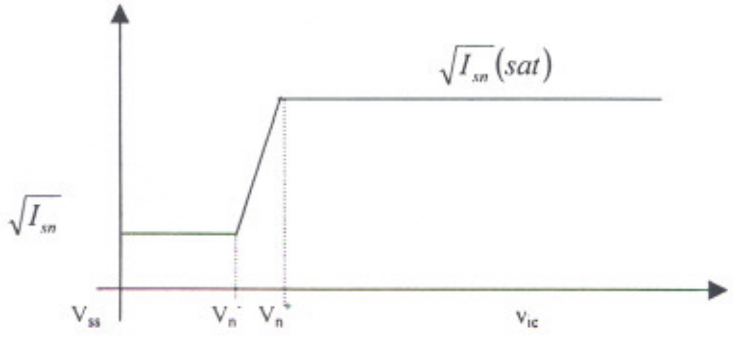


Figure 4.4: $\sqrt{I_{sn}}$ Vs common mode voltage for the n-type differential stage

Now to maximize the ICMR operation of the n- pair (type) we have

$$Vic\ (min) = V_{ss} + V_{on1n} + V_{onBn} + V_{tn}\ (max)$$

$$vic\ (min) = < V_{ss} + V_{tn} > + V_{onn} + V_{onBn}$$

In order to have vic (min) as small as small as possible, let us have $V_{onn} + V_{onbn}$ to be as small as possible. Now to look at the p-type differential pair,

$$V_p^+ = V_{dd} - |V_{tp}| \qquad \ldots 4.5.8$$

To find the start of the linear region, we have

$$V_{DG\_MBP} = |V_{tp}| \qquad \ldots 4.5.9$$

White still at threshold of saturation 0.5 $I_{sp(0)}$ flow through all transistors of the p pair

$$V_{SG\_P} = |V_{tp}| + V_{onp}$$

$$V_{s\_p} = |V_{tp}| + V_{onp} + V_{G\_p} \qquad \ldots 4.5.10$$

From equation 4.5.9 we have

$$V_{D\_MBP} - V_{G\_MBP} = |V_{tp}|$$

$$V_{D\_MBP} = V_{G\_MBP} + |V_{tp}| \qquad \ldots 4.5.11$$

We know

$$V_{DmBP} = V_{sp} \qquad \ldots 4.5.12$$

$$V_{GMBP} + |V_{tp}| = |V_{tp}| + V_{onp} + V_{Gp} \qquad \ldots 4.5.13$$

$V_{GP} = V_{GMBP} - V_{onp}$, which on the point of threshold reduces to

$$V_p^- = V_{GMBP} - V_{onp} \qquad \ldots 4.5.14$$

And similar remarks apply to the ICMR range of p pair of tx (transistors)

Let $\triangle V_n = V_{on1n} + V_{onBN} \qquad \ldots 4.5.15$

$$\triangle V_p = V_{onp} + V_{onBP} \qquad \ldots 4.5.16$$

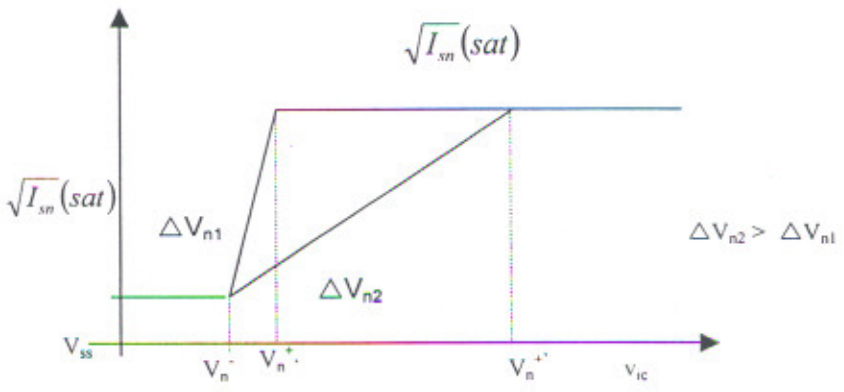


Figure.4.5 $\sqrt{I_{sn}}$ Vs V_{ic} For The N-Type Pair

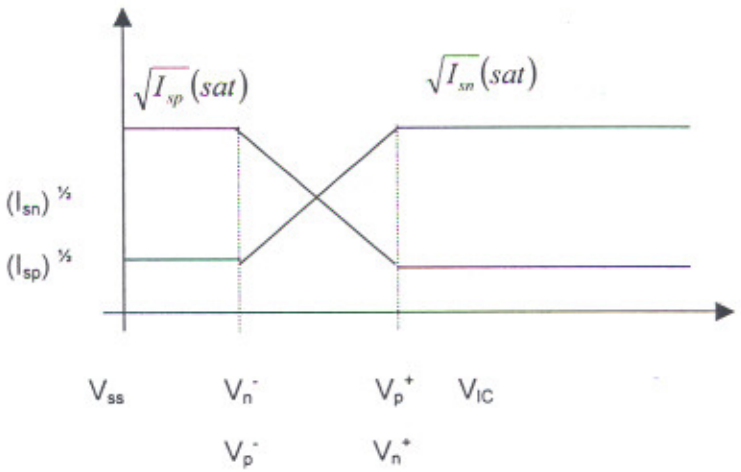


Figure 4.6: $(I_{sn})^{1/2}$, $(I_{sp})^{1/2}$ Vs common mode voltage for the complementary differential pair

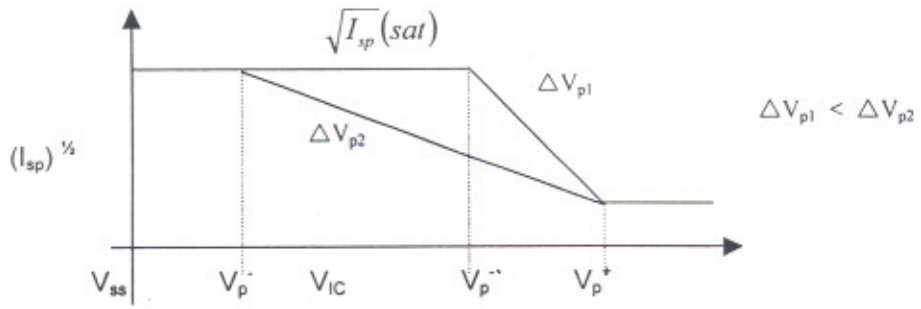


Figure 4.7: $(I_{sn})^{1/2}$ Vs common mode voltage for the p-type differential stage

now to make $V_n^- = V_p^-$,we have

$$V_{ss} + V_{tn} = V_{G\_NBP} + V_{onp} \qquad \ldots 4.5.17$$

$$V_{ss} + V_{tn} = V_{dd} - |V_{tp}| - V_{onBP} + V_{onp}$$

$$V_{dd} - V_{ss} - V_{tn} - |V_{tp}| = V_{onBP} + V_{onp} \qquad \ldots 4.5.18$$

$$V_{dd} - V_{ss} - V_{tn} - |V_{tp}| = \Delta V_p = V_{onBP} + V_{onp}$$

$$(V_{dd} - V_{ss} - V_{tn} - |V_{tp}| - v_{onBP})^2 = \frac{I_{sp(0)}}{k_p \times S_p} \qquad \ldots 4.5.19$$

$$S_p = \frac{I_{sp(0)}}{k_p \times (V_{dd} - V_{ss} - V_{tn} - |V_{tp}| - v_{onBP})^2}$$

Designing on $\pm$ 2.5 V power supply, so let's assume

$V_{onBp} \leq 0.25$ V

Let's say $V_{onBp} = 0.2$ V and $I_{sn(o)} = I_{sp(o)} = I_{sn(o)} = 50\ \mu A$, to this account we have

$S_{BP} = 100$

$$S_p = \frac{50}{25 \times (5 - 0.74 - 0.64 - 0.2)^2} \qquad \ldots 4.5.20$$

$$S_p = 0.17099.$$

In our design as explained earlier, we have

$$g_m = \sqrt{2\beta_n I_n} + \sqrt{2\beta_p I_p} = \text{Constant} \qquad \ldots 4.5.21$$

if we assume $\beta_{1n} = \beta_{1P}$, then we just have to overlap the 2 transition regions in order to have a constant gm transconductance. To this effect we have $S_n = 0.712$, which in terms of (W/L)'s and resistance capacitances is not a very good design. This design is very sensitive to noise and the perfect matching of the transistors is impossible. Considering this a low-voltage ($\pm$ 1.5 V) low-power design is presented below.

$I_{sn(o)} = I_{sp(o)} = 50\ \mu A$

$P_d = (100 \times 3)\ \mu W = 0.3 mW$

$v_{onBp} = v_{onBn} = 0.2V$ to have a symmetric design

$S_{Bp} = 100$

S_{Bn} = 41.667

To overlap the linear regions of I_{sn} & I_{sp}, we have

$$S_p = \frac{50}{25 \times (3 - 0.64 - 0.74 - 0.2)^2}$$

S_P = 0.9918

S_N = 0.4132

which is still not a reasonable range, let's have

V_{onBn} = 0.25V

S_{Bp} = 64

S_P = 1.0656

S_n = 0.443

So the linear region must have a minimum width to have feasible sizes and resistances and capacitances.

$V_{onBn} \geq$ 0.3V

V_{onBn} = 0.5 V = V_{onBp}

S_{Bn} = 6.667

$$S_p = \frac{50}{25 \times (3 - 0.64 - 0.74 - 0.2)^2} = \frac{2}{1.2544}$$

S_P = 1.59438 => V_{onn} = 1.12 V

S_n = 0.664 assuming $\beta_{1n} = \beta_{1p}$

Maximizing the linear range to this accord we design a stage with a dc-shift (level). Unfortunately, the small aspect ratios of the differential pairs degrade the noise performance and cause the circuit to be more sensitive to the mismatch between the pair transistors.

4.6 A DESIGN APPROACH OF AN OP-AMP WITH LEVEL SHIFTERS IN THE COMPLIMENTARY INPUT STAGE

Design of the folded cascode parallel transconductance constant g_m operational amplifier for low voltage low power applications has been presented below. For a Generic analysis figure 3.3 is referred.

To make sure that v_{out} has the maximum range it is supposed that

$V_{on24/28/27/23} < V_{on}$(minimum)

So that

$V_{on\,27} + V_{on28} < V_{on1}$ ...4.6.1

$V_{on\,25} + V_{on26} < V_{on2}$ ...4.6.2

Assuming the same parameters for the analysis, it is proposed assuming that we have ± 1.5 V power supply. Let us say $V_{on24} < 0.25V$ (a modestly low value).

Now to have minimum power dissipation We have $I_{24} = I_{28} = 60\mu A$ and $I_{sn(0)} = I_{sp(0)} = 30\ \mu A$. So that in saturation of either extreme of the ICMR we have either the n-pair/ p-pair supplying 15μA to each leg of folded- cascode implying

$V_{on23} < 0.25\ V$

and $I_3 = 45\ \mu A = I_7$

Now taking an appropriate value of $von_{24/28}$ and not very different from $Von_{23/27}$ we can find (W/L)'s of the n-type transistors in the folded cascode o/p stage as:

$$S = \frac{2 \times I}{k_n \times v_{on2}^2} \quad \text{...4.6.3}$$

Now to aspect ratio's for the p-type folded cascode be have for the self biased configuration as

$V_{SG\_2} = V_{SD\_21} + V_{SD\_22}$ ...4.6.4

$V_{SG\_21} = |V_{tp}| + V_{on1}$ (say) ...4.6.5

Where V_{on1} corresponds to M_{21}

And $V_{s22} = |V_{tp}| + V_{on2}$, where V_{on2} corresponds to M_{22}

Now to have constraints on the various parameters, we have M21 should be in saturation

$V_{SD\_21} > V_{SG\_21} - |V_{tp}|$ ...4.6.6

$V_{SG\_21} - V_{SD\_22} > V_{SG21} - |V_{tp}|$ ...4.6.7

$V_{SD\_22} < |V_{tp}|$ ...4.6.8

$V_{d22} < |V_{tp}|$ for M_{22} to be in saturation

$V_{SG\_21} = |V_{tp}| + V_{on1}$ ...4.6.9

$V_{S\_21} - V_{G\_21} = |V_{tp}| + V_{on}$, we know $V_{S\_21} = V_{dd}$

$V_{G\_21} = V_{D\_22}$

$$V_{dd} - |V_{tp}| - V_{on1} = V_{G21} = V_{d22}$$

$$V_{dd} - V_{tp} - V_{on} < |V_{tp}|$$

$$V_{on1} > V_{dd} - 2|V_{tp}| \qquad \ldots 4.6.10$$

Now Similarly for M21

$$V_{D\_21} = V_{S\_21} = |V_{tp}| + V_{on2}$$

$$|V_{tp}| + V_{on2} - (V_{dd} - |V_{tp}| - V_{on1}) < |V_{tp}|$$

$$V_{on2} + V_{on1} < V_{dd} - |V_{tp}|$$

and from 4.6.9 we also have

$$V_{SD\_21} + V_{SD\_22} = |V_{tp}| + V_{on1}$$

Now, using the theoretical values of the parameters

$$V_{SD\_22} < 0.64V$$

$$V_{on1} > 1.5 - 2 \,.\, (0.64) = 0.22V$$

$$V_{on1} + V_{on2} < 0.86V$$

$$V_{SD\_21} + V_{SD\_22} = 0.64 + V_{on1}$$

$$V_{SD\_22} > V_{on2}$$

$$V_{S\_22} = 0.64 + V_{on2}$$

$$V_{SD\_21} > V_{on1}$$

$$V_{D\_22} = V_{dd} + |V_{tp}| - V_{on1}$$

It is assumed $V_{SD22} = P$ (say some constant), while $P < 0.64$

$$V_{S\_22} - V_{D\_22} = P$$

$$|V_{tp}| + V_{on2} - (V_{dd} - |V_{tp}| - V_{on1}) = P$$

$$2 \,.|V_{tp}| + V_{on2} + V_{on1} - V_{dd} = P$$

$$V_{on1} + V_{on2} = V_{dd} + P - 2. |V_{tp}|$$

Now $V_{dd} + P - 2. |V_{tp}| < 0.86V$ from 4.6.6 and 4.6.8

$$V_{dd} - 2.|V_{tp}| + p < V_{dd} - |V_{tp}| - |V_{tp}| + P < 0$$

=> $P < |V_{tp}|$, which has been already taken account for.

$$V_{SD\_22} = 0.5V < 0.64\ V$$

$$V_{on1} + V_{on2} = 0.72V$$

Now let's say we assume V_{on1} = 0.25V yielding us,

V_{on2} = 0.47V

$V_{SD\_21} + V_{SD\_22}$ = 0.89V

V_{SD_21} = 0.89 V- V_{sd22} = 0.39V

And we have for the same current following:

$S_{22} . V_{on2}^2 = 2I_{22}/K_n$ ...4.6.11

$S_{21} . V_{on1}^2 = 2I_{21}/K_n$ ...4.6.12

From 4.6.11 and 4.6.12 we have $V_{on1}^2 . S_{21} = 3.6 = V_{on2}^2 . S_{22}$

$S_{21} = 3.6/V_{on1}^2$ => $S_{21} = 57.6$

$S_{22} = 16.3969$

Now, having biased the folded cascode pair, let us bias the differential pair stage: To make it happen it is assumed

$V_{on24} = V_{on23} = 0.25V$

$I_{23} = 45\mu A$

$I_{24} = 60\mu A$

$S_{24}=32$

$S_{23}=24$

To have I_{BN} (sat) = 30 μA, we have

$S_{NB} = S_{BI} = 16$

Where V_{onBN} = 0.25V

Similarly V_{onBP} =0.25 V => S_{Bp} =38.4

Now assuming $V_{on3} = V_{on4} = V_{on5} = V_{on6} = V_{onSB11}$ = 0.25V

For a symmetric design, we have $S_{B11} = S_3 = S_4 = S_5 = S_6 = 38.4$

To this effect, parallel differential stage is biased to have a good G.B. and fairly good amplification. g_{mn} is assumed to be a modestly good value

So that $S_{1n} = \frac{g_{mn}^2}{2 \times k_n \times I_{1n}}$ ...4.6.13

As, already assumed , we have $\beta_{1n} = \beta_{1p}$ => $S_{1p} = (k_n / k_p) . S_{1n}$

p_1 And from here we get $V_{onn} = V_{onp}$

$g_{mn} = g_{mp}$

To have a symmetric design. Looking for the level-shifter for the above bias point we have

$$V_p^- = V_{G\_mBp} - V_{onp} \qquad \ldots 4.6.14$$

$$V_p^- = \langle V_{dd} - |V_{tp}| \rangle - V_{onBp} - V_{onp}$$

$$V_n^- = V_{ss} - V_{tn} \text{ (almost fixed)} = 0.75 \text{ V} \qquad \ldots 4.6.15$$

Hence to overlap both linear regions, we have

$$V_p^- = V_n^- + \Delta V_{shift} \qquad \ldots 4.6.16$$

$$\Delta V_{shift} = \langle V_{dd} - |V_{tp}| - V_{ss} \rangle - V_{onBp} - V_{onp} \qquad \ldots 4.6.17$$

We should have the much shift on source follower configuration of M_{32} and M_{s4}. We have to do various simulations for the optimal shift ΔV_{shift} (optimal) due the variations in the parameters of our simulation.

To have bias the $M_{s2/s1}$, we have

$$I_{S2} = \frac{\beta_{S2} \bullet \left(\Delta V_{shift} - |V_{tp}|\right)^2}{2} \qquad \ldots 4.6.18$$

$$\Rightarrow \quad S_{s2} = \frac{2 \times I_{s2}}{k_p \times \left(\Delta V_{shift} - |V_{tp}|\right)^2} \quad \text{assuming } I_{s2} = I_{BN} \text{ (sat)} = 30\ \mu A$$

Here is an example:

$g_{mn} = g_{mp} = 200 \mu A/V$

$S_{1n} = 22.22$

Let $S_{1n} = 23$, an integral value $\Rightarrow g_{mn} = 203.469\ \mu A/V$

$V_{onn} = 0.14744 = V_{onp}$

Now to Calculate $V_{p-} = 0.46256V$

$V_n^- = -0.75V$

$\Delta V_{shift} = 1.21256V$

By taking various values around it and simulating them we have S_{s2} more accurate

$$S_{s2} = \frac{2 \times 30}{25 \times (1.21256 - 0.64)^2} = 0\ 7.32098$$

Now since we have biased all transistors from the bias circuitry. We have

$$R_{B11} = \frac{V_{dd} - V_{ss} - |V_{tp}| - v_{onBP}}{I_{s11}} \quad \ldots 4.6.19$$

$$R_{B1} = \frac{V_{dd} - V_{ss} - |V_{tp}| - v_{onB1}}{I_{sB1}} \quad \ldots 4.6.20$$

Putting the above values of the parameters of the signals into the above equations we have

$R_{B11} = 70.33K$

$R_{B1} = 66.67K$

To finally Evaluate the power we have $P_d = 3.(30.6 + 60.2)\ \mu W = 900\ \mu W$

SIMULATION RESULTS

In this chapter we illustrate the simulations carried out following the design procedures given in the previous chapter.

5.1 Conventional two stage amplifier

Parameters	Under ±2.5V supply (As designed by the procedure given in [1])	Under ±2.5V supply (As designed by the procedure given in section 4.3)	Under ±1.5V supply (As designed by the procedure given in section 4.3)
A_v	55.6dB	35dB	28.3dB
p_1	10KHz	30KHz	100KHz
p_2	10MHz	10.3MHz	13MHz
z_1	5000MHz	2000MHz	1100MHz
Gain Bandwidth	5MHz	2MHz	1.2MHz
$v_{ic}(\max)$	1.951V	2.37V	1.458
$v_{ic}(\min)$	-1.06V	-0.9V	0.1V
P_d	500µW	500µW	300µW

Table: 5.1

Initially the Op-Amp was designed using the approach illustrated in [1]. It was designed to operate under ±2.5V supply The conventional two stage amplifier has been illustrated in figure 5.1, with its spice netlist containing all the aspect ratios of the transistors is enlisted on page 63. The Bode plot is given at page67 .The output files (T-spice netlist) can be witnessed on pages 64-66.

The amplifier was then designed to operate under ±2.5V supply by following the design procedure as given in section 4.3, we optimized on the following values. The

spice netlist along with the simulation results can be seen on 69. Various aspect ratios of the transistors have been given in the T-spice file on 68.:

Next we design on ±1.5 V power supply by following the same design procedure as given in section 4.3. The output simulation plot (Bode plot) can be seen on page70.

A comparison of the results of the both the designs can be witnessed in Table 5.1.

5.2 Folded Cascode Amplifier

The folded cascode amplifier (refer figure 5.2) was designed using the design procedure as given in section 4.4. The spice netlist and the simulation results are given on page 73and 74 respectively.

The design under ±1.5 V power supply by following the same design procedure as given in section 4.4. The output simulation plot (Bode plot) can be seen on page 74.

Parameters	Under ±1.5V supply
A_v	50.25dB
p_1	7.9KHz
p_2	100MHz
z_1	1780MHZ
$v_{ic}(\max)$	1.308V
$v_{ic}(\min)$	-0.24V
Gain Bandwidth(GB)	1.2MHz
P_d	510μA

Table: 5.2

5.3 Parallel Transconductance Stage

The figure 5.3 can be referred on page 75. The amplifier has been designed as given in section 4.4. We can view the spice netlist and the output files on page76 and 77-78 respectively. It is first biased for the low Power, low Voltage constraints to find the operating regions of the complimentary Transistor pairs. After designing the Aspect Ratio's for the n-pair we then design the Aspect Ratio for the p-pair so that we overlap the linear regions of $\sqrt{I_{sp}}$ and $\sqrt{I_{sn}}$ to make sure that we have a constant Transconductance(g_m). Here's attached a simulation result of overlapped Parabolic regions of the currents in the respective pairs on page 79. Various aspect ratios of the transistors have been given in the T-spice file on page 76.

5.4. Constant Transconductance, Input Complimentary Differential Pair with DC level Shifters Operational Amplifier

We first design the self bias Folded cascode Stage to save on our Bias circuitry, and then design the n-pair (Aspect ratio calculation) refer to figure 5.4 on page 80.After calculating the critical points of the $\sqrt{I_{sn}}$ and $\sqrt{I_{sp}}$ curves, the design of the DC level shift stage has been presented. After we calculate the Δv_{shift} , the aspect ratio for the level shift stage was calculated. A simulation for various values for the Δv_{shift} to obtain the optimal shift as I have designed with the Theoretical parameters and not accounting for the variations in the various process parameters and the variations in the threshold values. I have tried to simulate for two different values of the current division. Finally I summarize my results in the Graphs displayed in the end. Various aspect ratios of the transistors for the first design and the second design keeping different values of the currents have been given in the T-spice files on page 81 and 102 respectively.

a. Graph displaying v_{ic}(common mode voltages) Vs Amplification(Gain) of this Op-Amp on page 101.

b. Graph displaying the variations of the Transconductance with the $\Delta v_{shift}$for the two different values of the currents can be seen on pages 93-101 and 104 -112 respectively.

The simulations for two values of the currents have been carried out and the results can be seen on page 93-112 . The Power dissipation values are as follows:

Case 1 refer section 4.5

$I_{total} = I_4 + I_5 + I_2 + I_9 + I_{11} + I_{22} + I_{19} + I_{10}$

$= 2I_4 + I_9 + I_{22} + 2I_2 + 2I_{10}$

$= 2(60\mu A) + 2(30\mu A) + 2(30\mu A) + 2(30\mu A)$

$= 300\mu A$

$P_d = 3(300\mu A) = 900\mu W$

Case 2 refer section 4.5

$I_{total} = I_4 + I_5 + I_2 + I_9 + I_{11} + I_{22} + I_{19} + I_{10}$

$= 2I_4 + I_9 + I_{22} + 2I_2 + 2I_{10}$

$= 2(30\mu A) + 2(30\mu A) + 2(30\mu A) + 2(30\mu A)$

$= 240\mu A$

$P_d = 3(240\mu A) = 720\mu W$

```
**********************************************************
*
* MCNC 1.25um CMOS Process
* Nominal Level 2 MOSFET Parameters
* 2/26/87
*
**********************************************************

.model nmos nmos
+    Level=2            Ld=0.0u          Tox=225.00E-10
+    Nsub=1.066E+16     Vto=0.622490     Kp=6.326640E-05
+    Gamma=.639243      Phi=0.31         Uo=1215.74
+    Uexp=4.612355E-2   Ucrit=174667     Delta=0.0
+    Vmax=177269        Xj=.9u           Lambda=0.0
+    Nfs=4.55168E+12    Neff=4.68830     Nss=3.00E+10
+    Tpg=1.000          Rsh=60           Cgso=2.89E-10
+    Cgdo=2.89E-10      Cj=3.27E-04      Mj=1.067
+    Cjsw=1.74E-10      Mjsw=0.195

.model pmos pmos
+    Level=2            Ld=.03000u       Tox=225.000E-10
+    Nsub=6.575441E+16  Vto=-0.63025     Kp=2.635440E-05
+    Gamma=0.618101     Phi=.541111      Uo=361.941
+    Uexp=8.886957E-02  Ucrit=637449     Delta=0.0
+    Vmax=63253.3       Xj=0.112799u     Lambda=0.0
+    Nfs=1.668437E+11   Neff=0.64354     Nss=3.00E+10
+    Tpg=-1.00          Rsh=150          Cgso=3.35E-10
+    Cgdo=3.35E-10      Cj=4.75E-04      Mj=.341
+    Cjsw=2.23E-10      Mjsw=0.307
```

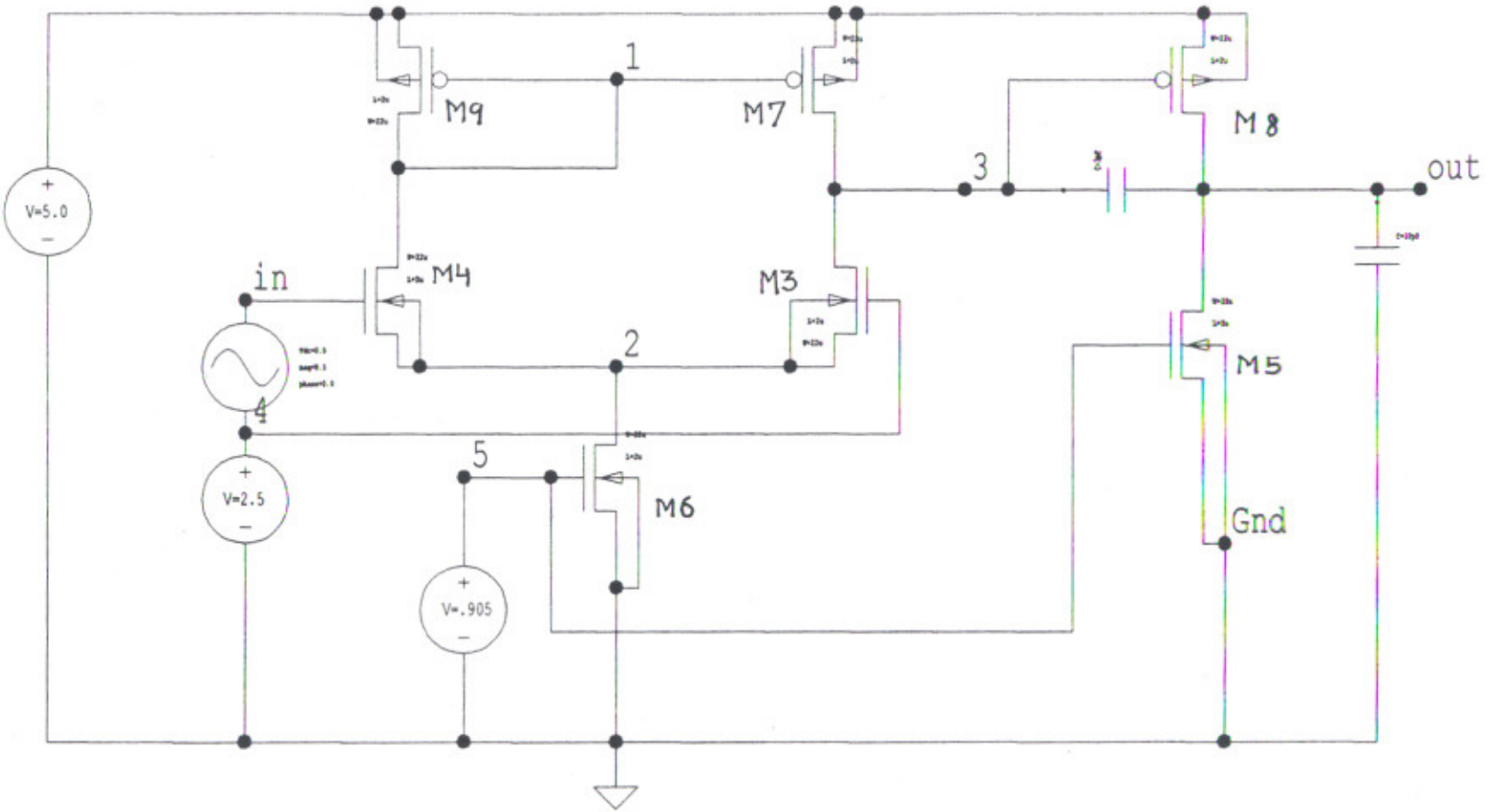


FIG: 5.1. CONVENTIONAL TWO STAGE OP-AMP

```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 4, 2002 at 23:40:09

* Waveform probing commands
.probe
.options probefilename="simdif2.5.dat"
+ probesdbfile="C:\sush\simdif2.5.sdb"
+ probetopmodule="simdif2.5"

* Main circuit: simdif2.5
C1 out Gnd 10pF
C2 3 out 3pF
M3 3 4 2 2 NMOS L=2u W=20u AD=66p PD=24u AS=66p PS=24u
M4 1 in 2 2 NMOS L=2u W=20u AD=66p PD=24u AS=66p PS=24u
M5 out 5 Gnd Gnd NMOS L=2u W=550u AD=66p PD=24u AS=66p PS=24u
M6 2 5 Gnd Gnd NMOS L=2u W=74u AD=66p PD=24u AS=66p PS=24u
M7 3 1 N3 N3 PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
M8 out 3 N3 N3 PMOS L=2u W=373u AD=66p PD=24u AS=66p PS=24u
M9 1 1 N3 N3 PMOS L=2u W=22u AD=66p PD=24u AS=66p PS=24u
v10 in 4 0.0 AC 0.5 0.0
v11 N3 Gnd 5.0
v12 4 Gnd 2
v13 5 Gnd .925
.include "C:\Program Files\Tanner EDA\T-Spice Pro v6.02\models\ml2_125.md"
.op
.ac dec 10 10 20000MEG
.print ac vdb(out)
.print ac vp(out)
*.dc lin v12 0 5 0.5
*.print dc v(out)

* End of main circuit: simdif2.5
```

```
* T-Spice 6.02 Simulation  Tue Mar 04 04:07:03 2003   C:\sush\simdif2.5.sp  (CAZM)
* Command line: tspice -o C:\sush\simdif2.5.out C:\sush\simdif2.5.sp
* T-Spice Win32 6.02.20000302.11:47:10
* Operating System: Windows NT/95

*SEDIT: probesdbfile="C:\sush\simdif2.5.sdb"
*SEDIT: probetopmodule="simdif2.5"
*SEDIT: Alter blocks = 0

* Device and node counts:
*              MOSFETs - 7                  MOSFET geometries - 5
*                 BJTs - 0                              JFETs - 0
*              MESFETs - 0                           Diodes - 0
*            Capacitors - 2                       Resistors - 0
*             Inductors - 0                 Mutual inductors - 0
*  Transmission lines - 0        Coupled transmission lines - 0
*     Voltage sources - 4                  Current sources - 0
*                VCVS - 0                             VCCS - 0
*                CCVS - 0                             CCCS - 0
*    V-control switch - 0                 I-control switch - 0
*       Macro devices - 0        Functional model instances - 0
*         Subcircuits - 0              Subcircuit instances - 0
*   Independent nodes - 4                   Boundary nodes - 5
*         Total nodes - 9


*SEDIT: Alter=0
*SEDIT: Analysis types DCOP 1 ACMODEL 1 AC 1 TRANSIENT 0 TRANSFER 0 NOISE 0

* BEGIN NON-GRAPHICAL DATA

DC ANALYSIS
v(2) =    9.8126e-001
v(3) =    3.7292e+000
v(out) =    3.0371e+000
v(1) =    3.7292e+000
v(5) =    9.2500e-001
v(4) =    2.0000e+000
v(N3) =    5.0000e+000
v(in) =    2.0000e+000
i(v10) =    0.0000e+000
i(v11) =   -1.0227e-003
i(v12) =    0.0000e+000
i(v13) =    0.0000e+000

* END NON-GRAPHICAL DATA

* BEGIN NON-GRAPHICAL DATA

AC SMALL-SIGNAL MODELS
```

	M3	M4	M5	M6	M7
MODEL	nmos	nmos	nmos	nmos	pmos
TYPE	NMOS	NMOS	NMOS	NMOS	PMOS
ID	5.21e-005	5.21e-005	9.18e-004	1.04e-004	-5.21e-005
VGS	1.02e+000	1.02e+000	9.25e-001	9.25e-001	-1.27e+000
VDS	2.75e+000	2.75e+000	3.04e+000	9.81e-001	-1.27e+000
VBS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
VTH	7.24e-001	7.24e-001	7.23e-001	7.38e-001	-6.47e-001
VDSAT	3.07e-001	3.07e-001	2.46e-001	2.33e-001	4.61e-001
RS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
RD	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
GM	2.26e-004	2.26e-004	5.08e-003	5.99e-004	1.50e-004
GDS	3.15e-006	3.15e-006	5.83e-005	1.20e-005	3.32e-006

GMB	0.00e+000	0.00e+000	0.00e+000	0.00e+000	3.72e-005
GBD	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
GBS	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
CGS	5.36e-014	5.36e-014	1.48e-012	1.99e-013	5.17e-014
CGD	5.78e-015	5.78e-015	1.59e-013	2.14e-014	7.37e-015
CGB	0.00e+000	0.00e+000	0.00e+000	0.00e+000	5.28e-015
CBD	7.97e-015	7.97e-015	6.62e-015	1.40e-014	2.58e-014
CBS	1.69e-014	1.69e-014	-1.85e-013	-3.84e-015	4.91e-014

	M8	M9
MODEL	pmos	pmos
TYPE	PMOS	PMOS
ID	-9.18e-004	-5.21e-005
VGS	-1.27e+000	-1.27e+000
VDS	-1.96e+000	-1.27e+000
VBS	0.00e+000	0.00e+000
VTH	-6.45e-001	-6.47e-001
VDSAT	4.62e-001	4.61e-001
RS	0.00e+000	0.00e+000
RD	0.00e+000	0.00e+000
GM	2.65e-003	1.50e-004
GDS	4.49e-005	3.32e-006
GMB	6.53e-004	3.72e-005
GBD	1.00e-014	1.00e-014
GBS	1.00e-014	1.00e-014
CGS	8.77e-013	5.17e-014
CGD	1.25e-013	7.37e-015
CGB	8.96e-014	5.28e-015
CBD	2.58e-014	2.58e-014
CBS	2.59e-013	4.91e-014

* END NON-GRAPHICAL DATA

*WEDIT: .ac DEC 10 1.000000000000e+001 2.000000000000e+010
AC ANALYSIS

Frequency<Hz>	vdb(out)<dB>	vp(out)<deg>
1.00000e+001	5.2936e+001	1.7995e+002
1.25893e+001	5.2936e+001	1.7994e+002
1.58489e+001	5.2936e+001	1.7992e+002
1.99526e+001	5.2936e+001	1.7990e+002
2.51189e+001	5.2936e+001	1.7988e+002
3.16228e+001	5.2936e+001	1.7985e+002
3.98107e+001	5.2936e+001	1.7981e+002
5.01187e+001	5.2936e+001	1.7976e+002
6.30957e+001	5.2936e+001	1.7970e+002
7.94328e+001	5.2936e+001	1.7962e+002
1.00000e+002	5.2936e+001	1.7952e+002
1.25893e+002	5.2936e+001	1.7940e+002
1.58489e+002	5.2936e+001	1.7924e+002
1.99526e+002	5.2935e+001	1.7905e+002
2.51189e+002	5.2934e+001	1.7880e+002
3.16228e+002	5.2933e+001	1.7849e+002
3.98107e+002	5.2932e+001	1.7810e+002
5.01187e+002	5.2929e+001	1.7760e+002
6.30957e+002	5.2924e+001	1.7698e+002
7.94328e+002	5.2917e+001	1.7621e+002
1.00000e+003	5.2906e+001	1.7523e+002
1.25893e+003	5.2889e+001	1.7400e+002
1.58489e+003	5.2861e+001	1.7246e+002
1.99526e+003	5.2818e+001	1.7054e+002
2.51189e+003	5.2750e+001	1.6816e+002
3.16228e+003	5.2644e+001	1.6521e+002
3.98107e+003	5.2482e+001	1.6162e+002

5.01187e+003	5.2236e+001	1.5729e+002
6.30957e+003	5.1874e+001	1.5222e+002
7.94328e+003	5.1355e+001	1.4645e+002
1.00000e+004	5.0642e+001	1.4013e+002
1.25893e+004	4.9707e+001	1.3356e+002
1.58489e+004	4.8545e+001	1.2706e+002
1.99526e+004	4.7171e+001	1.2094e+002
2.51189e+004	4.5618e+001	1.1544e+002
3.16228e+004	4.3926e+001	1.1068e+002
3.98107e+004	4.2132e+001	1.0665e+002
5.01187e+004	4.0268e+001	1.0332e+002
6.30957e+004	3.8355e+001	1.0060e+002
7.94328e+004	3.6411e+001	9.8380e+001
1.00000e+005	3.4447e+001	9.6582e+001
1.25893e+005	3.2470e+001	9.5121e+001
1.58489e+005	3.0484e+001	9.3925e+001
1.99526e+005	2.8493e+001	9.2935e+001
2.51189e+005	2.6499e+001	9.2099e+001
3.16228e+005	2.4503e+001	9.1374e+001
3.98107e+005	2.2505e+001	9.0721e+001
5.01187e+005	2.0506e+001	9.0107e+001
6.30957e+005	1.8506e+001	8.9498e+001
7.94328e+005	1.6506e+001	8.8863e+001
1.00000e+006	1.4504e+001	8.8167e+001
1.25893e+006	1.2502e+001	8.7374e+001
1.58489e+006	1.0498e+001	8.6442e+001
1.99526e+006	8.4923e+000	8.5321e+001
2.51189e+006	6.4826e+000	8.3953e+001
3.16228e+006	4.4671e+000	8.2268e+001
3.98107e+006	2.4427e+000	8.0179e+001
5.01187e+006	4.0435e-001	7.7585e+001
6.30957e+006	-1.6557e+000	7.4362e+001
7.94328e+006	-3.7492e+000	7.0373e+001
1.00000e+007	-5.8929e+000	6.5462e+001
1.25893e+007	-8.1106e+000	5.9479e+001
1.58489e+007	-1.0433e+001	5.2292e+001
1.99526e+007	-1.2895e+001	4.3830e+001
2.51189e+007	-1.5531e+001	3.4106e+001
3.16228e+007	-1.8363e+001	2.3232e+001
3.98107e+007	-2.1391e+001	1.1385e+001
5.01187e+007	-2.4589e+001	-1.2482e+000
6.30957e+007	-2.7910e+001	-1.4508e+001
7.94328e+007	-3.1295e+001	-2.8246e+001
1.00000e+008	-3.4695e+001	-4.2266e+001
1.25893e+008	-3.8073e+001	-5.6256e+001
1.58489e+008	-4.1416e+001	-6.9799e+001
1.99526e+008	-4.4724e+001	-8.2455e+001
2.51189e+008	-4.8007e+001	-9.3891e+001
3.16228e+008	-5.1283e+001	-1.0397e+002
3.98107e+008	-5.4578e+001	-1.1273e+002
5.01187e+008	-5.7929e+001	-1.2024e+002
6.30957e+008	-6.1383e+001	-1.2652e+002
7.94328e+008	-6.4977e+001	-1.3143e+002
1.00000e+009	-6.8738e+001	-1.3468e+002
1.25893e+009	-7.2683e+001	-1.3586e+002
1.58489e+009	-7.6826e+001	-1.3433e+002
1.99526e+009	-8.1165e+001	-1.2886e+002
2.51189e+009	-8.5581e+001	-1.1722e+002
3.16228e+009	-8.9481e+001	-9.6501e+001
3.98107e+009	-9.1616e+001	-6.9200e+001
5.01187e+009	-9.1823e+001	-4.6197e+001
6.30957e+009	-9.1332e+001	-3.1552e+001
7.94328e+009	-9.0834e+001	-2.2562e+001

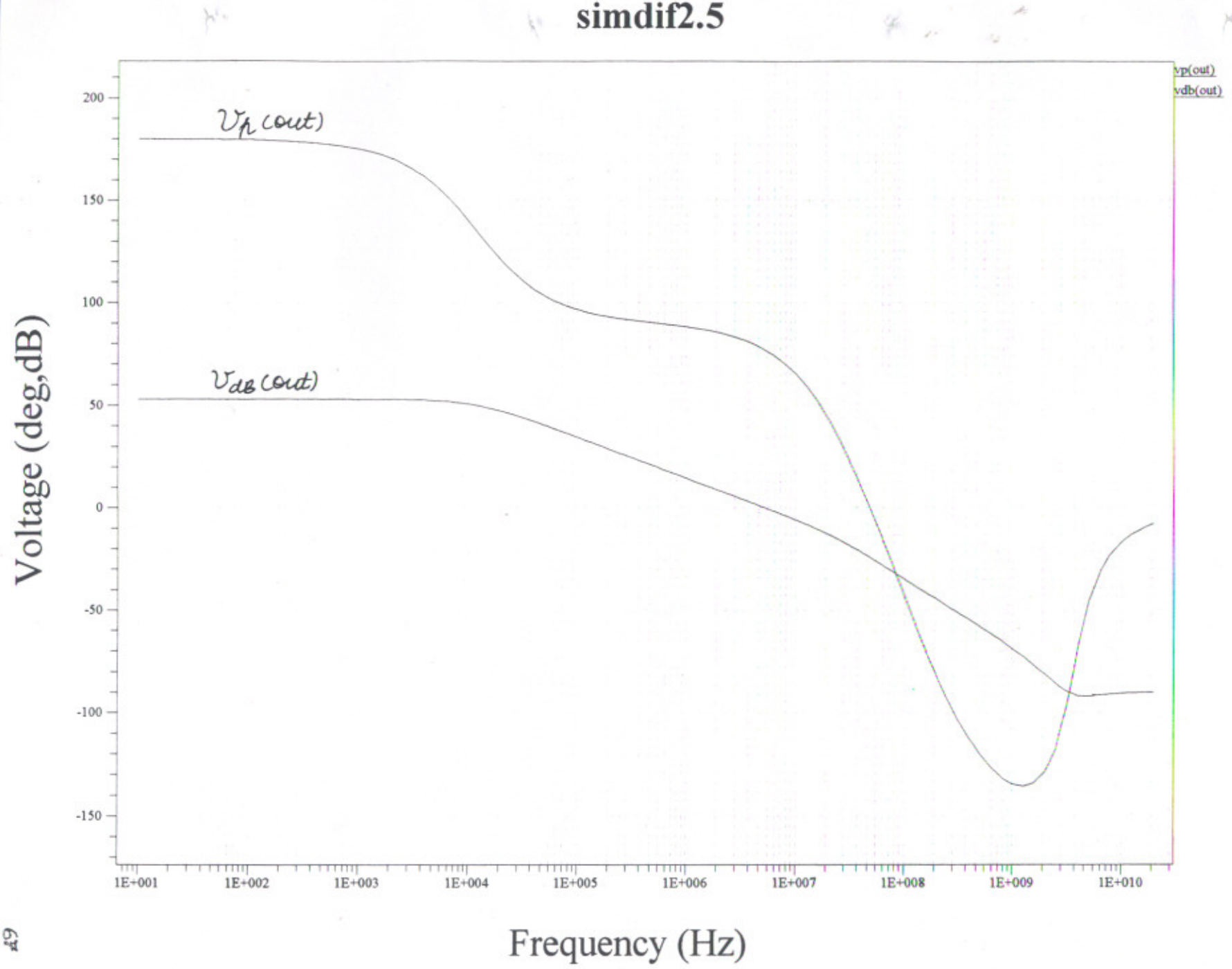


FIGURE 5.1.1. BODE PLOT (SCHEMATIC 5.1)

```
C:\sush\simdif2.5(newmodpar2.5).sp
Page 1

* SPICE netlist written by S-Edit Win32 6.02
* Written on Dec 4, 2002 at 23:40:09

* Waveform probing commands
.probe
.options probefilename="simdif2.5.dat"
+ probesdbfile="C:\sush\simdif2.5.sdb"
+ probetopmodule="simdif2.5"

* Main circuit: simdif2.5
C1 out Gnd 10pF
C2 3 out 3pF
M3 3 4 2 2 NMOS L=2u W=5.268u AD=66p PD=24u AS=66p PS=24u
M4 1 in 2 2 NMOS L=2u W=5.268u AD=66p PD=24u AS=66p PS=24u
M5 out 5 6 6 NMOS L=2u W=60.694u AD=66p PD=24u AS=66p PS=24u
M6 2 5 6 6   NMOS L=2u W=60.694u AD=66p PD=24u AS=66p PS=24u

M7 3 1 7  7 PMOS L=2u W=711.56u AD=66p PD=24u AS=66p PS=24u
M8 out 3 7 7 PMOS L=2u W=949u AD=66p PD=24u AS=66p PS=24u
M9 1 1  7  7  PMOS L=2u W=711.56u AD=66p PD=24u AS=66p PS=24u
v10 in 4 0.0 AC 0.5 0.0
vdd 7 Gnd 2.5
vic 4 6  2
v13 5 6  1
vss 6 Gnd -2.5
.include "C:\Program Files\Tanner EDA\T-Spice Pro v6.02\models\ml2_125.md"
.op
.ac dec 10 10 20000MEG
.print ac vdb(out)
.print ac vp(out)
*.dc lin v12 0 5 0.5
*.print dc v(out)

* End of main circuit: simdif2.5
```

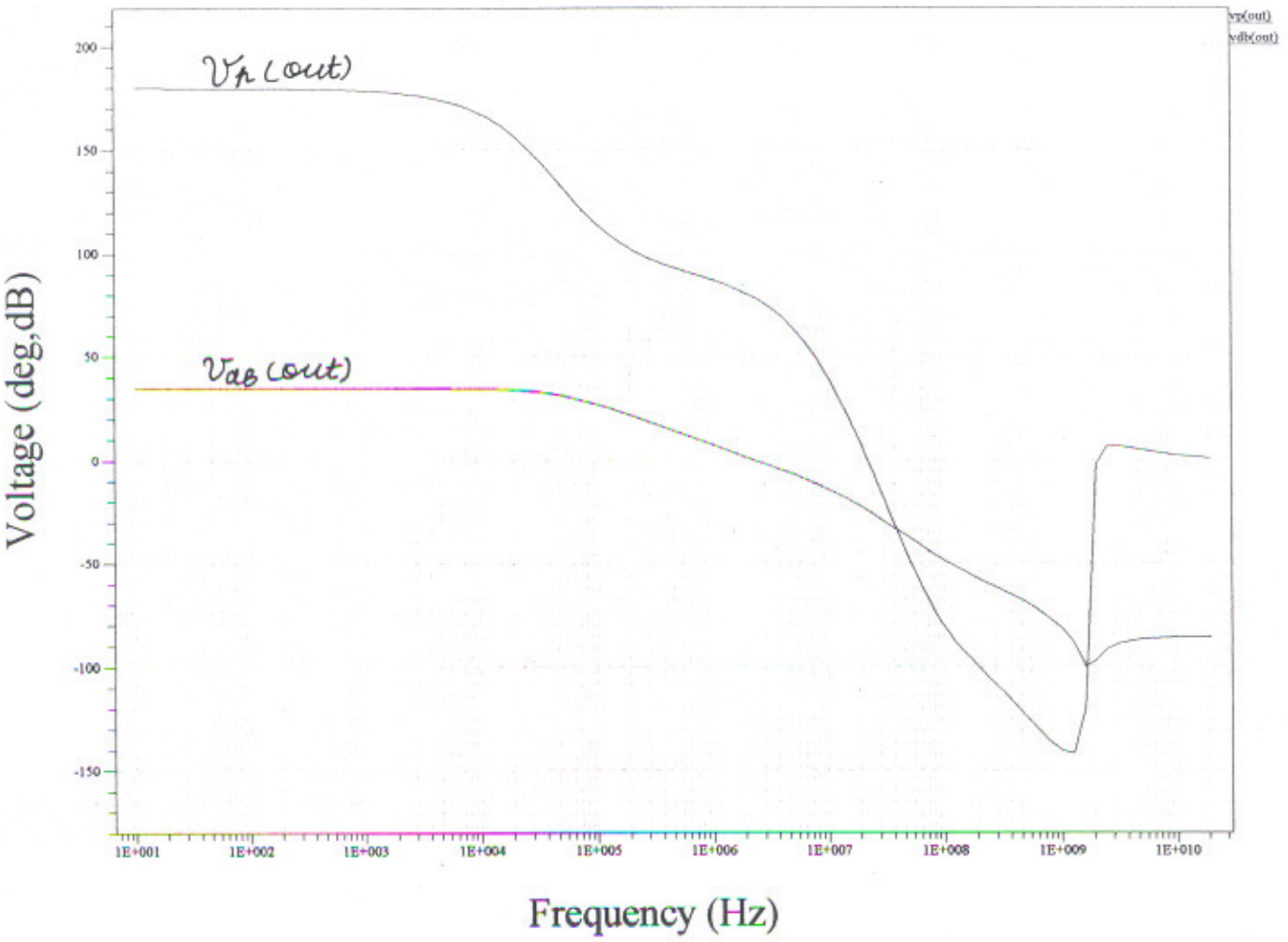


FIGURE 5.1.2 BODE PLOT (SCHEMATIC 5.1)

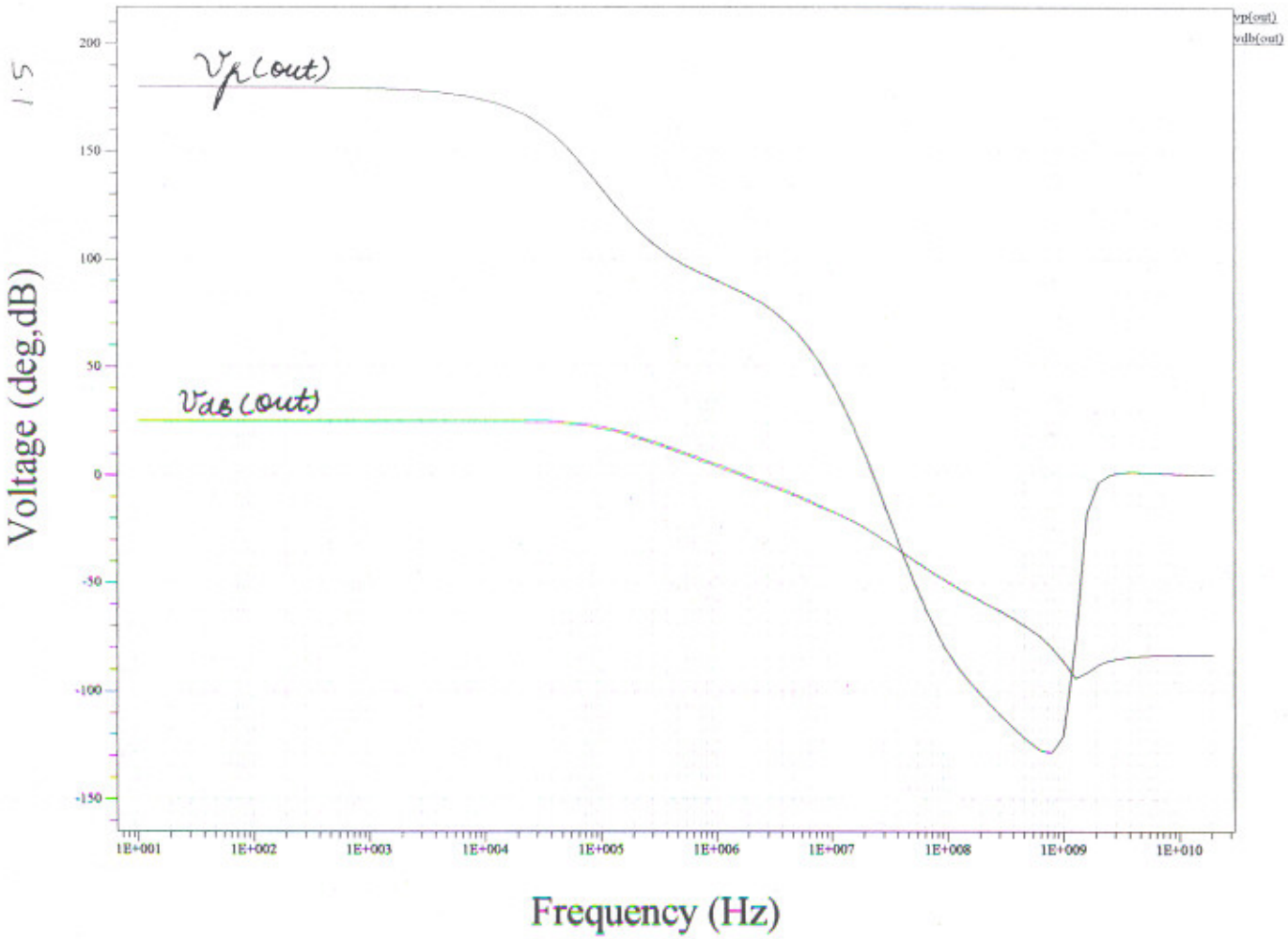


FIGURE 5.1.3 BODE PLOT (±1.5V SUPPLY)

FIGURE 5.1.4. LAYOUT OF (SCHEMATIC FIGURE 5.1)

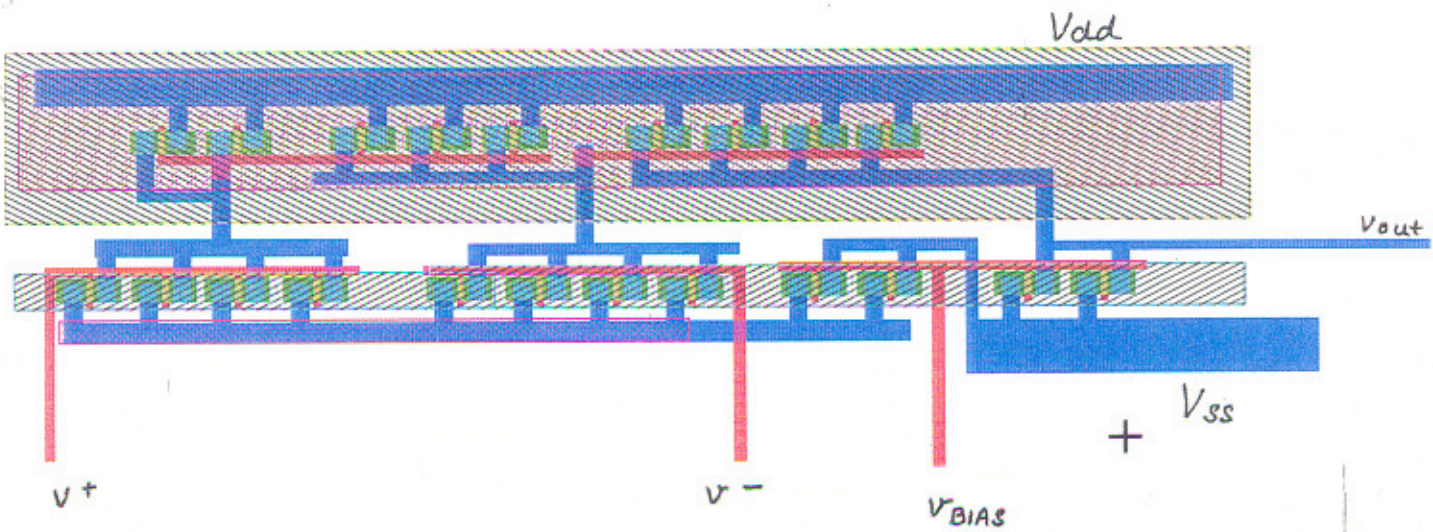
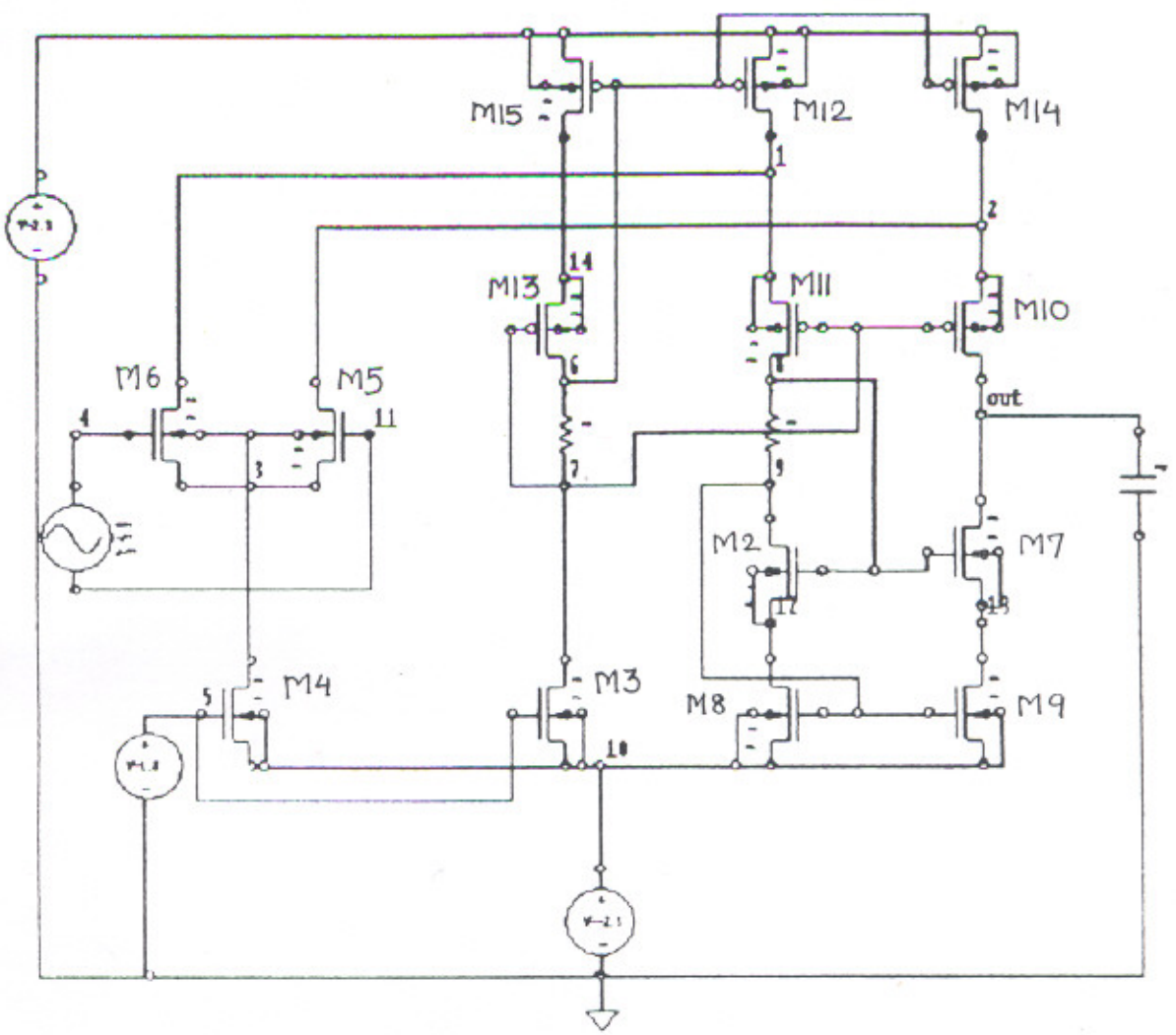
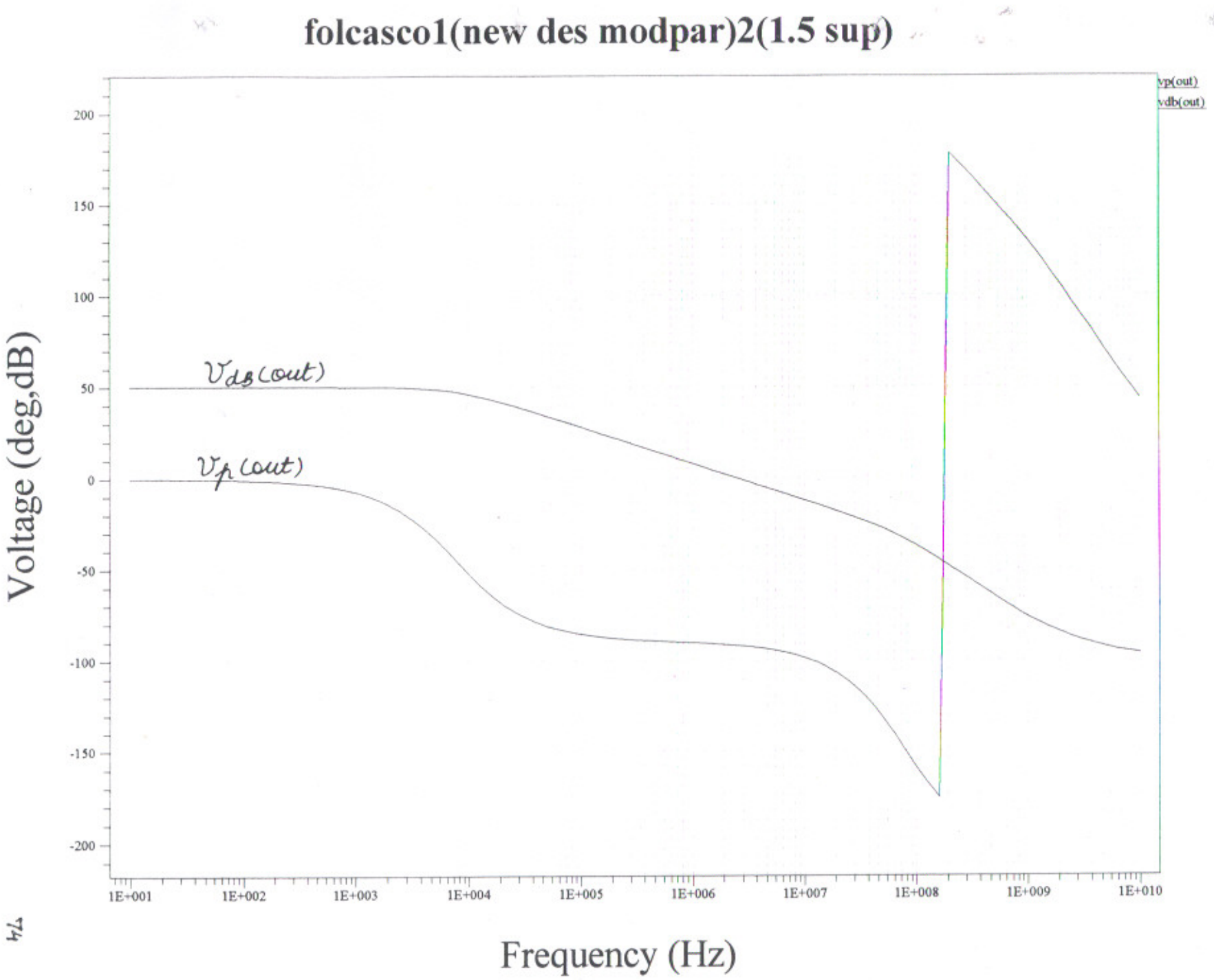


FIGURE 5.2 FOLDED CASCODE AMPLIFIER



```
C:\sush\folcasco1(new des modpar)2(1.5 sup).sp
Page 1

* SPICE netlist written by S-Edit Win32 6.02
* Written on Jan 1, 2003 at 22:41:48

* Waveform probing commands
.probe
.options probefilename="folcasco1.dat"
+ probesdbfile="C:\sush\folcasco1.sdb"
+ probetopmodule="folcasco1"

* Main circuit: folcasco1
C1 out Gnd 10pF
M2 9 8 12 12 NMOS L=2u W=15.1738u AD=66p PD=24u AS=66p PS=24u
M3 7 5 10 10 NMOS L=2u W=30.347u AD=66p PD=24u AS=66p PS=24u
M4 3 5 10 10 NMOS L=2u W=60.69456u AD=66p PD=24u AS=66p PS=24u
M7 out 8 13 13 NMOS L=2u W=15.1738u AD=66p PD=24u AS=66p PS=24u
M8 12 9 10 10 NMOS L=2u W=15.1738u AD=66p PD=24u AS=66p PS=24u
M9 13 9 10 10 NMOS L=2u W=15.1738u AD=66p PD=24u AS=66p PS=24u
*ip tx
M5 2 11 3 3 NMOS L=2u W=40u AD=66p PD=24u AS=66p PS=24u
M6 1 4 3 3 NMOS L=2u W=40u AD=66p PD=24u AS=66p PS=24u
*Pmos Tx
M10 out 7 2 2 PMOS L=2u W=36.43266u AD=66p PD=24u AS=66p PS=24u
M11 8 7 1 1 PMOS L=2u W=36.4326u AD=66p PD=24u AS=66p PS=24u
M12 1 6 N13 N13 PMOS L=2u W=109.28u AD=66p PD=24u AS=66p PS=24u
M13 6 7 14 14 PMOS L=2u W=36.43266u AD=66p PD=24u AS=66p PS=24u
M14 2 6 N13 N13 PMOS L=2u W=109.28u AD=66p PD=24u AS=66p PS=24u
M15 14 6 N13 N13 PMOS L=2u W=109.28u AD=66p PD=24u AS=66p PS=24u

R17 8 9 8.333K TC=0.0, 0.0
R18 6 7 6.25K TC=0.0, 0.0
v19 4 11 0.0 AC 0.5 0.0
v20 10 Gnd -1.5
v21 5 10 1.0
v22 N13 Gnd 1.5
.include "C:\Program Files\Tanner EDA\T-Spice Pro v6.02\models\ml2_125.md"
.print ac vdb(out)
.print ac vp(out)
.op
.ac dec 10 10 10000MEG
* End of main circuit: folcasco1
```


folcasco1(new des modpar)2(1.5 sup)
vp(out)
vdb(out)
200
150
100
50
0
-50
-100
-150
-200
$V_{dB}(out)$
$V_p(out)$
1E+001
1E+002
1E+003
1E+004
1E+005
1E+006
1E+007
1E+008
1E+009
1E+010
Voltage (deg,dB)
Frequency (Hz)

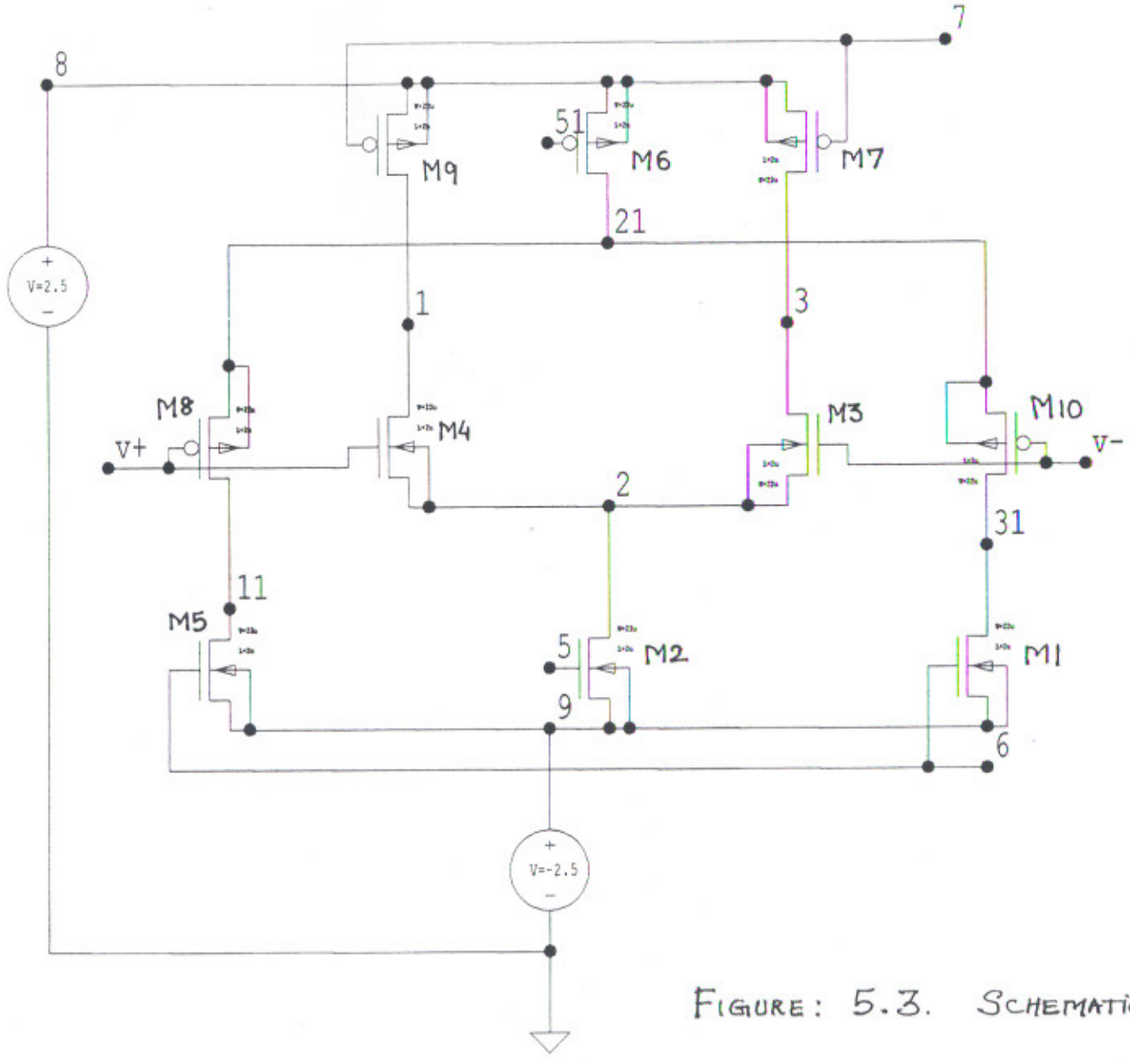


FIGURE: 5.3. SCHEMATIC OF PARALLEL INPUT STAGE

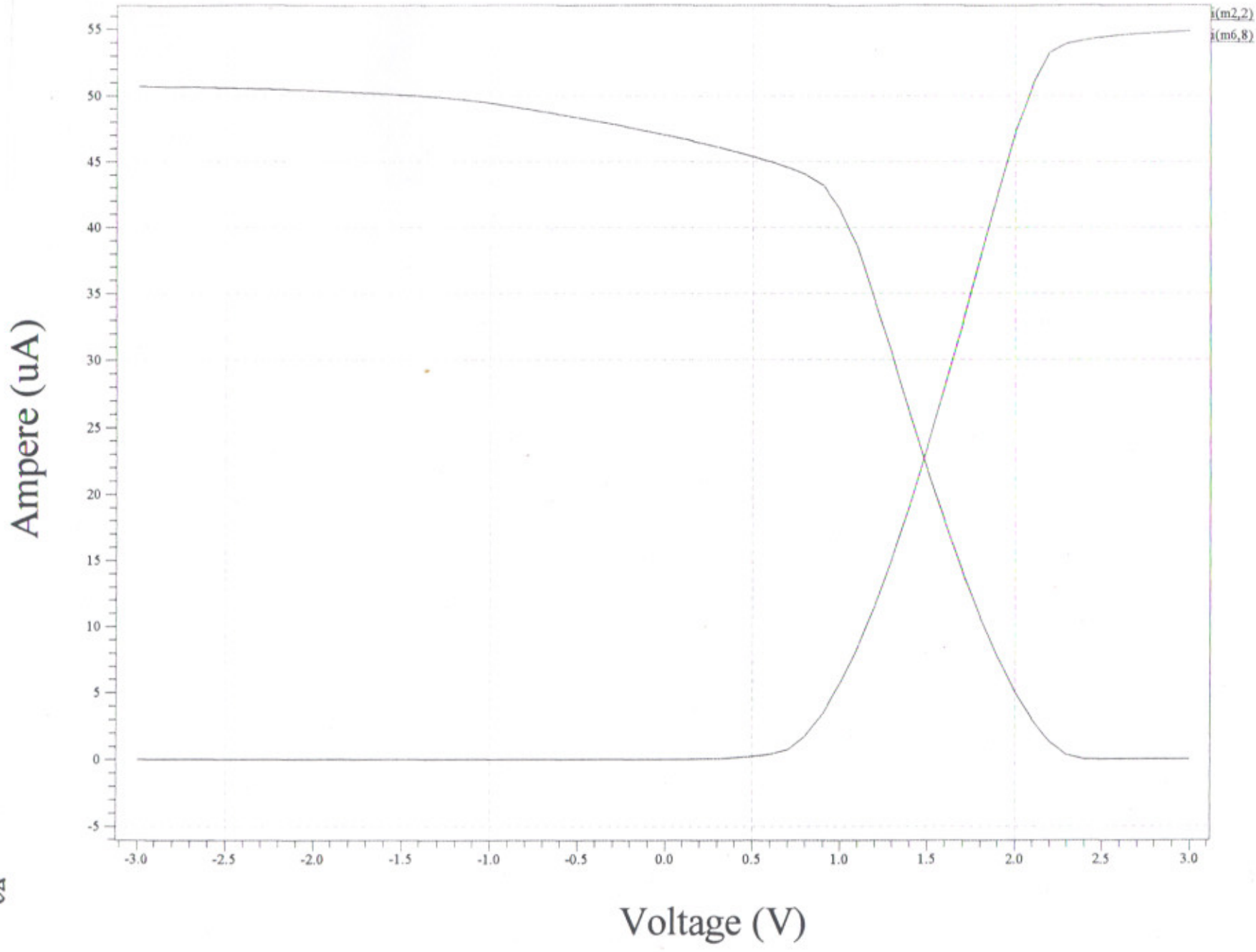
```
* SPICE netlist written by S-Edit Win32 6.02
* Written on Feb 13, 2003 at 02:41:56

* Waveform probing commands
.probe
.options probefilename="gmpll3.dat"
+ probesdbfile="C:\sush\gmpll3.sdb"
+ probetopmodule="gmpll3"

* Main circuit: gmpll3

M1 31 6 9 9 NMOS L=2u W=50u AD=66p PD=24u AS=66p PS=24u
M2 2 5 9 9 NMOS L=2u W=13.34u AD=66p PD=24u AS=66p PS=24u
*ip tx
M3 3 v- 2 2 NMOS L=2u W=1.305u AD=66p PD=24u AS=66p PS=24u
M4 1 v+ 2 2 NMOS L=2u W=1.3050u AD=66p PD=24u AS=66p PS=24u
M5 11 6 9 9 NMOS L=2u W=50u AD=66p PD=24u AS=66p PS=24u

M6 21 51 8 8 PMOS L=2u W=32u AD=66p PD=24u AS=66p PS=24u
M7 3 7 8 8 PMOS L=2u W=64u AD=66p PD=24u AS=66p PS=24u
*ip tx
M10 31 v- 21 21 PMOS L=2u W=3.1324u AD=66p PD=24u AS=66p PS=24u
M8 11 v+ 21 21 PMOS L=2u W=3.1324u AD=66p PD=24u AS=66p PS=24u
M9 1 7 8 8 PMOS L=2u W=64u AD=66p PD=24u AS=66p PS=24u

vin  v+ v- 0.0  AC 0.0 0.0
vdd 8 Gnd 1.5
vss 9 Gnd -1.5
v5  5  9   1.24
v7  8  7   0.88
v6  6  9  .9325
v51 8  51   1.13
vic v- 9  -1
.dc lin vic  -3 3 0.1
.include "C:\Program Files\Tanner EDA\T-Spice Pro v6.02\models\ml2_125.md"
.op
.print dc i(m6,8)
.print dc i(m2,2)

* End of main circuit: gmpll3
```

```
C:\sush\gmpll3.out
Page 1

* T-Spice 6.02 Simulation  Tue Mar 04 04:16:25 2003   C:\sush\gmpll3.sp  (CAZM)
* Command line: tspice -o C:\sush\gmpll3.out C:\sush\gmpll3.sp
* T-Spice Win32 6.02.20000302.11:47:10
* Operating System: Windows NT/95

*SEDIT: probesdbfile="C:\sush\gmpll3.sdb"
*SEDIT: probetopmodule="gmpll3"
*SEDIT: Alter blocks = 0

* Device and node counts:
*             MOSFETs - 10                MOSFET geometries - 6
*                BJTs - 0                          JFETs - 0
*             MESFETs - 0                         Diodes - 0
*          Capacitors - 0                      Resistors - 0
*           Inductors - 0                Mutual inductors - 0
*  Transmission lines - 0       Coupled transmission lines - 0
*     Voltage sources - 8                 Current sources - 0
*                VCVS - 0                            VCCS - 0
*                CCVS - 0                            CCCS - 0
*    V-control switch - 0                I-control switch - 0
*       Macro devices - 0       Functional model instances - 0
*         Subcircuits - 0             Subcircuit instances - 0
*   Independent nodes - 6                   Boundary nodes - 9
*         Total nodes - 15


*SEDIT: Alter=0
*SEDIT: Analysis types DCOP 1 ACMODEL 1 AC 0 TRANSIENT 0 TRANSFER 1 NOISE 0

* BEGIN NON-GRAPHICAL DATA

DC ANALYSIS
v(2) =  -1.5000e+000
v(1) =   1.5000e+000
v(3) =   1.5000e+000
v(31) =  -1.4438e+000
v(11) =  -1.4438e+000
v(21) =  -6.3356e-001
v(9) =  -1.5000e+000
v(v-) =  -2.5000e+000
v(8) =   1.5000e+000
v(51) =   3.7000e-001
v(6) =  -5.6750e-001
v(7) =   6.2000e-001
v(5) =  -2.6000e-001
v(v+) =  -2.5000e+000
i(vin) =   0.0000e+000
i(vdd) =  -4.9424e-005
i(vss) =   4.9424e-005
i(v5) =   0.0000e+000
i(v7) =   0.0000e+000
i(v6) =   0.0000e+000
i(v51) =   0.0000e+000
i(vic) =   0.0000e+000
i(m6,8) =   4.9424e-005
i(m2,2) =   1.8179e-011

* END NON-GRAPHICAL DATA

* BEGIN NON-GRAPHICAL DATA

AC SMALL-SIGNAL MODELS
            M1          M2          M3          M4          M5
```

MODEL	nmos	nmos	nmos	nmos	nmos
TYPE	NMOS	NMOS	NMOS	NMOS	NMOS
ID	2.47e-005	1.82e-011	9.06e-012	9.06e-012	2.47e-005
VGS	9.33e-001	1.24e+000	-1.00e+000	-1.00e+000	9.33e-001
VDS	5.62e-002	7.36e-008	3.00e+000	3.00e+000	5.62e-002
VBS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
VTH	7.51e-001	7.52e-001	7.23e-001	7.23e-001	7.51e-001
VDSAT	2.27e-001	4.24e-001	1.09e-001	1.09e-001	2.27e-001
RS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
RD	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
GM	8.89e-005	3.11e-011	5.68e-011	5.68e-011	8.89e-005
GDS	4.40e-004	2.47e-004	4.74e-013	4.74e-013	4.40e-004
GMB	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
GBD	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
GBS	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
CGS	9.81e-014	2.56e-014	4.38e-015	4.38e-015	9.81e-014
CGD	8.41e-014	2.35e-014	3.77e-016	3.77e-016	8.41e-014
CGB	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
CBD	6.27e-014	3.52e-014	7.97e-015	7.97e-015	6.27e-014
CBS	-1.64e-014	1.32e-014	2.04e-014	2.04e-014	-1.64e-014

	M6	M7	M10	M8	M9
MODEL	pmos	pmos	pmos	pmos	pmos
TYPE	PMOS	PMOS	PMOS	PMOS	PMOS
ID	-4.94e-005	-8.92e-012	-2.47e-005	-2.47e-005	-8.92e-012
VGS	-1.13e+000	-8.80e-001	-1.87e+000	-1.87e+000	-8.80e-001
VDS	-2.13e+000	-4.94e-008	-8.10e-001	-8.10e-001	-4.94e-008
VBS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
VTH	-6.45e-001	-6.53e-001	-6.49e-001	-6.49e-001	-6.53e-001
VDSAT	3.68e-001	1.89e-001	8.29e-001	8.29e-001	1.89e-001
RS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
RD	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
GM	1.99e-004	4.30e-011	3.43e-005	3.43e-005	4.30e-011
GDS	2.35e-006	1.80e-004	7.55e-006	7.55e-006	1.80e-004
GMB	4.35e-005	1.19e-011	8.57e-006	8.57e-006	1.19e-011
GBD	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
GBS	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
CGS	7.52e-014	1.29e-013	7.04e-015	7.04e-015	1.29e-013
CGD	1.07e-014	1.06e-013	2.23e-015	2.23e-015	1.06e-013
CGB	7.96e-015	-1.75e-016	5.11e-016	5.11e-016	-1.75e-016
CBD	2.28e-014	7.07e-014	2.95e-014	2.95e-014	7.07e-014
CBS	5.54e-014	6.28e-014	3.77e-014	3.77e-014	6.28e-014

* END NON-GRAPHICAL DATA



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Transfer Curve Plot (SCHEMATIC 5.3)

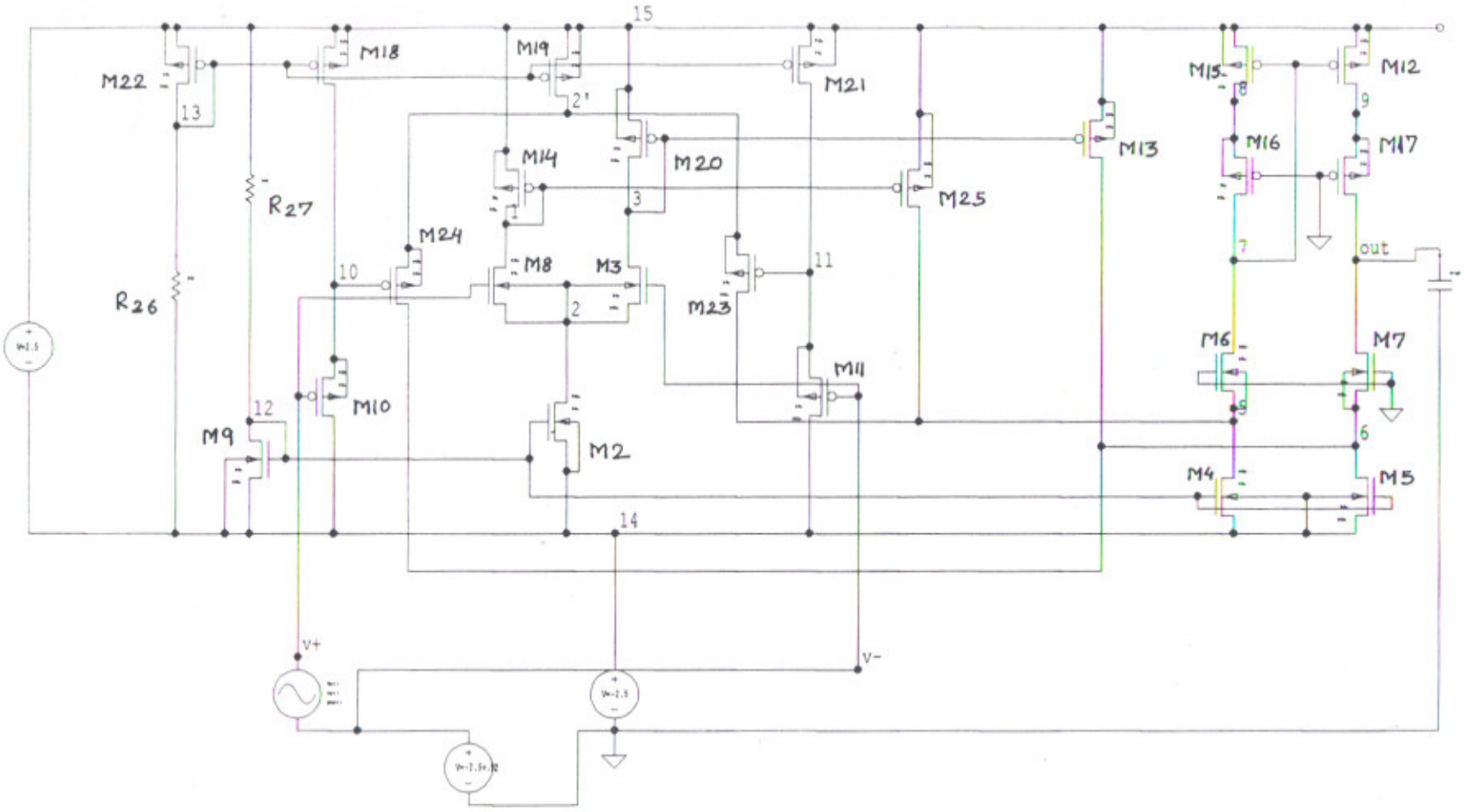


FIGURE 5.4 'CONSTANT TRANSCONDUCTANCE' WITH DC LEVEL SHIFTERS STAGE

```
 * SPICE netlist written by S-Edit Win32 6.02
* Written on Feb 5, 2003 at 23:27:41

* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+ probesdbfile="C:\sush\parall const gm.sdb"
+ probetopmodule="parall const gm"

* Main circuit: parall const gm
C1 out Gnd 10pF

M2 2 12 14 14 NMOS L=2u W=32u AD=66p PD=24u AS=66p PS=24u
*folcasco
M4 5 12 14 14 NMOS L=2u W=64u AD=66p PD=24u AS=66p PS=24u
M5 6 12 14 14 NMOS L=2u W=64u AD=66p PD=24u AS=66p PS=24u
M6 7 Gnd 5 5 NMOS L=2u W=48u AD=66p PD=24u AS=66p PS=24u
M7 out Gnd 6 6 NMOS L=2u W=48u AD=66p PD=24u AS=66p PS=24u
*ip tx
M3 3 v- 2 2  NMOS L=2u W=80u AD=66p PD=24u AS=66p PS=24u
M8 1 v+  2 2  NMOS L=2u W=80u AD=66p PD=24u AS=66p PS=24u
M9 12 12 14 14 NMOS L=2u W=32u AD=66p PD=24u AS=66p PS=24u

M13 6 3 15 15 PMOS L=2u W=76.8u AD=66p PD=24u AS=66p PS=24u
M14 1 1 15 15 PMOS L=2u W=76.8u AD=66p PD=24u AS=66p PS=24u
*folcasco
M12 9 7 15 15 PMOS L=2u W=115.2u AD=66p PD=24u AS=66p PS=24u
M15 8 7 15 15 PMOS L=2u W=115.2u AD=66p PD=24u AS=66p PS=24u
M16 7 Gnd 8 8 PMOS L=2u W=23u AD=66p PD=24u AS=66p PS=24u
M17 out Gnd 9 9 PMOS L=2u W=23u AD=66p PD=24u AS=66p PS=24u

M18 10 13 15 15 PMOS L=2u W=76.8u AD=66p PD=24u AS=66p PS=24u
M19 22 13 15 15 PMOS L=2u W=76.8u AD=66p PD=24u AS=66p PS=24u
M21 11 13 15 15 PMOS L=2u W=76.8.4u AD=66p PD=24u AS=66p PS=24u
M20 3 3 15 15 PMOS L=2u W=76.8u AD=66p PD=24u AS=66p PS=24u
M10 14 v+ 10 10 PMOS L=2u W=14.324u AD=66p PD=24u AS=66p PS=24u
M11 14 v- 11 11 PMOS L=2u W=14.324u AD=66p PD=24u AS=66p PS=24u
M25 5 1 15 15 PMOS L=2u W=76.8u AD=66p PD=24u AS=66p PS=24u
M22 13 13 15 15 PMOS L=2u W=76.8u AD=66p PD=24u AS=66p PS=24u

*ip tx
M23 5  11  22 22 PMOS L=2u W=240u AD=66p PD=24u AS=66p PS=24u
M24 6  10  22 22 PMOS L=2u W=240u AD=66p PD=24u AS=66p PS=24u


R26 13 14 67K TC=0.0, 0.0
R27 15 12 70.67K TC=0.0, 0.0
vin v+ v- 0.0 AC 0.5 0.0
vdd 15 Gnd 1.5
vss 14 Gnd -1.5
.print dc i(vdd,15)
.print dc i(m2,2)
.print dc i(m19,15)

vic v- Gnd 0
.dc lin vic -3 3 0.1

.include "C:\Program Files\Tanner EDA\T-Spice Pro v6.02\models\ml2_125.md"
.op
.ac dec 10 10 10000MEG
.print ac vdb(out)
.print ac vm(out)
```

```
C:\sush\parall const gm3.out
Page 1

* T-Spice 6.02 Simulation  Tue Mar 04 04:21:04 2003   C:\sush\parall const gm3.sp  (CAZM)
* Command line: tspice -o C:\sush\parall const gm3.out C:\sush\parall const gm3.sp
* T-Spice Win32 6.02.20000302.11:47:10
* Operating System: Windows NT/95

*SEDIT: probesdbfile="C:\sush\parall const gm.sdb"
*SEDIT: probetopmodule="parall const gm"
*SEDIT: Alter blocks = 0

* Device and node counts:
*              MOSFETs - 24                MOSFET geometries - 9
*                  BJTs - 0                          JFETs - 0
*              MESFETs - 0                         Diodes - 0
*            Capacitors - 1                      Resistors - 2
*             Inductors - 0                Mutual inductors - 0
*  Transmission lines - 0        Coupled transmission lines - 0
*     Voltage sources - 4                Current sources - 0
*                 VCVS - 0                          VCCS - 0
*                 CCVS - 0                          CCCS - 0
*    V-control switch - 0                I-control switch - 0
*       Macro devices - 0        Functional model instances - 0
*          Subcircuits - 0              Subcircuit instances - 0
*   Independent nodes - 14                 Boundary nodes - 5
*          Total nodes - 19


*SEDIT: Alter=0
*SEDIT: Analysis types DCOP 1 ACMODEL 1 AC 1 TRANSIENT 0 TRANSFER 1 NOISE 0

* BEGIN NON-GRAPHICAL DATA

DC ANALYSIS
v(3) =    6.9915e-001
v(8) =    1.3086e+000
v(12) =  -6.3534e-001
v(13) =   6.1305e-001
v(7) =    1.9296e-001
v(out) =    1.9646e-001
v(6) =  -8.5018e-001
v(22) =    1.5000e+000
v(10) =    1.2048e+000
v(5) =  -8.5024e-001
v(11) =    1.2048e+000
v(1) =    6.9915e-001
v(9) =    1.3086e+000
v(2) =  -7.3754e-001
v(v-) =    0.0000e+000
v(14) =  -1.5000e+000
v(15) =    1.5000e+000
v(v+) =    0.0000e+000
i(vin) =    0.0000e+000
i(vdd) =  -2.6770e-004
i(vss) =    2.6770e-004
i(v31) =    0.0000e+000
i(vdd,15) =  -2.6770e-004
i(m2,2) =    2.9783e-005
i(m19,15) =    3.5116e-010

* END NON-GRAPHICAL DATA

* BEGIN NON-GRAPHICAL DATA

AC SMALL-SIGNAL MODELS
```

	M2	M4	M5	M6	M7
MODEL	nmos	nmos	nmos	nmos	nmos
TYPE	NMOS	NMOS	NMOS	NMOS	NMOS
ID	2.98e-005	5.86e-005	5.86e-005	4.19e-005	4.19e-005
VGS	8.65e-001	8.65e-001	8.65e-001	8.50e-001	8.50e-001
VDS	7.62e-001	6.50e-001	6.50e-001	1.04e+000	1.05e+000
VBS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
VTH	7.40e-001	7.42e-001	7.42e-001	7.37e-001	7.37e-001
VDSAT	1.91e-001	1.90e-001	1.90e-001	1.84e-001	1.84e-001
RS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
RD	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
GM	2.22e-004	4.38e-004	4.38e-004	2.93e-004	2.93e-004
GDS	4.38e-006	9.21e-006	9.21e-006	5.39e-006	5.39e-006
GMB	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
GBD	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
GBS	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
CGS	8.63e-014	1.73e-013	1.73e-013	1.30e-013	1.30e-013
CGD	9.25e-015	1.85e-014	1.85e-014	1.39e-014	1.39e-014
CGB	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
CBD	1.40e-014	1.40e-014	1.40e-014	1.05e-014	1.05e-014
CBS	1.21e-014	-2.24e-016	-2.24e-016	5.78e-015	5.78e-015

	M3	M8	M9	M13	M14
MODEL	nmos	nmos	nmos	pmos	pmos
TYPE	NMOS	NMOS	NMOS	PMOS	PMOS
ID	1.49e-005	1.49e-005	3.02e-005	-1.67e-005	-1.49e-005
VGS	7.38e-001	7.38e-001	8.65e-001	-8.01e-001	-8.01e-001
VDS	1.44e+000	1.44e+000	8.65e-001	-2.35e+000	-8.01e-001
VBS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
VTH	7.34e-001	7.34e-001	7.39e-001	-6.45e-001	-6.49e-001
VDSAT	1.11e-001	1.11e-001	1.92e-001	1.40e-001	1.37e-001
RS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
RD	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
GM	1.70e-004	1.70e-004	2.24e-004	1.74e-004	1.58e-004
GDS	1.68e-006	1.68e-006	4.19e-006	9.58e-007	1.43e-006
GMB	0.00e+000	0.00e+000	0.00e+000	2.40e-005	2.15e-005
GBD	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
GBS	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
CGS	1.25e-013	1.25e-013	8.63e-014	1.75e-013	1.75e-013
CGD	1.33e-014	1.33e-014	9.25e-015	2.57e-014	2.57e-014
CGB	0.00e+000	0.00e+000	0.00e+000	2.64e-014	2.64e-014
CBD	1.05e-014	1.05e-014	1.40e-014	2.28e-014	2.91e-014
CBS	6.22e-015	6.22e-015	1.21e-014	7.59e-014	7.59e-014

	M12	M15	M16	M17	M18
MODEL	pmos	pmos	pmos	pmos	pmos
TYPE	PMOS	PMOS	PMOS	PMOS	PMOS
ID	-4.19e-005	-4.19e-005	-4.19e-005	-4.19e-005	-2.95e-005
VGS	-1.31e+000	-1.31e+000	-1.31e+000	-1.31e+000	-8.87e-001
VDS	-1.91e-001	-1.91e-001	-1.12e+000	-1.11e+000	-2.95e-001
VBS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
VTH	-6.52e-001	-6.52e-001	-6.48e-001	-6.48e-001	-6.51e-001
VDSAT	4.81e-001	4.81e-001	4.85e-001	4.85e-001	1.96e-001
RS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
RD	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
GM	7.49e-005	7.49e-005	1.22e-004	1.22e-004	2.06e-004
GDS	1.56e-004	1.56e-004	2.98e-006	2.98e-006	4.95e-006
GMB	2.17e-005	2.17e-005	2.83e-005	2.83e-005	4.00e-005
GBD	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
GBS	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
CGS	6.02e-014	6.02e-014	3.76e-014	3.76e-014	1.82e-013
CGD	4.31e-014	4.31e-014	5.36e-015	5.36e-015	2.57e-014
CGB	1.44e-015	1.44e-015	3.81e-015	3.81e-015	1.87e-014

CBD	4.72e-014	4.72e-014	2.58e-014	2.58e-014	3.30e-014
CBS	5.02e-014	5.02e-014	4.55e-014	4.55e-014	8.15e-014

	M19	M21	M20	M10	M11
MODEL	pmos	pmos	pmos	pmos	pmos
TYPE	PMOS	PMOS	PMOS	PMOS	PMOS
ID	-3.51e-010	-2.95e-005	-1.49e-005	-2.95e-005	-2.95e-005
VGS	-8.87e-001	-8.87e-001	-8.01e-001	-1.20e+000	-1.20e+000
VDS	-1.57e-006	-2.95e-001	-8.01e-001	-2.70e+000	-2.70e+000
VBS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
VTH	-6.53e-001	-6.51e-001	-6.49e-001	-6.44e-001	-6.44e-001
VDSAT	1.94e-001	1.96e-001	1.37e-001	4.20e-001	4.20e-001
RS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
RD	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
GM	1.64e-009	2.06e-004	1.58e-004	1.05e-004	1.05e-004
GDS	2.24e-004	4.95e-006	1.43e-006	1.23e-006	1.23e-006
GMB	4.61e-010	4.00e-005	2.15e-005	2.31e-005	2.31e-005
GBD	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
GBS	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
CGS	1.54e-013	1.82e-013	1.75e-013	3.36e-014	3.36e-014
CGD	1.28e-013	2.57e-014	2.57e-014	4.80e-015	4.80e-015
CGB	5.66e-016	1.87e-014	2.64e-014	3.50e-015	3.50e-015
CBD	7.79e-014	3.30e-014	2.91e-014	2.28e-014	2.28e-014
CBS	6.88e-014	8.15e-014	7.59e-014	4.46e-014	4.46e-014

	M25	M22	M23	M24
MODEL	pmos	pmos	pmos	pmos
TYPE	PMOS	PMOS	PMOS	PMOS
ID	-1.67e-005	-3.15e-005	-1.76e-010	-1.76e-010
VGS	-8.01e-001	-8.87e-001	-2.95e-001	-2.95e-001
VDS	-2.35e+000	-8.87e-001	-2.35e+000	-2.35e+000
VBS	0.00e+000	0.00e+000	0.00e+000	0.00e+000
VTH	-6.45e-001	-6.49e-001	-6.45e-001	-6.45e-001
VDSAT	1.40e-001	1.98e-001	2.89e-002	2.89e-002
RS	0.00e+000	0.00e+000	0.00e+000	0.00e+000
RD	0.00e+000	0.00e+000	0.00e+000	0.00e+000
GM	1.74e-004	2.20e-004	4.09e-009	4.09e-009
GDS	9.58e-007	2.61e-006	1.38e-011	1.38e-011
GMB	2.40e-005	4.26e-005	2.55e-010	2.55e-010
GBD	1.00e-014	1.00e-014	1.00e-014	1.00e-014
GBS	1.00e-014	1.00e-014	1.00e-014	1.00e-014
CGS	1.75e-013	1.82e-013	5.59e-014	5.59e-014
CGD	2.57e-014	2.57e-014	3.70e-014	3.70e-014
CGB	2.64e-014	1.87e-014	9.81e-014	9.81e-014
CBD	2.28e-014	2.91e-014	2.28e-014	2.28e-014
CBS	7.59e-014	8.15e-014	1.71e-014	1.71e-014

	R26	R27
R	6.70e+004	7.07e+004
VDROP	2.11e+000	2.14e+000
CURRENT	3.15e-005	3.02e-005

* END NON-GRAPHICAL DATA

*WEDIT: XFER cycles v31 61
*WEDIT: .dc v31 -3 3 0.1
TRANSFER ANALYSIS

v31<V>	i(vdd,15)<A>	i(m2,2)<A>	i(m19,15)<A>
-3.0000e+000	-2.4966e-004	2.7787e-011	3.4006e-005
-2.9000e+000	-2.4958e-004	5.2293e-011	3.3967e-005
-2.8000e+000	-2.4950e-004	9.6984e-011	3.3920e-005
-2.7000e+000	-2.4939e-004	1.8072e-010	3.3863e-005
-2.6000e+000	-2.4925e-004	3.3888e-010	3.3788e-005

ID	2.98e-005	5.86e-005	5.86e-005	4.19e-005	4.19e-005
VGS	8.65e-001	8.65e-001	8.65e-001	8.50e-001	8.50e-001
VDS	7.62e-001	6.50e-001	6.50e-001	1.04e+000	1.05e+000
VBS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
VTH	7.40e-001	7.42e-001	7.42e-001	7.37e-001	7.37e-001
VDSAT	1.91e-001	1.90e-001	1.90e-001	1.84e-001	1.84e-001
RS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
RD	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
GM	2.22e-004	4.38e-004	4.38e-004	2.93e-004	2.93e-004
GDS	4.38e-006	9.21e-006	9.21e-006	5.39e-006	5.39e-006
GMB	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
GBD	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
GBS	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
CGS	8.63e-014	1.73e-013	1.73e-013	1.30e-013	1.30e-013
CGD	9.25e-015	1.85e-014	1.85e-014	1.39e-014	1.39e-014
CGB	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
CBD	1.40e-014	1.40e-014	1.40e-014	1.05e-014	1.05e-014
CBS	1.21e-014	-2.24e-016	-2.24e-016	5.78e-015	5.78e-015

	M3	M8	M9	M13	M14
MODEL	nmos	nmos	nmos	pmos	pmos
TYPE	NMOS	NMOS	NMOS	PMOS	PMOS
ID	1.49e-005	1.49e-005	3.02e-005	-1.67e-005	-1.49e-005
VGS	7.38e-001	7.38e-001	8.65e-001	-8.01e-001	-8.01e-001
VDS	1.44e+000	1.44e+000	8.65e-001	-2.35e+000	-8.01e-001
VBS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
VTH	7.34e-001	7.34e-001	7.39e-001	-6.45e-001	-6.49e-001
VDSAT	1.11e-001	1.11e-001	1.92e-001	1.40e-001	1.37e-001
RS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
RD	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
GM	1.70e-004	1.70e-004	2.24e-004	1.74e-004	1.58e-004
GDS	1.68e-006	1.68e-006	4.19e-006	9.58e-007	1.43e-006
GMB	0.00e+000	0.00e+000	0.00e+000	2.40e-005	2.15e-005
GBD	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
GBS	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
CGS	1.25e-013	1.25e-013	8.63e-014	1.75e-013	1.75e-013
CGD	1.33e-014	1.33e-014	9.25e-015	2.57e-014	2.57e-014
CGB	0.00e+000	0.00e+000	0.00e+000	2.64e-014	2.64e-014
CBD	1.05e-014	1.05e-014	1.40e-014	2.28e-014	2.91e-014
CBS	6.22e-015	6.22e-015	1.21e-014	7.59e-014	7.59e-014

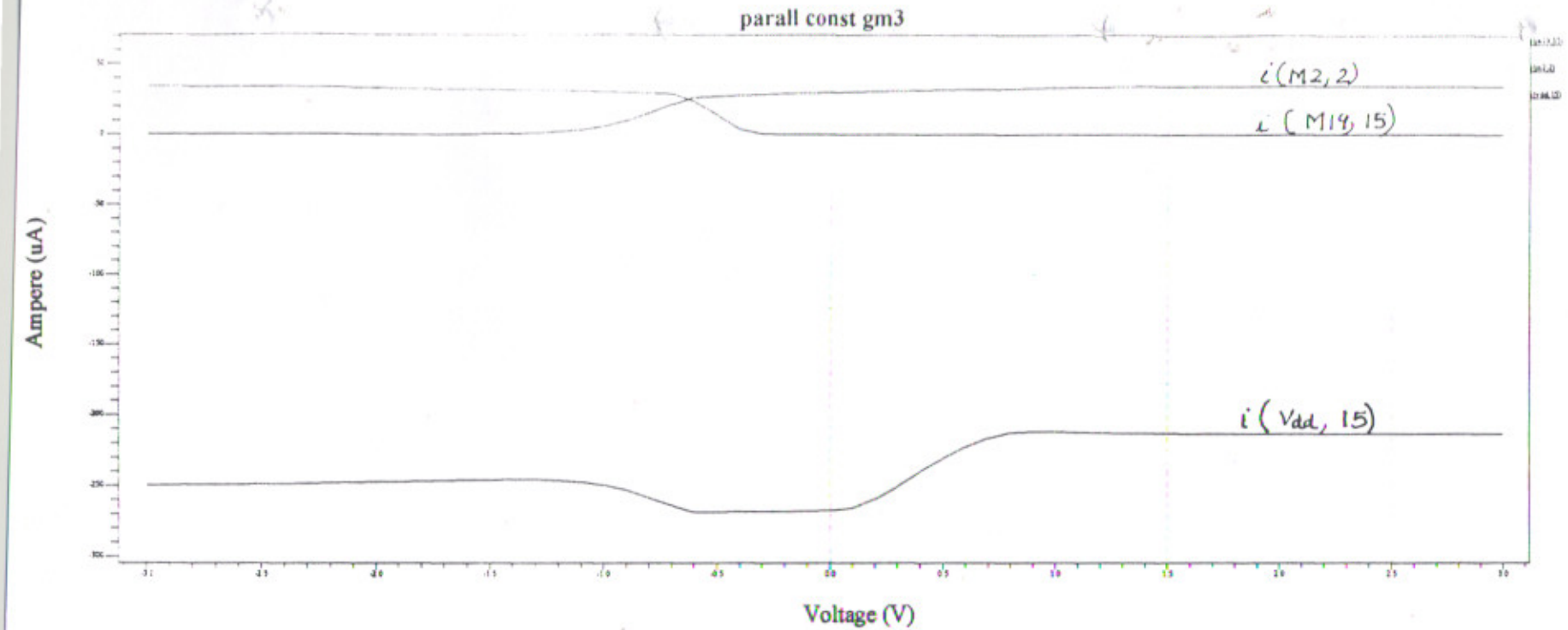
	M12	M15	M16	M17	M18
MODEL	pmos	pmos	pmos	pmos	pmos
TYPE	PMOS	PMOS	PMOS	PMOS	PMOS
ID	-4.19e-005	-4.19e-005	-4.19e-005	-4.19e-005	-2.95e-005
VGS	-1.31e+000	-1.31e+000	-1.31e+000	-1.31e+000	-8.87e-001
VDS	-1.91e-001	-1.91e-001	-1.12e+000	-1.11e+000	-2.95e-001
VBS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
VTH	-6.52e-001	-6.52e-001	-6.48e-001	-6.48e-001	-6.51e-001
VDSAT	4.81e-001	4.81e-001	4.85e-001	4.85e-001	1.96e-001
RS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
RD	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
GM	7.49e-005	7.49e-005	1.22e-004	1.22e-004	2.06e-004
GDS	1.56e-004	1.56e-004	2.98e-006	2.98e-006	4.95e-006
GMB	2.17e-005	2.17e-005	2.83e-005	2.83e-005	4.00e-005
GBD	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
GBS	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
CGS	6.02e-014	6.02e-014	3.76e-014	3.76e-014	1.82e-013
CGD	4.31e-014	4.31e-014	5.36e-015	5.36e-015	2.57e-014
CGB	1.44e-015	1.44e-015	3.81e-015	3.81e-015	1.87e-014
CBD	4.72e-014	4.72e-014	2.58e-014	2.58e-014	3.30e-014
CBS	5.02e-014	5.02e-014	4.55e-014	4.55e-014	8.15e-014

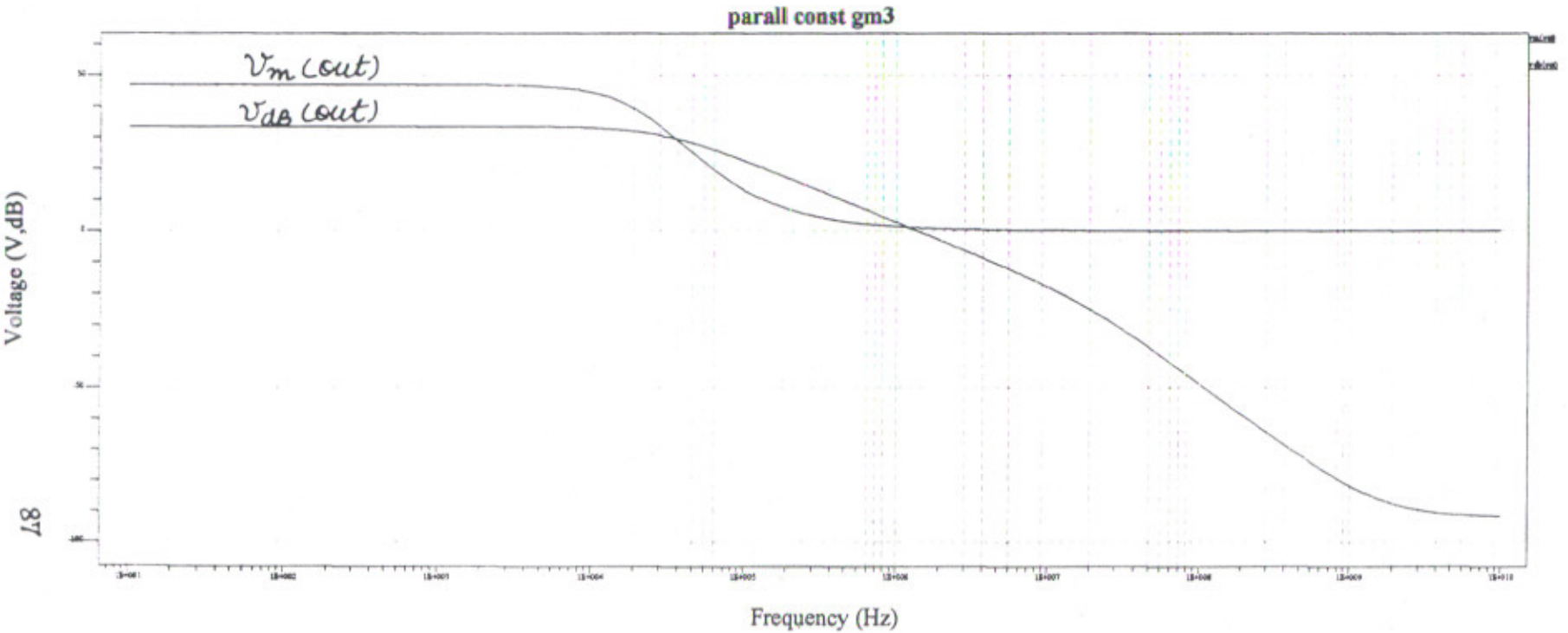
	M19	M21	M20	M10	M11
MODEL	pmos	pmos	pmos	pmos	pmos
TYPE	PMOS	PMOS	PMOS	PMOS	PMOS
ID	-3.51e-010	-2.95e-005	-1.49e-005	-2.95e-005	-2.95e-005
VGS	-8.87e-001	-8.87e-001	-8.01e-001	-1.20e+000	-1.20e+000
VDS	-1.57e-006	-2.95e-001	-8.01e-001	-2.70e+000	-2.70e+000
VBS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
VTH	-6.53e-001	-6.51e-001	-6.49e-001	-6.44e-001	-6.44e-001
VDSAT	1.94e-001	1.96e-001	1.37e-001	4.20e-001	4.20e-001
RS	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
RD	0.00e+000	0.00e+000	0.00e+000	0.00e+000	0.00e+000
GM	1.64e-009	2.06e-004	1.58e-004	1.05e-004	1.05e-004
GDS	2.24e-004	4.95e-006	1.43e-006	1.23e-006	1.23e-006
GMB	4.61e-010	4.00e-005	2.15e-005	2.31e-005	2.31e-005
GBD	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
GBS	1.00e-014	1.00e-014	1.00e-014	1.00e-014	1.00e-014
CGS	1.54e-013	1.82e-013	1.75e-013	3.36e-014	3.36e-014
CGD	1.28e-013	2.57e-014	2.57e-014	4.80e-015	4.80e-015
CGB	5.66e-016	1.87e-014	2.64e-014	3.50e-015	3.50e-015
CBD	7.79e-014	3.30e-014	2.91e-014	2.28e-014	2.28e-014
CBS	6.88e-014	8.15e-014	7.59e-014	4.46e-014	4.46e-014

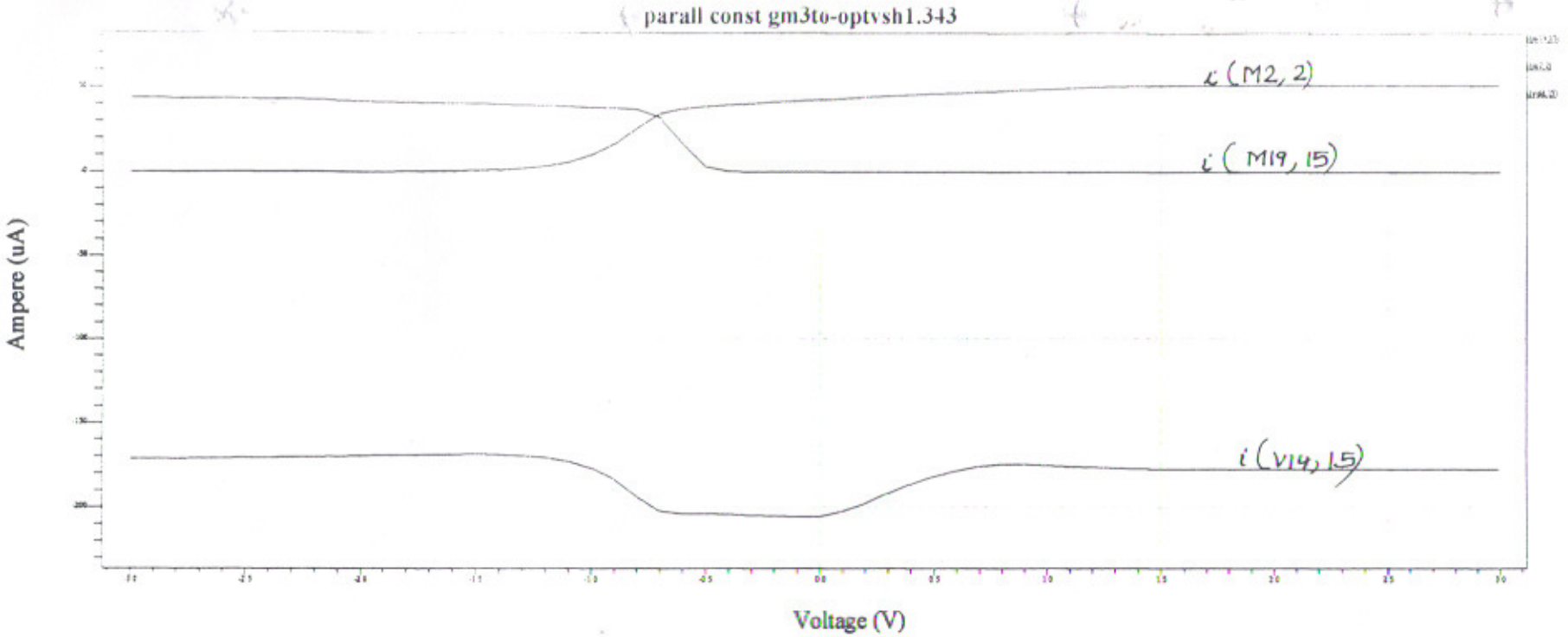
	M25	M22	M23	M24
MODEL	pmos	pmos	pmos	pmos
TYPE	PMOS	PMOS	PMOS	PMOS
ID	-1.67e-005	-3.15e-005	-1.76e-010	-1.76e-010
VGS	-8.01e-001	-8.87e-001	-2.95e-001	-2.95e-001
VDS	-2.35e+000	-8.87e-001	-2.35e+000	-2.35e+000
VBS	0.00e+000	0.00e+000	0.00e+000	0.00e+000
VTH	-6.45e-001	-6.49e-001	-6.45e-001	-6.45e-001
VDSAT	1.40e-001	1.98e-001	2.89e-002	2.89e-002
RS	0.00e+000	0.00e+000	0.00e+000	0.00e+000
RD	0.00e+000	0.00e+000	0.00e+000	0.00e+000
GM	1.74e-004	2.20e-004	4.09e-009	4.09e-009
GDS	9.58e-007	2.61e-006	1.38e-011	1.38e-011
GMB	2.40e-005	4.26e-005	2.55e-010	2.55e-010
GBD	1.00e-014	1.00e-014	1.00e-014	1.00e-014
GBS	1.00e-014	1.00e-014	1.00e-014	1.00e-014
CGS	1.75e-013	1.82e-013	5.59e-014	5.59e-014
CGD	2.57e-014	2.57e-014	3.70e-014	3.70e-014
CGB	2.64e-014	1.87e-014	9.81e-014	9.81e-014
CBD	2.28e-014	2.91e-014	2.28e-014	2.28e-014
CBS	7.59e-014	8.15e-014	1.71e-014	1.71e-014

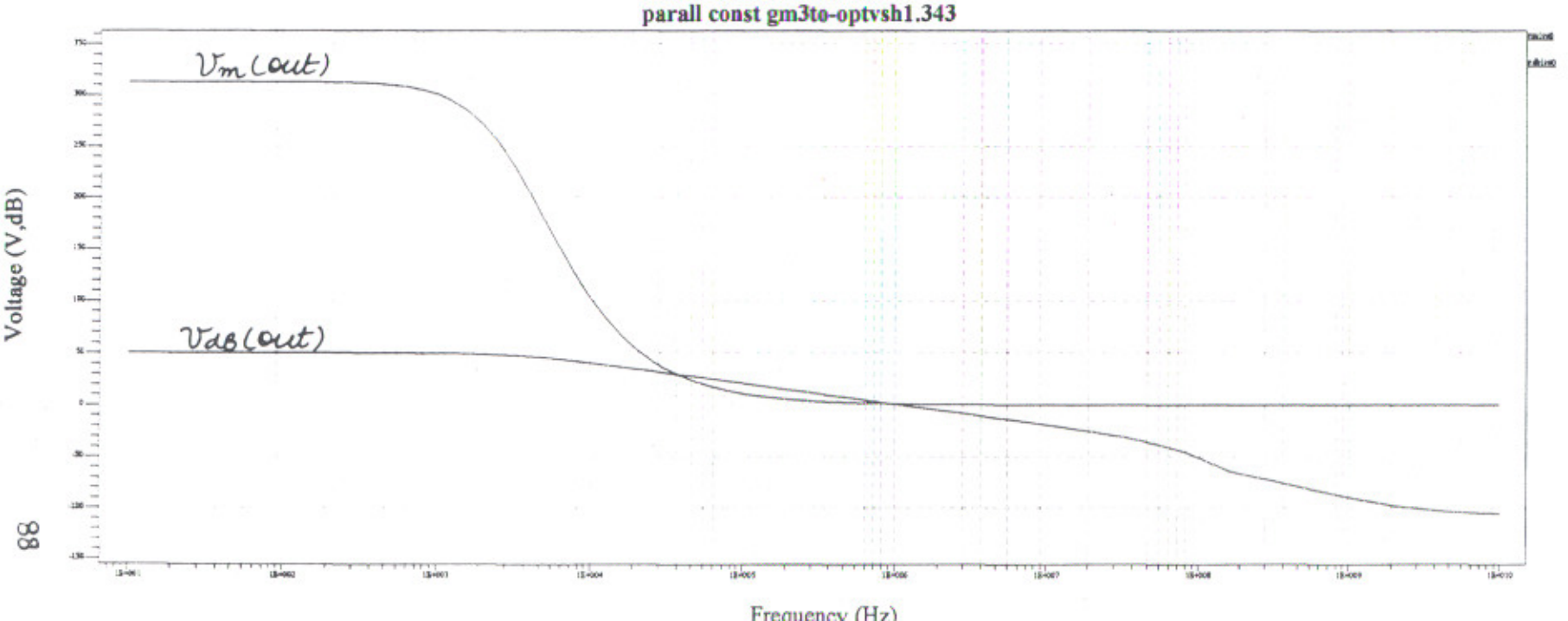
	R26	R27
R	6.70e+004	7.07e+004
VDROP	2.11e+000	2.14e+000
CURRENT	3.15e-005	3.02e-005

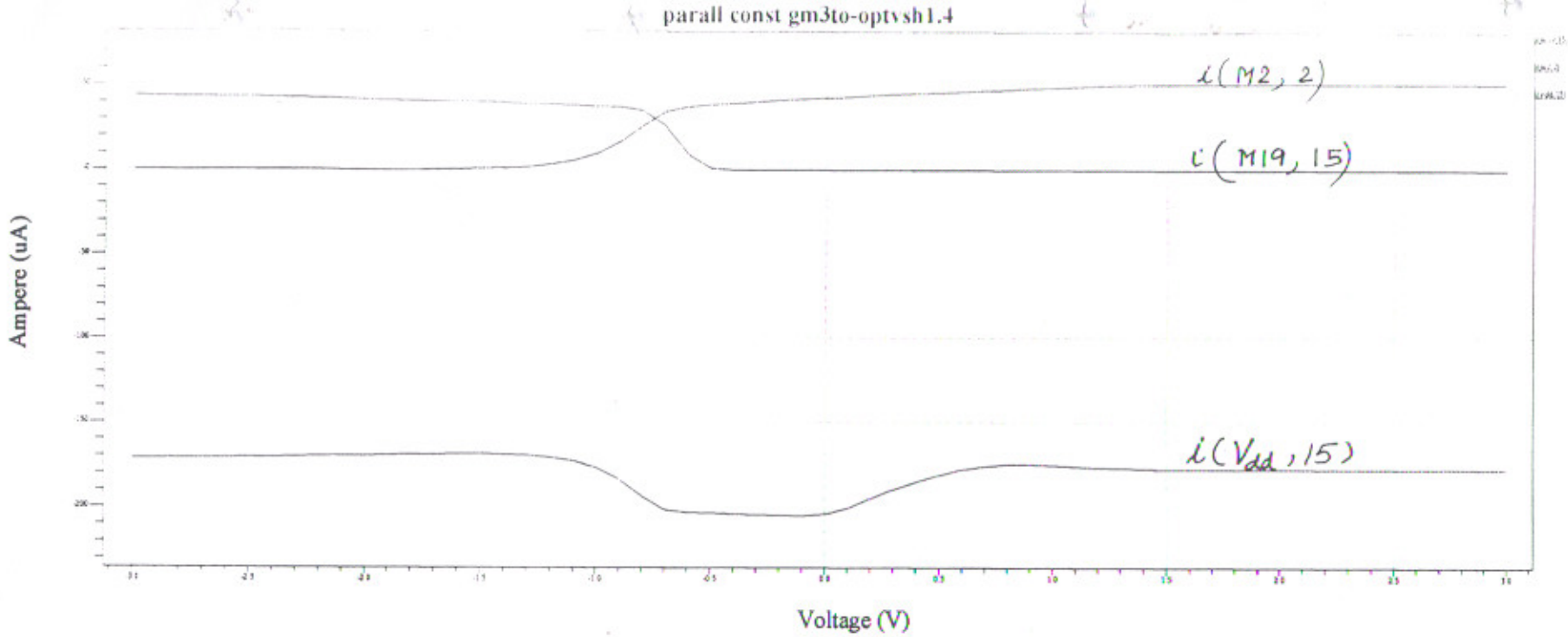
* END NON-GRAPHICAL DATA

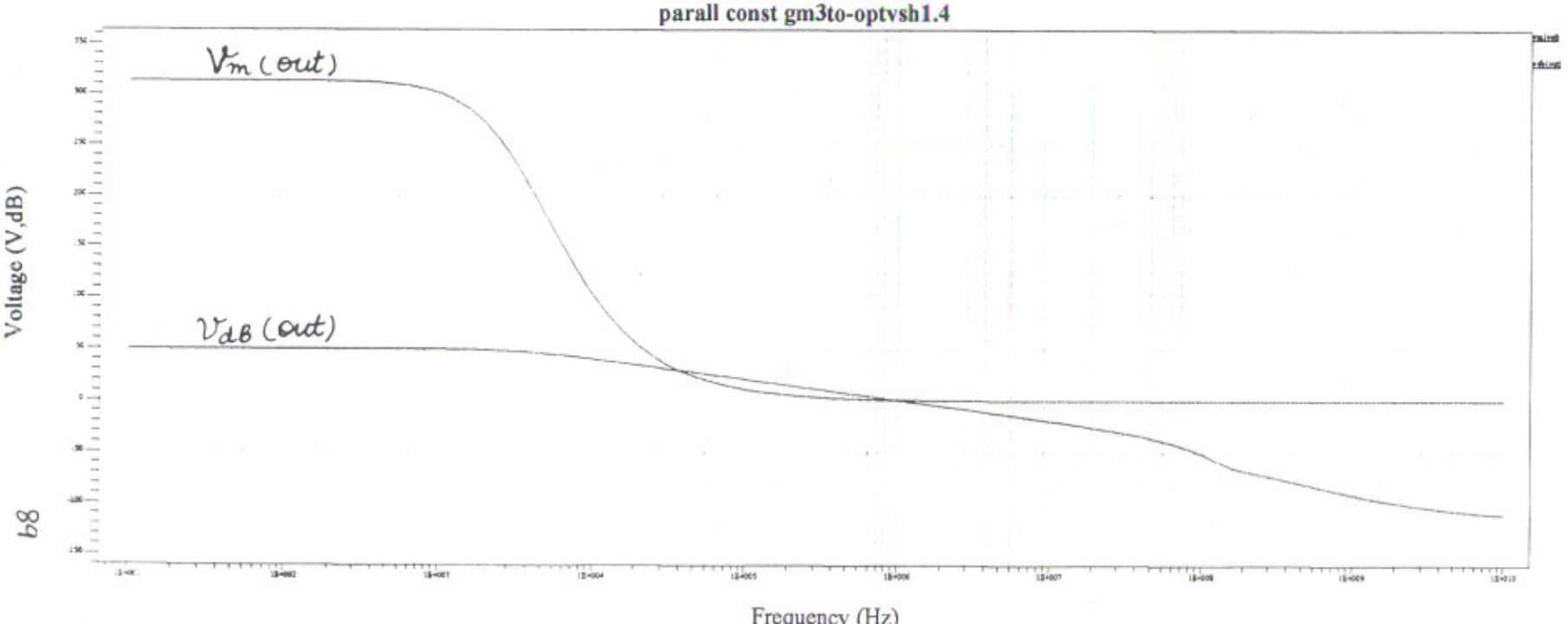

parall const gm3
i(M2, 2)
i (M19, 15)
i (Vdd, 15)
Ampere (uA)
Voltage (V)

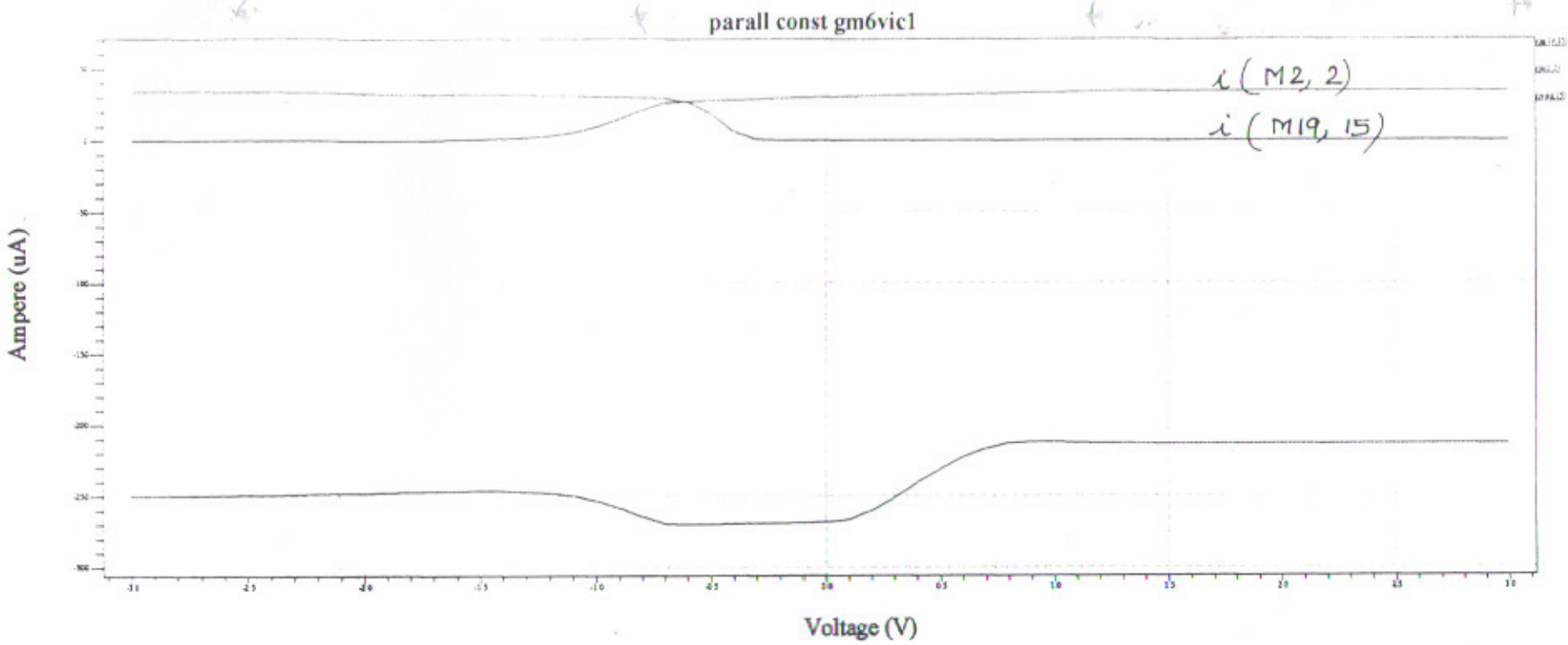

parall const gm3
Vm (out)
VdB (out)
Voltage (V,dB)
Frequency (Hz)

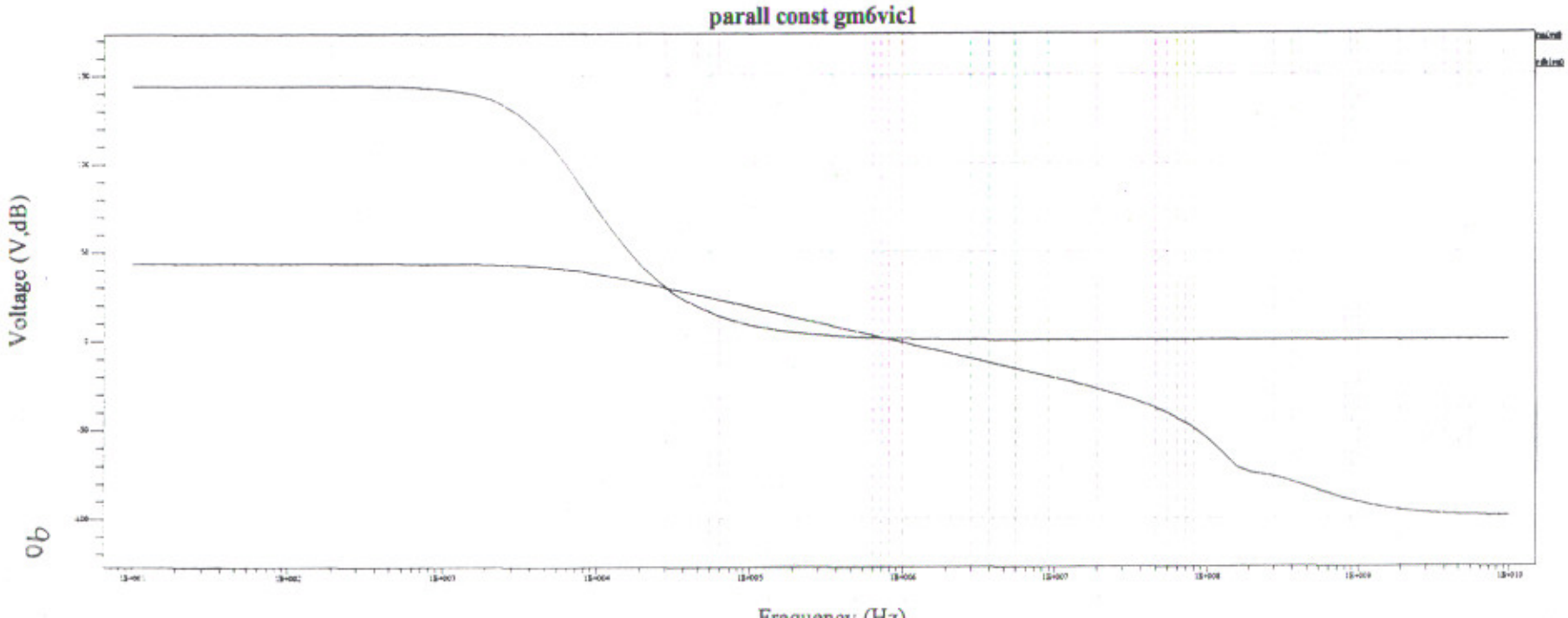

parall const gm3to-optvsh1.343
i (M2, 2)
i (M19, 15)
i (V14, 15)
Ampere (uA)
Voltage (V)

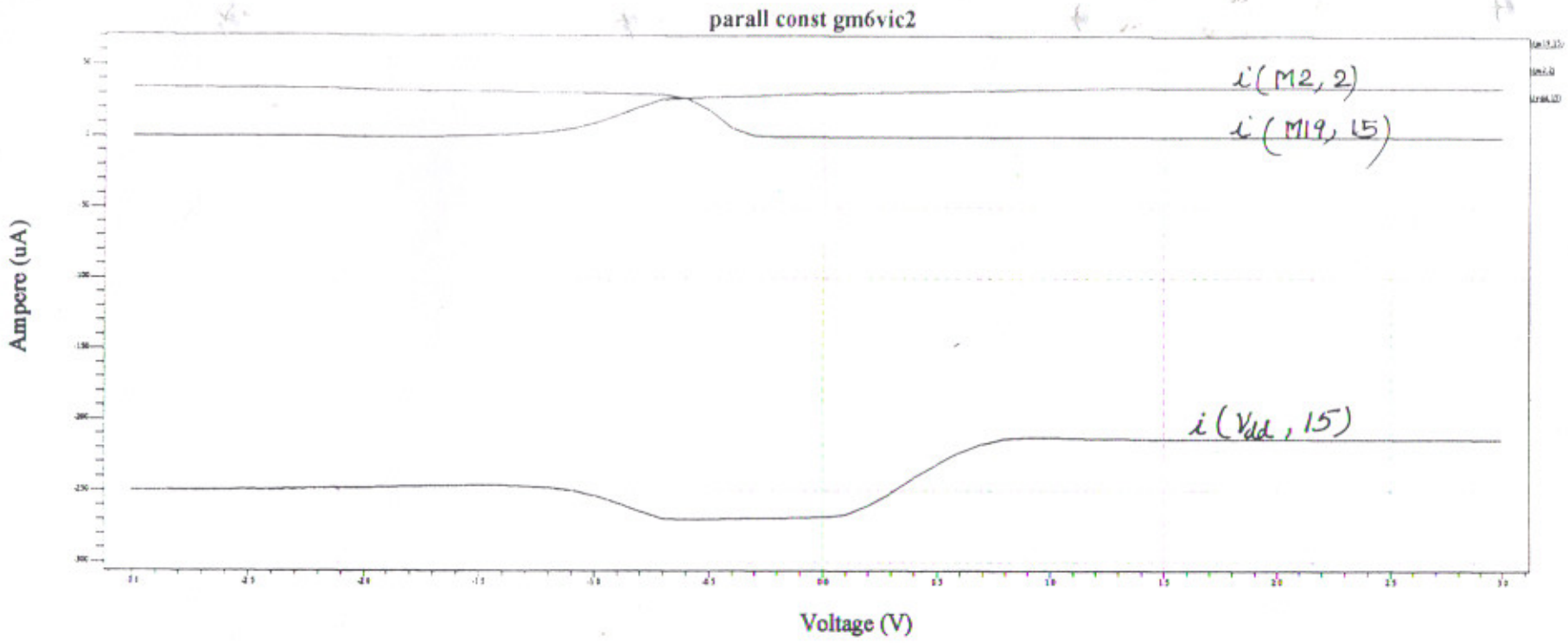

parall const gm3to-optvsh1.343
Vm(out)
Vdb(out)
Voltage (V,dB)
Frequency (Hz)

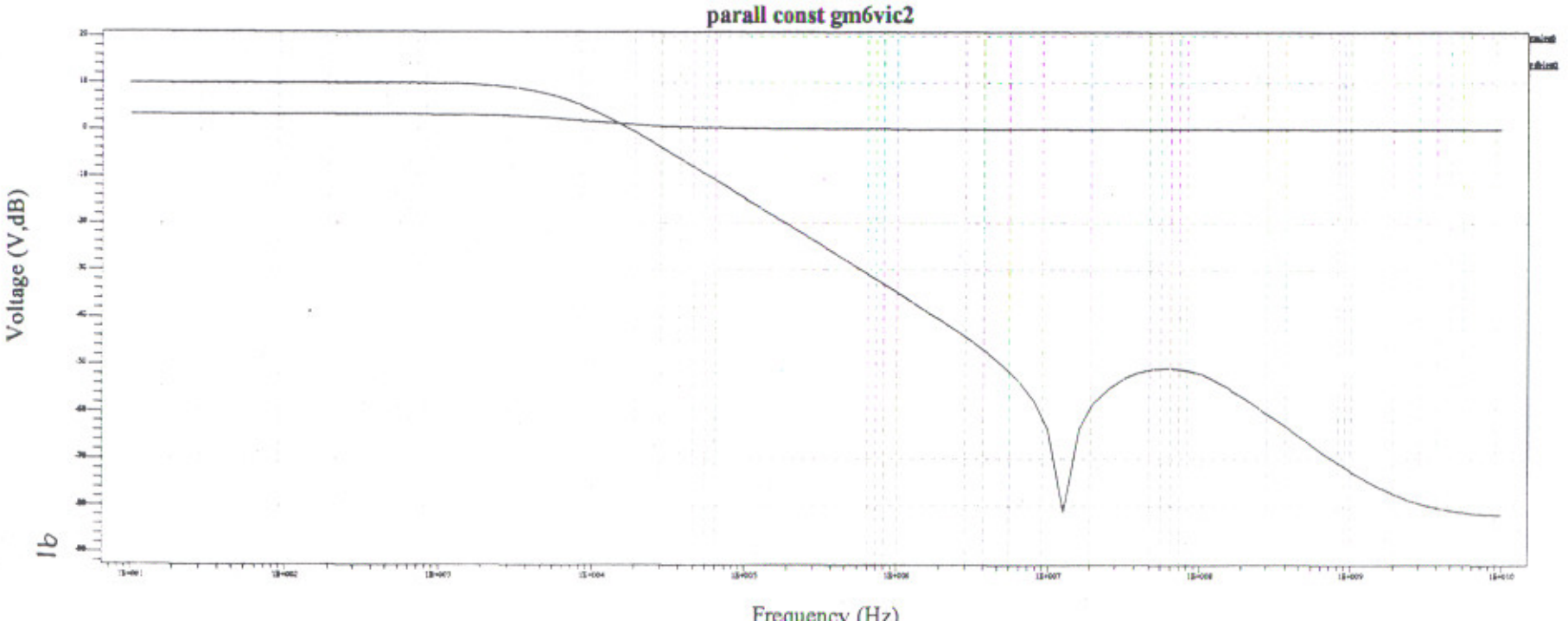

parall const gm3to-optvsh1.4
i(M2, 2)
i(M19, 15)
i(Vdd, 15)
Ampere (uA)
Voltage (V)


parall const gm3to-optvsh1.4
Vm(out)
VdB(out)
Voltage (V,dB)
Frequency (Hz)

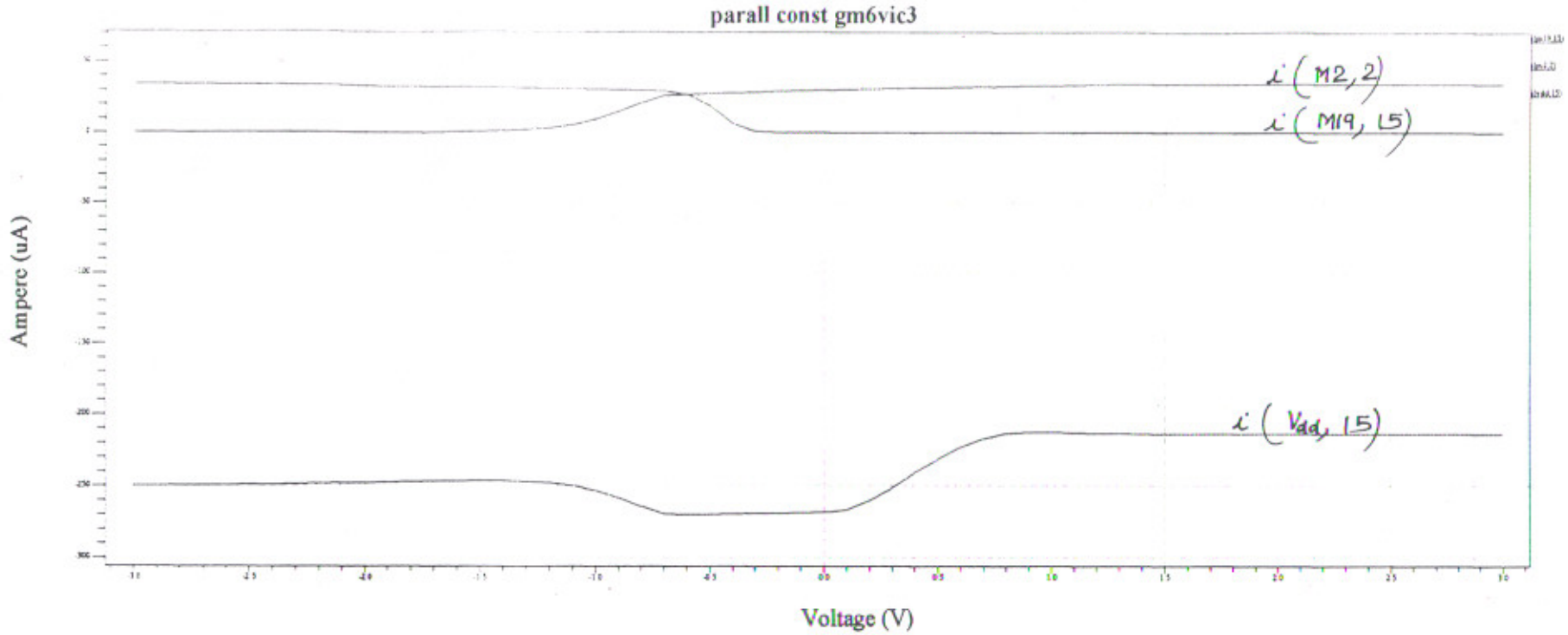

parall const gm6vic1
i (M2, 2)
i (M19, 15)
Ampere (uA)
Voltage (V)

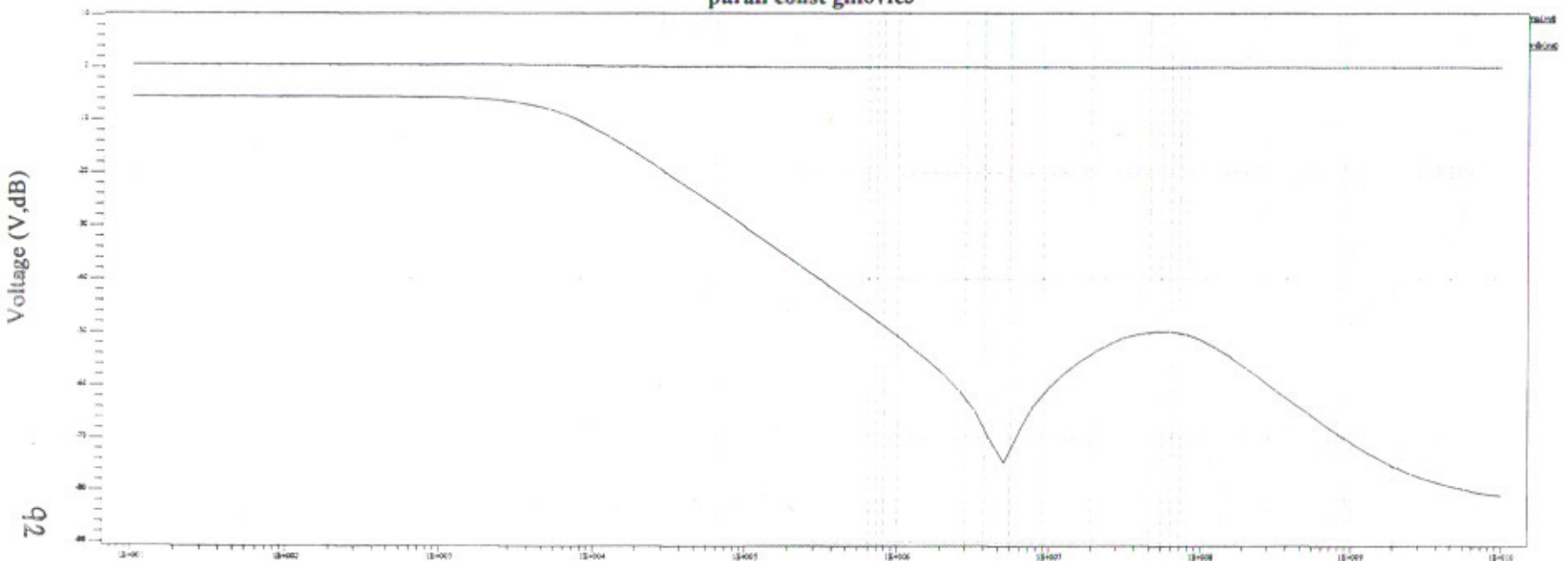

parall const gm6vic1
Voltage (V,dB)
Frequency (Hz)

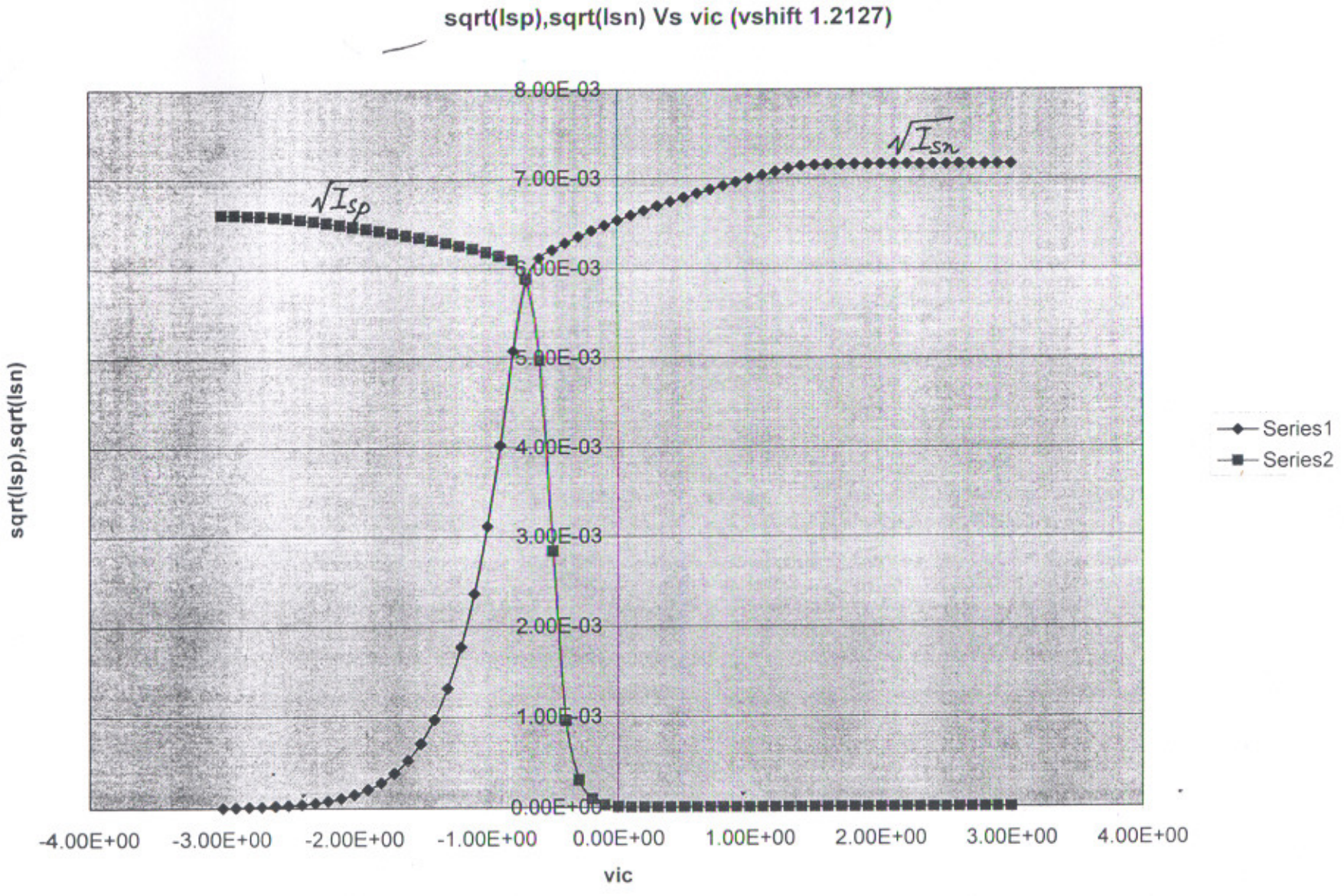

parall const gm6vic2
i(M2, 2)
i(M19, 15)
i(Vdd, 15)
Ampere (uA)
Voltage (V)


parall const gm6vic2
Voltage (V,dB)
Frequency (Hz)

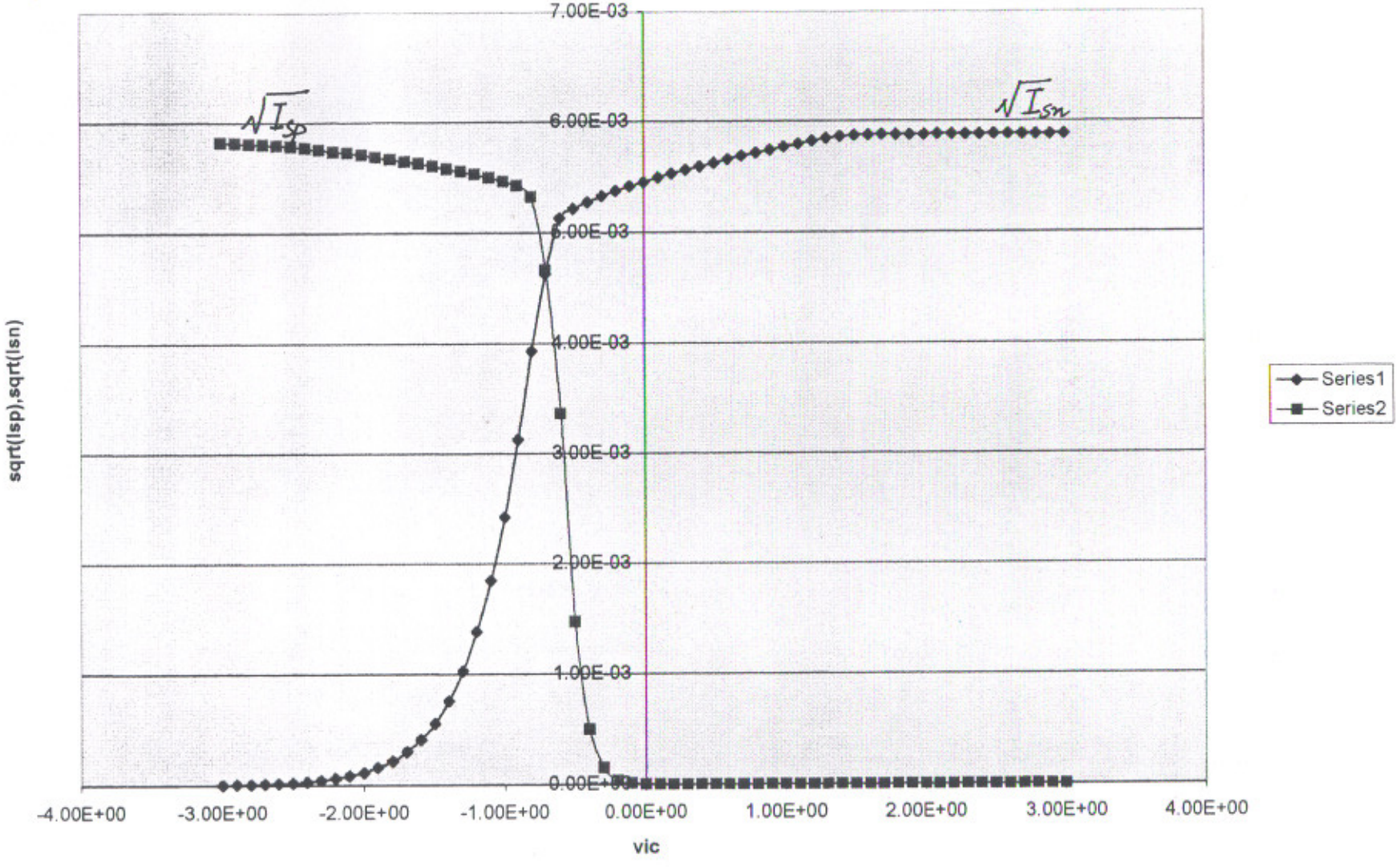
1b

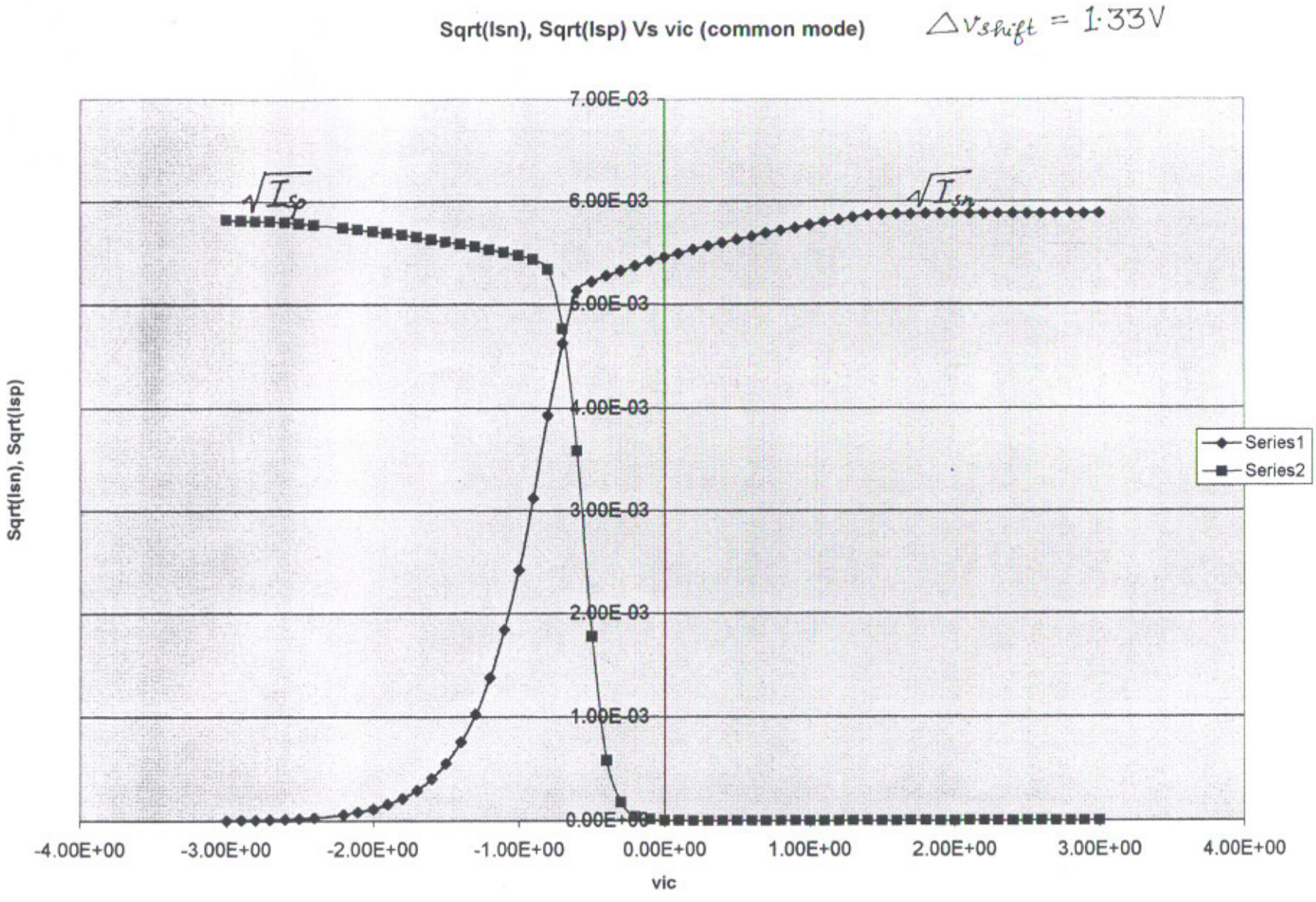

parall const gm6vic3
i (M2, 2)
i (M19, 15)
i (Vdd, 15)
Ampere (uA)
Voltage (V)

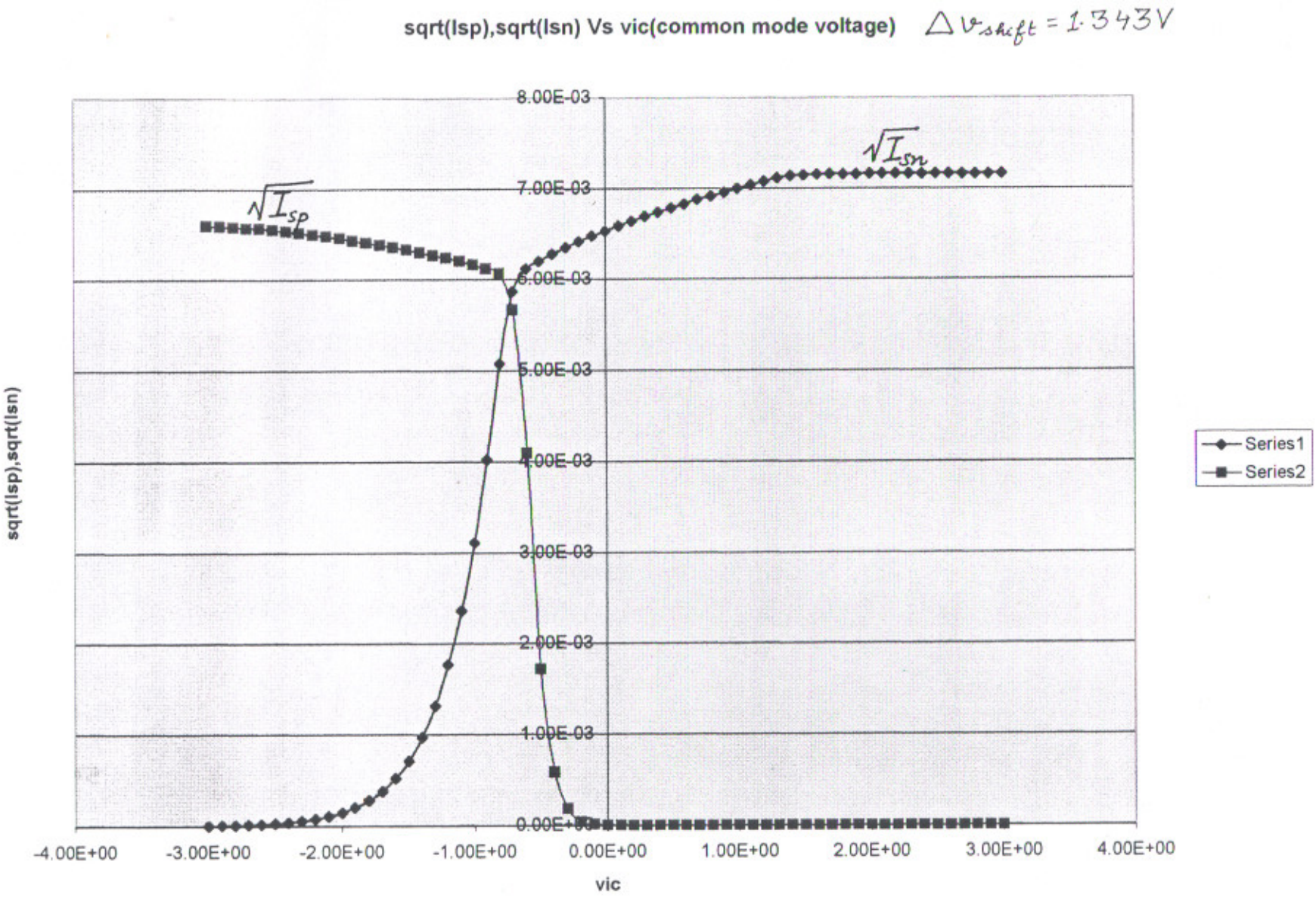

parall const gm6vic3
Voltage (V,dB)

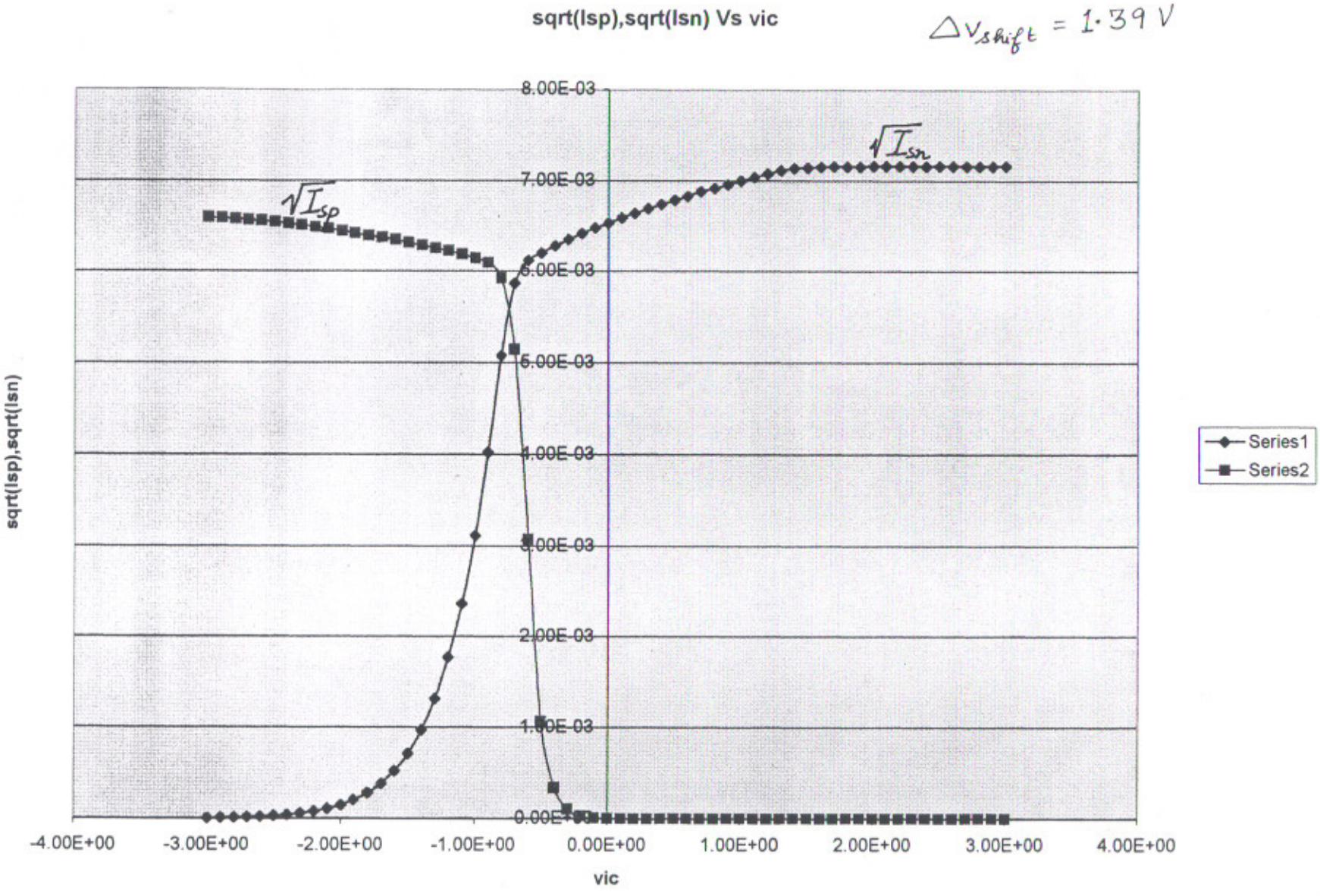

sqrt(Isp),sqrt(Isn) Vs vic (vshift 1.2127)
sqrt(Isp),sqrt(Isn)
vic
8.00E-03
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
-4.00E+00
-3.00E+00
-2.00E+00
-1.00E+00
0.00E+00
1.00E+00
2.00E+00
3.00E+00
4.00E+00
√Isp
√Isn
Series1
Series2

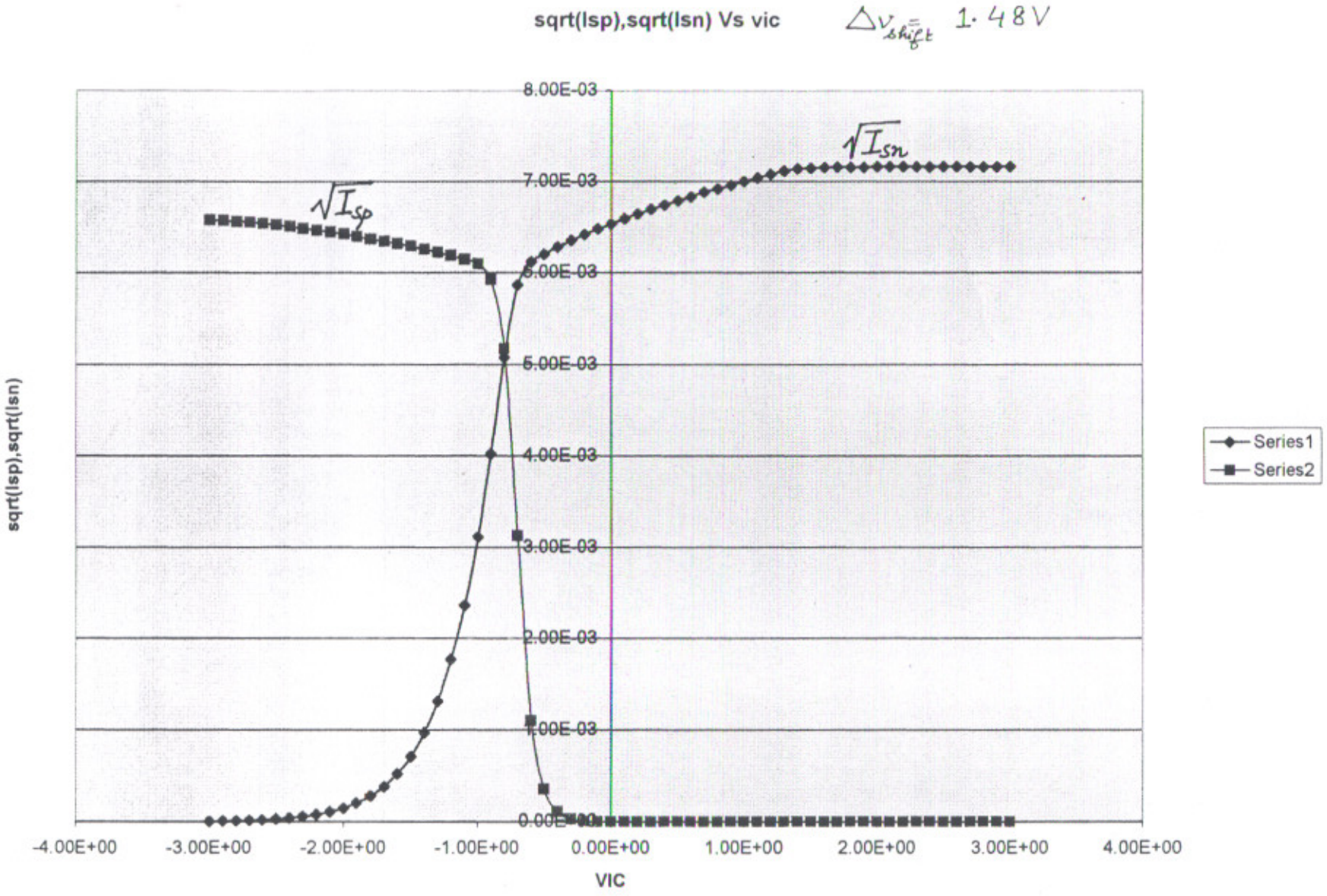
sqrt(Isp),sqrt(Isn) Vs vic(common mode) $\Delta V_{shift} = 1.32V$

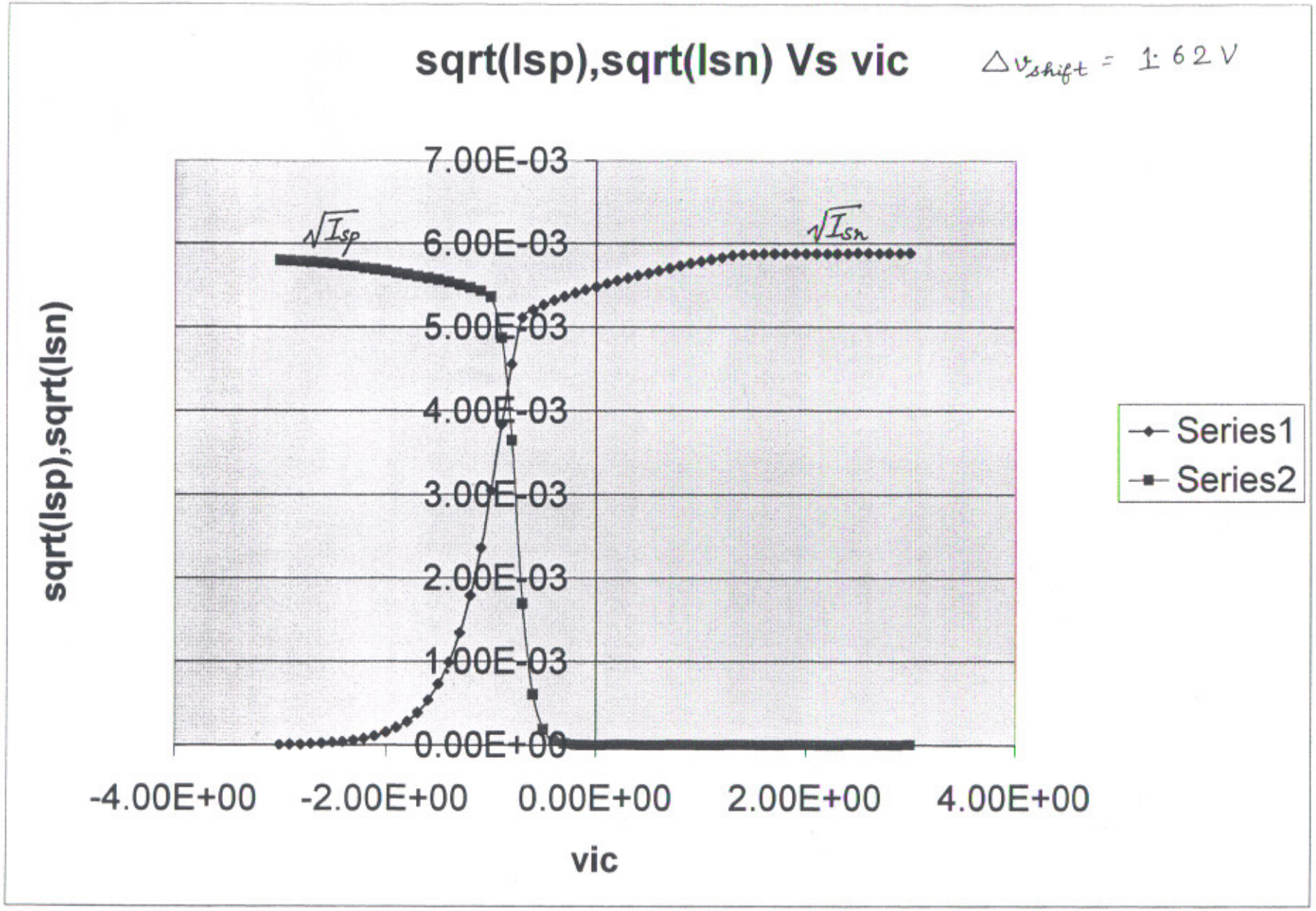


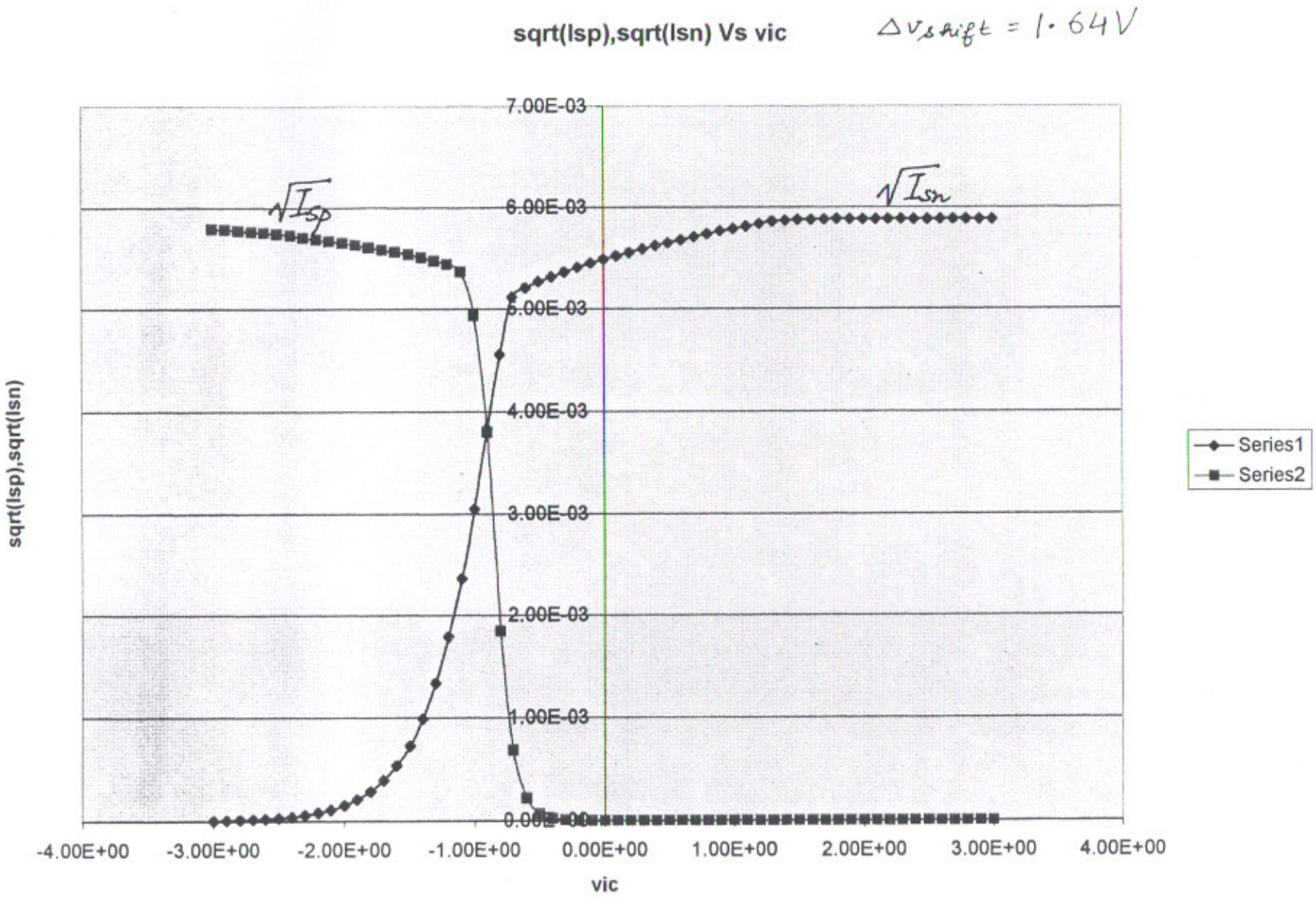

Sqrt(Isn), Sqrt(Isp) Vs vic (common mode)
$\Delta V_{shift} = 1.33V$
$\sqrt{I_{sp}}$
$\sqrt{I_{sn}}$
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
Sqrt(Isn), Sqrt(Isp)
-4.00E+00
-3.00E+00
-2.00E+00
-1.00E+00
0.00E+00
1.00E+00
2.00E+00
3.00E+00
4.00E+00
vic
Series1
Series2

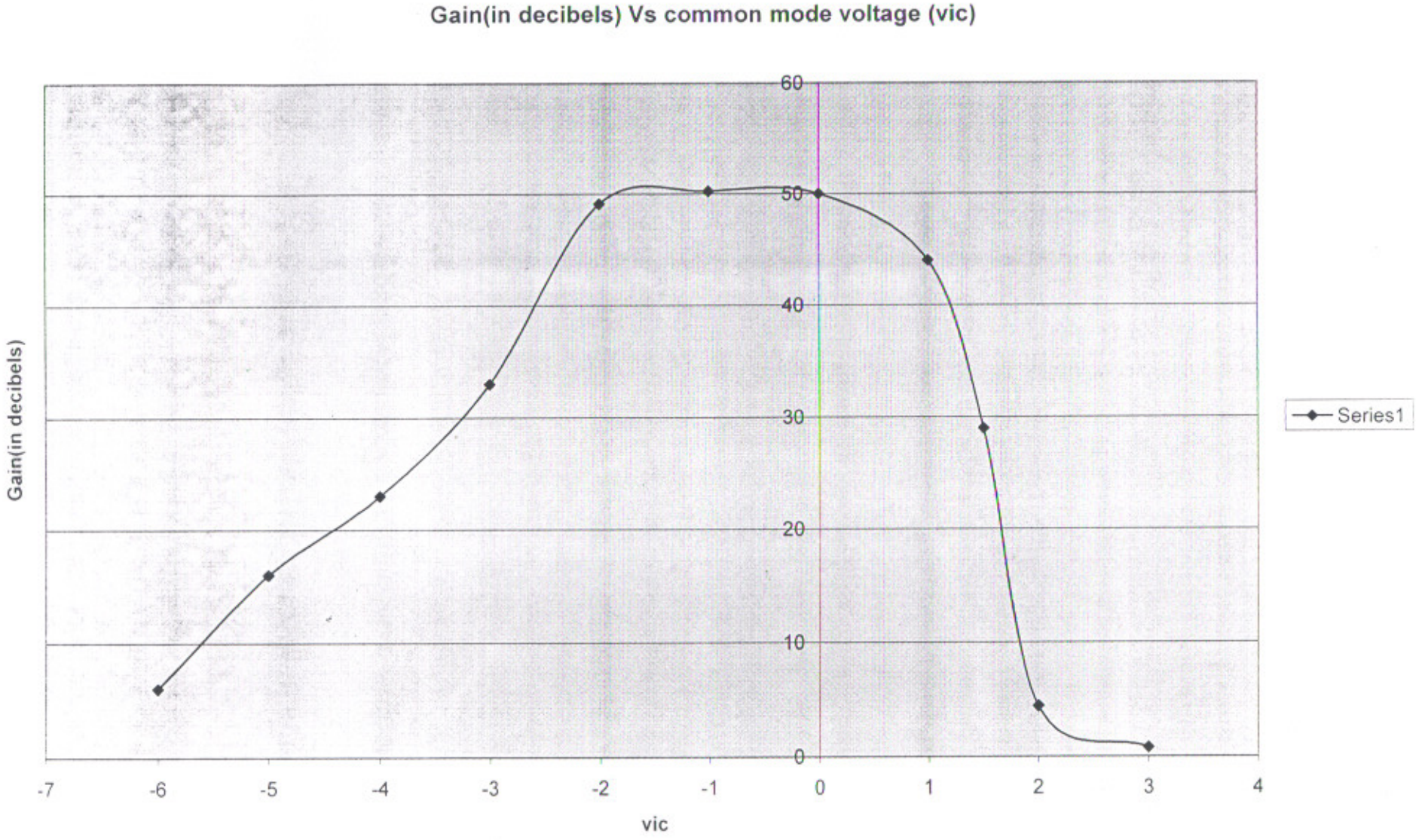

sqrt(Isp),sqrt(Isn) Vs vic(common mode voltage)
$\Delta V_{shift} = 1.343V$
$\sqrt{I_{sp}}$
$\sqrt{I_{sn}}$
8.00E-03
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
-4.00E+00
-3.00E+00
-2.00E+00
-1.00E+00
0.00E+00
1.00E+00
2.00E+00
3.00E+00
4.00E+00
sqrt(Isp),sqrt(Isn)
vic
Series1
Series2


sqrt(Isp),sqrt(Isn) Vs vic
$\Delta V_{shift} = 1.39\ V$
$\sqrt{I_{sp}}$
$\sqrt{I_{sn}}$
8.00E-03
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
sqrt(Isp),sqrt(Isn)
-4.00E+00
-3.00E+00
-2.00E+00
-1.00E+00
0.00E+00
1.00E+00
2.00E+00
3.00E+00
4.00E+00
vic
Series1
Series2

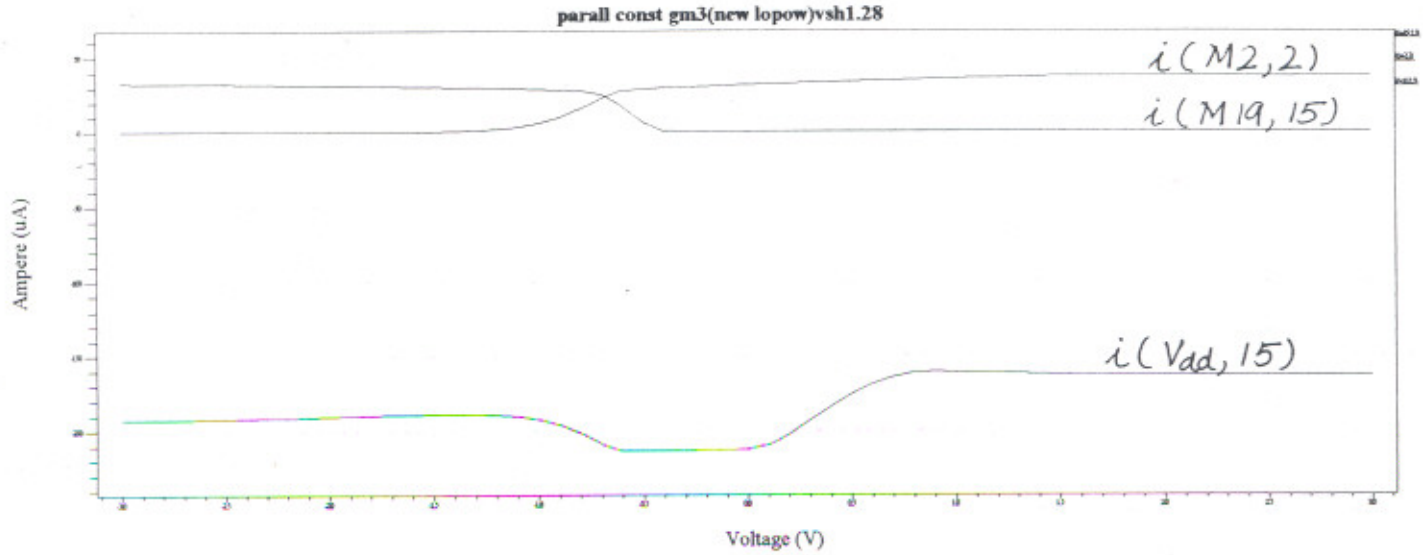

sqrt(Isp),sqrt(Isn) Vs vic
$\triangle V_{shift} = 1.48V$
$\sqrt{I_{sp}}$
$\sqrt{I_{sn}}$
8.00E-03
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
sqrt(Isp),sqrt(Isn)
-4.00E+00
-3.00E+00
-2.00E+00
-1.00E+00
0.00E+00
1.00E+00
2.00E+00
3.00E+00
4.00E+00
VIC
Series1
Series2

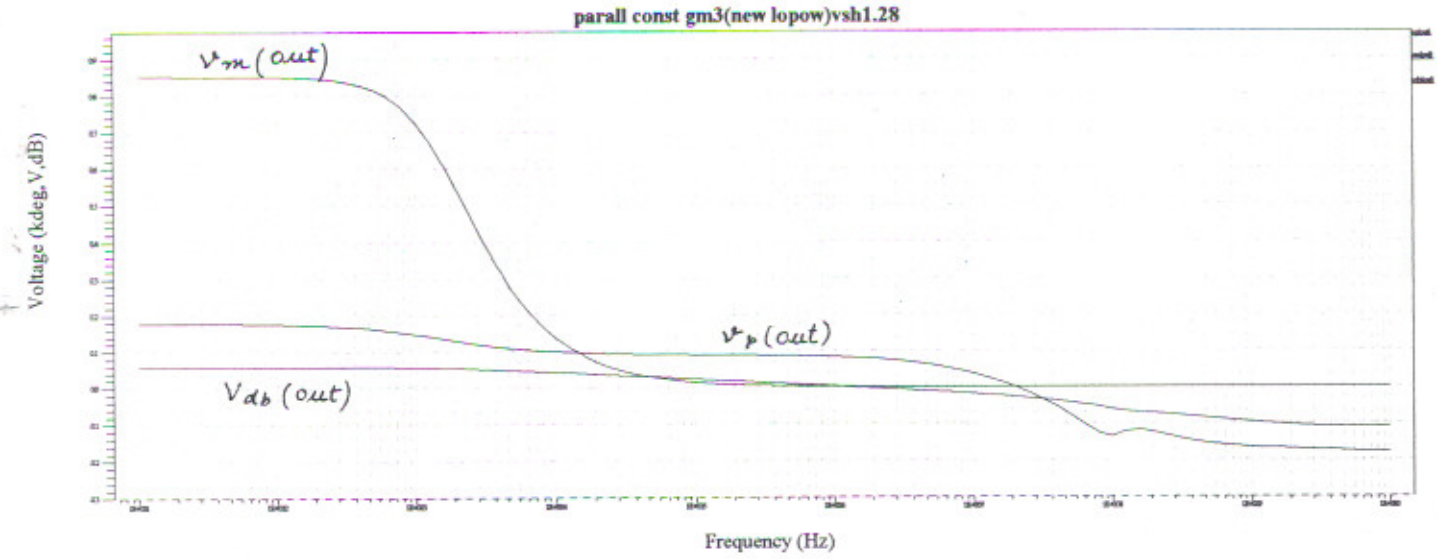

sqrt(Isp),sqrt(Isn) Vs vic
Δv_{shift} = 1.62 V
$\sqrt{I_{sp}}$
$\sqrt{I_{sn}}$
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
sqrt(Isp),sqrt(Isn)
-4.00E+00
-2.00E+00
0.00E+00
2.00E+00
4.00E+00
vic
Series1
Series2

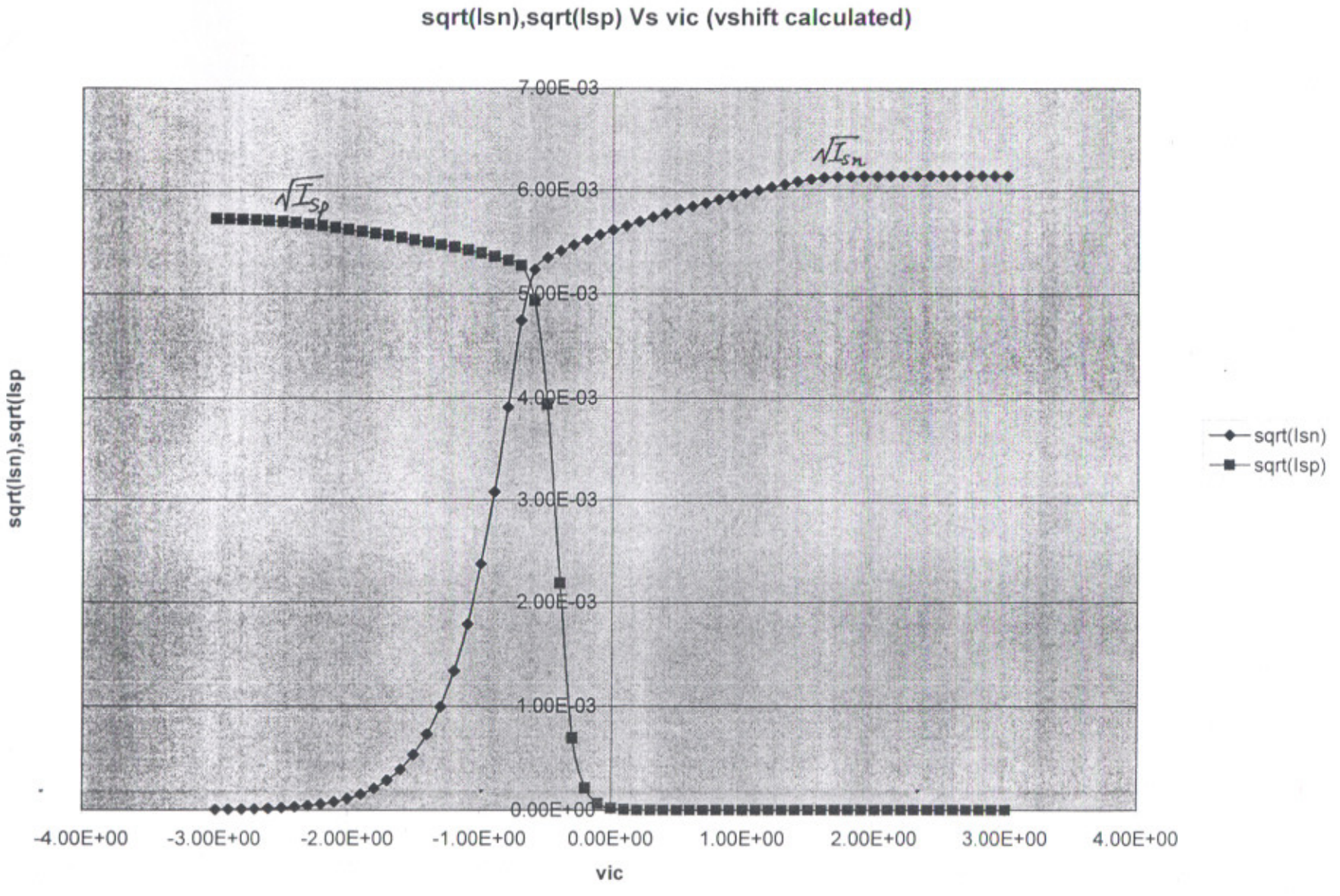

sqrt(Isp),sqrt(Isn) Vs vic
$\Delta V_{shift} = 1.64V$
$\sqrt{I_{sp}}$
$\sqrt{I_{sn}}$
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
sqrt(Isp),sqrt(Isn)
-4.00E+00
-3.00E+00
-2.00E+00
-1.00E+00
0.00E+00
1.00E+00
2.00E+00
3.00E+00
4.00E+00
vic
Series1
Series2

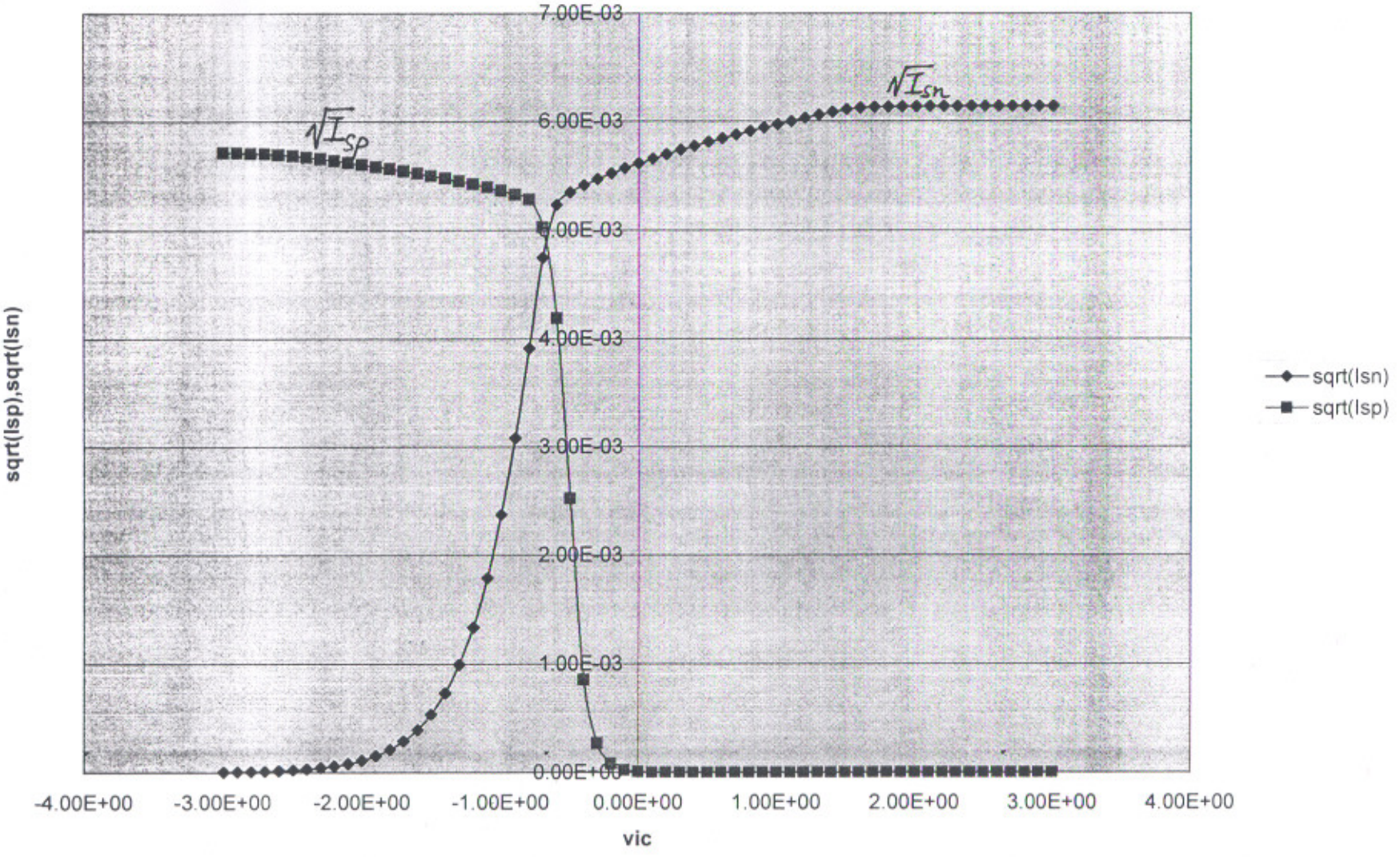

Gain(in decibels) Vs common mode voltage (vic)
Gain(in decibels)
60
50
40
30
20
10
0
-7
-6
-5
-4
-3
-2
-1
0
1
2
3
4
vic
Series1

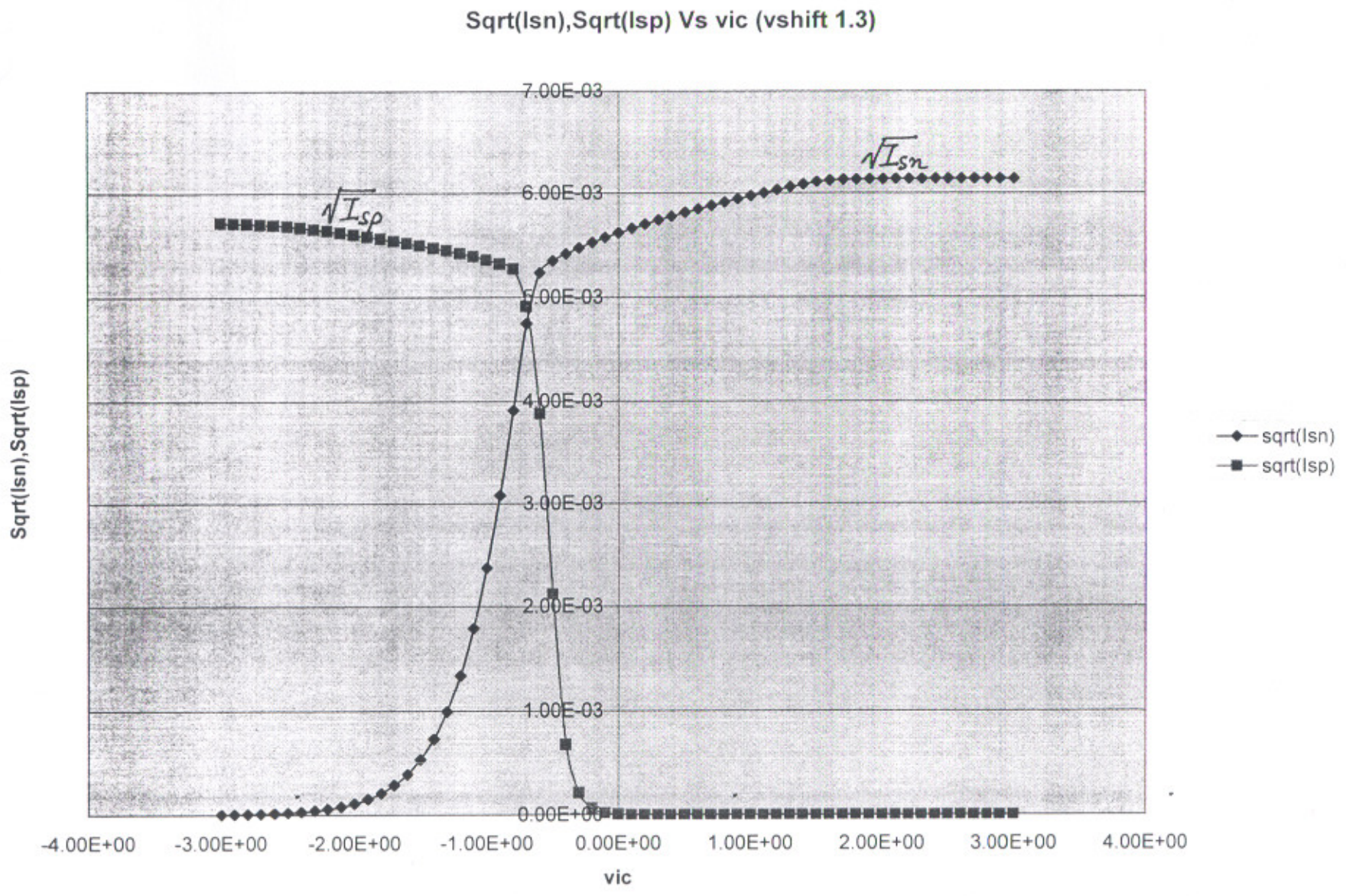
```
 * SPICE netlist written by S-Edit Win32 6.02
* Written on Feb 5, 2003 at 23:27:41

* Waveform probing commands
.probe
.options probefilename="sedit.dat"
+ probesdbfile="C:\sush\parall const gm.sdb"
+ probetopmodule="parall const gm"

* Main circuit: parall const gm
C1 out Gnd 10pF

M2 2 12 14 14 NMOS L=2u W=47.418u AD=66p PD=24u AS=66p PS=24u
*folcasco
M4 5 12 14 14 NMOS L=2u W=47.418u AD=66p PD=24u AS=66p PS=24u
M5 6 12 14 14 NMOS L=2u W=47.418u AD=66p PD=24u AS=66p PS=24u
M6 7 Gnd 5 5 NMOS L=2u W=23.708u AD=66p PD=24u AS=66p PS=24u
M7 out Gnd 6 6 NMOS L=2u W=23.708u AD=66p PD=24u AS=66p PS=24u
*ip tx
M3 3 v- 2 2 NMOS L=2u W=42.1494u AD=66p PD=24u AS=66p PS=24u
M8 1 v+ 2 2 NMOS L=2u W=42.1494u AD=66p PD=24u AS=66p PS=24u
M9 12 12 14 14 NMOS L=2u W=47.418u AD=66p PD=24u AS=66p PS=24u

M13 6 3 15 15 PMOS L=2u W=700u AD=66p PD=24u AS=66p PS=24u
M14 1 1 15 15 PMOS L=2u W=700u AD=66p PD=24u AS=66p PS=24u
*folcasco
M12 9 7 15 15 PMOS L=2u W=36.4326u AD=66p PD=24u AS=66p PS=24u
M15 8 7 15 15 PMOS L=2u W=36.4326u AD=66p PD=24u AS=66p PS=24u
M16 7 Gnd 8 8 PMOS L=2u W=56.926u AD=66p PD=24u AS=66p PS=24u
M17 out Gnd 9 9 PMOS L=2u W=56.926u AD=66p PD=24u AS=66p PS=24u

M18 10 13 15 15 PMOS L=2u W=113.852u AD=66p PD=24u AS=66p PS=24u
M19 22 13 15 15 PMOS L=2u W=113.852u AD=66p PD=24u AS=66p PS=24u
M21 11 13 15 15 PMOS L=2u W=113.852u AD=66p PD=24u AS=66p PS=24u
M20 3 3 15 15 PMOS L=2u W=700u AD=66p PD=24u AS=66p PS=24u

M10 14 v+ 10 10 PMOS L=2u W=11.847244u AD=66p PD=24u AS=66p PS=24u
M11 14 v- 11 11 PMOS L=2u W=11.847244u AD=66p PD=24u AS=66p PS=24u
M25 5 1 15 15 PMOS L=2u W=700u AD=66p PD=24u AS=66p PS=24u
M22 13 13 15 15 PMOS L=2u W=113.852u AD=66p PD=24u AS=66p PS=24u

*ip tx
M23 5  11  22 22 PMOS L=2u W=101.16u AD=66p PD=24u AS=66p PS=24u
M24 6  10  22 22 PMOS L=2u W=101.16u AD=66p PD=24u AS=66p PS=24u

R26 13 14 72K TC=0.0, 0.0
R27 15 12 68.3333K TC=0.0, 0.0
vin v+ v- 0.0 AC 0.5 0.0
vdd 15 Gnd 1.5
vss 14 Gnd -1.5
.print dc i(vdd,15)
.print dc i(m2,2)
.print dc i(m19,15)

v31 v- Gnd 0
.dc lin v31 -3 3 0.1

.include "C:\Program Files\Tanner EDA\T-Spice Pro v6.02\models\ml2_125.md"
.op
.ac dec 10 10 10000MEG
.print ac vdb(out)
.print ac vm(out)
```

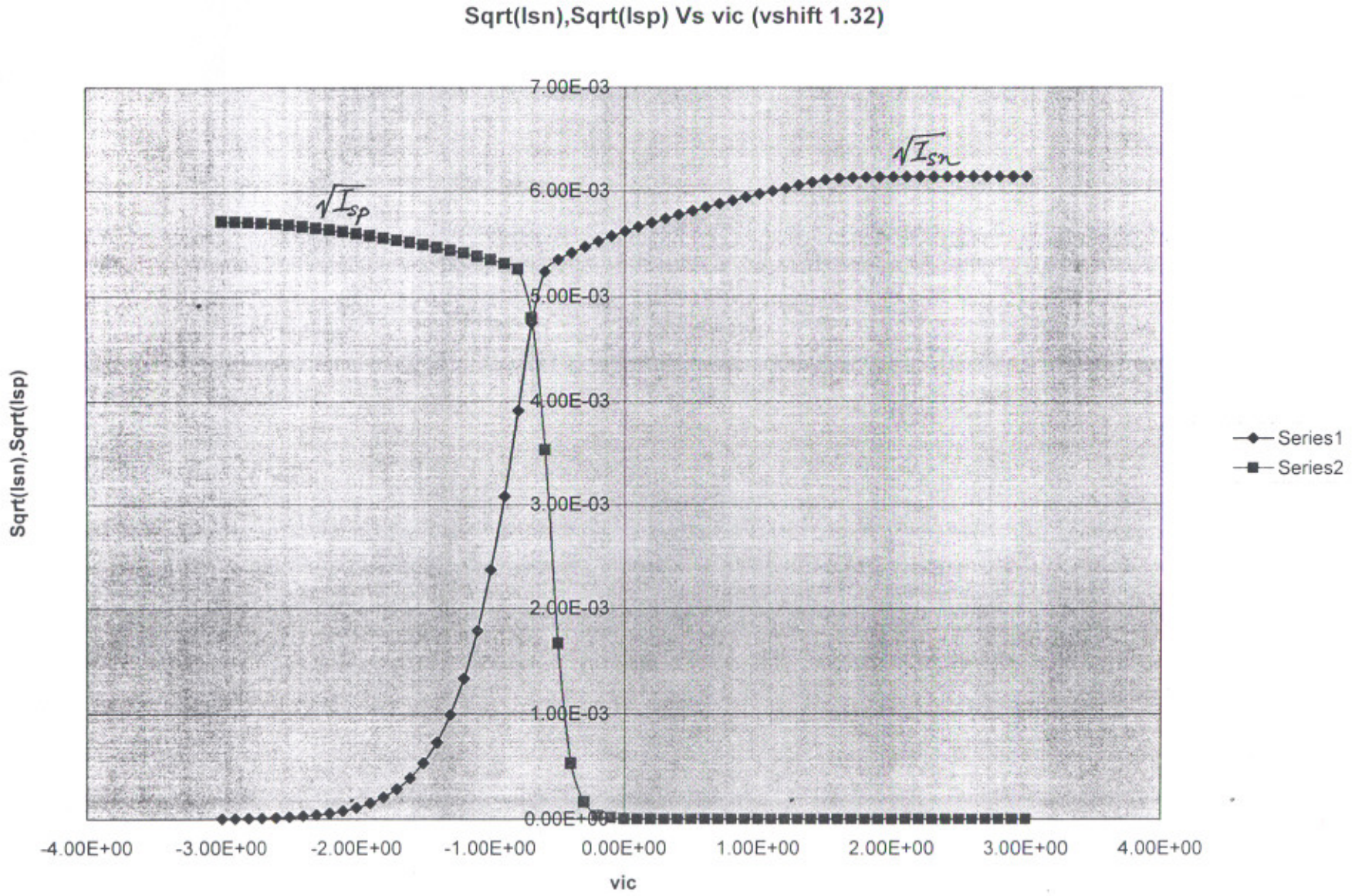

parall const gm3(new lopow)vsh1.28
i(M2,2)
i(M19,15)
i(Vdd,15)
Ampere (uA)
Voltage (V)

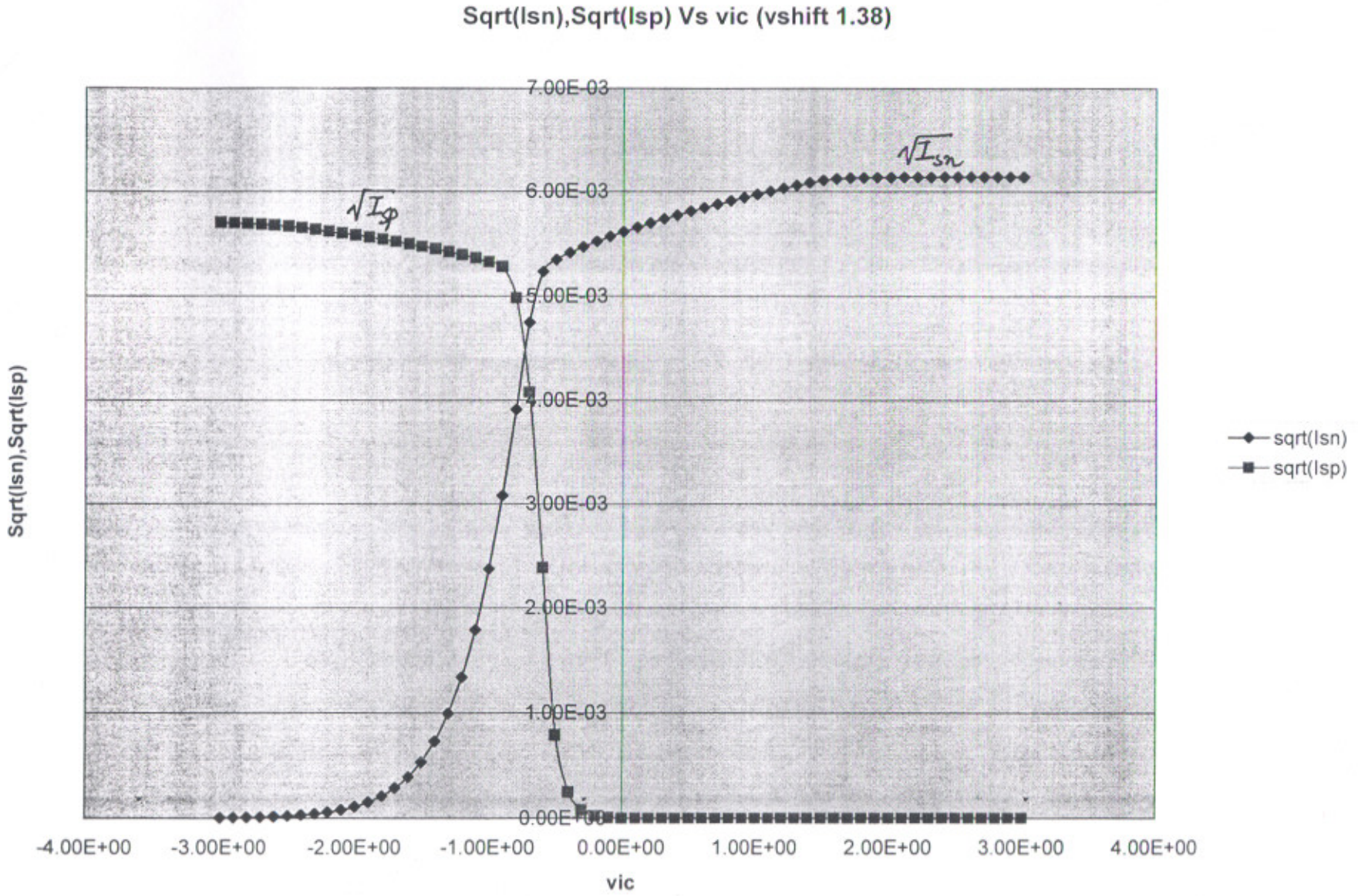

parall const gm3(new lopow)vsh1.28
Vm(out)
Vp(out)
Vdb(out)
Voltage (kdeg,V,dB)
Frequency (Hz)

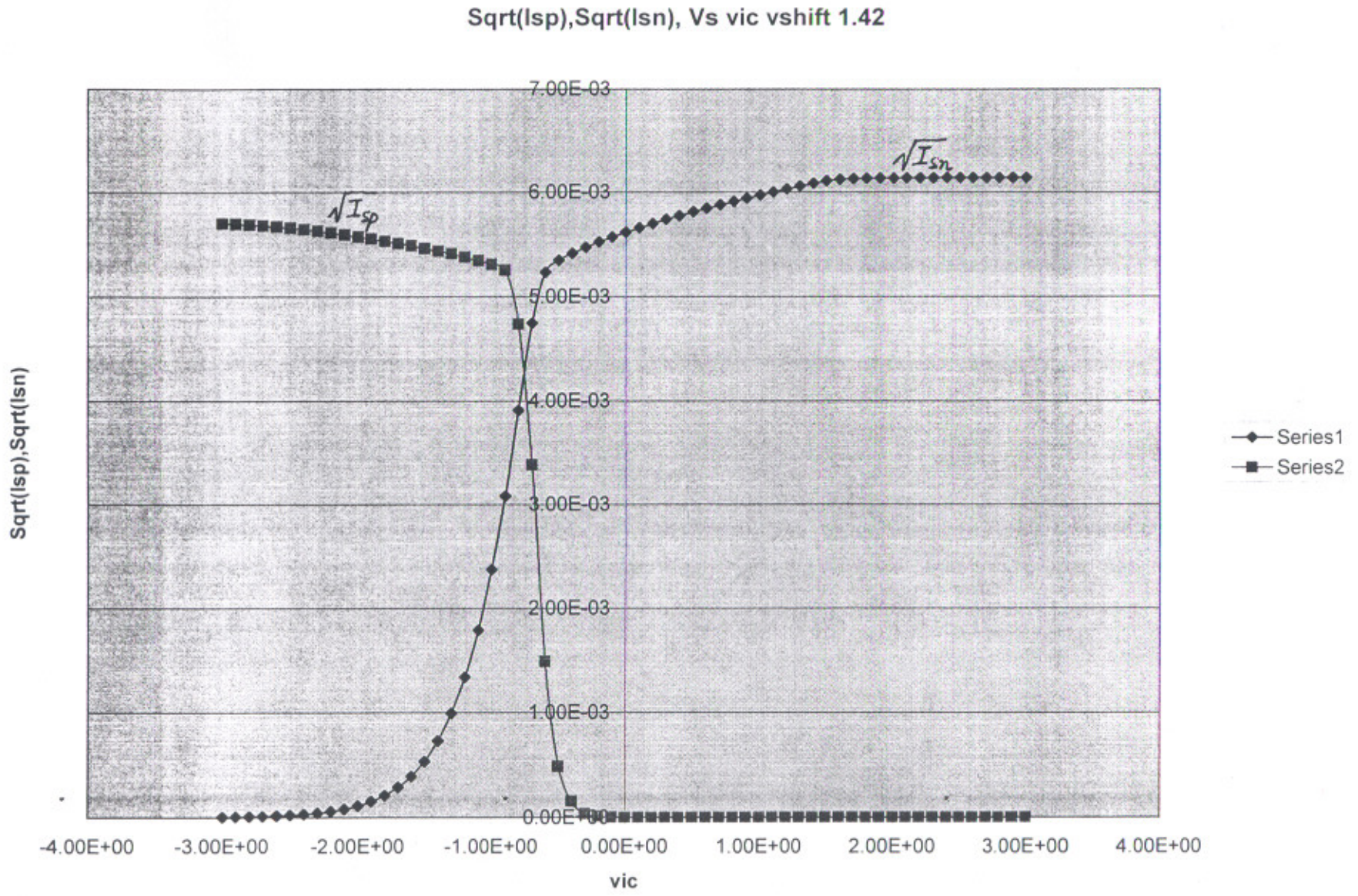

sqrt(Isn),sqrt(Isp) Vs vic (vshift calculated)
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
sqrt(Isn),sqrt(Isp
-4.00E+00
-3.00E+00
-2.00E+00
-1.00E+00
0.00E+00
1.00E+00
2.00E+00
3.00E+00
4.00E+00
vic
sqrt(Isn)
sqrt(Isp)

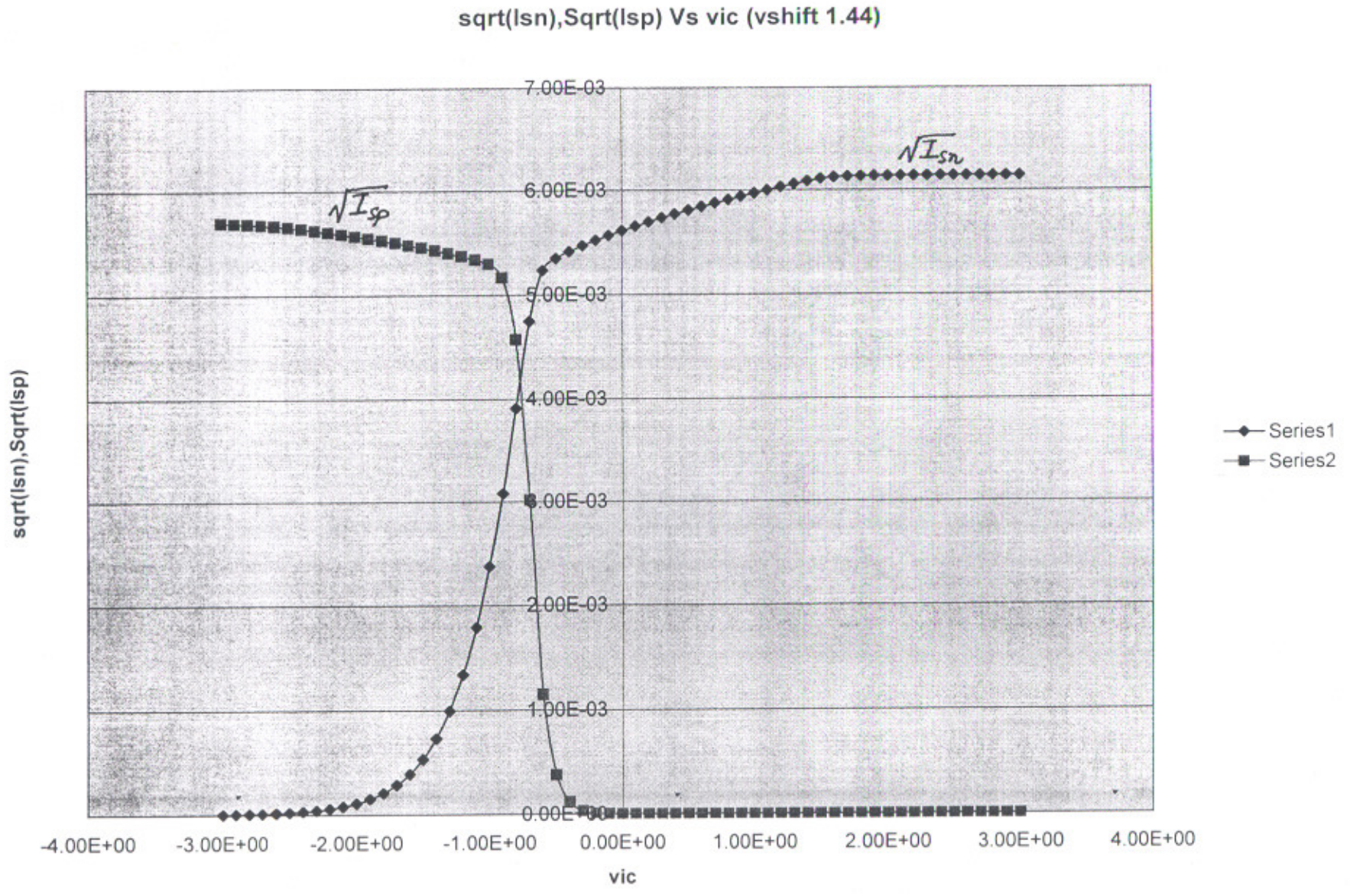

sqrt(Isp),sqrt(Isn) Vs vic (vshift 1.28)
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
sqrt(Isp),sqrt(Isn)
-4.00E+00
-3.00E+00
-2.00E+00
-1.00E+00
0.00E+00
1.00E+00
2.00E+00
3.00E+00
4.00E+00
vic
sqrt(Isn)
sqrt(Isp)

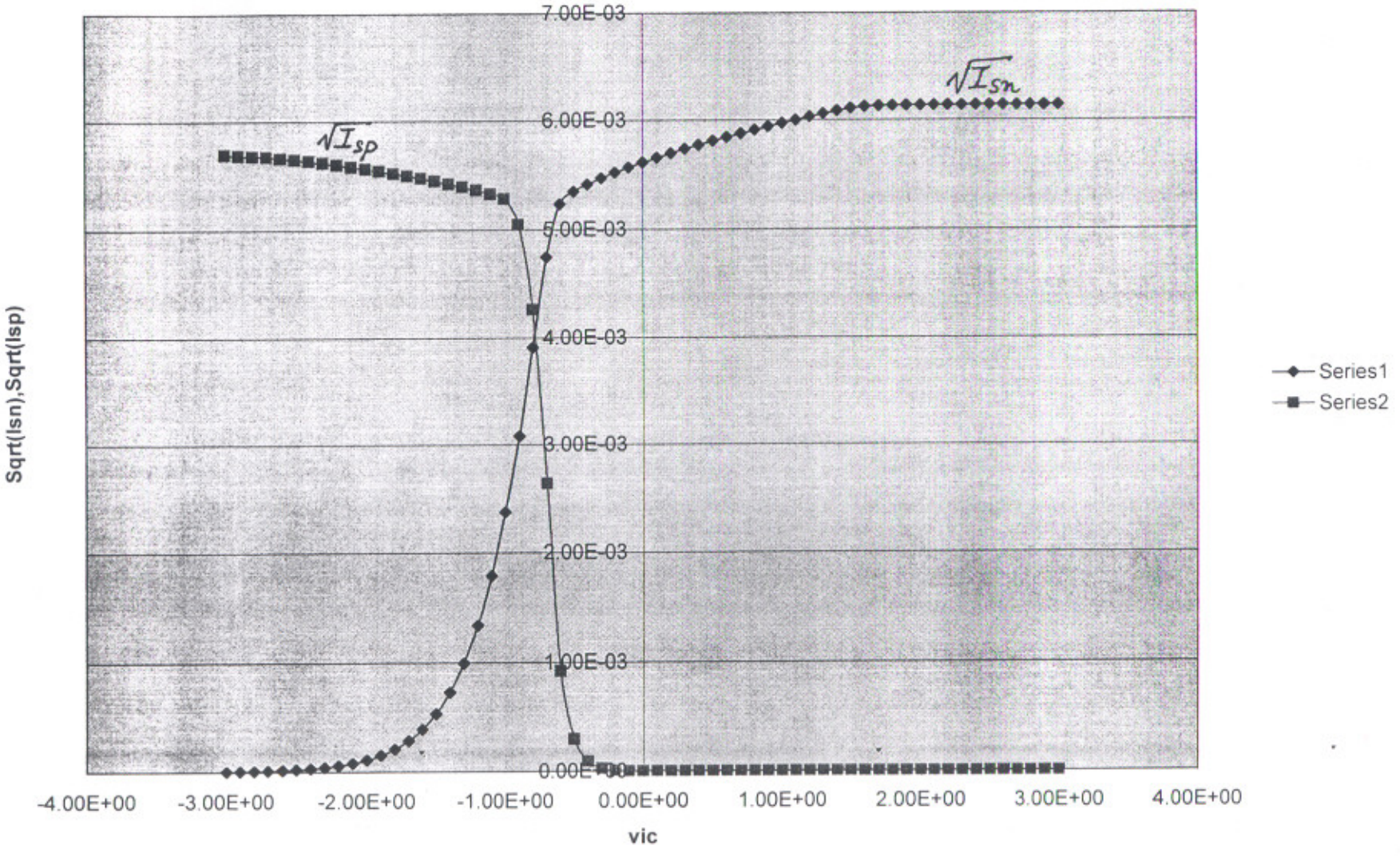

Sqrt(Isn),Sqrt(Isp) Vs vic (vshift 1.3)
Sqrt(Isn),Sqrt(Isp)
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
-4.00E+00
-3.00E+00
-2.00E+00
-1.00E+00
0.00E+00
1.00E+00
2.00E+00
3.00E+00
4.00E+00
vic
sqrt(Isn)
sqrt(Isp)


Sqrt(Isn),Sqrt(Isp) Vs vic (vshift 1.32)
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
Sqrt(Isn),Sqrt(Isp)
-4.00E+00
-3.00E+00
-2.00E+00
-1.00E+00
0.00E+00
1.00E+00
2.00E+00
3.00E+00
4.00E+00
vic
√Isp
√Isn
Series1
Series2


Sqrt(Isn),Sqrt(Isp) Vs vic (vshift 1.38)
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
Sqrt(Isn),Sqrt(Isp)
-4.00E+00
-3.00E+00
-2.00E+00
-1.00E+00
0.00E+00
1.00E+00
2.00E+00
3.00E+00
4.00E+00
vic
sqrt(Isn)
sqrt(Isp)


Sqrt(Isp),Sqrt(Isn), Vs vic vshift 1.42
Sqrt(Isp),Sqrt(Isn)
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
-4.00E+00
-3.00E+00
-2.00E+00
-1.00E+00
0.00E+00
1.00E+00
2.00E+00
3.00E+00
4.00E+00
vic
√Isp
√Isn
Series1
Series2


sqrt(Isn),Sqrt(Isp) Vs vic (vshift 1.44)
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
sqrt(Isn),Sqrt(Isp)
-4.00E+00
-3.00E+00
-2.00E+00
-1.00E+00
0.00E+00
1.00E+00
2.00E+00
3.00E+00
4.00E+00
vic
√Isp
√Isn
Series1
Series2


Sqrt(Isn),Sqrt(Isp) Vs vic (vshift 1.46)
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
0.00E+00
√Isp
√Isn
Sqrt(Isn),Sqrt(Isp)
-4.00E+00
-3.00E+00
-2.00E+00
-1.00E+00
0.00E+00
1.00E+00
2.00E+00
3.00E+00
4.00E+00
vic
Series1
Series2

CONCLUSIONS

An economical but efficient technique to achieve a constant g_m rail to rail complimentary NP differential input stage has been applied and we have demonstrated that DC level shifters can be used to overlap the transition region of the complimentary pairs of differential amplifier with the proper amount DC level shift the variation of the g_m is within 5%.

A new voltage input stage has been also described which utilizes the body effect to modulate the depletion mode n-channel input voltage followers which levels shift the input voltage to a bulk driven p-channel differential pair. Results [5] [3] demonstrate that g_m variation can be restricted to be within $\pm$ 4% with improved CMRR and the frequency response namely the GB (Gain Bandwidth).

Compared to the previously discussed rail-to-rail input architectures, the depletion-mode differential pair [5] [3] is also an elegant approach supplied head on by a 0.9V battery. However, to operate properly with a 0.9V supply voltage, the use of the n-channel depletion-mode differential pair places constraints upon the intrinsic threshold voltage and the bulk or well doping concentration of the n-channel depletion-mode transistors. Although as we operate on bulk driven devices the transconductance decreases to about one tenth as compared to above gate driven devices.

A deign Procedure for various configurations were presented starting from the conventional two stage differential Amplifier to the constant Transconductance parallel Input differential Op-Amp. The main constraints for the design were primarily as follows:

A_v. The Amplification Factor

ICMR. The Input common mode range

P_d. The power Dissipation

I optimized on these parameters where the value for upper range for the ICMR obtained was excellent, having low power dissipation while still maintaining a reasonable Amplification. Various other parameters have not been optimized for, such as PSRR, CMRR and further Amplification can also be raised.

The constant Transconductance stage having DC level shift presents itself as a simple and a elegant design to operate on wider common mode ranges still dissipating almost same power as a Conventional two stage amplifier.

References

1. Allen E.Philip, Holeberg R.Douglas, "CMOS Analog Circuit Design" Oxford University Press, London, 2002.
2. Hogervorst .R, Tero .J.P, R.G.H. Eschauzier, J.H. Huijsing, "A Compact Power-Efficient 3 V CMOS Rail-to-Rail Input/Output Operational Amplifier for VLSI Cell Libraries", *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 1505-1513, Dec. 1994.
3. J.H. Huijsing, D. Linebarger, "Low-voltage operational amplifier with rail-to-rail input and output ranges", *IEEE Journal of Solid-State Circuits*, vol. SC-20, pp. 1144-1150, Dec. 1985.
4. Lehmann T., Cassia M., "One Volt Power Supply Cascade Amplifier", *IEEE Journal Of Solid State Circuits*, Volume 36, No.7, July 2001.
5. Stockstad Troy, Yoshizawa Hirokazu, "A 0.9 Volt, 0.5 Micro Ampere Rail-To-Rail CMOS Op-Amplifier", *IEEE Journal Of Solid State Circuits*, Volume 37, No.3, March 2002.
6. Tsividis.Yannis "Operation and Modelling of the C-MOS Transistor" Mc Graw Publishing 1997.
7. Wang Minsheng, Mayhug, Terry L, Embabi, Sherif H. K., "Constant G_m Rail-To-Rail CMOS Op-Amp Input Stage With Overlapped Transition Regions", *IEEE Journal Of Solid State Circuits*, Volume 34, No.2, February 1999.