# UPIO Delayline Delay Extraction Using ELDO

*Project report submitted in partial fulfilment of the requirement for the*

*Award of the Degree of*

**Master of Technology**

in VLSI Design

Submitted By

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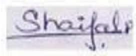
## Declaration

I, **Shaifali Yadav**, hereby declare that the project report entitled "**UPIO Delayline Delay Extraction Using ELDO**" in partial fulfillment for the award of the degree of Master of Technology in VLSI Design to the Department of Electronics and Communication, Thapar Institute of Engineering and Technology is an original record of the work carried out by me under the guidance and supervision of **Mr. Sanjay Kumar(Group Manager)**, **Dr. Faseehuddin (Assistant Professor) & Dr.Amit Kumar Kohli (Associate Professor)** from July-2024 to May-2025. This report has not been submitted toany other university or institution for the award of any degree or diploma.



Date:22/06/2025

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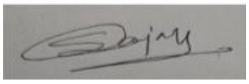
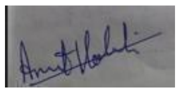
| <br>Mr. Sanjay Kumar<br>Group Manager<br>ST Microelectronics Pvt Limited ,Greater Noida<br>Date:22/06/2025 | <br>Dr. Mohd. Faseehuddin (Supervisor)<br>Assistant Professor<br>Department of Electronics and Communication Engineering, Thapar Institute of Engineering & Technology, Patiala<br>Date:22/06/2025<br><br><br>Dr. Amit Kumar Kohli (Co-Supervisor)<br>Associate Professor<br>Department of Electronics and Communication Engineering, Thapar Institute of Engineering & Technology, Patiala<br>Date:22/06/2025 |

# Internship Certificate

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This is to certify that **Shaifali YADAV** has undergone internship in our **MDG** Group from **June 12, 2024 to May 30, 2025**. and has successfully completed the project on: **Cheetah , Mustang**

During the internship period, Shaifali was found to be sincere and professional in conduct.

We wish her all the best for the future endeavors.

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I wish to express my thanks to all my team members of the St microelectronics who were helpful in many ways for the completion of my project.

## Abstract

This report focuses on the extraction of delay in Universal Programmable Input/Output (UPIO) Delayline circuits using Eldo, a high-precision SPICE simulator. The accurate determination of delay characteristics in UPIO Delaylines is essential for the performance and reliability of high-speed digital circuits.

The study begins with an overview of the importance of delay lines in digital circuit design and the specific applications of UPIO Delaylines. It then outlines the theoretical foundations of delay extraction, emphasizing the critical parameters and metrics that influence delay performance.

The methodology section details the simulation setup, including the configuration of the Eldo simulator, the design of test benches, and the simulation conditions. It provides a step-by-step guide for setting up the Eldo environment, running simulations, and extracting delay data to ensure precision and reproducibility.
Simulation results are presented and analyzed, illustrating the delay characteristics of the UPIO Delayline under various operating conditions. The report compares the simulated results with theoretical predictions and discusses any observed discrepancies.

In this report, we present a novel method for extracting resistance values in electronic circuits using a custom routing approach. The accurate extraction of resistance values is crucial for ensuring the performance and reliability of electronic designs, particularly in high-speed and high-frequency applications where precise impedance control is necessary.

Our method involves the development of a custom routing algorithm that not only optimizes the physical layout of the circuit but also accurately calculates the resistance values of the interconnects. The algorithm takes into account various factors such as wire length, cross-sectional area, and material properties to compute the resistance. Additionally, it integrates seamlessly with existing electronic design automation (EDA) tools, providing a comprehensive solution for designers.

## Table of contents

**S. No. Chapter Name Page No.**

## List of Figures

**Figure Title** **Page No.**

# Chapter-1
# Introduction

Delay extraction is a critical process in the design and analysis of Very Large Scale Integration (VLSI) circuits. It involves determining the time delays associated with signal propagation through various paths in a circuit. Accurate delay extraction is essential for ensuring that the circuit meets its timing requirements, which is crucial for the overall performance and reliability of the system.

## 1.1 Importance of Delay Extraction

In VLSI design, timing analysis is performed to ensure that signals propagate through the circuit within the required time constraints. Delay extraction plays a pivotal role in this process by providing accurate estimates of the delays introduced by various circuit elements, interconnects, and parasitics. The key reasons for the importance of delay extraction include:

- **Timing Verification**: Ensures that the circuit meets its timing specifications, preventing setup and hold time violations.
- **Performance Optimization**: Helps in optimizing the design for speed and efficiency by identifying critical paths and bottlenecks.
- **Reliability**: Enhances the reliability of the circuit by ensuring that timing-related issues are addressed during the design phase.
- **Power Consumption**: Aids in power analysis by providing insights into the timing behavior of different components, enabling power optimization.
- **Challenges in Delay Extraction**
- Delay extraction in VLSI design presents several challenges, especially as technology scales down to deep submicron and nanometer regimes:
- **Complexity**: Modern VLSI circuits are highly complex, with millions of transistors and interconnects, making delay extraction computationally intensive.
- **Parasitic Effects**: Accurate modeling of parasitic capacitances, resistances, and inductances is crucial for precise delay extraction.
- **Process Variations**: Variations in the manufacturing process can lead to discrepancies in delay estimates, necessitating robust extraction methods.
- **Signal Integrity**: Crosstalk and noise can affect signal propagation, complicating the delay extraction process.

## 1.2 What is an ELDO?

Eldo Platform delivers the required SPICE accuracy and performance to design and verify complex automotive IC designs using the BCD technology and to address their design and verification challenges efficiently and in a timely manner.

Reliability verification is made possible with Eldo's industry-proven advanced aging simulations to predict reliability issues due to circuit degradation, electrothermal simulation to analyze thermal impact due to power dissipation, and safe operating area simulation and analysis to detect dangerous operating condition violations over the lifetime of the IC.


***Fig1.1. Eldo platform Advanced verification for analog-centric ICs***
***Source: Eldo Platform | Siemens Software***

**1.3 Role of Eldo in Delay Extraction**

Eldo, being a SPICE-based simulator, provides several features that make it suitable for delay extraction in VLSI circuits:

- **High Precision:** Eldo offers high-precision simulation capabilities, ensuring accurate delay estimates.
- **Advanced Modeling:** Supports advanced device models and parasitic extraction, essential for accurate delay analysis.
- **Mixed-Signal Simulation:** Capable of simulating both analog and digital components, making it versatile for mixed-signal VLSI designs.
- **User-Friendly Interface:** Provides a user-friendly interface and scripting capabilities, facilitating efficient setup and execution of simulations.

**1.4 Required Files in ELDO:**

- **<file>.cir:**The main Eldo control file, containing circuit netlist, stimulus and simulation control commands.
- **<file>.chi:** SPICE compatible output log file containing ASCII data, including results and error messages.
- **<file>.wdb:** A binary output file for mixed-signal JWDB format files. This is always generated by

default. Viewed with the EZwave waveform viewer.

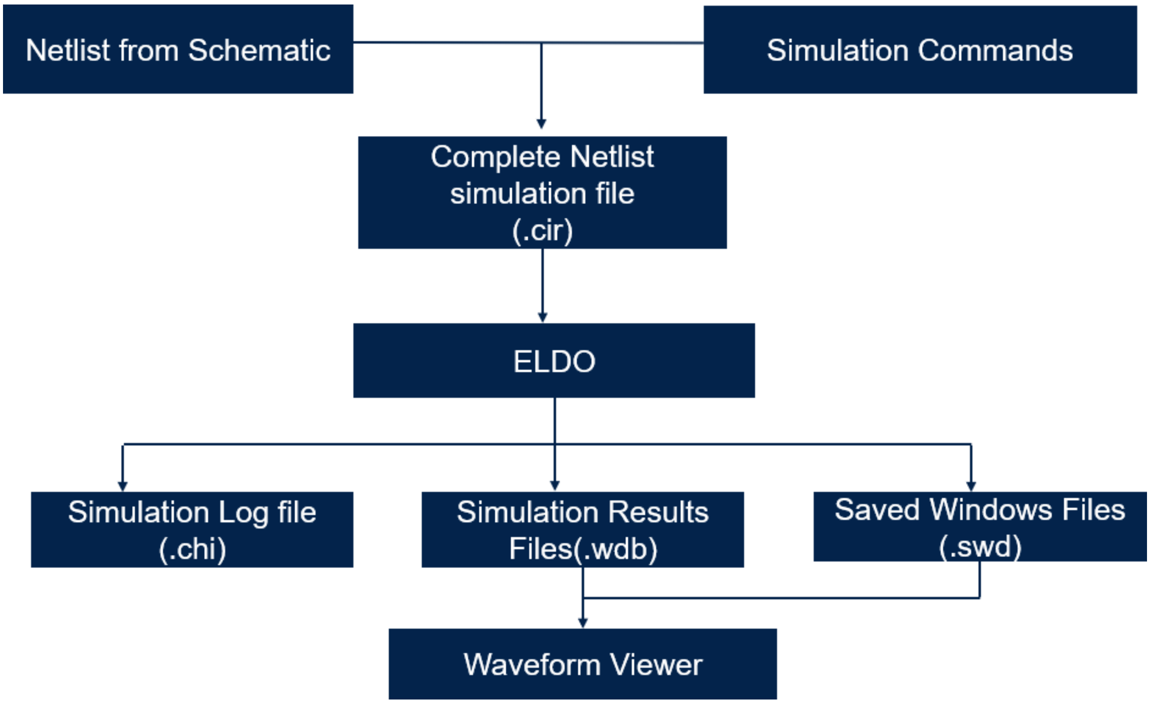



***Fig1.2 Required files in eldo***

- **<file>.swd:** A saved windows file used by the EZwave waveform viewer. This file contains information on waveforms and their display and cursor settings,window format settings and complex waveform transition settings.
- **<file>.cou:** A binary output file containing Eldo analog simulation results data. A special interface is provided to access this data from your own post- processor software if required.
- **<file>.ext:** A file containing extraction or waveform information, created when using a .EXTRACT command in the netlist and the .cou format output is specified.

**1.5 ELDO Command lines:**

**eldo [-b] [-l log_file_name][-o output_file_name][-outpath output_dir_name] [-i]cir_file_name**

**-b** Runs the simulation in the background.

**-l** Log file name for a background simulation.

**-o** Output .chi file name.

**-i** Input .cir file name

**eldo -help [commands|devices|sources|manual]**

commands Simulator

commands devices Device models

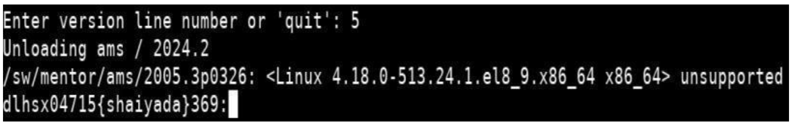
sources Macromodels

manual Full Eldo User s Manual

## 1.6 How to invoke Eldo on terminal

Step1: Write the sw ams command to install the eldo and hit enter.


Step2: Enter the line number according to version




Step3:To run the cir file we will use:

bsub -I -q short -P [project_name] -app eldo Eldo [cir file_name]

Step4: To see the waveform window,use this command:

bsub -q gui -I -P bcd_adv ezwave

Step5: To open the eldo manual

acroread /sw/mentor/ams/2014.1/amsv/docs/pdfdocs/eldo_ref.pdf

# Chapter 2
## Literature Review

The literature on VLSI interconnects and FinFET technology presents a range of advancements in delay modeling, parasitic extraction, and optimization techniques.

The paper "Novel and Efficient Approach for RC Delay Evaluation of On-chip VLSI Interconnect under Current Mode Signaling Technique" explores the advantages of current-mode signaling over traditional voltage-mode signaling in VLSI interconnects. The authors present a closed-form delay model based on an effective lumped element resistance and capacitance approximation of distributed RC lines. This approach significantly improves bandwidth and reduces propagation delay, addressing the challenges posed by interconnect scaling in modern integrated circuits.[1]

Current-Mode Signaling in Deep Submicron Global Interconnects: A Delay and Power Model closed-form latency and power dissipation model for current-mode signaling in deep submicron interconnects is presented in this study. Effective lumped element resistance is used by the authors, and RC lines that are distributed are analyzed using the capacitance approximation. The accuracy of a novel closed-form solution for delay under step input stimulation is within 5% for a range of parameters. A power dissipation model for current-mode signaling is also presented in the work, along with a comparison to voltage-mode repeater insertion methods. The results show that current-mode signaling is a promising substitute for high-speed VLSI designs since it provides reduced latency and enhanced energy efficiency over lengthy interconnects [2].

A Parasitic Extraction Technique for Pre-Route Timing Analysis of VLSI Interconnects The parasitic extraction methods for pre-route time analysis in VLSI circuits are the main topic of this study. The authors suggest a technique that uses common cell placement data to assess congestion and provide virtual routing. The work offers an enhanced FLUTE algorithm for creating parasitic RC trees as well as a pattern-library approach for extracting interconnect parasitics. By taking congestion effects in route segments into account, the suggested method improves the accuracy of capacitance extraction.Experimental results on industrial design cases demonstrate high computational speed and comparable accuracy to commercial tools, making it a valuable approach for early-stage timing verification[3].

A novel parasitic extraction method for pre- route timing analysis in VLSI circuits. The authors propose a technique that generates virtual routing and estimates congestion using standard cell placement information. The work presents an enhanced technique for creating parasitic RC trees as well as a pattern-library approach for extracting interconnect parasitics.It is a useful method for early-stage timing verification since studies on industrial design scenarios show good computational speed and accuracy equivalent to commercial tools [4].

The Present Status of Parasitic Extraction and Upcoming Developments: Resistance, capacitance, and inductance modeling are all included in this paper's thorough analysis of parasitic extraction methods. In their discussion of the growing significance of interconnect parasitic effects in deep submicron (DSM) designs, the authors highlight how these effects affect signal integrity and circuit performance. The study highlights upcoming developments in parasitic extraction and interconnect modeling while also examining delay calculation techniques and crosstalk mitigation tactics. The results indicate that layout-based extraction methods and sophisticated field solver algorithms will be essential for enhancing the precision and effectiveness of DSM designs [5]. Accurate Prediction of CMOS Device Performance from 180 nm to 7 nm Using Scaling Equations: This study creates polynomial-based scaling equations to forecast CMOS device performance across technology nodes between 180 nm and 7 nm.

Delay Extraction-Based Passive Macromodeling Techniques for Transmission Line Type Interconnects :This paper introduces a novel algorithm for delay extraction-based passive macromodeling of multiconductor transmission line interconnects characterized by tabulated multiport data. The authors propose a method that determines a unique logarithm of the H parameters, which is then approximated using a low-order rational function. The DEPACT algorithm is applied to obtain a passive and causal macromodel for SPICE simulation, leading to compact, low-order macromodels that result in faster transient simulations [6]. Passivity Verification in Delay-Based Macromodels of Multiconductor Electrical Interconnects :This study presents a generalized theory for passivity verification in delay-based macromodels for multiconductor transmission line networks. The authors demonstrate that passivity in a method-of-characteristics (MoC) macromodel is equivalent to the nonnegative definiteness in the admittance matrices of two submodels. They provide necessary and sufficient conditions for each submodel to maintain passivity, developing an algebraic test for verification[7].

Delay Extraction-Based Passive Compact Transmission-Line Macromodeling Algorithm : DEPACT algorithm is designed to address signal integrity challenges in high-speed interconnects. It ensures compact macromodels while maintaining passivity by using delay extraction before approximating the exponential stamp. The study highlights DEPACT's effectiveness in long lossy delay lines by contrasting it with other macromodeling approaches [8].

For placed gate-level netlists, the authors concentrate on narrowing the error gap in cell delay estimate. They significantly increase timing precision by employing the Random Forest model to train different machine learning models on 16 nm designs, achieving 91.25% accuracy. Data-driven optimization is crucial for electronic design automation (EDA) technologies, according to the study[12]. According to the study, 14nm circuits show more fluctuations in dynamic power and leakage power than 22nm FinFETs [11]. improving cell delay accuracy in combinational circuits in the post-placement stage by the application of machine learning algorithms.

Non-Incremental Genetic Algorithm for Testing and Diagnosing Delay Faults in FinFET VLSI Circuits: An enhanced test algorithm for identifying delay problems in FinFET circuits is presented in this study. The authors estimate mean, standard deviation, and variance for fault detection while integrating non-incremental genetic algorithms to optimize critical path delay. The work shows that FinFET-based combinational circuits have better fault analysis and error correction [9]. A 3-D Parasitic Extraction Flow for FinFET Structure Modeling and Timing Analysis: This study suggests a three-dimensional parasitic extraction flow for circuits based on FinFETs. The technique captures coupling effects between FinFETs and lower-layer interconnects by extracting resistances and capacitances using precise field solvers. The method's effectiveness in timing analysis is demonstrated by the study's validation using SPICE RC netlists [10]. FinFET Circuit Module Delay/Power Modeling and Optimization Under PVT Variations: This study investigates the modeling of delay and power for FinFET circuits under process, voltage, and temperature (PVT) variations. The authors examine FinFET logic gates and SRAM cells spanning 22nm and 14nm technology nodes using GenFin, an optimizer based on evolutionary algorithms.

A model of crosstalk noise for coupled RLC interconnects that tackles issues with signal integrity in deep submicron VLSI circuits. In comparison to SPICE simulations, the authors' decoupling method achieves an average inaccuracy of 6.8%. In order to assess shielding approaches and show how effective they are at lowering crosstalk noise, the paper presents the idea of effective mutual inductance [13]. This study presents closed-form analytical solutions for noise estimates while examining coupling noise patterns in dynamic circuits. The authors' analysis of noise tolerance measures demonstrates that noise immunity can be increased by raising frequency and lowering supply voltage. The paper highlights the effects of capacitive and inductive coupling effects on high-speed CMOS designs [14].

Evaluation of Interconnect Latency for 0.18μm and Upward Technologies: This study uses an inverter ring oscillator model to assess RC delay trends in different connectivity systems. When employing low-k anti-diffusion layers, the authors show that twin damascene Cu interconnects perform better than Al-based interconnects. Very High-Speed VLSI Interconnection Delay: A thorough examination of signal propagation latency in high-speed VLSI circuits is presented in this study. By demonstrating that RC models by themselves are insufficient for subnanosecond delay estimate, the authors emphasize the importance of wire inductance[17].

VLSI Interconnect Analytical Delay Models using Ramp Input: The shortcomings of conventional Elmore delay models are addressed in this study by introducing new analytical delay models for VLSI interconnects under ramp input excitation. In comparison to SPICE simulations, the authors' first- and second-moment-based analytical models predict propagation delay in RLC interconnects with an accuracy of 4%. The work emphasizes the significance of rise time in delay estimate by showing that, when applied to ramp input signals, Elmore delay might differ by up to 100%. The suggested models are appropriate for performance-driven synthesis and layout optimization since they significantly increase delay prediction accuracy while preserving computing efficiency [18].

An Interconnect Analytical Delay Model: By adding inductance effects to delay estimation for high-speed VLSI interconnects, this study builds on earlier research. In order to improve accuracy over conventional RC-based models, the authors suggest a closed-form analytical model based on first and second moments. According to the study, Elmore delay causes significant mistakes in high-speed circuits because it ignores inductance. The suggested approach provides a quick and effective substitute for source-sink delay estimates in interconnect trees, with an accuracy of 15% when compared to SPICE simulations [19]. Part I: Small Distributed RLC Interconnect Models Expressions for Single Line Transient, Time Delay, and Overshoot: Compact formulas for time delay, overshoot, and transient response in high-speed distributed RLC interconnects are presented in this study. Accurate delay estimate is made possible by the authors' rigorous derivation of closed-form solutions using on-chip global interconnect boundary conditions. By adding self and mutual inductance, the study improves time delay and crosstalk predictions in Sakurai's RC connection model. According to the findings, inductance effects take center stage in multi-GHz gigascale integration (GSI) circuits, requiring sophisticated modeling methods [20]. Better Analytical Delay Models for RC-Coupled Interconnects: In order to address the growing severity of crosstalk delay in deep submicron VLSI designs, this work proposes improved analytical delay models for RC-coupled interconnects.

Improved Analytical Delay Models for RC-Coupled Interconnects :This paper presents enhanced analytical delay models for RC-coupled interconnects, addressing the increasing severity of crosstalk delay in deep submicron VLSI designs. The authors propose technology-independent delay models that explicitly establish connections between transition patterns and interconnect delays, enabling crosstalk alleviation techniques such as crosstalk avoidance codes (CACs). Unlike previous models, which rely on numerical approaches, this study introduces closed-form analytical solutions that improve accuracy by considering loading capacitance and multiple wire interactions. The findings demonstrate that existing Elmore-based delay models fail to capture coupling effects, leading to significant errors in delay estimation. The proposed models achieve higher accuracy and better portability, making them suitable for high-performance global interconnects[21].
A Method for the Multi-Net Multi-Pin Routing Problem with Layer Assignment :This research focuses on multi-net multi-pin global routing in deep submicron VLSI designs, where interconnect constraints such as delay, congestion, and crosstalk significantly impact performance. The authors introduce a minimum crossing Y-Steiner tree algorithm with multi-layer assignment, optimizing routing paths while minimizing wire intersections. The study explores non-Manhattan routing architectures, demonstrating that Y-routing provides better manufacturability and congestion control compared to traditional rectilinear routing. Experimental results show that the proposed method reduces interconnect delay and improves routing efficiency, making it a promising approach for custom-built design styles.The study highlights the importance of matching constraints in high-performance analog circuits, demonstrating that automated placement techniques can achieve compact and optimized layouts[22,23].

## Research Gaps and Future Directions

Together, these works advance our knowledge of parasitic modeling, FinFET circuit optimization, and VLSI connection performance. In order to increase computational efficiency and accuracy in intricate circuit architectures, parasitic extraction techniques must be refined. Emerging materials and production methods beyond 7 nm must be taken into consideration in scaling equations for CMOS performance prediction. Improved passivity verification approaches are necessary for delay extraction-based macromodeling techniques to guarantee stability in high-speed interconnect simulations. More reliable statistical models are required for FinFET-based circuit optimization under PVT changes in order to precisely forecast performance variances. Furthermore, there is room for more study on machine learning-based methods for FinFET circuit failure identification, which are still relatively unexplored. The following lists the specific research gaps found in these studies concerning advanced VLSI interconnect approaches, parasitic extraction, delay modeling, and RC delay evaluation: Even though modeling RC delay and parasitic effects in VLSI interconnects has advanced significantly, there are still a number of unanswered questions. A few articles have examined current-mode signaling, but there aren't any thorough modeling frameworks that take into account capacitive and inductive couplings in dense multi-wire systems.

## Chapter-3

## Problem Statement

In the design and analysis of Very Large Scale Integration (VLSI) circuits, accurate timing analysis is crucial to ensure that the circuit meets its performance and reliability requirements. Delay extraction, which involves determining the propagation delay of signals through various paths in the circuit, is a fundamental aspect of timing analysis. Eldo, a SPICE-based circuit simulator, is widely used for its high-precision simulation capabilities, making it an essential tool for delay extraction in VLSI design.

### 3.1 Problem Statement: Perform Delay Extraction using ELDO

Despite the advanced capabilities of Eldo, there are several challenges and limitations associated with delay extraction in VLSI circuits that need to be addressed to improve accuracy, efficiency, and scalability. The key problems can be summarized as follows:

1. **Scalability Issues:** Traditional delay extraction methods struggle with scalability when applied to large-scale VLSI circuits, leading to increased computational overhead and simulation time.
2. **Parasitic Effects:** Accurate modeling of parasitic capacitances, resistances, and inductances is challenging, especially in deep submicron and nano-scale technologies. Inaccurate parasitic modeling can lead to imprecise delay estimates.
3. **Mixed-Signal Environments:** Delay extraction in mixed-signal circuits presents unique challenges due to the interaction between analog and digital components. Existing methods may not adequately address these complexities.
4. **Computational Overhead:** High computational overhead associated with traditional delay extraction n methods limits their efficiency, making it difficult to perform accurate and timely analysis for complex designs.
5. **Process Variations:** Variations in the manufacturing process can lead to discrepancies in delay estimates. Current methods may not adequately account for these variations, affecting the reliability ofthe extracted delays.
6. **Environmental Variations:** Modeling the impact of temperature variations, crosstalk, and power supply noise on delay extraction is challenging. Existing techniques may not provide accurate delay estimates under varying environmental conditions.
7. **Integration of Advanced Techniques:** Limited integration of advanced techniques such as machine learning and statistical analysis in delay extraction processes hinders the potential for improved accuracy and robustness.

### 3.2 Problem Statement: Perform Custom Route using Fusion Compiler

The custom route problem in electronic design automation (EDA) involves developing an efficient and effective method for routing connections between various components on a printed circuit board (PCB) or integrated circuit (IC) layout. The goal is to create a routing solution that meets specific design constraints and performance criteria while optimizing for factors such as wire length, signal integrity, power consumption, and manufacturability.

Key challenges in the custom route problem include:

1. **Complexity and Scalability**:
   - The routing algorithm must handle complex and large-scale designs with numerous nets and pins, ensuring scalability without significant increases in computational time and resources.
2. **Design Constraints**:
   - The solution must adhere to various design constraints, including spacing rules, layer restrictions, and specific routing topologies required for different types of signals (e.g., high-speed, analog, power).
3. **Performance Optimization**:
   - The routing method should optimize for critical performance metrics such as minimizing wire length, reducing signal delay, and ensuring signal integrity by minimizing crosstalk and electromagnetic interference.
4. **Adaptability**:
   - The routing solution must be adaptable to different technology nodes, manufacturing processes, and design environments, providing flexibility for various applications and design requirements.

### 3.3 Problem Statement: Perform DMSA using Prime Time

Modern integrated circuit designs must operate reliably across a wide range of process, voltage, and temperature (PVT) corners and functional modes. Traditional static timing analysis (STA) workflows often require sequential execution of multiple scenarios, leading to excessive runtime, high memory consumption, and increased complexity in script management. As design complexity grows, this approach becomes inefficient and error-prone. Synopsys PrimeTime offers Distributed Multi-Scenario Analysis (DMSA) to address these challenges by enabling parallel analysis of multiple timing scenarios. However, implementing DMSA effectively requires careful orchestration of scenario creation, data partitioning, and resource allocation, which can be non-trivial for design teams. There is a need for a robust and scalable methodology to integrate DMSA into STA flows using PrimeTime, ensuring accuracy, reducing turnaround time, and optimizing resource utilization without compromising analysis coverage.

## Chapter-4

## Possible solutions and Proposed Methodology

**Possible solutions**

To address the challenges associated with delay extraction using Eldo, several solutions can be proposed:

1. **Scalable Algorithms:**

   Develop optimized algorithms that can handle large-scale VLSI circuits efficiently.

   Utilize hierarchical simulation techniques to break down complex circuits into manageable sub-circuits.

2. **Enhanced Parasitic Modeling:**

   Implement advanced parasitic extraction techniques to accurately model capacitances, resistances, and inductances.

   Use 3D field solvers to capture parasitic effects more precisely in deep submicron and nano-scale technologies.

3. **Mixed-Signal Environment Handling:**

   Develop specialized modeling techniques that address the interaction between analog and digital components in mixed-signal circuits.

   Use co-simulation approaches that integrate both analog and digital simulation tools.

4. **Computational Efficiency:**

   Introduce novel delay extraction methods that reduce computational overhead, such as parallel processing and multi-threading.

   Optimize simulation parameters and use approximation techniques where exact solutions are not critical.

5. **Process Variation Accounting:**

   Incorporate statistical analysis techniques to account for process variations in delay extraction.

   Use Monte Carlo simulations to model the impact of process variations on delay.

6. **Environmental Variation Modeling:**

   Develop methods to accurately model the impact of temperature variations, crosstalk, and power supply noise on delay extraction.

   Use temperature-aware and noise-aware simulation techniques.

7. **Integration of Advanced Techniques:**

   Apply machine learning algorithms to predict delays based on historical data and simulation results.Use statistical methods to enhance the robustness of delay extraction against variations.

**Proposed Methodology**

The methodology outlines the steps for extracting delay in Universal Programmable Input/Output(UPIO) Delayline circuits using Eldo, a high-precision SPICE simulator. The goal is to achieve accurate and reliable delay measurements critical for high-speed digital circuit performance.

8. **Simulation Environment Setup**

   **Eldo Installation:** Ensure Eldo is installed and properly configured on the simulation workstation.

   **Design Import:** Import the UPIO Delayline circuit design into the Eldo environment.

   **Library Files:** Load necessary technology library files and device models required for the simulation.

9. **Test Bench Design**

   **Test Bench Creation:** Design a test bench that includes the UPIO Delayline circuit, input signal sources, and measurement probes.

   **Input Signal Configuration:** Configure the input signals to mimic realistic operating conditions,including different frequencies and voltage levels.

   **Measurement Points**: Place measurement probes at critical points in the circuit to capture delay information.

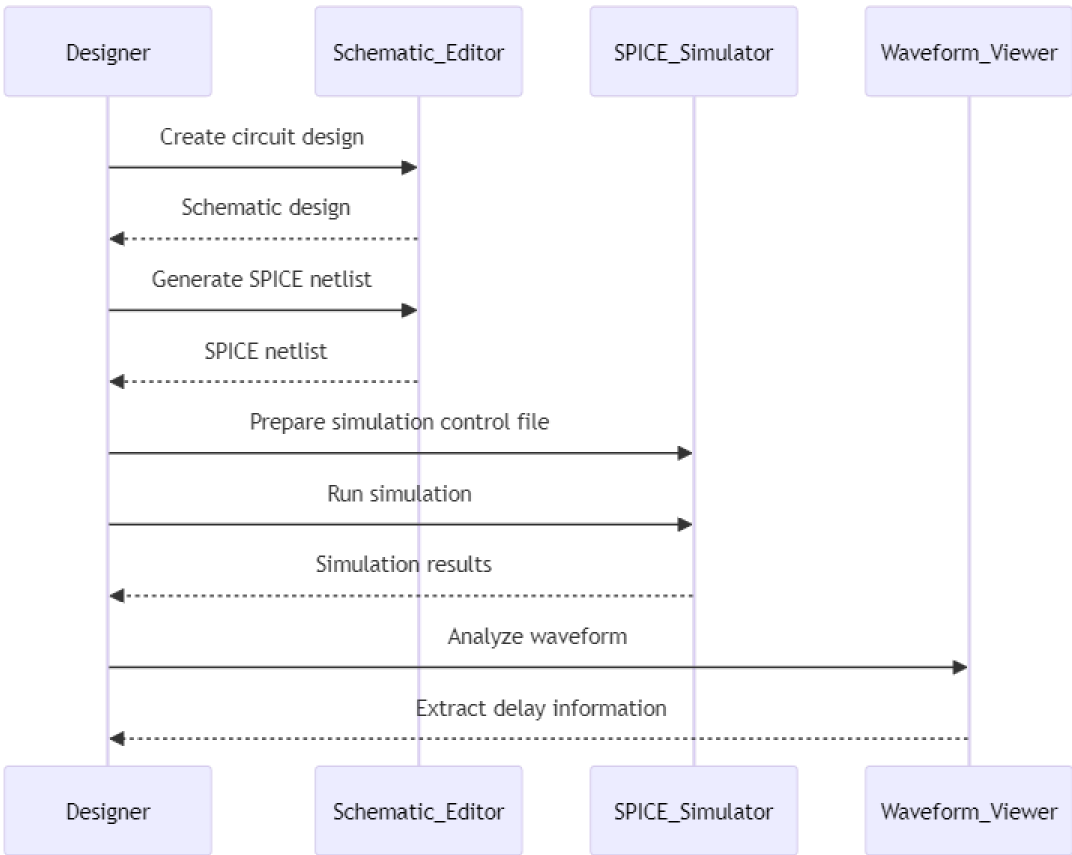



***Figure 4.1 Delay Extraction Methodology Design Flow***

10. **Simulation Configuration**

    **Simulation Parameters**: Set up simulation parameters such as simulation time, time step, and accuracy settings to ensure precise results.

    **Temperature and Process Corners**: Configure simulations to run under different temperature and process corner conditions to capture variability in delay.

11. **Running Simulations**

    **Initial Simulation:** Run an initial simulation to verify the setup and ensure the circuit operates as expected.

    **Parameter Sweeps:** Perform parameter sweeps by varying input signal characteristics (e.g., frequency, amplitude) and observe the impact on delay.

    **Monte Carlo Simulations:** Conduct Monte Carlo simulations to account for statistical variations in process parameters and obtain a distribution of delay values.

12. **Data Extraction and Analysis**

    **Delay Measurement**: Extract delay measurements from the simulation results using Eldo's post-processing tools.

    **Data Analysis:** Analyze the extracted delay data to identify trends and correlations with input parameters and operating conditions.

    **Comparison with Theoretical Models:** Compare the simulation results with theoretical delay model validate the accuracy of the simulations.

13. **Reporting Results**

    **Result Documentation:** Document the simulation results, including delay measurements, analysis, and comparisons with theoretical models.

    **Graphs and Tables:** Present the data in the form of graphs and tables for clear visualization of delay characteristics.

14. **Conclusion and Recommendations:** Summarize the findings, highlight key insights, and provide recommendations for future work and improvements in delay extraction methodology.

The proposed methodology ensures a systematic approach to extracting delay in UPIO Delayline circuits using Eldo. By following these steps, accurate and reliable delay measurements can be obtained, aiding in the design and verification of high-speed digital circuits.

# Chapter-5

# UPIO Delayline and Simulation Results

UPIO delaylines are designed to introduce controlled delays in digital signal paths. They are commonly used in applications such as timing adjustment, signal synchronization, and clock distribution.

UPIO typically refers to a flexible and programmable interface that can be configured to handle various input and output tasks in electronic systems. It is often used in microcontrollers, FPGAs (Field-Programmable Gate Arrays), and other programmable devices to interface with external components.

A delay line is an electronic component or circuit that delays the signal by a certain amount of time. Delay lines are used in various applications, including signal processing, communication systems, and timing adjustments.

Applications:

- **Timing Adjustments:** In digital systems, precise timing is crucial. A UPIO Delayline could be used to adjust the timing of signals to ensure proper synchronization between different parts of the system.
- **Signal Processing:** Delay lines are often used in signal processing to create effects such as echoes or to align signals in time. In a programmable context, this could be useful for various real-time processing tasks.
- **Communication Systems:** Delay lines can be used to manage signal propagation delays in communication systems, ensuring that signals arrive at the correct time for proper decoding and processing.

## 5.1 Delay Extraction Techniques

Delay extraction involves measuring and optimizing the delay introduced by the delayline. Accurate delay extraction is crucial for ensuring the performance and reliability of digital circuits.

- Delay extraction method using time-domain reflectometry, achieving high accuracy in delay measurements.
- Developed a delay extraction technique based on phase-locked loops (PLLs), demonstrating improved precision in delay control.

### Generic Retime Padlogic

The Generic Retime Padlogic is an UPIO functional Padlogic that provides a programmable retiming function to IO data at the padring. A configurable delay can also be applied to the data or clock. It can be used to improve the IO timing margins of external synchronous interfaces.

The functions of the retiming Padlogic are:

- Retiming of device IO data to selectable clocks, with optional bypass.
- Provide dedicated paths for IO clocks, with optional inversion.
- Optional configurable delay line for input/output data/clock
- Supports both single-edge and double-edge data:
  single-edge: IO data changing on rising or falling clock edge, but not both
  double-edge: IO data changing on both rising and falling clock edges

**5.2 Size of UPIO Delayline**

The size of a delay line involves specifying several key parameters that determine its overall delay characteristics and performance. Here are the main factors to consider:

- **Number of Stages (N)**
  The number of stages in the delay line directly impacts the total delay. Each stage typically consists of a delay element that introduces a specific amount of delay. For a UPIO Delayline [15:0], there are 16 stages.
- **Delay per Stage (τ)**
  The delay introduced by each stage is a crucial parameter. This can be determined by the design of the delay element (e.g., inverters, capacitors, resistors) and the technology used. The total delay (T) can be calculated as:
  1. $T=N\times\tau$

  where N is the number of stages and $\tau$ is the delay per stage.
- **Control Mechanism**
  The ability to control or program the delay introduced by each stage is vital for a programmable delayline. This can be achieved through various methods such as:
  Digital Control: Using digital signals to switch delay elements in
  and out. Analog Control: Using voltage or current levels to adjust
  the delay.
- **Total Delay Range**
  The total delay range is the maximum delay that the delay line can introduce. This is determined by the number of stages and the maximum delay per stage. For example, if each stage can introduce a delay between 0 and τmax$\tau max$, the total delay range is:

  $$Tmax=N\times\tau max \quad Tmax=N\times\tau max$$

- **Resolution**

  The resolution of the delay line is the smallest increment of delay that can be controlled. Higher resolution allows for finer control over the delay.

- **Technology and Process Parameters**

  The technology node (e.g., 65nm, 45nm) and process parameters (e.g., voltage, temperature) affect the delay characteristics. These factors need to be considered during the design and simulation phases.

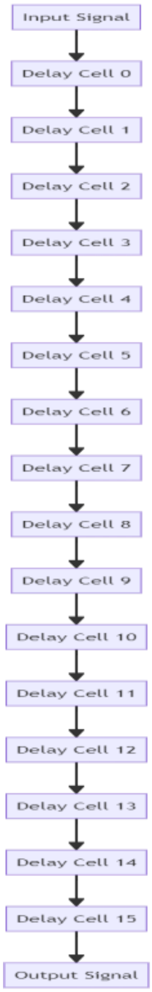



***Figure 5.1 Circuit diagram for a UPIO Delayline [3:0]***

### 5.3 Delay cell:

- **Input Signal:** The initial signal that needs to be delayed**.**
- **Delay Cells [0-15]:** Each delay cell represents a programmable delay stage. The signal passes through each delay cell sequentially, adding delay at each stage.
- **Output Signal:** The final delayed signal after passing through all 16 delay cells**.**

Each delay cell can be configured to introduce a specific amount of delay, allowing for precise control over the overall delay of the signal.

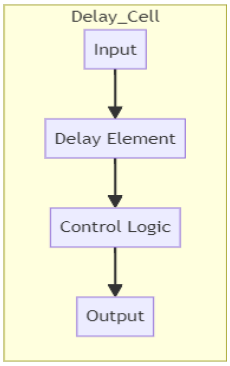



*Figure 5.2 Delay Cell*

**5.4 Simulation Results:**

Extracted Delay for different corners:

This section presents the delay analysis of a UPIO Delayline [3:0] under the slow-slow (SS) process corner using Eldo SPICE simulator. The slow-slow corner represents the worst-case scenario where both NMOS and PMOS transistors exhibit slower than typical performance due to process variations.

| Cfg_Delay[3:0] | Corners | Rise Delay(ns) | Fall_Delay(ns) |
|---|---|---|---|
| 0 | ssgnp_0.72V_125C_cworst_Ccworst | 0.040 | 0.041 |
| 1 | ssgnp_0.72V_125C_cworst_Ccworst | 0.301 | 0.296 |
| 2 | ssgnp_0.72V_125C_cworst_Ccworst | 0.556 | 0.567 |
| 3 | ssgnp_0.72V_125C_cworst_Ccworst | 0.817 | 0.812 |
| 4 | ssgnp_0.72V_125C_cworst_Ccworst | 1.072 | 1.073 |
| 5 | ssgnp_0.72V_125C_cworst_Ccworst | 1.333 | 1.328 |
| 6 | ssgnp_0.72V_125C_cworst_Ccworst | 1.588 | 1.589 |
| 7 | ssgnp_0.72V_125C_cworst_Ccworst | 1.849 | 1.844 |
| 8 | ssgnp_0.72V_125C_cworst_Ccworst | 2.104 | 2.105 |
| 9 | ssgnp_0.72V_125C_cworst_Ccworst | 2.365 | 2.360 |
| 10 | ssgnp_0.72V_125C_cworst_Ccworst | 2.620 | 2.621 |
| 11 | ssgnp_0.72V_125C_cworst_Ccworst | 2.881 | 2.876 |
| 12 | ssgnp_0.72V_125C_cworst_Ccworst | 3.136 | 3.137 |
| 13 | ssgnp_0.72V_125C_cworst_Ccworst | 3.397 | 3.392 |
| 14 | ssgnp_0.72V_125C_cworst_Ccworst | 3.652 | 3.653 |
| 15 | ssgnp_0.72V_125C_cworst_Ccworst | 3.912 | 3.907 |

*Figure 5.3: Extracted Delay of ssgnp_0.72V_125C_cworst_Ccworst*

This section presents the delay analysis of a UPIO Delayline [3:0] under typical (TT) process corner conditions using the Eldo SPICE simulator. The typical corner represents the nominal performance of both NMOS and PMOS transistors.

| Cfg_Delay[3:0] | Corners | Rise Delay(ns) | Fall Delay(ns) |
|---|---|---|---|
| 0 | tt_0.80V_25C_typical | 0.029 | 0.029 |
| 1 | tt_0.80V_25C_typical | 0.185 | 0.183 |
| 2 | tt_0.80V_25C_typical | 0.339 | 0.339 |
| 3 | tt_0.80V_25C_typical | 0.495 | 0.492 |
| 4 | tt_0.80V_25C_typical | 0.649 | 0.649 |
| 5 | tt_0.80V_25C_typical | 0.804 | 0.802 |
| 6 | tt_0.80V_25C_typical | 0.958 | 0.958 |
| 7 | tt_0.80V_25C_typical | 1.114 | 1.112 |
| 8 | tt_0.80V_25C_typical | 1.268 | 1.268 |
| 9 | tt_0.80V_25C_typical | 1.424 | 1.422 |
| 10 | tt_0.80V_25C_typical | 1.578 | 1.578 |
| 11 | tt_0.80V_25C_typical | 1.734 | 1.732 |
| 12 | tt_0.80V_25C_typical | 1.888 | 1.888 |
| 13 | tt_0.80V_25C_typical | 2.044 | 2.042 |
| 14 | tt_0.80V_25C_typical | 2.198 | 2.198 |
| 15 | tt_0.80V_25C_typical | 2.353 | 2.350 |

***Figure 5.4: Extracted Delay of ttgnp_0.81V_25C_cworst_Ccworst***

This section presents the delay analysis of a UPIO Delayline [3:0] under the fast-fast (FF) process corner using the Eldo SPICE simulator. The fast-fast corner represents the best-case scenario where both NMOS and PMOS transistors exhibit faster than typical performance due to process variations.

| Cfg_Delay[3:0] | Corners | Rise Delay(ns) | Fall Delay(ns) |
|---|---|---|---|
| 0 | ffgnp_0.88V_125C_cbest_Ccbest | 0.023 | 0.025 |
| 1 | ffgnp_0.88V_125C_cbest_Ccbest | 0.141 | 0.139 |
| 2 | ffgnp_0.88V_125C_cbest_Ccbest | 0.257 | 0.257 |
| 3 | ffgnp_0.88V_125C_cbest_Ccbest | 0.376 | 0.374 |
| 4 | ffgnp_0.88V_125C_cbest_Ccbest | 0.492 | 0.491 |
| 5 | ffgnp_0.88V_125C_cbest_Ccbest | 0.610 | 0.608 |
| 6 | ffgnp_0.88V_125C_cbest_Ccbest | 0.726 | 0.726 |
| 7 | ffgnp_0.88V_125C_cbest_Ccbest | 0.844 | 0.842 |
| 8 | ffgnp_0.88V_125C_cbest_Ccbest | 0.960 | 0.960 |
| 9 | ffgnp_0.88V_125C_cbest_Ccbest | 1.079 | 1.077 |
| 10 | ffgnp_0.88V_125C_cbest_Ccbest | 1.196 | 1.196 |
| 11 | ffgnp_0.88V_125C_cbest_Ccbest | 1.313 | 1.311 |
| 12 | ffgnp_0.88V_125C_cbest_Ccbest | 1.430 | 1.429 |
| 13 | ffgnp_0.88V_125C_cbest_Ccbest | 1.548 | 1.545 |
| 14 | ffgnp_0.88V_125C_cbest_Ccbest | 1.665 | 1.663 |
| 15 | ffgnp_0.88V_125C_cbest_Ccbest | 1.782 | 1.780 |

***Figure 5.5: Extracted Delay of ffgnp_0.88V_125C_cworst_Ccworst***

## Chapter-6
## Custom Route

In VLSI (Very Large Scale Integration) design, custom routing refers to the manual or semi-automated process of defining the paths that electrical signals take through an integrated circuit (IC). This process is a critical step in the physical design phase of VLSI, where the abstract circuit design is transformed into a physical layout that can be fabricated on a semiconductor wafer.

### 6.1 Routing:

Routing in VLSI involves creating the physical paths (wires) that connect different components (such as transistors, gates, and other circuit elements) on the chip. This ensures that the electrical signals can travel between these components as required by the design.

- **Custom Routing:**
  Custom routing is often used for critical nets or signal paths that require special attention due to their impact on the overall performance, power consumption, or reliability of the IC. Unlike automated routing, which is done by electronic design automation (EDA) tools, custom routing involves manual intervention to optimize these paths.
- **Critical Nets:**
  These are specific signal paths that are crucial for the performance of the IC. They might include clock signals, power distribution networks, and high-speed data paths. Custom routing ensures that these nets meet stringent electrical and timing requirements.

### 6.2 Steps in Custom Routing

- **Floorplanning:**
  Before routing, the placement of major functional blocks on the chip is defined. This step sets the stage for efficient routing by minimizing the distance between interconnected components.

- **Placement:**
  Individual components within the functional blocks are placed. This step is crucial for ensuring that the routing can be done efficiently and that the design meets timing and area constraints.

- **Routing:**
  **Global Routing:** This step defines the general paths that the interconnections will take across the chip. It does not specify the exact geometries but provides a high-level plan.
  **Detailed Routing:** This step involves defining the exact geometries of the interconnections, including the specific layers of metal to be used, the widths of the wires, and the precise paths they will take.

- **Custom Routing:**
  For critical nets, custom routing is performed to ensure that these paths meet specific electrical

and timing requirements. This might involve:

**Manual Adjustment:** Manually adjusting the paths to avoid congestion, minimize crosstalk, and reduce resistance and capacitance.

**Shielding:** Adding shielding to sensitive signal paths to protect them from interference.

Layer Optimization: Selecting the optimal metal layers for routing to balance performance and manufacturing considerations.

- **Verification:**

  After routing, the design is verified to ensure that it meets all electrical, timing, and manufacturing requirements. This involves running simulations and performing checks such as Design Rule Checking (DRC) and Layout Versus Schematic (LVS) verification.

Metal layers are used to create the physical interconnections between various components on an integrated circuit (IC). These layers are part of the metallization process, where different metal layers are deposited and patterned to form the wiring of the chip. The choice and use of metal layers are crucial for ensuring the performance, power efficiency, and reliability of the IC.

### 6.3 Metal Layers

Metal layers are thin films of metal deposited on the semiconductor substrate. These layers are used to create the electrical connections between transistors, gates, and other components on the chip.

**Typical Metal Layer Stack**

A typical IC might have several metal layers, each serving different purposes:

- **Metal 1 (M1):**

  The first metal layer, closest to the silicon substrate. It is primarily used for local interconnections between transistors and other components within a small area.

- **Metal 2 (M2):**

  The second metal layer, used for slightly longer interconnections and to connect to the first metal layer through vias (vertical interconnects).

- **Metal 3 (M3) and Above:**

  Higher metal layers are used for increasingly longer interconnections. These layers are typically wider and thicker to reduce resistance and capacitance, improving signal integrity and reducing delay.

- **Top Metal Layers:**

  The uppermost metal layers are used for global interconnections, such as clock distribution, power distribution networks, and high-speed signal paths. These layers are designed to handle high currents and minimize signal delay.

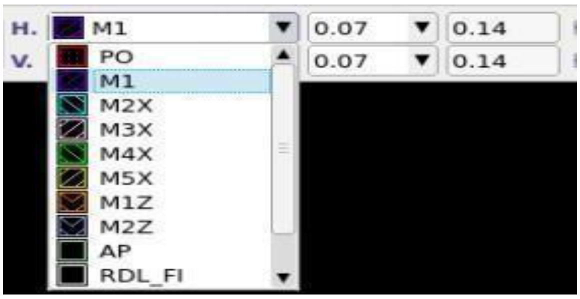



*Fig.6.1 Vertical & Horizontal layer with width(Tool: Fusion Compiler)*

### 6.4 Key Aspects of Custom Routing in VLSI

- **Precision Control**: Custom routing allows designers to precisely control the path of each signal, ensuring that critical signals have the shortest and most direct routes. This can help minimize signal delay, crosstalk, and electromagnetic interference (EMI).
- **Optimization**: By manually routing signals, designers can optimize the layout for specific performance criteria, such as minimizing signal delay, reducing power consumption, or improving signal integrity.
- **Design Constraints**: Custom routing allows designers to adhere to specific design constraints, such as spacing requirements, layer restrictions, and manufacturing tolerances. This is particularly important in high-density designs where space is limited.
- **Critical Signals**: Custom routing is often used for critical signals that require special attention, such as high-speed data lines, clock signals, and power distribution networks. Ensuring that these signals are routed correctly can significantly impact the overall performance of the system.
- **Design Tools**: Custom routing is typically performed using specialized design tools, such as Cadence Virtuoso, Synopsys IC Compiler, or Mentor Graphics Calibre. These tools provide features for manual routing, including interactive routing, constraint management, and design rule checking.

*Fig 6.2 Before route floorplan*

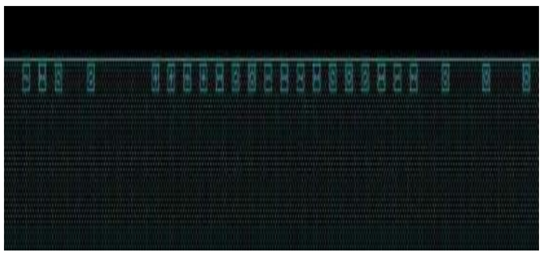


*Fig 6.3 UPIO Delayline pins(Un-Routed Pins)*

### 6.1 Methodology for Custom Routing in Fusion Compiler

- **Preparation and Setup**

  **Design Import:** Import the design files (netlist, constraints, etc.) into Fusion Compiler. **Floorplanning:** Define the layout of major blocks to minimize interference and optimize performance.

**Technology File:** Load the correct technology file that includes design rules, layer definitions, and other process-specific parameters.

- **Placement**

  **Automatic Placement:** Use automatic placement for non-critical components.

  **Manual Placement:** Place critical components manually to ensure optimal performance.

- **Routing Strategy**

  **Global Routing:** Perform an initial global routing to define the general paths for interconnections.

  **Detailed Custom Routing:** Manually route critical nets to ensure they meet stringent requirements for performance.

- **Verification and Optimization**

  **Design Rule Checking (DRC):** Verify that the custom routing adheres to all design rules specified by the technology file.

  **Layout Versus Schematic (LVS):** Ensure that the layout matches the original schematic design.

  **Parasitic Extraction:** Extract parasitic capacitances and resistances to analyze their impact on performance.

  **Post-Layout Simulation:** Perform post-layout simulations to verify that the routed design meets the required performance specifications.

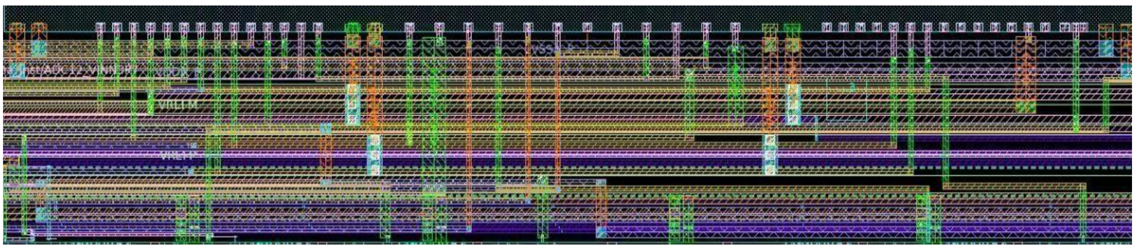


*Fig 6.4 UPIO Delayline (Routed Pins)*

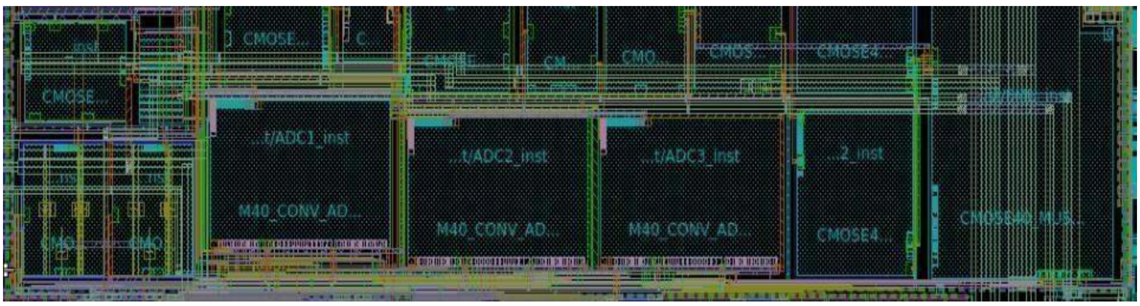



*Fig 6.5 Routed Floorplan*

After routing in VLSI design, extracting the resistance of nets is a crucial step to ensure that the design meets its performance, power, and reliability specifications. This process is part of parasitic extraction, where both resistance (R) and capacitance (C) of the interconnects are calculated.

### 6.5 Process of Extracting Net Resistance

- **Parasitic Extraction Tools:**
  Use parasitic extraction tools like Synopsys StarRC, Cadence Quantus QRC, or Mentor Graphics Calibre xRC to extract resistance and capacitance values from the routed design.
- **Extraction Steps:**
  **Load Design:** Load the routed design into the parasitic extraction tool.
  **Define Extraction Parameters:** Set up the extraction parameters, including the technology file, extraction rules, and accuracy settings.
- **Run Extraction:** Execute the extraction process to generate an RC netlist that includes the resistance and capacitance values of the interconnects.
- **Review Results:** Analyze the extracted parasitics to identify any high-resistance paths that may need optimization.

Extracting the resistance of nets after routing is a critical step in the VLSI design process. It ensures that the design meets its performance, power, and reliability specifications by providing accurate information for timing analysis, power analysis, signal integrity checks, and reliability assessments. By using parasitic extraction tools and following a systematic extraction process, designers can identify and mitigate potential issues, leading to a robust and high-performance IC design.

# Chapter-7

## Distributed Multi-Scenario Analysis

Primetime provides an efficient way to analyze timing at different corners and different operating modes. MMMC (multi-mode multi corner) refers to performing timing analysis at various modes and corner.

### 7.1 Distributed Multi-Scenario Analysis

Distributed Multi-Scenario Analysis (DMSA) refers to timing analysis at different scenarios in a distributed manner. Scenarios are combination of various operating corners(process, voltage, temperature, RC corners) and different operating modes (functional mode, test mode, sleep mode, read mode, write mode etc).

Scenarios can be different for timing and power analysis. Some significant scenarios for timing and power are mentioned below,

- **RC_worst_slowProcess_HighTemp_LowVoltage:** This scenario is generally used for checking setup time. RC_worst indicates the worst values of Resistance and worst values for coupling and ground capacitance on interconnects are taken into the account. Slow process indicates variation across the chip that can slow down the performance like slow operation of both pmos and nmos in a CMOS configuration. High temperature increases the resistance and low voltage (VDD) increases the charging time of output capacitance; both reducing the performance. Hence this slow-corner is used for checking setup time along with any operating mode of the chip. Hold timing is also checked at this corner but most of the time it will be clean as hold is getting checked at slow corner.

- **RC_best_fastProcess_LowTemp_HighVoltage:** This scenario is generally used for checking hold time. RC_best indicates the best values of Resistance and best values for coupling and ground capacitance on interconnects are taken into the account ; fast process indicates variation across the chip that can speed up the process like fast operation of both pmos and nmos in a CMOS configuration. Low temperature reduces the resistance and high voltage (VDD) decreases the charging time of output capacitance; both speeding up the performance. Hence this fast-corner is used for checking hold time along with any operating mode of the chip. Setup timing is also checked at this corner but most of the time it will be clean as setup is getting checked at fast corner.

- **RC_worst_fastProcess_LowTemp_HighVoltage:** This scenario is worst case check for power analysis. RC worst parasitic corner results in high power dissipation in interconnects, whereas fast process, low temperature and high voltage result in fast transition of the signal. Again, this corner can be used to analyze power at any functional mode.

## 7.2 DMSA ECO Fixes

- **Transition Time Fixing:** Transition time can be fixed in 3 ways, i) swapping the cell to lower vts, ii) up-sizing the cell, iii) inserting buffer. To avoid any area penalty i.e. to avoid up-sizing of cell or adding any buffer; swapping to lower vts is a safe option to fix transition time on the paths which are violated by less margin. Moreover, inserting a buffer may hamper the setup timing of that particular path. Following is the command used for fixing transition time,

- The size_cell option in above command may up-size the driver cell also. In order to avoid this up-sizing, set PT variable eco_alternative_area_ratio_threshold to 1.0; as setting it to 1.0 will ensure that area of cell will remain same. Other method for fixing transition time is insert_buffer. If insert_buffer method is used to fix the transition time, then the list of buffers should also need to be mentioned that should be used during buffer insertion. We can also specify setup and hold margin so as to preserve both the timing parameter when fixing transition time.
- **Setup Time Fixing:** The very basic step in fixing setup timing is to swaps higher vts to lower
- vts. Other fixes like up-sizing, cross-talk analysis can be done afterwards if the timing is not getting improved by swapping of the cell.
- Setting PT variable eco_alternative_area_ratio_threshold to 1.0 will ensure that size_cell option in above command will prevent any area changes of a cell. If it is set to 2.0, it will allow to increase the cell area by 2 times the original area. Setting it to 0 will impose no restriction on area and tool may size it to any driver strength which is not recommendable.

- **Power Optimization:** Cells in the timing path that have higher setup margin can be converted to higher vts, their driver strength can be reduced (downsizing) to optimize leakage and dynamic power, or extra redundant buffers can also be removed if it has enough setup and hold slack. Following is the command that is used for fixing power.When -pattern_priority is specified, tool will only swaps the lower vts to higher vts depending upon the priority given to VT cells, and will not do any downsizing. If -pattern_priority option is not specified than tool will downsize the cells to optimize the dynamic power.

- **Hold Time Fixing:** Hold fixing can be done by either swapping lower vts to higher vts or by inserting buffers. For fixing hold using swapping, set the PT variable eco_alternative_area_ratio_threshold to 1.0.
- -setup_margin option in the above command will make sure that the setup timing will be preserved by the value specified. If hold fix is to be done by buffer insertion than list of buffer need to be specified that are to be used during buffer insertion. Option -physical_mode will insert buffers by extracting cell placement information from lef and def. Following command for hold fixing is used.

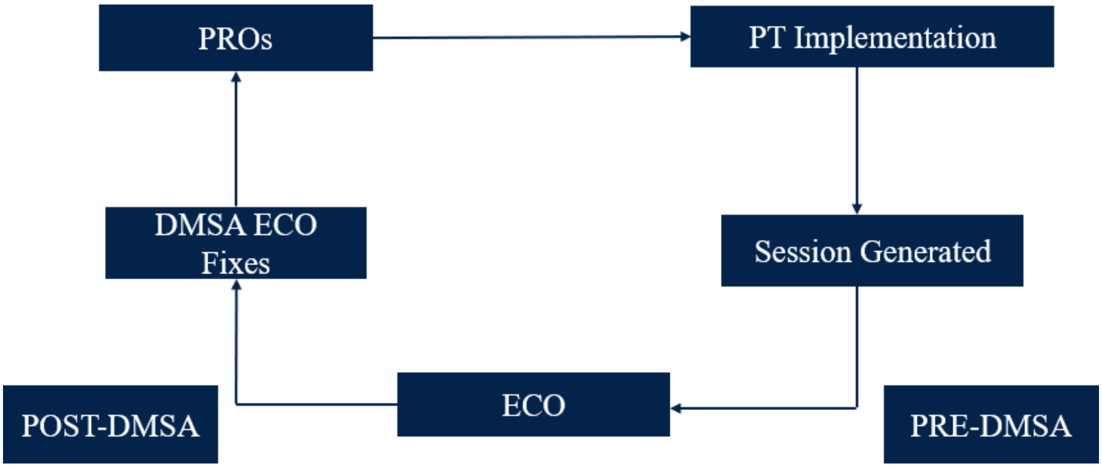



*Fig 7.1 DMSA Implementation*

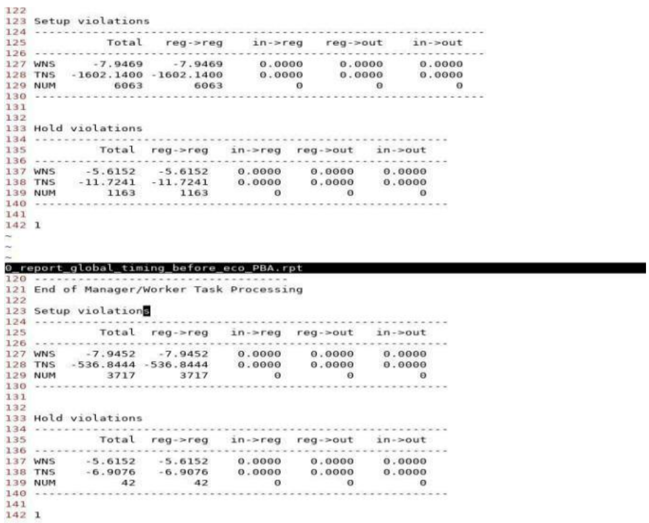
To set up a DMSA run, three key components must be configured:

- Number of licenses
- Saved Sessions
- Scenario definitions

### 7.3 Simulation Result:

**Setup Violations:**

- WNS: Indicates the worst case where the setup time requirement is not met. In the first report, it's -7.9469, and in the second report, it's -7.9452.
- TNS: Shows the total slack deficit across all violating paths. Initially, it is -1602.1400, and after some changes, it reduces to -536.8444.
- NUM: The number of paths failing the setup check. Initially, 6063 paths are failing, which reduces to 3717 after adjustments.



```
Setup violations
------------------------------------------------------------
            Total    reg->reg    in->reg    reg->out    in->out
------------------------------------------------------------
WNS       -7.9469     -7.9469     0.0000     0.0000     0.0000
TNS    -1602.1400  -1602.1400     0.0000     0.0000     0.0000
NUM          6063        6063          0          0          0
------------------------------------------------------------


Hold violations
------------------------------------------------------
          Total   reg->reg   in->reg   reg->out   in->out
------------------------------------------------------
WNS     -5.6152    -5.6152    0.0000    0.0000    0.0000
TNS    -11.7241   -11.7241    0.0000    0.0000    0.0000
NUM        1163       1163         0         0         0
------------------------------------------------------

1
~
~
~
0_report_global_timing_before_eco_PBA.rpt
-------------------------------
End of Manager/Worker Task Processing

Setup violations
------------------------------------------------------
          Total   reg->reg   in->reg   reg->out   in->out
------------------------------------------------------
WNS     -7.9452    -7.9452    0.0000    0.0000    0.0000
TNS   -536.8444  -536.8444    0.0000    0.0000    0.0000
NUM        3717       3717         0         0         0
------------------------------------------------------


Hold violations
------------------------------------------------------
          Total   reg->reg   in->reg   reg->out   in->out
------------------------------------------------------
WNS     -5.6152    -5.6152    0.0000    0.0000    0.0000
TNS     -6.9076    -6.9076    0.0000    0.0000    0.0000
NUM          42         42         0         0         0
------------------------------------------------------

1
~
```

*Fig 7.2 Pre- DMSA and Post DMSA Result*

**Hold Violations:**

- WNS: Reflects the worst case where the hold time requirement is not met. It remains consistent at -5.6152 across both reports.
- TNS: Total slack deficit for hold violations. Initially, it is -11.7241, and then it changes to -6.9076.
- NUM: The number of paths failing the hold check. Initially, 1163 paths are failing, which reduces to 42 after adjustments.

The DMSA implementation appears to have reduced the number of timing violations significantly, particularly for setup checks, indicating a positive impact on the design's timing performance.
Further efforts might be needed to address the worst-case violations, especially for hold checks, to ensure all timing requirements are met.

# Chapter-8

## Conclusion and Future Scope

The research on delay extraction using Eldo has highlighted several key challenges and proposed solutions to improve the accuracy, efficiency, and scalability of delay extraction methods. By addressing these challenges, the following outcomes can be achieved:

**Improved Accuracy:** Enhanced accuracy of delay extraction in VLSI circuits, leading to more reliable timing analysis.

**Increased Efficiency:** Reduced computational overhead and simulation time, making delay extraction more efficient for large-scale designs.

**Enhanced Scalability:** Development of scalable methods that can be applied to complex and large-scale VLSI circuits.

**Ensured Robustness:** Provision of robust delay extraction techniques that account for process and environmental variations.

**Advanced Mixed-Signal Analysis:** Improved delay extraction methods for mixed-signal circuits, addressing the unique challenges of such designs.

**Leveraged Advanced Techniques:** Utilization of machine learning and statistical analysis to further enhance the delay extraction process.

By achieving these outcomes, the research will contribute to the advancement of VLSI design and timing analysis, ensuring that circuits meet their performance and reliability requirements in an efficient and accurate manner.

Extracting the resistance of nets after routing in VLSI design yields several important outcomes that are crucial for ensuring the performance, power efficiency, and reliability of the integrated circuit (IC). Here are the key outcomes:

**1. Accurate Timing Analysis**

**Signal Delay Calculation:**

The resistance values, combined with the capacitance values, are used to calculate the RC delay of signal paths. This helps in determining the propagation delay of signals through the interconnects.

**Static Timing Analysis (STA):**

Accurate resistance values are essential for STA, which verifies that all timing constraints (setup, hold, clock skew, etc.) are met. This ensures that the design operates correctly at the target clock frequency.

**2. Power Analysis**

**Dynamic Power Consumption:**

The resistance of interconnects affects the charging and discharging of capacitive loads, influencing the dynamic power consumption of the circuit. Accurate resistance values help in estimating the power consumption more precisely.

**IR Drop Analysis:**

Resistance extraction allows for the analysis of voltage drops (IR drop) in power and ground nets. High resistance can cause significant voltage drops, leading to insufficient voltage levels at various parts of the circuit, which can affect performance and reliability.

**3. Signal Integrity Analysis**

**Voltage Level Accuracy:**

High resistance can cause signal degradation, leading to incorrect voltage levels at the receiving end of interconnects. Accurate resistance values help in identifying and mitigating such issues.

**Crosstalk Analysis:**

Resistance values are used in conjunction with capacitance values to analyze crosstalk between adjacent signal lines. This helps in ensuring signal integrity and minimizing interference.

**Future Scope**

The future scope of delay extraction using Eldo in VLSI (Very Large Scale Integration) design is promising, given the continuous advancements in semiconductor technology and the increasing complexity of integrated circuits. Here are several key areas where future research and development can focus to further enhance delay extraction methodologies:

**1. Scalability Enhancements**

As VLSI circuits continue to grow in complexity and size, scalable delay extraction methods will become increasingly important. Future research can focus on:

- **Hierarchical Simulation Techniques:** Developing advanced hierarchical simulation techniques to manage and simulate large-scale circuits efficiently.
- **Parallel Processing:** Leveraging parallel processing and distributed computing to reduce simulation time and handle larger designs.

**2. Advanced Parasitic Modeling**

Accurate modeling of parasitic effects is crucial for precise delay extraction. Future work can aim to:

- **3D Parasitic Extraction:** Enhance 3D parasitic extraction tools to capture parasitic effects more accurately in advanced technology nodes.
- **Machine Learning Models:** Utilize machine learning models to predict parasitic effects based on circuit layout and process parameters.

**3. Mixed-Signal and RF Circuit Analysis**

Mixed-signal and RF circuits present unique challenges for delay extraction. Future research can explore:

- **Co-Simulation Approaches:** Developing integrated co-simulation approaches that combine analog and digital simulation tools for mixed-signal environments.
- **RF-Specific Techniques:** Creating specialized delay extraction techniques tailored for RF circuit designs.

**4. Process Variation and Reliability Analysis**

Process variations can significantly impact delay extraction accuracy. Future studies can focus on:

- **Statistical Analysis:** Incorporating advanced statistical analysis techniques to model and mitigate the impact of process variations.
- **Reliability Modeling:** Developing reliability models that account for aging effects, electro migration,and other reliability concerns in delay extraction.

**5. Environmental Variation Modeling**

Environmental factors such as temperature, crosstalk, and power supply noise affect signal propagation delays. Future research can aim to:

- **Temperature-Aware Simulation:** Enhance temperature-aware simulation techniques to provide accurate delay estimates under varying thermal conditions.
- **Noise Modeling:** Develop noise-aware delay extraction methods that consider the impact of power supply noise and crosstalk on signal delays.

**6. Integration of Machine Learning and AI**

Machine learning and artificial intelligence (AI) offer significant potential for improving delay extraction. Future work can explore:

- **Predictive Models:** Creating predictive models using machine learning to estimate delays based on historical data and simulation results.
- **Optimization Algorithms:** Applying AI-based optimization algorithms to enhance the accuracy and efficiency of delay extraction processes.

**7. Automation and Tool Integration**

Automation and seamless integration with design tools can streamline the delay extraction process. Future developments can include:

- **Automated Workflows:** Developing automated workflows that integrate delay extraction with other design and verification tools.
- **Cloud-Based Solutions:** Leveraging cloud-based simulation platforms to provide scalable and accessible delay extraction services.

**8. Emerging Technologies**

As new technologies emerge, delay extraction methods will need to adapt. Future research can focus on:

- **FinFET and Beyond**: Developing delay extraction techniques for advanced transistor technologies such as FinFETs, GAAFETs, and other emerging devices.
- **3D ICs:** Enhancing delay extraction methods for 3D integrated circuits, considering the unique challenges of 3D stacking and interconnects.

**9. Real-Time and In-Situ Analysis**

Real-time and in-situ delay extraction can provide immediate feedback during the design process. Future work can explore:

- **Real-Time Monitoring:** Developing techniques for real-time delay monitoring and extraction during circuit operation.
- **In-Situ Measurements:** Creating in-situ measurement methods to validate and calibrate delay extraction models.

**10. Interdisciplinary Approaches**

Collaborative efforts across disciplines can lead to innovative solutions. Future research can benefit from:

- **Interdisciplinary Collaboration:** Encouraging collaboration between electrical engineers, computer scientists, and material scientists to address complex delay extraction challenges.
- **Cross-Domain Applications:** Applying delay extraction techniques to other domains such as bioelectronics, photonics, and quantum computing.

## References

1. Rajib Kar Ashis Kumar Mal *A Novel and Efficient Approach for RC Delay Evaluation of On-chip VLSIInterconnect under Current Mode Signaling Technique* February 2010 International Journal of Computer Applications 1(10) DOI: 10.5120/220-369

2. Bashirullah, R, Liu, W, Cavin, R, *Delay and power model for current-mode signaling in deep submicronglobal interconnects,* Proceedings of IEEE Custom Integrated Circuits Conference, May 2002, pp. 513 -516

3. Weibing Gong, Wenjian Yu , Yongqiang Lu , Qiming Tang, Qiang Zhou , Yici Cai A *Parasitic Extraction Method of VLSI Interconnects for Pre-Route Timing Analysis*, School of Mathematics and Statistics, Lanzhou University, Lanzhou, China Department of Computer Science and Technology,Tsinghua University, Beijing, China

4. W. Kao, Chi-Yuan Lo,M. Basel, *Parasitic extraction: current state of the art and future trends* ISCAS 2001. The 2001 IEEE International Symposium on Circuits and Systems (Cat. No.01CH37196)

5. Aaron Stillmakera,b , Bevan Baasa . *Scaling equations for the accurate prediction of CMOS device performance from 180 nm to 7 nm* Department of Electrical and Computer Engineering, University of California, Davis, One Shields Ave., Davis, CA 95616, USA b Department of Electrical and Computer Engineering, California State University, Fresno, 2320 E. San Ramon Ave., Fresno, CA 93740, USA

6. Andrew Charest, Ram Achar, Michel Nakhla & *Ihsan Erdin Delay extraction-based passive macromodeling techniques for transmission line type interconnects characterized by tabulated multiport data* Published: 01 August 2008 Volume 60, pages 13–25, (2009)

7. Chen, C., Gad, E., Nakhla, M., & Achar, R. (2007). *Passivity verification in delay-based macromodels of multiconductor electrical interconnects.* IEEE Transactions on Advanced Packaging, 30(2), 246–256.

8. Nakhla, N. M., Dounavis, A., Achar, R., & Nakhla, M. S. (2005). DEPACT: *Delay extraction-based passive compact transmission-line macromodeling algorithm.* IEEE Transactions on Advanced Packaging, 28(1), 13–23.

9. K.V.B.V Rayudu, D R Jahagirdar, P Srihari Rao ,*Testing and Diagnosis of Delay Faults in Finfet VLSI Circuits using Non-Incremental Genetic Algorithm* , International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075 (Online),

Volume-9 Issue-2, December 2019

10. Kuangya Zhai1 , Qingqing Zhang1,2, Li Li3 , Wenjian Yu1, *A 3-D Parasitic Extraction Flow for the Modeling and Timing Analysis of FinFET Structures* Tsinghua National Laboratory for Information Science and Technology, Department of Computer Science and Technology, Tsinghua University, Beijing 100084

11. Aoxiang Tang, Xun Gao, Lung-Yen Chen, *Delay/Power Modeling and Optimization of FinFET Circuit Modules under PVT Variations:* Observing the Trends between the 22nm and 14nm Technology Nodes

12. Yassine Attaoui, Mohamed Chentouf, Zine El Abidine Alaoui Ismaili, *Machine learning application for cell delay accuracy improvement at post-placement stage: :* A case study for combinational cells Volume 90, Issue C Pages 261 – 270 , https://doi.org/10.1016/j.vlsi.2023.02.011 Published: 01 May 2023

13. *Crosstalk Modeling for Coupled RLC Interconnects With Application to Shield Insertion* Junmou Zhang and Eby G. Friedman EEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 14, NO. 6, JUNE 2006

14. Masud H. Chowdhury and Yehea I. Ismai *Analysis of Coupling Noise and it's Scalability in Dynamic Circuits* ,IEEE 2004 CUSTOM INTEGRATED CIRCUITS CONFERENCE, Northwestern University, Evanston, IL 60208, USA

15. H.B. Bakoglu and J.D Meindl, "*Optimal Interconnection Circuits for VLSI* ",IEEE Trans.EletcronDevices,Vol,ED-32,No.5,pp.903-909,May 1985.

16. YangWu,Shien,Boon-Khim,Liew,K.L.Young,C.H.Yu, and S.C. "*Analysis of Interconnect Delay for 0.18µmTechnology and Beyond*" IEEE International Conference Interconnect Technology, May 1999 , pp. 68 - 70

17. D. Zhou, F. P. Preparata, and S. M. Kang, ―*Interconnection delay in very high-speed VLSI,*‖ *IEEE Transaction Circuits Systems*., vol. 38, no. 7,pp. 779– 790, Jul. 1991

18. B. Kahng, A. Masuko, and S. Muddu, ―*Analytical delay models for VLSI interconnects* under ramp input,‖ in Proc. ACM/IEEE International Conference Computer.-Aided Design, Nov. 1996, pp. 30–36.

19. *An Analytical Delay Model for Interconnects* Andrew B. Kahng and Sudhakar Muddu IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, VOL. 16, NO. 12, DECEMBER 1997

20. J. A. Davis and J. D. Meindl, ―*Compact distributed RLC interconnect models—Part I: Single line transient, time delay and overshoot expressions*,‖ IEEE Transaction Electron Devices, vol. 47, no. 11, pp. 2068–2077, Nov. 2000

21. Feng Shi, Xuebin Wu and Zhiyuan Yan, ―*Improved Analytical Delay Models for RC–coupled Interconnects*,‖ IEEE Transaction Very Large Scale Integration (VLSI) Systems, vol. 22, no. 7, July 2014

22. T. Samantam, H. Rahaman, P. Ghosal and P. Dasgupta, "*A Method for the Multi-Net Multi-Pin Routing Problem with Layer Assignment*," 2009 22nd International Conference on VLSI Design, New Delhi, India, 2009, pp. 387-392, doi: 10.1109/VLSI.Design.2009.30.

23. P. -H. Lin, H. -C. Yu, T. -H. Tsai and S. -C. Lin, "*A Matching-based Placement and Routing System for Analog Design,*" 2007 International Symposium on VLSI Design, Automation and Test (VLSI-DAT), Hsinchu, Taiwan, 2007, pp. 1-4, doi: 10.1109/VDAT.2007.373200

## Appendix A

## Conference Paper

This chapter is based on the paper titled "**Modeling of the Effects of Process Variations on UPIO[3:0] Delayline at 12nm FinFET using ELDO,**" which has been submitted to the IEEE on June 27,2025.

In this paper,This study investigates the impact of process variations on the delay characteristics of the UPIO[3:0] delayline implemented in 12nm FinFET technology using ELDO simulations.
The performance of UPIO delayline is extremely important in high-speed digital circuits where timing accuracy is most important. At the 12 nm technology nodes,process variations can have a significant impact on the performance of these delaylines. This paper presents a comprehensive study on the effects of process variation on UPIO delayline using ELDO simulations. The variations in key process parameters such as doping concentration and oxidation thickness are modeled to analyze the effects on delay characteristics. Our simulations show that variations in doping concentration have a significant effect on signal delay and jitter, followed by variation in oxidation damage. These results provide valuable insight into design and manufacturing process optimization to mitigate the negative effects of process variation and improve the reliability and efficiency of semiconductor devices at 12 nm nodes. The key findings are summarized below:

- **Delay Sensitivity to Process Variations**
- **Impact of Inter- and Intra-Die Variations**
- **Statistical Delay Distribution**
- **Simulation Efficiency Using ELD O**

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