

**Design of Low Drop-out Voltage Regulator with
Improved PSRR and Low Quiescent Current**

*A dissertation submitted in partial fulfillment of the
requirement for the award of degree of*

Master of Technology

in

VLSI Design



Submitted By:

Swati Wadhwa

Roll No. 601461029

Under the supervision of:

Dr. Rishikesh Pandey

Assistant Professor, ECED

Thapar University, Patiala

Department of Electronics & Communication Engineering

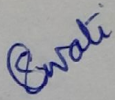
Thapar University, Patiala-147004

CERTIFICATE

I hereby declare that the work which is being presented in this dissertation entitled, “**Design of Low Drop-out Voltage Regulator with Improved PSRR and Low Quiescent Current**” in partial fulfillment of the requirement for the award of degree of Master of Technology in **VLSI Design** submitted in Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of **Dr. Rishikesh Pandey**, Assistant Professor, ECED and refers other researcher’s work which are duly listed in the reference section.

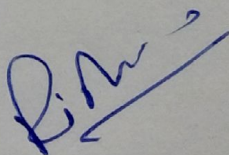
The matter presented in this dissertation has not been submitted in any University/Institute for the award of degree.

Date: 08.07.2016


Swati Wadhwa
601461029

It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

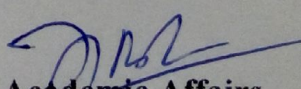
Date: 08.07.2016


Dr. Rishikesh Pandey
Assistant Professor
ECED, Thapar University

Countersigned by:


Head

ECED, Thapar University
Patiala – 147004


Dean of Academic Affairs

Thapar University

Patiala - 147004

ACKNOWLEDGEMENT

First of all, I would like to express my gratitude to **Dr. Rishikesh Pandey**, Assistant Professor, Electronics and Communication Department, Thapar University, Patiala for his patient guidance and support throughout my work. I am truly very fortunate to have the opportunity to work with him. I found his guidance to be extremely valuable.

I am also thankful to Head of the Department, **Dr. Sanjay Sharma** and Program Coordinator Dr. Amit Kumar Kohli of Electronics and Communication Engineering Department for their encouragement and inspiration for the execution of this dissertation work. I would also like to thank my friends who devoted their valuable time and helped me in all possible ways towards successful completion of this work. I thanks all those who have contributed directly or indirectly to this work.

Lastly, I would like to thank my parents for their unconditional support and encouragement.

Swati Wadhera

601461029

ABSTRACT

Portable electronic devices mostly use batteries as their primary source for operation. Hence, longer running batteries or power sources are vital for any portable device. Need of stable voltage supplies have led to development of low drop-out voltage regulators. Low drop-out voltage regulator provides stable regulated output voltage in various operating conditions, which makes it so useful in portable devices. The design of high performance and stable low drop-out voltage regulators is a challenge nowadays with decreasing device sizes and increasing power densities.

In the dissertation, a capacitor-less Low Drop-out Voltage regulator has been designed with improved PSRR and low quiescent current. The proposed circuit is simulated using Cadence in 180nm CMOS technology parameters with the supply voltage of 1.8V. The proposed circuit provides 1.25V as the output voltage with PSRR of -61.5 dB and quiescent current of 290 μ A. For improvement of PSRR, high gain two-stage operational amplifier has been designed with miller compensation and ESR compensation technique. The transmission gate is used in the error amplifier circuit as an active resistor in place of nulling resistor. The vital parameters of LDO have also been compared with existing LDO circuits available in literature.

TABLE OF CONTENTS

CERTIFICATE		i
ACKNOWLEDGEMENT		ii
ABSTRACT		iii
TABLE OF CONTENTS		iv
LIST OF ACRONYMS		vi
LIST OF FIGURES		vii
LIST OF TABLES		viii
ABBREVIATIONS		ix
Chapter 1	INTRODUCTION	1-3
1.1	INTRODUCTION	1
1.2	MOTIVATION	2
1.3	KEY CONTRIBUTIONS	2
1.4	ORGANIZATION OF THE DISSERTATION	2
Chapter 2	LITERATURE SURVEY	4-10
2.1	TOPOLOGIES OF LOW DROP-OUT VOLTAGE REGULATOR	4
	2.1.1 LOW DROP-OUT REGULATOR WITH CAPACITOR	4
	2.1.2 CAPACITOR-LESS LDOS	7
Chapter 3	LOW DROP-OUT VOLTAGE REGULATOR	11-23
3.1	VOLTAGE REGULATOR	11
3.2	BLOCK DIAGRAM OF LDO	12
	3.2.1 ERROR AMPLIFIER	13
	3.2.2 VOLTAGE REFERENCE	13
	3.2.3 FEEDBACK NETWORK	13
	3.2.4 PASS ELEMENT	13
3.3	LOW DROP-OUT VOLTAGE REGULATOR	14

	3.3.1 CMOS OPERATIONAL AMPLIFIER	14
	3.3.2 BANDGAP VOLTAGE REFERENCE	17
3.4	LDO COMPENSATION TECHNIQUES	18
	3.4.1 COMPENSATION USING EQUIVALENT SERIES RESISTANCE	18
	3.4.2 CAPACITIVE FEEDBACK COMPENSATION TECHNIQUE	19
	3.4.3 FEED-FORWARD COMPENSATION TECHNIQUE	20
	3.4.4 MILLER COMPENSATION TECHNIQUE	21
3.5	LDO CIRCUIT PARAMETERS	22
Chapter 4	DESIGN OF PROPOSED LOW DROP-OUT VOLTAGE REGULATOR	24-32
4.1	PROPOSED LDO DESIGN	24
4.2	DESIGN OF ERROR MPLIER	26
4.3	DESIGN OF PMOS PASS ELEMENT	30
4.4	DESIGN OF TRANSMISSION GATE	31
Chapter 5	SIMULATION RESULTS	33-38
5.1	SIMULATION RESULTS OF ERROR AMPLIFIER	33
5.2	SIMULATION RESULTS OF BANDGAP VOLTAGE REFERENCE CIRCUIT	35
5.3	SIMULATION RESULTS OF LDO	36
Chapter 6	CONCLUSIONS AND FUTURE SCOPE	39-40
6.1	CONCLUSIONS	39
6.2	FUTURE SCOPE	39
Chapter 7	REFERENCES	41-45
	APPENDIX I	46-48
	ORIGINALITY REPORT	49-50

LIST OF ACRONYMS

LDO	Low Drop-out Voltage Regulator
DC	Direct Current
PSRR	Power Supply Rejection Ratio
RF	Radio Frequency
RFID	Radio Frequency Identification
OTA	Operational trans-conductance amplifier
EA	Error Amplifier
MOS	Metal Oxide Semiconductor
NMOS	n-channel Metal Oxide Semiconductor
PMOS	p-channel Metal Oxide Semiconductor
FFRC	Fast Feedback Ripple Rejection
CMOS	Complementary Metal Oxide Semiconductor
SoC	System on Chip
IC	Integrated Circuit
CMRR	Common Mode Rejection Ratio
TG	Transmission Gate
SR	Slew Rate
ESR	Equivalent Series Resistance

LIST OF FIGURES

Figure 3.1	Block Diagram of Low drop-out Voltage Regulator	12
Figure 3.2	Operational Amplifiers	14
Figure 3.3	CMOS Operational Amplifier	15
Figure 3.4	Two stages Opamp Hierarchy	16
Figure 3.5	Bandgap Voltage Reference circuit	17
Figure 3.6	LDO with ESR compensation [4]	18
Figure 3.7	Two-stage operational amplifier with capacitive feedback technique	19
Figure 3.8	LDO with Feed-Forward Compensation	20
Figure 3.9	Error Amplifier with Miller Compensation	22
Figure 4.1	Design of the proposed LDO	24
Figure 4.2	Nulling resistor in the compensation network	25
Figure 4.3	Design of error amplifier for the proposed circuit	27
Figure 4.4	Small Signal model of error amplifier	27
Figure 4.5	Basic structure of a Transmission Gate (TG)	31
Figure 5.1	Gain vs. frequency plot of uncompensated error amplifier	33
Figure 5.2	Phase vs. frequency plot of uncompensated error amplifier	34
Figure 5.3	Gain vs. frequency plot of compensated error amplifier	34
Figure 5.4	Phase vs. frequency plot of compensated error amplifier	35
Figure 5.5	Output Voltage of Bandgap Voltage Reference Circuit	35
Figure 5.6	Output voltage vs. input voltage	36
Figure 5.7	Output voltage vs. load current	36
Figure 5.8	PSRR plot without improvement technique	37
Figure 5.9	PSRR plot of compensated LDO	37

LIST OF TABLES

Table 2.1	Comparison of different topologies with external capacitor LDO	7
Table 2.2	Comparison of different topologies of Capacitor-less LDO	9
Table 3.1	Comparison between LDO and Switching regulators	12
Table 3.2	Comparison of different topologies of CMOS Opamp	17
Table 4.1	Design Specifications of the proposed LDO circuit	25
Table 4.2	Design Specifications of the error amplifier	26
Table 4.3	Design Specifications of the PMOS pass element	31
Table 5.1	Comparison of LDO architectures in literature with the proposed LDO	38

LIST OF SYMBOLS

V_{DD}	Supply Voltage
W	Channel Width
L	Channel Length
g_m	Transconductance
V_{REF}	Reference Voltage
C	Capacitance
R	Resistance
V_{in}	Input Voltage
V_{OUT}	Output Voltage
Gnd	Ground
Z_{OUT}	Output Impedance
$C_{O\Box T}$	Output Capacitance
C_c	Compensation Capacitance
C_C	Compensation Resistance
R_{null}	Nulling Resistance
g_{ds}	Drain-to-Source Transconductance
C_{gd}	Gate-to-Drain Capacitance
C_{db}	Drain-to-Bulk Capacitance
C_{gs}	Gate-to-Source Capacitance
C_{ox}	Oxide Capacitance
C_L	Load Capacitance

Chapter 1

INTRODUCTION

1.1 INTRODUCTION

Portable devices such as mobile, laptop, calculator, etc. have become so popular and so has become the need of keeping them charged for longer times. A device cannot perform without energy and needs a stable and powerful supply voltage. With technology improvements and device scaling, it becomes important to manage power along with other factors such as output voltage, stability, etc. [1]. The low power requirement of devices has made possible the economic use of battery as a power source [2]. The power sources available such as generators, batteries, cells, transformers, and other supplies have inbuilt voltage and current variations under wide range of operating conditions [3]. Regulators have become an important part of power management systems with the growing demand of portable battery operated products. Current efficiency is very important in low load current conditions as high quiescent current highly affects the performance of the device and hence the battery life. On the other hand, current efficiency improves and is high in case of high load current conditions because quiescent current is lower than load current [4].

It is desirable to have a dc power supply giving stable power output for various operating conditions. DC-DC converter provides stable voltage supply for noisy environments but need large battery filters, which reduce the battery voltage ripples [5]. Need of high ripple rejection battery sources have alleviated the development of low drop-out voltage regulator (LDO). It has all the properties that match the need of stable power supplies with high performance portable, automotive and biomedical applications [6].

LDOs work at low power inputs and low load current. Low power consumption makes them ideal for use in portable low energy requirement circuits.

1.2 MOTIVATION

The motivation to study and develop a better LDO came from the fact that how important it is nowadays the requirement of portable devices to be having longer shelf life and better operation. There are other alternatives of LDO available already such as switching regulators, dc-dc converters, etc. The advantage of LDO over these circuits is that development of LDO is less complex and less expensive than others available. Switching regulator provide wide range of output voltage, greater or lesser than the input voltage but LDO, binding to its specific use, provides output voltage less than the input supply voltage within a specified required range. Also, switching regulators are more prone to noise and disturbances than LDO. To make LDOs even less prone to power supply ripples, LDOs with high power supply rejection ratio over wide range of frequency has been developed.

1.3 KEY CONTRIBUTIONS

The major work that has led to the success of the proposed circuit is as follows:

1. Design and simulate an error amplifier i.e. two stage operational amplifier with higher gain and better stability using transmission gate as an active resistor.
2. Design and simulate the PMOS Low drop-out voltage regulator with improved PSRR and low quiescent current.

1.4 ORGANIZATION OF THE DISSERTATION

The organization of this dissertation is as follows:

Chapter 1: This chapter discussed the major concerns related to low power, development of LDO, its motivation and the key contributions to this dissertation.

Chapter 2: This chapter introduces low drop-out voltage regulator. It consists of its block diagram, explains each block and its features and usability in the LDO structure. This chapter also introduces the various technical specific parameters related to LDO.

Chapter 3: This chapter consists of literature reviews of different topologies of LDO that have been studied to form the proposed circuit. This chapter also discusses some compensation techniques.

Chapter 4: This chapter addresses the proposed circuit and the design process used to construct the same with all the design specifications.

Chapter 5: It contains the simulation results of the basic building blocks and the proposed LDO structure. It shows the output plots for improved dc gain and PSRR for the proposed LDO.

Chapter 6: In this chapter, the conclusion of the dissertation and the future scope of LDO have been suggested.

CHAPTER 2

LITERATURE SURVEY

This chapter discusses the recent researches and developments [7-25] in the field of LDO reported by various authors in literature. A succinct review based on the study is as follows:

2.1 TOPOLOGIES OF LOW DROP-OUT VOLTAGE REGULATOR

LDO has various topologies based on the type of pass element used – NMOS, PMOS and CMOS. Also, LDOs can be differentiated on the basis of need of external capacitors in the LDOs – with capacitor LDOs and capacitor-less LDOs.

2.1.1 LOW DROP-OUT REGULATORS WITH CAPACITOR

Crepaldi et al. [7] have presented bio-implanted systems involving power supply management by LDO. Activation energy for the classic structure of LDO is from a RF link using RFID tag. The proposed design has low power consumption, reduced area and almost no use of external discrete components.

Mora et al. [8] have suggested a circuit that focuses on reducing the quiescent current and hence increased battery life under low drop-out voltages. Power supply systems are connected to regulators for reducing noise and voltage fluctuations that can cause power consumption or reduced battery life.

Chung-Hsun Huang et al. [9] suggested an LDO design which uses operational trans-conductance amplifier (OTA) as an error amplifier (EA) along with gain boosting techniques. A power noise cancellation mechanism is formed which minimizes the size of power MOS transistor. These advantages allow the proposed LDO regulator to operate over a wide range of operating conditions while achieving high current efficiency. The authors have improved the transient response at low

quiescent current values. They have achieved low quiescent current, high PSR, faster and stable operation.

Vanama et al. [10] presented an LDO giving output of 1V with input supply voltage to be of around 1.2 V. The authors have introduced a current-sourcing PMOS at the output stage that is to be pulled to ground to be in saturation region all the time. The existing topology is modified by adding a common source stage of amplifying device acting as a pull down device.

Aminzade et al. [11] proposed a high order temperature controlled low drop-out voltage source (LDVS). It operates at very low order supply voltages and gives sufficient output load current even with minimal consumption of input current. The authors have suggested an alternative to conventional LDO and band-gap reference issues. They have compared the values of calculated circuit parameters of LVDS with the values of other researchers with conventional LDO and it has shown improvement in most of the parameters. A line-voltage compensation technique reduces the line sensitivity by a factor of three.

Giustolisi et al. [12] have analyzed that PMOS LDOs are more efficient than NMOS LDOs but needs supply voltage to be always at drain voltage V_{DD} . The proposed architecture used the NMOS as the pass element with the addition of a charge pump. The NMOS LDO with charge pump makes use of dynamic biasing technique for driving the gate of output transistor.

Patel et al. [13] analyzed that System on chip solutions have limited on chip capacitance that induces noise while switching activities. The proposed architecture discusses a bipolar current mode dual loop LDO that attenuates the high frequency ripple by introduced because of switching. The authors have analyzed the stability of

the proposed structure and suppressed the supply ripple by 6 times thus, preventing the switching noise.

Dokania et al. [14] showed interest in only property of load regulation of low drop-out regulators. They discussed a method for cancelling load regulation while monitoring load current for dynamically adapting the value of reference voltage. The proposed structure drops load regulation from 2.5% to mere 0.2% without disturbing system stability.

El-Nozahi et al. [15] presented a feed forward ripple cancellation (FFRC) technique for low drop-out regulator that helps in achieving high power supply rejection ratio PSRR over a wide range of frequencies. The proposed architecture is constructed on to achieve a better PSRR under low load currents. The quiescent current observed is also low.

Garimella et al. [16] proposed the architecture with internal frequency compensation of low drop-out voltage regulator with the help of a small-value, ESR-independent output capacitor. A common gate transistor acting as a current buffer, an optional series resistance and a compensation capacitor resulting in dominant pole and stable LDO design is implemented. A power good feature is also included which is used for interfacing a microprocessor and LDO.

Table 2.1 compares the different LDO architectures in terms of technology parameters. High PSRR has been achieved in and good load regulation is achieved in [8] as compared to other architectures. Sufficiently low quiescent current has been achieved in [16]. Architectures in [7,9] have tried to keep a trade off between technology parameters.

Table 2.1 Comparison of different topologies with external capacitor LDO

Design Parameters	[7]	[8]	[9]	[10]	[15]	[16]
CMOS Technology	0.3 μm	2 μm	90 nm	-	0.13 μm	0.5 μm
Supply Voltage	-	1.2 V	1V	1.2V	>1.15V	-
PSRR	-	-	> 48 dB	-35 dB	>-56 dB	-58 dB
Load Current	0.5 mA	18/50mA	100 mA	-	-	100 mA
Load Regulation	13 mV/mA	19mV/50 mA	0.28/0.24	3%	1.2mV/2 5 mA	0.001%
Line Regulation	39 mV/V	4 mV/3.8 V	-	-	-	0.05%
Quiescent Current	-	23 μA	60 μA	0.5 mA	50 μA	111 μA

2.1.2 CAPACITOR-LESS LOW DROP-OUT VOLTAGE REGULATORS

The external capacitors connected on chip incur extra area, cost and power dissipation, leads to inability of SoC solutions, and increase the pin count of the IC. Therefore, the external capacitor is substituted by an internal capacitor.

Milliken et al. [17] have studied that LDOs with external discrete components such as capacitor or resistance becomes bulky in construction and also consume more area. This architecture proposes a system on chip (SoC) solution to external capacitor bulky low drop-out voltage regulators with a capacitor-less LDO architecture. Proposed LDO architecture improved the transient response. The architecture not only removes the external capacitor but also guarantees the stability under all operating conditions. A comparison is made with other capacitor-less designs showing the best results in the proposed architecture with low drop-out voltage and fast settling time best suited for SoC applications.

Shirahatti et al. [18] have presented a LDO with capacitor-less approach improving line and load regulation of the circuit with fast transient loop implementation. The proposed design improves stability and gives high performance in terms of PSRR and slew rate, which are significant performing parameters for an LDO.

Torres et al. [19] have presented a comparative study between different architectures for capacitor-less LDO as damping factor, Q – Reduction, Voltage subtractor, trans-impedance, and differentiator which, suggested that no single architecture or structure is good for all LDO circuit parameters and hence the user can choose as per the requirements. There are always trade-offs between two circuit parameters that a designer has to take into account for the application.

Chang-Joon Park et al. [20] discusses a technique to reduce effects of power supply noise leakage on output voltages over different frequency limits. The approach used is also capacitor-less LDO with an internally compensated achievement of high PSRR.

Guo et al. [21] proposed a design with capacitor-less LDO concept to utilize chip area efficiently. The structure is presented to make use of damping control frequency compensation technique with first order high pass feedback network. Proposed structure has stability for wide ranges of capacitances.

Abbasi et al. [22] has proposed a design to achieve high PSRR with capacitor-less approach. The proposed structure has achieved stability for wide range of load current and full load current as well.

Leo et al. [23] has proposed a architecture to achieve high peak load current. The circuit proposed also used capacitor-less approach for LDO. The proposed circuit stabilizes and achieves high PSR along high peak load current. The reference circuit

used in the proposed design is a nano-power bandgap circuit having low power consumption and has no resistor. Moreover, the capacitor-less makes the circuit even more effective and stable than conventional LDOs.

Roldan et al. [24] have proposed a LDO design with high power supply rejection ratio with the ability to drive larger capacitive loads. A technique of compensation is used with wide bandwidth capacitance multiplier. Its frequency response is similar to an externally off chip capacitor compensated LDO.

Kim et al. [25] proposed a LDO with low quiescent current. It employs a circuit of ultra low quiescent class AB error amplifier. It also performs slew rate enhancement to reduce circuit compensation and improving transient response over CMOS process.

Table 2.2 Comparison of different topologies of Capacitor-less LDO

Design Parameters	[19]	[20]	[21]	[22]	[23]	[24]
Technology	0.18 μ m	0.18 μ m	90nm	0.18 μ m	0.13 μ m	0.18 μ m
Supply Voltage	2.2V	1.8V	1.2V	3V	1.2V	1.8V
Output Voltage	1.4V	1.6V	-	1V	0.9V	1.2V
Line Regulation	0.3mV/V	-	3.78mV/V	370 μ V/V	-	-
Load Regulation	0.22mV/mA	200mV/mA	0.1mV/mA	0.01173%/mA	-	4mV/mA
PSRR	-	-50dB	-	-40dB	-95dB	-41dB

Table 2.2 compares the different capacitor-less LDO architectures available in literature. High PSRR with least output voltage as compares to other architectures has been achieved in [23]. Good load regulation has been achieved in [21] and regulation of 1.6V, the highest of all other architectures has been achieved in [20].

Chapter 3

LOW DROP-OUT VOLTAGE REGULATOR

The low drop-out voltage regulators are vital blocks for power supply in portable electronic devices. Low drop-out voltage regulator comprises of four sections, an error amplifier, a bandgap reference voltage, feedback network and a pass transistor. In this chapter, these building blocks and performance parameters of Low drop-out voltage regulator are discussed.

3.1 VOLTAGE REGULATOR

A voltage regulator provides a constant output voltage by adjusting its internal resistance to any changes occurring at load stage to provide a stable regulated output constantly [26]. The internal resistance should be much less than the load resistance in order to get stable output voltage. Under no-load conditions, the output voltage is same as input voltage. Altering load resistance changes the output voltage and hence produces an error voltage output [26]. The output voltage error is defined as percentage difference between maximum output voltage under no load condition and maximum output voltage under load conditions.

The linear voltage regulator having internal resistance much lesser than load resistance regulates voltage only for a specified load resistance. As soon as the load resistance is altered, the circuit fails to regulate the output voltage. There arises need of a circuitry that senses the change in the load resistance (increasing or decreasing) and changes the internal resistance accordingly to produce stable output voltage for various load values. The linear voltage regulators are of two types [27] – standard linear regulators and Low drop-out voltage regulators. A standard linear regulator or switching regulators are conventional voltage regulators, which regulate the output voltage for a fixed load and fixed internal resistance values. A low drop-out voltage regulator is one that regulates output voltage even when it is almost equal to input supply voltage [26]. The basic difference between LDO and switching regulator is of the pass element and dropout voltage or headroom they require to maintain output voltage at a certain level. The Table 3.1 shows the basic comparison between LDO

and switching regulators. LDOs are easy, simple to design and inexpensive way to regulate voltage in electronic devices.

Table 3.1 Comparison between LDO and Switching regulators [32]

Regulators	Linear	Switching
Function	Only steps down	Step-up, Step-down, inverts
Efficiency	Low to medium	High
Waste Heat	High	Low
Complexity	Low	Medium to High
Size	Low to medium	Larger than linear
Total Cost	Low	Medium to High
Ripple/Noise	Low	Medium to High

3.2 BLOCK DIAGRAM OF LDO

The block diagram of LDO is shown in Figure 3.1. Main building blocks of LDO are shown by dotted lines in the Figure 3.1, which consists of an error amplifier, voltage reference (V_{REF}), feedback network ($R1$ and $R2$) and pass element. The upcoming sections will be describing them in detail.

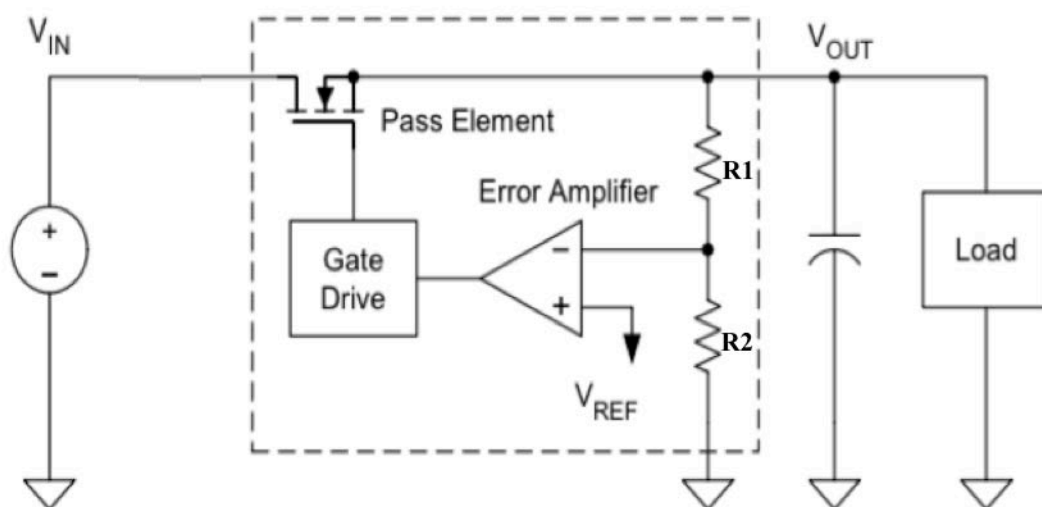


Figure 3.1 Block Diagram of Low drop-out Voltage Regulator [31]

3.2.1 ERROR AMPLIFIER

The error amplifier is an electronic circuit that calculates the error based on the inputs. It is commonly used in feedback unidirectional voltage control circuits where a portion of the output voltage of the circuit is fed back to the main circuit and then compared to a reference voltage. The difference between the two voltages generates an error voltage designed in such a manner to move the output voltage to the desired value. The output voltage of error amplifier is given as

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \times V_{REF}$$

(3.1)

3.2.2 VOLTAGE REFERENCE

This is usually of the bandgap-type, since this kind of reference has the ability to operate on low supply voltages, and provides enough accuracy and thermal stability to meet the less-stringent performance requirements of regulators. Bandgaps typically have an initial error of 0.5% – 1.0% and a temperature coefficient of 25 – 50 ppm/°C.

3.2.3 FEEDBACK NETWORK

The feedback network is for feeding back a portion of the output voltage back to the error amplifier circuit so as to calculate error between the reference voltage and the output voltage and bringing the output voltage to the desired value. Since reference voltage is always fixed for the error amplifier, the only way to adjust the fed back voltage as per the output voltage is by adjusting the ratio of feedback resistor divider $R2/R1$.

3.2.4 PASS ELEMENT

Its function is to boost the output-current capabilities of the error amplifier to the higher levels required by the load. This involves transferring large currents from the source V_{in} to the load under the low-power supervision of the error amplifier.

3.3 LOW DROP-OUT VOLTAGE REGULATOR

As shown in Figure 3.1, the basic building blocks of LDO are error amplifier, voltage reference circuit, feedback network and pass element. This section will discuss the requirements and design of error amplifier and voltage reference in detail.

3.3.1 CMOS OPERATIONAL AMPLIFIER

The error amplifier used to design the LDO structure in this work is a 2-stage CMOS operational amplifier (opamp) [28]. Figure 3.2 shows the basic structure of an operational amplifier. An opamp is a DC-coupled high-gain electronic voltage amplifier with a differential input and, usually, a single-ended output [29]. Operational amplifiers generally have a very large gain so that when a negative feedback is applied to such amplifiers the closed loop gain then becomes independent of the large gain of opamp. The opamps are made with a sufficiently large so as to have a proper negative feedback, larger the gain more efficient will be negative feedback opamp. With negative feedback, the concerns like gain, stability, and bandwidth become little dependent on internal circuitry and temperature coefficients.

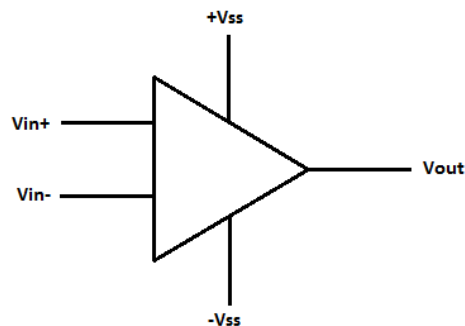


Figure 3.2 Operational Amplifiers

Operational amplifiers have two general configurations based on input-output relation namely inverting and non-inverting amplifiers. Inverting amplifier has its input on the negative terminal and non-inverting terminal has its input on the positive terminal. Inverting amplifier inverts the input i.e. the output is out of phase of the input by 180 degrees but non-inverting output is in phase with the input. Opamps are among the

most widely used electronic devices today, being used in a vast array of consumer, industrial, and scientific devices.

The opamp has ideally is considered to be infinite loop gain, PSRR, bandwidth, and zero output impedance, noise. These ideals summarize the situation of operational amplifier that the closed loop out does whatever is required to bring down the voltage different for both the inputs to zero and the input draws no current. But in real life, none of these ideals are actually true. The design can be so made to achieve high voltage ranges, CMRR, PSRR and very less output impedance and noise. Figure 3.3 shows the basic two-stage opamp.

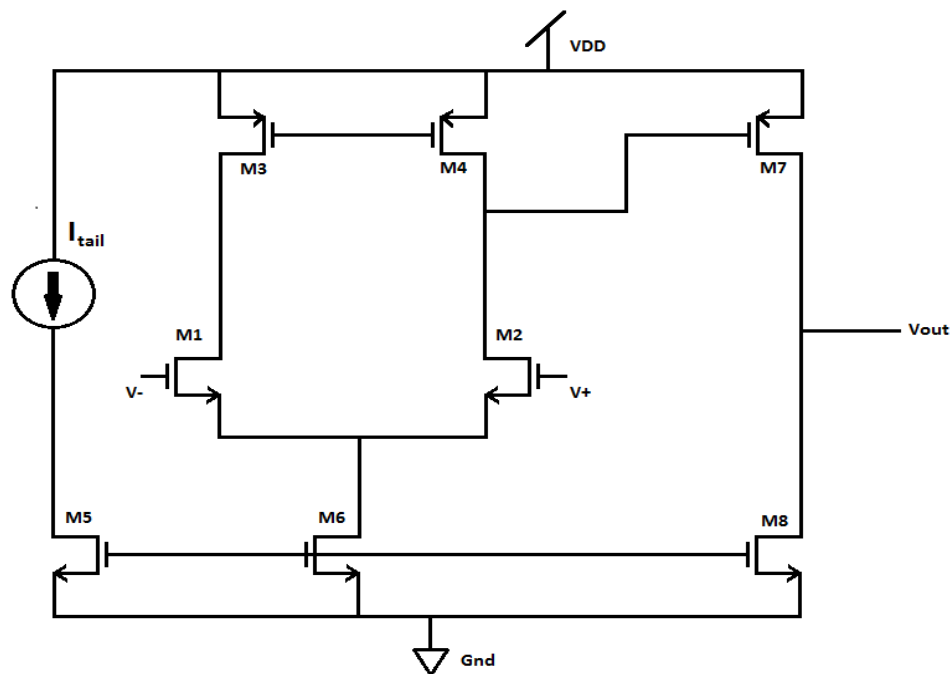


Figure 3.3 CMOS Operational Amplifier

This two-stage topology of CMOS operational amplifier provides good output voltage, high open loop gain, good common mode range, slew rate and CMRR. Variations in opamp circuit with addition of cascade or folded-cascade configuration improve certain features but degrade voltage swing.

A two-stage operational amplifier consists of cascading of current to voltage and voltage to current converting stages [28]. A current to voltage stage is known as load stage and a voltage to current stage is known as trans-conductance stage. The cascading of stages is done so as to improve the gain after the last stage. Figure 3.4 shows the basic hierarchy of two-stage opamp.

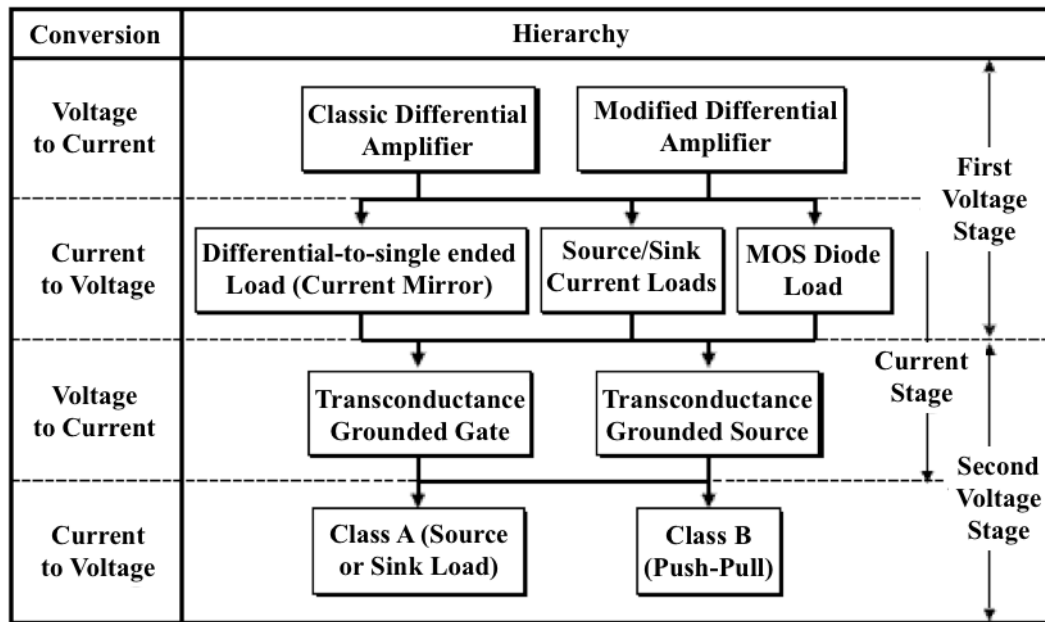


Figure 3.4 Two stages Opamp Hierarchy

First stage in opamp is a high gain differential amplifier giving the dominant pole to the system. For second stage, a common source amplifier also known as unity-gain source follower circuit is used with high output voltage swing. Table 3.2 shows the comparison between different topologies of CMOS operational amplifier.

The two-stage opamp used here introduces an important concern of compensation. Since frequency Compensation techniques maintains the required stability of the circuit in negative feedback condition. A number of frequency compensation techniques are proposed to stabilize a closed loop two-stage amplifier [30][31]. We will discuss the compensation techniques in this chapter at a later stage. In LDO, gain and compensation are used to improve the power supply rejection ratio and hence improving the performance of the LDO. Compensation improves stability but affect

other specification, a good approach is to design an opamp with a frequency compensation that provides good stability and meets other specifications as well.

Table 3.2 Comparison of different topologies of CMOS Opamp

Topologies	Gain	Speed	Output Swing	Noise	Power Consumption
Telescopic	Medium	High	Low	Low	Low
Folded-Cascode	Medium	Medium to High	Medium	Medium	Medium
Multi - Stage	High	Low	High	Low	Medium
Gain-Boosted	Medium to High	Medium	Medium	Medium	High

Table 3.2 compares the different topologies available in literature for the operational amplifier. In this work, two-stage operational amplifier is chosen because it has the highest output swing and required gain boosting for the design of the error amplifier.

3.3.2 BANDGAP VOLTAGE REFERENCE

The voltage reference circuit used in this work is bandgap voltage reference. As the name suggests, this is a voltage reference circuit based on bandgap voltage of Silicon i.e. 1.1 eV. This circuit has the ability to work at different and low supply voltages. It provides enough thermal stability and accuracy required to drive a voltage regulator. Bandgaps have a minimal error of 0.5%-1.5% and a temperature coefficient of 25 – 50 ppm/C. Figure 3.5 shows the circuit for bandgap reference.

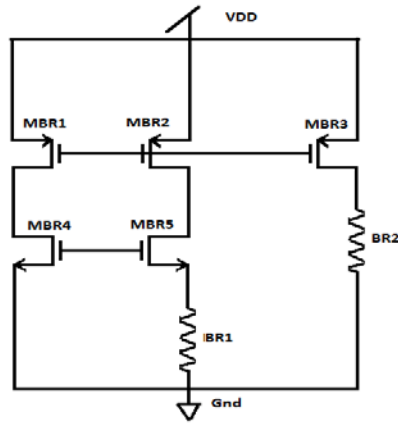


Figure 3.5 Bandgap Voltage Reference circuit

Bandgap reference voltage circuits are temperature independent. A voltage is generated proportional to absolute temperature current in first resistor BR1. This current is then used to generate the other voltage in another resistor BR2.

The voltage generated using proportional to absolute current is complementary to absolute temperature. Choosing the correct ratio and values for resistors (BR1 and BR2), the first order effects of dependency on temperature of diode and proportional to absolute current current will cancel out. The voltage at the output is received of about 1.2-1.3 V. In the proposed circuit here and other LDO circuits employing bandgap reference for CMOS operational amplifier have output voltage fixed at 1.25 V.

3.4 LDO COMPENSATION TECHNIQUES

In various LDO designs, PMOS is used as pass element. Its gate is connected to the output of the error amplifier to sense the variation in the output and bringing it to the level of required voltage. The pass elements have high output impedances and hence the output pole location is dependent on it. The location of this pole is important to analyze the stability and load variations. To minimize this, some compensation techniques are required. The various compensation techniques referred in literature [4, 32-36] are discussed as follows.

3.4.1 COMPENSATION USING EQUIVALENT SERIES RESISTANCE

The equivalent series resistance (ESR) compensation technique is shown in Figure 3.6. LDO uses the output capacitor for improving the stability.

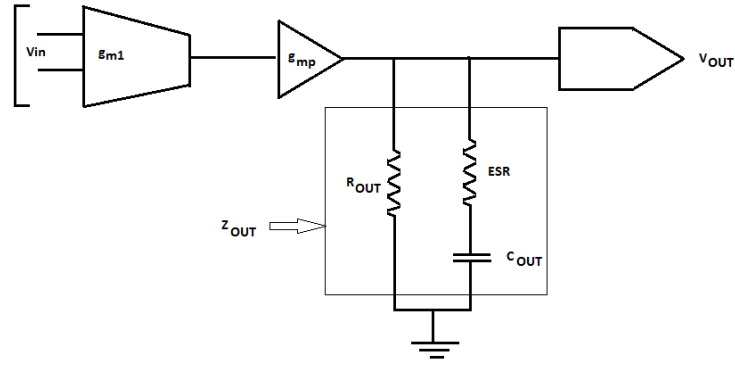


Figure 3.6 LDO with ESR compensation [4]

The internal resistance of the capacitor C_{OUT} is represented by ESR. The equivalent output impedance is

$$Z_{OUT} = \frac{R_{OUT} \cdot (1 + sC_{OUT} \cdot ESR)}{1 + sC_{OUT}(R_{OUT} + ESR)} \quad (3.2)$$

From the equation 3.2, it is obvious that the output impedance has a zero in the system due to ESR. This introduced zero decreases the excess negative phase shift. The ESR frequency is inversely proportional to the output capacitor (C_{OUT}) and the value of ESR zero frequency is

$$f_{ZERO} = \frac{1}{2\pi \cdot C_{OUT} \cdot ESR} \quad (3.3)$$

In this technique, the output capacitor is required to be of an appropriate value to match with ESR and alleviate stability and reduce oscillations [4, 32].

3.4.2 CAPACITIVE FEEDBACK COMPENSATION TECHNIQUE

The equivalent series resistance (ESR) added in the output path in series with the capacitance makes the circuit bulky. The compensation using capacitive feedback is required to omit the requirement of ESR in the circuit for compensation. This technique adds an internal left hand side zero and pole to compensate the LDO. It is

generally used nowadays for 2-stage operational amplifiers. The Figure 3.7 shows the design of LDO with this capacitive feedback compensation technique.

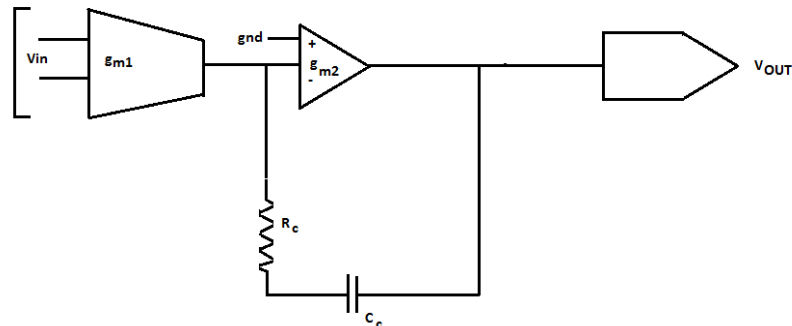


Figure 3.7 Two-stage operational amplifier with capacitive feedback technique [33]

From the Figure 3.7, the zero frequency without zero resistance (R_C) is given as

$$f_Z = \frac{1}{2\pi \cdot C_c} \quad (3.4)$$

The location of zero in the feedback circuit including zero resistance R_C is given as

$$f_Z = \frac{1}{2\pi \cdot C_c \cdot \left(\frac{1}{g_{m2}} - R_C\right)} \quad (3.5)$$

Capacitive feedback paths enable the non-dominant complex poles of the amplifier to be located at high frequencies for bandwidth extension under low power condition [34]. Requirement of ESR rigorous compensation method is eliminated and a new implementation of compensation is achieved [33].

3.4.3 FEED-FORWARD COMPENSATION TECHNIQUE

Feed-Forward compensation technique is widely used for LDO designs. In this style of compensation, a feed-forward capacitor is added across feedback path, between the feedback signal and the output path as shown in Figure 3.8.

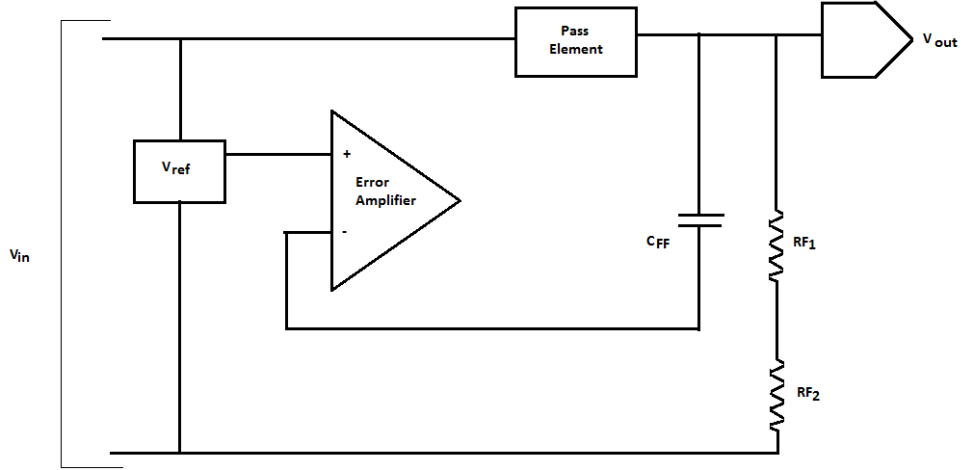


Figure 3.8 LDO with Feed-Forward Compensation

R_{F1} , R_{F2} and C_{FF} form a pole zero pair and the pole zero pair frequency is given by

$$f_{ZERO} = \frac{1}{2\pi \cdot C_{FF} \cdot R_{F1}} \quad (3.6)$$

$$f_{POLE} = \frac{1}{2\pi \cdot C_{FF} \cdot (R_{F1} \parallel R_{F2})} \quad (3.7)$$

The pole zero pair created is more significant than pole zero created in compensation techniques discussed in section 3.4.1 and 3.4.2. The zero is responsible for beneficial phase lead and the pole is responsible for the phase lag in the circuit. The both pole and zero cancel out each other lag and lead since they are both at equal and opposite frequency parameters. To improve the unity gain bandwidth, this pair of pole and zero must be at unity gain frequency [35]. From equations (3.6) and (3.8), it is observed clearly that when R_{F2} is much less than R_{F1} , the pole-zero pair will be much far apart from each other leading to better and maximum phase compensation for the LDO circuit. When R_{F1} is reduced coming close to R_{F2} , the pole-zero pair actually gets closer minimizing the effect of compensation on LDO and hence affecting the phase margin. Therefore, high value of C_{FF} and larger ratio of R_{F1} and R_{F2} is required to make this feed-forward compensation technique effective and successful. The R_{F1}

and RF_2 also help in regulation of the output voltage. With larger values of the feedback resistance, the quiescent current can be reduced and improvement in the efficiency of the circuit can be achieved [36].

3.4.4 MILLER COMPENSATION TECHNIQUE

Few electronic amplifiers exploit the technique of pole splitting for the frequency compensation. A capacitor is introduced between the input and the output sides of the amplifier. This insertion of a capacitor known as compensation or coupling capacitor, results in shifting the pole lowest in frequency (input pole) to at a even more low frequency and the other pole (output pole) to a higher frequency. This pole splitting improves the stability and the step response of the system but degrades the speed [37]. Figure 3.9 shows the error amplifier with the addition of R_L and C_C added for miller compensation technique.

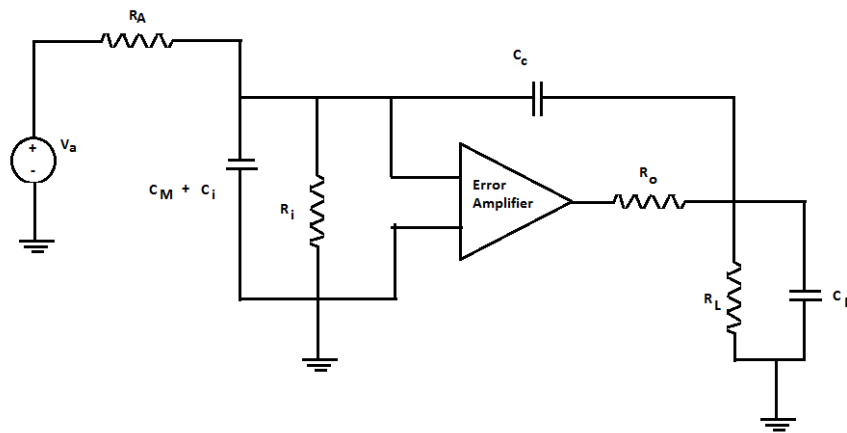


Figure 3.9 Error Amplifier with Miller Compensation [37]

Frequency f_1 of first pole with $C_C = 0$ is

$$f_1 = \frac{1}{2\pi C_i (R_A/R_i)} \quad (3.8)$$

Frequency f_1 of first pole with introduction of C_C

$$f_1 = \frac{1}{2\pi (C_M + C_i) (R_A/R_i)} \quad (3.9)$$

which is lower than initial frequency of the pole when $C_C = 0$.

The amplifier is given a high frequency output pole by addition of the load resistance R_L and load capacitance C_L with the time constant $R_o || R_L$. The shifting of the pole to higher frequency is caused due to compensation capacitor C_C . It alters the frequency dependency of the output voltage divider.

3.5 LDO CIRCUIT PARAMETERS

The following are the parameters that define the LDO performance and behavior [38].

- **Dropout Voltage**

This is the difference between minimum input supply voltage for which the output is regulated and the output voltage. It actually informs about the minimum voltage required at the input to maintain the output in the regulated region. Dropout voltage is determined by the on resistance of the pass element and output current of the LDO.

- **Output regulated voltage range**

This is the output voltage variation the regulator guarantees. When output voltage is in this range, it is said to be in regulation.

- **Output Current Range**

This is the output current handling capability of the regulated output voltage.

- **Load regulation**

This is the variation in output voltage as current moves from minimum to maximum.

$$\text{Load Regulation} = \frac{\Delta V_o}{\Delta I_o} \quad (3.10)$$

where, ΔV_o is change in output voltage and ΔI_o is change in output current.

- **Line regulation**

This is the variation in output voltage as supply voltage is varied from minimum to maximum.

$$\text{Line regulation} = \frac{\Delta V_o}{\Delta V_i} \quad (3.11)$$

where, ΔV_o is change in output voltage and ΔV_i is change in input voltage.

- **PSRR**

Power Supply Rejection (or ripple rejection) ratio is a measure of the ac coupling between the input supply voltages on the output voltage.

- **Output Capacitor range**

This is the specified output capacitance the regulator is expected to accommodate without going unstable for a given load current range.

- **Range of Stable ESR**

An LDO regulator would require an output capacitor with an output equivalent series resistor (ESR) to stabilize the control.

CHAPTER 4

DESIGN OF PROPOSED LOW DROP-OUT REGULATOR

This chapter proposes the low drop-out voltage regulator for better PSRR with improved stability and low quiescent current. This chapter is divided in various sections. Section 4.1 discusses the proposed circuit and its design specifications. Section 4.2 discusses the construction and designing of LDO circuit elements such as error amplifier, bandgap reference, and pass element.

4.1 PROPOSED LDO DESIGN

The proposed LDO is developed for achieving high PSRR with improved stability and low quiescent current as compared to reported LDOs in literature. In general improving PSRR comes with the cost of stability. The method employed in the proposed circuit to improve PSRR is improvement of open loop gain and stability of error amplifier using optimized length of the transistor, miller compensation technique and equivalent series resistance (ESR) compensation technique. The circuit diagram of proposed LDO is shown in Figure 4.1.

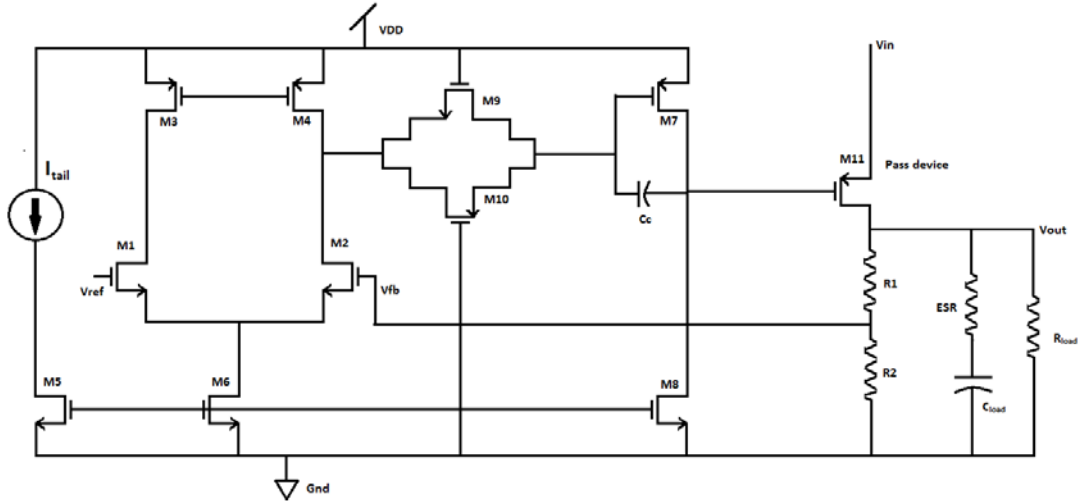


Figure 4.1 Design of the proposed LDO

The output of the error amplifier fed to pass element PMOS is proportional to its gate capacitance so as to generate an output voltage as per the error voltage generated by the error amplifier. The transistor M1-M8 is used to form the error amplifier, M9–M10 form the transmission gate, M11 is used as the pass transistor. The resistors R1 and R2 form the feedback network for closed loop operational amplifier.

Table 4.1 Design Specifications of the proposed LDO circuit

Circuit Parameters	Specifications
Technology	0.18 μm
Input Voltage Range	1.0 - 1.8 V
Power Supply	1.8 V
Gain	> 60dB
Phase Margin	> 65 degree
UGB	10 MHz
Load Current	50mA
Dropout voltage	< 200mV
Slew Rate	5 V/ μs

Figure 4.2 shows the basic structure of error amplifier with nulling resistor. The nulling resistor R_z is used in the circuit for compensation along with C_c to improve the stability. In the proposed design, the nulling resistor is replaced by a transmission gate to reduce the effect of right hand plane zero in the transfer function of the error amplifier.

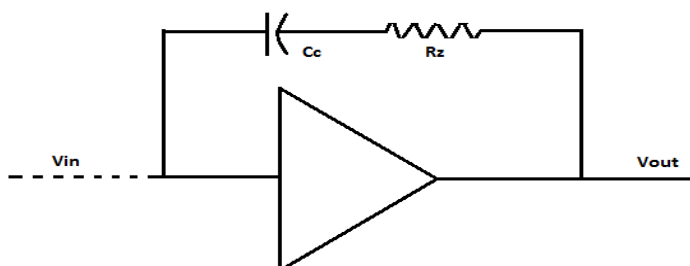


Figure 4.2 Nulling resistor in the compensation network

4.2 DESIGN OF ERROR AMPLIFIER

As discussed in section 3.1, the basic building block of an LDO is error amplifier. A small portion output voltage fed back from the feedback network to the input of error amplifier where it compares this voltage with reference voltage and generates an error signal or voltage if there is a difference between reference and output voltage. The main purpose of the error amplifier is to generate a signal that switches the pass element ON and hence brings the output voltage to the desired value. The Table 4.2 shows the design specifications for the error amplifier circuit.

Table 4.2 Design Specifications of the error amplifier

Circuit Parameters	Specifications
Technology	0.18 μ m
Power Supply	1.8 V
Gain	> 60dB
Phase Margin	> 65 degree
UGB	10 MHz

A two-stage error amplifier designed to meet specifications mentioned in Table 4.2 for the proposed circuit is shown in Figure 4.3. The error amplifier consists of a NMOS differential pair (M1-M2) with PMOS current mirror load (M3-M4).

The design specifications so chosen are somewhat for an ideal error amplifier such as high gain, low output impedance and greater than 60 degree phase margin. A phase margin greater than 45 degrees is also good for a circuit but more than 60 degrees confirms stability.

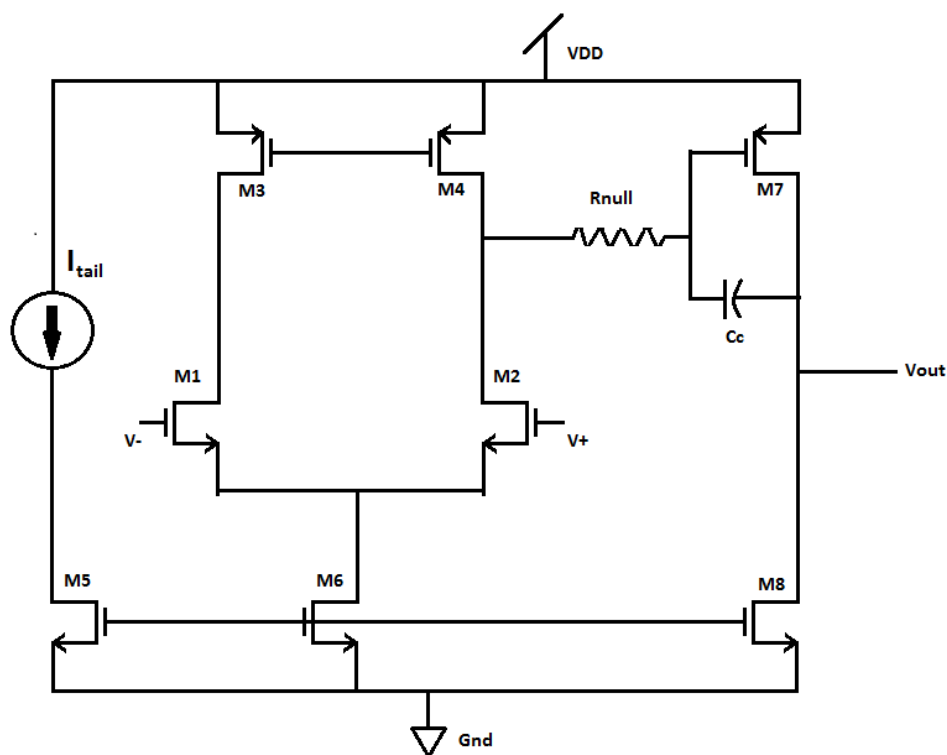


Figure 4.3 Design of error amplifier for the proposed circuit

The small signal model of the error amplifier is shown in the Figure 4.4. All the transistors are required to be in the saturation region for proper operation.

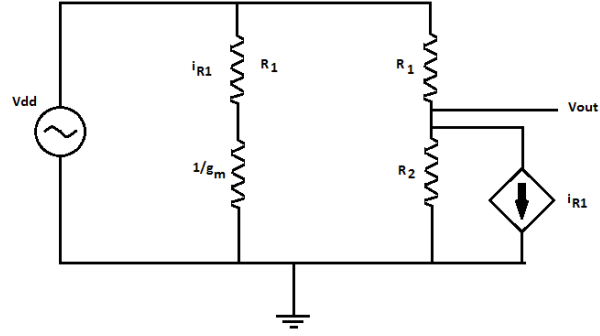


Figure 4.4 Small Signal model of error amplifier

As per small signal model, the amplifier gain is given by

$$A_v = A_1 \times A_2 \quad (4.1)$$

where A_1 is the gain of first stage and A_2 is the gain of second stage of error amplifier.

$$A_1 = -g_{m1} (r_{o2} || r_{o4}) = -g_{m1} R_1 \quad (4.2)$$

$$A_2 = -g_{m6} (r_{o6} || r_{o7}) = -g_{m6} R_2 \quad (4.3)$$

where g_{m1} is transconductance of M1 and g_{m6} is transconductance of M6

The frequency response consideration is important for understanding the poles and zeroes location in the gain or bode plot of the error amplifier.

$$\text{Assuming, } C_1 = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{gs6} \quad (4.4)$$

where, C_{gd2} is gate to drain capacitance of M2, C_{db2} is drain to bulk capacitance of M2, C_{gd4} is gate to drain capacitance of M4, C_{db4} is drain to bulk capacitance of M4, C_{gs6} is gate to source capacitance of M6

$$\text{Assuming, } C_2 = C_{db6} + C_{db7} + C_{gd7} + C_L \quad (4.5)$$

where, C_{db6} is drain to bulk capacitance of M6, C_{db7} is drain to bulk capacitance of M7, C_{gd7} is gate to drain capacitance of M7, C_L is load capacitance

$$f_{p1} \approx \frac{1}{2\pi R_1 G_{m2} R_2 C_c} \quad (4.6)$$

$$f_{P2} \approx \frac{1}{2\pi} \frac{G_{m2}}{C_2} \quad (4.7)$$

$$f_{Z1} \approx \frac{1}{2\pi} \frac{G_{m2}}{C_c} \quad (4.8)$$

f_{P1} is the dominant pole and f_{P2} is the pole of our major concern since f_{P2} decreases with a higher capacitive load and hence affects the stability of the circuit [34].

Phase Margin,

$$\phi_{P2} = -\tan^{-1}(f_t/f_{P2}) \quad (4.9)$$

$$\phi_Z = -\tan^{-1}(f_t/f_Z) \quad (4.10)$$

$$\phi_{total} = 90^\circ + \tan^{-1}\left(\frac{f_t}{f_{P2}}\right) + \tan^{-1}\left(\frac{f_t}{f_Z}\right) \quad (4.11)$$

$$PM = 180^\circ - \phi_{total} = 90^\circ - \tan^{-1}\left(\frac{f_t}{f_{P2}}\right) - \tan^{-1}\left(\frac{f_t}{f_Z}\right) \quad (4.12)$$

Phase margin can be improved by adding a series resistance in the feedback path. The other technique for improving the phase margin is by moving the zero f_{Z1} given in the equation towards higher frequencies.

Slew rate is defined as the maximum voltage change rate at the output, associated with charging and discharging of the C_c . There is a direct relationship between C_c and slew rate i.e.

$$SR = I_{tail}/C_c$$

where, I_{tail} is the tail current.

From the small signal model, the output voltage V_{out} is given as

$$V_{out} = V_{DD} \left(\frac{R1}{R1+R2} \right) - \frac{V_{DD}}{R_1} (R_1 \parallel R_2) \quad (4.13)$$

or

$$V_{out} = V_{DD} \left(\frac{R1}{R1+R2} \right) - \frac{V_{DD}}{R_1} \left(\frac{R1 \times R2}{R1+R2} \right) \quad (4.14)$$

or

$$V_{out} = 0 \quad (4.15)$$

It is observed that the output voltage does not contain any ac ripples.

Following are the equations used in the design of the two-stage opamp [34].

$$g_{m1} = g_{m2} = g_{mI}, \quad g_{m6} = g_{mII}, \quad (4.16)$$

$$g_{ds2} + g_{ds4} = G_I, \quad \text{and} \quad g_{ds6} + g_{ds7} = G_{II} \quad (4.17)$$

$$I_d = \frac{\mu_{n,p} C_{ox} \left(\frac{W}{L} \right) V_{eff}^2}{2} \quad (4.18)$$

where, I_d is drain current, $\mu_{n,p}$ is mobility, C_{ox} is oxide capacitance, V_{eff} is overdrive voltage

$$g_m = \sqrt{2\mu_{n,p} C_{ox} \frac{W}{L} I_d} \quad (4.19)$$

$$g_m = 2 \frac{I_d}{V_{eff}} \quad (4.20)$$

$$\text{Slew rate, } SR = \frac{I_5}{C_c} \quad (4.21)$$

$$\text{First Stage gain, } A_{v1} = \frac{-g_{m1}}{g_{ds2} + g_{ds4}} = \frac{-2g_{m1}}{I_5(\lambda_2 + \lambda_4)} \quad (4.22)$$

$$\text{Second Stage gain, } A_{v2} = \frac{-g_{m6}}{g_{ds6} + g_{ds7}} = \frac{-g_{m6}}{I_6(\lambda_6 + \lambda_7)} \quad (4.23)$$

$$\text{Gain Bandwidth, } GB = \frac{g_{m1}}{C_c} \quad (4.24)$$

$$\text{Output pole, } p_2 = \frac{-g_{m6}}{C_L} \quad (4.25)$$

$$\text{RHP zero, } Z_1 = \frac{g_{m6}}{C_c} \quad (4.26)$$

$$\text{Positive CMR, } V_{in}(\max) = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{TO3}|(\max) + V_{T1}(\min) \quad (4.27)$$

$$\text{Negative CMR, } V_{in}(\min) = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1}(\max) + V_{DS5}(\text{sat}) \quad (4.28)$$

$$\text{Saturation Voltage, } V_{DS}(\text{sat}) = \sqrt{\frac{2I_{DS}}{\beta}} \quad (4.29)$$

where, V_{DD} = supply voltage, λ is technology parameter

4.3 DESIGN OF PMOS PASS ELEMENT

The PMOS device is used to cancel out the ripples coming from the LDO output. In the Figure 4.1, the drain terminal of NMOS (M8) of second stage of error amplifier is connected to gate of the PMOS pass device (M11) of LDO to cancel out the output ripples.

The Table 4.3 shows the design specifications of PMOS pass device in 0.18 μm CMOS technology.

Table 4.3 Design Specifications of the PMOS pass element

Circuit Parameters	Specifications
Technology	0.18 μm
Input Voltage Range	1.0 - 1.8 V
Power Supply	1.8 V
Output Voltage	1.25 V
Ground Current	0 A

4.4 DESIGN OF TRANSMISSION GATE

In the proposed LDO circuit, the miller compensation technique is used. A compensation capacitor C_c and nulling resistor R_{null} is inserted in the compensation network. The nulling resistor inserted in the circuit in series with compensation capacitor C_c shifts the right hand plane zero in the transfer function even more far away to reduce its effects over the stability. The inserted nulling resistor allows independent control over right hand plane zero placement [34]. As a result, the pole added due to output load capacitance is nullified. To accomplish this, $f_{z1} = f_{p2}$ according to 4.7 and 4.8 must be satisfied.

In this proposed LDO circuit, the nulling resistor is replaced by transmission gate (TG). Basic structure of TG is shown in Figure 4.5. A TG or an analog switch is defined as an electronic element that will selectively block or pass a signal from the input to the output. It comprises of two transistors - PMOS and NMOS. The selection of the signal is based on the gate input of these two transistors. TG can be considered as a bi-directional relay that can move the data in either direction. Both PMOS and NMOS work simultaneously in saturation region.

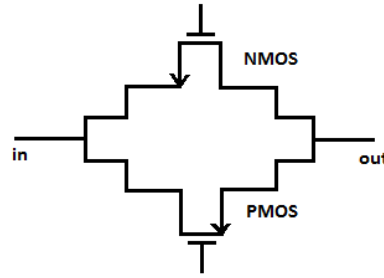


Figure 4.5 Basic structure of a Transmission Gate (TG)

The gate of the PMOS transistor is biased at ground (GND) and gate of the NMOS transistor is biased at supply voltage (V_{DD}). Its on and off resistance is given by the following equations.

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Thn})} \quad (4.30)$$

$$R_{OFF} = \frac{1}{\mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{Thp}|)} \quad (4.31)$$

In Figure 4.5, when NMOS input is at V_{DD} and PMOS input is GND, the data input is transferred to the output i.e. giving a low impedance state. When both are OFF, it creates an open circuit state. The body or substrate potentials of NMOS and PMOS are taken at the lowest and highest levels respectively. The primary advantage of using a TG in place of a resistor is that CMOS switch provides a great increase in dynamic analog signal range in ON condition and hence improves the stability [34].

Chapter 5

SIMULATION RESULTS

The proposed low drop-out voltage regulator has been simulated using Cadence in 0.18 μm CMOS technology parameters. This chapter is organized as follows. Section 5.1 presents the simulation results of the proposed error amplifier circuit. The simulation result of bandgap reference voltage circuit is addressed in section 5.2. Section 5.3 presents the simulation results of proposed low drop-out voltage regulator.

5.1 SIMULATION RESULTS OF ERROR AMPLIFIER

The error amplifier circuit is operated at the supply voltage of 1.8 V. The differential amplifier calculates a difference of the two input voltages and gives it to the second stage where the signal is amplified. Figures 5.1 and 5.2 show the dc gain and frequency response of the uncompensated error amplifier respectively. The dc gain is 51 dB and phase margin is 61 degrees. The unity gain bandwidth is 12 MHz.

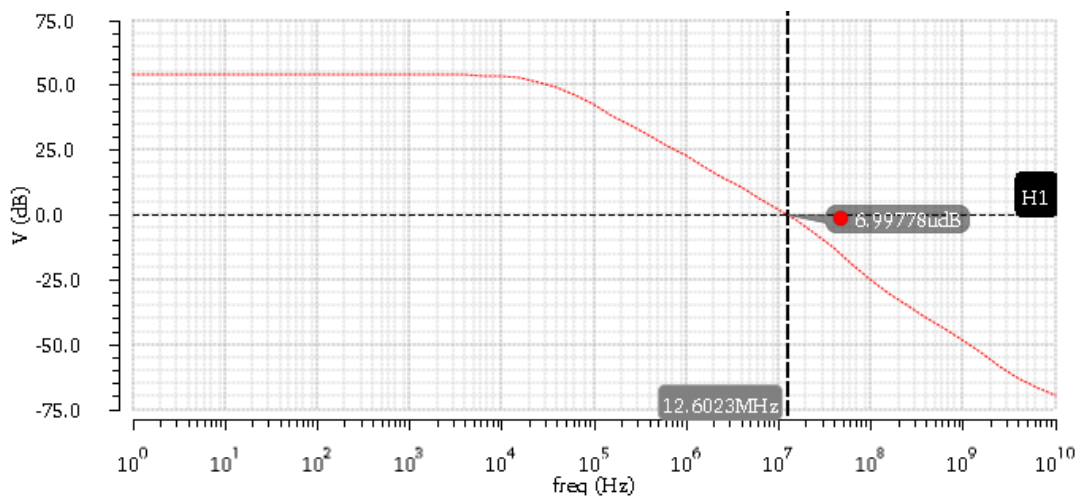


Figure 5.1 Gain vs. frequency plot of uncompensated error amplifier

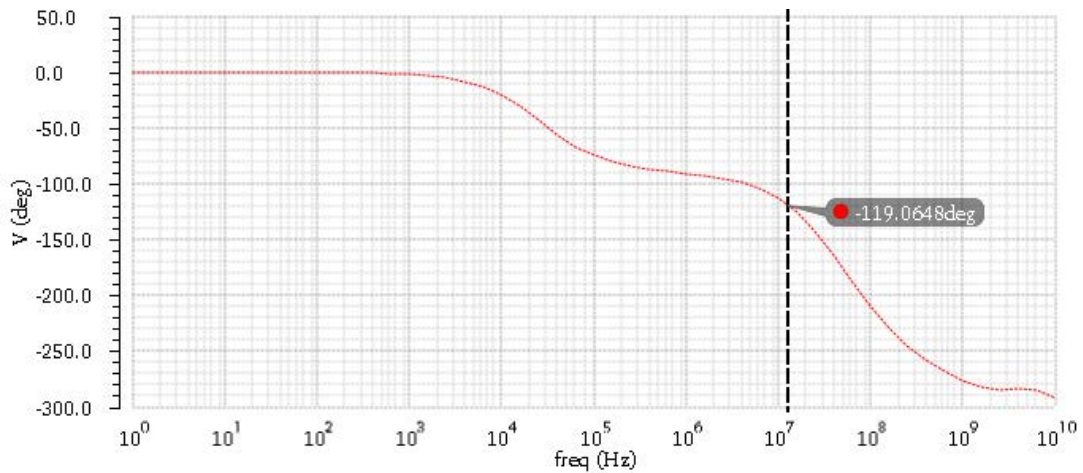


Figure 5.2 Phase vs. frequency plot of uncompensated error amplifier

Figure 5.3 and 5.4 shows the improved dc gain and phase margin of the compensated error amplifier respectively. The dimensions of the error amplifier are optimized to achieve higher gain and stability both at the same time in the same circuit. The dc gain achieved after including the improvement circuitry is 62 dB with the phase margin of 62 degrees. The unity gain bandwidth of the circuit is 18 MHz.

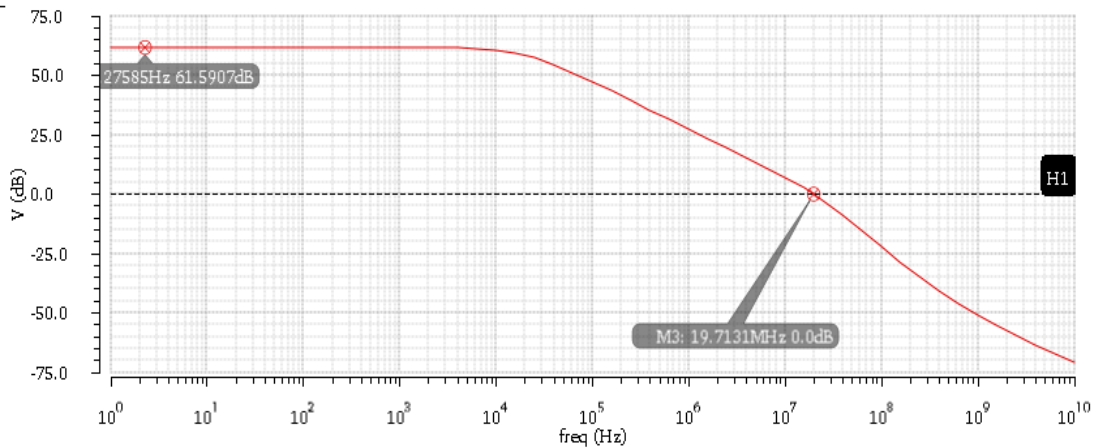


Figure 5.3 Gain vs. frequency plot of compensated error amplifier

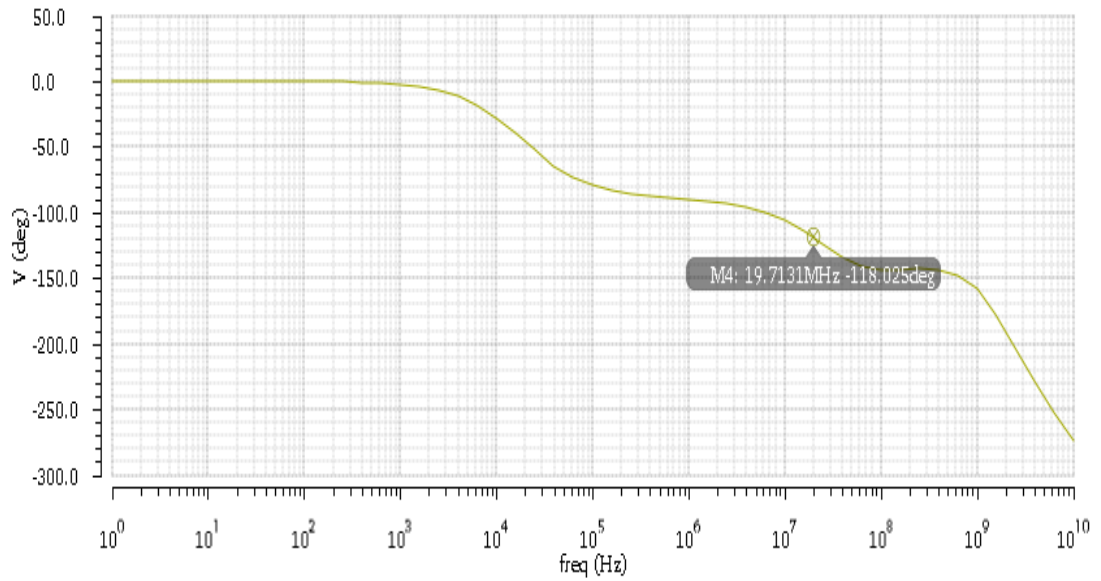


Figure 5.4 Phase vs. frequency plot of compensated error amplifier

5.2 SIMULATION RESULTS OF BANDGAP VOLTAGE REFERENCE CIRCUIT

Figure 5.5 shows the output voltage of the bandgap reference circuit. The transient analysis is performed for the circuit and it is observed that the output voltage of the circuit is constant.

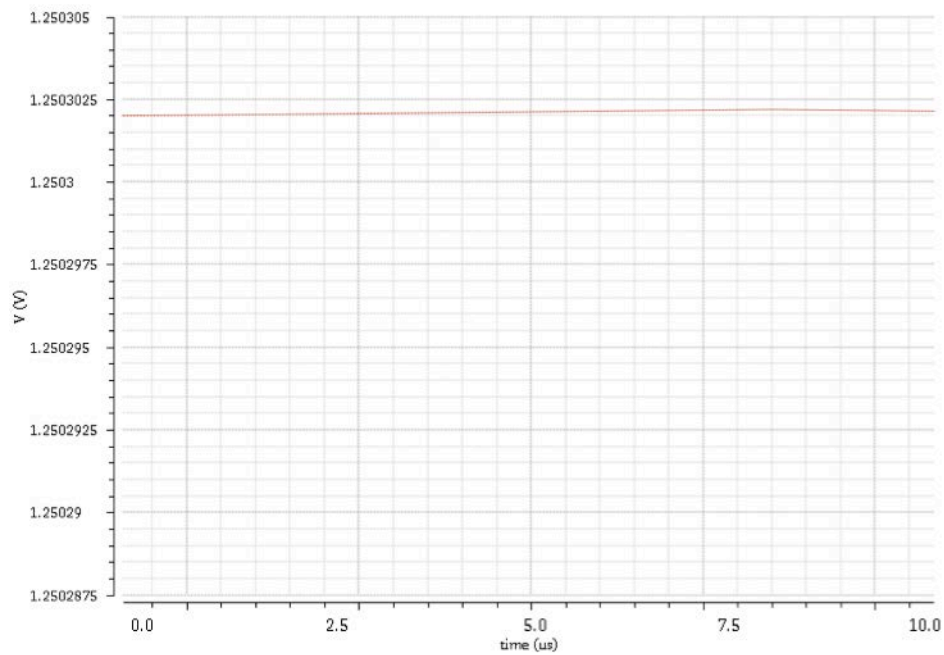


Figure 5.5 Output Voltage of Bandgap Voltage Reference Circuit

5.3 SIMULATION RESULTS OF LDO

Figure 5.6 shows the basic operation of the LDO i.e. output voltage regulation. From the plot, it is evident that the proposed LDO structure regulates the output voltage at 1.25 V for the input range of 1.4V to 2.7V. The proposed LDO has dropout voltage 190mV, which is less than 200mV.

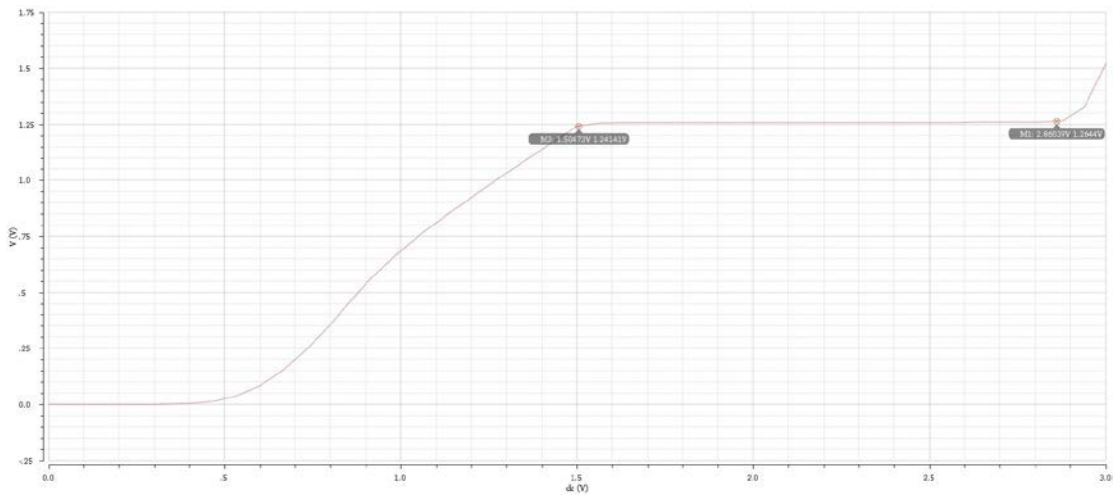


Figure 5.6 Output voltage vs. input voltage

Figure 5.7 plots the output voltage versus load current. It is used to find out the load regulation. Using 3.10, the load regulation of the proposed LDO is 0.8mV.

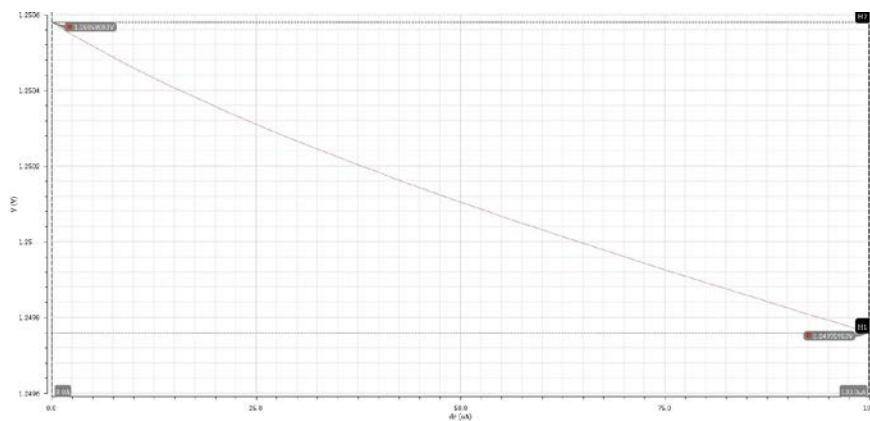


Figure 5.7 Output voltage vs. load current

Figure 5.8 shows the plot without PSRR improvement technique. The PSRR of the LDO is -51.74 dB.

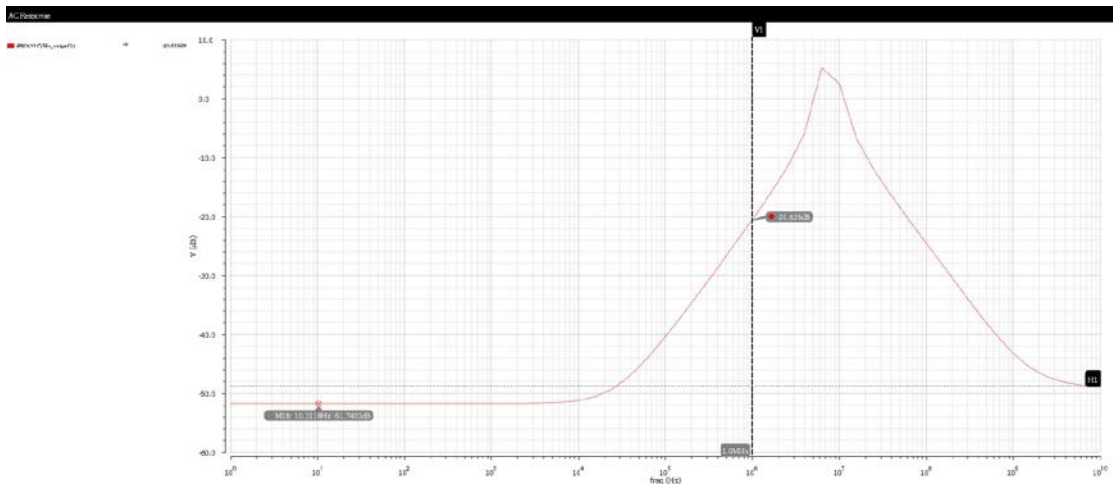


Figure 5.8 PSRR plot without improvement technique

Improvement in PSRR is achieved by increased open loop gain (62 dB) of the error amplifier. The improved PSRR plot of proposed LDO is shown in Figure 5.9 and the value of PSRR is -61.5 dB.

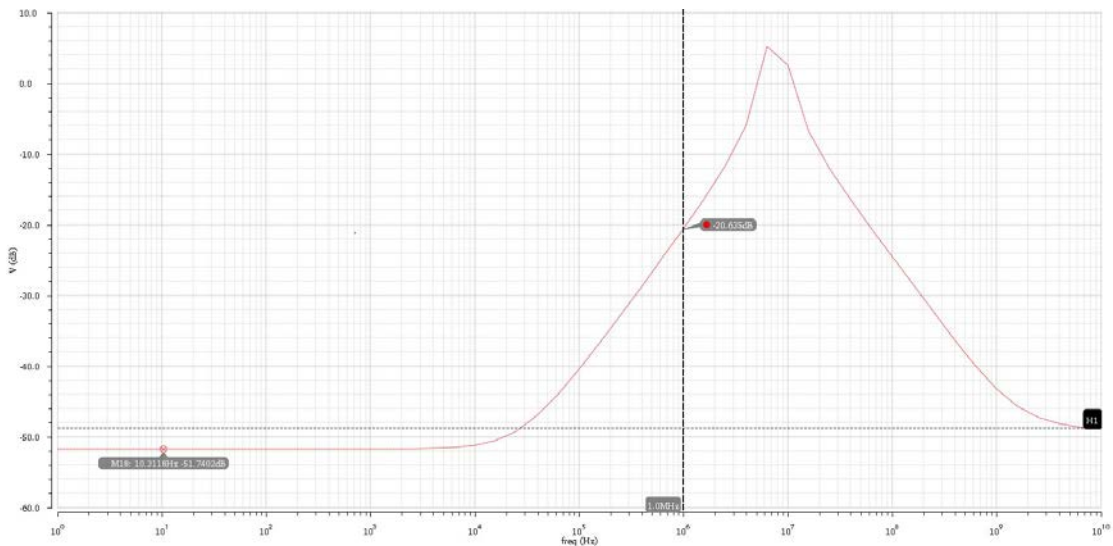


Figure 5.9 PSRR plot of compensated LDO

The load current and quiescent current of the proposed LDO circuit is 200mA and 290uA respectively.

Table 5.1 shows the comparison between proposed LDO architecture and existing LDO architectures available in literature [19, 20, 22, 24, 36, 38]. From the Table 5.1, it can be seen that the proposed LDO structure regulates the output voltage at 1.25 V for the input range of 1.4V to 2.7V. Also, the proposed circuit has improved quiescent current of 290 μ A and PSRR of -61.5 dB.

Table 5.1 Comparison of LDO architectures in literature with the proposed LDO

Design Parameters	[8]	[9]	[20]	[22]	[24]	[36]	[39]	Proposed LDO
Year	2010	2014	2014	2010	2016	2010	2009	2016
Technology	0.35 μ m	90nm	0.18 μ m	0.18 μ m	0.18 μ m	0.18 μ m	0.35 μ m	0.18 μ m
Supply Voltage	2.2 V	1 V	1.8V	3V	1.8V	1.8V	3V	1.8V
Input Range	-	-	2-3.2V	3-5V	-	4 – 5.5V	3-5V	1.4-2.7V
Output Voltage	-	0.5 V	1.6V	1V	1.2V	2.8	2.5	1.25V
Gain	75.8 dB	-	-	-	-	-	-	62 dB
Phase Margin	66.5 ⁰	-	-	-	-	-	-	62 ⁰
PSRR	-38 dB	- 48.1 dB	-50dB	-40dB	-39dB	-69dB	-75dB	-61.5dB
Line Regulation	39mV/V	-	-	370 μ V/V	-	-	-	-
Load Regulation	13mV	0.28 mV	200mV	1.73mV	4mV	-	-	0.8mV
Quiescent Current	35.7 μ A	60 μ A	80 μ A	-	-	-	-	290 μ A

CHAPTER 6

CONCLUSIONS AND FUTURE SCOPE

6.1 CONCLUSIONS

A Low Drop-out Voltage Regulator is capable of keeping its specified output voltage over a wide range of load current and input voltage. Low Drop-out Voltage Regulator provide constant supply rail for integrated circuits. Many of the Low Drop-out Voltage Regulators in today's portable devices are integrated into multifunction Power-management integrated circuits. Stability is major concern for Low Drop-Out Regulator design, which can be achieved by either using external capacitor or by using some special compensation techniques. Low Drop-out Voltage Regulator has found applications in portable devices for power management.

In this dissertation, a PMOS low drop-out voltage regulator with improved PSRR and low quiescent current has been designed. The proposed circuit utilizes the transmission gate properties of gain and stability for improving the value of PSRR at dc level along with two stage error amplifier with PMOS mirror load, which provides better PSRR bandwidth. The proposed circuit has been simulated using TSMC 0.18 μm CMOS technology process parameters and the simulation results have been presented. The proposed circuit provides an output voltage of 1.25V for the input voltage range of 1.4 to 2.7V. The proposed circuit has been compared with the existing circuits available in the literature and it has been observed that the proposed circuit has better dc PSRR. The proposed circuit has applications in PLL/VCO, audio devices and other devices where the high PSRR along with bandwidth is required.

6.2 FUTURE SCOPE

Some suggestions and ideas for future work:

- The two-stage error amplifier block gain can be improved by using gain improvement techniques. With this gain boosting techniques employed in the circuit, PSRR of LDO can be improved.

- Improvements in low drop-out voltage regulator's slew rate can be achieved by using class AB amplifier at the output stage or by increasing the bias current. Sufficient slew rate improves the performance of an LDO.

CHAPTER 6

REFERENCES

- [1] Amrani, Hafid, and Hubert Cordonnier. "Power and battery management ICs for low-cost portable electronics." *Annales des télécommunications*. vol. 59. No. 7-8. Springer-Verlag, 2004.
- [2] Edgar Sanchez-Sinencio, "Low Drop-Out (LDO) Linear Regulators- Design Considerations and Trends for High Power Supply Rejection (PSR)," *IEEE Santa Clara Valley (SCV) Solid State Circuits Society*, Feb 2011
- [3] Lincoln Phelps Rice, "A transistorized Regulated Power Supply," Ph.D. dissertation, Electrical Engineering, Georgia Inst. of Technology, Atlanta, 1954
- [4] G. A. Rincon-Mora, "Current efficient, low voltage, low drop-out regulators," Ph.D. dissertation, Elect. Comp. Eng. Dept., Georgia Inst. of Technology, Atlanta, 1996
- [5] H. Armani and H. Cordonnier, "Power and battery management ICs for low-cost portable electronics", *Annales Telecommunications Juillet*, vol.59, pp. 974-983, Jul. 2004
- [6] G. A. R. - Mora and P.E. Allen, "Optimized Frequency-Shaping Circuit Topologies for LDO's," in *IEEE Transactions on Circuits and Systems - ii: Analog and Digital Signal Processing*, vol. 45, pp.703-707, June 1998
- [7] Crepaldi, P; Pimenta, T.; Moreno, R., "A CMOS Low Drop out Voltage Regulator," *Microelectronics (ICM), 2010 International Conference*, pp. 208 - 211, 19-22 Dec 2010
- [8] G. A. Rincon-Mora and P.E. Allen, "A low voltage low quiescent current low drop out regulator," *IEEE J. Solid-State Circuits*, vol. 33, no. 1, pp. 1265–1272, Jan. 1998

- [9] Chung-Hsun Huang et al., "Design of a Low-Voltage Low-Dropout Regulator", *IEEE Transaction on very large scale integration (VLSI) systems*, 22(6), 2014
- [10] Jayanthi Vanama and G.L. Sampurna, "Design of a Programmable Low Power Low Drop-Out Voltage Regulator," *International Journal of VLSI design & Communication Systems*, Vol.4, No.3, June 2013
- [11] Aminzadeh, H.; Nabavi, M.R.; Serdijn, W.A., "Low-Dropout Voltage Source: An Alternative Approach for Low-Dropout Voltage Regulators," *Circuits and Systems II: Express Briefs, IEEE Transactions*, vol. 61, Issue. 6, pp. 413-417, June 2014
- [12] G. Giutilisi, G. Palumbo, C. Falconi, "NMOS Low Drop-out Regulator with Dynamic biasing", *ICECS '06*, 13
- [13] P. Patel and G. A. Rincon-Mora "High power-supply-rejection (PSR) current-mode low-dropout (LDO) regulator", *IEEE Trans. Circuits Syst. II*, vol. 57, no. 11, pp.868 -873, 2010
- [14] R. K. Dokaniz and G. A. Rincon-Mora "Cancellation of load regulation in low drop-out regulators", *Electron. Letter*, vol. 38, no. 22, pp.1300 -1302, 2002
- [15] M. El-Nozahi , A. Amer , J. Torres , K. Entesari and E. Sanchez-Sinencio "High PSR low drop-out regulator with feed-forward ripple cancellation technique", *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp.565 - 577, 2010
- [16] Garimella, P. M. Furth, P. R. Surkanti and N. R. Thota, "Current buffer compensation topologies for LDOs with improved transient performance," *Analog Integrated Circuits and Signal Processing*, pp. 1-12, 19 Nov. 2011

- [17] R. J. Milliken, J. Silva-Martinez and E. Sanchez-Sinencio "Full on-chip CMOS low-dropout voltage regulator", *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 9, pp.1879 -1890, 2007
- [18] Shirahatti, Sunita, and Anilkumar Nandi. "A Capacitor-less Low Drop out Voltage Regulator." In *Communication Control and Computing Technologies (ICCCCT), 2010 IEEE International Conference on*, pp. 177-182. IEEE, 2010
- [19] Torres, J. ; El-Nozahi, M. ; Amer, A. ; Gopalraju, S. ; Abdullah, R. ; Entesari, K.; Sanchez-Sinencio, E. "Low Drop-Out Voltage Regulators: Capacitor-less Architecture Comparison," *Circuits and Systems Magazine, IEEE*, vol. 14, Issue 2, pp. 6-26, May 2014
- [20] Park, C.J., Silva-Martinez, J. and Onabajo, M., 2014, August. "Design techniques for external capacitor-less LDOs with high PSR over wide frequency range", *IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS)* (pp. 342-345).
- [21] Guo, J. and Leung, K.N., 2010. A 6-W chip-area-efficient output-capacitorless LDO in 90-nm CMOS technology. *IEEE Journal of Solid-State Circuits*, 45(9), pp.1896-1905
- [22] Abbasi, M.U., Bagnall, D. and Bn, V., 2010, September. A high PSRR capacitor-less on Chip low dropout voltage regulator. In *IEEE 8th International Symposium on Intelligent Systems and Informatics* (pp. 361-364). IEEE
- [23] Leo, C.J., Raja, M.K. and Minkyu, J., 2013, December. An ultra low-power capacitor-less LDO with high PSR. In *Microwave Workshop Series on RF and Wireless Technologies for Biomedical and Healthcare Applications (IMWS-BIO), 2013 IEEE MTT-S International* (pp. 1-3). IEEE

- [24] J. Zarate-Roldan; M. Wang; J. Torres; E. Sánchez-Sinencio, "A Capacitor-Less LDO With High-Frequency PSR Suitable for a Wide Range of On-Chip Capacitive Loads," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* , vol.PP, no.99, pp.1-13
- [25] Kim, Y.I. and Lee, S.S., 2013. A capacitorless LDO regulator with fast feedback technique and low-quiescent current error amplifier. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 60(6), pp.326-330.
- [26] *Texas Instruments*, "Fundamental Theory of PMOS Low Drop-out Voltage Regulators," Application Report, Apr. 1997
- [27] *Texas Instruments*, "Understanding Low Drop Out (LDO) Regulators," Application Report, 2006
- [28] P.E. Allen and D.R. Holberg, "CMOS Analog Circuit Design" Oxford University Press, 2nd edition
- [29] Maxim Application Note 1108: Understanding Single-Ended, Pseudo-Differential and Fully-Differential ADC Inputs – Retrieved November 10, 2007
- [30] B. Razavi, "Design of Analog CMOS Integrated Circuits," Tata McGraw-Hill, 2002
- [31] M.Jyothi, L.Ravi Chandra, J.Poornima,k.Rajasekhar , S.Daya Sagar Chowdary, "Design Of Two Stage Operational Amplifier On Zero Cross Detector Using 0.18 μ m Technology" *International Journal Of VLSI & Signal Processing Applications*, Vol2, Issue2 , April 2012, ISSN 2231-3133 (189- 195)
- [32] Rincon-Mora, Gabriel. *Analog IC design with low-dropout regulators (LDOs)*. McGraw-Hill, Inc., 2009
- [33] Simpson, Chester. "Linear regulators: Theory of operation and compensation." *National Semiconductor Application Note 5* (2000): 24-29

- [34] S. Guo and H. Lee, "Dual Active-Capacitive-Feedback Compensation for Low-Power Large-Capacitive-Load Three-Stage Amplifiers," in *IEEE Journal of Solid-State Circuits*, vol. 46, no. 2, pp. 452-464, Feb. 2011
- [35] Wang, Chua-Chin, Chi-Chun Huang, Tzung-Je Lee, and U. Fat Chio. "A linear LDO regulator with modified NMCF frequency compensation independent of off-chip capacitor and ESR." In *APCCAS 2006-2006 IEEE Asia Pacific Conference on Circuits and Systems*, pp. 880-883. IEEE, 2006
- [36] Simpson, Chester. "Linear regulator to optimize feedforward compensation." *The United States National Semiconductor Application Notes* (2007)
- [37] Miller Compensation - Wally M. C. Sansen (2006). *Analog design essentials*. New York; Berlin: Springer. pp. §097, p. 266 *et seq.* ISBN 0-387-25746-2.
- [38] *Texas Instruments*, "Technical Review of Low Dropout Voltage Regulator Operation and Performance," Application Report, Aug. 1999
- [39] V. Majidzadeh, K. Silay, A.Schmid, C. Dehollain and Y. Leblebici, "A fully on-chip LDO voltage regulator with 37 dB PSRR at 1 MHz for Remotely Powered Biomedical Implants," *Analog Integr Circ Sig Process*, vol. 67, pp. 157–168, Nov. 2011.
- [40] Z. Kamal, Q. Hassan, "Full On Chip Capacitance PMOS Low Dropout Voltage Regulator," in *IEEE International Conference on Multimedia Computing and Systems*, Ouarzazate, Apr. 2011, pp. 1-4.

APPENDIX I

A.1. Level 53 simulation model parameters

```
.MODEL NOTCHEDROW C
.MODEL HR R
.MODEL Nmos NMOS (          LEVEL = 53
+VERSION = 3.1      TNOM   = 27      TOX   = 4.1E-9
+XJ   = 1E-7      NCH   = 2.3549E17  VTH0  = 0.3725327
+K1   = 0.5933684  K2    = 2.050755E-3  K3    = 1E-3
+K3B  = 4.5116437  W0    = 1E-7      NLX   = 1.870758E-7
+DVT0W = 0        DVT1W = 0        DVT2W = 0
+DVT0  = 1.3621338  DVT1  = 0.3845146  DVT2  = 0.0577255
+U0   = 259.5304169  UA   = -1.413292E-9  UB   = 2.229959E-18
+UC   = 4.525942E-11  VSAT = 9.411671E4   A0   = 1.7572867
+AGS  = 0.3740333   B0   = -7.087476E-9  B1   = -1E-7
+KETA  = -4.331915E-3  A1   = 0          A2   = 1
+RDSW  = 111.886044  PRWG  = 0.5      PRWB  = -0.2
+WR   = 1          WINT  = 0          LINT  = 1.701524E-8
+XL   = 0          XW   = -1E-8      DWG   = -1.365589E-8
+DWB  = 1.045599E-8  VOFF  = -0.0927546  NFACTOR = 2.4494296
+CIT  = 0          CDSC  = 2.4E-4      CDSCD = 0
+CDSCB = 0          ETA0  = 3.175457E-3  ETAB  = 3.494694E-5
+DSUB  = 0.0175288  PCLM  = 0.7273497  PDIBLC1 = 0.1886574
+PDIBLC2 = 2.617136E-3  PDIBLCB = -0.1      DROUT  = 0.7779462
+PSCBE1 = 3.488238E10  PSCBE2 = 6.841553E-10  PVAG  = 0.0162206
+DELTA = 0.01      RSH   = 6.5      MOBMOD = 1
+PRT  = 0          UTE   = -1.5      KT1   = -0.11
+KT1L = 0          KT2   = 0.022     UA1   = 4.31E-9
+UB1  = -7.61E-18  UC1   = -5.6E-11   AT    = 3.3E4
+WL   = 0          WLN   = 1          WW    = 0
+WWN  = 1          WWL   = 0          LL    = 0
+LLN  = 1          LW    = 0          LWN   = 1
+LWL  = 0          CAPMOD = 2      XPART  = 0.5
```

+CGDO = 8.53E-10 CGSO = 8.53E-10 CGBO = 1E-12
 +CJ = 9.513993E-4 PB = 0.8 MJ = 0.3773625
 +CJSW = 2.600853E-10 PBSW = 0.8157101 MJSW = 0.1004233
 +CJSWG = 3.3E-10 PBSWG = 0.8157101 MJSWG = 0.1004233
 +CF = 0 PVTH0 = -8.863347E-4 PRDSW = -3.6877287
 +PK2 = 3.730349E-4 WKETA = 6.284186E-3 LKETA = -0.0106193
 +PU0 = 16.6114107 PUA = 6.572846E-11 PUB = 0
 +PVSAT = 1.112243E3 PETA0 = 1.002968E-4 PKETA = -2.906037E-3)
 *

.MODEL Pmos PMOS (LEVEL = 53
 +VERSION = 3.1 TNOM = 27 TOX = 4.1E-9
 +XJ = 1E-7 NCH = 4.1589E17 VTH0 = -0.3948389
 +K1 = 0.5763529 K2 = 0.0289236 K3 = 0
 +K3B = 13.8420955 W0 = 1E-6 NLX = 1.337719E-7
 +DVT0W = 0 DVT1W = 0 DVT2W = 0
 +DVT0 = 0.5281977 DVT1 = 0.2185978 DVT2 = 0.1
 +U0 = 109.9762536 UA = 1.325075E-9 UB = 1.577494E-21
 +UC = -1E-10 VSAT = 1.910164E5 A0 = 1.7233027
 +AGS = 0.3631032 B0 = 2.336565E-7 B1 = 5.517259E-7
 +KETA = 0.0217218 A1 = 0.3935816 A2 = 0.401311
 +RDSW = 252.7123939 PRWG = 0.5 PRWB = 0.0158894
 +WR = 1 WINT = 0 LINT = 2.718137E-8
 +XL = 0 XW = -1E-8 DWG = -4.363993E-8
 +DWB = 8.876273E-10 VOFF = -0.0942201 NFACTOR = 2
 +CIT = 0 CDSC = 2.4E-4 CDSCD = 0
 +CDSCB = 0 ETA0 = 0.2091053 ETAB = -0.1097233
 +DSUB = 1.2513945 PCLM = 2.1999615 PDIBLC1 = 1.238047E-3
 +PDIBLC2 = 0.0402861 PDIBLCB = -1E-3 DROUT = 0
 +PSCBE1 = 1.034924E10 PSCBE2 = 2.991339E-9 PVAG = 15
 +DELTA = 0.01 RSH = 7.5 MOBMOD = 1
 +PRT = 0 UTE = -1.5 KT1 = -0.11
 +KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9
 +UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0
+WWN = 1 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 6.28E-10 CGSO = 6.28E-10 CGBO = 1E-12
+CJ = 1.160855E-3 PB = 0.8484374 MJ = 0.4079216
+CJSW = 2.306564E-10 PBSW = 0.842712 MJSW = 0.3673317
+CJSWG = 4.22E-10 PBSWG = 0.842712 MJSWG = 0.3673317
+CF = 0 PVTH0 = 2.619929E-3 PRDSW = 1.0634509
+PK2 = 1.940657E-3 WKETA = 0.0355444 LKETA = -3.037019E-3
+PU0 = -1.0227548 PUA = -4.36707E-11 PUB = 1E-21
+PVSAT = -50 PETA0 = 1E-4 PKETA = -5.167295E-3)
*
.END

ORIGINALITY REPORT

601461029

by Swati Wadhera

FILE	601461029.DOCX (2.28M)		
TIME SUBMITTED	06-JUL-2016 05:18PM	WORD COUNT	8703
SUBMISSION ID	688134181	CHARACTER COUNT	46150

601461029

ORIGINALITY REPORT

19%	11%	11%	8%
SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS

PRIMARY SOURCES

1	dspace.thapar.edu:8080 Internet Source	2%
2	Submitted to Thapar University, Patiala Student Paper	2%
3	focus.ti.com Internet Source	1%
4	sites.ieee.org Internet Source	1%
5	cirworld.org Internet Source	1%
6	www.qucosa.de Internet Source	1%
7	Kok, . "Error Sources in Bandgap Voltage Reference Circuit", CMOS Voltage References An Analytical and Practical Perspective, 2012. Publication	1%
8	ijireeice.com Internet Source	1%
9	Huey Jen Lim. "Double regulated voltage	