REAL TIME IMPLEMENTATION OF DIGITAL MODULATION TECHNIQUES ON WARP FPGA

A THESIS SUBMITTED IN PARTIAL FULFILMENT OF THE

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SUBMITTED BY

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CERTIFICATE

I hereby declare that the work, which is being presented in this thesis, entitled "**Real time Implementation of Digital Modulation Techniques on WARP FPGA**" in partial fulfilment of the requirements for the award of degree of Master of Engineering in Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the guidance of Mrs. Surbhi Sharma.

The matter in this thesis has not been submitted in any other University or Institute for the award of any degree.

Lokesh Bhardwaj

This is to certify that that the above statement made by the candidate is correct and true to best of my knowledge.

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ABSTRACT

In wireless communication, a signal is modulated before it is transmitted. Modulation is superimposing of modulating signal over a high frequency carrier. The carrier is a sinusoidal signal with a very high frequency. Modulation is required so as to achieve easy radiation, achieving simultaneous transmission of several signals and the bandwidth of the transmitted signal can be increased for better transmission quality. Different modulation techniques are used such as M-PSK, M-QAM and M-DPSK. The M-ary modulation is done and the signals obtained after modulation are transmitted through the antenna associated with the transmitting radio board of WARTP board. These signals are then received by the antenna associated with receiving radio board. The generation of information bits and their modulation along with activation of modules of WARP FPGA such as radio boards, clocks and downloading of signals to be transmitted through the antenna are done through the program running offsite of the WARP FPGA board. WARP is Wireless Open Access Research Platform.

The WARP board is equipped with the radio boards which are responsible for the processing of signals to be transmitted and received. The signals are modulated by different techniques for their transmission and bit error rate performances of these techniques are compared to show the best modulation technique among all. Theoretical bit error rates for M-PSK and M-QAM are evaluated using MGF approach. The information bits of 12000 length is taken and bit error rate is evaluated for the base band gain of range from 1 to 3. It can be seen that the BER for BPSK is least while it increases as order of modulation increases. However QAM shows slightly better performance than PSK due to its dual modulation standards. DPSK uses one and a half cycle of carrier wave in the single information bit. DPSK is simpler to implement than ordinary PSK since there is no need for the demodulator to have a copy of the reference signal to determine the exact phase of the received signal, however the probability of erroneous demodulation is greater in DPSK. The performance of these modulation techniques in real time makes the bit error rate to increase initially for all techniques; however it gets reduced with increase in the transmitter base band gain. Also demodulated signals in every case can be seen. The maximum distortion in demodulated signals can be seen in case of higher order modulation.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

WARP	Wireless Open Access Research Platform
SDR	Software Defined Radio
ASIC	Application Specific Integrated Circuit
TDM	Time Division Multiplexing
VLSI	Very High Speed Integrated Circuit Hardware Descriptive Language
W-CDMA	Wideband Code Division Multiple Access
RAM	Random Access Memory
QOS	Quality of Service
WiMAX	Worldwide Interoperability for Microwave Access
LAS-CDMA	Large Area Synchronized Code Division Multiple Access
H-ARQ	Hybrid Automatic Repeat Request
OFDM	Orthogonal Frequency Division Multiplexing
VoIP	Voice Only Internet Protocol
DSL	Digital Subscriber Line
3GPP-LTE	Third Generation Partnership Project-Long Term Evolution
GPRS	General Packet Radio Service
FDD	Frequency Division Duplexing
TDD	Time Division Duplexing
MIMO	Multiple Input Multiple Output

RSSI	Received Radio Strength Indicator
PLL	Phase Locked Loop
DAC	Digital to Analog Converter
ADC	Analog to Digital Converter
MAC	Media Access Control
FPGA	Field Programming Gate Array
PROM	Programmable Read Only Memory
RF	Radio Frequency
BPSK	Binary Phase Shift Keying
QPSK	Quadrature Phase Shift Keying
DPSK	Differential Phase Shift Keying
MGF	Moment Generation Function
PAPR	Peak to Average Power Ratio
SYNC	Synchronization
PAM	Pulse Amplitude Modulation
LED	Light Emitting Diode
MGT	Multi Gigabit Transceivers
CBS	Constant Bandwidth Server
WCCCBS	Window Constrained Constant Bandwidth Server
DWCS	Dynamic Window Constrained Scheduling

CHAPTER 1

INTRODUCTION

In current scenario emphasis is laid more on real time research rather than simulating the system design on software. However one has to simulate in order to determine the basic behaviour but implementing in real time provides the correct and actual behaviour of the system. The real time implementation can be done on various hardware platforms such as Software Defined Radio, WARP FPGA board, ASIC and DSP based hardware. Doing so allows the practical usage of the design and its areas of implementation for the purpose of benefit of society. Further real time systems give opportunity for one to remove or minimize the problems which are encountered practically so that technology given is more reliable and efficient. It is so because the actual conditions responsible for the disruption can be known only in the case of practical and real time systems.

1.1 Real Time System

In a Real-Time System the correctness of the system behaviour depends not only on the logical results of the computations, but also on the physical instant at which these results are produced.. Real-Time systems are classified from a number of viewpoints i.e. on factors outside the computer system and factors inside the computer system. A real-time system changes its state as a function of physical time. The block diagram for the real time system is shown in figure 1.1.

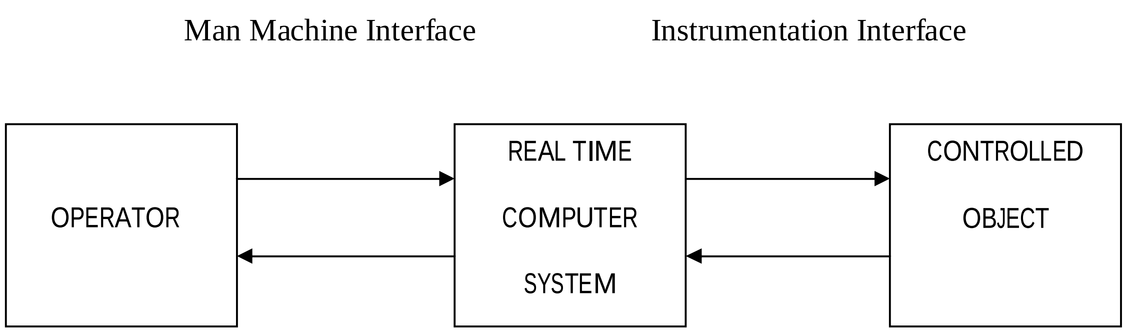

Figure 1.1: Real Time System

A real time system shown in the figure consists of an operator, a human being who operates the overall computer system by giving commands and simulating the design or program responsible for further processing. This computer system is a real time computer system which is controlling the object which is a platform on which the design has to be implemented. Thus a real time system depends on both factors i.e. on the factors inside computer system and outside the computer system. A real time system can handle a multimedia application for which QOS becomes a major constraint as it must be as high as possible [1]. So to maintain QOS, CBS algorithm can be employed which uses DWCS to reduce the variance in all tasks in real time systems. If in a computer system computer utilization is larger than 1 then CBS algorithm shows good performance, however if the CPU utilization changes then WCCBS algorithm can be used since it has some adaptive ability. Further real time system can be classified into two broad categories:

1.1.1 Hard Real Time System

Hard real time systems are those whose response time is of the order of milliseconds or less and can result in a catastrophe is the conditions are not met [1]. The parameters are set and any delay then desired one result in the violation and the system failure occurs. Hard real time systems must remain synchronous with the state of the environment in all cases. Hard real time systems are often safety critical.

1.1.2 Soft Real Time System

Soft real time systems are those whose response time is higher and not very stringent. Soft real-time systems slow down their response time if the load is very high. If an error occurs in a soft real-time system, the computation is rolled back to a previously established checkpoint to initiate a recovery action. In case of soft real time systems a critical real-time task gets priority over other tasks and retains that priority until it completes. Further Soft real-time systems are typically used where there is some issue of concurrent access and the need to keep a number of connected systems up to date with changing situations. Typical example of soft real time system exists in case of phone calling. If the call is not connected in the desired time then queuing of that call occurs until channel becomes free. Once it gets free then call is automatically shifted to unused channel. Table 1.1 describes the difference between Hard and Soft real time systems.

Table 1.1: Difference between Hard and Soft real time systems

CHARACTERSTICS	HARD-REAL TIME	SOFT-REAL TIME
Response Time	Hard Required	Soft Desired
Peak Load Performance	Predictable	Degraded
Control of Pace	Environment	Computer
Safety	Often critical	Non critical
Size of Data Files	Small/Medium	Large
Redundancy Types	Active	Check point recovery
Data Integrity	Short term	Long term
Error Detection	Autonomous	User assisted

A hard real-time system must execute a set of concurrent real-time tasks in such a way that all time-critical tasks meet their specified deadlines. Complex real time systems need databases to support concurrent data access and provide well defined interfaces between software modules [2].

On the other hand non real time systems are those where there is no deadline or time limit for an activity to occur. In these systems a process does not occur immediately. It takes hours or even days for the process to execute. Further a real time system can also be called a distributed real time system which is an integrated system comprising of a set of dedicated hardware that monitors real-world phenomena and acts or reacts on events within specified time period [3]

1.2 Benefits of Real Time Systems

Firstly Real time systems aware all of the value of time. It shows how the efficiency can be enhanced if the work is done in the desired time. Further wastage of time and resources can be minimized since for progressing, time is the main constraint in the today's world. Also automatic tracking of all the processes which is being carried out can be done through real time systems so that any problems if encountered in the work can be removed or analysed at the right time. In the research field real time systems play an important role since real Time Processing generally gives all time slices and system resources to the application or process running in real time. This means that there will be (in most cases) no processing lag caused by the system or other slow applications. Monitoring and control of devices can be achieved only when real time systems are employed. Further signal conditioning systems such as amplifiers, multiplexers, Analog to digital, Digital to Analog converters, Telemetry work only in real time. Real time systems reduces cost and physical footprints, quick partitioning of RAM and I/O devices, sharing of data between different Operating systems take, make better use of multi core hardware.

- **Reduces cost and physical footprints**

  Multi-OS systems that make use of multiple computers often result in inefficiency. By using the NI Real-Time Hypervisor, you can lower hardware costs while reducing the amount of physical space that your system requires. This is especially important in deployed applications, or in locations where floor space is at a premium.

- **Synchronization**

  In multiplexing processing involved in communication such as TDM synchronization is necessary between transmission and reception. Data from different channels are required to be sent on the same channel with the help of commutator. The data received at the destination from the channel is de-commutated to individual channel which is done in real time.

- **Quick partitioning of RAM and I/O devices**

  Different I/O devices can be partitioned to different operating systems such as Lab VIEW and Windows in real time according to supported configurations. Partitioning I/O between operating systems helps to maximize performance. Further RAM can also be divided but speed of execution limits the partitioning. For the same reason RAM size can be increased to avoid delay.

- **Data sharing between different Operating systems**

  The NI Real-Time Hypervisor introduces a virtual Ethernet connection between instances of Lab VIEW Real-Time and Windows XP running on the same controller. This connection is implemented in system memory and enables seamless porting of applications written for traditional (multi-computer) real-time systems.

- **Better Use of Your Multi core Hardware**
  As number of multi processors are increasing on the same chip abruptly because of VLSI technology, due to which there is a need of parallel processing of these multi processors. Hence timing constraint is the most important feature which is overcome by real time processing.

1.3 Advancements in wireless communication

Although the new, third generation (3G) wireless technology has not yet been implemented fully, the work on 4G technology is being carried out with a great pace. 4G consists of those technologies which are not implemented and some are still in planning stages. The first generation (1G) and second generation (2G) of mobile telephony were intended primarily for voice transmission. The third generation of mobile telephony (3G) is serving both voice and data applications. 4G will be employed widely for internet access which is a super-enhanced version of 3G i.e., an entirely packet switched network with all digital network elements and extremely high available bandwidth. Also 4G will bring true multimedia capabilities such as high-speed data access and video conferencing to the handset. It is also envisioned that 4G systems will be deployed with software defined radios, allowing the equipment to be upgraded to new protocols and services via software upgrades. 4G also holds the promise of worldwide roaming using a single handheld device. There are two approaches being used to develop 4G access techniques:

(A). 3xRTT (currently 1xRTT for 2.5 and 3G)

(B). Wideband CDMA (W-CDMA).

These disparate access techniques currently do not interoperate. This issue may be solved with software defined radios. 4G has more fault tolerance capabilities built-in to avoid unnecessary network failure, poor coverage, and dropped calls. 4G is able to enhance QOS by the use of better diagnostic techniques and alarms tools. 4G has better support of roaming and handoffs across heterogeneous networks. 4G technologies such as WiMAX, multiplexing technique like LAS-CDMA, H-ARP as error correction coding

1.3.1 WiMAX

WIMAX is worldwide interoperability for microwave access is the fast growing wireless technology used for internet access. It is third most widely used internet access technology after digital subscriber line and cable modems. Mobile communications such as broadband wireless access is a strong driver for WiMAX. The technology uses OFDM as multiplexing technique which prevents a quite considerable portion of bandwidth from waist age as different frequency bands which are obtained from the single band are orthogonal to each other and due to this property bandwidth is saved as compared to FDM technique. 3G or 4G cellular services have already been deployed for access to advanced voice, video, multimedia, and broadband data services. Now work on voice over Internet protocol (VoIP) on WiMAX is being carried out. Further WiMAX services will be beneficial for those living in rural areas where installation of cables and DSL is limited [4]. It is possible because the WiMAX standard supports mesh topology and smart antenna technologies that increase coverage and throughput especially in extreme environments. This technology has the ability to operate with other networks such as two systems based on different protocols and technologies.

1.3.2 LAS-CDMA

Large Area Synchronized code-division multiple access is the new technology which is being developed by Link Area Communication. LASCDMA will be compatible with all current and future standards, and there is a relatively easy transition from existing systems to LAS-CDMA (using software defined radios). LASCDMA will accommodate all the advanced technologies planned for 4G and that LASCDMA will further enhance both 3xRTT or W-CDMA system's performance and capacity. Chip level equalization can be employed to restore the orthogonality of the user signals which can be destroyed by frequency selective multipath channels [5].

1.3.3 GPP LTE

3GPP LTE is known as 3.9 G technology operating under one name the European Telecommunications Standards Institute. LTE standard includes System architecture evolution, a flat IP based architecture which is designed to replace the GPRS core network. The main features of 3GPP LTE involves:

- Enhancement of the speed and capacity of mobile telephone networks.
- High throughput, low latency, plug and play i.e., FDD and TDD in the same platform.
- A simple architecture resulting in low operating costs.
- MIMO technology can be used in 3GPP LTE providing peak download rates of 326.4 Mb/sec for $\mathbf{4} \times \mathbf{4}$ antennas and 172.8 Mb/s for 2x2 antennas and along with this peak upload rates of 86.4 Mb/s for every 20 MHz of spectrum using a single antenna is provided.
- It provides spectrum flexibility by spectrum slices of as small as 1.4 MHZ and as large as 20MHZ. Further it provides good support for mobility.

The advancements to new technology from the older one can be achieved by using software defined radios. It is done by adding new features to previous technology through software. There are several platforms of SDR which are existing like WARP FPGA, Sundance 8036 etc. In such platforms real time implementation can be done. This implementation involves transmission and reception of data through antennas which are associated with respective daughter radio boards. In Sundance platform a block set is formed associated with the design to be implemented. The individual blocks are programmed either in C or VHDL since both DSP and FPGA processors are available on the kit. Input and outputs of each block are connected in such a way that if both programming languages are used than comports and strobes are used as connectors while simply wires are used if single programming language is used. The simulation is done through Diamond 3L software and signals are then transmitted in real time which is obtained at the receiving antenna. These signals are then processed through the programming done in either processor. On the other hand WARP FPGA board is another platform on which real time implementation can be done. It is so because simulation is done on the Mat lab software and the signals to be transmitted through that software are sent through the antenna at a specified time instant with an entry of transmission delay. Further clocks are provided and no transmission and reception takes place until active age of clock occurs, so if transmission of signals and effect of clock does not occur after the specified delay and active age respectively then the system becomes non real in nature. The board includes radio board as daughter cards which are responsible for transmission and reception.

1.4 System Model

Downloading of the signals from Host PC and its transmission and reception is shown in the figure 1.2. WARP Lab is a framework which brings together WARP and MATLAB

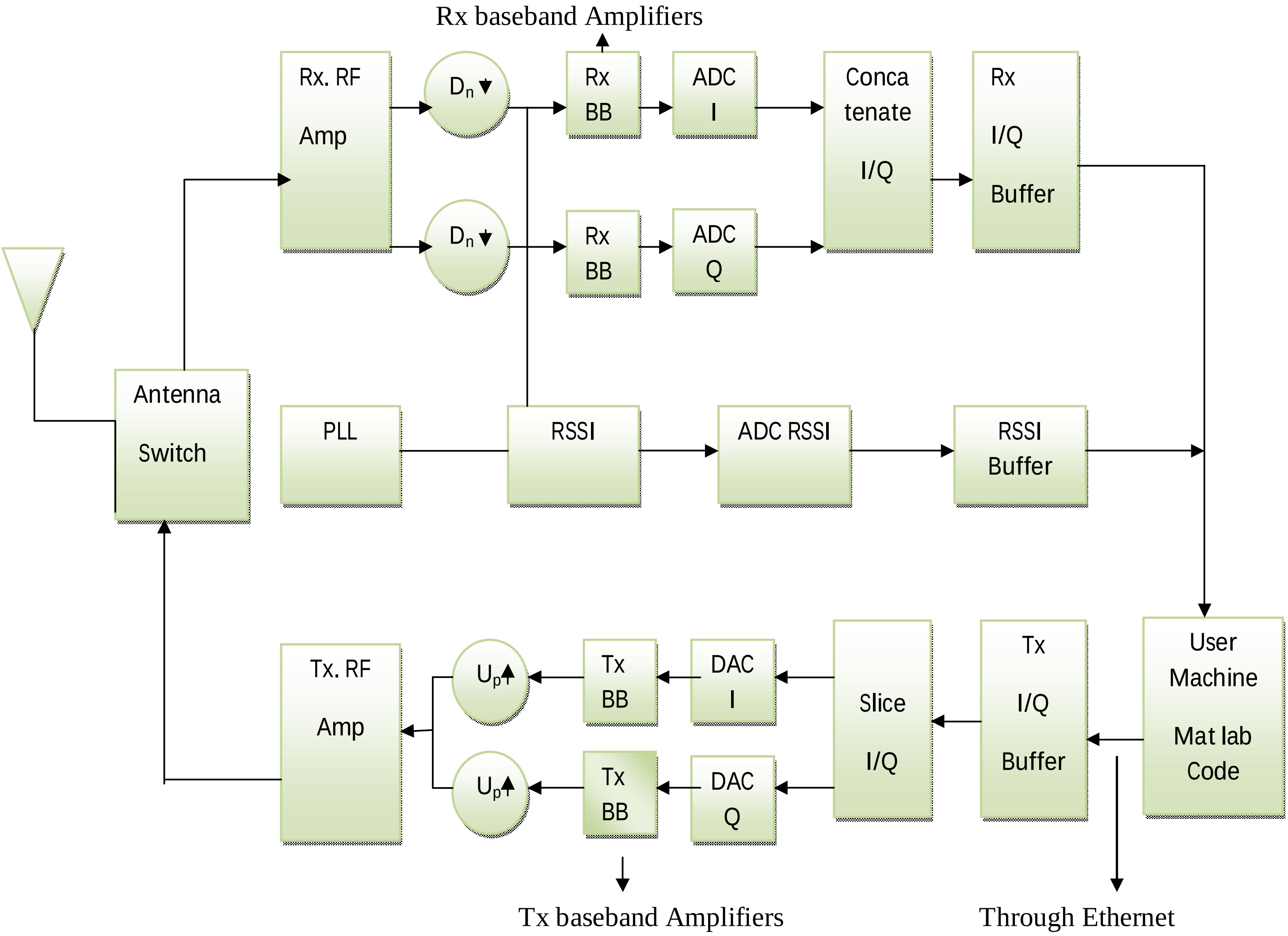

Figure 1.2: System model showing the signal flow and processing

With WARP Lab, interaction between WARP nodes and MATLAB workspace can be done directly and signals generated in MATLAB can be transmitted in real-time over-the-air using WARP nodes.

The Host PC and WARP node are two devices between which the interaction takes place. The Host PC includes the main M-Code and its sub modules such as functions. The MATLAB program can be run and associated with WARP board only through Ethernet interface and is shown in figure 1.2. The Ethernet MAC is designed for operation in 10/100/1000 Mb/sec. In full duplex mode the data rate is 100/1000 Mb/sec and in half duplex mode it is 10/100 Mb/sec. It also provides support for frames of any length. Through Ethernet the signals are downloaded on to the radio boards with the help of Radio controller and Radio bridges. The radio bridge is a custom peripheral which provides the external connections for the radio controller core. The radio controller is a custom peripheral designed to utilize the many functions of the radio boards. It contains SPI logic to set the registers in the Radio and DAC chips on the boards and logic to keep track of the control pins for both of the chips. Also provided with the radio controller are drivers that enable the use of the radio controller The Radio bridge which is supporting the radio controller contains very little logic; its only job is to tie the radio controller's ports to whichever daughter card slots contain WARP radio boards. Abstracting these connections to a separate peripheral allows the use of a single radio controller core with arbitrary arrangements of radio boards. WARP FPGA board has a simple circuitry for handling the different issues related to downloading, processing and transmission of signals. The tool used for the accessing the processor is Xilinx *ISE* IMPACT. This tool is responsible for configuring the upstream and downstream devices using JTAG boundary scan, preparing PROM file, system ACE file, Boundary-scan file and downloading connection cable (Ethernet) and bit stream required for the processing of the signal. The block constitutes Ethernet as the mode for accepting the signal to be transmitted. The I/Q signals entered is buffered using transmitter buffer which is sliced into I and Q form individually. The Digital to Analog converters are given inputs in I/Q form whose amplified outputs are then up converted to increase the frequency. This interpolated RF is then amplified and sends via TX antenna. The signals transmitted are received at the antenna of receiving board where these signals are amplified. The amplified signals are decimated with the help of PLL (phase locked loop) so as to make the received frequency same as that of transmitted baseband signal. The down converted baseband is amplified and then given to Analog to digital converters which individually convert the Analog I and Q waveforms into digital domain. Concatenation of I and Q occurs and this combined signal is then buffered to Ethernet. The received signals are now further processed offline so as to obtain the correct signal.

1.5 Objective of Thesis

- Study of Real time systems and its benefits in practical usage.
- Study of WARP FPGA board
- Study of Different modulation techniques
- Implementation of various digital modulation techniques on WARP platform.
- Comparison of the modulation techniques for their performance in real time.

1.6 Outline of Report

In this report performance of different modulation techniques in real time hardware implementation is presented. The remaining of the report is organized as follows:

In chapter 1, Introduction of Real time systems, its benefits and new advancements in wireless communication are discussed.

In chapter 2, Literature survey of real time systems, applications of modulation techniques and WARP FPGA board is briefly presented.

In chapter 3, Description of WARP FPGA board involving its main modules used in the signal processing is presented.

In chapter 4, Different modulation techniques along with diversity, maximal ratio combining are briefly described. Also the expressions for bit error rate and symbol error rates using MGF approach for BPSK, MPSK and MQAM are also presented.

In chapter 5, Simulation details and parameters used in simulating the design code are presented. A flow chart of total procedure is also shown.

In chapter 6, Implementation Results for various modulation techniques is presented.

CHAPTER 2

LITERATURE SURVEY

According to "**J. Sifakis and S. Tripakis**" [6] timed models can be build in real time by adding constraints to the application software. The constraints taken into account for building models are the execution times of the statements, the behaviour of system's external environment and scheduling policies. The analyzable timed model of real time can be build by composing a high level language code.

According to "**M.A. Hannan and A. Hussain**" [7] BPSK modulation scheme for SDR can be employed to pick the constellation size that offers the best reconstructed signal quality for each average SNR. BPSK has the better quality for a given SNR and due to this reason, it is used as the basic mode for each physical layer since it has the maximum coverage range among all transmission modes.

According to "**Y. Linn**" [8] a channel signal-to-noise ratio (SNR) estimator for M-ary phase shift keying (M-PSK) and differential M-PSK is proposed which does not require prior carrier synchronization, has a compact Fixed-point hardware implementation suitable for Field-programmable gate arrays and application-specific integrated circuits, requires only 1sample/symbol and the estimator is resistant to imperfections in the automatic gain control circuit.

According to "**R. Kowalski**" [9] adaptive QAM modulation results in the preventing the disruption of signals by changing the order of modulation. The radio system automatically changes the modulation on encountering with non favourable conditions; however non real time systems may be affected by this while real time systems remain uninterrupted. It also increases the throughput but signal to noise ratio must be maintained to overcome interference and noise.

According to "**H. G. Yeh and H. Seo**" [10] a bit level decoding scheme based on the signal constellation can be used to decode the QAM signal with less complexity as this scheme does not require multiplications and addition computations as the order of modulation increases which is done in case off conventional Log likelihood detectors. BER performance is same as that of conventional demodulators.

According to "**Yair Linn**" [11] an architecture i.e. Linn architecture for coherent M-PSK reception which covers the structures of carrier PLL phase detection, carrier PLL lock detection, symbol timing and error detection, symbol timing PLL lock detection, SNR estimation, loop filter design is very resilient to automatic gain control imperfections and is optimized for implementation using fixed point binary arithmetic. Further the architecture is suitable for low power operation and high data rates.

According to "**Y. Wu and Y. R. Shayan**" [12] a high speed multi level Quadrature amplitude modulation modems can be implemented using field programming gate arrays. For this different algorithms and architectures available for digital filters are exploited since digital filter is a key component of a QAM modem. The design is based on parallel pipelined structure and Look up table implementation so that it can be benefited from the chip size. Also arithmetic precision is employed to avoid over flow so that output is always précised and it is not sacrificed to attain high speeds.

According to "**G. Wang and B. Yin**" [13] WARP FPGA hardware can be used for the implementation of high data rate LTE uplink receiver with multiple antennas to ensure high reliability and data rate. 4G technologies such as OFDM suffer from high peak to average power ratio which requires sophisticated power amplifiers in the handsets which is a major problem. To combat this LTE uplink is optimum choice which uses Single carrier frequency division multiple access scheme and has lower PAPR due to its inherent structure.

According to "**Franz Edbauer**" [14] a coherent detection scheme for differentially encoded binary and quaternary PSK modulation can be employed to reduce the bit error rate. The improvement is based on regeneration of bits and PSK symbols which is based on using multiple delayed symbols as phase references and on feedback of detected symbols.

CHAPTER 3
WARP FPGA DESCRIPTION

WARP is wireless open access research platform. WARP was developed in Rice University in U.S.A. by Murphy Brothers. WARP is being widely used throughout the world for research in wireless domain. Many wireless applications can be run and implemented on WARP-FPGA board such as SISO, MIMO and SIMO. WARP, the Wireless Open-Access Research Platform is a hardware involving FPGA as the main module. WARP board consists of other modules such as Analog board, Clock board, Radio board, User I/O board and Video board [15]. The most important of these is Radio board which is responsible for transmission and reception of signals. To each radio board, antennas are connected with helical radiation pattern. The transmitted signal frequency is 2.4 GHZ. Along with this other hardware modules and I/O ports associated with WARP board are WARP FPGA board memory resources, WARP FPGA board user I/O, WARP FPGA Board Power Supplies, WARP FPGA Board Clocking, Ethernet, WARP Multi gigabit Transceivers. The WARP FPGA board has been shown in the figure 3.1 in operating mode.

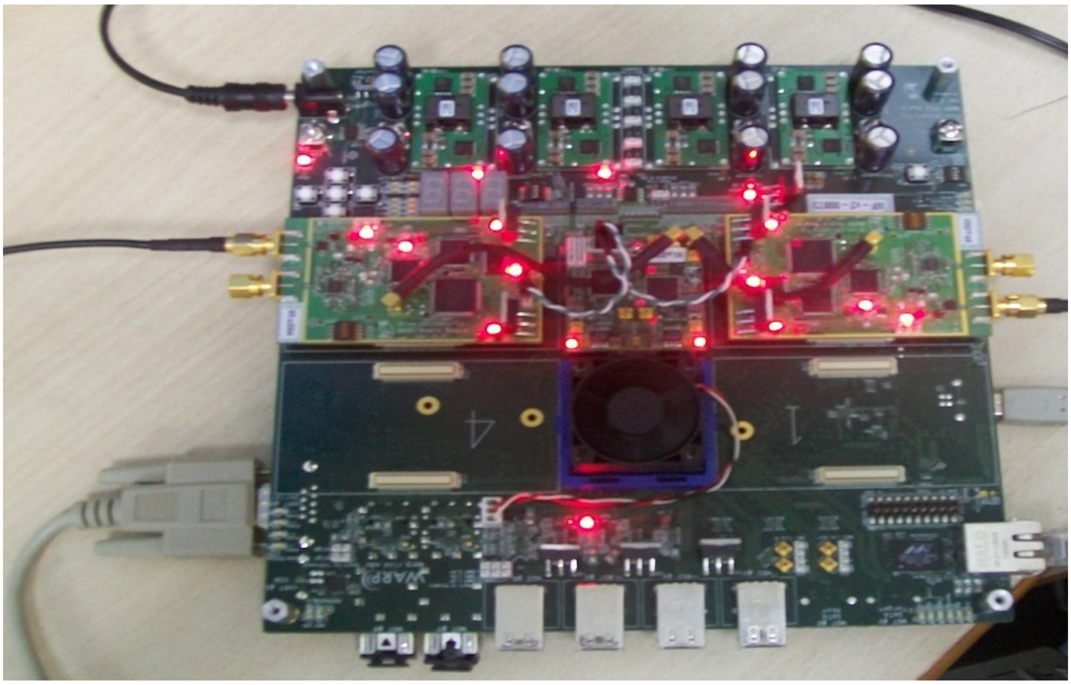

Figure 3.1: WARP FPGA in operating mode

To use the board firstly generate a vector of samples to be transmitted and send the samples to the WARP board. Then WARP board is prepared for the transmission and reception by connecting accurately the I/O ports. The signals generated for the transmission through MATLAB programming are then downloaded to the buffer of the transmission board and then these signals are processed and transmitted through the antenna associated with that radio board. The boards must be programmed with the WARP Lab bit stream because this bit stream provides storage of RSSI values and the receiver reads these RSSI values. The signals to be transmitted are undergone different modulation techniques separately and are then transmitted through radio board which is one of the modules of WARP board discussed below.

3.1 Modules of WARP FPGA board

WARP board involves various hardware modules along with I/O interfaces such as WARP FPGA board memory resources, WARP FPGA board user I/O, WARP FPGA Board Power Supplies, WARP FPGA Board Clocking, Ethernet, WARP Multi gigabit Transceivers, etc.

3.1.1 WARP FPGA Daughter Cards

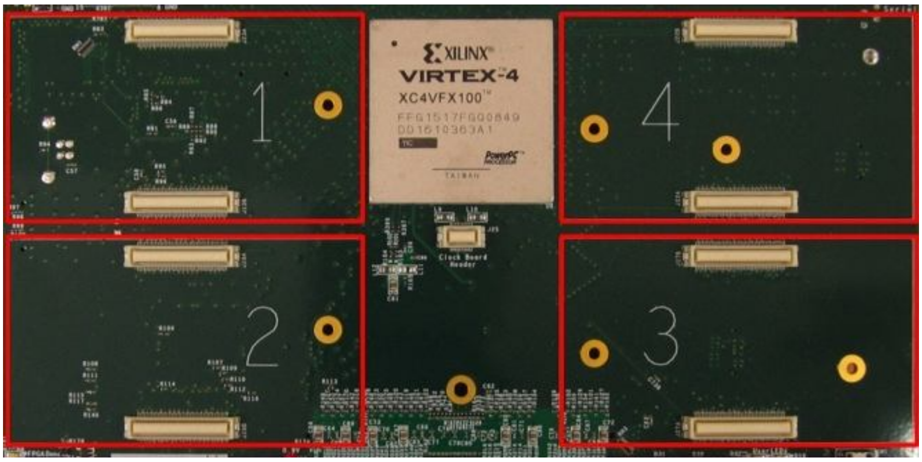

Figure 3.2: WARP FPGA Radio Daughter Card [15]

The WARP FPGA Board has four daughter card slots. One of the Daughter card has been shown in the figure 3.2.The four slots are electrically and mechanically identical. The WARP hardware supports any combination of daughter cards in the four slots. However, a given FPGA design will require a specific arrangement of daughter cards once synthesized. The four Daughter card slots on the WARP FPGA board are given with 5v supply. A second power plane is also connected to the Daughter card slots and can be driven by an off-board supply via a dedicated 6-pin header on the FPGA board. A Clock is provided which initiates transmission and reception of signals by sending SYNC pulse whenever required.

3.1.2 ETHERNET

The FPGA Board has one 10/100/1000 Ethernet device present which is shown in figure 3.3. The design uses the Marvell Gigabit Ethernet PHY which implements all the physical layer functionality and the Virtex-4 FPGA uses one of the hardened Tri-mode Ethernet MAC for the MAC layer.

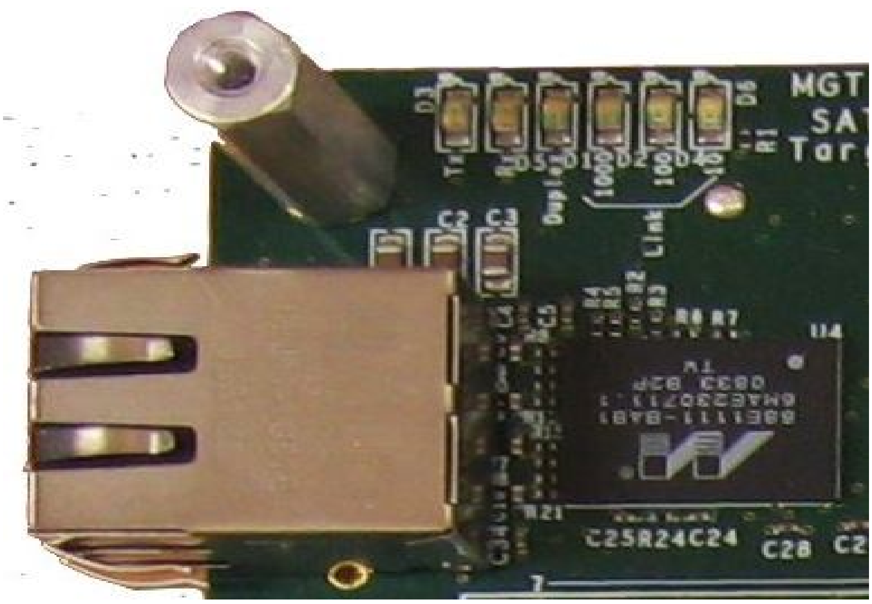

Figure 3.3: Ethernet for Interfacing WARP Board and MATLAB [15]

Physical layer link is shown by LEDs which show the status such as packet transmission, packet reception, duplex link and speed. Maximum Speed of 1Gbps and minimum of 10Mbps can be achieved.

WARP FPGA consists of Multi gigabit transceivers (MGT) as another module. There are ten pairs of MGTs each of which works in full duplex mode and supports data rate of 6.5Gbps. Eight MGT interfaces are there in all which are mapped to the corresponding MGT in FPGA through different connectors known as jumpers. Off board connectors and Oscillators are two sources for providing clock to MGT. Further MGT can be given clock externally as an input and also can give clock externally. A global clock is provided on the WARP board to provide clocking to radio boards. WARP also consists of RAM having 6.7 MB of memory in the form of logic slices. A DDR slot is there which is routed to dedicated I/O and clocking resources and supports up to 2GB modules. Further a user I/O is also provided which are intended for debugging custom designs in the hardware. Five FPGA inputs are provided which are connected to external pull down registers such that when a button is pressed logic high occurs and otherwise logic low. WARP FPGA board operates from a single external 12v supply while Radio daughter cards slot supply is 5v supply.

CHAPTER 4

MODULATION TECHNIQUES USING MGF APPROACH

Fading in the signals has been the major issue of all times and it has to be minimized to reduce the error rates of the received signal. In wireless communications, fading is deviation of the attenuation that a carrier-modulated telecommunication signal experiences over certain propagation media. The fading may vary with time, geographical position and/or radio frequency, and is often modelled as a random process. A fading channel is a communication channel that experiences fading. In wireless systems, fading is either due to multipath propagation, referred to as multipath induced fading, or due to shadowing from obstacles affecting the wave propagation, sometimes referred to as shadow fading. Radio waves emitted by a transmitter antenna may arrive at a receiver antenna by travelling along a multitude of paths. While a direct line-of-sight (LOS) path between the transmitter antenna and the receiver antenna may exist in some systems, there is no LOS path available for many urban and indoor wireless links [16]. Multiple transmitted signal rays arrive at the receiver, some experiencing reflection, refraction, and/or diffraction along the transmission path. The rays arriving at the receiver have random amplitudes and phases. This gives rise to multipath signal fading as the rays add destructively in some locations and constructively in others. Different types of fading exist such as Rayleigh fading, Rician fading, Nakagami fading, Weibull fading**.**

4.1 Diversity

In telecommunications, a diversity scheme refers to a method for improving the reliability of a message signal by using two or more communication channels with different characteristics. Diversity plays an important role in combating fading and co-channel interference and avoiding error bursts. It is based on the fact that individual channels experience different levels of fading and interference. Multiple versions of the same signal may be transmitted and/or received and combined in the receiver. Alternatively, a redundant forward error correction code may be added and different parts of the message transmitted over different channels. Diversity techniques may exploit the multipath propagation, resulting in a diversity gain.

4.1.1 Transmitter Diversity

Transmit diversity is radio communication using signals that originate from two or more independent sources that have been modulated with identical information-bearing signals and that may vary in their transmission characteristics at any given instant.

4.1.2 Receiver Diversity

Diversity combining is the technique applied to combine the multiple received signals of a diversity reception device into a single improved signal.

4.2 Modulation Techniques

4.2.1 M-PSK (M-ary Phase Shift Keying)

This is the modulation technique which used M=2^K symbols such that there are k number of bits in each symbol. On the basis of value of M different PSK modulations are described below.

BPSK (Binary Phase Shift Keying)

In BPSK, phase of carrier changes whenever there is a change in bit sequence occurs. BPSK (also sometimes called PRK, Phase Reversal Keying, or 2PSK) is the simplest form of phase shift keying (PSK). It uses two phases which are separated by 180° and so can also be termed 2-PSK. It does not particularly matter exactly where the constellation points are positioned, and in this figure they are shown on the real axis, at 0° and 180°. The number of bits contained in a symbol is decided by the formulae $M = 2^K$, where M denotes the number of symbols and K represents the number of bits in that symbol. This modulation is the most robust of all the PSKs since it takes the highest level of noise or distortion to make the demodulator reach an incorrect decision. It is, however, only able to modulate at 1 bit/symbol and so is unsuitable for high data-rate applications when bandwidth is limited. The constellation diagram for BPSK is shown in the figure 4.1 with 0 and 1 as the symbols.

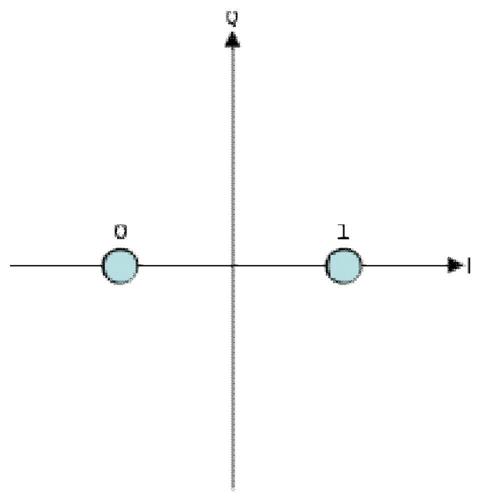

Figure 4.1: Constellation diagram for BPSK

QPSK (Quadrature Phase Shift Keying)

QPSK is a modulation scheme which uses four symbols and each symbol has two bits associated with it. QPSK uses four points on the constellation diagram, equispaced around a circle. With four phases, QPSK can encode two bits per symbol, shown in the diagram with Gray coding to minimize the BER — twice the rate of BPSK. Analysis shows that this may be used either to double the data rate compared to a BPSK system while maintaining the bandwidth of the signal or to maintain the data-rate of BPSK but halve the bandwidth needed. The implementation of QPSK is more general than that of BPSK and also indicates the implementation of higher-order PSK. Further the symbols in the constellation diagram in terms of the sine and cosine waves are shown in the figure 4.2

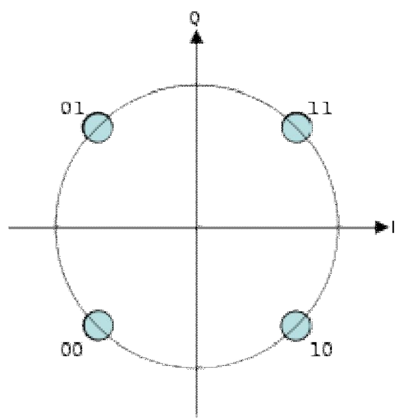

Figure 4.2: Constellation of QPSK

8-PSK

In 8 PSK modulation three bits are contained in a particular symbol i.e. K=3. These symbols are mapped onto the constellation diagram. Gray coding is done so as to minimize the error probability since there is only one bit difference between two consecutive symbols if we are using gray coding. 8 PSK is higher order constellation with symbols very close to each other causing more bit error as compared to lower order modulations. The constellation diagram is shown in figure 4.3

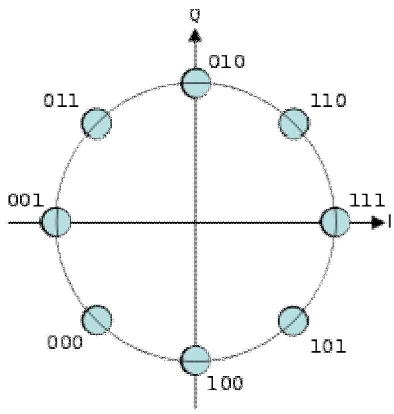

Figure 4.3: Constellation diagram of 8PSK

Likewise 16 PSK and 32 PSK are higher order modulation techniques which have four and five bits per symbol respectively. The bit error rate reduces as the modulation order increases. For BPSK and QPSK there is an ambiguity of phase if the constellation is rotated by some effect in the communications channel through which the signal passes. This problem can be overcome by using the data to change rather than set the phase. This can be achieved by using DPSK (Differential Phase Shift Keying).

4.2.2 DPSK (Differential Phase Shift Keying)

In differentially-encoded BPSK a binary '1' may be transmitted by adding 180° to the current phase and a binary '0' by adding 0° to the current phase. In differentially-encoded QPSK, the phase-shifts are 0°, 90°, 180°, -90° corresponding to data '00', '01', '11', '10'. This kind of encoding may be demodulated in the same way as for non-differential PSK but the phase ambiguities can be ignored. Thus, each received symbol is demodulated to one of the M points in the constellation and a comparator then computes the difference in phase between this received signal and the preceding one. The difference encodes the data as described above.

4.2.3 QAM (Quadrature Amplitude Modulation)

Quadrature amplitude modulation (QAM) is both an analog and a digital modulation scheme. It conveys two analog message signals, or two digital bit streams, by changing (modulating) the amplitudes of two carrier waves, using the amplitude-shift keying (ASK) digital modulation scheme or amplitude modulation (AM) analog modulation scheme. These two waves, usually sinusoids, are out of phase with each other by 90° and are thus called quadrature carriers or quadrature components — hence the name of the scheme. The modulated waves are summed, and the resulting waveform is a combination of both phase-shift keying (PSK) and amplitude-shift keying (ASK), or in the analog case of phase modulation (PM) and amplitude modulation. In the digital QAM case, a finite number of at least two phases and at least two amplitudes are used. PSK modulators are often designed using the QAM principle, but are not considered as QAM since the amplitude of the modulated carrier signal is constant. QAM is used extensively as a modulation scheme for digital telecommunication systems. 8-QAM constellation is known to be the optimal 8-QAM constellation in the sense of requiring the least mean power for a given minimum Euclidean distance. QAM amplitude modulate the signals which are phase modulated by PSK modulation technique due to which performance is increased since two modulations are taking place concurrently. Rectangular 16 QAM constellations is shown in the figure 4.4 where four bits are incorporated in a particular symbol

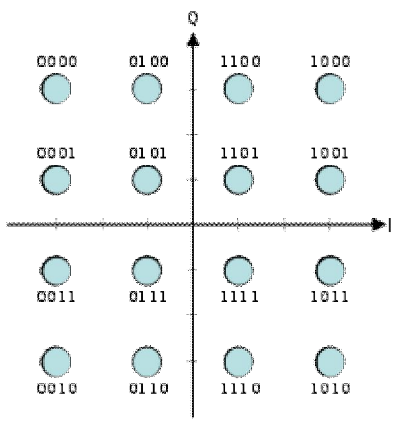

Figure 4.4: Constellation of 16 QAM

QAM can be of various types such as rectangular, non rectangular or circular. In rectangular QAM constellations are, in general, sub-optimal in the sense that they do not maximally space the constellation points for a given energy. However, they have the considerable advantage that they may be easily transmitted as two pulse amplitude modulation (PAM) signals on quadrature carriers, and can be easily demodulated. The non-square constellations, dealt with below, achieve marginally better bit-error rate (BER) but are harder to modulate and demodulate. The circular 8-QAM constellation is known to be the optimal 8-QAM constellation in the sense of requiring the least mean power for a given minimum Euclidean distance. The 16-QAM constellation is suboptimal although the optimal one may be constructed along the same lines as the 8-QAM constellation. The circular constellation highlights the relationship between QAM and PSK. Other orders of constellation may be constructed along similar (or very different) lines. It is consequently hard to establish expressions for the error rates of non-rectangular QAM since it necessarily depends on the constellation. The comparison for modulation techniques is shown in the Table 2.1 below:

Table 2.1: Comparison between various modulation techniques [17]

Comparison parameter	**M-ary PSK**	**DPSK**	**QAM**
Equation of the transmitted signal	s(t)=b(t)$\sqrt{2P_s}$ cos(2$\pi f_c t + \varphi_m)$ $\varphi_m)$=(2m+1)p/M m=0,1,2,...M-1	s(t)=b(t)$\sqrt{2P_s}$ cos(2$\pi f_c t)$ b(t) differentially coded	s(t)=Acos($2\pi f_c t + \varphi)$
Bits per symbol	N	One	One
Detection method	coherent	Non coherent	coherent
Minimum Euclidean distance signal points	2$\sqrt{E_s}$ sin$\frac{\pi}{M}$	--	$\frac{\sqrt{2}}{\sqrt{M-1}}$
Minimum Bandwidth	$2f_{b/N}$	f_b	f_b

4.3 Maximal Ratio Combining

In Wireless communication, maximal-ratio combining is a method of diversity combining in which the signals from each channel are added together, the gain of each channel is made proportional to the RMS signal level and inversely proportional to the mean square noise level in that channel, different proportionality constants are used for each channel. It is also known as ratio-squared combining and pre detection combining. Maximal-ratio-combining is the optimum combiner for independent AWGN channels. The performance of MRC over fading channels is of great interest. Most of the models for these systems typically assume either Rayleigh paths or independent identically distributed Nakagami or Rician paths. These idealizations are not always realistic since the average fading power and the severity of fading may vary from one path to another when, for example, multipath diversity is employed. The modulation techniques employed for the transmission are M-PSK and M-QAM. The bit error rate for these techniques can be found by the MGF approach. MGF is Moment Generation Function responsible for finding of bit/symbol error rate of the various modulation techniques.

4.4 MGF (Moment Generation Function)

MGF is Moment Generation Function responsible for finding of bit/symbol error rate of the various modulation techniques [18]. Let X be one dimensional variate and let F(x) be its distribution function .Then the function in equation (1) is moment generation function of $\boldsymbol{X}$.

$$\boldsymbol{G(\propto) = E(e^{a\propto)}dF(x)}$$, $\boldsymbol{a}$ is a real quantity (1)

The integral is assumed to converge for a in some neighbourhood of the origin.

4.4.1 Average bit error rate of binary PSK signals using MGF approach

The one-dimensional Gaussian function$Q(x)$, is defined as the complement of the cumulative distribution function (CDF) corresponding to the normalized (zero mean, unit variance) Gaussian random variable X. The canonical representation of this function is in the form of a semi-infinite integral of the corresponding probability density function (PDF) as represented in equation (2)

$$Q(x) = \int_{x}^{\infty} 1/2\pi \exp\left(\frac{-y^2}{2}\right) dy \quad (2)$$

If L branch MRC receiver is considered then for equally likely transmitted symbols, the total conditional SNR per symbol, γ_t at the output of the MRC combiner is given by the (3) equation

$$\gamma_t = \sum_{l=1}^{L} \gamma_l \quad (3)$$

Equation (4) gives the conditional BER, $P_b(E|\{\gamma_l\}_{l=1}^{L})$, for coherent binary signals

$$P_b(E|\{\gamma_l\}_{l=1}^{L}) = Q(\sqrt{2g\gamma_t}) \quad (4)$$

where g=1 for coherent BPSK. Using equation (2) in equation (4), the conditional BER is given by the equation (5)

$$P_b(E|\{\gamma_l\}_{l=1}^{L}) = 1/\pi \int_0^{\frac{\pi}{2}} \exp\left(\frac{-g\gamma_t}{sin^2\varphi}\right) d\varphi = 1/\pi \int_0^{\frac{\pi}{2}} \prod_{l=1}^{L} \exp\left(\frac{-g\gamma_l}{sin^2\varphi}\right) d\varphi \quad (5)$$

This form of the conditional BER is more desirable since we can independently average over the individual statistical distributions of the γ_l's and then perform the integral over φ.

4.4.1.1 Average BER with Multichannel Reception

To obtain the unconditional BER, $P_b(E)$, when multichannel reception is used, we must average the multichannel conditional BER $P_b(E|\{\gamma_l\}_{l=1}^{L})$ over the joint PDF of the instantaneous SNR sequence $\{\gamma_l\}_{l=1}^{L}$. Since the random variables $\{\gamma_l\}_{l=1}^{L}$are assumed to be statistically independent therefore

$p_{\gamma_1,\gamma_2,\ldots,\gamma_l}(\gamma_1,\gamma_2,\ldots\gamma_l) = \prod_{l=1}^{L} p_{\gamma l}(\gamma_l)$ and the averaging procedure results in the equation (6)

$$P_b(E) = \int_0^{\infty}\int_0^{\infty} \dots\dots \int_0^{\infty} P_b\,(\{\gamma_l\}_{l=1}^{L}) \prod_{l=1}^{L} p_{\gamma l}(\gamma_l) d\gamma_1\, d\gamma_2 \dots .\, d\gamma_L \qquad (6)$$

Using equations (5) in (6) alternative product form representation of BER is given by the equation (7)

$$P_b(E) = \int_0^{\infty}\int_0^{\infty} \dots\dots \int_0^{\infty} \frac{1}{\pi} \times \int_0^{\frac{\pi}{2}} \prod_{l=1}^{L} \exp\left(\frac{-g\gamma_l}{sin^2\varphi}\right) \prod_{l=1}^{L} p_{\gamma l} d\emptyset(\gamma_l) d\gamma_1\, d\gamma_2 ..\, d\gamma_L \quad (7)$$

The integrand in 6 is absolutely integrable, and hence the order of integration can be interchanged. Thus, grouping terms of index , equation (8) is obtained

$$P_b(E) = 1/\pi \int_0^{\frac{\pi}{2}} \prod_{l=1}^{L} M_{\gamma_l}\left(\frac{-g}{sin^2\varphi}\right) d\emptyset \qquad (8)$$

Where $M_{\gamma_l}(s) = \int_0^{\infty} p_{\gamma_l}(\gamma_l) e^{s\gamma_l} d\gamma_l$ is the MGF of the SNR per symbol associated with the path l. If the fading is identical throughout for all models then equation (8) reduces to equation (9)

$$P_b(E) = 1/\pi \int_0^{\pi/2} (M_{\gamma}\left(\frac{-g}{sin^2\varphi}\right))^L d\varphi \qquad (9)$$

Hence, in all cases this approach reduces the $(L + 1)$-fold integral with infinite limits of equation (7) to a single Finite range integral of equation (9) whose integrand contains only elementary functions such as exponentials and trigonometric, and which can therefore easily be evaluated numerically.

4.4.1.2 Average symbol error rate for M-PSK

In M-PSK, symbols are formed from the input bit stream by binary to decimal conversion. Now following the same steps as in equation 6 and 8, the SER for M-PSK is given by the equation (10)

$$P_s(E|\{\gamma_l\}_{l=1}^{L}) = 1/\pi \int_0^{(M-1)\pi/M} \exp\left(\frac{-g_{PSK}\gamma_t}{sin^2\varphi}\right) d\varphi \tag{10}$$

$$= 1/\pi \int_0^{(M-1)\pi/M} \prod_{l=1}^{L} \exp\left(\frac{-g_{PSK}\gamma_l}{sin^2\varphi}\right) d\varphi$$

Where $g_{PSK} = sin^2(\frac{\pi}{M})$

The average SER of M-PSK modulation over generalized fading channel is given by the equation (11)

$$P_s(E) = 1/\pi \int_0^{(M-1)\pi/M} \prod_{l=1}^{L} \mathrm{M}_{\gamma_l}\left(\frac{-g_{PSK}\gamma_l}{sin^2\varphi}\right) d\varphi \tag{11}$$

The equation10 generalizes the M-PSK average SER results for L independent identically distributed Rayleigh paths. Further if $L = 1$, the equation 10 can be used to evaluate the average SER performance of M-PSK with single-channel reception. Therefore generalized SER performance for single channel reception is given by equation (12)

$$P_s(E) = 1/\pi \int_0^{(M-1)\pi/M} \mathrm{M}_{\gamma_l}\left(\frac{-g_{PSK}\gamma_l}{sin^2\varphi}\right) d\varphi \tag{12}$$

4.4.2 Average SER of M-QAM

M-QAM modulation technique is a hybrid modulation of PSK and AM i.e. the bit stream is phase modulated after its division into groups which depend on the value of M and then it is amplitude modulated to form a QAM signal.

4.4.2.1 Average Symbol Error Rate of M-AM Signals

The signal points located symmetrically about the origin, is given by the equation (13)

$$P_s(E|\{\gamma_l\}_{l=1}^{L}) = \frac{2(M-1)}{M} Q\left(\sqrt{2g_{AM}\gamma_t}\right) \quad (13)$$

Where $g_{AM} = \frac{3}{(M^2-1)}$. The Gaussian Q function is given by equation (14)

$$Q(x) = 1/\pi \int_0^{\pi/2} \exp\left(\frac{-x^2}{2sin^2\theta}\right)d\theta, \text{ for } x \geq 0 \quad (14)$$

Using equation (14) in equation (13) SER in desired product form can be obtained and is shown in equation (15)

$$P_s(E|\{\gamma_l\}_{l=1}^{L}) = \frac{2(M-1)}{M\pi}\int_0^{\pi/2} \exp\left(\frac{-g_{AM}\gamma_t}{sin^2\varphi}\right)d\varphi$$

$$= \frac{2(M-1)}{M\pi}\int_0^{\pi/2}\prod_{l=1}^{L} \exp\left(\frac{-g_{AM}\gamma_t}{sin^2\varphi}\right)d\varphi \quad (15)$$

Now following the same steps from equation (6) to equation (8) SER for generalized fading channels is given by equation (16)

$$P_s(E) = \frac{2(M-1)}{M\pi}\int_0^{\pi/2}\prod_{l-1}^{L} M_{\gamma_l}\left(\frac{-g_{AM}}{sin^2\emptyset}\right)d\emptyset \quad (16)$$

4.4.2.2 Average Symbol Error Rate of Square M-QAM Signals

Consider square M-QAM signals whose constellation size is given by $M = 2^K$ with K even. The conditional SER for square M-QAM is given by equation (17)

$$P_s(E\big|\{\gamma_l\}_{l=1}^{L}) = 4\left(1-\frac{1}{\sqrt{M}}\right)Q(\sqrt{2g_{QAM}\gamma_t}$$

$$- 4(1-1/\sqrt{M})^2\ Q^2(\sqrt{2g_{QAM}\gamma_t}) \qquad (17)$$

Where g_{QAM} = 3/2(M -1), now using alternative Q function in equation 13 and its square form the conditional SER may shown by equation (18)

$$P_s(E\big|\{\gamma_l\}_{l=1}^{L}) =$$

$$\frac{4}{\pi}\left(1-\frac{1}{\sqrt{M}}\right)\int_0^{\frac{\pi}{2}}\exp\left(\frac{-g_{AM}\gamma_t}{sin^2\varphi}\right)d\varphi - \frac{4}{\pi}(1-1/\sqrt{M})^2\int_0^{\pi/4}\exp\left(\frac{-g_{AM}\gamma_t}{sin^2\varphi}\right)d\varphi \qquad (18)$$

The average SER of square M-QAM signal is given by the equation (19)

$$P_s(E\big|\{\gamma_l\}_{l=1}^{L}) = 4/\pi(1-\frac{1}{\sqrt{M}})\int_0^{\pi/2}\prod_{l=1}^{L}\exp\left(\frac{-g_{QAM}\gamma_l}{sin^2\emptyset}\right) - 4/\pi(1-1/$$

$$\sqrt{M})^2\int_0^{\pi/4}\prod_{l=1}^{L}\exp\left(\frac{-g_{QAM}\gamma_l}{sin^2\emptyset}\right)d\emptyset \qquad (19)$$

Steps from equation 5 to equation 7 are followed to yield the average SER of M-QAM over generalized fading channel and given by equation (20)

$$P_{s\,(E)} =$$

$$\frac{4}{\pi}(1-\frac{1}{M})\int_0^{\frac{\pi}{2}}\prod_{l=1}^{L}M_{\gamma_1}(\frac{-g_{QAM}\gamma_l}{sin^2\emptyset})d\emptyset - \frac{4}{\pi}(1-1/\sqrt{M})^2\int_0^{\pi/4}\prod_{l=1}^{L}M_{\gamma_l}(\frac{-g_{QAM}}{sin^2\emptyset})d\emptyset$$

(20)

The expression shown above is SER for the M-QAM modulation technique. For single channel reception L must be set to 1.

CHAPTER 5

SIMULATION PARAMETERS

Different modulation techniques have been implemented on the WARP FPGA board and comparison has been made between bit error rate and baseband signal gain. The bit error rate for BPSK is least and it increases with the modulation order. The SISO configuration has been taken into account for transmission and reception of signals.

5.1 Simulation Details

A lot of parameters are used in the simulation of program which are shown in the Table 3.1.

Table 3.1: Simulation parameters

Transmission Delay	**0 to 16384**
Transmission Length	0 to 16384-Transmission delay
Carrier Channel	1 to14
Base Band Transmitter Gain	0 to 3
RF Transmitter Gain	0 to 63
Base Band Receiver Gain	0 to 31
RF Receiver Gain	1 to 3
Transmission Mode	0 for single transmission 1 for continuous transmission
Gain Control	0 to enable automatic gain control 1 to enable manual gain control

5.2 Flow Chart of working model

Below is the description of step by step procedure of process which takes place outside and inside of WARP FPGA board. There are two devices interfacing of which results in the proper signal flow and its processing. Interfacing of these two devices is done through Ethernet which provides a speed of 100Mbps. JTAG cable has to be downloaded to provide connectivity between Host PC and WARP FPGA board. Further JTAG RS232 provides compatibility between these two devices. Initialization of various global parameters like RF and BB gains of transmitter and receiver is done. Socket handling and nodes are also initialized as global parameters. Along with these Transmission parameters such as Transmission Length, TX Delay,

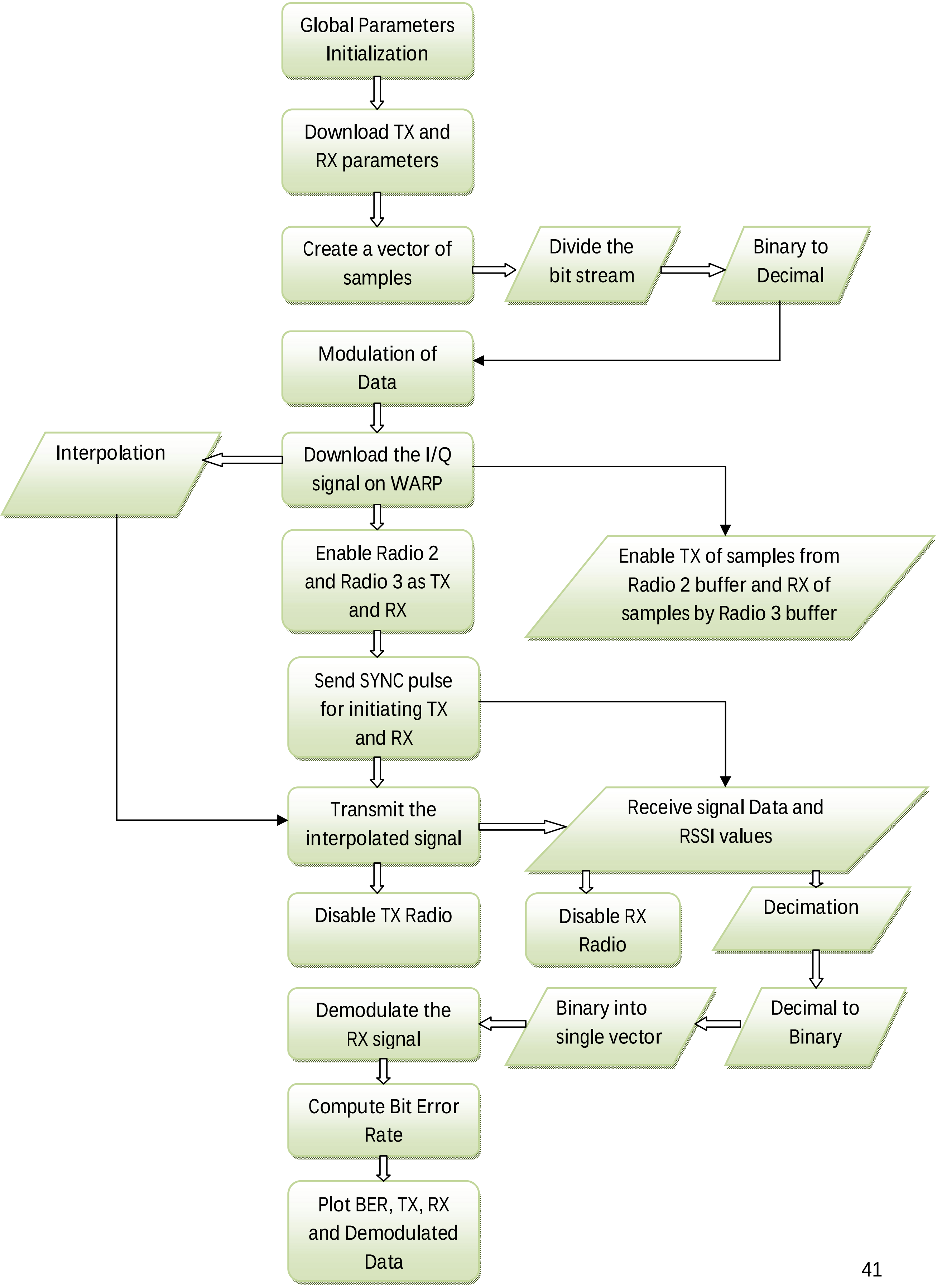
Global Parameters Initialization
Download TX and RX parameters
Create a vector of samples
Divide the bit stream
Binary to Decimal
Modulation of Data
Download the I/Q signal on WARP
Interpolation
Enable Radio 2 and Radio 3 as TX and RX
Enable TX of samples from Radio 2 buffer and RX of samples by Radio 3 buffer
Send SYNC pulse for initiating TX and RX
Transmit the interpolated signal
Receive signal Data and RSSI values
Disable TX Radio
Disable RX Radio
Decimation
Demodulate the RX signal
Binary into single vector
Decimal to Binary
Compute Bit Error Rate
Plot BER, TX, RX and Demodulated Data

Figure 5.1: Flowchart of procedure for working model

Carrier channel, Baseband and RF gains of transmitter and receiver are other parameters which are also initialized. For continuous transmission parameter has to be set as 1 and the transmitting antenna continues to transmit the samples until the antenna is manually disabled by the user, otherwise it is 0 in the case of single transmission. Parameters such as Manual gain control and automatic gain control can be set depending on the requirement. These all parameters are downloaded onto the WARP FPGA transmitter and receiver daughter cards. Input is now created which is a vector of samples or it can be a frame based matrix such that columns represent individual channels or frames and rows, number of bits in a particular channel or frame. This bit stream of input is divided into groups of bits depending on the value of M in M-ary modulation. If value of M is 4 then groups of two bits are formed which are then converted into decimal form so that integers can now be modulated by respective modulation technique. If this modulated data is a column vector then it has to be first converted into row vector and then this I/Q signal is downloaded on to the daughter card of WARP BOARD through Ethernet. The Radio 2 and Radio 3 are enabled as transmitter and receiver. Also Transmitter buffer is enabled so that transmission of signals can take place which are stored in this buffer and receiver buffer is enabled too for storing the received samples. For transmission to takes place the Radio 2 must receive the SYNC pulse and similarly reception takes place only when SYNC pulse is received by the Radio 3. It shows that synchronization is very essential so that samples are transmitted and received at the desired time and so is the reason of a Real time system. When SYNC is received Radio 3, reception of signal data and its RSSI values occur. The received data is now decimated to bring the frequency same as that of the original modulated signal. The signals are still having decimal values which are converted into binary groups. These groups are converted into a single stream of bits which is demodulated to get the original bit stream. The bits which are sent initially are compared with the bits received after demodulation and mismatch is calculated between these bit streams. This mismatch is divided by total number of bits to yield the bit error rate. This procedure is repeated for different modulation techniques such as M-PSK, M-QAM, DPSK. The demodulated signals are also compared for each of modulation techniques and finally these compared parameters are plotted.

CHAPTER 6

RESULTS AND DISCUSSIONS

Various modulation techniques have been employed in simulating the design using WARP FPGA board. The hardware used is responsible for real time analysis of different modulation techniques under natural environment. In the just simulation scenario when the hardware is not used, actual behaviour of signals can't be determined, however introducing the parameters manually in the simulation objective can bring out the results which might be close to that of the results obtained in real time conditions. WARP FPGA is virtex-4 hardware on which real time implementation of various designs are possible such as designs using system generator, Power PC and programming through languages such as VHDL and MATLAB. However the results shown are through the source code running in the MATLAB. The code comprises of a number of standard functions responsible for the correct operation of a few modules of WARP board which are responsible for desired and effective functioning of intermediate nodes used for the signal processing. Daughter cards work on the basis of these functions such as the socket and node initialization, radio boards association, initialization of global parameter from WARP lab, enabling and disabling of transmitter and receiver radio boards and their associated antennas etc. The variable parameter in the design code is transmitting signal base band gain which is varied over each iteration to study the performance of modulation techniques in lieu of bit error rate. The modulation techniques used are M-PSK, M-QAM and DPSK. The results obtained for these techniques consist of transmitting row vector with both In phase and Quadrature phase waveforms, also received signal with In phase and Quadrature phase components are also shown. Besides this demodulated signal for each technique is also plotted in the result and finally bit error rate performance with respect to different values of base band gain is shown.

WARP board has transmitter radio board with a variation of three values of transmitter base band gain i.e. from 1 to 3. So for each value of this gain bit error rate is calculated and it will be seen below that which modulation technique has the best performance. It is also shown how the performance of modulation techniques varies with the order of modulation. Also the usage of number of bits per symbol affects the capacity and interference of these techniques. Comparison has been made between the simulation of the modulation techniques with and without WARP

FPGA board. Different cases have been taken one by one and then analysis is done on the results.

Case 1: BPSK (Binary Phase Shift Keying)

In BPSK the phase of signal is varied to Transmit information. The carrier phase is varied according to the bit i.e. the carrier gets out of phase as the bit changes. The figure 6.1 shows the performance of BPSK modulation technique under non ideal conditions.

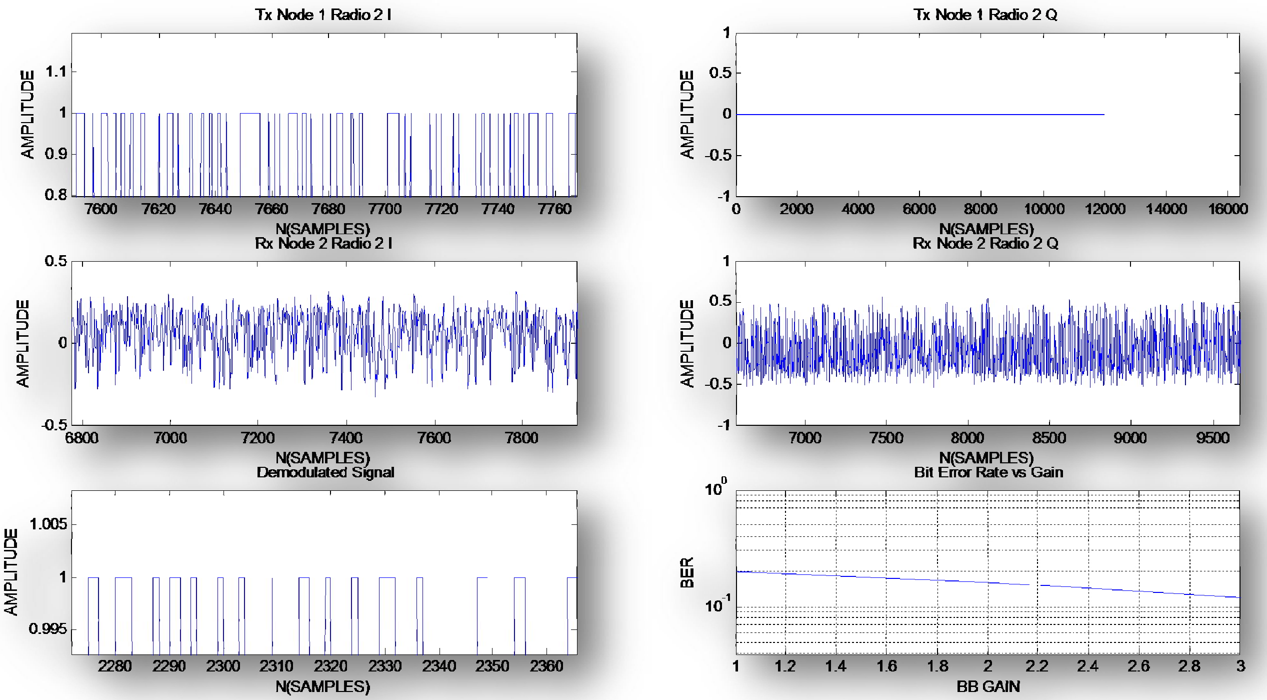

Figure 6.1: Performance of BPSK modulation

In BPSK modulation the modulated signal has two values -1 and +1 which correspond to two phases that are out of phase by 180^0. There are no imaginary components in BPDK modulation and due to this reason only the transmitted signal has no quadrature component which can be seen in the above figure. Further it is the best modulation since the bit error rate is least in this case due to large spacing between the symbols. However this modulation technique is unsuitable for high data rate applications where quite large bandwidth is needed and it is due to the fact that it is able to modulate only 1bit/symbol.

Case 2: QPSK (Quadrature Phase Shift Keying)

In this case phase of the carrier is varied according to the bit level but two phases constitute one symbol. In all there are four phases on the constellation diagram. Each phase has its In phase and Quadrature phase component associated with it. The figure 6.2 shows the performance of QPSK under practical conditions.

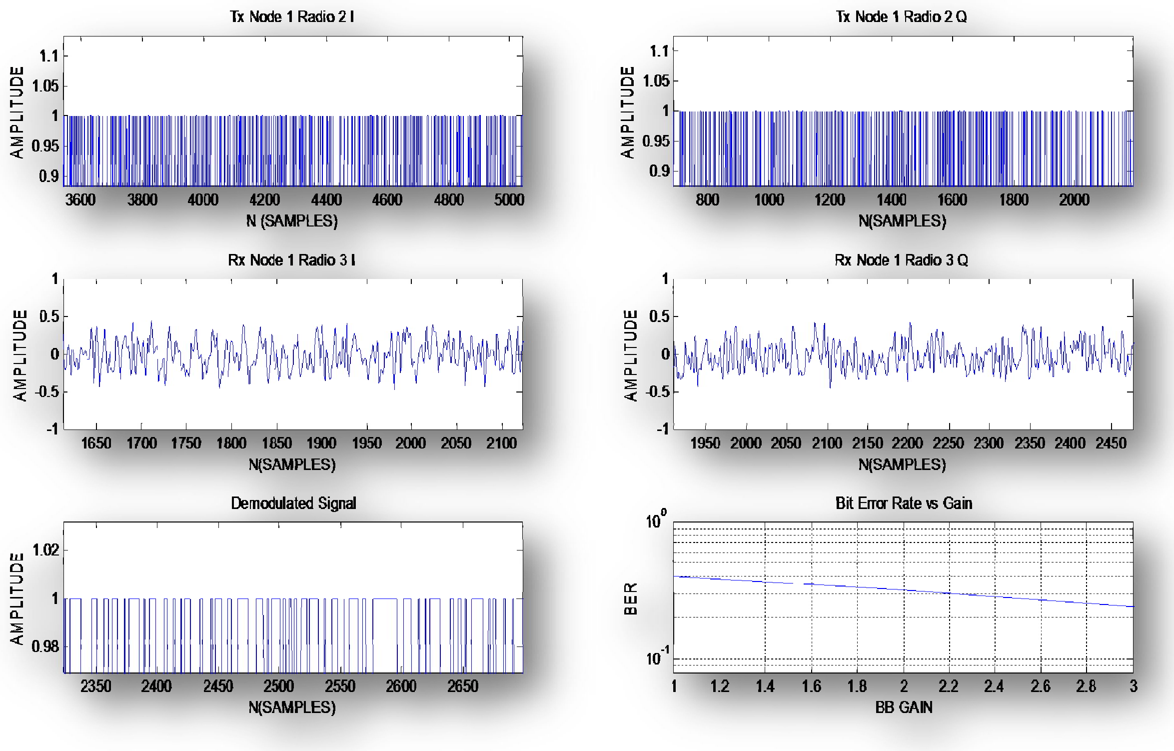

Figure 6.2: Performance of QPSK modulation

In the above figure transmission, reception, demodulation and bit error rate for QPSK modulation is shown. The transmission signal length is 6000 i.e. it contains symbols and each symbol constitutes of two bits. However the number of input bits is 12000. Transmission delay is kept to be 0 so as to avoid any mismatch between input and output symbols. The transmission gain of base band signal is varied through iterations and the number of iterations looped is 3. The RF gain of transmitter is 40. The baseband and RF gain of receiver are 13 and 1. Since only single transmission is required i.e. Transmission mode is set to 0. Manual gain control is required in some applications, so if gain has to be altered manually the parameter must be selected and set to 0. It can be seen from the figure that the transmitted signal is composed of bits in the form of 1 and -1 with imaginary components also which can be seen. The received signal is somewhat seems to be distorted due to presence of noise and may be due to multipath effect. However it is decoded easily and the samples can be seen in the demodulated signal figure. The bit error rate figure is showing that the inter symbol interference in case of QPSK is slightly larger than BPSK.

Case 3: 8 PSK (8 Phase Shift Keying)

8 PSK modulation has $log_2 8$ number of bits in one symbol i.e. 3 bits per symbol. The total number of phases in 8 PSK is eight which are organized in some fashion on the constellation diagram. The symbols are gray coded which organizes these symbols in such a way that there is only one bit difference between the two consecutive symbols. The signals which are transmitted contain the symbols which are quite more compactly spaced as compared to QPSK scheme. The figure 6.3 shows details of performance of 8 PSK.

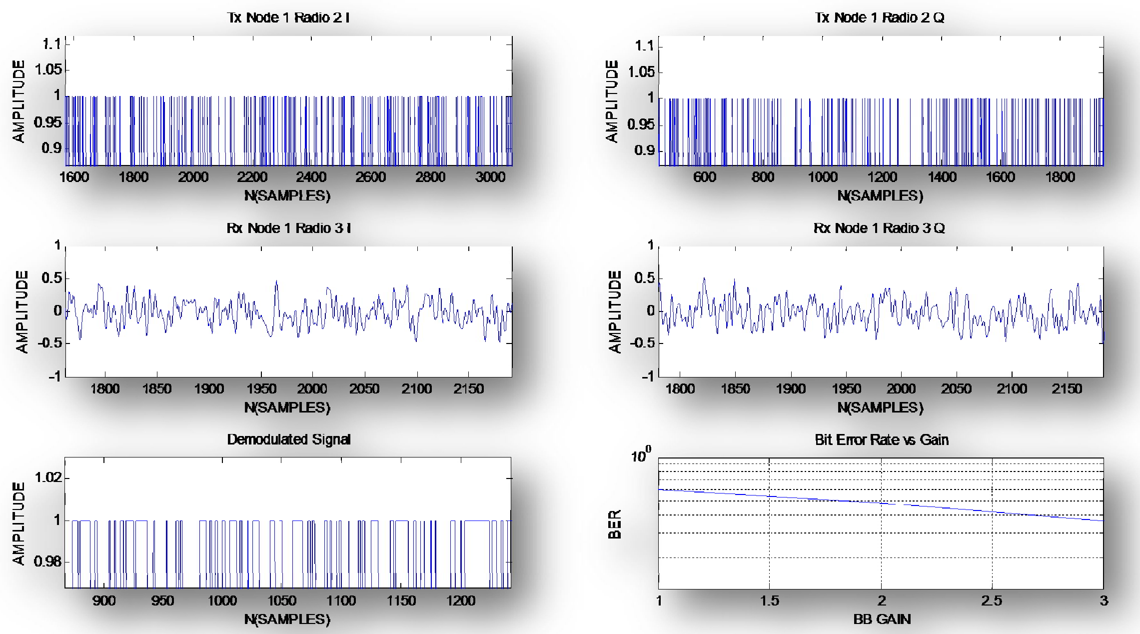

Figure 6.3: Performance of 8 PSK modulation

It can be seen from the figure that the total number of symbols transmitted from the antenna is 4000. The symbols are close to each other and thus can cause inter symbol interference due to which the performance is decreased slightly as far as bit error rate is concerned, however the capacity approaching feature can be seen in this technique. Therefore this modulation is used where erroneous detection can be considered to some extent while capacity is more important constraint. In phase and Quadrature phase waveforms are shown for the received signal. The demodulated signal now consists of 12000 bits. All the transmission parameters are kept same and from the last figure, it can be seen that more error is introduced in 8 PSK due to compactness.

Case 4: 16 PSK (16 Phase Shift Keying)

The modulation technique has $log_2 16$ bits per symbol making it a good choice for high capacity wireless applications. However the performance is degraded if sufficiently large numbers of samples are not used. Before its transmission through the antenna, the transmission buffer is enabled so that samples are stored in the transmission buffer.

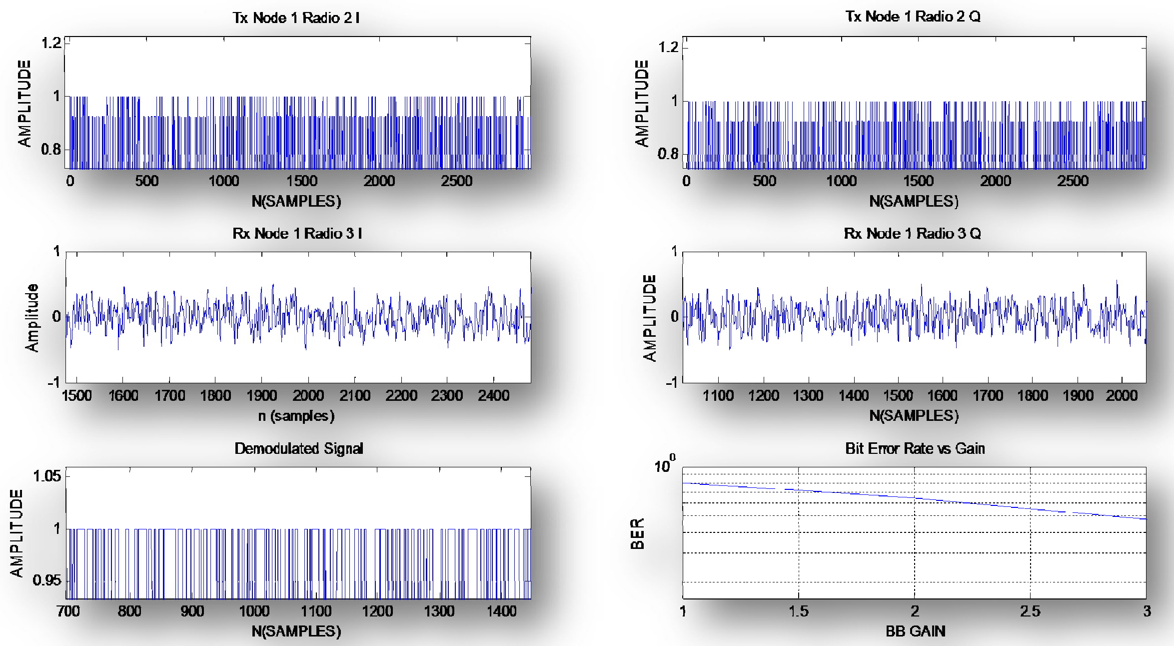

Figure 6.4: Performance of 16 PSK

However the buffer is disabled once the transmission occurs. The transmission vector consists of 3000 symbols having 4 bits in each symbol. The figure 6.4 shows the performance of this technique. It can be seen from the figure that bit error rate is increased due to presence of four bits in a one symbol. The transmitted signal has the symbols with values varying between 0 and 1. It can be concluded from the figure that bit error rate approaches the maximum value with the variation of transmitter gain.

Case 5: 32 PSK

This modulation technique employs $log_2 32$ bits in one symbol. The input bit stream is divided into five sub streams and the consecutive bits are mapped on to the symbol from each bit stream. The capacity is highest in this case but error rate is also maximum, so the technique is not widely used. The figure 6.5 shows the performance of 32 PSK modulations.

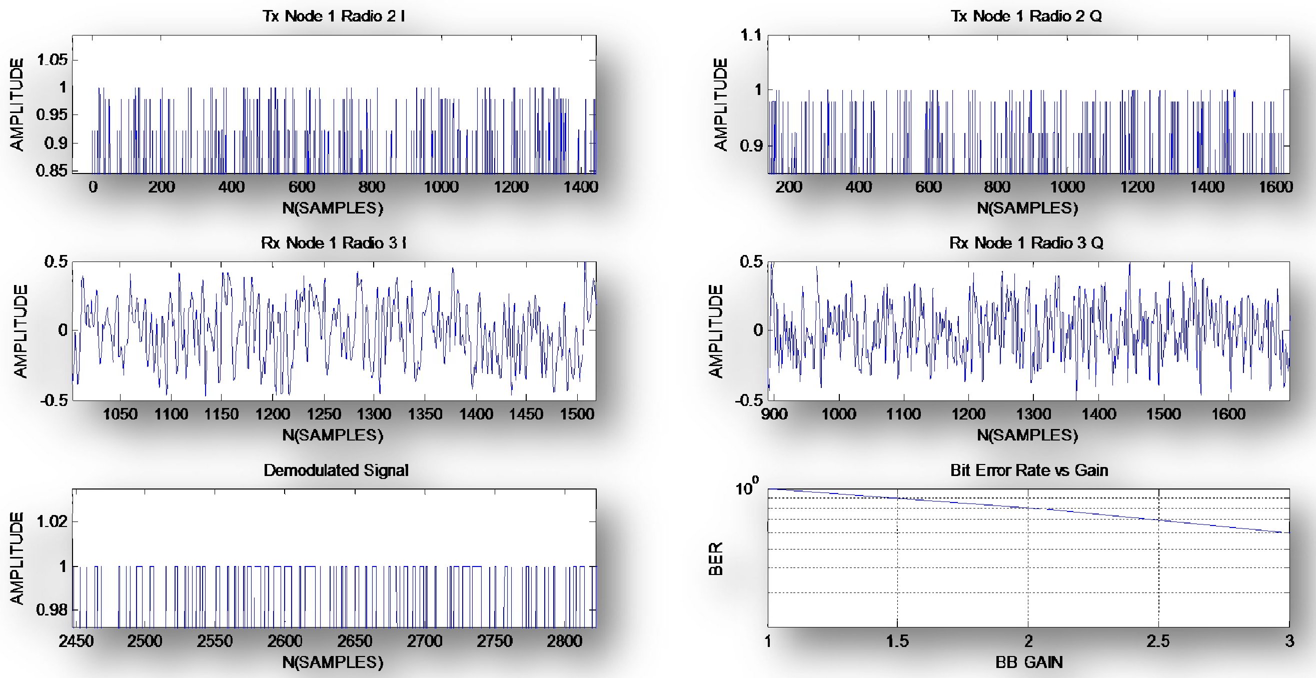

Figure 6.5: Performance of 32 PSK

The bit error rate is calculated by dividing the total number of mismatches by total number of bits. Further the modulated signal which is received at the receiving side is the high frequency version of the basic I/Q signal which is downloaded onto the radio board. Also the reception of this modulated signal takes place only when the radio card receives the SYNC pulse from the global clock provided for both transmitter as well as receiver daughter cards.

Case 6: QAM (Quadrature Amplitude Modulation)

QAM modulation technique is a hybrid technique for modulating digital signals. The input bit vector of length 12000 is partitioned into two bit streams which are phase modulated and corresponding phases of both streams are mapped into a single stream. The mapping of two phases results in the formation of a symbol which is then amplitude modulated by a carrier. The resulting signal is then interpolated and transmitted which is one of the parts shown in the figure 6.6

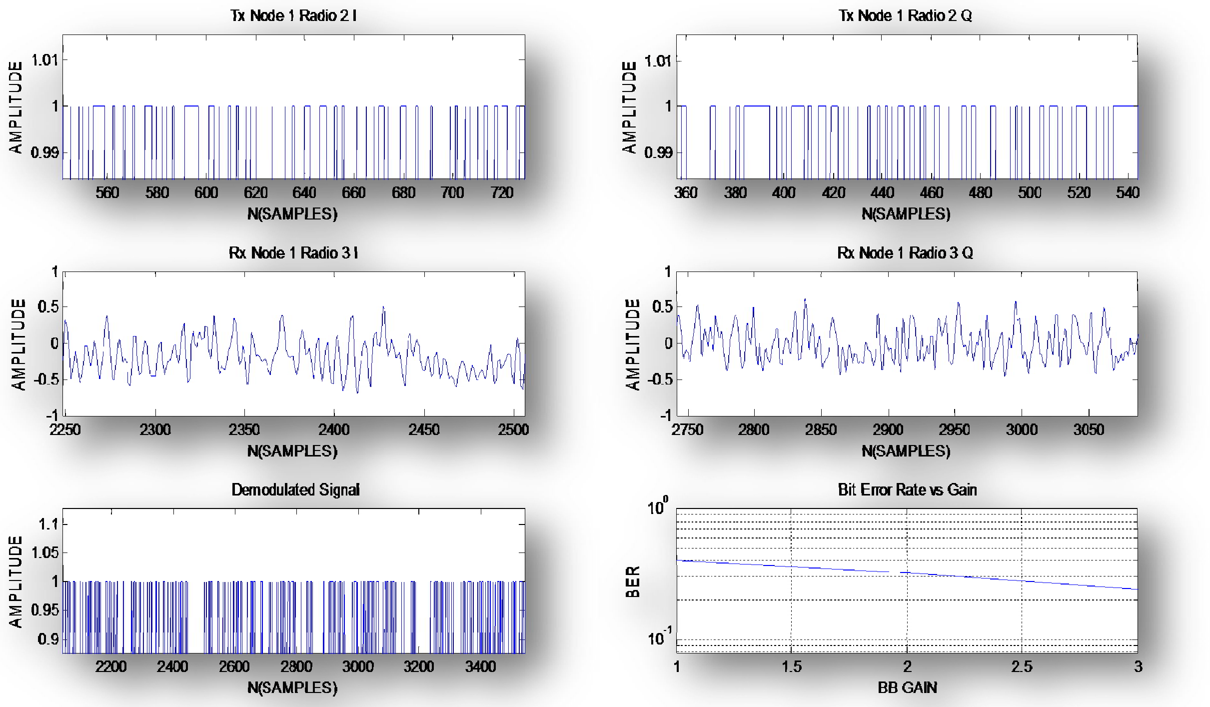

Figure 6.6: Performance of QAM modulation technique

It can be seen from the figure that bit error rate is slightly better than the higher order PSK. Also QAM appears to increase the efficiency of transmission by utilizing both amplitude and phase variations.

Case 7: 8 QAM

In 8 QAM modulation technique three bits exist in one symbol. The technique has almost the same performance as that of 8 PSK but due to hybrid modulation it also shows some better efficiency. As the order of modulation increases the demodulated signal also becomes quite disrupted which can be seen in the figure 6.7 . There is a usage of Linear Amplifiers in case of QAM since amplitude variation occurs and it has to be maintained in linear form while in PSK such amplifiers are employed due to the absence of amplitude components.

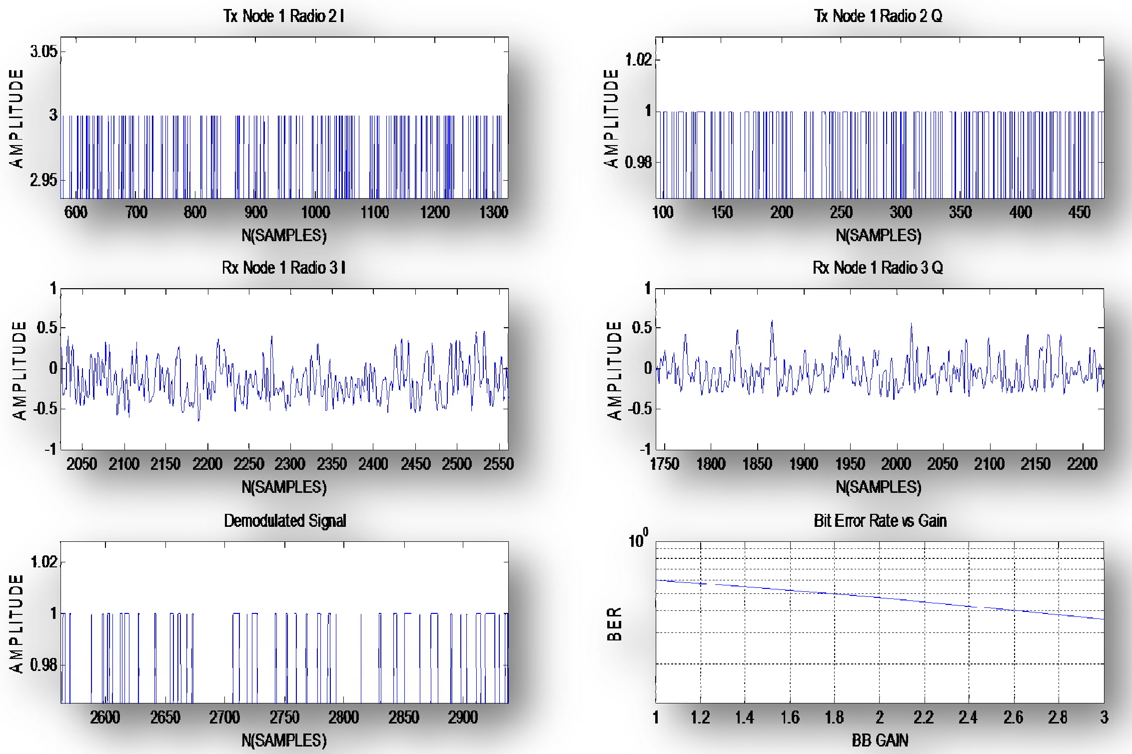

Figure 6.7: Performance of 8 QAM

Case 8: 16 QAM

Error rate in this case is increased further due to presence of 16 symbols and each symbol has four bits associated with them. Due to this the constellation becomes compact and probability of interference between two consecutive symbols also increases as shown in the figure.

However on the WARP platform the signal is transmitted through the antenna associated with the transmission radio board with 3000 symbols having four bits each in the form of integers. Further binary transmission can also be done but this is efficient in the case of BPSK since the main aim of higher order modulation is to increase the capacity of the system. The Figure 6.8 shown below represents the complex transmitted I and Q waveforms and the demodulated signal. Also bit error rate performance of 16 QAM is almost analogous to that of its PSK counterpart but the transmission efficiency is better due to presence of amplitude components

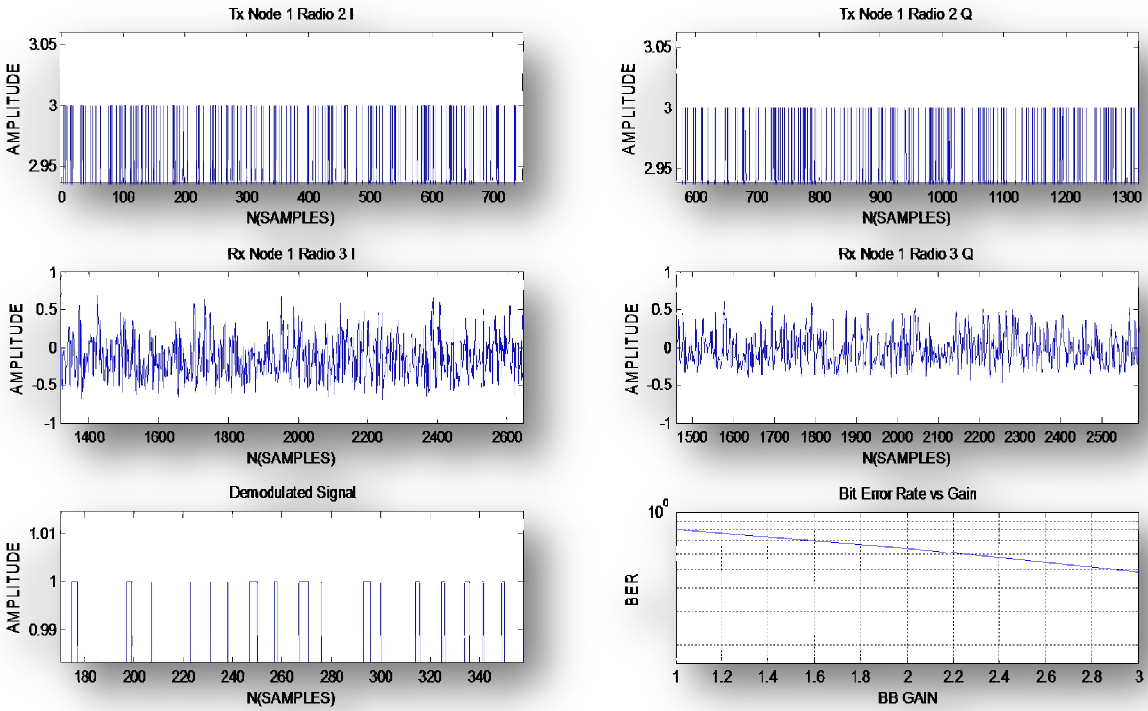

Figure 6.8: Performance of 16-QAM

Case 9: 32 QAM

This modulation technique employs $log_2 32$ bits in one symbol. It is modulation technique having largest capacity among all which are discussed. However error probability is quite high but its transmission efficiency is also high due to presence of amplitude components.

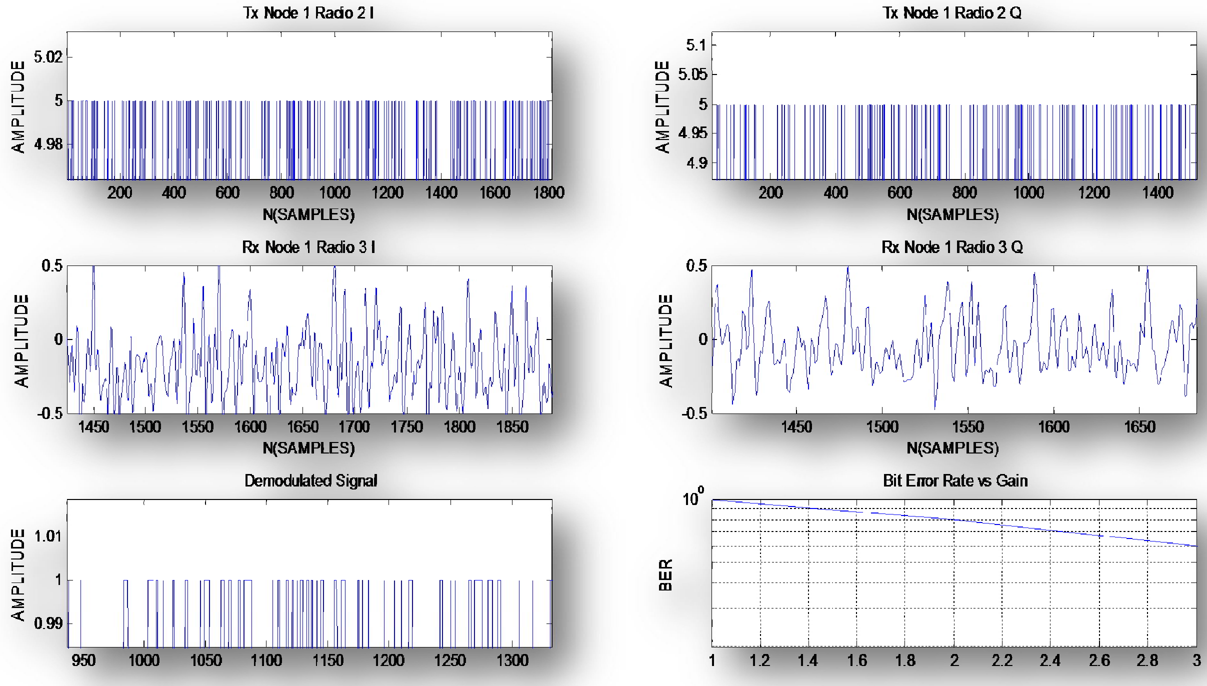

Figure 6.9: Performance of 32 QAM

The transmitted signal is shown in the figure 6.9 which comprises of 32 symbols due to which symbols are very close to each other and hence gray coding is employed.

Case 10: 4 DPSK

Differential phase shift keying uses the two phases of carrier which are 180^0 out of phase. The input bit stream is modulated by these two carriers in such a way that one and a half cycle occurs in a single bit and the phase changes as with the bit state reversal. The figure 6.10 below shows the transmitted signal contains four symbols and each symbol is having two bits with one and a half cycle each.

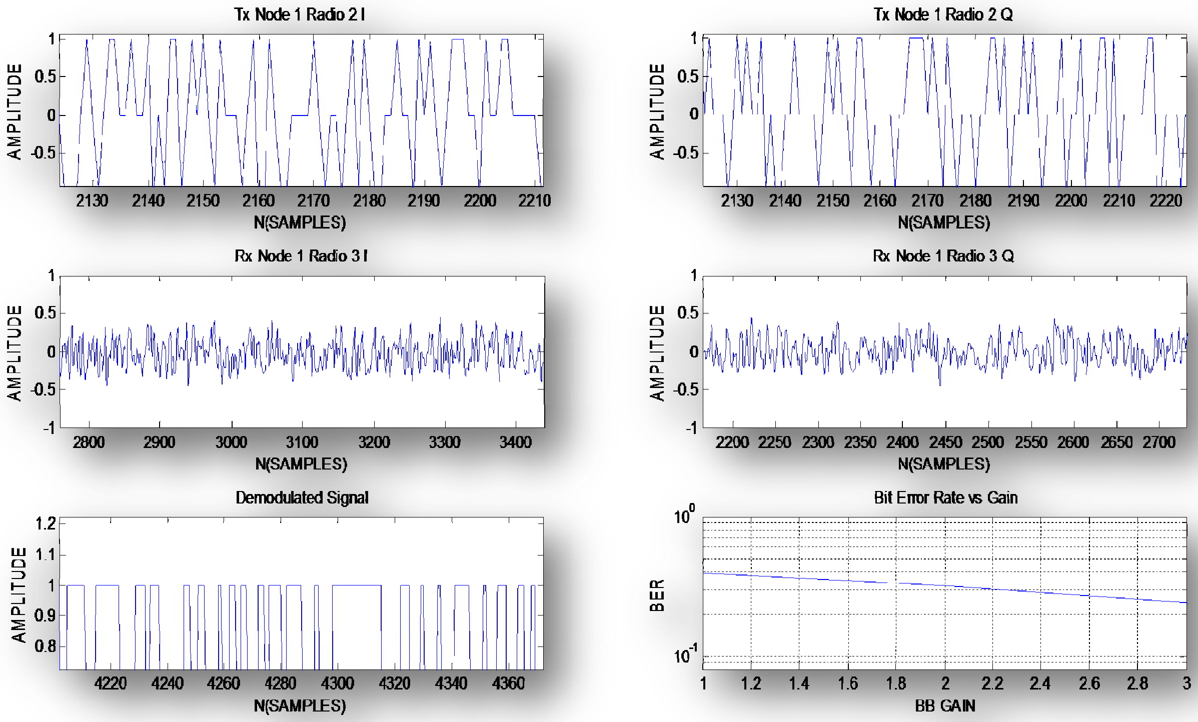

Figure 6.10: Performance of 4 DPSK

In normal PSK technique when the phases are mapped on to the symbols, phase ambiguities occur at the boundaries of bit transition. However using DPSK ambiguities are reduced to much extent. Further demodulation process of DPSK results in slightly better performance due to removal of ambiguities. Further bit error rate under real time conditions is shown which is almost same as that of its PSK counterpart.

Case 11: 8 DPSK

The performance of 8 DPSK modulation technique has been shown in which transmitted signal has the form of ‘W’ AND ‘M’ as shown in figure 6.11. The number of symbols transmitted is 4000. It is so because of phases are used for modulating the information bits. Further presence of more than one phase per bit widens the shape of the modulated signal.

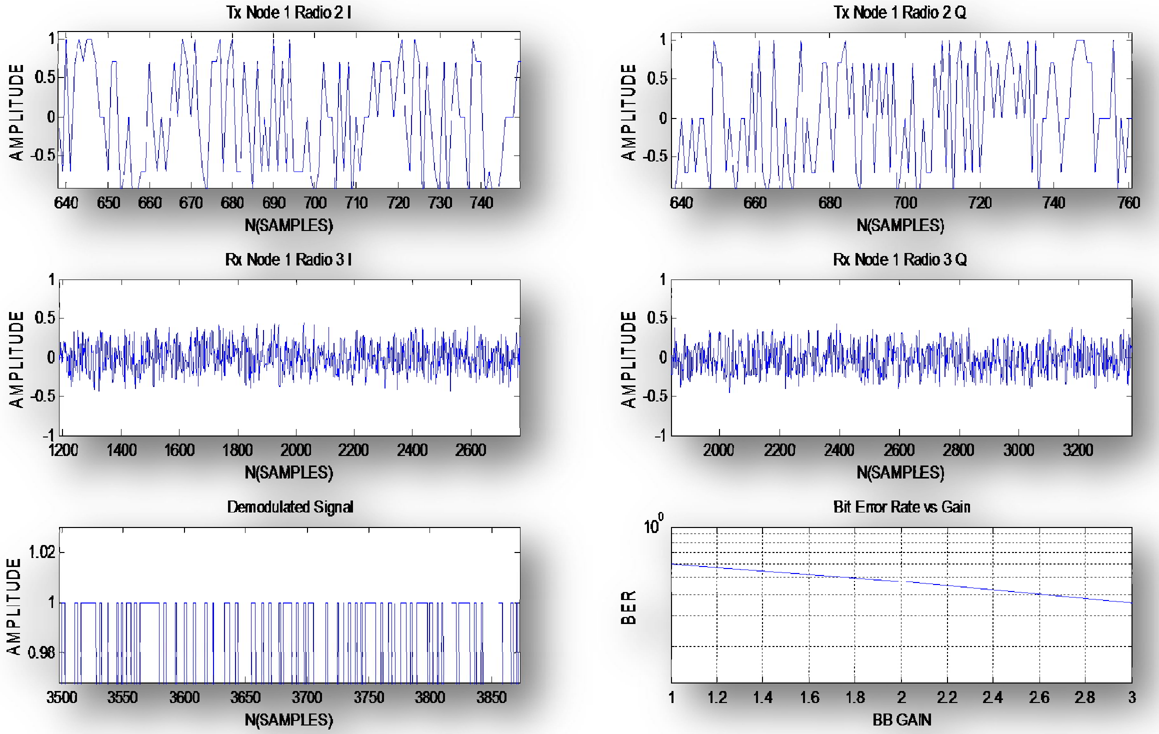

Figure 6.11: Performance of 8 DPSK

The natural transmission and reception conditions make the bit error rate somewhat high but it decreases with the value of base band gain. The demodulated signal is a continuous stream of bits which were originally sent as source but with certain deformations and errors.

The bit error rate and more improved demodulation can be achieved with the help of error correction codes. The error correction codes popularly known today are LDPC codes which can approach Shannon's capacity and are able to give destination, the correct information through their iterative decoding behaviour.

CONCLUSION

In this report comparison between various modulation techniques has been done. The data involves simply modulated data and coded data involves introduction of error correction codes in the information bits. The form of data is implemented in real time on the WARP FPGA Board. It has been concluded that by introducing BPSK, BER is least which is made possible due to presence of a single bit in one symbol. Only two phases are there in BPSK modulation making it most efficient modulation in terms of error; however the data rate provided by BPSK is least making it unsuitable for high data rate application such as satellite communication. Using considerably a higher order modulation, capacity keeps on increasing but at the cost of increased inter symbol interference. QAM is a hybrid modulation technique i.e. firstly phase modulation of the digital input is done and then the analog waveform which is obtained by mapping the symbols is amplitude modulated by a high frequency carrier making it suitable for considerably high data rate as well as reasonable low bit error rate. DPSK uses one and a half cycle of carrier wave in the single information bit. DPSK is simpler to implement than ordinary PSK since there is no need for the demodulator to have a copy of the reference signal to determine the exact phase of the received signal, however the probability of erroneous demodulation is greater in DPSK. Further the demodulated signal also varies in respect of accuracy as the modulation order increases. In BPSK technique the demodulation results in most accurate output and it gets maximum distortion in case of 32 PSK. WARP FPGA makes it possible to realize the various modulation techniques in real time so that practical performance can be achieved.

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