Design of CMOS Low Drop-out Regulator with Improved PSRR

A dissertation submitted in partial fulfillment of the requirement for the award of degree of

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Submitted by

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DECLARATION

I hereby declare that the work which is being presented in the dissertation entitled, **" Design of CMOS Low Drop-out Regulator with improved PSRR"** in partial fulfillment of the requirement for the award of degree of Master of Engineering in VLSI Design submitted in Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Dr. Rishikesh Pandey, Assistant Professor, ECED and refers other researcher's work which are duly listed in the reference section.

The matter presented in this dissertation has not been submitted in any other University/Institute for the award of degree.

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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ABSTRACT

The advancement in battery operated portable devices, noise sensitive devices and other devices, which need high precision supply voltages has fuelled the growth of Low Drop-Out Regulators. Low Drop-Out Regulators showed advantage over its counterpart. The design of Low Drop-Out Regulators with high performance is challenging problem now-a-days. The increasing demand, however, is especially apparent in mobile battery operated products, such as cellular phones, pagers, camera recorders and laptops.

In this dissertation, A CMOS Low Drop-out Regulator with Improved PSRR is proposed. The proposed circuit is developed using error amplifier, subtractor circuit and PMOS as pass device. For the improvement of dc PSRR, a subtractor circuit is introduced along with two stage error amplifier with NMOS mirror load in conventional low drop-out regulator topology. The proposed circuit is simulated using TSMC 0.18μm CMOS technology process parameters and the simulation results are presented. The layout of the compensated error amplifier is designed using Cadence Virtuoso XL Design Environment tool. The performance parameters of the proposed LDO has also been compared with the existing LDO circuits available in literature and the comparison shows that the proposed LDO has wider range of PSRR with better dc PSRR.

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LIST OF SYMBOLS

g_m	Transconductance
I	Current
V	Voltage
R	Resistance
V_{DO}	Drop-out Voltage
W	Channel Width
L	Channel Length
V_T	Threshold Voltage
K	Transconductance Parameter
MN	NMOS Transistor
MP	PMOS Transistor
V_{ref}	Reference Voltage
C	Capacitance

ABBRIVEATIONS

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
LDO	Low Drop-Out Voltage Regulator
FVF	Flipped Voltage Follower
DFC	Damping Factor Control
UGF	Unity Gain Frequency
PLL	Phase Locked Loop
PSRR	Power Supply Rejection Ratio
VCO	Voltage Controlled Oscillator
CFA	Current Feedback Amplifier
PSRR BW	PSRR Bandwidth
ESR	Equivalent Series Resistance
SoC	System on a chip

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

Conditioning and supplying of power are the most elementary functions of an electrical system. Any loading application, be it a cellular phone, pager, or wireless sensor node, cannot sustain itself without energy, and cannot fully perform its functions without a stable supply. The fact is transformers, generators, batteries, and other off-line supplies incur substantial voltage and current variations across time and over a wide range of operating conditions. They are normally noisy and jittery not only because of their inherent nature but also because high-power switching circuits like central-processing units (CPUs) and digital signal-processing (DSP) circuits usually load it. These rapidly changing loads cause transient excursions in the supposedly noise-free supply, the end results of which are undesired voltage drops and frequency spurs where only a dc component should exist [1]. Use of switching power supply or DC to DC converter, provides portable applications, which makes those systems to operate in noisy environments. Mostly electronics systems are very sensitive to noise present on power supply. Consequently, they need large battery filters to reduce the ripple on battery voltage [2]. The explosive proliferation of battery-powered equipment in the past decade has accelerated the development and use of Low-Dropout voltage regulators for noise sensitive circuits [2, 3]. Low drop-out regulators is driven by the growing demand for higher performance power supply circuits [4]. The low drop-out nature of the regulator makes it appropriate for use in many applications, namely, automotive, portable and biomedical applications. The increasing demand, however, is especially apparent in mobile battery operated products, such as cellular phones, pagers, camera recorders, and laptops. In a

cellular phone, for instance, switching regulators are used to boost up the voltage but LDO's are cascaded in series to suppress the inherent noise associated with switchers. LDO's benefit from working with low input voltages because power consumption is minimized accordingly, $P = I_{Load} * V_{in}$. Low voltage and low quiescent current are intrinsic circuit characteristics for increased battery efficiency and longevity. Low voltage operation is also a consequence of process technology. This is because isolation barriers decrease as the component densities per unit area increase, thereby exhibiting lower breakdown voltages. Therefore, low power and finer lithography require regulators to operate at low voltages, produce precise output voltages, and have characteristically lower quiescent current flow [5]. The thrust is towards reducing the number of battery cells, required to decrease cost and size, while maintaining power supply rejections and other specification of regulators [6].

1.2 MOTIVATION

The Low drop-out regulators are appropriate for many circuit applications such as mobile, laptop and other handheld devices. There are some alternatives of LDOs also present in the market. The alternatives of low drop-out regulators are dc-to-dc converters, switching regulators, etc. Switching regulators are mixed-mode circuits feedback an analog error signal and digitally controlled gate to provide bursts of current to the output. These circuits are inherently more complex and costly than LDOs realizations. Switching regulators can provide a wide range of output voltages including values that are lower or greater than the input voltage depending on the circuit configurations (buck or boost), but LDOs provide output voltages lower than the input voltage. In many applications, Switching regulators and LDOs are connected in series to utilize the improved performance characteristics of LDOs. Power management circuits are very sensitive to noise. Therefore, these circuits should be less affected by noise. To make circuits less affected by power supply ripple should have high power supply rejection ratio (PSRR) over a wide range of frequency.

1.3 KEY CONTRIBUTIONS

The work in this dissertation can be summarized as follows.

1. Design and simulate a compensated error amplifier for wide range of PSRR bandwidth.
2. Design and simulate a CMOS low drop-out regulator with improved PSRR.

In this dissertation, a CMOS low drop-out regulator with improved PSRR has been proposed. The proposed circuit can be used in may applications such as PLLs/VCOs, audio devices, etc. The low drop-out regulator proposed in this dissertation has been simulated using TSMC 0.18μm CMOS technology process parameters and the simulation results are presented. The performance parameters of the circuit has also been compared with the existing LDO circuits available in literature and the comparison shows that the proposed LDO has wider range of PSRR with better dc PSRR.

1.4 ORGANIZATION OF THE THESIS

The organization of thesis is as follows:

CHAPTER 1: This chapter discusses the motivation, key contributions and the organization of the thesis.

CHAPTER 2: It contains the description of low drop-out regulator (LDO) block diagram in detail along with its various specifications.

CHAPTER 3: In this chapter, the various literature reviews based on different topologies of low drop-out regulators such as on-chip and off-chip capacitor LDOs are discussed. This chapter also deals with stability issues in design of LDOs and available compensation techniques.

CHAPTER 4: This chapter discusses the proposed low drop-out regulator and its design specifications in detail.

CHAPTER 5: In this chapter, the simulation results of proposed low drop-out regulator and layout of compensated error amplifier have been discussed.

CHAPTER 6: This chapter summarizes the dissertation and suggests future scope of the work.

CHAPTER 2

LOW DROP-OUT REGULATOR

2.1 INTRODUCTION

The low drop-out regulators are the essential building block of portable electronic devices. LDOs basically composed of error amplifier, pass device and feedback network. The chapter is organized as follows. The block diagram and operation of LDOs are discussed in section 2.2. The performance specifications of LDOs such as drop-out voltage, load regulation and power supply rejection ratio (PSRR) are discussed in section 2.2.

2.2 LOW DROP-OUT REGULATOR:

A series low-drop-out regulator provides a specified and stable dc voltage, whose input to output voltage difference is low. The drop-out voltage is defined as the value of the input/output differential voltage where the LDO stops regulating. Power transistor (pass device) is connected in series between the input and the output terminals of the regulator that's why it termed as series voltage regulator. The operation of the circuit is based on feeding back an amplified error signal to the power transistor. The output current flow of the power transistor is key parameter which is actually responsible for driving the load. This type of regulator has two inherent characteristics: (1) the magnitude of the input voltage is greater than the respective output and (2) the output impedance is low to obtain good performance. Low drop-out (LDO) regulators can be divided as either low power or high power. Low power LDOs are typically those with a maximum output current of less than 1 A, exhibited by most portable applications. On the other hand, high power LDOs can yield currents that

are equal to or greater than 1 A to the output, which are mainly demanded by many automotive and industrial applications [1, 6].

Figure 2.1 shows the basic low drop-out regulator. The circuit contains four basic components: a voltage reference, a pass element, an error amplifier, and a feedback network.

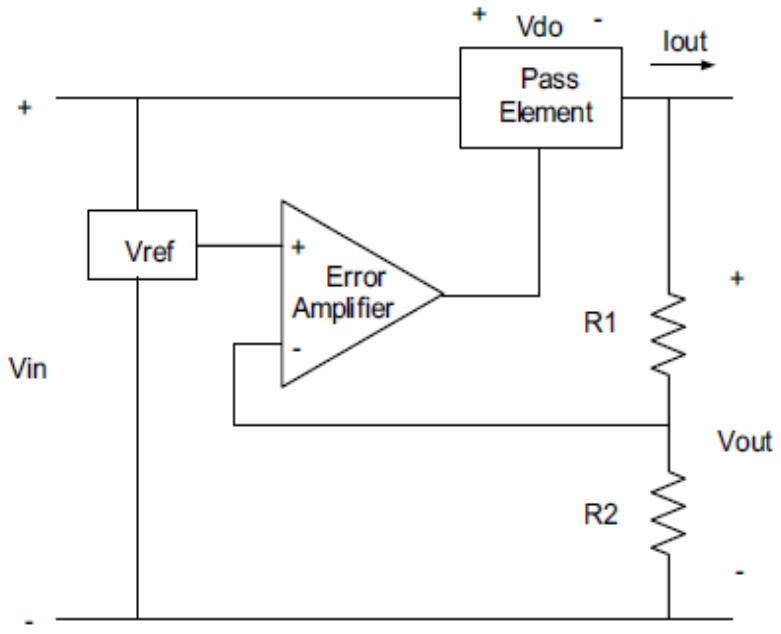

Figure 2.1: Basic low drop-out regulator [7].

The Voltage Reference provides a precise output voltage for the operation of the regulator [6]. The pass element governs the value of load current. The error amplifier is used to sense the some part of output voltage, compare it against the reference voltage to adjust the output voltage level. The feedback network, whose function is to scale V_{out} to a value suitable for comparison against reference voltage (V_{ref}) by the error amplifier.

2.2.1 VOLTAGE REFERENCE

The voltage reference is starting point of all regulators which is responsible for the output voltage of the regulator. This is usually of the bandgap-type, since this kind of reference has the ability to work down to low supply voltages, and provides enough accuracy and thermal stability to meet the less-stringent performance requirements of regulators [8].

2.2.2 PASS ELEMENTS

The Pass Element provides the output current required for driving the load, under the control of the error amplifier. Several configurations of the pass element have been proposed, depending on the system specifications. LDOs can be classified depending on the basis of pass devices. Their different structures and characteristics offer various advantages and drawbacks. There are four types of pass devices as shown in Figure 2.2, including NPN and PNP bipolar transistors, Darlington circuits and PMOS transistors.

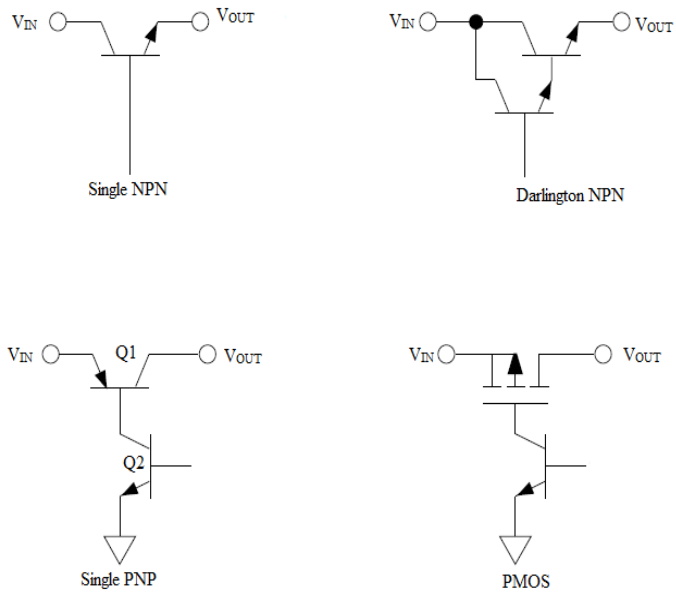

Figure 2.2 Examples of pass elements [9]

For a supply voltage, the bipolar pass devices can deliver the highest output current. A PNP is preferred over NPN, because the base of the PNP can be pulled to ground. The base of the NPN can only be pulled as high as the supply voltage, limiting the minimum voltage drop to one V_{BE}. Therefore, NPN and Darlington pass devices can not provide dropout voltages below 1 V. They can be valuable, however, where wide bandwidth and immunity to capacitive loading are necessary. PMOS and PNP transistors can be effectively saturated, minimizing the voltage loss and the power dissipated by the pass device, thus allowing low dropout, high-efficiency voltage regulators. PMOS pass devices can provide the lowest possible drop-out voltage. Therefore, the most widely used configurations include NMOS transistor and common source PMOS transistor. PMOS devices are typically the best overall

choice yielding a good compromise of dropout voltage, quiescent current flow, output current, PSRR and speed. The circuit design of an LDO is thoroughly affected by the physical requirements of the pass devices. The pass elements must be physically large to yield high output currents and low dropout voltage characteristics [9].

2.2.3 ERROR AMPLIFIER

The error amplifier produces an error signal whenever output voltage is differ from the reference voltage. The error output is used to control the amount of current the pass element flows into the load. The error amplifier seeks to set the value of V_{out} to a level where the error signal is as close as possible to zero [10].

A conventional error amplifier is shown in Figure 2.3. The transistors MN_1 and MN_2 form a differential pair and transistors MP_1 and MP_2 are used to form a current-mirror.

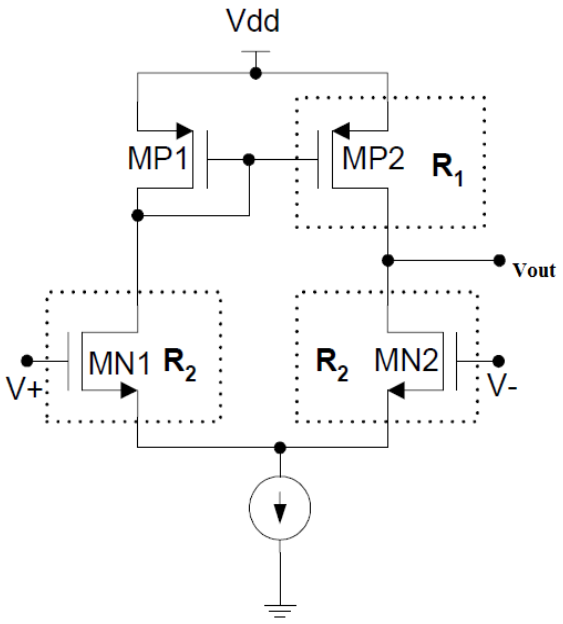

Figure 2.3 Conventional error amplifier with PMOS mirror load [10].

The output voltage is expressed as

$$V_{out} = V_{dd} \tag{2.6}$$

In this error amplifier topology, the entire supply ripple is transferred to the output over a wide frequency range with assumption that g_m is very large.

2.2.4 FEEDBACK NETWORK

The feedback network produces the output voltage to be compared with the voltage reference. This voltage is produced by a voltage divider is given as

$$V_{out} = V_{ref}\left(1 + \frac{R_1}{R_2}\right) \tag{2.7}$$

Feedback network can be designed using passive elements (resistors) or active elements (transistors) [7].

2.3 SPECIFICATIONS OF LDOs

The important aspects of LDOs can be summarized into three categories, namely, regulating performance, quiescent current flow, and operating voltages. Some of the specifications that serve as metrics for the LDO include drop-out voltage, line regulation, load regulation, output capacitor and ESR range, quiescent current flow, maximum load-current and PSRR. The requirements of these performance characteristics generally contradict each other on the cost of necessary compromises. The priority of the performance parameters is defined according to the particular application. Drop-out voltage is the minimum input/output differential voltage where the circuit just ceases to regulate. This can be expressed in terms of switch "on" resistance (Ron),

$$V_{drop-out} = I_{Load} * R_{on} \tag{2.8}$$

The variation in output voltage arising from a certain change in input voltage is defined as line regulation. Similarly, load regulation is the change in output voltage for specific changes in load-current [1]. Load regulation is essentially the output resistance of the regulator (Ro-reg),

$$R_{o-reg} = \frac{\Delta V_{LDR}}{\Delta I_o} = \frac{R_{o\text{-}pass}}{1 + A_{ol} * \beta} \tag{2.9}$$

Where ΔV_{LDR} and ΔI_o are the output voltage and the load-current changes, $R_{o\text{-}pass}$ is the output resistance of the pass element, A_{ol} is the open-loop gain of the system, and β is the

feedback factor. Therefore, load regulation performance is improved as the dc open-loop gain is increased. The temperature dependence of the output voltage is a function of the temperature drift of the reference and that of the input offset voltage of the error amplifier.
The power supply rejection ratio (PSRR) is defined as product of the ratio of the change in supply voltage to the change in output voltage caused by change in the power supply and the open-loop gain [11]. Thus,

$$\text{PSRR} = \frac{\Delta V_{DD}}{\Delta V_{OUT}} A_V(s) \tag{2.10}$$

Low drop-out regulators use a feedback loop to maintain a constant output voltage. As with any feedback loop there is phase shift around the loop and the amount of phase shift determines loop stability of LDO. To have a stable loop the phase shift around the (open) loop must always be less than 180° (lagging) at the point where the loop has unity gain, or 0 dB. There is various compensation techniques which can provide stabile operation of LDO depending on topology used.

CHAPTER

3

LITERATURE REVIEW

3.1 INTRODUCTION

Low-dropout regulators (LDO) are widely used in electronic products due to their precision output voltage and less prone to noise. In designing of LDOs, stability is an important issue. In some topologies external capacitors are used for the stability of LDOs. These topologies are termed as low drop-out regulators with capacitors. Use of external capacitors provides a good stability on the cost of portability of device. The stability of LDOs can be achieved by some special compensation techniques and topologies without using external capacitors. LDOs without any requirement of external capacitors are termed as capacitor free low drop-out regulators. Main cause of instability in LDOs is due to pass devices. In CMOS low drop-out regulators, usually common-source PMOS pass elements are used, which have high output impedance. Due to high output impedance the output pole location will be changed with the variation in load and in turns low circuit stability. So, there is requirement of some compensation techniques to improve the stability of LDOs. The chapter is organized as follows. Section 3.2 discusses the various topologies and operations of LDOs available in the literature. The compensation techniques used in the designing of LDOs are discussed in the Section 3.3.

3.2 DIFFERENT TOPOLOGIES OF LOW DROP-OUT REGULATORS

In power management system, LDOs are special class of linear regulators. There are various topologies of low drop-out regulators reported in [12-26]. These topologies are broadly classified on the basis of requirement of external capacitors as LDOs with capacitor [12-18] and capacitor-free LDOs [19-26].

3.2.1 LOW DROP-OUT REGULATORS WITH CAPACITOR

The several authors have been reported low drop-out regulators with capacitor [12-18]. Leung *et al.* [12] proposed a low drop-out structure to reduce chip area. The structure utilizes damping-factor control frequency compensation scheme along with first-order high-pass feedback network. Due to virtue of this scheme, this structure provides high stability, load transient and fast line load transient responses.

Adaptive miller compensation (AMC) technique based LDO structure in [13] provides high stability, as well as fast line and load transient responses. This structure also provides good performance on PSRR at high frequency. However, there are some disadvantages with this structure. The gain-band width (GBW) of this LDO is directly proportional to trans-conductance of pass device, which depends on output current, so it is not suitable for large current design.

Oh *et al.* [14] presented an LDO with current feedback amplifiers (CFAs) as shown in Figure 3.1. The suggested LDO provides fast response and high slew rate with class-AB operation.

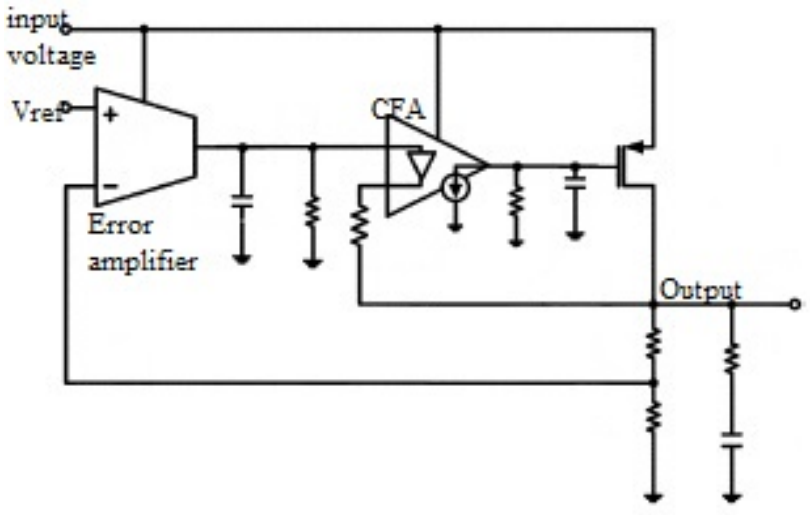

Figure 3.1 LDO structure using CFA based buffer amplifier [14].

CMOS LDO has major problem of high impedance feedback path which has been removed in the suggested structure. This structure utilizes a low ac impedance feedback path to achieve fast response while maintaining low quiescent power consumption. The low ac

impedance feedback path is constructed using a CFA based second-stage buffer. CFAs are popular to provide fast response with minimum slew-rate limiting. It uses global voltage mode feedback for steady state accuracy.

The LDO structure with an impedance attenuated buffer for driving the pass device has been suggested in [15]. In the structure, error amplifier has been realized by single-stage folded-cascode structure. This LDO structure is stabilized by using current-buffer (or cascode-Miller) frequency compensation, which is a pole-splitting compensation designed for splitting of two poles. The use of the current-buffer compensation scheme allows the amplifier to achieve wider unity-gain frequency, improved stability and enhanced PSRR.

Man *et al.* [16] presented a LDO structure using flipped voltage follower (FVF) cell. By using FVF in the structure, the output impedance is reduced which provides better stability than conventional LDO. The loop bandwidth at low load current is independent of the load current. It has wider bandwidth than the conventional LDO. The LDO structure based on CFA with inverting output buffer suggested in [17] is shown in Figure 3.2. Very low impedance at the inverting input of the CFA is the reason to achieve high regulation and fast transient response of this structure. The use of CFA in the circuit gives excellent performance in terms of bandwidth and slew rate.

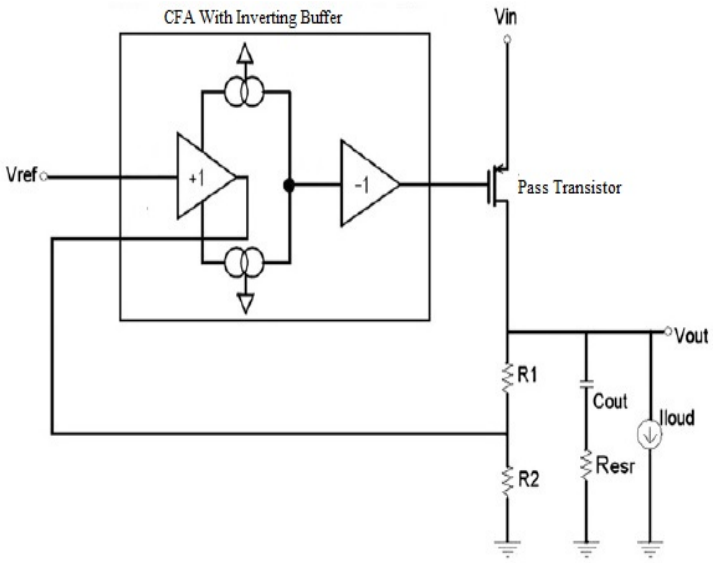

Figure 3.2 LDO architecture based on CFA with inverting output buffer [17].

Chava *et al.* [18] proposed a low drop-out voltage regulator with low equivalent series resistance (ESR) capacitive loads as shown in Figure 3.3.

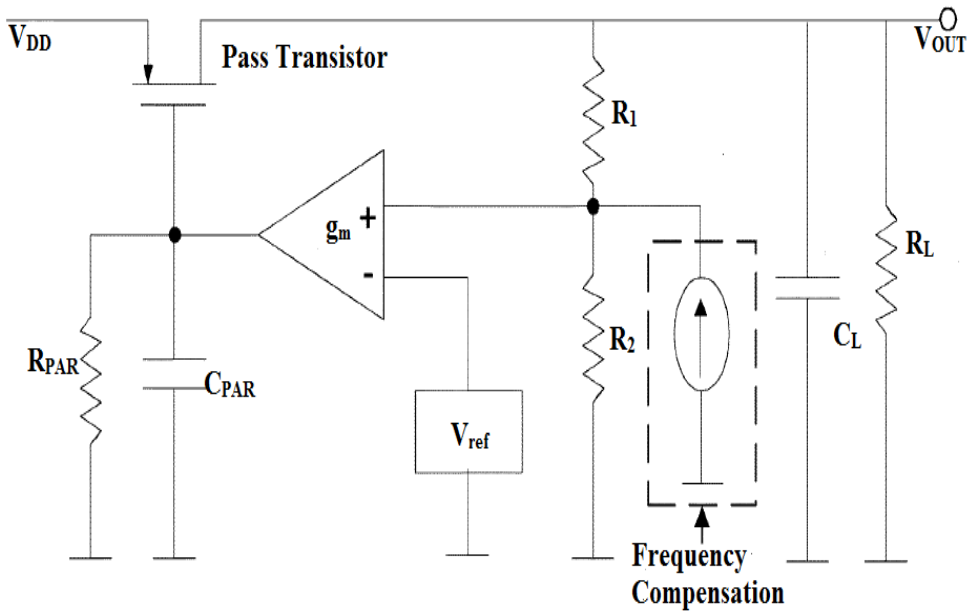

Figure 3.3 LDO with frequency compensation technique [18].

In this approach a zero is generated internally by using frequency compensation technique. Due to generation of internal zero there is less dependency on ESR for stability. In frequency compensation approach, this structure utilizes the concept of capacitive feedback. The capacitive feedback introduces a zero in left side of the s-plane. This introduced zero in the feedback loop is used to eliminate the requirement of ESR. It also minimizes the overshoot as it has less requirement of ESR. This structure does not consume significantly higher ground current or chip area compared to conventional low drop-out regulator. The authors have also suggested that the charge pump as voltage booster is an alternative of ESR. The charge pump voltage booster generates a voltage higher than supply voltage and the error amplifier utilizes that voltage for driving a pass device. This structure provides low output impedance, which in return provides stability. This structure has some disadvantage of requirement of additional circuitry.

Table 3.1 shows the comparison of various specifications of existing low drop-out regulators with capacitor.

Table 3.1 Comparison of different low drop-out regulators with capacitor available in literature

Parameters	Unit	[12]	[14]	[15]	[16]	[17]
Year		2003	2007	2007	2008	2012
CMOS Process	µm	0.6	0.25	0.35	0.35	0.35
Drop-out Voltage	mV	200	_	54	_	99.8
C_L	μF	10	0.05	1	1	1
ESR	ohm	1	0.1	N.A.	0.016	-
Ground Current(I_q)	mA	-	0.1	0.02	6	59-189
PSRR	dB	-60 at 10Hz	>43at 30kHz	_	_	>56 at (0 Hz-100 MHz)
Current Efficiency	%	_	99.8	99.8	-	99.8
Line Regulation	mV/V	_	_	2	18	13.5
Load Regulation	mV/mA	_	_	0.17	0.28	0.025
Area	mm^2	0.31	0.23	0.264	4.48	_

From Table 3.1, it is observed that without external capacitor stability can not be achieved. But, the use of capacitor increases the chip area.

3.2.2 CAPACITOR FREE LOW DROP-OUT REGULATORS

Capacitor free low drop-out regulators have several advantages over the low drop-out regulators with capacitance discussed in section 3.2.1 on the basis of small size and portability. Hazucha *et al.* [19] proposed a LDO structure, which uses replica-biased source follower for multi-supply voltage. This topology achieves fast response time and good figure of merit which accounts for the decoupling capacitance, output drop, current efficiency and current rating. The LDO structure with a capacitor-multiplier frequency compensation technique suggested in [20] is shown in Figure 3.4. This technique eliminates the cascode structure or buffer stage, due to which suggested LDO facilitates low voltage operation.

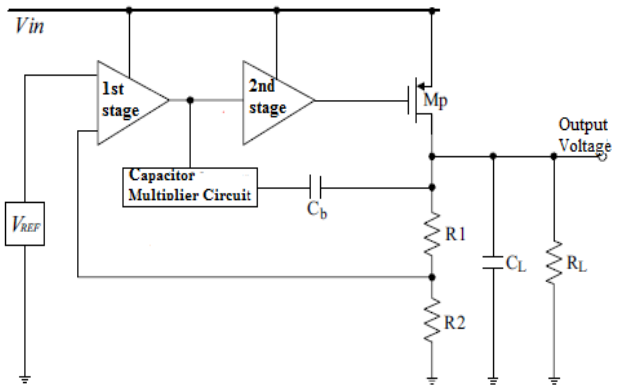

Figure 3.4 LDO with capacitor-multiplier frequency compensation [20].

Shiyang *et al.* [21] has been presented a LDO using Damping-factor-control (DFC) block along with miller compensation shown in Figure 3.5.

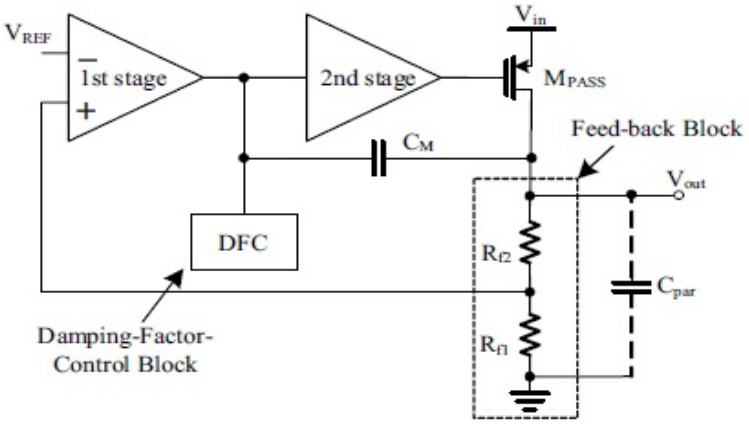

Figure 3.5 Structure of LDO with DFC block [21]

By using Miller compensation, a low frequency dominant pole, configured by DFC block is at higher frequencies than the unity gain frequency (UGF).

A capacitor free LDO structure with an input current differencing technique to achieve sleep-mode efficiency and area saving has been proposed in [22] as shown in Figure 3.6.

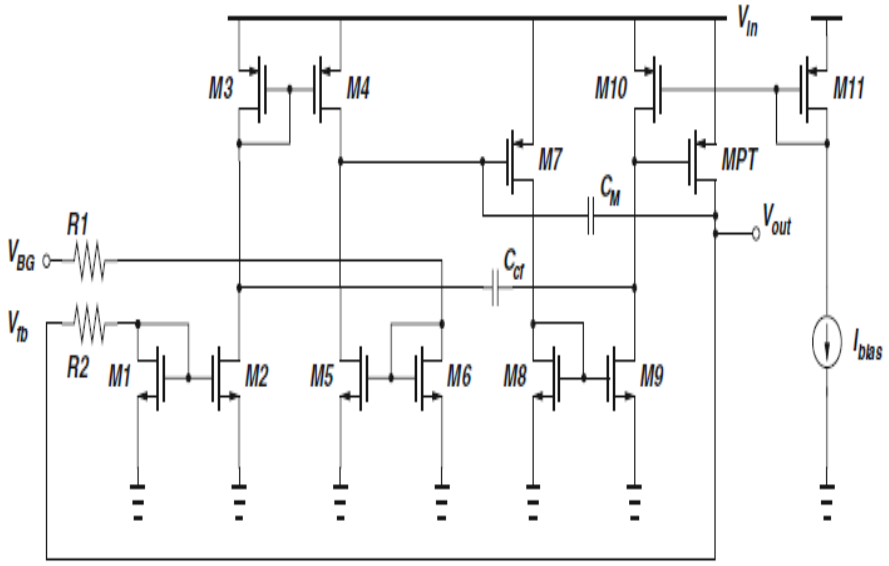

Figure 3.6 LDO schematic with current-differencing structure [22].

Instead of using an operational amplifier as the error amplification block, it consists of a current differencing (CD) stage. The main advantage of this technique is that it allows low-voltage operation. Also, the configuration renders a smaller feedback factor that reduces the excessive loop gain.

Kamal *et al.* [23] proposed a topology in which an external capacitor is not required for the stability. The topology uses PMOS as pass device and implements a compensation circuitry in between output of error amplifier and drain of pass devices for improving its performance over uncompensated system.

The LDO with NMOS as a pass device proposed in [24] consists of an error amplifier, a floating voltage source, the pass element, and the feedback network. This architecture uses switched floating capacitors to take advantage of using NMOS transistor as a pass device.

Wang *et al.* [25] have suggested high precision low dropout regulator with nested feedback loops. A zero-tracking compensation loop is nested inside of the negative feedback loop comprising an error amplifier. It utilizes PMOS transistor as pass device.

Couto *et al.* [26] proposed a low drop-out regulator using multi-gate transistors. In this approach, LDO includes a multi-gate transistor at differential stage. First gate of this multi-gate transistor responsible for generating a nominal bias current and second gate is responsible for adjusting the bias voltage based on output. This approach reduces the transients in the regulator output voltage resulting from sudden changes in current drawn by the device load.

Table 3.2 compares the performance parameters of existing capacitor free low drop-out regulators available in literature. From table 3.2, it is observed that there is no need of external capacitor for that stability of LDOs while maintaining its specifications.

Table 3.2 Comparison of Different Capacitor Free Low Drop-out Regulators

Parameters	Unit	[15]	[16]	[17]	[21]
Year		2005	2008	2009	2011
CMOS Technology	µm	0.09	0.18	0.25	0.35
Drop-out Voltage	mV	90	160	50	110
Ground Current (I_q)	mA	6	0.2	0.04	0.05
PSRR	dB	–	70 at 10k Hz	-80 at 1kHz	>50 at 3kHz
Current Efficiency	%	94.3	99.99	-	-
Line Regulation	mV/V	-	1.27%	-	0.012%
Load Regulation	mV/mA	-	0.002%	-	0.005%
Area	mm^2	0.008	-	-	0.056

3.3 ANALYSIS OF VARIOUS LDOs COMPENSATIONS TECHNIQUES

In low drop-out regulators, common-source PMOS pass elements are used. Due to the high output impedance of common source pass elements the output pole location changes with the variation in load and the stability of the circuit decreases. Therefore some compensation schemes are required to increase the stability. The various compensation schemes reported in literature [6, 27-29] are as follows:

3.3.1 COMPENSATION OF LDOs USING EQUIVALENT SERIES RESISTANCE (ESR)

The compensation technique shown in Figure 3.7, the output capacitor is used by the LDOs to improve the stability [6]. The output capacitor has inherent characteristics of ESR.

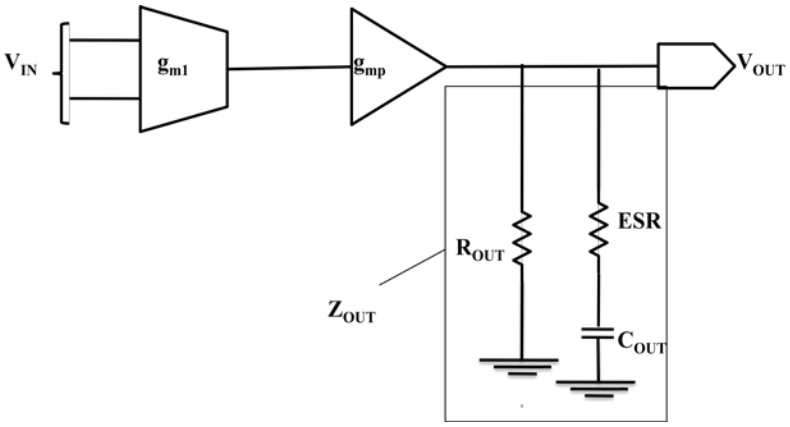

Figure 3.7 LDO with ESR compensation [6]

The equivalent output impedance (Z_{OUT}) is defined as

$$Z_{OUT} = R_{OUT} \parallel \left(\frac{1}{sC_{OUT}} + ESR \right) \quad (3.1)$$

$$Z_{OUT} = \frac{R_{OUT}.\ (1+sC_{OUT}.ESR)}{1+s\ C_{OUT}(R_{OUT}+ ESR)} \quad (3.2)$$

From equation (3.2), it can be seen that the output impedance contains zero introduced by ESR. The zero introduced by ESR is used to reduce excess negative phase shift. The ESR zero frequency is inversely proportional to the output capacitor (C_{OUT}) and the value of ESR zero frequency is given as.

$$f_{ZERO} = \frac{1}{(2\pi * C_{OUT} * ESR)} \quad (3.3)$$

In this technique, the LDO normally require the output capacitor of appropriate value to assure regulator stability and avoid oscillation [1, 6].

3.3.2 COMPENSATION OF LDOs USING CAPACITIVE FEEDBACK FOR FREQUENCY COMPENSATION

The basic idea for capacitive feedback is to reduce the requirements of ESR compensation by generating the internal left hand side pole zero to compensate the LDO. It is common approach to compensate two stage operational amplifier compensation. The Figure 3.8 shows the two-stage operational amplifier with capacitive feedback compensation technique.

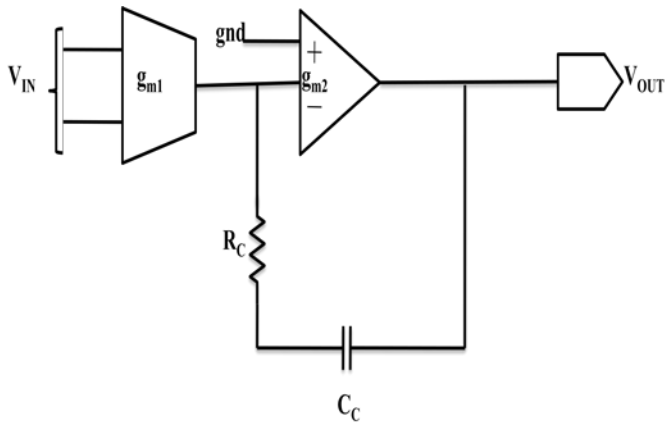

Figure 3.8 The two-stage operational amplifier block with capacitive feedback [27]

From Figure 3.8, the resultant zero location without zero resistance (R_C) is defined as

$$f_Z = \frac{gm_2}{2\pi * C_C} \tag{3.4}$$

The zero location with R_C in feedback is given as

$$f_Z = \frac{1}{2\pi * C_C * \left(\frac{1}{gm_2} - R_C\right)} \tag{3.5}$$

Thus stability requirement can meet through without using rigorous ESR compensation scheme [27].

3.3.3 COMPENSATION OF LDOs USING FEED-FORWARD COMPENSATION

The feed-forward compensation is also a commonly used compensation method. In feed-forward compensation a feed-forward capacitor is placed across RF_1 between output signal and feedback signal as shown in Figure 3.9.

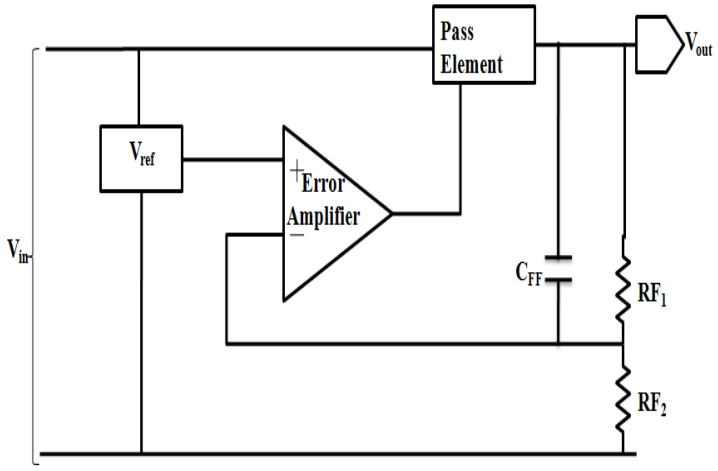

Figure 3.9 LDO with feed-forward compensation [28].

RF_1, RF_2 and C_{FF} form a pole-zero pair and the frequency of pole-zero pair is given as

$$f_{ZERO} = \frac{1}{2\pi * C_{FF} * RF_1} \tag{3.6}$$

$$f_{POLE} = \frac{1}{2\pi . C_{FF} . (RF_1 \,||\, RF_2)} \tag{3.7}$$

or

$$f_{POLE} = \frac{RF_1 + RF_2}{2\pi . C_{FF} . (RF_1 . RF_2)} \tag{3.8}$$

The zero adds some beneficial phase lead and the pole adds phase lag in the circuit. The phase lag generated by pole tends to cancel out the phase lead generated by the zero. The net compensation phase is obtained by the difference between the zero phases increased and the pole phase has decreased. In order to improve the phase margin, pole-zero pair must be positioned at unity gain frequency. From equations (3.6) and (3.8), it can be seen that when RF_1 is much larger than RF_2, the pole-zero pair are far apart from each other to obtain the maximum phase compensation. When RF_1 is reduced, the pole-zero pair get closer to each

other, gradually reducing the effect of phase compensation. Therefore, for higher ratio of RF_1 and RF_2 and the greater value of capacitor C_{FF}, the feed-forward compensation technique is more efficient. Besides of compensating the circuit, resistances RF_1 and RF_2 regulate the LDO's output voltage. A larger value of feedback resistances can reduce the quiescent current of LDO and improve the efficiency [28].

3.3.4 COMPENSATION OF LDOs USING CASCODE COMPENSATION

The cascode compensation is used to achieve the stability in LDOs. In cascode compensation, a common-gate transistor is used as a buffer along with miller capacitance.

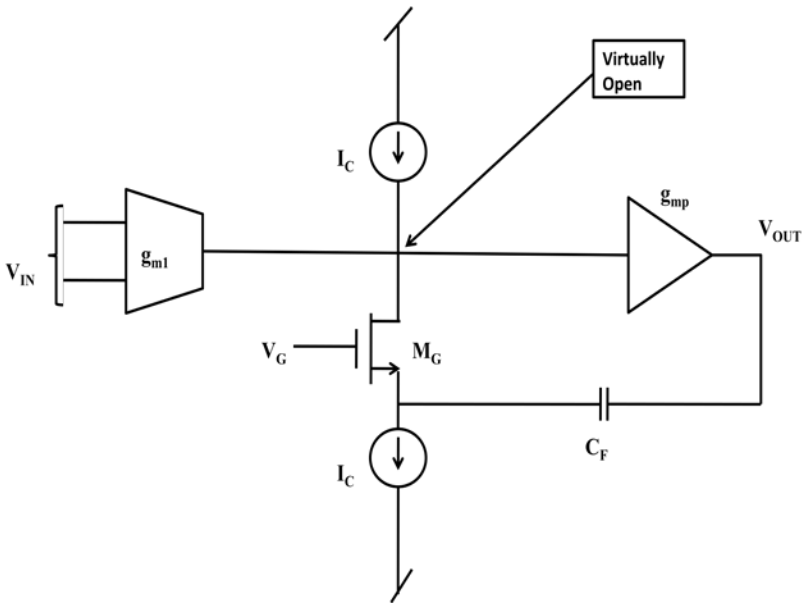

Figure 3.10 Cascode compensation scheme for LDO [29]

In Figure 3.10, compensation capacitor (C_F) is connected between V_{OUT} and source terminal of a common-gate MOSFET (M_G). The current I_C is a dc bias current. Using this compensation technique, the left half plane zero is obtained as

$$\omega_{Z,CF} = -\frac{g_{mG}}{C_F} \tag{3.8}$$

In capacitive feedback technique discussed in section 3.3.2, instead of using a resistor, a current buffer with low input impedance is used in cascode compensation technique to create a left-half plane zero by removing feed-forward path [29].

CHAPTER 4

DESIGN OF PROPOSED LOW DROP-OUT REGULATOR

4.1 INTRODUCTION

This chapter proposes a CMOS low drop-out voltage regulator with improved PSRR. Low drop-out regulators are essential analog building blocks that shield a system from fluctuation in supply rails. The importance of determining their power supply rejection ratio performance is magnified in SoC systems. Power supply ripple rejection ratio (PSRR) is ripple rejection ability of the circuit to reject the ripple of power supply at various frequencies. The chapter is organized as follows. Section 4.2 explains the block diagram and operation of proposed low drop-out regulator. In section 4.3, the circuit description of error amplifier block is discussed. Section 4.4 discusses the need of subtractor circuit and design of pass device.

4.2 BLOCK DIAGRAM REPRESENTAION OF PROPOSED CIRCUIT

The proposed low drop-out regulator is designed to improve power supply rejection ratio (PSRR) of the conventional LDO. In conventional LDO topology, the output of error amplifier is proportional to the gate capacitance of pass device that provides a better PSRR value.

To further improve the PSRR value, one block (B1) is used in the conventional LDO topology [6] as shown in Figure 4.1.

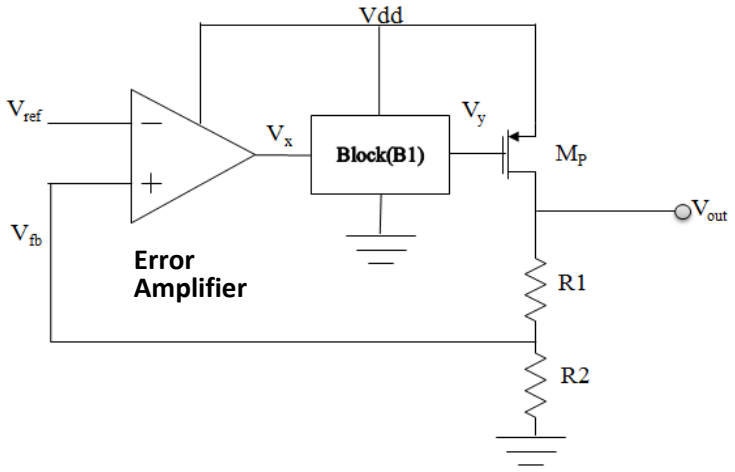

Figure 4.1 Proposed low drop-out regulator block diagram

The circuit diagram of proposed CMOS low drop-out voltage regulator with improved PSRR is shown in Figure 4.2. The output of error amplifier (V_x) is proportional to the gate capacitance of pass transistor so it will provide better PSRR. The transistors (M1-M8) are used to form the error amplifier, transistors (M9-M10) are used to form the block (B1), M_P is the pass transistor, passive elements R1 and R2 are used to form the feedback network to provide feedback voltage (V_{fb}) to the error amplifier.

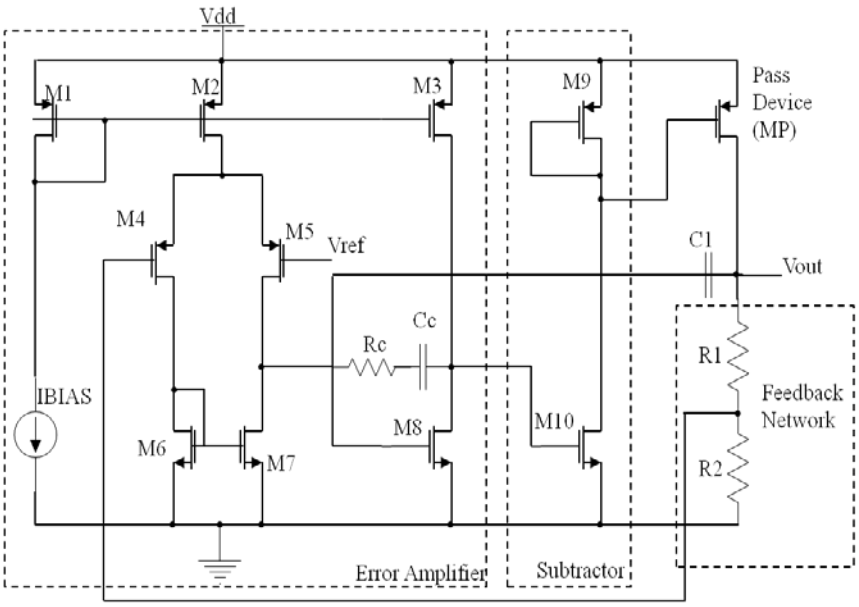

Figure 4.2 Schematic of proposed low drop-out regulator

The compensation capacitor C_1, which is connected between output terminal and gate of transistor M8 is used to reflect the miller capacitance as the gain of three stages for better stability. The RC compensation, which is formed by R_C and C_C, is used to improve the stability of two stage error amplifier.

Table 4.1 Design specification of the proposed circuit

Circuit Parameters	Specifications
Technology	0.18um
Input Voltage Range	1.0-1.8V
Power Supply	1.8V
Gain	>60 dB
Phase Margin	>60 degree
GBW	1 MHz
Output Voltage	1.1V
Load Current	50mA
Ground Current	0A
Drop-out Voltage (V_{DO})	≤200 mV

4.3 DESIGN OF ERROR AMPLIFIER

The Error Amplifier produces an error signal whenever output voltage is differ from the reference voltage. The error output is used to control the amount of current the pass element flows into the load. The error amplifier seeks to set the value of V_{out} to a level where the error signal is as close as possible to zero.

Design specifications for the error amplifier using 0.18um CMOS technology are listed in Table 4.2.

Table 4.2 Design specifications for error amplifier

Circuit Parameters	Specifications
Technology	0.18um
Gain	>60 dB
Phase Margin	>60 Degree
GBW	> 2MHz
Power Supply	1.8V

A topology of two stage error amplifier is shown in Figure 4.3[18]. The circuit consists of a PMOS differential pair and a NMOS current-mirror load connected to ground.

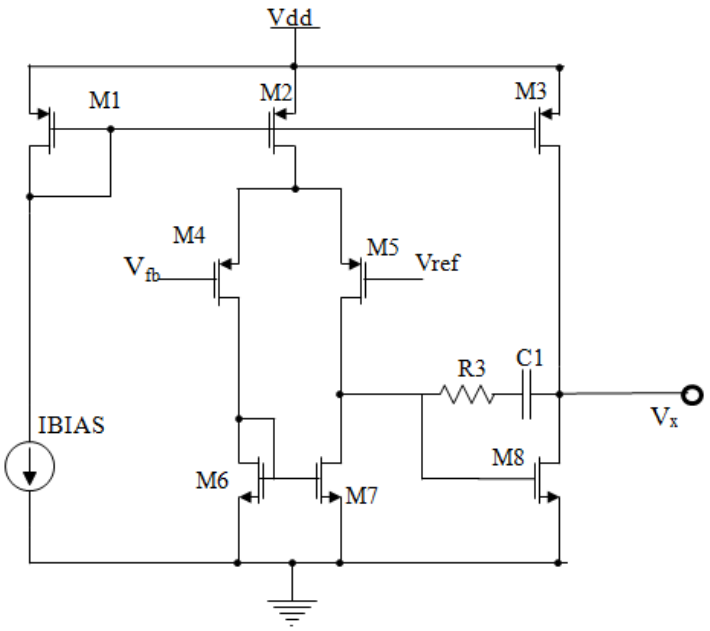

Figure 4.3 Two stage error amplifier with NMOS mirror load

The error amplifier with PMOS as input differential pair and NMOS as mirror load provides better PSRR bandwidth (PSRR BW) at the cost of dc PSRR [10]. There are some ideal design requirements for error amplifier such as high dc gain, low output impedance and greater than 60 degree phase margin [18].

The small signal model of conventional error amplifier with NMOS mirror load is shown in Figure 4.4. Resistances R_1 and R_2 represent the channel resistance of the PMOS input differential pair and NMOS mirror load respectively. The current dependent current source i_{R1}, represents the current flowing through resistor R_2.

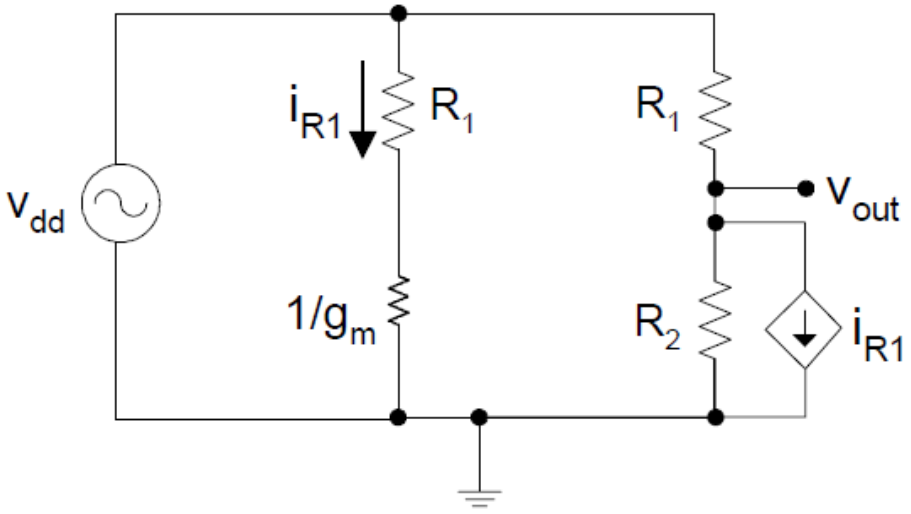

Figure 4.4 Small signal model of error amplifier with PMOS mirror load

The current (i_{R1}) is given as

$$i_{R1} = \frac{V_{dd}}{\frac{1}{gm} + R_1} \tag{4.1}$$

If the trans-conductance parameter (g_m) is very large, the current (i_{R1}) is modified as

$$i_{R1} = \frac{V_{dd}}{R_1} \tag{4.2}$$

The output voltage (V_{out}) is given as

$$V_{out} = V_{dd} \cdot \left(\frac{R_2}{R_1 + R_2}\right) - \quad (iR1 \,.\, (R1 \,||\, R2))$$

(4.3)

Using equation 4.2, the output voltage (V_{out}) is modified as

$$V_{out} = V_{dd} \cdot \left(\frac{R_2}{R_1 + R_2}\right) - \frac{V_{dd}}{R_1} \cdot (R_1 \,||\, R_2)$$

(4.4)

or

$$V_{out} = V_{dd} \cdot \left(\frac{R_2}{R_1 + R_2}\right) - \frac{V_{dd}}{R_1} \cdot \frac{R_1 * R_2}{R_1 + R_2} \tag{4.5}$$

or

$$V_{out} = 0 \tag{4.6}$$

From equation (4.6), it is observed that ac ripples are not available at the output.

4.4 DESIGN OF SUBTRACTOR CIRCUIT AND PASS TRANSISTOR

In the proposed low drop-out regulator block diagram (shown in Figure 4.1) discussed in section 4.2, the PMOS pass device requires noise at its gate terminal due to V_{dd} so that ripples at the output of LDO get cancelled out. To achieve this, an additional subtractor circuit (block B1) is added in between the output of error amplifier and the pass device. Schematic of subtractor circuit is shown in Figure 4.5.

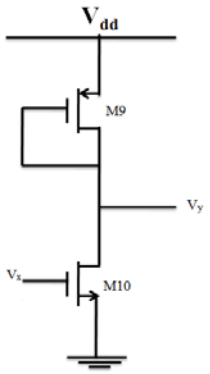

Figure 4.5 Subtractor circuit

Since the resistance across PMOS of subtractor circuit is $1/g_m$, so most of the ripples of power supply are appear at the drain terminal of NMOS transistor as shown in Figure 4.4. The drain terminal of NMOS transistor is connected to gate of pass device to bring ripples of power supply at the gate terminal of pass device so that it removes the effect of power supply ripples from the LDO output. In order to design the block (B1) there is a prime requirement of less resistance of PMOS transistor (M9) to cancel out power supply ripples.

The Pass device (PMOS transistor) shown in Figure 4.6, is responsible for the value of the load current provided by the regulator and value to drop-out voltage.

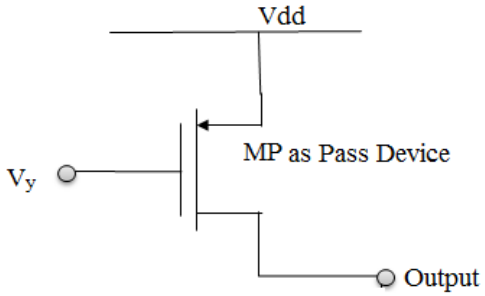

Figure 4.6 PMOS transistors as a pass device

Design specifications of the pass device using 0.18um CMOS technology are listed in Table 4.3.

Table 4.3 Design specifications for pass device

Circuit Parameters	Specifications
Technology	0.18um

Input Voltage Range	1.0-1.8 V
Output Voltage	1.1 V
Load Current	50mA
Ground Current	0A
Drop-out Voltage (V_{DO})	≤ 200 mV

CHAPTER 5

SIMULATION RESULTS & LAYOUT

5.1 INTRODUCTION

The proposed low drop-out regulator circuit has been simulated using TSMC 0.18μm CMOS technology process parameters. The chapter is organized as follows. Section 5.2 presents the simulation results of proposed low drop-out regulator with improved PSRR. In Section 5.3, the layout of the error amplifier block of the proposed circuit, designed using TSMC 0.18μm CMOS process technology is addressed.

5.2 SIMULATION RESULTS OF PROPOSED CMOS LOW DROP-OUT REGULATOR WITH IMPROVED PSRR

The error amplifier circuit shown in Figure 4.2 has been simulated without compensation using TSMC 0.18 μm CMOS technology. The dimension of the transistors of proposed circuit is listed in Table 5.1.

Table 5.1 Transistor sizing of error amplifier

MOSFETS	W(µm)	L(µm)
M1	54	0.72
M2	54	0.72
M3	60	0.38
M4	36	0.72
M5	36	0.72
M6-M7	12	0.72
M8	20	0.72

Figure 5.1 shows the frequency response of proposed uncompensated error amplifier circuit and plots the gain vs. frequency and phase vs. frequency in Figure 5.1(a) and (b), respectively. From Figure 5.1, it is observed that the uncompensated error amplifier shows poor phase margin of 18 degree. For stable operation of the error amplifier, phase margin should be at least of 45 degree and for industrial application it should be 60 degree or more than these values [18].

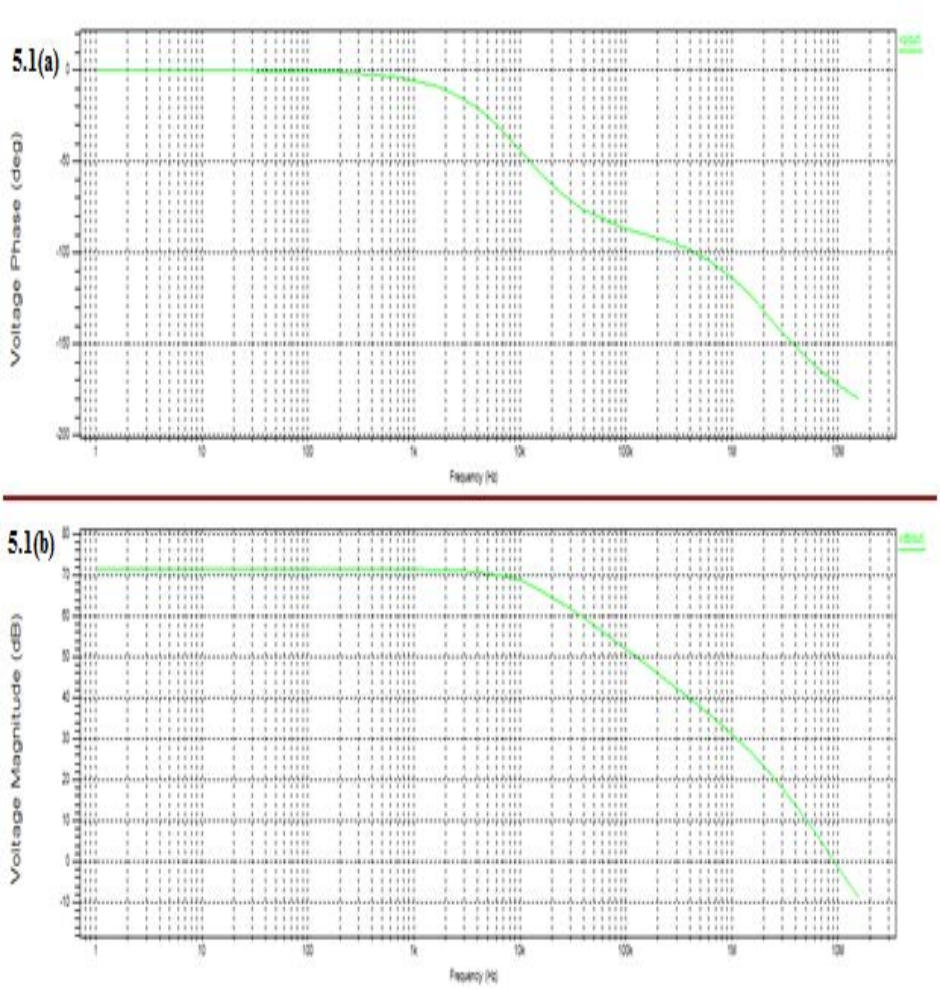

Figure 5.1 AC characteristics of uncompensated error amplifier
(a)Phase Vs Frequency (b) Gain Vs Frequency

The compensated error amplifier block has been simulated using TSMC 0.18 µm CMOS technology. To make the error amplifier circuit stable, the RC compensation technique is used. Using this technique, the value of resistance R_C and capacitance C_C are chosen as 20KΩ and 0.1pF, respectively.

Figure 5.2 shows the frequency response of compensated error amplifier circuit and plots the gain vs. frequency and phase vs. frequency in Figure 5.2(a) and (b), respectively.

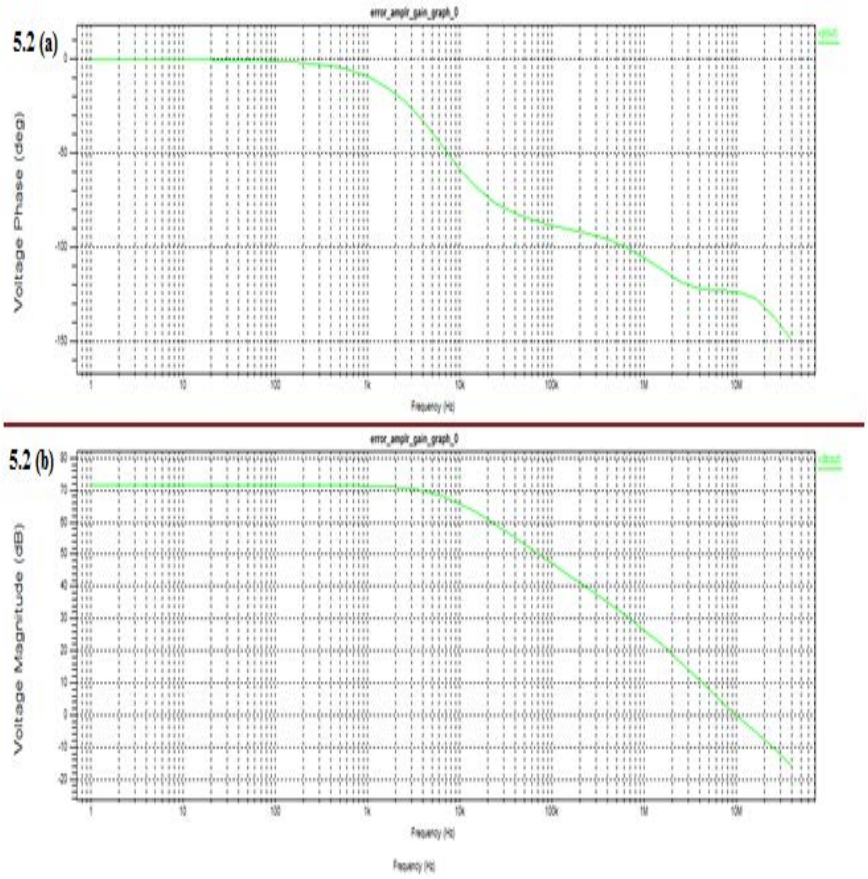

Figure 5.2 AC characteristics of compensated error amplifier

(a)Phase Vs Frequency (b) Gain Vs Frequency

From Figure 5.2, it is observed that the compensated error amplifier shows the better phase margin of 62 degree. It is also observed that the gain of compensated error amplifier is 72dB. Therefore, stability and phase margin have been improved by using RC compensation technique.

The other important aspect of designing an error amplifier besides gain and stability is power supply rejection ratio (PSRR). Power supply ripple rejection ratio (PSRR) is the ripple rejection ability of the circuit to reject the ripples of power supply at various frequencies.

The plot of PSRR for the compensated error amplifier is shown in Figure 5.3.

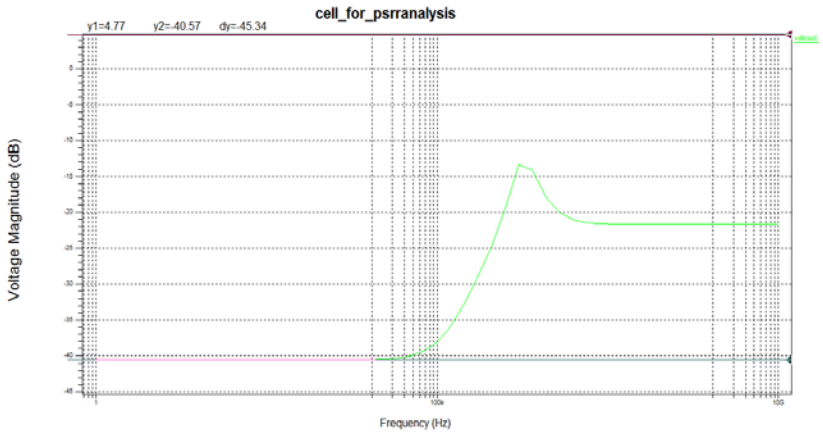

Figure 5.3 Plot of PSRR for error amplifier

From the Figure 5.3, it is observed that the error amplifier has a dc PSRR of -42 dB and PSRR bandwidth of 96 KHz. The high PSRR bandwidth, the basic property of PMOS differential input error amplifier as discussed in section 5.2 has been achieved.

The proposed CMOS Low drop-out regulator with improved PSRR has been simulated using TSMC 0.18 µm CMOS technology. Figure 5.4 shows the frequency response of proposed CMOS Low drop-out regulator with improved PSRR and plots the gain vs. frequency and phase vs. frequency in Figure 5.4(a) and (b), respectively.

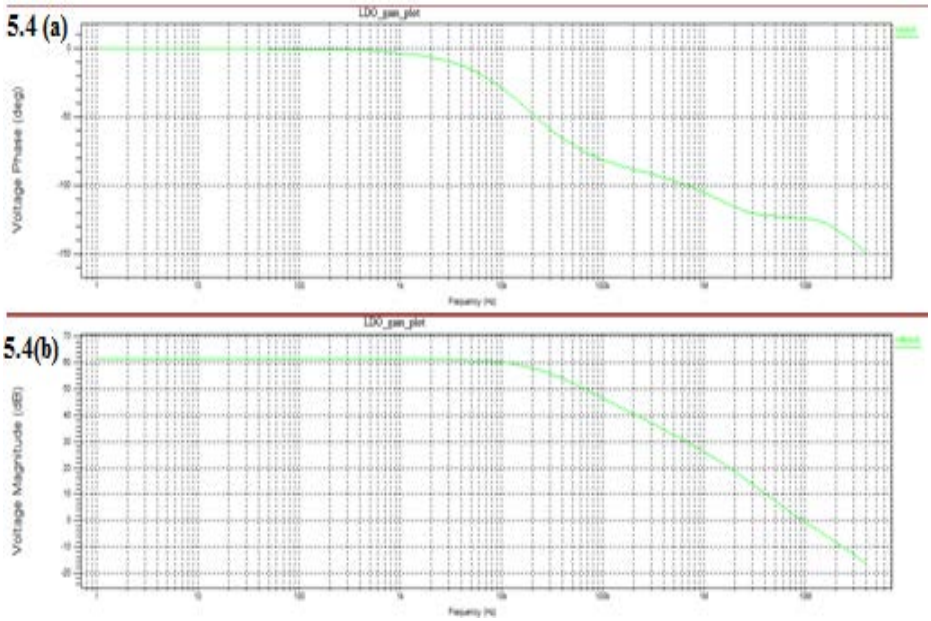

Figure 5.4 Gain plot of proposed LDO circuit (a) Phase vs. Frequency (b) Gain vs. Frequency

From Figure 5.4, it is observed that proposed LDO has gain of 62 dB and phase margin of 61 degree. Therefore, the proposed LDO is stable as it shows phase margin of 61 degree, which is more than required 60 degree phase margin.

The plot of output voltage (V_{out}) vs. input voltage (V_{dd}) is shown in Figure 5.5. From Figure 5.5, it is observed that the regulation range of proposed LDO is 1.25 to 1.8V and for this range the output voltage is 1.2V.

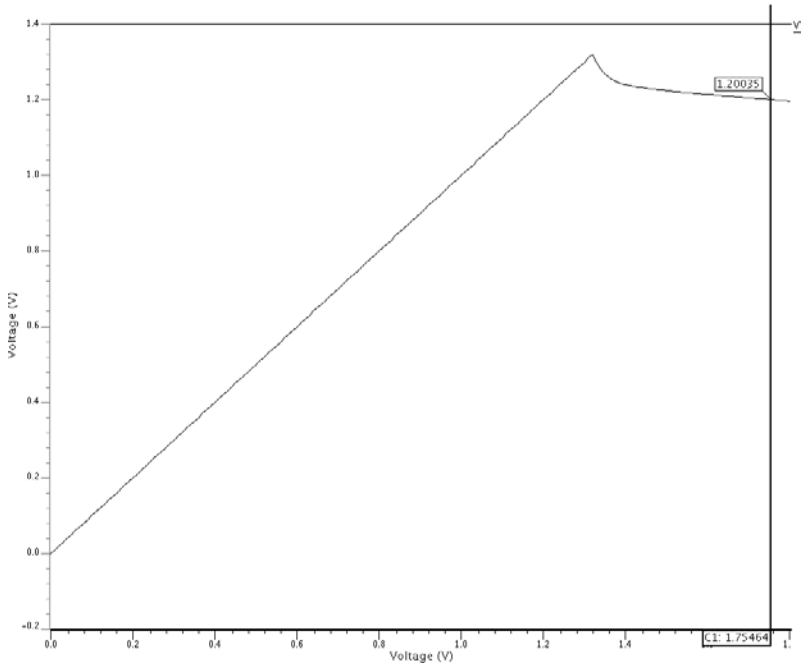

Figure 5.5 Plot of output voltage versus input voltage

The Plot of PSRR of proposed LDO is shown in Figure 5.6. From Figure 5.6, it is observed that the proposed LDO has high dc PSRR of -57.68 dB and PSRR bandwidth of 95 KHz. It is also observed that by the use of block (B1), better dc PSRR with wider PSRR bandwidth has been achieved.

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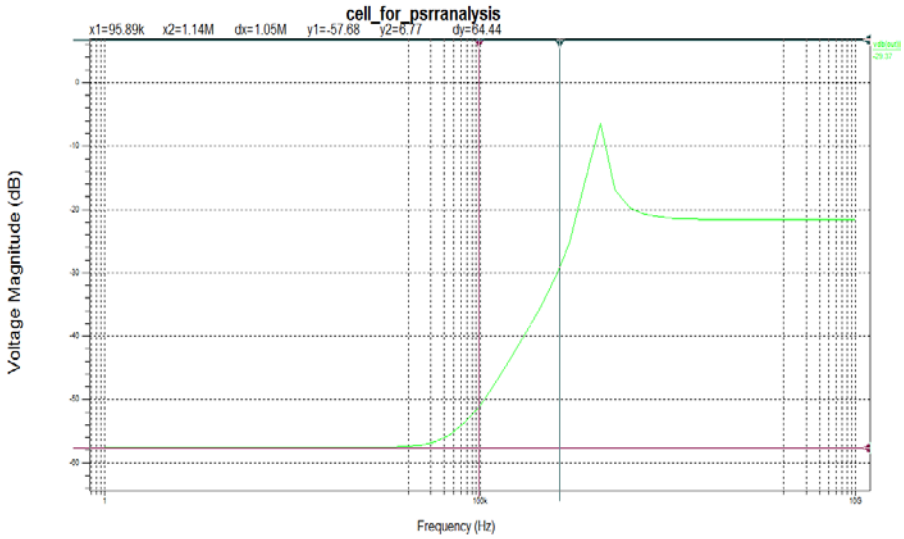

Figure 5.6 Plot of PSRR of proposed LDO

Figure 5.7 shows the variation of output voltage with the load current. The load regulation of proposed LDO is 0.3817% .

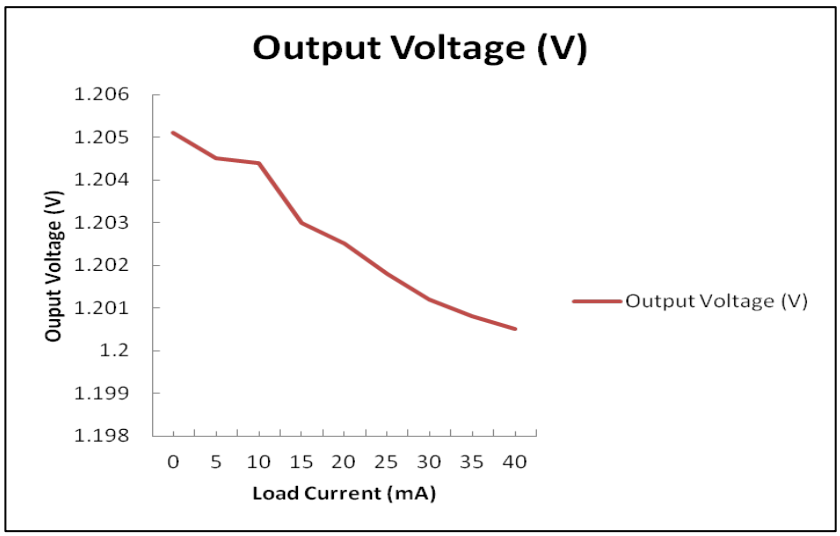

Figure 5.7 Plot of output voltage versus load current

The variation of output voltage with load current is listed in Table 5.2.

Table 5.2 Variation of output voltage with load current

Output Voltage (V)	Load Current (mA)
1.2051	0
1.2045	5
1.2044	10
1.2030	15
1.2025	20
1.2018	25
1.2012	30
1.2008	35
1.2005	40

The output voltage is plotted with respect to temperature and is shown in Figure 5.7. From the plot, it is observed that the proposed LDO provides stable output over a wide range of temperature.

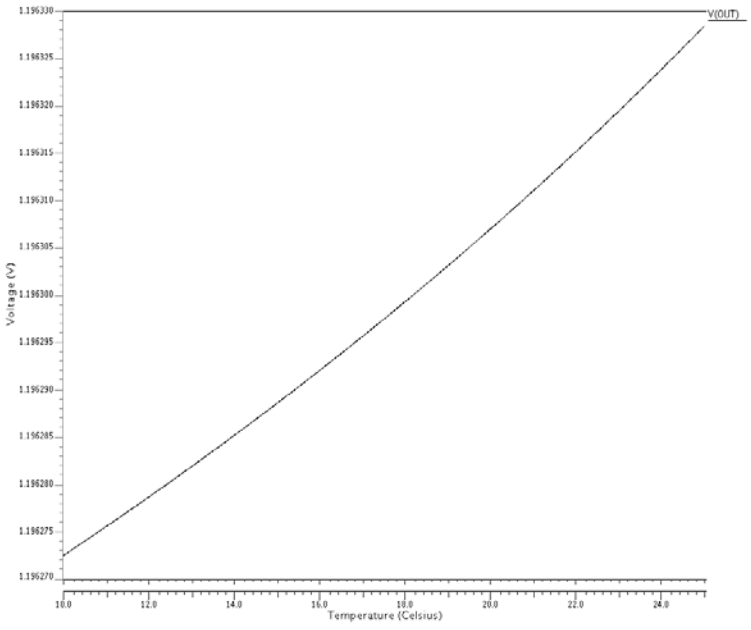

Figure 5.7 Output voltage vs. temperature plot

5.3 LAYOUT DESIGN

The physical layout of error amplifier has been designed using UMC 0.18μm CMOS process technology in cadence virtuoso layout editor. Design Rule Check (DRC) is performed in order to verify that layout fulfills all electrical and geometric rules provided by foundry. The basic design rules are:

Metal 1 to metal 1 spacing	0.24 μm
Minimum contact size	0.24 μm . 0.24 μm
Poly to poly spacing	0.24 μm
Poly to metal spacing	0.28/0.00 μm
Contact overlap to p+ diffusion	0.1 μm
Metal 1 width	0.24 μm
Poly extension beyond active	0.22 μm
Minimum contact spacing	0.26 μm
N well overlap p+ diffusion	0.43 μm
Diffusion contact to poly spacing	0.15 μm
Minimum p+ implant overlap p+ diffusion	0.22 μm
Poly width	0.18 μm
Minimum poly extension on to field region	0.22 μm
Poly contact to diffusion edge spacing	0.18 μm
Minimum poly overlap contact	0.1 μm
Minimum metal area	0.1764 μm^2
Minimum metal2 width	0.28 μm
Metal1 and metal2 overlap over via	0.08 μm
Minimum non equal potential 1.8 V N well spacing	2 μm

The layout of compensated error amplifier is shown in Figure 5.8.

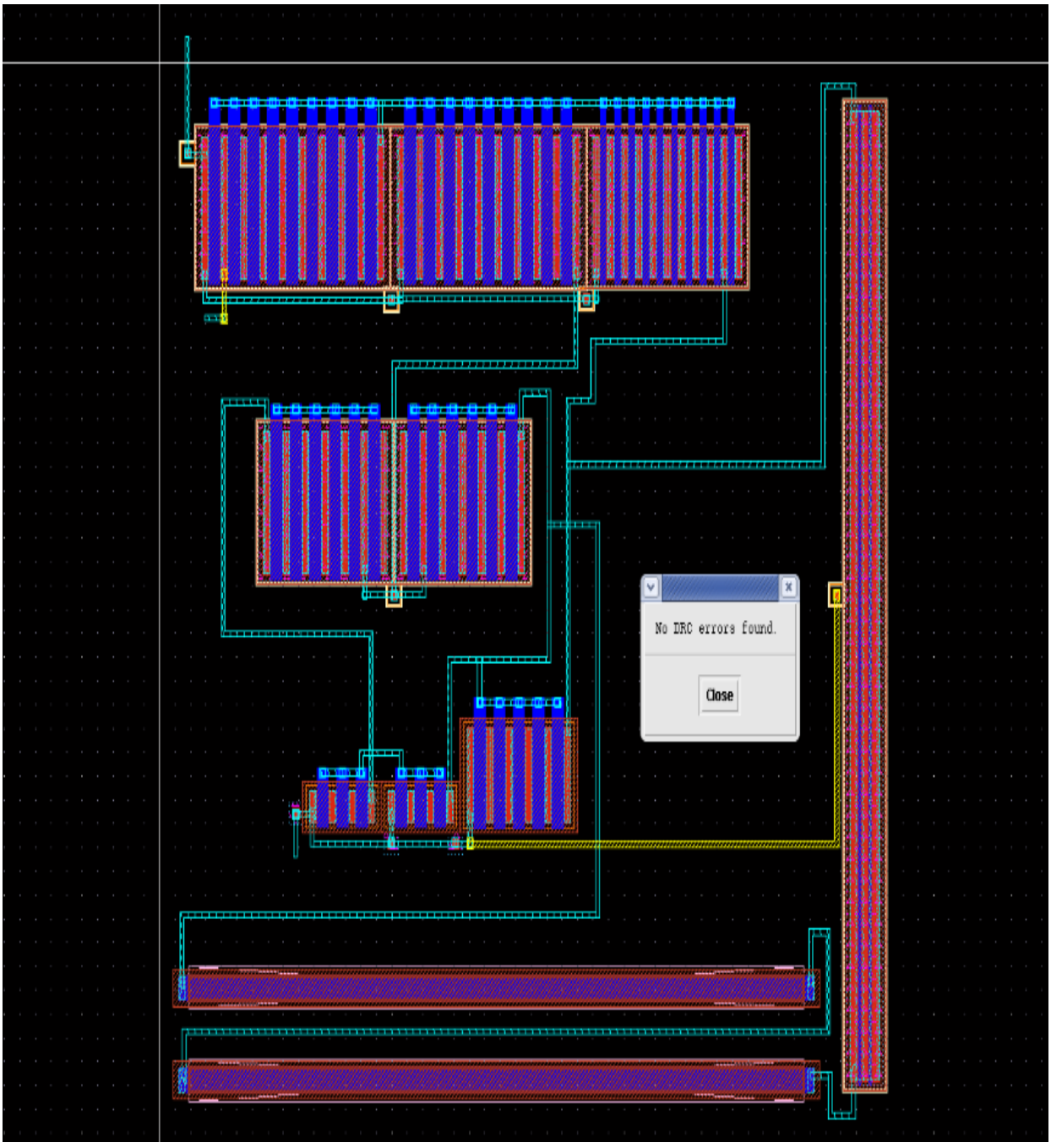

Figure 5.8 Layout of the Error Amplifier block

Table 5.4 compares the performance parameters of proposed CMOS low drop-out regulator with improved PSRR with the existing low drop-out regulators available in literature. From the table it is observed that the proposed circuit has wider range of PSRR with better dc PSRR.

Table 5.4 Comparison of proposed circuit with the LDOs available in literature [7,15,18,22,30-34]

Circuit Parameters	**[7]**	**[15]**	**[18]**	**[30]**	**[31]**	**[32]**	**[33]**	**[34]**	**[22]**	**Proposed LDO**
Year	2006	2007	2004	2012	2008	2012	2010	2009	2009	2013
Technology (µm)	0.5	0.35	0.5	0.18	0.35	0.18	0.18	0.35	0.18	0.18
Input voltage range (V)	2.8-3.8	2.5-5.5	3.3	2.0-3.2	1.2	3.0-5.0	4.0-5.5	3-5	1.2-1.8	1.25-1.8
Output Voltage (V)	1.8	1.8	2.8	1.25	1.0	2.8	2.8	2.5	1.0	1.2
PSRR (dB)	-30dB at 20KHz	45dB at dc	-	64.3dB at dc	-30dB at dc	-56dB at dc	-69dB at dc	-75dB at 1kHz	-41dB at 1KHz	-57.68dB at dc, -31dB at 1MHz
PSRR BW (KHz)	-	20KHz	-	<1KHz	-	-	25KHz	1kHz	1KHz	96 KHz
Gain (dB)	58dB	61dB	55dB	40dB	-	60dB	-	-	-	62dB
Phase Margin (Degree)	60°	65°	60°	-	-	63°	-	-	-	61°
Load Capacitor C_L (µF)	2.2 µF	1 µF	2.2 µF	(0.47-4.7)µF	-	1 µF	-	3 µF	-	-
Load Current I_L (mA)	20	-	23	-	-	-	25 mA	-	50 mA	40mA

CHAPTER 6

CONCLUSIONS AND FUTURE SCOPE

6.1 CONCLUSIONS

A Low Drop-Out Regulator is capable of keeping its specified output voltage over a wide range of load current and input voltage. Low Drop-Out Regulator provide constant supply rail for integrated circuits. Many of the Low Drop-Out Regulators in today's portable devices are integrated into multifunction Power-management integrated circuits. Stability is major concern for Low Drop-Out Regulator design, which can be achieved by either using external capacitor or by using some special compensation techniques. Low Drop-Out Regulator has found applications in portable devices for power management.

In this work, a CMOS low drop-out regulator with improved PSRR has been developed. The proposed circuit utilizes the common source circuit for improving the value of PSRR at dc level along with two stage error amplifier with NMOS mirror load, which provides better PSRR bandwidth. The proposed circuit has been simulated using TSMC 0.18μm CMOS technology process parameters and the simulation results have been presented. The proposed circuit provides an output voltage of 1.2V for the input voltage range of 1.25 to 1.8V. The proposed circuit has been compared with the existing circuits available in the literature and it has been observed that the proposed circuit has better PSRR bandwidth while maintaing the dc PSRR at appropriate level. The proposed circuit can found application in PLL/VCO, audio devices and other devices where the high PSRR along with bandwidth is required. The physical layout of compensated error amplifier is designed using standard UMC 0.18 μm CMOS process technology.

6.2 FUTURE SCOPE

Some suggestions and ideas for future work:

- The two stage error amplifer block based on FGMOS transistors can be used as an error amplifier to reduce the transients in the regulator output voltage resulting from sudden changes in current drawn by the device load while maintaining its PSRR.
- The low drop-out regulator based on flipped voltage follower structure can be designed with utlizing the features of multi-gate transistors to provide better load transients and accuracy, while maintaing the low voltage operation.

LIST OF PUBLICATION

- Ashvani Kumar Mishra and Rishikesh Pandey, “Design Of CMOS Low Drop-Out Regulators: A Comparative Study,” *International Journal of Computer and Technology*, Vol. 4, No2, pp. 324-330, April 2013.

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APPENDIX I

The TSMC 0.18μm CMOS technology model file is listed below.

```
.MODEL CMOSN NMOS (     LEVEL   = 49
+VERSION = 3.1          TNOM    = 27            TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 2.3549E17     VTH0    = 0.3694303
+K1      = 0.5789116    K2      = 1.110723E-3   K3      = 1E-3
+K3B     = 0.0297124    W0      = 1E-7          NLX     = 2.037748E-7
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 1.2953626    DVT1    = 0.3421545     DVT2    = 0.0395588
+U0      = 293.1687573  UA      = -1.21942E-9   UB      = 2.325738E-18
+UC      = 7.061289E-11 VSAT    = 1.676164E5    A0      = 2
+AGS     = 0.4764546    B0      = 1.617101E-7   B1      = 5E-6
+KETA    = -0.0138552   A1      = 1.09168E-3    A2      = 0.3303025
+RDSW    = 105.6133217  PRWG    = 0.5           PRWB    = -0.2
+WR      = 1            WINT    = 2.885735E-9   LINT    = 1.715622E-8
+XL      = 0            XW      = -1E-8         DWG     = 2.754317E-9
+DWB     = -3.690793E-9 VOFF    = -0.0948017    NFACTOR = 2.1860065
+CIT     = 0            CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0            ETA0    = 2.665034E-3   ETAB    = 6.028975E-5
+DSUB    = 0.0442223    PCLM    = 1.746064      PDIBLC1 = 0.3258185
+PDIBLC2 = 2.701992E-3  PDIBLCB = -0.1          DROUT   = 0.9787232
+PSCBE1  = 4.494778E10  PSCBE2  = 3.672074E-8   PVAG    = 0.0122755
+DELTA   = 0.01         RSH     = 7             MOBMOD  = 1
+PRT     = 0            UTE     = -1.5          KT1     = -0.11
+KT1L    = 0            KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0            WLN     = 1             WW      = 0
+WWN     = 1            WWL     = 0             LL      = 0
+LLN     = 1            LW      = 0             LWN     = 1
```

```
+LWL     = 0            CAPMOD  = 2            XPART   = 0.5
+CGDO    = 8.58E-10     CGSO    = 8.58E-10     CGBO    = 1E-12
+CJ      = 9.471097E-4  PB      = 0.8          MJ      = 0.3726161
+CJSW    = 1.905901E-10 PBSW    = 0.8          MJSW    = 0.1369758
+CJSWG   = 3.3E-10      PBSWG   = 0.8          MJSWG   = 0.1369758
+CF      = 0            PVTH0   = -5.105777E-3 PRDSW   = -1.1011726
+PK2     = 2.247806E-3  WKETA   = -5.071892E-3 LKETA   = 5.324922E-4
+PU0     = -4.0206081   PUA     = -4.48232E-11 PUB     = 5.018589E-24
+PVSAT   = 2E3          PETA0   = 1E-4         PKETA   = -2.090695E-3  )
*
.MODEL CMOSP PMOS (                            LEVEL   = 49
+VERSION = 3.1          TNOM    = 27           TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 4.1589E17    VTH0    = -0.3823437
+K1      = 0.5722049    K2      = 0.0219717    K3      = 0.1576753
+K3B     = 4.2763642    W0      = 1E-6         NLX     = 1.104212E-7
+DVT0W   = 0            DVT1W   = 0            DVT2W   = 0
+DVT0    = 0.6234839    DVT1    = 0.2479255    DVT2    = 0.1
+U0      = 109.4682454  UA      = 1.31646E-9   UB      = 1E-21
+UC      = -1E-10       VSAT    = 1.054892E5   A0      = 1.5796859
+AGS     = 0.3115024    B0      = 4.729297E-7  B1      = 1.446715E-6
+KETA    = 0.0298609    A1      = 0.3886886    A2      = 0.4010376
+RDSW    = 199.1594405  PRWG    = 0.5          PRWB    = -0.4947034
+WR      = 1            WINT    = 0            LINT    = 2.93948E-8
+XL      = 0            XW      = -1E-8        DWG     = -1.998034E-8
+DWB     = -2.481453E-9 VOFF    = -0.0935653   NFACTOR = 2
+CIT     = 0            CDSC    = 2.4E-4       CDSCD   = 0
+CDSCB   = 0            ETA0    = 3.515392E-4  ETAB    = -4.804338E-4
+DSUB    = 1.215087E-5  PCLM    = 0.96422      PDIBLC1 = 3.026627E-3
+PDIBLC2 = -1E-5        PDIBLCB = -1E-3        DROUT   = 1.117016E-4
+PSCBE1  = 7.999986E10  PSCBE2  = 8.271897E-10 PVAG    = 0.0190118
+DELTA   = 0.01         RSH     = 8.1          MOBMOD  = 1
```

+PRT = 0 UTE = -1.5 KT1 = -0.11

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 7.82E-10 CGSO = 7.82E-10 CGBO = 1E-12

+CJ = 1.214428E-3 PB = 0.8461606 MJ = 0.4192076

+CJSW = 2.165642E-10 PBSW = 0.8 MJSW = 0.3202874

+CJSWG = 4.22E-10 PBSWG = 0.8 MJSWG = 0.3202874

+CF = 0 PVTH0 = 5.167913E-4 PRDSW = 9.5068821

+PK2 = 1.095907E-3 WKETA = 0.0133232 LKETA = -3.648003E-3

+PU0 = -1.0674346 PUA = -4.30826E-11 PUB = 1E-21

+PVSAT = 50 PETA0 = 1E-4 PKETA = -1.822724E-3)

*