Impact of Voltage Scaled Repeaters on Delay and Power Dissipation of CNT and Copper Interconnects

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CERTIFICATE

I, Sandeep Saini, hereby certify that the work which is being presented in this dissertation entitled "**Impact of Voltage Scaled Repeaters on Delay and Power Dissipation of CNT and Copper Interconnects**" by me in partial fulfilment of the requirements for the award of degree of Master of Engineering in Electronics and Communication Engineering from Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of **K. S. Sandha** and refers other researcher's works which are duly listed in the reference section.

The matter presented in this dissertation has not been submitted in any other University/Institute for the award of any other degree.

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It is certified that the above statement made by the student is correct to the best of our knowledge and belief.

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Abstract

In VLSI circuits, at sub-micron level, the resistivity of copper increases due to several factors due to which delay and power dissipation increase. This degrades the system performance of the circuits. Carbon nanotubes (CNTs) have provided an attractive solution over Copper at deep sub-micron level very large scale integration (VLSI) technologies. Propagation delay and power dissipation are the major design constraints in very large scale integration (VLSI) circuits.

Long interconnections between devices in VLSI circuits also give rise to power dissipation and propagation delay as it increases RC time constant. Repeater insertion is the answer to these challenges. This thesis presents an analysis of propagation delay and effect of repeater insertion on propagation delay for both CNT and Cu interconnects. It has been observed that CNT interconnects have lower propagation delay than the Copper interconnects. Also, propagation delay reduces as we increase the number of repeaters. The above trends are studied with different technology nodes viz. 32nm and 22 nm.

In addition, this work deals with the effect of voltage scaling on propagation delay and power dissipation in repeaters loaded long interconnect used in VLSI circuits. It has been observed that the use of voltage scaling reduces the propagation delay. Use of voltage scaling results in decrease in number of optimum repeaters required.

Power dissipation increases as voltage is scaled down. Thus, the down scaling of voltage in the inserted repeaters in an interconnect can be useful for the cases where control of power dissipation is a stern requirement.

The results for the propagation delay and power dissipation have been obtained using SPICE simulations. The simulation results for 32 nm and 22 nm CMOS technologies have been given for both CNT and Copper interconnects.

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CHAPTER 1

INTRODUCTION TO INTERCONNECTS

1.1 Motivation

All VLSI circuits contain millions of devices and components like transistors. These are linked electrically by the metal wires which are called as Interconnect. In deep submicron technologies interconnects play a critical role. Earlier only gate delay was considered for timing, but now interconnect delay dominates the gate delay. This is because in deep submicron technologies, more number of interconnections have to be used to connect the millions of devices. Thus resistance of the wires increase significantly giving rise to propagation delay.

Due to technology scaling, each IC today contains millions of devices which in turn need millions of interconnections to create links between them [1]. This makes power dissipation another major design constraint in very large scale integration circuits. As projected by International Technology Roadmap to Semiconductors (ITRS) (2000–2003) the total power dissipation in a chip will increase rapidly with increase in total chip capacitance, leakage current and operating frequency.

Copper interconnects are being used as interconnect in the VLSI circuits. With technology being scaled down, the resistivity of copper is also increasing significantly, which in turn; increases interconnect delay [2]. Thus as the technology will advance, the resistivity of the copper will keep increasing. So, other alternative to copper material as interconnect is required. CNT have been seen as the potential interconnect material for future as it favourable properties over copper.

1.2 Background

Aluminium was being used for several years as the interconnect material. Aluminium had some favourable properties like low resistivity, ease of deposition, high melting point, excellent adhesion to dielectrics. As feature size reduced to submicron levels with technology, the delay caused due to the interconnects on the chip became more prominent making the system less reliable. ITRS predicted that, for nanometre size gate, interconnect lengths would decide the communication speed of a VLSI chip [3] as delay due to interconnects dominate gate delay at submicron levels. The interconnect delay is mostly influenced by electrical parasitic i.e. resistance and capacitance. For reducing the

resistance part of the RC delay, various alternatives to aluminium were considered in early 1990s.

Copper emerged as the favourable candidate as copper have nearly half the resistivity as compared to aluminium [4]. Also copper have more melting point as compared to aluminium thus fares better when electro migration is concerned. Thus current carrying capability of copper interconnects is much higher than aluminium interconnects.

The requirement of lower resistance and higher bandwidth is the major concern in interconnects design with the increase in the integration density of the semiconductor chips. To accommodate more interconnects in a chip the cross-sectional dimensions are being reduced rapidly, resulting in dimensions reaching to the order of the mean free path of electrons [5]. Furthermore, the resistivity of copper interconnects is increasing rapidly under the effects of enhanced grain and surface scattering; larger interconnect length; and higher frequency operation. Thus, researchers needed serious alteration in copper interconnect technology because copper interconnect is limited by skin effect, dispersion, signal degradation, power dissipation, and electromagnetic interference at higher frequency.

1.3 Interconnect delay and power dissipation

Interconnects can be modelled as lumped (RC or RLC), distributed, full-wave models, or measured linear sub networks depending on the operating frequency, signal rise times, and the nature of the structure. Initially interconnect circuits were modelled only with RC equivalent circuits and the propagation delay was calculated using a form of Elmore delay [5] through RC, which generally gave good time constant approximation for step responses. But at higher speeds, the electrical length of interconnect becomes a fraction of the operating wavelength, which gives rise to distortion that do not exist at lower frequencies [6]. This made the conventional lumped impedance interconnect models inadequate, and transmission line models such as RLC equivalent models came into effect [7]. An example of such an RLC equivalent model is shown in fig. 1.1.

These RLC values give rise to delay and power dissipation thus degrading the performance of the ICs [7]. To enhance the performance of the ICs, both propagation delay and power dissipation have to be minimised. The increase in load in VLSI circuits

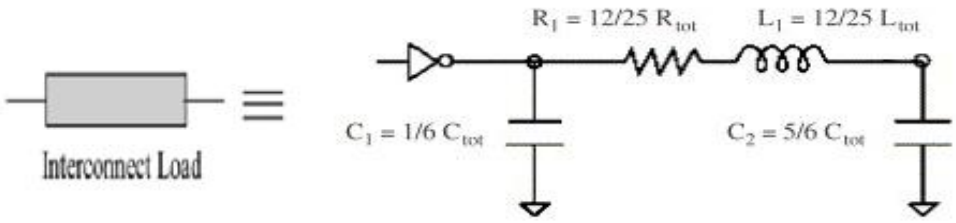


Fig. 1.1: Equivalent RLC Π-model Interconnect model [5]

due to long interconnect and large fan-outs, emphasize the need for effective driver circuits that can discharge capacitances with sufficient speed. The insertion of repeater is used to minimize the overall interconnect response time by reducing the effect of resistance and capacitance.

1.4 Interconnect challenges and future interconnect

In the past only gate delay was considered for timing, but now interconnect delay dominates the gate delay as shown in the figure below Fig.1.2. Now the technology has reached at sub-micron level. At sub-micron level interconnect feature size shrinks. As a result increase in copper resistivity is results due to surface and grain boundary scatterings [8,9] and also due to surface roughness. Further, wires are becoming more and more susceptible to electromigration due to rapid increase in the current densities. Due to the shrinking feature size, a sharp rise in the resistance of copper interconnects is observed. It causes higher propagation delay thus degrading the system performance of VLSI circuits. These are the most important shortcomings which limit the efficiency of copper in future. Thus, to remove these problems other interconnect material has been sought earlier, one such transition was from aluminium to copper interconnects.

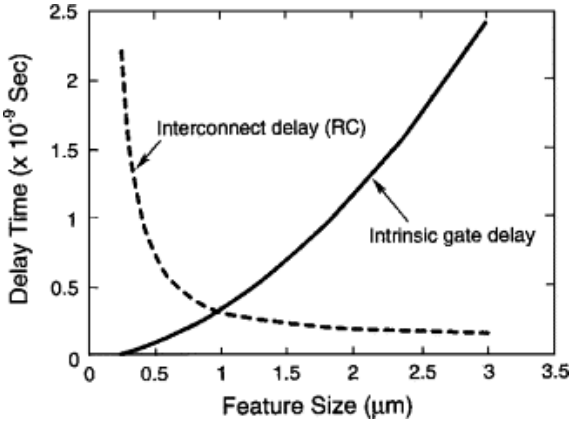


Fig. 1.2 Interconnect delay dominates gate delay in sub-micron technologies [1]

Carbon nanotubes have been proposed as the possible replacement for these metal interconnects in the coming technologies [10]. Carbon nanotubes (CNTs) are simple

graphene sheets that are rolled up into cylindrical form. They have a diameter of the order of 1nm. Depending upon the angle at which the graphene sheets are rolled CNTs show metallic or semiconducting properties. CNTs possess high thermal stability and mechanical strength and large current carrying capacity [11]. CNTs have thus shown capabilities of its being the future interconnect in VLSI circuits. Physical models can be used to study the performance of CNT interconnects [12] and then can be compared to the performance of copper interconnects. Further CNT interconnect can be a single nanotube called single-walled nanotube or can be a bundle of it. A single-walled nanotube provides a very high contact resistance, more than 6.45 kΩ [13] and thus a bundle CNT interconnects is preferably used. The performance of copper interconnects fares poor as the interconnect size decrease due to electromigration as well as increased resistivity. Thus CNTs is seen as the effective replacement of the copper interconnects as there is no problem of electromigration and they are capable of conducting large current densities.

1.5 Objective of the thesis

The main objectives of this thesis are:

- To observe the variation in RLC parameters with change in number of repeaters of SWCNT bundle and Copper interconnect.
- To compare the propagation delay between CNT and Copper for 32 nm and 22 nm technologies for different number of repeaters.
- To study the effect of voltage scaling on the propagation delay of CNT and Copper interconnects.
- To study the effect of voltage scaling on the power dissipation of CNT and Copper interconnects.

1.6 Thesis Organisation

In the **second chapter**, a literature review of various papers is done because with this it become easier to perform the work. A review of papers that are based on Voltage Scaling to improve the performance of interconnect is done.

Third chapter, briefly introduces the basic concepts of interconnect analysis, its types and its modelling. The factors affecting metal interconnects and challenges faced by Cu Interconnects in deep sub-micron technologies are explained.

In **fourth chapter**, Carbon Nanotubes are discussed. Its types are also discussed. The unique properties of the CNTs that make it prime choice for the photonic applications are given.

In **fifth chapter,** circuit modelling of Copper and CNT interconnects is done. Various formulae to calculate Resistance, Inductance and Capacitance of interconnect have been discussed.

In **sixth chapter,** concept of repeater insertion in interconnects and voltage scaling is discussed. Further, parameters used for the simulation purpose are also given.

In **seventh chapter**, variation in propagation delay and power dissipation with technology node has been done for both Copper and CNT interconnects. Hspice simulator tool has been used to observe the values of propagation delay and power dissipation.

Eighth chapter draws conclusions of the thesis and discuss about the future scope.

CHAPTER 2

LITERATURE SURVEY

Rajeevan Chandel *et al.* [14] Delay and power dissipation are the two major design constraints in very large scale integration (VLSI) circuits. These arise due to millions of active devices and interconnections connecting this gigantic number of devices on the chip. This paper gives a bibliographic survey of power dissipation and delay trade off in repeaters loaded long interconnects in VLSI circuits. The significance of the voltage-scaled repeaters for low power VLSI applications has been shown. Voltage-scaled repeaters lead to high-speed low-power VLSI circuits. They also result in saving chip area along with power saving Important technique of repeater insertion in long interconnections to reduce delay in VLSI circuits has been reported during the last two decades. This paper deals with delay, power dissipation and the role of voltage-scaling in repeaters loaded long interconnects in VLSI circuits for low power environment. Trade-off between delay and power dissipation in repeaters inserted long interconnects has been reviewed here. Optimum number of uniform sized CMOS repeaters inserted in long interconnects, lead to delay minimization. Voltage-scaling is highly effective in reduction of power dissipation in repeaters loaded long interconnects. The new finding given here is that optimum number of repeaters required for delay minimization decreases with voltage-scaling. This leads to area and further power saving.

Kaustav Banerjee *et al.* [15] . In this paper, various carbon nanomaterials are discussed, along with their prospects for next-generation interconnects and passive devices. Also a comparative analysis of these nanomaterials with optical and RF interconnects is provided, and is then illustrated why carbon nanomaterials constitute the ideal interconnect technology choice for next-generation ICs. The semiconductor industry is facing an acute problem in the interconnect area as IC feature sizes continually scale below 32 nm. When the cross-sectional dimension of copper wires approach their mean free path, about 40 nm at room temperature, the resistivity of copper rises sharply. According to the International Technology Roadmap for Semiconductors copper's resistivity could be more than three times higher than its bulk value at the 22-nm technology node. This steep rise in resistivity will adversely impact both performance and reliability in terms of circuit delay, chip temperature, and current-carrying capacity. This

limitation of copper interconnects is driving research for alternative interconnect materials and technologies for next-generation IC and is citing carbon nanomaterials, with their many attractive properties, as the frontrunners to potentially replace copper for interconnects and passive devices in ICs, including vias and through-silicon vias (TSVs), horizontal wires(local, intermediate, and global levels) and off-chip interconnects.

Ashok Srivastava *et al.* [16] Based on one-dimensional fluid theory, models for CNT interconnects (SWCNT, MWCNT and SWCNT bundle) are discussed in this paper. They investigated the application of one-dimensional fluid model in modelling of electron transport in carbon nanotubes and equivalent circuits for interconnections and compared the performances with the currently used copper interconnects in very-large-scale integration (VLSI) circuits. In this model, electron transport in carbon nanotubes is regarded as quasi one-dimensional fluid with strong electron-electron interaction. Also Verilog-AMS in Cadence/Spectre was used in simulation studies. Carbon nanotubes of the types single-walled, multiwalled and bundles were considered for ballistic transport region, local and global interconnections. Study of the S-parameters showed higher transmission efficiency and lower reflection losses. Theoretical modelling and computer-aided simulation studies through a complementary CNT-FET inverter pair, interconnected through a wire, exhibited reduced delays and power dissipations for carbon nanotube interconnects in comparison to copper interconnects in 22 nm and lower technology nodes. The performance of CNT interconnects was shown to be further improved with increase in number of metallic carbon nanotubes. This study suggests the replacement of copper interconnect with the multiwalled and bundles of single-walled carbon nanotubes for the sub-nanometer CMOS technologies.

Krishna C. Saraswat *et al.* [17] This paper illustrates why optical interconnects and carbon nanotubes (CNTs) present promising options for replacing the existing Cu-based global/semiglobal (optics and CNT) and local (CNT) wires. The performance of these novel interconnectsare first quantified and is then compared with Cu wires for future high-performance integrated circuits. It is found that for a local wire, a CNT bundle exhibits a smaller latency than Cu for a given geometry. Also, by leveraging the superior electromigration properties of CNT and optimizing its geometry, the latency advantage can be further amplified. For semiglobal and global wires, both optical and CNT options are compared with Cu in terms of latency, energy efficiency/power dissipation, and

bandwidth density. It is observed that optical wires have the lowest latency and the highest possible bandwidth density using wavelength division multiplexing, whereas a CNT bundle has a lower latency than Cu. The power density comparison is highly switching activity (SA) dependent, with high SA favoring optics. At low SA, optics is only power efficient compared to CNT for a bandwidth density beyond a critical value.

C. Bailey *et al.* [18] In this paper the current status and the future challenges of interconnect technologies using carbon nanotubes is discussed. Heterogeneous electronics based systems are driven by an increasing demand for smaller form factor, faster and higher-density interconnection, and miniaturization all at a cheaper cost. 3D packaging, using through-silicon-via technology, is positioned to satisfy these requirements and Carbon Nanotubes as an interconnection technology is gaining extensive interest in the community. This paper provides a summary of the latest advances in such technology, and discusses the challenges that need to be addressed by the community in terms of modeling technologies

Navin Srivastava and Kaustav Banerjee [19] This paper discusses the ability of carbon nanotube bundles to work as interconnect. The work in this paper analyses the applicability of carbon nanotube (CNT) bundles as interconnects for VLSI circuits, while taking into account the practical limitations in this technology. For this a model is developed to calculate equivalent circuit parameters for a CNT-bundle interconnect based on interconnect geometry and the performance of CNT-bundle interconnects (at local, intermediate and global levels) is compared to copper wires of the future. It is shown that CNT bundles can outperform copper for long intermediate and global interconnects, and can be engineered to compete with copper for local level interconnects. The technological requirements necessary to make CNT bundles eligible as future interconnects are also discussed.

Xia Zhangl *et al.* [20] This paper presents an overview of the research work performed on CNTs based electronics and also covers the recent work performed on the development of CNTs as off-chip interconnects including both the advances in aligned CNTs bundles synthesis as well CNTs transfer technology. In addition, some challenges facing CNTs implementation in electronic industry are also pointed. Carbon Nanotubes (CNTs) have drawn a lot of attention due to a combination of extraordinary properties and

a wide range of potential applications. Due to the large potentials in satisfying future large scale integrated circuit requirements, much effort has been focused on the study of CNTs as on-chip interconnects. Combined with other conventional materials, CNTs are also promising alternatives for off-chip interconnect applications. The area of CNTs as off-chip interconnects has, currently, attracted a large research interest from both study point of view and industry.

Wen-Sheng Zhao *et al.* [21] Metallic carbon nanotube (CNT) interconnects has been regarded as a competitive candidate for next generation of interconnects. This paper investigates the equivalent circuit models of CNTs. Based on these models, the performance of CNT interconnects is predicted in comparison with Cu wire counterpart. Further, crosstalk effects in single and double-walled CNT (SWCNT & DWCNT) bundle interconnect architectures are examined. It is found that compared with SWCNT bundle, the DWCNT one can lead to a reduction of crosstalk-induced time delay. Finally, electro-thermal characterization of a metallic SWCNT interconnect array is performed, with self-heating effect treated carefully. In this paper, an equivalent circuit model of SWCNT and MWCNT are proposed. Based on these circuit model, the performance of CNT interconnects is outlined. It is found that the time delay of CNT interconnects is smaller than that of Cu ones at intermediate level or even global one, although it is larger than that of Cu interconnects at local level. This indicates that CNT interconnect is a potential candidate for next generation interconnect applications.

Navin Srivastava *et al.* [22] in this paper ability of single-walled carbon nanotubes (SWCNTs) as interconnects in nanoscale integrated circuits. A detailed analysis of SWCNT interconnect resistance (considering its dependence on all physical parameters, as well as factors affecting the contact resistance), and a quantitative evaluation of the importance of inductive effects in SWCNT interconnects are presented. Also the applicability of carbon nanotube (CNT) based vias (vertical interconnects)—the most realizable CNT interconnects in the current state of the art— is addressed for the first time. It is shown that CNT interconnects can provide 30%–40% improvement in the delay of millimeter long global interconnects. Dense CNT bundle global interconnects are shown to offer a four times reduction in power dissipation while achieving the same delay as optimally buffered Cu interconnects at the 22 nm node. This power saving increases to 8 times at the 14 nm node. Furthermore, 3-D finite-element electrothermal simulations

show that CNT bundles used as vias in between Cu metal layers can provide large improvement in metal interconnect lifetime by lowering the temperature of the hottest interconnects.

Luigi Egiziano *et al.* [13] In this paper the study of the high-frequency effects due to the presence of drivers, repeaters and loads along an intermediate/global interconnects made of a densely-packed carbon nanotube (CNT) bundle, comparing the results with those obtained for an ideally-scaled Cu-based interconnect is done. The CNT interconnect is described by means of a multi-conductor transmission line in cascade with suitable lumped circuit elements. In this paper, the performances of the SWCNT bundles have been analyzed in order to consider their possible use for the future next generation interconnects on intermediate and global level.

Kaustav Banerjee *et al.* [23] The applicability of MWCNTs as an interconnect candidate in future design of integrated circuits has been explored theoretically in this paper. Metallic carbon nanotubes (CNTs) have received much attention for their unique characteristics as a possible alternative to Cu interconnects in future ICs. In this paper, a detailed investigation of MWCNT-based interconnect performance is done. A compact equivalent circuit model of MWCNTs is presented, and the performance of MWCNT interconnects is evaluated and compared against traditional Cu interconnects, as well as Single-Walled CNT (SWCNT)-based interconnects, at different interconnect levels (local, intermediate, and global) for future technology nodes. It is shown that at the intermediate and global levels, MWCNT interconnects can achieve smaller signal delay than that of Cu interconnects, and the improvements become more significant with technology scaling and increasing wire lengths. At 1000-μm global or 500-μm intermediate level interconnects, the delay of MWCNT interconnects can reach as low as 15% of Cu interconnect delay. It is also shown that in order for SWCNT bundles to outperform MWCNT interconnects, dense and high metallic-fraction SWCNT bundles are necessary. On the other hand, since MWCNTs are easier to fabricate with less concern about the chirality and density control, they can be attractive for immediate use as horizontal wires in VLSI, including local, intermediate, and global level interconnects.

B. K. Kaushik *et al.* [24] In this paper, models for MWNT and SWNT bundle interconnects are reviewed. These models are compared at 32 nm technology nodes in

terms of propagation delay and area. Simulation result shows that MWNT requires lesser area than SWNT bundle at different interconnect lengths for same performance of propagation delay. Therefore, for future VLSI technology, MWNTs may be proven as more promising candidate than copper. Multi-wall carbon nanotubes (MWNTs) have potentially provided an attractive solution over single-wall carbon nanotube (SWNT) bundles at deep sub-micron level very large scale integration (VLSI) technologies. This paper presents a comprehensive analysis of propagation delay for both MWNT and SWNT bundles at different interconnect lengths (global) and shows a comparison of area for equivalent number of SWNTs in bundle and shells in MWNTs. It has been observed that irrespective of the type of CNTs, propagation delay increases with interconnect lengths. For same propagation delay performance, the area occupied by SWNT bundle is more than the MWNTs for a specified interconnect length.

Sankar Sarkar *et al.* [25] This paper analyzes the effect of driver size and number of shells on propagation delay for Multi-Walled Carbon Nanotubes (MWCNT) interconnects at 22nm technology node. An equivalent circuit model of MWCNT is used for estimation and analysis of propagation delay. The delay through MWCNT and Cu interconnects are compared for various driver sizes and number of MWCNT shells. The SPICE simulation results show that the MWCNT interconnect has lower propagation delay than Cu interconnects. The delay ratio of MWCNT to Cu decreases with increase in length for different driver size and number of MWCNT shells. However, the delay ratio increases with reduction in number of MWCNT shells. MWCNT is considered to be potential alternative to copper interconnects in future. MWCNT provides significant improvement in propagation delay performance over Copper for long (global) interconnects. Furthermore it is also observed that as the size of driver or number of shells in MWCNT increases the propagation delay through it reduces.

Hossein Sheikhassadi *et al.* [26] .In this paper an efficient and accurate RC model for MWCNT interconnects has been proposed. Before this paper various equivalent circuit models have been demonstrated to study the performance of multiwall carbon nanotubes (MWCNTs). However, most of these models are very complex and predominately use SPICE/HSPICE simulations resulting in high computational time. This paper presents a compact RC model for MWCNT interconnects by different analysis of resistance in RC model. Using this approach, an efficient RC model for MWCNT bundle is also proposed

here, for the first time. In this work, delay modeling of MWCNT interconnects is performed by using Elmore delay expression (EDE), that has shown good agreement with the reference model. The percentage error of the delay for both MWCNT and MWCNT bundle interconnects is found to be less than 2%.

Yehea I. Ismail *et al.* [27] a closed-form expression for the propagation delay of a CMOS gate driving a distributed line is introduced that is within 5% of dynamic circuit simulations for a wide range of loads. It is shown that the error in the propagation delay if inductance is neglected and the interconnect is treated as a distributed line can be over 35% for current on-chip interconnect. It is also shown that the traditional quadratic dependence of the propagation delay on the length of the interconnect for lines approaches a linear dependence as inductance effects increase. On-chip inductance is therefore expected to have a profound effect on traditional high-performance integrated circuit (IC) design methodologies. The closed-form delay model is applied to the problem of repeater insertion in interconnect. Closed-form solutions are presented for inserting repeaters into lines that are highly accurate with respect to numerical solutions. Models can create errors of up to 30% in the total propagation delay of a repeater system as compared to the optimal delay if inductance is considered. The error between the models increases as the gate parasitic impedances decrease with technology scaling. Thus, the importance of inductance in high-performance very large scale integration (VLSI) design methodologies will increase as technologies scale.

Feng Liang *et al.* [28] in this paper a closed-form expression for estimation of the 50% time delay and an empirical formula for the optimal number of repeaters to minimize the total time delay in a single multiwall carbon nanotube (MWCNT) interconnect line with a driver and a load are presented. The comparisons between the results from these empirical formulas and those from the numerical circuit simulations show that these empirical formulas can provide accurate estimations of the time delay and the optimal number of repeaters for the MWCNT interconnects. Moreover, it is also observed that the insertion of repeaters into long MWCNT interconnects can effectively reduce the total time delay of the MWCNT interconnects, as often observed in the traditional copper interconnects. It further reveals that the number of repeaters needed in the MWCNT interconnect is only

about one third of that in their copper counterparts. Moreover, compared with the Cu interconnects of the same geometrical dimensions, only about one third of the repeaters are needed in the MWCNT interconnects to minimize the total time delay.

Patrizia Lamberti *et al.* [29] in the paper the impact of the physical parameters on the EM performances of CNT interconnects is studied by using an optimization method based on the DoE. In this paper the level of influence of the most important geometrical and physical parameters on the 50% propagation delay of a realistic interconnect structure based on a CNT bundle and taking into account both driver and load characteristics is analyzed. The performed study is based on the Design of Experiments approach, and leads to the definition of the relative weight of the different parameters on the considered output ones. The proposed procedure can be adopted in order to study other relevant performances of the nanointerconnect. The impact of the physical parameters on the EM performances of CNT interconnects is studied by using an optimization method based on the DoE.

Debaprasad Das *et al.* [30] The work analyses the crosstalk effects in Carbon Nanotube (CNT), and its impact on the gate oxide reliability. Using the existing models of CNT, the circuit parameters for CNT-bundle interconnect are calculated and the equivalent circuit has been developed to perform the crosstalk analysis. The crosstalk induced overshoot/undershoots have been estimated and the impact of the overshoot/undershoots on the gate oxide reliability in terms of failure-in-time (FIT) rate is calculated. A similar analysis is performed for Cu interconnects and comparisons are made with CNT based interconnect results and it is found that the CNT based interconnect is more suitable in VLSI circuits as far as the gate oxide reliability is concerned. Therefore the impact on gate oxide reliability in not critically impacted with the increase in length of CNT based interconnect. This shows that CNT based interconnect length does not impact the gate oxide reliability and hence router can route long interconnects using CNT without critically affecting the gate oxide reliability.

S. K. Manhas *et al.* [31] In this paper, crosstalk delay is analyzed for three line bus architecture implemented by RLC interconnect models of MWNT and bundled SWNT. Carbon nanotubes (CNTs) are one of the most promising interconnect material for future deep-submicron and nano scale technology. They are more advantageous than copper or

other interconnect materials because of their robustness to electromigration. In this paper, the RLC interconnect models are presented on basis of multi-walled CNT (MWNT) and bundled single-walled CNT (SWNT) by including the concept of CMOS driver. By performing HSPICE simulations, the effect of crosstalk is examined for the both kinds of CNTs. A comparative analysis has been done for crosstalk delay and area for these both kinds of CNTs. From simulation results, it has been observed that numbers of SWNTs in bundle are more than the number of shells in MWNTs for same performance of crosstalk delay. Furthermore, irrespective of the type of CNTs, crosstalk delay is extensively affected by transition time, diameter of CNTs and spacing between two lines. In this paper, crosstalk delay is analyzed for three line bus architecture implemented by RLC interconnect models of MWNT and bundled SWNT. From simulation results, it has been observed that crosstalk delay increases with interconnect length. For same performance, it has been found that numbers of SWNTs in bundle are more than the numbers of shells in MWNTs. As a consequence, area of bundled SWNT is also more than the area of MWNT. Therefore it can be concluded that significant improvement in crosstalk delay can be achieved for MWNT as compared to bundled SWNT at same interconnect length.

Bruce C. Kim *et al.* [32] This paper presents an electrical model of a SWCNT based TSV and compared with that of Copper vias. In this paper analysis of carbon nanotube (CNT) based Through Silicon Vias (TSVs) for package interconnects is provided. The package interconnects are fundamental bottlenecks to achieving high performance and reliability. Electrical modeling is provided and simulations on TSV with copper and carbon nanotubes is provided. The results from the CNT-based TSVs were greatly superior to conventional vias with copper. This paper presents an electrical model of a SWCNT based TSV and compared with that of Copper vias. The analysis shows that CNT-filled through-silicon vias have superior performance to copper filled vias.

A. G. Chiariello1 *et al.* [33] The paper investigates the high-frequency distribution of the current density in Through-Silicon Vias made by bundles of carbon nanotubes (CNTs). These bundles are described by means of a recently proposed circuit model which, in spite of its simplicity, accounts for the kinetic and quantum phenomena involved in the electrical propagation along CNTs and includes the effects of size, temperature and chirality. The particular electrical properties of such a new material make the CNT-based TSVs quite insensitive to skin-effect and

proximity effect.

N.D. Pandya *et al.* [34] An accurate modelling hierarchy for mixed carbon nanotube (CNT) bundle interconnects is presented in this paper. Based on hierarchical modelling, different bundled structures are proposed for different arrangements of single-walled CNTs (SWCNTs) and multi-walled CNTs (MWCNTs). An equivalent model of mixed CNT bundles has been developed by combination of an equivalent single conductor (ESC) model of bundled SWCNTs and MWCNTs. Propagation delay under the effect of dynamic crosstalk has been compared for these proposed structures of mixed CNT bundles. It has been observed that crosstalk induced time delay improves significantly for the structure where MWCNTs are at the periphery and SWCNTs are at the centre in the bundle.

CHAPTER 3

INTERCONNECTS

3.1 Introduction

Aluminium and copper are the commonly used metals for the purpose of interconnect. For the chips of submicron geometry, it is the interconnect delays rather than the device delay that determine performance of the chip. Thus interconnect has attracted attention over the past years because of its growing influence on the overall performance of VLSI circuits. Currently microprocessors contain about 1000m of interconnect for each square centimetre of the die area. Interconnects introduce parasitic resistances, capacitances and inductances that degrade the overall performance of the VLSI system. The interconnect capacitance presents loading to circuits which in turn increase the propagation delay and power dissipation. Also larger die sizes need longer interconnects thus the parasitic resistance must be considered along with the capacitance. Therefore the associated RC delay and power dissipation further degrade the overall circuit performance. It has been predicted that interconnections will be responsible for about 70 to 80% of the signal delay in VLSI systems [35].

3.2 Interconnect types:

Interconnects can be classified as global, semi global or local. In general, local interconnects are the first, or lowest, level of interconnects [36]. Interconnects find their application in integrated circuit (IC) manufacturing. They usually connect gates, sources and drains in MOS technology, and emitters, bases, and collectors in bipolar technology.
They consist of very thin lines and generally used for making very short connections at the basic stage of device. The various types of interconnects are shown in the Fig. 3.1 and are explained below:-

1) **Semi global:-** This type of interconnects provides the connectivity between large modules and input/output circuitry of the device. They are generally wider and taller than local interconnects in order to provide lower resistance. They provide clock and signal distribution within a functional block with typical lengths up to 3 to 4mm.
2) **Global interconnects:-** They provides clock, power and long distance communication between functional blocks and deliver ground to all functions. They

occupy the top one or two layers, and they are longer than 4mm as long as half the chip parameter.

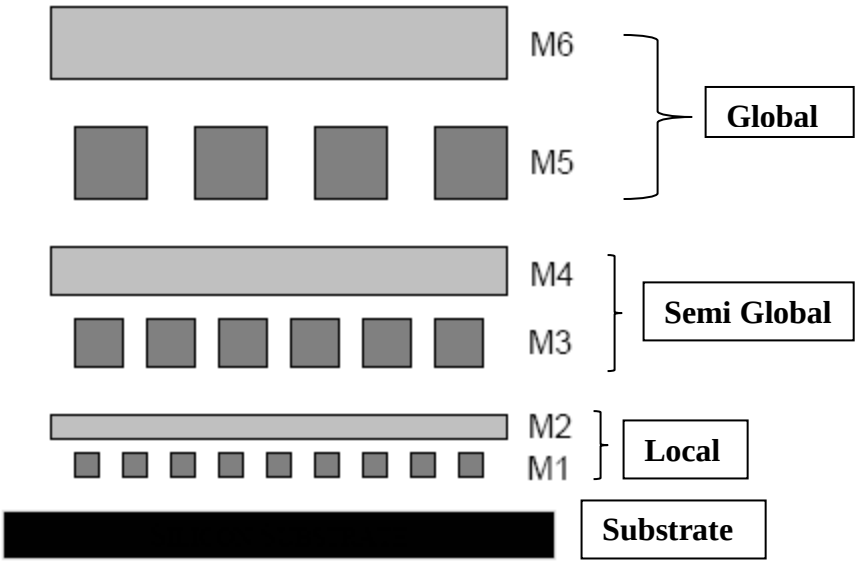


Fig. 3.1 Interconnect hierarchy of 0.25µm CMOS process [47]

3) **Local interconnects:-** These type of interconnects can have higher resistivity than global interconnects since they do not travel very long distances. But they must also be able to withstand higher processing temperatures. Global interconnects covers large distances, between different devices and different parts of the circuit, and therefore are always made up of low resistant metals.

RLC parasitic cause an increase in propagation delay and power dissipation, and introduce extra noise sources, which affect the reliability of the circuit.

3.3 Various modelling methods of interconnects

To study the effect of RLC the introduction of electrical models is required that estimate the real behaviour of the interconnect as a function of its parameters. Depending upon the effects that are being studied and the required accuracy these models vary from simple to complex form.

3.3.1 The Lumped Model

The circuit parasitic of a wire are generally distributed along its length. They are not lumped into a single position. But, for fast observation of the effects of RLC parameters, it is often useful to lump the different fractions into a single circuit element. As long as the inductance of the interconnect is small and the switching frequencies are in the low to medium range, only the resistance and capacitive component of the wire are considered. The distributed capacitive component is lumped into a single RC model as described below.

3.3.1(a) The Lumped RC model

There are different configurations of RC Interconnect models [37] as shown in Fig. 3.2 below

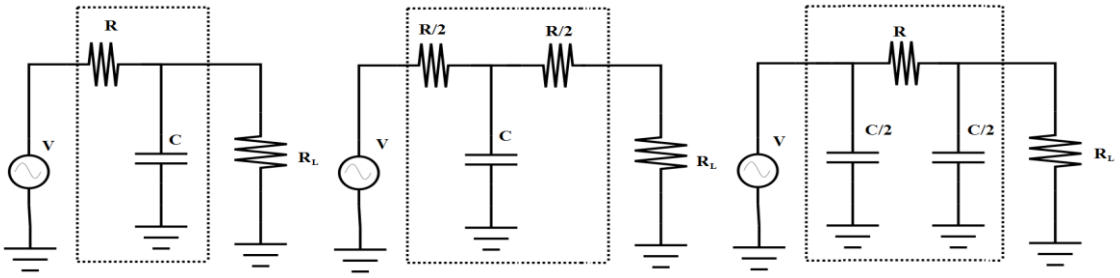


Fig. 3.2 L, T and pi configurations of RC Interconnect models.

Kahng and Muddu [38] proposed a pi-model for distributed RLC interconnect to estimate the driving point admittance at the output of a CMOS gate. A good and simple approximation of an interconnect is obtained with the pi-model. It gives better accuracy in estimating output waveform and delay calculations.

3.3.1(b) The Lumped RLC model

With the adoption of low-resistive interconnect materials and the increase of switching frequencies to the super GHz range, inductance starts to play a role even on a chip. Global interconnects are often wide wires. These wires are low resistance lines that can exhibit significant inductive effects. The lumped-RC model, is no longer adequate, and a resistive inductive- capacitive (RLC) model as in Fig. 3.3 has to be adopted [39].

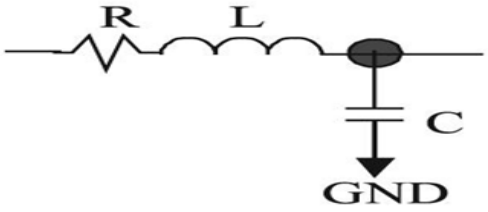


Fig. 3.3 RLC Interconnect model [39]

3.3.2 The Distributed RC Line

The lumped RC model described above is a an inaccurate model. For a resistive-capacitive wire a distributed RC model is more appropriate. As before, l represents the total length of the wire, while R and C stand for the resistance and capacitance per unit length. For computer-aided analysis distributed RC line can be approximated by a lumped multi-stage RC ladder network. Defining the individual element values by

$$RN = R/N \text{ and } CN = C/N \tag{3.1}$$

the desired ladder network can be constructed. Figure 3.4 below shows the equivalent circuits for the cases of m. With m=3,

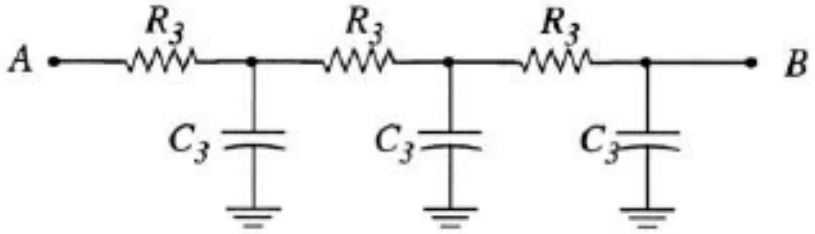


Fig. 3.4 Distributed RC Interconnect model divided into 3 parts [39]

It has been observed that the distributed rc ladder yields more accurate results. However, as the introduction of additional nodes into the circuit simulation program increases the CPU time, the ladder simulation will take more time to execute.

3.4 Importance of repeaters in interconnect line

Repeaters are intermediate buffers in the wire that are used to enhance the vlsi system performance. They are the driver circuits that can discharge capacitances with significant speed, thus helping in delay minimization. The repeaters divide the interconnect into smaller subsections thus making the time delay linear with length as in Fig. 3.5.

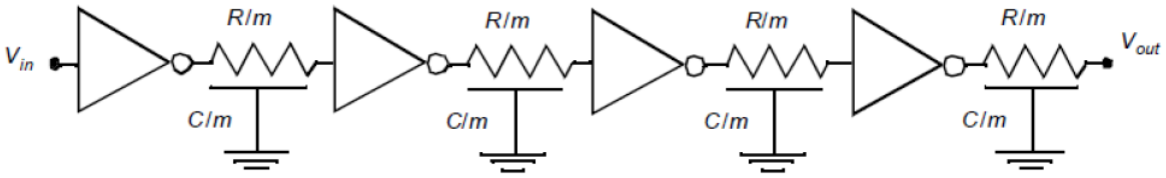


Fig. 3.5 Distributed RC Interconnect with Repeaters inserted in between [40].

The insertion of repeaters helps in minimizing the interconnect response time by alleviating the effect of resistance and capacitance. The delay of the interconnect varies quadratically with its length. The signal delay of long wires therefore tends to dominated by the RC effect. This problem is becoming more tedious in modern technologies, which feature an increasing average length of the global wires at the same time that the average delay of the individual gates is going down. This leads to a peculiar situation that it may take multiple clock cycles to get a signal from one side of a chip to its opposite end. Thus it becomes a major challenge to provide accurate synchronization and correct operation under these circumstances.

3.5 Copper as interconnect

Aluminium was used for decades as the on chip interconnects metal and SiO_2 as insulator in between interconnects. As discussed earlier, due to rapid scaling in the die size the signal delay caused by interconnects become more prominent as compared to the delay caused by the gate. The interconnect delay is adversely affected by parasitic capacitance and resistance. In earlier years, various alternatives to aluminium were considered such as silver, copper and gold, so that resistive part of RC delay can be decreased by using low resistive metals as compared to aluminium (bulk resistivity 2.65μΩcm). Gold leads to deep levels in the silicon band gap and thus diffuses in SiO_2 and affects electronic properties of the VLSI device. Gold (bulk resistivity 2.4μΩcm) is less affected by electro migration but due to above demerit it was not preferred [41]. Although silver (bulk resistivity 1.6μμcm) has the lowest resistivity among these options but due to low melting point and low resistance to electro migration it was not preferred. Copper with close to half resistivity (1.7μΩcm) as compared to aluminium alloy (3.0μΩcm) and with electro migration of the order of ten times better appeared to be the most appropriate for the VLSI interconnect. Copper has higher melting point (1357K) as compared to aluminium

(933K) which gives copper the edge over aluminium in electro migration and as well as in stress migration.

Since copper film has nearly 35% lower bulk resistivity than aluminium, it is expected that the number of interconnect lines with copper will be less than the number required with aluminium one. It has been estimated that by using copper rather than aluminium a reduction of almost 40% in the RC time constant can be achieved. In other words it can said that the speed of circuit will be more with copper interconnects as compared to aluminium interconnects.

3.5.1 Drawbacks of copper interconnect and future interconnect material

In last decade it was found that even copper is not able to fulfil the demands of high speed interconnects. Today the requirement of lower resistance and higher bandwidth is the major concern in interconnects design with the increase in integration density of devices. The cross sectional area is being reduced rapidly to accommodate more number of interconnects in a chip, resulting in dimensions reaching to the order of the mean free path of electrons. The resistivity of copper interconnects is increasing rapidly, as discussed earlier, due to the effects of enhanced grain boundary effect, electromigration and surface scattering, larger interconnect length. Increase in wire resistance due to scaling has caused more voltage drop and power dissipation at the same voltage through wires. However, it is expected that the use of superconducting wires for global interconnects might be a possible solution for the reliable performance of global interconnects in the near future.

Thus change in copper interconnect technology is required since copper interconnect is limited by skin effect, dispersion, signal degradation, power dissipation and electromagnetic interference at high frequency. Electron transmitted through metal wires has an information carrying capacity which is limited by the resistance and capacitance of the cable. Thus to overcome this problem search for methods and materials is on which will be of eminent use in upcoming days. One promising candidate is CNT. Research activities in this field show that metallic CNT has the potential for being next generation of interconnect. CNTs exhibit ballistic flow of electron mean free path of several micrometres and thus is capable of conducting very large current densities which removes the problem of electromigration. They would possess larger lifetime as compared to copper interconnect.

CHAPTER 4

CNT INTERCONNECTS AND ITS PROPERTIES

4.1 INTRODUCION

Carbon nanotubes were discovered in 1991 by Iijima. Since then carbon nanotubes have been of great interest, both from fundamental point of view and for future applications [2]. The most eye-catching features of these structures are their electronic, mechanical, optical and chemical characteristics, which open away to future applications. These properties can even be measured on single nanotubes.

Carbon nanotube (CNT) are hollow cylinders of graphite sheets (called graphene) with a radius of nanometre scale and length ranging from hundreds of nanometres to microns or even millimetres. Carbon nanotubes are carbon allotropes that are made up of carbon atoms in the form of hexagons and are covalently bonded (each bond being an sp^2 bond or bonded to three atoms) to each other and rolled into tubes.

There are infinitely many ways to roll a sheet into a cylinder thus resulting in different diameters and microscopic structures of the tubes. The angles at which the graphene sheet are rolled are known as the chiral angles. CNTs can be classified in many ways such as single wall and multi wall, semiconducting and metallic, bundles, networks or isolated, and in a broad distribution of chiralities.

By using the unit vectors a_1 and a_2, as in Fig. 4.1, with chiral indices given by n and m, geometric parameters of carbon nanotube can be defined.

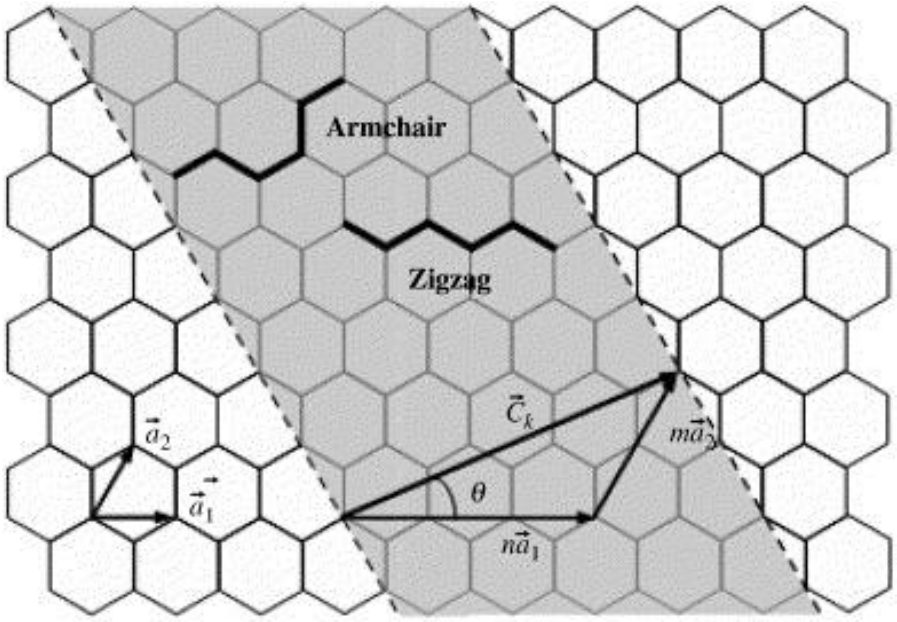


Fig. 4.1 Illustration of chiral vector C in terms of vector a_1 and a_2 [42]

The two main aspects of nanotubes that determine their electrical properties are their chirality and diameter. The chiral vector C represents where the graphite sheet attaches to itself to form the nanotube. The vector is directed along the circumference of the tube and perpendicular to its axis. The magnitude of the vector is equal to the diameter of the tube, while its direction indicates its chirality. Carbon nanotubes have three distinct categories classifying their chirality: armchair, zigzag and chiral tubes. Tubes are also classified as being either metallic or semi conducting. All armchair tubes, described by n = m, are metallic. Zig-zag tubes, described by m=0, are metallic if n is a multiple of three. The condition for a nanotube to be conducting can be stated as the difference between n and m must be a multiple of three or zero. The conditions for the nanotubes to be metallic are equivalent to the chiral vector intersecting the points were valence and conduction bands in the first brillouin zone of the equivalent graphite sheet are degenerate and therefore no band gap occurs. For the tubes having a band gap, the band gap is inversely proportional to the diameter of the tube [43].

4.2 Classification of CNT on the basis of structure

Carbon nanotubes can be classified into two types on the basis of their structure:

(1) Single-walled Carbon Nanotubes (SWCNTs)

(2) Multi-walled Carbon Nanotubes (MWCNTs)

(1) Single-walled carbon nanotubes

Single Wall CNT (SWCNT) consists of a single layer of graphene sheet seamlessly wrapped into a cylindrical tube as shown in Fig. 4.2. They are generated when a two dimensional graphene sheet of a certain size that is wrapped in a certain direction. SWCNTs have only one layer of grapheme sheet with diameters of 0.7 to 10 nm.

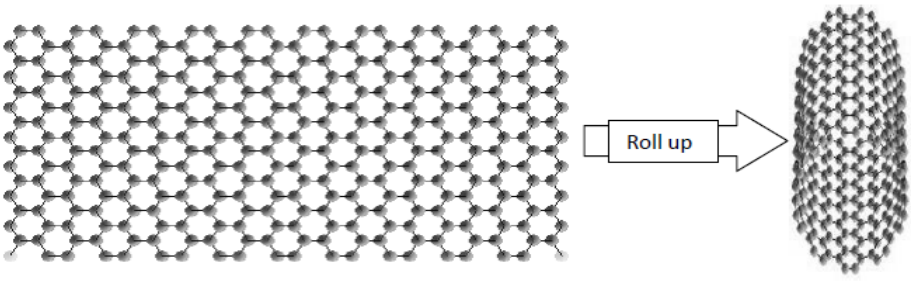


Fig. 4.2 A graphene layer folded in to SWCNT [44]

(2) Multi-walled carbon nanotubes

Multi walled carbon nanotubes (MWCNT) consist of concentric CNT cylinders held within each other by vander Waals forces. The distance between shells is approximately

3.4Å, which is the vander Waals distance for two graphite carbon lattices [44]. An example of a MWCNT is shown in Figure 4.3.

There are two models which can be used to describe the structures of multi-walled nanotubes. In the Russian Doll model, sheets of graphite are arranged in concentric cylinders. In the Parchment model, a single sheet of graphite is rolled in around itself, resembling a scroll of parchment or a rolled up newspaper.

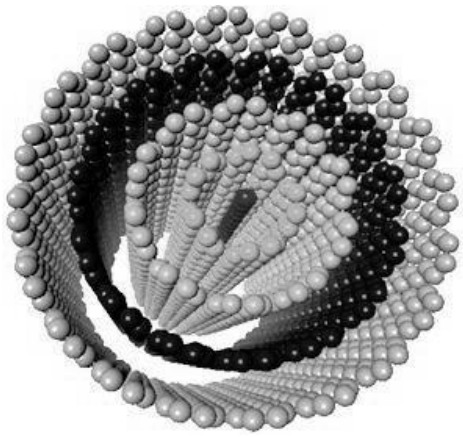


Fig. 4.3 Multiwalled carbon nanotube (MWCNT) [44]

While SWCNTs can be either metallic or semiconducting depending on their chirality, MWCNTs are always metallic and easier to fabricate. However, they are less favourable for interconnects because

- they typically exhibit ballistic conductance over very short lengths as compared to SWCNTs which have typical mean free paths of the order of a micron.
- the concentric shells of MWCNTs can differ in their chirality and can consist of both semiconducting and metallic nanotubes. This translates to different MFPs and the resistances of different shells cannot be assumed to be equal as in the case of SWCNT bundles. This coupling resistance will be dependent on the point of contact of wire and conducting shell, and in turn can be very large.

4.3 Electronics Property of carbon nanotube:

The most exciting properties of nanotube relates to its electronic band structure. CNTs can be metallic or semiconducting, depending on their helicity and diameter. The armchair tubes are always metallic, whereas the zigzag and chiral tubes can be either metallic or semiconducting. The electronic conduction process in nanotubes is quantum confined, because, in the radial direction, the electrons are confines in the singular plane

of the graphene sheet. The conduction process occurs in armchair (metallic) tubes through gapless modes because the valance and conduction bands always cross each other at Fermi energy for a certain wave vector. In most of the chiral tubes, where the unit cell contains a large number of atoms, the one-dimensional band structure shows an opening of the gap at Fermi energy and, hence has semiconducting properties. When the diameter of the tubes increases, the band gap (which varies inversely with the tube diameter) tends to zero, yielding a zero gap semiconductor that is essentially equivalent to the planar graphene sheet. Hence, in a MWNT, the electronic structure of the smallest inner tubes is superimposed by several outer, larger planar graphene like tubes.

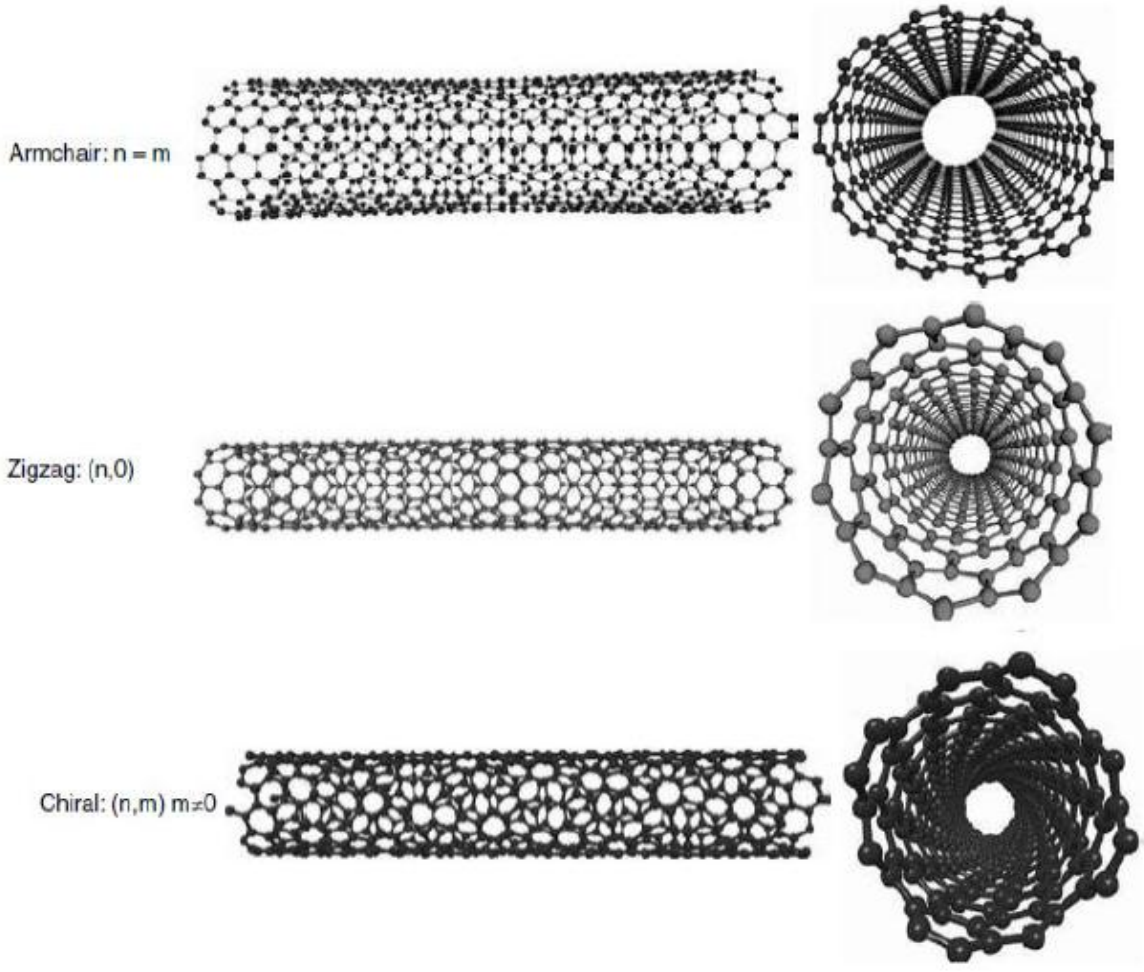


Fig. 4.4 By rolling a graphite sheet (GRPHNE) in different directions, two typical nanotubes can be obtained: zigzag (n, 0), armchair (m, m) and chiral (n, m) where n>m>0 by definition [45].

The electronic properties of the nanotube depend on the diameter and the direction in which the sheet has been rolled up as shown in Fig. 4.4. Some nanotubes are metals with

high electrical conductivity, while others are semiconductors with relatively large band gaps. Because of the interaction between different layers of multi-walled carbon nanotubes, it is difficult to predict their electronic nature. The interlayer interaction is expected in MWNTs but they show no electronic-scattering behaviour. These tubes carry such high current density that it should heat the nanotube to its vaporization temperature. But electrons are thought to be strongly de-coupled from the lattice and, hence the heat is not transferred to the lattice.

4.4 Ballistic flow in CNT

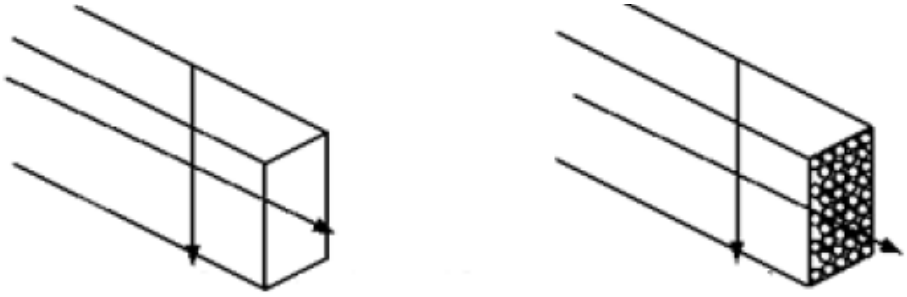
Ideally any perfect metal tube should be a ballistic conductor. In the ballistic conductor, the resistance is independent of the length of the conductor. In other words, all electrons that are injected at one end of the tube should reach the other end without a single electron being lost [46]. The electronic transport is ballistic when the length of the conductor is smaller than the electronic mean free path. On the other hand, diffusive conductors follow ohm's law and, hence, depend upon the length of the conductor. In the band structure of metal carbon nanotubes, there are two distinct linear bands in contrast to single band in normal metals. One band is formed by bonding molecular orbitals and another one is formed by anti-bonding molecular orbitals, and the electrons move in opposite directions in these two bands. Thus it is very unlikely that the electron moving in one direction will change direction as then it has to move to another band i.e. another molecular orbital for changing direction. This keeps them moving in a single direction, and that means no scattering and, hence ballistic nature. Basic electrical properties of semiconducting carbon nanotubes change when they are places inside a magnetic field. The band gap of semiconducting nanotubes narrowed down steadily in the presence of a strong magnetic force. It is anticipated that at very high magnetic fields, the band gap may even disappear completely and the nanotubes can become a metal [46].

4.5 CNT as an Interconnect

Both SWCNTs and MWCNTs are usually many micrometres long and hence can fit well as components in sub-micrometre-scale devices and nanocomposite structures that may play an important role in emerging technologies [44]. IBM has recently been able to manipulate the nanotubes in a controlled way. It has developed the capability of changing a nanotube‘s position, shape, and orientation as well as cutting it by using an atomic force

microscope. NASA researchers have reported a new method for producing ICs using CNTs instead of copper for interconnections. This technology may extend the life of the silicon chip industry by 10 years.

To a large extent, the unique electrical properties of CNTs such as their extremely low electric resistance are derived from their 1D character and the unique electronic structure of graphite. Resistance primarily occurs due to defects in crystal structure, impurity atoms, or an atom vibrating about its position in the crystal. In the case of a CNT, the electrons are not so easily scattered. Due to their small diameter and huge aspect ratio (length to width), nanotubes are essentially 1D systems and therefore electrons have a low chance of scattering, giving rise to very low resistance. The electronic properties of perfect MWCNTs are rather similar to those of perfect SWCNTs because the coupling between the cylinders is weak in MWCNTs.



(a) **(b)**

Fig. 4.5 Schematic showing the comparison of a Copper interconnect (a) and a CNT interconnect (b) bundle [44].

Electrical transport in metallic SWCNTs and MWCNTs is ballistic, that is, without scattering over long nanotube lengths, enabling them to carry high currents with essentially no heating. In contrast, electrons in copper travel only 40–50 nm before they scatter. The low resistance ensures that the energy dissipated in CNTs is very small, thereby solving the problem of dissipated power density that adversely affects silicon circuits. Current densities of more than 1010A/cm2 have been reported for the metallic CNTs without any signs of damage even a an elevated temperature of 250oC, thereby eliminating EM reliability concerns that plague Cu interconnects. Since CNTs do not have any leftover bonds, there is no need to grow a film on the surface in order to tie up the free bonds and there is no need to restrict the gate insulator to silicon dioxide. This

fact implies the use of other superior materials to insulate the gate terminal in a transistor which can result in a much faster device.

However, the high resistance associated with an isolated CNT (greater than 6.45 KΩ) [42] necessitates the use of a bundle (rope) of CNTs, as in Fig. 4.5 and Fig. 4.6, conducting current in parallel to form an interconnection. A single walled nanotube results in a very high contact resistance and high characteristic impedance, and hence a bundle of closely packed parallel CNTs is preferably used above a ground plane.

Moreover, due to the lack of control on chirality, any bundle of CNTs consists of metallic as well as semi-conducting nanotubes (the semi-conducting CNTs do not contribute to current conduction in an interconnect). Furthermore, the observed resistance of a CNT is much higher than the resistance derived due to the presence of imperfect metal-nanotube contacts which give rise to an additional contact resistance. The resistance arising from these imperfect contacts is often so high that it masks the observation of intrinsic transport properties.

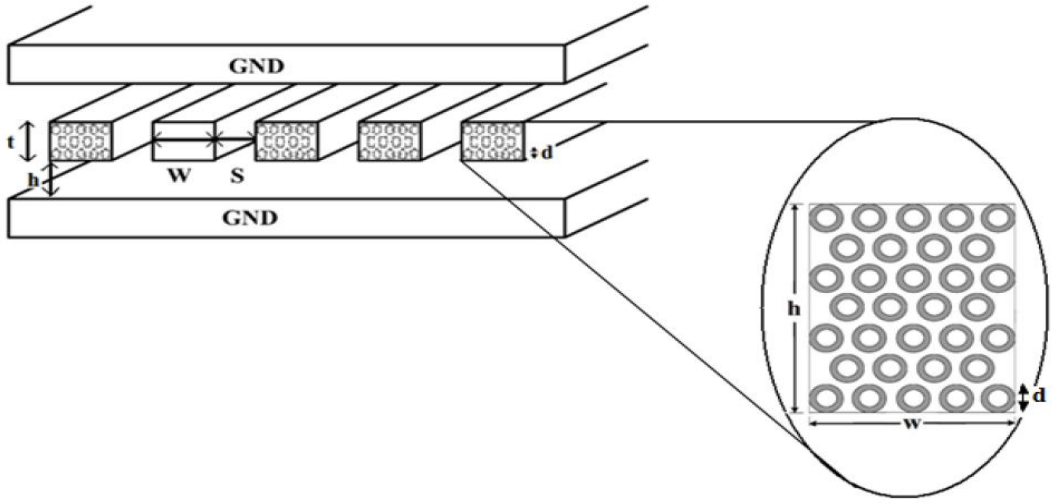


Fig. 4.6 The 2-D structural model of SWCNT bundle interconnect with the inset showing the nanotubes within its bundle [12]

The properties of CNTs as well as the advantages of CNTs over Copper Interconnections can be summarized as follows:

1) The carrier transport is 1D, resulting in ballistic transport with no scattering and much less power dissipation. Scattering-free current transport allows high current densities and improved signal delays.

2) All chemical bonds of the carbon atoms are satisfied and there is no need for chemical passivation of free bonds as in silicon.
3) The strong C–C covalent bonding gives the CNTs high mechanical and thermal stability and resistance to electromigration. Current densities as high as 1010 A/cm2 can be sustained in metallic CNTs.
4) The diameter of a CNT is controlled by chemistry, not by fabrication.
5) Both active devices and interconnections can be made of semiconducting and metallic nanotubes.

CHAPTER 5

CIRCUIT MODELLING OF CNT AND COPPER INTERCONNECTS

5.1 Introduction

The analysis of copper and one dimensional CNT bundle as interconnects for VLSI circuit is done in the chapter. A model is developed to calculate equivalent circuit parameters for a CNT bundle and copper based on interconnect geometry. Using this model, the performance of CNT bundle interconnects at global, local and intermediate level is compared to copper wires. It is shown that CNT bundles can outperform copper for long intermediate and global interconnects, and can be engineered to compete with copper for local level interconnects.

For analytical model equivalent resistance, capacitance and inductance is calculated using equations (given below) for CNT bundle and copper interconnects. On the basis of these parasitic analytical model is designed. Delay is determined at global, local and intermediate level for CNT bundle and compared with copper. This delay analysis is done using Tanner EDA tools in which simulation is done with the equivalent circuit SPICE files.

5.2 Equivalent Circuit model of Copper interconnect

The winbond TSM model [23] is for top global layer interconnect lines with coupling above one ground. According to the model, the thickness of the interconnect is t, the width of CNT bundle is w, and h is the height of the interconnect above the ground. The spacing between the interconnect S is assumed to be equal to the interconnect width, i.e. S = W as in Fig. 5.1.

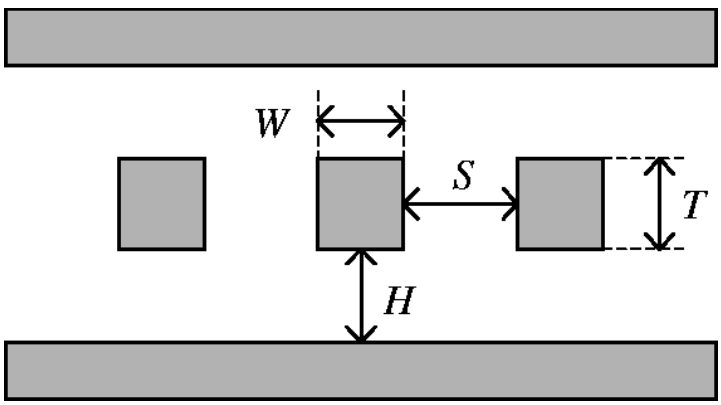


Fig. 5.1 Geometry of Global Interconnect [13]

5.2.1 Equivalent resistance

Based on this model, the resistance of a CNT bundle of length L is given by following equation where ρ is the resistivity of copper,

$$R = \frac{\rho l}{wt} \tag{5.1}$$

Equivalent circuit model of a copper interconnect is shown in Fig. 5.2 below.

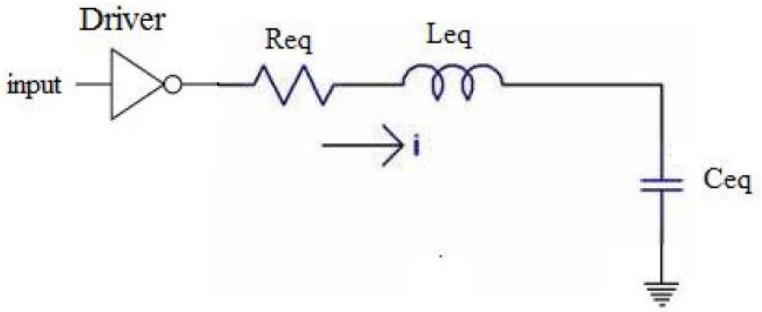


Fig. 5.2 Equivalent Circuit model of copper interconnect [23]

5.2.2 Equivalent Capacitance

The total effective capacitance of the copper interconnect is given by

$$C_g = \varepsilon \left[\frac{w}{h} + 2.04\left(\frac{s}{s+0.54h}\right)^{1.77} . \left(\frac{t}{t+4.53h}\right)^{0.07}\right] \tag{5.2}$$

Where εo is the dielectric permittivity; and εr is the relative dielectric permittivity of copper

$\varepsilon = \varepsilon r \times 8.86 \times 10^{-12}$

Thickness t is determined by t = 3 × W (width of interconnect)

5.2.3 Equivalent Inductance

Inductance associated with copper interconnects is given by the following expression:

$$L = \frac{\mu_\circ . l}{2\pi}\left[\ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{0.22(w+t)}{l}\right] \tag{5.3}$$

Whereas mutual inductance M is given by the following expressions

$$M = \frac{\mu_o}{2\pi}\left[\ln\left(\frac{2l}{d}\right) - 1 + \frac{d}{l}\right] \tag{5.4}$$

Where μ_o is the permeability and given as $\mu_o = 4\pi \times 10^{-7}$

Due to high density of interconnect the pitch (space in between interconnects) s is assumed equal to the w width of interconnect i.e. s = w. Hence the distance between layers of interconnect d is assumed to be equal to the twice the interconnect width.

5.3 Equivalent Circuit Model for Carbon nanotube

The interconnect behaviour of carbon nanotube is described by the transmission line with an RLC model as shown in following figure. Equivalent circuit model of isolated single walled carbon nanotube (SWCNT) is used for simulation because it is more convenient than Multiwall carbon nanotube (MWCNT). This model is taken from Luttinger Liquid Theory as in Fig. 5.3 proposed by PJ Burke [24]. The model and its component are explained in the following subsection.

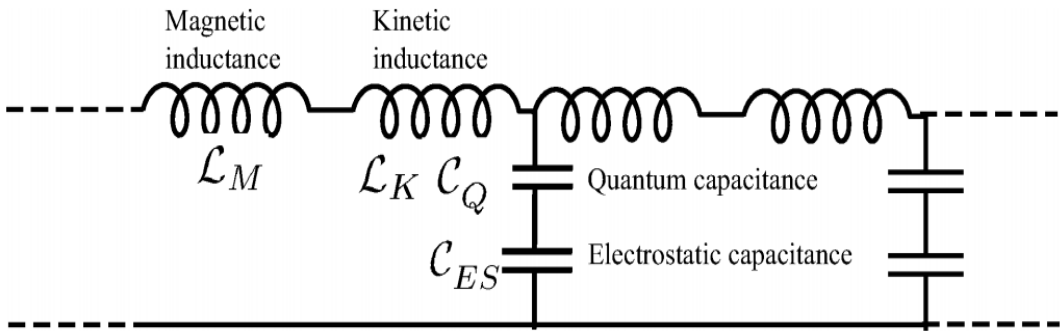


Fig. 5.3 Luttinger theory model [24]

5.3.1 Resistance of Isolated SWCNT

The diffusive component R was not modelled and was taken in ballistic limit. In such case, intrinsic impedance (also called contact or quantum resistance) is given by h/e^2 where e is the electronic charge and h is the planks constant.

Due to spin degeneracy and sublattice degeneracy of electrons each nanotube has four conducting channels in parallel. Therefore the total conductance will be $4e^2/h$ or 155μS. In resistance terms this corresponds to 6.5kΩ. Hence, the minimum resistance that an electron will see when it enters a nanotube is 6.5kΩ; this is independent of nanotube length or chirality. Resistance is given by the following expression

$$R_F = \frac{h}{4e^2} \tag{5.5}$$

This is the fundamental resistance associated with a SWCNT as shown in Fig. 5.4 below that cannot be avoided. As shown in following figure this fundamental resistance (R) is equally divided between the two contacts on either side of the nanotube.

The mean free path of electrons (the distance across which no scattering occurs) in a CNT is typically 1μm [25]. For CNT lengths less than 1μm, electron transport is essentially ballistic within the nanotube and the resistance is independent of length (6.45 KΩ).

However, for lengths greater than the mean free path, resistance increases with length [36], where L_0 is the mean free path and L is the length of the CNT. Hence resistance of CNT is given by

$$R_{CNT} = \left(\frac{h}{4e^2}\right)\frac{L}{L_o} \tag{5.6}$$

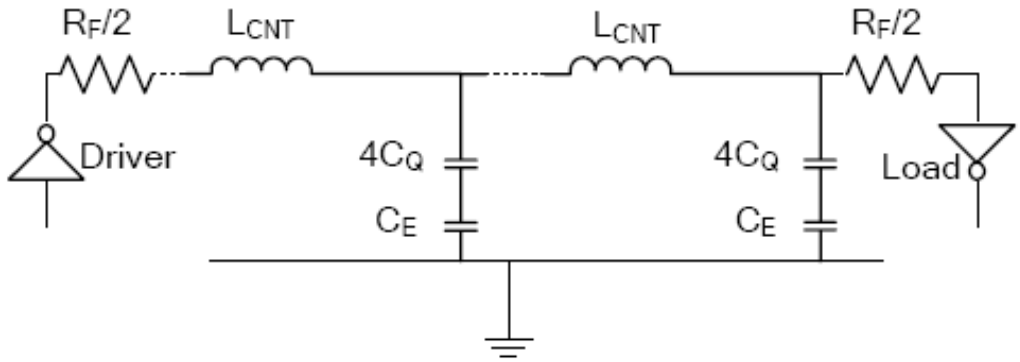


Fig. 5.4 Equivalent circuit model for an isolated SWCNT [16]

5.3.2 Capacitance of Isolated SWCNT

The capacitance of a CNT arises from two sources. The electrostatic capacitance (C_E) is calculated by treating the CNT as a thin wire, with diameter 'd', placed a distance 'y' away from a ground plane as shown in Fig. 5.5. The quantity d and y is shown in the following figure.

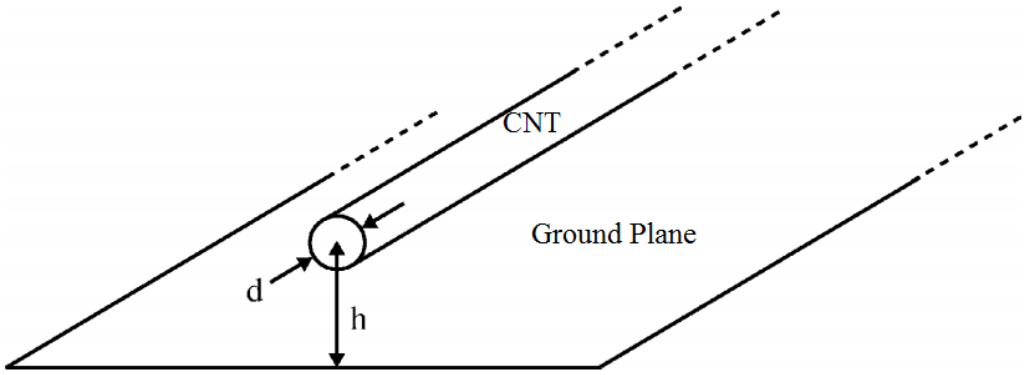


Fig. 5.5 Carbon nanotube with diameter 'd' and, distance 'y' below it [27]

This is the intrinsic plate capacitance of an isolated CNT.

$$C_E = \frac{2\pi\varepsilon}{(y/d)} \tag{5.7}$$

The quantum capacitance (C_Q) accounts for the quantum electrostatic energy stored in the nanotube when it carries current. Due to the Pauli Exclusion Principle, it is only possible

to add electrons into the nanotube at an available quantum state above the Fermi energy level. By equating this energy to an effective capacitance, the expression for the quantum capacitance (per unit length) is obtained as shown in Equation 5.8 [40], where h is the Planck's constant and v_f is the Fermi velocity. For a carbon nanotube ($v_f \approx 8x10^5$m/s), $C_Q \approx 100$aF/um [15].

$$C_Q = \frac{2e^2}{hv_F} \tag{5.8}$$

As a CNT has four conducting channels as described in the previous sub-section, the effective quantum capacitance resulting from four parallel capacitances C_Q is given by $4C_Q$. The same effective charge resides on both these capacitances (C_E and $4C_Q$) when the CNT carries current, as is true for any two capacitances in series. Hence these capacitances appear in series in the effective circuit model.

5.3.3 Inductance of an Isolated SWCNT

The inductance associated with an isolated SWCNT can be calculated from the magnetic field of an isolated current carrying wire some distance away from a ground plane**.** In addition to this magnetic inductance (L_M), the kinetic inductance is calculated in [40] by equating the kinetic energy stored in each conducting channel of the CNT to an effective inductance. The four parallel conducting channels in a CNT give rise to an effective kinetic inductance of $L_K/4$. The expressions for L_M and L_K are shown in Equation 5.9 below:

$$L_M = \frac{\mu}{2\pi}\ln\left(\frac{y}{d}\right) \tag{5.9}$$

$$L_K = \left(\frac{h}{2e^2 v_F}\right) \tag{5.10}$$

For d=1 nm and y=1 um, LM (per unit length) evaluates to ≈1.4 pH/um. On the other hand, LK (per unit length) for a CNT evaluates to 16 nH/um. However, the kinetic inductance (LK) in is derived considering no potential drop along the nanotube; hence it must be treated with care. Since $L_K >> L_M$, the inclusion of LK can have a significant impact on the delay model for interconnects. In the light of experimental evidence of potential drop appearing along the length of a nanotube, LK is excluded from the calculations in this work. The large inductive effects expected due to LK are not observed up to frequencies as high as 10 GHz and the high frequency response is effectively damped by the nanotube resistance.

5.4 Equivalent Circuit Parameters for a Bundle of SWCNTs

A CNT-bundle interconnect is assumed to be composed of hexagonally packed identical metallic single-walled carbon nanotubes. Each CNT is surrounded by six immediate neighbours, their centres uniformly separated by a distance‘s’. The densely packed structure shown in Fig. 5.6, will lead to best interconnect performance.

The expressions to calculate the number of CNTs in the bundle are shown in following equations where n_H is the number of “rows” in the interconnect bundle, n_W is the number of “columns” n_{CNT} is the total number of CNTs and denotes the largest integer less than or equal to ‘y’.

Number of rows in interconnect bundle is given by

$$n_w = [\frac{w-d}{s}] \tag{5.11}$$

Number of columns in interconnect bundle is given by

$$n_H = \left[\frac{h-d}{(\sqrt{3}/2)s}\right] + 1 \tag{5.12}$$

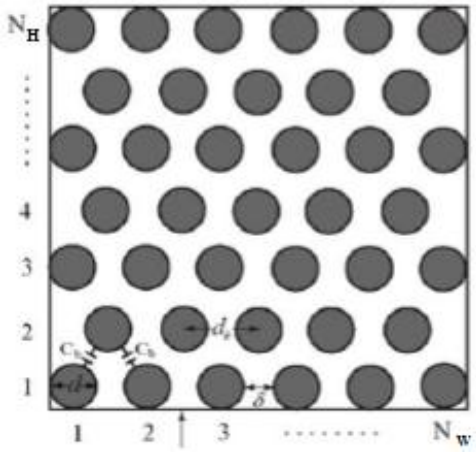


Fig. 5.6 Cross-section of a SWNT bundle interconnects [28]

Therefore number of CNT used in the interconnect bundle is given by the following equation.

If number of rows n_H in the CNT bundle is even, the number of CNT used is given by

$$n_{CNT} = n_w n_H - \frac{n_H}{2} \tag{5.13}$$

If number of rows n_H in the CNT bundle is odd, the number of CNT used is given by

$$n_{CNT} = n_w n_H - \frac{n_H - 1}{2} \tag{5.14}$$

5.4.1 Resistance of CNT bundle:

In order to calculate the effective resistance of a CNT bundle, it is assumed that all CNTs packed into the interconnect structure are metallic and conducting. The CNT-bundle resistance is then given by following Equation, where $R_{isolated}$ is the resistance of an isolated CNT and n_{CNT} is the total number of CNTs forming the bundle.

$$R_{bundle} = \frac{R_{isolated}}{n_{CNT}} \tag{5.15}$$

5.4.2 Capacitance of CNT bundle:

The total electrostatic capacitance of the bundle is given by the sum of the contribution from each of these CNTs.

$$C_E^{bundle} = 2C_{En} + \frac{n_w - 2}{2} C_{Ef} + \frac{3(n_H - 2)}{2} C_{En} \tag{5.16}$$

Where C_{En} and C_{Ef} are the intrinsic plate capacitances calculated for an isolated CNT over a ground plane.

C_{En} is calculated assuming the ground plane to be at a distance equal to the separation distance 's' from the adjacent interconnect.

$$C_{En} = \frac{2\pi\varepsilon}{\ln(s/d)} \tag{5.17}$$

C_{Ef} is calculated assuming the ground plane to be at a distance equal to the separation distance 's+w' from the "far" adjacent interconnect.

$$C_{Ef} = \frac{2\pi\varepsilon}{\ln(\frac{s+w}{d})} \tag{5.18}$$

The effective quantum capacitance of the bundle is the sum of the individual quantum capacitances. C_Q^{CNT} is the quantum capacitance of an isolated CNT and n_{CNT} is the total number of CNTs forming the bundle.

Quantum capacitance of the bundle is given by the following expression:

$$C_Q^{bundle} = C_Q^{CNT} . n_{CNT} \tag{5.19}$$

The effective capacitance (C_{bundle}) of the series combination of a quantum and electrostatic capacitance is given by

$$\frac{1}{C_{bundle}} = \frac{1}{C_Q^{bundle}} + \frac{1}{C_E^{bundle}} \tag{5.20}$$

5.4.3 Inductance of CNT Bundle

The inductance of a CNT bundle is given by the parallel combination of the inductances corresponding to each CNT forming the bundle where LCNT is the (magnetic) inductance of an isolated SWCNT.

$$L_{bundle} = \frac{L_{CNT}}{n_{CNT}} \tag{5.21}$$

CHAPTER 6

REPEATER INSERTION AND VOLTAGE SCALING

6.1 Need of Repeaters

Earlier, interconnect delay and power dissipation were very small and were neglected. Due to recent technological enhancements more number of interconnections have to be used to connect the millions of devices. Thus resistance of the wires increase significantly giving rise to propagation delay and power dissipation.

Interconnects can be modelled as lumped (RC or RLC), distributed, full-wave models, or measured linear sub networks depending on the operating frequency, signal rise times, and the nature of the structure. Initially interconnect circuits were modelled only with RC equivalent circuits and the propagation delay was calculated using a form of Elmore delay [5] through RC, which generally gave good time constant approximation for step responses. But at higher speeds, the electrical length of interconnect becomes a fraction of the operating wavelength, which gives rise to distortion that do not exist at lower frequencies [6]. This made the conventional lumped impedance interconnect models inadequate, and transmission line models such as RLC equivalent models came into effect [7]. An example of such a RC and RLC equivalent model is shown in fig. 6.1 below.

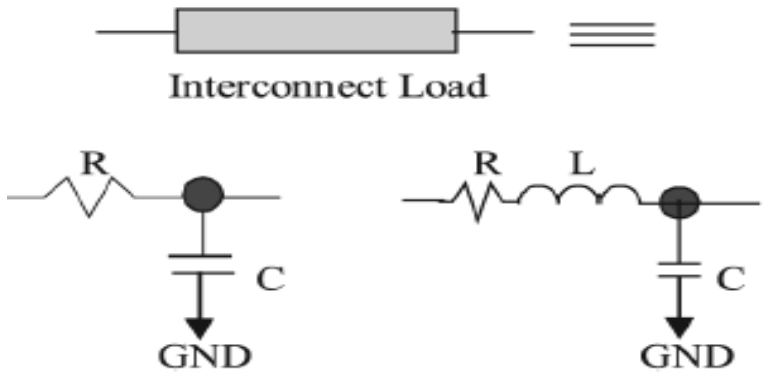


Fig. 6.1 L type lumped model representations of an interconnect line

These RLC values give rise to delay and power dissipation thus degrading the performance of the ICs. To enhance the performance of the ICs, both propagation delay and power dissipation have to be minimised. The increase in load in VLSI circuits due to long interconnect and large fan-outs, emphasize the need for effective driver circuits that can discharge capacitances with sufficient speed. This can be achieved by the insertion of

repeater. Repeaters are used to minimize the overall interconnect response time by reducing the effect of resistance and capacitance. This is discussed in following sections.

6.2 Repeaters

A lot of work has been done regarding Repeaters (inverters). These are the simplest buffers or repeaters in VLSI interconnect circuits. Figure. 6.2 [14] shows a CMOS repeater or buffer driving an interconnect load and its equivalent symbolic representation in the design.

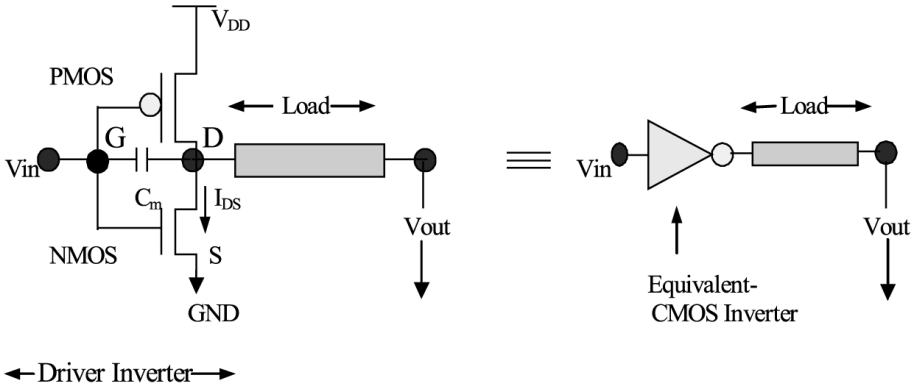


Fig. 6.2 CMOS buffer driving an interconnect load and its equivalent representation[14]

Several methodologies for designing the repeater driven interconnect have been given in the literature. This thesis work deals primarily with the influence of voltage-scaling on the optimum number of repeaters for global interconnects. The insertion of voltage-scaled repeaters in global interconnections have shown significant results in deep submicron technologies, as it leads to a decrease in optimum number of repeaters required to be inserted in a long interconnect for delay and power dissipation minimization. Thus voltage scaled repeaters can enhance the performance of the interconnects largely. Voltage scaling is discussed in the next section.

6.3 Insertion of repeaters in interconnect

Propagation delay of an interconnect is a quadratic function of its length. Thus, if this quadratic nature of interconnect with length is removed the propagation delay of a long wire can be reduced. By subdividing the long wires into small segments and inserting a repeater between every two segments, the propagation delay of the resulting wire

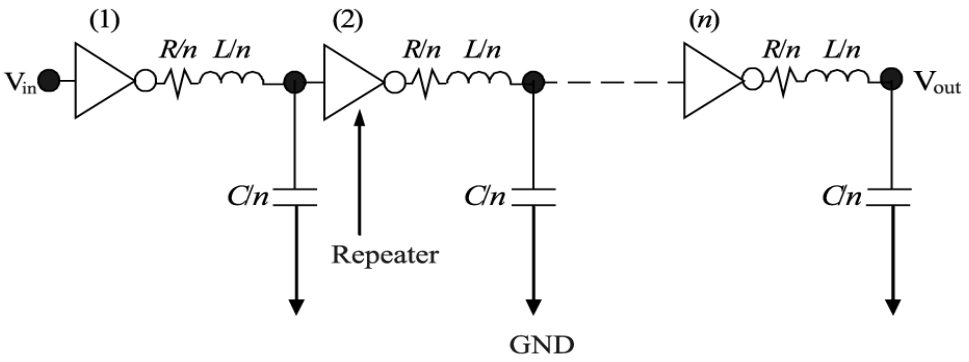


Fig. 6.3 Distributed RC Interconnect with Repeaters inserted in between [47]

becomes a linear function of the number of segments as in Fig. 6.3[47]. Repeaters reduces the interconnect response time by mitigating the effect of capacitance and resistance. This technique is known as repeater (or buffer) insertion.

Meindl *et al.* [48, 49] and Ismail *et al.* [39] have derived various models for delay calculation for repeater inserted RLC interconnect lines. Fig.6.4 [14] below shows N number of repeaters inserted in an interconnect thus dividing it into small subsections.

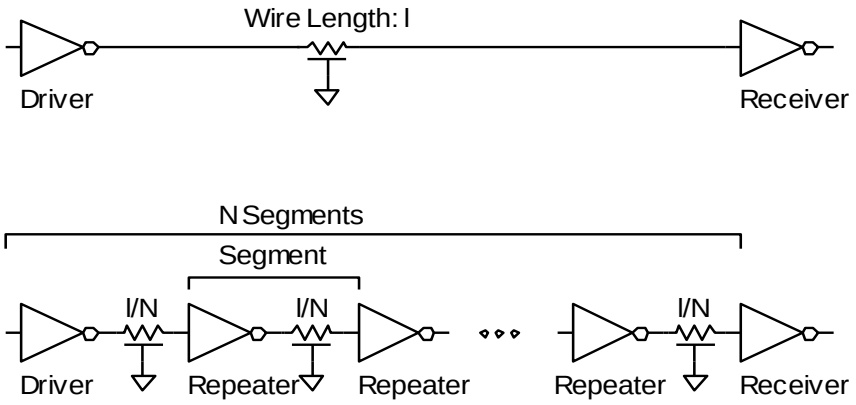


Fig. 6.4 N number of repeaters driving an interconnect divided into subsections [14]

As interconnect is divided into subsections, the total RC time constant is reduced [50, 51]. The additional delay occurring due to the inserted repeaters should be taken into account for the final calculation of the propagation delay. The number of repeaters that can be inserted in an interconnect are limited because at certain point, the sum of the delay caused by the repeaters would become comparable, or may exceed, to the propagation delay of the interconnect.

6.4 Voltage Scaled Repeaters:

Broadly the methodologies for designing the repeater inserted interconnect can be classified as: delay centric and throughput (bits per second) centric. The primary goal of the delay-centric design methodology is to optimize the number and size of the repeaters to achieve minimum propagation delay. In the other method, the optimizations are carried out to get maximum possible throughput. Voltage-scaling now-a-days is considered one of the most effective methods of reducing power dissipation and propagation delay. Deodhar and Davis [52] applied voltage-scaled repeater system methodology with the help of SPICE simulation. Through the simulation results they demonstrated that voltage-scaling could control power dissipation in a repeater inserted interconnect system. But in these simulations they only considered throughput maximisation approach, but didn't considered the effect of voltage scaling on the propagation delay. This thesis work basically deals with the effect of voltage-scaling on propagation delay and power dissipation for long interconnects.

Table 6.1 ITRS 2005 based simulation parameters [3]

Technology Node (nm)		32	32	14
Local and Intermediate	Width W(nm)	32	22	14
	A/R	2	2	2
	ILD Thickness t_{ox} (nm)	54.4	39.6	25.2
	$\rho_{cu}(\mu\Omega\, cm)$	4.83	6.01	8.19
	$C_{cu}(\rho F/m)$	144.93	131.01	111.83
Global	Width W(nm)	48	32	21
	A/R	3	3	3
	ILD Thickness t_{ox} (nm)	110.4	76.8	52.5
	$\rho_{cu}(\mu\Omega\, cm)$	3.52	4.2	5.38
	$C_{cu}(\rho F/m)$	179.78	163.3	139.03
K_{ILD}		2.25	2.05	1.75

The insertion of voltage-scaled repeaters in long interconnections gave favourable results in deep submicron technologies. Use of voltage scaled repeaters leads to a decrease in optimum number of repeaters required to be inserted in a long interconnect for delay minimization, thus minimizing overall propagation delay an power dissipation. Thus,

Voltage-scaled repeaters lead to high-speed low-power VLSI circuits. They also result in saving chip area along with power saving.

Spice simulation tool is used to show the effect of voltage scaling on delay and power. Various simulation parameters used are tabulated in Table 6.1 above. The aspect ratio (A/R) for global level interconnects in ITRS is in the range of 2.5-2.8. For convenience, we have used aspect ratio (A/R) =3.

CHAPTER 7

SIMULATION RESULT AND DISCUSSION

7.1 Introduction

From the equations for RLC explained in previous chapters the equivalent resistance, capacitance and inductance of Copper and CNT bundle is determined. Variation in resistance, capacitance and inductance of interconnect is observed with change in technology node and number of repeaters which is shown with the help of graphs and tables.

7.2 Parameters used for calculation

Table 7.1 gives the values of parameters used for the simulation and calculation purpose.

Table 7.1 ITRS 2005 based parameters for calculation [3]

Parameters	**CNT/Copper**	
Technology	32 nm	22nm
Length of interconnect1mm	1mm	1mm
Width of interconnect	48 nm	32 nm
Aspect Ratio	3	3
ILD thickness t_{OX}	110.4 nm	76.8 nm
K_{ILD}	2.25	2.05
Diameter	1 nm	1nm
Pitch of interconnect	1 nm	1nm

7.3 Variation in RLC with change in number of repeaters

The change in number of repeaters results in change in RLC parameters also. These variations are described below:

7.3.1 Variation in values of RLC for CNT interconnects:

(a) Variation of Resistance with change in number of repeaters of CNT bundle at 32nm and 22nm technology. Here length of interconnect is 1mm.

Tables 7.2 below gives the comparison between the resistance values for 32 nm and 22 nm for different number of repeaters viz. 2,4,6,8,10,12 for CNT interconnects. As can be seen from the table, the resistance values decrease as the number of repeaters increases.

Table 7.2: Resistance values for CNT

No. of Repeaters	Resistance, k ohm (32)	Resistance, ohm (22 nm)
2	133.69	307
4	80.22	185
6	57.27	132
8	44.56	102
10	36.46	84
12	30.85	71

(b) Variation of Capacitance with change in number of repeaters of CNT bundle at 32nm and 22nm technology.

Table 7.3: Capacitance values for CNT

No. of Repeaters	Capacitance (32 nm), pF		Capacitance (22 nm), pF	
	C_1	C_2	C_1	C_2
2	0.201	1.006	0.141	0.707
4	0.121	0.603	0.085	0.425
6	0.087	0.433	0.061	0.303
8	0.067	0.335	0.047	0.236
10	0.055	0.274	0.039	0.193
12	0.046	0.232	0.033	0.163

(c) Variation of Inductance with change in number of repeaters of CNT bundle at 32nm and 22nm technology.

Table 7.4: Inductance values for CNT in nH

No. of Repeaters	Inductance (32 nm), fH	Inductance (22 nm), fH
2	19.50	41.40
4	11.70	24.84
6	8.36	17.74
8	6.499	13.80
10	5.32	11.29
12	4.497	9.56

Tables 7.3 and 7.4 above gives the comparison between the 32 nm and 22 nm technology for capacitance and inductances with number of repeaters. As can be observed from the observations, values of both capacitance and inductance decrease with the number of repeaters.

7.3.2 Variation in values of RLC in Copper interconnects:

(a) Variation of Resistance with change in number of repeaters of Copper interconnect at 32nm and 22nm technology.

Tables 7.5, 7.6 and 7.7 below gives the comparison between the resistance, capacitance and inductance values, respectively, for 32 nm and 22 nm for different number of repeaters viz. 2,4,6,8,10,12 for copper interconnect. As can be seen from the table, the resistance values decrease as the number of repeaters increases.

Table 7.5: Resistance values for Copper

No. of Repeaters	Resistance, kohm (32 nm)	Resistance, ohm (22 nm)
2	814.8	2187
4	488.89	1312
6	349.20	937
8	271.6	729
10	222.22	596
12	188.03	505

(b) Variation of Capacitance with change in number of repeaters of Copper interconnect at 32nm and 22nm technology.

Table 7.6: Capacitance values for Copper

No. of Repeaters	Capacitance (32 nm), fF		Capacitance (22 nm), fF	
	C_1	C_2	C_1	C_2
2	0.941	4.72	0.788	3.94
4	0.571	2.83	0.473	2.37
6	0.403	2.02	0.338	1.69
8	0.313	1.57	0.263	1.32
10	0.257	1.28	0.215	1.07
12	0.218	1.09	0.182	0.909

(c) Variation of Inductance with change in number of repeaters of Copper interconnect at 32nm and 22nm technology.

Table 7.7: Inductance values for Copper in pH

No. of Repeaters	Inductance (32 nm)	Inductance (22 nm)
2	312.04	325.01
4	187.42	195.00
6	133.73	139.29
8	104.01	108.34
10	85.099	88.64
12	72.011	75.01

7.4 Propagation delay analysis

On the basis of values of RLC of CNT bundle and Copper calculated above. With the help of Spice simulation tool these parasitic values are used as a load to inverter. By performing transient analysis by spice simulation tool at 32nm and 22nm technology at 0.1GHz frequency, delay is determined for bundled CNT and copper interconnect.

7.4.1 Simulation Parameters

The parameters used in simulations are shown in Table 7.8.

Table 7.8 ITRS 2005 based parameters for calculation [3]

Parameters	**CNT/Copper**	
Technology	32 nm	22nm
Length of interconnect1mm	1mm	1mm
Width of interconnect	48 nm	32 nm
Aspect Ratio	3	3
ILD thickness t_{OX}	110.4 nm	76.8
K_{ILD}	2.25	2.05
Diameter	1 nm	1nm
Pitch of interconnect	1 nm	1nm

7.4.2 Delay analysis for Interconnect

The length of interconnect is taken as 1mm. The width of interconnect is taken as 48 nm. Resistance, capacitance and inductance of CNT bundle and copper interconnect is calculated using equations in chapter 5. At these technologies capacitance dominate over resistance. Due to close packing of interconnects, the distance between interconnect reduces and leads to rise in the capacitance. SWCNT can conduct more current densities as compared to copper and SWCNT bundle offer a significant reduction in capacitance.

Table7.9 Propagation delay (ns) between CNT and Copper for 32 nm technology

Repeaters	CNT	Copper
2	2.395	2.781
4	1.675	2.172
6	1.455	1.795
8	1.271	1.445
10	1.215	1.315
12	1.126	1.201

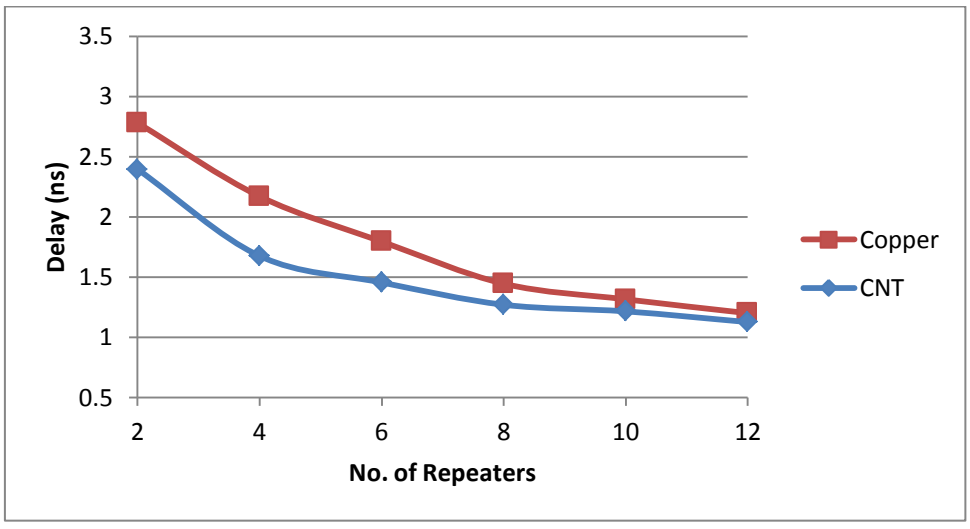


Fig.7.1 Comparison of delay between CNT and Copper for 32nm technology

Propagation Delay in Copper and CNT interconnects for 32nm, 22nm technologies is calculated using SPICE simulation. Simulation is done here for different no. of repeaters

viz. 2, 4, 6, 8, 10, 12. Aspect ratio of the inverters used here in the buffer is 40. Fig. 7.1 and 7.2 gives the comparison of delay between CNT and Copper for 32nm and 22nm technologies respectively with various number of repeaters, viz.2,4,6,8,10,12 with various voltages for varying number of repeaters. The repeater Aspect Ratio has a fixed ratio of 40. Propagation Delay comparison of CNT bundle and Copper interconnects for different number of repeaters is done below and is explained with the help of graphs and tables. It can be observed from the tables 7.9 and 7.10, the propagation delay in case of copper interconnects is more as compared to CNT interconnects.

Table 7.10 Propagation delay (ns) between CNT and Copper for 22 nm technology

Repeaters	CNT	Copper
2	2.341	4.842
4	1.565	3.425
6	1.265	2.635
8	1.131	2.161
10	1.015	1.975
12	0.9695	1.825

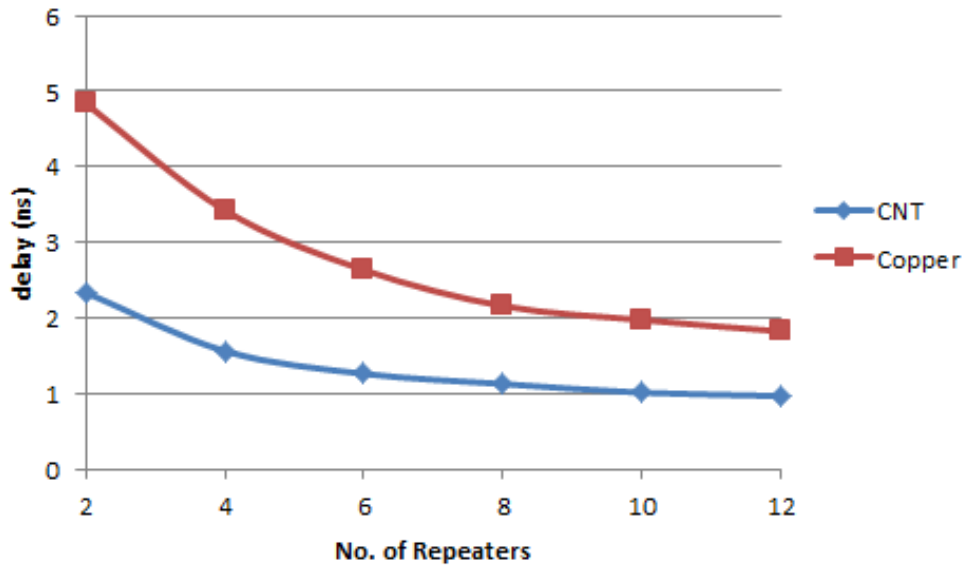


Fig.7.2 Comparison of delay between CNT and Copper for 22 nm technology

It can be seen that propagation delay reduces as we increase the number of repeaters inserted in the interconnect for both CNT and copper.Also from these results we can see that as we keep on increasing the number of repeaters in the interconnect, the difference between the propagation delay for CNT and Copper keep on narrowing.

7.5 Effect of voltage scaling on delay and power dissipation

Here concept of Voltage scaling is used to observe the variation in propagation delay and power dissipation at different no. of repeaters. Tables 7.11 and 7.12 below give the SPICE simulated propagation delay for CNT and Copper Interconnects respectively for 32nm technology. These values are shown graphically in fig.7.3 and 7.4. Here n is number of repeaters inserted in the interconnect.

Table 7.11 Variation of propagation delay with n for different V_{DD} values for 32nm CNT interconnects

n → V_{DD}(V)	2	4	6	8	10	12
0.7	3.281	2.055	1.745	1.711	1.463	1.34
0.8	2.525	1.835	1.532	1.391	1.272	1.23
0.9	2.395	1.675	1.455	1.272	1.215	1.132
1.0	2.305	1.661	1.383	1.245	1.133	1.103
1.1	2.242	1.641	1.381	1.232	1.113	1.056
1.2	2.225	1.612	1.355	1.231	1.124	1.078
1.3	2.241	1.615	1.325	1.205	1.112	1.085
1.4	2.292	1.630	1.365	1.237	1.140	1.081
1.5	2.385	1.645	1.382	1.245	1.143	1.105

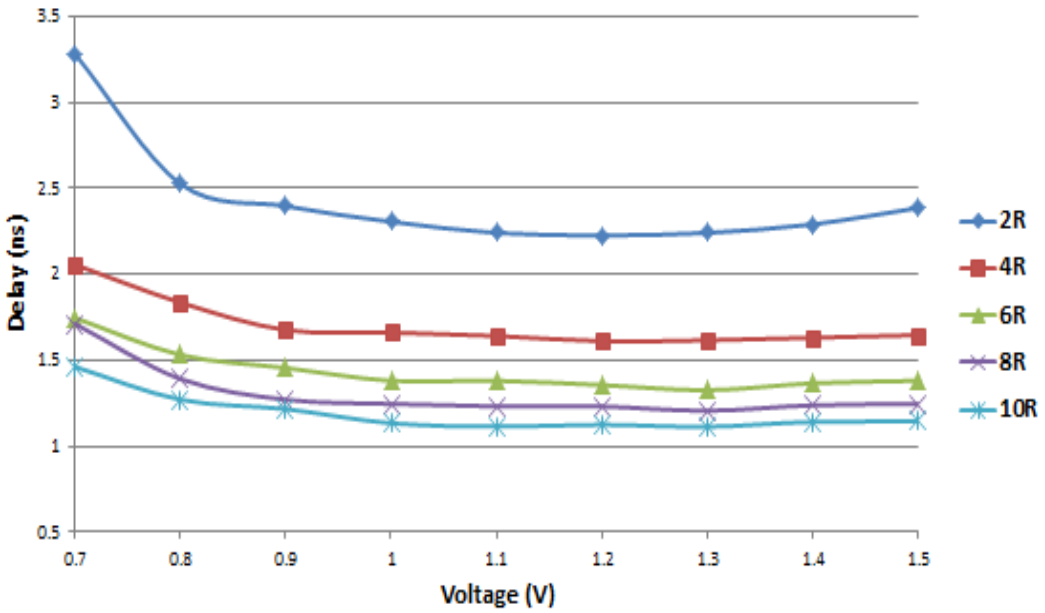


Fig.7.3 Variation of delay with voltage for CNT (32nm)

Table 7.12 Variation of propagation delay with n for different V_{DD} values for 32nm Copper interconnects

n→ V_{DD}(V)	2	4	6	8	10	12
0.7	2.635	1.935	1.665	1.612	1.519	1.425
0.8	2.815	2.125	1.660	1.515	1.408	1.245
0.9	2.781	2.171	1.795	1.445	1.315	1.213
1.0	2.575	1.845	1.631	1.315	1.255	1.165
1.1	2.565	1.821	1.630	1.310	1.213	1.125
1.2	2.751	1.803	1.465	1.300	1.185	1.151
1.3	2.532	1.812	1.505	1.331	1.242	1.115
1.4	2.461	1.825	1.495	1.325	1.241	1.156
1.5	2.605	1.871	1.505	1.345	1.260	1.172

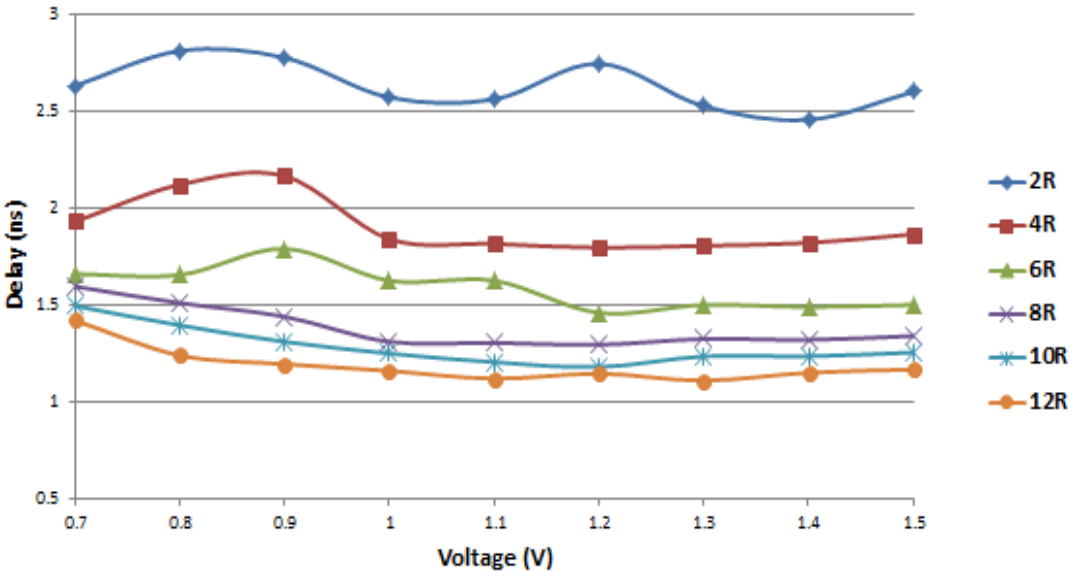


Fig.7.4 Variation of delay with voltage for Copper (32nm)

It can be observed from these tables and graphs that propagation delay reduces with voltage for the same number of repeaters inserted in the interconnects for both copper and CNT. This trend can be observed for both 32nm and 22nm technologies. Thus use of voltage scaling with optimum number of repeaters can enhance the performance of the VLSI circuits.

Tables 7.13 and 7.14 give the SPICE simulated propagation delay for CNT and Copper Interconnects respectively for 22nm technology which is shown graphically in fig. 7.5 and 7.6.

Table 7.13 Variation of propagation delay with n for different V_{DD} values for 22nm CNT interconnects

n → V_{DD}(V)	2	4	6	8	10	12
0.7	2.616	1.765	1.485	1.285	1.205	1.175
0.8	2.451	1.655	1.285	1.176	1.094	1.035
0.9	2.347	1.565	1.265	1.132	1.015	0.969
1.0	2.252	1.501	1.245	1.075	1.023	0.964
1.1	2.231	1.512	1.225	1.069	1.014	0.947
1.2	2.275	1.465	1.215	1.084	1.006	0.939
1.3	2.215	1.501	1.215	1.061	1.007	0.929
1.4	2.295	1.540	1.223	1.086	1.002	0.953
1.5	2.355	1.552	1.251	1.111	1.029	0.971

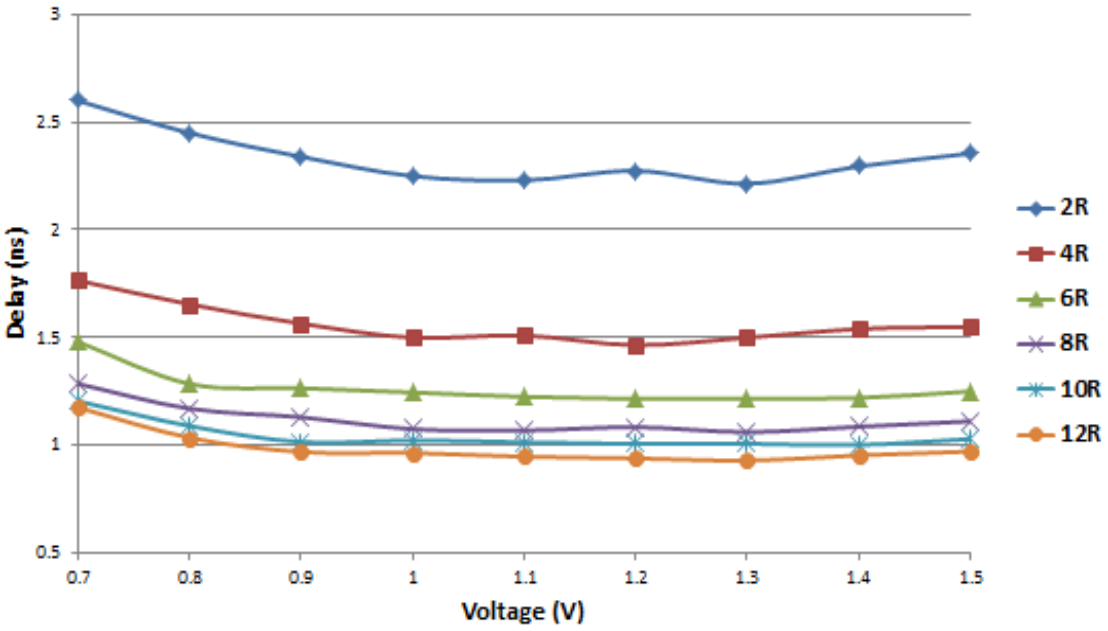


Fig.7.5 Variation of delay with voltage for CNT (22nm)

Table 7.14 Variation of propagation delay with n for different V_{DD} values for 22nm Cu interconnects

n → V_{DD}(V)	2	4	6	8	10	12
0.7	4.851	3.465	2.554	2.255	2.095	1.967
0.8	4.855	3.304	2.715	2.201	2.026	1.905
0.9	4.842	3.425	2.635	2.163	1.975	1.825
1.0	4.821	3.360	2.725	2.141	1.915	1.775
1.1	4.830	3.411	2.771	2.245	1.865	1.713
1.2	4.811	3.375	2.705	2.246	1.941	1.710
1.3	4.825	3.483	2.455	2.245	1.970	1.755
1.4	4.945	3.565	2.681	2.245	1.975	1.805
1.5	4.855	3.695	2.795	2.281	1.991	1.793

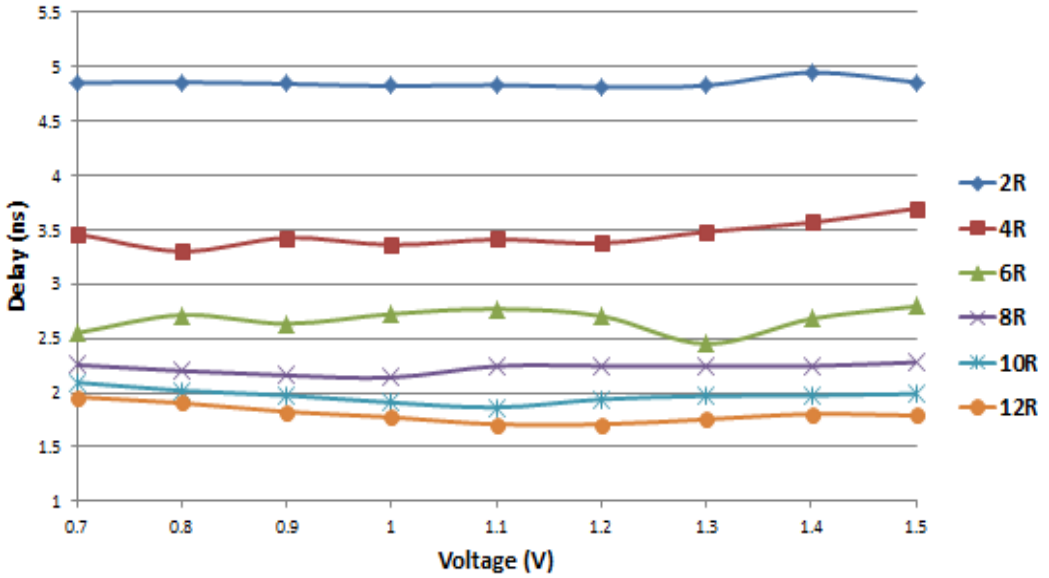


Fig.7.6 Variation of delay with voltage for Copper (22nm)

7.6 Power analysis of Interconnect

The power dissipation in vlsi circuits consists of two components,. static and dynamic. Leakage current of reverse-biased junctions and sub-threshold current accounts for the static power dissipation. Dynamic power dissipation further consist of two parts, first the power consumed by short circuit current and second the power consumed by the transistors during charging and discharging loading capacitors [43].

Charging and discharging power dissipation is proportional to square of supply voltage

and linearly proportional to both loading capacitance and operating frequency. Whereas short circuit power dissipation is proportional to the rise time and fall times of the input signal. So dynamic power is given by the expression,

$$P = C_1 {V_{DD}}^2 f_p \qquad (7.1)$$

Where C_l is load capacitance, V_{DD} is supply and f_p is the operating frequency.

So, dynamic power can be reduced by reducing the value of capacitance C. Therefore at different level, power dissipation of SWCNT bundle and copper interconnect is calculated and compared at different voltages with varying number of repeaters.

Tables 7.15 and 7.16 below give the SPICE simulated power dissipation for CNT and Copper Interconnects respectively for 32nm technology which are shown graphically in fig. 7.7 and 7.8.

Table 7.15 Variation of power dissipation (10^{-4} W) with n for different V_{DD} values for 32nm CNT interconnects

V_{DD}(V)→ ↓ n	0.7	0.8	0.9	1.0	1.1	1.2
2	1.601	2.194	2.928	3.776	4.728	5.768
4	2.088	2.868	3.854	4.974	6.272	7.969
6	2.232	3.045	4.043	5.324	6.896	9.058
8	2.339	3.228	4303	5.667	7.361	10.004
10	2.495	3.509	4.704	6.118	8.074	11.199
12	2.511	3.528	4.766	6.263	8.330	11.846

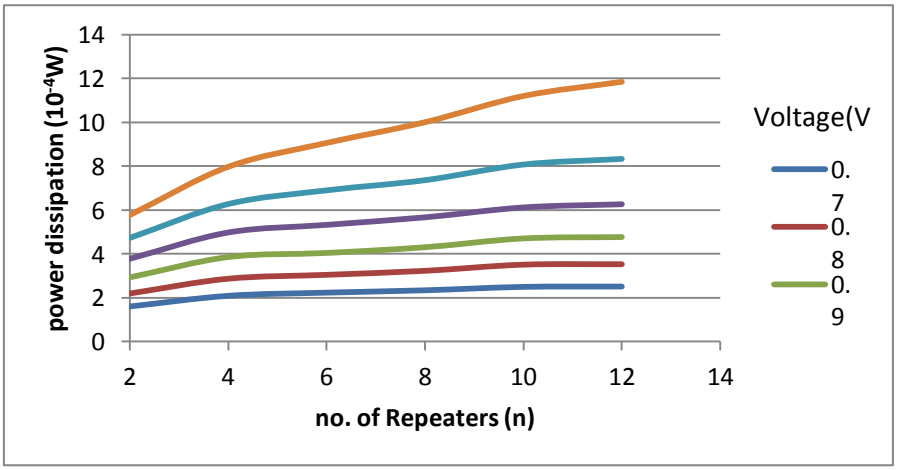


Fig.7.7 Variation of power dissipation (10^{-4} W) with n for different V_{DD} values for 32nm CNT interconnects

Table 7.16 Variation of power dissipation (10^{-4} W) with n for different V_{DD} values for 32nm Copper interconnects

V_{DD}(V)→ ↓ n	0.7	0.8	0.9	1.0	1.1	1.2
2	0.325	0.461	0.646	0.887	1.213	1.636
4	0.481	0.717	1.011	1.404	2.109	2.957
6	0.543	0.984	1.132	1.846	2.623	3.881
8	0.728	1.115	1.551	2.18	3.101	4.825
10	0.854	1.228	1.715	2.428	3.595	5.735
12	0.921	1.343	1.899	2.687	4.052	6.651

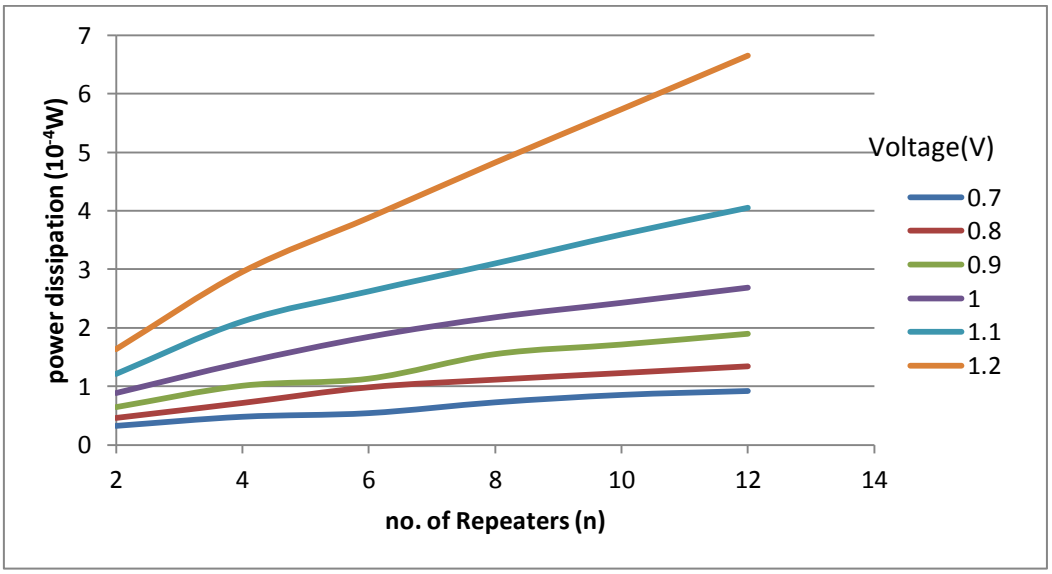


Fig.7.8 Variation of power dissipation (10^{-4} W) with n for different V_{DD} values for 32nm Copper interconnects

It can be seen from this result that as voltage is scaled up, power dissipation increases for the same number of repeaters.

Tables 7.17 and 7.18 below gives the comparison of the SPICE simulated power dissipation for CNT and Copper Interconnects respectively for 22nm technology with number of repeaters, which are shown graphically in fig. 7.9 and 7.10. It is observed that for the same number of repeaters as voltage is increased power dissipation also increases. Also, for same drain voltage as the number of repeaters are increased the power dissipation also increases.

Table 7.17 Variation of power dissipation (10^{-4} W) with n for different V_{DD} values for 22nm CNT interconnects

V_{DD}(V) → ↓n	0.7	0.8	0.9	1.0	1.1	1.2
2	0.862	1.184	1.595	2.056	2.629	3.246
4	1.653	2.201	2.973	3.924	5.035	6.353
6	1.763	2.420	3.197	4.127	5.294	6.826
8	1.816	2.513	3.299	4.317	5.528	7.271
10	1.889	2.587	3.45	4.395	5.798	7.728
12	1.931	2.609	3.532	4.645	5.991	8.221

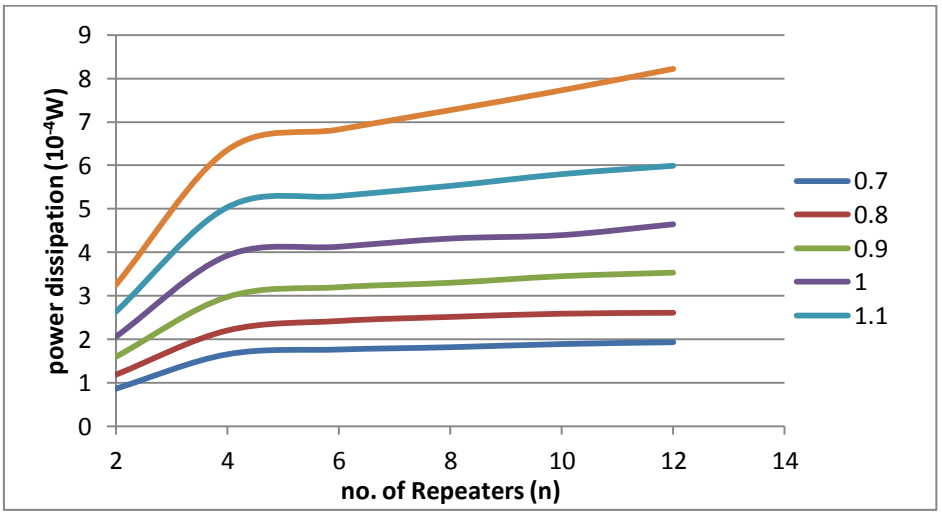


Fig.7.9 Variation of power dissipation (10^{-4} W) with n for different V_{DD} values for 22nm CNT interconnects

Table 7.18 Variation of power dissipation (10^{-4} W) with n for different V_{DD} values for 22nm Copper interconnects

V_{DD}(V) → ↓n	0.7	0.8	0.9	1.0	1.1	1.2
2	0.134	0.207	0.333	0.506	0.713	0.999
4	0.371	0.615	0.792	1.092	1.631	2.158
6	0.463	0.777	0.917	1.355	2.145	2.844
8	0.635	0.881	1.155	1.641	2.422	3.454
10	0.688	0.962	1.281	1.872	2.666	3.877
12	0.731	1.028	1.431	1.979	2.877	8.485

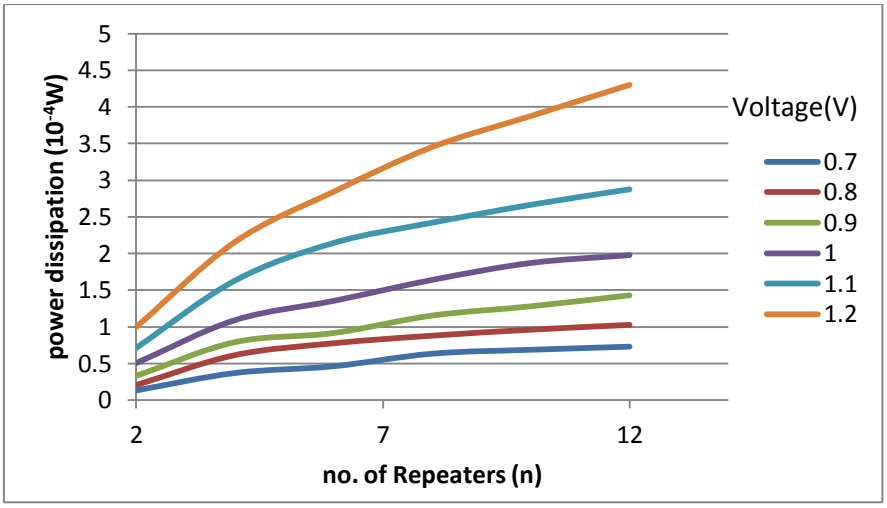


Fig.7.10 Variation of power dissipation (10^{-4} W) with n for different V_{DD} values for 22nm Copper interconnect

It can be observed from these results that the power dissipation reduces significantly with voltage-scaling. However, voltage-scaling leads to higher delay. Thus voltage scaling can be used in accordance with requirement of either low propagation delay or low power dissipation. A trade-off has to be made between propagation delay and power dissipation.

CHAPTER 8

CONCLUSION AND FUTURE SCOPE

8.1 CONCLUSION

The value of various parameters of interconnects viz. resistance, capacitance and inductance have been calculated and compared for different number of repeaters. As number of repeaters increase it is seen that these parameters decrease for both CNT and Copper interconnects.

The delay performance of CNT and Copper interconnects have been compared for various number of repeaters. CNT interconnects show significant improvement in performance as compared to copper interconnects. This is due to the fact that Copper have a resistivity value of double magnitude of that of CNT.

Optimum speed can be achieved with the use of voltage scaled repeaters. It has been observed from results that propagation delay reduces with voltage scaling for same number of repeaters. It has also been observed that lower delay can be achieved with less number of repeaters at high voltage as compared to more number of repeaters at less voltage.

Effect of voltage scaling on power dissipation is observed for both CNT and Copper interconnects for varying number of repeaters. From the simulation results, it has been observed that the power dissipation reduces significantly with voltage-scaling. However, voltage-scaling leads to higher delay. Thus a trade-off has to be made between propagation delay and power dissipation according to the need.

8.2 FUTURE SCOPE

In this thesis, it was seen that single-walled carbon nanotube bundle can be used instead of copper as an interconnect material for the 32nm and 22nm technology. Further, it has been deduced that very less work has been done regarding operating frequency. Effect of operating frequency on speed and power dissipation could be seen. Also, as technology is further being scaled down under 14 nm level, further analysis of RLC parameters, delay and power dissipation can be done.

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