Design and Analysis of All-Digital Flash Analog-to-Digital Converter

A Thesis

Submitted for the Award of the Degree of

Doctor of Philosophy

in

Department of Electronics & Communication Engineering

Submitted by

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August, 2021

CERTIFICATE

I, **Ashima Gupta**, hereby certify that the research work presented in the thesis entitled **"Design and Analysis of All-Digital Flash Analog-to-Digital Converter"** being submitted by me with **Registration No. 901706006** to the Department of Electronics and Communication Engineering, Thapar Institute of Engineering and Technology, Patiala, India in the fulfillment of the requirements for the award of the degree of **"Doctor of Philosophy"**. It is an authentic record of bonafide research work carried out under the guidance and supervision of ***Prof. (Dr). Alpana Agarwal and Asst. Prof. (Dr). Anil Singh, ECED, TIET, Patiala***.

The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

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ACKNOWLEDGEMENTS

First of all, I would like to express my heartfelt gratitude to **Almighty God** for providing me with strength, courage, good health, and the ability to learn understand during the full period of my Ph.D. studies. This work could never have happened without the grace, guidance and blessings of God.

I express my heart full indebtedness and owe a deep sense of gratitude to my respected supervisors ***Dr. Alpana Agarwal***, Professor and ***Dr. Anil Singh***, Assistant professor, Department of Electronics and Communication Engineering, Thapar Institute of Engineering and Technology, Patiala for their sincere expert guidance and support of mentor. It would be impossible to complete my research work without the motivation to do novel work with innovative design ideas. Their experience, knowledge and facility to provide solutions at every stage help me to improve the quality of my research work. I have learned a lot from their passion towards work, problem solving and management skills.

I would also like to acknowledge ***Prof. Prakash Gopalan***, (Director, TIET) and ***Dr. Rafat Siddique*** (Dean of Research and Sponsored Projects) for all research and academic support in TIET and ***Dr. Alpana Agarwal*** (Head of Department, ECED) for constant inspiration and appreciations.

I would like to thanks the ***Council of Scientific and Industrial Research*** (CSIR), New Delhi, India under SRF-Direct scheme with the Award no. File No.09/677(0036)/2018-EMR-I for funding my research work and the ***Ministry of Electronics & Information Technology*** (Meity), GOI through SMDP-VLSI C2SD for providing the necessary research facility and resources.

Also, I would like to thank several international journals for reviewing my research work and providing their valuable comment for improving my thesis work. Once again, I would like to express my sincere gratitude to ***Dr. Alpana Agarwal and Dr. Anil Singh*** for valuable support and supervision regarding manuscripts and research paper. They provide me time to time suggestion to enhance the quality of my research paper and always motivate to do latest research.

I would also like to appreciatively show gratitude to my cherished friends, ***Arvind Thakur and Caffey,*** for technical with other non-technical discussion and offering me advise**.** I will be always indebted to them for bouncing ideas to each other and share a laugh. It has been a wonderful support during Ph.D. work. Our evening snacks time brainstorming sessions were always pleasurable. I also acknowledge the support from SMDP staff, ***Ms. Kiranjit and Ms. Jagdeep,*** for providing tool support and ***Ms. Jaskaranbeer Kaur*** for morale support. I would like to thank ***Naveen, Vidushi, Akanksha*** for their love and support. I would also like to extend my sincere gratitude to ***Dr. Arun Kumar Chatterjee*** and ***Ms. Madhu Kushwaha*** of the Department of Electronics and Communication Engineering, TIET, Patiala, for their moral support, inspiration, guidance and encouragement throughout this Ph.D. journey. Also, I recognized the support from my teachers and friends at TIET for helping me to complete my research work directly or indirectly.

Last but not the least, I would also like to show greatest gratitude to my ***FAMILY*** for every emotional and mental support with encouragement to go ahead. This journey would have not been with the continuous cheer of my parents, ***Mrs. Anju Mahajan and Mr. Anil Kumar***. They have always wanted the best for me and I admire their determination and sacrifice. Also, I would like to thanks my other family members (uncles and aunts), ***Mr. Ashwani, Mrs Rekha, Mr. Ajay, Mrs. Reeta, Mr. Arun and Mrs. Seema and my cousins Dr. Aastha, Abhinav, Ayush, Arunabh, Anshul, Arushikha, Anubhav, Akshita.*** Most of all, I am grateful to my grandfather, ***Sh. Dharam Chand Gupta*** for their teachings, great support and continuous care. My grandfather always encouraged me with two saying, first “Do your duty without thinking about results” and second “Go step by step and say Jai Mata Di”. I am also very thankful to my grandmother (***Smt. Nirmal Gupta***) and my grandparents ***(Nana ji and Nani ji)*** for their love and care.

ASHIMA GUPTA

DEDICATED TO MY

FAMILY

&

FRIENDS

ABSTRACT

With the advancement of the integrated circuit (IC) industry, there is a growing demand for battery-powered and low-power devices for portable applications in consumer electronics, medical science, communication, and automatic vehicles, *etc*. In mixed-signal circuits, analog circuits are about 20% in portion but consume 80% of the design time and effort, and have higher power, process variations and interference, whereas digital circuits are power efficient, robust, and require less design effort; thus, less time-to-market, has less process, voltage and temperature (PVT) variations and scalable. A methodology for designing analog/mixed signal circuits employing digital-in-concept circuits has been proposed in the present work. A flash ADC has been chosen to demonstrate this digital-in-concept circuit design methodology for SoC applications such as autonomous navigation, collision avoidance, distance measuring, and robot ranging sensor. A voltage reference ladder, comparators, and an encoder are the three basic components of a flash ADC. Due to the analog nature of the comparators and voltage reference ladder, which form the basic analog building blocks of the flash ADC, were redesigned using digital-in-concept circuits.

Different versions of digital-based analog comparators (pseudo comparators) have been proposed to operate across the entire input range. The proposed pseudo comparators have a power dissipation ranging from 75 µW to 196 µW, an offset voltage of less than 4.97 mV, a maximum delay of 2.9 ns and a FOM of 1.2 fJ/conv. To test the functionality, some of the proposed comparators have been implemented on FPGA. Further, fully-digital and synthesizable analog comparators have been proposed. The post layout simulations of the proposed synthesizable voltage comparator show offset, delay and power of 0.72 mV, 0.532 ns and 269.8 µW, respectively and the physical layout area is 728 μm^2.

A novel digital-in-concept voltage reference ladder, consisting of a delay-based network and a time-to-voltage converter has been presented. It operates in the range of 0.46 V to 1.8 V with an LSB of about 20 mV and have a negligible process variation in the delay-based network.

The proposed pseudo comparators have been used to implement 4-bit and 5-bit flash ADCs with FOMs of 0.81 pJ/conv. and 0.55 pJ/conv., respectively. The all-digital 6-bit flash ADC has been implemented using the synthesizable comparator and the digital-in-concept voltage

reference ladder in 180 nm 1.8 V CMOS SCL technology. The physical layout of chip's core occupies an area of 534.53 µm × 301.2 µm and is integrated in a 2 mm × 2 mm die. The proposed all-digital 6-bit flash ADC has a FOM of 1.03 pJ/conv. At a sampling frequency of 400 MHz, the proposed ADC consumes 16.6 mW of power. ENOB, SNDR, SNR, and SFDR for this ADC are correspondingly 5.33, 33.8 dB, 35.2 dB, and 39.73 dB. The values of INL and DNL are +0.7/−0.2 LSB and ±0.5 LSB, respectively. Hence, the proposed all-digital flash ADC is suitable for low power and high speed SoC application with reduced design effort time-to-market.

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LIST OF ABBRIVATIONS

ΔΣ	: Sigma-Delta
µOP	: Micro-Operational Amplifier
ADC	: Analog-to-Digital Converters
ADC-I	: 4-bit flash ADC using Pseudo-DVC1
ADC-II	: 4-bit flash ADC using Pseudo-DVC2
ADC-III	: 4-bit flash ADC using Pseudo-DVC3
ADC-IV	: 5-bit flash ADC using Pseudo-DVC3
ADE	: Analog Design Environment
AMD	: Advanced Micro Devices
AOI	: And-Or-Inverter
ASIC	: Application-Specific Integrated Circuit
BUF	: Buffer
CAD	: Computer-Aided Design
CDF	: Cumulative Distribution Function
CML	: Current Mode Logic
CMOS	: Complementary Metal Oxide Semiconductor
CMR	: Common Mode Range
CVTC	: Complementary Voltage-to-Time Converters
DAC	: Digital-to-Analog Converters
DCP	: Dickson Charge Pump
DDPM	: Dyadic Digital Pulse Modulation
DNL	: Differential Non-Linearity
DQOS	: Differential Quasi-One-Junction
DSP	: Digital Signal Processing
DSW	: Differential SQUID Wheel
DTDC	: Double Tail Dynamic Comparator
EDA	: Electronic Design Automation
ENOB	: Effective Number of Bits
FD-DVC4	: Fully-Digital and Scalable Differential Analog Voltage comparator

FDSOI : Fully Depleted Silicon-on-Insulator

FOM : Figure of Merit

FFT : Fast Fourier Transform

FPGAs : Field Programmable Gate Arrays

IC : Integrated Circuit

INL : Integral Non-Linearity

INV : Inverter

ITIQ : Improved Threshold Inverter Quantization

LSB : Least Significant Bit

LTE : Linear Tuneable Transconductance Element

LUT : LookUp Table

MASH : Multi Stage Noise Shaping

MCML : MOS-Based Current Mode Logic

MIMCAP : Metal Insulator Metal Capacitor

MOMCAP : Metal Oxide Metal Capacitor

MOSCAP : MOSFET Capacitor

MOSFET : Metal-Oxide-Semiconductor Field-Effect Transistor

MPG : Multiplexer Pass Gate

MSB : Most Significant Bit

MSO : Mixed Signal Oscilloscope

OAI : Or-And-Inverter

PCM : Pulse-Code Modulation

PIPCAP : Poly Insulator Poly Capacitor

PLA : Programmable Logic Array

PLL : Phase-Lock Loops

Pseudo-DVC : Pseudo Digital-based Differential Voltage Comparator

PSRR : Power Supply Rejection Ratio

PTL : Pass Transistor Logic

PVT : Process-Voltage-Temperature

RF : Radio Frequency

RNS : Remainder Number System

ROM : Read Only Memory

SAR : Successive Approximation Register

SCL : Semi-Conductor Laboratory

SDSW : Symmetric Differential SQUID Wheel

SFDR : Spurious-Free Dynamic Range

SNDR : Signal-to-Noise and Distortion Ratio

SNR : Signal to Noise Ratio

SoC : Systems-on-Chip

SPICE : Simulation Program with Integrated Circuit Emphasis

SPS : Samples Per Second

STDC : Single Tail Dynamic Comparator

Syn-DVC5 : Synthesizable Differential Analog voltage comparator

TC : Time Comparators

TDC : Time-to-Digital Convertor

TDI : Time-Domain Interpolation

TG : Transmission Gate

THD : Total Harmonic Distortion

TIQ : Threshold Inverter Quantization

TMCC : Threshold Modified Comparator Circuit

TVC : Time-to-Voltage Converter

VTC : Voltage-to-Time Converters

VTDC : Voltage-to-Time Difference Converter

WLAN : Wireless Local Area Network

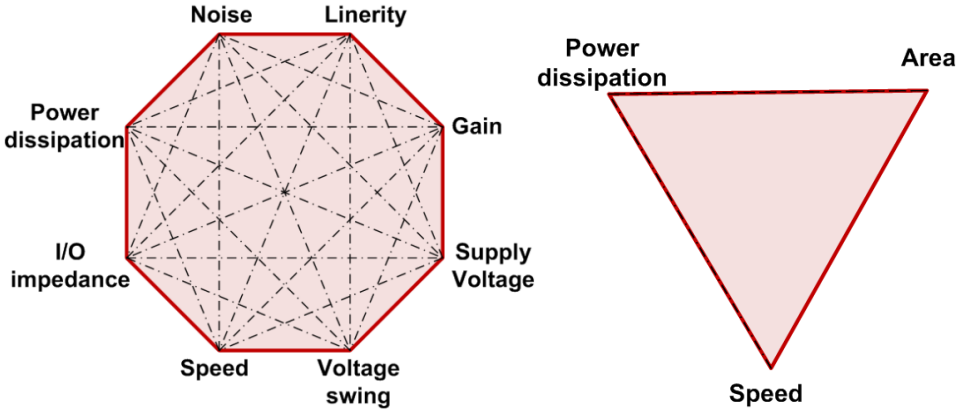
CHAPTER 1

INTRODUCTION

1.1 Introduction

With the growth of the integrated circuit (IC) industry, there is a great interest in battery-operated and low power devices for lightweight/portable applications in the area of customer electronics, medical science, communication, computer system, wireless sensor networks, and automatic vehicles, *etc.* [1-6]. The complementary metal oxide semiconductor (CMOS) IC design is divided into two categories *i.e.,* analog IC design and digital IC design. While designing analog circuits, shown in Figure 1.1 (a), various performance parameters such as supply voltage, input/output impedance, voltage swings, gain, linearity, speed, noise, and power dissipation are analyzed to validate the performance. These circuits are more sensitive to noise, crosstalk and more influenced by second-order effects. In digital circuits, major performance parameters are shown in Figure 1.1 (b), there is typically a trade-off between speed, area and power dissipation.

In the real world, the majority of the signals are analog in nature which is continuous in time and value. The processing of analog signals to extract the information is complex as compared to the processing of digital signals [7]. Moreover, in comparison with analog signals, digital signals are more secure, robust, cost-effective, more immune to electrical noises, easily transmitted over long-range, and easy to store and manipulate, *etc.*



(a) (b)

Figure 1.1 (a) Analog circuit design performance parameters (b) Digital circuit design performance parameters

Hence, digital signal processing (DSP) attains more demand than analog signal processing with the advancement in the IC technology.

In order to take the above advantages, an intermediate system is required which consists of analog-to-digital converter (ADC) and digital-to-analog converter (DAC), to interface the real-world analog signals with the digital processing modules. An ADC converts an analog signal obtained from various sources (such as microphone, ultrasonic sensor, audio and video recorder) into digital information for computing and processing through a digital system. The digital information is transformed back to an analog signal using DAC once it has been processed and is fed to various output sources (such as speaker, voltmeter, display screen). Figure 1.2 shows the entire conversion of signals from real world and back to real world through ADC, DSP system, and DAC. Therefore, ADCs and DACs are used in almost every application such as audio and video processing applications, smartphones, biomedical equipment, digital cameras, and system-on-chip (SoC) applications, *etc.* [8-10]. Figure 1.3 (a) shows ADC with N-bit digital output and Figure 1.3 (b) shows DAC with N-bit digital input and analog output signal.

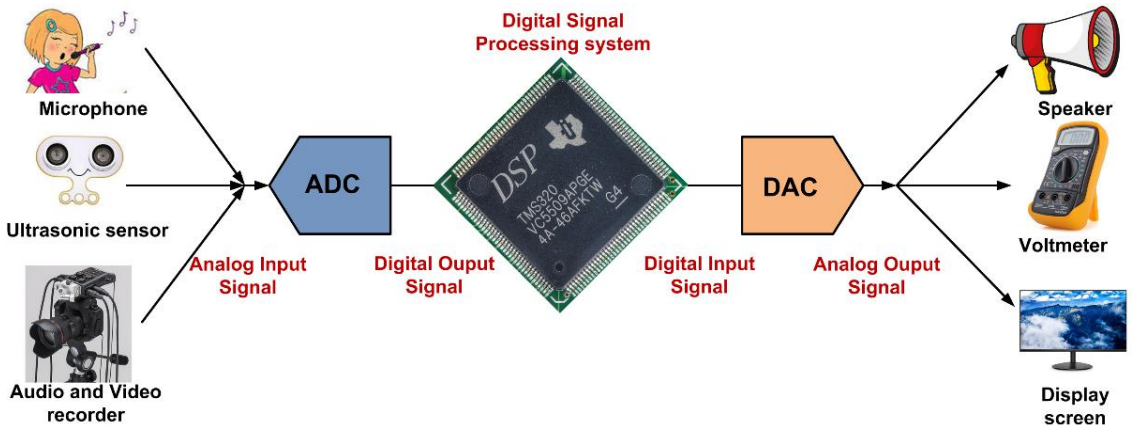
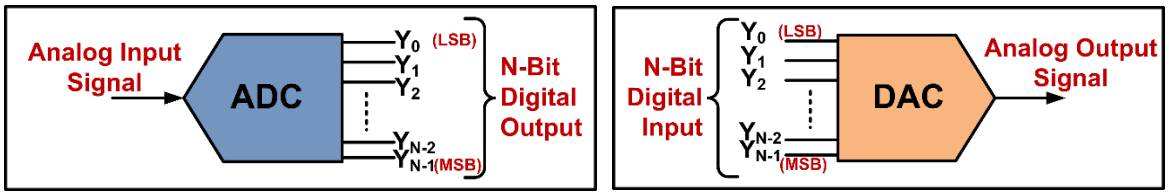


Figure 1.2 Block diagram of communication system



(a) (b)

Figure 1.3 (a) N-bit ADC (b) N-bit DAC

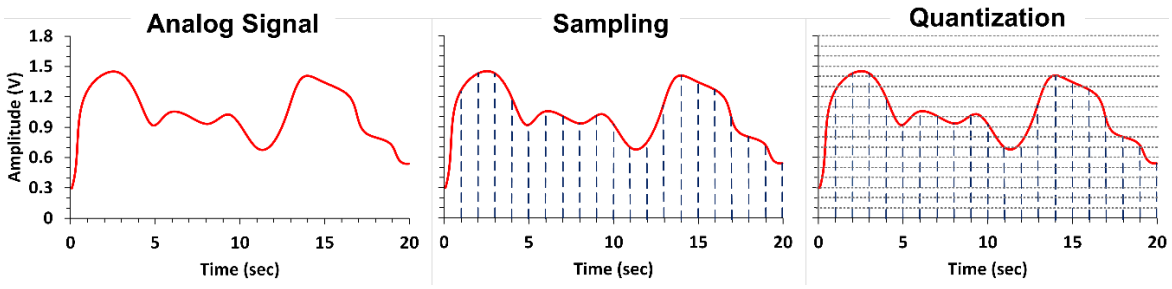


Figure 1.4 Sampling and Quantization [6-7]

An ADC converts the analog signal into discrete-time and discrete-amplitude digital signal through sampling and quantization process, respectively, as shown in Figure 1.4. Sampling divides the continuous signal into a discrete signal in the time domain whereas quantization divides the amplitude at specific discrete levels. Sampling period (T_S) is the uniform gap between the consecutive signals whereas sampling frequency (F_S) is termed asa

$$F_{SP}=\frac{1}{T_{SP}} \tag{1.1}$$

1.2 Parameters of ADC

To define an ADC's overall performance, various performance parameters have been studied in the following section [11-14]. These parameters are majorly divided into two categories such as Static Parameters and Dynamic Parameters.

Figure 1.5 shows the transfer characteristic of a 3-bit ADC whose output is divided into 2^3 (=8) quantization levels.

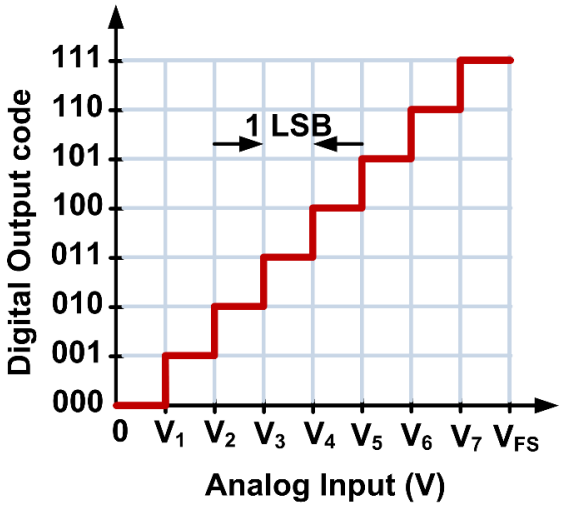


Figure 1.5 Ideal transfer characteristic of 3-bit ADC

A reference voltage is required to digitize the analog signal into small equal quantization levels. In this graph, if the analog input voltage changes by 1 least significant bit (LSB), the output code shifts by 1 bit.

1.2.1 Static Parameters

The static parameters are measured to analyze the device behaviour for DC performance of an ADC which provides accuracy information. Static parameters are calculated by providing a low-frequency ramp signal at the input of an ADC to get the digitized output signal. Quantization error, offset error, gain error, differential non-linearity (DNL) error, and integral non-linearity (INL) error are included in static performance parameters.

1.2.1.1 Quantization Error

The difference between the analog signal and the nearest available digital value at each sampling instant of the ADC is defined as quantization error. If the small input signal change cannot be detected by an ADC, it results in quantization error. Quantization error can be understood through the 3-bit ADC transfer characteristics shown in Figure 1.6. In this graph, when the analog input signal is 0 V, then the digital output produced is '000'. As the analog input voltage rises from 0 V to V_1, the value of quantization error is increased because when input signal is rising, the output signal is still at '000' output code. Again, when input reached V_1, the output code is switched to '001', representing zero quantization error.

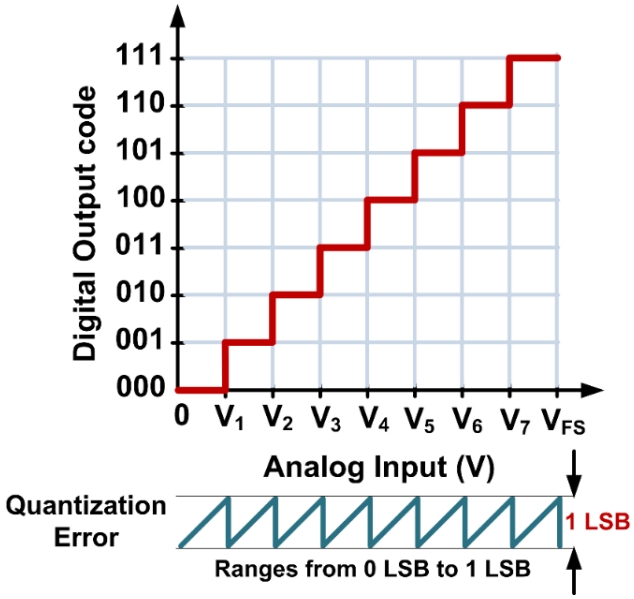


Figure 1.6 Quantization error of ADC

It is observed from graph that the quantization error lies in the range of 0 LSB to 1 LSB. The sawtooth waveform is obtained as error signal, e(t) and q denote the LSB. The root-mean-square (rms) quantization error is written as

$$\text{rms quantization error} = \sqrt{\overline{e^2(t)}} = \frac{q}{\sqrt{12}} \tag{1.2}$$

1.2.1.2 Offset error

The offset error is the difference between the ideal transfer function and the actual transfer function when the 1st output code changes its state, and shown in Figure 1.7. Due to offset error, the complete transfer curve shifts with the same value. The offset error value can be positive as well as negative and calibrated by shifting the actual transfer function to origin (zero point).

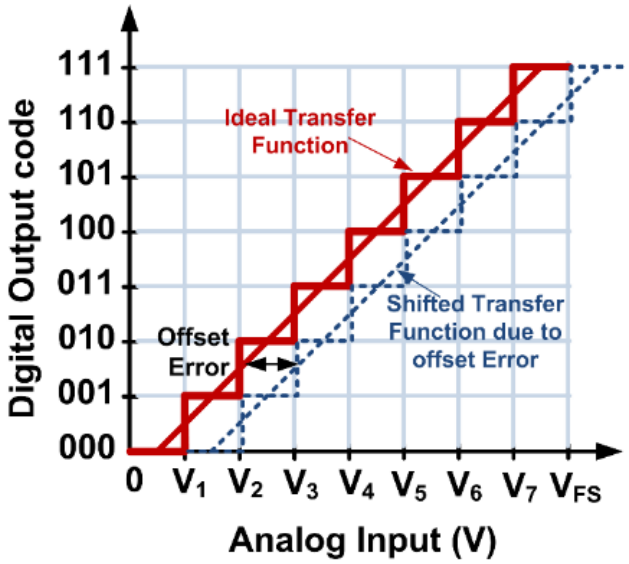


Figure 1.7 Offset error of ADC

1.2.1.3 Gain Error

The gain error is caused by the difference between the slope of the ideal transfer function and the actual transfer function of an ADC. The graph of the gain error is shown in Figure 1.8. If the offset error is removed by shifting the transfer curve to the origin, the gain error is obtained at full-scale value (111). The positive and negative gain error can be calibrated by rotating the transfer function to obtain the ideal value.

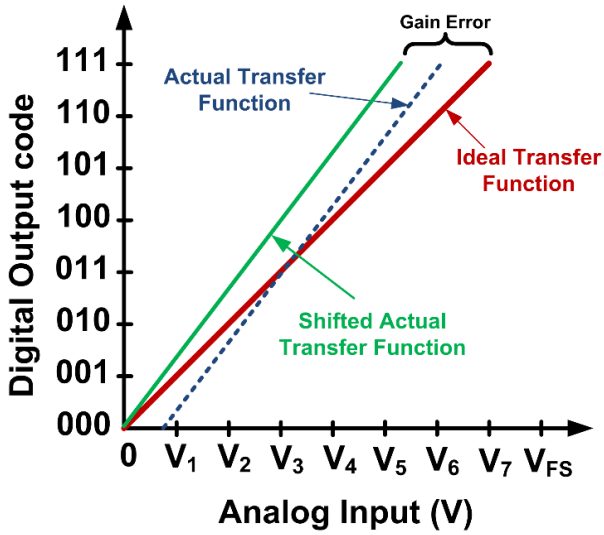


Figure 1.8 Gain error

1.2.1.4 Differential non-linearity (DNL)

The non-linearity error defines the accuracy of an ADC which is calculated after the removal of gain error and offset error. The DNL error is the difference between the ideal quantization step size (*i.e.*, 1 LSB) and actual quantization step size obtained from the transfer function. The equation 1.3 is used to measure the DNL [11]

$$\mathrm{DNL(k)} = \frac{\mathrm{V(k+1)-V(k)}}{\text{Ideal step size}} - 1\mathrm{LSB} \tag{1.3}$$

where k ∈ 0 to 2^N-1 and V(k) belongs to the voltage at k^{th} step in the actual transfer curve. In an ideal case, when the difference between two consecutive steps is 1 LSB then the value of DNL is 0. From Figure 1.9, it is observed that if the actual step size is less than 1 LBS then a negative DNL error is present and if the actual step size is greater than the 1 LSB the positive DNL error is there. The DNL error lies between 0 to 1 LSB assures that there is no missing code with a monotonic transfer function. Non-monotonicity in the transfer function happens if the DNL error is greater than +1 LSB, and a missing code occurs if the DNL error is less than −1 LSB. The positive DNL, negative DNL and missing code errors are shown in Figure 1.9.

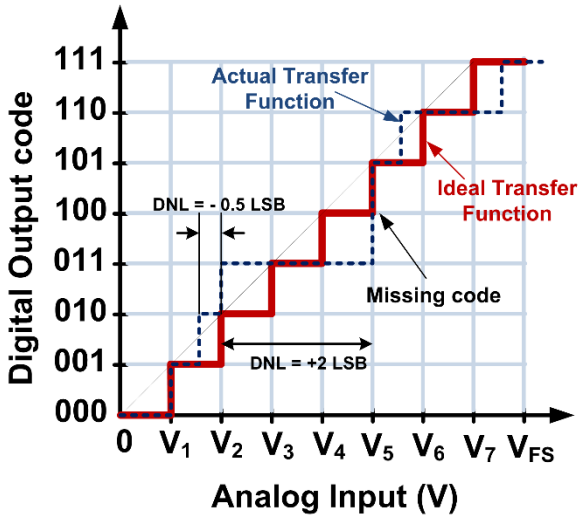


Figure 1.9 Differential non-linearity error

1.2.1.5 Integral non-linearity (INL)

According to the name, the INL error is the summation of all the DNL errors. It is also the maximum difference between the ideal transfer curve and the actual transfer curve. The INL error is defined as

$$\mathrm{INL[k]} = \sum_{i=0}^{k} \mathrm{DNL[i]} \quad (\text{where } k \in 0 \text{ to } 2^N - 1) \tag{1.4}$$

Figure 1.10 shows the graph of INL error where the resulting INL value is also positive and negative LSB. Both INL and DNL are measured in terms of LSB.

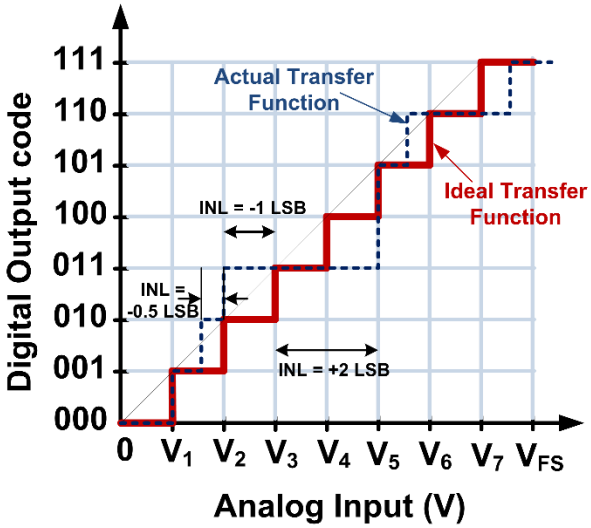


Figure 1.10 Integral non-linearity error

1.2.2 Dynamic Parameters

The dynamic parameters are measured to analyze the AC performance of an ADC, *i.e.*, when the input varies quickly. The high-frequency signal (within bandwidth) is provided at the input of the testing ADC to determine dynamic parameters, and the digitized high-frequency signal is reconstructed at the output of an ADC. The frequency spectrum of this reconstructed signal is extracted from the fast fourier transform (FFT) test. Coherent sampling is used to determine the input frequency of an ADC for FFT test. The rational relationship of coherent sampling is given by

$$F_{in} = \frac{M}{N} \times F_s \tag{1.5}$$

where F_{in} is the input frequency, N is number of FFT point to be power of 2, M is the integer odd prime number to eliminate the common factor with N and F_s is the sampling frequency. The effective number of bits (ENOB), the signal-to-noise ratio (SNR), the spurious-free dynamic range (SFDR), the signal-to-noise and distortion ratio (SNDR), the total harmonic distortion (THD) are included in dynamic performance parameters.

1.2.2.1 Effective number of bits (ENOB)

The ENOB (in bits) defines the effective resolution of an ADC. The ideal resolution of the ADC is disturbed from the actual resolution due to the non-idealities and mismatches present in the circuit. The ENOB is measured at a specific input frequency which must be chosen according to equation 1.5. The ENOB is calculated using the following equation:

$$\text{ENOB (bits)} = \frac{\text{SNDR (dB)} - 1.76}{6.02} \tag{1.6}$$

1.2.2.2 Signal to noise ratio (SNR)

The ratio of the output signal power to the output noise power is known as SNR which does not include any dc or harmonics. The signal power is obtained at the fundamental frequency and noise power includes linearity errors, thermal noise, and clock jitter. The value of SNR should be high for good ADC performance.

The SNR is measured using the following equation:

$$\mathrm{SNR_{max}(dB)} = 6.02 * \mathrm{N} + 1.76 \; = \; 10 \; \log_{10} \left[\frac{\text{Signal power}}{\text{Noise power}}\right] \tag{1.7}$$

where N is ADC resolution.

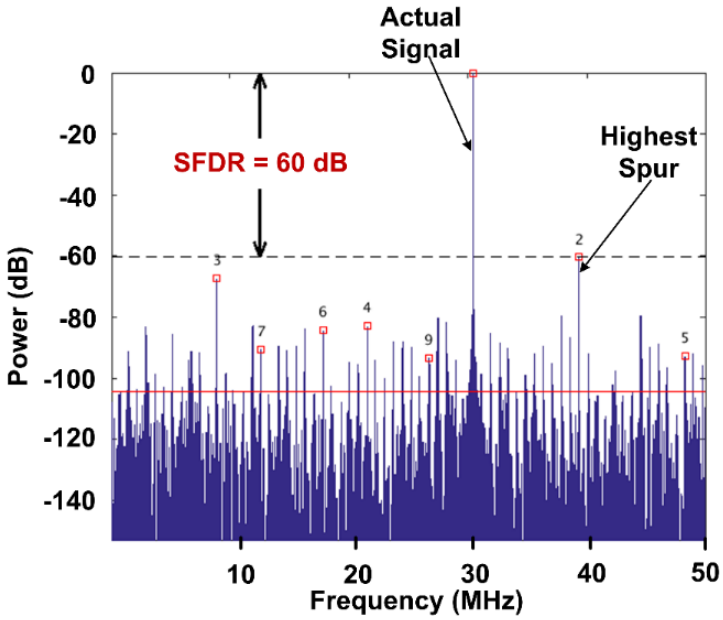


Figure 1.11 Spurious-free dynamic range graph

1.2.2.3 Spurious-free dynamic range (SFDR)

The SFDR is the difference between the value of the fundamental signal power and the strongest spurious signal power. The spurious frequencies are the non-integer multiple of the fundamental frequency, *i.e.*, the unwanted tone present at the output of the ADC. The graph SFDR is shown in Figure 1.11.

1.2.2.4 Signal-to-noise and distortion ratio (SNDR)

The SNDR is the complete dynamic performance parameter to determine the performance of ADC as it includes noise as well as harmonics. It is the ratio of the signal power to the summation of harmonics power and noise power. The equation of SNDR is expressed as:

$$\mathrm{SNDR\ (dB)} = 10 \log_{10} \left[\frac{\text{Signal power}}{\sum_{h=2}^{m} \text{Harmonics power} + \text{Noise power}}\right] \tag{1.8}$$

1.2.2.5 Total harmonic distortion (THD)

THD is defined as the ratio of the sum of harmonics power to the signal power. The harmonics are produced due to the non-idealities present in the circuit. The equation of THD is obtained as:

$$\text{THD (dB)} = 10 \log_{10} \left[\frac{\sum_{h=2}^{m} \text{Harmonics power}}{\text{Signal power}} \right] \quad (1.9)$$

1.2.3 Other performance parameters

Some other parameters that define the performance of an ADC are discussed below.

1.2.3.1 Sampling frequency

The speed of the ADC depends on the sampling frequency which is defined as the rate at which the output digital signal (bits) respond to the input signal changes.

1.2.3.2 Resolution

The resolution is the major design specification for the selection of the ADC. The resolution can be defined as the minimum input difference that can be detected by the ADC and output is changed by 1 LSB (where LSB = $\frac{V_{ref}}{2^N}$ or LSB = $\frac{V_{FS}}{2^N - 1}$ and V_{FS}=V_{ref} -1LSB is the full-scale range of the ADC).

1.2.3.3 Area

The silicon area defines the area of the ADC. Larger the area consumed by any design leads to higher cost. Hence, the requirement of the area is low for every application.

1.2.3.4 Power

The total power consumed by an ADC is known as power consumption. The power consumption of the ADC should be as low as possible for portable, battery-operated devices and other low-power applications.

1.2.3.5 Dynamic range

The ratio of maximum input signal level to the smallest signal level that can be measured is defined as dynamic range.

Dynamic range is expressed as

$$\text{Dynamic Range} = 20 \log_{10}(2^{N} - 1) \tag{1.10}$$

1.2.3.6 Input range

The range for an ADC which converts an input peak-to-peak analog signal into digital bits is known as input range.

1.2.3.7 Temperature range

The range is the variation of the temperature for which an ADC can operate properly. The temperature range is chosen based on military applications and industrial applications.

The performance of ADC would not be complete without analysing the figure-of-merit (FOM). To compare the performance of ADC, FOM [15] is defined as

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} * \text{Sampling Frequency}} \tag{1.11}$$

Based on the above specifications, different ADC architectures have been studied and discussed in the following section.

1.3 ADC Architectures

The different ADC architectures [13-14] have been discussed in this section depending on various performance parameters such as resolution, power, and speed. The high-resolution ADC with low power and high speed is required in nanoscale CMOS technology. The following are the types of ADCs: sigma-delta ($\Delta\sum$) ADC, pipelined ADC, successive approximation register (SAR) ADC and flash ADC architectures.

1.3.1 Sigma-Delta ($\Delta\sum$) ADC Architecture

The $\Delta\sum$ has become an attractive choice for low cost, low speed, low power consumption, and high-resolution applications such as instrumentation, process control, voice band, and audio. Figure 1.12 depicts the block diagram of a $\Delta\sum$ ADC which consists of two blocks *i.e.*, modulator and digital/decimation filter.

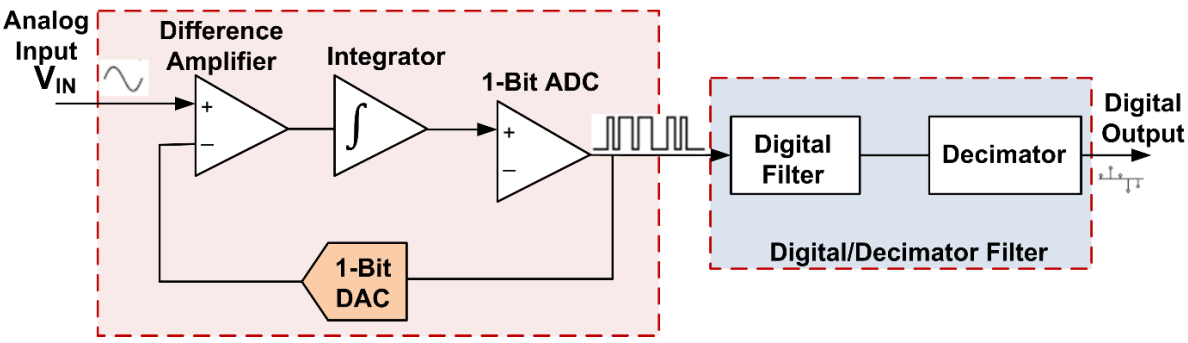


Figure 1.12 Block diagram of ΔΣ ADC

A difference amplifier, an integrator, a 1-bit ADC (comparator), and a 1-bit DAC form a ΔΣ modulator, which is the major building block of ΔΣ ADC. The difference between the analog input and feedback DAC output is measured by difference amplifier. The output of the difference amplifier is fed to the integrator which provides a sloping analog signal. The analog signal is converter to the sequence digital bits through 1-bit ADC. The output of the ADC is given to the digital/decimator filter as well as to the 1-bit DAC through a feedback loop. The modulator block and digital filter are operating at the same frequency. The digital version of data is obtained by digital filter and decimator reduces the digital signal output frequency to Nyquist frequency.

1.3.2 Pipelined ADC Architecture

The pipelined ADC is required in various applications such as ethernet, digital videos, ultrasonic medical sensing, *etc*. The pipelined ADC is an excellent option for high accuracy, low power consumption and high speed with less hardware applications. To enhance the resolution of ADC pipelining is a simple design idea. In this architecture, the number of smaller resolution ADCs are pipelined to realize higher resolution ADC. The block diagram of pipelined ADC is shown in Figure 1.13 which consists of sample and hold circuit, M-bit DAC, M-bit ADC, subtractor, and amplifier (gain stage).

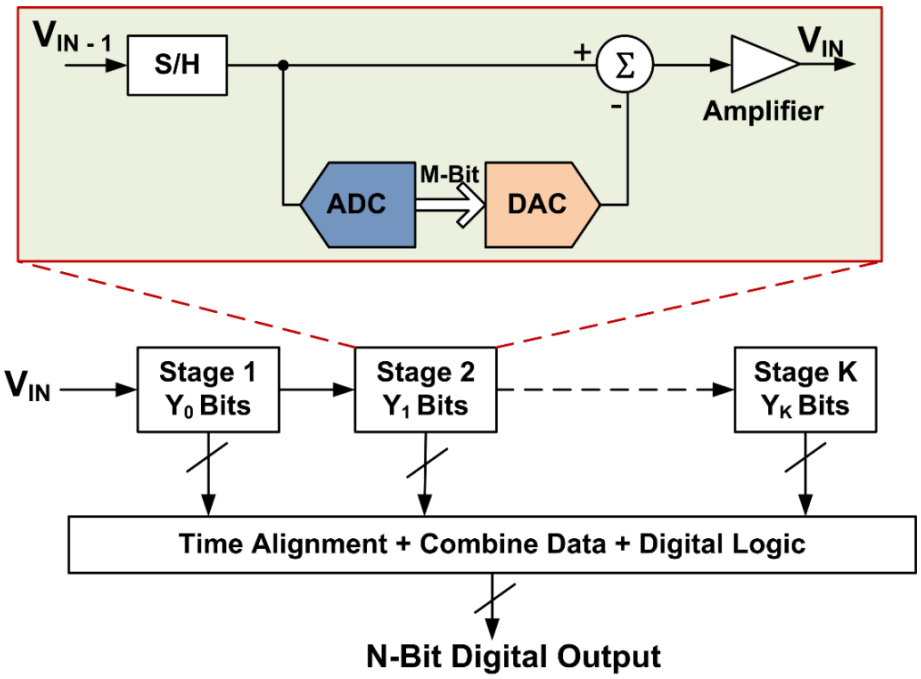


Figure 1.13 Block diagram of Pipelined ADC

A few M-bit ADC are cascaded to achieve N-bit resolution in N-bit pipelined ADC. In this, the sample and hold circuit provides the sampled input to M-bit ADC which provides the digital output. Subsequently, the digital output is given to M-bit DAC to reconstruct the analog signal. The residue signal is generated by subtracting the reconstructed output signal from the input analog signal, which is then amplified to full-scale and fed to the next stage for processing. This process is repeated for the number of instances depending upon the desired resolution. The time alignment and digital logic block combine all the bits obtained from various stages to form N-bit digital output.

1.3.3 Successive Approximation Register (SAR) ADC Architecture

The SAR ADC is the most popular fully integrated solution for moderate-performance systems and its architecture is shown in Figure 1.14. SAR ADC is used in low power and medium speed data converters where medium-to-high resolution is required. It can be used in various applications such as biomedical devices and smartwatches. The SAR ADC consists of successive approximation register control logic, DAC, and comparator. The sampled input voltage is compared with the DAC output through a comparator in an iterative process until both inputs in the comparator are approximately equal.

This comparison has been made through a binary search algorithm using a feedback loop. The full-scale input signal is divided into two parts where the mid voltage is compared with the input signal to see if it is larger or smaller than the input voltage. The comparator outputs a '1' and a '0' depending on whether the input is greater or lesser than the DAC output.

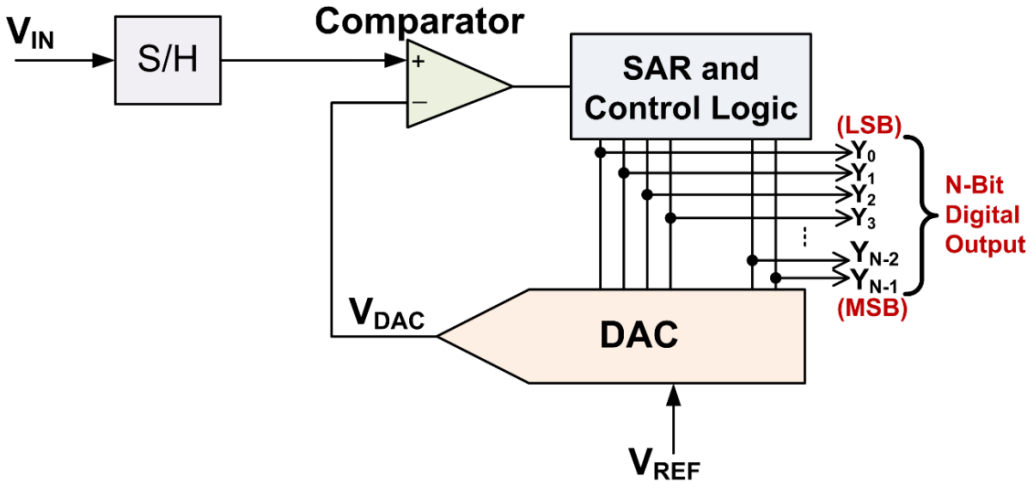


Figure 1.14 Block diagram of SAR ADC

Further, the input full-scale range is reduced according to the comparator output. Again, the new mid-value is compared until all of the bits are determined. Starting with the most significant bit (MSB) and working down to the LSB, each bit is tested through a comparator.

1.3.4 Flash ADC Architecture

With the recent trends in technology, low-power high-speed ADC with large bandwidth and high ENOBs is required. The flash ADC is a good candidate for various applications such as automatic vehicles, high-density disk drivers, and wireless communication. The flash ADC has the simplest architecture comprising a series of resistances to generate the reference voltages for an array of comparators and a thermometer-to-binary encoder. Figure 1.15 shows the block diagram of the flash ADC. A resistive ladder divides the reference voltage into equal levels in a conventional flash ADC. The comparator is the fundamental component of flash ADC that converts the analog signal into a digital signal. Each discrete reference voltage level is compared with the input voltage through the array of the comparators.

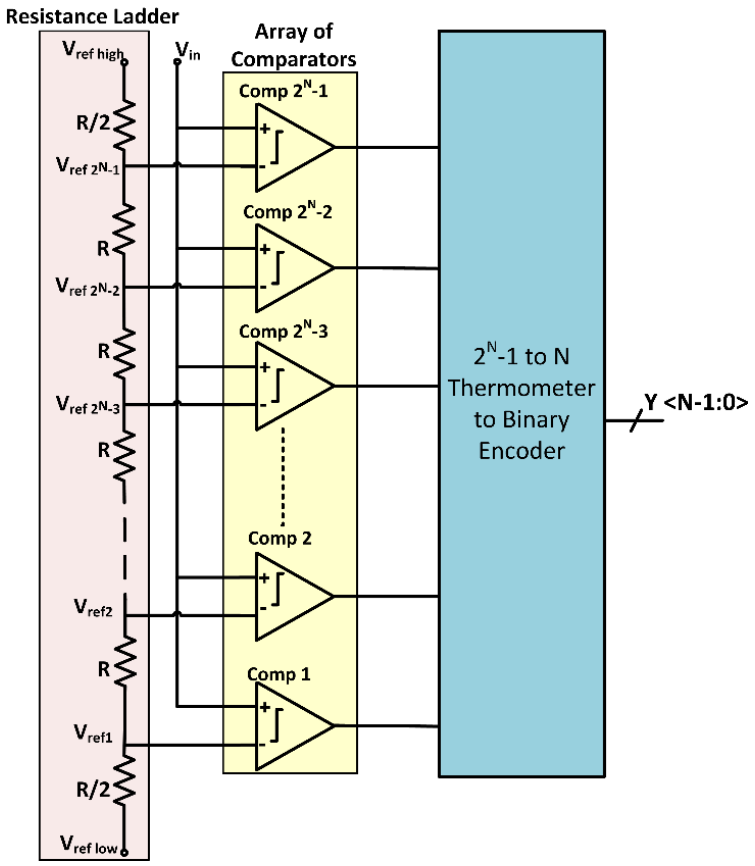


Figure 1.15 Block diagram of Flash ADC

When the input voltage is less than the reference voltage, the comparator produces a logic 'low' output, and when the input voltage is greater than the reference voltage, the comparator produces a logic 'high' output.The digital data obtained from the comparators is known as the thermometer code (consist of series of 1's and 0's). Further, the encoder is used to convert the thermometer code into binary code. For an N-bit flash ADC, 2^N resistances, 2^N-1 comparators, and 2^N-1 to N thermometer to binary encoder are required.

The widespread ADC architectures, which are used in various applications, have been discussed in this section. From this, it can be concluded that the $\Delta\sum$ ADC is developed for high-resolution applications whereas SAR ADC is very useful in low power and low-speed applications. For moderate speed-resolution applications, the pipelined ADC is best suitable. Also, the flash ADC is used for high-speed and low-resolution applications. The trends of resolution versus sampling rate for different types of ADCs along with their applications are shown in Figure 1.16.

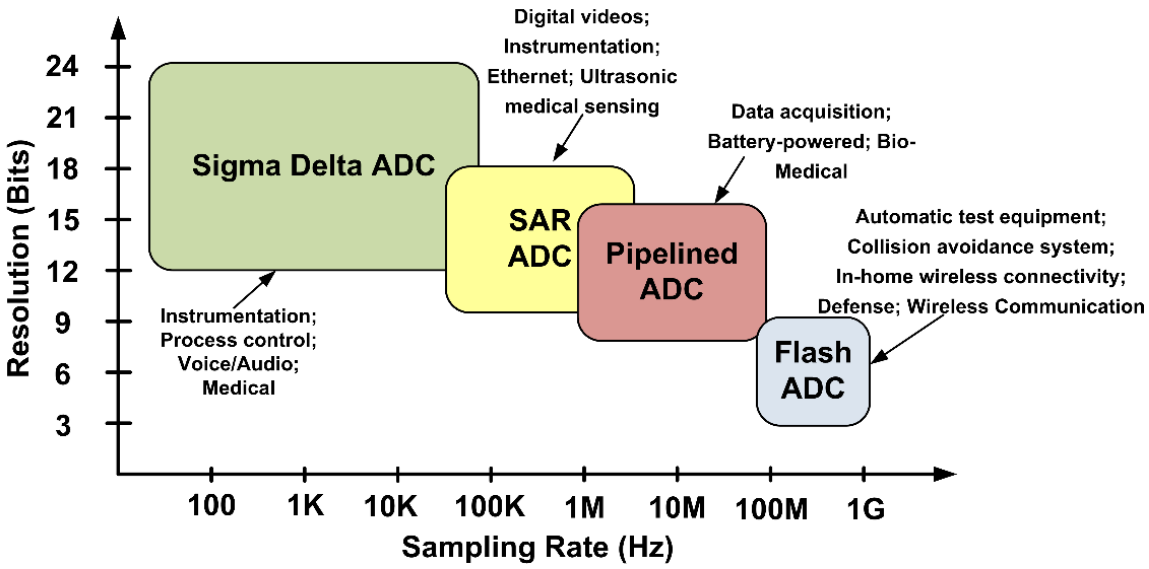


Figure 1.16 Trend of resolution versus sampling rate for various ADCs with applications [12-14]

Table 1.1 Summary of ADC architectures

Architecture	**Sigma-Delta**	**Pipelined**	**SAR**	**Flash**
Resolution (bits)	12-24	8-16	10-18	4-8
Sampling frequency (Hz)	>200 K	1M- 100 M	75 K - 5 M	100M- 1G
Advantages	High bandwidth; High resolution	Low power; Medium speed	High resolution; High accuracy	Extremely Fast; High bandwidth; No latency
Disadvantages	Limited speed; Complex design	Large latency	Limited sampling rate	Large power consumption; Large Area
Applications	Audio; Medical; Instrumentation	Digital videos; Ethernet; Ultrasonic medical sensing	Data acquisition; Battery-powered devices; Bio Medical;	Automatic test equipment; Autonomous navigation; Collision avoidance system; Distance measuring; Robot ranging sensor; Defense; Wireless Communication

All ADC architectures have some trade-off between power consumption, resolution, and speed. Table 1.1 shows the summary of the ADC architecture along with its advantages and disadvantages.

1.4 Motivation

With the fast-changing industrial technology, an ADC that requires less time-to-market and tuneable to various applications is high in demand. Analog designs are made in custom fashion due to which the time required for designing the analog circuit is very high as compared to digital standard cell-based design. In ADC design, the layout of the analog part and the digital part should be kept separate, and also, the additional efforts are required for system integration [16]. Thus, trending research is motivated towards the implementation of the analog circuit through digital design to take all the benefits of digital design methodology. From the above-mentioned analog-based ADC architectures, flash ADC is best suited to reconstruct it into digital form for achieving less time-to-market, high speed with low power consumption, and less design efforts. Also, the impact of process, voltage and temperature (PVT) variations on the digital-based designs is less along with the advantage of scalability.

Also, flash ADC is a favourable choice in applications such as autonomous navigation, distance measuring, robot ranging sensor and collision-avoidance system. These applications require an analog sensor (LV-MaxSonar-EZX) that can detect the distance and convert into voltage. 5-bit to 8-bit resolution is required to measure the accurate distance between two objects. The distance (analog value) is converted into digital bits through ADC for further processing of data. The main focus of this research to design a flash ADC in digital design methodology with low power and large input range. This ADC design development proposal is under consideration in Special Manpower Development Program for Chip to System Design (SMDP-C2SD) project. The desired typical specifications of the flash ADC for low power (*i.e.,* < 20 mW) applications are 200 MHz to 400 MHz sampling frequency with the emphasis on the digital design-based methodology as shown in Table 1.2.

Table 1.2 Required specifications of the flash ADC

Parameters	**Specifications**
Design methodology	Digital design methodology
Architecture	Flash ADC
Technology	SCL 180 nm CMOS
Supply voltage	1.8 V ± 10 %
Resolution	5-bits (min)
INL/DNL	< 0.5 LSB
Sampling rate	200 MHz - 400 MHz
Power	< 20 mW

1.5 Organization of the Thesis

The complete thesis work is divided into following chapters.

Chapter 1 introduces the motivation behind the research topic. After that, the various performance parameters and specifications of ADCs have been discussed briefly. Also, various ADC architectures along with their applications have been discussed in this chapter.

Chapter 2 describes the survey of flash ADC presented in recent literature. Different design architectures of flash ADC have been discussed. Also, the sub-block of the flash ADC *i.e.*, analog voltage comparators implemented with analog/digital concept and encoder are studied. After that, comparison table has been prepared to identify the gaps in the research. From the research gaps, objectives are defined and methodology of the proposed work is explained.

Chapter 3 explains the design of digital-based analog comparators. The simulation results of different proposed analog voltage comparators are analyzed and compared with the existing voltage comparators present in the literature. Three different digital-based analog comparators (Pseudo-DVC1 and Pseudo-DVC2 and Pseudo-DVC3) are discussed and simulation results are further illustrated. Also, it discusses the trade-off between delay, power, and offset for various proposed analog voltage comparators.

Chapter 4 illustrates the design of 4-bit flash ADCs (ADC-I, ADC-II, and ADC-III) using the proposed digital-based analog comparators (Pseudo-DVC1, Pseudo-DVC2 and Pseudo-

DVC3) discussed in chapter 3. The 5-bit flash ADC (ADC-IV) is implemented using the proposed comparator (Pseudo-DVC3). Further, the simulation results to analyze the various performance parameters of flash ADC are shown.

Chapter 5 describes the design of wide input range all-digital 6-bit flash ADC. An all-digital voltage reference ladder has been proposed. Also, the detailed analysis and simulation results of all-digital analog voltage comparators (FD-DVC4 and Syn-DVC5) have been discussed and their simulation results are shown. A complete chip layout of proposed all-digital 6-bit flash ADC is shown and its various results have been analyzed. This chapter has been concluded with a fair comparison on the basis of FOM of the proposed all-digital 6-bit flash ADC with other state-of-the-art work. The trade-off between various performance parameters of flash ADC such as INL/DNL, ENOB, SNDR, SFDR, and SNR are also discussed.

Chapter 6 summarizes and concludes the thesis work. The design methodology and results of the proposed work have been concluded. The future scope of the proposed work is also discussed in this chapter.

CHAPTER 2

LITERATURE SURVEY

2.1 Introduction

Analog circuits and digital circuits are combined on a single semi-conductor die to form a mixed-signal IC such as ADC, DAC or ADPLL, *etc*. In the real environment, mixed-signal ICs are present all over the place such as smart watches, mobile phones, tablets, *etc*. The different types of ADC architectures present in the literature have distinct features and limitations. In the applications such as automatic collision avoidance systems, wireless communication, defense, *etc*., the flash ADC is the chosen architecture. In this chapter, different existing flash-based ADC architectures have been explored to find the gaps.

2.2 Survey of Flash ADC Architectures

The concept of the flash converter was first developed by P. M. Rainey [17]. It was used in electro-mechanical pulse-code modulation (PCM) facsimile system in 1921 and a patent was issued in 1926. Further, Bell labs invented electron beam coding tube which enhances the growth in ADC technology. R. W. Sears [18] described an electron beam coding tube with a 7-bit resolution and 96 kS/s (samples per second) sampling rate. Later in the 1960s, with the advancements in the ADC design technique, the electron tube technology become obsolete. In 1975, the first onboard flash ADC using AM685 comparator was introduced by Computer Labs [14] with a 100 MS/s sampling rate and 4-bit resolution. The TRW LSI division introduced the first IC of the flash converter (TDC1007J) in 1979 with a 30 MS/s sampling rate and 8-bit video resolution [19-20]. Later 6-bit flash ADC (TDC1014J) is also introduced. Also, Advanced Micro Devices (AMD) Inc. developed a 4-bit 100 MS/s flash converter IC (AM6688) in 1979. With the advancements in research, different architectures of the flash ADCs have been proposed using CMOS technology.

S. Sheikha *et al.* [21] presented low signal swing 4-bit 5 GS/s flash ADC for low power and high-speed operations. To minimize the offset effects on the comparator, an offset averaging scheme is applied. Also, the presented flash ADC is immune to the common-mode noise because of its differential nature and low signal swing reduces the noise at a higher frequency. To further enhance the speed of ADC, a 2-stage pipelined encoder is proposed in Ref [22].

In this, current mode logic (CML) is used to implement the encoder for high-speed applications. The thermometer-to-gray and gray-to-binary code converter is used to eliminate the bubble error in 2-stage pipelined encoder.

The MOS-based CML (MCML) approach is used to implement high-speed flash ADC and is proposed by H. Dang *et al.* [23]. In comparison to the conventional latch-based comparator used in the ADC, this MCML based comparator circuit reduces the speed-to-power ratio. As a result, the circuit's power consumption is also less and supply voltage is independent of switching speed.

J. Ceballos *et al.* [24] presented the first novel effective way to eliminate the reference ladder circuit. Due to mismatches in the circuit, the input-referred offset voltage concept has been used as the comparator's reference voltages.

S. C. Hisa *et al.* [25] presented a two-step architecture for 6-bit flash ADC where 6-bit ADC is divided into 4-bit course ADC and 2-bit fine ADC. The 4-bit course ADC uses an array of inverter in place of comparators and the output of this block is further transferred to 2-bit fine ADC which consists of DAC-core and 3 comparators to enhance the resolution. With this approach, high-speed flash ADC is designed with less silicon size and lower power consumption.

S. Park *et al.* [26] proposed a non-interleaved 4-bit 4 GS/s flash ADC with an on-chip inductor. The inductor is used in the comparator core of the ADC to enhance the speed of the design. Also, the area consumed by the inductor is less in comparison with the resistance-based comparator circuit. Two extra laches are introduced after the comparator core to enhance the voltage gain. Further, comparator redundancy and current trimming technique are used in the circuit to reduce the mismatches due to the small size of the transistor.

C. N. Yeh *et al.* [27] have discussed a novel flash ADC architecture with an improved encoder. In this circuit, the conventional 2^N-1 to N encoder is replaced by two parallel $2^{N/2}$-1 to $N/2$ encoder to encode lower and upper bits respectively. Also, the bubble error tolerance is enhanced by using an encoding algorithm. The area, power, and processing time have been reduced with this novel technique.

P. Iyappan *et al.* [28] depicted an architecture of flash ADC using threshold inverter quantization (TIQ) technique where the resistive ladder is removed and the comparator part is implemented using CMOS inverters. The threshold voltages of the CMOS inverters are used as a reference for the ADC. The fat-tree encoder has been employed to enhance the speed of ADC by the factor of 2. The proposed circuit consumes less silicon area and less power. The limitation of this circuit is restricted input range with less resolution.

T Sundström *et al.* [29] have reported an experimental study that utilizes the benefits of the process variations in CMOS circuits to attain high speed and low power ADC designs with less area. In this work, 4-bit flash ADC without voltage reference ladder has been proposed. The inherent mismatches and process variations present in the comparators results in random offset voltage that offset voltage is used as reference voltage levels. The proposed architecture of the flash ADC has a very limited input range *i.e.* 100 mV. This concept of input-referred offset voltage is further used in later research [30-31].

In 2010 S Weaver *et al.* [31] demonstrated the synthesis of a stochastic flash ADC. In this random offset voltage is generated due to process variations and mismatches to set the trip points. This circuit eliminates the reference ladder, but the number of comparators for this architecture is very large, consuming a large area and power consumption.

M. K. Adimulam *et al.* [32] presented a low-power configurable resolution flash ADC which consists of a sub-flash ADC block, comparators, encoder, multiplexer, and biasing block. Depending on the input signal magnitude, the sub-flash ADC block will control different blocks of ADC to achieve the desired resolution. For lowest, medium, and highest magnitude, the 8-bit, 6-bit, and 4-bit modes are selected, respectively. When no input signal is provided to the ADC, it will consume negligible power because of standby mode.

Y. Y Hsieh *et al.* [33] introduced an 8-bit low-power flash ADC. In this architecture, the traditional TIQ based comparator is replaced by a single MOS comparator which comprises of CMOS inverter and resistor. The resistance is connected to the source of NMOS to vary the threshold voltage of the comparator. With this technique, high-speed, high-resolution flash ADC can be achieved with less silicon area.

Y. S. Shu [34] discussed a fully dynamic 6-bit flash ADC which consists of 30 comparators along with 29 SR latches. The dynamic comparator used in this circuit has a built-in feature

of reference voltage generated by 10-bit digital code through the tail-steering array and compared with analog input. The output of two consecutive comparators is fed to SR latches to generate binary bits. Due to the lesser number of comparators, this circuit consumes less area and less power.

O. Aytar *et al.* [35] proposed a 5-bit high-speed flash ADC consists of a resistance array, comparator block, and decoder block. The differential comparator used in this circuit is connected to positive feedback through cross-coupled PMOS transistors to enhance the gain and balance of the output resistance. The encoder block comprises of 1-N decoder block with a fat-tree-based decoder block where a 1-N decoder is designed using a 2:1 multiplexer. The proposed architecture reduces the die area and power consumption.

R. Megha *et al.* [36] overcomes the complexity in multiplexer-based flash ADC architecture, the multiplexers have been incorporated to multiplex the reference voltages. In order to create an N-bit ADC, only N-1 multiplexers and N comparators are used which helps in reduction of comparator. The proposed low-power, high-speed 4-bit flash ADC is suitable for portable electrocardiogram **(**ECG) and wireless applications.

S. Weaver *et al.* [37] presented a synthesizable stochastic flash ADC using digital standard cells. Two cross-coupled 3-input NAND gates are used to implement an analog voltage comparator. The non-linearity of the gaussian offset distribution is corrected by the piecewise-linear inverse Gaussian CDF function which is implemented using HDL language. Also, voltage comparators have been implemented using Verilog code.

X. Yang *et al.* [38] introduced a partially active time-interleaved 6-bit flash ADC architecture which is separated into two sub-blocks: 2-bit course flash ADC and 4-bit fine flash ADC. The sub-block of 4-bit flash ADC is further divided into 4-channel where each channel consists of the sub-ADC block to enhance the speed and source follower-based sample and hold circuit which increases the bandwidth and lessen kickback noise. One channel out of 4 channels is active depending on the output of the 2-bit ADC block. Thus, only the critical comparator close to the input level is active to enhance the power efficiency and reduce the power consumption.

N. Katic *et al.* [39] proposed a time-domain reference ladder using digital gates to implement fully digital flash-ADCs. The voltage-to-time converter (VTC) is used to transform the

analog signal into input digital pulse which is compared with the reference pulses generated by the inverter chain. The proposed circuit is robust, compact and consumes less power consumption but with limited speed and resolution. Also, the limitations of this circuit are timing skew.

A. Fahmy *et al.* [40] presented a programmable and reconfigurable stochastic ADC. The programmability and reconfigurability are archived by dividing the design into 8 banks which contains comparator groups (255 comparators/group), Wallace tree adder, and a block performing inverse gaussian cumulative distribution function (CDF) followed by data combiner. Also, the digital voltage reference generator provides a reference voltage to each comparator group characterized by the 9^{th} comparator bank. Finally, the combiner block is present to combine the output of the 8 channels into one final ADC output. Three different techniques are used to generate the reference voltages at different input ranges and resolutions. To achieve the larger dynamic range, the offset should be large which can be achieved by minimum sized transistors.

O. Aytar [41] presented a common gate differential MOS-based comparator for 5-bit flash ADC. The comparator consists of differential pair based on common gate design and NMOS cross couple transistors and inverters. The output of the comparator block is further fed to the latch block for holding the data and transfer that data to a multiplexer-based (transmission gate (TG) based circuit) 1-N decoder block. The programmable logic array read only memory (PLA-ROM) structure is used to convert 1-N code to binary output. The proposed ADC is good for wide bandwidth and high-speed applications with the limitation of large power consumption.

H. Y. Lee *et al.* [42] introduced a time-domain comparator for high-speed flash ADC. In the proposed differential comparator, the preamplifier stage and source follower are removed to reduce the power consumption of the circuit and SR latch and two inverters are added to the conventional sense amplifier to reduce the kickback noise and to enhance the operating frequency. Also, interpolation used in the ADC reduces the number of comparators by the factor of 2. This time-based ADC is suitable for less area and low power consumption with a high operating speed.

J. Kim *et al.* [43] designed a 7-bit 2 GS/s flash ADC with a lesser number of comparators. The 4X latch interpolation technique is employed in comparator block by cascading two-stage latches. The core area is reduced using this interpolation technique and power consumption is reduced by using a small transistor at the first stage. Also, the foreground calibration is introduced to reduce the PVT variations due to small size transistors.

The novel technique to use a single-bit periodic comparator for multiple-bit flash ADC is proposed by A. Inamdar *et al.* [44] in 2015. Three techniques are used to implement comparators such as differential quasi-one-junction (DQOS), differential and symmetric differential SQUID wheel comparator (DSW and SDSW). DQOS-based comparator is used to implement 4-bit and 8-bit flash ADC and SDWS-based comparator is used to implement 3-bit time-interleaved flash ADC.

Y. Dong *et al.* [45] proposed a multi-stage noise shaping (MASH) continuous-time ADC. In this, two stages are used such as input signal is digitized using first-order front end-stage and quantization noise of course flash ADC is digitized using second-order back end-stage. The discussed high-speed continuous-time ADC consumes large power.

G. Tretter *et al.* [46] introduced an ultra high-speed 3-bit flash ADC which consists of a track-hold stage with buffer and the output of the buffer is provided to comparators followed by amplifier and latches. Further, the output of latches is converted to binary bit through thermometer to binary converter. In the proposed design, small size MOS transistors are used to achieve high speed. The circuit has low power and low cost but it has limited resolution

B. Razavi [47] described an article named “the circuit of all seasons” *i.e.,* flash ADC. In this, two different variants of flash architecture and circuit solutions have been developed to ease the trade-offs in flash stages. With the increase in resolution, the input capacitance of comparators grows exponentially. The “interpolating” flash architecture doubles the resolution without increasing the differential pair-based comparators. Another approach for reducing the power consumption, input capacitance and complexity is “folding”. The complexity is approximately decreased by the factor of 2 as the number of comparators reduces from 2^N to $2^{N/2}+1$.

The time-based 5-bit 5-GS/s flash ADC is presented by C. H. Chan *et al.* [48] in 2017. The proposed time-based flash ADC architecture consists of dual edge VTC, dual-edge clock

buffers, and time comparators (TC) with an on-chip offset calibration scheme. The input signal is sampled and quantized on both the positive and negative edge of the clock cycle to save power by reducing frequency requirements. In addition, the on-chip offset calibration technique is used to reduce mismatches by clock edges and layout routing.

Designing a 5-bit flash ADC in a novel way using standard cells is proposed by S. Khalapure *et al.* [49]. In the proposed circuit, the resistive ladder network is eliminated and comparators are designed using different combinations of digital gates. Each comparator is different from another comparator to generate the specific offset voltage. The 5-input gates have been used to enhance the dynamic range of the comparator but at the cost of a large silicon area and limited resolution. The power consumption of the proposed design is less.

S. M. Mayur *et al.* [50] proposed a standard cell-based low-power flash ADC. The proposed design consists of digital gate-based comparators along with a gain booster circuit and the encoder block. In this circuit, NAND gate-based comparators are used to generate the MSB, and NOR gate-based comparators are used to generate the LSB. Only half comparators are active at a time depending on input signal voltage. If the input signal voltage is more than $VDD/2$ than MSB comparators are active and LSB comparators are in standby mode and vice-versa. The proposed design has less power consumption but the input range and resolution of the ADC are limited.

M. K. Jeon *et al.* [51] proposed stochastic flash ADC with a large number of comparators. The comparators are divided into two groups to enhance the linearity. The proposed design uses a reference swapping technique in which another set of comparators exchanges the reference voltage of one set if the offset voltage is not present in the linear input range. The proposed ADC has a relatively narrow input range at the cost of large number of comparators and higher power consumption.

D. R. Oh *et al.* [52] proposed a complementary VTC (CVTC) for flash ADC. In this initial analog signal is converted to time using CVTC followed by SR-latch and D flip flop that will convert the time information into binary data. The proposed CVTC consists of a NOR-based and NAND-based latch operating in a time-interleaving manner to improve the power efficiency.

S. Zhu *et al.* [53] introduced a novel technique based on the remainder number system (RNS) to propose a time-domain 8-bit flash ADC. It consists of an RNS quantizer, VTC, and time-to-digital converter (TDC). Using this design approach, the input capacitance of the proposed design is less with high input bandwidth. RNS quantizer divided flash quantizer into sub-block to reduce its power consumption and complexity.

A. Bekal *et al.* [54] presented a linear relation between resolution and number of comparators to realize the conversion. To select the reference voltages, it uses the concept of binary search tree algorithm. It required N comparators and N-1 multiplexers for N-bit ADC which help in reducing area and power consumption. The preamplifier is used to minimize the offset voltage at the input side. The sample and hold circuit utilizes clock bootstrapping techniques which allow sampling at peak voltages and helps to minimize charge injection error. Also, off-chip calibration is used to improve the performance of ADC.

J. Liu *et al.* [55] presented a fully synthesized analog bi-quad filter designed with digital standard cells. A NAND/NOR-based micro-operational amplifier (μOP) operating in weak inversion is proposed. As the digital standard cells are available in different sizes, it provides freedom from different application environments. In this, an amplifier is designed which is operated at the low supply voltage hence easily tuneable. A reconfigurable operational amplifier array achieves the large degree of controllability over its bandwidth and gain.

H. Molaei *et al.* [56] introduced a 4-bit and 8-bit hybrid-flash ADC with a smaller number of comparators. To reduce power consumption by reference voltage ladder, analog switches have been used. In the proposed N-bit flash ADC, only N comparators are required. The output of the higher polarity comparator is fed to the lower polarity comparator and soon to achieve the full conversion. Due to this serial data transfer speed of the proposed ADC is reduced but power consumption is highly improved. To achieve high-speed and low-kickback noise, the dynamic comparator is proposed with reduced offset voltage.

M. Damghanian *et al.* [57] proposed a novel technique for reducing the power consumption of 6-bit flash ADC operating at 2.3 GS/s. The proposed ADC consists of folded reference ladder with MCML based comparator followed by the 3-segment encoder. In this, the conventional 2^N- 1 to N encoder is substituted by three $2^{N/3}$- 1 to N/3 encoders which result in higher frequency with less power consumption and area. The complexity of the design is

highly reduced with a lesser number of transistors required. Also, the metastability and bubble error is eliminated using a 3-segment encoder.

G. Prathiba *et al.* [58] implemented a 4-bit flash ADC which consists of improved TIQ (ITIQ) based comparators, bubble error corrector, and multiplexer pass gate (MPG) based encoder. The proposed flash ADC have low power consumption and a smaller number of transistors which is suitable for microwave applications.

S. Mukherjee *et al.* [59] introduced a programable flash ADC consisting of two blocks such as comparator block and encoder block. The threshold modified comparator circuit (TMCC) with double gate MOSFET is introduced to design area optimized, low power, and programmable flash ADC. The ADC's reference voltage is determined by the comparator's built-in threshold voltage. This novel technique helps in achieving high bandwidth and low power consumption for radio frequency (RF) range applications.

A. Bekal *et al.* [60] proposed a 6-bit ADC using binary search SAR ADC and flash ADC. In this design, SAR and flash ADC architecture are merged to achieve high-speed and low-power. The number of comparators is reduced with the help of the logic gates and reused to generate the next bit comparison. Only N number of comparators are required to design N-bit ADC which helps in reducing power consumption and chip area but the speed of the proposed design is less.

K. Ohhata *et al.* [61] proposed a time-based 8-bit ADC architecture that consists of flash ADC and vernier TDC. The proposed design is divided into two parts such as 4-bit flash ADC and 5-bit time-based ADC. The output of interpolated 4-bit flash ADC is fed to the residue generation block. After that residue signals are amplified through a charge steering amplifier and converted to digital bits through the voltage-to-time converter and time-to-digital converter. The flash-based ADC and time-based ADC are pipelined to reduce silicon area and enhance the sampling frequency. This novel architecture has low power and high resolution.

W. El-Halwagy *et al.* [62] time-based reconfigurable ADC based upon Nyquist rate. The complete ADC is divided into subparts such as 4X time-interpolated flash ADC, SAR mode ADC and 2X time-interpolated SAR ADC. The proposed ADC operating for the sampling frequency ranging from 100 MS/s to 5 GS/s and variable resolution ranging from 13-bits to

5-bits. The reconfigurable approach made the proposed ADC suitable for low-power, high resolution, and high speed applications.

A. Zandieh *et al.* [63] proposed a 5-bit flash ADC designed using Si-Ge Bi-CMOS technology. The proposed 2X time-interleaved flash ADC consists of two sub-blocks each with a 5-bit resolution to ehance the sampling frequency by the factor of 2. The power consumption is very less with a very high sampling rate which is suitable for fibreoptics applications

D. R. Oh *et al.* [64] proposed a 6-bit flash ADC using time-domain interpolation which comprises of a resistive ladder, VTCs, time-domain interpolation (TDI) block, and SR latches. To reduce the number of VTC, 8X interpolation has been employed in the TDI block with an offset calibration scheme. The reduced silicon area helps in reducing calibration burden, input capacitance, and power consumption.

P. Mroszczyk *et al.* [65] introduced a TIQ comparator for energy-efficient flash ADC. The advanced body biasing technique has been applied to the comparator to reduce PVT variations and mismatches. The fully depleted silicon-on-insulator (FDSOI) CMOS technology has been used on the comparator to taking the benefits of a broader range of body bias voltage and higher body factor for generating the self-reference voltage. The proposed design is well-suited to for high-speed applications including data acquisition systems and wireless communication.

X. Zou *et al.* [66] proposed a stochastic flash ADC with an inverter-based comparator. Because the stochastic flash ADC contains a large number of comparators, inverter-based comparators have been used to reduce area and power.

A. Amini *et al.* [67] proposed a 6-bit flash ADC with an on-chip bulk-driven based offset calibration technique. The proposed ADC is composed of a resistance array, comparators with offset calibration technique, bubble error detector, and barrel to the binary detector. The offset error is removed through the offset calibration technique which ultimately reduces bubble error. The proposed design has high resolution, high-speed and low power consumption.

M. Zhang *et al.* [68] introduced VTC and TDC-based two-step 13-bit 20 MS/s SAR ADC. The time-domain and voltage-domain techniques have been merged to achieve low-power

and high speed. This circuit is more prone to PVT variations because of the inherent features of TDC.

A time-domain 5-bit flash ADC is presented by Y. C. Lin *et al.* [69] consists of a voltage-to-time difference converter (VTDC), flash-based TDC, and error correction code converter. The input analog signal is converted to a time signal through VTDC and the obtained time signal is converted to digital bits through TDC and code converter. This proposed highly digital circuit is suitable for low power and high speed applications.

A. Esmailiyan *et al.* [70] proposed a dickson charge pump (DCP) based comparator for time-domain flash ADC. The VTC has been realized using DCP based comparator to convert voltage information to time information. Further, digital gates and latches convert the time information into the digital bit. The almost digital implementation of flash ADC operating at ultra-low voltage consumes very less power at 5 MS/s sampling frequency.

Y. S. Abdalla [71] presented a novel MOS-based flash ADC for various applications such as communication systems, radar, and electronics products, *etc*. The proposed flash ADC composed of five stages such as voltage divider network made up of MOS transistors, binary level generator made up of inverters, one-hot bit generator, pass transistors, and decoder block. The linearity of the proposed ADC is very less because the MOS-based voltage divider is highly sensitive to PVT variations. This circuit achieves low power consumption due to less transistor count.

G. Prathiba *et al.* [72] designed a fault-tolerant low-power flash ADC with a resistive ladder network. It comprises of NOR-based CMOS linear tuneable transconductance element (NOR-LTE) comparator, bubble error corrector, and dynamic priority encoder. The unary output of NOR-LTE is converted to binary output through a priority encoder after bubble error correction. The proposed design improves power supply rejection ratio (PSRR), reduces offset error, and reduces power utilization which is suitable for instrument applications.

O. Aiello *et al.* [73] proposed a voltage and current input-based fully synthesizable SAR ADC. The conventional capacitive DAC has been replaced by the dyadic digital pulse modulation (DDPM) DAC to implement the ADC circuit in digital form in the proposed design. Also, the proposed design contains two passive components that are automatically placed and routed with the help of scripting. This digital-in-concept SAR ADC benefited in

terms of reduced silicon area, less design effort, and voltage scaling.

I-M. Yi *et al.* [74] reported a high-speed 6-bit 6 GS/s flash ADC composed of voltage-domain conversion block, 8X time-domain conversion block, and 6-bit encoder. The proposed design uses 8X time interpolation and reduces dynamic comparators to 10 for 6-it flash ADC. Further to decrease the power, only 2 out of 8 time-domain conversions are selectively active. Large input is used for conversion to improve VTC's linearity, and just the linear input range is used for interpolation. The flash ADC has low power consumption, high linearity, and high speed.

Y. L. Yu *et al.* [75] proposed a two-step ADC with calibration. The proposed structure consists of front-end SAR ADC and back-end time-domain ADC. Digital calibration has been applied to resolves the issues of mismatches and non-linearity present in the circuit. The ADC has low-power consumption and suitable for scaled CMOS technology.

Also, the other conventional state-of-the-art 4-bit and 5-bit flash ADCs are available in the literature. I. S. A Halim *et al.* [76] suggested non-ROM type encoder with an open loop comparator to design a 4-bit 500 MHz flash ADC. S. Banik *et al.* [77] proposed a novel technique to eliminates the need of input common-mode pre-amplifier stage. Y. Z. Lin *et al.* [78] proposed a high-speed flash ADC with offset calibration. Some other design techniques and schemes are also used to enhance the performance of flash ADC such as voltage interpolation based, ratio averaging scheme, digital calibration, offset calibration and time-domain technique, *etc.*, however, these designs consume large power [79-89].

2.3 Survey of Voltage Comparators and Encoders for Flash ADC

The analog comparator is required in almost all types of ADCs, the ADC’s performance is strongly dependent on the comparator’s performance. The key performance parameters of the comparators are delay, resolution, offset, power, and area [90-93]. The comparators are categorized into two types specifically static and dynamic comparators [11, 94]. The static comparator provides the output after some delay when input is given to it. The major problem of the static comparator is low speed as there is no positive feedback present and high-power consumption as it is always on. Also, the static comparator suffers from kickback noise and low input voltage range [94]. The solution to the above limitations can be solved by dynamic comparators. Because the functionality of the dynamic comparator is depending upon the

positive feedback and clock signal which decreases the power and increases the speed. The high-speed single tail dynamic comparator (STDC) has a preamplifier stage and the latch stage. The preamplifier stage amplifies the input difference and the latch stage regenerates the output. The STDC has a large offset, consumes more power, large delay, and high kickback noise [95-96]. Further, double tail dynamic comparator (DTDC) is introduced to reduce power consumption and improve the speed [97]. The DTDC has a separate tail MOSFET to flow the current from both the preamplifier as well as the latch stage. The different design techniques for DTDC were presented in recent literature.

M. B. Guermaz *et al.* [98] proposed a low-power CMOS differential comparator for high-speed applications such as RF WLAN. This comparator uses a two-phases non-overlapping clock based on a switched-capacitor network. The differential clocked comparator comprises an amplification stage and a positive feedback stage. The large MOSFET is included in the amplifier stage and the positive feedback circuit helps in reducing the offset voltage. The buffers present in the circuit increase bandwidth but at the cost of reduced gain. A cascaded amplification stage and latch stage have been used to design a low-power dynamic comparator by M. Hassanpourghadi *et al.* [99]. This circuit reduces the power but at the cost of higher offset voltage and low resolution. L. F. Rahman *et al.* in 2014 [100] presented a dynamic latch comparator without the preamplifier stage to reduce the power. The circuit provides low power and low offset voltage but at the cost of the speed. The dynamic comparator without boosted voltage and less staking of transistors was suggested by S. B. Mashhadi *et al.* [101]. Also, the minimum sized transistor is used in the latch stage to reduce the delay. This circuit achieves a high speed of 2.4 GHz at a low supply voltage of 0.8 V but it consumes large power. A. Khorami *et al.* [102] presented a high-speed two-stage dynamic comparator with limited preamplifier swing to reduce the power consumption. In 2017, A. Khorami [103] suggested a new method to reduce power by more than 50 %. In this circuit, the end of the comparison stage is detected and further, it will off the preamplifier stage to reduce the extra power during latching. V. G. Savani *et al.* [104] introduced an adaptive power control technique for dynamic latched comparator power reduction. The suggested circuit offers large power at a lower operating frequency. P. P. Gandhi *et al.* [105] presented a low offset low power dynamic comparator which consists of differential pair and double tail latched comparator to overcome the limitations of offset and power. The low power

dynamic comparator presented by A. Khorami *et al.* [106] uses a power reduction technique without affecting the offset voltage. In this method, two tail transistors of smaller size are added in the tail current path to achieve lower power with the degradation of the speed (10%). M. A. Dehkordi *et al.* [107] proposed an energy-efficient dynamic comparator in which two transistors are added in the preamplifier stage to reduce the kickback noise. This comparator achieves higher speed; however, it suffers from large power consumption. G. Raut *et al.* [108] proposed a reconfigurable high-resolution dynamic comparator. To decrease the circuit's power, the preamplifier stage is bypassed when input is greater than 0.5 V and input is provided to latch through the analog switch. According to the specific applications, the proposed comparator consumes higher power at low input voltage and low power at higher input voltage. Hence, the overall power consumption of the circuit is high for the full input range of the circuit. Also, there are some other state-of-the-art voltage comparators that show large delay [109], less input range [110-113], and high-power consumption [114]. Finally, it can be concluded that there are different design techniques to reduce the circuit's power. From the above survey, it has been observed that the major power component in the dynamic comparator is the preamplifier stage [90, 101-103, 105-108]. Therefore, the different technique has been applied to the dynamic comparators to reduce power such as bulk driven load [115], charge sharing technique [96, 116], early shutdown and adaptive power control switches [104, 117], *etc*.

The above discussed static and dynamic comparators require more design efforts and also these designs are not scalable to lower technology nodes. Because of these disadvantages, the digital-in-concept analog comparator has efficiently replaced the analog dynamic comparator and overcome its limitations and challenges. The existing digital-based and synthesizable voltage comparators have been explored and discussed further.

P. S. Crovetti [118] proposed a novel low-power digital-based analog differential circuit suitable for scaling. The voltage comparator and an operational amplifier based on differential stage are discussed. S. Weaver *et al.* [37] proposed a replacement of an analog voltage comparator by a digital standard cells-based voltage comparator. A cross couple 3 input NAND gate is used in this design, followed by SR Latch. Using this comparator, a synthesizable stochastic flash ADC is introduced, with a large number of comparators and a smaller input range as compared to conventional flash ADC. The differential input range of

this ADC is 280 mV, and the comparators required are 4^N where N is the resolution of flash ADC leads to large number of comparators.

The other method to solve the limited input common-mode range and for stable operation. A. Fahmy [40] proposed a comparator with three NAND-based latches whereas the upper two NAND latch performs the operation of pseudo-differential comparator and the third latch is for stable operation. The input range of this circuit is 800mV at the supply of 1V (in 130 nm CMOS technology). This ADC consists of a large area because 8 comparator banks are present in the circuit to enhance the linearity range.

The above limitations of synthesizable comparators are solved by O. Aiello *et al.* [16]. NAND3 and NOR3 based circuit is combined to increase the input. As the NOR-based design is compatible with low common-mode range (CMR) values which are close to ground and NAND based design is compatible with high CMR values which are close to VDD. The outputs of 3-input NAND gate-based latch and 3-input NOR gate-based latch are applied to dual input SR-Latch. The input range of this circuit is 700mV at the supply of 0.9 V (in 40nm CMOS technology).

The other hybrid rail-to-rail input common-mode range comparator is given by J. E. Park [119] which uses NAND and NOR-based architecture and 2:1 MUX at the output. The input range detector and V_{DAC} are required to implement the circuit. This input range detector is used to determine which comparator is suitable for the operation. The additional delay is added into the circuit due to extra multiplexing circuitry.

In 2020 X. Zou *et al.* [120] proposed a low voltage low power fully synthesizable dynamic voltage comparator. The and-or-inverter (AOI) and or-and-inverter (OAI) gates based dynamic voltage comparator for the wide common-mode range have been implemented. The merged dynamic voltage comparator which achieves low-power and full rail-to-rail swing for 0.3V, 0.6 V, and 0.9 V supply voltage.

The encoder is another major block for the flash ADC which is used to convert thermometer code [94] to binary coded information. In an ideal condition, the parallel comparators give the output in the sequence of 1's and 0's which is converted into binary code. The different encoders have been implemented for the conversion such as MUX based design, programmable logic array (PLA), read-only-memory (ROM), fat tree encoder, and Wallace

tree encoder, *etc.* [121-122]. The mux-based encoder is designed on the principle of binary search algorithm [123]. The ROM-based encoder comprises of two stages [124-125]. The first stage consists of the NAND gate array used to translate 1 out of 2^N-1 code from thermometer code. The second stage converts 1 out of 2^N-1 code to binary output through the row of ROM. The ROM-based encoder is simple but consumes a large area and power with slow speed. To enhance the speed of the ROM-based encoder, extra circuitry is required which affects the power and increases the complexity of the design [126-127]. For high-speed applications, ROM based encoder is not a good choice for flash ADCs. Fat tree encoder, which is composed of two stages, can also be used. The first stage is employed to convert the thermometer code to one out of N encoding and the second stage is employed to obtain binary code from one out of N coding through the tree of OR gate [128]. The noise immunity is more and static power dissipation is less than ROM-based encoder. On the other hand, the fat-tree encoder is more complex in layout designing. Wallace tree encoder is another good and simple method to obtain binary code from thermometer code. The Wallace tree encoder consists of full adders where 2^N-N-1 full adders are required for the N-bit encoder [129]. It provides the binary output by adding the number of ones in the thermometer code. The Wallace tree encoder has an equal propagation delay because each input bit passes through an equal number of full adders to obtain the binary output. In this encoder, no additional circuitry is required for bubble error correction, unlike the ROM-based and fat-tree encoders required an additional three-input NAND gate array. Also, the first and second order bubble error can be corrected by using the Wallace tree encoder [130]. Further, pipelining has been implemented to enhance the speed of operation. J. M. Mathana *et al.* [131] proposed a high-performance Wallace tree encoder with modified full adder designed using pass transistor logic (PTL). This proposed design is suitable for low power and optimum delay with less complexity.

The comparative analysis of various flash ADC architectures based on the literature survey has been given in Table 2.1.

Table 2.1 Performance comparison of different flash ADC architectures

References	[23]	[25]	[26]	[29]	[31]	[32]			[33]	[34]
Year	2005	2006	2007	2009	2010”	2010			2011	2012
Architecture	Flash	Flash	Flash	Flash	Stochastic Flash	Sub-Flash			Flash	Flash
Technology (nm)	180	350	180	90	180	65	65	65	180	40
Supply Voltage (V)	-	3.3	1.8	1.2	0.9	1	1	1	1.8	1.1
Input Range (Vpp)	460 m	0.5V-1.51V	460 m	-	280 m	-	-	-	-	-
Resolution (bits)	6	6	4	4	6	4	6	8	8	6
Sampling Speed (S/s)	1.25G	100M	4G	1.5G	8M	1.6G	1.6G	1.6G	1.4G	3
ENOB (bits)	5.5	-	3.47	3.69	-	3.6	5.45	7.4	-	-
INL (LSB)	0.27	0.5	0.20	<0.53	1.07	0.28	0.32	0.36	0.55	0.35
DNL (LSB)	0.13	0.5	0.15	<0.38	0.50	0.3	0.36	0.4	0.42	-
SNDR (dB)	37.07	-	36.5	-	33.59	23.4	34.6	46.3	-	36.2
Power Consumption (W)	340m	13.22m	530m	23m	182µ*	15m	36m	48m	0.54m	11m

References	[35]	[36]	[37]	[38]	[41]	[42]	[43]	[45]	[46]	[48]
Year	2013	2014	2014”	2014	2015	2015	2015	2016	2016	2017”
Architecture	Flash	Flash	Stochastic Flash	PA-Flash	Flash	Flash	Flash	1-2 CT MASH	Flash	Time based
Technology (nm)	180	90	90	65	180	65	65	28	28	65
Supply Voltage (V)	1.8	1.2	1.2	-	1.8	1	1.8	1	-	1
Input Range (Vpp)	1	-	280 m	-	-	-	-	-	-	-
Resolution (bits)	5	4	-	6	5	6	8	-	3	5
Sampling Speed (S/s)	1.05G	2G	210M	10G	5G	1.6G	2G	8G	24G	5G
ENOB (bits)	-	-	-	5.4	-	5.58	6.04	-	2.2	4.06
INL (LSB)	0.56	-	-	0.5	0.7	0.41	0.64	-	-	0.79
DNL (LSB)	0.32	-	-	0.8	1.07	0.28	0.58	-	0.85	0.83
SNDR (dB)	-	-	35.8	44.7	-	35.37	38.12	67	17	26.19
Power Consumption (W)	36m	23m	65m	83m	340m	17.3m	20.7m	890m	400m	7.8m

References	[49]	[51]	[52]	[53]	[54]	[57]	[60]	[61]	[62]	[64]
Year	2017”	2017”	2017	2017	2017	2018	2017	2018	2018	2019”
Architecture	Flash	Flash	Flash (VTC)	RNS TD	Flash	Flash	SAR-Flash	Time-based	Time-Domain	Time domain
Technology (nm)	180	65	40	65	0.5	180	180	65	65	65
Supply Voltage (V)	1.8	0.9	0.9	1.2/1.3	2.5	1.2	1.8	1.0	1.2	0.85
Input Range (Vpp)	304 m	-	-	1.2	-	-	-	-	-	800m
Resolution (bits)	5	7	5	8	4	6	6	8	13-5	6
Sampling Speed (S/s)	400M	200M	2.5G	2G	800M	2.3G	110M	900M	100 M-5 G	2.5 G
ENOB (bits)	4.78	6.2	4.86	7.93	3.34	5.94	5.87	-	11.7-4.51	5.33
INL (LSB)	0.218	-	-	0.61	0.40	0.20	0.53/-0.56	0.9	0.73	0.65
DNL (LSB)	0.2.06	-	-	0.14	0.42	0.16	0.47/-0.53	0.7	0.67	0.68
SNDR (dB)	30.56	39	31.02	40.7	25.71	37.52	36.02	41.9	73.6 to 30.3	33.84
Power Consumption (W)	18.62m	63.9m	4.37m	21m	7m	20.56m	0.64m	3.5m	8.4 to 22.3m	7.5m

References	[65]		[67]	[69]	[70]	[71]	[72]	[73]	[74]	[75]
Year	2019		2019	2020”	2020”	2020	2020	2020	2020	2020
Architecture	Flash		Flash	Time-Domain	Time-Domain	Flash	Flash	Digital-SAR	Time-Domain & Flash	SAR+TDC
Technology (nm)	28		180	180	28	130	250	40	65	40
Supply Voltage (V)	0.9		0.6	1.8	0.36	1.2	1.5	1	1	0.9
Input Range (Vpp)	270 m	250 m	-	1	-	242 m	-	1	-	-
Resolution (bits)	4	6	6	5	5	5	4	8	6	12
Sampling Speed (S/s)	5G	3G	2G	400M	5M	0.5G	1.3	2.8K	6G	20M
ENOB (bits)	3.4	5.2	5.06	3.89	4.6	4.6	3.44	6.4	-	11
INL (LSB)	0.07	0.4	-	1.7	1.6	0.45	1.5	2.2	0.55	1.8
DNL (LSB)	0.12	0.5	-	1	1.4	0.26	1	2.3	0.46	0.7
SNDR (dB)	22.5	33.1	32.25	25.2	29.4	28.5	22.5	49.7	31.18	62.8
Power Consumption (W)	0.96m	2.2m	35m	16m	88µ*	3.23m	2.77m	7.3m	15.1m	366 µ*

Note: * Denotes the digital and analog-based flash ADC with the lowest power

” Denotes the digital based flash ADC

Table 2.1 shows the year-wise advancement in the architecture of flash ADC along with various performance parameters. It is concluded that from the year 2005 to 2009, the traditional flash ADC architectures have limited input range (*i.e.*, approximately less than 50 % of the supply voltage) and large power consumption. In 2010 and 2014, the stochastic flash ADCs have been proposed at 180 nm and 90 nm CMOS technology with the sampling rate of 8 MS/s and 210 MS/s, respectively. These stochastic ADCs dissipate large power with a limited input range. In 2015, partially active flash ADC had been proposed to reduce the power. Over the years, various time-based flash ADC architectures had been proposed. After that voltage-to-time converter-based ADC, remainder number system-based ADC, and other hybrid architecture-based flash ADCs came into existence. The power consumed by the stochastic, time-domain, and SAR+TDC flash ADC is in the range of few hundred µW with a limited sampling frequency ranging from 5 MS/s to 20 MS/s.

Table 2.2 The current state-of-art work with desired specifications

References→ Parameters↓	**[29]"**	**[31]"**	**[37]"**	**[40]"**	**[51]"**	**Desired specifications**
Technique	Stochastic	Stochastic / 2-group comparator	Inverse gaussian	8-group comp., inverse gaussian	2-group comp. w ref. swapping	Digital design methodology
Supply voltage (V)	1.2	0.9	1.2	1	0.9	1.8
Tech. (nm)	90	180	90	130	65	180
Resolution	4	6	-	-	7	5-bit (min)
ENOB (bits)	3.69	5.3	5.7	5.2	5.7/ 6.2*	-
Max. Samp. Freq. (MHz)	1500	8	210	320	100	200-400
Power (mW)	23	0.6	34.8	87	33	< 20
SNDR (dB)	23.97	33.5	35.89	32.8	39	-
INL (LSB)	<0.53	-0.99	-	-	-	<0.5
DNL (LSB)	<0.38	-0.76	-	-	-	<0.5
Analog input swing	100 mVpp	280 mVpp	280 mVpp	800 mVpp	440 mVpp	Wide input range
Number of comparators	63	7680	2047	2040	8190	less
FOM (pJ/conv.)	1.2	1.9	3.2	7.3	6.3/ 4.49*	-

The current state-of-the-art work has been shown in Table 2.2, from table it can be observed that J. Ceballos *et al.* presented the first novel way to eliminate the reference ladder circuit and used the concept of input-referred offset voltage due to mismatches in the circuit as the reference voltages for the comparator. This concept of input-referred offset voltage is used in further research work but the number of comparators used in the ADCs are high [29-31, 37]. S. Weaver *et al.* [37] proposed a digital standard cells-based voltage comparator. Using this comparator, a stochastic flash ADC is introduced where the number of comparators is high and the input voltage range is limited. A. Fahmy *et al.* [40] proposed an all-digital wide input range stochastic ADC. The input range of this circuit is more, but the rail-to-rail input swing is not obtained (800 mVpp). Min *et al.* [51] presented a reference swapping technique between two groups of comparators for linearization in stochastic flash ADC. The effective number of bits is improved in this linearization technique, but the input range is still less (440 mVpp).

From the above table, it can be observed that the research is focused on low power, high speed, high resolution, and low area flash ADC by applying different design techniques. The comparative study of flash ADC architecture led to various gaps which are explained in the following section. It is also found that there has been very less attempt so far to design a flash ADC with a fully digital design methodology. Hence, there is a scope of work in designing a flash ADC using the digital circuit design methodology.

2.4 Research Gaps Identified

A lot of research work has been done on flash ADC to optimize its performance in terms of its resolution, area, power, *etc*. The architectures proposed in recent years are studied and the following research gaps are identified:

- Analog voltage comparators are more prone to process and temperature variations.
- With the scaling down of technology, full rail-to-rail input range is difficult to achieve in an analog comparator.
- The power dissipation in analog circuits is more as compared to digital circuits, because of the continuous current flow in analog circuits.
- With technology scaling the digital circuits achieve higher efficiency in terms of area, speed and power density, on the other hand, the analog circuits face problems to keep the same pace. Hence, it is required to re-design analog/mixed-signal circuits through a novice

approach which combat the shortcomings of analog design methodologies discussed in recent literature.

- A resistive ladder network used in the flash ADC consumes a large silicon area and suffers from process variations. Further, the resistive ladder network proves to be a power-hungry block. Therefore, the resistive network can be replaced by an alternative area-power efficient technique.

2.5 Objectives of Proposed Work

From research gaps following objectives are formulated:

- To propose a digital-based analog comparator for flash ADC.
- To propose a flash ADC using digital based analog comparator.
- To analyze the possibility of an all-digital flash ADC and study the trade-offs amongst its various performance parameters.

2.6 Proposed Methodology

To meet the objectives, the following research methodology will be followed:

- To study various architectures of the flash ADC and define the specifications required to design the ADC in 180 nm CMOS technology.
- Analyze the various flash ADC components such as comparators and voltage reference ladder, using digital-in-concept circuit design methodology.
- The various EDA tools like Cadence Virtuoso for schematics and layout, Synopsys Design Compiler for RTL coding and Synopsys VCS for RTL simulations can be used to design a flash ADC.
- Further, a flash ADC using digital design methodology will be proposed using proposed digital-based comparators and voltage reference ladder.
- Cadence Virtuoso Layout XL editor and Synopsys ICC Complier will be used to create the physical layout of the proposed flash ADC. After parasitic extraction with Mentor Graphics Calibre, post-layout simulation will be carried out with the HSpice simulator.
- A mathematical tool such as MATLAB will be used to post process the output data of the flash ADC.

CHAPTER 3

DIGITAL-BASED ANALOG COMPARATOR

3.1 Introduction

With the shrinking in MOS device sizes and rapid growth of technology, there is a demand for the portable, compact, battery-operated, and lightweight devices that consume less area and power. However, with the scaling down of the technology, for a substantial number of CMOS circuits, power dissipation has become a critical design metric. Analog circuits hardly take advantage of technology scaling due to the mismatches and process variations in the small-sized transistors. With the downscaling of the technology and the supply voltage, analog circuits face problems due to PVT variations and various short channel effects. These problems can be minimized using large-sized transistors, but it eventually increases physical area and parasitic capacitances, leading to large power dissipation. Also, the analog circuits suffer from various limitations such as being more prone to PVT variation, noise, lacks flexibility and its time-to-market is very high because of manual designing. On the other hand, digital circuits can be easily shifted to lower technologies, and their integration on the Systems-on-a-Chips (SoCs) is simple as compared to the analog counterpart. Also, the digital designs are power efficient, robust, less prone to noise, require less design efforts hence time-to-market is less, and easily tuneable to lower technologies. Digital designs can be also implemented on field programmable gate arrays (FPGAs) [132]. To process the real-world analog signals, they are first transformed into the digital domain through ADCs because of the various advantages of being in the digital domain. With the latest trends in the market to make things portable, digital IC design has become a favourable choice over analog IC designs. Digital design methodology allows scalability, higher circuit density, auto-placement and routing by computer-aided design (CAD) tools whereas analog designs are complex and take more design efforts, making them costly to achieve the same performance parameters. So, we have to re-design analog circuits in a digital way to take advantage of technology scaling and device mismatches in the field of microelectronics. There are various circuits such as phase-lock loops (PLLs), ADCs, and amplifiers which are close to the digital world to take the advantage of this approach. The comparator is one of the essential building blocks of mixed-signal designs, particularly in ADCs. Hence, there is a need to reconstruct

the analog voltage comparator with a digital approach which can be used in several data converters.

The offset, speed, resolution, and power dissipation are the crucial performance parameters of a comparator. The comparator is working on the basic concept, *i.e.*, reference voltage and input voltage levels are compared and it gives the output in the form of '1' and '0' according to the comparison as shown in Figure 3.1. The positive terminal receives an input voltage (V_{INP}), whereas the negative terminal receives a reference voltage (V_{INN}). The output will be logic '1' or '0', according to the V_{INP} is larger or smaller in value as compared to V_{INN}. Statistically, if $V_{INP} \geq V_{INN}$, V_{OUTP} = '1' and V_{OUTN} = '0' and if $V_{INP} < V_{INN}$, V_{OUTP} = '0' and V_{OUTN} = '1'.

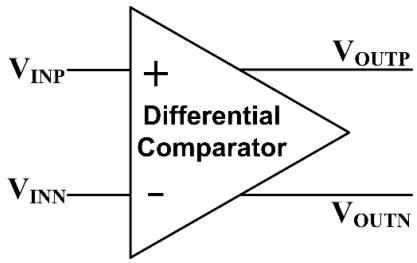


Figure 3.1 Basic block diagram of the differential analog voltage comparator

In this chapter, different digital-based analog voltage comparators (Pseudo-DVC1, Pseudo-DVC2, and Pseudo-DVC3) have been proposed. To verify the performance of the digital-based analog comparators, simulation results and detailed analysis have been shown further. Also, some of the proposed comparators have been implemented on FPGAs to validate the performance on hardware.

3.2 Pseudo Digital-based Differential Analog Voltage Comparator (Pseudo-DVC1)

The circuit of the proposed pseudo digital-based differential analog voltage comparator (Pseudo-DVC1) is shown in Figure 3.2. It depends on the digital-in-concept differential circuit [118] and is composed of standard CMOS-based inverters, NAND and NOR gates. It has a summing logic comprising four resistors of equal values. Summing logic provides the average of the external inputs and a feedback signal (V_f) obtained from the common-mode (CM) extractor (which is stored in a capacitor, C_f). The capacitor (C_f) has been implemented by MOSCAP (MOSFET capacitor) [133-135].

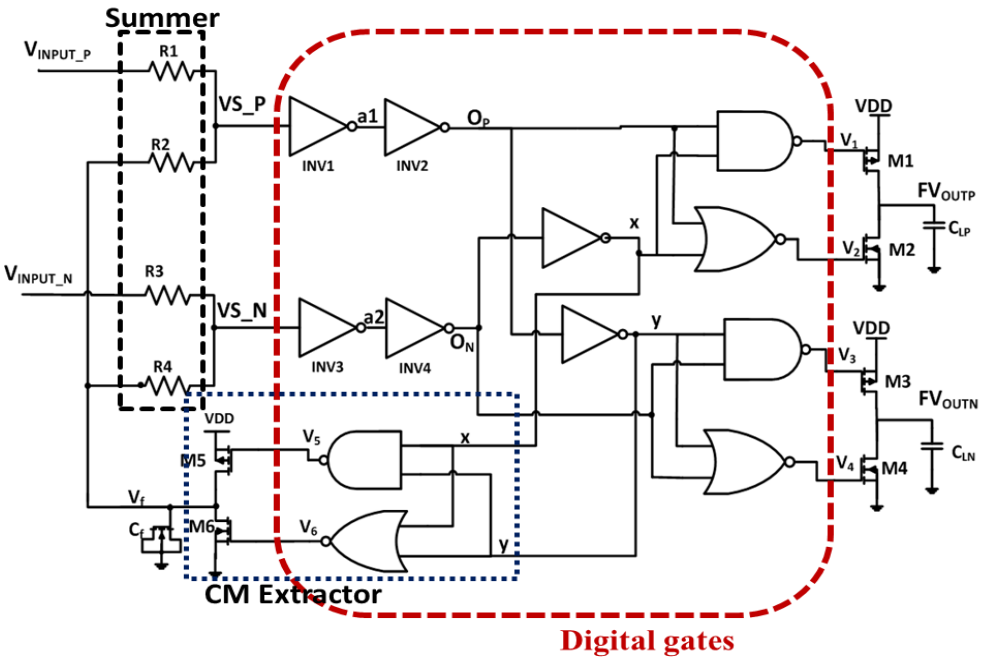


Figure 3.2 Pseudo digital-based differential analog voltage comparator (Pseudo-DVC1)

A MOSCAP requires less area, a lesser number of fabrication mask layers, and offers more capacitive density as compared to other monolithic capacitors such as MIMCAP (metal insulator metal capacitor), MOMCAP (metal oxide metal capacitor) and PIPCAP (poly insulator poly capacitor), *etc.*

The synthesized logic portion of the circuit, *i.e.*, digital gates is the major contributor to the circuit's functionality and power. The complete internal operation of the proposed circuit is described in the following text. An inverter provides a logic high output when a signal less than the switching threshold voltage (V_{th}) is applied at its input and a logic low output when the input voltage is more than V_{th}. Thus, if two inverters with different inputs are taken, input voltage less than V_{th} is applied at one inverter and voltage greater than V_{th} is applied at the other inverter, then the differential output (FV_{OUTP} and FV_{OUTN}) will be 1 and 0. But, in case the input voltages applied at both the inverters are the same, *i.e.*, both voltages are greater than V_{th} or less than V_{th}, the circuit becomes non-responsive to the differential mode component and hence, the outputs are not complementary.

As shown in Figure 3.2, the solution to this deadlock condition is a common mode negative feedback signal (V_f), which is generated with the help of a common-mode extractor block. V_f gets added up with both the input voltages V_{INPUT_N} and V_{INPUT_P} with the help of summing

network which gives the average (if R1=R2=R3=R4=R) of the feedback signal (V_f) and the external inputs. Hence, the outputs of summing network are VS_P $= \frac{V_{INPUT\_P}+V_f}{2}$ and VS_N $= \frac{V_{INPUT\_N}+V_f}{2}$. All the inverters used in this circuit are symmetric with their switching threshold voltage (V_{th}) $= \frac{V_{DD}}{2}$. These voltages (VS_P and VS_N) are passed through inverters (INV1-4) to get full logic values at O_P and O_N, and the correct comparator output is obtained, eventually.

When both input voltages, V_{INPUT_P} and V_{INPUT_N} are less than V_{th}, then M5 transistor turns ON to increase V_f. Also, when both V_{INPUT_P} and V_{INPUT_N} are more than V_{th}, then M6 transistor turns ON to decrease V_f. This is done to obtain V_f in such a range that after adding up, it leads to distinguishable values at O_P and O_N. In these two cases, the output transistors (M1-M4) are OFF, until differential voltages are obtained at O_P and O_N through a CM extractor block. As soon as the valid digital values are obtained at O_P and O_N, the correct outputs are obtained at the output stage. In this case V_f signal is not required, hence the CM extractor block is in OFF condition and the transistors present at the output stage (M1-M4) are ON accordingly, to provide the differential output.

Considering the case of differential inputs, let V_{INPUT_P} be higher than V_{INPUT_N} at an dc offset of V_{th}. Once the voltages at the summing nodes VS_N and VS_P cross the V_{th} of the inverters INV1-2 and INV3-4, respectively, O_P equals to logic '1' and O_N equals to logic '0' are obtained.

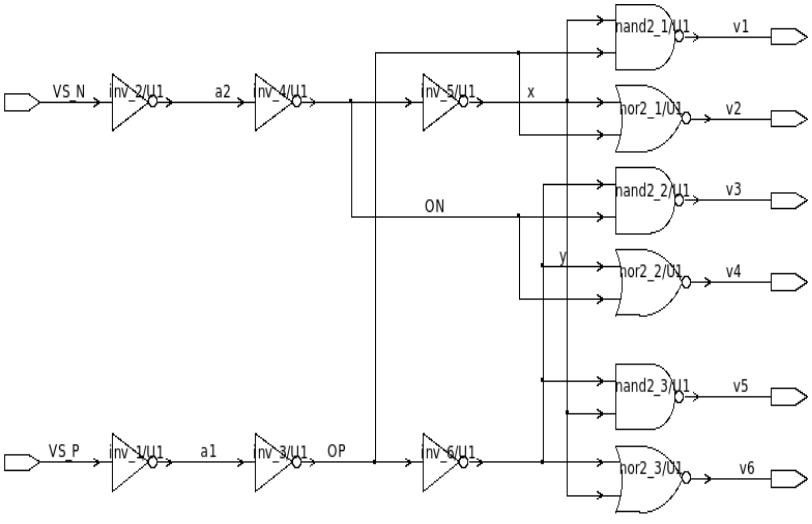


Figure 3.3 Digital comparator with synthesized design

From these O_P and O_N values, it is observed that the M1 and M4 transistors turn ON and M2 and M3 transistors turn OFF. Therefore, FV_{OUTP} becomes '1' and FV_{OUTN} becomes '0'. Similarly, when V_{INPUT_P} decreases and V_{INPUT_N} increases, FV_{OUTP} becomes '0' and FV_{OUTN} becomes '1'. Figure 3.3 shows the synthesized design for the digital part of the proposed comparator (Pseudo-DVC1) using the Synopsys Design compiler.

The proposed comparator is differential in nature as compared to single-ended output comparator shown in Ref. [118]. The fully differential circuits have certain benefits over single-ended circuits like error subtraction, larger output swings, rejection of common-mode noise, a high closed-loop speed, *etc.* [136]. However, all this is achieved at the cost of large power requirements [95, 101]. But the proposed pseudo-DVC1 requires less power as it is designed using digital design methodology

The proposed comparators have been designed in the Cadence virtuoso analog design environment using SCL (Semi-Conductor Laboratory) 180 nm CMOS technology at a supply voltage of 1.8 V and simulated by using Cadence Spectre and Hspice simulators.

3.2.1 Delay of Pseudo-DVC1

Figure 3.4 (a) shows the summing network at the input side with R1=R2=R3=R4=R and parasitic capacitance C_P/C_N at the input of inverters INV1/INV3. Time constant thus formed causes some delay from V_{INPUT_P} node to VS_P node. The delay is formulated [7-8] in equation (3.1) as:

$$VS\_P(t) = V_{INPUT\_P}(t)\left(1 - e^{-t/\tau}\right) \text{ where } \tau = 3RC \tag{3.1}$$

where $C=C_P=C_N$ is the capacitance at VS_P and VS_N nodes. From the simulations, the total delay observed from V_{INPUT_P} node to VS_P node is 0.3 ns. R1 - R4 resistances are implemented using polysilicon resistance (RNLPOLY2T) having a sheet resistance of 5-6 Ohm/square at TT corner. The process variations and mismatches of R1 - R4 effects the VS_P node voltage which has been analyzed using Monte Carlo simulations as shown in Figure 3.4 (b). It can be seen that the mean value is 899.9 mV with the standard deviation of 0.26 mV. The proposed Pseudo-DVC1 has been designed for the load capacitance of 2 pF, the critical path from input to output is observed from VS_P to FV_{OUTN} as shown in Figure 3.2. Hence, the total delay from V_{INPUT_P} to FV_{OUTN} is typically 2.9 ns and varies from 2.5 ns to 3.9 ns at different corners as shown in Figure 3.4 (c). Figure 3.4 (d) depicts the variations

in delay due to mismatches in the comparator circuit. It is observed that the mean value of the delay is 2.9 ns, 1 σ and 3 σ values are 0.17 ns and 0.51 ns, respectively. Table 3.1 shows the variation of delay at different PVT corners.

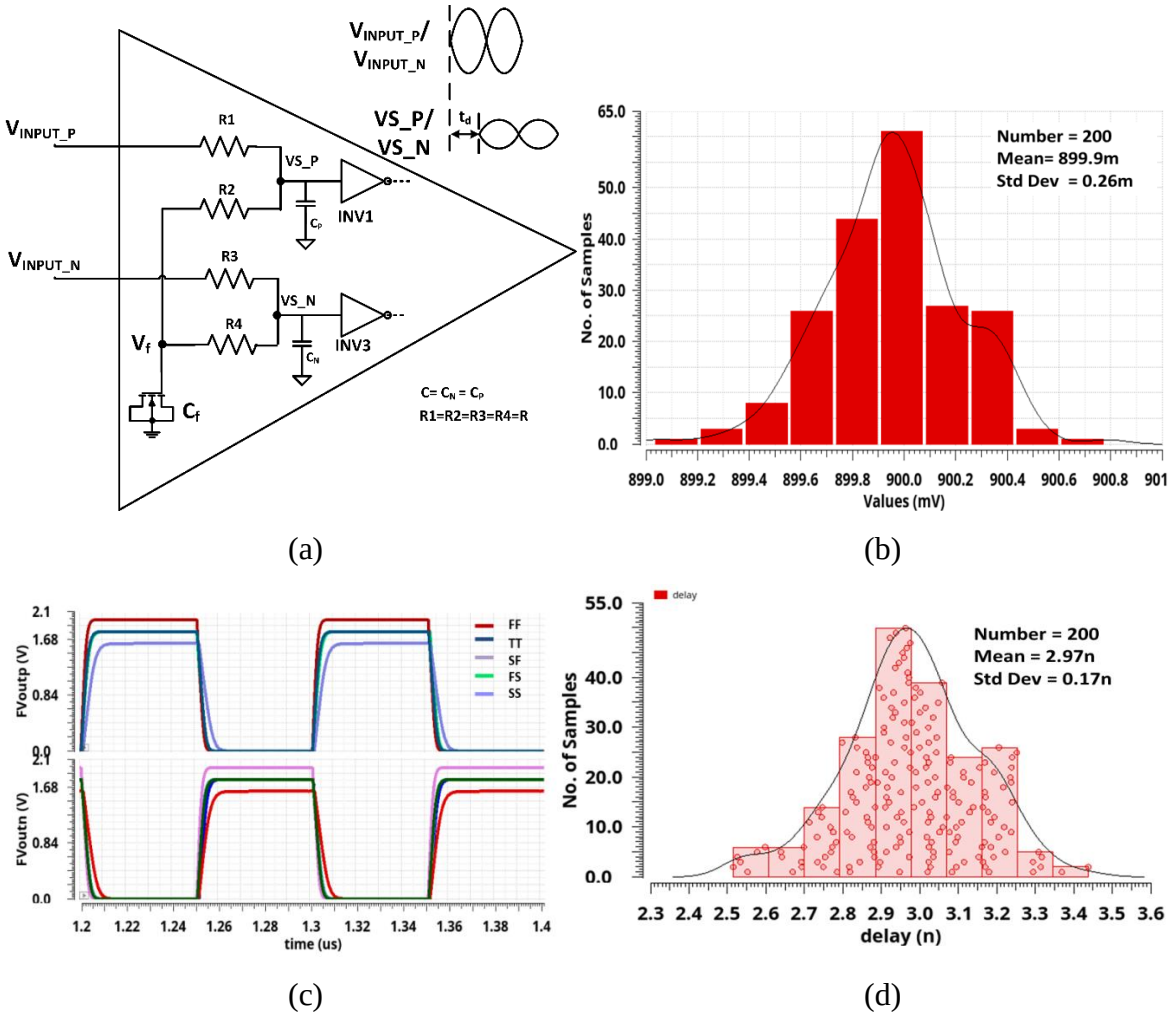
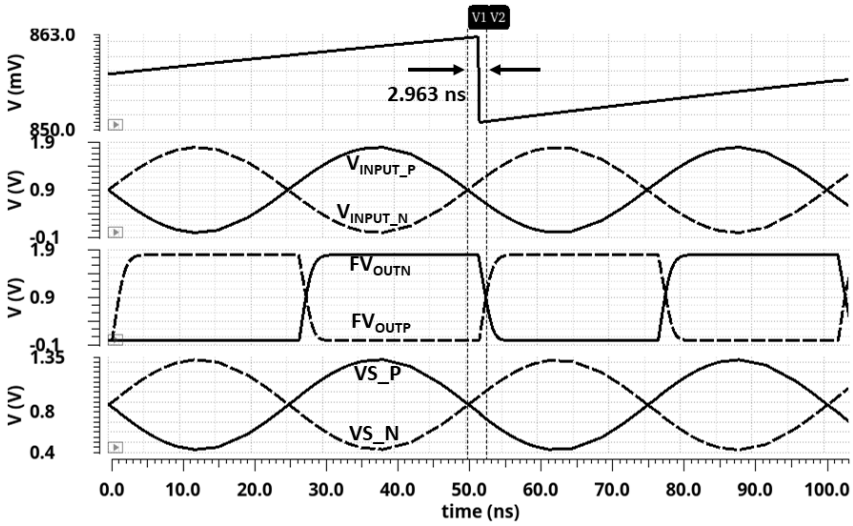


Figure 3.4 (a) Delay of Pseudo-DVC1 (b) Monte Carlo simulations of R1 and R2 variation at VS_P node (c) Output of Pseudo-DVC1 (FV_{OUTP} and FV_{OUTN}) at different PVT corners (d) Variation of delay at FV_{OUTP} node due to mismatches in M1-M2

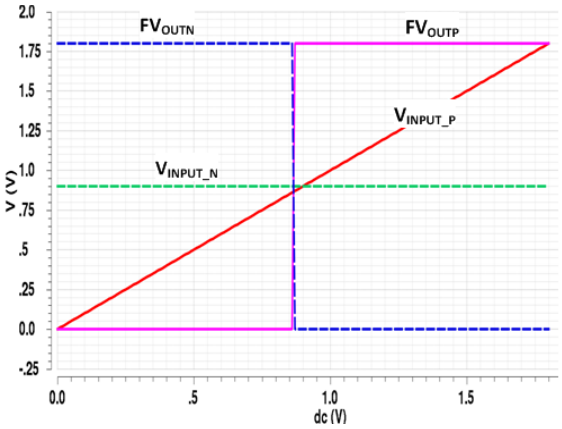
Figure 3.5 (a) shows the propagation delay analysis for the path from V_{INPUT_N} to FV_{OUTP}. Some internal node voltages are also plotted. DC analysis of the proposed digital-based differential voltage comparator is shown in Figure 3.5 (b). When V_{INPUT_P} crosses V_{INPUT_N}, it can be observed that the outputs switch quickly. Also, the delay is calculated for the different values of input voltage amplitude Vp and its plot is shown in Figure 3.5 (c). The value of delay is relatively constant above 500 mV.

Table 3.1 Delay of Pseudo-DVC1 at different PVT corners

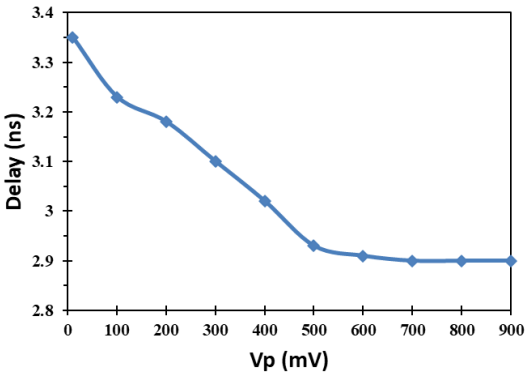
Corner (P)	VDD (V)	Temp. (T) (°C)	Delay (ns)
SS	1.62	85	3.9
SF	1.8	27	3.1
TT	1.8	27	2.9
FS	1.8	27	3.4
FF	1.98	0	2.5



(a)



(b)



(c)

Figure 3.5 (a) Simulation result of differential voltage comparator (Pseudo-DVC1) (b) DC analysis of digital-based voltage comparator (Pseudo-DVC1) (c) Variation of propagation delay with change in input voltage amplitude Vp

3.2.2 Input Offset Voltage of Pseudo-DVC1

The input offset voltage is another important design parameter in the comparator design. The offset voltage of the digital-based differential voltage comparator depends on the delay of the inverters (INV1-4), mismatches in the resistances (R1-R4), and the threshold voltages of inverters (INV1-4). As shown in Figure 3.4 (b), there is a voltage divider at the input side, the process variations in the resistive network do not affect the voltages at VS_P and VS_N much (the value of σ is 0.26 mV with a mean of about 0.9 V). So, the resistive network does not affect the offset voltage. The signal amplitude at VS_P and VS_N nodes are less; hence inverters (INV1, INV2, INV3, and INV4) are used to amplify the signals up to the supply rails. The main source of the offset in the circuit is the mismatches in rising (falling) time delays t_{d_rise1} and t_{d_rise2} (t_{d_fall1} and t_{d_fall2}) of digital inverters (INV1 and INV3). It leads to an increase in the offset voltage, $V_{offset1} = (Io/Co)\, dt$ where Io is the current flowing through load Co ($C_{LP} = C_{LN}$ in Figure 3.2) and $dt = (t_{d\_rise1} - t_{d\_rise2}) - (t_{d\_fall1} - t_{d\_fall2})$ and mismatches in the switching threshold voltages of INV1 and INV3 leads to $V_{offset2} = V_{th1} - V_{th3} = dV$. The total offset voltage is given by

$$V_{offset} = V_{offset1} + V_{offset2} \tag{3.2}$$

$$V_{offset} = \frac{Io}{Co} dt + (V_{th1} - V_{th3}) \tag{3.3}$$

To see the variations in offset voltage, the Monte Carlo simulations for 500 runs are performed and are shown in Figure 3.6. It is observed that the mean value of the offset voltage is 4.97 mV with a standard deviation of 2.5 mV.

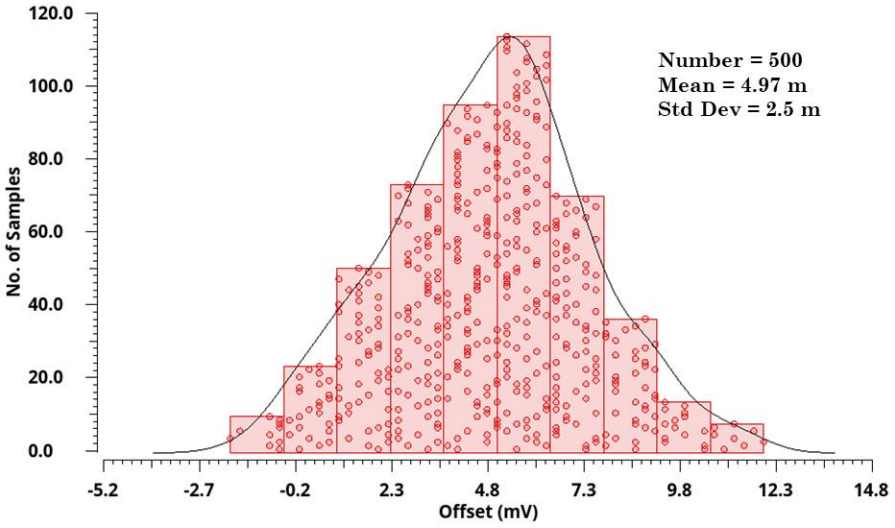


Figure 3.6 Monte Carlo Simulations of offset for 500 runs

3.2.3 Power Analysis of Pseudo-DVC1

While designing a comparator, power dissipation is one of the critical design parameters. There is a demand for low-power circuits due to widespread applications for portable and battery-operated devices. The total power is the sum of dynamic and static power dissipation, which is given by

$$P_{Total} = P_{Dynamic} + P_{Static} \tag{3.4}$$

where $P_{Dynamic}$ is the sum of the switching power and short circuit power. The switching power $P_{Switching}$ is because of the charging and discharging of the load capacitance when there is a change in the input voltage. The short circuit power $P_{short\_circuit}$ is due to the current flowing from the supply, *i.e.*, VDD to the ground. So, the dynamic power is termed as

$$P_{Dynamic} = P_{Switching} + P_{short\_circuit} \tag{3.5}$$

$$P_{Dynamic} = \alpha\, C\, (VDD)^2\, f + t_{short\_circuit} VDD\, I_{peak} \tag{3.6}$$

where α is the switching factor, C is the load capacitance of the corresponding gate, $t_{short\_circuit}$ represents the time during which the short circuit current flows, I_{peak} is the peak current that flows from VDD to the ground, and f is the frequency of operation.

Table 3.2 Switching factor α for different gates

$P_{0\to1}$ ($P_0 \cdot P_1$)	Switching Factor (α)
Inverter	1/4
2 Input NAND/NOR	3/16
3 Input XOR	1/4
3 Input NAND	7/64

The values of α for different gates are shown in Table 3.2 [137].

The main components of static power dissipation are the leakage currents and subthreshold leakage currents P_{Static} is given by

$$P_{Static} = (I_{sub\_th} + I_{leak})\, VDD \tag{3.7}$$

The proposed Pseudo-DVC1 designed at the supply of 1.8 V in 180 nm CMOS technology gives an average power dissipation of 192 µW. Most of the power is consumed by the inverters INV1 and INV3 because of the large short circuit current flowing through them as they are biased around the midpoint of supply voltage to maximize the amplification. The remaining part of the circuit components consumes almost negligible static power.

The layout of the proposed comparator (Pseudo-DVC1) designed in the SCL 180 nm CMOS process and is shown in Figure 3.7. It covers an area of 9600 µm^2 with dimensions of 160 µm x 60 µm.

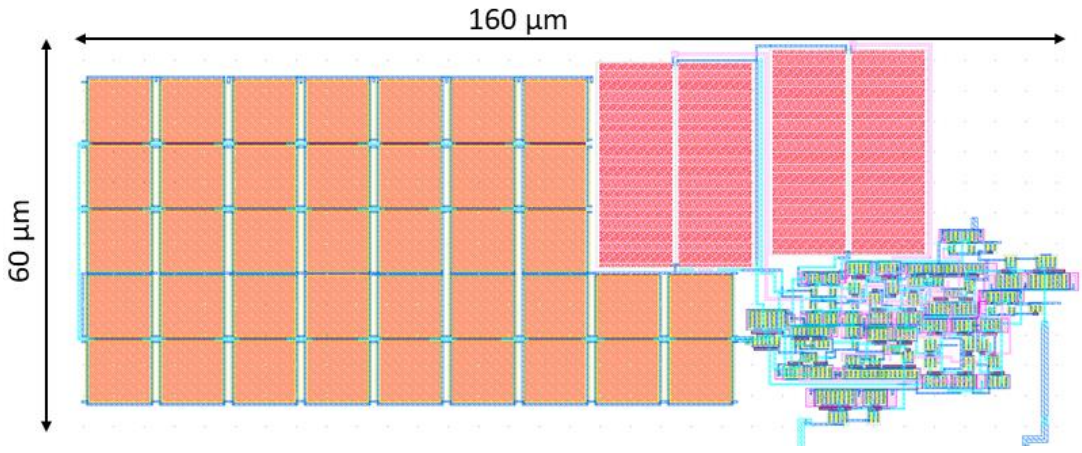


Figure 3.7 Layout of proposed Pseudo-DVC1

3.3 Pseudo Digital-based Low Power Differential Voltage Comparator (Pseudo-DVC2)

The proposed Pseudo-DVC1 shown in Figure 3.2 in previous section is further improved for low power following the digital design methodology. In the proposed circuit, the MOS M1-M6 present in Pseudo-DVC1 are replaced with digital logic. The proposed comparator (Pseudo-DVC2) have been shown in Figure 3.8. It is based upon the digital design methodology and uses standard cells like CMOS based Inverters, XOR, NOR, and NAND gates. The operation of this proposed Pseudo-DVC2 is similar to the comparator presented earlier (in section 3.2 *i.e.*, Pseudo-DVC1) except the MOS transistors present at output and feedback circuit are replaced with digital gate-based circuit consists of XOR gates, inverters, and D-latches. Except for the summing network, the proposed design is fully synthesizable and can be easily implemented on flexible devices such as FPGAs. Table 3.3 shows the variation of voltages at the output nodes due to various input voltages. When both the input A_{INP} and A_{INN} are less than V_{th} then the feedback loop is active and V_{com} node voltage increases through D-latch-3. When both the input A_{INP} and A_{INN} are more than V_{th} then the feedback loop is active to decrease the V_{com} node voltage through D-latch-3.

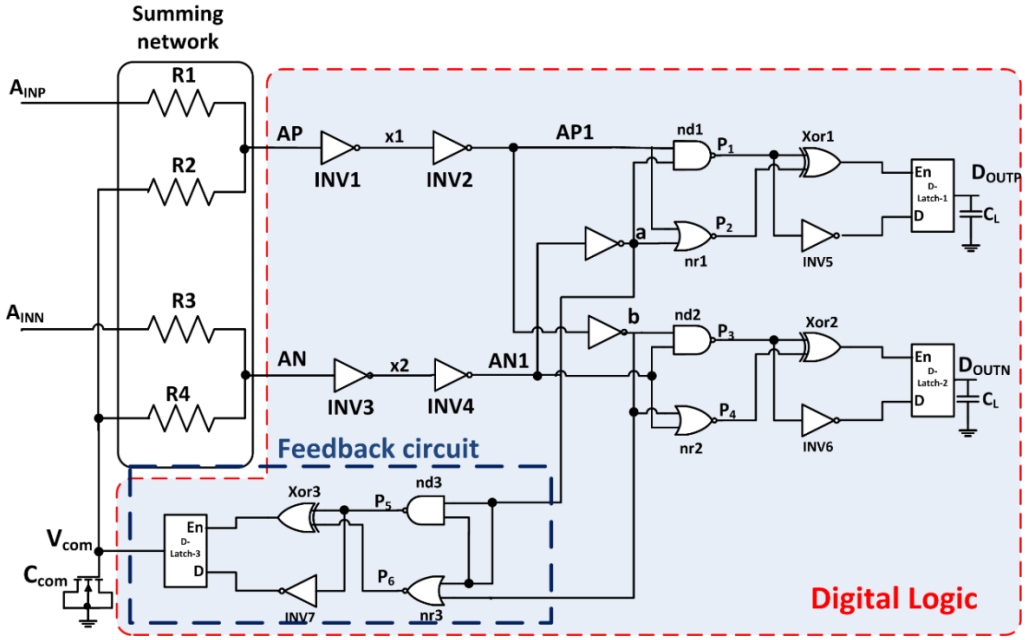


Figure 3.8 Pseudo digital-based low power differential voltage comparator (Pseudo-DVC2)

Table 3.3 Variations of different nodes voltages of Pseudo-DVC2 due to input change

Input	AP1	AN1	V_{com}	D_{OUTP}	D_{OUTN}
$A_{INP} < V_{th}$ & $A_{INN} < V_{th}$	0	0	↑	Z	Z
$A_{INP} > V_{th}$ & $A_{INN} > V_{th}$	1	1	↓	Z	Z
$A_{INP} > V_{th}$ & $A_{INN} < V_{th}$	1	0	Z	↑	↓
$A_{INP} < V_{th}$ & $A_{INN} > V_{th}$	0	1	Z	↓	↑

When both the input A_{INP} and A_{INN} are less than V_{th} then the feedback loop is active and V_{com} node voltage increases through D-latch-3. When both the input A_{INP} and A_{INN} are more than V_{th} then the feedback loop is active to decrease the V_{com} node voltage through D-latch-3. This feedback circuit will bring the input voltages in differential conditions to enable the D-latch-1 and D-latch-2 at the output of the comparator. Considering the case of the differential input, let A_{INP} be more than A_{INN}. This causes AN1 rises to logic '1' and AP1 falls to logic '0'. Therefore, D_{OUTP} becomes '1' and D_{OUTN} becomes '0'. Similarly, when A_{INP} is lesser than A_{INN} , D_{OUTP} becomes '0' and D_{OUTN} becomes '1'. The Synopsys Design Compiler is used to synthesize the comparator and implemented by referencing the standard library cells in the RTL Verilog code. The spice-based transient simulation of the comparator is shown in Figure 3.9 with an average current of 41.6 µA.

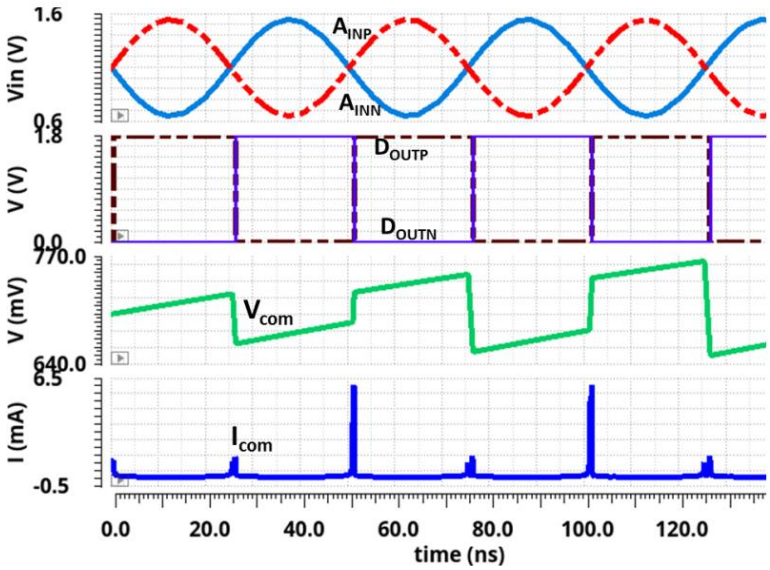


Figure 3.9 Transient analysis of Pseudo-DVC2

3.3.1 Delay and Power of Pseudo-DVC2

As shown in Figure 3.8, the critical path in Pseudo-DVC2 is from node A_{INP} to node D_{OUTN}. The total delay between these two nodes is typically 1.4 ns as obtained from the transient analysis shown in Figure 3.10 (a). Figure 3.10 (b) shows the variations in power and delay versus input amplitude (Vamp) at the supply of 1.8 V. Delay is minimum at 285 mV *i.e.*, approximately 0.5 ns, and power consumption is maximum at that point which is approximately 400 µW. With the increase in Vamp, power and delay are relatively constant above 500 mV. Figure 3.10 (c) shows the simulation result of the proposed comparator at different supply voltages.

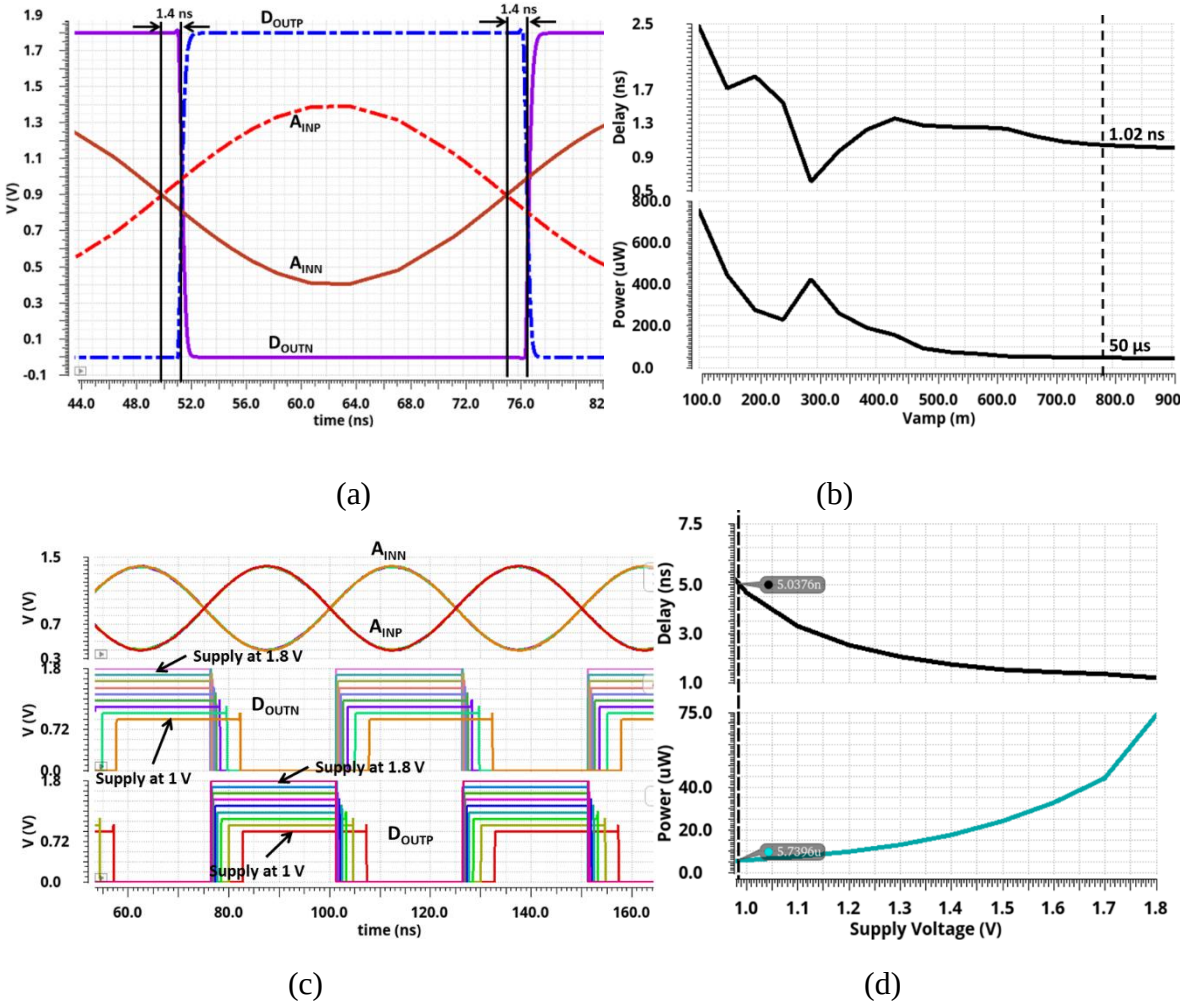


Figure 3.10 (a) Delay analysis of the Pseudo-DVC2 (b) Variations of power and delay with respect to input signal amplitude (c) Transient analysis of the comparator (Pseudo-DVC2) at different supply voltages (1 V - 1.8 V) (d) Variation of power and delay of the comparator (Pseudo-DVC2) at different supply voltages (1 V - 1.8 V)

The operating range of the proposed comparator is 1 V to 1.8 V; hence the supply voltage of the proposed comparator can be reduced to 1 V only. Delay and power graphs obtained with the variations in the supply voltage is depicted in Figure 3.10 (d). It is observed that power and delay are inversely proportional to each other, the delay of the circuit reduces with an increase in power.

3.3.2 Input Offset Voltage of Pseudo-DVC2

The offset voltage analysis of Pseudo-DVC2 is similar to the analysis of pseudo-DVC1 shown in section 3.2.2 because of analogous circuitry present at the input side. The mean value of the observed offset voltage is 4.97 mV.

3.3.3 Implementation of Pseudo-DVC2 on FPGA

The hardware implementation of the digital part of the proposed Pseudo-DVC2 (which requires 6 LUTs) except the summing network is synthesized and implemented on Xilinx Basys-3 Artix-7 FPGA using Vivado software platform to prove its functional validity as depicted in Figure 3.11. It consumes only 6 lookup tables (LUTs) and 5 input/output (I/O) ports.

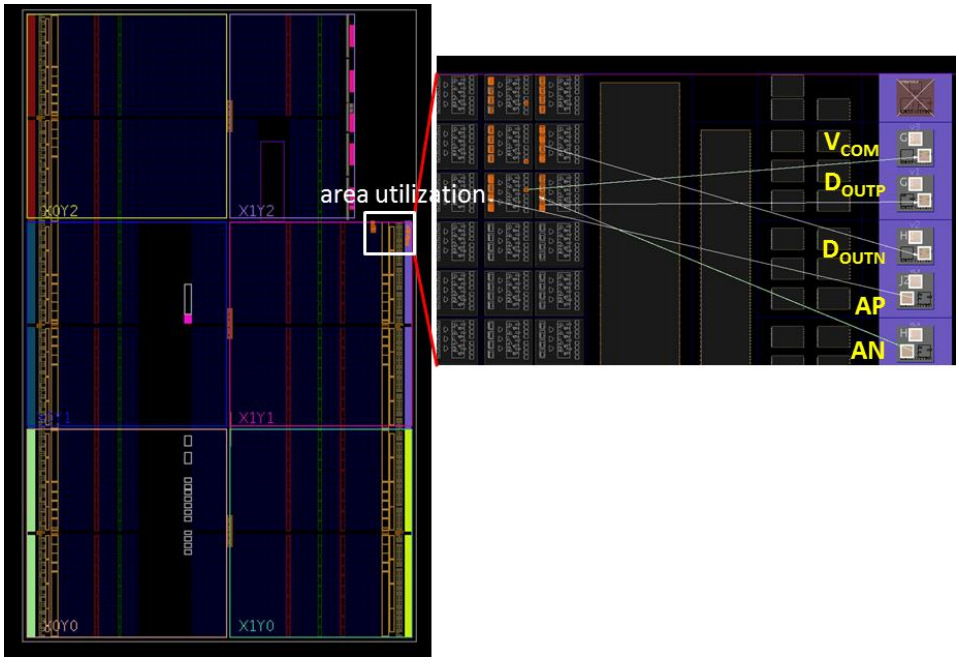


Figure 3.11 Hardware Implementation of the comparator in Xilinx Artix-7 FPGA board

Figure 3.12 demonstrates the testing circuit diagram with the analog input provided by the function generator (Tektronix AFG1022). Both sinusoidal and ramp signals are applied at the input nodes for testing purposes. The digital signal oscilloscope TBS1102B (from Tektronix) is used to observe the output. In order to validate the digital concept, the Basys-3 FPGA board and some off-the-shelf components are used to implement the proposed comparator. Figure 3.13 (a) shows the circuit of the proposed comparator along with the other instruments needed for measurement. The proposed comparator has been tested by applying the input sinusoidal signal of 100 kHz with an offset of 1.65 V and peak-to-peak voltage of 3.3 V.

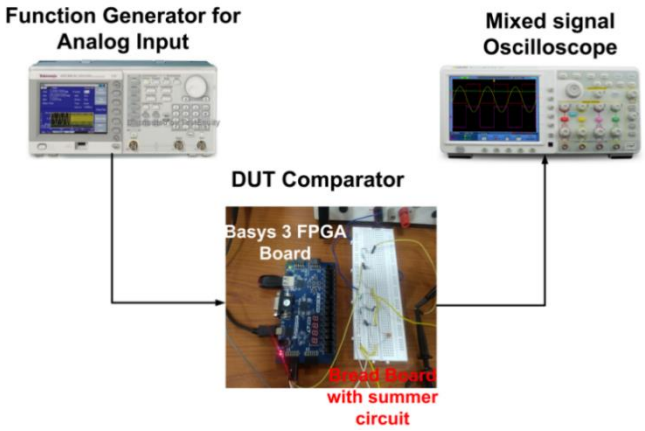
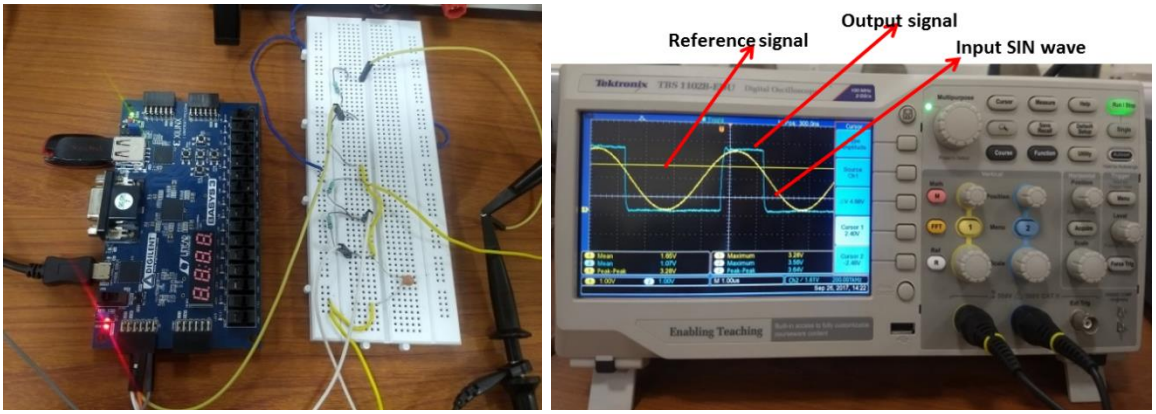


Figure 3.12 Physical testing flow diagram of the proposed comparator



(a) (b)

Figure 3.13 (a) Testing setup of proposed comparator showing the implementation on FPGA with off-the-shelf components (b) Signals of the proposed comparator with 2.2 V reference voltage

A reference DC voltage of 2.2 V is applied at the other input terminal of the comparator. When the input voltage crosses the reference voltage, the output is changed from '1' to '0' or vice versa depending on the condition, whether the input voltage is higher or lower than the reference voltage, and shown in Figure 3.13 (b).

3.4 Pseudo Digital-based Differential Voltage Comparator (Pseudo-DVC3)

Further to reduce the complexity and the area of voltage comparator Pseudo-DVC2 (explained in section 3.3), a supply scalable differential analog voltage comparator (Pseudo-DVC3) without passive components is proposed in this section. The circuit diagram of the proposed comparator is shown in Figure 3.14. The summing network has been implemented with the help of transmission gates (TGs) and the complexity of the digital part is reduced by decreasing the number of digital gates. It uses CMOS standard cells such as inverters, tri-state inverters, and XOR gates. The summing network gives the average of the feedback signal Vx stored in a capacitor Cx and the external inputs.

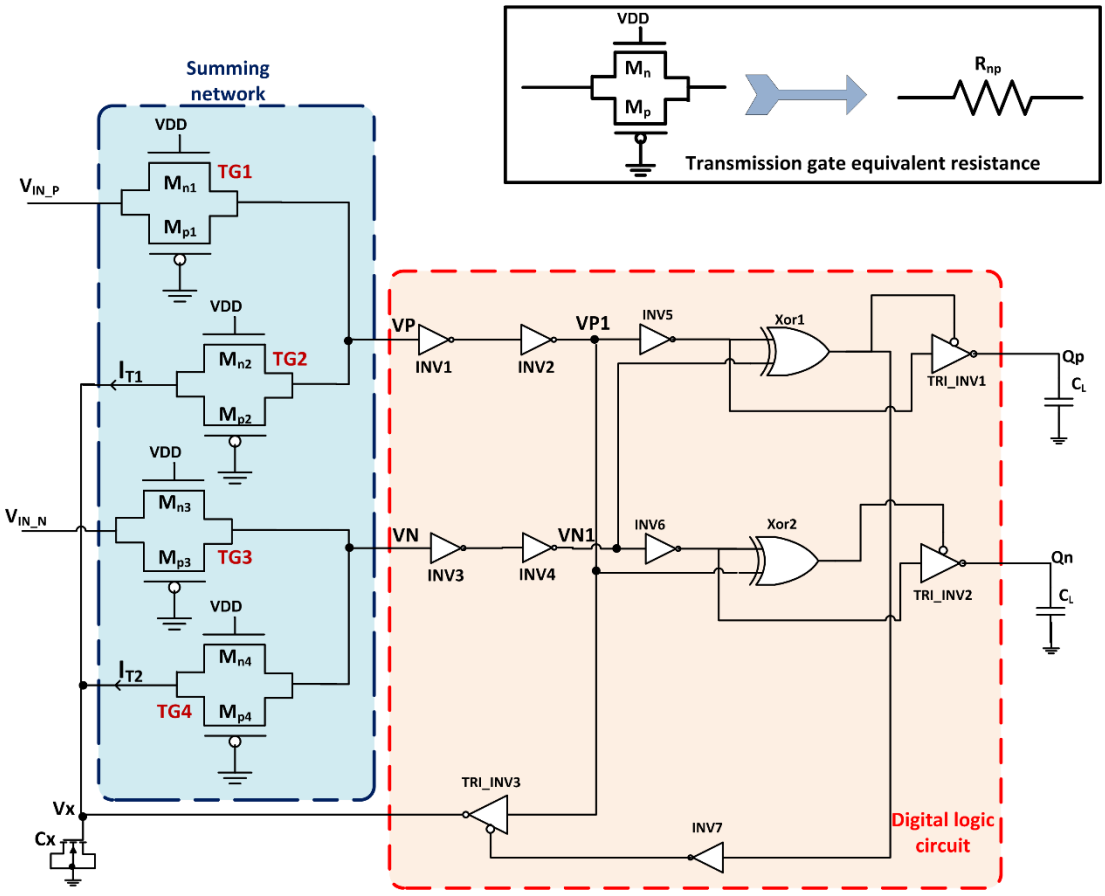


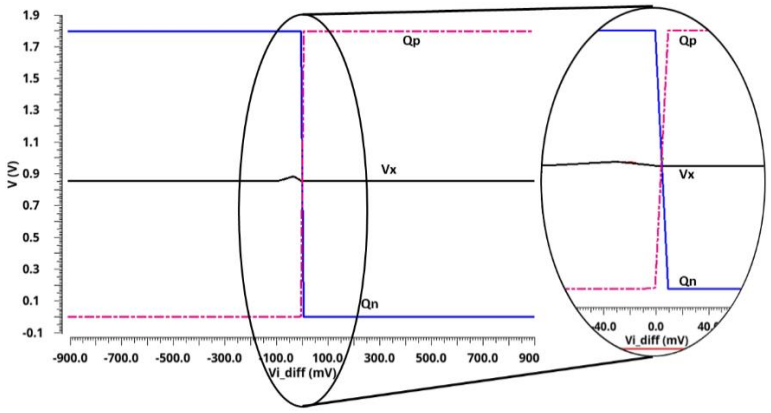
Figure 3.14 A digital-based differential analog comparator (Pseudo-DVC3)

The following text explains the detailed working of the circuit. All the tri-state inverters (TRI_INV1-3) used in the circuit are active low enabled inverters *i.e.*, if the enable signal is low then only the output will be inverted of the inputs otherwise outputs are in a high impedance state. The feedback circuit comprises of tri-state inverter TRI_INV3 and inverter INV7. Vx, thus, obtained gets added up using summing network with both the input voltages V_{IN_P} and V_{IN_N} to bring the VP/VN nodes around V_{th} of INV1 and INV3. Mathematically, $VP = \frac{V_{IN\_P}*R_{np2}+V_x*R_{np1}}{R_{np1}+R_{np2}}$ and $VN = \frac{V_{IN\_N}*R_{np4}+V_x*R_{np3}}{R_{np3}+R_{np4}}$ where R_{np1}, R_{np2}, R_{np3}, and R_{np4} are the resistances offered by the respective transmission gates TG1, TG2, TG3, and TG4.

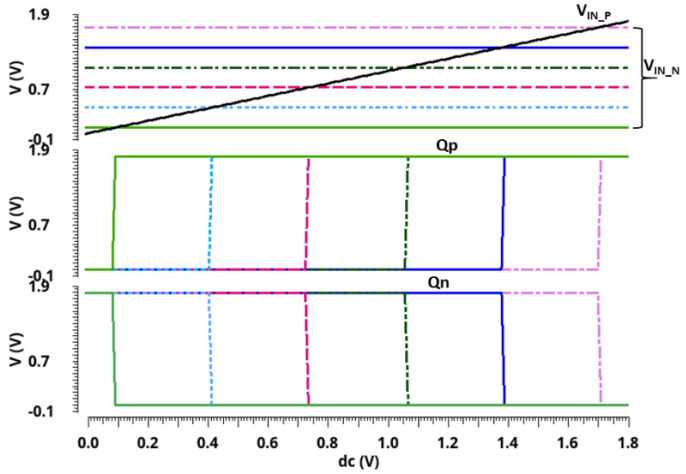
If voltage levels V_{IN_P} and V_{IN_N} are lower than V_{th} then VP1= VN1= '0'. This causes the voltage on Vx to increase by charging the capacitor Cx through a feedback logic circuit. When both V_{IN_P} and V_{IN_N} are larger than V_{th}, then VP1= VN1= '1'and the voltage on Vx decreases by discharging the capacitor Cx through a feedback logic circuit. In the above condition, TRI_INV1 and TRI_INV2 are OFF which disables the outputs Qp and Qn through TRI_INV1 and TRI_INV2, respectively. The variation of the voltage level on the Vx node is further added to the inputs through the summing network and takes the node voltages at VP and VN to the differential value. As soon as VP/VN nodes become more/less than V_{th} of INV1/INV3, the TRI_INV1 and TRI_INV2 provide the correct logic at the output nodes *i.e.*, Qp and Qn. Also, once VP1 and VN1 are complementary to each other, it disables the feedback network and Cx holds the previous value of Vx .

If V_{IN_P} is more than V_{IN_N} at an offset of V_{th}, VN1 rises towards logic '1' and VP1 falls towards logic '0' and Qp becomes '1' and Qn becomes '0' eventually. Similarly, when V_{IN_P} is lesser than V_{IN_N} around an offset of V_{th}, Qp becomes '0' and Qn becomes '1', respectively.

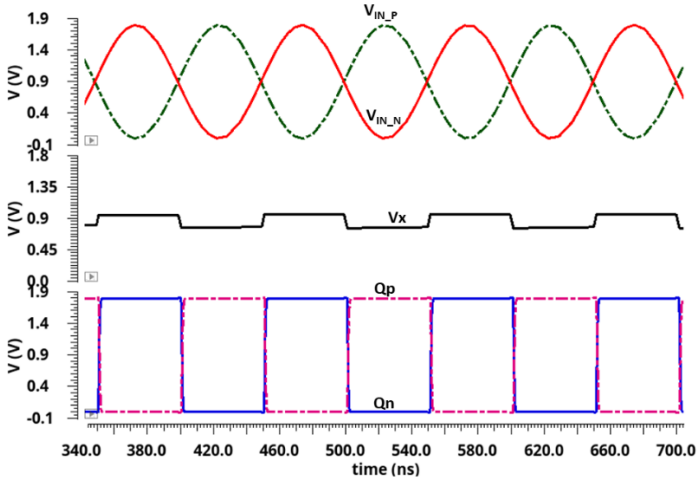
Figure 3.15 (a) shows the DC characteristic of the proposed comparator when $V_{IN\_P} - V_{IN\_N}$ (= Vi_diff) is applied at the input. It is observed that switching takes place when voltage Vx remains close to VDD/2 *i.e.*, 0.9 V for different values of Vi_diff ranging from − 0.9 V to 0.9 V. Figure 3.15 (b) shows the transition in differential output when a ramp signal V_{IN_P} is compared with different values of V_{IN_N} varying from 0.1 V to 1.7 V. Figure 3.15 (c) shows the transient analysis to observe the variation in feedback voltage Vx when a fully differential input is applied to the proposed comparator. It can be seen that Vx varies around mid of the supply voltage *i.e.*, 0.9 V for all the values of Vi_diff.



(a)



(b)



(c)

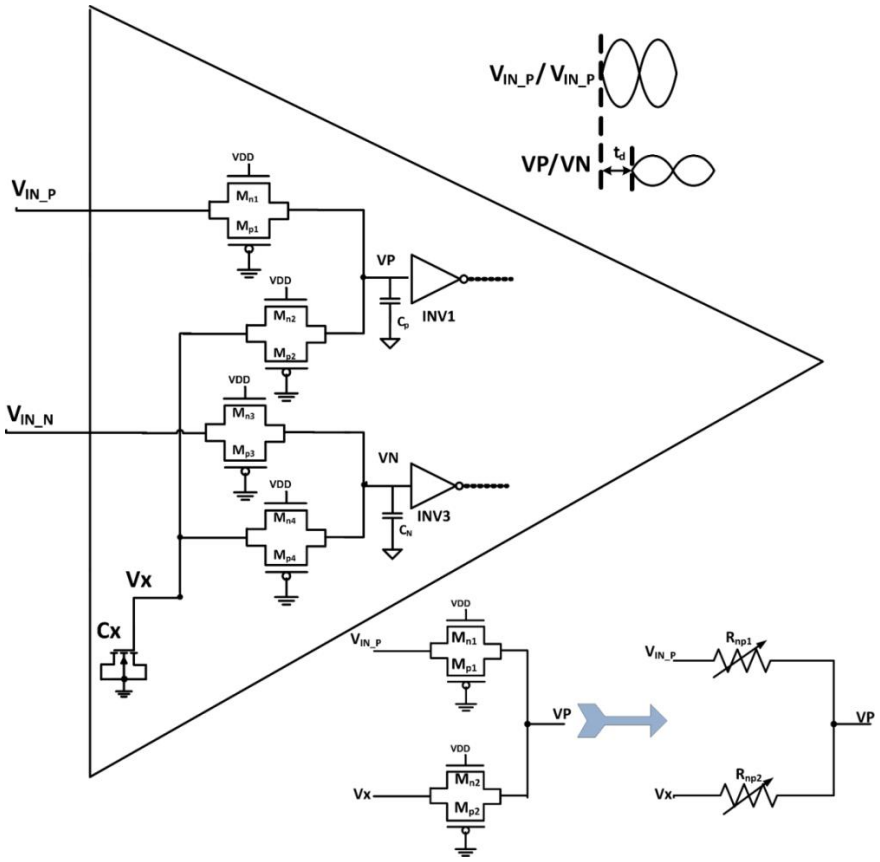
Figure 3.15 (a) DC analysis of Pseudo-DVC3 (b) Change in Qp and Qn for different V_{IN_N} (c) Variation of feedback voltage Vx with respect to the fully differential input

3.4.1 Delay of Pseudo-DVC3

As shown in Figure 3.16 (a), the resistances (R_{npx} where x ∈ 1-4) offered by the TG varies with the voltage across it. Therefore, TG-based resistances (R_{np1}, R_{np2}, R_{np3} and R_{np4}) and parasitic capacitances C_N/C_P develop some voltage dependent time constant. The delay from the input node V_{IN_P} to VP is t_d which is also the worst-case delay if $R_{np1} = R_{np2} = R_{np3} = R_{np4} = R$ (where R is voltage dependent resistance). The delay is formulated in equation (3.8) [12, 13] as:

$$VP(t) = V_{IN\_P}(t)\left(1 - e^{-t/\tau}\right) \text{ with } \tau = 3RC \tag{3.8}$$

where $C_P = C_N = C$ is the parasitic capacitance at the input node of INV1/INV3. The variation of transmission gate-based resistance with the change in voltage across it is shown in Figure 3.16 (b). The simulation result shows a delay of 0.29 ns from V_{IN_P} node to VP node.



(a)

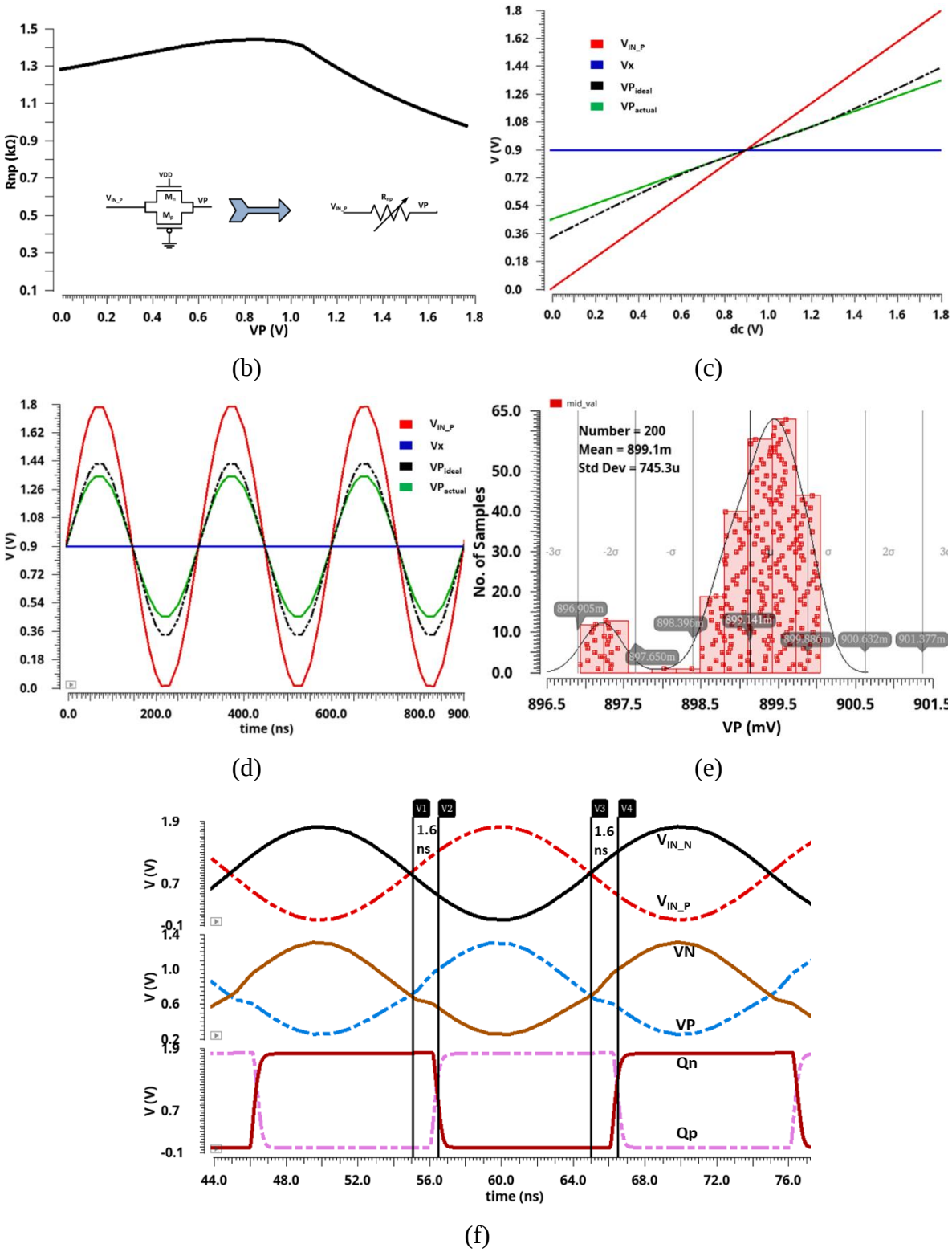
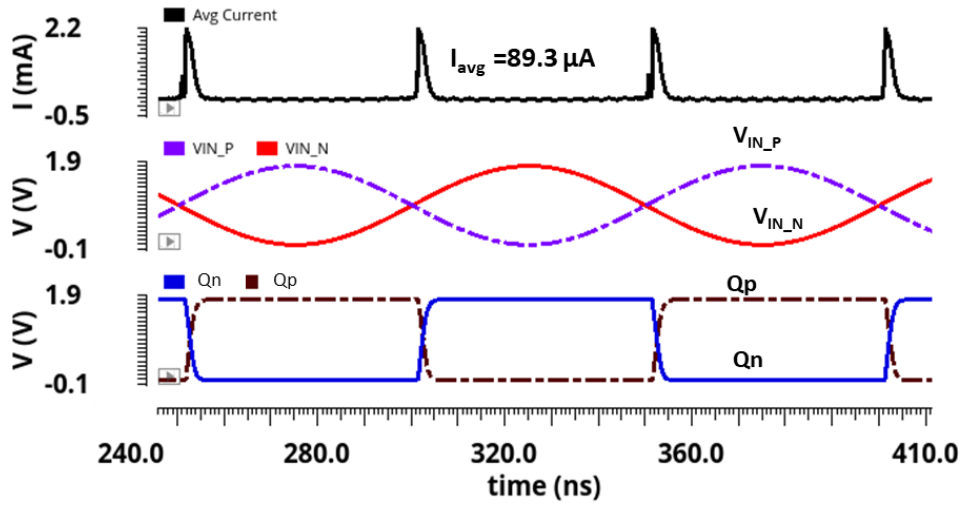


Figure 3.16. (a) Circuit diagram to analyze the delay of Pseudo-DVC3 (b) Equivalent resistance R_{np} of transmission gate (c) DC analysis of Pseudo-DVC3 (d) Transient analysis of TG based voltage divider (e) Monte Carlo simulation for the node voltage VP (f) Transient analysis of Pseudo-DVC3

Figure 3.16 (c) shows the ideal and actual simulations at the node voltage VP, where ideal simulations are obtained by using the passive resistances and actual simulations are obtained using TGs in the summer network. Here, the input V_{IN_P} is varying from 0 V to 1.8 V while keeping Vx constant at the mid of supply voltage *i.e.*, 0.9. The difference is due to the formation of a voltage-dependent resistive voltage divider at the VP node. A similar analysis is applicable for the VN node as well. The transient analysis is depicted in Figure 3.16 (d). Monte Carlo simulation shown in Figure 3.16 (e) is performed to analyze the effect at the VP node due to changes in the value of resistances R_{np1} and R_{np2} due to the process variations. The mean and the standard deviation of the voltage at node VP are 899.1 mV and 745.3 µV, respectively. Therefore, even with process variations, the VP node varies by 0.1 % from its typical value of VDD/2. Figure 3.16 (f) shows the transient analysis of the proposed differential voltage comparator where the input V_{IN_P} is crossing the reference voltage level V_{IN_N} and differential outputs are changing accordingly.

In the proposed comparator, most of the power is consumed during the switching of various nodes. The average current consumed by the proposed comparator at 1.8 V supply is 89.3 µA as shown in Figure 3.17 (a). The transient response of the comparator at different PVT corners is shown in Figure 3.17 (b) and the observed values of delay are shown in Table 3.4. From the table, it is clear that the best value of delay is 1.32 ns at FF corner while the worst-case delay of 2.11 ns is obtained at SS corner.



(a)

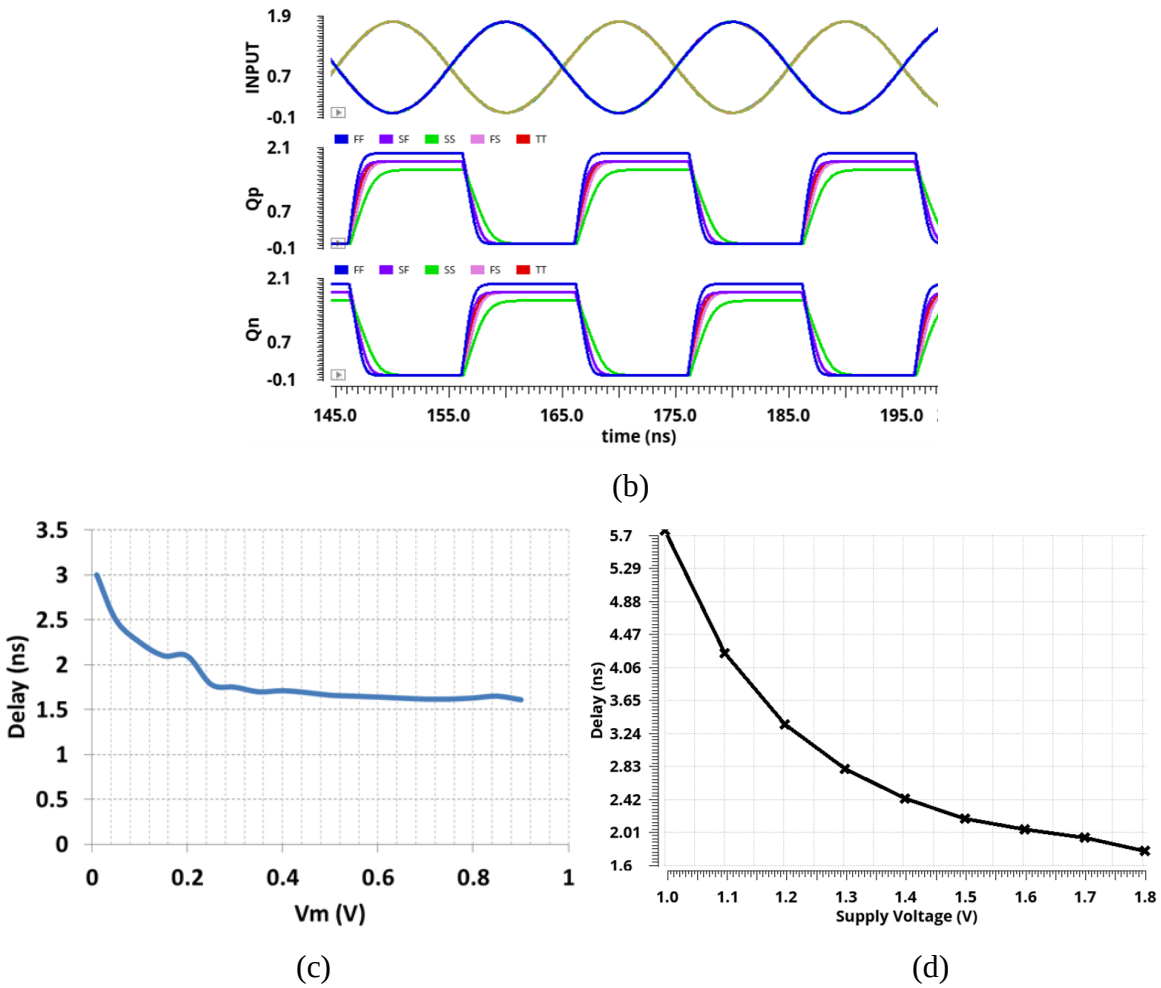


Figure 3.17 (a) Simulations result of Pseudo-DVC3 (b) Output of Pseudo-DVC3 (Qp and Qn) at different corners variations (c) Propagation delay versus input amplitude Vm (d) Variation of delay with respect to supply voltage

Table 3.4 Delay of Pseudo-DVC3 at different PVT corners

Process Corner (P)	**VDD (V)**	**Temp. (°C) (T)**	**Delay (ns)**
SS	1.62	85	2.11
SF	1.8	27	1.81
TT	1.8	27	1.63
FS	1.8	27	2.0
FF	1.98	0	1.32

Also, the simulation result of the delay with the variation in input amplitude, Vm is plotted in Figure 3.17 (c). From the figure, it is evident that the delay of the comparator for the input amplitude of 10 mV at an offset of 0.9 V is 3 ns and it decreases with the increase in the input amplitude as the comparator takes fewer iterations to resolve the input difference. Figure 3.17 (d) shows the proposed comparator works properly for the supply voltage ranging from 1 V to 1.8 V.

3.4.2 Input Offset Voltage of Pseudo-DVC3

In the proposed comparator Pseudo-DVC3, the foremost cause of the offset voltage is the difference in rising (falling) time delays between $t_{d_{r1}}$ and $t_{d_{r2}}$ ($t_{f_{r1}}$ and $t_{f_{r2}}$) of node voltages (VP1/VN1) in the upper and lower arms. The variation in rising and falling delay leads to the offset voltage, $V_{os1} = (I(C_L)/C_L) \cdot dt$ where $I(C_L)$ is the current flowing through the load C_L and $dt = (t_{d_{r1}} - t_{d_{r2}}) - (t_{f_{r1}} - t_{f_{r2}})$. Also, the mismatch in the switching threshold voltages of inverters INV1 and INV3 at the input side causes the offset voltage, *i.e.*, $V_{os2} = V_{th1} - V_{th3} = dV$. Also, MOSFET based resistances in TG, which has a random variation, are given by

$$R_n \approx \frac{L}{\mu_n c_{ox} W(V_{GS} - V_{tn})} \tag{3.9}$$

$$R_p \approx \frac{L}{\mu_p c_{ox} W(V_{GS} - V_{tp})} \tag{3.10}$$

Therefore, equivalent resistance R_{np} offered by TG is expressed as

$$R_{np} = R_n \parallel R_p \tag{3.11}$$

$$R_{np} \approx \frac{L_p}{\mu_p c_{ox} W_p(V_{GS} - V_{tp})} \parallel \frac{L_n}{\mu_n c_{ox} W_n(V_{GS} - V_{tn})} \tag{3.12}$$

Due to mismatches, the above value of R_{np} may change by ΔR_{np}, *i.e.*

$$R_{np} + \Delta R_{np} \approx \frac{(L_p + \Delta L_p)}{(\mu_p + \Delta\mu_p)C_{ox}(W_p + \Delta W_p)(V_{GS} - [V_{tp} - \Delta V_{tp}])} \parallel \frac{(L_n + \Delta L_n)}{(\mu_n + \Delta\mu_n)C_{ox}(W_n + \Delta W_n)(V_{GS} - [V_{tn} - \Delta V_{tn}])} \tag{3.13}$$

$$R'_{np1,2,3,4} \approx R_{np} + \Delta R_{np} \tag{3.14}$$

where $R'_{np1,2,3,4}$ are the individual resistance values offered due to mismatches. Also, the mismatches and process variation of resistance formed by the transmission gate affect the node voltages VP and VN *i.e.*, $V_{os3} = VP - VN$ at similar input condition of V_{IN_N}, V_{IN_P} and Vx where $VP = \frac{V_{IN\_P} * R'_{np2} + Vx * R'_{np1}}{R'_{np1} + R'_{np2}}$ and $VN = \frac{V_{IN\_N} * R'_{np4} + Vx * R'_{np3}}{R'_{np3} + R'_{np4}}$. The total offset voltage (V_{os}) of the proposed comparators is

$$\begin{aligned} V_{os} &= V_{os1} + V_{os2} + V_{os3} \\ &= \frac{I(C_L)}{C_L} \cdot dt + (V_{th1} - V_{th3}) + (VP - VN) \end{aligned} \tag{3.15}$$

Figure 3.18 (a) shows the Monte Carlo simulations of VP-VN due to process variations.

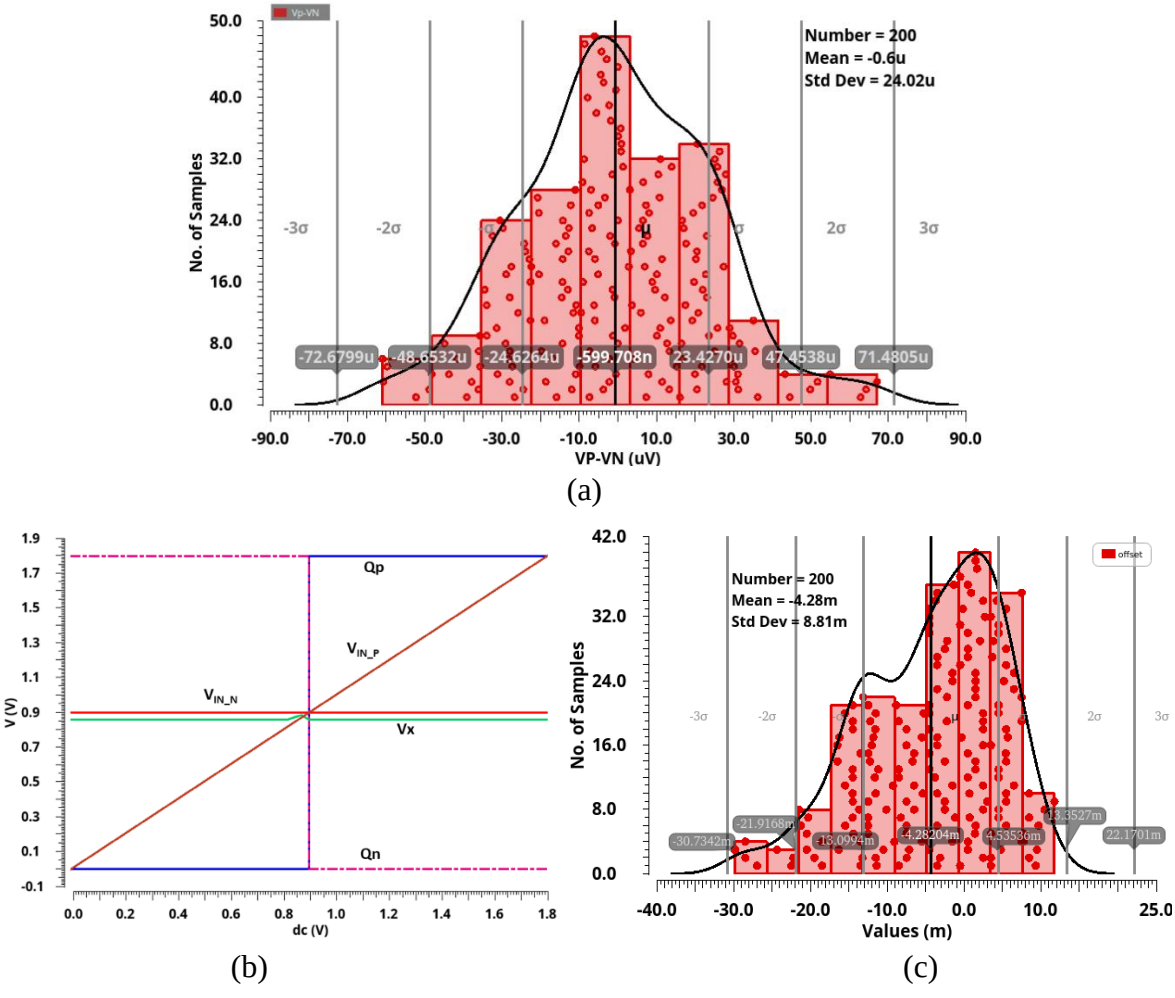
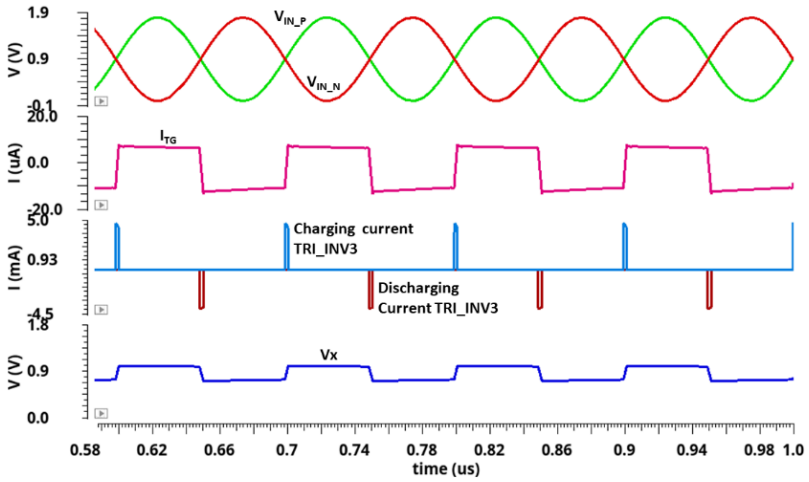


Figure 3.18. (a) Monte Carlo simulations for VP-VN variation (b) DC analysis to calculate the offset voltage (c) Monte Carlo simulations for offset calculations

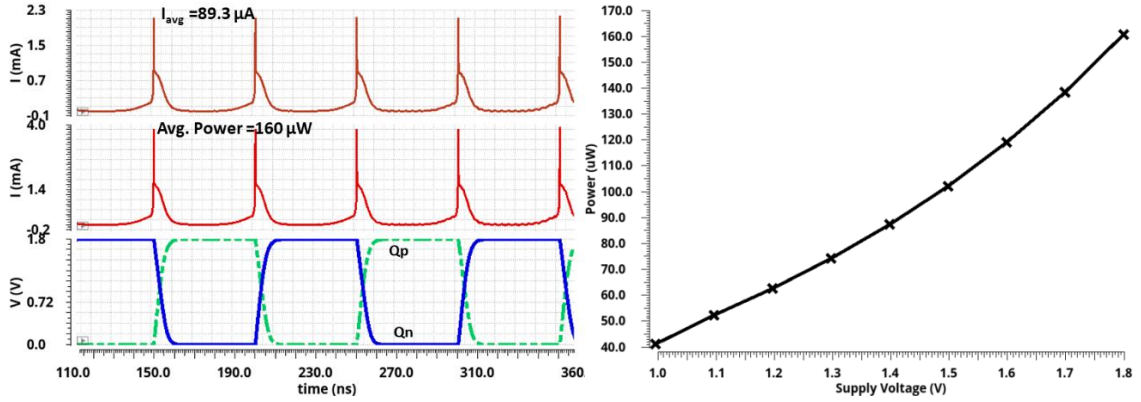
The DC analysis to calculate the offset voltage is shown in Figure 3.18 (b). The Monte Carlo simulations for 200 runs are done to observe the variations in comparator offset voltage as shown in Figure 3.18 (c) which gives the mean value of the offset voltage is 4.28 mV.

3.4.3 Power Analysis of Pseudo-DVC3

The detailed power analysis of the proposed comparator Pseudo-DVC3 is explained in the following text. During the transition phase, dynamic and short circuit currents are the major components of power dissipation. The inverters INV1-INV4 are used for the amplification of the signals VP and VN. For maximum amplification, inverters INV1-INV4 are biased around VDD/2 *i.e.,* half of the supply voltage. This causes the short circuit current to flow through these inverters. After the nodes are settled to either VDD or ground, the proposed comparator consumes static power which is negligible. Figure 3.19 (a) shows the current (I_{TG}) flowing through the summing network consisting of transmission gates (TG1-TG4) and charging and discharging current flowing through the tri-state inverter (TRI_INV3) when fully differential input is applied. The average value of I_{TG} is 2.69 µA. The peak value of the charging and discharging current during the transition phase from TRI_INV3 is 4.4 mA and 3.94 mA, respectively. This current charges Cx to 1 V and discharges it to 0.78 V, and the average static current flowing through TRI_INV3 is 0.353 µA. The average power dissipated by the proposed comparator at 200 MHz and 1.8 V supply, is about 160.14 µW as shown in Figure 3.19 (b).



(a)



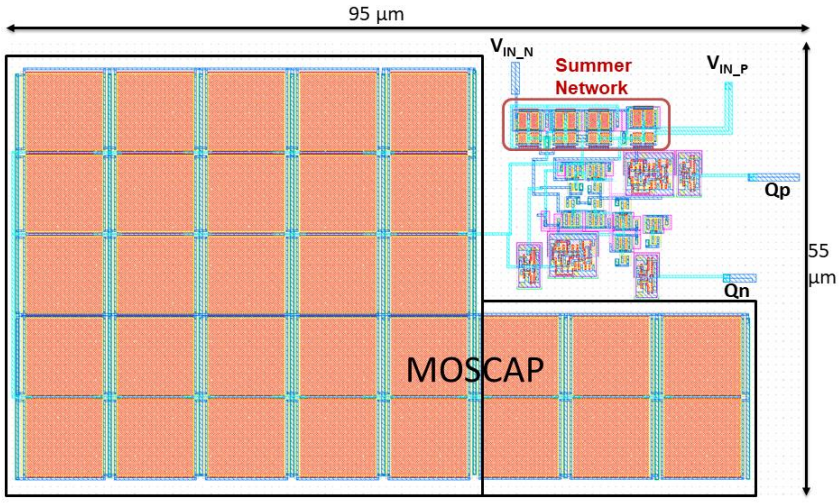
(b) (c)

Figure 3.19 (a) Charging and discharging current of Tri-state inverter (TRI_INV3) present in the feedback loop and the current flowing from transmission gates (TG1-TG4) to Cx (b) Transient analysis to show the current and power of Pseudo-DVC3 (c) Power dissipation for the supply range of 1 V to 1.8 V

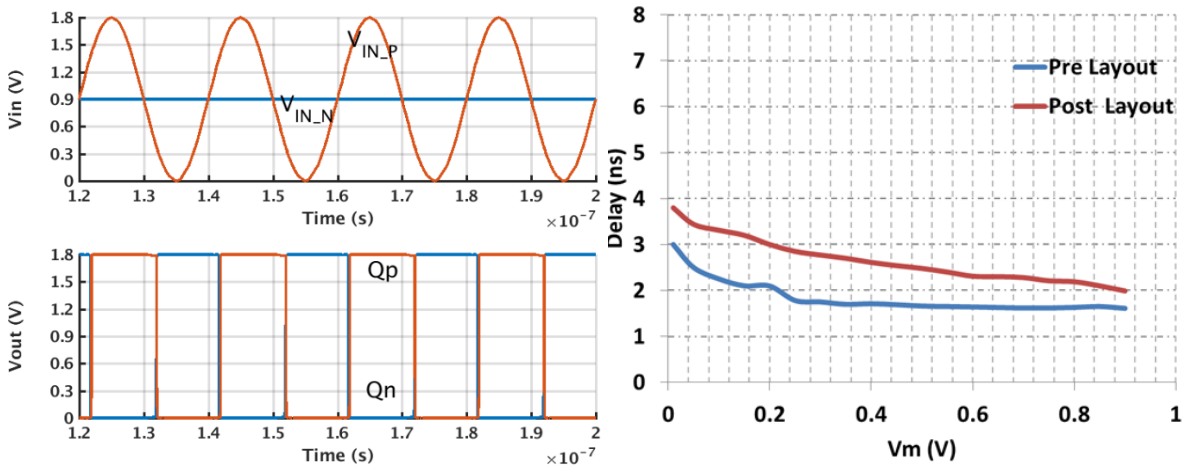
Figure 3.19 (c) shows the variation of power with supply voltage. From this plot, it can be seen that the average powers of 41.2 µW and 160.14 µW have been dissipated at a supply of 1 V and 1.8 V, respectively. Therefore, the proposed comparator can be used in various low voltage applications where power requirement is less.

3.4.4 Layout and Post Layout Simulations

Figure 3.20 (a) shows the layout of the proposed comparator designed in the SCL 180 nm CMOS process. It occupies an area of 5225 µm^2 with dimensions of 95 µm x 55 µm. Figure 3.20 (b) shows the post-layout transient analysis.



(a)



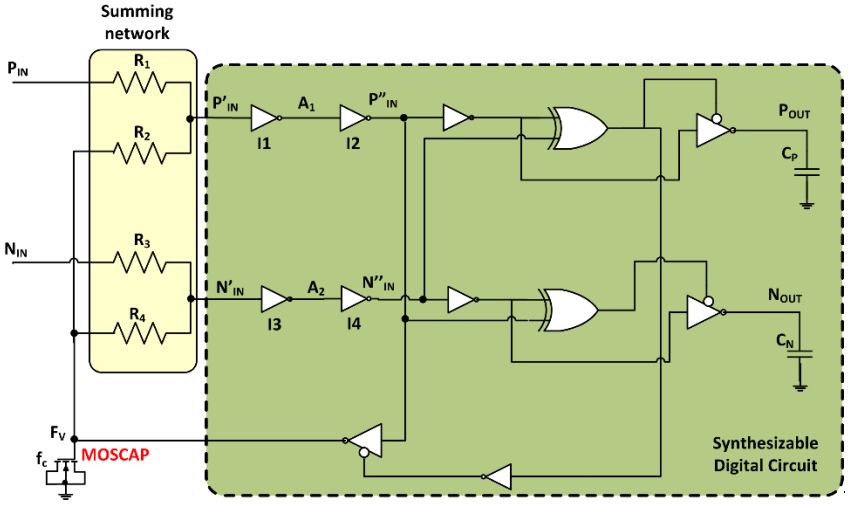
(b) (c)

Figure 3.20 (a) Layout of the Pseudo-DVC3 (b) Post-layout transient analysis of Pseudo-DVC3 (c) Pre-layout and post-layout analysis of delay versus input amplitude

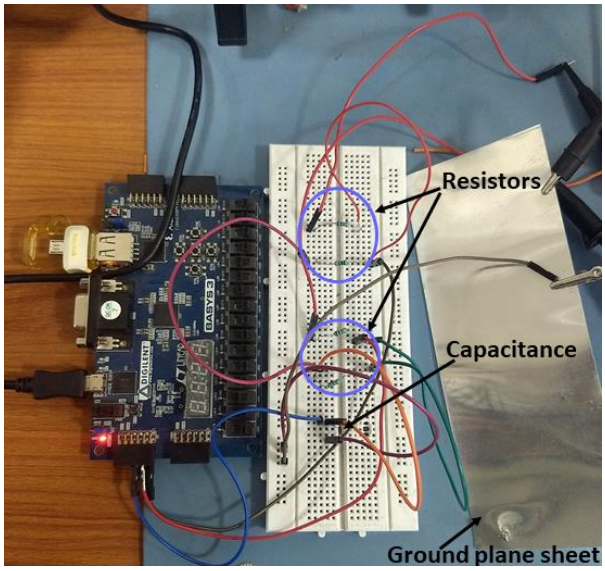
Figure 3.20 (c) shows the pre-layout and post-layout simulations of the delay versus input amplitude of applied sinusoidal. The maximum difference in delay between pre-layout and post-layout is 1ns.

3.4.5 Implementation of Pseudo-DVC3 on FPGA

The full input range voltage supply scalable analog voltage comparator has been implemented on FPGA using other off-the-shelf components (resistances and electrolytic capacitance). Figure 3.21 (a) shows the circuit diagram of differential analog voltage comparator which uses CMOS standard cells such as tri-state inverters, XOR gate, inverters and summing network formed by resistances (R_1-R_2).



(a)



(b)

Figure 3.21 (a) Schematic of voltage comparator Pseudo-DVC3 for FPGA implementation (b) Hardware implementation of Pseudo-DVC3 using physical components

Figure 3.21 (b) shows the hardware implementation of the proposed comparator using FPGA. To prove the synthesizable nature of the proposed analog voltage comparator, the digital part of the proposed Pseudo-DVC3 is implemented on Xilinx Artix-7 FPGA with the help of Basys-3 FPGA kit and Xilinx Vivado software as shown in Figure 3.22. From Table 3.5, it is observed that the proposed comparator consumes only one slice out of available 8150 slices (0.01%) and 2 LUTs out of the existing 20800 LUTs (<0.1%) in Artix-7 FPGA.

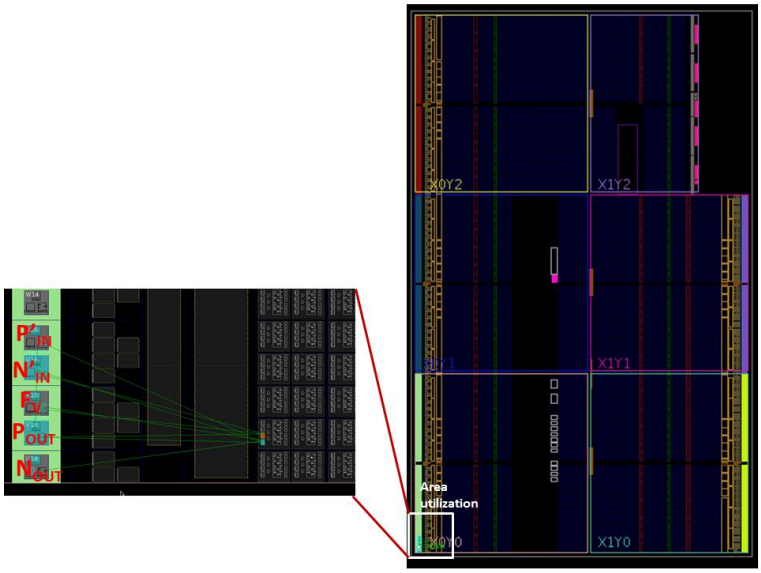


Figure 3.22 Hardware Implementation in Xilinx Artix-7 FPGA

Table 3.5 Core Utilization of the digital part of Pseudo-DVC3

Name	Slice LUTs (20800)	Slice (8150)	LUT as Logic (20800)	Bonded IOB (106)
Comparator	<0.01%	0.01%	<0.01%	4.72%

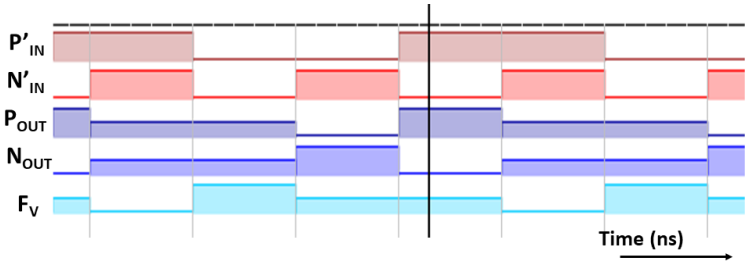


Figure 3.23 Simulation result for the digital part of the Pseudo-DVC3

Figure 3.23 shows the simulation result of the digital part of the proposed Pseudo-DVC3. For testing purposes, both ramp and sinusoidal signals are applied at the input nodes of the comparator by using a function generator. The output has been observed with the help of a mixed-signal oscilloscope. Figure 3.24 presents the testing setup of the proposed analog voltage comparator and its setup in Basys-3 FPGA Kit with a function generator and mixed signal oscilloscope (MSO). The output result of the comparator when two sinusoidal inputs are compared is shown in Figure 3.25 (a). Both the inputs are differential in nature with 1 MHz of input frequency, and an amplitude of 5 Vpp over an offset voltage of 2.5 V. Figure 3.25 (b) shows the change at the output node when the input sinusoidal signal crosses the reference signal. Since, the functionality on an FPGA is implemented through LUTs, better performance can be achieved by implementing the proposed circuit at the application-specific integrated circuit (ASIC) level.

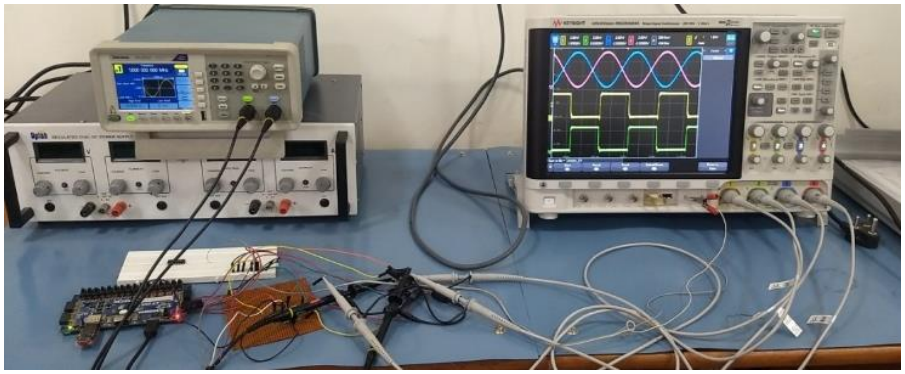
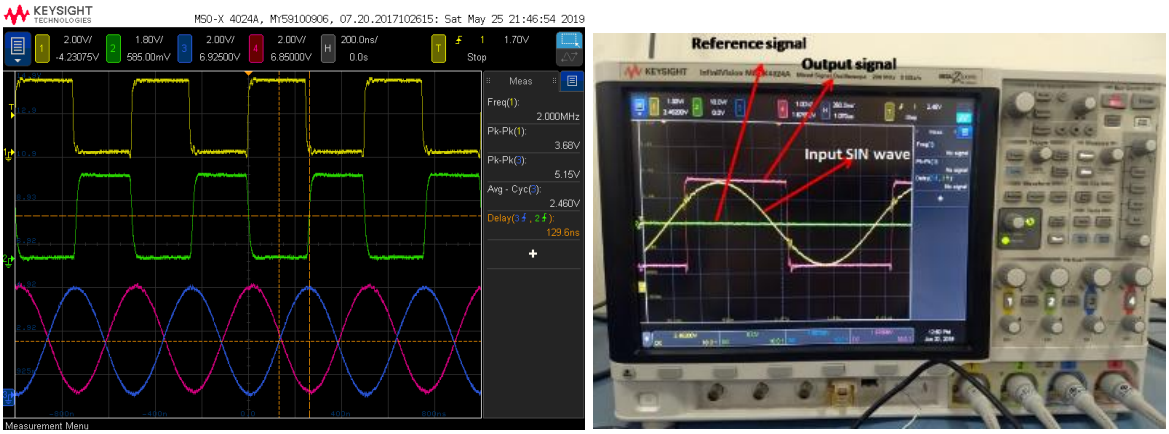


Figure 3.24 Testing setup showing the implementation on FPGA



(a) (b)

Figure 3.25 (a) Experimental waveform obtained by using Basys-3 and off-the-shelf components (b) Transient Simulation results on MSO

The design of proposed analog voltage comparators is based on digital design methodology, which have been compared with the previously available analog and digital-based comparators. Table 3.6 shows the comparative analysis of previously published papers and the proposed comparators explained in this chapter such as Pseudo-DVC1, Pseudo-DVC2 and Pseudo-DVC3. Also, the performance parameters of the proposed voltage comparators and existing voltage comparators are compared on the basis of FOM [138] and listed in Table 3.6. The FOM is expressed in the terms of power, sampling frequency, and ENOB as

$$\text{FOM (fJ/conv)} = \frac{\text{Power}}{2^{\text{ENOB}} * \text{Sampling Frequency}} \tag{3.16}$$

where ENOB is calculated using offset voltage of the comparator [138]. From the table, it can be seen that the proposed comparators have lower FOM than the existing voltage comparators [98-101, 109-110, 113]. The input range of the proposed comparators is rail-to-rail (*i.e.*, 100 %) which is better than many existing designs in the table. The present work proposes three different versions of a fully differential analog comparators using digital design methodology. The delay of the proposed comparators is more for the same technology as compared to the regenerative latch-based dynamic voltage comparator [101, 108, 112, 139] whereas it is lesser than some other prior art designs [16, 100, 109, 110, 114]. The delay of the proposed circuit is mainly limited by the technology used in the design. The offset and power of the proposed circuits are less than the existing comparator for the similar technology [101, 108, 113-114]. The offset and delay of the comparator design given by Ref. [100, 112]

are better than the proposed work because of their pure analog nature. However, they are not scalable to lower technologies. The offset voltage of the proposed digital-based analog comparators is less than the digital designs present in the literature [16, 37]. The power dissipation given by Ref [16, 99] is less than the proposed comparators because of the lower technology node. Also, it is observed that the proposed comparators have lesser power consumption than the existing comparators [100-101, 108, 110, 111, 113-114]. Because of the digital-in-concept power scalable design, the performance of the present comparators can be increased by scaling down the technology. Compared to pure analog implementations [99-101, 108-114, 139], the proposed comparator requires fewer design efforts, can be tuned easily to a target application, and is cost-effective.

Table 3.6 Comparator characteristics of proposed work compared with previous solutions are summarized

Parameter **References**	**CMOS Tech (µm)**	**Design Method-ology**	**Input range**	**Supply Voltage (V)**	**Delay (ns)**	**Avg. power Dissipation (µW)**	**Offset Voltage (mV)**	**Max. Frequency (MHz)**	**FOM (fJ/ conv)**
[16]	0.04	Digital	83%	0.6	3*	1.5	40	-	-
[37]	0.09	Digital	33%	1.2	-	-	45	210	-
[99]	0.18	Analog	30%	1.8	1.21	51	17	100	9.62
[100]	0.18	Analog	-	1.8	4.2	158.5	3.44	50	12.1
[101]	0.18	Analog	41.6%	1.2	0.55	329	7.8	500	8.55
[108]	0.18	Analog	100%	1.8	0.3	554	-	500	-
[109]	0.5	Analog	-	1	4000	44	10	0.25	3518.6
[110]	0.8	Analog	20%	5	17.3	800	77.3	20	1236.3
[111]	0.13	Analog	66%	1	-	600	7.78	-	-
[112]	0.18	Analog	50%	1.8	0.5	150	2.4	500	0.8
[113]	0.18	Analog	41.6%	1.2	0.27	225	7.3	500	5.5
[114]	0.18	Analog	100%	1.8	1.69	460	-	100	-
[139]	0.18	Analog	-	1.8	0.9	158	-	700	-
Pseudo-DVC1	**0.18**	**Partially Digital**	**100%**	**1.8**	**2.9**	**196**	**4.97**	**200**	**5.4**
Pseudo-DVC2	**0.18**	**Partially Digital**	**100%**	**1.8**	**2.5**	**75**	**4.97**	**300**	**1.3**
Pseudo-DVC3	**0.18**	**Partially Digital**	**100%**	**1.8**	**1.63**	**160.1**	**4.28**	**500**	**1.5**

* Delay of the circuit including latch

3.5 Conclusion

In this chapter, the three different versions of digital-in-concept differential voltage comparators (Pseudo-DVC1, Pseudo-DVC2, and Pseudo-DVC3) have been designed and analysed. The proposed comparators have been designed in 180 nm CMOS technology for the supply range of 1 V to 1.8 V. Power, delay and offset are the important performance parameter of proposed analog comparators are discussed in section 3.2, 3.3 and 3.4. It is observed that the proposed pseudo comparators have power dissipation is in the range of 75 µW to 196 µW, an offset voltage less than 4.97 mV with the maximum delay of 2.9 ns. The minimum FOM of the proposed comparators is 1.3 fJ/conv and achieves lower FOM as compared with existing voltage comparators which indicates that the proposed circuit has higher sampling frequency and ENOB with low power. Also, some of the proposed comparators have been implemented on FPGA to validate its functionality. However, these designs are not fully digital, some parts of the circuit are still analog in nature. Therefore, fully digital comparators will be described and discussed in the latter chapters to take the complete technology advantage and time-to-market with optimized performance parameters.

CHAPTER 4

FLASH ADC USING DIGITAL BASED ANALOG COMPARATORS

4.1 Introduction

The flash ADC is widely used for 4-bit to 8-bit resolution and high-speed applications such as automatic test equipment, collision avoidance system, in-home wireless connectivity, defense systems, *etc*. This chapter presents the design of flash ADC using the proposed digital-based analog comparators discussed in chapter 3. Figure 4.1 shows the conventional flash ADC architecture [12], consisting of a resistive ladder, an array of comparators, and an encoder. A N-bit flash ADC requires 2^N resistors, 2^N-1 comparators, and 2^N-1:N encoder. The resistive ladder generates the reference voltages at various nodes, and these reference voltages are compared with the input voltage V_{in} through the comparators. The comparators give the output in the form of thermometer code, *i.e.*, series of 0's and 1's. Further, after passing through the thermometer to the binary encoder, binary output is obtained. The synchronized comparators are used to achieve high data conversion rates.

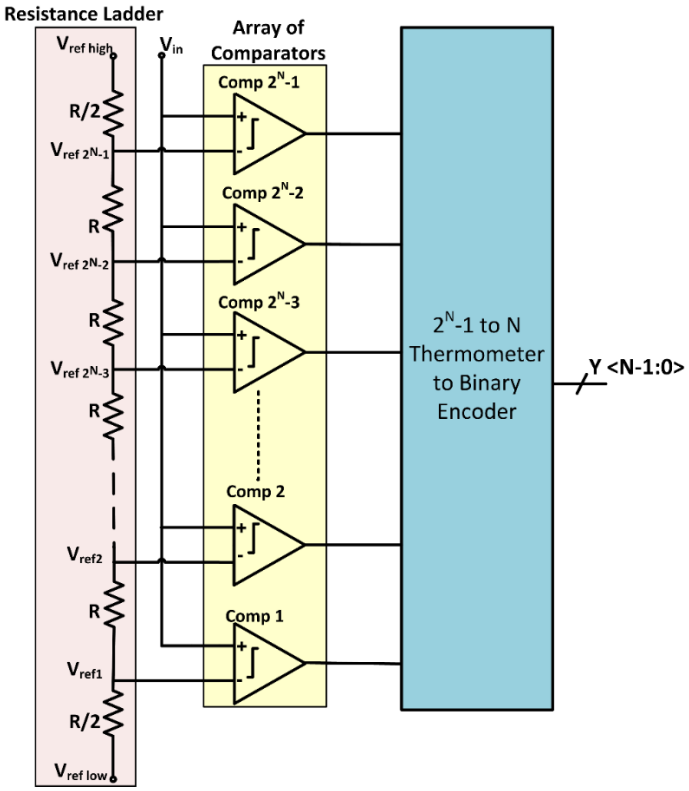


Figure 4.1 Block diagram of N-bit conventional Flash ADC

4.1.1 Resistive Ladder

The resistive ladder is used in the flash ADC to generate the stable reference voltages [12]. This resistive divider equally divides the voltages between the high reference voltage ($V_{ref\,high}$) and the low reference voltage ($V_{ref\,low}$) in $2^N - 1$ voltage levels. It is denoted by the least significant bit (LSB), such as

$$LSB = \frac{V_{ref\,high} - V_{ref\,low}}{2^N} \tag{4.1}$$

For N-bit flash ADC, 2^N resistors are required. The ladder is composed of M equal resistors ($R_1 = R_2 =$ -------- $= R_M$) and can be implemented by using different device resistors such as diffusion resistor, metal resistors or poly resistors. The sheet resistance of diffusion, metal, and polysilicon resistors ranges from 70−120 Ohm/square, 40−80 mOhm/square, and 5−6 Ohm/square, respectively. INL and DNL errors occur due to process variations and mismatches present in the resistors of the resistive ladder. Therefore, the value of INL and DNL must lie within 1 LSB to guarantee a monotonic transfer function with no missing codes. A polysilicon resistor (RNLPOLY2T) is used in proposed ADC designs for better linearity, better voltage and temperature insensitivity than diffusion resistors. In addition, polysilicon resistors consume a lesser area than metal resistors to obtain the same resistance value.

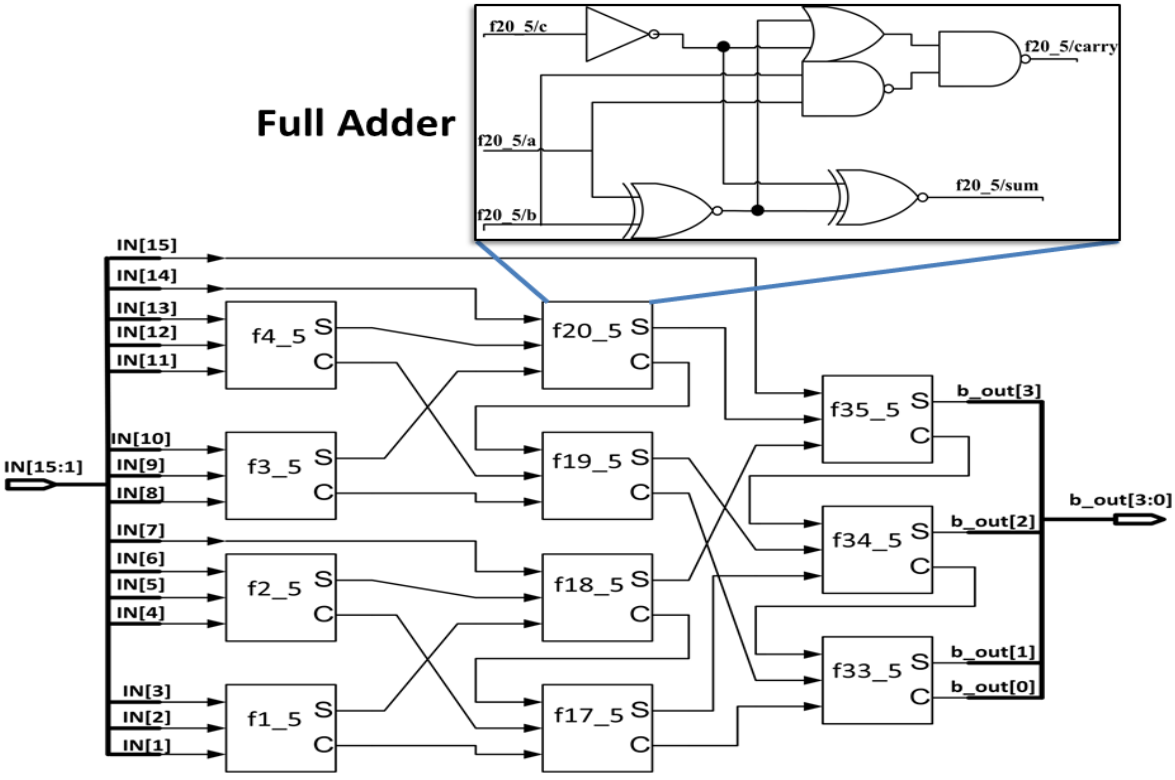
4.1.2 Array of Comparators

The array of comparators compares the reference voltages produced by the resistive ladder with the input signal voltage and generates the output depending upon whether the input voltage is greater or less than the reference voltage. Different digital-based differential analog voltage comparators (Pseudo-DVC1, Pseudo-DVC2, and Pseudo-DVC3) have been designed in chapter 3. These are suitable for flash ADC implementation upto 5-bit resolution. Beyond that, total area consumed by the summing network increases significantly. These proposed comparators work for different frequencies (ranging from 100 MHz to 400 MHz) at the supply voltage of 1 V to 1.8 V. The power consumption of the proposed comparators is ranging from 75 µW to 196 µW for different design configurations. Also, the offset voltage is ranging from 4.28 mV to 4.97 mV, which is sufficient for 4-bit and 5-bit flash ADC with rail-to-rail input swing.

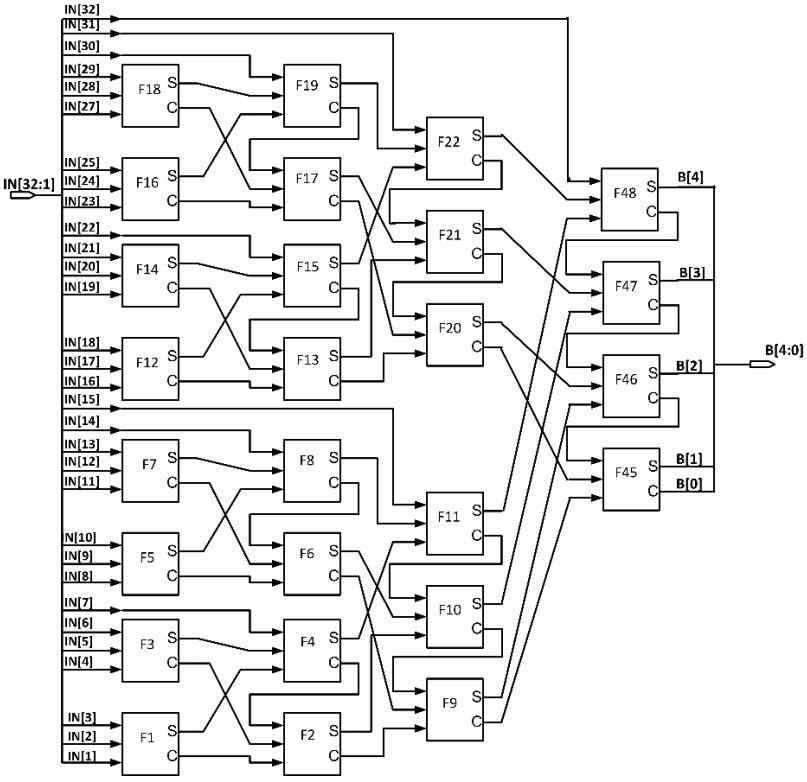
4.1.3 Implementation of Encoder for Flash ADC

One of the challenges in a high-speed flash ADC design is the conversion of the thermometer code to binary code [140]. The encoder is implemented using Wallace tree architecture which comprises of full adders. It is also called one's counter as it counts the number of one's [141-143] and accordingly gives the binary output without any bubble error of higher order. The power dissipation of the Wallace tree encoder is less than ROM based encoder [128]. Another advantage of this encoder is that all the inputs traverse through an equal number of full adders, so the propagation delay is equal. Also, it is flexible and gives good results for any resolution. This circuit is also fully synthesizable where the total number of full adders required for the N-bit encoder is $2^{N} - N - 1$.

Figure 4.2 (a) shows the synthesized design of a 4-bit Wallace tree encoder with an enlarged full adder design. The Synopsys Design Compiler is used to synthesize the encoder. Figure 4.3 (b) shows the block level implementation of the 5-bit Wallace tree encoder structure.



(a)



(b)

Figure 4.2 (a) Block diagram of 4-bit Wallace tree encoder (b) Block diagram of 5-bit Wallace tree encoder

The proposed ADCs have been designed in the Cadence virtuoso analog design environment using SCL (Semi-Conductor Laboratory) 180 nm CMOS technology at a supply voltage of 1.8 V and simulated by using Cadence Spectre and Hspice.

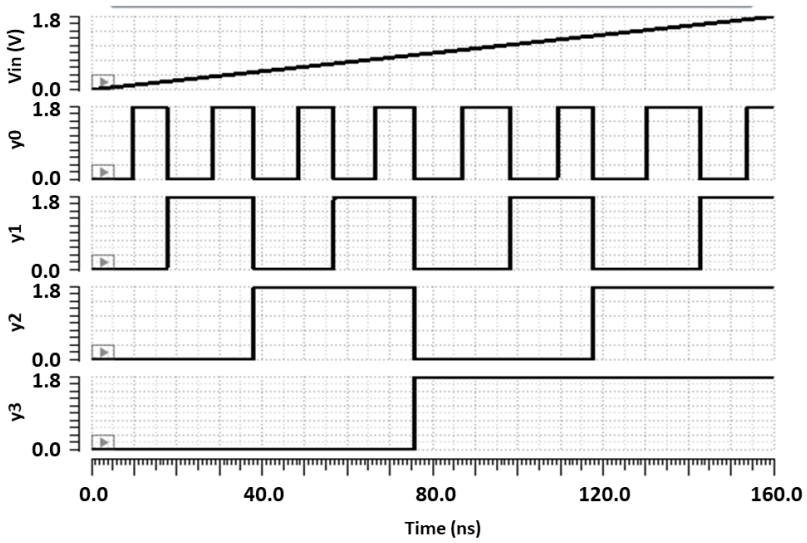
4.2 Implementation of 4-bit Flash ADC using Pseudo-DVC1 (ADC-I)

A 4-bit flash ADC has been designed using a resistive ladder, an array of comparators (Pseudo-DVC1), and an encoder. It has been simulated using HSPICE with SCL 180 nm CMOS process with a supply voltage of 1.8 V. The value of $V_{ref\,high}$= 1.8 V and $V_{ref\,low}$ = 0 V, therefore, the LSB of the proposed 4-bit flash ADC can be written as

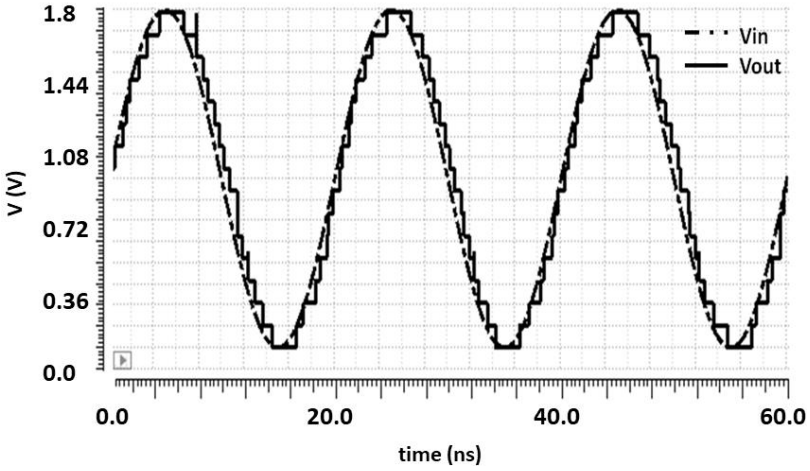
$$\text{LSB} = \frac{1.8\text{ V} - 0\text{ V}}{16} = 112.5\text{ mV} \tag{4.2}$$

Figure 4.3 (a) shows the 4-bit output of the ADC with respect to the input ramp signal, Vin. The transient analysis of complete 4-bit flash ADC with the sinusoidal input at frequency of 50 MHz is shown in Figure 4.3 (b).

The DNL and INL of 4-bit flash ADC are shown in Figure 4.4. From the figure it is observed that the DNL of the proposed flash ADC is ±0.25 LSB and INL is +0.6/−0.1 LSB. Resistance ladder mismatches, gain error, and inconsistent quantization intervals are the most notable of source of non-linearity. Also, the other sources of non-linearity errors considered in the circuit are due to mismatches in the input resistors of comparator, mismatches in the threshold of the inverter that is present at the input side of comparator and mismatches in the rising and falling edges of the comparators. The INL and DNL values are affected by above discussed mismatches.



(a)



(b)

Figure 4.3 (a) Simulation result of 4-bit Flash ADC (ADC-I) with the ramp signal as input (b) Simulation result of 4-bit Flash ADC (ADC-I) with sinusoidal as input where input frequency is 50 MHz

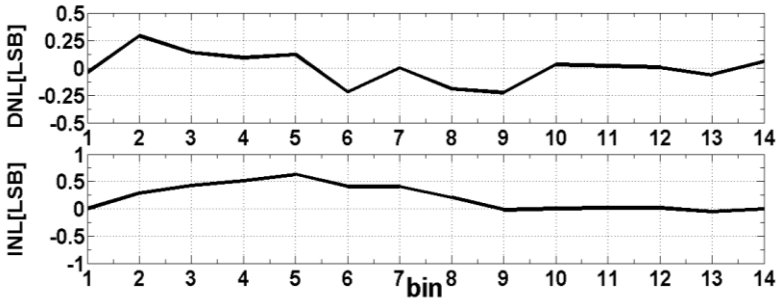
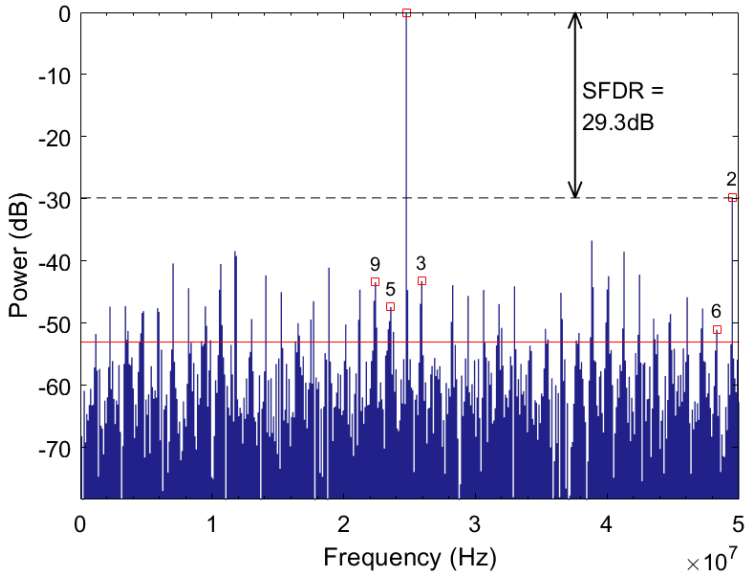
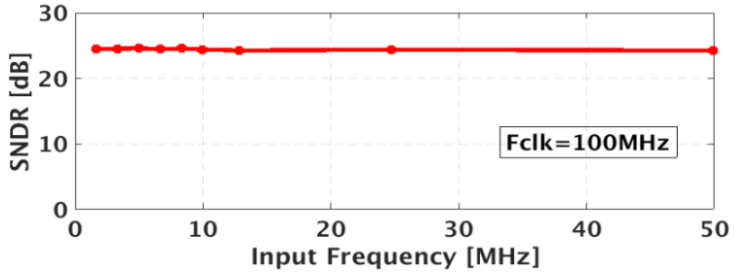


Figure 4.4 INL and DNL of proposed 4-bit Flash ADC (ADC-I)

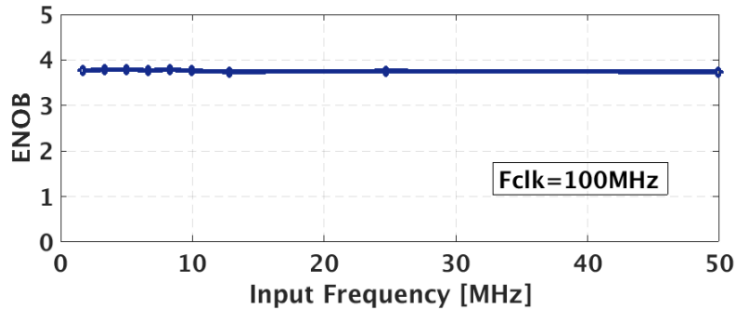
The FFT spectrum of the reconstructed signal is used to calculate the dynamic performance of ADC-I. Figure 4.5 (a) and Figure 4.6 (a) shows the reconstructed signal spectrum for an input signal frequency of 24.21 MHz and 33.2 MHz sampled at 100 MHz and 200 MHz, respectively following the coherent sampling technique. The dynamic performance of the ADC is shown in Figures 4.5 and Figure 4.6. When the input frequency is 24.21 MHz and the clock frequency is 100 MHz, the value of ENOB, SNDR, SNR, and SFDR are obtained as 3.7, 24.03 dB, 25.7 dB, and 29.3 dB, respectively. The value of ENOB, SNDR, SNR, and SFDR are obtained as 3.5, 23.3 dB, 25.2 dB, and 30.1 dB, respectively, when the input frequency is 33.20 MHz at a sampling frequency of 200 MHz.



(a)

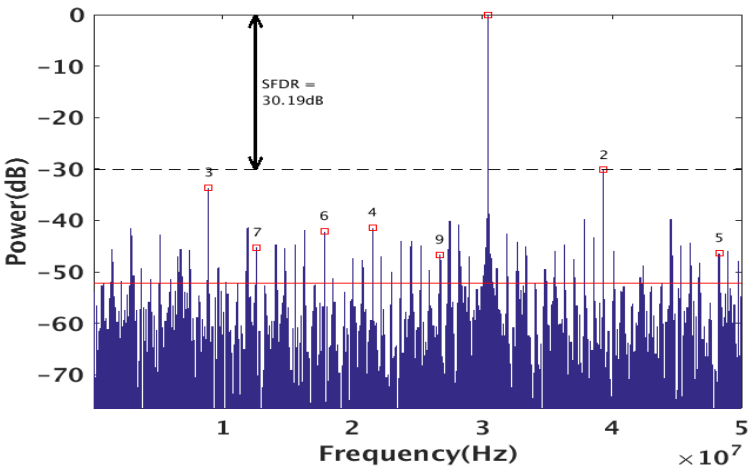


(b)

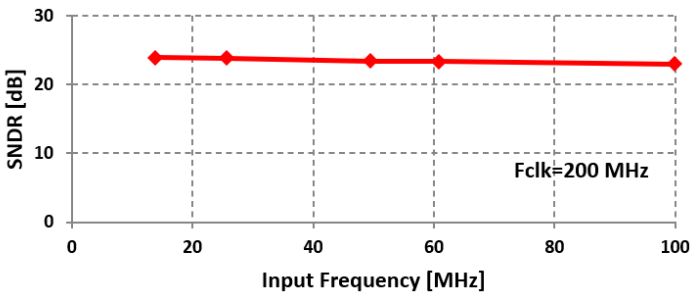


(c)

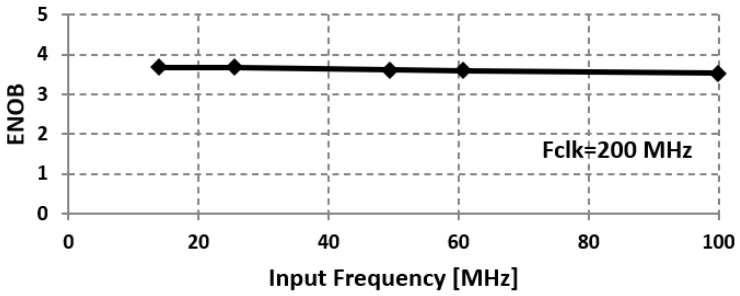
Figure 4.5 (a) FFT of proposed ADC-I at an input frequency of 24.21 MHz (b) SNDR of ADC-I at an input frequency of 24.21 MHz (c) ENOB of ADC-I at an input frequency of 24.21 MHz



(a)



(b)



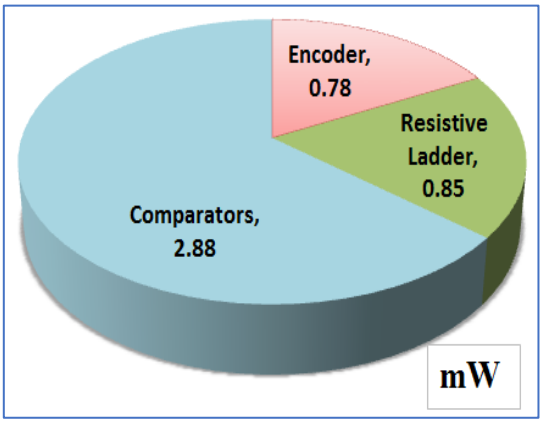
(c)

Figure 4.6 (a) FFT of proposed ADC-I with an input frequency of 33.20 MHz (b) SNDR of ADC-I at an input frequency of 33.20 MHz (c) ENOB of ADC-I at an input frequency of 33.20 MHz

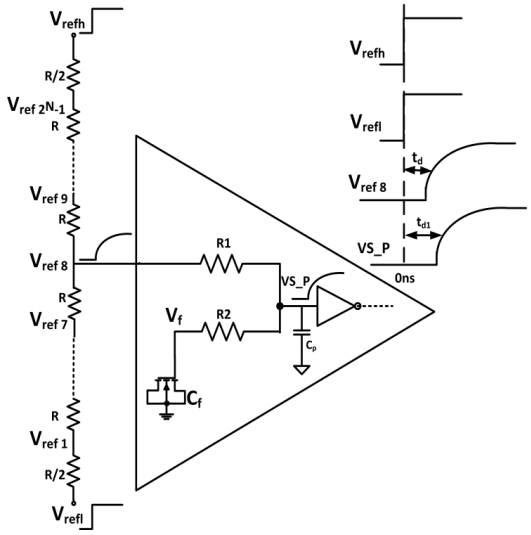
The power consumed by the resistive ladder, comparators, and an encoder are 0.85 mW, 2.88 mW, and 0.78 mW, respectively with a total power consumption of 4.51 mW and are shown in Figure 4.7 (a). Figure 4.7 (b) shows the delay of the resistive ladder. The worst-case delay of the resistive ladder network is observed at the middle node of the reference ladder, *i.e.*, V_{ref8} (shown as t_d) and total delay from node V_{refl} and V_{refh} to VS_P is t_{d1}. Delay is formulated as

$$VS\_P(t) = VS\_P_o(t)\left(1 - e^{-t/\tau}\right) \tag{4.3}$$

Also, $VS\_P_o(t) = V_{refl} + LSB * 2^{N-1}$ with $\tau = \frac{2^{N-1}(2^{N-1}+1)}{2}RC$ and N is the number of bits in flash ADC.



(a)



(b)

Figure 4.7 (a) Power (in mW) of ADC-I (b) Circuit to analyze the delay of resistive ladder and comparator of ADC-I

Table 4.1 Performance of proposed 4-bit flash (ADC-I) using Pseudo-DVC1 at the different clock frequency

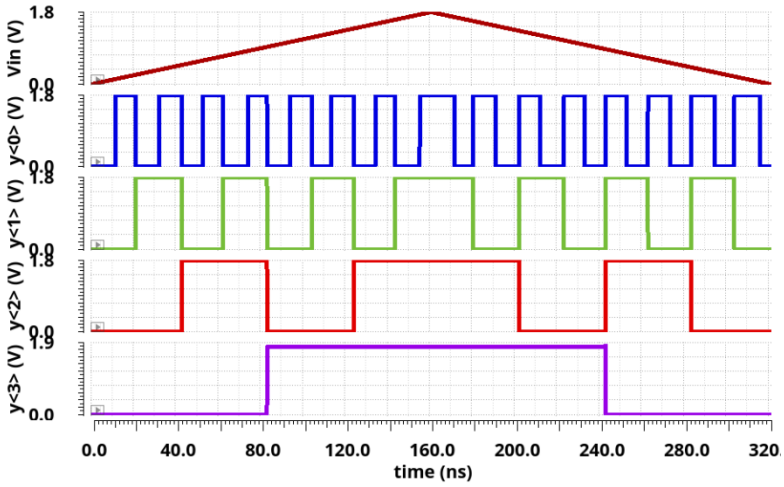
Parameters	**4-bit flash ADC using Pseudo-DVC1 (ADC-I)**	
Resolution	4-bit	
Supply voltage (V)	1.8	
Technology (nm)	180	
Power (mW)	4.51	
DNL (LSB)	± 0.25	
INL (LSB)	+ 0.6/−0.1	
Maximum Sampling Frequency (MHz)	200	
Clock Frequency (MHz)	100	200
Input Signal Frequency (MHz)	24.21	33.20
ENOB (bits)	3.7	3.57
SNDR (dB)	24.03	22.83
SNR (dB)	25.7	25.2
SFDR (dB)	29.3	30.1

The delay of the resistive ladder and comparator is approximately 2.94 ns whereas the delay of the encoder is 1.89 ns. The total delay of ADC obtained is 4.83 ns. Table 4.1 shows the performance parameters of 4-bit flash ADC (ADC-I) using Pseudo-DVC1 at different clock frequencies such as 100 MHz and 200 MHz.

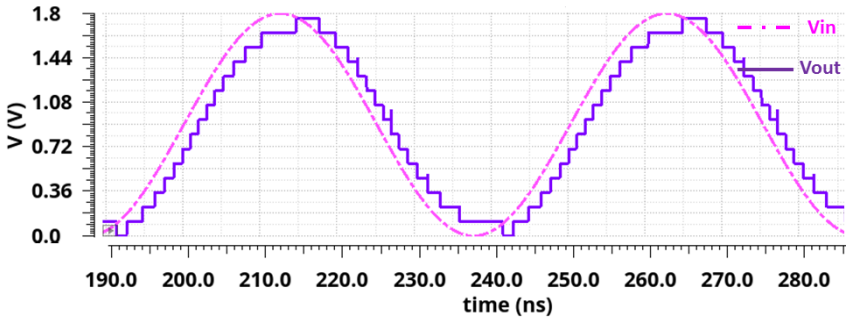
4.3 Implementation of 4-bit Flash ADC using Pseudo-DVC2 (ADC-II)

The proposed 4-bit flash ADC (ADC- II) is implemented using a low power and wide input range differential voltage comparator (Pseudo-DVC2) discussed in section 3.3. As the input range of Pseudo-DVC2 is rail-to-rail swing, hence, an ADC can be designed for 0 V to 1.8 V input range. The value of $V_{ref\,high}$= 1.8 V and $V_{ref\,low}$ = 0 V; therefore, the LSB of the proposed 4-bit flash ADC is 112.5 mV.

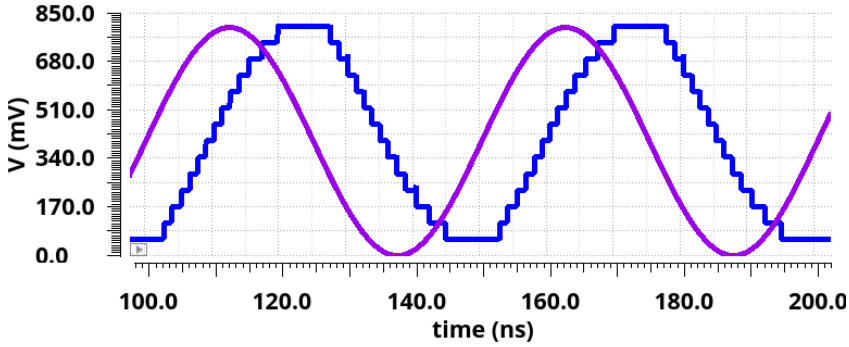
The slow ramp input signal (Vin) is applied at the input to get the digital output y <3:0> as shown in Figure 4.8 (a). Figure 4.8 (b) shows the discrete sinusoidal output both in time and amplitude when the sinusoidal input signal at a frequency of 20 MHz applied at 1.8 V supply voltage. Figure 4.8 (c) shows the output when the supply voltage is reduced to 1 V.



(a)

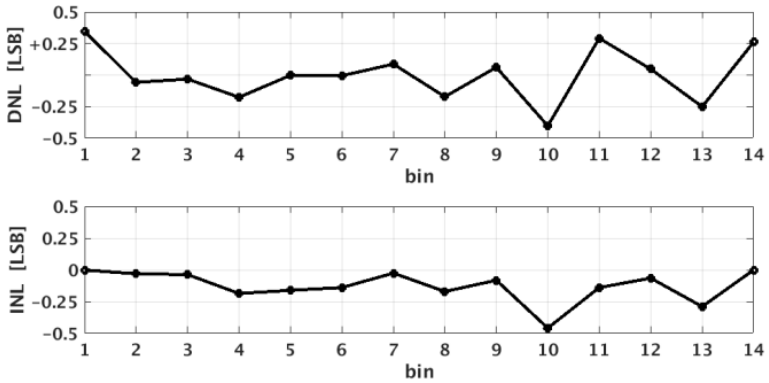


(b)

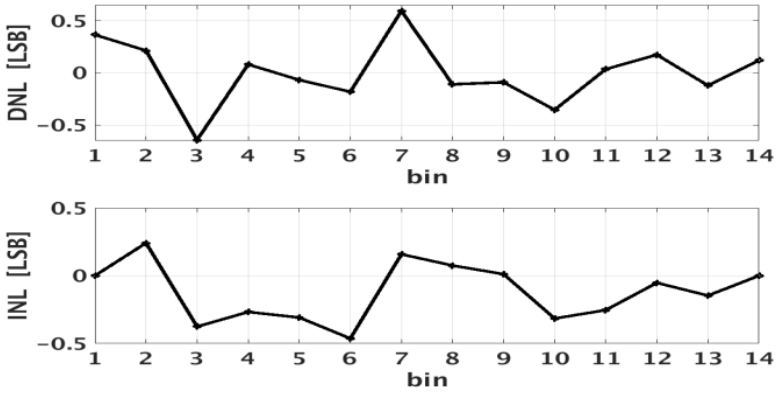


(c)

Figure 4.8 (a) Simulation result of the 4-bit binary output of ADC-II with the ramp signal as input (b) Transient response of ADC-II with 20 MHz sinusoidal input at the supply voltage of 1.8 V (c) Transient response of ADC-II at the supply voltage of 1 V and frequency 20 MHz



(a)

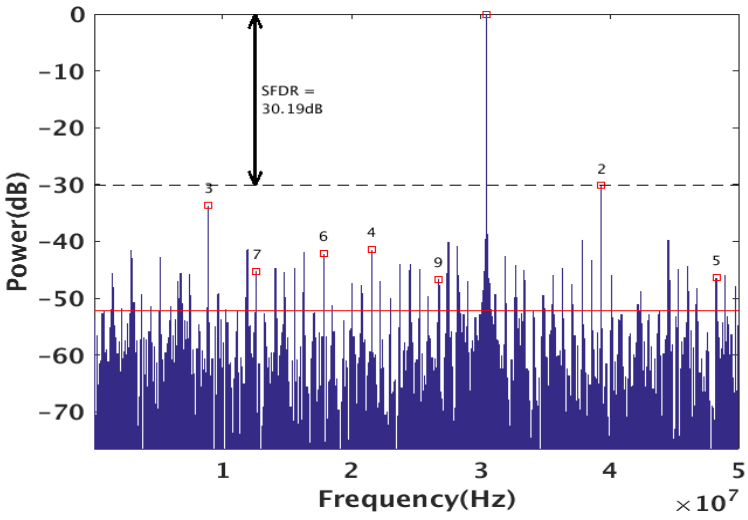


(b)

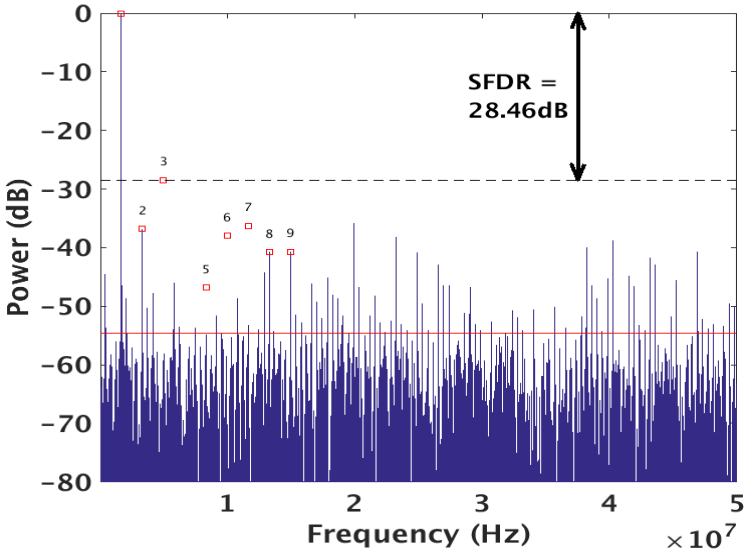
Figure 4.9 (a) INL and DNL at a supply voltage of 1.8 V (b) INL and DNL at a supply voltage of 1 V

Figure 4.9 (a) shows the calculated DNL and INL of the ADC-II. The calculated value of DNL and INL are within ±0.5 LSB for the supply voltage of 1.8 V. Figure 4.9 (b) shows the values of DNL and INL at a supply voltage of 1 V.

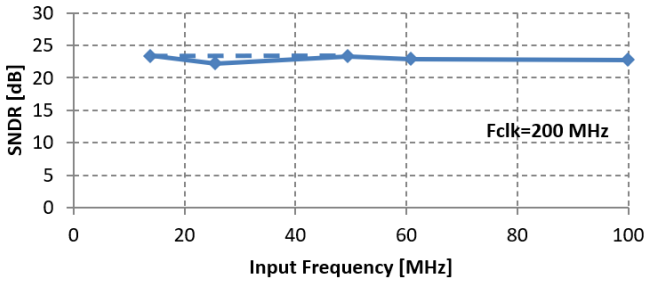
The dynamic performance of the ADC-II is shown in Figures 4.10 (a) and 4.10 (b), where the FFT spectrum of the reconstructed signal is shown for input signal frequencies of 31 MHz at a supply voltage of 1.8 V and 3.2 MHz at a supply voltage of 1 V, respectively. Variation of SNDR and ENOB with respect to input frequency at a sampling frequency of 200 MHz is depicted in Figure 4.10 (c) and Figure 4.10 (d), respectively. It is observed from the figure that the minimum and maximum value of SNDR is 21.8 dB and 23.41 dB, respectively, whereas the minimum and maximum value of ENOB is 3.49 and 3.6, respectively.


SFDR =
30.19dB
Power(dB)
Frequency(Hz)
×10^7

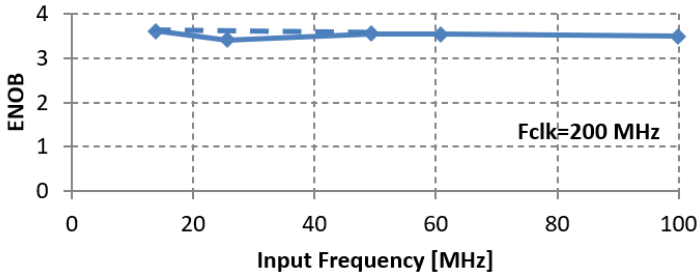
(a)


SFDR =
28.46dB
Power (dB)
Frequency (Hz)
×10^7

(b)


SNDR [dB]
Fclk=200 MHz
Input Frequency [MHz]

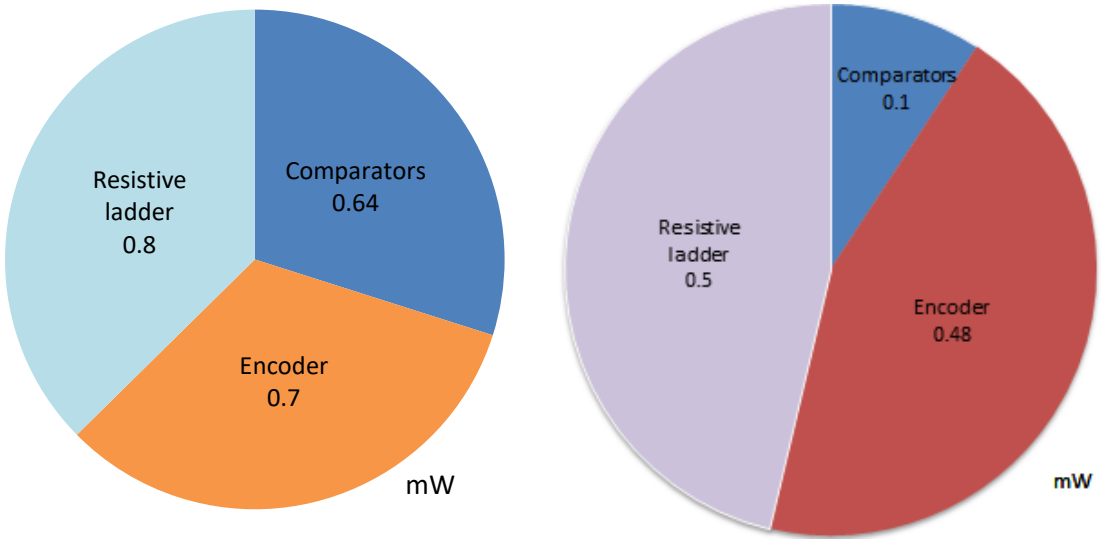
(c)



(d)

Figure 4.10 (a) FFT of proposed ADC-II with input frequency of 33.20 MHz at the supply voltage of 1.8 V (b) FFT of proposed ADC-II with input frequency of 3.2 MHz at the supply voltage of 1 V (c) Variation of SNDR (dB) with input frequency at a clock frequency of 200 MHz (d) Variation of ENOB with the input frequency at a clock frequency of 200 MHz

Figure 4.11 (a) and (b) shows the total power consumed by individual blocks of 4-bit flash ADC-II with the total power consumption of 2.14 mW at a supply voltage 1.8 V and 1.08 mW at a supply voltage 1 V, respectively. The total measured value of the delay is 3.6 ns, where the delay of encoder and comparator is 1.89 ns and 1.45 ns, respectively at a supply voltage 1.8 V.



(a) (b)

Figure 4.11 (a) Calculated power (in mW) of 4-bit flash ADC (ADC-II) at the supply voltage of 1.8 V (b) Calculated power (in mW) of 4-bit flash ADC (ADC-II) at the supply voltage of 1 V

Table 4.2 Simulations results of the proposed 4-bit flash ADC (ADC-II) using Pseudo-DVC2

Parameters	**4-bit flash ADC using Pseudo-DVC2 (ADC-II)**	
Supply voltage (V)	1.8	1
Resolution	4-bits	4-bits
Sampling Frequency (MHz)	200	200
Power (mW) @ 200 MHz	2.14	1.08
SNDR (dB)	23.43	22.83
SNR (dB)	25.2	24.63
SFDR (dB)	30.19	28.46
INL (LSB)	±0.5	±0.5
DNL (LSB)	±0.4	+0.6/−0.2
ENOB (bits)	3.6	3.5

Table 4.2 shows the various performance parameters of ADC-II at a supply voltage of 1 V and 1.8 V. It is observed from the table that the total reduction in power is approximately 50 % when operated at a supply of 1 V without much degradation in other performance parameters.

In this section, 4-bit flash ADC (ADC-II) utilizing the advantage of the digital-based analog comparator (Pseudo-DVC2) is implemented. Due to its low power and high speed, this can be a potential candidate for various low power applications.

Furthermore, the Table 4.3 demonstrates the comparative analysis of the proposed 4-bit flash ADC (ADC-I and ADC-II) with the state-of-art published conventional flash ADCs. The performance parameters of the proposed ADCs (ADC-I and ADC-II) and existing ADCs are compared on the basis of FOM (pJ/conv.) using equation (1.11) and listed in Table 4.3. From the table, it can be seen that the proposed ADCs have lower FOM than the existing ADC [26, 29, 49, 76-79]. The power consumed by ADC-I and ADC-II is less as compared to other pre-existing ADCs [26, 29, 49, 76-80]. The enhancement in the speed can be achieved by using the lower CMOS technology. This digital approach requires less design efforts and takes less time-to-market as compared to its analog counterpart.

Table 4.3 Comparison of proposed 4-bit flash ADC (ADC-I and ADC-II) with existing ADC circuits

Parameters	Technology	No. of bits	DNL (LSB)	INL (LSB)	ENOB	Sampling Frequency (MHz)	Power (mW)	FOM* (pJ/conv.)
[26]	180 nm	4	<0.47	<0.46	3.47	4000	530	11.9
[29]	90 nm	4	<0.38	<0.53	3.69	1500	23	1.18
[49]	180 nm	5	<0.6	0.218	4.78	400	18.62	1.69
[76]	180 nm	4	-	-	-	500	24.26	3.1
[77]	180 nm	4	0.4	1.1	3.24	400	20	5.3
[78]	130 nm	5	<0.24	<0.39	4.44	200	120	27.6
[79]	350 nm	4	0.2/-0.5	0.2/-0.9	-	200	12.4	3.8
[80]	250 nm	4	± 0.65	+0.45/−0.5	3.56	1200	3.24	-
ADC-I	**180 nm**	**4**	**± 0.25**	**+0.6/−0.1**	**3.57**	**200**	**4.51**	**1.89**
ADC-II	**180 nm**	**4**	**±0.4**	**±0.5**	**3.6**	**200**	**2.14**	**0.88**

$$*\text{FOM}=\frac{\text{Power}}{2^{\text{ENOB}} * \text{Sampling Frequency}}$$

4.4 Implementation of 4-bit flash ADC (ADC-III) and 5-bit flash ADC (ADC-IV) using Pseudo-DVC3

In order to use the voltage supply scalable analog comparator Pseudo-DVC3 (discussed in section 3.4) in a flash ADC, a 4-bit flash ADC (ADC-III) has been implemented which is further extended to the 5-bit flash ADC (ADC-IV). Various performance parameters have been analyzed in this section to validate 4-bit and 5-bit flash ADCs. Figure 4.12 shows the transient analysis of 4-bit flash ADC-III where a slow triangular signal is provided at the input to obtain the digital output (M3-M0). Figure 4.13 shows the simulated DNL and INL of the converters. The calculated DNL and INL is ± 0.4 LSB and ± 0.4 LSB, respectively for ADC-III. For 5-bit flash ADC, the measured DNL is ±0.42 LSB and INL is +0.6/−0.2 LSB, respectively.

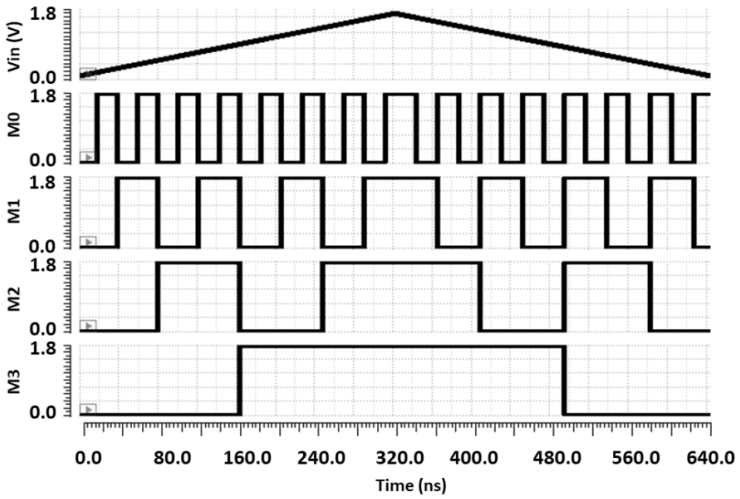


Figure 4.12 Transient simulation of 4-bit Flash ADC (ADC-III)

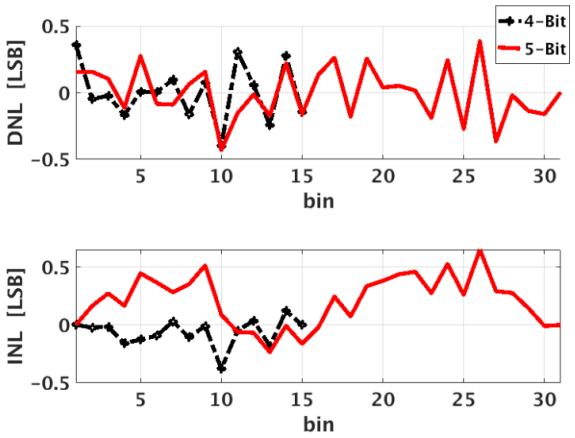


Figure 4.13 Simulation result of INL and DNL for 4-Bit ADC-III and 5-Bit ADC-IV

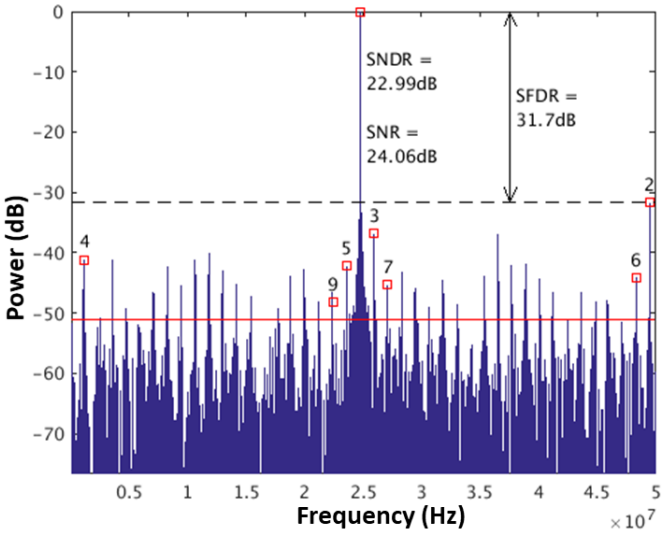


Figure 4.14 FFT of 4-bit flash ADC (ADC-III) at the input frequency of 24.21 MHz

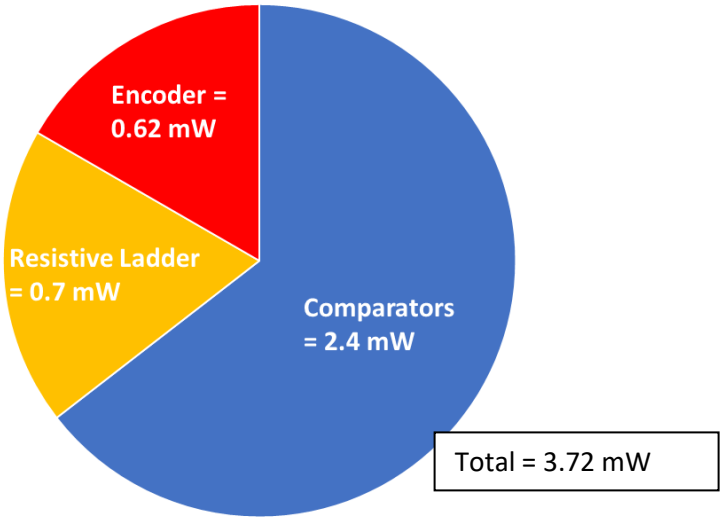


Figure 4.15 Power (in mW) for different components in 4-bit Flash ADC (ADC-III)

The FFT of 4-bit flash ADC is depicted in Figure 4.14 at an input frequency of 24.21 MHz and sampling frequency of 400 MHz to show the dynamic performance. The calculated value of ENOB, SFDR, SNDR, and SNR is 3.52, 31.7 dB, 22.99 dB, and 24.06 dB, respectively. Figure 4.15 shows the total power consumed by the 4-bit flash ADC is 3.72 mW.

Figure 4.16 shows the transient analysis of 5-bit flash ADC-IV. The FFT response of 5-bit flash ADC is obtained for an input signal frequency of 24.21 MHz when sampled at 400 MHz as shown in Figure 4.17. The archived values of SFDR, SNDR, ENOB, and SNR are 38.96 dB, 30.59 dB, 4.78, and 31.27 dB, respectively with a total power consumption of 6.14 mW, as shown in Figure 4.18.

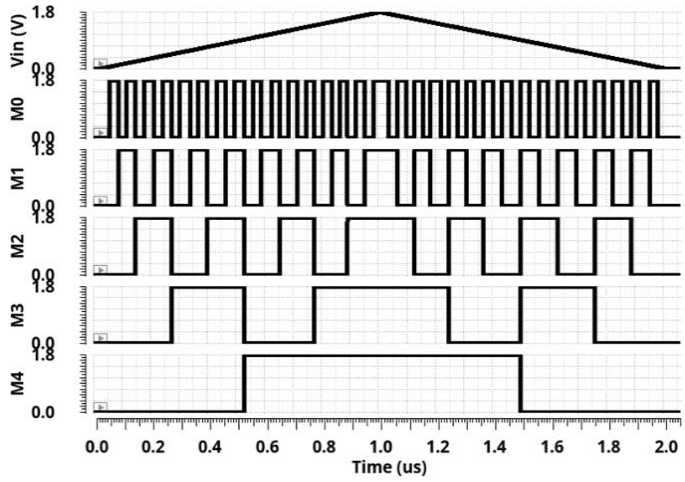


Figure 4.16 Transient simulation of 5-bit Flash ADC (ADC-IV)

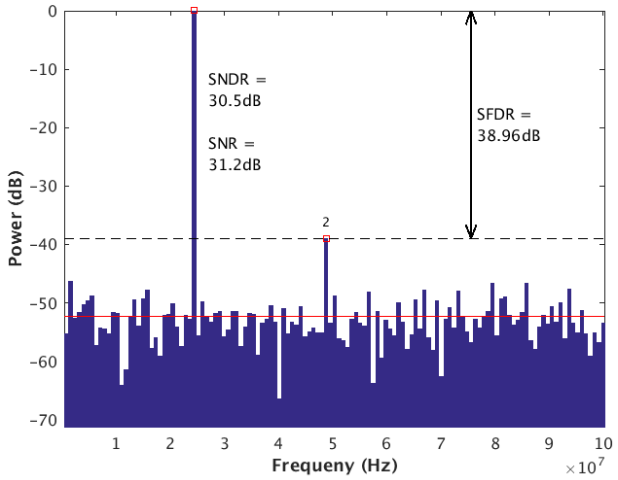


Figure 4.17 FFT response of 5-bit ADC-IV at an input frequency of 24.21 MHz

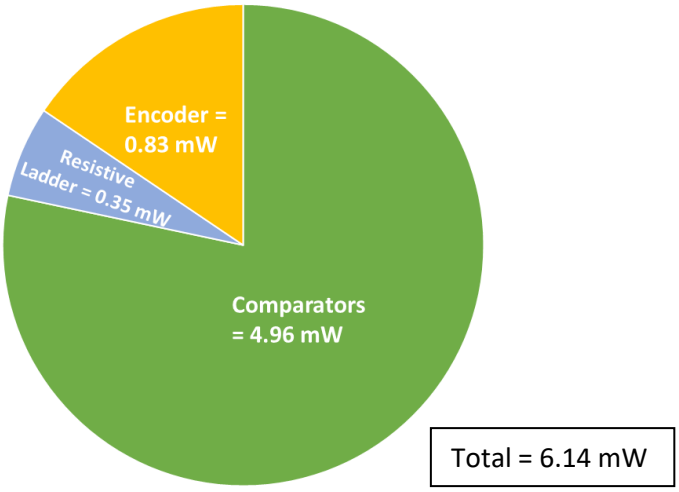


Figure 4.18 Power consumed by different blocks in 5-bit Flash ADC (ADC-IV)

Table 4.4 shows the comparison of ADC-III and ADC-IV using the proposed comparator (Pseudo-DVC3) with previously published designs. The power consumption is lesser than the other reported works for both 4-bit and 5-bit resolution. It is also observed that at a sampling rate of 400 MHz, all the static and dynamic parameters of both ADC-III and ADC-IV are better than the reported by Banik et al. [77]. The 5-bit flash ADC in the presented work has lesser power consumption and improved INL and DNL than the existing flash ADCs [81-82]. Further, it has also been observed that the 5-bit flash ADC in the present work has higher ENOB, SNDR, and SFDR as compared to the earlier reported work [81-82]. Also, it is can be seen that the presented work has less FOM than the existing ADCs [29, 49, 54, 69, 77-79, 81].

Table 4.4 Comparison of the 4-bit flash ADC (ADC-III) and 5-bit flash ADC (ADC-IV) implemented using Pseudo-DVC3 with previously published designs

Parameters	This Work		[29]	[54]	[77]	[41]	[49]	[69]	[78]	[81]	[82]
	ADC-III	ADC-IV									
Resolution (bits)	**4**	**5**	4	4	4	5	5	5	5	5	5
Supply Voltage (V)	**1.8**	**1.8**	1.2	2.5	1.8	1.8	1.8	1.8	1.2	1.8	1.2
Technology (nm)	**180**	**180**	90	500	180	180	180	180	130	180	130
Methodology	**Highly Digital**	**Highly Digital**	Analog	Analog	Analog	Analog	Digital	Analog	Analog	Time Domain	Analog
Sampling Rate (MHz)	**400**	**400**	1500	800	400	5000	400	400	2000	500	1800
INL (LSB)	**±0.4**	**+0.6/−0.2**	<0.53	0.4	1.1	+0.7/ -1.0	0.218	1.7	<0.39	<0.43	<0.66
DNL (LSB)	**±0.4**	**±0.42**	<0.38	0.42	0.4	+1.07/ -0.58	0.206	1	<0.24	<0.58	<0.64
ENOB (bits)	**3.52**	**4.78**	3.69	3.34	3.24	-	4.78	3.89	4.44	4.13	4.57
SFDR (dB)	**31.7**	**38.96**	-	34	27.6	-	42.05	30.7	37	35.1	37.6
SNDR (dB)	**22.99**	**30.59**	-	25.71	21.25	-	30.56	25.2	27	26.6	-
SNR (dB)	**24.06**	**31.27**	-	24.4	-	-	-	-	-	-	-
Power (mW)	**3.72**	**6.14**	23	7	20	340	18.63	16	120	8	76
FOM (pJ/conv.)	**0.81**	**0.55**	1.18	0.86	5.2	2.12	1.69	2.69	2.84	0.91	1.77

Table 4.5 summarises the performance parameters achieved by the proposed 4-bit and 5-bit flash ADCs (ADC-I, ADC-II, ADC-III, and ADC-IV) using digital-in-concept comparators (Pseudo-DVC1, Pseudo-DVC2, and Pseudo-DVC3). The proposed 4-bit and 5-bit ADCs are working for the frequency ranging from 200 MHz to 400 MHz. ADC-I dissipates more power in comparison to ADC-II, ADC-III, and ADC-IV. The lowest power is achieved by ADC-II which is 1.08 mW at a supply voltage of 1V with a sampling frequency of 200 MHz. The speed of the ADC is further enhanced, i.e., 400 MHz in ADC-III and ADC-IV as compared to 200 MHz for ADC-I and ADC-II.

Table 4.5 Summary for the comparison of the proposed flash ADCs

Parameters	**ADC-I**		**ADC-II**		**ADC-III**	**ADC-IV**
Resolution	4-bit		4-bit		4-bit	5-bit
Supply voltage (V)	1.8		1.8	1	1.8	
Technology (nm)	180		180		180	
Power (mW)	4.51		2.14	1.08	3.72	6.14
INL (LSB)	± 0.25		±0.5	±0.5	±0.4	+0.6/−0.2
DNL (LSB)	+ 0.6/−0.1		±0.4	+0.6/−0.2	±0.4	±0.42
Maximum Sampling Frequency (MHz)	200		200	200	400	400
Sampling Frequency (MHz)	100	200	200	200	400	400
Input Signal Frequency (MHz)	24.21	33.20	33.2	3.2	24.21	24.21
ENOB (bits)	3.7	3.57	3.6	3.5	3.52	4.78
SNDR (dB)	24.03	22.83	23.43	22.83	22.99	30.59
SNR (dB)	25.7	25.2	25.2	24.63	24.06	31.27
SFDR (dB)	29.3	30.1	30.19	28.46	31.7	38.96

4.5 Conclusion

The implementation and simulation of the proposed ADC-I, ADC-II, ADC-III, and ADC-IV have been discussed in this chapter. The 4-bit flash ADCs have been designed using Pseudo-DVC1 and Pseudo-DVC2 at a clock frequency of 200 MHz. Further, 4-bit flash ADC and 5-bit flash ADC have been designed at a sampling frequency of 400 MHz using Pseudo-DVC3. The main focus of this chapter is to achieve low power, high resolution, and high-speed flash ADC using digital-based analog comparators. The power of ADC-I is 4.51 mW with an SNDR of 22.83 dB at the clock frequency of 200 MHz. It is also observed that among ADC-I and ADC-II, ADC-II dissipates lesser power for the same supply voltage and sampling frequency. Also, the speed of ADC-III and ADC-IV is higher and can be suitable for low-power high-speed SoC applications with reduced time-to-market. The ADC-IV achieves lowest FOM as compared to existing ADCs and proposed ADCs which confirms its better performance. As these ADCs are not fully digital to take all the benefits of the digital design methodology, the following chapter describes all-digital flash ADC with improved static and dynamic performance parameters.

CHAPTER 5

ALL DIGITAL 6-BIT FLASH ANALOG-TO-DIGITAL CONVERTER

5.1 Introduction

In the last decades, most communication systems such as radios, telephones, mobiles, and televisions were communicating through analog signals, as the information desired to send and receive is continuous [7, 11]. With the advancement in IC technology, digital signal processing has attained more demand than analog signal processing. Analog designs, on the other hand, are made in a custom fashion, which means that the time spent on designing analog circuits is longer than digital standard cell-based designs. Therefore, converting an analog signal into a digital signal for digitally processing the analog signals is required. These conversions are done with the help of an ADC. But, in ADC designs, the layouts of the analog and digital parts must be separated, which necessitates extra effort at the system integration level. Also, digital ICs are more advantageous than analog ICs in the exploding market of new lightweight and portable devices. Being digital-in-concept, the digital designs are robust, power-efficient, less prone to PVT variations and require fewer design efforts. Hence time-to-market is less and easily tuneable to lower technologies. Thus, trending research is motivated towards the implementation of the analog/mixed-signal circuits using digital-in-concept design methodology. In this chapter, a flash ADC is reconstructed using the digital methodology and taking advantage of automated synthesis, place, and route, which further reduces the design time and efforts.

The comparator is the crucial component of any ADC, which is the central unit to convert analog signals into digital signals. The flash ADC is selected as it consists of a analog-in-concept voltage reference ladder and analog-in-concept comparators and a digital block encoder. A voltage reference ladder generates the reference voltages which are compared with the applied input signal and converted to digital outputs through the comparators. There are different ways to generate the reference voltages in literature, such as using the resistive ladder [144] and analog interpolation technique [145], but the concept to generate the reference voltage for each comparator is almost the same. J. Ceballos *et al.* [24] presented the first novel way to eliminate the reference ladder circuit and used the concept of input-referred offset voltage due to mismatches in the circuit as the reference voltages for the

comparator. This concept of input-referred offset voltage is used in further research work but the number of comparators used in the ADCs are high [29-31, 37, 146]. S. Weaver [37] *et al.* proposed a digital standard cells-based voltage comparator. Using this comparator, a stochastic flash ADC is introduced where the number of comparators is high and the input voltage range is limited. A. Fahmy *et al.* [40] proposed an all-digital wide input range stochastic ADC. The input range of this circuit is more, but the rail-to-rail input swing is not obtained (800 mVpp). Min *et al.* [51] presented a reference swapping technique between two groups of comparators for linearization in stochastic flash ADC. The effective number of bits is improved in this linearization technique, but the input range is still less (440 mVpp). Also, some synthesizable voltage comparators for ADCs to obtain full input range are reported, but complexity and area of the ADCs are high [16, 119].

This chapter aims to design an all-digital wide input range 6-bit flash ADC to overcome the above problems in flash ADC. In this design, an all-digital voltage reference ladder for the ADC is implemented. The proposed voltage reference ladder consists of delay-based network and time-to-voltage converters (TVCs). Besides the reference ladder, all-digital rail-to-rail analog voltage comparators are also realized and the array of comparators generate thermometer code. The Wallace tree encoder is finally used to convert thermometer code to binary bits. After that the 6-bit flash ADC has been implemented using Cadence virtuoso in SCL 180 nm CMOS technology at the supply voltage of 1.8 V.

5.2 Flash ADC Architecture

Figure 5.1 (a) shows the conventional flash ADC which consists of resistive ladder, array of comparators, and an encoder. For N-bit ADC, 2^{N} resistors, $2^{\mathrm{N}}-1$ comparators and a $2^{\mathrm{N}}-1{:}\,\mathrm{N}$ encoder are required. A resistance-based reference ladder is used to generate the reference voltage for each comparator, which is a 1 LSB difference from its consecutive reference voltage. Figure 5.1 (b) shows the proposed N-bit flash ADC architecture. The resistance-based voltage reference ladder has been replaced with a digital-in-concept voltage reference ladder followed by a gate-based comparator and an encoder in the proposed design.

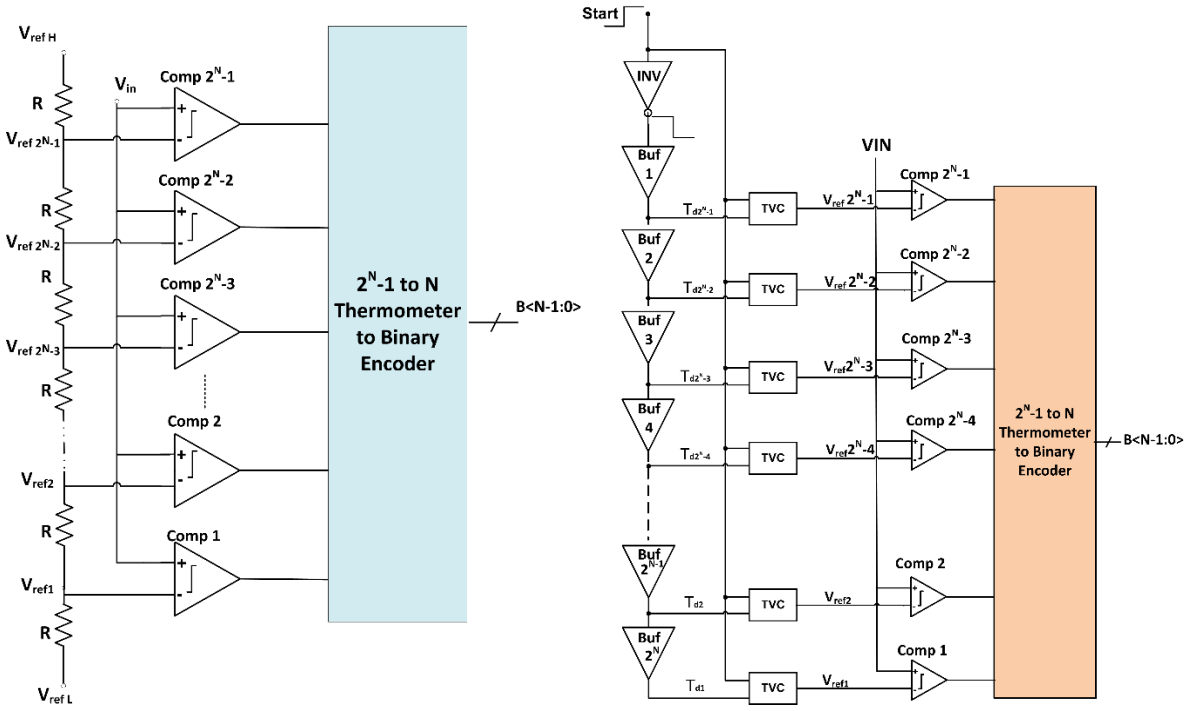
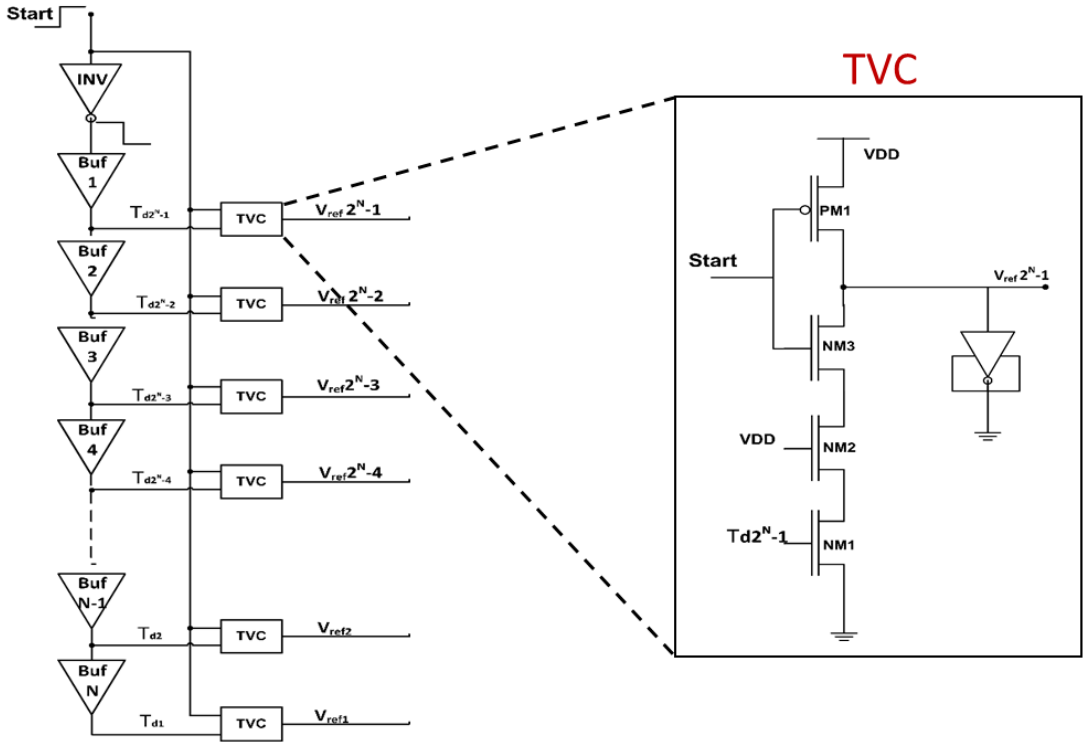


Figure 5.1 (a) Conventional flash ADC architecture (b) Proposed flash ADC architecture

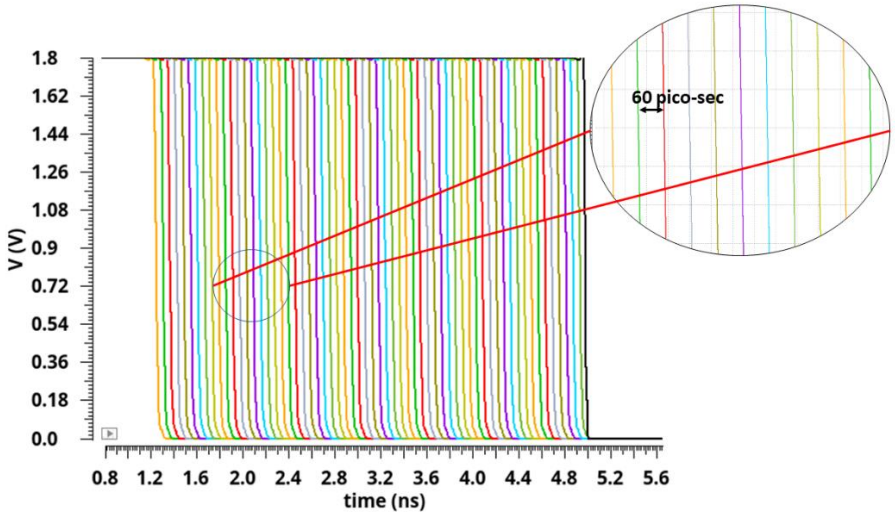
5.3 Implementation of All-digital Voltage Reference Ladder for Flash ADC

A few fundamental changes must be made to the conventional flash ADC architecture to design an all-digital flash ADC. First of all, the passive component-based reference ladder must be replaced by active digital-based components. For this, a combination of delay-based network and time-to-voltage converters (TVCs) is used in this architecture to generate a reference voltage, as shown in Figure 5.2 (a). A buffer is used to generate delay signals in relation to the start signal. Initially, the rising edge start signal (rising from 0 V to 1.8 V) is inverted through an inverter INV and provides a falling edge signal. Then, 2^N buffers are connected in series to obtain the delayed signals T_{d2^N-1} to T_{d1}. Figure 5.2 (b) shows that each signal is delayed by the delay of buffer which is 60 ps in the present SCL 180 nm CMOS technology. In order to see the effect of process variations and mismatches on the delay-based reference ladder, Monte Carlo simulations are performed which shows the variation in the delay-based reference ladder is negligible and is shown in Figure 5.2 (c). The mean value of the delay is 60 ps and the standard deviation is 321.62 fs. After that, the obtained delayed signals and reference start signal are feed to an array of TVC.

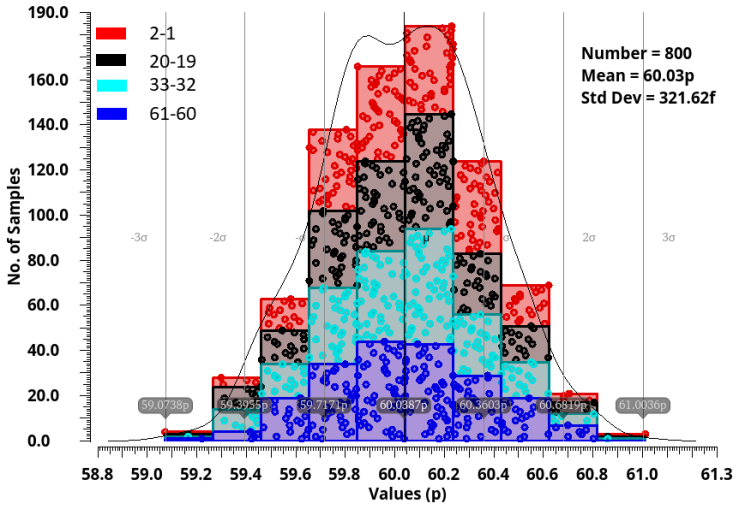
Figure 5.2 (d) shows that each delayed signal is compared with the start signal to generate a reference voltage. In order to generate 2^{N-1} reference voltages, a total of 2^{N} buffers and 2^{N-1} TVCs are required.



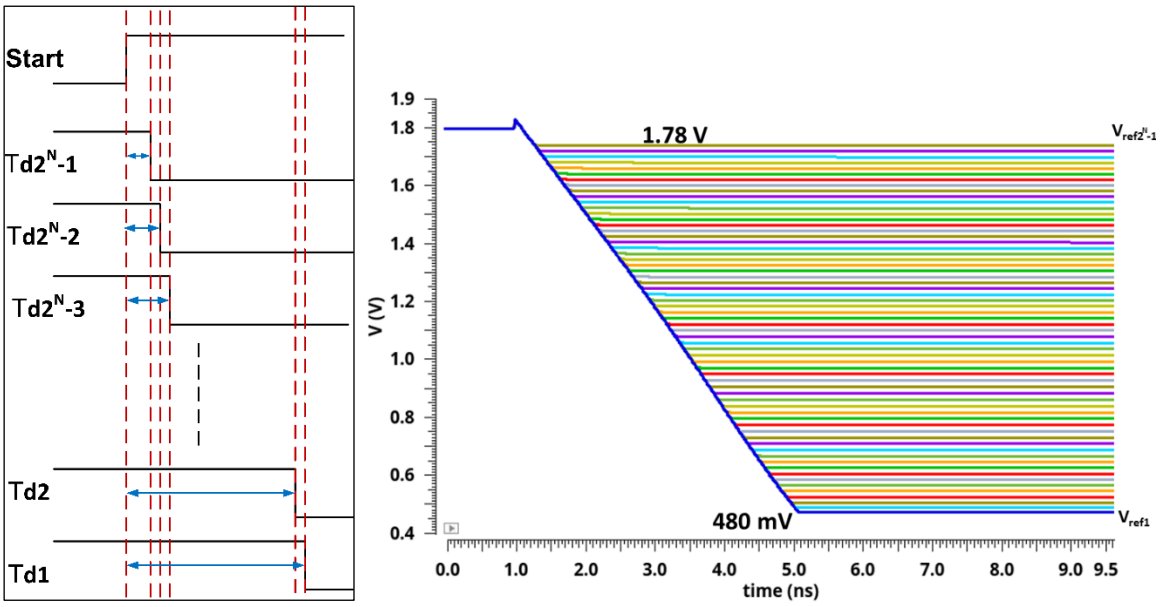
(a)



(b)



(c)



(d)

Figure 5.2 (a) Delay-based network with time-to-voltage converters (b) Transient analysis of delay-based network (c) Monte Carlo simulations of consecutive buffers (d) Generated reference voltages from all-digital reference ladder

The time difference between these two signals is converted to reference voltage through TVC. Initially, when the start signal is LOW, then PMOS transistor PM1 is ON, and NMOS transistor NM3 is OFF. In this condition, all the nodes present at the output of TVC (V_{ref2^N-1} to V_{ref1}) is charged to VDD through MOS transistor PM1. When the start signal goes from LOW to HIGH, PM1 switches to OFF and NM3 switches to ON condition. After some delay,

the time delay signals (T_{d2^N-1} to T_{d1}) goes from HIGH to LOW depending upon the delay of buffers present between each node. When both the start signal and delayed signal are HIGH, the output node of the TVC has been discharged through a pull-down circuit consisting of NMOS transistors NM1, NM2 and NM3.

The reference voltage has been obtained when both the start signal and delay signal are HIGH. With the increase in the delay, reference voltage reduces from its maximum value. The reference voltage range is shown in Figure 5.2 (d) where $V_{ref2^N-1} = 1.78$ V and $V_{ref1} = 0.48$ V. The value of V_{ref2^N-1} and V_{ref1} depends on the linearity range of TVC. The LSB value is 20 mV in the proposed flash ADC, therefore, working input range of ADC is 0.46 V to 1.8 V approximately.

5.4 Proposed Analog Voltage Comparators for All-Digital Flash ADC

The next component of the flash ADC is the comparator that converts the analog signal to digital form. With the improvement in the previously discussed pseudo digital comparator explained in chapter 3, fully-digital, synthesisable and scalable analog voltage comparators are proposed in this section.

5.4.1 Fully-Digital Differential Analog Voltage Comparator (FD-DVC4)

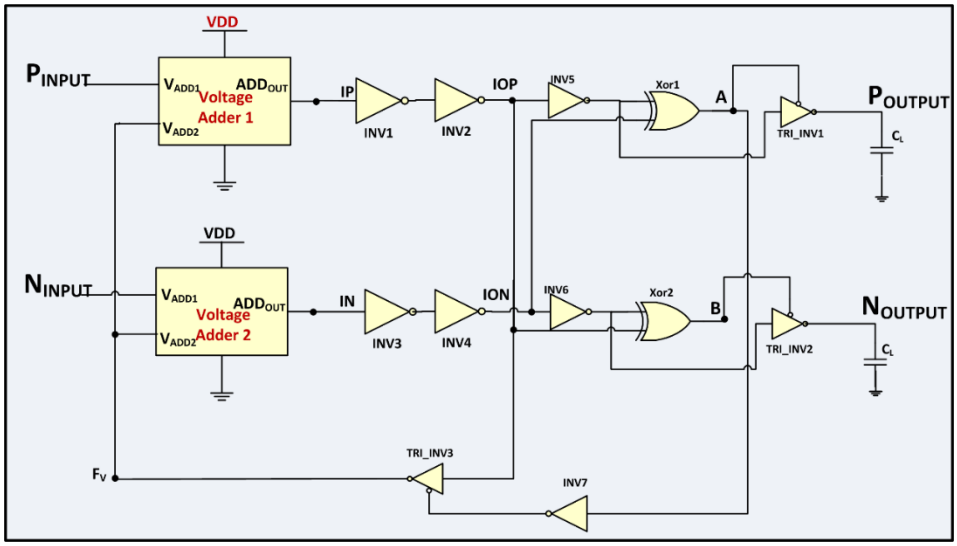
Figure 5.3 (a) shows the circuit diagram of proposed scalable fully-digital analog voltage comparator (FD-DVC4). In the proposed comparator, the summer network comprises of digital gates only; earlier this was designed using resistances or TGs, discussed in earlier sections 3.2, 3.3, and 3.4. The proposed FD-DVC4 uses standard cells such as inverters, XOR gate, tri-state inverters, and custom-made voltage adders. The proposed comparator receives P_{INPUT} and N_{INPUT} as differential input and provides P_{OUTPUT} and N_{OUTPUT} as differential output.

Figure 5.3 (b) shows the proposed digital gate-based voltage adder for FD-DVC4. The equivalent network of the voltage divider consists of standard NAND-NOR gates. The voltage adder network averages the two signals, V_{ADD1} and V_{ADD2}, and gives ADD_{OUT}, *i.e.*,

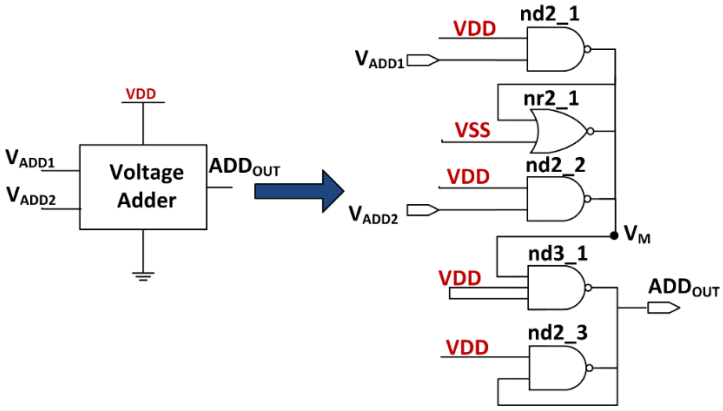
$$ADD_{OUT} \approx \frac{V_{ADD1}+V_{ADD2}}{2} \tag{5.1}$$

Assuming that V_{ADD1} is HIGH and V_{ADD2} is LOW to show the operation of voltage adder. Referring to Figure 5.3 (b), the PMOSs of nd2_1-3 and nd3_1 connected to VDD, and

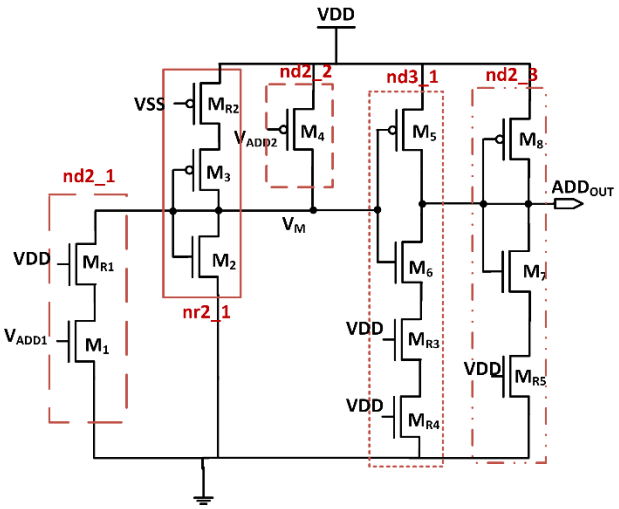
NMOSs of nr2_1 and nd2_2 connected to VSS are operating in the cutoff region. The circuit diagram of the voltage adder is shown in Figure 5.3 (c) after removing the MOSFETs present in the cut-off region. After that $M_{R1\text{-}5}$ transistor has been replaced with their equivalent resistance R_1-R_5 present in the linear region. The equivalent circuit diagram of voltage adder is shown in Figure 5.3 (d). As gate and drain terminal of MOSFETs M_2 and M_3 are connected together so these are in saturation region. A mathematical analysis of the voltage adder is shown below.



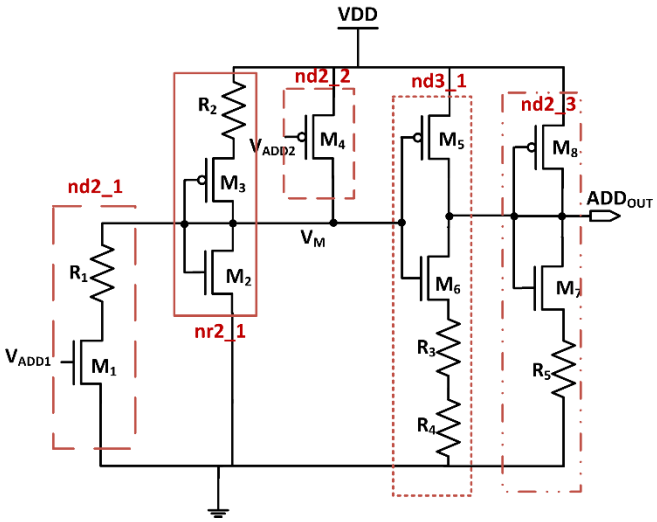
(a)



(b)



(c)



(d)

Figure 5.3 (a) Circuit diagram of fully-digital analog voltage comparator (FD-DVC4) (b) Digital-based voltage adder network (c) Model of voltage adder network (d) Equivalent model of voltage adder network

Since, the variation around V_M is smaller in amplitude and is closed to VDD/2, a small-signal analysis is applicable to analyze the node voltages, therefore applying KCL on node V_M gives

$$V_M\left(\frac{1}{R_2 + R_{M_{3(V_M)}}} + \frac{1}{R_{M_{2(V_M)}}}\right) = -\left(g_{m\,(M_1)}V_{ADD1} + g_{m\,(M_4)}V_{ADD2}\right) \qquad (5.2)$$

$$V_M = -\left(g_{m\,(M_1)}V_{ADD1} + g_{m\,(M_4)}V_{ADD2}\right)\left(R_{eq1(V_M)}\right) \tag{5.3}$$

where $R_{eq1(V_M)} = \left(\frac{\left(R_2+R_{M_{3(V_M)}}\right)R_{M_{2(V_M)}}}{R_2+R_{M_{3(V_M)}}+R_{M_{2(V_M)}}}\right)$. Similarly, MOSFETs M_7 and M_8 are in saturation. Also, applying KCL at ADD_{OUT} node.

$$ADD_{OUT}\left(\frac{1}{R_5 + R_{M_{7(ADD_{OUT})}}} + \frac{1}{R_{M_{8(ADD_{OUT})}}}\right) = -\left(g_{m\,(M_6)}V_M + g_{m\,(M_5)}V_M\right) \tag{5.4}$$

$$ADD_{OUT} = -\left(g_{m\,(M_6)}V_M + g_{m\,(M_5)}V_M\right)\left(R_{eq2(ADD_{OUT})}\right) \tag{5.5}$$

where $R_{eq2(ADD_{OUT})} = \left(\frac{\left(R_5+R_{M_{7(ADD_{OUT})}}\right)R_{M_{8(ADD_{OUT})}}}{R_5+R_{M_{7(ADD_{OUT})}}+R_{M_{8(ADD_{OUT})}}}\right)$.

Now, Substituting V_M from equation (5.3) into equation (5.5), we get

$$ADD_{OUT} = \left(g_{m\,(M_1)}V_{ADD1} + g_{m\,(M_4)}V_{ADD2}\right)\left(R_{eq1(V_M)}\right)\left(g_{m\,(M_6)} + g_{m\,(M_5)}\right)\left(R_{eq2(ADD_{OUT})}\right) \tag{5.6}$$

Assuming $g_{m\,(M_1)} = g_{m\,(M_4)} = g_{m\,(M_5)} = g_{m\,(M_6)} = g_{mY}$ where Y is function of V_{ADD1} and V_{ADD2} $(f(V_{ADD1}, V_{ADD2}))$ and $R_{eq1(V_M)} = R_{eq\,(f(V_M))}$ & $R_{eq2(ADD_{OUT})} = R_{eq\,(f(ADD_{OUT}))}$, substitute these values into equation (5.6), we obtain

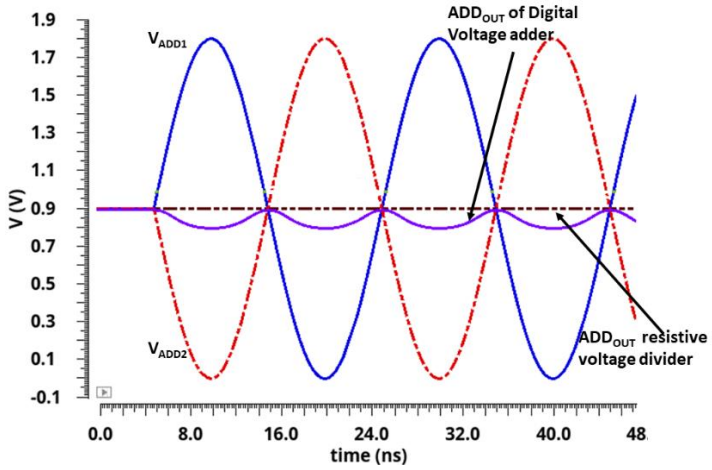
$$ADD_{OUT} \approx \frac{(V_{ADD1} + V_{ADD2})}{Q} \tag{5.7}$$

where $Q = \frac{1}{2g_{m\,(f(V_{ADD1},V_{ADD2}))}^{\,2}\, R_{eq\,(f(V_M))}\, R_{eq\,(f(ADD_{OUT}))}}$ which is $f(V_{ADD1}, V_{ADD2}, V_M, ADD_{OUT})$.

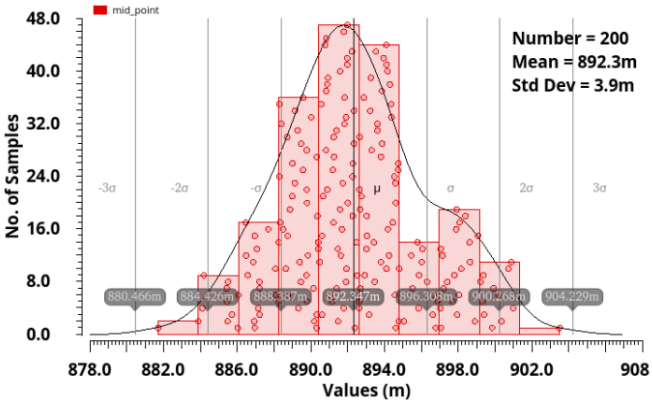
By properly selecting the values of $g_{m\,(f(V_{ADD1},V_{ADD2}))}^{\,2}$, $R_{eq\,(f(V_M))}$ and $R_{eq\,(f(ADD_{OUT}))}$. The proposed voltage adder averages the two input signals.

Figure 5.4 (a) shows the transient analysis of the proposed digital-based voltage adder and compared with a resistive voltage divider. The digital-based voltage adder network averages both the inputs (V_{ADD1} and V_{ADD2}) of the voltage adder and provides the output ADD_{OUT}. Here, ADD_{OUT} reaches its minimum value when the maximum value of V_{ADD1} and the minimum value of V_{ADD2} is applied at the input of the voltage adder. However, in the real

scenario when the proposed comparator works, V_{ADD1} changes to its max value but V_{ADD2} is maintained approximately to the common-mode voltage of 0.9 V by the feedback network. Therefore, ADD_{OUT} is the average of the voltage F_V obtained through feedback network and the input voltages. A Monte Carlo simulation is performed to observe the variation in the node voltage (ADD_{OUT}) due to process variations, as shown in Figure 5.4 (b). The mean and the standard deviation of the node voltage ADD_{OUT} are 892.3 mV and 3.9 mV, respectively. The operation of the digital part of the comparator was explained in section 3.4. For a differential case, $P_{INPUT} > N_{INPUT,}$ then P_{OUTPUT} is '1', and N_{OUTPUT} is '0'. In the same way, when $P_{INPUT} < N_{INPUT,}$ then P_{OUTPUT} is '0', and N_{OUTPUT} is '1'.



(a)

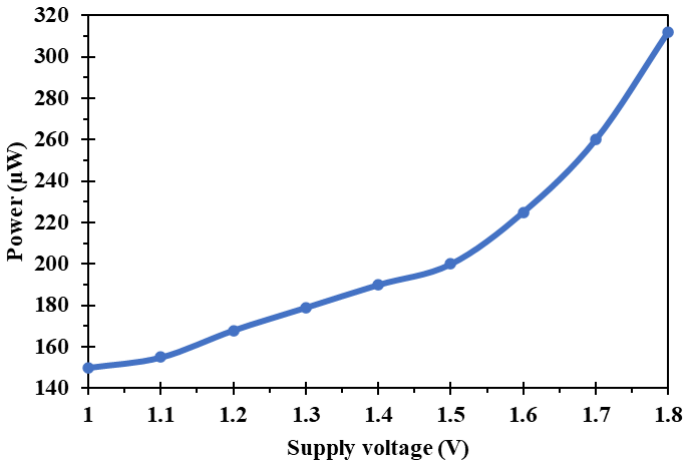


(b)

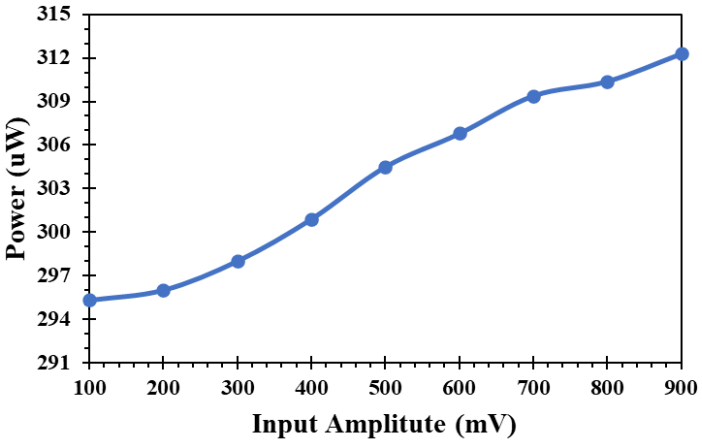
Figure 5.4 (a) Simulation result of digital voltage adder compared with resistive voltage divider (b) Monte Carlo simulation for the node voltage ADD_{OUT}

5.4.1.1 Power of FD-DVC4

The fully-digital analog voltage comparator has been implemented and simulated using 180 nm SCL CMOS technology at 1.8 V supply. The total power is calculated from the transient analysis. The dynamic power dissipation is mainly dissipated by voltage adder block, INV1 and INV3 due to the continuous flow of short circuit current flowing in these. Static power dissipation is significantly less as compared to dynamic power dissipation. The comparator is working at the supply range from 1 V to 1.8 V. Minimum supply voltage is limited by a standard cell-based voltage adder and inverters in the circuit. Figure 5.5 (a) shows the variation in power dissipation with the change in supply voltage from 1 V to 1.8 V. The total power dissipation of the circuit is 150 µW at 1 V supply voltage and 312 µW at 1.8 V supply voltage. Figure 5.5 (b) shows the variation of the power with the change in the input amplitude at the supply voltage of 1.8 V. In the proposed comparator, the total average power is 312 µW which includes both dynamic and static power components as shown in Figure 5.5 (c) It is observed that the average dynamic power dissipation by Voltage Adder 1-2 and INV1-4 is 213.8 µW with negligible static power dissipation whereas average dynamic power dissipated by INV5-7, XOR1-2 and TRI_INV1-3 is 96.1 µW with average static power of 1.2 µW approximately.



(a)



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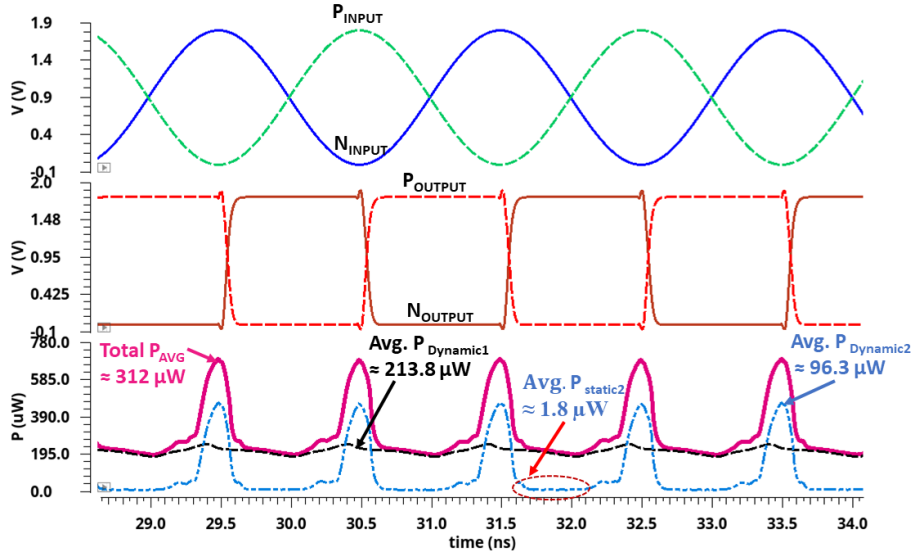


(c)

Figure 5.5 (a) Variation of power with respect to the supply voltage (b) Variation of power with the change in input signal amplitude at the supply of 1.8 V (c) Total average power including dynamic and static power components

5.4.1.2 Delay of FD-DVC4

The transient analysis for the sinusoidal input at a supply of 1.8 V is shown in Figure 5.6 (a). As observed from figure, the total delay from P_{INPUT} to the output P_{OUTPUT} is 0.72 ns approximately at a supply voltage of 1.8 V. Figure 5.6 (b) shows the transient analysis of the proposed comparator for the supply range of 1 V to 1.8 V. With the decrease in the supply voltage, delay of the comparator increases. As observed in Figure 5.6 (c), the maximum delay of the comparator at a supply voltage of 1 V is 1.95 ns which changes approximately by 1 ns if we vary the supply from 1 V to 1.8 V.

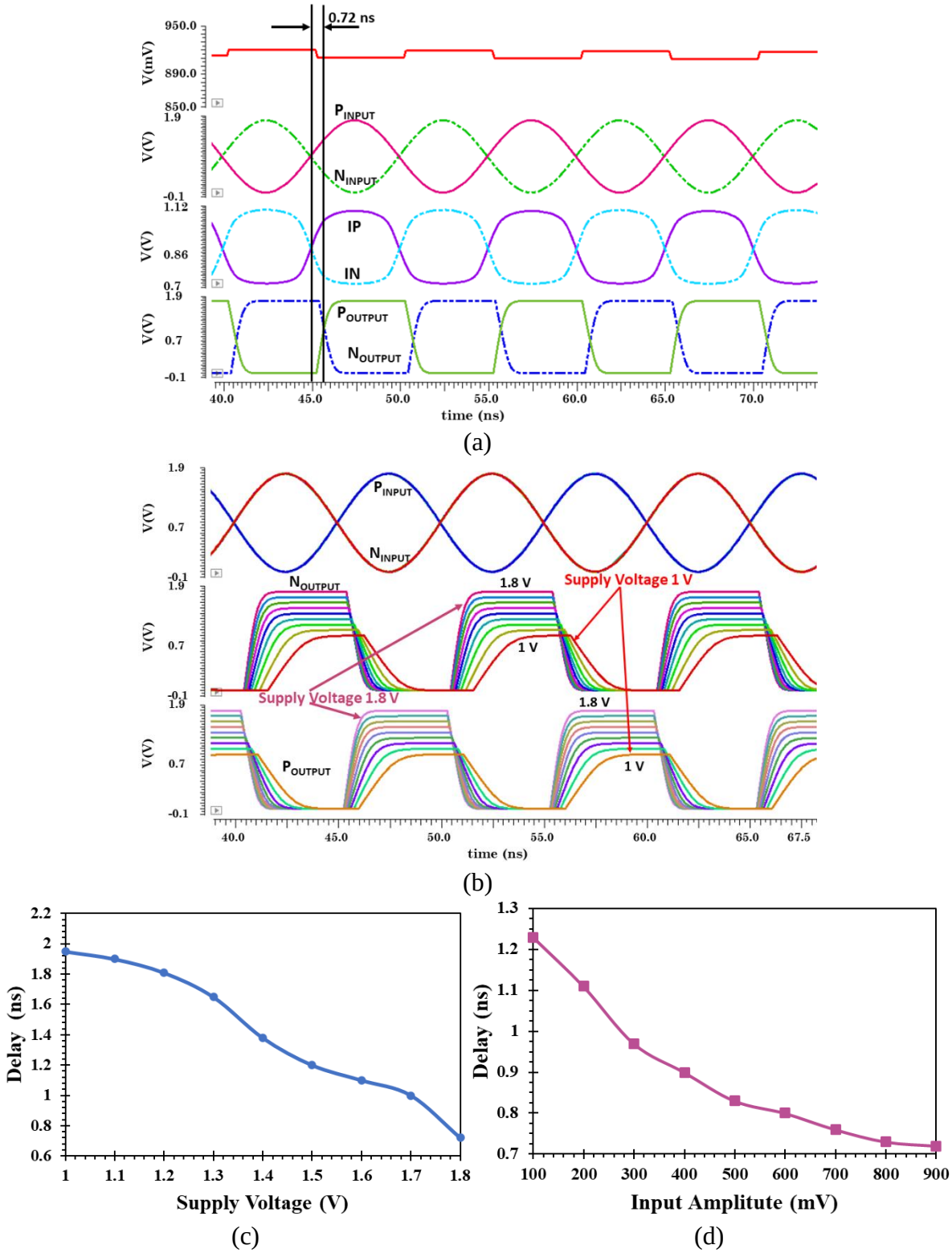
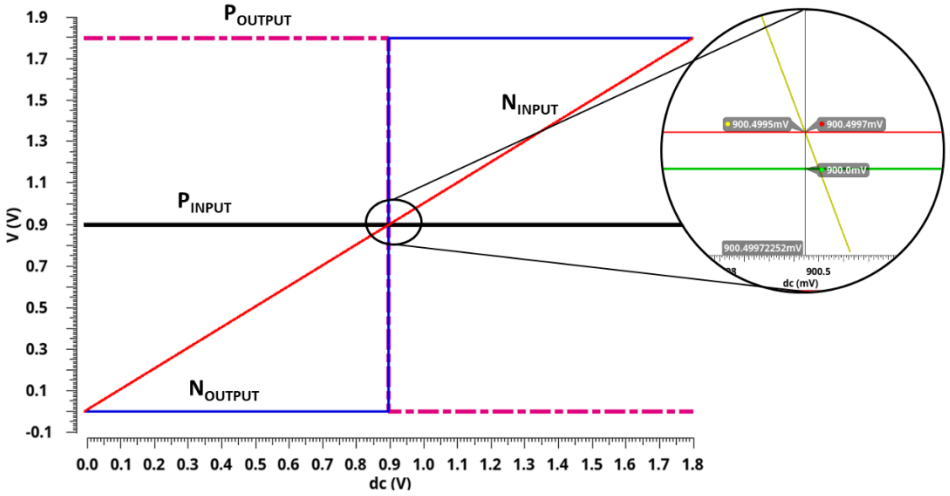


Figure 5.6 (a) Delay analysis of FD-DVC4 (b) Transient analysis of FD-DVC4 at different supply voltages (c) Variation of delay with respect to the supply voltage (d) Variation of delay with respect to input amplitude

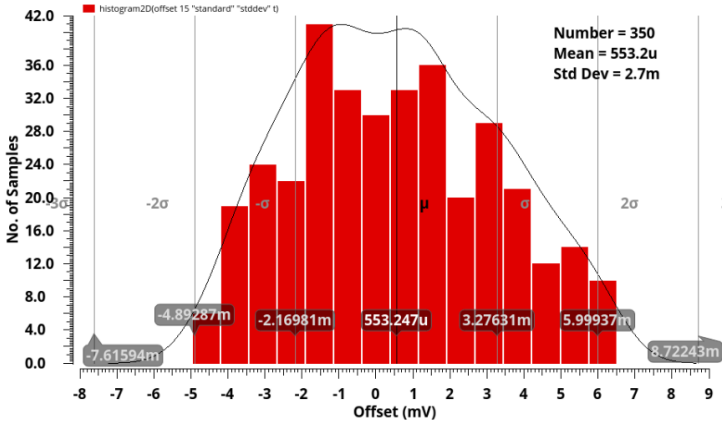
Figure 5.6 (d) shows the variation in delay with respect to input signal amplitude. As the input amplitude increases, the delay of the circuit reduces. This is due to the fact that with the larger signal amplitude, it takes less iteration for the feedback loop to make IOP/ION nodes to valid logic levels.

5.4.1.3 Offset voltage of FD-DVC4

Figure 5.7 (a) shows the DC analysis of the proposed comparator to estimate the value of the offset voltage. The observed value of the offset from the DC analysis is 0.5 mV approximately. The Monte Carlo simulations of the proposed comparator for the offset voltage is shown in Figure 5.7 (b). The observed mean value of the offset voltage is 0.55 mV, and the standard deviation is 2.7 mV which is sufficient for applications of up to 7-bit resolution at a supply voltage of 1.8 V.



(a)



(b)

Figure 5.7 (a) DC analysis to calculate the offset voltage FD-DVC4 (b) Monte Carlo simulations of offset voltage variation for 350 runs

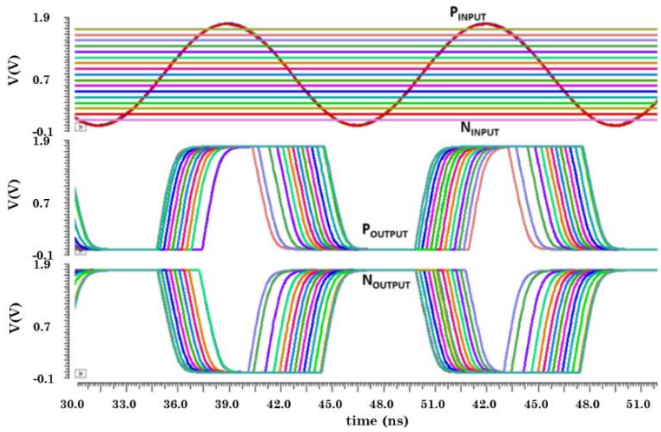


Figure 5.8 Differential output of FD-DVC4 at the different reference voltage

Figure 5.8 shows simulation results for different reference voltages varying from 0.1 V to 1.7 V at a supply voltage of 1.8 V. To determine the comparator performance delay and power have been measured at different PVT corners and given in Table 5.1. The physical layout of the proposed analog voltage comparator is shown in Figure 5.9. It consumes an area of 879.75 μm^2. The voltage adder consists of custom-made NAND and NOR gates, designed in SCL 180 nm CMOS technology and the rest of the circuit is designed through standard cell design methodology.

Table 5.1 Delay and power analysis of FD-DVC4 at different PVT corners for the input amplitude of 900 mV

Process (P)	**FF**	**FS**	**TT**	**SF**	**SS**
Voltage (V)	1.98	1.8	1.8	1.8	1.62
Temperature (℃)	-20	27	27	27	85
Power (µW)	418.2	331.5	312	300.3	242.1
Delay (ns)	0.41	0.55	0.72	0.86	1.2

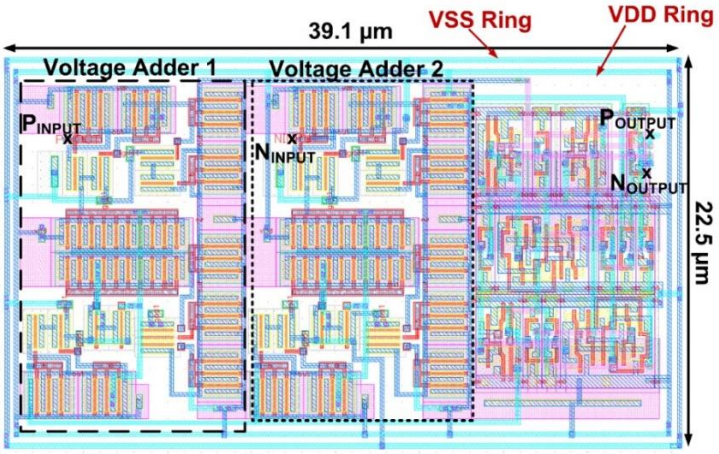
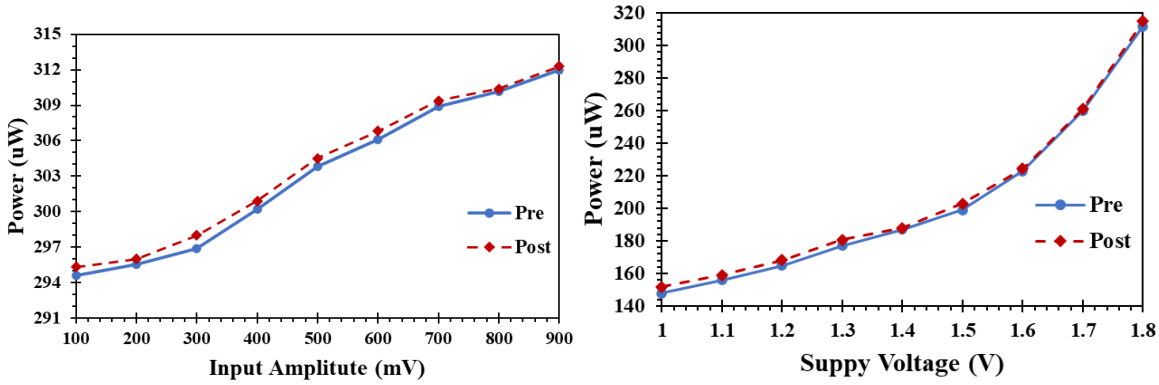


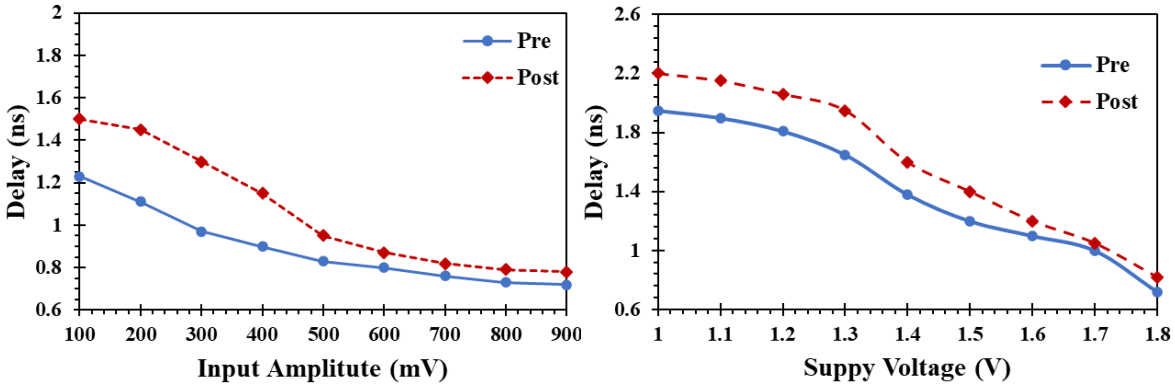
Figure 5.9 Layout of fully-digital analog voltage comparator (FD-DVC4)

The post-layout simulations have been performed to validate the performance of the proposed analog voltage comparator. Figure 5.10 (a) and (b) show both pre-layout and post-layout simulation of power versus input amplitude ranging from 100 mV to 900 mV and power versus supply voltage varying from 1 V to 1.8 V, respectively. Figure 5.11 (a) and (b) show the pre-layout and post-layout simulations of delay versus input amplitude ranging from 100 mV to 900 mV and delay versus supply voltage varying from 1 V to 1.8 V, respectively.



(a) (b)

Figure 5.10 (a) Pre-layout versus post-layout simulation results of power versus input amplitude (mV) (b) Pre-layout versus post-layout simulation results of power versus supply voltage (V)



(a) (b)

Figure 5.11 (a) Pre-layout versus post-layout simulation results of the delay versus input amplitude (mV) (b) Pre-layout versus post-layout simulation results of the delay versus supply voltage (V)

The performance of the proposed analog voltage comparator (FD-DVC4) is compared with the existing voltage comparators available in the literature and is shown in Table 5.2. This design is implemented with a digital gate-based design approach. Compared to various

analog-based comparators [37, 101, 111, 113, 147-148] and digital-based comparators [16, 113], this circuit is scalable to lower technologies and takes less time and design efforts. In comparison to existing comparators [16, 37, 101, 108, 111, 113, 147-148], the value of offset voltage is significantly less in the proposed circuit. For the same supply voltage as given in Ref. [147], the value of offset and delay is less, and also, the area consumed by the proposed comparator is less due to the elimination of capacitor (MOSCAP) and resistors (voltage divider network). The delay and power can be further reduced at lower technology nodes. This design provides a good trade-off between delay and power. The power dissipation of the proposed fully-digital differential comparator is 47 % lesser than the differential voltage comparator reported by G. Raut *et al.* [105] at the supply voltage of 1.8 V. Therefore, the proposed comparator can be used to design low power flash ADCs.

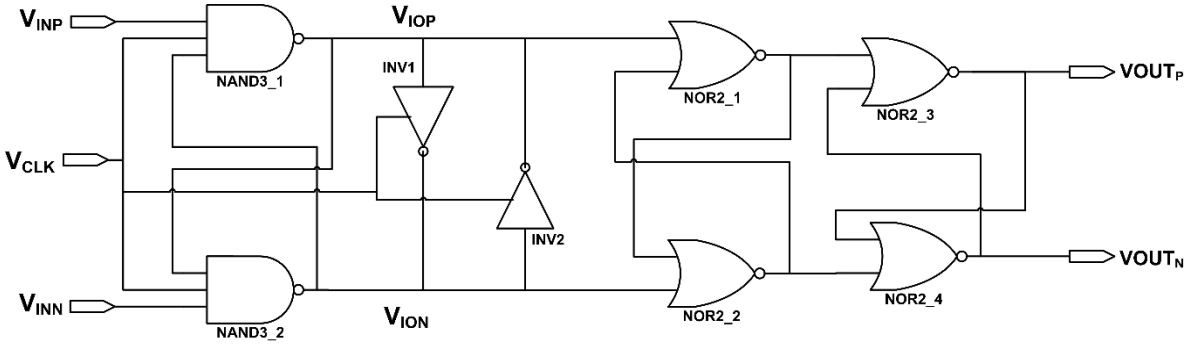
Table 5.2 Comparison of FD-DVC4 with existing analog-based and digital-based voltage comparators

Parameters References	**Year**	**CMOS Technology (nm)**	**Avg. power Dissipation (µW)**	**Supply Voltage (V)**	**Offset Voltage (mV)**	**Delay (ns)**	**Design Methodology**
[37]	2014	90	-	1.2	45	-	Digital
[101]	2014	180	329	1.2	7.8	0.6	Analog
[111]	2015	130	600	1	7.78	-	Analog
[147]	2016	180	177.5	1.8	5	5	Partially Digital
[148]	2017	65	-	1.2	7.25	0.8	Analog
[16]	2018	40	1.5	0.6	40	3*	Digital
[113]	2019	180	225	1.2	7.3	0.3	Analog
[108]	2020	180	554	1.8	-	0.3	Analog
This work (FD-DVC4)	-	180	150 @ 1V 312 @ 1.8 V	1- 1.8	0.55	1.92* 0.72*	Digital

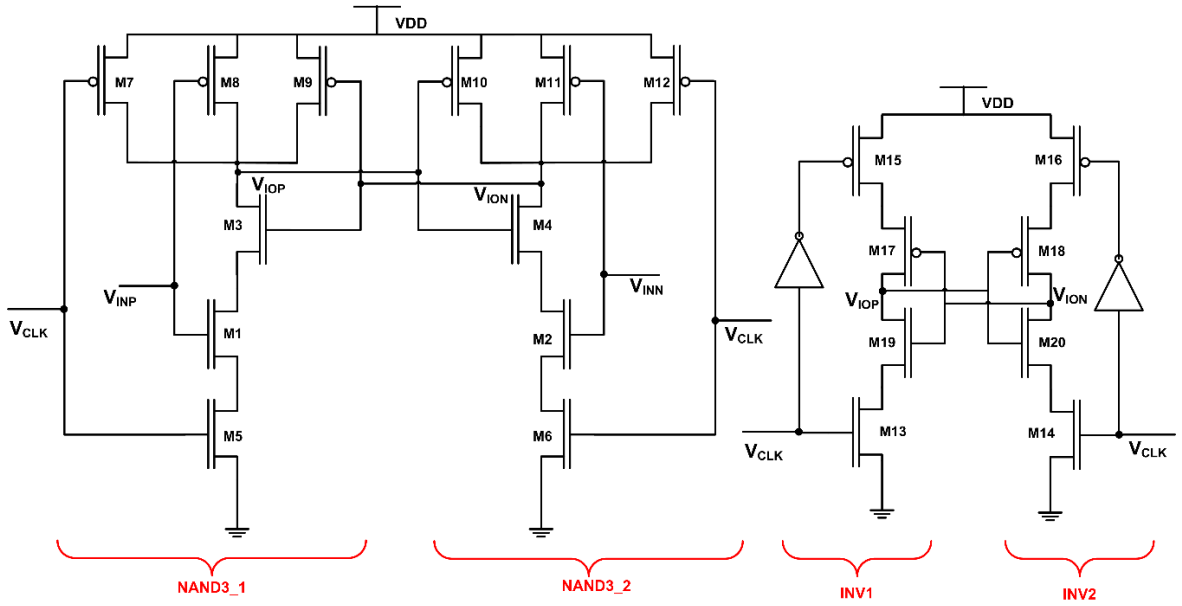
*Delay of the circuit including latch delay

5.4.2 Synthesizable Differential Analog Voltage Comparator (Syn-DVC5)

The comparator explained in the previous section 5.4.1 is a fully-digital differential analog voltage comparator but not fully synthesizable. Further to improve the power, offset, and delay, a fully synthesizable dynamic differential analog voltage comparator (Syn-DVC5) is proposed in this section and is shown in Figure 5.12. The proposed Syn-DVC5 consists of two 3-input NAND gates which are used at the input side in the cross-coupled fashion, clocked-inverter based positive feedback latch and NOR gate-based SR-latch. Figure 5.12 (b) shows the MOS transistor level implementation of the comparator. The MOS transistors M1, M8 and M2, M11 are connected to the analog inputs.



(a)



(b)

Figure 5.12 (a) Circuit diagram of the proposed analog voltage comparator (Syn-DVC5) **(b)** Equivalent transistor-level circuit of the input stage

M3-M4 and M9-M10 are connected in the feedback loop. M5, M6, and M7, M12 are connected to the input clock signal (V_{CLK}). When the clock signal is low, V_{IOP} and V_{ION} are charged to VDD through MOS transistors M7 and M12 during the pre-charge phase. When the clock signal changes from low to high during the evaluation phase, M7 and M12 are switched off, while M5 and M6 are in the saturation region. Also, MOS transistors M3 and M4 are ON as their output node is charged to VDD. The positive analog input (V_{INP}) is applied to the input gate terminal of M1 and M8 while the negative analog input (V_{INN}) is applied to the input gate terminal of the M2 and M11. When the input voltage V_{INP} is greater than V_{INN}, V_{IOP} discharges faster than V_{ION}. As V_{IOP} reaches the threshold voltage of NMOS transistor (M4) and MOS transistor M4 reaches the cut-off region earlier than M3. The positive feedback circuit pushes the output V_{IOP} to logic HIGH and V_{ION} to logic LOW. This cross-coupled fashion latch (consists of MOS transistors M3, M9, M4 and M10) is not enough for proper operation because the discharging rate of the pull-down network is also affected by charging rates of M8 and M11. Hence, a clocked inverter based positive feedback circuit is used to increase the speed of the regeneration operation.

Similarly, when V_{INN} is higher than V_{INP}, the output V_{IOP} switches to logic HIGH, and V_{ION} turns to logic LOW. The SR Latch, in a later stage, is used to stabilize the output voltages. The proposed comparator, Syn-DVC5 is designed in 1.8 V 180 nm SCL CMOS technology. The transient analysis is shown in Figure 5.13 where V_{INP} and V_{INN} signal are compared at the positive edge of the clock and produces $VOUT_P$ and $VOUT_N$ according to the input comparison.

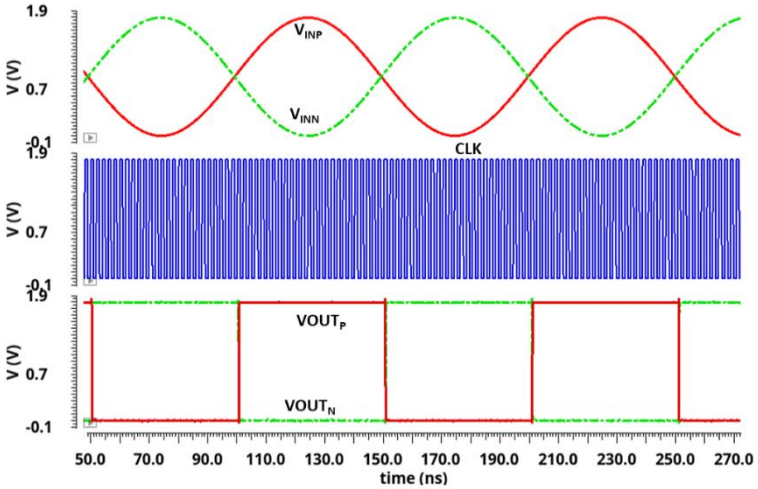


Figure 5.13 Transient analysis of Syn-DVC5

5.4.2.1 Delay of the Syn-DVC5

Figure 5.14 shows the delay of Syn-DVC5 where the total delay of this voltage comparator is the sum of t_0 and t_{latch} time delays. The t_0 time delay is due to charging and discharging of the load capacitor (C_{Lout}) at nodes V_{IOP} and V_{ION} before the regeneration phase. The t_{latch} is the regeneration time taken by the cross-coupled inverter pair (INV1 and INV2) to bring the node voltages at V_{IOP} and V_{ION} to VDD and ground or vice-versa.

$$t_{delay} = t_0 + t_{latch} \tag{5.8}$$

Thus t_0 is obtained as

$$t_0 = \frac{V_{thn} C_{Lout}}{I_{19,20}} \tag{5.9}$$

where $I_{19,20}$ represents the current flowing through NMOS transistor M19 and M20.

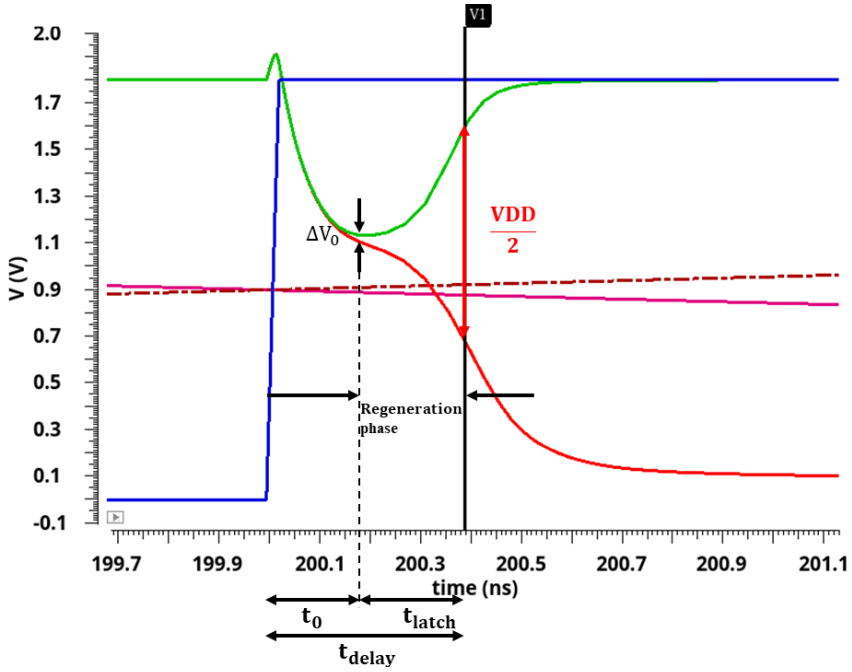


Figure 5.14 Delay analysis of the Syn-DVC5

After 1st NMOS (M19) of the cross-coupled latch gets ON, the corresponding output V_{IOP} discharges through M19 and M13 towards 0 V. Therefore, it will turn ON PMOS transistor M18, which leads to charging of the node V_{ION} to VDD.

Hence, the regeneration time delay [82] (t_{latch}) of the cross-coupled latch is given by

$$t_{latch} = \frac{C_{Lout}}{g_{m,eff}} \ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) \cong \frac{C_{Lout}}{g_{m,eff}} \ln\left(\frac{VDD/2}{\Delta V_0}\right) \tag{5.10}$$

where $g_{m,eff}$ is the effective transconductance of the cross-coupled pair positive feedback inverters INV1-INV2. The initial voltage difference ΔV_0 [82] is expressed as

$$\Delta V_o = V_{thn} \frac{\Delta I_{latch}}{I_{B1}} = V_{thn} \frac{\Delta I_{latch}}{I_{tail\ 13,14}}$$

$$= V_{thn} \frac{g_{m\ 19,20}}{I_{tail\ 13,14}} \Delta V_{IOP/ION} \tag{5.11}$$

where V_{thn} is the threshold voltage of NMOS transistors and assumed to equal for all MOS NMOS transistors, $g_{m\ 19,20}$ is the transconductance of MOS transistor M19 and M20. It is observed from the circuit diagram that a combination of controlling transistor M9 and M10 along with two switches M3 and M4 matches the operation of two cross-coupled inverter pair. Using small-signal model, $\Delta V_{IOP/ION}$ is calculated as [101, 149].

$$\Delta V_{IOP/ION} = \Delta V_{IOP(N)} \exp^{((A_v-1)t/\tau)} \tag{5.12}$$

$$\frac{\tau}{A_v - 1} \cong \frac{C_{L,ION(P)}}{G_{m,eff1}} \tag{5.13}$$

In the equation (5.13), A_v is the low frequency gain of each inverter, τ is the RC time constant at each inverter's output, $\Delta V_{IOP(N)}$ is the initial V_{IOP}/V_{ION} node difference voltage when one of the controlling transistors gets into working condition (M9 or M10). Therefore, it is represented by

$$\Delta V_{IOP(N)} = |V_{thp}| \frac{g_{m\ 1,2} \Delta V_{in}}{I_{tail\ 5,6}} \tag{5.14}$$

Substituting the equation (5.12), (5.13), (5.14) into (5.11), ΔV_o is

$$\Delta V_o = V_{thn} \frac{g_{m\ 19,20}}{I_{tail\ 13,14}} \Delta V_{IOP(N)} \exp^{((A_v-1)t/\tau)} \tag{5.15}$$

$$\Delta V_o = V_{thn} \frac{g_{m\ 19,20}}{I_{tail\ 13,14}} |V_{thp}| \frac{g_{m\ 1,2} \Delta V_{in}}{I_{tail\ 5,6}} \exp^{((A_v-1)t/\tau)} \tag{5.16}$$

$$\Delta V_o = V_{thn}\frac{g_{m\,19,20}}{I_{tail\,13,14}}\left|V_{thp}\right|\frac{g_{m\,1,2}\Delta V_{in}}{I_{tail\,5,6}}\exp^{\left(\frac{G_{m,eff1}\cdot t_0}{C_{L,ION(P)}}\right)} \tag{5.17}$$

By substituting ΔV_o from equation (5.17) into equation (5.10), we get

$$t_{latch} \cong \frac{C_{Lout}}{g_{m,eff}}\ln\left(\frac{VDD/2}{V_{thn}\frac{g_{m\,19,20}}{I_{tail\,13,14}}\left|V_{thp}\right|\frac{g_{m\,1,2}\Delta V_{in}}{I_{tail\,5,6}}\exp^{\left(\frac{G_{m,eff1}\cdot t_0}{C_{L,ION(P)}}\right)}}\right) \tag{5.18}$$

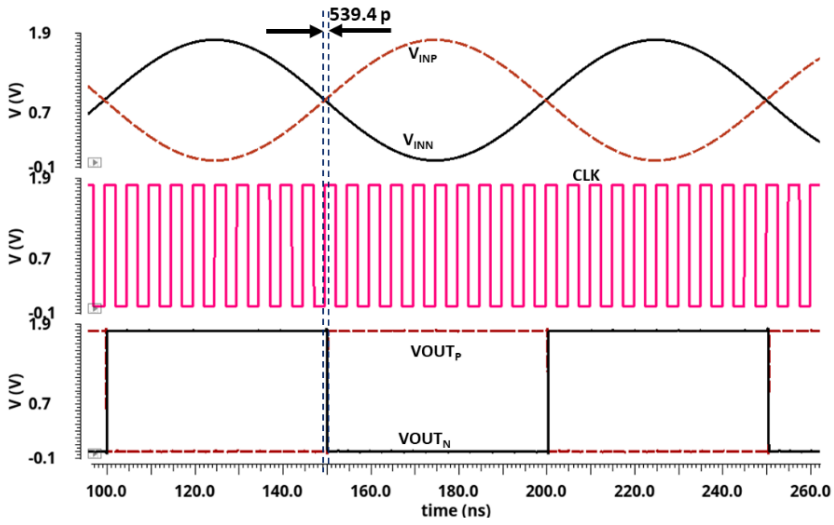
From equation (5.8), (5.9) and (5.18), the obtained t_{delay} is

$$t_{delay} = \frac{V_{thn}C_{Lout}}{I_{19,20}} + \frac{C_{Lout}}{g_{m,eff}}\ln\left(\frac{VDD/2}{V_{thn}\frac{g_{m\,19,20}}{I_{tail\,13,14}}\left|V_{thp}\right|\frac{g_{m\,1,2}\Delta V_{in}}{I_{tail\,5,6}}\exp^{\left(\frac{G_{m,eff1}\cdot t_0}{C_{L,ION(P)}}\right)}}\right) \tag{5.19}$$

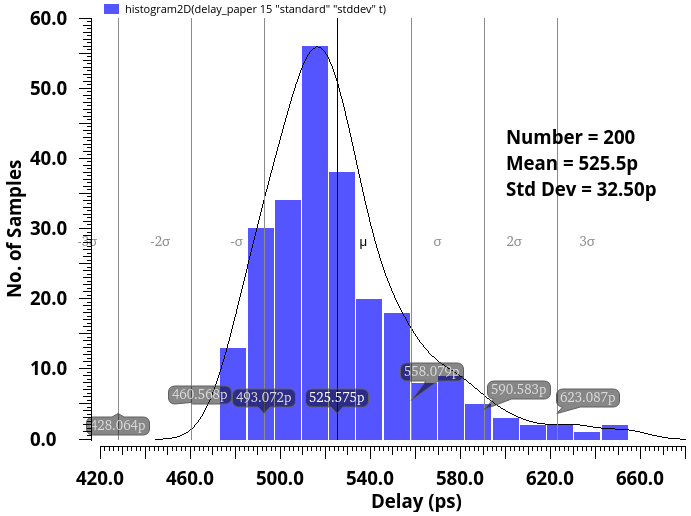
The worst-case propagation delay is calculated from V_{INP}/V_{INN} to $VOUT_P/VOUT_N$ and its value is 539.4 ps as shown in Figure 5.15 (a). The total delay of the comparator ($t_{tot-delay}$) is the sum of t_{delay} and delay of the SR latch (t_{SR}) and given by

$$t_{tot-delay} = t_{SR} + t_{delay} = t_{SR} + \frac{V_{thn}C_{Lout}}{I_{19,20}} + \frac{C_{Lout}}{g_{m,eff}}\ln\left(\frac{VDD/2}{V_{thn}\frac{g_{m\,19,20}}{I_{tail\,13,14}}\left|V_{thp}\right|\frac{g_{m\,1,2}\Delta V_{in}}{I_{tail\,5,6}}\exp^{\left(\frac{G_{m,eff1}\cdot t_0}{C_{L,ION(P)}}\right)}}\right) \tag{5.20}$$

Figure 5.15 (b) shows the Monte Carlo simulations to observe the mismatches and process variations on the propagation delay. The mean value of propagation delay is 525.5 ps with the standard deviation of 32.5 ps. Finally, the delay values of the proposed Syn-DVC5 at different PVT corners is shown in Table 5.3.



(a)



(b)

Figure 5.15 (a) Propagation delay of Syn-DVC5 (b) Monte Carlo simulation for propagation delay of Syn-DVC5

Table 5.3 Delay analysis of Syn-DVC5 at different PVT corners

Process (P)	**FF**	**FS**	**TT**	**SF**	**SS**
Voltage (V)	1.98	1.8	1.8	1.8	1.62
Temperature (°C)	-20	27	27	27	85
Delay (ps)	416.9	499.8	522.2	611.7	675.5

5.4.2.2 Static Offset Voltage from β and V_{th} Mismatches of Syn-DVC5

The offset analysis of op-amp based comparator is defined in the literatures whereas offset of dynamic and digital comparators have not been calculated using traditional method. The transconductance of digital and dynamic comparators with positive feedback depends on the input level and time, and hence, not defined. Therefore, the dynamic comparator is observed as non-linear and time-varying system. In the proposed comparator, a balanced approach is used to analyze the offset of non-linear and time-varying system. If there is no mismatch in the circuit, a fully differential comparator will retain a balanced state. Balanced condition for static offset voltage means $V_{IOP} = V_{ION}$; currents I_1 and I_2 in both branches are the same at all times during the transient process. The balanced state can be defined by a space variable ϕ_s consists of power supply voltages, node voltages, biasing voltages, threshold voltages where ϕ_s = {VDD, $V_{CLK,}$ V_{IOP}, V_{ION}, V_{DS}}. Due to mismatches between these nodes, the circuit loses its balanced state and output becomes $V_{IOP} \neq V_{ION}$. To compensate the mismatch effect and make $V_{IOP} = V_{ION}$, a voltage ΔV_{IO} can be applied to the input which is the offset voltage of the comparator. When the input transistor of both the branches are perfectly matched, then the threshold voltage of the comparator is zero. To find the offset voltage from the mismatch in current factor β $\left(\frac{1}{2}\mu c_{ox}\frac{W}{L}\right)$ and the threshold voltage V_{th}, a perfectly matched balanced biasing condition has been applied. It is essential to know the operating regions of different MOS transistors to calculate the offset voltage due to mismatches. It is supposed that the influence of each MOS transistor is independent of the other MOS transistors [149]. According to Figure 5.16, initially, when V_{CLK} is LOW during pre-charge conditions, the output nodes IOP and ION are charged to VDD. Therefore, gate and drain voltages of M3-M4 and M9-M10 are equal, and they are operating in the saturation region. The MOS transistors M1-M2 and M8-M11 connected to the input voltages which are acting as the voltage-controlled resistor and working in the triode region because of low drain-source voltage (V_{DS}). During the evaluation phase when V_{CLK} goes to HIGH, the MOS transistors M5 and M6 are working in the saturation region. In this phase, M9 and M11 are initially OFF, but after the discharging of either V_{IOP} or V_{ION}, one of them (M9 or M11) turned ON and others turned OFF which fasten the decision cycle. The calculation of offset voltage is done during a balanced condition. So,

M9 and M11 do not affect the offset voltage. The unbalance process is defined when the positive feedback activates, and the mismatches impacts on these transistors are minimal with no interference in the decision phase. Also, M7 and M12 are OFF during the decision phase. So, it will not affect the offset voltage. After obtaining the operating regions, KCL is applied to calculate the offset voltage caused by each pair.

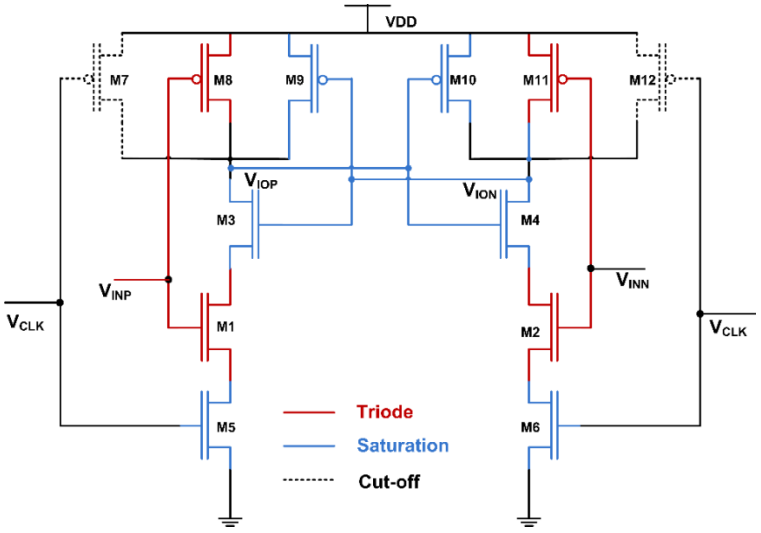


Figure 5.16 Circuit diagram to calculate the offset voltage of Syn-DVC5

In order to calculate the random offset from the mismatches in the differential pair M1 and M2 under balanced condition, currents flowing through both the transistors are equal, *i.e.*,

$$I_1 = I_2 \tag{5.21}$$

$$\beta_1^*\left(V_{GS1}^* - V_{thn1}^* - \frac{V_{DS1}}{2}\right)V_{DS1} = \beta_2^*\left(V_{GS2} - V_{thn2}^* - \frac{V_{DS2}}{2}\right)V_{DS2} \tag{5.22}$$

The superscript * represents the parameter subject to mismatches. The variations are described as

$$\beta_{1,2}^* = \beta + \Delta\beta_{1,2} \tag{5.23}$$

$$V_{thn1,2}^* = V_{thn} + \Delta V_{thn1,2} \tag{5.24}$$

$$V_{GS1}^* = V_{INP}^* - V_{D5} \tag{5.25}$$

$$V_{GS2} = V_{INN} - V_{D6} \tag{5.26}$$

where β and V_{thn} are the typical value of the current factor and threshold voltage, respectively. $\Delta V_{thn1,2}$ is the variation in the threshold voltage and $\Delta\beta_{1,2}$ is the current factor

variation of M1 or M2. V_{INN} and V_{INP} are the two input voltages. The offset voltage ΔV_{IN} is obtained by the mismatches in M1 or M2.

Substituting equation (5.23)−(5.26) into equation (5.22), the following equation is obtained

$$\beta_1^*\left(V_{INP}^* - V_{D5} - V_{thn1}^* - \frac{V_{DS1}}{2}\right)V_{DS1} = \beta_2^*\left(V_{INN} - V_{D6} - V_{thn2}^* - \frac{V_{DS2}}{2}\right)V_{DS2} \quad (5.27)$$

$$\beta + \Delta\beta_1\left(V_{INP} + \Delta V_{IN} - V_{D5} - V_{thn} - \Delta V_{thn1} - \frac{V_{DS1}}{2}\right)V_{DS1} = \beta + \Delta\beta_2\left(V_{INN} - V_{D6} - V_{thn} - \Delta V_{thn2} - \frac{V_{DS2}}{2}\right)V_{DS2} \quad (5.28)$$

$$1 + \frac{\Delta\beta_1}{\beta}\left(V_{INP} + \Delta V_{IN} - V_{D5} - V_{thn} - \Delta V_{thn1} - \frac{V_{DS1}}{2}\right)V_{DS1} = 1 + \frac{\Delta\beta_2}{\beta}\left(V_{INN} - V_{D6} - V_{thn} - \Delta V_{thn2} - \frac{V_{DS2}}{2}\right)V_{DS2} \quad (5.29)$$

As the variables are independent and uncorrelated, their cross null product and covariance is zero. By applying this property, the above equation is rewritten as

$$\left(1 + \frac{\Delta\beta_1}{\beta}\right)\left\{\left(V_{INP} - V_{D5} - V_{thn} - \frac{V_{DS1}}{2}\right)V_{DS1} - \Delta V_{thn1}V_{DS1} + \Delta V_{IN}V_{DS1}\right\} = \left(1 + \frac{\Delta\beta_2}{\beta}\right)\left\{\left(V_{INN} - V_{D6} - V_{thn} - \frac{V_{DS2}}{2}\right)V_{DS2} - \Delta V_{thn2}V_{DS2}\right\} \quad (5.30)$$

Also, under the balanced conditions

$$V_{DS1} = V_{DS2} \quad (5.31)$$

$$\left(1 + \frac{\Delta\beta_1}{\beta}\right)\left\{\left(V_{INP} - V_{D5} - V_{thn} - \frac{V_{DS1}}{2}\right) - \Delta V_{thn1} + \Delta V_{IN}\right\} = \left(1 + \frac{\Delta\beta_2}{\beta}\right)\left\{\left(V_{INN} - V_{D6} - V_{thn} - \frac{V_{DS2}}{2}\right) - \Delta V_{thn2}\right\} \quad (5.32)$$

$$\frac{\Delta\beta_1}{\beta}\left(V_{INP} - V_{D5} - V_{thn} - \frac{V_{DS1}}{2}\right) - \Delta V_{thn1} + \Delta V_{IN} = \frac{\Delta\beta_2}{\beta}\left(V_{INN} - V_{D6} - V_{thn} - \frac{V_{DS2}}{2}\right) - \Delta V_{thn2} \quad (5.33)$$

$$\Delta V_{IN} = \Delta V_{OS1,2}$$
$$= \frac{\Delta\beta_2}{\beta}\left(V_{INN} - V_{D6} - V_{thn} - \frac{V_{DS2}}{2}\right) - \Delta V_{thn2}$$
$$- \frac{\Delta\beta_1}{\beta}\left(V_{INP} - V_{D5} - V_{thn} - \frac{V_{DS1}}{2}\right) + \Delta V_{thn1} \quad (5.34)$$

$$\sigma^2_{V_{OS1,2}} = \sigma^2_{\beta_2}\left(V_{INN} - V_{D6} - V_{thn} - \frac{V_{DS2}}{2}\right)^2 + \sigma^2_{V_{thn2}}$$
$$+ \sigma^2_{\beta_1}\left(V_{INP} - V_{D5} - V_{thn} - \frac{V_{DS1}}{2}\right)^2 + \sigma^2_{V_{thn1}} \quad (5.35)$$

Similarly, by considering the random offset from the mismatches between M8 and M11 operating in the triode region, we obtain

$$\sigma^2_{V_{OS8,11}} = \sigma^2_{\beta_8}\left(VDD - V_{INP} - |V_{thp}| - \frac{V_{SD8}}{2}\right)^2 + \sigma^2_{V_{thp8}}$$
$$+ \sigma^2_{\beta_{11}}\left(VDD - V_{INN} - |V_{thp}| - \frac{V_{SD8}}{2}\right)^2 + \sigma^2_{V_{thp11}} \quad (5.36)$$

Also, to see the offset voltage due to mismatch between M5 and M6 which are operating in the saturation region, equation (5.30) is re-written as

$$I_1 + \Delta V_{IN} V_{DS1} = I_2 \quad (5.37)$$

$$I_5 + \Delta V_{IN} V_{DS1} = I_6 \quad (5.38)$$

$$\frac{\beta_5^*}{2}(V_{CLK} - V^*_{thn5})^2 + \Delta V_{IN} V_{DS1} = \frac{\beta_6^*}{2}(V_{CLK} - V^*_{thn6})^2 \quad (5.39)$$

$$V^*_{thn5,6} = V_{thn} + \Delta V_{thn5,6} \quad (5.40)$$

$$\beta^*_{5,6} = \beta + \Delta\beta_{5,6} \quad (5.41)$$

Substituting equation (5.40)-(5.41) into (5.39), we obtain

$$\left(\frac{\beta+\Delta\beta_5}{2}\right)(V_{CLK}-V_{thn}-\Delta V_{thn5})^2+\Delta V_{IN}\,V_{DS1} = \left(\frac{\beta+\Delta\beta_6}{2}\right)(V_{CLK}-V_{thn}-\Delta V_{thn6})^2 \tag{5.42}$$

$$\left(\frac{1}{2}+\frac{\Delta\beta_5}{2\beta}\right)\left[\left((V_{CLK}-V_{thn})^2+(\Delta V_{thn5})^2-2(V_{CLK}-V_{thn})(\Delta V_{thn5})\right)+\Delta V_{IN}\,V_{DS1}\right] = \left(\frac{1}{2}+\frac{\Delta\beta_6}{2\beta}\right)[(V_{CLK}-V_{thn})^2+(\Delta V_{thn5})^2-2(V_{CLK}-V_{thn})(\Delta V_{thn5})] \tag{5.43}$$

By applying the property of independent and uncorrelated variables, the equation (5.43) becomes

$$\Delta V_{IN}\,V_{DS1} = \frac{\Delta\beta_6}{\beta}\frac{(V_{CLK}-V_{thn})^2}{2}-(V_{CLK}-V_{thn})(\Delta V_{thn6})-\frac{\Delta\beta_5}{\beta}\frac{(V_{CLK}-V_{thn})^2}{2}+(V_{CLK}-V_{thn})(\Delta V_{thn5}) \tag{5.44}$$

$$\Delta V_{IN} = \Delta V_{OS5,6} = \frac{\Delta\beta_6}{\beta}\frac{(V_{CLK}-V_{thn})^2}{2\,V_{DS1}}-\frac{(V_{CLK}-V_{thn})(\Delta V_{thn6})}{V_{DS1}}-\frac{\Delta\beta_5}{\beta}\frac{(V_{CLK}-V_{thn})^2}{2V_{DS1}}+\frac{(V_{CLK}-V_{thn})(\Delta V_{thn5})}{V_{DS1}} \tag{5.45}$$

$$\sigma^2_{V_{OS5,6}} = \sigma^2_{\beta_6}\left(\frac{(V_{CLK}-V_{thn})^2}{2\,V_{DS1}}\right)^2+\sigma^2_{V_{thn6}}\left(\frac{(V_{CLK}-V_{thn})}{V_{DS1}}\right)^2+\sigma^2_{\beta_5}\left(\frac{(V_{CLK}-V_{thn})^2}{2\,V_{DS1}}\right)^2+\sigma^2_{V_{thn5}}\left(\frac{(V_{CLK}-V_{thn})}{V_{DS1}}\right)^2 \tag{5.46}$$

$$\sigma^2_{V_{OS5,6}} = \sigma^2_{\beta_6}\frac{(V_{CLK}-V_{thn})^4}{4\,{V_{DS1}}^2}+\sigma^2_{V_{thn6}}\frac{(V_{CLK}-V_{thn})^2}{{V_{DS1}}^2}+\sigma^2_{\beta_5}\frac{(V_{CLK}-V_{thn})^4}{4\,{V_{DS1}}^2}+\sigma^2_{V_{thn5}}\frac{(V_{CLK}-V_{thn})^2}{{V_{DS1}}^2} \tag{5.47}$$

Similarly, considering the random offset from the mismatches between M3 and M6 which are operating in the saturation region, we get

$$\sigma^2_{V_{OS3,4}} = \sigma^2_{\beta_4} \frac{(V_{ION} - V_{s4} - V_{thn})^4}{4\,{V_{DS1}}^2} + \sigma^2_{V_{thn4}} \frac{(V_{ION} - V_{s4} - V_{thn})^2}{{V_{DS1}}^2} + \sigma^2_{\beta_3} \frac{(V_{IOP} - V_{s3} - V_{thn})^4}{4\,{V_{DS1}}^2} + \sigma^2_{V_{thn3}} \frac{(V_{IOP} - V_{s3} - V_{thn})^2}{{V_{DS1}}^2} \quad (5.48)$$

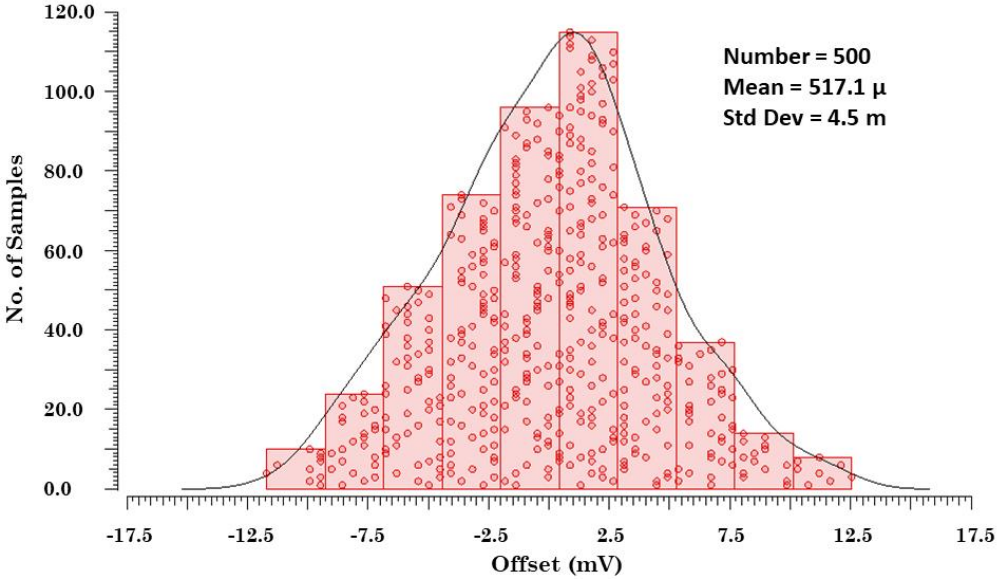


Figure 5.17 Monte Carlo simulation of Syn-DVC5 to calculate the offset voltage

Therefore, the overall static voltage $\sigma^2_{V_{OS}}$ obtained from the mismatch in threshold voltage and current factor can be defined as follows:

$$\sigma^2_{V_{OS}} \approx \sigma^2_{V_{OS1,2}} + \sigma^2_{V_{OS8,11}} + \sigma^2_{V_{OS5,6}} + \sigma^2_{V_{OS3,4}} \quad (5.49)$$

$$V_{OS} \approx \sigma_{V_{OS}} \approx \sqrt{\sigma^2_{V_{OS1,2}} + \sigma^2_{V_{OS8,11}} + \sigma^2_{V_{OS5,6}} + \sigma^2_{V_{OS3,4}}} \quad (5.50)$$

Figure 5.17 shows the Monte Carlo simulation for 500 runs to observe the effect of mismatches and process variations on offset voltage. From the figure it is observed that the mean value of offset voltage is 517.1 µV with the standard deviation of 4.5 mV.

5.4.2.3 Power of Syn-DVC5

Figure 5.18 (a) shows that average current consumed by the proposed circuit is 148.8 µA at 1.8 V supply and therefore the total power consumed by the proposed circuit is 267.84 µW. Figure 5.18 (b) shows the power and delay variation with respect to input amplitude.

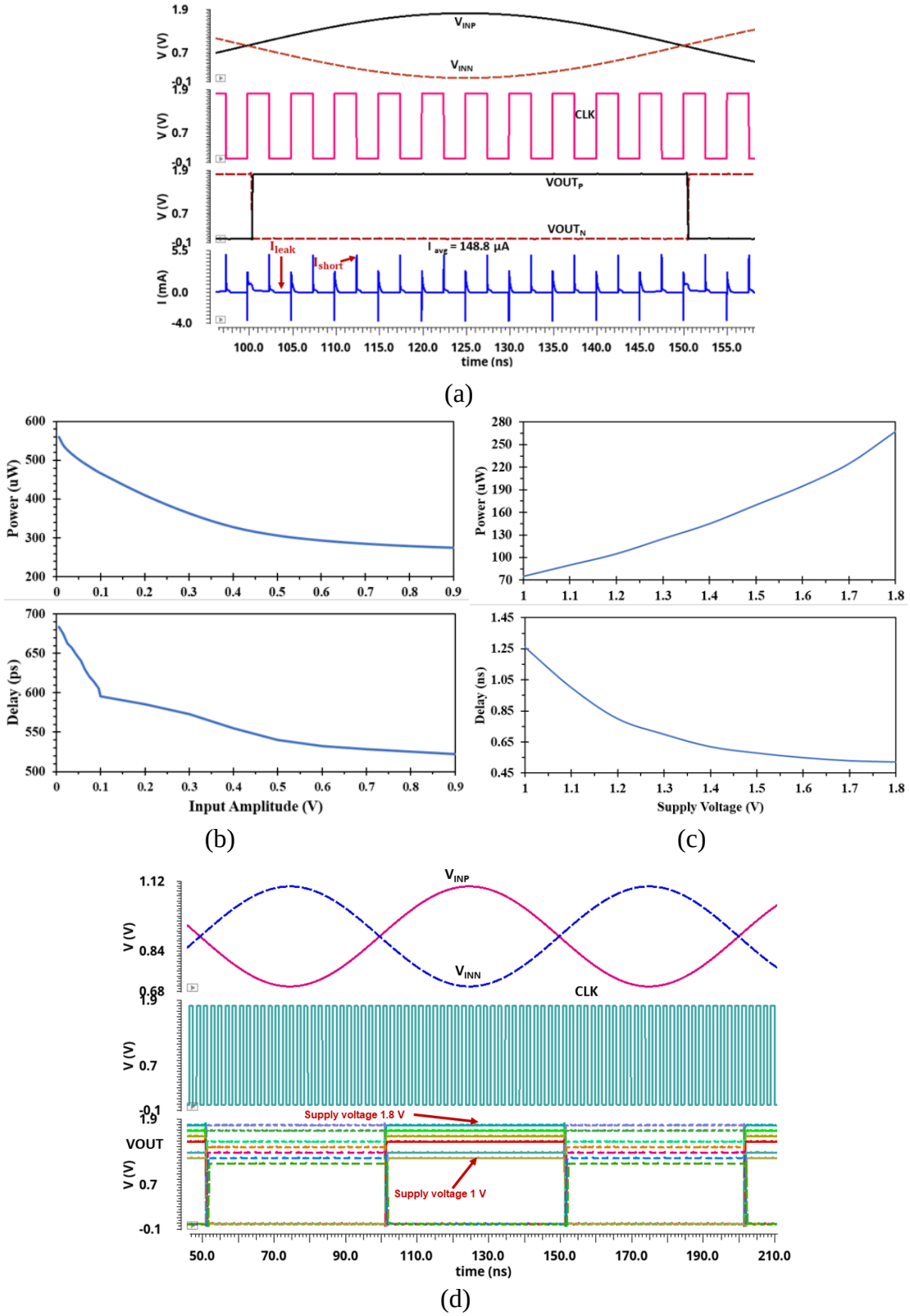


Figure 5.18 (a) Transient analysis to show the current variation (b) Variation of delay and power with input amplitude (c) Variation of delay and power with supply voltage (d) Transient analysis for the supply range of 1 V to 1.8 V

From the figure, it is observed that power and delay are maximum at lower input amplitude difference, and it decreases with an increase in input amplitude. With the scaling of the supply voltage, the power consumption of the circuit reduces, but the delay of the circuit increases, as shown in Figure 5.18 (c). The proposed circuit is working for the supply range of 1 V to 1.8 V as shown in Figure 5.18 (d).

Figure 5.19 shows the physical layout of the proposed analog voltage comparator drawn using SCL 180 nm CMOS technology which consumes 52 µm × 14 µm area *i.e.*, 728 µm^2. Figure 5.20 (a) shows the pre-layout and post-layout simulation results of power and delay versus input amplitude. Delay and power variations with the supply voltage ranging from 1 V to 1.8 V for the pre-layout and post-layout simulation is shown in Figure 5.20 (b).

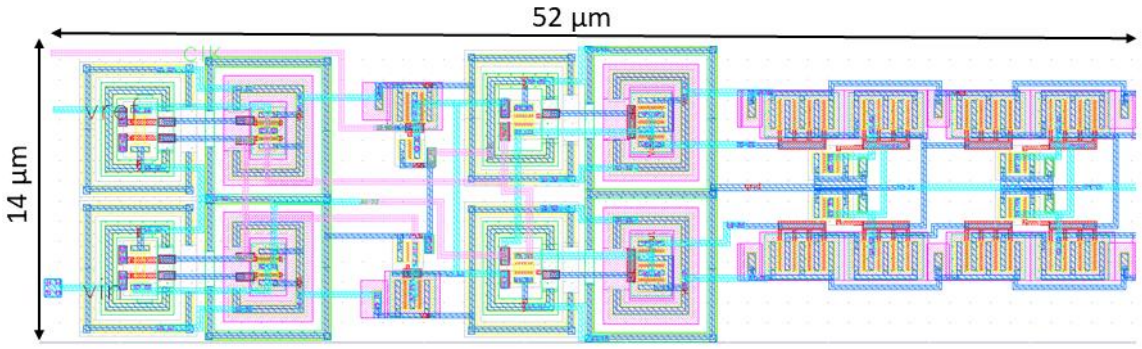
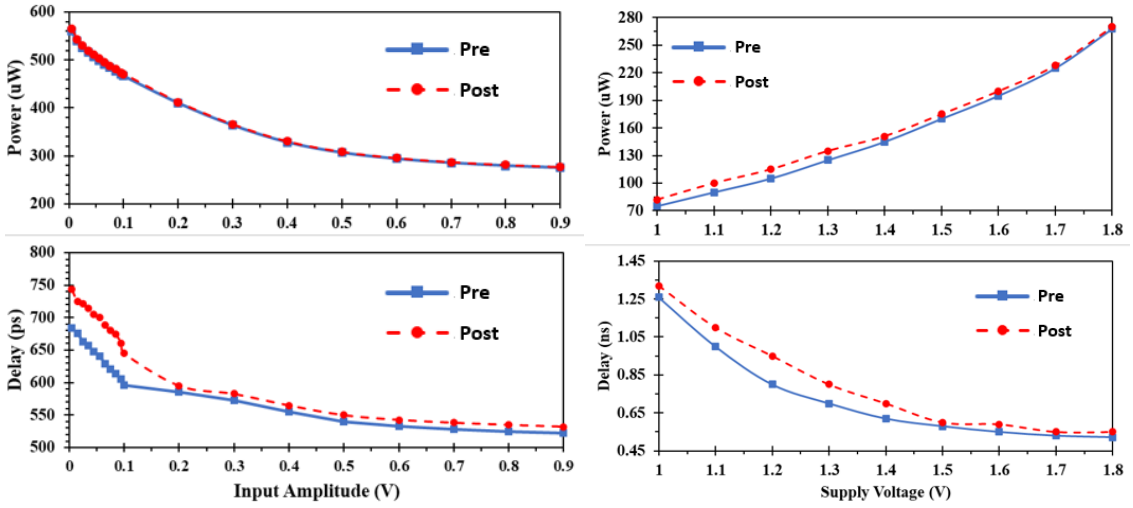


Figure 5.19 Layout of analog voltage comparator (Syn-DVC5)



(a) (b)

Figure 5.20 (a) Pre and post layout simulations of power and delay versus input amplitude (b) Pre and post layout simulations of power and delay versus supply voltage

Table 5.4 Comparison table for the post layout simulations of proposed FD-DVC4 versus proposed Syn-DVC5

Parameters	**FD-DVC4**	**Syn-DVC5**
Delay (ns)	0.79	0.532
Power (µW)	315	269.8
Offset (mV)	0.78	0.72
Supply Voltage (V)	1 to 1.8	1 to 1.8
Technology (nm)	180	180
Methodology	Digital	Digital
Layout Area (µm^2)	879.75	728

The performance parameters of the proposed comparators FD-DVC4 and Syn-DVC5 are compared and shown in Table 5.4. It is observed that the value of delay, power and offset voltage of Syn-DVC5 is lesser as compared to that of the FD-DVC4. Therefore, all-digital 6-bit flash ADC has been implemented using a Syn-DVC5.

5.5 Implementation of All-Digital 6-bit Flash ADC

The 6-bit flash ADC is designed and implemented using digital-in-concept design methodology. The all-digital 6-bit flash ADC comprises of a delay ladder, TVCs, array of comparators (Syn-DVC5), and an encoder, as shown in Figure 5.1 (b). The voltage reference ladder consists of delay ladder and TVCs to generate the reference voltages. The design has been simulated in 180 nm SCL CMOS technology at 1.8 V supply voltage using Cadence virtuoso. The reference voltages generated by the reference ladder are compared with the input signal with the help of comparators. The value of the reference voltages is 1 LSB apart from its preceding value by

$$\mathrm{LSB} = \frac{1.8\ \mathrm{V} - 0.46\ \mathrm{V}}{64} \approx 20\ \mathrm{mV} \tag{5.51}$$

The comparator's output is the thermometer code, which is then translated to binary using the Wallace tree encoder. Figure 5.21 shows the 6-bit Wallace tree encoder which consists of full adders to add the number of ‘1’s and provides the output in binary format.

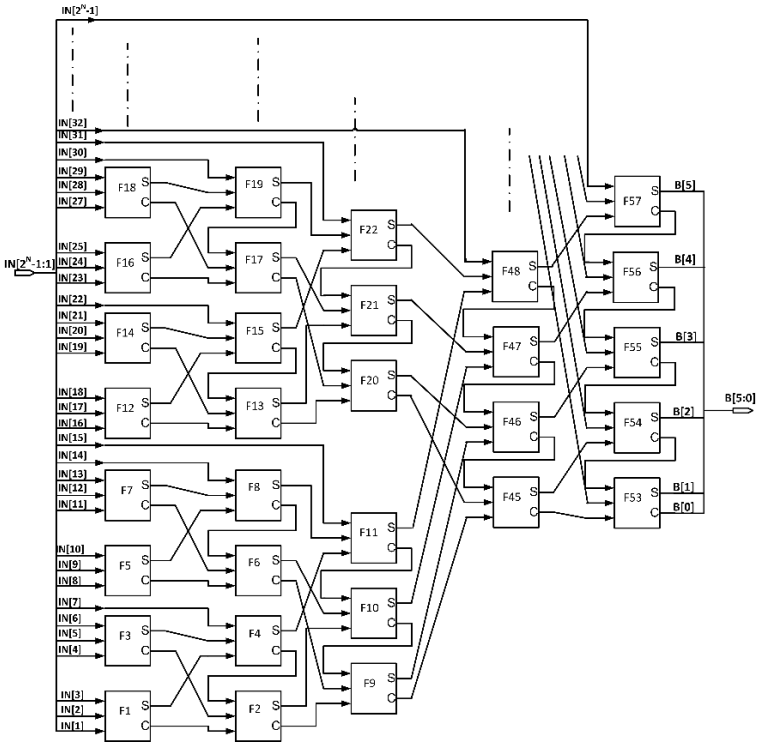
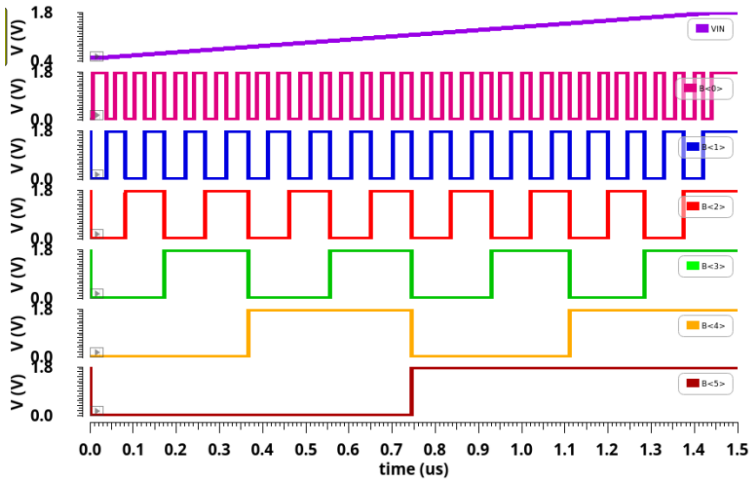
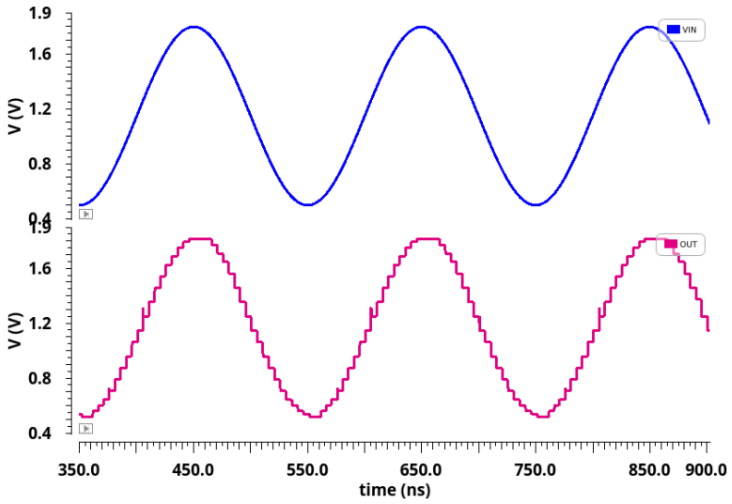


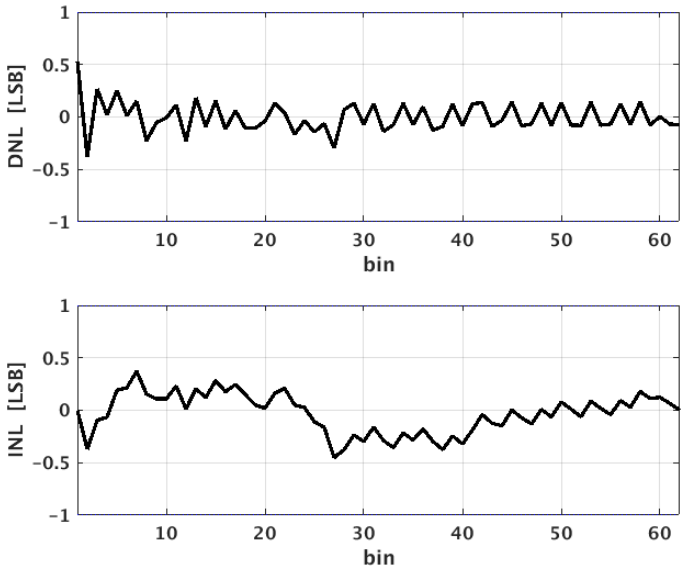
Figure 5.21 6-Bit Wallace tree encoder (63:6)



(a)



(b)



(c)

Figure 5.22 (a) Simulated result of 6-bit all-digital flash ADC with slow input ramp (b) Transient analysis of the sinusoidal input at the input frequency of 5 MHz (c) INL and DNL at the supply voltage of 1.8 V

Figure 5.22 (a) shows the 6-bit digital output B <5:0> with respect to the slow ramp input analog signal. The transient analysis of the sinusoidal analog input signal at the input frequency of 5 MHz and clock frequency of 200 MHz is shown in Figure 5.22 (b). The measured value of the INL and DNL is ±0.5 LSB and ±0.4 LSB, respectively as shown in Figure 5.22 (c).

For the different values of the input frequency and clock frequency, different dynamic parameters such as SNDR, SFDR, SNR and ENOB have been calculated as shown in Table 5.5.

The value of F_{in} is calculated using the following formula

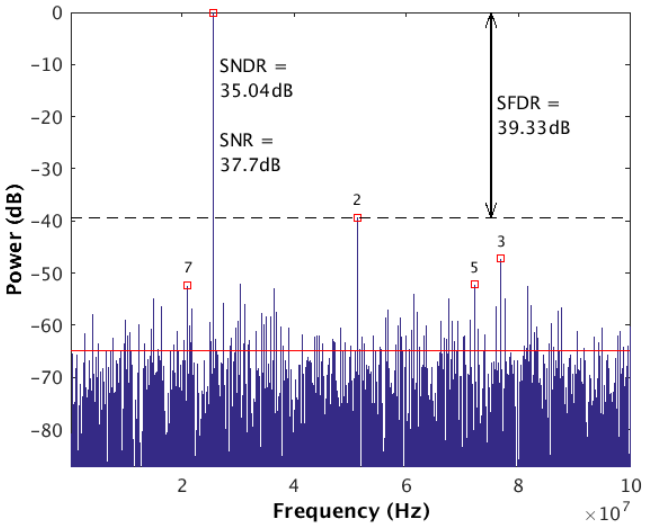
$$F_{in} = \frac{M}{N} \times F_{clk} \tag{5.52}$$

where F_{clk} is the clock frequency, and M is a prime number, N is the number of FFT points.

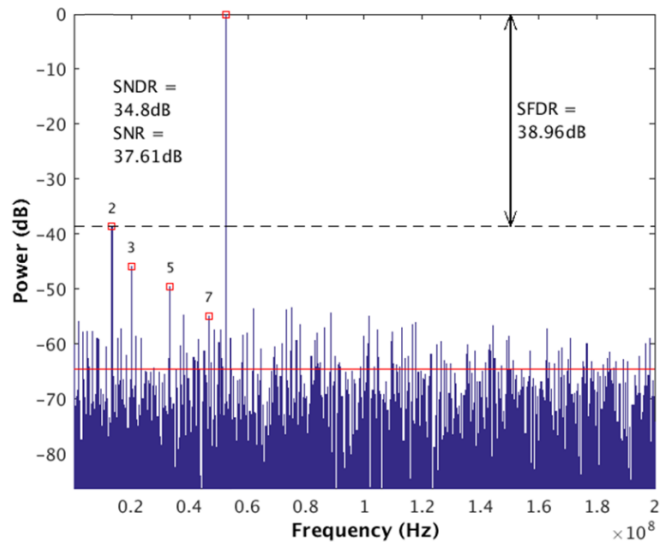
Table 5.5 Dynamic parameters of all-digital 6-bit flash ADC

F_{clk} (MHz)	F_{in} (MHz)	SNDR (dB)	SNR (dB)	ENOB (dB)	SFDR (dB)
100	16.89	35.23	37.82	5.56	39.62
200	25.58	35.05	37.7	5.53	39.33
300	38.37	34.87	37.5	5.5	39.04
400	51.17	34.8	37.61	5.49	38.96

The FFT spectrum of the reconstructed signal at 200 MHz sampling frequency and 25.58 MHz input signal frequency is plotted in Figure 5.23 (a). Also, the FFT spectrum of reconstructed output signal at the 400 MHz sampling frequency and 51.17 MHz of input signal frequency is observed in Figure 5.23 (b). Figure 5.23 (c), 5.23 (d), and 5.23 (e) show the value of ENOB, SNR, and SNDR with the variation in input frequency at F_{clk} of 200 MHz.



(a)



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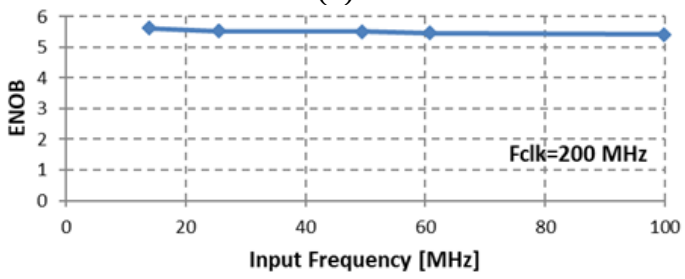
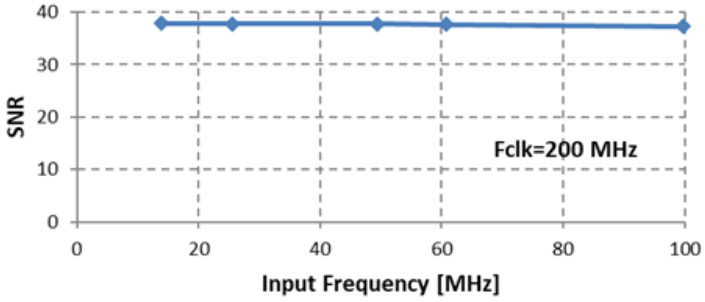
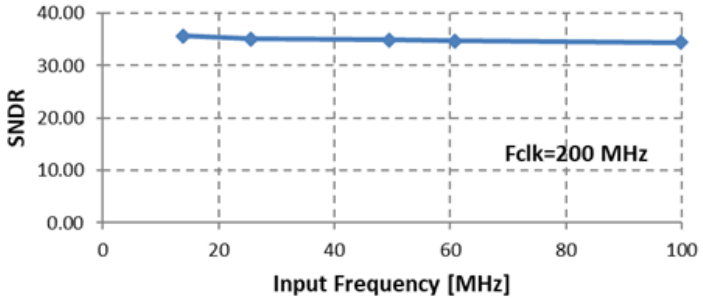


(c)



(d)



(e)

Figure 5.23 (a) FFT of the proposed all-digital 6-bit flash ADC at F_{in} = 25.58 MHz and F_{clk}=200 MHz (b) FFT of the proposed all-digital 6-bit flash ADC at F_{in} = 51.17 MHz and F_{clk}=400 MHz (c) Variation of ENOB with the variation in input frequency (d) Variation of SNR with the variation in the input frequency (e) Variation of SNDR versus input frequency

5.6 Layout and Post Layout Simulations of All-Digital 6-bit Flash ADC

The physical layout of the proposed all-digital 6-bit flash ADC is drawn using SCL 180nm CMOS technology. It consumes a chip's core area of 534.53 µm × 301.2 µm and integrated in a 2 mm × 2 mm die. Figure 5.24 shows the complete chip layout of the proposed ADC including PADS and seal ring.

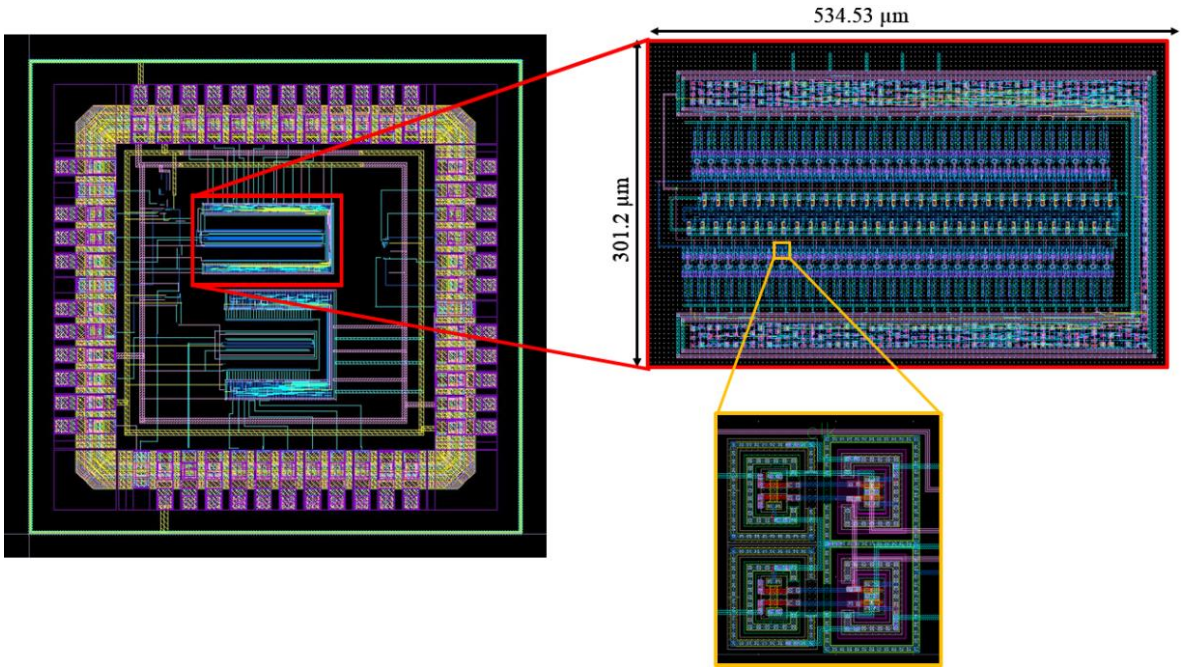
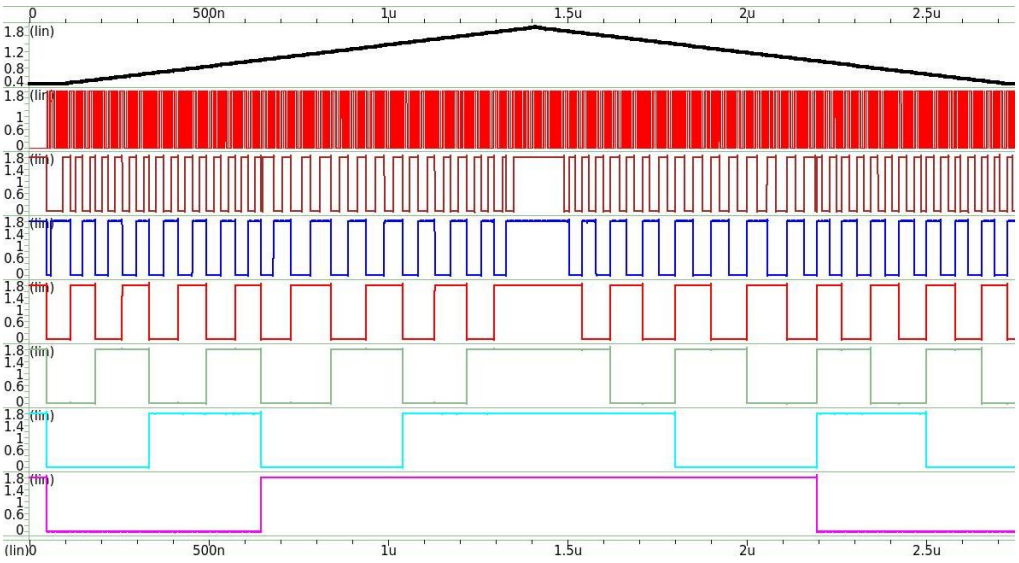
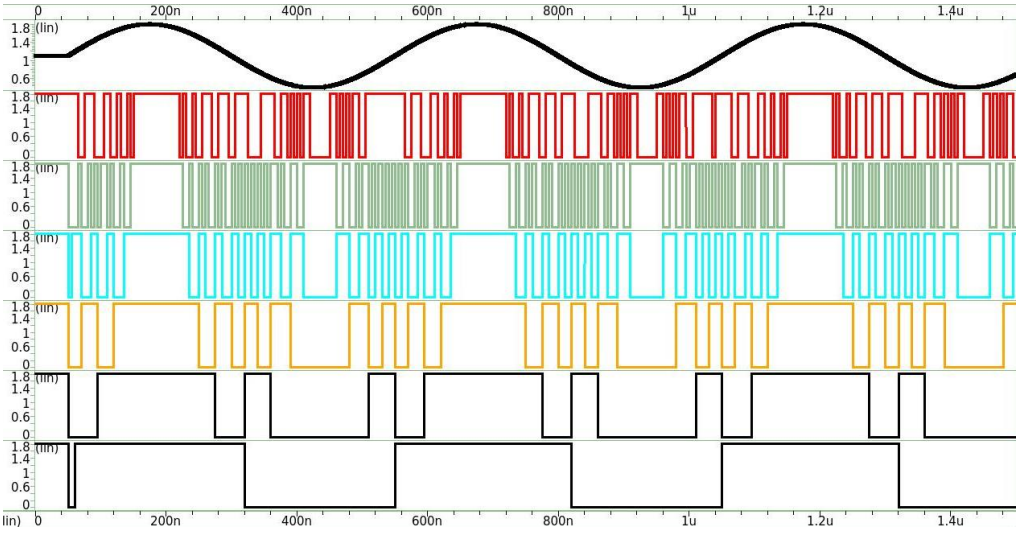


Figure 5.24 Layout of 6-bit all-digital flash ADC

The post-layout results of the proposed 6-bit flash ADC are discussed below. Figure 5.25 (a) and Figure 5.25 (b) shows the 6-bit digital output B <5:0> with respect to the slow ramp input analog signal and sinusoidal signal, respectively, at a clock frequency of 400 MHz. The measured value of the INL and DNL after post layout simulations are +0.7/−0.2 LSB and ±0.5 LSB, respectively as shown in Figure 5.26. Figure 5.27 (a) and Figure 5.27 (b) shows the post-layout FFT of the proposed all-digital 6-bit flash ADC at Fin = 25.58 MHz, Fclk=200 and at Fin = 51.17 MHz, Fclk=400 MHz, respectively. The total power consumed by various blocks in 6-bit flash ADC is 16.6 mW, as shown in Figure 5.28. The post layout simulation results show the ENOB, SNDR, SNR and SFDR are 5.33, 33.8 dB, 35.2 dB and 39.73 dB, respectively at a sampling frequency of 400 MHz. Pre-layout and post-layout performance analysis of the proposed 6-bit Flash ADC is discussed in Table 5.6.



(a)



(b)

Figure 5.25 (a) Post-layout results of 6-bit all-digital flash ADC with slow input ramp (b) Post-layout transient analysis of the sinusoidal input

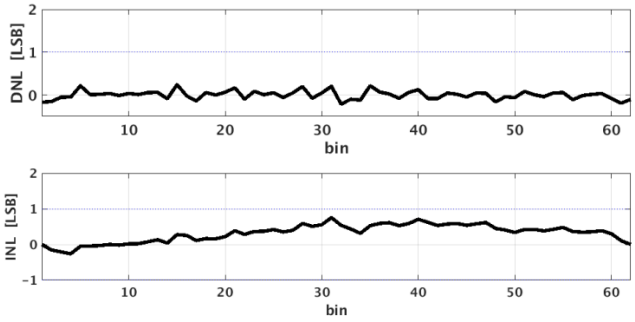
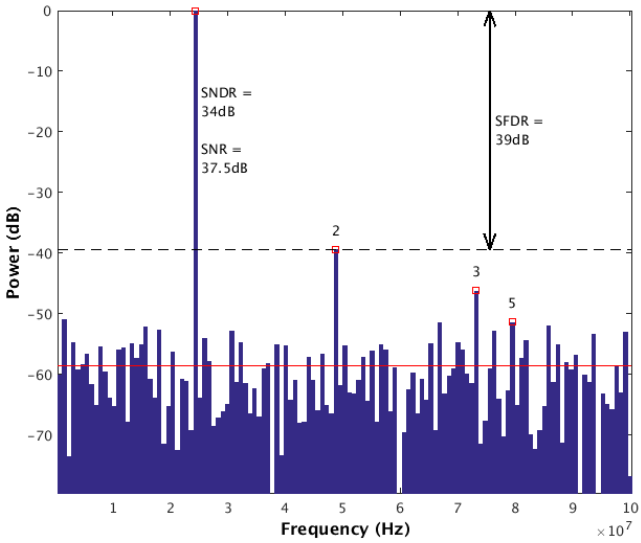
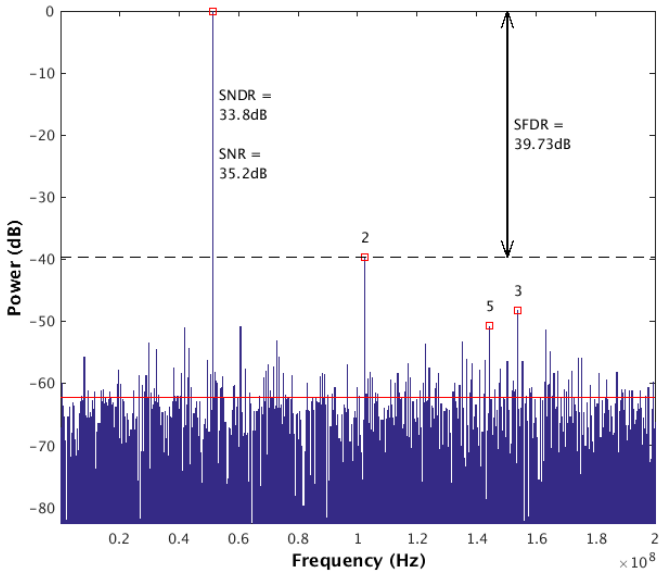


Figure 5.26 Measured post-layout value of INL and DNL



(a)



(b)

Figure 5.27 (a) Post-layout FFT of the proposed all-digital 6-bit flash ADC at F_{in} = 25.58 MHz and F_{clk}=200 MHz (b) Post-layout FFT of the proposed all-digital 6-bit flash ADC at F_{in} = 51.17 MHz and F_{clk}=400 MHz

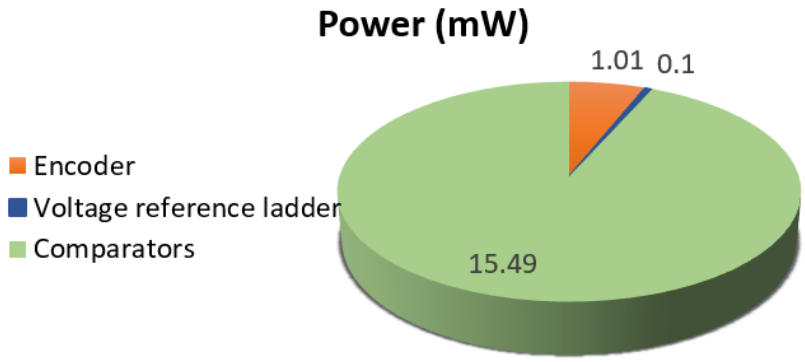


Figure 5.28 Power analysis of all-digital 6-bit Flash ADC

Table 5.6 Results of the proposed all-digital 6-bit flash ADC

Parameters	**Pre-layout ADC results**	**Post-layout ADC results**
Supply voltage (V)	1.8 V	1.8 V
Resolution	6	6
Max. Sampling Frequency (MHz)	400	400
SNDR (dB)	34.8	33.8
SNR (dB)	37.61	35.2
SFDR (dB)	38.96	39.73
INL (LSB)	±0.5	+0.7/−0.2
DNL (LSB)	±0.4	±0.5
ENOB (bits)	5.49	5.33

The performance parameters of the proposed all-digital 6-bit flash ADC and existing state-of-the-art ADCs are listed in Table 5.7. For a fair comparison FOM (equation (1.11) has also been presented. From the table, it can be seen that the proposed 6-bit flash ADC have lower FOM than the existing ADCs [29, 31, 37, 40, 51, 69, 83-88] The input range of the proposed 6-bit ADC is better than other existing designs. The all-digital 6-bit ADC has achieved higher ENOB at 1.8 V 180 nm CMOS technology. Because of the digital-in-design concept, the power consumed by the proposed all-digital flash ADC is very less as compared to other state-of-the-art work [29, 37, 40, 51, 67, 83-89]. As the number of comparators required in the proposed all-digital flash ADC design is very less as compared to the flash ADCs designed using digital-based stochastic approach [29, 31, 37, 40, 51]. Hence, the area of the proposed ADC is less. Also, the proposed ADC design can easily be migrated to lower CMOS technologies, and its performance can be further improved.

Table 5.7 Performance comparison of all-digital 6-bit flash ADC with existing flash ADCs in literature

References→ Parameters↓	**This work"**	**[29]"**	**[31]"**	**[37]"**	**[40]"**	**[51]"**	**[67]**	**[69]"**	**[83]**	**[84]**	**[85]**	**[86]**	**[87]**	**[88]**	**[89]**
Technique	**All-digital**	Stocha-stic	Stochastic/ 2-group comparator	Inverse Gauss-ian	8-group comp., inverse gaussian	2-group comp. & ref. swapping	Offset cance-lation	Time-domain	Conve-ntional	Voltage Interpola-tion Based	Ratio averaging scheme	Digital calibra-tion	Offset calibra-tion	Off-chip calibra-tion	Offset Drift Suppress
Supply voltage (V)	**1.8**	1.2	0.9	1.2	1	0.9	1.8	1.8	1.8	1.2	3.3	1.2	0.9	1.2	1.15
Tech. (nm)	**180**	90	180	90	130	65	180	180	180	90	350	90	40	90	45
Resolution	**6**	4	6	-	-	7	6	5	6	6	6	6	6	7	7
ENOB (bits)	**5.33**	3.69	5.3	5.7	5.2	5.7/6.2*	5.06	3.89	4.85	3/5.29*	5.06	3/5.1*	5.3*	6.05	6.05
Max. Samp. Freq. (MHz)	**400**	1500	8	210	320	100	2000	400	400	2000	800	2000	3500	1500	1400
Power (mW)	**16.6**	23	0.6	34.8	87	33	35	16	70	25	45.12	28	242	204	33.24
SNDR (dB)	**33.8**	23.97	33.5	35.89	32.8	39	32.25	25.2	31	33.5	32.24	32.7	34	-	39
INL (LSB)	**+0.7/ −0.2**	<0.53	-0.99	-	-	-	-	1.7	-	+0.36/-0.32	-	0.4	0.4/0.5	0.64/0.7	<1
DNL(LSB)	**±0.5**	<0.38	-0.76	-	-	-	-	1	-0.75	+0.39/-0.42	-	0.38	-	-	<0.74
Analog input swing (mVpp)	**1300**	100	280	280	800	440	-	1	-	720	-	800	400	600	700
Number of comparators	**63**	63	7680	2047	2040	8190	-	-	63	63	63	-	63	-	-
FOM (pJ/conv.)	**1.03**	1.2	1.9	3.2	7.3	6.3/ 4.49*	0.52	2.7	6.06	1.56/0.32*	1.7	1.75/ 0.41*	1.7	2.05	0.36

*ADC with Calibration " Digital-in-concept ADCs

5.7 Conclusion

The proposed all-digital 6-bit flash ADC is designed in 180 nm CMOS SCL technology at a supply voltage of 1.8 V. The proposed all-digital design is cost-effective, scalable, and more immune to PVT variations. A novel fully digital-in-concept voltage reference ladder has been proposed which consists of the delay-based reference ladder and time-to-voltage converter. It works in the range of 0.46 V to 1.8 V with an LSB of 20 mV approximately. The proposed voltage reference ladder consumes an average power of 0.1 mW with the negligible effect of PVT variations on its performance. The proposed Syn-DVC5 has been chosen to demonstrate an all-digital 6-bit flash ADC due to its low power, less area, less delay and low offset voltage. The physical layout of the chip consumes an area of 534.53 µm × 301.2 µm and integrated in a 2 mm × 2 mm die. The post layout simulation results show that power consumed by the proposed ADC is 16.6 mW at a sampling frequency of 400 MHz. The ENOB, SNDR, SNR, and SFDR are 5.33, 33.8 dB, 35.2 dB and 39.73, respectively. The calculated values of INL and DNL are +0.7/−0.2 LSB and ±0.5 LSB, respectively. It achieved lower FOM value than the existing digital-based ADC which indicates that proposed digital-in-concept flash ADC has better performance parameters.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

In the present work, a methodology has been proposed to design analog/mixed signal circuits using digital-in-concept circuits in digital technology. To demonstrate the methodology, a flash ADC has been chosen for SoC applications. The three fundamental building blocks of flash ADC are comparators, voltage reference ladder and an encoder. The comparators and voltage reference ladder being analog in nature, have been redesigned using digital-in-concepts circuits. The major conclusions drawn are as follows:

- The different versions of digital-based analog comparators (Pseudo-DVC1, Pseudo-DVC2 and Pseudo-DVC3) have been proposed for the full input range. It is observed that the proposed pseudo comparators have power dissipation is in the range of 75 µW to 196 µW, an offset voltage less than 4.97 mV with the maximum delay of 2.9 ns. The minimum FOM of the proposed comparators is 1.2 fJ/conv which are better than the existing state-of-the-art work available in the literature.
- Some of the proposed comparators were implemented on FPGA to verify the functionality.
- In addition, a fully-digital analog comparator (FD-DVC4) has been designed. The offset voltage, delay and power of the post layout are 0.78 mV, 0.79 ns and 315 µW, respectively and the physical layout occupies an area of 879.75 μm^2.
- Also, a synthesizable analog voltage comparator (Syn-DVC5) has been designed. The post-layout simulations show an offset of 0.72 mV, delay of 0.532, and power as 269.8 µW and the area consumed by layout is 728 μm^2.
- A novel fully digital-in-concept voltage reference ladder has been proposed which consists of a delay-based network and time-to-voltage converter. It works in the range of 0.46 V to 1.8 V with an LSB of 20 mV approximately. The proposed voltage reference ladder consumes an average power of 0.1 mW with the effect of negligible PVT variations. The mean value of consecutive delay cell is 60 ps and standard deviation is 0.32 ps. Also, it is robust against PVT variations.
- Various 4-bit flash ADC (ADC-I, ADC-II, and ADC-III) and 5-bit flash ADC (ADC-IV) have been implemented using the proposed comparators. The 4-bit flash ADCs have been designed using Pseudo-DVC1 and Pseudo-DVC2 at the clock frequency of 200 MHz. Further, 4-bit

flash ADC and 5-bit flash ADC have been designed at the frequency of 400 MHz using Pseudo-DVC3 which are suitable for low-power SoC applications. The achieved FOM of the proposed 4-bit and 5-bit ADCs are 0.81 pJ/conv. and 0.55 pJ/conv., respectively and are less as compared to the existing ADCs.

- The synthesizable comparator has been chosen to implement an all-digital 6-bit flash ADC due to its low power, low offset voltage, and high speed. The proposed all-digital 6-bit flash ADC is designed in 180 nm 1.8 V CMOS SCL technology. The physical layout of the chip's core consumes an area of 534.53 µm × 301.2 µm and is integrated in a 2 mm × 2 mm die.
- The achieved FOM of the proposed all-digital 6-bit flash ADC is 1.03 pJ/conv. The power consumed by the proposed ADC is 16.6 mW at a sampling frequency of 400 MHz. The ENOB, SNDR, SNR and SFDR for this ADC are 5.33, 33.8 dB, 35.2 dB and 39.73, respectively. The calculated values of INL and DNL are +0.7/−0.2 LSB and ±0.5 LSB, respectively. Due to digital-in-concept circuits, the proposed all-digital flash ADC is suitable for low power and high speed SoC application with reduced design effort and less time-to-market.

6.2 Future Scope of Work

A methodology has been proposed to design analog/mixed signal circuits using digital-in-concept circuits and has been demonstrated using a 6-bit flash ADC. The work can be extended to the following.

- The proposed concept can be applied to implement the other types and architecture of ADCs.
- The proposed concept can also be extended to other types of analog/mixed signal circuits such as PLL, LDO, *etc.*
- The proposed methodology can be used to develop a CAD tool to synthesize analog/mixed signal circuits from RTL to the layout.

List of Publications

SCI Journal Papers

- Ashima Gupta, Anil Singh and Alpana Agarwal, "Highly-Digital Voltage Scalable 4-bit Flash ADC*", IET Circuits, Devices & Systems*, vol.13, no. 1, pp. 91-97, 2019. DOI: 10.1049/iet-cds.2018.5148. (SCI Journal**, Impact factor-1.297**).
- Ashima Gupta, Anil Singh and Alpana Agarwal, "Implementation of Low Supply Rail-to-Rail Differential Voltage Comparator on Flexible Hardware for a Flash ADC," *Journal of Circuits, Systems and Computers*, vol. 29, no. 5, pp. 2050073 (1-21), 2019. DOI: 10.1142/S0218126620500735. (SCI Journal**, Impact factor-1.333**).
- Ashima Gupta, Anil Singh and Alpana Agarwal, "A full input range, 1–1.8 V voltage supply scalable analog voltage comparator in 180nm CMOS", *International Journal of Electronics*, vol. 108, no. 8, pp. 1360-1380, 2021. DOI: 10.1080/0020 7217.2020.1870724. (SCI Journal**, Impact factor-1.336**).
- Ashima Gupta, Anil Singh, Alpana Agarwal, "A low-power high-resolution dynamic voltage comparator with input signal dependent power down technique", *AEU - International Journal of Electronics and Communications*, vol. 134, pp. 152382 (1-10), 2021. DOI: 10.1016/j.aeue.2021.153682. (SCI Journal**, Impact factor-3.183**).
- Ashima Gupta, Anil Singh and Alpana Agarwal, "A Scalable Fully-Digital Differential Analog Voltage comparator", *Journal of Circuits, System and Computers*. vol. 31, no. 04, pp. 2250059 (1-25), 2022. DOI: 10.1142/S0218126622500591. (SCI Journal**, Impact factor-1.333**).
- **Ashima Gupta**, Anil Singh, Manu Bansal and Alpana Agarwal, "Functional validation of highly synthesizable voltage comparator on FPGA", Integration. (2022) DOI:https://doi.org/ 10.1016/j.vlsi.2022.02.004. (SCI Journal**, Impact factor-1.211**).

Patent

Ashima Gupta, Anil Singh and Alpana Agarwal, (2022). *An advanced system of All-Digital Voltage Reference Ladder for Analog-to-Digital Converter*. (Indian Patent Application Filed)

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