Power Efficient High DC Gain Adaptive Biased CMOS Operational Transconductance Amplifier

A dissertation submitted in partial fulfilment of the requirement for the award of degree of

Master of Technology

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VLSI Design

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DECLARATION

I hereby declare that the work which is presented in the dissertation entitled, **"Power Efficient High DC Gain Adaptive Biased Operational Transconductance Amplifier"** in partial fulfilment of the requirement for the award of degree of Master of Technology in VLSI Design submitted in Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Dr. Rishikesh Pandey, Assistant Professor, ECED and refers other researcher's work which are duly listed in the reference section.

The matter presented in this dissertation has not been submitted in any other University/Institute for the award of degree.

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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ABSTRACT

The rapid increasing use of battery operated portable equipment in the application areas such as telecommunication and medical electronics have increased the importance of low power and small sized circuits realized with VLSI technology. The most efficient way to reduce power consumption is to decrease both the supply voltage and the stand-by current. Reduced supply voltage is not a favourable choice for analog design since it leads to several performance degradations because threshold voltage of MOS transistors does not scale well with the reduced supply. Therefore, current becomes more favourable than voltage as the information-carrying quantity in a low-voltage low-power environment. A circuit using current mode technique has many advantages such as larger dynamic range, higher bandwidth, greater linearity, simpler circuitry and low power consumption. Operational Transconductance Amplifier (OTA) is an important building block of current mode circuit in analog design. To achieve lower stand-by power consumption in OTAs by reducing stand-by current is a better choice. Adaptive biasing technique may be very useful in this context. Also high dc gain of the OTA is a very important parameter to ensure the performance of the whole system. However, it is becoming more and more difficult to obtain high dc gain of OTA with low voltage operation. Hence, the technique of partial positive feedback is explored which is a good way to boost the gain without speed penalty.

In the dissertation, current adder, current subtractor and a Power Efficient High DC Gain Adaptive biased CMOS OTA are proposed. The proposed CMOS OTA circuit is developed using the proposed current subtractor, which provide adaptive biasing in OTA. For achieving improved DC gain, the partial positive feedback loop is used. The proposed circuits are simulated using UMC 0.18μm CMOS technology process parameters and the simulation results are presented. The layouts of all the proposed circuits are designed using Cadence Virtuoso XL Design Environment tool. The performance parameters of the proposed CMOS OTA have also been compared with the existing similar OTA circuits available in literature to demonstrate the effectiveness of the proposed circuit.

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LIST OF SYMBOLS

g_m	Transconductance
I	Current
V	Voltage
V_{GS}	Gate-source voltage
V_{DS}	Drain-source voltage
V_T	Thermal Voltage
V_{DSat}	Drain saturation voltage
V_{TH}	Threshold Voltage
W	Channel Width
L	Channel Length
K	Boltzmann's Constant
T	Temperature
q	Charge on electon
e	Exponential function
μ_n	Charge-carrier effective mobility
C_{ox}	Gate-oxide capacitance per unit area
β	Loop Gain
MN	NMOS Transistor
MP	PMOS Transistor
dB	Decibel

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ABBREVIATIONS

CMOS	Complementary Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
VMC	Voltage Mode Circuit
CMC	Current Mode Circuit
OTA	Operational Transconductance Amplifier
VCCS	Voltage Controlled Current Source
GBW	Gain Bandwidth
UGF	Unity Gain Frequency
CCM	Cascode Current Mirror
SR	Slew Rate
CMRR	Common Mode Rejection Ratio
PSRR	Power Supply Rejection Ratio
ICMR	Input Mode Common Range
DRC	Design Rule Check
LVS	Layout Versus Schematic

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

The ever increasing inclination towards the portable electronic equipment brings forth the need of low power operation in battery operated electronic products such as implantable medical electronic devices like cardiac pacemakers, hearing aids, handheld multimedia gadgets, cell phones etc. In order to get reasonable battery life and weight for these electronic applications, achieving low power dissipation is indispensable. Since the battery contributes to the significant volume and weight to the device, the ultimate target is to achieve the battery less operation. Therefore the voltage levels associated with these power sources are of significant concern. Also, in sub-micron technology as the feature size of CMOS process scales down, the supply voltage has to be lowered for reduction in power dissipation per cell. Supply voltage reduction ensures the reliable operation of the MOS device as the lower electrical fields inside layers of a MOSFET poses less risk to the thinner gate-oxides (only several nanometre thick), which results from device scaling**.** The other concern emanates from the increasing integration of components/devices on a single chip. The heat removal and internal power distribution introduces major problems in the growth of CMOS circuits on the given area of chip. The cost of heat removal (i.e. cooling, to prevent the overheating of chip) has resulted in considerable concern in power reduction even in non-portable electronic applications. The most usual practice adopted to reduce power consumption is operating circuit at lower supply voltages. However, the reduced power supply voltage is generally not a favourable choice for analog design and a low supply voltage may require some exceptional/novel circuit techniques. Low voltage analog circuit design deviate appreciably from those of high voltage analog circuit design [1, 2]. The conventional voltage mode circuits (VMC) used in analog design, suffers from problems of reduced voltage swings, bandwidth and slew rate limitations etc. when operated in low voltage environments. This necessitates the adaptation of alternative analog design techniques to accommodate the low

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supply voltage environments. The current mode approach turns out to be a better option for low voltage high performance analog circuit design, in which the circuit designer is more involved with current levels for the operation of the circuits. The voltage levels present at various nodes are irrelevant. So, if the input and output signals are currents, some of the preceding demerits could be eliminated [3]-[5]. In order to conserve the compatibility with current mode circuit, it is often essential to convert the input voltage to output current that can be achieved by a transconductor [6]. Operational transconductance amplifier (OTA) is an important current mode device whose input signal is voltage, and its output signal is in the form of current. Thus, OTA's function is to transfer the input voltage into the output current. Operational transconductance amplifiers (OTAs) are extensively used as one of the most significant building blocks in analog and mixed-mode circuits. An ideal operational transconductance amplifier (OTA) is a voltage-controlled current source (VCCS) with a constant transconductance and infinite input/output impedances.

1.2 MOTIVATION

The trend towards lower operating supply voltages is strongly motivated by some prominent factors such as

- requirement of portable electronic equipment which favours low voltage- low power circuits,
- voltage limitations as a result of scaling of feature size in modern deep submicron CMOS process technology
- large scale integration on the same area of chip which is limited by power dissipation/overheating of chip.

The traditional analog voltage mode circuits (VMCs) are vulnerable to performance degradations when operated at low supply voltage. Reduction of power supply voltage causes decrease in signal dynamic range especially for voltage mode analog circuit designs. Also it suffers from gain bandwidth product limitation [7, 8]. Therefore, in low-power analog circuit design, current-mode signal processing has been usually been considered an attractive strategy because of its striking features such as high-speed operation and low-voltage compatibility. The main advantage of current mode circuit is apparent from the non- linear characteristics of MOSFET, where small change in input voltage produces a much larger change in the output current. For a fixed value of voltage, the dynamic range of current mode

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circuit (CMC) is larger than the voltage mode circuit (VMC). So even if the supply voltage is reduced, it is possible to get the required signals represented by current. The second advantage of CMC is that they are much faster (slew rate) than VMCs. In VMCs the parasitics present in the analog circuit has to be charged and discharged with changes in the voltage levels. However in CMC changes in current level is not always necessarily accompanied by voltage change and hence parasitic capacitances do not affect the speed of circuit operation in considerable manner. Also CMCs do not require specially processed resistors or capacitors and hence they are quite compatible with digital CMOS technology which favours the integration of mixed signal design [9]. The CMCs thus have the advantages of larger dynamic range, higher bandwidth, greater linearity, simpler circuitry and lower power consumption [7]-[10]. Operational Transconductor Amplifiers (OTAs) are widely used current mode devices which replace the conventional VMCs such as operational amplifier in low voltage operation [11]-[15].

Another crucial design aspect is the transistor's operating region. The distinctive behaviour of the MOS transistors in subthreshold/weak inversion region not only allows a designer to work at low voltage but also at low input bias current. So the behaviour of OTA in subthreshold region is explored in this dissertation.

In order to improve the amplifier's performance i.e. slew rate, without affecting GBW, biasing current has to be increased but this in turn raises the power dissipation as well. So the use of adaptive biasing technique helps to decrease static/standby power consumption without deteriorating circuit's dynamic performance. Also the transconductance gain of OTA is enhanced by a technique of controlled partial positive feedback which increases DC gain and unity gain frequency (UGF).

1.3 KEY CONTRIBUTIONS

The work in this dissertation can be summarized as follows:

1. Design and simulate the analog computational circuits such as current adder and current subtractor.
2. Design and simulate adaptive biased OTA in subthreshold and saturation regions of operation.

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3. Design and simulate DC gain enhanced adaptive biased CMOS OTA using controlled partial positive feedback technique

In the dissertation, current adder, current subtractor and adaptive biased OTA are proposed. The open loop DC gain of the proposed adaptive biased CMOS OTA has been improved by the technique of partial positive feedback. All the proposed circuits have been simulated using UMC 0.18μm CMOS process technology parameters and the simulation results have been presented to show the effectiveness of the circuits. Layout designs of the proposed circuits have also been presented using Cadence Virtuoso layout editor. The performance parameters of the proposed adaptive biased CMOS OTA has been compared with the existing OTAs available in literature and the comparison shows that the proposed adaptive biased CMOS OTA has high DC gain, better phase margin, high gain bandwidth product (GBW), high unity gain frequency (UGF), low standby current and low static power dissipation. The proposed circuits can be used for various analog signal processing applications such as filters, resistors, capacitors, integrators etc.

1.4 ORGANIZATION OF THE THESIS

The organization of thesis is as follows:

CHAPTER 2: The chapter addresses the operation of Operational Transconductance Amplifier (OTA), adaptive biasing of amplifiers, subthreshold region of operation for low voltage and low power analog design and DC gain enhancement techniques.

CHAPTER 3: In this chapter, the literature survey related to the low voltage low power adaptive biased OTA has been discussed.

CHAPTER 4: The chapter proposes the power efficient high DC gain adaptive biased OTA. The circuit parameters of power efficient high DC gain adaptive biased OTA are also discussed.

CHAPTER 5: The simulation results and layout designs of the proposed circuits have been presented in this chapter.

CHAPTER 6: The chapter summarizes the dissertation and suggests future scope of the work.

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CHAPTER 2

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

2.1 INTRODUCTION

In recent years, the quest of portable electronic equipment and with the advancement of CMOS fabrication process technology, analog circuits are also required to operate at low power supply voltage for low power consumption. Low voltage low power analog and mixed signal designs are gaining considerable attention. However, the performance of the analog circuits, including the linearity and dynamic range, deteriorates significantly because the amplitude of signals is decreased with the reduction of the power supply voltage [16]. So, the conventional voltage mode approach of circuit design such as op-amp is not suitable for low voltage analog circuit design. To achieve high performance low voltage analog circuits, novel architectures need to be developed. Current mode approach of analog circuit design is viable solution to the performance degradations suffered by voltage mode circuit (VMC) in low voltage environments. Operational Transconductance Amplifier (OTA) is an excellent active current mode device with wide band capability. Its simple, regular, modular and programmable structure suits very well with the VLSI implementation. Therefore OTA is conceived as a potential candidate for high speed integrated analog circuits design [17].

Operational transconductance amplifiers (OTAs) are the fundamental building block of analog circuits/systems and are extensively employed as active elements to implement many kinds of analog circuits such as data converters sample and hold circuits, switched-capacitor, mixers, modulators and continuous-time filters, op-amps or as buffer amplifiers for driving large capacitive loads [18,19]. The applications of OTAs are increasing rapidly and it has become one of the most stimulating areas of research. The chapter is organized as follows. The basic principle of operation of OTA is discussed in section 2.2.In section 2.3, the subthreshold region of operation is discussed. The technique of adaptive biasing is introduced in section 2.4. In section 2.5, the DC gain enhancement technique is addressed.

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2.2 BASIC PRINCIPLE OF OPERATION OF OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The operational transconductance amplifier (OTA) is one of the most important building blocks in analog and mixed-mode circuit design. It is a transconductance type device whose input signal is voltage, and its output signal is in the form of current. Therefore, the basic function of OTA is to transfer the input voltage signal into the output current. An ideal operational transconductance amplifier (OTA) is a voltage-controlled current source (VCCS) in contrast to the conventional op-amp, which is a voltage-controlled voltage source (VCVS) [20]. The term "operational" comes from the fact that it takes the input as difference of two voltages for converting it into output current. It's ideal behaviour is characterized by a high input impedance and high output impedance [21]. The OTA representation and its small signal equivalent are shown in Figure 2.1(a) and (b).

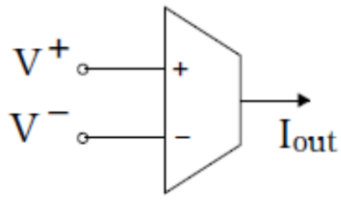

Figure 2.1(a) Ideal OTA representation [21]

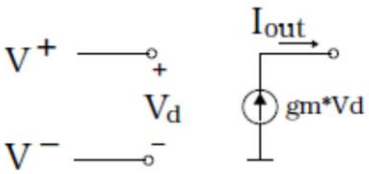

Figure 2.1(b) Small signal equivalent of OTA [21]

In an ideal OTA, the output current is a linear function of the differential input voltage i.e.(V^+ - V^-) , given by:

$$I_{out} = g_m (V^+ - V^-) \quad (2.1)$$

where V^+ is the voltage at the non-inverting input, V^- is the voltage at the inverting input and g_m is the transconductance of the amplifier.

The OTA circuit produces a current output (I_{out}) as a response to the differential input voltage (i.e. $V_d = V^+ - V^-$). The ideal transfer function of this device, i.e. proportionality factor between output current and input differential voltage is known its transconductance (g_m). Therefore OTA is best represented in terms of its transconductance gain (g_m) rather than voltage gain. The transconductance of the amplifier is usually controlled by an input current i.e amplifier bias current (I_{bias}). The amplifier's transconductance is directly proportional to this bias

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current I_{bias}. This characteristic makes it useful for electronic control of amplifier gain. The common mode input range of ideal OTA is infinite and the differential voltage between two inputs is used to control an ideal current source (i.e. the output current is independent of the output voltage) that functions as an output of the OTA [22].

2.3 SUBTHRESHOLD REGION FOR LOW POWER OPERATION

The transistor's region of operation is another important design aspect. In recent years circuits operating in the subthreshold region have earned significance because of the need for low voltage and low power battery operated circuits in human implantable biomedical instruments. With the transistors operating in strong inversion, it is often the case that more power is used than the required to meet the specifications. Optimal designs imply minimum power consumption and silicon chip area while satisfying design specifications. Therefore, the designers should investigate having transistors operating in non-conventional regions of operation. The extreme cases of weak inversion and strong inversion often do not provide a good compromise between frequency response, power consumption and silicon area. Operation of CMOS circuits such as OTAs in the subthreshold region brings in a versatile solution for the realization of low-power analog VLSI building blocks [23, 24].

The unique behaviour of the MOS transistors in subthreshold region not only allows a designer to work at low input bias current but also at low voltage. For CMOS analog circuits, the g_m/I_D efficiency achieves the maximum value when the transistors are operated in subthreshold region. Therefore the minimum power consumption can be attained due to the small quiescent current at the cost of slow speed and large silicon area. When MOS transistors operate in saturation/strong inversion, although good frequency response and small area are obtained, but non-optimum larger power is dissipated, and saturation voltage ($V_{DS\ (sat)}$) is high. Therefore operating the transistors in weak inversion region incurs a painful trade-off between high speed and low power. To compensate this trade-off the technique of adaptive biasing is employed which favours low power consumption by minimizing the standby/quiescent current and improves slew rate without affecting gain bandwidth product (GBW**)** [25]-[27].

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2.4 ADAPTIVE BIASING TECHNIQUE FOR LOW POWER ANALOG DESIGN

The proliferation of competent portable electronic equipment is pushing the semiconductor industry towards the area of low power consumption and lower supply voltage of circuits. The new sub-micron process technologies offer opportunities to operate at higher frequencies and consuming less power. But for analog circuits, this fact is not fully applicable since it is often the case that additional current is required to attain the similar performance when the power supply voltage is reduced. Power dissipation in a circuit can be reduced by reducing either supply voltage or total current in the circuit or by reducing the both. As the input current is reduced though the power dissipation is reduced, but the dynamic range is degraded as well. As the power supply voltage decreases, it also becomes increasingly difficult to keep transistors in saturation with the available voltage headroom. This is because the decrease in supply voltage does not bring a similar decrease in threshold voltage. For low-power OTAs, both the supply voltage and the quiescent/stand-by current can be decreased. Minimizing power by reducing stand-by current seems to be a better choice because the threshold voltage of MOS transistors does not scale well with the reduction of supply voltage. Adaptive biasing technique is useful technique for achieving low stand-by current. This technique aids the bias current of the input differential pair for large signals. It provides a variable bias current only in the presence of an input signal. With no input signal, a minor and controllable quiescent standby current is required. So the bias current of circuit is made signal dependent and hence the static power consumption is reduced further [28].

In order to enhance the OTA slew rate (SR) (so as to improve the amplifier's performance without affecting the gain-bandwidth GBW, biasing current must be increased but this requires a more power consumption. For this reasons, the use of the adaptive biasing technique helps to reduce stand-by power without degrading the circuit dynamic performances. Several adaptive biasing techniques have been reported in literature [29]-[32].

2.5 PATIAL POSITIVE FEEDBACK FOR DC GAIN ENHANCEMENT

The high gain of the amplifiers is one of the most important desirable characteristic of high performance analog designs. However, it is becoming more and more difficult to obtain high

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DC gain of OTA with low voltage. Cascoding of transistors is an effective method to enhance the DC gain of OTA but it is not suitable for low voltage environment because of the limit of output swing. Multistage design is another effective way to get high dc gain through more than two stages cascaded. The multi-stage design with long-channel transistors biased at a low current level which leads to the degradation of frequency performance. It is very complicated to achieve stability. Hence multistage design needs frequency compensation which causes bandwidth reduction and extra power consumption. In OTA design one of the techniques used to increase the effective transconductance is to increase the ratio "B" between current mirrors of first and second stage. The main limitation of this method is that is reduces the frequency of secondary poles by increasing the parasitic capacitance and also it increases the power dissipation of amplifier. Therefore use of local feedback to enhance the output impedance of the transistor with the loop gain is a good way to boost the OTA gain without speed penalty. The use of this technique of partial positive feedback also increases unity gain frequency (UGF) in addition to DC gain. The signal flow graph of the positive feedback system is shown in Figure 2.2, where A is the forward path amplifier gain and B is the feedback path factor. The quantity loop gain is defined as β=A.B.

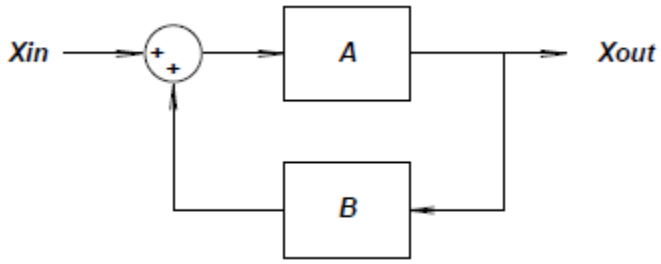

Figure 2.2 Block diagram of positive feedback system [33]

If X_{in} and X_{out} is the input and output signal respectively then the closed loop gain of the positive feedback system is given as,

$$G = \frac{X_{out}}{X_{in}} = \frac{A}{1-\beta} \tag{2.2}$$

From the equation (2.2) it can be seen that, if the value of β is set between 0<β<1, the amplifier gain is enhanced by the factor $\frac{1}{1-\beta}$ which is greater than 1. When β =1, gain factor tends to infinity, and when β=0 then gain factor tends to unity. If β is close to 1, then system becomes unstable. However if the value of β is small, the value of enhancement factor $\frac{1}{1-\beta}$

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will be close to 1 or no gain enhancement. Therefore for achieving maximum efficiency and stability, careful choice of ŋ is necessary [33].

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CHAPTER 3

LITERATURE REVIEW

3.1 INTRODUCTION

The research in analog circuit design is heading in the direction of low-power structures needed for battery operated portable electronic equipment, medical implantable applications, hearing aids, communication terminals and for advanced process technology with smaller feature size having lower breakdown and threshold voltages accompanying lower power consumption. With the continual trend towards reduced supply voltages, the high performance analog circuit design is progressively becoming challenging. Therefore the use of current-mode techniques in the design of analog circuits has become widespread with the increasing demand for low power circuits while maintaining dynamic range and high bandwidth. Current-mode design of analog circuits leads to enhancement of their bandwidth. One of the fundamental and versatile building blocks in current-mode analog signal processing is the operational transconductance amplifier (OTA), which is basically a voltage to current converter. OTAs are well known as the amplifiers in which all the nodes have low impedance except the input and output nodes. The ideal OTA is an infinite bandwidth voltage controlled current source (VCCS), with an infinite input and output impedance. Thus all the current flow through the external capacitive load. The output current does not flow into the OTA due to infinite output resistance [34, 35].

Operational transconductance amplifiers (OTA) have been viewed as potential candidates to substitute the operational amplifiers (op-amps) in high-frequency analog applications. It has been demonstrated that OTAs are capable of implementing not only all of the functions of the operational amplifier from summation and integration to high-order filtering functions, but also other functions with great simplicity, such as variable resistors and variable active inductors [36,37] etc. Several authors have reported various topologies to design OTA which are discussed in Section 3.2. [28, 29], [33], [38]-[49],

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3.2 LITERATURE SURVEY

Martin et al. [38] have proposed low voltage super class AB CMOS OTA cells with high slew rate and power efficiency. A simple technique has been utilized to achieve low-voltage, power efficient class AB OTA. The circuit is based on combination of class AB differential input stages and local common feedback which provides an additional dynamic current boosting, increased gain bandwidth (GBW) and optimal current efficiency. The principle proposed is completely general and has been extended to virtually any class AB input stage by properly including local common mode feedback. Various class AB differential input stages have been employed with local common mode feedback leading to different class AB OTA topologies.

A low voltage low power class AB OTA with negative resistance load has been presented in [39]. The architecture is based on current mirror topology with a local feedback between output nodes of the first stage. The negative resistance has been employed for compensation parasitic resistance of the first stage. In addition to this it also improves the DC gain. The class AB output stage has been implemented to obtain output rail-to-rail swing and higher slew rate.

Ferri et al [40] proposed a fully differential OTA with reduced power consumption and high DC gain. The authors have suggested the adaptive biasing technique based on current subtractor. This technique boosts the bias current of the input differential pair when large signals are applied, so increasing circuit dynamic characteristics without affecting stand-by dissipation. In order to obtain a fully differential characteristic from relatively simple circuit architecture, a classical symmetrical OTA structure has been considered by the authors. A high DC gain has been achieved by a technique useful for low voltage applications, by placing negative resistance in parallel with output resistance of the amplifier which increases the output impedance of the OTA. For the amplifier compensation it has not been applied a classical Miller compensation because the right half plane zero has not been nulled but has been designed at a frequency close to that related to the non-dominant pole, so to take the benefit of the lead effect.

Rail-to-rail fully differential OTA with reduced power consumption and high DC gain has been discussed in [41]. An embedded adaptive biasing circuit makes it possible to obtain low

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stand-by power dissipation while the high DC gain has been ensured by positive feedback. Adaptive biasing has been implemented by conventional current mirror based current subtractor. It adds current at the input stage only if a differential input is applied. To increase the DC gain, the negative conductance technique has been used. This technique is better than others, such as cascode, because it is possible to obtain a DC gain enhancement also for low-voltage applications. The designed amplifier is a two-stage OTA. The designed OTA has not been applied a classical Miller compensation because the right half plane zero has not been nullified; rather, it has been designed at a frequency close to that related to the non- dominant pole to benefit from the lead effect.

Linet al. [42] proposed a low-voltage low-power CMOS OTA with near rail-to-rail output swing .The authors have proposed a low-power CMOS OTA that is capable of producing large output swing under low supply voltage, while still achieving high gain and wide bandwidth. The suggested circuit is based on the current-mirror topology. To circumvent the low-gain problem of a CMOS OTA, several design techniques employed by the authors have been discussed. First, the output impedance has been increased by reducing the bias currents of the output branches, which has been realized by shunting partial mirror currents away. These shunt currents have been reused then to realize the second input stage. In addition, body terminals are utilized as inputs to augment the transconductance. Finally, the push-pull output stage has further enhanced the gain. The noise and settling behaviour of the circuit has also been analysed by the authors. It has been identified that the level shifter contributes considerable noise and adds a PZP to the OTA transfer function, which prolongs the circuit settling time.

A symmetrical PMOS OTA which is used to build rail-to- rail amplifier with improved DC-gain and reduced power consumption has been suggested in [29]. The authors have used the adaptive biasing circuit for two differential inputs. The technique boosts the bias current of the input differential pair for large signals. It provides a variable bias current only in the presence of an input signal. With no input signal, minor and controllable quiescent standby current flows through circuit, thereby achieving a low stand-by current and hence reducing power consumption. The adaptive biasing circuit based on the current subtractor by using the simple current mirror circuits has been used. However, current-mirror based subtractors have serious loss of signal swing and inefficient mirroring operation. Therefore, the authors have proposed the subtractor using PMOS type high-swing cascode with the fixed bias which

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offers high output voltage swing. The use of local feedback enhances the output impedance of the transistor and hence the gain.

A low-power high slew rate class-AB CMOS OTA has been presented in [43]. The authors have suggested the use of class AB operation using adaptive biasing circuit. The adaptive biasing circuit has a low and well-controlled quiescent current and temporarily increases the output current when needed. The suggested circuit senses the voltage difference of input and boosts the tail current by a positive feedback. For the static condition, all the transistors in the proposed circuit are designed to operate in the weak inversion region to minimize the static power consumption.

Cao et al. [44] have proposed a rail-to-rail OTA with improved DC gain and reduced power consumption. The circuit uses the adaptive biasing circuit and two differential inputs, thus a low standby current has been achieved together with the low power consumption. The technique of adaptive biasing has provided variable bias only in the presence of the input signal. A Common-Mode Feedback (CMFB) circuit has been employed for fully differential rail-to-rail operation. A simple CMFB circuit has been used to control the common mode voltage. The gain of the CMFB amplifier has been used to increase the CMRR (common-mode rejection ratio) of the OTA. A partial feedback loop has been employed to improve the DC-gain of the OTA circuit.

Current boosting Class-AB OTAs have been discussed in [45]. The authors have presented the techniques which are the two different topologies based on current boosting in class- AB stage achieving considerable improvement of slew rate and gain-bandwidth while maintaining the same power consumption as the conventional design. Two topologies for two stage OTAs with nonlinear current mirror based on flipped voltage follower current sensor (FVFCS) and flipped voltage follower (FVF) have been discussed by the authors. The two current boosting methods result in a reduction of total power consumption for high speed and low voltage OTAs compared to the second stage operating as class-AB. The solutions proposed by the authors utilize circuit modifications based on nonlinear current mirrors that boost the output current in the second stage.

Torfifard et al. [46] proposed a two stage power efficient class AB OTA. The circuit uses adaptive biasing circuit suited to low power dissipation and low voltage operation. The

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current source provides an additional current dynamically for the tail current to enhance the slew rate which plays the leading role in optimizing the performance and managing the power dissipation of an amplifier. The OTA shows significant improvements in driving capability and power dissipation owing to the adaptive biasing circuit.

The technique of partial positive feedback for gain enhancement in CMOS OTAs has been discussed in [33]. These schemes have been classified as Type 1 and Type2 circuits. Type 1 circuits use differential input pair with positive feedback and Type 2 circuits use active load positive feedback. The primary emphasis has been laid on micropower operation, so the authors have discussed the circuits in subthreshold region. A comparison of primary characteristics of the circuits has been discussed. The authors have suggested that the partial positive feedback is a viable technique to increase gain and bandwidth.

Degrauwe et al. [28] have proposed the adaptive biasing of CMOS amplifiers. The authors have presented two transconductance amplifiers namely differential feedback amplifier and direct feedback amplifier. The amplifier circuits regulate their own biasing current. If no signal is applied the amplifiers operate at a very low current level. Only when a signal is applied the current in the amplifiers increases so that these amplifiers have a high driving capability. The direct feedback amplifier has been designed to be used as a micropower buffer for large capacitive loads. The design has been made so that the almost whole supply current is used to charge the load capacitor.

The design of dynamic bias current source circuit for a low-power subthreshold OTA is suggested in [47]. A dynamic biasing circuit has been suggested by the authors in order to overcome the undesirable biasing current change, which produces compensation current that cancels any changes in the amplifier's transconductance. The dynamic biasing current circuit has been developed to maintain the transconductance of a differential pair constant and increase the input common mode voltage range. This has been achieved by cancelling the transconductance sensitivity to voltage changes by using a replica differential pair and a current subtractor circuit to sense and generate the main bias current and injecting the opposite polarity of the current offset into the auxiliary current source. By keeping the bias current constant, the total transconductance of the input differential pair has been maintained uniform which results in uniform amplifier gain with respect to the entire input common mode voltage range.

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A wide linear CMOS OTA has been presented in [48].The linearization technique has been achieved by squaring the transconductance of the CMOS OTA. The balanced single-output CMOS OTA has been employed as a basic building block and the realized circuit uses two OTAs and an active resistor. The balanced OTA has been formed by a source coupled pair and current mirrors. The first OTA converts a differential input signal voltage into a signal current to flow into an active resistor .The active resistor has been formed by two-MOSFET transistors. The second OTA converts the voltage drop across active resistor into the output current. The effective transconductance gain of the circuit is electronically and linearly tuned by the bias current. The OTA circuit has been used to realize a biquad filter, where its natural frequency has been made linearly tuneable by the DC bias current.

A CMOS fully differential OTA operating in sub-threshold region and its application has been proposed in [49]. The circuit allows the use of very small current for low-power and low-voltage features. The authors have employed fully differential operational transconductance based on simple architecture operated in sub-threshold region to achieve lower power consumption. It consists of two tranconductance cells and current mirrors. The transconductance value is adjustable by bias current source. The authors have also discussed the application as balance output full-wave rectifier of the fully differential operational transconductance amplifier. It consisted of only three fully differential operational transconductance amplifiers.

Table 3.1 shows the comparison of different OTAs available in literature. From the literature survey it is apparent that the most efficient way to reduce power consumption is to decrease both the supply voltage and the stand-by current. Reduced supply voltage has made the design of analog circuits even more challenging, and hence new circuits are required. In this context, the technique of dynamic biasing is viable alternative for achieving the lower static power dissipation by decreasing standby current, instead of reducing supply voltages which leads to degradation of circuit's dynamic performance. This technique leads to the improvement of slew rate without increasing standby current and power dissipation. The use of partial positive feedback for DC gain improvement is an efficient technique to increase gain and bandwidth.

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Table 3.1 Comparison of different OTAs available in literature [29] ,[38]-[46]

	[38]	**[39]**	**[40]**	**[41]**	**[42]**	**[43]**	**[29]**	**[44]**	**[45]**	**[46]**
Year	2005	2006	2007	2007	2007	2009	2009	2010	2012	2013
CMOS Process	0.5 µm	0.18 µm	0.35 µm	0.35 µm	0.18 µm	90 nm	0.18 µm	90 nm	0.18 µm	0.18 µm
Supply VoltageV	2V	1V	1.5	1.5	0.8V	+/- 0.6	1.8V	+/- 0.6	1.5V	+/-0.6 V
Capacitive Load	80pF	5pF	15pF	15pF	2pF	10pF	10pF	10pF	-	1pF
DC Gain (dB)	37.5	58.25	75	78	62	79.2	48.97	80.2	70.15	44
Phase Margin	90°	61°	89°	-	67°	83.5°	78.18°	84.9°	63°	68°
GBW	470 KHz	79.53 MHz	4.6 MHz	8.9 MHz	160 MHz	7.6 MHz	57.27 KHz	9.5 MHz	136 MHz	590 KHz
CMRR (dB)	69	-	132	126	-	129	124.37	124	100	110
PSRR +/- (dB)	57/46	-	147/150		-	116/111	81.4/50.3	135/140		73/48
SR +/- (V/µs)	42/80	2.3	40	37	-	32	4.92/5.04	37	236	71
Input Offset	-	-	-	200 µV	-	11.2 µV	-	599.96 mV	-	0.7 mV
Input mode common range	-	-	-	-	-		0.4V – 1.8V	-	-	-
Settling Time	100/33ns	-	310ns	390ns		262µs	1.0/2.1 µs	247µs	19ns	160ns
Static Power Dissipation	140 µW	67 µW	-	169 µW	250 µW	57.6 µW	1.96µW	96µW	1.5mV	0.4µW
Unity Gain Frequency	-	-	-	-	-	64.8 MHz	-	71.8 MHz	-	-

From the Table 3.1 it can be observed that high DC gain of 80.2 dB has been achieved in [44] while the phase margin of 90° has been obtained in [38]. The GBW is maximum in [42] having the value of 160 MHz. In [40] a high CMRR of 132dB has been obtained. The PSRR value of 147/150 dB is observed in [40]. In [45] the high value of slew rate of 236v/µs is achieved but at the cost of high static power dissipation of 1.5mW. Power dissipation value of 0.4µW is obtained in [46]. In [45] a least setting time value of 19ns has been achieved.

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CHAPTER 4

PROPOSED POWER EFFICIENT HIGH DC GAIN ADAPTIVE BIASED CMOS OTA

4.1 INTRODUCTION

This chapter proposes a power efficient high DC gain adaptive biased CMOS operational transconductance amplifier (OTA). The chapter is organized as follows. Section 4.2 proposes the current mode analog computational circuits. In section 4.3, working principle of proposed adaptive biased CMOS OTA is presented. Section 4.4 discusses the analysis of proposed adaptive biased CMOS OTA in subthreshold region. Section 4.5 presents the technique of partial positive feedback for DC gain enhancement. Section 4.6 proposes the complete design of power efficient high DC gain adaptive biased CMOS OTA.

4.2 CURRENT MODE ANALOG COMPUTATIONAL CIRCUITS

In this section, two current mode analog computational circuits such as current adder and subtractor based on cascode current mirror (CCM) are proposed. The idea of CCM has been employed to overcome the drawback of channel length modulation effect in conventional current mirrors.

4.2.1 PROPOSED CURRENT ADDER BASED ON CCM

The proposed current adder based on CCM is shown in Figure 4.1. All the transistors are biased in saturation region and the transistors M1-M2, M3-M4, M5-M6, and M7-M8 are perfectly matched. The cascode current mirrors are formed using transistors M1-M4 and M5-M8 whose function is to precisely copy the input currents AI_{in1} and AI_{in2}, in transistors M4 and M8, respectively.

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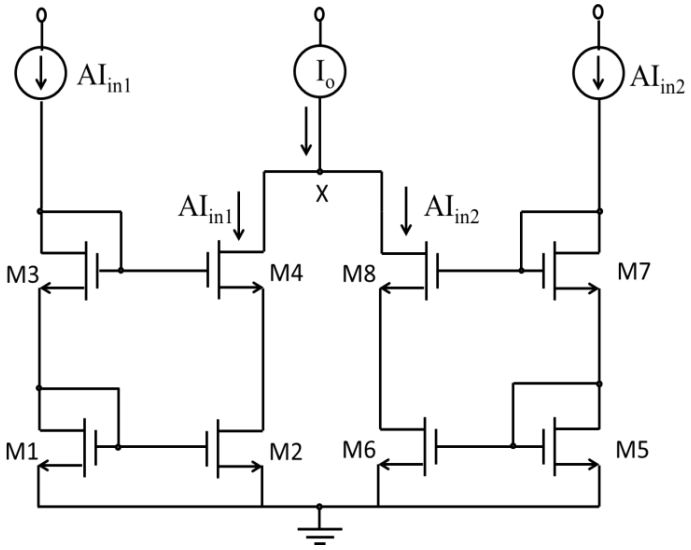

Figure 4.1: Proposed current adder based on CCM

To achieve proper biasing voltage of cascode structure, the aspect ratios of transistors are chosen as [50],

$$\frac{(W/L)_4}{(W/L)_3} = \frac{(W/L)_2}{(W/L)_1}, \qquad \frac{(W/L)_7}{(W/L)_8} = \frac{(W/L)_5}{(W/L)_6} \tag{4.1}$$

Applying KCL at node X, the output current I_o is given as

$$I_o = A\, I_{in1} + AI_{in2} = A\,(I_{in1} + I_{in2}) \tag{4.2}$$

From equation (4.2), it can be seen that the output current is the addition of two input currents AI_{in1} and AI_{in2}, where A is the gain factor.

4.2.2 PROPOSED CURRENT SUBTRACTOR BASED ON CCM

Using the same topology of CCM, the current subtractor is also proposed which is shown in Figure 4.2. The cascode current mirrors are formed by using NMOS transistors. All the transistors are biased in saturation mode and the transistor pairs M1-M2, M3-M4, M5-6, and M7-M8 are perfectly matched. The transistors M1-M4 and M5-M8 are used to form cascode current mirror in which transistor pairs M1, M3 and M6, M8 are configured as diode connected to operate them in saturation region.

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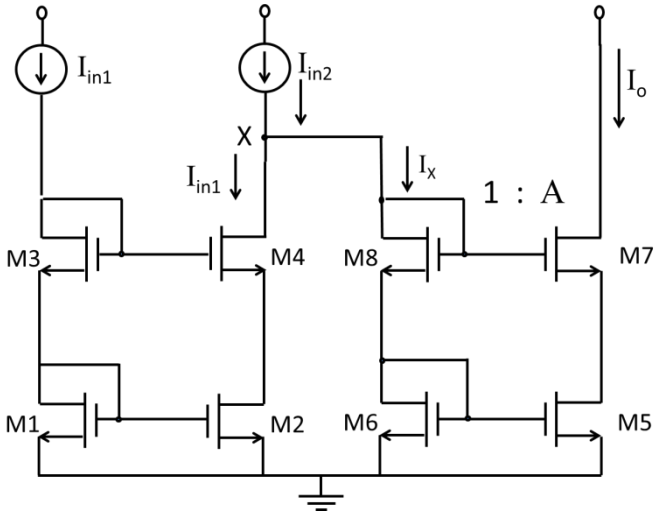

Figure 4.2: Proposed current subtractor based on CCM

For the proper biasing voltage of cascode structure the aspect ratio of transistors are chosen as [50],

$$\frac{(W/L)_4}{(W/L)_3} = \frac{(W/L)_2}{(W/L)_1}, \qquad \frac{(W/L)_7}{(W/L)_8} = \frac{(W/L)_5}{(W/L)_6} \tag{4.3}$$

From Figure 4.2, it can be seen that current I_{in1} through transistors M1, M3 is copied accurately in transistors M2, M4 (i.e. I (M4, M2) = I_{in1}).

By applying KCL at node X, the current I_X is given as

$$I_X = I_{in2} - I_{in1} \tag{4.4}$$

Therefore, the output current I_o is given as

$$I_o = AI_X = A\,(I_{in2} - I_{in1}) \tag{4.5}$$

From equation (4.5), it can be seen that the output current is the subtraction of two input currents AI_1 and AI_2, where A is the gain factor. The proposed current subtractor circuit find wide application in adaptive biasing of amplifiers.

4.3 PROPOSED ADAPTIVE BIASED OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The proposed adaptive biased operational transconductance amplifier is shown in Figure 4.3. The circuit consists of a classical differential input and double-to-single ended output stage. In the proposed circuit two additional tail current sources have been added in the simple OTA topology to implement the adaptive biasing technique. These additional current sources are realized by the current subtractor discussed in Section 4.2.2. By using transistors M5-M12 the

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differential current source "$A(I_2 - I_1)$" has been realised. Similarly the differential current source "$A(I_1 - I_2)$" is realised by transistors M13-M20.The currents at the inputs of the subtractors have been provided by means of current mirrors present in differential pair of OTA circuit. The proposed OTA functions as a differential feedback amplifier. If there is no disturbance on the virtual ground then the drain currents I_1 and I_2 are equal then the total bias current is I_B. When a voltage is applied across the inputs of the OTA, the currents I_1 and I_2 become different. The total tail current is thus either $I_B + A(I_1 - I_2)$or $I_B + A(I_2 - I_1)$ depending on the signal of the disturbance of the virtual ground .Therefore, one of the additional current sources will draw a current while the other source tries to draw a negative current which is not feasible and thus keeps drawing zero current. The total bias current is given by equation (4.6). In addition to this, because of feedback the bias currents will further increase.

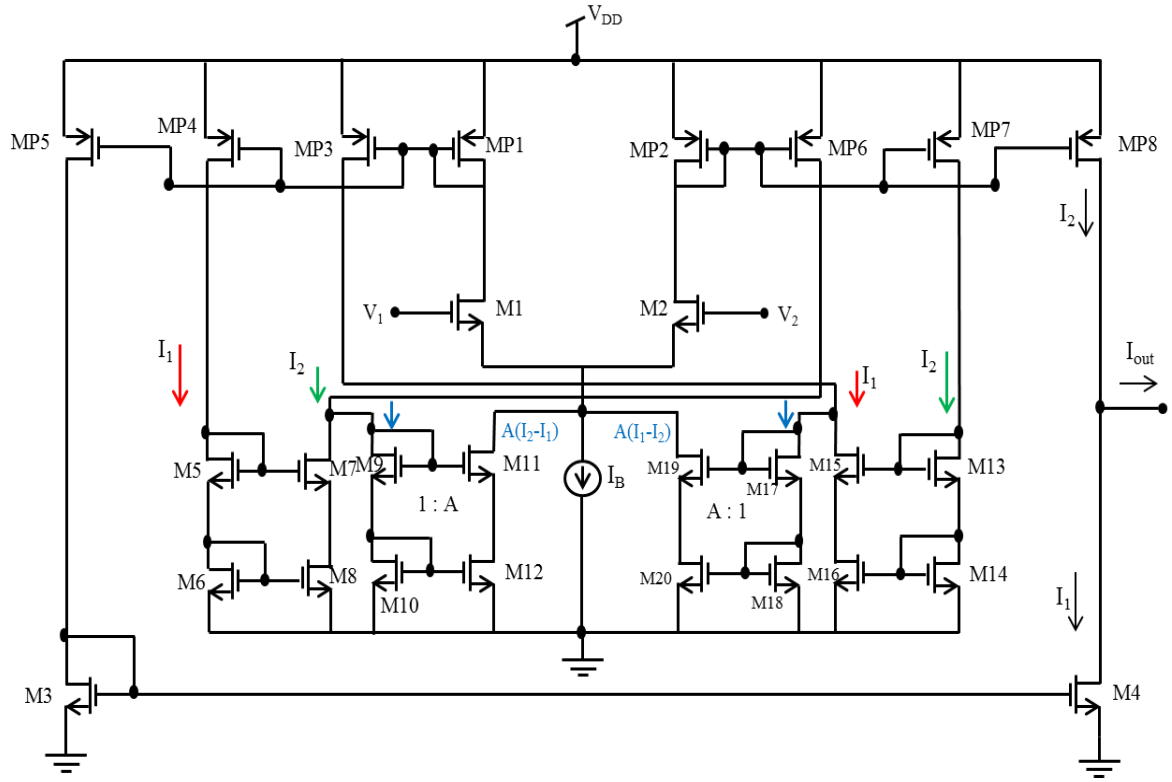

Figure 4.3 Proposed adaptive biased operational transconductance amplifier

$$I_B + A|I_2 - I_1|. \tag{4.6}$$

The maximum total current available through M1 occurs when M2 is off. Positive feedback exists through the loop M1, MP1, MP4, and M11. Initially, when M2 turns off, the current in M1, MP1 is I_B. This current is mirrored in MP4, M5 and the current through M11 is thus AI_B. At a particular instant of time, the tail current, which flows through M1, is now $I_B + AI_B$.The

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transistors M1, MP1, M11 have been ensured to remain saturation, thus this current flows around the positive feedback loop and increases by a factor of "A". This continues, resulting in a final or total tail current given by,

$$I_{TOTAL} = I_B(1 + A + A^2 + A^3..) \quad (4.7)$$

If $A < 1$, then by using infinite geometric series progression, equation (4.7) can be written as

$$I_{TOTAL} = \frac{I_B}{1-A} \quad (4.8)$$

From equation (4.8), it can be seen that that in the presence of adaptive biasing, the total bias current is increased without increasing the standby current and power dissipation. Also the slew rate limitation due to fixed bias current source has been eliminated by the use of adaptive biasing technique. It provides variable bias in the presence of input signal.

4.4 ANALYSIS OF PROPOSED ADAPTIVE BIASED OTA IN SUBTHRESHOLD REGION

The transistors M1 and M2 of the proposed OTA circuit shown in Figure 4.3 are operated in the subthreshold region. The transistors MP1 and MP2 are the active current mirror loads, and the transistors MP3- MP6, form the current mirror in dual input-single ended output OTA. The drain current equation of transistor operating in subthreshold region is given as

$$I_D = \mu_n C_{ox}(\eta - 1)V_T{}^2 e^{-\frac{V_{TH}}{\eta V_T}} \frac{W}{L} e^{\frac{V_{GS}}{\eta V_T}} \quad (4.9)$$

where μ_n is the charge-carrier effective mobility, C_{ox} is the gate-oxide capacitance per unit area, W/L is aspect ratio, V_{GS} is the gate-source voltage, V_{TH} is threshold voltage of the transistor.

$$I_{DO} = \mu_n C_{ox}(\eta - 1)V_T{}^2 e^{-\frac{V_{TH}}{\eta V_T}}$$

$$V_T = \frac{KT}{q} = 26mV$$

η is the process parameter whose value lies between $1 < \eta < 2$

Let I_1 and I_2 be the drain currents through transistors M1 and M2 of the proposed OTA circuit. Using equation (4.9), the two basic equations (4.10) and (4.11) that define the operation of differential pair in subthreshold region are given as

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$$\frac{I_2}{I_1} = \frac{I_{Do}\, e^{\frac{V_2}{\eta V_T}}}{I_{Do} e^{\frac{V_1}{\eta V_T}}} = e^{\frac{V_2 - V_1}{\eta V_T}} \tag{4.10}$$

$$I_B = I_1 + I_2 \tag{4.11}$$

The differential output current I_{out} of the OTA is given as

$$I_{out} = B(I_2 - I_1) \tag{4.12}$$

where B is the ratio of aspect ratios of transistors MP4 to MP2 and M4 to M3.

$$B = \frac{W/L_{MP8}}{W/L_{MP2}} = \frac{W/L_{M4}}{W/L_{M3}}$$

Multiplying and dividing the equation (4.12) by $(I_1 + I_2)$, the equation is modified as

$$I_{out} = B\frac{I_2 - I_1}{(I_2 + I_1)}(I_1 + I_2) \tag{4.13}$$

The equation (4.13) is further modified by dividing numerator and denominator by I_2 as

$$I_{out} = I_B \frac{(\frac{I_2}{I_1} - 1)}{(\frac{I_2}{I_1} + 1)} \tag{4.14}$$

Using the trigonometric formula: $\tanh(x) = \frac{(e^{2x}-1)}{(e^{2x}+1)}$ in equation (4.14), the output current is given as

$$I_{out} = I_B \tanh(\frac{V_2 - V_1}{2\eta V_T}) \tag{4.15}$$

The differential voltage V_{in} is defined as,

$$V_{in} = V_1 - V_2 \tag{4.16}$$

Using equation (4.15) and (4.16), the output current is given as

$$I_{out} = I_B \tanh(\frac{-V_{in}}{2\eta V_T}) \tag{4.17}$$

The effective transcondctance of the OTA circuit is given by the partial derivative of output current I_{out} with respect to V_{in} evaluated at $V_{in=0}$.

$$g_m = \frac{\partial I_{out}}{\partial V_{in}}\Big|_{V_{in=0}} = \frac{I_B}{2\eta V_T} \tag{4.18}$$

When the adaptive biased feedback factor "A" is finite then the total tail/ bias is given by

$$I_1 + I_2 = I_B + A(I_1 - I_2) \tag{4.19}$$

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where $I_1$and I_2 are the drain current of transistor M1 and M2 respectively which are given as,

$$I_1 = I_{DO} \ e^{\frac{V_1}{\eta V_T}} \tag{4.20}$$

$$I_2 = I_{DO} \ e^{\frac{V_2}{\eta V_T}} \tag{4.21}$$

where V_1 and V_2 are the input voltages of transistors M1 and M2

Using the equation (4.16) the current equation (4.20) is modified as

$$I_1 = I_{DO} \ e^{\frac{V_2+V_{in}}{\eta V_T}} \tag{4.22}$$

By using equation (4.21), current I_1 is given as

$$I_1 = I_2 \ e^{\frac{V_{in}}{\eta V_T}} \tag{4.23}$$

Using the equation (4.23) in equation (4.19) the current is given as

$$I_B = I_2(1+A) + I_2 \ e^{\frac{V_{in}}{\eta V_T}}(1-A) \tag{4.24}$$

The current I_2 is given as

$$I_2 = \frac{I_B}{(1+A) + \ e^{\frac{V_{in}}{\eta V_T}}(1-A)} \tag{4.25}$$

Using equation (4.23), the current I_1 is calculated as

$$I_1 = I_2 \ e^{\frac{V_{in}}{\eta V_T}} = \frac{I_B \ e^{\frac{V_{in}}{\eta V_T}}}{(1+A) + \ e^{\frac{V_{in}}{\eta V_T}}(1-A)} \tag{4.26}$$

Using equation (4.25) and (4.26) the output current I_{out} is given by

$$I_{out} = \frac{BI_B(\ e^{\frac{V_{in}}{\eta V_T}}-1)}{(1+A) + \ e^{\frac{V_{in}}{\eta V_T}}(1-A)} \tag{4.27}$$

4.5 GAIN ENHANCEMENT TECHNIQUE IN PROPOSED OTA

In order to develop high performance analog circuits it is necessary to design large value of transconductance (gain) for the OTAs. Cascoding transistors can raise the circuit impedance and thereby boost the gain. However, this is at the cost of reduced output swing, and such circuit becomes infeasible if the supply voltage is further decreased. The high gain requirement leads to a multistage design with long-channel transistors biased at low current level. This leads to the degradation of frequency performance. Another technique to increase effective transconductance is to increase the ratio “B” of current mirrors between the two

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stages of OTA. But the limitation of this technique is that it reduces the frequency of secondary poles by increasing the parasitic capacitance. In addition to this it also increases the static power dissipation of the amplifier. Therefore the technique of partial positive feedback which increases the output impedance of the OTA input stage through positive feedback is an efficient technique for improved gain and bandwidth of CMOS OTAs. The use of partial positive feedback not only increases the DC gain but also increases the unity gain frequency (UGF). The increased DC gain and bandwidth is a direct result of an increase in the effective transconductance of the input gain stage.

The expression of output current and effective transconductance when differential pair of the proposed OTA is operated in subthreshold mode is given by equation (4.17) and (4.18). Based on these equations there are two methods that can be used to enhance the effective transconductance. One method attempts to enlarge the coefficient inside the hyperbolic tangent function, while the other attempts to enlarge the coefficient outside the hyperbolic tangent function. Circuits that use the first method to enhance transconductance are classified as type I or Input pair enhancement circuits and circuits that use the second method to enhance transconductance are classified as Type II or Active load enhancement circuits.
In this work the gain enhancement by using Type II circuits have been presented.

4.5.1 ANALYSIS OF DC GAIN ENHANCED OTA

The proposed DC gain enhanced OTA is shown in Figure 4.4. The differential pair is composed of transistors M1-M2. The output differential current is enhanced by positive feedback loop consisting of transistors MP5 and MP6 connected to output load transistors MP1 and MP2 as shown in Figure 4.4.

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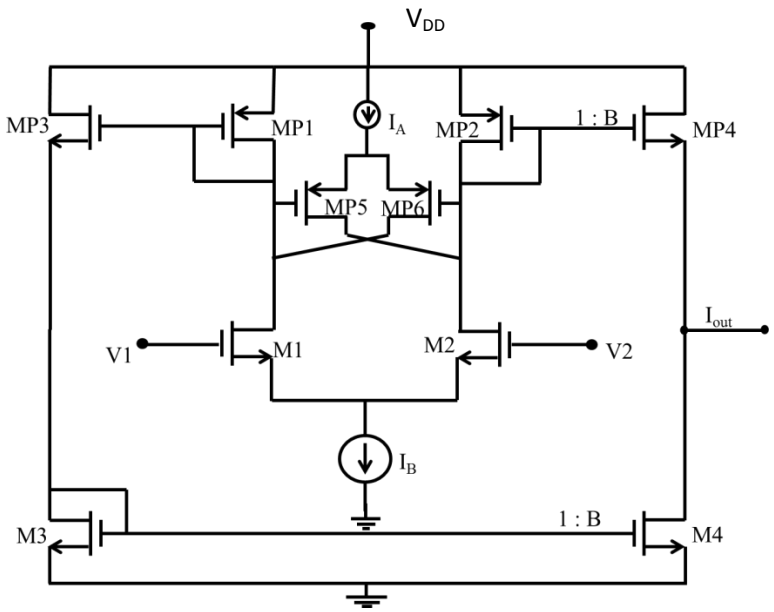

Figure 4.4 Proposed DC gain enhanced OTA using partial positive feedback technique

The output current I_{out} is given as

$$I_{out} = I_{MP2} - I_{MP1} \tag{4.28}$$

The output current I_{out} can be also expressed in terms of current differences as

$$I_1 = I_{MP1} + I_{MP6} \text{ or } I_{MP1} = I_1 - I_{MP6} \tag{4.29}$$

$$I_2 = I_{MP2} + I_{MP5} \text{ or } I_{MP2} = I_2 - I_{MP5} \tag{4.30}$$

Using equations (4.29) and (4.30), the output current is given as

$$I_{out} = (I_2 - I_1) - (I_{MP5} - I_{MP6}) \tag{4.31}$$

Since the gate terminal of transistor MP5 and MP6 is connected to drain terminal of transistors M1 and M2 respectively, the current difference$(I_{MP5} - I_{MP6})$ and voltage difference$(V_{D1} - V_{D2})$ can be related as

$$\left(I_{MP5} - I_{MP6)}\right) = g_{MP5.6}(V_{D1} - V_{D2}) \tag{4.32}$$

where $I_{MP5} = V_{D1} g_{MP5}$ and $I_{MP6} = V_{D2} g_{MP6}$

$(V_{D1} - V_{D2})$ can be further expressed in terms of currents given as

$$(V_{D1} - V_{D2}) = \frac{I_{MP1}}{g_{MP1}} - \frac{I_{MP2}}{g_{MP2}} \tag{4.33}$$

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Assuming the transistors to be perfectly matched, thus $g_{MP1}$and g_{MP2} are equal, thus the current difference $I_{MP2} - I_{MP1}$ is related to $(V_{D1} - V_{D2})$ as

$$(V_{D1} - V_{D2}) = \frac{I_{MP1-} I_{MP2}}{g_{MP1,2}} = \frac{-(I_{MP2-} I_{MP1})}{g_{MP1,2}} \tag{4.34}$$

Using equation (4.32) in equation (4.31), the output current is rewritten as,

$$I_{out} = (I_2 - I_1) - g_{MP5.6}(V_{D1} - V_{D2}) \tag{4.35}$$

By substituting the value of $(V_{D1} - V_{D2})$ from equation (4.34) in (4.35), the output current I_{out} is modified as,

$$I_{out} = (I_2 - I_1) + g_{MP5.6} \frac{(I_{MP2-} I_{MP1})}{g_{MP1,2}} \tag{4.36}$$

Putting the value of $I_{MP2-} I_{MP1}$ in equation (4.36), it is modified as

$$I_{out} = (I_2 - I_1) + g_{MP5.6} \frac{I_{out}}{g_{MP1,2}} \tag{4.37}$$

After simplification the output current is given as

$$I_{out} = \frac{(I_2 - I_1)}{(1 - \frac{g_{MP5.6}}{g_{MP1,2}})} \tag{4.38}$$

Since the difference current $(I_2 - I_1)$ can be expressed in terms of differential input voltage V_{in} , therefore the output current is expressed as

$$I_{out} = \frac{1}{\left(1 - \frac{g_{MP5.6}}{g_{MP1,2}}\right)} I_B \tanh\left(\frac{-V_{in}}{2\eta V_T}\right) \tag{4.39}$$

From equation (4.39), the output current I_{out} is a function of loop gain β which is defined as transconductance ratio as

$$\beta = \frac{g_{MP5.6}}{g_{MP1,2}} \tag{4.40}$$

The expression of output current is reduces to

$$I_{out} = \frac{1}{1-\beta} I_B \tanh(\frac{V_{in}}{2\eta V_T}) \tag{4.41}$$

From the equation (4.41) it is implied that if $V_{in} \gg 2\eta V_T$, then I_{out} tends to $\frac{I_B}{1-\beta}$. If β <1 , then I_{out} becomes greater than I_B . However, this is not possible, because the supply current

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is limited to I_B . The saturation current cannot exceed I_B . For a given tail currentI_B , when V_{in} exceeds the saturation voltage, defined as V_{SAT} in equation (4.42), the output current is limited to I_B .

$$V_{SAT} = 2\eta V_T tanh^{-1}(1-\beta) \tag{4.42}$$

Therefore when $|V_{in}| < V_{SAT}$, the I_{out} is described by equation (4.41) and when $|V_{in}| > V_{SAT}$, I_{out} takes the value of saturation current I_B . From this result we also observe that when 0 < β< 1, the coefficient outside the hyperbolic tangent is enhanced by the gain factor $\frac{1}{1-\beta}$ which is greater than 1.

We can define the new effective transconductance of OTAs with partial feedback when $|V_{in}| < V_{SAT}$ as,

$$g_{m,new} = \frac{1}{1-\frac{g_{MP5,6}}{g_{MP1,2}}} B I_B \frac{\partial \tanh(\frac{V_{in}}{2\eta V_T})}{\partial V_{in}} |_{Vin=0} \tag{4.43}$$

$$g_{m,new} = \frac{g_m}{1-\beta} \tag{4.44}$$

From equation (4.44), the effective transconductance is enhanced by a factor of $\frac{1}{1-\beta}$. This gain factor can be determined by the size of transistors.

$$\beta = (\frac{I_B}{I_A - I_B})^{\frac{1}{2}} (\frac{W_{MP5}/L_{MP5}}{W_{MP1}/L_{MP1}})^{\frac{1}{2}} \tag{4.45}$$

Thus the loop gain factor is a function of bias currents I_A and I_B and the device sizes.

4.6 COMPLETE DESIGN OF POWER EFFICIENT HIGH DC GAIN ADAPTIVE BIASED CMOS OTA

In the proposed circuit, symmetrical OTA with dual input and single ended output has been considered as shown in Figure 4.5. The differential pair consisting of transistors M1 and M2 samples the differential input voltage and converts it into current signal. The transistors MP1 and MP2 act as active load transistors for the differential current signal I_1 and I_2. Also the transistors MP3-MP8 and M3, M4 form the current mirror for differential to single ended converter. The bias current of the OTA is made signal dependent using the technique of adaptive biasing. The tail current source (I_B) is the fixed/quiescent current bias source and the

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additional tail current sources are realised by current subtractors based on cascode current mirror topology. These additional bias current sources consists of transistors M5-M12 and M13-M20 which provides the current $A|\Delta I|$ where $|\Delta I|$ is the absolute value of the difference between the current of I_1 and I_2 and "A" is the current feedback factor. The additional tail current is dependent upon the polarity of the input signal and disturbance at virtual ground. When there is no disturbance on the virtual ground, the currents I_1 and $I_2$are

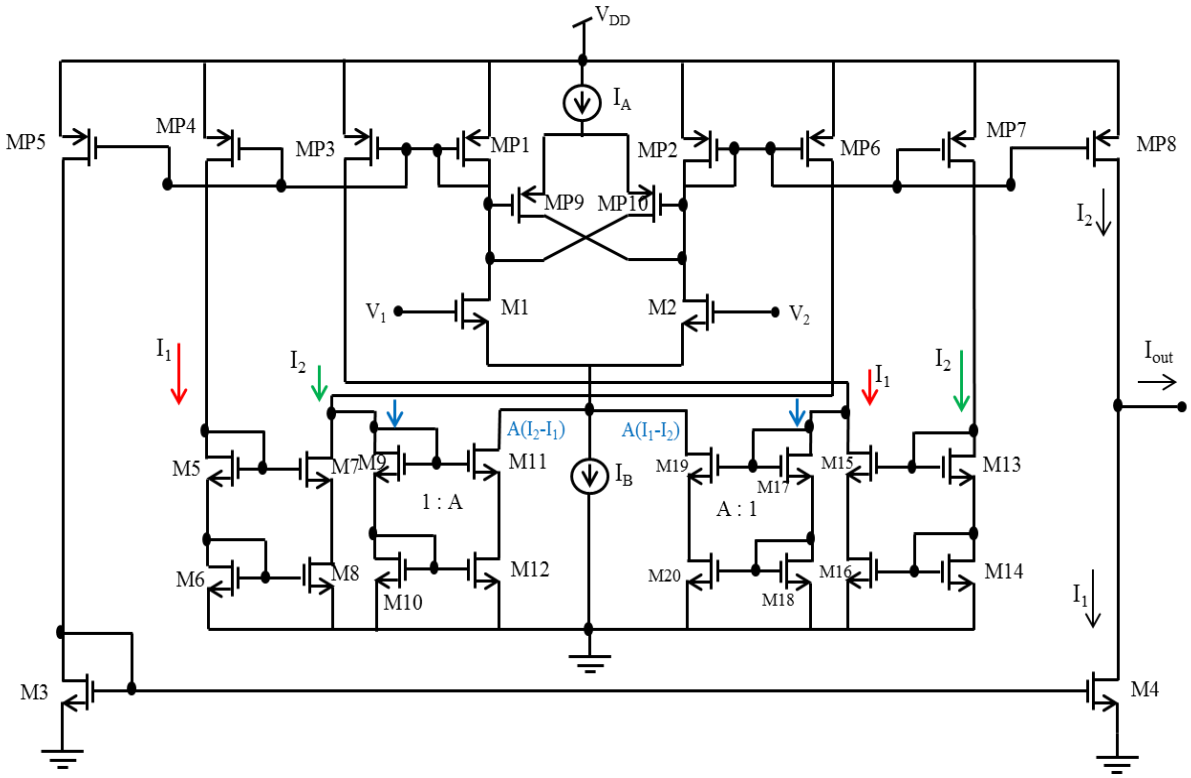

Figure 4.5 Complete circuit of power efficient high DC gain adaptive biased CMOS OTA

equal; the total bias current is equal to the quiescent current I_B. If there is signal on the virtual ground, the current I_1 and I_2becomes different and one of the additional current source will draw current, while the other current source tries to draw negative current which is not feasible and hence draws no current. So at steady state only one of the current sources is turned on. In addition positive feedback occurs through the loop M1, MP1, MP4, M11 and similarly in M2, MP7, M13, and M19. The transistors remain in saturation, the bias current circles around the positive feedback loop and increase by the factor of A. This phenomenon of feedback leads to the total tail current of $\frac{I_B}{1-A}$ Thus the slew-rate limitation which is a consequence of a fixed tail current source is eliminated by adding an extra tail current source, the current of which increases with the disturbance of the virtual ground. Hence a much higher slew-rate can be obtained.

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The high performance analog circuits demands for the high gain (transconductance).In the proposed design OTA gain has been enhanced by the partial positive feedback. The feedback transistors MP9 and MP10 are connected to the active loads MP1, MP2 in the differential stage. The transfer function between input and output is enhanced by the factor of $\frac{1}{1-\beta}$ which is greater than 1 if the value of lies between 0<β<1.

From equation (4.38) and (4.40) the value of output current and β are given by,

$$I_{out} = \frac{(I_2 - I_1)}{(1-\frac{g_{MP9,10}}{g_{MP1,2}})} \tag{4.46}$$

$$\beta = \frac{g_{MP9,10}}{g_{MP1,2}} \tag{4.47}$$

4.6.1 MISMATCH ANALYSIS

The output current of the OTA operating in weak inversion is given by equation (4.16) as

$$I_{out} = B(I_2 - I_1) = \frac{BI_B(\ e^{\frac{V_{in}}{\eta V_T}} - 1)}{(1+A) + \ e^{\frac{V_{in}}{\eta V_T}}(1-A)}$$

Where $I_B$the quiescent is bias current and V_{in} is the differential input voltage. Suppose all possible mismatches are taken into account in the current source and assume that the matching factor is defined as

$$m = 1 - \alpha_{mismatch} \tag{4.48}$$

Here m is the match factor and $\alpha_{mismatch}$ is the mismatch factor. The current I_1 and I_2 are delivered by the differential pair through transistors of the current mirror present in OTA.

$$I_{s1} = A(I_1 - \ m_2 I_2) \tag{4.49}$$

$$I_{s2} = A(I_2 - \ m_1 I_1) \tag{4.50}$$

Therefore the output current is defined as

$$I_{out} = B(I_2 - mI_1) \tag{4.51}$$

$$I_{out} = \frac{BI_B\left(\ (e^{\frac{V_{in}}{\eta V_T}} - 1) - m\right)}{(1+mA) + \ e^{\frac{V_{in}}{\eta V_T}}(1-A)} \tag{4.52}$$

Thus the minimum voltage required for the amplifier to operate in adaptive biased mode is as follows

$$V_{min} = \ \eta V_T \ln(m) \tag{4.53}$$

The equation (4.60) highlights the condition when the OTA does not slew and output current tends to go to infinity.

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$$V_{escape} = \eta V_T \ln\left(\frac{Am+1}{A-1}\right) \quad (4.54)$$

$$V_{escape} = \eta V_T \ln\left(\frac{A+1}{A-1} - \frac{A\alpha_{mismatch}}{A-1}\right) \quad (4.55)$$

In addition, when a differential signal (small or large) is applied, only one of the current sources is guaranteed to be functional, providing additional current. This leads to extremely reduced mismatched effects. Therefore steady output current of the amplifier is derived as,

$$I_{out} = B\frac{I_B}{1-A\alpha_{mismatch}} \quad (4.56)$$

Equation (4.56) clearly indicates that the steady state conditions only one of the current sources should be inclined to the maximum value.

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CHAPTER 5

SIMULATION RESULTS AND LAYOUT DESIGNS

5.1 INTRODUCTION

The proposed current mode analog computational circuits and power-efficient high DC gain adaptive biased CMOS OTA have been simulated using UMC 0.18µm CMOS technology process parameters. The chapter is organized as follows. Section 5.2 presents the simulation results of proposed current mode computational circuits. In section 5.3 the simulation results of the proposed adaptive biased CMOS OTA have been discussed. In section 5.4 the simulation results of proposed OTA with partial positive feedback have been presented. Section 5.5 discusses the simulation results of proposed power efficient high DC gain adaptive biased CMOS OTA. The layout designs of the proposed circuits, designed in Cadence Virtuoso layout editor using UMC 0.18µm CMOS process technology are addressed in section 5.6.

5.2 SIMULATION RESULTS OF PROPOSED CURRENT MODE ANALOG COMPUTATIONAL CIRCUITS

In this section the simulation results of analog computational circuits such as current adder and subtractor based on cascode current mirror (CCM) topology have been discussed.

5.2.1 SIMULATION RESULTS OF THE PROPOSED CURRENT ADDER CIRCUIT

The proposed current adder circuit based on CCM shown in Figure 4.1 has been simulated using UMC 0.18 µm CMOS process technology parameters. The dimension of the transistors of the proposed current adder circuit is listed in Table 5.1.

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Table 5.1 Transistor sizing of proposed current adder circuit

MOSFET	W(µm)	L(µm)
M1,M2,M3,M4	0.27	0.18
M5,M6,M7,M8	0.27	0.18

The DC characteristics of the proposed current adder is shown in Figure 5.1, in which output current varies from 10 µA to 90 µA with respect to input current variation from 0 µA to 80µA while one of the current sources fixed at 10 µA. From the plot it is observed that the proposed current adder shows high linearity over appreciable range of input current.

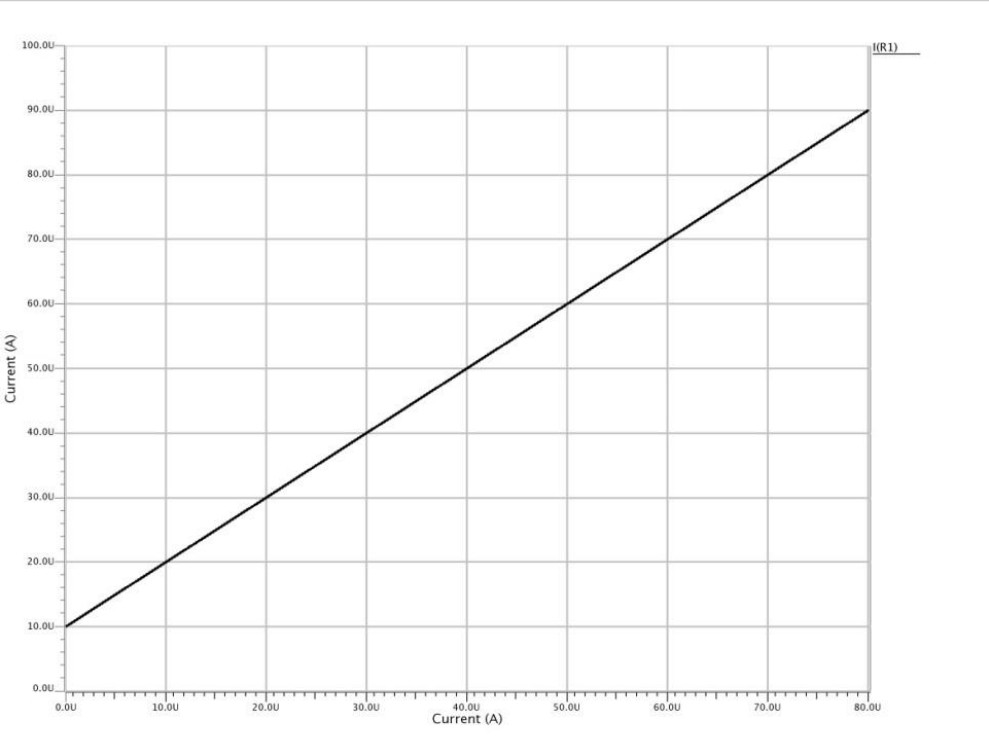

Figure 5.1: DC characteristics of proposed current adder circuit

Table 5.2 compares the theoretical and simulated values of output current. From the table, it can be seen that the percentage error between theoretical and simulated output current is less than or equal to 0.025%.

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Table 5.2: Comparison between theoretical and simulated values of output current of proposed current adder circuit

Input Current I_{in1}(µA)	*Input Current* I_{in2}(µA)	*Output Current* I_o(µA) *(Theoretical Values)*	*Output Current* I_o(µA) *(Simulated Values)*	*Percentage Error (%)*
0	10	10	10.002	0.020
10	10	20	20.005	0.025
20	10	30	30.005	0.016
30	10	40	40.004	0.010
40	10	50	50.001	0.002
50	10	60	59.998	0.003
60	10	70	69.994	0.008
70	10	80	79.988	0.015

5.2.2 SIMULATION RESULTS OF THE PROPOSED CURRENT SUBTRACTOR CIRCUIT

The proposed current subtractor circuit based on CCM shown in Figure 4.2 has been simulated using UMC 0.18 µm CMOS process technology parameters. The dimension of the transistors of the proposed current subtractor circuit is listed in Table 5.3.

Table 5.3 Transistor sizing of proposed current subtractor

MOSFET	W(µm)	L(µm)
M1,M2,M3,M4	0.27	0.18
M5,M6,M7,M8	0.27	0.18

The DC characteristics of the proposed current subtractor are shown in Figure 5.2, in which the output current varies from 80 µA to 0 µA w.r.t input current variation from 0 µA to 80 µA while one of current sources is fixed at 80 µA.

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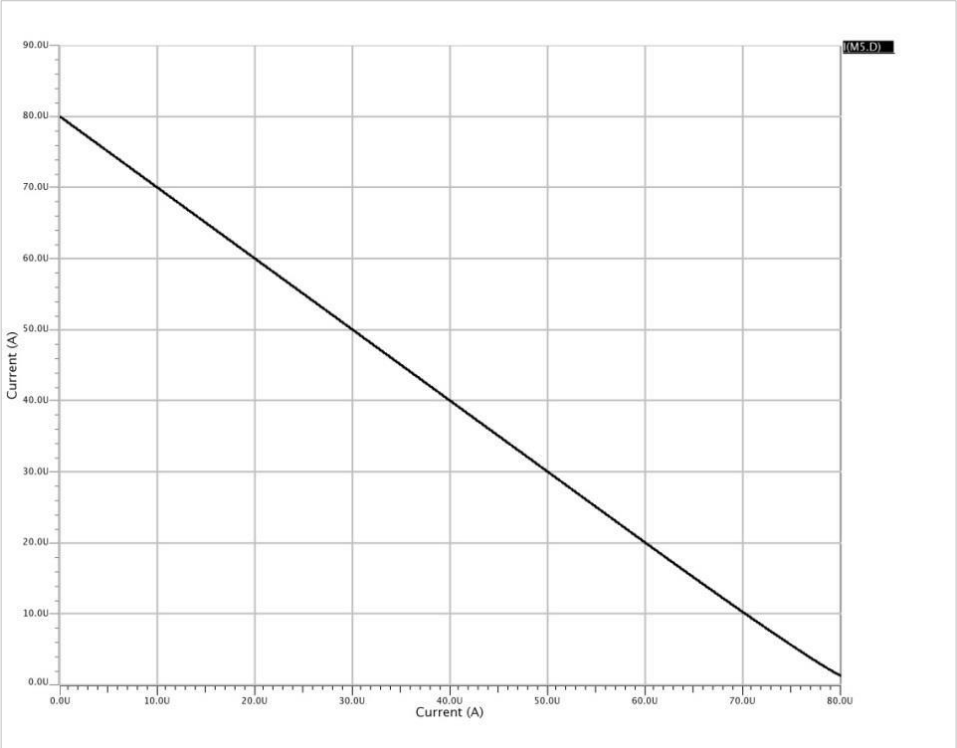

Figure 5.2: DC characteristics of proposed current subtractor circuit

Table 5.4 compares the theoretical and simulated values of output current. From the table, it can be seen that the percentage error between theoretical and simulated output current is less than or equal to 2.50%

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Table 5.4: Comparison between theoretical and simulated values of output current in proposed current subtractor circuit

Input Current I_{in1}(µA)	*Input Current* I_{in2}(µA)	*Output Current* I_o(µA) *(Theoretical Values)*	*Output Current* I_o(µA) *(Simulated Values)*	*Percentage Error (%)*
0	80	80	80.000	0.000
10	80	70	69.994	0.008
20	80	60	59.994	0.010
30	80	50	49.996	0.008
40	80	40	40.000	0.000
50	80	30	30.006	0.020
60	80	20	20.030	0.150
70	80	10	10.250	2.500

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5.3 SIMULATION RESULTS OF THE PROPOSED ADAPTIVE BIASED CMOS OTA

The output current plot of the proposed adaptive biased CMOS OTA (Figure 4.3) operating in subthreshold region is governed by the expression given by equation (4.17). The differential voltage V_{in} $(= V_1 - V_2)$ has been obtained by keeping one of the voltage inputs constant to a fixed DC value and varying the other input. Table 5.5 compares the theoretical and simulated values of output current (I_{out}) for different values of the differential input voltage in subthreshold region.

Table 5.5 Comparison of theoretical and simulated output current values for different values of differential input voltage in subthreshold region.

Input Voltage V1(V)	*Input Voltage V2 (V)*	V_{in}=V1-V2 (V)	$tanh(\frac{V_2 - V_1}{2\eta V_T})$	I_{out} (nA) *Theoretical Value*	I_{out} (nA) *Simulated Value*
0.150	0.250	0.100	0.921	22.03	21.73
0.160	0.250	0.090	0.894	21.74	21.33
0.170	0.250	0.080	0.857	21.27	20.02
0.180	0.250	0.070	0.807	20.61	20.77
0.190	0.250	0.060	0.744	19.71	20.02
0.200	0.250	0.050	0.644	18.45	19.02
0.210	0.250	0.040	0.565	16.68	17.66
0.220	0.250	0.030	0.446	14.21	13.39
0.230	0.250	0.020	0.309	10.81	10.14
0.240	0.250	0.010	0.158	06.17	05.84
0.250	0.250	0.000	0.000	0.00	0.004

From the Table 5.5, it can be seen that both the theoretical and simulated current values are closely matched and hence follows the equation (4.17) quite appropriately. In the absence of adaptive biasing the bias current I_B is the summation of the drain currents of transistors M1 and M2 given by equation (4.11).

When the adaptive biased circuit realised by proposed current subtractors are functional then any disturbance around the virtual ground is sensed and difference current between the two

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drain currents I_1 and I_2 is generated by one of the current subtractor depending upon the polarity of the currents. The other subtractor remains inoperable since it is supposed to draw negative current which is not feasible. When $V_{in} > 0$ or $I_1 > I_2$ the current subtractor $A(I_1 - I_2)$ is functional and when $V_{in} < 0$ or$I_2 > I_1$, then the current subtractor $A(I_2 - I_1)$ is functional. The graphs shown in Figures 5.3 and 5.4 depict that both the current subtractors are operable in their respective regimes of operation.

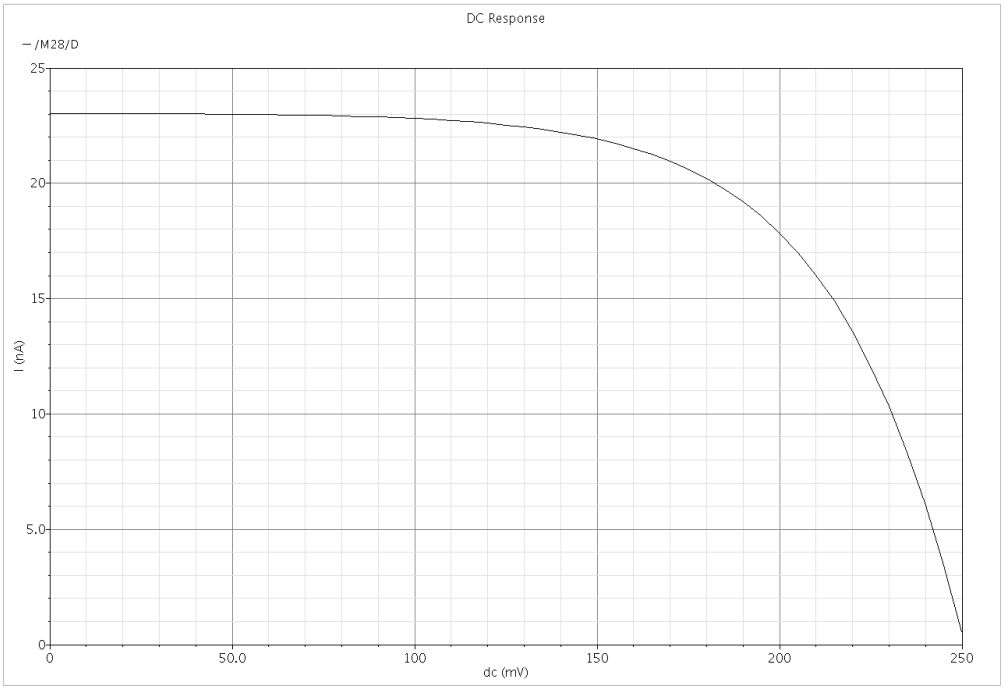

Figure 5.3 Plot of current through current subtractor circuit "A (I_1-I_2)" when Vin>0

Table 5.6 shows the values of current flowing in the current subtractor for different values of the differential voltage applied to the proposed circuit.

Table 5.6 Current values in current subtractor "$A(I_1 - I_2)$" when V_{in}>0

Input Voltage V1 (V)	*Input Voltage V2 (V)*	*I_1 (nA)*	*I_2 (nA)*	*Current values in Current Subtractor(nA)*
0.250	0.150	22.83	1.09	21.73
0.250	0.170	22.80	2.02	20.77
0.250	0.190	22.76	3.74	19.02
0.250	0.210	22.68	6.85	15.83
0.250	0.230	22.56	12.44	10.14
0.250	0.250	22.51	22.17	0.004

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If V_1 is fixed to a value of 0.250V and V_2 is varied from 0 to 0.250V, the current I_1 is greater than I_2,so the current subtractor $A(I_1 - I_2)$ is drawing current which is the difference between the two drain current of I_1 and I_2.

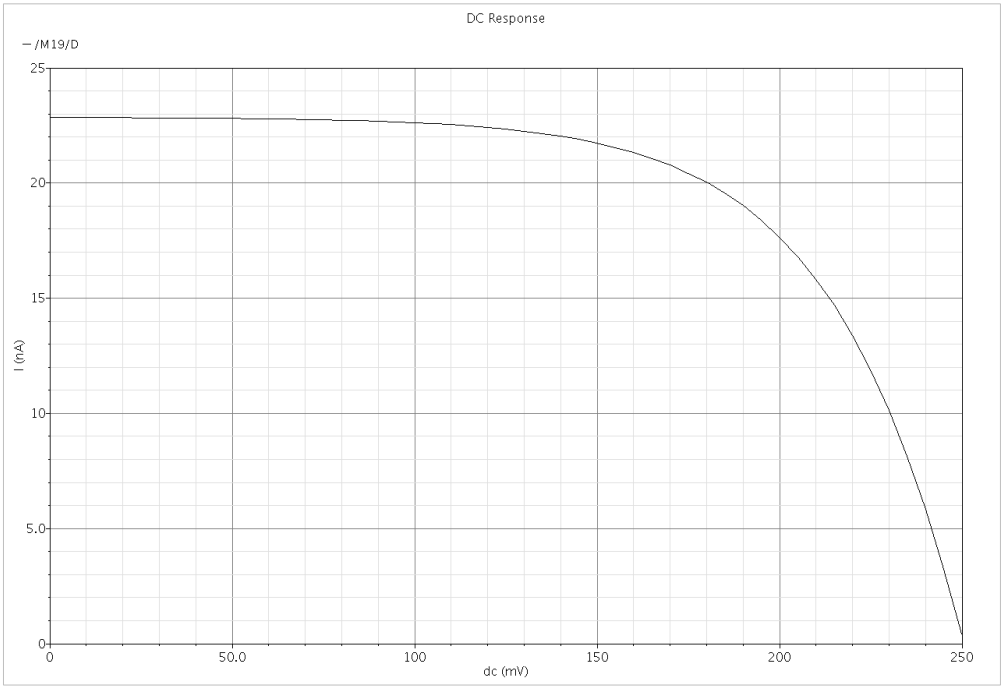

Figure 5.4 Plot of current through current subtractor circuit "$A(I_2 - I_1)$" when Vin<0

Table 5.7 shows the drain current values and the corresponding values of current flowing in the current subtractors for different values of differential voltage. If V_2 is fixed to a value of 0.250 V and V_1 is varied from 0 to .250, the current I_2 is greater than I_1, so the current subtractor $A(I_2 - I_1)$ is drawing current which is the difference between the two drain current of $I_1$and I_2.

Table 5.7 Current values in current subtractor "$A(I_2 - I_1)$" when V_{in}<0

Input Voltage V1 (V)	*Input Voltage V2 (V)*	I_1 *(nA)*	I_2 *(nA)*	*Current values in Current Subtractor(nA)*
0.150	0.250	22.83	1.09	21.73
0.170	0.250	22.80	2.02	20.77
0.190	0.250	22.76	3.74	19.02
0.210	0.250	22.68	6.85	15.83
0.230	0.250	22.56	12.44	10.14
0.250	0.250	22.51	22.17	0.004

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The OTA with adaptive biasing operation function as feedback amplifier by adding current iteratively to the fixed bias current (I_B) in a looping fashion giving rise to the increased total bias current described by equation (4.8).The Figure 5.5(a) and (b) shows the total bias current variation in transistor M1 and M2 respectively with respect to differential voltage for different values of the adaptive bias feedback factor "*A*". The maximum bias current flows when one of the transistors completely turns off. When the differential voltage is zero then the equal current flows through both the input transistors that are half of the fixed bias current (I_B).

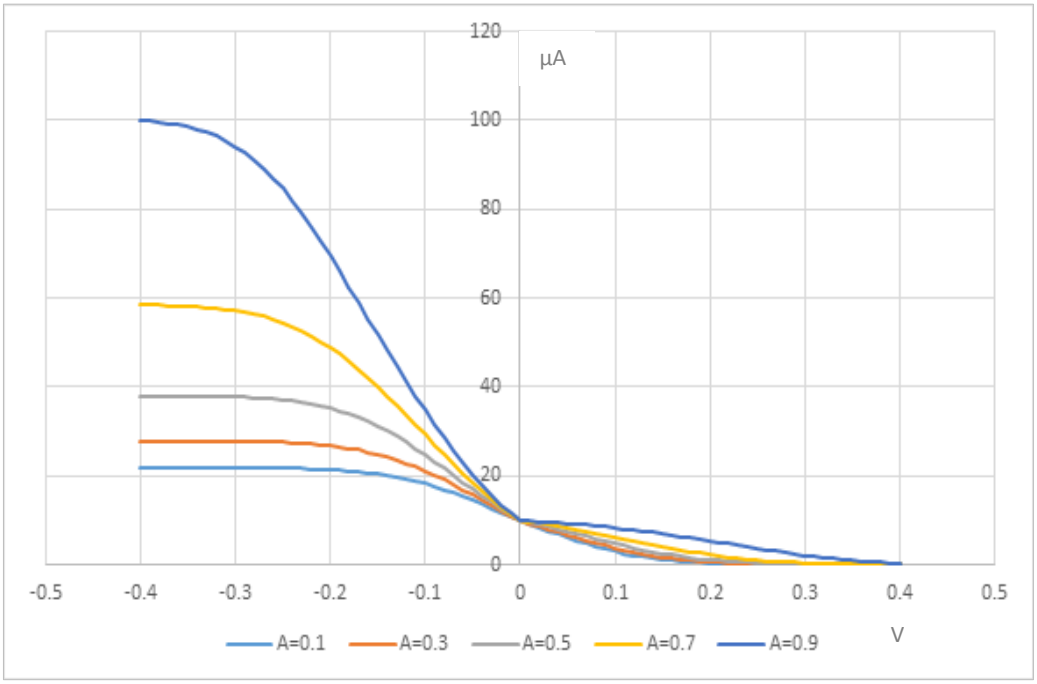

Figure 5.5(a) Current through transistor M1 w.r.t differential voltage in the presence of adaptive biasing for different values of "A".

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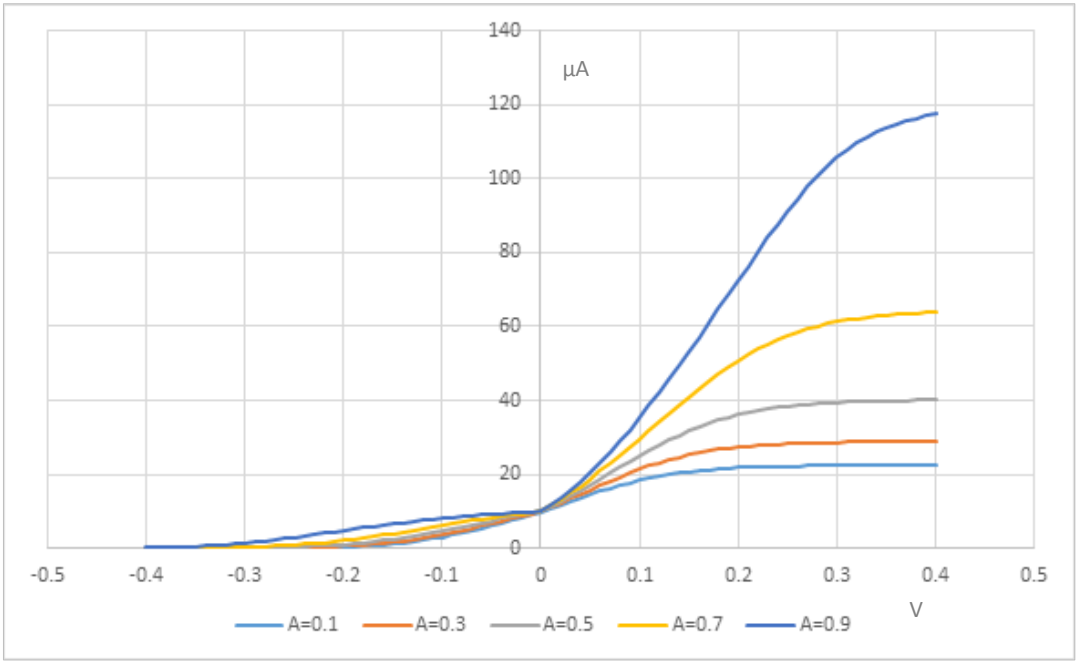

Figure 5.5(b) Current through transistor M2 w.r.t differential voltage in the presence of adaptive biasing for different values of "A".

5.4 SIMULATION RESULTS OF THE PROPOSED DC GAIN ENHANCED OTA USING PATIAL POSTIVE FEEDBACK

The output current expression for the DC enhanced OTA (Figure 4.4) is given by equation (4.38). The output current is enhanced by the factor of$\frac{1}{1-\beta}$, where β is given by equation (4.40). It depends on the value of bias current and aspect ratio of load and feedback transistors. The dependence of output current on different values of bias current is shown in Figure 5.6. Table 5.8 shows the value of output current in the presence of partial positive feedback for different values of bias current (I_A).

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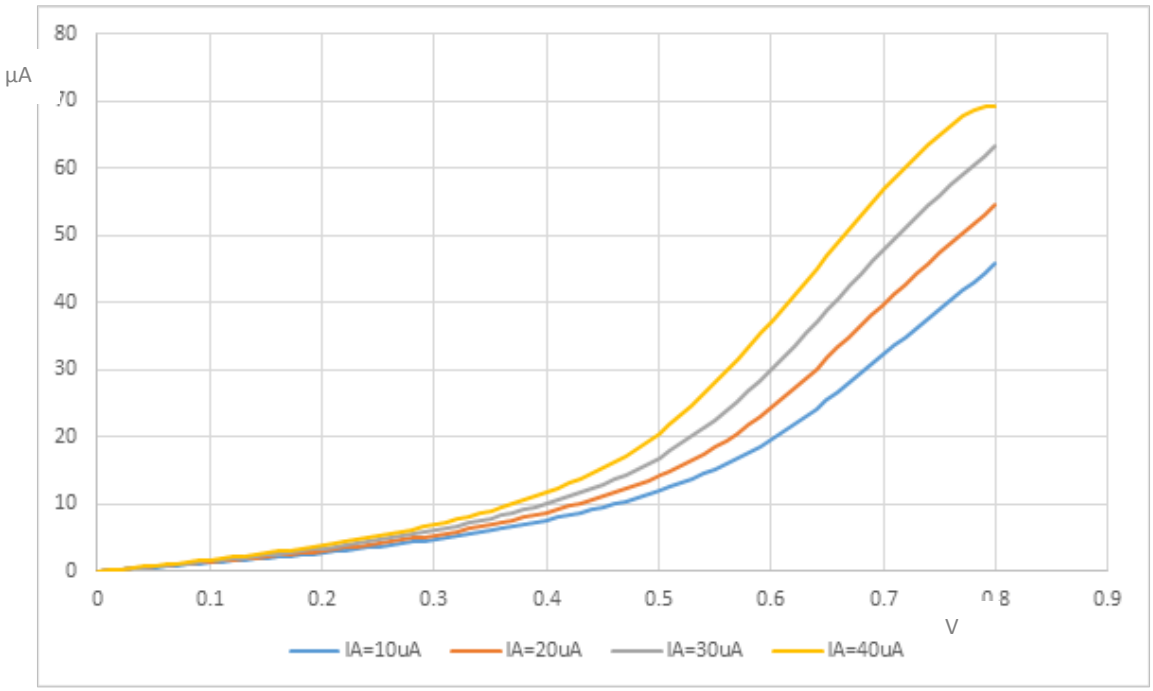

Figure 5.6 Graph of output current for different values of bias current (I_A)

Table 5.8 Output current variation with the different values of bias current (I_A)

Input Voltage V1 (V)	*Input Voltage V2 (V)*	I_{out} *(µA)* I_A*=10µA*	I_{out}*(µA)* I_A*=20 µA*	I_{out} *(µA)* I_A*=30 µA*	I_{out} *(µA)* I_A*=40 µA*
1.0	1.8	45.71	54.55	63.31	69.33
1.1	1.8	32.08	39.55	66.10	56.70
1.2	1.8	19.58	24.30	45.98	37.16
1.3	1.8	11.93	14.11	25.77	20.56
1.4	1.8	7.65	8.74	13.65	11.68
1.5	1.8	4.71	5.34	7.91	6.89
1.6	1.8	2.69	3.02	4.28	3.80
1.7	1.8	1.18	1.30	1.83	1.62
1.8	1.8	0.0006	0.0007	0.001	0.004

The output current for different values of aspect ratios between load and feedback transistors is shown Figure 5.7. Table 5.9 shows the value of output current in the presence of partial positive feedback for different values of aspect ratio between load and feedback transistors.

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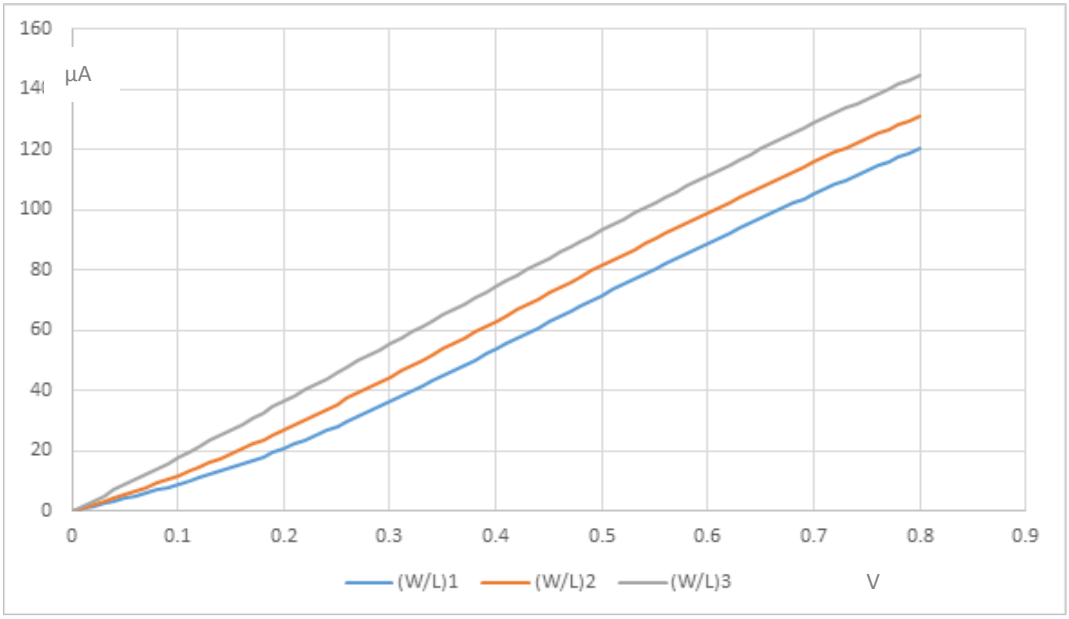

Figure 5.7 Graph of output current for different values of aspect ratios between load and feedback transistors

Table 5.9 Output current variation with the different values of aspect ratio between feedback and load transistors.

Input Voltage V1 (V)	*Input Voltage V2(V)*	*I_{out} (μA) for $(W/L)_1$ (W)MP1,2=5(W)MP5,6)*	*I_{out}(μA) for $(W/L)_2$ (W)MP1,2=10(W)MP5,6)*	*I_{out}(μA) for $(W/L)_3$ (W)MP1,2=15(W)MP5,6))*
1.0	1.8	120.34	131.07	144.56
1.1	1.8	105.22	115.82	128.65
1.2	1.8	88.90	99.11	111.32
1.3	1.8	51.57	81.22	93.17
1.4	1.8	53.69	62.70	74.46
1.5	1.8	36.18	44.38	55.43
1.6	1.8	20.73	26.93	36.34
1.7	1.8	8.82	11.71	17.60
1.8	1.8	0.0006	0.062	0.010

5.5 SIMULATION RESULTS OF THE PROPOSED POWER EFFICIENT HIGH DC GAIN ADAPTIVE BIASED CMOS OTA

The complete circuit of power efficient high DC gain adaptive biased OTA shown in Figure 4.5 has been simulated using UMC .18μm CMOS process technology. The circuit parameters

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of the proposed OTA has been calculated and compared with the existing OTAs in the literature.

The frequency response of the proposed OTA is shown in Figure 5.8 shows. From the plot the open loop DC gain of the proposed OTA circuit is calculated.

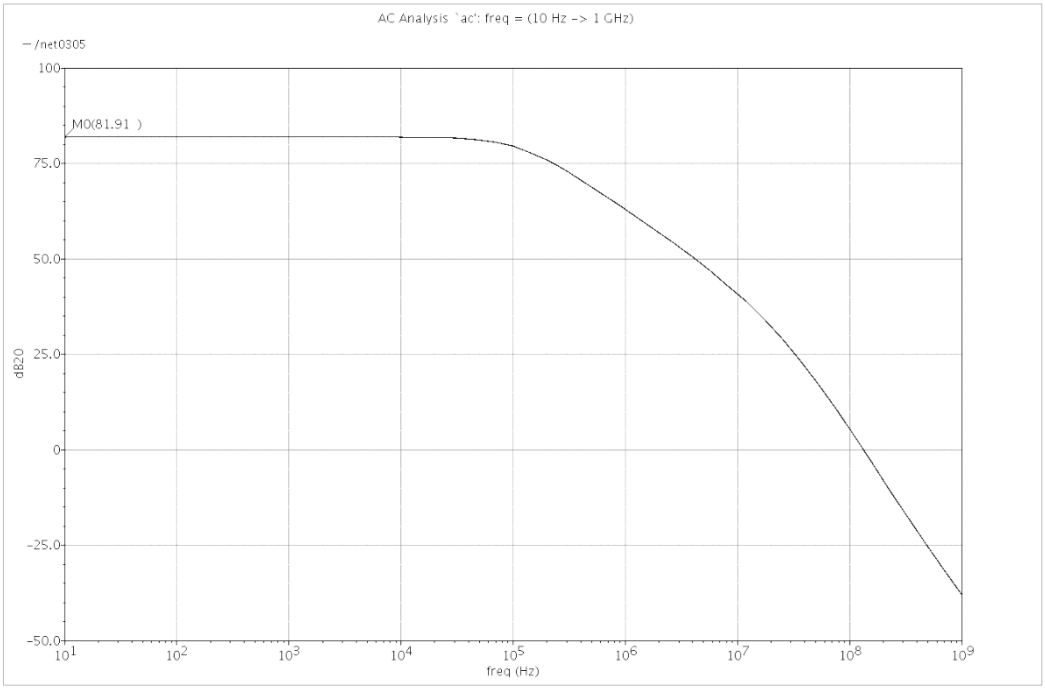

Figure 5.8 Gain v/s frequency plot of the proposed OTA circuit.

The enhanced open loop DC gain of the OTA is 81.91dB. The significant improvement in the gain has been achieved due to the presence of partial positive feedback present in the circuit. The high value of gain is suitable for high performance analog circuits. The unity gain frequency is calculated from the gain v/s frequency plot, by calculating the value of frequency at which the gain value of 0 dB. From the Figure 5.8 the value of unity gain frequency (UGF) is calculated as 132.16MHz. The proposed circuit has GBW of 1387.7MHz.

The standby current graph is shown in Figure 5.9. The value of standby current has been reduced significantly owing to the presence of adaptive biasing in the circuit. Its value lies in the range which is less than 6uA, that is quite good for the power efficient system design.

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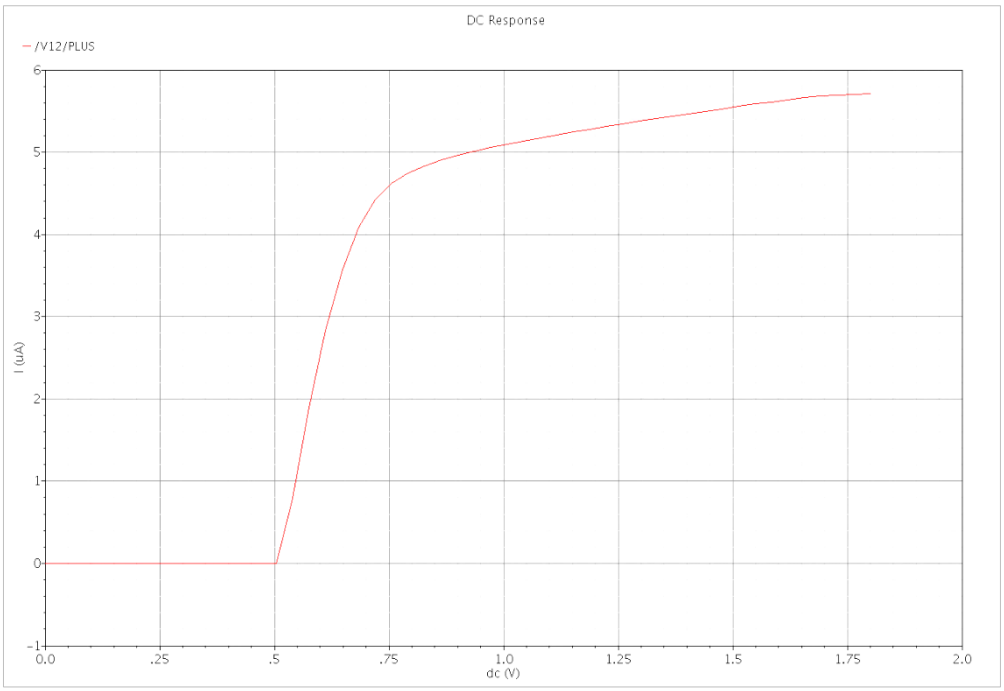

Figure 5.9 Standby current of the proposed OTA circuit

The CMRR of the circuit shows its ability to reject common mode input signal. This is the ability of an OTA to cancel out or reject any signals that are common to both inputs, and amplify any signals that are differential between them.

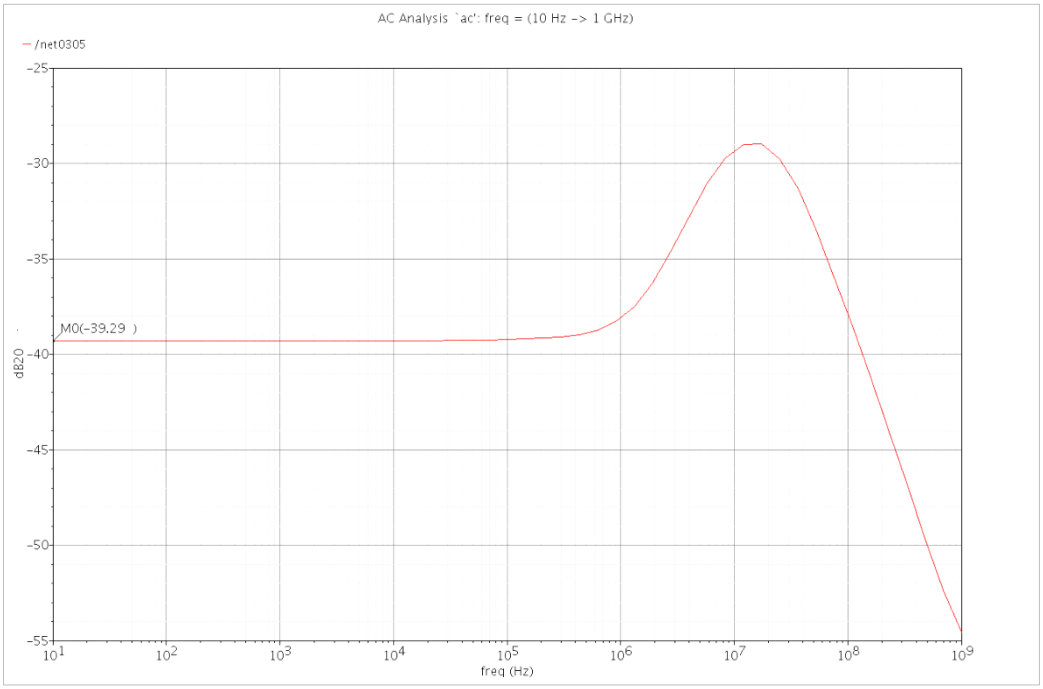

Figure 5.10 Plot of common mode gain of the proposed OTA circuit

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High value of CMRR is always desirable. CMRR is simply the magnitude of the ratio of the differential gain to the common-mode gain. The common mode gain of the proposed OTA is shown in Figure 5.10 whose value is -39.29dB. The value of CMRR of the proposed OTA is 121.2dB.

Power supply ripple rejection ratio (PSRR) is the ripple rejection ability of the circuit to reject the ripples of power supply at various frequencies. It is the measure of OTA's ability to prevent its output from being affected by noise or ripples at the power supply. The PSRR value of the circuit is shown in Figure 5.11. The proposed CMOS OTA has PSRR of 54.34dB.

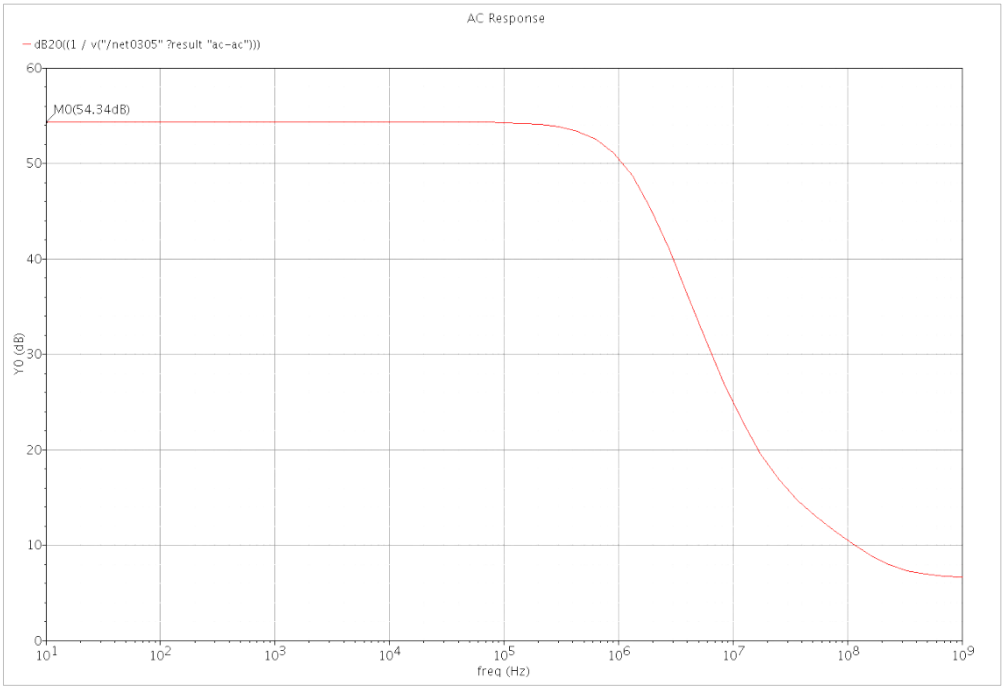

Figure 5.11 Plot of PSRR of the proposed OTA circuit

Input Common Mode Range is the maximum voltage (negative or positive) that can be applied at both inputs of an OTA at the same time, with respect to the ground. It is the range of OTA for which there is a linear relationship between input and output. This is the range of voltage which ensures the input transistors to remain in saturation mode of operation. The ICMR of the proposed OTA is shown in Figure 5.12. For the proposed OTA the value lies in the range of 0.5 – 1.7V.

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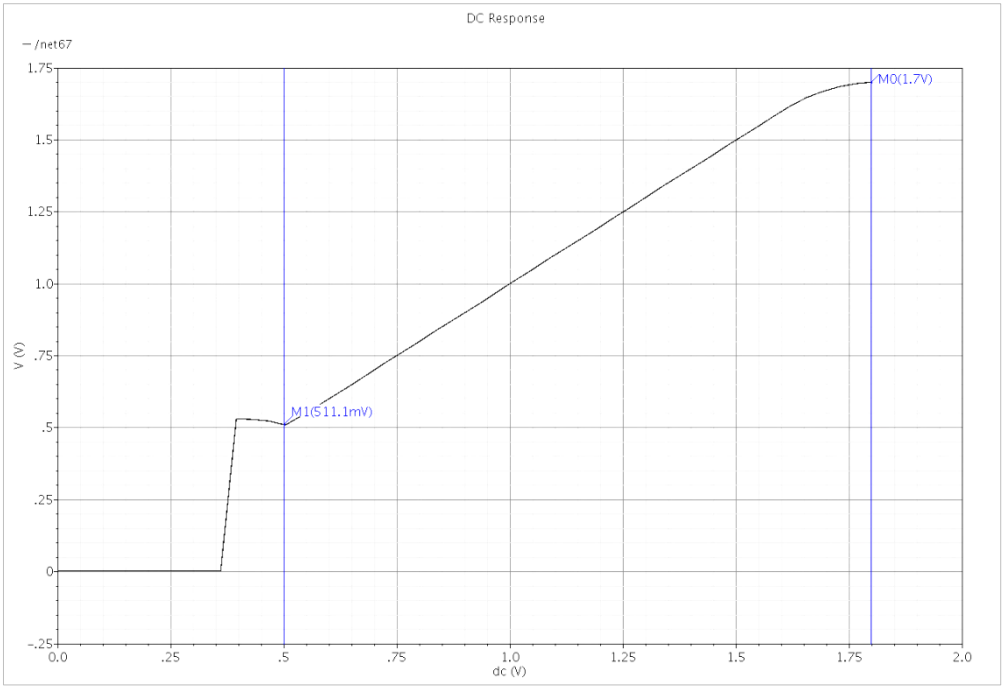

Figure 5.12 Plot of input mode common range of the proposed OTA circuit

The transient analysis of the proposed circuit has been done by applying time varying pulse and sinusoidal inputs. The sinusoidal input response of the proposed OTA is shown in Figure 5.13.

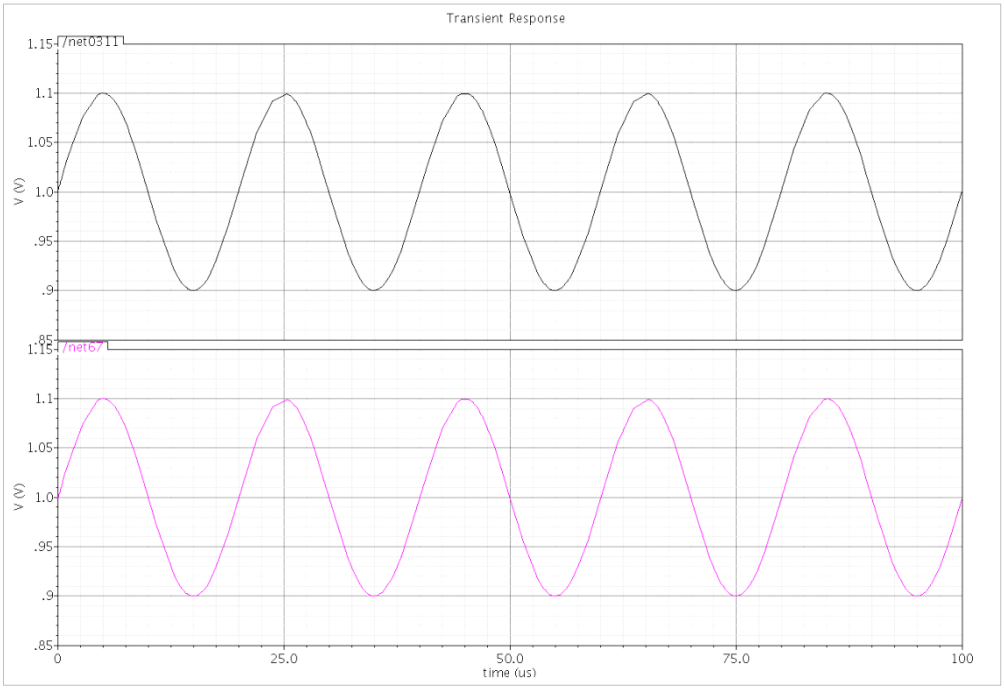

Figure 5.13 Sinusoidal input response of the proposed OTA circuit

The proposed OTA functions as unity gain buffer when its ouput is connected to the inverting input terminal and the other input terminal is provided with the transient pulse. The OTA

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functions as unity gain buffer in this mode as shown in Figure 5.14. The pulse input response of the OTA is shown in Figure 5.14. From the transient response the slew rate is calculated to be equal to 27.2 V/µS and the setting time is 409.1ns.

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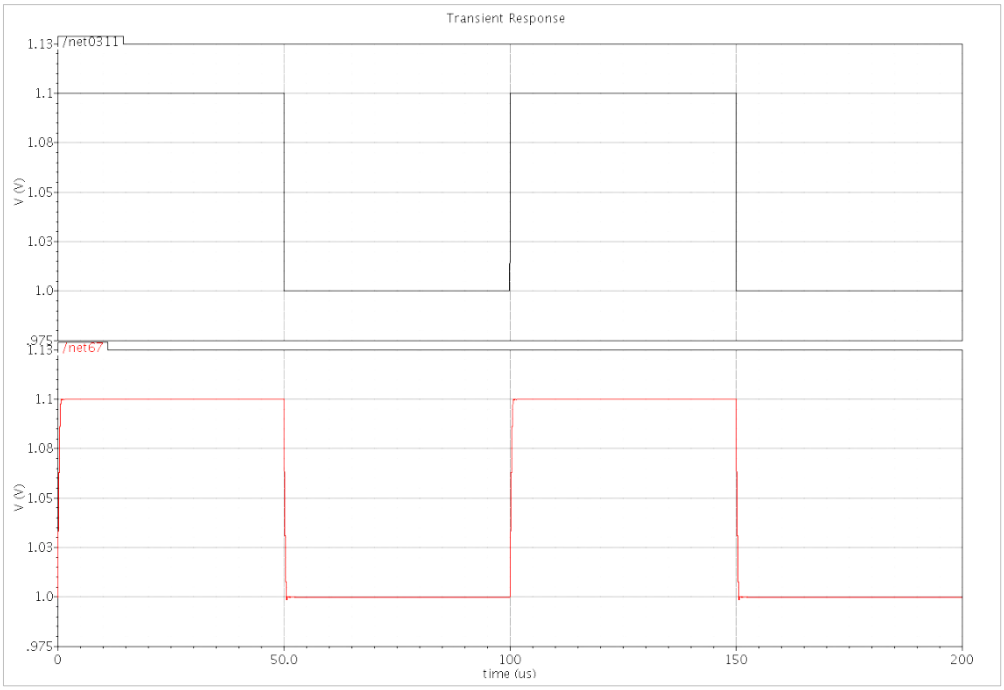

Figure 5.14 Pulse input response of the proposed OTA circuit

The slew rate limitation of the conventional OTA's design has been overcome by using the technique of adaptive biasing in the proposed OTA which provides additional biasing current without increasing the standby power consumption. This technique increases slew rate without affecting GBW, which is shown by the fact that the proposed circuit has a GBW of 1387.7MHz

5.6 LAYOUT DESIGNS

The physical layouts of proposed circuits have been designed using UMC 0.18µm CMOS process technology in cadence virtuoso layout editor. Design Rule Check (DRC) and Layout vs Schematic (LVS) is performed in order to verify that layout fulfils all electrical and geometric rules provided by foundry. The basic design rules are:

Metal 1 to metal 1 spacing	0.24 µm
Minimum contact size	0.24 µm

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Poly to poly spacing	0.24 μm
Poly to metal spacing	0.28/0.00μm
Contact overlap to p+ diffusion	0.1 μm
Metal 1 width	0.24 μm
Poly extension beyond active	0.22 μm
Minimum contact spacing	0.26 μm
N well overlap p+ diffusion	0.43 μm
Diffusion contact to poly spacing	0.15 μm
Minimum p+ implant overlap p+ diffusion	0.22 μm
Poly width	0.18 μm
Minimum poly extension on to field region	0.22 μm
Poly contact to diffusion edge spacing	0.18 μm
Minimum poly overlap contact	0.1 μm
Minimum metal area	$0.1764\mu m^2$
Minimum metal2 width	0.28 μm
Metal1 and metal2 overlap over via	0.08 μm
Minimum non equal potential 1.8 V N well spacing	2μm

5.6.1 LAYOUT OF CURRENT MODE ANALOG COMPUTATIONAL CIRCUITS

The current mode analog computational circuits such as current adder and subtractor based on CCM perform the operation of addition and subtraction of input currents with high linearity over wide range of current. The designed current subtractor has been employed for adaptive biasing of the proposed OTA. The layout of the proposed current adder and subtractor has been designed using UMC 0.18μm CMOS process technology in Cadence Virtuoso layout editor. The layout of current adder and current subtractor circuits are shown in Figures 5.15 and 5.16, respectively. The Design Rule Check (DRC) of both the circuits are successfully performed.

The Layout vs Schematic (LVS) of these circuits are also performed and the LVS reports of current adder and subtractor are shown in Figures 5.17 and Figure 5.18, respectively. From the Figures 5.17 and 5.18, it is clear that LVS of these circuits are matched.

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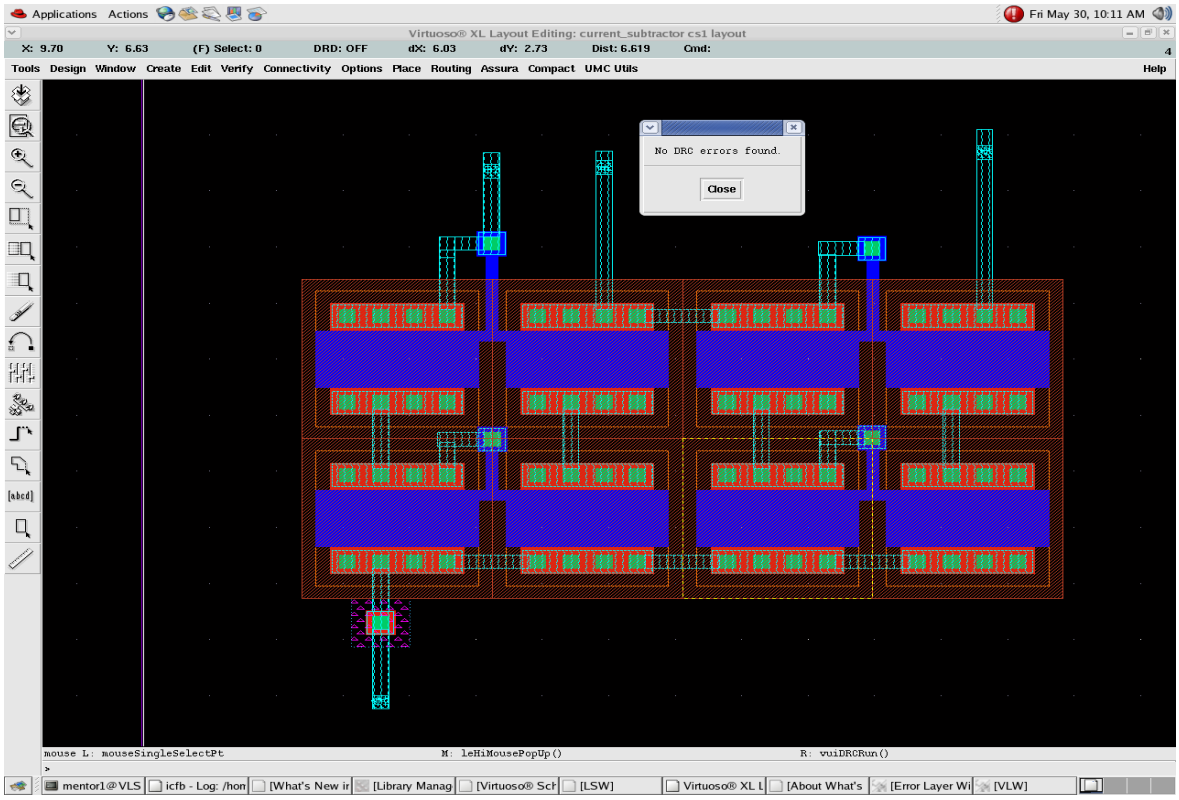

Figure 5.15 Layout of the proposed current adder circuit

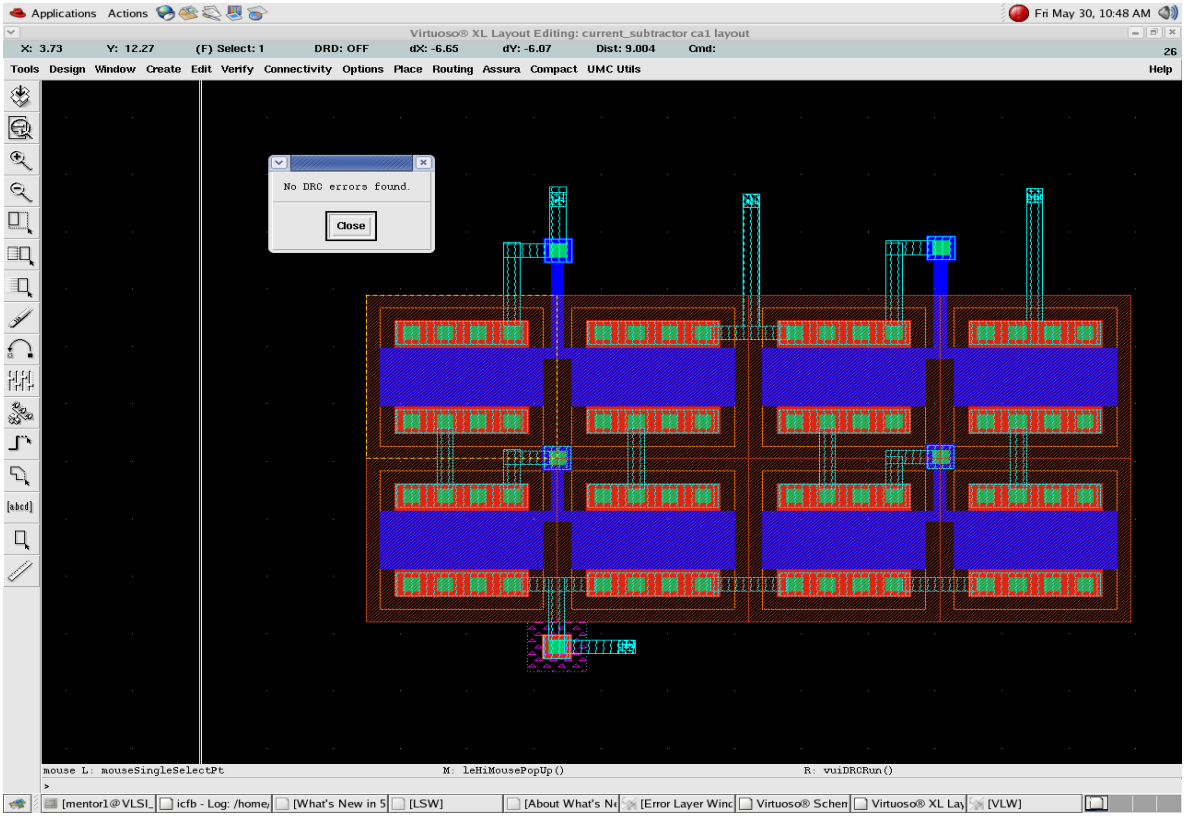

Figure 5.16 Layout of the proposed current subtractor circuit

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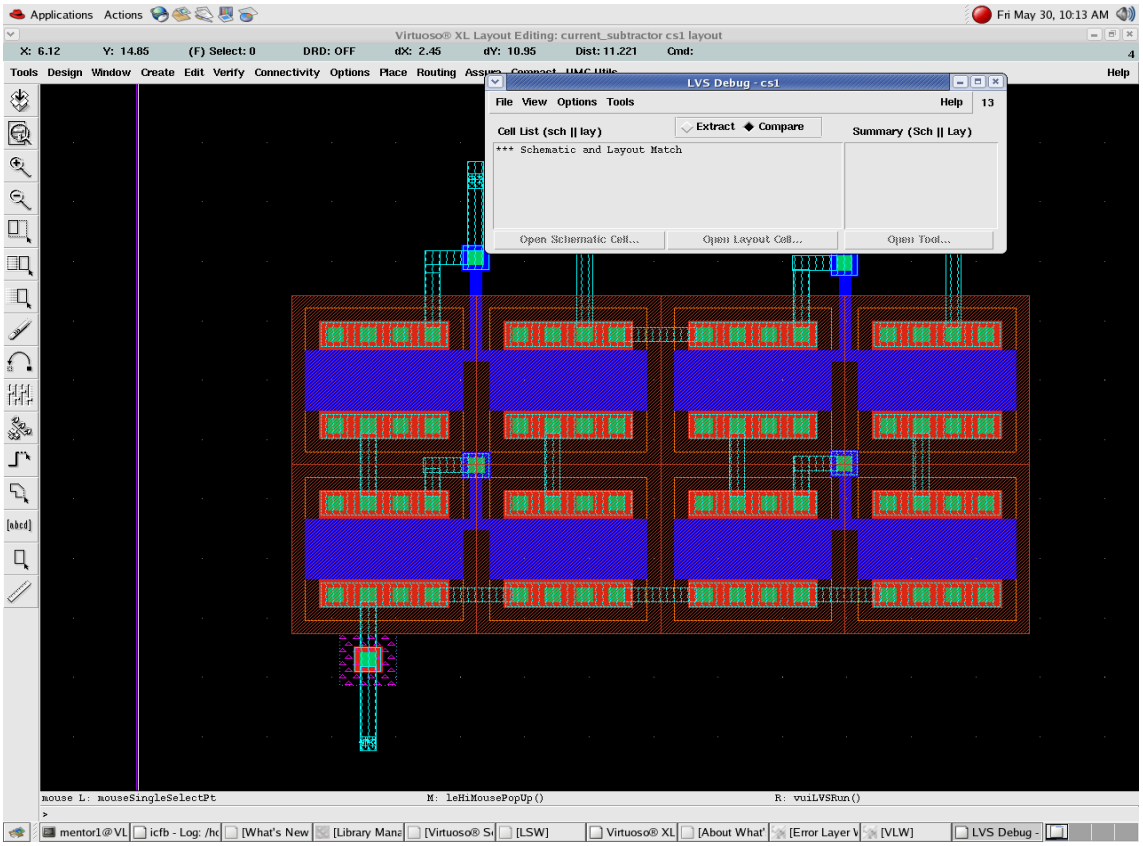

Figure 5.17 LVS of the proposed current adder circuit

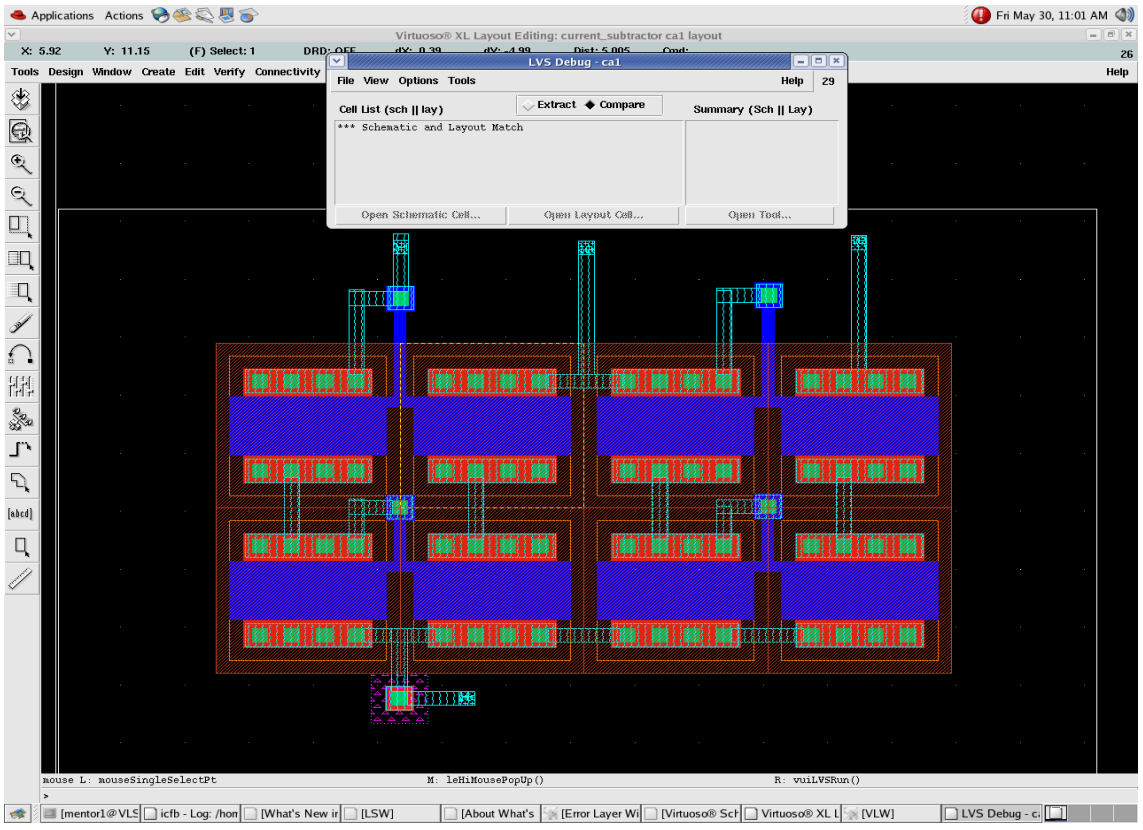

Figure 5.18 LVS of the proposed current subtractor circuit

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5.6.2 LAYOUT OF THE PROPOSED POWER EFFICIENT HIGH DC GAIN CMOS ADAPTIVE BIASED OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The layout of proposed OTA circuit has been designed using UMC 0.18µm CMOS process technology in Cadence Virtuoso layout editor. Design Rule Check (DRC) and Layout v/s Schematic (LVS) has been performed to show that the proposed OTA fulfils the geometric rules of the foundry. Figure 5.19 shows the layout of the proposed OTA and Figure 5.20 shows that the proposed OTA circuit is LVS matched.

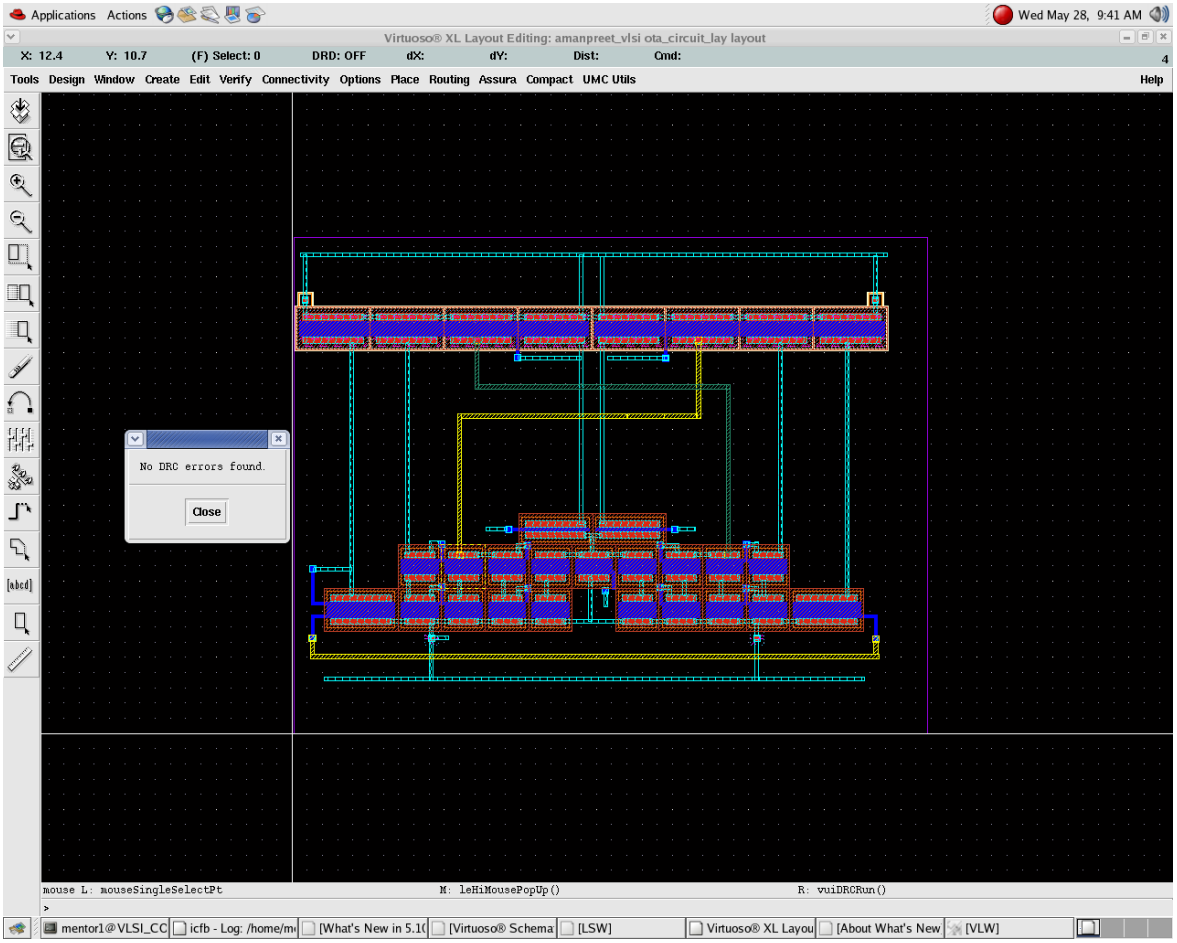

Figure 5.19 Layout of the proposed OTA circuit

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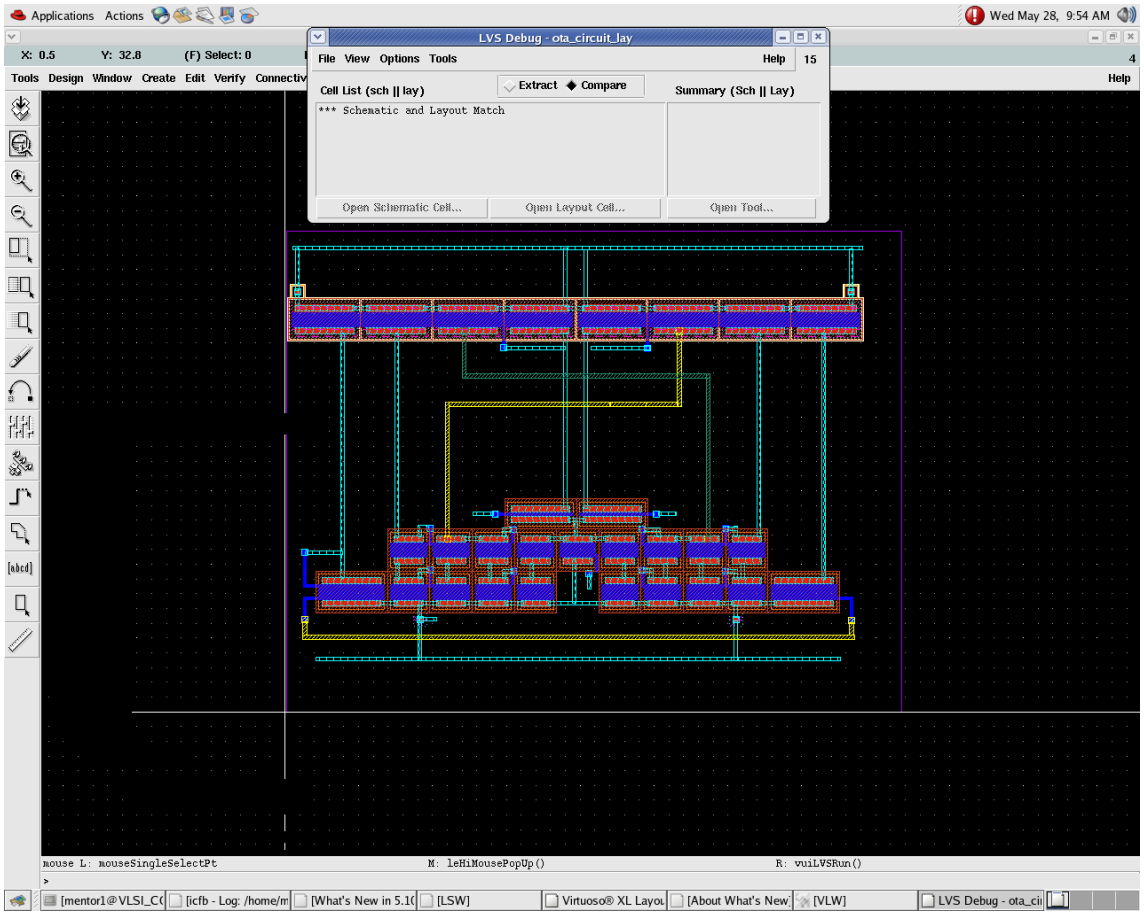

Figure 5.20 LVS of the proposed OTA circuit

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Table 5.10 compares the performance parameters of proposed OTA with the existing similar OTA circuits available in literature and the comparison shows that the proposed circuit has high open loop DC gain, high GBW, high UGF and low static power dissipation and low standby current. The proposed OTA is suitable for various high frequency analog applications because of these attributes.

Table 5.10 Comparison of proposed power efficient high dc gain adaptive biased CMOS OTA circuit with existing OTA's in literature [29], [38]-[46]

	[38]	**[39]**	**[40]**	**[41]**	**[42]**	**[43]**	**[29]**	**[44]**	**[45]**	**[46]**	**Proposed OTA**
Year	2005	2006	2007	2007	2007	2009	2009	2010	2012	2013	2014
CMOS Process	0.5 µm	0.18 µm	0.35 µm	0.35 µm	0.18 µm	90 nm	0.18 µm	90 nm	0.18 µm	0.18 µm	0.18 µm
Supply Voltage	2V	1V	1.5	1.5	0.8V	+/- 0.6	1.8V	+/- 0.6	1.5V	+/-0.6 V	1.8V
Capacitive Load	80Pf	5pF	15pF	15pF	2pF	10pF	10pF	10pF	-	1pF	10Pf
DC Gain (dB)	37.5	58.25	75	78	62	79.2	48.97	80.2	70.15	44	81.91
GBW	470 KHz	79.53 MHz	4.6 MHz	8.9 MHz	160 MHz	7.6 MHz	57.27 KHz	9.5 MHz	136 MHz	590 KHz	1387.7 MHz
CMRR (dB)	69	-	132	126	-	129	124.37	124	100	110	121.2
PSRR +/- (dB)	57/46	-	147/ 150		-	116/111	81.4/ 50.3	135/140		73/48	54.34
SR +/- (V/µs)	42/80	2.3	40	37	-	32	4.92/ 5.04	37	236	71	27.2
Input Offset	-	-	-	200µV	-	11.2µV	-	599.96 mV	-	0.7mV	10.56 µV
Input mode common range	-	-	-	-	-		0.4V – 1.8V	-	-	-	0.5V-1.7V
Settling Time	100/3 3	-	310ns	390ns		262µs	1.0/2.1 µs	247µs	19ns	160ns	409.1ns
Static Power Dissipation	140 µW	67 µW	-	169 µW	250 µW	57.6 µW	1.96 µW	96 µW	1.5 mV	0.4 µW	54 µW
Unity Gain Frequency	-	-	-	-	-	64.8 MHz	-	71.8 MHz	-	-	132.16 MHz

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CHAPTER 6

CONCLUSIONS AND FUTURE SCOPE

6.1 CONCLUSIONS

In this work, a power efficient high DC gain adaptive biased CMOS operational transconductance amplifier has been developed. The proposed CMOS OTA circuit utilizes the designed current subtractor based on CCM for providing extra tail current sources in addition to fixed bias current sources. The current subtractor provides the variable bias i.e. adaptive biasing, in the presence of input signal by providing additional bias current when the large signal is applied. The DC gain improvement has been achieved by using partial positive feedback technique. This technique improves gain and bandwidth of the circuit. The proposed circuit has been simulated using UMC 0.18μm CMOS technology process parameters and the simulation results have been presented. The proposed circuit has a DC gain of 81.91 dB. The proposed circuit has bandwidth of 111.51 KHz and the value of UGF is 132.16MHz. The slew rate of 27.2V/μs has been achieved with static power dissipation of 54μW. The proposed circuit has been compared with the existing similar circuits available in the literature and it has been observed that the proposed circuit has high DC gain, high phase margin, high bandwidth and high UGF and low static power dissipation. The proposed circuits can be widely used in various signal processing applications such as filters, data convertors, resistors, inductors, integrators etc. The physical layout of all the proposed circuits is designed using Cadence Virtuoso layout editor in standard UMC 0.18 μm CMOS process technology.

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6.2 FUTURE SCOPE

Some suggestions and ideas for future work:

- The proposed circuits can be used in various analog signal processing applications to design analog building blocks such as filters, integrators, data converters, ADCs, mixers, resistors etc.
- Class AB operation can be used to improve power efficiency further.
- Negative resistance gain enhancement technique is another possible method to improve gain in low voltage and low power analog environment.

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LIST OF PUBLICATION

• Amanpreet Kaur and Rishikesh Pandey, "Current Mode Computational Circuits for Analog Signal Processing," *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*, Vol. 3, Issue 4, pp.8987-8995, April 2014.

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APPENDIX A

MODELS PARAMETERS

The UMC 0.18μm CMOS technology model file is listed below.

MODEL PARAMETERS FOR NMOS TRANSISTOR

```
==================================================================
Model n_18_mm bsim3v3 type=n

==================================================================

+ version=3.2000e+00        binunit=1.0000e+00     mobmod=1.0000e+00
+ capmod=2.0000e+00         nqsmod=0.0000e+00
+ tox=4.2000e-09 + dtox_n_18_mm                      toxm=4.2000e-09
+ xj=1.6000e-07             nch=3.7446e+17           rsh=8.0000e+00
+ ngate=1.0000e+23          vth0=3.0750e-01 + dvth0_n_18_mm
+ k1=4.5780e-01             k2=-2.6380e-02           k3=-1.0880e+01
+ k3b=2.3790e-01            w0=-8.8130e-08           nlx=4.2790e-07
+ dvt0=4.0420e-01           dvt1=3.2370e-01         dvt2=-8.6020e-01
+ dvt0w=3.8300e-01          dvt1w=6.0000e+05       dvt2w=-2.5000e-02
+ lint=1.5870e-08           wint=1.0220e-08          dwg=-3.3960e-09
+ dwb=1.3460e-09            u0=3.1410e+02 + du0_n_18_mm
+ ua=-9.2010e-10            ub=1.9070e-18             uc=4.3550e-11
+ vsat=7.1580e+04           a0=1.9300e+00             ags=5.0720e-01
+ b0=1.4860e-06             b1=9.0640e-06            keta=1.7520e-02
+ a1=0.0000e+00             a2=1.0000e+00           voff=-1.0880e-01
+ nfactor=1.0380e+00        cit=-1.5110e-03          cdsc=2.1750e-03
+ cdscd=-5.0000e-04         cdscb=8.2410e-04         eta0=1.0040e-03
+ etab=-1.4590e-03          dsub=1.5920e-03          pclm=1.0910e+00
+ pdiblc1=3.0610e-03        pdiblc2=1.0000e-06    pdiblcb=0.0000e+00
+ drout=1.5920e-03          pscbe1=4.8660e+08      pscbe2=2.8000e-07
+ pvag=-2.9580e-01          rdsw=4.9050e+00          prwg=0.0000e+00
+ prwb=0.0000e+00           wr=1.0000e+00          alpha0=0.0000e+00
+ alpha1=0.0000e+00         beta0=3.0000e+01        xpart=1.0000e+00
+ cgso=2.3500e-10 + dcgso_n_18_mm
+ cgdo=2.3500e-10 + dcgdo_n_18_mm                     cgbo=0.0000e+00
+ cgsl=0.0000e+00           cgdl=0.0000e+00        ckappa=6.0000e-01
+ cf=1.5330e-10             clc=1.0000e-07           cle=6.0000e-01
+ dlc=2.9000e-08            dwc=0.0000e+00         vfbcv=-1.0000e+00
+ noff=1.0000e+00           voffcv=0.0000e+00        acde=1.0000e+00
+ moin=1.5000e+01           lmin=1.8000e-07          lmax=5.0000e-05
+ wmin=2.4000e-07           wmax=1.0000e-04
+ xl= - 1.0500e-08 + dxl_n_18_mm
+ xw=0.0000e-00 + dxw_n_18_mm                         js=1.0000e-06
+ jsw=7.0000e-11            cj=1.0300e-03 + dcj_n_18_mm
+ mj=4.4300e-01             pb=8.1300e-01
+ cjsw=1.3400e-10 + dcjsw_n_18_mm                     mjsw=3.3000e-01
+ tnom=2.5000e+01           ute=-1.2860e+00          kt1=-2.2550e-01
+ kt1l=-4.1750e-09          kt2=-2.5270e-02           ua1=2.1530e-09
+ ub1=-2.6730e-18           uc1=-3.8320e-11           at=1.4490e+04
+ prt=-1.0180e+01           xti=3.0000e+00            wl=0.0000e+00
```

`

```
+ wln=1.0000e+00            ww=7.2620e-16              wwn=1.0000e+00
+ wwl=0.0000e+00            ll=-1.0620e-15             lln=1.0000e+00
+ lw=2.9960e-15             lwn=1.0000e+00             lwl=0.0000e+00
+ llc=-2.1400e-15           lwc=0.0000e+00            lwlc=0.0000e+00
+ wlc=0.0000e+00            wwc=0.0000e+00            wwlc=0.0000e+00
+ lvth0= - 1.0000e-03 + dlvth0_n_18_mm
+ wvth0=6.027e-02 + dwvth0_n_18_mm          pvth0=0 + dpvth0_n_18_mm
+ lnlx=-2.8540e-08           wnlx=0.0000e+00           pnlx=0.0000e+00
+ wua=-1.8800e-11            wu0=5.4000e-01 + dwu0_n_18_mm
+ pub=3.8000e-20             pw0=1.3000e-09           wrdsw=0.0000e+00
+ weta0=0.0000e+00           wetab=0.0000e+00         leta0=1.5740e-03
+ letab=0.0000e+00           peta0=0.0000e+00         petab=0.0000e+00
+ wpclm=0.0000e+00           wvoff=-4.0780e-04       lvoff=-4.2080e-03
+ pvoff=-3.7880e-04          wa0=-4.7310e-02           la0=-4.6670e-01
+ pa0=-2.6490e-02            wags=4.2420e-03           lags=3.0280e-01
+ pags=0.0000e+00            wketa=0.0000e+00        lketa=-1.9420e-02
+ pketa=0.0000e+00           wute=6.3730e-02           lute=0.0000e+00
+ pute=0.0000e+00            wvsat=5.0660e+03         lvsat=0.0000e+00
+ pvsat=0.0000e+00 + dpvsat_n_18_mm              lpdiblc2=-4.7520e-03
+ wat=7.0670e+03             wprt=0.0000e+00           ldif=8.0000e-08
+ hdif=2.6000e-07            n=1.0000e+00              pbsw=8.8000e-01
+ cjswg=5.0000e-10 + dcjgate_n_18_mm                   ctp=9.1400e-04
+ ptp=9.2400e-04             cta=9.1900e-04            pta=1.5800e-03
+ elm=5.0000e+00             tlevc=1.0000e+00
+ noimod=2                   noia=1.3182567385564E+19
noib=144543.977074592
+ noic=-1.24515794572817E-12                           ef=0.92
+ em=41000000
```

MODEL PARAMETERS FOR PMOS TRANSISTOR

```
==================================================================

Model p_18_mm bsim3v3 type=p

==================================================================

+ mobmod=3.0000e+00         version=3.2000e+00     capmod=2.0000e+00
+ binunit=1.0000e+00        nqsmod=0.0000e+00
+ tox=4.2000e-09 + dtox_p_18_mm                       toxm=4.2000e-09
+ xj=1.0000e-07             nch=6.1310e+17          ngate=1.0000e+23
+ vth0= - 4.5550e-01 + dvth0_p_18_mm                   k1=5.7040e-01
+ k2=6.9730e-03             k3=-2.8330e+00            k3b=1.3260e+00
+ w0=-1.9430e-07            nlx=2.5300e-07           dvt0=4.8850e-01
+ dvt1=7.5780e-02           dvt2=1.2870e-01        dvt0w=-1.2610e-01
+ dvt1w=2.4790e+04          dvt2w=6.9150e-01         lint=-1.0410e-08
+ wint=-1.5250e-07          dwg=-1.1510e-07           dwb=-1.0390e-07
+ u0=1.1450e+02 + du0_p_18_mm                          ua=1.5400e-09
+ ub=2.6460e-19             uc=-9.5870e-02           vsat=5.3400e+04
+ a0=1.3500e+00             ags=3.8180e-01            b0=-3.0880e-07
+ b1=0.0000e+00             keta=1.0440e-02           a1=0.0000e+00
+ a2=1.0000e+00             voff=-1.0730e-01      nfactor=1.5350e-00
+ cit=-1.0670e-03           cdsc=7.5780e-04         cdscd=-2.8830e-05
+ cdscb=1.0000e-04          eta0=1.0710e+00          etab=-9.2910e-01
+ dsub=1.9191e+00           pclm=2.6530e+00       pdiblc1=0.0000e+00
+ pdiblc2=5.0000e-06        pdiblcb=0.0000e+00      drout=1.4570e+00
```

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+ pscbe1=4.8660e+08         pscbe2=2.8000e-07        pvag=1.1620e+00
+ rdsw=7.9210e+02           prwg=0.0000e+00          prwb=0.0000e+00
+ alpha0=0.0000e+00         alpha1=0.0000e+00       beta0=3.0000e+01
+ cgdo=2.0540e-10 + dcgdo_p_18_mm                    cgbo=0.0000e+00
+ cgso=2.0540e-10 + dcgso_p_18_mm                   xpart=1.0000e+00
+ cf=1.5330e-10             dlc=5.6000e-08           cgsl=0.0000e+00
+ cgdl=0.0000e+00           ckappa=6.0000e-01         clc=1.0000e-07
+ cle=6.0000e-01            dwc=0.0000e+00         vfbcv=-1.0000e+00
+ noff=1.0000e+00           voffcv=0.0000e+00        acde=1.0000e+00
+ moin=1.5000e+01           lmin=1.8000e-07          lmax=5.0000e-05
+ wmin=2.4000e-07           wmax=1.0000e-04
+ xl= - 2.0000e-09 + dxl_p_18_mm
+ xw=0.0000e+00 + dxw_p_18_mm                         js=3.0000e-06
+ jsw=4.1200e-11            cj=1.1400e-03 + dcj_p_18_mm
+ mj=3.9500e-01             pb=7.6200e-01
+ cjsw=1.7400e-10 + dcjsw_p_18_mm                    mjsw=3.2400e-01
+ tnom=2.5000e+01           ute=-4.4840e-01          kt1=-2.1940e-01
+ kt1l=-8.2040e-09          kt2=-9.4870e-03           ua1=4.5710e-09
+ ub1=-6.0260e-18           uc1=-9.8500e-02           at=1.2030e+04
+ prt=0.0000e+00            xti=3.0000e+00            ww=1.2360e-14
+ lw=-2.8730e-16            ll=6.6350e-15             wl=0.0000e+00
+ wln=1.0000e+00            wwn=1.0000e+00            wwl=0.0000e+00
+ lln=1.0000e+00            lwn=1.0000e+00            lwl=0.0000e+00
+ llc=-7.4500e-15           lwc=0.0000e+00           lwlc=0.0000e+00
+ wlc=0.0000e+00            wwc=0.0000e+00           wwlc=0.0000e+00
+ lvth0=4.4000e-03 + dlvth0_p_18_mm
+ wvth0= - 1.4800e-02 + dwvth0_p_18_mm
+ pvth0=3.2000e-03 + dpvth0_p_18_mm                 lnlx=-1.5840e-08
+ wrdsw=1.0070e+01          weta0=0.0000e+00        wetab=0.0000e+00
+ wpclm=0.0000e+00          wua=2.6300e-09           lua=-8.1530e-11
+ pua=5.8550e-11            wub=0.0000e+00           lub=0.0000e+00
+ pub=0.0000e+00            wuc=0.0000e+00           luc=0.0000e+00
+ puc=0.0000e+00            wvoff=-9.8160e-03      lvoff=-9.8710e-04
+ pvoff=-9.8330e-05         wa0=-4.8070e-02          la0=-2.8100e-01
+ pa0=8.6610e-02            wags=-4.1770e-02         lags=4.4540e-02
+ pags=-4.0760e-02          wketa=0.0000e+00       lketa=-1.2000e-02
+ pketa=0.0000e+00          wute=-2.6820e-01         lute=0.0000e+00
+ pute=0.0000e+00           wvsat=-1.4200e+04       lvsat=0.0000e+00
+ pvsat= - 4.3400e+02 + dpvsat_p_18_mm           lpdiblc2=3.0120e-03
+ cjswg=4.200e-10 + dcjgate_p_18_mm                  wat=-6.4050e+03
+ wprt=2.1660e+02           n=1.0000e+00             pbsw=6.6500e-01
+ cta=1.0000e-03            ctp=7.5300e-04            pta=1.5500e-03
+ ptp=1.2400e-03            ldif=8.0000e-08           rsh=8.0000e+00
+ rd=0.0000e+00             rsc=0.0000e+00            rdc=0.0000e+00
+ hdif=2.6000e-07           rs=0.0000e+00
+ noimod=2                  noia=3.57456993317604E+18 noib=2500
+ noic=2.61260020285845E-11 ef=1.1388
+ em=41000000
```

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APPENDIX B

LAYOUT VS SCHEMATIC (LVS) REPORT

The LVS report of the proposed current adder and subtractor is shown in Figure B.1 and B.2 respectively

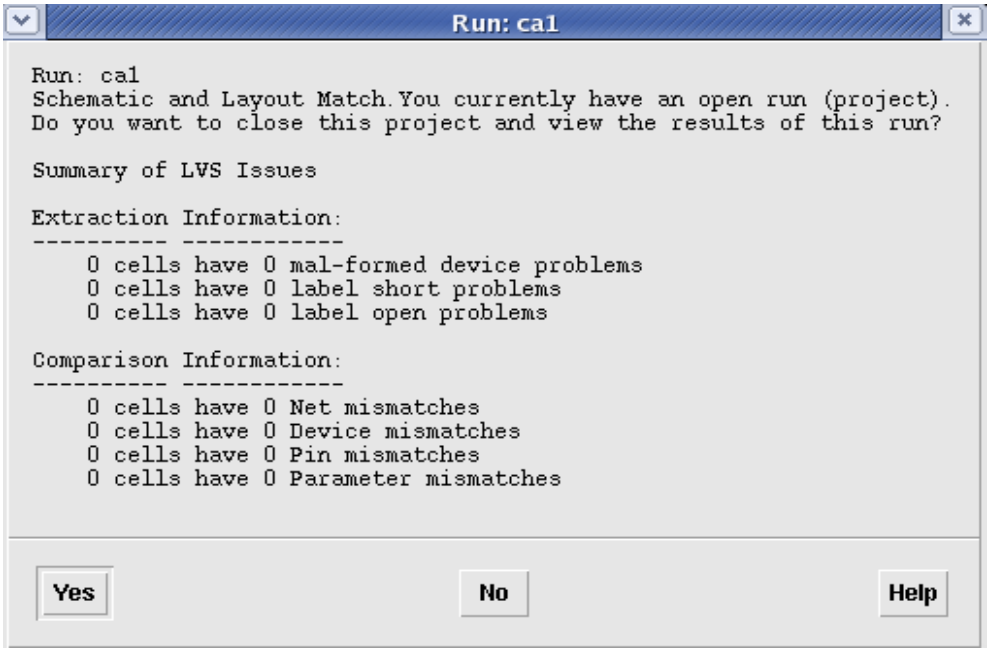

Figure B.1 LVS report of the proposed current adder

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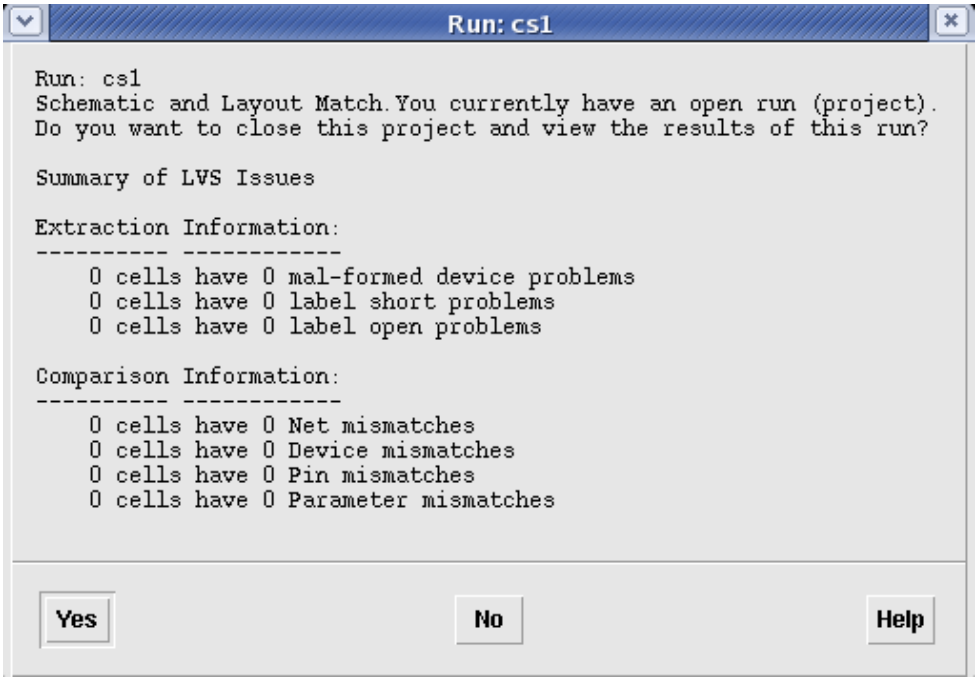

Figure B.2 LVS report of the proposed current subtractor

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The LVS report of the proposed OTA is shown in Figure B.3

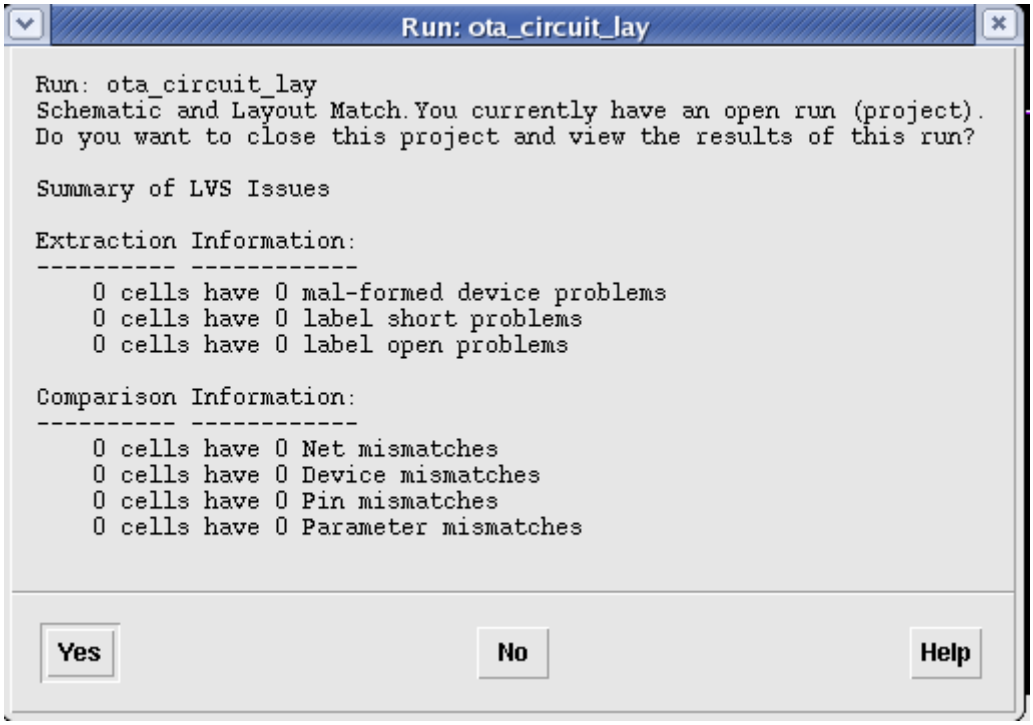

Figure B.3 LVS report of the proposed current subtractor