Design and Analysis of Structurally Engineered Junctionless Field-Effect-Transistor

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OF ENGINEERING & TECHNOLOGY
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submitted by

Sandeep Kumar
(Registration no. 901806020)

Under the supervision of

Dr. Arun Kumar Chatterjee
Assistant Professor (ECED)
TIET, Patiala, Punjab

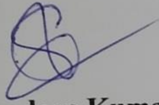
Dr. Rishikesh Pandey
Assistant Professor (ECED)
TIET, Patiala, Punjab

Department of Electronics and Communication Engineering
Thapar Institute of Engineering & Technology
(Deemed to be University)
Patiala, Punjab, India – 147004

(October - 2023)

Declaration

This is to certify that the work which is being presented in this thesis entitled "**Design and Analysis of Structurally Engineered Junctionless Field-Effect-Transistor**," submitted by me to the Thapar Institute of Engineering & Technology, Patiala in fulfilment of the requirements for the award of the degree of **Doctor of Philosophy** is an authentic record of work carried out by me under the supervision of **Dr. Arun Kumar Chatterjee** and **Dr. Rishikesh Pandey**. The contents of this thesis, in full or in parts have not been submitted to any other Institute or University for the award of any degree or diploma.



Sandeep Kumar
Registration No. - 901806020
Department of Electronics and Communication Engineering
Thapar Institute of Engineering & Technology
(Deemed to be University)
Patiala, Punjab, India - 147001

Certificate

THAPAR INSTITUTE
OF ENGINEERING & TECHNOLOGY
(Deemed to be University)

Department of Electronics and Communication Engineering
Thapar Institute of Engineering & Technology, Patiala
(Deemed to be University)

This is to certify that the thesis entitled "**Design and Analysis of Structurally Engineered Junctionless Field-Effect-Transistor**," being submitted by **Mr. Sandeep Kumar**, to the Thapar Institute of Engineering & Technology, Patiala in fulfilment of the requirements for the award of the degree of **Doctor of Philosophy** is an authentic work carried out by him in **Department of Electronics and Communication Engineering** under my supervision. The research reports and results embodied in this thesis have not been submitted in full or in parts to any other Institute or University for the award of any other degree or diploma.

Dr. Arun Kumar Chatterjee
Assistant Professor, ECED
TIET (Deemed to be University)
Patiala, Punjab, INDIA–147001

(Supervisor)

Dr. Rishikesh Pandey
Assistant Professor, ECED
TIET (Deemed to be University)
Patiala, Punjab, INDIA–147001

(Supervisor)

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Abstract

The development of smart computing devices has evolved due to the relentless scaling of conventional MOSFETs. In the nanoscale regime, the MOSFET scaling has reached a physical limit owing to the increased short-channel effects. To unravel the issue of rising short-channel effects the multigate MOSFETs and high-k dielectric materials have been introduced. Nevertheless, the realization of multigate MOSFETs with short-channel dimensions becomes extremely challenging due to the ultra-steep doping concentration gradient at p-n junctions. The fabrication of these ultra-steep p-n junctions has been avoided in the junctionless FET (JLFET) which reflects lesser leakage current and smaller thermal budget in comparison to the conventional multigate MOSFETs. However, as the channel length approaches to sub-20 nm region, the performance of JLFETs degrades too due to poor channel depletion which leads to increased OFF-state leakage current and hence, high static power dissipation with immoderate short-channel effects.

Therefore, this thesis addresses this vital issue of increased OFF-state current in JLFETs by proposing a recessed double gate JLFET (R_DGJLFET) with improved electrical performance. By employing the gate electrode over the recessed silicon channel, a remarkable performance improvement has been achieved with smaller OFF-state leakage current, better ON-to-OFF current ratio, steeper subthreshold slope, and lesser drain-induced-barrier-lowering.

It has been investigated that the proposed R_DGJLFET maintains its performance edge over the conventional counterpart in terms of channel length scaling. The depth and length of the recessed silicon channel have been found as the additional performance tuning parameters. In comparison to conventional double gate JLFET (C_DGJLFET), the proposed device offers similar electrical performance with a larger effective oxide thickness. Additionally, the device reflects optimum and robust performance with smaller variations in subthreshold slope within a range of gate work functions. Besides, the proposed device behaves sturdily against misaligned recessed silicon channel with smaller variations in digital and analog performance parameters.

At the circuit level, it has been investigated that the inverter based on the proposed R_DGJLFET depicts steeper voltage transfer characteristics, wider noise margins, smaller static and short-circuit power dissipation with the desired transient response. Also, the common-source amplifier based on the proposed R_DGJLFET amplifies a small signal within a wide frequency range.

Moreover, to enhance the physical insight into the device operation a potential-based analytical drain current model has been developed for the proposed R_DGJLFET. The effect of various design parameters affecting the potential profile and drain current in the device have also been considered. It has been found that the model results agree with the simulation results in a close manner.

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List of Abbreviations

AFM	Atomic force microscopy
BJT	Bipolar junction transistor
BTBT	Band-to-band-tunneling
BTI	Bias temperature instability
C_DGJLFET	Conventional double gate junctionless field-effect-transistor
CMOS	Complementary metal-oxide-semiconductor
CP	Charge-plasma
CS	Common-source
CS_DGJLFET	Core-shell double junctionless field-effect-transistor
CV	Charge-voltage
DG	Double gate
DGM	Dual gate material
DIBL	Drain-induced-barrier-lowering
DRAM	Dynamic random-access-memory
EOT	Effective oxide thickness
FET	Field-effect-transistor
GAA	Gate-all-around
GBW	Gain bandwidth product
GFP	Gain frequency product
GIDL	Gate-induced-drain-leakage
HCE	Hot-carrier-effect
IC	Integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
IM	Inversion mode
IRDS	International roadmap for devices and systems
ITC	Interface trapped charges
JLFET	Junctionless field-effect-transistor
JLT	Junctionless transistor
LAO	Local anodic oxidation
L-BTBT	Lateral band-to-band-tunneling
LER	Line edge roughness
MOSFET	Metal-oxide-semiconductor field-effect-transistor
NBTI	Negative bias temperature instability

NC	Negative capacitance
NM	Noise margin
PPA	Parabolic potential approximation
QCE	Quantum-confinement-effect
R_DGJLFET	Recessed double gate junctionless field-effect-transistor
RDF	Random dopant fluctuation
RF	Radio frequency
RO	Ring oscillator
RT	Retention time
SCE	Short-channel-effect
SOI	Silicon-on-insulator
SPICE	Simulation program with integrated circuit emphasis
SRAM	Static random-access-memory
SRH	Shockley-Read-Hall
SS	Subthreshold slope
TAT	Trap assisted tunnelling
TCAD	Technology computer added design
TFET	Tunneling field-effect-transistor
TFP	Transconductance frequency product
TG	Tri-gate
TGF	Transconductance generation factor
TPV	Trench process variation
VST	Variable separation technique
VTC	Voltage transfer characteristics
WFW	Work function window
WKB	Wentzel-Kramers-Brillouin

Chapter-1
Introduction

The insatiable wish to make the day-to-day life of human beings easier and more comfortable has contented the development of smart electronic gadgets such as mobile phones, laptops, smart watches, etc. The quality features of these electronic gadgets demand continuous improvement in the speed and computing power of the integrated circuits (ICs) embedded inside.

1.1 Device scaling

The need for more and more computational functionality in the same chip area of ICs has been fulfilled by considering the metal-oxide-semiconductor field-effect-transistor (MOSFET) as the mainstream component and remains the key reason for the device scaling [1]. The scaling results in the systematic miniaturization of MOSFETs with the goal of enhanced performance, smaller transistor area, and lower active power [2].

The semiconductor industry has faced several challenges in the scaling of MOSFETs such as (a) the requirement of improved lithography and ion-implantation technics (b) improved MOSFET design for enhanced performance (c) the introduction of novel materials and structures including silicon-on-insulator (SOI), high-k dielectrics, metal gates, and strained silicon (d) increased circuit sensitivity to the soft errors from radiation (e) on-chip interconnections with a smaller cross-section (f) device reliability and circuit stability (g) denser on-chip memory segments and (h) affordable capital cost.

However, the electrostatic integrity of MOSFET has been preserved with preceding the device scaling in a controlled manner. For instance, with a reduction in gate length (L_G), the thickness of gate dielectric (t_{ox}) has to decrease along the source/drain junction depth (t_j), supply voltage (V_{DD}), and gate width (W_G) by a factor $\alpha > 1$ (typically $\sqrt{2}$), while the doping concentration (N_D or N_A) needs to be increased by α so that the electric field strength in scaled MOSFET remains constant as that of the original device, known as *constant field scaling* [3] [4].

1.1.1 Effect of scaling on device physics

As the device dimensions have been made smaller, the length of depletion region at the source/drain-channel edge becomes equivalent to the gate length, called the *short-channel device*. In short-channel devices, the leakage power dissipation increases significantly due to various undesired physical mechanisms called *short-channel effects* (SCEs) e.g. threshold voltage (V_{TH}) variations, hot-carrier-effect (HCE), velocity saturation, etc. [5], [6].

Consequently, the SCEs results in degraded gate control over the channel and do not let the device OFF completely which allows a flow of leakage current hence, power dissipation occurs even when the voltage on the gate terminal is not changing. Decisively, the MOSFET scaling impacts the device physics which governs its electrical behaviour.

One way to address the increased SCEs is to highly dope the channel [7]. Alternatively, various MOSFET devices with multi-gate structures have been proposed in the literature. In multi-gate MOSFETs, an increased number of gates share the channel region to be depleted and hence, results in improved gate control with better subthreshold slope (SS) closer to 60 mV/dec. The SOI double gate (DG) FinFET [8] provides the flexibility to be used as a double gate device with a thicker hard mask which ceases the effect of gate material in the top layer over the fin region. The gate controllability can further be improved by keeping the dielectric thickness equal on all three or four sides i.e. SOI tri-gate (TG) FinFET [9], SOI based Π-gate FinFET [10], Ω-gate FinFET [11], gate-all-around nanowire (GAA) with rectangular and circular cross-section and bulk-TG FinFET [12] respectively.

However, with undesired parasitic effects such as capacitance between source/drain and substrate, latch-up phenomena, and radiation hardening, the bulk FinFET technology is not as popular as that of SOI based FinFETs [8]. The multi-gate structures allow relaxed channel dimensions due to better gate control which improves the total current derive in proportion to the gate width. However, increasing the number of gate electrodes results in higher gate capacitance, which results in slower device switching along with increased fabrication complexities in patterning the gate electrode around the silicon fin [8].

1.1.2 Effect of scaling on power dissipation

In addition to the need for improved gate influence across the channel region to alleviate the SCEs, the implication of increased power dissipation has also been boiled up in the short-channel devices while addressing need for more and more logic functionality on a chip area as predicted by International Roadmap for Devices and Systems (IRDS) [13]. Moreover, as notified in IRDS 2020 the power reduction rate leans to be flattened due to the slow scaling of supply voltage [14]. As the basic component in complementary metal-oxide-semiconductor (CMOS) technology, the development of a nanoscale MOSFET with novel materials and structures for minimum power dissipation has been the ultimate demand of various hand-held devices in today’s consumer market. Among the two different mechanisms of power dissipation namely the static or leakage power and dynamic power, the latter dominated the overall power dissipation in the late 1990s [6]. However, with the advancement of technology, the dynamic power dissipation starts lowering due to a reduction in gate capacitance of nanoscale devices. Mathematically, the static power dissipation (P_{SC})

can be expressed as the product of subthreshold leakage current (I_{Sub}) flowing in the device for zero gate-to-source voltage (V_{GS}) with maximum power supply voltage (V_{DD}) as given in Eq. 1.1 [1].

$$P_{SC} = I_{Sub} \times V_{DD} \quad (1.1)$$

Therefore, scaling of modern MOSFETs has been emphasized for reducing the power dissipation dictated by its static component. The static power dissipation can be slashed with the reduction in voltage supply but is not popular as the subthreshold slope (SS) starts degrading. This infers that the miniaturizing the MOSFETs to the sub-20 nm scale would result in higher power dissipation due to increased SCEs which would ultimately lead to an increased temperature of various handheld devices and laptops etc. [6], [15]. Therefore, the search for a highly scalable MOSFET with increased power efficiency is still desirable.

1.1.3 Effect of scaling on device fabrication

Moreover, the source/drain regions in MOSFET are processed with a high doping concentration of ~10^{20} cm^{-3}. Whereas, the doping in the channel region changes abruptly to ~10^{15} – 10^{17} cm^{-3} with the opposite type of dopant atoms [16]. However, in short-channel devices, realizing the p-n junctions at source/drain-channel edges with such abrupt profiles is extremely challenging as shown in Figure 1.1.

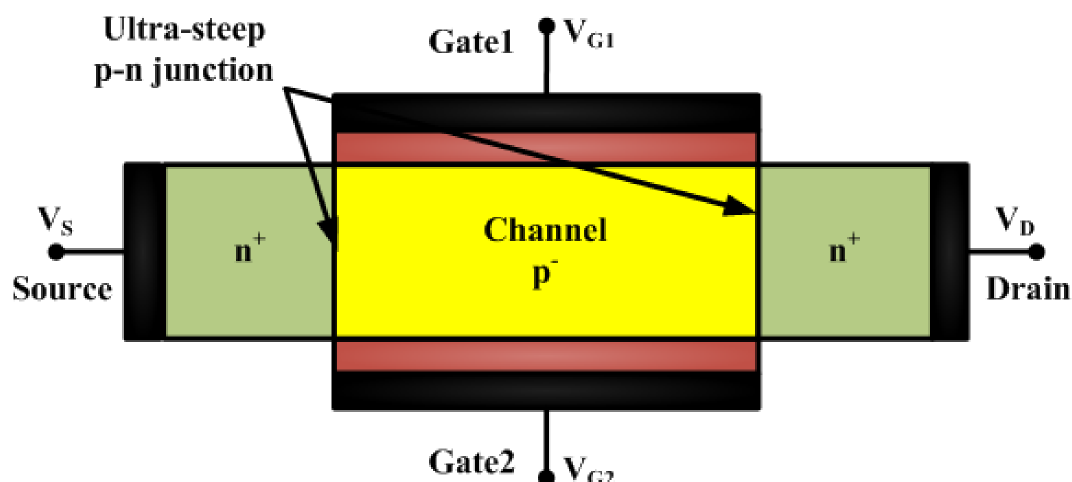


Figure 1.1 Two-dimensional view of conventional n-type double gate MOSFET [16].

This is because of the stochastic distribution of dopant atoms obtained from ion implantation which results in a doping gradient of 2-3 nm/dec [16]-[18]. This implies that changing the doping concentration from ~10^{19} cm^{-3} to 10^{17} cm^{-3} will take ~10 nm of a channel region which equals the effective channel length in the sub-10 nm regime.

Besides, a compulsory post-ion-implantation annealing step for electrical activation of dopant atoms results in diffusion of impurities from the source/drain to the channel which also curtails the probability of fabricating the p-n junctions with an ultra-steep profile for nanoscale devices [16]-[18]. Recently, great relief from fabricating the nano MOSFET with

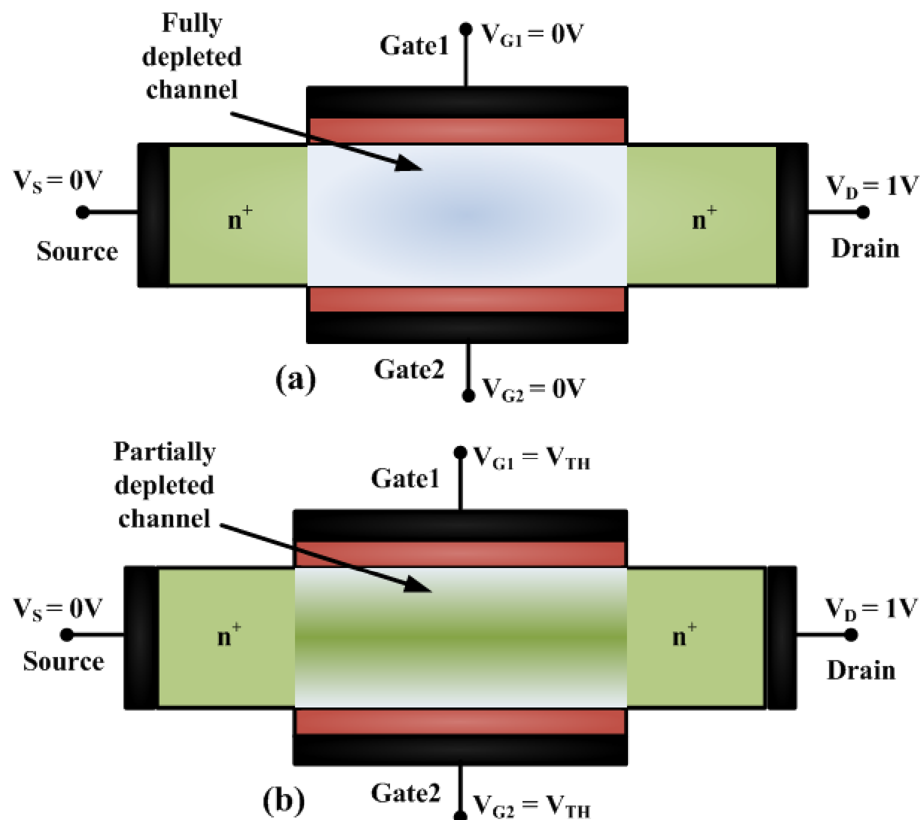
ultra-steep p-n junctions has been obtained with the introduction of a state-of-the-art device without junctions called, junctionless field-effect-transistor (JLFET) or gated resistors [18]. The device utilizes a uniformly doped semiconductor layer from the source to drain region. Gate stacked over the semiconductor layer is used to tune the channel resistance and eventually the flow of current [16-19]. In the following section, this emerging device based on its transport mechanism has been discussed.

1.2 The junctionless field-effect-transistors

The JLFET has been realized without any p-n junction by utilizing a heavy uniformly doped semiconductor layer from source to drain end with typical values of dose from 8×10^{18} cm^{-3} to 8×10^{19} cm^{-3}. The flow of current between the drain and source is controlled by the gate electrode that electrically controls the existence of charge carriers in channel [16-20].

1.2.1 The working principle of JLFETs

The JLFETs based on various multi-gate structures have been reported in the literature. But, the fundamental working principle for all JLFETs remains the same. The entire silicon film is uniformly n-type doped i.e. source and drain are not differently doped from the channel. However, the channel remains in *full depletion* for $V_{GS} = 0$ V as shown in Figure 1.2(a). The gate work function decides the quality of channel depletion achieved in the OFF-state and induces the electrostatic field in such a way that the charge carriers move away from the channel to its adjacent source/drain region [18].



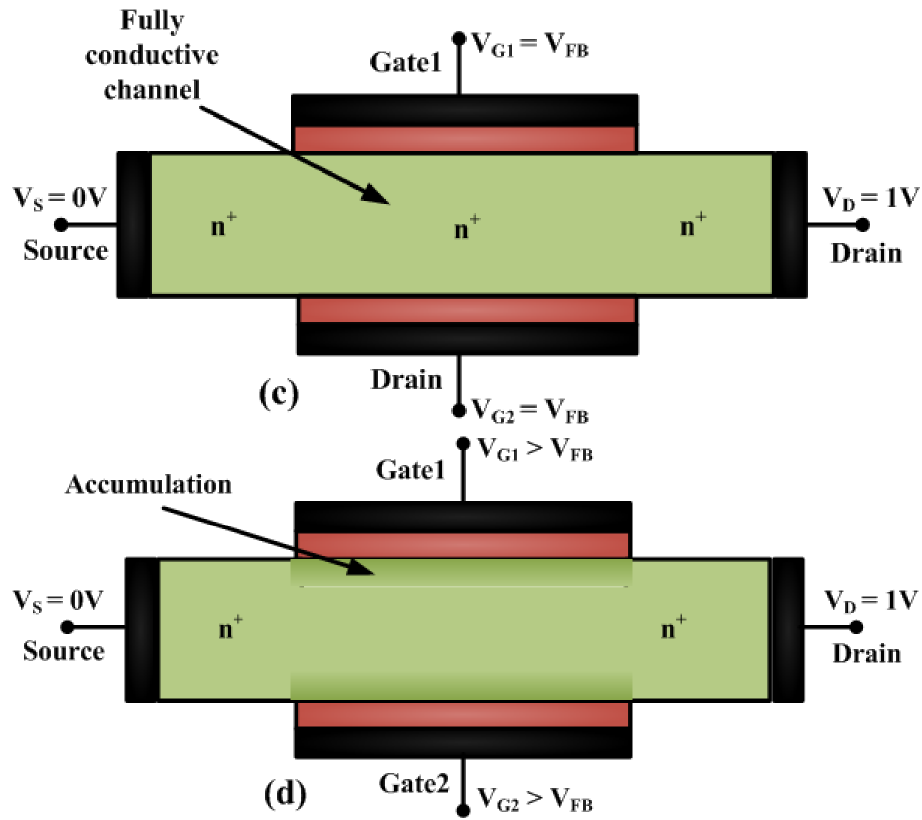


Figure 1.2 Various operating regions for DG JLFET: (a) full depletion region (b) partial depletion region, (c) flat band state, and (d) accumulation state [18].

However, increasing the gate voltage to positive values leads to a reduction in the width of the depletion region across the channel caused by moderated electric field. This allows the uncovering of the neutral region and the charge carriers start coming into the channel. At a particular gate voltage known as *threshold voltage*, a conductive path is formed at the central part of the channel called *bulk conduction*.

Increasing the V_{GS} further enhances the neutral region in the channel which leads to an increased number of charge carriers and hence, more current flows in the semiconductor layer called *partial depletion* [18] as revealed in Figure 1.2(b). At a particular value of V_{GS}, the entire channel becomes neutral i.e. conductive and the depletion region disappears from the channel region called *flat band state* [18] as shown in Figure 1.2(c).

Beyond flat band state, any further increase in V_{GS} causes a slight increment in drain current as the whole channel is already conducting and the extra charge accumulates near the surface underneath the gate dielectric called *accumulation state* [18] as shown in Figure 1.2(d). The JLFETs have been designed to operate in OFF and ON-state in full depletion and flat band conditions, respectively.

1.2.2 The design flow for JLFETs

The operation of conventional junctionless FET is governed by the mutual dependence of three design parameters namely gate electrode work function (Φ_G), thickness of silicon film(t_{si}), and doping density of semiconductor film (N_D) as shown in Figure 1.3.

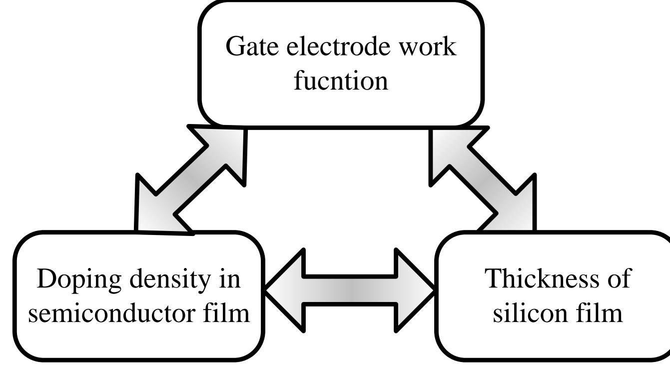


Figure 1.3 Design flow for conventional junctionless FETs.

In OFF-state, the gate electrode work function causes the depletion of charge carriers in the underlying silicon layer. The full depletion of the channel is achievable only if the thickness of the induced depletion region is greater than the semiconductor film thickness. Hence, to achieve full depletion ultrathin silicon film is used in junctionless devices. But, the ultra-low thickness of silicon film rsults in smaller channel zone for the movement of charge carriers, which leads to the lowering of ON-current (I_{ON}) in the conventional junctionless device as given in Eq. 1.2 [18].

$$I_{ON} \approx q\mu_n N_D \frac{t_{si}.W_{si}}{L_G} V_{DD} \quad (1.2)$$

where q symbolizes the charge of an electron, μ_n is the electron mobility, W_{si} represents the width of the silicon film and V_{DD} denotes the power supply. From Eq. 1.2 it is clear that to overcome the loss of current due to ultrathin silicon film, N_D should be increased [18]. But heavy silicon film doping results in more charge carriers in the channel which again weakens the depletion [21]. Hence, tuning of Φ_G becomes critical for zero V_{GS} to achieve efficient depletion in ultrathin and heavily doped silicon film [18, 22]. In double gate junctionless FET, the entire silicon film can be depleted if the depletion region width becomes equal to or greater than half of the channel thickness.

Alternatively, Φ_G can be used effectually to expand the depletion region width in OFF-state without decreasing the thickness of silicon channel. Hence, for achieving the full depletion in the JLFETs the combinations of gate work function, silicon layer thickness, and silicon doping concentration must be selected carefully. Moreover, the design of a JLFET can be started by fixing two of the three parameters and the remaining parameter can be varied to achieve the desired performance.

1.2.3 Pros and cons of JLFETs

The prominent features of JLFET include its compatibility with the existing CMOS fabrication technology [18]. A smaller number of process steps are required due for removal of p-n junctions in the silicon layer as a result the post-ion-implantation annealing process is absent which leads to a smaller thermal budget [23]. This gives more freedom to the device engineer to play with gate metal and gate dielectrics. The JLFETs show better control over the SCEs with reduced drain-induced-barrier-lowering (DIBL) [18], smaller SS, and lesser OFF-state leakage current which enhances the device scalability [24]. Many JLFETs with different V_{TH} can be fabricated on single-chip by just changing the device's width [25]. Besides, unlike the conventional MOSFET in which the I_{ON} flows at the surface only, the JLFET reflects bulk conduction as the major part of the total current flowing is separated from the semiconductor's surface with a depletion region. The device can also be fabricated with high-mobility materials such as Germanium, InAs, etc. [26]. Since the JLFETs are biased in flat band mode for operating in ON-state, hence, the lesser electric field across the channel is present in the semiconductor layer due to which the device shows better immunity against HCEs [27], lesser venerability against bias temperature instability (BTI) [28] and reliability issues [26]. Due to the homogenous doping and bulk conduction mechanism, the JLFETs also show better noise performance in comparison to conventional MOSFETs. The flicker noise (1/f) is also smaller in JLFETs comparatively [29].

However, with many aforementioned assets, the JLFETs also have some challenges as well. The JLFETs have been found as more sensitive to the process and temperature variations as compared to conventional MOSFETs [30]. The heavy doping in the semiconductor layer results in random dopant fluctuation effects which significantly affect the device's robustness with variations in V_{TH} and SS [31]. To obtain a considerable value of ON-current, the heavy doping in the semiconductor layer results in poor channel depletion which causes an increament in leakage current [32]. The doping density of the source/drain region (~10^{19} cm^{-3}) results in higher series resistance in JLFET which leads to smaller I_{ON} and transconductance (g_m) than that of conventional MOSFET devices [30]. In the case of non-planar JLFETs, the requirement of ultrathin (~10 nm) and heavily doped semiconductor layer also presents strict process challenges [31].

1.2.4 Circuit applications based on JLFETs

The simpler process sequence to realize the JLFET and smaller leakage current makes it a popular choice for CMOS circuit applications. The device has been used to implement various CMOS circuits in both digital and analog domains such as memory cells [34-37], digital logic gates [38-39], common-source amplifiers [40], and ring oscillators [39][41], etc.

Smaller static power dissipation, comparable switching speed, improved g_m, and maximum oscillation frequency (f_{max}) have been reported with JLFET based circuits [36-37][39]. The excellent performance shown by JLFETs at the circuit level establishes it as an emerging solution for low-power applications [41-43].

1.2.5 Modeling of drain current in JLFETs

The fabrication of an electronic device is an expensive task used for characterizing and understanding the physic working behind its operation. It requires special manpower working in a sophisticated environment for a large number of hours. An alternative way to understand the behaviour is to design and simulate the device using technology computer aided design (TCAD) tools which also require specially trained manpower to generate the desired outputs. Instead, to understand the effect of various external voltages on the device conduction is to work on and develop a mathematical tool called an *analytical model*. The analytical model helps to develop insights about the device's working principle without the requirement of any TCAD tool. The device modeling also shortens the device design time which is highly important in today's competitive market. However, the accuracy of the developed analytical model is crucial as it aids to comprehend the non-linear conduct of MOSFETs.

The JLFETs have also been focussed from the modeling perspective in various national and international institutes worldwide. People in the research community have mainly used surface-potential and charge based modeling approaches to formulate the subthreshold and full-range analytical/compact models. Sallese *et al.* [44] have developed a charge based analytical model for double-gate JLFETs. Duarte *et al.* [45] have presented a compact drain current model for of JLFETs for full operating range. Gnudi *et al.* [46] have developed a semi analytical subthreshold drain current model for short-channel double gate JLFETs. Hur *et al.* [47] have developed a compact model for multiple-gate JLFETs. Baruah *et al.* [48] have formulated a surface-potential based analytical model in the subthreshold region for drain current in short-channel double-gate JLFET. Kumari *et al.* [49] have modeled double gate JLFET while considering the effect of fringing fields. Chanda *et al.* [50] have considered the impact of quantum confinement in developing the analytical model of nanoscale JLFET. Verilog-A compatible have also been developed for double gate and gate-all-around junctionless devices [51]. The modeling efforts for the junctionless device from different parts of the world continue till now and have been detailed in Chapter 2.

1.3 Motivation behind the work

A variety of structures have been focused on by the various researchers for the JLFETs such as single-gate JLFET, DG JLFET, TG JLFETs, and GAA junctionless nanowires [8-12][31][52-53]. However, in this work, the symmetric double gate JLFET has been

considered as this structure helps to suppress the SCEs with better gate controllability which improves the device scalability. The structural symmetricity also helps to achieve a better quality of channel depletion in OFF-state. The double gate structure also provides the flexibility of tuning the device performance by operating in an asymmetric mode which is completely absent in other multi-gate structures [53] and can be used to implement a logic function with two inputs or in frequency mixing applications. Also, increasing the number of gate electrodes leads to higher gate capacitance which eventually limits the device's performance in ON-state. The double gate structure does not require engineering of the extension region of source/drain and effectively controls the SCEs [54].

Moreover, as the channel length advances in the sub-20 nm regime, the advantage of improved gate control with multigate structures fades as the performance of conventional JLFET starts overwhelming owing to feeble gate control across the channel region. This leads to inefficient depletion of the semiconductor layer. Eventually, it promotes the increased SCEs in the device with higher DIBL and degraded SS. The interaction of the source with the drain end outcomes in a higher leakage current through the device which leads to more static power dissipation. Hence, one of our motivations is the reduction in leakage current by improving the influence of gate electrode in OFF-state. It has also been found that the junctionless device is more susceptible to the variations induced by fabrication process. One such important aspect related to double gate structure is the precise alignment of both gate electrodes. Proposing a robust JLFET which shows lesser variations in performance is also a challenging task. Furthermore, developing the analytical model to enhance the physical insight and verifying the device performance in various circuit applications is equally important. The presented work in this thesis tries to address these issues.

1.4 Thesis organization

The research investigations in this thesis have been ordered in the subsequent means.

Chapter 1: **Introduction**

This chapter describes the need and strategy for scaling the conventional MOSFET. The effect of scaling on device physics, power dissipation, and fabrication process of short-channel devices has been discussed with existing solutions. The working principle of conventional junctionless FET (JLFET) has been presented while briefly introducing the status of its circuit applications and modeling efforts made worldwide. The motivation of the present work has also been illustrated.

Chapter 2: Literature survey

This chapter discusses the literary background of the JLFETs from different angles like the study of various physical phenomena in the JLFETs, technological advancements for

boosting the device performance, developed analytical/compact models, circuit applications in both digital and analog domains presented so far in the literature.

Chapter 3: Proposed recessed double gate JLFET

This chapter presents the proposed device structure and the effect of variations in different technological parameters such as channel length, depth, and length of recessed silicon area, effective oxide thickness, and gate electrode work function in both symmetric and asymmetric modes on the device performance has been investigated. The study is further extended while studying the effect of misalignment on various performance parameters of the proposed device.

Chapter 4: Proposed recessed double gate JLFET based digital logic gates

In this chapter the proposed JLFET based digital logic gates namely NOT, NAND, and NOR gates have been implemented. The DC, transient, and power analysis of the inverter based on the proposed recessed double gate JLFET has been performed. A popular analog block namely a common-source amplifier based on the proposed device has also been implemented.

Chapter 5: Analytical modeling of proposed recessed double gate JLFET

In this chapter, the potential based analytical model has been developed for the proposed recessed double gate JLFET in the subthreshold region. The results obtained from the analytical model have been validated with TCAD simulation results. The effect of different design parameters such as L_G, N_D, EOT, and Φ_G have also been incorporated.

Chapter 6: Conclusions and future scope

This chapter summarizes the overall conclusions leading from the presented research work. The future scope of the current work has also been mentioned.

Chapter-2
Literature survey

2.1 Introduction

The JLFETs have been introduced with no p-n junctions between the source/drain and the channel region. These devices offer fabrication simplicity, a smaller leakage current, and better control over the SCEs in comparison to conventional inversion mode (IM) devices.

In this chapter, various elemental parts necessary to understand the larger concept of the fundamentals of physics and technology for JLFETs have been presented. The recent state-of-the-art in junctionless devices with different types of structural modifications such as spacer engineering, gate engineering, and channel engineering have been reviewed. The developed analytical models for different types of JLFETs have been analyzed. Furthermore, performance of JLFET in various digital and analog circuits have been discussed.

2.2 Study of physical phenomena in JLFETs

In literature, the effect of physical phenomena and properties such as temperature, electric field, random dopant fluctuations (RDFs), line edge roughness (LER), lateral band-to-band tunneling (L-BTBT), series resistance, hot carrier effects (HCEs), low-frequency noise on the electrical behaviour of JLFETs have been studied by various researchers. The journey of JLFETs start long back ago in the year 1930, when J. E. Lilienfeld has been granted a patent on “gated trans-resistors” by the United States Patent Office aimed at demonstrating the idea of “field-effect” with an apparatus for controlling the electric currents flowing between two terminals of a conducting bar by inducing a potential from the third terminal [55].

However, based on this concept, in 2009, Lee *et al.* [17] presented a simulation study on the concept of a MOS transistor with no p-n junctions as shown in Figure 2.1. The authors have reported that the junctionless transistor offers easier fabrication and reduced variability than the conventional MOSFET.

In the same year, Colinge *et al.* [56] at Tyndall National Institute had experimentally produced the first SOI based n+ and p+ junctionless nanowires/nanoribbons of length 1 μm and width 30 nm and characterized with full CMOS functionality. The authors have experimentally confirmed that the JLFETs offer near-ideal SS at room temperature, lower leakage current, and smaller mobility degradation with increased V_{GS} in comparison to regular CMOS devices. Lee *et al.* [57] have demonstrated the electrical performance of SOI based multigate junctionless nanowires. With a smaller value of SS and DIBL the multigate JLFET reflects outstanding current-voltage (I-V) characteristics.

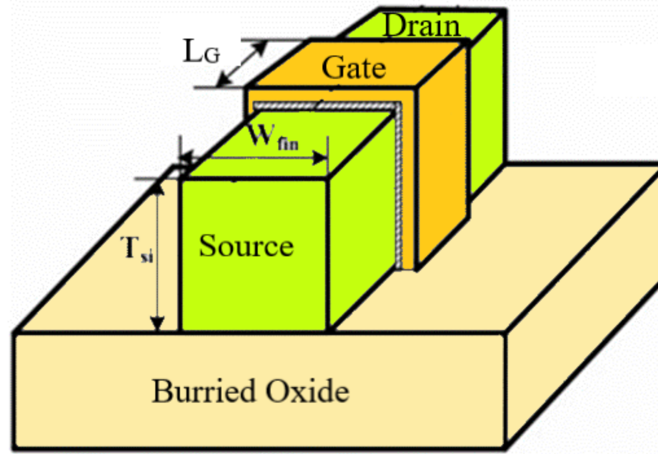


Figure 2.1 Bird's eye view of SOI based multigate junctionless FinFET (The gate length, fin width, and fin thickness have been labeled) [17].

In successive years various studies on the different physical phenomena have been published in the literature. Colinge *et al.* [58] have observed the presence of maximum electron concentration in the region of ~10 times smaller electric field (E<0.02 MV/cm) in nanowire JLFET as that of IM device which may be advantageous in terms of the current drive at the nanoscale. The lesser value of the electric field also results in a smaller rate of reduction in mobility with an increase in V_{GS} comparatively.

Koukab *et al.* [59] have studied the scaling performance of junctionless devices. The authors have shown that the JLTs are very similar in terms of speed of operation to the bulk MOSFETs. Also, the JLFETs require thinning of gate dielectric to increase the drive current and operating speed like the regular MOSFETs.

Lee *et al.* [30] have investigated the electrical performance of silicon nanowire JLFET in a temperature range from 30°C to 200°C. The paper describes that junctionless devices with an increase in temperature mobility reduce at a slower rate and do not compensate for the reduction in V_{TH}, leading to a monotonous rise in I_D. Moreover, it has also been pointed out that the absence of an ion-implantation step to realizing the heavily doped source/drain region diminishes the defect density in junctionless FETs which leads to a smaller gate-induced-drain-leakage (GIDL).

The need for good I_{ON} necessitates a heavily doped silicon layer in junctionless devices [56], which leads to performance fluctuations. Leung *et al.* [60] have shown that the V_{TH} and leakage current varies significantly in heavily doped nanoscale junctionless FinFETs (N_D >10^{19} cm^{-3}) due to RDFs as compared to inversion mode counterparts. Giusi *et al.* [61] have investigated the drain current variability due to RDFs in DG JLFET. The authors have found that the drain current disperses lower in the ON-state than that in OFF-

state. The variability in drain current and threshold voltage increases with the rise of SCEs. Sahu *et al*. [62] have reported that the undoped DG junctionless transistors (JLT) reflect lesser sensitivity against RDFs and variations in the gate and spacer lengths in comparison to heavily doped junctionless FET.

Gundapaneni *et al*. [63] have evaluated the effect of band-to-band tunneling (BTBT) on the OFF-state performance of n-type JLT. The authors have observed the significant band overlapping in the lateral direction which results in a parasitic bipolar junction transistor (BJT) action in the device and facilitates the tunneling of electrons from the valence band of the channel to the conduction band of the drain. This leads to increased BTBT current or GIDL and contributes to the overall I_{OFF}.

Sahay *et al.* [64] have demonstrated that the diameter dependency of I_{OFF} is governed by the lateral (L)-BTBT phenomenon of the nanowire JLFETs. The authors have shown that for nanowire JLFETs with a diameter of ≤ 10 nm, the DIBL gets reduced due to increased gate control which in turn increases the energy barrier height at the source-channel interface and leads to diminished BTBT effect and smaller I_{OFF}.

Wan *et al*. [65] have presented a solution for reducing the effect of LER magnitude with charge-plasma based doping less JLT by patterning the S/D metal with suitable Φ_G in lateral and top position over the high-k dielectric. In this paper, it has been shown that the proposed device reflects smaller fluctuations in I_{ON}, I_{OFF}, SS, and V_{TH} in comparison to conventional JLT.

Doria *et al*. [66] have presented that junctionless transistor (JLT) reflects higher series resistance (R_S) than the IM device due to lower doping concentration in the source and drain. The study suggests a length of underlap region towards source/drain ($L_{SD} \leq 10$ nm) for short channel JLT to obtain a similar behaviour of R_S with a reduction in temperature as that of IM counterpart.

Lee *et al*. [67] have investigated the effect of back gate bias device degradation due to HCE in multiple gates JLT. In this paper, it has been concluded that the drain current decreases with past hot carrier stress and the impact is more significant in JLTs due to higher sensitive interface coupling than that of IM counterparts.

Singh *et al.* [68] have presented that n-type GAA junctionless nanowire FET reflects lesser low-frequency noise concerning N_D and V_{GS}. The superior low-frequency noise behaviour has been attributed to the carrier's conduction in a uniformly doped channel.

Ghosh *et al.* [41] have demonstrated excellent analog performance with JLT for a drain current of 30 μA/μm. The authors have attributed the enhanced A_V and V_{EA} to a smaller electric field peak at the gate edge on the drain side.

Moreover, with these pros and cons, the performance of conventional JLFETs has been further boosted with different types of structural modifications focusing on the spacer, gate material, gate dielectric, channel, and misalignment, which have been discussed in the following section.

2.3 Performance boosters for JLFETs

As described in section 2.1, the JLFET offers multiple advantages over the conventional IM MOSFET. However, the scaling limitations with increased I_{OFF}, higher DIBL, degraded SS, etc. have commanded the introduction of performance boosters for conventional JLFET in the literature. The physical engineering based on spacer dielectric, gate dielectric, gate material, channel length, doping concentration, and misalignment in the conventional JLFET has a significant impact on its performance parameters.

2.3.1 Research status of spacer engineering in JLFETs

Gundapaneni *et al.* [69] have proposed a way of strengthening the electrostatic integrity of a JLT in the sub-22 nm regime using high-k spacer material. In this paper, it has been shown that the use of HfO_2 as spacer material results in increased effective channel length which leads to smaller I_{OFF} in JLT. However, the study did not discuss the effect of high-k spacer material on the variability and dynamic performance of the device.

Baruah *et al.* [70] have investigated the effect of a high-k spacer on digital and analog performance parameters of a DG JLFET with a gate length of 20 nm in the 2-D Atlas device simulator. The study reveals that the use of high-k spacers leads to smaller I_{OFF} and improved I_{ON}/I_{OFF} current ratio with a minor reduction in I_{ON}, higher intrinsic gain (A_{V0}) and trans generation factor (TGF) and reduction in output conductance (g_{ds}) with lowering of unity gain-frequency (f_T).

Saini *et al.* [71] have shown the benefits of using a combination of high-k and low-k spacer material for improved analog and radio frequency (RF) performance of JLFET such as g_m, g_{ds}, TGF, f_T, f_{MAX}, and A_{V0} comparatively which has been attributed to the increased electron transport efficiency due to extra peak of the electric field in the proximity of source region.

Yang *et al.* [72] have addressed the performance optimization of ultrashort GAA JLFET in the ballistic regime using high-k spacer material. The authors have suggested that using a high-k spacer with k >12 can lead to suppressed performance variation of GAA JLFET in the ballistic regime while keeping a note of surface roughness scattering.

2.3.2 Research status of gate material/gate dielectric engineering in JLFETs

Moving to the effect of variations in gate material on the performance of JLFET, Lou *et al.* [73] have proposed nanowire JLT with dual gate material (DGM). The authors have

presented that the two peaks of the electric field in DGM based JLT with a reduced peak near the drain side facilitate the suppression of SCEs and HCEs. The peak of the electric field near the source region promotes electron acceleration and results in 3 times higher electron velocity than the single gate material based JLT which eventually leads to higher I_{ON} with improved g_m.

Baidya *et al*. [74] have explored the use of high-k gate dielectric material in JLT for better g_m, TGF, g_{ds}, and A_{V0}. However, the authors have pointed out that the increase in gate capacitance nullifies the enhanced g_m, which results in constant f_T. Moreover, the authors suggest that a lower Φ_G is beneficial except for increased V_{TH} and high-k gate dielectric is advantageous for better analog performance of JLT.

Tayal *et al*. [75] have investigated the effect of variations in channel thickness on the analog performance of a high-k gate stack-based tri-gate junctionless FinFET with mixed mode simulation in the Santaurus TCAD tool. In this paper, it has been shown that f_T, f_{MAX}, and A_{V0} degrade with increasing the k-value from 3.9 to 40 which gets more pronounced with a reduction in t_{si}. The authors have recommended the larger thickness of the interfacial layer in high-k gate stacked JLFETs with smaller t_{si}.

Lou *et al*. [76] have presented a numerical simulation study by considering the effect of sidewall angle and gate overlap on the performance of three JLTs with a different type of recessed gates called gate-over, gate-out, and gate-in configurations. The study reveals that for a silicon thickness of 12 nm, the gate-over configuration reflects superiority over the other two architectures with I_{OFF} of the order of 10^{-11} A/μm, SS of 79 mV/dec, and DIBL of 36 mV V^{-1}. However, an increased value of sidewall angle results in higher V_{TH} with a further reduction in I_{OFF}.

Ajay *et al*. [77] have used the concept of recessed in conventional DG JLFET with a 16 nm gate length which is greater than the length of the recessed channel region. With an increased energy barrier, the device reflects good digital and analog performance through smaller I_{OFF}, better I_{ON}/I_{OFF} ratio, g_m, f_T, f_{MAX}, etc.

Kumar *et al*. [78] have presented a TCAD tool-based analysis of black phosphorous recessed channel junctionless FET as a bio-sensor. The study reveals that the accumulation of various bio-molecule inside the nanocavities embedded in the gate-insulating layer leads to a change in the gate capacitance which eventually modulates the V_{TH}. The authors have recommended the device for the early detection of protein-related diseases due to its higher sensitivity.

Mehta *et al*. [79] have demonstrated that the internal gate in negative capacitance (NC) based JLFET induces the channel depletion more efficiently and allows the lowering of gate metal

work function to mid-gap values. With the mid-gap work function for gate electrodes, the NC based JLFET reflects reduced I_{OFF} with improved I_{ON}.

2.3.3 Research status of channel engineering in JLFETs

In literature, the channel region has also been targeted to play with various performance parameters of JLFET. The effect of variations in different device design parameters such as doping concentration along/across the channel, thickness, and length of the channel, etc. have been evaluated.

Gundapaneni *et al.* [80] have shown smaller leakage current due to a reduction in effective silicon layer thickness in comparison to SOI based JLT. In bulk planar JLT, the oppositely doped silicon substrate helps to deplete the device silicon layer from top-to-bottom surface which leads to lesser leakage in OFF-state.

Kumar *et al.* [81] have presented that taking the hybrid channel with a p+ layer under the n+ active layer in JLFET results in suppression of bipolar junction transistor (BJT) action induced due to BTBT. The inclusion of the p+ layer leads to increased tunneling width of electrons which causes a reduction in I_{OFF}. Moreover, the authors have shown that the proposed device allows improvement in ON-current with higher silicon thickness.

Chen *et al.* [82] have proposed a channel-engineered JLFET with a graded doping profile. The proposed device consists of a very high doping concentration of 2.5×10^{19} cm^{-3} near the drain in comparison to 2.0×10^{19} cm^{-3} in the remaining silicon layer. The graded doping profile results in an extra electric field peak in the middle part of the channel region which enhances the electron velocity near the source. The overall effect has been observed in improved f_T and A_{V0}.

Song *et al.* [83] have reported that the step doping profile with high/low concentration near the surface/core in JLTs leads to smaller effective fin width which results in smaller V_{TH}, a better I_{ON}/I_{OFF} ratio with improved immunity against the SCEs.

Park *et al.* [84] have analyzed that triangular-shaped fins based JLFET can show smaller variations in V_{TH} and doping concentration due to stronger coupling between the gates and channel in comparison to rectangular-shaped fins based JLFET which arises due to smaller sidewall angle and higher effect of sidewall gate at the bottom part of the channel.

Sahu *et al.* [85] have proposed the novel concept of doping less charge-plasma (CP) based JLT with a channel length of 15 nm. In this paper, the authors have illustrated that, unlike the conventional JLT, the source/drain contact has been induced electrically in the intrinsic silicon body which makes it more immune against process variations, RDF, and mobility degradations.

Kumar *et al.* [86] have investigated the impact of doping profile in shell region for a JLFET with an intrinsic core using numerical simulations. The authors have shown that the proposed structure depicts a smaller leakage current. However, the junction depth of less than 2 nm accounts for a penalty in terms of I_{ON}.

Sahay *et al*. in [32] have proposed the oppositely doped core-shell based nanowire JLFET. In this paper, it has been presented that the p^+ type core allows more depletion at the drain end which results in a simultaneous increase of tunneling width and barrier height at the source-channel side. The increased tunneling width results in suppressed L-BTBT component which diminishes the parasitic BJT action and improves the channel depletion in the device. Hence, leading to a considerable lowering in I_{OFF}.

Singh *et al.* [87] have proposed a DG JLFET with dielectric pockets in the channel region. The authors have pointed out that the dielectric pocket suppresses the electric field penetration along the channel which effectively curtails the I_{OFF} with an improved I_{ON}/I_{OFF} ratio, smaller SS, and lesser DIBL.

Pourian *et al*. [88] have presented a numerical study on the effect of uniaxial strain on the performance of carbon nanotube based JLFET. The study reveals that the application of tensile strain increases the energy band gap (E_G) which in turn reduces the I_{OFF} and improves the I_{ON}/I_{OFF} ratio in the digital domain, whereas, in the analog domain better value of f_T has been achieved in comparison to a non-stressed JLFET.

2.3.4 Research status of misalignment in JLFETs

In multigate JLFET architectures, the double gate structure can operate in both symmetric and asymmetric modes. Apart from the many types of structural asymmetries like a different type of gate material/gate dielectric/effective oxide thickness (EOT)/bias voltages and misalignment the latter one has been addressed as a critical process issue in the literature.

Amin *et al.* [89] have presented a simulation study on 50% gate misaligned DG JLFET from an analog perspective. The authors have shown that the DG JLFET reflects smaller performance variations for gate misalignment than that of the IM counterpart. Also, the gate misalignment towards the source results in improved performance in comparison to the drain side in DG JLFETs whereas for IM DG FET the opposite is true.

Gupta *et al.* [90] have shown that gate misalignment in junctionless devices can also be used as an effective way to obtain steeper SS. It has been exhibited that the gate misalignment results in an inclined channel with increased current density and enhances the degree of impact ionization which leads to sharp subthreshold switching.

Abhinav *et al.* [91] have studied the effect of gate misalignment on the analog/RF performance of DG JLFET. The authors have noticed that the DIBL, SS, I_{ON}/I_{OFF} ratio, gm,

V_{EA}, A_v, f_T, gain-frequency product (GFP), and transconductance frequency product (TFP) degrade with an increase in gate misalignment due to poor channel control. The authors have claimed to find the thermal stable point for all analog/RF figure of merits which is imminent between V_{GS} = 0.5-0.9 V.

Jana *et al.* [92] have explored the effect of gate misalignment in a DG JLFET. The study reveals that the effect of gate misalignment can be mitigated to a small extent by considering the graded doping profile in the channel region. However, this may lead the parasitic bipolar action in the device, hence, the doping profile must be chosen carefully.

Mendiratta *et al*. [42] have proposed an asymmetric DG JLFET with a gate length of 18 nm which reflects improved SCEs. The authors have stressed the utility of the device in low-power applications with diminished OFF-state leakage current of ~10^{-17} A/µm and small I_{ON} of ~10^{-6} A/µm.

Concurrent with the TCAD based simulation study, the analytical models for JLFETs have also been developed by various researchers to strengthen the theoretical foundations. The research status of analytical modeling for JLFETs using different assumptions has been reviewed in the coming section.

2.4 Research status of analytical modeling for JLFETs

A variety of analytical models have been developed for single as well as multigate JLFETs. However, as the single gate JLFET suffers from poor channel depletion, most of the analytical models have been developed for symmetric DG and GAA nanowire JLFETs. The structural symmetricity in these devices results in additional boundary conditions which simplify the solution of Poisson's equation. Moreover, both charge based and potential based approaches have been used to model the drain current in JLFETs.

2.4.1 Charge based analytical models for JLFETs

Sallese *et al.* in [44] have developed a charge based analytical drain current model for symmetric DG JLFET. The model results have been validated in all operating regions for the device i.e., from depletion to accumulation and in both linear and saturation modes without using any empirical parameter. However, in this work, the related physical phenomena such as SCEs, quantization effects, and dependence of carrier mobility on the electric field were not considered.

Trevisoli *et al*. in [93] have presented the analytical model for drain current in nanowire JLTs while considering the SCEs. The SCEs have been considered with solving Poisson's equation to obtain the analytical expression for minimum channel potential and reflect the dependence of V_{TH} and SS on L_G.

Jazaeri *et al*. [94] have aimed at the charge-based drain current modeling of asymmetric operation in DG JLFET by combining two virtual symmetric devices with both gates biased at different voltages. In addition, the technological asymmetry affecting C_{ox} has also been accurately incorporated into the model.

In charge based analytical modeling, the charge density in the channel is approximated which governs the flow of drain current in JLFET. However, developing an analytical and computationally efficient charge-based model remains a challenge, which limits their popularity in circuit simulations. Alternatively, a popular modeling technique based on potential has also been used for understanding the physics of JLFETs.

2.4.2 Potential based analytical models for JLFETs

The potential based analytical models have been formulated with either of the two assumptions. In the first case, the 2-D channel potential distribution is obtained by decomposing it into two parts (variable separation) while in the second case, the potential distribution across the channel has been assumed parabolic (parabolic potential) in nature.

2.4.2.1 Analytical models based on variable separation technique

Jin *et al*. [95] have proposed an analytical subthreshold drain current model for symmetric DG JLFET using a variable separation technique (VST) to solve the 2-D Poisson's equation. The model successfully considers the effect of L_G, t_{si}, t_{ox}, and N_D without any fitting parameter.

Gnudi *et al*. [96] have given the analytical expression for variation in V_{TH} due to RDFs in both cylindrical and double-gate JLFETs. The authors have shown that in 20 nm JLFET, the RDFs lead to a large V_{TH} variation of ~115 mV which can limit the device's suitability in advanced technological applications.

Holtij *et al*. [97] have developed a 2-D analytical model for calculating the V_{TH} and potential profiles for short-channel DG JLFET in the subthreshold region. The authors have estimated the channel potential by superimposing the 1-D particular solution and 2-D Laplacian solution which has been solved using Schwarz-Christoffel conformal mapping.

Woo *et al*. [98] have considers the effect of fluctuations in depletion width with localized charge introduced at the silicon-oxide interface to develop the analytical threshold voltage model for DG JLFET. The authors have reported that the positive/negative trap charge density (N_f) leads to a decrease/increase in flat band voltage according to the relation $V_{FB}' = V_{FB} - qN_f/C_{ox}$, which modulated the V_{TH} of the device. Here, V_{FB}' and V_{FB} represent the flat band voltages of damaged and undamaged silicon-oxide interface, respectively.

Kumari *et al*. [99] have reported a 2-D analytical drain current model for DGM JLFET based on VST by decomposing the channel potential into 1-D Poisson's and 2-D Laplace equations.

In this work, the underlap regions have not been considered and the drain current model in linear and saturation mode has been provided using two fitting parameters.

In the case of DG JLFET, the VST introduces a transcendental equation in terms of eigenvalues, which cannot be evaluated numerically [100]. Alternatively, the parabolic potential approximation can be used to model the surface/center potential in the device.

2.4.2.2 Analytical models based on parabolic potential approach

This method of analytical modeling assumes that the potential distribution across the channel is parabolic and works well for JLFET operating in full depletion and partial depletion. As the JLFETs are designed to operate in accumulation region only once they achieve the ON-state, hence, the parabolic potential approach (PPA) can also be used for analytical modeling of JLFETs.

Duarte *et al*. [100] have formulated an analytical model for bulk current in long-channel DG JLFET in the subthreshold region. In this paper, the channel potential has been obtained by deriving Poisson's equation while considering the depletion approximations. The authors have used the unique concept of high doping in JLFETs to obtain a simplified expression of depletion width.

Duarte *et al*. [101] have introduced an analytical model for DG JLFET. The authors claim that the proposed model is free from convergence problems unlike [50] and [104] as it captures the device conduction in all operating regions while using the parabolic potential approximation (PPA) and Pao-Sah integral.

Chen *et al*. [102] have developed a surface-potential based analytical model for drain current in long-channel DG JLFET. The authors have assumed appropriate approximation in deep depletion, partial depletion, and accumulation regions to derive the relationship between V_{GS} and surface potential. Although the SCE and quantum confinement were ignored, the model has been validated in subthreshold as well as linear and saturation regions.

Sallese *et al*. [103] have introduced the common core model to establish a link between DG JLFET and cylindrical nanowire JLFETs for long-channel devices. In this paper, the authors have unified the electrostatic concepts of the two junctionless structures by defining a correspondence between silicon thickness (t_{si}) with silicon radius (t_R), C_{ox}, n_i, and N_D. However, SCEs were not considered in this analysis.

Holtij *et al*. [104] have reported an analytical model for symmetric DG JLFET including the carrier quantization effects. Applying the PPA approach, the QCEs have been considered by solving the Schrodinger equation in the subthreshold region for larger and smaller t_{si}. The analysis causes a correction in mobile charge density and V_{TH} which increases the accuracy of analytic results.

Jazaeri *et al*. [105] have analytically formulated the subthreshold drain current model for ultra-thin body DG JLFET. Considering the PPA across the channel, the authors have solved the 2-D Poisson's equation to determine the explicit relationships for I_{DS}, SS, and DIBL. The proposed model effectively predicts the effect of V_{DS} on minimum body potential. However, the authors have suggested applying the Boundary conditions on surface or center potential carefully as it may lead to a small deviation in approximated results.

Li *et al*. [106] have given the analytical subthreshold drain current model for short-channel cylindrical JLFET. The authors have presented the exact solution of 2-D Poisson's equation representing the potential profile with the Fourier-Bessel series. However, due to increased complexity in the analysis, the length of the depletion region in source/drain extension has been considered as zero, although, the model successfully describes the subthreshold behaviour of the device considering the effect of L_G, t_{ox}, and t_R.

Parvin *et al.* [107] have developed an analytical drain current model for DGM JLFET with enhanced digital performance. The 2-D Poisson's equation has been solved with PPA and SCEs have been considered for obtaining the expressions for electric potential and drain current.

Xiao *et* al. [108] have proposed a new analytical drain current model valid in all operating regimes to include the effect of dynamic channel boundary on the performance of DG JLFET. The authors have solved 2-D Poisson's equation to obtain the potential in both channel parts i.e., physical and dynamic.

Djeffal *et al*. [109] have analytically investigated the analog and RF performance of cylindrical GAA junctionless FET considering the effect of highly doped source and drain extension regions. The authors have reported improvement in g_m, f_T, TGF, and gain due to heavy doping in the extension regions.

Jaiswal *et al*. [110] have developed a 2-D quasi-analytical model for short-channel DG JLFET accounting for the effect of gate-underlap regions. The authors have divided the silicon layer into five-adjacent regions for evaluating the potential and then drain current. The effect of SCEs has also been included, but, QCEs were discarded.

The same authors in [111] have modeled the SCE in asymmetric short-channel DG JLFET with a five-region approach. In this work the authors have not only analyzed the effect of independent gate bias but, the structural asymmetries such as t_{ox}, Φ_G, and length of underlap regions (L_U) have also been considered. It has been suggested that along with N_D and L_U, the suitable back gate bias can also be used to optimize the device's subthreshold operation.

Furthermore, in [112] these authors have analytically modeled the SCEs in core-shell based DG JLFET. In this work, the impact of depletion extensions in source/drain regions on the

SCEs has been captured. Moreover, the effect of variations in core-thickness, and doping in the shell region, L_G, V_{GS}, and V_{DS} in the subthreshold region have been successfully incorporated into the model. It has been pointed out that core-thickness and shell doping can be used as additional controlling parameters to control the SCEs. Kumar *et al.* [113] have illustrated the importance of nanoelectronics in engineering.

Ajay *et al.* [114] have developed a PPA based analytical model for DG JLFET incorporating gate dielectric modulation. The neutral molecule in the nanogap cavity under the gate metal changes the dielectric constant, gate capacitance, V_{TH}, and eventually the surface potential in DG JLFET. It has also been found that n-type/p-type DG JLFET can be used in bio-sensing applications with the detection of negatively/positively charged biomolecules.

Chakraborty *et al.* [115] have formulated a model for analyzing the bio-sensitivity of based GAA JLFET with dielectric modulation in gate-stacked structure with HfO_2 as a high-k dielectric. In this work, the neutral biomolecule with a dielectric constant of more than 1 such as streptavidin, protein, biotin, etc. has been used in the nano-size cavities. The authors have reported the maximum sensitivity for a channel doping of 3×10^{18} cm^{-3}.

Hur *et al.* [116] have proposed a generalized potential model for symmetric and asymmetric DG JLFETs operating with tied and untied gates. In this paper, it has been revealed that the asymmetric DG JLFET with untied gates put strong control over V_{TH}. Moreover, small variations in back gate bias led to dynamic changes in V_{TH}.

T. K. Chiang in [117] has presented the subthreshold drain current model for tri-gate JLFET considering the effect of interface trapped charges (ITC). The authors have shown that either the thin gate oxide or thick silicon layer can be used to suppress the drain current degradation caused by ITC. In addition, the SCEs increase/diminish with positive/negative types of ITC. Importantly, the author has commented that the DG JLFET with lesser gate coverage over the channel region leads to better suppression of drain current degradation due to ITC in comparison to tri-gate and GAA JLFET. Cohen *et al.* [118] have shown that the quality of surface quality can affect the electronic properties of semiconductor namely electronic affinity and band bending

With extensive research on its physical properties using TCAD based simulation and the development of analytical models, the JLFETs are the potential candidate to be used in circuit implementation. In the following section, the research efforts made on circuits application based on various JLFETs have been reviewed.

2.5 Research status of circuit applications based on JLFETs

The use of electronic devices in circuit applications is the true measure of their utility in the real world. The performance of different types of JLFETs has also been explored in various types of circuits such as memories, CMOS inverters, common-source (CS) amplifiers, etc.

Baidya *et al*. [121] have analyzed the circuit performance of an ultrathin DG JLFET by implementing the inverter, 2-input NAND, and NOR gates using mixed-mode simulation in Atlas TCAD. The authors have presented the effect of different gate dielectric materials (SiO_2, Si_3N_4, and HfO_2) on circuit performance. It has been noticed that the use of high-k gate dielectric material results in steeper voltage transfer characteristics (VTC), transient gain, DC gain, and noise margin (NM).

Guin *et al*. [38] have compared the performance of CMOS circuits based on junctionless and IM FinFETs. It has been shown that for 10 nm technology, in comparison to IM FinFET, the junctionless FinFET based CMOS inverter reflects smaller rise and fall times with reduced dynamic power dissipation by ~28 %, ~10 %, and 25.1 % respectively. Whereas, the maximum frequency of oscillations in a 3-stage ring oscillator (RO) implemented with n-type and p-type junctionless devices improves by ~12 % due to smaller gate capacitance comparatively.

Wagaj *et al*. [123] have demonstrated the circuit performance of n-type and p-type DGM SOI JLFET in comparison to DGM SOI IM FET by implementing the CMOS inverter. The author has reported that the DGM SOI JLFET based inverter reflects improvement in NM, f_T, A_{V0}, and static power dissipation. Moreover, the CS amplifier based on DGM SOI JLFET shows an amplification of 1.25 times in comparison to DGM SOI IM FET based counterpart.

Garg *et al*. [39] have investigated the performance of DG JLFET based circuits due to localized or fixed charges at the semiconductor-oxide interface with uniform, step, graded, and Gaussian profiles. It has been depicted that the presence of positive/negative trap charges leads to a decrease/increase in the V_{TH} of the device and results in a maximum shift of VTC towards left/right and switching threshold voltage of the CMOS inverter with a uniform doping profile. However, for a uniform profile, the NMs change minimally due to the least variations in minimum surface potential and I_D.

Li *et al*. [124] have investigated the effect of trench process variation (TPV) angle on the performance of CMOS inverters based on recessed JLFET. In this work, it has been exhibited that the TPV can significantly impact the V_{TH} and SS of the device which can introduce fluctuations in propagation delay and static NM of the CMOS inverter. It has been commented that for $L_G < 20$ nm the TPV impacts the subthreshold characteristics more severely than the RDF and LER.

Gupta *et al*. [125] have designed various digital and analog circuits based on conventional DG JLFET at 20 nm gate length. The authors have reported DG JLFET based inverter shows the switching threshold voltage, NM, and delay of 0.43 V, 0.265 V, and 19.18 ps, respectively. In the analog application, the CS based on DG JLFET has been designed which depicts high g_m and gain with low output impedance.

Panchore *et al*. [126] have investigated the circuit performance reliability due to hot-carrier effects in DG JLFET by incorporating TiO_2 as high-k gate dielectric towards the source side and vacuum gate dielectric towards the drain side. The effect of hot-carrier stress has been applied for 2000 seconds at the supply voltage of 0.5 V on various designed circuits namely RO, SRAM cell, and CS amplifier. The 11-stage RO made from vacuum dielectric-based DG JLFET reflects the improved oscillating frequency with before and after hot carrier stress comparatively. The 6T SRAM cell designed with the proposed device depicts smaller degradation of ~23 % and ~15 % in both read and write delays due to post-hot carrier stress, respectively. Moreover, the CS amplifier reflects a smaller reduction in a voltage gain of ~30 % after applying the hot carrier stress.

Liao *et al*. [119] have investigated the implications of structural variations on read and write noise margins of GAA JLFETs based static random-access memory (SRAM). In comparison to the conventional counter circuit the JLFET based SRAM has been found more susceptible to nanowire diameter due to significant variations in V_{TH}, hence, to produce good quality SRAM cells based on JLFETs the fabrication must be controlled firmly.

Tayal *et al*. [35] have investigated the impact of high-k gate dielectric in junctionless nanotube FET based 6T SRAM cells. The authors have confirmed that using TiO_2 as high-k dielectric material leads to marginal improvement in static noise margins while the write and read access times boost by ~20 % and ~18 %, respectively. In addition, it has been suggested that the read and write access times can be further improved by using a thin interfacial layer under the high-k gate dielectric.

Ansari *et al*. [120] have implemented a 1T dynamic random-access-memory (DRAM) cell based on JLFET and studied the effect of N_D, Φ_G, bias, etc. for optimizing the retention time (RT) at 85 °C. In this work, it has been exhibited that an increase in doping concentration reduces both carrier lifetime ($N_D \leq 10^{18}$ cm^{-3}) and the potential depth ($N_D \geq 10^{18}$ cm^{-3}) which results in smaller RT. However, high doping puts a tradeoff between higher speed and increased power dissipation. Moreover, optimizing Φ_G and bias can be used to retain a potential depth which improves the RT.

The same authors in [36] have addressed the issue of shallower potential depth due to high doping in JLFET which leads to enhanced RT in 1T DRAM cell. The authors have used a

shell-doped architecture to improve the depletion with deeper potential well. It has been reported that thinner shell results in the reduced generation and recombination of holes which is important for obtaining high RT.

G. Giusi in [37] investigated the effect of trap-assisted tunneling (TAT) in 1T DRAM cell based on floating-body JLFET. It has been pointed out that the TAT occurs mainly during the HOLD process and affects the RT due to large doping concentrations. The author has suggested that in the proposed DRAM cell the large doping variability can be controlled with longer L_G (~100 nm) and whereas independent gate bias can be used to control the doping fluctuations for smaller L_G. However, QCEs were not included in such theoretical analysis.

Remarkably, the performance of JLFETs has not only been explored with only TCAD based simulation or mathematical analytical models at the device and circuit level but it has also been demonstrated with the experimental work through the characterization of its electrical behaviour.

2.6 Performance comparison of various JLFETs reported in the literature

The performance comparison between various major performance boosters for JLFETs in terms of I_{ON}, I_{OFF}, and I_{ON}/I_{OFF} ratio have been listed in Table 2.1. From Table 2.1, it can be observed that maximum I_{ON}, lowest I_{OFF}, and highest I_{ON}/I_{OFF} have been achieved in the order of ~10^{-3} A, ~10^{-14} A, and ~10^{9}, respectively.

Table 2.1 Performance comparison of different JLFETs reported in the literature.

Reference	Applied Engineering	L_G (nm)	I_{ON} (A) @ V_{GS} = 1.0 V	I_{OFF} (A) @ V_{GS} = 0.0 V	I_{ON}/I_{OFF}
Gundapaneni *et al.*, IEEE Transactions on Electron Devices, 2011, [69]	Single gate bulk planar junctionless FET with high-k spacer	20	~10^{-4}	~10^{-10}	~10^{6}
Baruah *et al.*, Journal of Computational Electronics, 2013, [70]	DG junctionless FET with high-k spacers (HfO_2)	20	~10^{-4}	~10^{-12}	~10^{8}
Ghosh *et al.*, Journal of Semiconductors, 2014, [128]	DG junctionless FET with hetro-gate dielectric material	20	~10^{-4}	~10^{-11}	~10^{7}
Kumar *et al.*, IEEE Transactions on Electron Devices, 2015, [86]	DG junctionless FET with shell-core-shell profile	20	~10^{-4}	~10^{-12}	~10^{8}
Wang *et al.*, Microelectronics Reliability, 2015, [129]	DG junctionless FET with three gates with two different materials	30	~10^{-3}	~10^{-9}	~10^{6}
Amin *et al.*, Journal of Computational Electronics, 2015, [89]	DG junctionless FET with misaligned gate on source side	20	~10^{-4}	~10^{-12}	~10^{8}
Mondal *et al.*, Applied Physics A, 2015, [130]	JLFET with a non-uniform doping	20	~10^{-4}	~10^{-11}	~10^{7}

Singh *et al.*, Journal of Computational Electronics, 2016, [87]	DG junctionless FET with dielectric pocket	20	$\sim10^{-4}$	$\sim10^{-11}$	$\sim10^{7}$
Lahgere *et al.*, IEEE Transactions on Electron Devices, 2017, [131]	Tunnel dielectric based junctionless transistor	20	$\sim10^{-6}$	$\sim10^{-13}$	$\sim10^{7}$
Jaiswal *et al.*, IEEE Transactions on Electron Devices, 2018, [111]	Asymmetric DG junctionless FET with underlap	20	$\sim10^{-4}$	$\sim10^{-12}$	$\sim10^{8}$
Wagaj *et al.*, International Journal of Electronics, 2019, [123]	Dual material gate based junctionless FET	20	$\sim10^{-5}$	$\sim10^{-9}$	$\sim10^{4}$
Banerjee *et al.*, International Journal of Electronics and Communication, 2020, [150]	Charge plasma based junctionless C-FinFET	20	$\sim10^{-4}$	$\sim10^{-10}$	$\sim10^{6}$
Garg *et al.*, IEEE Transactions on Nanotechnology, 2021, [147]	Dielectric separated independent gates junctionless transistor	20	$\sim10^{-6}$	$\sim10^{-12}$	$\sim10^{6}$
Kumari *et al.*, IEEE Transactions on Nanotechnology, 2022, [186]	Split-gate junctionless field-effect-transistor	31	$\sim10^{-5}$	$\sim10^{-12}$	$\sim10^{7}$
Kumari *et al.*, IEEE Sensors Journal, 2023, [43]	Planar ground plane junctionless transistor	20	$\sim10^{-4}$	$\sim10^{-12}$	$\sim10^{8}$

2.7 Research gaps identified in the literature

Based on the literature reviewed following gaps/ challenges have been identified.

- The heavily doped junctionless devices offer comparable ON-current to IM FETs with similar device dimensions. However, the JLFETs suffer from poor channel depletion in OFF-state which leads to increased leakage current with degraded SS in OFF-state. Hence, there is a need to present/propose a JLFET with structural modification in terms of gate/channel engineering which provides improved depletion with smaller I_{OFF}, higher I_{ON}/I_{OFF}, and better SS than the conventional JLFET.
- Scaling the channel length results in a higher influence of drain into the channel which leads to increased SCEs in JLFET e. g. higher DIBL. Hence, there is a possibility to present a robust technological solution with suppressed SCEs in comparison to conventional JLFET.
- The analytical modeling of conventional JLFET and different performance boosters have been done using various approximation methods. Hence, there is a possibility to develop an analytical model for the novel/proposed junctionless FETs.
- The conventional JLFET has been used to implement various circuits in the digital and analog domains. Hence, there is a possibility to investigate the performance of the proposed junctionless device at the circuit level also.

2.8 Thesis objectives

Based on the literature gaps identified following objectives have been formulated for the work presented in this thesis.

- To design a structurally engineered junctionless FET in order to optimize the electrical parameters namely current ratio, drain induced barrier lowering, subthreshold slope, etc.
- To develop an analytical model of the designed junctionless FET.
- To implement a basic logic gate using the designed junctionless FET.

2.9 Research methodology

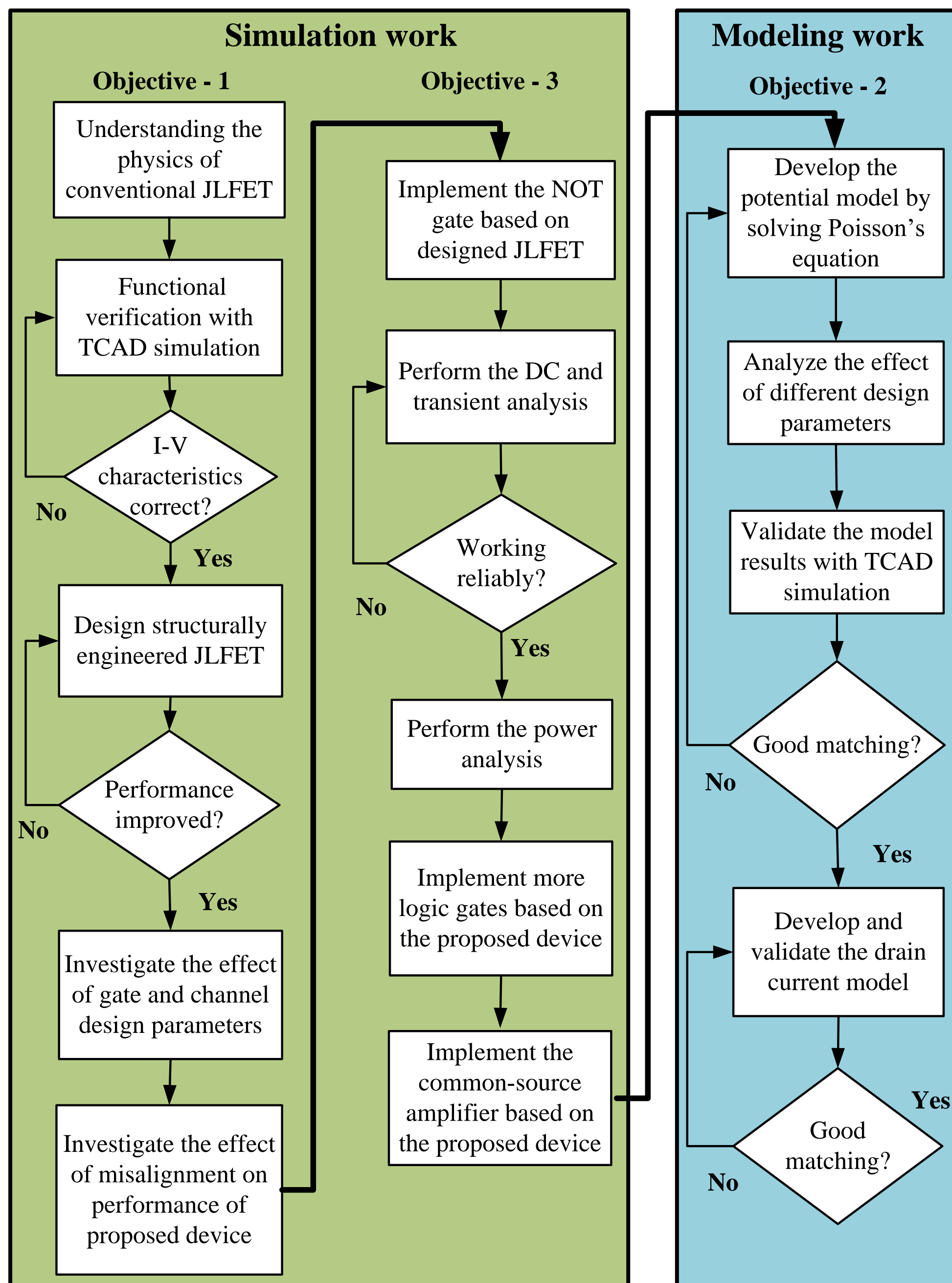


Figure 2.2 Flow chart of research methodology used to accomplish the defined objectives.

From the defined objectives, it is clear that the work accomplishment requires intense simulation to investigate the performance at both device and circuit levels along with rigorous mathematical analysis for the development of physical insight into the device's electrical behaviour. To achieve the defined research objectives, the used methodology has been shown in Figure 2.2.

Started working on objective-1, the electrical behaviour of conventional JLFET has been studied from the available literature and the device functionality has been simulated on the 2-D Silvaco Atlas TCAD tool. Once, the transfer and output characteristics of conventional JLFET have been obtained, the next step was to design a structurally engineered JLFET with improved performance in comparison to conventional JLFET. Additionally, the guidelines were set in terms of gate and channel parameters such as gate material work function, EOT, channel length, etc. Moreover, the impact of misalignment on the performance of the proposed JLFET has also been investigated.

Since, objective-3 also requires the TCAD simulation work, hence, it has been worked upon once objective-1 was accomplished. To achieve objective-3, the Mixed-mode circuit simulator has been used with input command file as a combination of simulation programs with integrated circuit emphasis (SPICE) and Atlas commands. A NOT gate has been implemented with the proposed JLFET and its operational reliability has been verified with DC and transient analysis. In addition, the power analysis of the implemented circuit has been performed.

Few more logic gates and common-source amplifier have also been implemented based on the proposed JLFET. Furthermore, to accomplish objective-2, rigorous mathematical analysis has been done to solve the 2-D Poisson’s equation with a parabolic potential approach. The surface potential-based drain current model has been developed which includes the effect of gate/drain voltages, doping concentration, gate work function, etc.

Chapter-3
Proposed recessed double gate JLFET

3.1 Introduction

With better device scalability due to its lower gate capacitance and operating capability in symmetric/asymmetric modes, the DG field-effect-transistor (FET) structure has been used to control the short channel effects in sub-100 nm MOSFETs. Besides these advantages, the DG FET structure has also been used in junctionless devices as the popular low-power solution with a relaxed thermal budget by avoiding the complex fabrication process of ultra-steep p-n junctions [17]. However, in the sub-20 nm regime, the gate controllability over the channel in the DG JLFETs structure becomes poorer due to the smaller distance between the source and drain terminal which results in a reduced energy barrier height at the source-channel boundary. This permits more electrons inside the channel in the OFF-state conditions (V_{GS} = 0.0 V) known as *poor channel depletion* and has been recognized as a significant challenge in designing of JLFETs [18]. Consequently, the OFF-state leakage current (I_{OFF}) increases in the junctionless device which reduces the ON-to-OFF current ratio (I_{ON}/I_{OFF}). The higher value of I_{OFF} results in a degraded slope of transfer characteristics of the device which leads to increased subthreshold slope (SS). The threshold voltage (V_{TH}) of JLFET is also lowered which results in increased drain-induced-barrier-lowering (DIBL) in the device [18]. Decisively, the reduction in channel length starts overwhelming the overall performance of the DG JLFETs with a weakening of depletion region in OFF-state. To compensate for this effect the thickness of the silicon layer can play an important role while improving the quality of OFF-state depletion in the DG JLFET [63]. This can be done if the distance between the two gate electrodes is decreased which leads to an improved electric field in the silicon layer.

In this chapter, it has been demonstrated that in the proposed recessed double gate junctionless field-effect-transistor (R_DGJLFET), the electrostatic effect is increased in the exterior parts of the channel and underlap regions with patterning of gate electrode over a recessed silicon layer. With 2-D TCAD simulations, the effect of gate and drain voltages on various physical phenomena such as electric field, potential distribution, electron concentration, and energy barrier in the device has been presented. Various performance parameters of the proposed R_DGJLFET namely, I_{OFF}, I_{ON}, SS, and DIBL have been compared with the conventional double gate junctionless field-effect-transistor (C_DGJLFET). It has been observed that the increased proximity between the gate electrodes provides better supervision of electrons in the channel which leads to smaller leakage current and improved I_{ON}/I_{OFF} in the device.

The placement of the gate electrode over the recessed silicon channel allows the designer to investigate the effect of the channel and gate engineering on the proposed R_DGJLFET. Hence, the effect of channel engineering on I_{OFF} and I_{ON}/I_{OFF} ratio has been investigated considering the variations in (a) the channel length (L_G), (b) the depth of recessed silicon (D_{RS}), and (c) the length of recessed silicon (L_{RS}). It has been demonstrated that the parameters D_{RS} and L_{RS} can be used for coarse and fine-tuning of the performance of R_DGJLFET.

Moreover, with the increased proximity of both gate electrodes, the effective oxide thickness (EOT) of the gate dielectric and work function of gate material (Φ_G) also becomes critical parameters that can affect the performance of R_DGJLFET. It has been found that the high-k gate dielectric based R_DGJLFET outperforms the conventional counterpart for a specified value of EOT. Furthermore, to explore the specialty of a double gate structure the performance of R_DGJLFET has been investigated with variations in a) equal value of Φ_G for both gate electrodes (*symmetric mode*) and b) different value of Φ_G for both gate electrodes (*asymmetric mode*). The proposed R_DGJLFET maintains its edge over the C_DGJLFET for the specified range of Φ_G in symmetric mode and reflects smaller performance variations in asymmetric mode.

From the literature, the misalignment has also been found as a critical fabrication issue that primarily affects the electrostatic coupling between the gate electrodes in the channel region and results in degraded subthreshold and analog/RF performance [42, 90, 91, 166]. The present work provides a study of the misalignment on the proposed R_DGJLFET. It has been found that the R_DGJLFET behaves sturdily against misalignment with smaller variations in SS, DIBL, transconductance generation factor (TGF), cut-off frequency (f_T), and gain-bandwidth product (GBW) in comparison to C_DGJLFET. Different performance parameters have been shown for the various devices produced at 5 nm technology. The value of DIBL and SS for the devices fabricated at 5 nm technology have been reported as 35 mV V^{-1} and 68 mV/dec, respectively by TSMC [187]. Moreover, in many publications the ON-current and OFF-current of the order of mA/μm and nA/μm have reported [122, 187-190]. Comparing to these state-of-the-art devices, with proposed R_DGJLFET, we can have similar kind of performance at a larger channel length by employing channel engineering.

3.2 Device structure

The 3-D view of both C_DGJLFET and proposed R_DGJLFET have been presented in Figure 3.1(a) and Figure 3.1(b), respectively. The proposed R_DGJLFET has been designed with L_G of 20 nm and a 10 nm thick silicon layer was doped with an n-type impurity concentration of 1×10^{19} cm^{-3} [64][128]. The HfO_2 has been considered as the promising

dielectric material for the gate as well as spacer regions due to its outstanding thermodynamic and chemical stability with Si, a wide band gap of ~5.8 eV, the suitable band offset values on Si substrate, and a high dielectric constant (≈25) [132][133]. In addition, with an effective oxide thickness (EOT) of 1 nm, it has been used to suppress the gate leakage current [134]. The length of underlap region towards the source (L_{US}) and drain (L_{UD}) has been fixed to 10 nm to lower the effect of series resistance on the overall drain current [66].

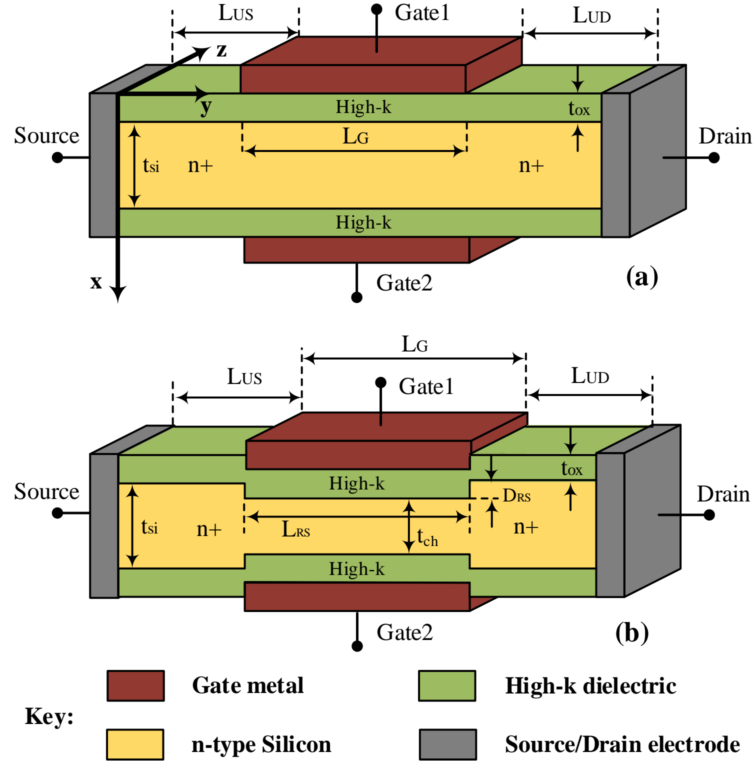


Figure 3.1 The 3-D view of (a) C_DGJLFET [17][21], and (b) the proposed R_DGJLFET.

Table 3.1 Device parameters used for simulation in Silvaco Atlas TCAD.

Name of the parameter	Proposed recessed DG JLFET	Conventional DG JLFET
Channel length (L_G)	20 nm	20 nm
The thickness of the silicon layer (t_{si})	10 nm	10 nm
Channel thickness (t_{ch})	06 nm	10 nm
The effective thickness of gate dielectric (EOT)	1 nm	1 nm
The doping concentration in the silicon layer (N_D) [63]	1×10^{19} cm^{-3}	1×10^{19} cm^{-3}
The work function of gate electrodes (Φ_G) [135]	5.1 eV	5.1 eV
Length of underlap region towards the source (L_{US}) [66]	10 nm	10 nm
Length of underlap region towards a drain (L_{UD}) [66]	10 nm	10 nm
Depth of recessed silicon area (D_{RS})	2 nm	--
Length of recessed silicon area (L_{RS})	20 nm	--

However, before patterning the two gate electrodes, the silicon channel has been recessed in the channel region for a specific depth (D_{RS}) and length (L_{RS}) of 2 nm and 20 nm, respectively. Hence, the thickness of the silicon layer in the channel region (t_{ch}) remains 6 nm, which is mathematically formulated as $t_{si} - 2 \times D_{RS}$. In symmetric mode, the typical value of Φ_G for both gate electrodes have been fixed to commonly used metal namely Gold (Au) with a value of 5.1 eV [134]. The thickness of source/drain contacts has been fixed to 5 nm with Aluminium as the electrode material.

The respective design parameters for C_DGJLFET are of the same value as taken for the proposed R_DGJLFET except that the $t_{ch} = t_{si}$ due to its uniform silicon thickness from source through the channel to the drain as shown in Figure 3.1(a). The parameters used to simulate the two devices have been listed in Table 3.1. From fabrication point of view, the proposed device can be viewed as a FinFET structure. A 5 nm FinFET structure produced by Yoon *et al*. [122] has been considered as an experimental reference for the proposed R_DGJLFET.

3.3 The physical models used in TCAD simulations

The entire simulations have been performed in the 2-D Silvaco Atlas TCAD tool with a constant gate width (W_G) of 1 μm. In this work, the default value for all constant parameters given in [137] has been used unless specified otherwise. It is necessary to simulate the device operation with the inclusion of necessary models available in the TCAD tool. Hence, to authenticate the device operation different physical models have been used while considering the effect of heavy doping, band gap narrowing, carrier recombination, band-to-band tunneling, quantum confinement, and mobility.

3.3.1 Fermi-Dirac statistics

JLFETs have been known as heavily doped devices to obtain a high value of ON-current. To consider the effect of heavy doping in the channel the Fermi-Dirac model has been considered in device simulation [143]. In thermal equilibrium at temperature (T) the electrons inside the semiconductor lattice follow the Fermi-Dirac statistics which defines the probability of occupying an energy state f(E) by an electron as given in Eq. 3.1 [137].

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{kT}\right)} \tag{3.1}$$

where, E_F denotes the Fermi energy level, and k represents Boltzmann's constant.

3.3.2 Effect of the band gap narrowing

For the doping concentration greater than 10^{18} cm^{-3}, the especially varying intrinsic carrier concentration (n_{ie}) becomes doping dependent due to variations in energy band gap (ΔE_g) as

given in Eq. 3.2 [138]. The effect of bandgap narrowing due to heavy doping has been included in the work [138].

$$n_{ie}^2 = n_i^2 \exp\left(\frac{\Delta E_G}{kT}\right) \tag{3.2}$$

where ΔE_g is given as in Eq. 3.3 [145]

$$\Delta E_G = BGN.E \times \left[\sqrt{\left\{BGN.C + \left(\ln\frac{N_D}{BGN.N}\right)^2\right\}} + \ln\frac{N_D}{BGD.N}\right] \tag{3.3}$$

where, BGN.E, BGN.C, and BGN.N are user-defined parameters with the respective value of 9.3×10^{-3}, 0.5, and 1.0×10^{17} [139].

3.3.3 Effect of carrier recombination

The semiconductor material tries to reach equilibrium with the generation and recombination process of the carriers. In the presence of defect states in the energy bandgap phonon transition occurs. Theoretically, this two-step process was introduced by Shockley and Read [140], and Hall [141] (SRH). Mathematically, the model for SRH carrier recombination is given in Eq. 3.4 [143].

$$R_{SRH} = \frac{n.p - n_{ie}^2}{\tau_{p0}\left[n + n_{ie}\exp\left(\frac{ETRAP}{kT_L}\right)\right] + \tau_{n0}\left[p + n_{ie}\exp\left(\frac{-ETRAP}{T_L}\right)\right]} \tag{3.4}$$

where the lattice temperature in degree Kelvin is denoted by T_L, ETRAP is the difference between intrinsic Fermi level and trap energy level, τ_{p0} and τ_{n0} denote the lifetime for hole and electron, respectively.

3.3.4 Effect of band-to-band tunneling

The non-local band-to-band tunneling (BTBT) model estimates the tunneling process across the heavily doped p-n junction more accurately while considering the special variation in energy bands in the presence of a high electric field in the device. Furthermore, the non-local BTBT model facilitates the modeling of tunneling current in both forward and reverse directions. Using Wentzel-Kramers-Brillouin (WKB) approximation the tunneling probability T(E) is calculated as given in Eq. 3.5 [137].

$$T(E) = \exp\left\{-2.\int_{x_{start}}^{x_{end}}\left(\frac{k_e k_h}{\sqrt{k_e^2 + k_h^2}}\right).dx\right\} \tag{3.5}$$

where x_{start} and x_{end} are the starting and ending point of tunneling paths. The parameters k_e and k_h are the evanescent wavevectors for electrons and holes in the tunneling direction [137].

3.3.5 The quantum confinement effects

The density gradient model based on the moments of the Wigner function is used to model the effect of carrier confinement associated with local potential variations at the scale of electron wave functions in small geometry devices [63][148]. The quantum corrections are applied to the carrier temperatures which leads to updated equations for electron current as given in Eq. 3.6 [145].

$$J_n = qD_n.\nabla n - qn\mu_n \nabla(\psi - \Lambda) - \mu_n n(kT_L \nabla(\ln n_{ie})) \quad (3.6)$$

where D_n is the diffusion constant for electron, ψ denotes the wave function and Λ denotes the quantum correction potential [139]. As described in section 3.2, the value of t_{ch} is < 7 nm for R_DGJLFET, hence, the quantum confinement effects (QCE) model have been considered with the increased value of bandgap in the recessed silicon channel of the proposed R_DGJLFET [142]. Moreover, in the case of C_DGJLFET as $t_{ch} = t_{si}$, hence, no such requirement arises with a uniform thickness of silicon layer.

3.3.6 The mobility model

Various scattering mechanisms lead to momentum loss of electrons and holes accelerated at a high electric field in semiconductor material [137]. Lombardi mobility model has been used which considers the mobility dependency on temperature, doping concentration, and transverse electric field [144]. Mathematically, the components are combined with Matthiessen's rule as given in Eq. 3.7 [137], [144].

$$\frac{1}{\mu_T} = \frac{1}{\mu_{AC}} + \frac{1}{\mu_b} + \frac{1}{\mu_{sr}} \quad (3.7)$$

where μ_{AC} represents the surface mobility which is limited by acoustic phonon scattering, μ_b denotes the mobility component limited by optical intervalley phonon scattering, and μ_{sr} reflects the surface roughness factor [144].

3.3.7 Tool calibration

The tool calibration is an important step required to ensure the accuracy of the device behaviour by observing and minimizing the errors/uncertainties in the simulation setup to an acceptable level. In Figure 3.2 the calibration of the used TCAD tool has been presented by redesigning the 20-nm n-channel junctionless transistor and matching the simulation results with published data of Gundapaneni *et al*. [63], who have already calibrated their models with the experimental results of nanowire junctionless transistor fabricated by Colinge *et al*. [18]. The open symbol depicts the simulation result while the solid symbols are related to the published data.

In Figure 3.2, it can be noted that the inclusion of the non-local BTBT model results in more OFF-current in comparison to the case when it was not considered. This reflects the need to minimize the OFF-current in the junctionless device. The carrier lifetime of 10^{-7} s accounts for a doping concentration of 10^{19} cm^{-3}, which is also related to the current work. However, reducing the SRH recombination rate with the addition of noble metals like Gold or Platinum leads to a lowering of OFF-current which results in fast switching action using lifetime engineering [63].

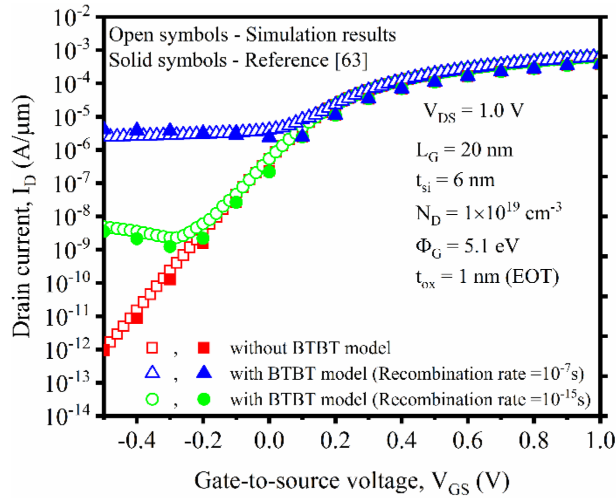


Figure 3.2 Comparison of simulation results with the published data for n-channel junctionless transistor [63].

The value of effective density of states for the electron (g_c) and holes (g_h) has been used as default while the value of tunneling masses for electrons and holes (i.e., m_e and m_h, respectively) have been tuned to closely match the simulation results with published data of [63].

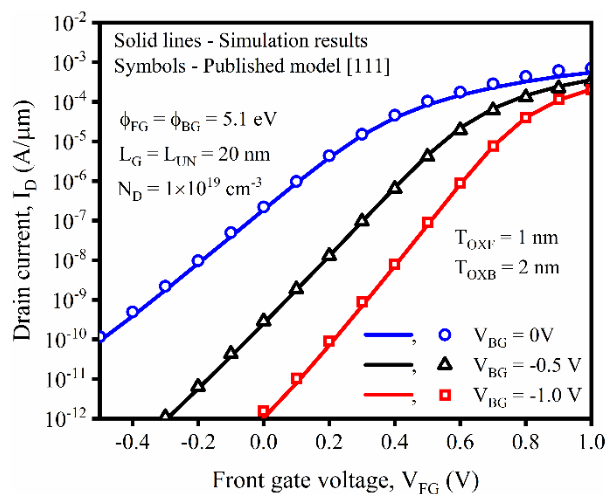


Figure 3.3 The impact of variations in front gate voltage on drain current of asymmetric junctionless MOSFET with underlap for L_G = 20 nm and W_G = 1 μm [111].

Furthermore, the I_D-V_{GS} characteristics of asymmetric junctionless DG MOSFET with underlap published by Jaiswal and Kranti [111] have also been matched as shown in Figure 3.3. Here, the impact of front gate voltage (V_{FG}) on drain current for different back gate voltages (V_{BG}) with asymmetric gate oxide thickness has been shown. The close agreement between the published data and simulation results is shown in Figure 3.2 and Figure 3.3 confirming the validation of our tool calibration.

3.4 Results and discussions

Before illustrating the performance of R_DGJLFET, it is important to discuss how recessing the silicon region influences the physical processes in the proposed device such as electric field, potential distribution, energy barrier height, etc. Along with that the possible shortcomings due to recessing the silicon region also need to be focussed.

3.4.1 Consequences of recessing the silicon channel

In C_DGJLFET for V_{GS} = 0.0V (OFF-state), the work-function difference between the gate metal and silicon surface introduces the electric field lines perpendicular to the direction of current, which forces the electrons away from the channel. However, in C_DGJLFET the poor OFF-state channel depletion has remained a challenge to achieve steeper subthreshold characteristics [18][70][87].

The limitation of poor depletion in the channel region has been addressed in R_DGJLFET by increasing the proximity between the gate electrodes by recessing the silicon channel region. The special placement of the gate electrode in R_DGJLFET sturdily affects the electric field strength in the silicon layer as shown in Figure 3.4(a).

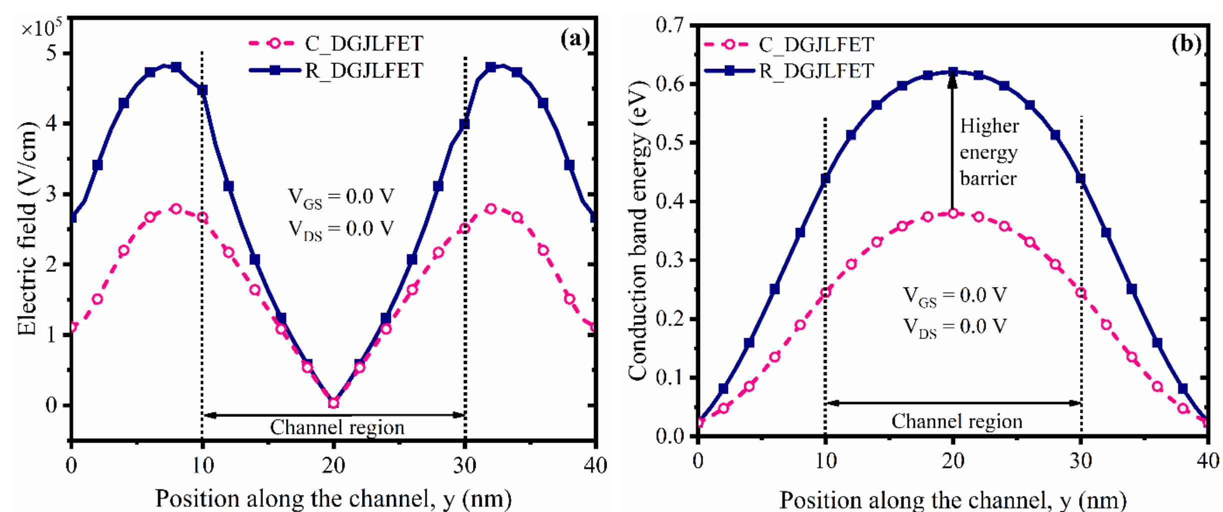


Figure 3.4 Effect of recessing the silicon area on (a) electric field b) conduction band energy.

The proximity of the gate electrode boosts the electric field strength in the lateral exterior parts of the channel and the underlap regions towards the source/drain, which can be attributed to the stronger fringing effect arising from gate edges in R_DGJLFET. Moreover,

due to the stronger electric field, the electrons see a higher energy barrier of ~0.03 eV in the case of R_DGJLFET as shown in Figure 3.4(b). This impacts the overall electrical performance and the proposed R_DGJLFET allows a smaller number of electrons in the channel for zero gate voltage. The higher energy barrier in R_DGJLFET leads to a much smaller potential distribution (i.e., more negative) in the channel, as presented in Figure 3.5. The contours of electron concentration in silicon film for C_DGJLFET and R_DGJLFET have been compared in Figure 3.6. Here, a small value of 50 mV has been applied between drain and source for considering the effect of V_{DS}, to observe the concentration difference in more favourable conditions.

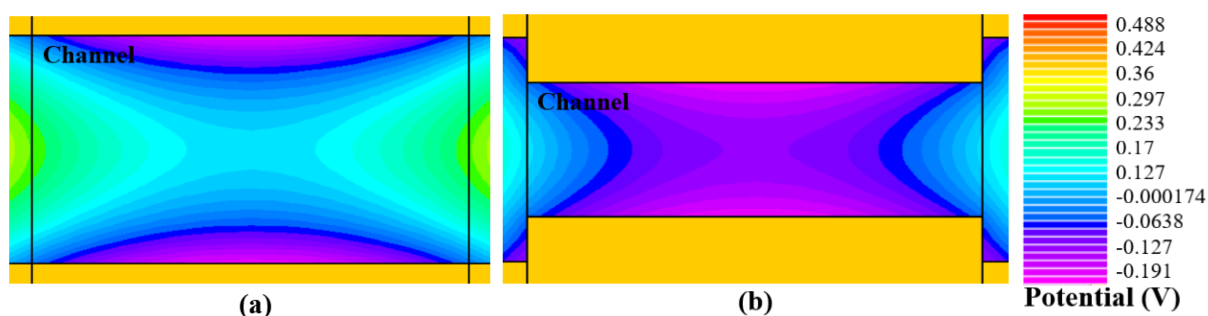


Figure 3.5 Contours of channel potential distribution in OFF-state of (a) C_DGJLFET, and (b) R_DGJLFET.

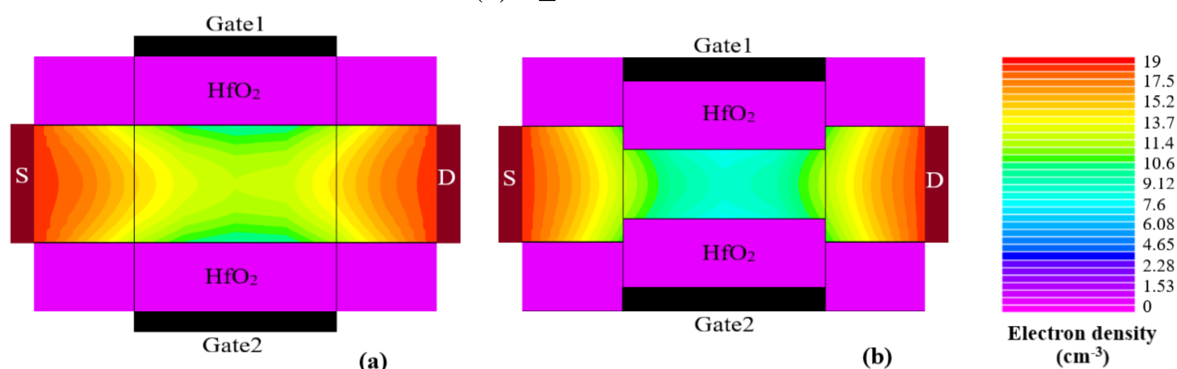


Figure 3.6 Contours of electron density in the silicon layer at $V_{GS} = 0.0$ V and $V_{DS} = 0.05$ V for (a) C_DGJLFET (b) R_DGJLFET.

As shown in Figure 3.6, the R_DGJLFET reflects a reduced electron concentration of the order of ~10^5 cm^{-3} in comparison to C_DGJLFET, which represents *more efficient channel depletion* in the OFF-state. Although, recessing the silicon region under the gate electrode seems to be a good choice for improving the OFF-state behaviour e. g. smaller I_{OFF}, yet, some consequences are important to be noted.

- In flat-band conditions, the ON-current which is governed by the channel thickness (t_{ch}) gets lowered proportionally as given in Eq. 3.8 [7].

$$I_{ON} \approx q\mu_n N_D \frac{t_{ch} W_G}{L_G} V_{DS} \tag{3.8}$$

where q is the electronic charge, μ_n is the mobility of electrons, N_D is the doping concentration in the silicon channel, W_G is the gate width, L_G is the channel length and V_{DS} is the drain-to-source voltage.

- In addition, at the circuit level, the smaller ON-current may lead to the charging/discharging of the load capacitor at a slower rate, which may impact the overall speed of the implemented circuit. Hence, controlling the value of D_{RS} and L_{RS} precisely may be critical for obtaining the desired performance.
- In addition, unlike the C_DGJLFET, the fabrication of R_DGJLFET requires an extra silicon etching step to obtain the recessed channel region. This will impact the process cost to realize such a device. The major fabrication steps for fabricating the proposed R_DGJLFET have been suggested in Appendix A.

With these pros and cons, the performance of the proposed R_DGJLFET has been detailed subsequently.

3.4.2 Device internal mechanisms

The effect of the gate and drain biases on electron density in both junctionless devices have been compared in Figure 3.7. In the R_DGJLFET the increased proximity of the two gate electrodes due to recessed silicon leads to a lesser channel region being depleted. Hence, the R_DGJLFET achieves better control over the channel region and the depletion of carriers is improved in OFF-state. The R_DGJLFET behaves similarly for V_{DS} = 1.0 V with reduced electron density extended in the underlap region towards the drain as shown in Figure 3.7(b). However, as represented in Figure 3.7(a) and Figure 3.7(b) the electron concentration profile in both recessed and conventional DG JLFET is almost similar in ON-state (i.e., V_{GS} = 1.0 V) for the value of V_{DS} = 50 mV and 1.0 V, respectively.

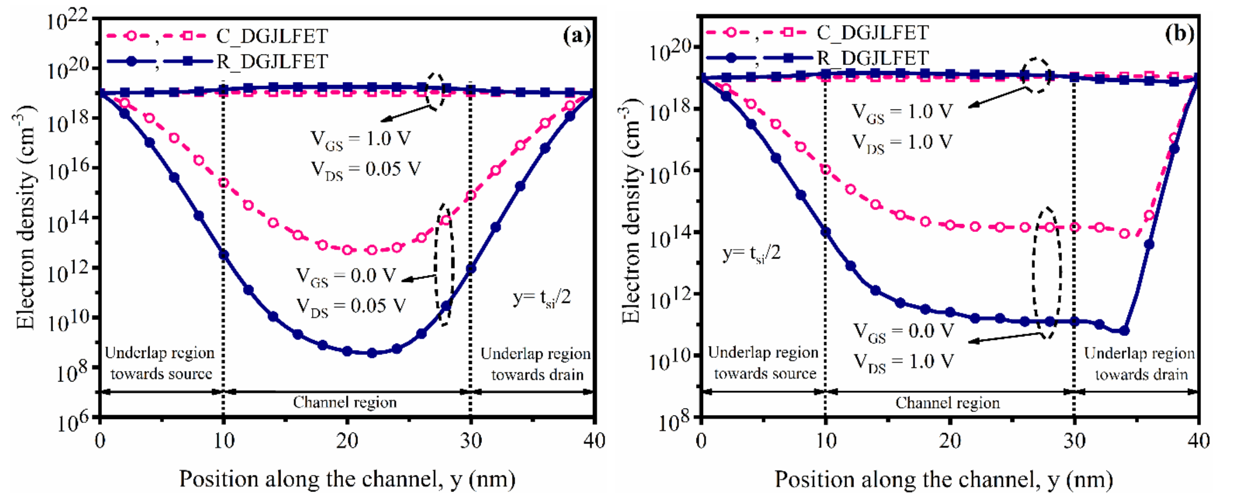


Figure 3.7 Electron density for C_DGJLFET and R_DGJLFET at x = $t_{si/2}$ with V_{GS} = 0.0 V and 1.0 V (a) for V_{DS} = 0.05 V (b) V_{DS} = 1.0 V.

The potential distribution along the channel (y-axis) of R_DGJLFET with variations in V_{GS} for a constant V_{DS} value of 1.0 V has been presented in Figure 3.8. The overall potential in the channel rises with an increase in V_{GS}. With increasing the value of V_{GS} from 0.0 V to 1.0 V the depletion region shrinks towards the Si-HfO_2 interface, which implies the presence of more electrons in the central part of the channel region and results in a rise of channel potential as depicted in Figure 3.8(a).

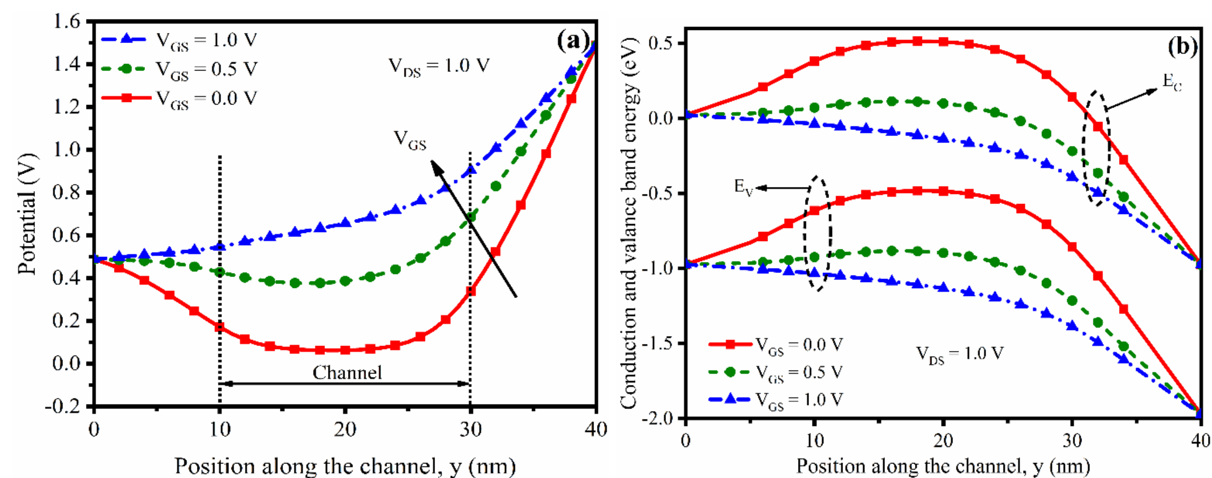


Figure 3.8 Effect of V_{GS} on (a) center potential distribution (b) conduction and valence band energy of R_DGJLFET at $x = t_{si/2}$.

With zero V_{GS} the channel in R_DGJLFET gets efficiently depleted. In this condition, the energy barrier in the channel prohibits the electrons to travel through the channel region. As the V_{GS} is increased, the potential barrier gets lower, which in turn allows more electrons to transport from source to drain. The conduction band and valence band energies in the channel region of R_DGJLFET depict a similar phenomenon as shown in Figure 3.8(b).

3.4.3 Performance comparison of R_DGJLFET with C_DGJLFET

The drain current vs. gate-to-source voltage (I_D-V_{GS}) characteristics for the R_DGJLFET have been compared with C_DGJLFET in Figure 3.9. It can be observed that for V_{GS} = 1.0 V, the R_DGJLFET shows the I_D of the order of ~10^{-4} A/μm which is comparable with the C_DGJLFET. However, for V_{GS} = 0.0 V, the device depicts significantly lower current with the values of ~10^{-14} A/μm and ~10^{-12} A/μm in linear (V_{DS} = 0.05 V) and saturation modes (V_{DS} = 1.0 V), respectively.

The drain current vs. drain-to-source voltage (I_D-V_{DS}) characteristics of the R_DGJLFET have been compared with C_DGJLFET as shown in Figure 3.10. From Figure 3.10, it is clear that the R_DGJLFET has similar output characteristics as that of the C_DGJLFET. However, the R_DGJLFET has a marginally lower I_D than the C_DGJLFET. It has been observed due to the reduced channel thickness between the two gate electrodes, leads to a reduction of available electrons for each value of V_{GS}.

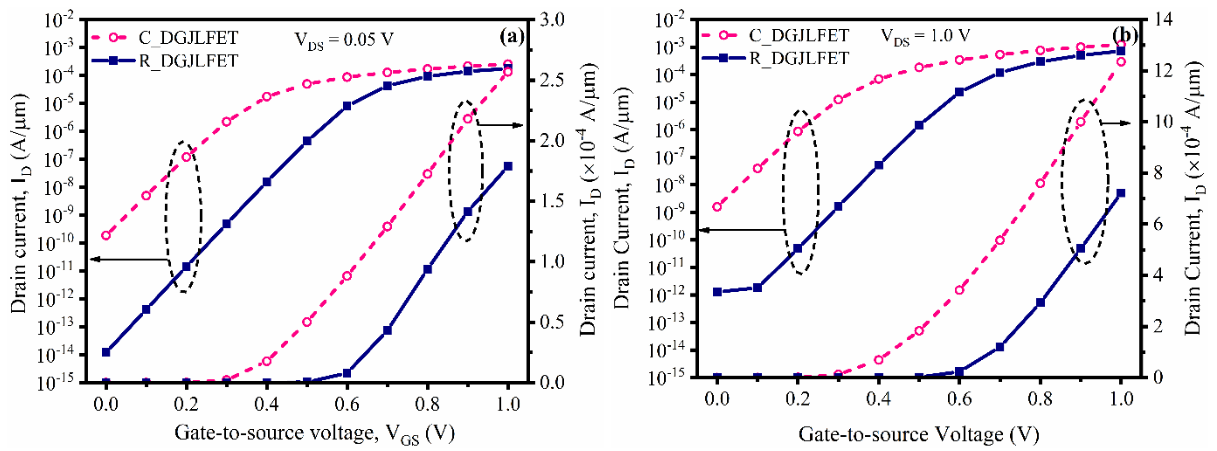


Figure 3.9 The I_D-V_{GS} characteristics of R_DGJLFET and C_DGJLFET (a) for V_{DS} = 0.05 V (b) for V_{DS} = 1.0 V.

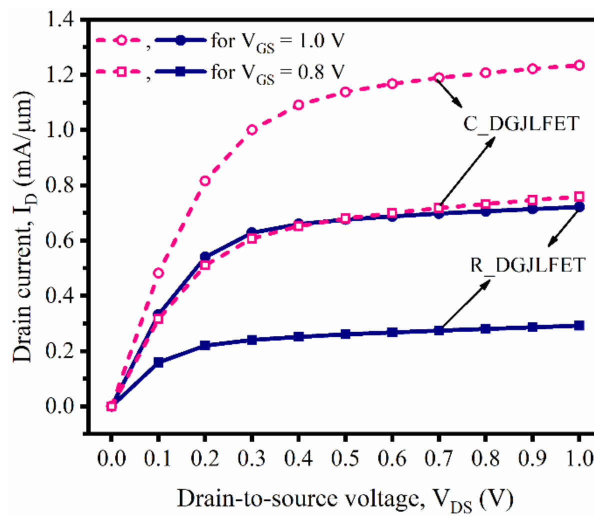


Figure 3.10 Comparison of I_D-V_{DS} curves for R_DGJLFET and C_DGJLFET.

Transconductance (g_m) is an important analog performance parameter of a MOSFET. It is the ratio of change in I_D for the respective change in V_{GS}. For R_DGJLFET and C_DGJLFET this parameter has been compared in Figure 3.11(a).

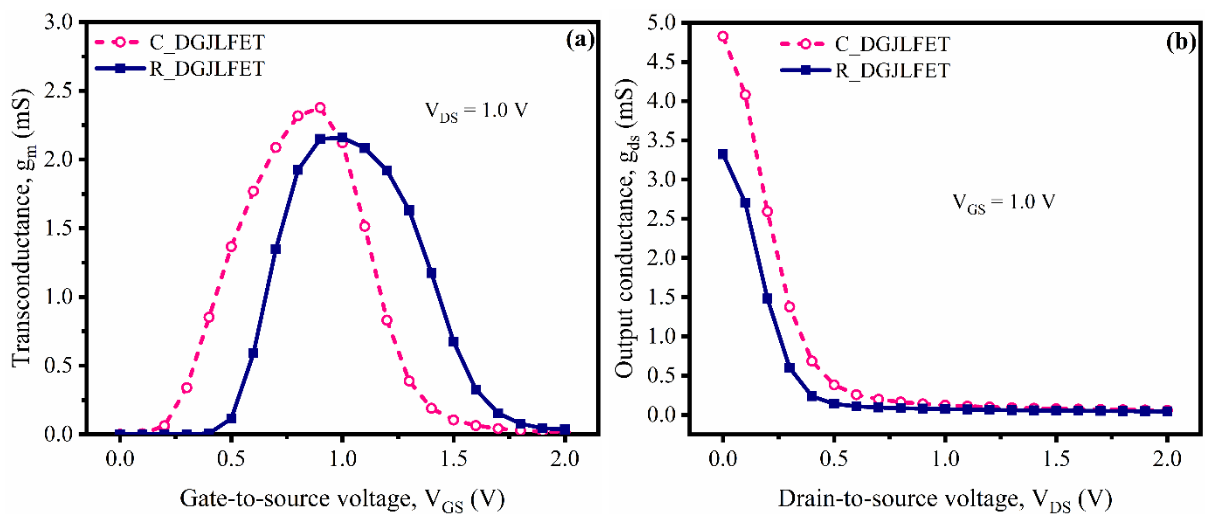


Figure 3.11 Comparison of (a) transconductance, and (b) output conductance between R_DGJLFET and C_DGJLFET.

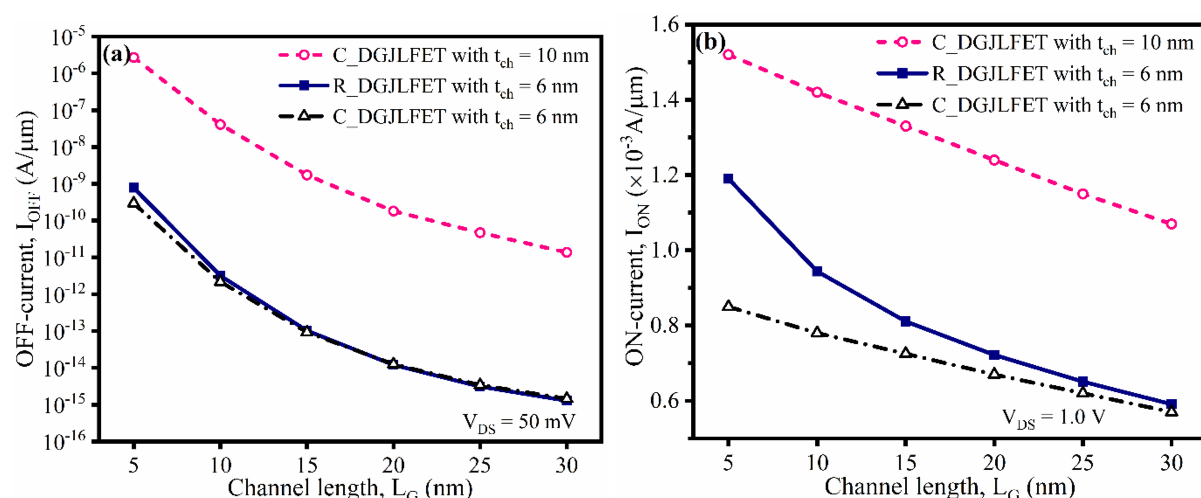
From Figure 3.11, it has been observed that for higher values of V_{GS} the R_DGJLFET reflects comparable g_m over the C_DGJLFET near flat band voltage (~1.0 V), which is important for operating the device in ON-condition. On the other side, the rise of the g_m curve of R_DGJLFET is delayed due to its higher V_{TH} as compared to C_DGJLFET. The device also shows comparable output conductance (g_{ds}) for higher V_{DS} as shown in Figure 3.11(b).

For lower values of V_{DS}, due to a weak lateral electric field, the effect of channel thickness dominates. The recessed silicon channel thickness results in reduced drain current proportionally [18] as given in Eq. 3.8. Reduction in silicon thickness increases the output resistance of the R_DGJLFET for low V_{DS} values which in turn lowers the g_{ds} as shown in Figure 3.11(b).

3.4.4 Effect of channel length scaling

The effect of scaling the L_G with constant L_{US} and L_{UD} on various performance parameters namely I_{OFF}, I_{ON} , I_{ON}/I_{OFF}, SS, and DIBL has been presented in Figure 3.12. In Figure 3.12(a), it has been seen that the reduction in L_G from 30 nm down to 5 nm leads to a significant rise in I_{OFF} due to the lowering of V_{TH} for both junctionless FETs. Simultaneously, the I_{ON} in both junctionless devices increases marginally as the electron density in ON-state is nearly saturated for different channel lengths as reflected by Figure 3.12(b).

As, the I_{OFF} and I_{ON} increase on logarithmic and linear scales, respectively, hence, a considerable reduction in I_{ON}/I_{OFF} has been observed as shown in Figure 3.12(c). Due to lower I_{OFF}, the R_DGJLFET always depicts better I_{ON}/I_{OFF} in comparison to C_DGJLFET. For 20 nm channel length the R_DGJLFET shows an I_{ON}/I_{OFF} of the order of ~10^{10} as that of C_DGJLFET with a value of ~10^6, which represents the ability to switch more effectively [145]. It has also been observed that R_DGJLFET shows the highest I_{OFF} of ~100 pA/µm for L_G = 5 nm and the best I_{ON}/I_{OFF} of the order of ~10^{11} for $L_G \geq 25$ nm.



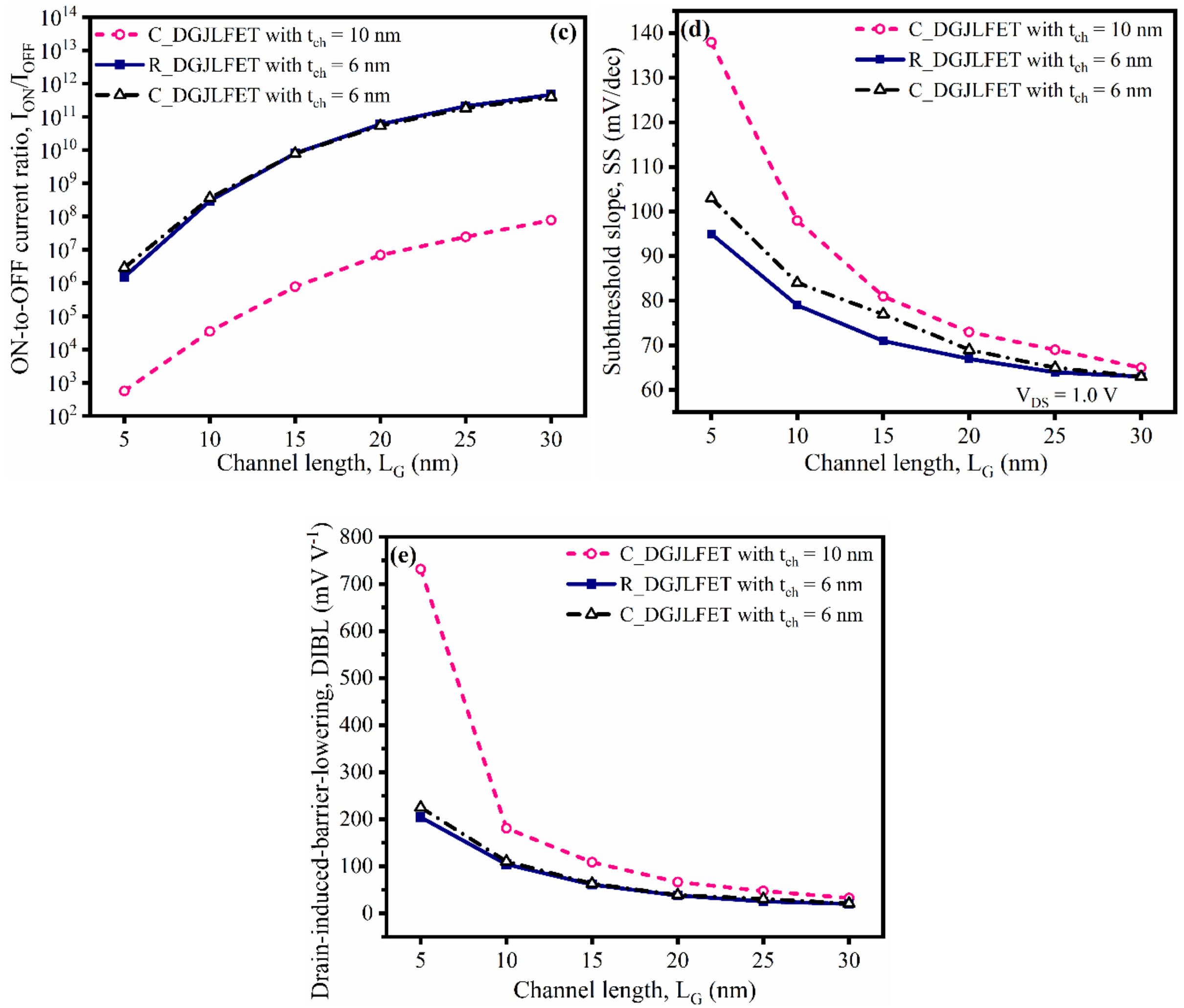


Figure 3.12 Effect of channel length scaling on various performance parameters of conventional and recessed DG JLFET (a) I_{OFF} (b) I_{ON} (c) I_{ON}/I_{OFF} (d) SS, and (e) DIBL.

The value of I_{ON}/I_{OFF} has been calculated by taking the value of I_{ON} and I_{OFF} for respective V_{DS}. In Figure 3.12(d) for SS, the V_{DS} of 1.0 V has been taken. As the channel length is scaled down from 30 nm to 5 nm the increased interaction between the drain and source results in a lowering of V_{TH} for both junctionless devices. However, the interaction between the drain and source is suppressed in the case of R_DGJLFET due to recessed silicon thickness under the gate region. Consequently, the R_DGJLFET shows much lower DIBL in comparison to C_DGJLFET as presented in Figure 3.12(e). The DIBL has been calculated by measuring the V_{TH} for V_{DS} = 50 mV (very low) and 1.0 V (= V_{DD}) using constant current method ($I_D = 1\times10^{-7}$ A) [109].

Quantitatively, the proposed R_DGJLFET reflects a ~43.83 % increment in SS and only a ~27.8 % rise in DIBL for the channel length scaling from 30 nm down to 5 nm. Additionally, the performance of the proposed R_DGJLFET has also been compared with C_DGJLFET having uniform silicon thickness i.e., t_{ch} = t_{si} as shown in Figure 3.12. Although both devices have the same channel thickness of 6 nm, the R_DGJLFET depicts more I_{ON} due to thicker

underlap silicon regions which allow more charge carriers in the device. The R_DGJLFET also reflects a smaller value of SS comparatively. However, the I_{OFF}, I_{ON}/I_{OFF} current ratio, and DIBL have been found comparable for both devices. Furthermore, the performance of the proposed DGJLFET has also been compared with various junctionless devices reported in the literature. For a fair comparison, all devices have been chosen for a channel length of 20 nm as listed in Table 3.2. In the table, it can be seen that the maximum value of I_{ON}/I_{OFF} has been achieved of the order 10^9 such as in the case of tri-gate junctionless MOSFET with P+ sidewall [146].

Table 3.2 The performance comparison of the proposed R_DGJLFET with other junctionless devices reported in the literature for L_G = 20 nm.

JLFET type	I_{ON} (A)	I_{OFF} (A)	I_{ON}/I_{OFF}	SS (mV/dec)	DIBL (mV V^{-1})
High-k spacer based DGJLFET, [70]	$\sim10^{-4}$	$\sim10^{-12}$	$\sim10^{8}$	~67	~31
Tunnel dielectric based JLT¸ [131]	$\sim10^{-6}$	$\sim10^{-13}$	$\sim10^{7}$	--	--
Trigate junctionless nanowire MOSFET with P^+ sidewall, [146]	$\sim10^{-5}$	$\sim10^{-14}$	$\sim10^{9}$	~63	~40
Dielectric separated independent gates junctionless transistor, [147]	$\sim10^{-6}$	$\sim10^{-12}$	$\sim10^{6}$	--	--
Vertical GAA nanowire JLT, [148]	$\sim10^{-6}$	$\sim10^{-14}$	$\sim10^{8}$	~65	~19
Dual-material DGJLFET, [149]	$\sim10^{-4}$	$\sim10^{-10}$	$\sim10^{6}$	~72	~70
Charge-plasma based JL C-FinFET¸ [150]	$\sim10^{-4}$	$\sim10^{-10}$	$\sim10^{6}$	~64.1	--
Proposed R_DGJLFET (present work)	$\mathbf{\sim10^{-4}}$	$\mathbf{\sim10^{-14}}$	$\mathbf{\sim10^{10}}$	**~67**	**~39**

Whereas, in most of the studies the improvement in SS and DIBL have been reported with a value of < 70 mV/dec and ~40 mV V^{-1}, respectively. Notably, the proposed R_DGJLFET reflects better performance with a higher I_{ON}/I_{OFF} ratio of the order $\sim10^{10}$. The SS and DIBL of the proposed device have also been found reasonably good with a value of 67.3 mV/dec and 39 mV V^{-1}, respectively. Conclusively, the proposed R_DGJLFET presents a strong alternative with remarkable performance among the different junctionless devices presented in the literature.

3.4.5 Effect of variations in depth and length of recessed silicon channel

Due to the work function difference between the gate metal and semiconductor material, the electric field in the silicon layer forces the mobile charge carriers to move away from the channel region in a junctionless FET [18]. The contour plot of the electric field for R_DGJLFET in OFF-state has been shown in Figure 3.13.

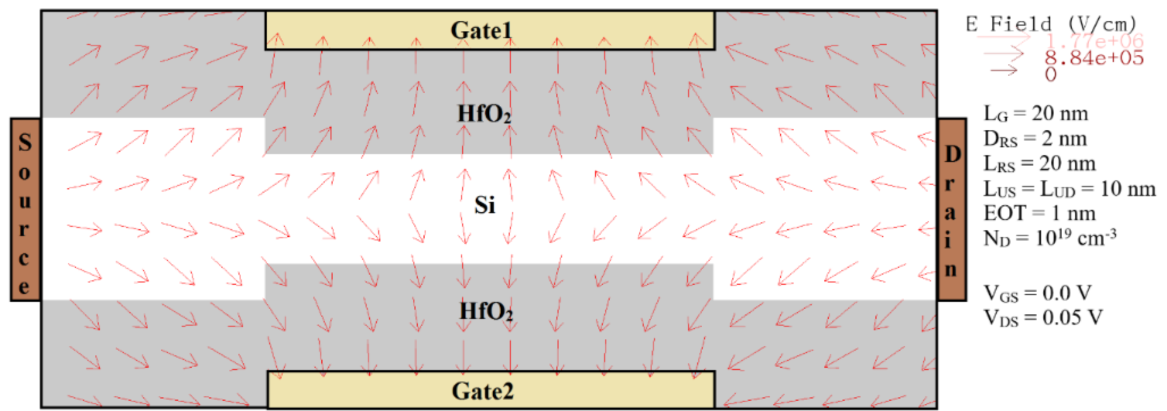


Figure 3.13 Contour plot of electric field for R_DGJLFET in OFF-state.

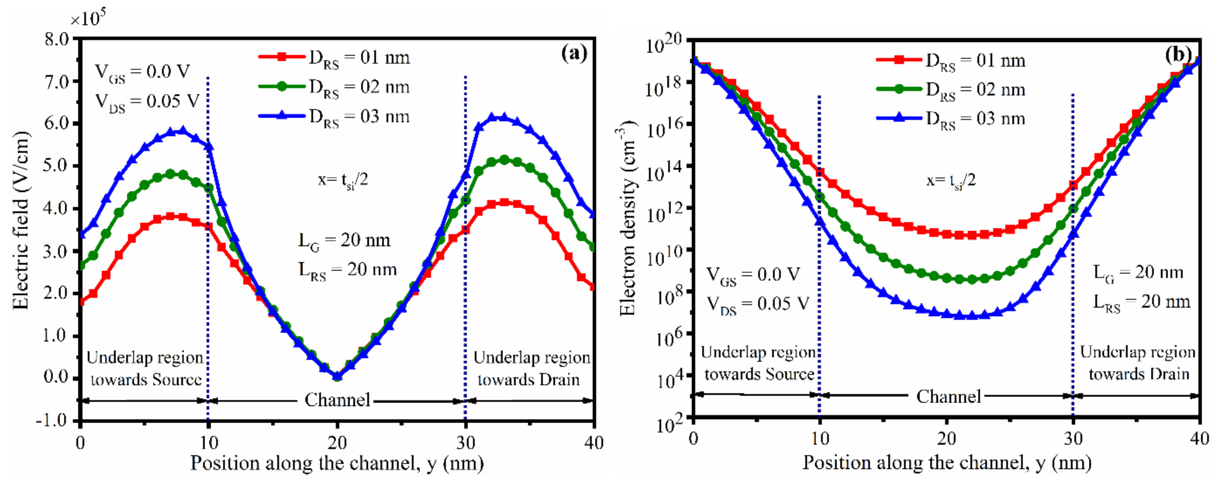


Figure 3.14 Effect of variations in D_{RS} on (a) electric field, and (b) electron density along the channel in R_DGJLFET.

For V_{GS} = 0.0 V, the electric field strength becomes stronger with a deeper recession of the silicon channel in R_DGJLFET as shown in Figure 3.14(a). The impact is more pronounced near the source/drain-channel interface. This reduces the electron density in the silicon layer as depicted in Figure 3.14(b). The smaller electron density leads to a significant reduction in I_{OFF} with considerable improvement in I_{ON}/I_{OFF} ratio as presented in Figure 3.15.

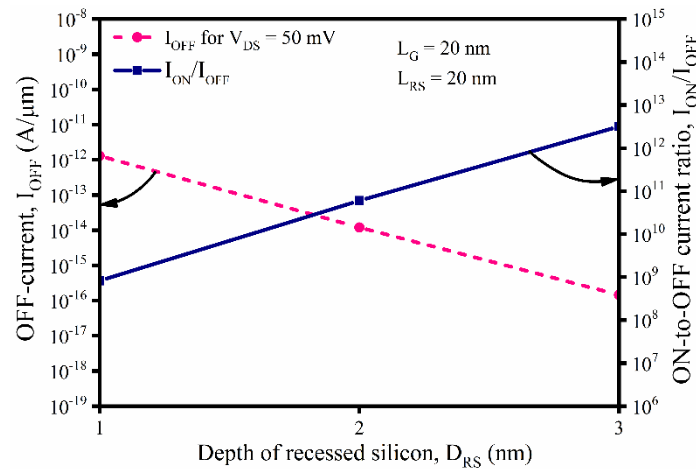


Figure 3.15 Effect of variations in D_{RS} on I_{OFF} and I_{ON}/I_{OFF} current ratio of R_DGJLFET.

Quantitatively, it has been observed that increasing the value of D_{RS} from 1 nm to 3 nm curtails the I_{OFF} by the order of ~10^{-4} A/µm, I_{ON}/I_{OFF} improves by the order of ~10^{4} while SS and DIBL improve by ~7.14 % and ~42.9 %, respectively in R_DGJLFET. However, recessing the silicon layer deeper increases the V_{TH} of the R_DGJLFET, which can lead to the degradation of g_m. Also, an increase in D_{RS} results in smaller channel thickness which curtails the number of charge carriers in ON-state i.e. I_{ON}. It may also increase the complexity of the fabrication of the device and its physical behaviour due to the strong impact of QCE. Hence, D_{RS} = 2 nm has been considered in the proposed R_DGJLFET, which results in better performance in comparison to C_DGJLFET with minimal impact on I_{ON} and its physical behaviour.

In R_DGJLFET the gate electrode is converted into a T-shape with a reduction in L_{RS} while maintaining a constant value of L_G and D_{RS} of 20 nm and 2 nm, respectively. For V_{GS} = 0.0 V, reducing the L_{RS} results in increased silicon thickness near the source-channel and drain-channel interfaces which diminishes the electric field in the silicon layer as shown in Figure 3.16(a). The reduced electric field allows more charge carriers in the silicon channel of R_DGJLFET as depicted in Figure 3.16(b).

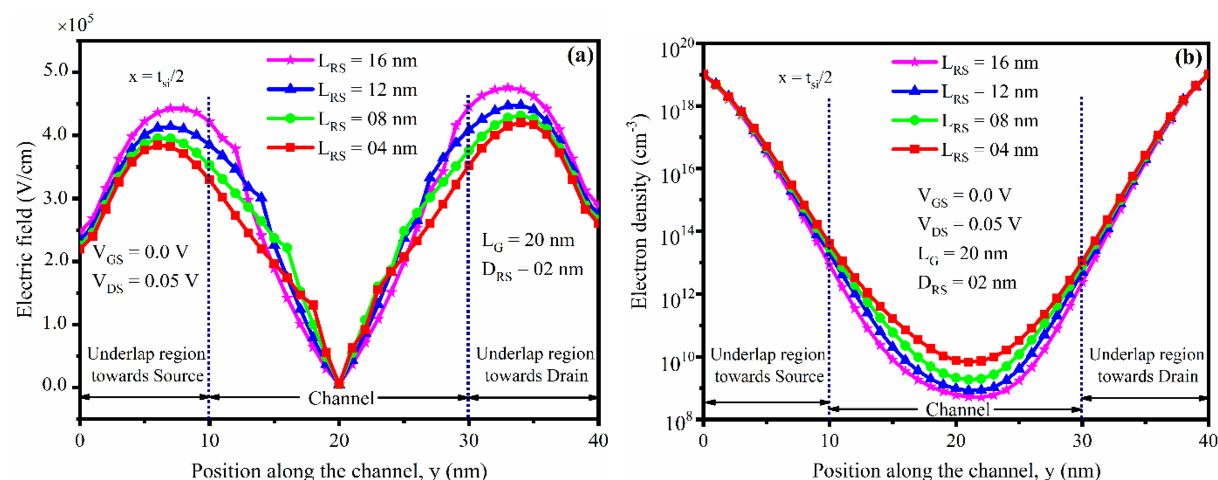


Figure 3.16 Effect of variations in L_{RS} on (a) electric field, and (b) electron concentration along the channel in R_DGJLFET.

This results in increased I_{OFF} and decreased I_{ON}/I_{OFF} as presented in Figure 3.17. Quantitatively, it has been observed that reduction in L_{RS} from 16 nm down to 4 nm increases the I_{OFF} by an order of ~10^{1} A/µm and I_{ON}/I_{OFF} degrades by the order of ~10^{1}. The I_{ON} is improved to the range of mA. The SS degrades by ~1.68 % and a minute increase of ~2.4 mV V^{-1} in DIBL has been observed. Since, reduction in L_{RS} results in overall performance degradation of R_DGJLFET, hence, its maximum value of 20 nm has been considered in the proposed structure. Comparing the impact of variations in D_{RS} and L_{RS} on the performance of

R_DGJLFET, it has been concluded that the device shows higher sensitivity to the variation in D_{RS} as compared to L_{RS}.

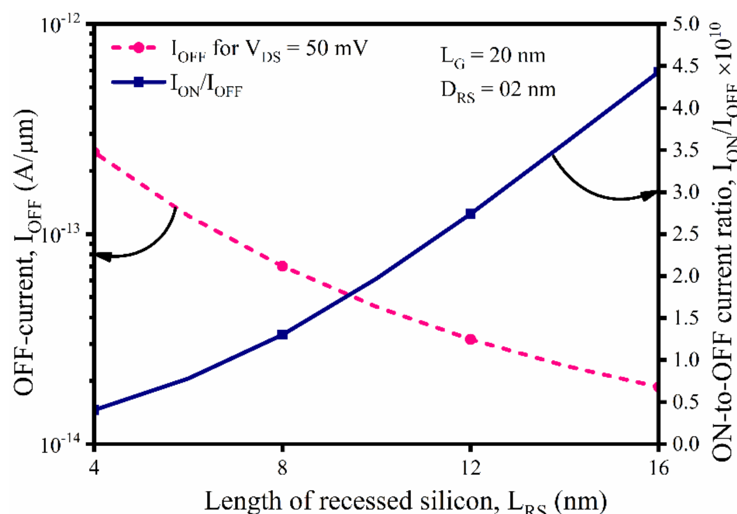


Figure 3.17 Effect of variations in L_{RS} on I_{OFF} and I_{ON}/I_{OFF} current ratio for R_DGJLFET.

Hence, the D_{RS} and L_{RS} of the recessed silicon area can be used as additional parameters for tuning the electrical performance of R_DGJLFET coarsely and finely. However, for performance optimization of R_DGJLFET, both D_{RS} and L_{RS} must be selected carefully.

3.4.6 Effect of variations in effective oxide thickness

Despite eliminating the p-n junctions, the scaling of channel length results in increased electrostatic interaction in the lateral direction between drain and source which leads to performance degradation of a JLFET. The lateral interaction can be suppressed by increasing the strength of the electric field in a direction perpendicular to the flow of electrons [151], which can be done with the application of gate material with a higher work function or by reducing the gate dielectric thickness. Applying the gate material with higher work function or reduction in gate dielectric thickness has been reported as a critical performance limiter along with associated process integration challenges [152][153]. For instance, the reduction in thickness of silicon-oxide (SiO_2) leads to increased gate-leakage current which has been addressed by using high-k dielectric materials such as Hafnium oxide (HfO_2). The high-k dielectrics offer similar charge-voltage (CV) characteristics for a specific EOT of SiO_2 [152]. Mathematically, the EOT can be defined as given by Eq. 3.9 [154]

$$\mathrm{EOT} = t_{h_k} \cdot \left(\frac{\kappa_{SiO_2}}{\kappa_{h_k}}\right) \tag{3.9}$$

where, t_{h_k} is the physical thickness of high-k dielectric material, κ_{SiO_2} and κ_{h_k} are the dielectric constant of SiO_2 and high-k dielectric material, respectively. Moreover, the deposition of high-k gate dielectric with precise EOT is also a challenging issue in nanoscale FETs [155]. Hence, in this work, the values of EOT have varied from 2.0 nm down to 0.8 nm.

The effect of variations in EOT on the performance of R_DGJLFET has been studied considering the value of κ_{SiO_2} and κ_{h_k} as 3.9 and 25, respectively [155].

3.4.6.1 Impact on physical properties of R_DGJLFET

The reduction in EOT boosts gate control with an increased vertical electric field which in turn increases the energy barrier in the silicon channel of both devices as shown in Figure 3.18(a), Figure 3.18(b), respectively. In the case of R_DGJLFET, the special placement of the gate electrode favours the electric field across the channel and restricts the presence of electrons in the silicon layer more efficiently. As a result, for a value of EOT, the height of the energy barrier is more in the case of R_DGJLFET than that of C_DGJLFET.

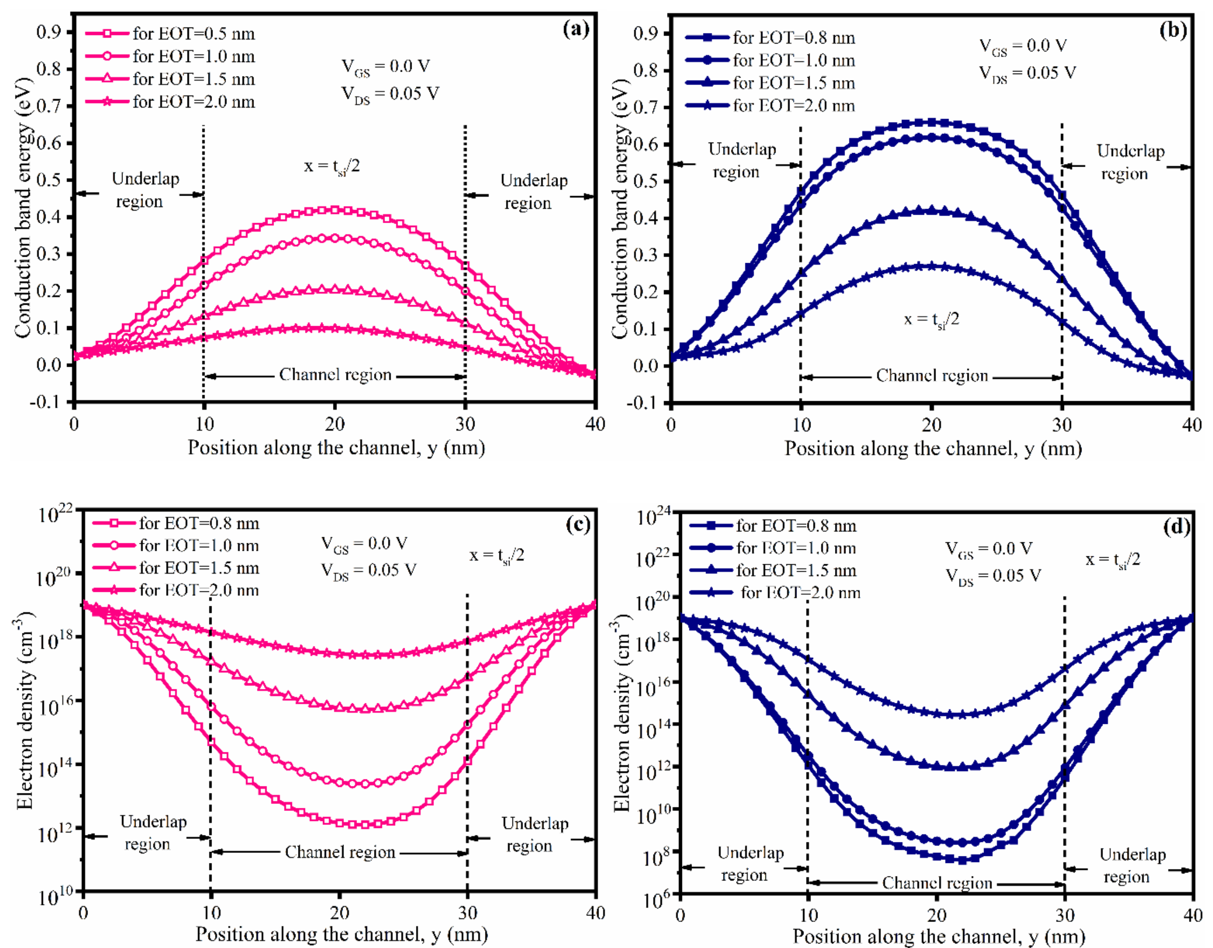


Figure 3.18 Effect of variations in EOT on conduction band energy and electron density (a) and (c) for C_DGJLFET, (b) and (d) for R_DGJLFET, respectively.

The improved gate control due to smaller EOT results in improved channel depletion in both devices which can be seen in terms of reduced electron density from Figure 3.18. However, the proposed R_DGJLFET depletes the channel more efficiently with a smaller electron density as presented in Figure 3.18(b).

3.4.6.2 Impact on performance parameters of R_DGJLFET

Figure 3.19 presents the I_D-V_{GS} curves for R_DGJLFET and C_DGJLFET for EOT of 0.8 nm and 2.0 nm. Here, it can be observed that in comparison to C_DGJLFET, the R_DGJLFET depicts smaller I_{OFF} for the specified values of EOT. Although, both devices have been designed considering the high-k gate dielectric material of equal EOT, interestingly, the I_D-V_{GS} curve for R_DGJLFET with EOT = 2.0 nm and C_DGJLFET with EOT of 0.8 nm are found almost similar.

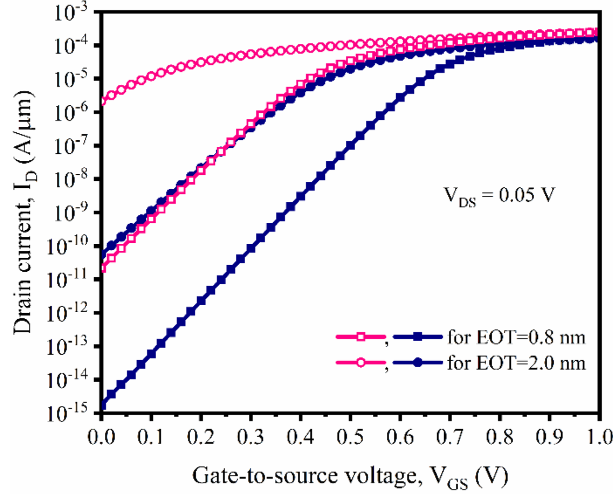


Figure 3.19 I_D-V_{GS} curves of R_DGJLFET (blue lines) and C_DGJLFET (pink lines) for EOT of 0.8 nm and 2.0 nm.

As the realization and characterization of the gate dielectric with smaller EOT nm are more challenging [156], hence, the proposed device can be used as an alternative to obtaining similar performance with relaxed gate dielectric dimensions. The variations in EOT also affect the V_{TH} of both devices. Mathematically, the relation between V_{TH} and the oxide thickness of a DG JLFET is represented in Eq. 3.10 [7]. Here, the t_{ox} should be understood in terms of EOT.

$$V_{TH} = V_{FB} - \frac{t_{si}}{8}\left(\frac{qN_D t_{si}}{\varepsilon_{si}} + \frac{4qN_D t_{ox}}{\varepsilon_{ox}}\right) \tag{3.10}$$

where V_{FB} is the flat band voltage of the junctionless device which is represented as the work function difference between the gate metal and semiconductor layer with consideration of ideal Si-HfO_2 interface, q is the electron charge, ε_{si} is the permittivity of silicon and ε_{ox} is the permittivity of the oxide layer. It is clear from Eq. 3.10 that lowering the EOT decreases the overall value of the term inside the parenthesis. Hence, with a constant value of V_{FB} the V_{TH} of a DG JLFET increases which influences the I_{OFF} and hence I_{ON}/I_{OFF}.

The I_{OFF} for conventional and recessed DG JLFET has been presented in Figure 3.20(a). It has been revealed that the reduction in EOT results in lowering the I_{OFF} for both DG JLFETs

due to increased V_{TH}. It has also been observed that the C_DGJLFET and R_DGJLFET reflect a reduction in I_{OFF} of ~10^{-5} A/µm and ~10^{-6} A/µm, respectively. Moreover, the I_{ON} has been reduced minorly as with reducing the EOT the improved gate control restricts the availability of electrons in the ON-state also. The R_DGJLFET shows a reduction of ~19.42 % in I_{ON} in comparison to ~11.02 % for C_DGJLFET.

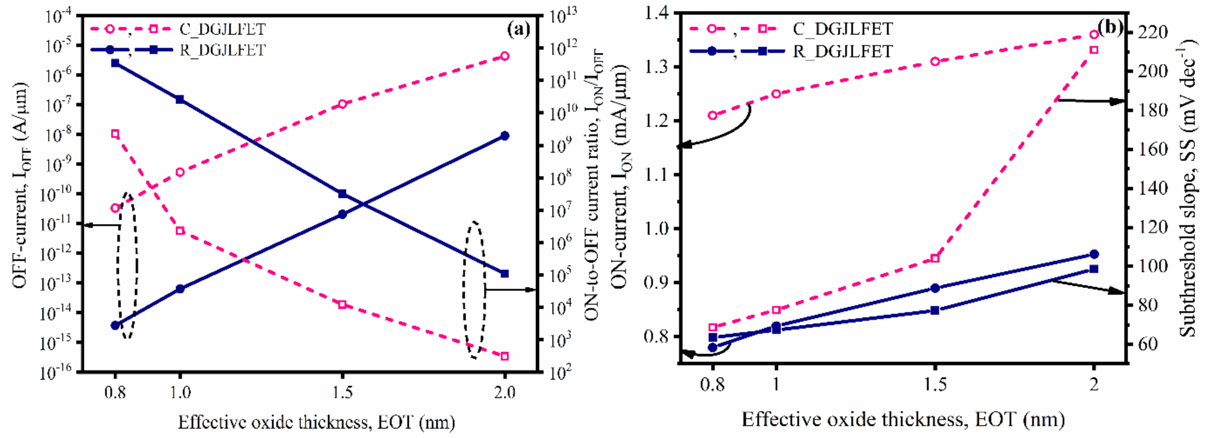


Figure 3.20 Effect of variations in EOT on (a) I_{OFF} and I_{ON}/I_{OFF} current ratio (b) I_{ON} and SS of R_DGJLFET and C_DGJLFET.

From Figure 3.20(a) and 3.20(b) the variations of I_{OFF} and I_{ON} have been observed on logarithmic and linear scales, respectively which results in improved I_{ON}/I_{OFF} as shown in Figure 3.20(a). Consequently, an improvement in I_{ON}/I_{OFF} of the order of ~10^5 and ~10^6 has been reflected by the C_DGJLFET and R_DGJLFET, respectively. The thinning of EOT also provides another souvenir with improved SS. This can be attributed to the increased proximity of the gate electrode to the silicon film which enhances its ability to switch the device more steeply.

For EOT=0.8 nm the R_DGJLFET shows near ideal subthreshold slope due to better gate influence in the silicon layer as shown in Figure 3.21(b). Hence, it has been concluded that due to comparable I_{ON}, lower I_{OFF}, and better I_{ON}/I_{OFF} with near-ideal SS, the R_DGJLFET can be used as a potential candidate for designing the low-power CMOS circuits with ultrathin nanoscale devices. Apart from the fluctuations in EOT, the variations in gate electrode work function can also lead to a significant impact on device performance, which has been discussed in the next subsection.

3.4.7 Effect of variations in gate work function

The effect of variations in gate work function from 4.6 eV to 5.6 eV on various performance parameters of R_DGJLFET namely I_{OFF}, I_{ON}, I_{ON}/I_{OFF}, and SS have been investigated. A range of work function values defined as work function window (WFW) has been found to obtain the optimum performance from the proposed R_DGJLFET for low-power applications.

The impact of different values of the work function of the two gate electrodes on R_DGJLFET has also been presented and it is found that the proposed R_DGJLFET reflects robustness with nearly constant SS in both symmetric and asymmetric modes.

3.4.7.1 Impact on physical properties of R_DGJLFET

In OFF-state, patterning the gate material of higher work function results in a higher electric field across the silicon channel which represents improved depletion of electrons. This leads to a lowering in the potential along the channel for both C_DGJLFET and R_DGJLFET as shown in Figure 3.21.

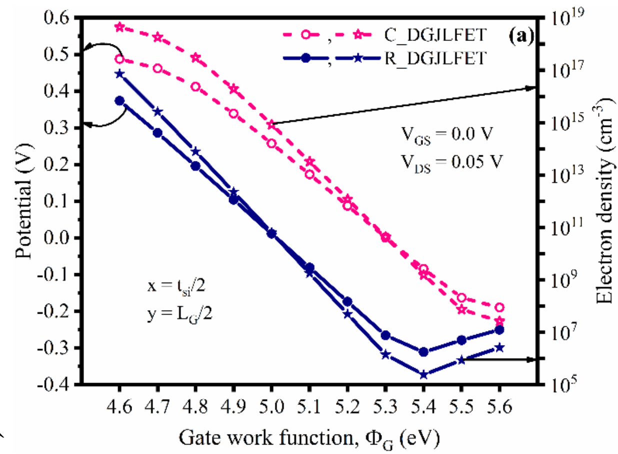


Figure 3.21 Effect of variations in gate work function on center potential and electron density of C_DGJLFET and R_DGJLFET.

In the case of R_DGJLFET for $\Phi_G > 5.3$ eV a rise in potential along the channel has been observed due to an increased BTBT effect in the device. The high value of Φ_G depletes the channel very strongly which converts the channel into a p-type. This results in more band bending and results in the considerable overlap between the valance band of the channel and the conduction band of the drain region. The tunneling across the thin energy barrier leads to increased potential and electron density [145] in R_DGJLFET as reflected in Figure 3.21.

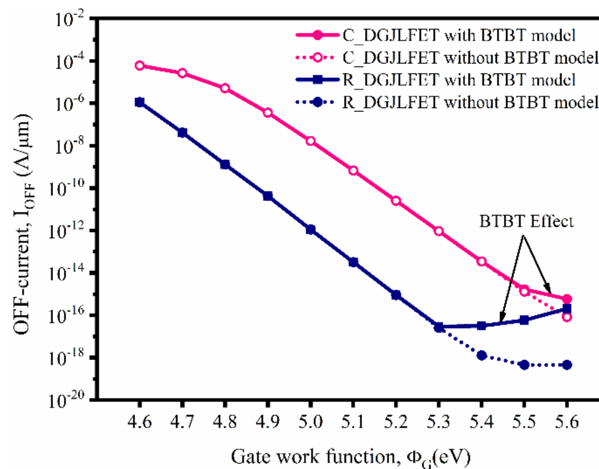


Figure 3.22 Increased I_{OFF} in C_DGJLFET and R_DGJLFET due to the effect of BTBT.

The effect of increased tunneling due to the higher value of Φ_G has been confirmed with the inclusion of the BTBT model in the simulation of C_DGJLFET and R_DGJLFET as shown in Figure 3.22. From Figure 3.22, it can be seen that the proposed R_DGJLFET reflects a considerable increase in I_{OFF} for $\Phi_G > 5.3$ eV considering the BTBT model. The phenomenon is completely absent without including the BTBT model and the I_{OFF} reduces continuously. However, the quality of channel depletion in C_DGJLFET is not enough to introduce the strong band-banding at the channel-drain interface and the effect is observed once Φ_G becomes > 5.5 eV.

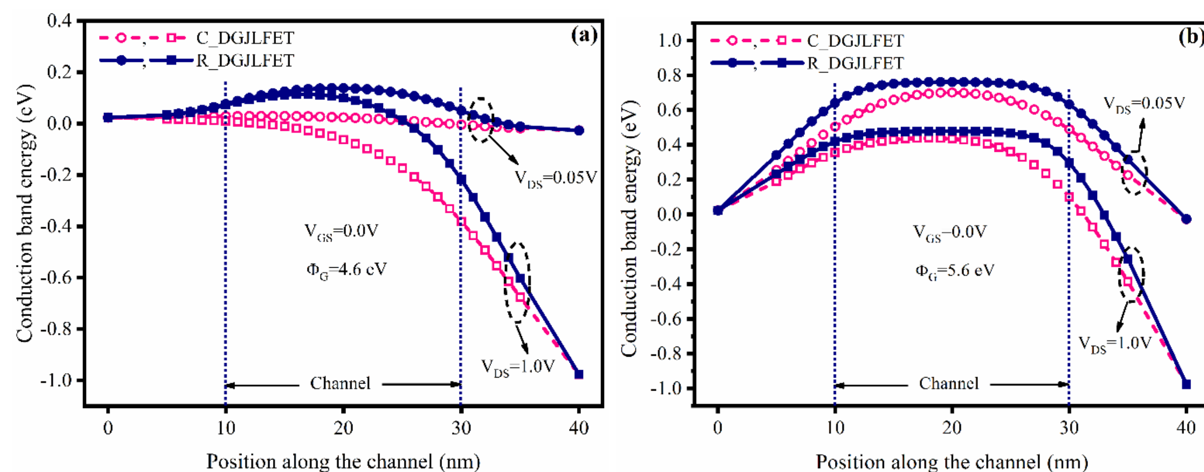


Figure 3.23 Conduction band energy along the channel in C_DGJLFET (pink lines) and R_DGJLFET (blue lines) for (a) $\Phi_G = 4.6$ eV, and (b) $\Phi_G = 5.6$ eV.

In Figure 3.23(a) and Figure 3.23(b), the conduction band energy along the channel has been shown for C_DGJLFET and R_DGJLFET, respectively. From Figure 3.23(a) it has been observed that for $V_{GS} = 0.0$ V and $V_{DS} = 0.05$ V, the C_DGJLFET reflects an almost flat energy barrier in the channel region, hence, the channel is fully conductive, whereas the R_DGJLFET offers significant barrier height, hence, the channel is depleted comparatively.

In Figure 3.23(b) the higher energy barrier in the channel region has been observed for R_DGJLFET due to its higher V_{TH} as compared to C_DGJLFET. However, in Figure 3.23, the flat energy band for R_DGJLFET reflects that the maximum level of channel depletion has been already achieved in the device for a smaller value of Φ_G. Hence, in the proposed R_DGJLFET, increasing the value of $\Phi_G > 5.3$ eV is not recommended as it can degrade the device performance.

3.4.7.2 Variations in equal work functions for both gate electrodes

The I_D-V_{GS} characteristics in linear mode for the C_DGJLFET and R_DGJLFET have been shown in Fig 3.24. From Figure 3.24, it has been observed that with increasing the value of Φ_G the I_D-V_{GS} characteristics shift from left to right as it linearly impacts the threshold voltage of the device as given in Eq. 3.11 [157].

$$V_{TH} = \Delta\phi_G + V_t \ln\left(\frac{N_D}{n_i}\right) - qN_D t_{si}\left(\frac{1}{2C_{ox}} + \frac{1}{8C_{si}}\right) \quad (3.11)$$

where $\Delta\Phi_G$ is the change in gate work function, V_t is the thermal voltage, n_i is the intrinsic carrier concentration, q is the charge on the electron, C_{ox} is the gate oxide capacitance and C_{si} is the capacitance of silicon film. Moreover, it can also be noticed that a higher value of Φ_G results in larger variations in I_D for negative values of V_{GS} in both junctionless devices.

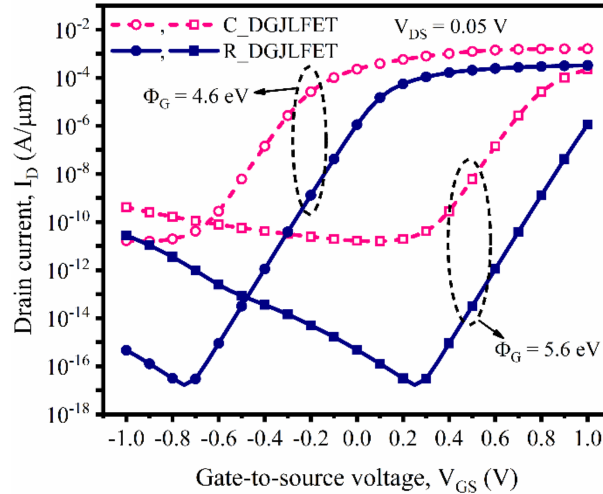


Figure 3.24 Effect of variations in Φ_G on I_D-V_{GS} characteristics of C_DGJLFET (pink lines) and R_DGJLFET (blue lines).

For $V_{GS} < 0.0$ V, the proposed device shows a higher current which reflects that the device is more prone to the gate-induced-drain-leakage effect. In addition, the value of Φ_G makes a significant impact on device OFF-state and ON-state behaviour, which leads to a reduction in I_{OFF} with a penalty in terms of I_{ON}. Hence, the higher value of Φ_G is not advisable neither for conventional nor for proposed DG JLFET. This necessitates estimating the value/range of gate work function in which the device can reflect optimum performance.

To do so, the effect of variations in Φ_G on the various performance parameters of R_DGJLFET has been compared with C_DGJLFET and an existing core-shell double gate junctionless field-effect-transistor (CS_DGJLFET) modeled by Jaiswal and Kranti [112]. It has been found that the V_{TH} of the proposed R_DGJLFET (V_{TH_R}) remains positive for the entire range of Φ_G from 4.6 eV to 5.6 eV due to its higher energy barrier in the channel region. But, for $\Phi_G > 5.3$ eV the V_{TH_R} starts becoming comparable to V_{DD} which can lower the gate drive.

Whereas the V_{TH} of C_DGJLFET (V_{TH_C}) and CS_DGJLFET (V_{TH_CS}) becomes negative for lower values of Φ_G. The V_{TH_C} becomes very small for $\Phi_G < 5.0$ eV the device may conduct in OFF-state. This might restrict the applicability of C_DGJLFET for low-power applications. Thus, a reasonable range of work function values from 5.0 eV to 5.3 eV has been identified to

obtain optimum performance from both C_DGJLFET, and R_DGJLFET, defined as a work function window (WFW).

From Figure 3.25(a), it can be noticed that the proposed R_DGJLFET depicts the lowest I_{OFF} among the three JLFETs due to its better gate control over the channel. Here, the rise in I_{OFF} for R_DGJLFET (I_{OFF_R}) for higher values of Φ_G is attributed to a more pronounced BTBT effect. Moreover, for V_{GS} = 1.0 V and V_{DS} = 1.0 V the entire silicon film becomes neutral and achieves maximum electron density [18]. In such conditions operating with higher values of Φ_G lowers the electron density in the channel which leads to a reduction in I_{ON} as shown in Figure 3.25(b). The overall effect results in considerable improvement in I_{ON}/I_{OFF}.

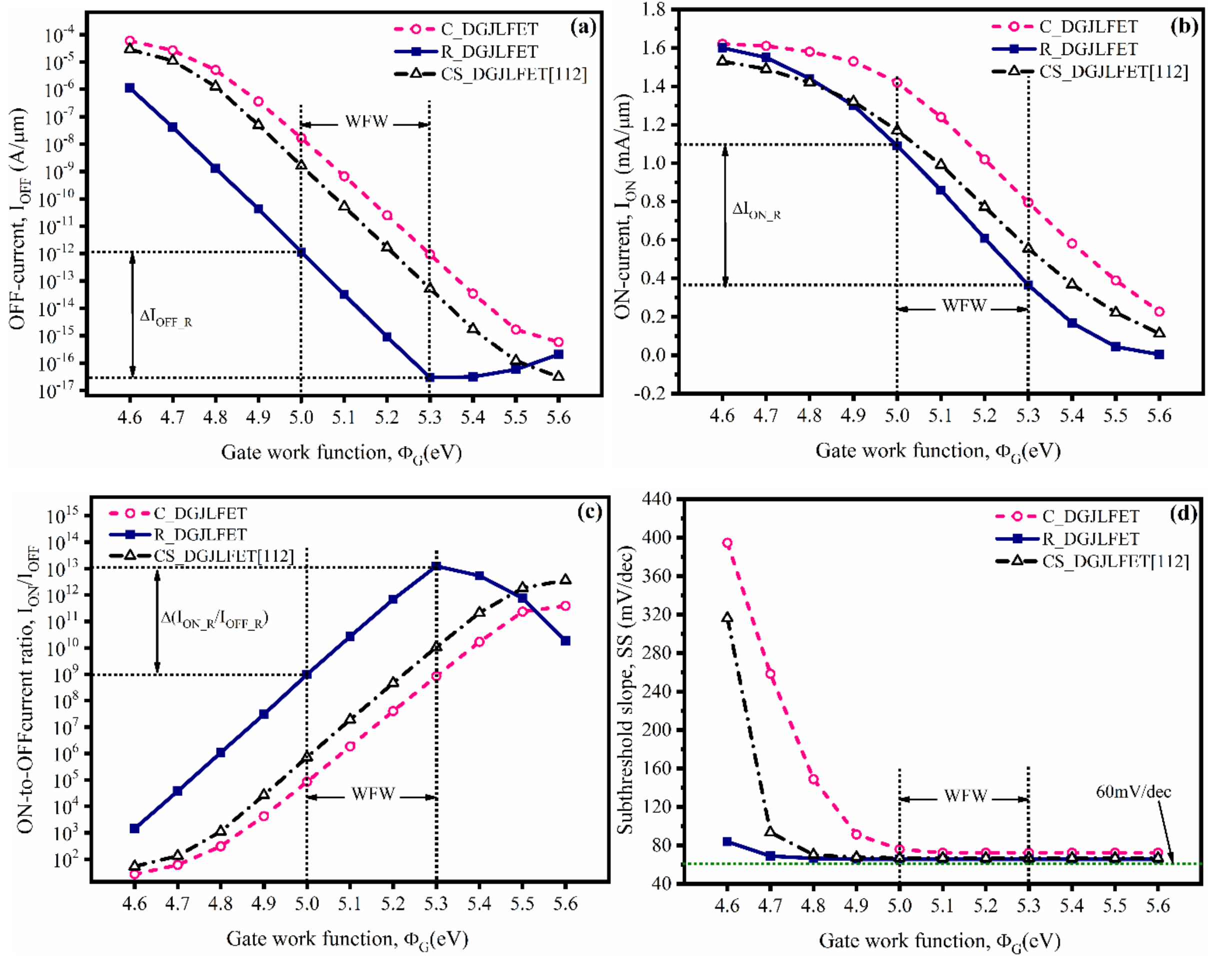


Figure 3.25 Effect of variations in Φ_G on various performance parameters of R_DGJLFET, C_DGJLFET, and CS_DGJLFET [112] namely (a) I_{OFF} (b) I_{ON} (c) I_{ON}/I_{OFF}, and (d) SS.

In Figure 3.25(c) it has been shown that the I_{ON}/I_{OFF} of the proposed R_DGJLFET (I_{ON_R}/I_{OFF_R}) is significantly higher than the C_DGJLFET and CS_DGJLFET due to its lower I_{OFF}. Moreover, in comparison to C_DGJLFET and CS_DGJLFET the proposed R_DGJLFET reflects a smaller value of SS for the entire range of Φ_G. Also, on the left side of WFW, the SS of C_DGJLFET and CS_DGJLFET rises sharply whereas a small increase in SS has been observed for the proposed R_DGJLFET. With smaller variations in SS, the

R_DGJLFET shows robustness against variations of Φ_G in symmetric mode i.e., equal values of work functions for the two gate electrodes.

3.4.7.3 Variations in different work functions both gate electrodes

As the R_DGJLFET is based on DG structure, hence, it also facilitates work in asymmetric mode i.e. different values of work functions for the two gate electrodes. The device shows the asymmetric potential distribution in the channel region, which facilitates the dynamic control over V_{TH} and other performance parameters such as I_{OFF}, I_{ON}/I_{OFF}, SS, etc.

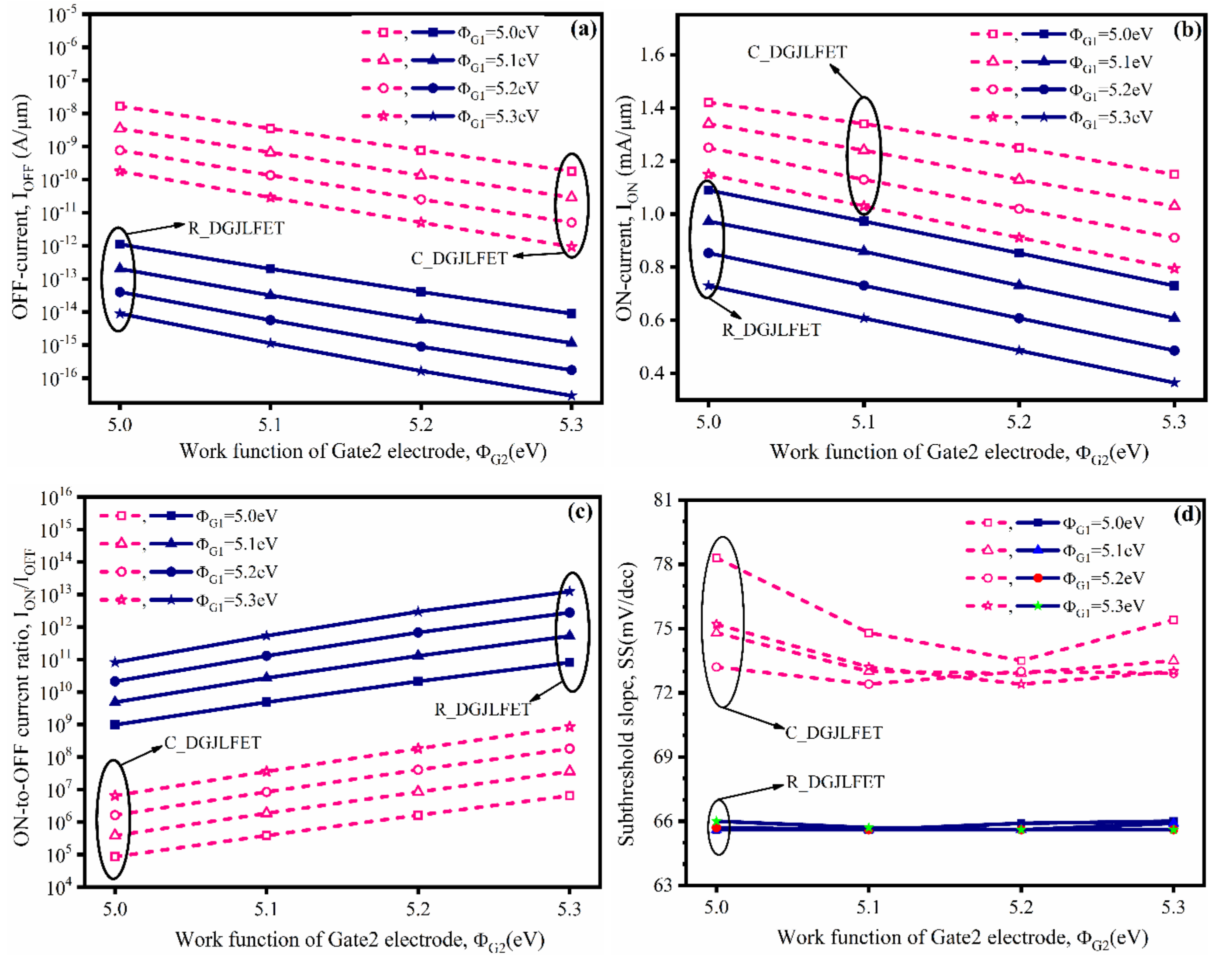


Figure 3.26 Effect of variations in Φ_{G1} and Φ_{G2} on various performance parameters of R_DGJLFET, C_DGJLFET namely (a) I_{OFF} (b) I_{ON} (c) I_{ON}/I_{OFF}, and (d) SS.

In Figure 3.26, the performance of R_DGJLFET has been compared with C_DGJLFET in asymmetric mode. As explained earlier that both of these devices can show optimum performance in the WFW. Hence, in asymmetric mode, the effect of work function for Gate1 and Gate2 electrodes has also been studied in WFW. In Figure 3.26(a) it has been observed that for fixed Φ_{G1} increasing the value of Φ_{G2} results in suppression of I_{OFF} in the R_DGJLFET due to improved depletion of electrons in the channel region. However, the I_{ON} reduces minutely with an increase in Φ_{G2} as well as Φ_{G1} as shown in Figure 3.26(b).

More I_{ON} can be achieved by lowering the values of both Φ_{G1} and Φ_{G2}. The C_DGJLFET shows a similar inclination with the higher value of I_{OFF} and I_{ON}. The impacts of variations in Φ_{G1} and Φ_{G2} on I_{ON}/I_{OFF} and SS of C_DGJLFET and R_DGJLFET have been shown in Figure 3.26(c) and Figure 3.26(d), respectively. From Figure 3.26(c) it has been noticed that the improved values of I_{ON}/I_{OFF} can be achieved with higher values of Φ_{G1} and Φ_{G2} in WFW. With reduced I_{OFF} the R_DGJLFET shows better I_{ON}/I_{OFF} comparatively.

Moreover, the R_DGJLFET reflects negligible changes in SS for the variations in Φ_{G1} and Φ_{G2} as compared to C_DGJLFET. As depicted in Figure 3.26(d), with almost constant SS, the proposed R_DGJLFET provides greater flexibility for tuning the I_{OFF} and I_{ON}/I_{OFF} in comparison to C_DGJLFET and reflects robustness in asymmetric mode too.

3.4.8 Effect of misalignment on the performance of R_DGJLFET

As the proposed device is a recessed double gate structure, hence, in case of R_DGJLFET the misalignment should be understood in terms of shifting the recessed silicon area towards the source/drain over which the gate electrode has been patterned. Whereas, in C_DGJLFET the misalignment reflects the shifting of the gate electrode towards the source/drain as there is no recessed silicon channel. In the proposed R_DGJLFET, the effect of misalignment has been studied by shifting the recessed silicon channel under the Gate2 electrode towards the source/drain sides with a maximum length of 8 nm, while fixing the position of the Gate1 electrode as shown in Figure 3.27.

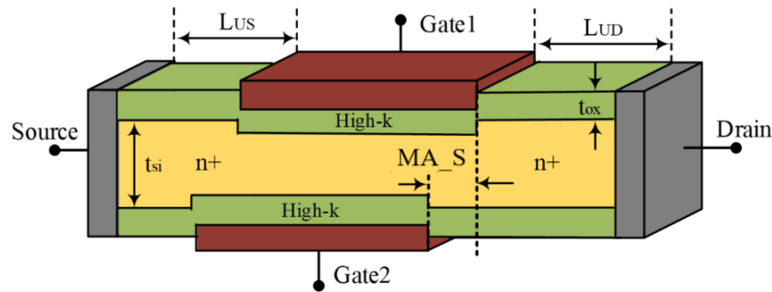


Figure 3.27 The 3-D schematic view of R_DGJLFET with misalignment towards source.

The misalignment influences the physical properties of R_DGJLFET as it causes a reduction in overlapped silicon channel between Gate1 and Gate2 electrodes which is maximum in case of perfect alignment (i.e., MA_S/D=0 nm). The electric field distribution becomes asymmetric which lowers the energy barrier in the silicon layer. This eases the transportation of electrons from the source to the drain and leads to higher electron density in the channel. Hence, both I_{ON} and I_{OFF} increases with misalignment towards source/drain (i.e., MA_S/MA_D) as shown in Figure 3.28(a) and Figure 3.28(b), respectively.

Nevertheless, for V_{DS}=1.0 V the device is operating in/or above the flat-band condition i.e. the electron density in the channel approaches its maximum value, hence, the I_{ON} increases minorly in comparison to I_{OFF}. Eventually, a reduction in I_{ON}/I_{OFF} ratio has been observed as shown in Figure 3.28(b). Furthermore, the variations in SS and DIBL for R_DGJLFET are relatively smaller even for MA_D > 4 nm as depicted in Figure 3.29. From Figure 3.28(b) and Figure 3.29(b), it can also be observed that in comparison to the source side, the misalignment towards the drain affects the performance parameters more severely which reflects poorer gate control over the channel.

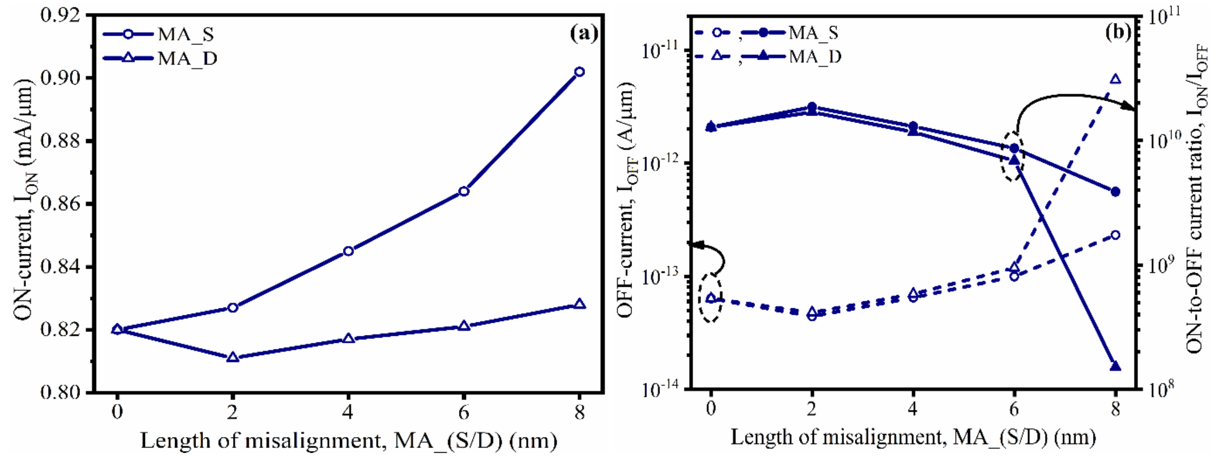


Figure 3.28 Effect of misalignment on (a) I_{ON}, and (b) I_{OFF} and I_{ON}/I_{OFF} of R_DGJLFET.

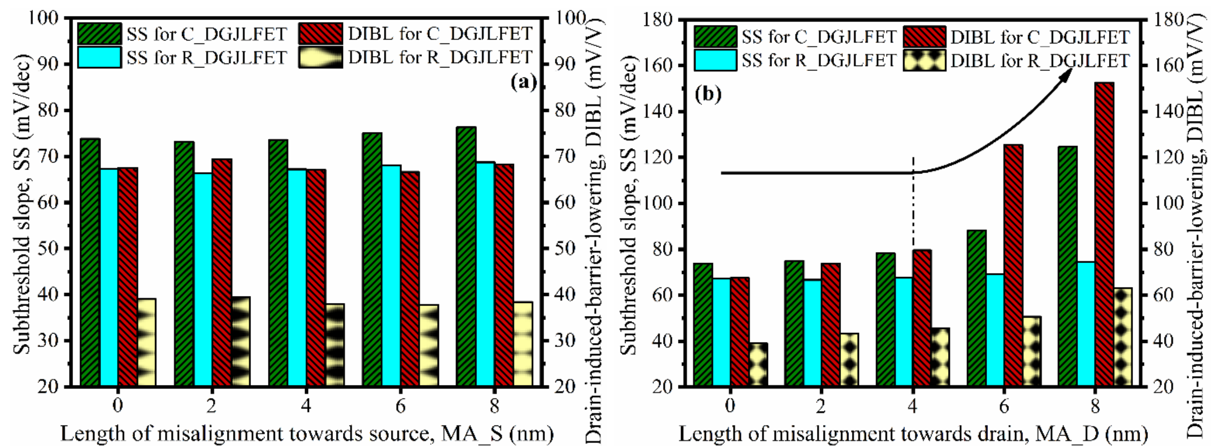


Figure 3.29 Effect of misalignment on (a) SS, (b) DIBL of C_DGJLFET and R_DGJLFET.

In the latter case the effect of drain voltage upsurges with increase in misalignment towards drain which promotes the degradation of channel depletion. The significant increase in I_{OFF} with MA_D also degrades the transconductance (g_m) [158] whereas relatively higher I_{ON} results in improved g_m with MA_S.

However, the parasitic total gate-to-gate capacitance (C_{gg}) gets reduced with misalignment on either side. The value of C_{gg} has been calculated by adding the values of gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}) which were obtained by applying a signal frequency of 1 MHz at V_{DS}= 0.05 V in TCAD tool. The effect of MA_S/MA_D on g_m

and parasitic gate capacitances further affects the TGF [158], f_T [158], and GBW [40] of the device as shown in Figure 3.30.

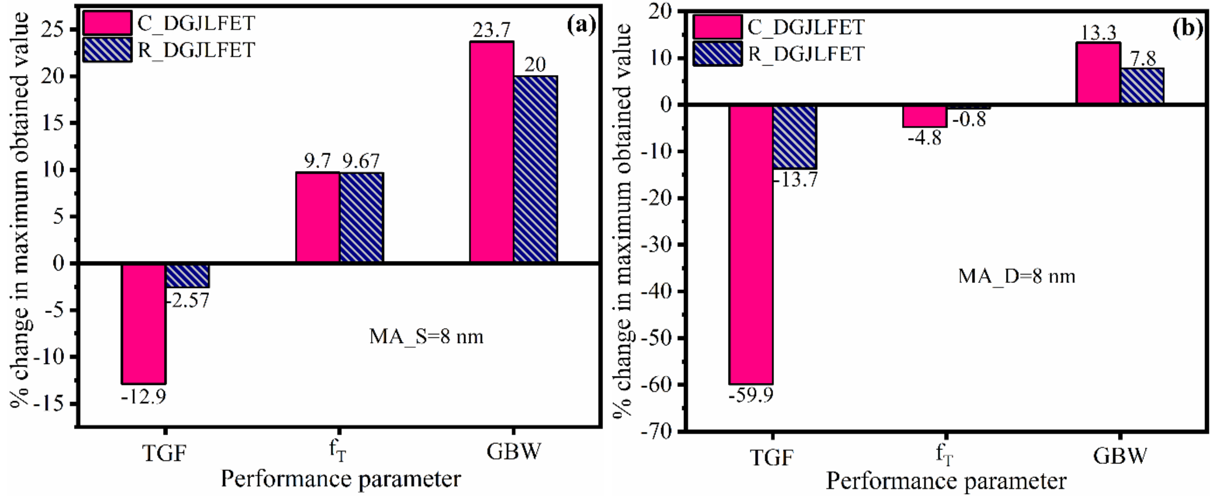


Figure 3.30 Percentage change in the maximum value of analog/RF performance parameters of C_DGJLFET and R_DGJLFET with misalignment (a) towards source (b) towards drain.

The bar diagram shown in Fig 3.30 depicts the effect of misalignment on the % change in the maximum obtained value of TGF, $f_{T,}$ and GBW for C_DGJLFET and R_DGJLFET. The positive/negative values show the increment/reduction in the maximum value of the performance parameters. From Figure 3.30 it can be observed that the misaligned R_DGJLFET depicts a smaller variation in these performance parameters as compared to the misaligned C_DGJLFET. Conclusively, the deprived performance changes against misalignment towards source/drain in terms of SS, DIBL, TGF, f_T, and GBW reflects the robustness of R_DGJLFET.

3.5 Conclusions

In this chapter, the TCAD tool-based simulation results of the proposed n-type R_DGJLFET have been presented. It has been noticed that the structural engineering with recessed silicon thickness between the two gate electrodes effectively helps to achieve improved channel depletion by restricting the number of electrons in OFF-state. Consequently, for a channel length of 20 nm, the R_DGJLFET reflects better performance with smaller I_{OFF} (~10^{-14} A/µm), higher I_{ON}/I_{OFF} (~10^{10}), steeper SS (~67 mV/dec), and lower DIBL (~39 mV V^{-1}) in comparison to C_DGJLFET. The investigation provides the guidelines to efficiently design the R_DGJLFET and optimize its performance through channel and gate engineering. It has been presented that due to reduced silicon thickness in R_DGJLFET, the interaction between drain and source is suppressed, hence, the device maintains its performance edge over the C_DGJLFET with smaller SCEs while scaling the L_G. In addition, the effect of variations in

D_{RS} and L_{RS} has been illustrated and found that these parameters can be used for coarse and fine-tuning of the performance of R_DGJLFET, respectively.

Focusing on the design of the gate electrode, the reduction in EOT improves the gate controllability in the channel which leads to better performance of R_DGJLFET. It has been concluded that the R_DGJLFET continuously outperforms the C_DGJLFET for different EOT with its smaller I_{OFF}, higher I_{ON}/I_{OFF}, and lesser SS, and offers comparable I_D-V_{GS} characteristics with relaxed gate dielectric dimensions. Furthermore, the performance of R_DGJLFET has also been investigated for equal and different values of Φ_G for the two gate electrodes. It has been concluded that increasing the value of Φ_G improves the gate controllability over the channel region which leads to a reduction in I_{OFF} with improved I_{ON}/I_{OFF}.

However, keeping a view on the value of V_{TH}, a range of Φ_G from 5.0 eV to 5.3 eV has been found for obtaining the optimum performance from R_DGJLFET and C_DGJLFET. It has been observed that the proposed R_DGJLFET shows improved electrical performance with lower I_{OFF}, better I_{ON}/I_{OFF}, and smaller variations SS as compared to C_DGJLFET in both symmetric and asymmetric modes. Thus, the proposed R_DGJLFET can be used as a potential candidate in low-power applications [42][77][79][123][124][127]. Moreover, the proposed R_DGJLFET depicts robustness against misalignment with smaller performance variations in terms of SS, DIBL, TGF, f_T, and GBW.

Chapter-4
Proposed recessed double gate JLFET based digital logic gates

4.1 Introduction

In conventional double gate JLFET (C_DGJLFET) the feebly controlled channel region by the gate electrode results in an increased I_{OFF} current. Nonetheless, the proposed recessed0020double gate JLFET (R_DGJLFET) efficiently depletes the channel region with stronger gate control and depicts improved performance in terms of smaller I_{OFF}, improved I_{ON}/I_{OFF} current ratio, steeper SS, and lesser DIBL. However, the ultimate goal of proposing a nanoscale semiconductor device is to use it in electronic circuits targeting digital and/or analog applications.

The performance of conventional DG JLFET has also been investigated in both digital and analog circuits [34-38, 41, 121, 160-165]. In digital circuit applications, Munteanu *et al.* [34] have designed a 6T based SRAM cell based on DG JLFET and reported that it is more immune to radiations in comparison to inversion mode (IM) SOI SRAM. Tayal *et al.* [35] have studied the performance of 6T SRAM cells using a high-k dielectric based junctionless nanotube and reported the improvement in read and write access times using TiO_2. Baidya *et al.* [121] have investigated the effect of variations in the dielectric constant of gate oxide on the performance of DG JLFET based logic gates. Guin *et al.* [38] have reported that junctionless FinFET based inverter reflects the improved rise and fall time despite minutely smaller ON-current in comparison to IM FinFET based corresponding circuits. Panchore *et al.* [159] have designed 11 stage ring oscillator and SRAM cell based on DG JLFET with a doping-less channel. The circuits reflect better performance against hot carrier effects with smaller degradation in drain current as compared to conventional DG JLFET based circuits.

Ansari *et al.* [36] have demonstrated the advantages of a shell-doped JLFET in 1T dynamic random-access memory (DRAM) with higher RT even at increased temperature. G. Guisi [37] has shown that the RT is severely limited by TAT in junctionless transistor based floating body DRAM. Garg *et al.* [39] have reported that the introduction of interface charges during the manufacturing process strongly affects the reliability of p-type JLFETs due to changes in V_{TH}, which reasons for a maximum shift in voltage transfer characteristics (VTC) in the case of a uniform doping profile-based inverter.

On the other side in the analog circuit domain, Doria *et al.* [164] reported that the n-type multigate JLFET shows better analog performance in terms of larger Early voltage (V_{EA}) and

intrinsic voltage gain (A_V) than the IM counterpart. Gosh *et al.* [41] have presented that the due to the smaller peak of the electric field on the gate edge near the drain end; the immense potential of JLFET for ultra-low power analog and radio frequency (RF) applications with $I_{DS} \leq 30$ µA/µm is credited to improvement in V_{EA} and A_V. Lakshmi *et al.* [160] have studied the effect of variations in different process parameters such as fin width, height, oxide thickness, doping concentration, and gate length on the unity-gain frequency (f_T) of JLFET.

Lu *et al.* [161] have demonstrated that the fluctuations in gate work function (Φ_G) result in smaller variations in V_{TH} for GAA nanowire FET but worse g_m in comparison to junctionless FinFET. Barman *et al.* [162] have shown that considerably larger f_T and gain-bandwidth product (GBW) can be achieved in a vertical JLFET with a super thin body using high-k dielectric and increasing the substrate doping [163].

The research work carried out on circuit applications based on conventional JLFETs motivates us too for investigating the efficacy of the proposed R_DGJLFET at the circuit level. The circuit applicability has been studied by implementing various digital logic gates namely NOT gate, 2-input NAND, and NOR gate, and an important analog building block namely common-source (CS) amplifier based on the proposed R_DGJLFET. The R_DGJLFET based inverter reflects steeper VTC, wider noise margins, and smaller short-circuit current (I_{SC}) expressing its suitability for low-power applications. Whereas, the CS amplifier based on R_DGJLFET shows a higher value of voltage gain (~4.75) in comparison to C_DGJLFET.

4.2 Results and discussions

Table 4.1 Performance comparison between C_DGJLFET and R_DGJLFET.

DGJLFET type	**I_{ON} (A/µm)**	**I_{OFF} (A/µm)**	**I_{ON}/I_{OFF}**	**SS (mV/dec)**	**DIBL (mV/V)**
C_DGJLFET	1.2×10^{-3}	3.88×10^{-10}	3.1×10^{6}	73.8	67.5
R_DGJLFET	8.2×10^{-4}	6.36×10^{-14}	1.28×10^{10}	67.3	39.0

Unless it has been mentioned, the device structure (refer to Figure 3.1 and Table 3.1) and simulation set-up for chapter-4 remain the same as described previously in sections 3.2, and 3.3 of chapter-3, respectively. The noteworthy performance of R_DGJLFET (shown in Table 4.1) persuades us to further investigate the working reliability of the proposed R_DGJLFET in digital logic circuits i.e., NOT gate, 2- input NAND and NOR gate implemented with a V_{DD} of 1.0 V as described in subsections 4.2.1, 4.2.2, and 4.2.3, respectively.

4.2.1 R_DGJLFET based NOT gate

The NOT gate i.e. inverter based on C_DGJLFET (INV1) and R_DGJLFET (INV2) has been implemented and simulated in the mixed-mode simulator of Silvaco Atlas TCAD [137]. The circuit diagram of the implemented inverter has been shown in Figure 4.1 [1].

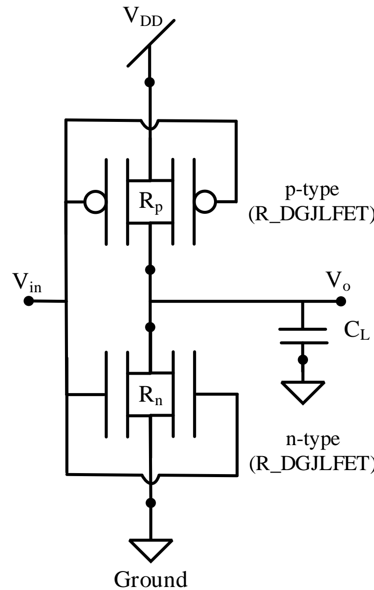


Figure 4.1 Circuit diagram for R_DGJLFET based NOT gate [1].

The pull-up and pull-down networks have been implemented using specific physical attributes for PMOS and NMOS devices, respectively. The gate width of NMOS devices (W_n) has been fixed to 1.0 µm in both INV1 and INV2 while the gate width for PMOS devices (W_p) has been increased to 1.8 µm and 4.1 µm, respectively to obtain symmetric transient behaviour. The load capacitance (C_L) has been connected at the output node which is a multiple of gate-to-gate capacitance (C_{gg}).

4.2.1.1 The DC analysis of R_DGJLFET based inverter

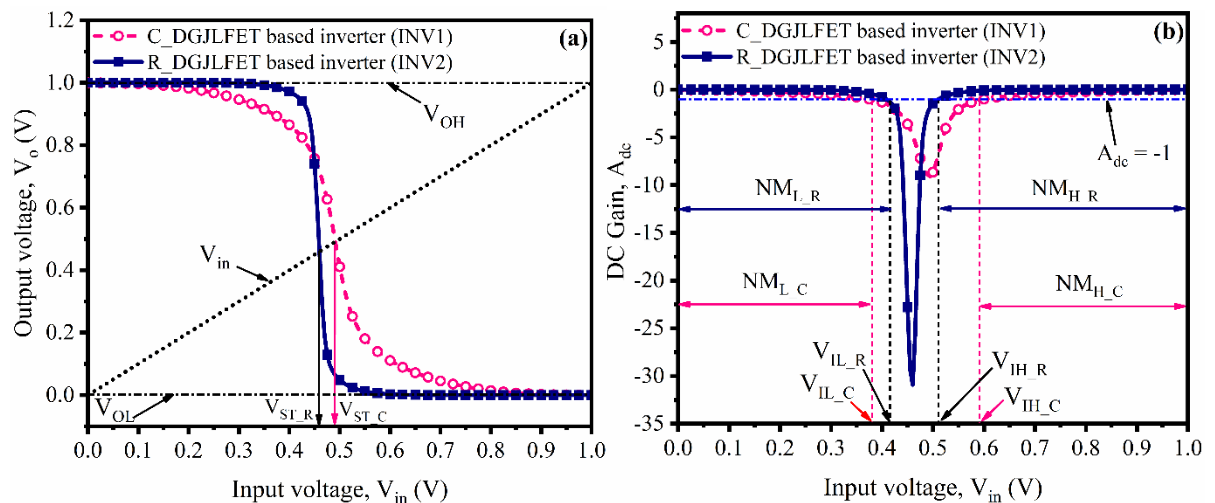


Figure 4.2 Comparison of (a) VTC, and (b) DC voltage gain of INV1 and INV2 with $V_{DD} = 1.0$ V.

The simulation results for DC analysis of INV1 and INV2 have been shown in Figure 4.2. From Figure 4.2(a) it can be observed that both inverters are capable to achieve maximum output voltage considered to be 'HIGH' (V_{OH} = 1.0 V) and minimum output voltage to be considered 'LOW' (V_{OL} = 0.0 V). The slope of VTC reflects the quality of an inverter. The INV2 switches more abruptly in comparison to INV1. Due to better gate control in R_DGJLFET, the number of charge carriers in the channel region are smaller, which aids to remain in the cut-off region for a larger voltage range in comparison to C_DGJLFET. Hence, INV2 reflects sharper VTC in comparison to INV1. The switching threshold voltage (V_{ST}) for INV1 and INV2 has been founded as 0.49 V and 0.46 V, respectively. In Figure 4.2(b) the DC voltage gain (A_{dc}) with low (NM_L) and high (NM_H) noise margins for both inverters have been shown. The DC voltage gain has been calculated using the slope of VTC as given in Eq. 4.1.

$$A_{dc} = \frac{\partial V_0}{\partial V_{in}} \tag{4.1}$$

From Figure 4.2(b), it can be analysed that INV2 shows better DC gain comparatively, and hence, reflects its potential to be used as an analog amplifier. Consequently, the operating voltage range would be smaller as compared to the C_DGJLFET based analog amplifier. Another desirable static characteristic of digital logic devices is high noise immunity. The maximum low-state input voltage to be considered as '0' (V_{IL}), and the minimum high-state input voltage to be considered as '1' (V_{IH}) have been measured for $A_{dc} = -1$. In Table 4.2, the calculated values of various static parameters for the two inverters have been listed and compared with inverters based on other junctionless devices from the literature.

Table 4.2 Various static parameters for INV1 and INV2.

Inverter based on	**L_G (nm)**	**V_{ST} (V)**	**V_{IL} (V)**	**V_{IH} (V)**	**NM_H (V)**	**NM_L (V)**
DG junctionless nanowire transistor [121]	20	--	--	--	0.316	0.228
Charge plasma based junctionless C-FinFET [150]	20	--	--	--	0.315	0.315
C_DGJLGET (INV1) This work	20	0.49	0.38	0.595	0.485	0.38
R_DGJLGET (INV2) This work	20	0.46	0.41	0.51	**0.49**	**0.41**

From Table 4.2 it can be observed that in the case of INV2 the narrower input voltage range from V_{IH} to V_{IL}, boosts the noise immunity in comparison to INV1 which can be quantified from the larger value of low (NM_L = 0.41 V) and high noise margin (NM_H = 0.49 V) for INV2. The proposed device-based inverter also reflects better noise margins in comparison to

other inverters based on other JLFETs from the literature for $L_G = 20$ nm. The mathematical relations are given in Eq. 4.2 and Eq. 4.3 [1] have been used to calculate the value of noise margins shown in Table 4.2.

$$NM_H = V_{OH} - V_{IH} \tag{4.2}$$

$$NM_L = V_{IL} - V_{OL} \tag{4.3}$$

4.2.1.2 Transient analysis of R_DGJLFET based inverter

The timing attributes namely rise time (τ_{Ri}), fall time (τ_{Fi}), time period (T_{cycle}), high time (T_H), and duty cycle of input signal have been fixed with the values of 2 ps, 2 ps, 1000 ps, 496 ps, and 50 %, respectively. The switching characteristics of both inverters have been presented in Figure 4.3 which are obtained for an input pulse signal (V_{in}) of frequency 1 GHz. With optimized width for PMOS and NMOS devices, the transient responses for both inverters are almost similar for $C_L = 10$ fF. Both inverters can switch instantly to produce complementary output as shown in Figure 4.3(a). However, the output switching is delayed by increasing the load capacitance to 0.1 pF as shown in Figure 4.3(b).

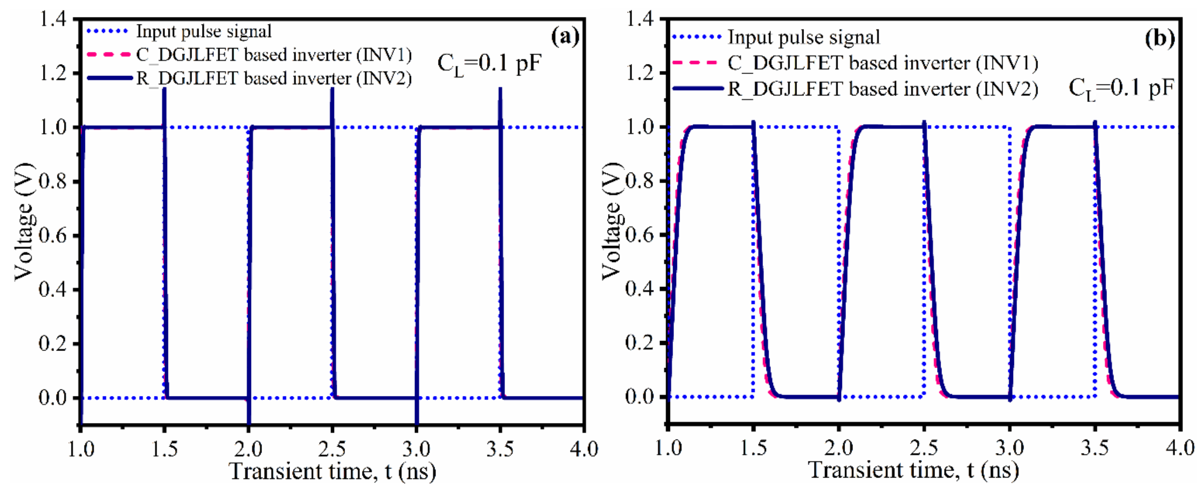


Figure 4.3 Switching characteristics for INV1 and INV2 for load capacitance of (a) 10 fF and (b) 0.1 pF.

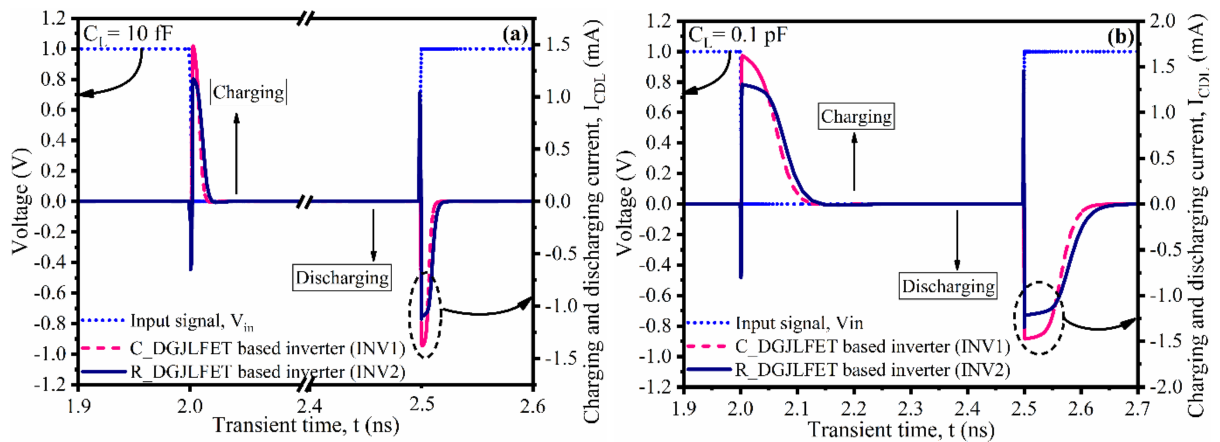


Figure 4.4 Charging/discharging currents in INV1 and INV2 (a) for $C_L = 10$ fF (b) $C_L = 0.1$ pF.

Observing Figure 4.3, INV2 is slightly slower in comparison to INV1. The reason for that is the R_DGJLFET based pull-up and pull-down networks provide a minutely lower current (I_{CDL}) for charging and discharging of load capacitance in comparison to the C_DGJLFET based counterpart as shown in Figure 4.4(a). In Figure 4.4(b), this difference in peak values of I_{CDL} becomes more visible for C_L = 0.1 pF due to which INV2 takes more time to fully charge/discharge the load capacitance.

The graphical representation of measuring the rise time (τ_R), fall time (τ_F), the propagation delay for the output switching from LOW-to-HIGH (τ_{pLH}), and propagation delay for output switching from HIGH-to-LOW (τ_{pHL}) have been shown in Figure 4.5. The rise/fall time (τ_R/τ_F) has been reflected as the time difference in which output voltage (V_o) rises/falls from 10%/90% to 90%/10% of the minimum/maximum value as shown in Figure 4.5(a) and Figure 4.5(b), respectively. In Figure 4.5(a) the parameter τ_{pLH} represents the time difference in which V_o rises and V_{in} falls to 50% of the maximum voltage value. Conversely, the parameter τ_{pHL} represents the time difference in which V_o falls and V_{in} rises to 50% of the maximum value as depicted in Figure 4.5(b).

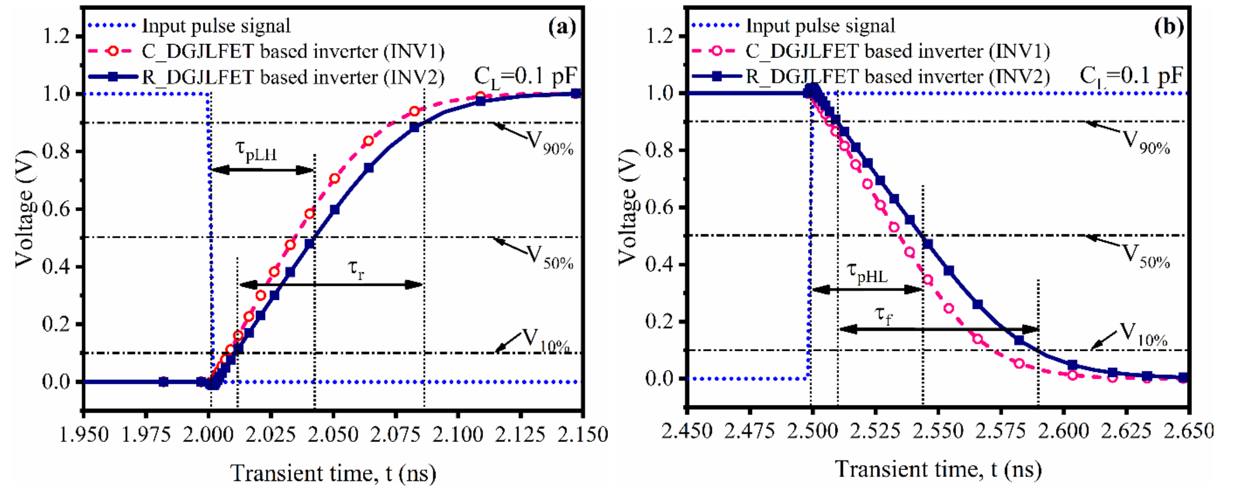


Figure 4.5 Graphical representation of transient delays for INV1 and INV2 (a) τ_R, and τ_{pLH} (b) τ_F, and τ_{pHL}.

Mathematically, τ_R, τ_F, τ_{pLH}, and τ_{pHL} can be expressed as given in Eq. 4.4 to Eq. 4.7 [1], respectively. The up and down arrow in these equations indicates the rising and falling edge of the signals, respectively.

$$\tau_R = \tau_{V(90\%)\uparrow} - \tau_{V(10\%)\uparrow} \quad (4.4)$$

$$\tau_F = \tau_{V(10\%)\downarrow} - \tau_{V(90\%)\downarrow} \quad (4.5)$$

$$\tau_{pLH} = \tau_{V_{o(50\%)}\uparrow} - \tau_{Vin_{(50\%)}\downarrow} \quad (4.6)$$

$$\tau_{pHL} = \tau_{V_{o(50\%)}\downarrow} - \tau_{Vin_{(50\%)}\uparrow} \quad (4.7)$$

The calculated value of various transient parameters has been listed in Table 4.3. From Table 4.3, it can be noticed that the τ_R and τ_F for INV1 and INV2 are almost equal, which confirms the symmetric design of both inverter circuits.

Table 4.3 Transient delays for INV1 and INV2.

Inverter based on	L_G (nm)	τ_r (ps)	τ_f (ps)	τ_{pLH} (ps)	τ_{pHL} (ps)	τ_p (ps)
C_DGJLFET (INV1)	20	~7.2	~7.0	~4.5	~4.7	~4.6
R_DGJLFET (INV2)	20	~9.3	~9.0	~6.0	~7.0	~6.5

Moreover, it can be analysed that INV2 reflects a slightly longer propagation delay (τ_p) in comparison to INV1 which can be attributed to the higher gate-to-gate capacitance (C_{gg}) offered by the R_DGJLFET. For V_{GS} = 1.0 V and V_{DS} = 0.05 V, the C_{gg} for the R_DGJLFET and C_DGJLFET have been found as ~8.39×10^{-16} F and ~7.05×10^{-16} F, respectively. Mathematically, τ_p can be written as given in Eq. 4.8 [1].

$$\tau_p = \frac{(\tau_{pLH} + \tau_{pHL})}{2} \tag{4.8}$$

Additionally, it has also been observed that increasing the value of C_L 10 times i.e., from 10 fF to 0.1 pF, the INV1 shows an increase of ~9.13, ~9.28, ~7.55, ~7.44, and ~7.5 times in τ_R, τ_F, τ_{pLH}, τ_{pHL}, and τ_p, respectively while the corresponding increase for INV2 has been reported as ~8.12, ~8.8, ~7, ~6.42, and ~6.69 times. Importantly, the increase in different transient delays depicted by INV2 is minutely smaller than INV1.

4.2.1.3 Power analysis of R_DGJLFET based inverter

Power dissipation is an important figure of merit for a digital circuit. Refer to Figure 3.9(a) in chapter-3 the I_D for V_{GS} = 0.0 V for the two devices has been shown; which agrees to conclude that the R_DGJLFET based INV2 will dissipate smaller static leakage power than that of INV1.

Table 4.4 Various components of power dissipation for INV1 and INV2 with W_G in µm.

Inverter based on	L_G (nm)	P_{DC}	P_{SW}	P_{SC}
Dielectrically separated independent gate JLT [143]	20	--	8.16 µW	--
Charge plasma based junctionless C-FinFET [150]	20	0.217nW	--	--
C_DGJLFET (INV1)	20	1.20 µW	11.314 µW	0.351 µW
R_DGJLFET (INV2)	20	0.104 nW	11.613 µW	0.472 nW

In Table 4.4, the static leakage power dissipation (P_{DC}), switching power dissipation (P_{SW}), and short-circuit power dissipation (P_{SC}) have been listed for INV1 and INV2. From Table 4.4, it can be noticed that the INV2 reflects smaller static leakage power dissipation of 0.104 nW than that of 1.20 µW for INV1 due to improved channel depletion which suppresses the leakage current in R_DGJLFET based NMOS and PMOS devices. Mathematically, P_{DC} can be described as given in Eq. 4.9 [1].

$$P_{DC} = I_{Davg} \times V_{DD} \tag{4.9}$$

where,

$$I_{Davg} = \frac{(I_{DD0} + I_{DD1})}{2} \tag{4.10}$$

Here, I_{DD0} and I_{DD1} represent the leakage currents drawn from the power supply and measured for V_{in} = 0.0 V and V_{in} = 1.0 V, respectively. Moreover, the switching power dissipation for both inverter circuits has been found comparable with 11.314 µW for INV1 and 11.613 µW for INV2. The P_{SW} has been calculated using Eq. 4.11 [1]. The input pulse signal of frequency 1 GHz has been applied for both inverters.

$$P_{SW} = C_{Ld} \times V_{DD} \times f_{in} \tag{4.11}$$

Here, C_{Ld} represents the sum of parasitic gate-to-drain capacitances for PMOS ($C_{gd,p}$) and NMOS ($C_{gd,n}$) devices with C_L of 10 fF. The minutely higher gate-to-drain capacitance for R_DGJLFET based PMOS ($C_{gd,p}$ = 0.775 fF) and NMOS ($C_{gd,n}$ = 0.839 fF) devices results in slightly increased P_{SW} for INV2. Furthermore, the C_DGJLFET based PMOS and NMOS poor gate control allows the flow of current drawn from the power supply for a longer range of V_{GS} in INV1 in comparison to INV2 as shown in Figure 4.6.

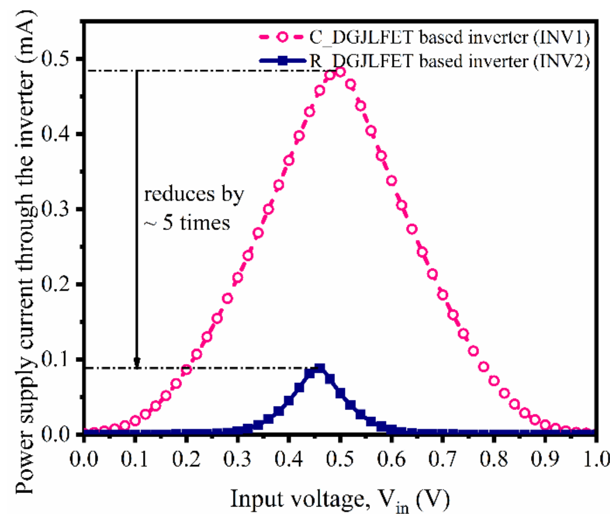


Figure 4.6 Comparison of power supply current through INV1 and INV2.

In INV1 a power supply current with a peak value of ~0.5 mA has been observed which flows when both PMOS and NMOS devices conduct simultaneously in the saturation region. Remarkably, this peak of power supply current is lowered by ~5 times in the case of INV2 due to quicker static transition i.e. steeper VTC. As a result, the short-circuit power dissipation (P_{SC}) gets reduced by ~1000 times for INV2 in comparison to INV1 as listed in Table 4.4. Mathematically, P_{SC} can be written as given in Eq. 4.12 [1].

$$P_{SC} = \frac{V_{DD} \times \left[\frac{I_{Dp(peak)} \times \Delta t_1}{2} + \frac{I_{Dn(peak)} \times \Delta t_2}{2}\right]}{T_{cycle}} \tag{4.12}$$

where Δt_1 denotes the time difference in which the input signal rises from V_{tn} to V_{DD}-$|V_{tp}|$ while the falling transition from V_{DD}-$|V_{tp}|$ to V_{tn} represents the time difference Δt_2. The $I_{Dp(peak)}$ and $I_{Dn(peak)}$ show the maximum value of I_D flowing through the PMOS and NMOS devices, respectively. The time period of the input signal has been represented with T_{cylce}.

With overall lesser power consumption, the R_DGJLFET shows its competence for low-power digital circuit applications. After the static and dynamic behaviour of R_DGJLFET based inverter has been investigated and compared with C_DGJLFET based counterpart part, the device's electrical fitness has been further analysed in various 2-input digital standard cells namely NAND, and NOR gate.

4.2.2 R_DGJLFET based NAND gate

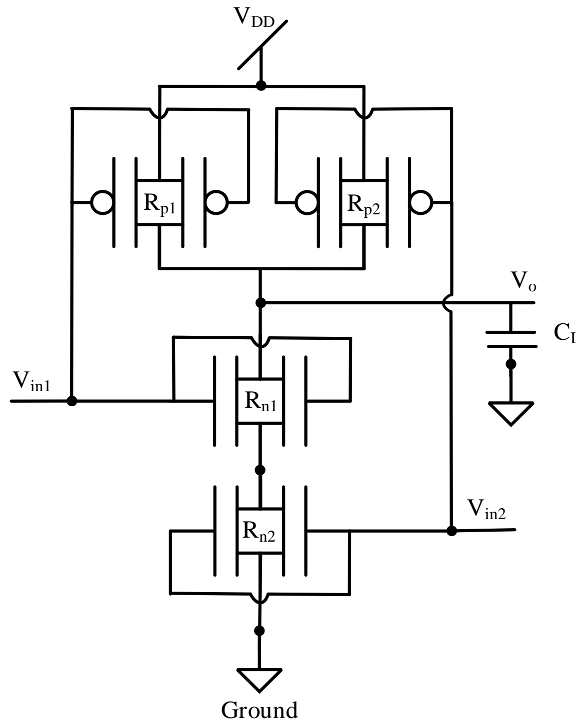


Figure 4.7 Circuit diagram for R_DGJLFET based 2-input NAND gate [1].

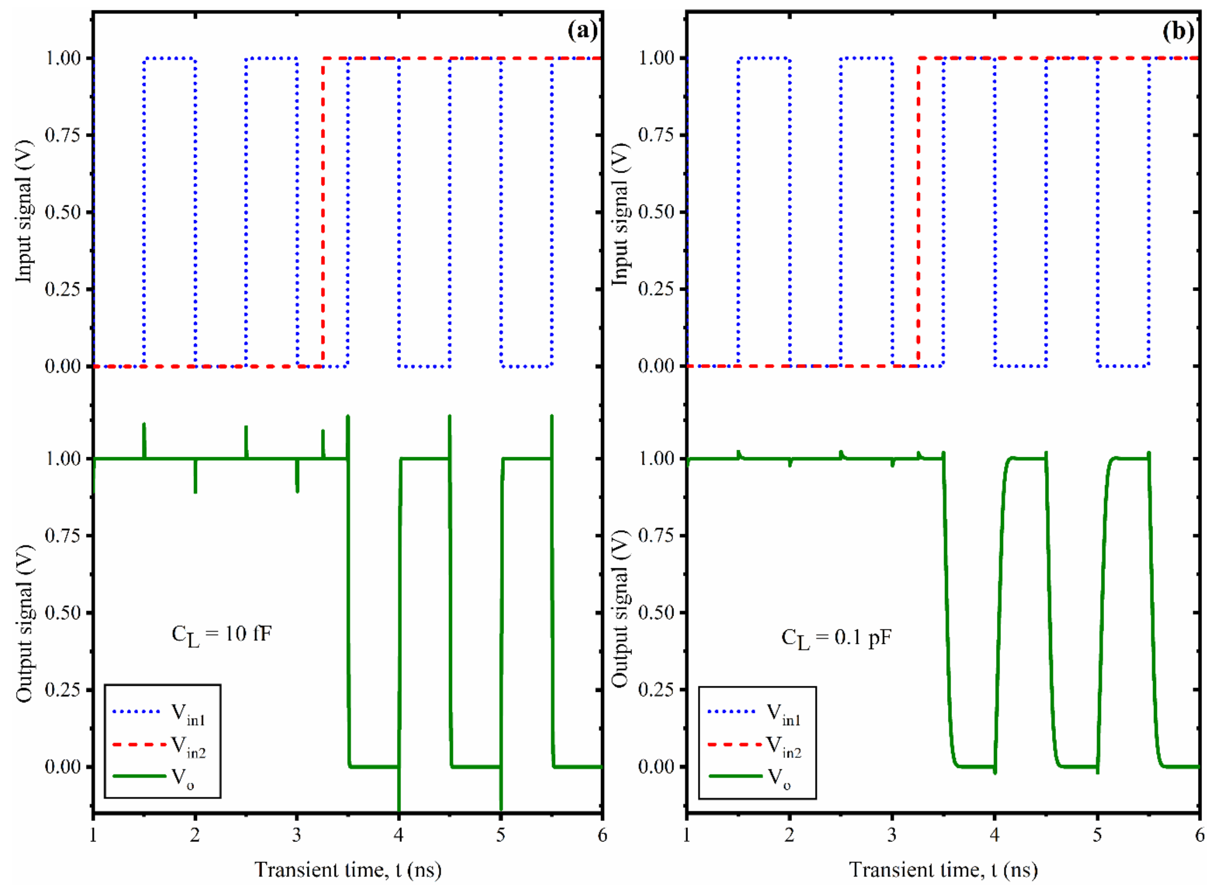


Figure 4.8 Transient response of R_DGJLFET based 2-input NAND gate for (a) $C_L = 10$ fF, (b) $C_L = 0.1$pF.

The circuit diagram for the 2-input NAND gate has been shown in Figure 4.7 [1], which have been implemented with parallel and series connection of R_DGJLFET based PMOS/NMOS, respectively and $V_{DD} = 1.0$ V. The physical sizes of all NMOS and PMOS devices have been referenced from the INV2 presented in subsection 4.2.1. However, the series connection of NMOS devices results in twice the path resistance in the pull-down network, which has been halved by considering the double gate width for NMOS devices i.e. $W_{Gn} = 2$ μm. When the inputs V_{in1} and V_{in2} have been set to '1', the transistors in the pull-down network fully discharge the load capacitance, as the PMOS in the pull-up network goes into cut-off. However, if either input or both have been set to '0', the pull-up network charges the C_L as the pull-down path is cut off. The obtained transient behaviour of the R_DGJLFET based NAND gate has been shown in Figure 4.8(a) and Figure 4.8(b) for C_L=10 fF and 0.1pF, respectively. From Figure 4.8(a), it has been observed that for C_L= 10 fF the circuit reflects a τ_R and τ_F of ~10 ps, and ~8.8 ps, respectively.

The measured data for τ_{pLH} = ~7.4 ps and τ_{pHL} = ~6.1 ps has been used to calculate the value of τ_p = ~6.75 ps. Moreover, the τ_R, τ_F, τ_{pLH}, τ_{pHL}, and τ_p for R_DGJLFET based NAND gate increases by an amount of ~7.64, ~7.7, ~5.67, ~5.73, and ~5.70 times for C_L = 0.1 pF with

minimized overshoot and undershoot due to parasitic feedback path from input to output node.

4.2.3 R_DGJLFET based NOR gate

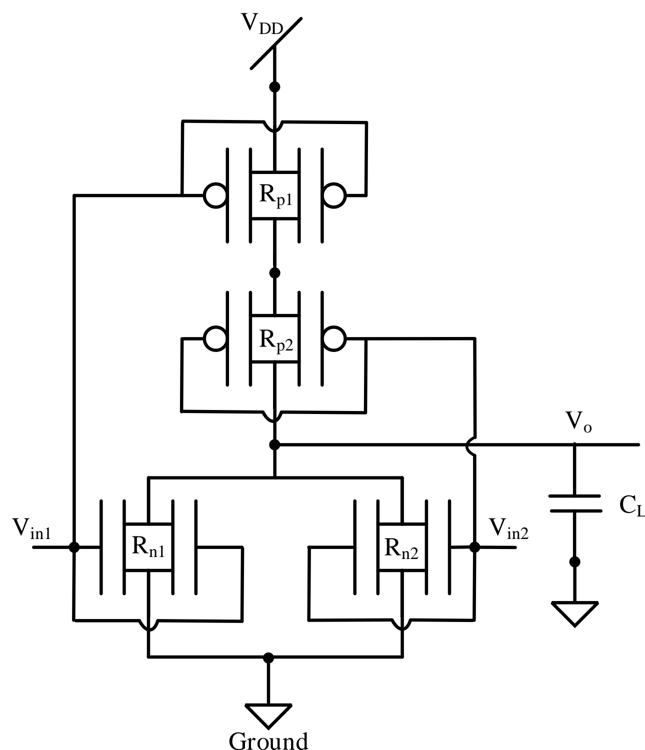


Figure 4.9 Circuit diagram for R_DGJLFET based 2-input NOR gate [1].

The 2-input NOR gate has been implemented with parallel and series connection of R_DGJLFET based PMOS and NMOS (V_{DD} = 1.0 V), respectively as shown in Figure 4.9 [1]. Here, due to the series connection of PMOS devices, the pull-up network has been designed with twice the gate width i.e. W_{Gp} = 8.2 µm, which cuts the path resistance by 50%. When the inputs V_{in1} and V_{in2} have been set to '0', the transistors in the pull-up network fully charge the load capacitance, as the NMOS devices in the pull-down network go in the cut-off. However, if either input or both have been set to '1', the pull-down network discharges the load capacitance fully as the pull-up path is cut-off. The obtained transient behaviour of NOR gate has been shown in Fig 4.10(a) and Fig 4.10(b) for C_L of the value of 10 fF and 0.1pF, respectively. Considering C_L = 10 fF, the τ_R, τ_F, τ_{pLH}, τ_{pHL}, and τ_p for R_DGJLFET based NOR gate have been measured as ~10 ps, ~14.5 ps, ~8 ps, ~13 ps, and ~10.5 ps, respectively. The τ_R, τ_F, τ_{pLH}, τ_{pHL}, and τ_p increase by ~6.9, ~5.86, ~4.86, ~3.84, and ~4.23 times, respectively for the range of C_L from 10 fF to 0.1 pF. The calculated values of different transient delays for NOT, NAND, and NOR gate have been listed in Table 4.5. Here, the symbol C_1 and C_2 reflect the case for which the transient delay values has been calculated considering the C_L of 10 fF and 0.1 pF, respectively.

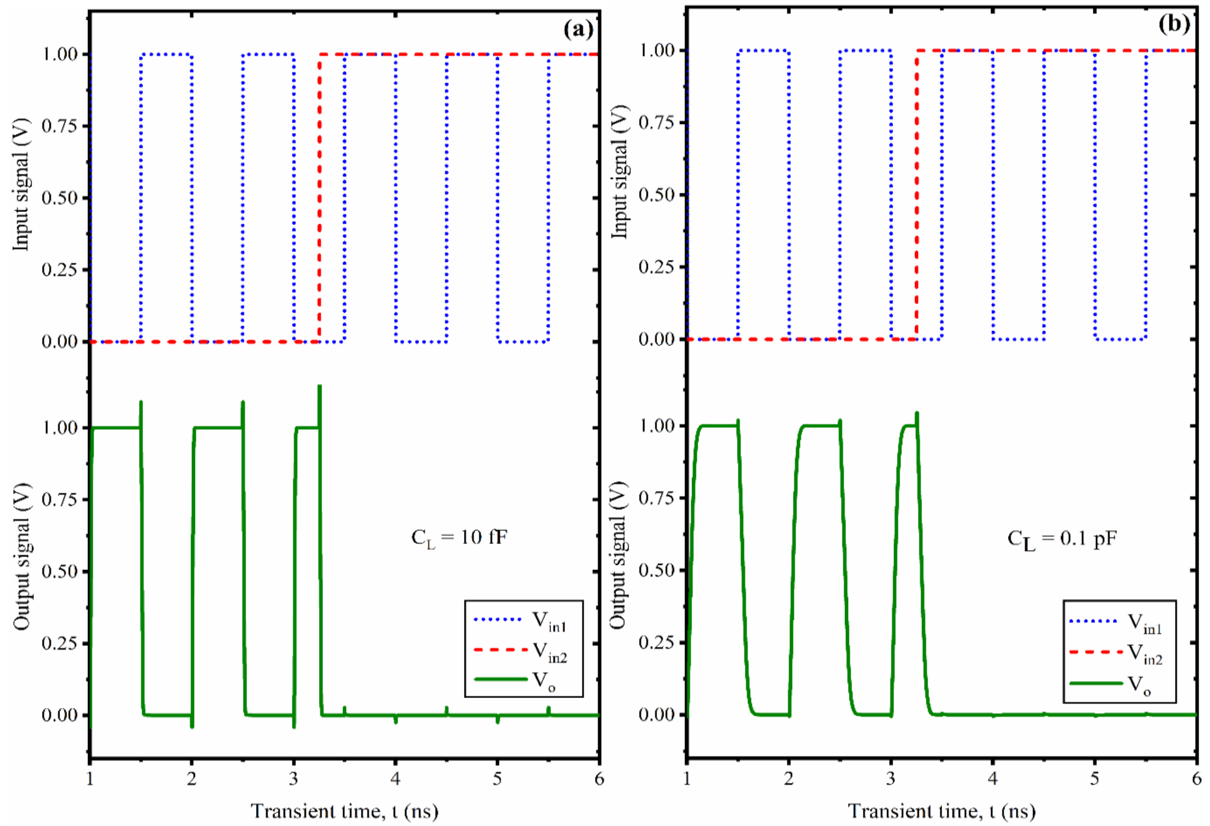


Figure 4.10 Transient response of R_DGJLFET based 2-input NOR gate for C_L = 10 fF, (b) C_L = 0.1 pF.

Table 4.5 Transient delays for implemented logic gates for C_L = 10 fF and 0.1 pF.

R_DGJLFET based gate	τ_r (ps)		τ_f (ps)		τ_{pLH} (ps)		τ_{pHL} (ps)		τ_p (ps)	
	C_1	C_2	C_1	C_2	C_1	C_2	C_1	C_2	C_1	C_2
NOT Gate	~9.3	~75.6	~9.0	~79.2	~6	~42	~7	~45	~6.5	~43.5
NAND Gate	~10	~76.4	~8.8	~67.8	~7.4	~42	~6.1	~35	~6.75	~38.5
NOR Gate	~10	~69	~14.5	~85	~8	~38.9	~13	~50	~10.5	~44.45

From Table 4.5, it has been observed that increasing the value of load capacitance increases the all-transient delays as the circuit is required to provide the charging/discharging current for a longer amount of time to charge/discharge the C_L. Moreover, the transient performance of asymmetric designs of all previously discussed logic gates considering equal gate width for all PMOS with NMOS devices in the circuit have been investigated for a C_L = 10 fF.

Table 4.6 Transient delays for R_DGJLFET based asymmetric NOT, NAND, and NOR gate.

R_DGJLFET based gate	τ_{pLH} (ps)	τ_{pHL} (ps)	τ_p (ps)
NOT Gate	~19.9	~5.6	~12.75
NAND Gate	~22	~9	~15.5
NOR Gate	~35	~6	~20.5

The calculated values of τ_{pLH}, τ_{pHL}, and τ_p for asymmetric designs have been listed in Table 4.6. From Table 4.6, it can be concluded that implementing the logic gates with equal gate widths for R_DGJLFET based PMOS and NMOS devices results in a weaker pull-up network as compared to pull-down network which leads to degraded τ_{pLH}, hence, longer τ_p have been reported in comparison to symmetric inverter design.

4.2.4 R_DGJLFET based common-source amplifier

Furthermore, the performance of the proposed R_DGJLFET has been studied by implementing a common-source amplifier. The amplifier is an important analog block used to derive the output load from the small signal. The schematic diagram for the CS amplifier based on R_DGJLFET has been shown in Figure 4.11 [185].

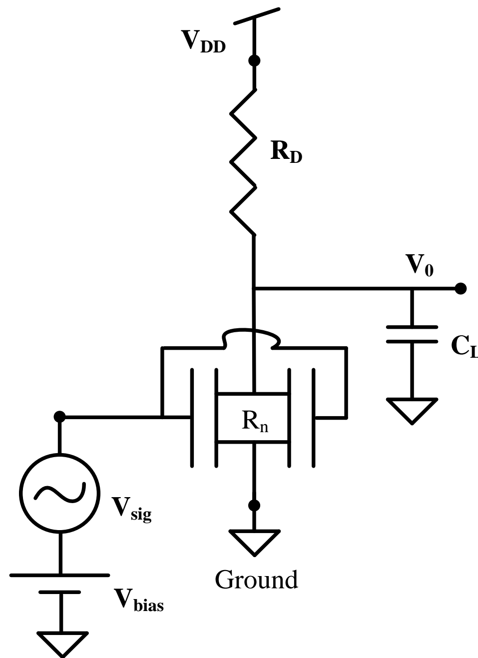


Figure 4.11 Schematic diagram of proposed R_DGJLFET based CS amplifier [185].

The parameters used for designing the CS amplifier have been listed in Table 4.7. The circuit has been implemented using R_DGJLFET with L_G=20 nm. The input bias has been applied with a fixed DC voltage (V_{bias}) of 0.47 V. A small signal with peak-to-peak amplitude ($V_{sig(p-p)}$) of 100 mV and a frequency (*f*) of 1 GHz has been superimposed on the V_{bias}.

Table 4.7 Simulation parameters for the proposed R_DGJLFET based CS amplifier.

Design parameter	Value
The input bias voltage, V_{bias} (V)	0.47 V
The peak-to-peak amplitude of sinusoidal input signal, $V_{sig(p-p)}$	100 mV
Frequency of input AC signal, *f*	1 GHz
Pull-up resistor, R_D	5 kΩ
Load capacitor, C_L	3 fF

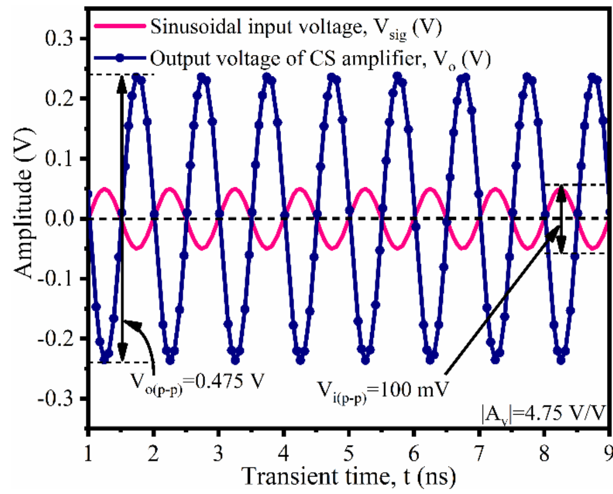


Figure 4.12 Transient response of R_DGJLFET based CS amplifier.

The load capacitor (C_L) of the value of 3 fF has been used with a pull-up resistor (R_D) of 5 kΩ. The transient simulation has been performed in the Mixed-mode simulator and an amplified output signal was observed as shown in Figure 4.12. In Figure 4.12, the peak-to-peak variations in output signal $V_{o(p-p)}$ of the value of 0.475 V can be observed with a small input signal of 100 mV. This clearly shows that the CS amplifier based on R_DGJLFET shows amplification of more than 4 times which means that the voltage gain |Av| of 4.75 V/V. It can also be observed that the amplifier produces the output signal with a -180-degree phase change w.r.t. the input signal which shows the reliable working of the device in the implemented CS amplifier.

To ensure the amplifying capability of the CS amplifier based on the proposed R_DGJLFET, its gain value has also been compared with the other structurally engineered FET based CS amplifiers as shown in Table 4.8. Here, it can be observed that the R_DGJLFET base CS amplifier reflects a higher gain value in comparison to marked references from the literature. Hence, the proposed R_DGJLFET can also work reliably in analog circuits like CS amplifiers. The frequency response of the R_DGJLFET based CS amplifier has been presented in Figure 4.13(a). The study of frequency response reveals that the R_DGJLFET based CS amplifier can provide a gain of 4.75 faithfully within the frequency range of 1kHz to 1GHz. Increasing the input signal frequency beyond this range strongly affects the gain and its value degrades sharply. For an input frequency of 40 GHz, the gain value for the CS amplifier based on R_DGJLFET to 1.26. Moreover, in Figure 4.13(b) it can be observed that for an input frequency of 1 GHz the R_DGJLFET based CS amplifier can drive the load capacitance up to 20 fF without much degradation in gain value. But, increasing the value of C_L greater than 20 fF lowers the reactance significantly and the output starts short-circuiting to the ground which leads to a sharp reduction in gain.

Table 4.8 Comparison of the voltage gain of R_DGJLFET based CS amplifier with other FET structures-based counterparts in the literature.

Device type used to design CS amplifier	Gain (A_v)
Dual material gate junctionless transistor (DMG SOI JL MOSFET) [123]	~1.25
Hetro-dielectric tri-material gate tunnelling FET (TFET) [40]	~3.00
R_DGJLFET (This work)	~4.75
C_DGJLFET (This work)	~3.00

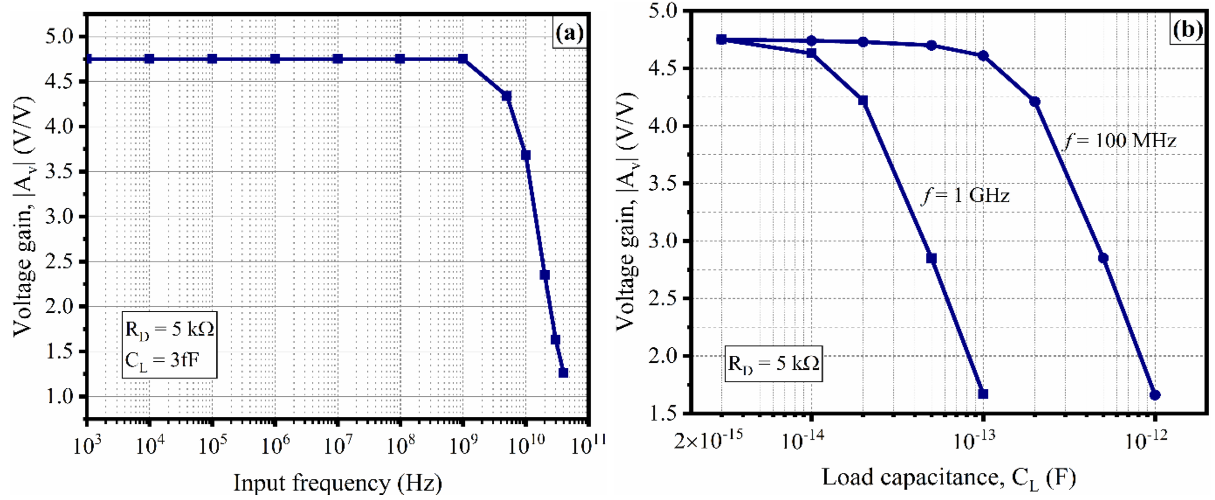


Figure 4.13 (a) Frequency response and, (b) effect of variations in C_L on the frequency response of R_DGJLFET based CS amplifier.

4.3 Conclusions

In this chapter, the performance parameters of R_DGJLFET in both digital and analog circuits have been investigated. The R_DGJLFET based inverter presents an attractive low-power solution for digital circuit applications by offering smaller P_{DC}, comparable P_{SW}, and lesser P_{SC} with the value of ~0.104 nW, ~11.613 μW, and ~0.472 nW, respectively along with steeper VTC and wider low/high noise margins. In digital circuits, the R_DGJLFET based logic gates namely NOT, 2-input NAND, and NOR gate have been implemented which successfully reflects the desired transient behaviour with the propagation delay of ~6.5 ps, ~6.75 ps, ~10.5 ps and ~18.3 ps, respectively. Whereas, in analog circuits, the R_DGJLFET based CS amplifier shows an amplification of 4.75 V/V within the wide frequency range of 1 kHz to 1 GHz.

Chapter-5
Analytical modeling of proposed recessed double gate JLFET

5.1 Introduction

The proposed recessed double gate JLFET (R_DGJLFET) reflects remarkable performance improvement over the conventional double gate JLFET (C_DGJLFET) at the device level considering the variations in different technological parameters related to channel and gate electrodes and at the circuit level with successful operation in both digital and analog circuits. Therefore, in this chapter, the development of an analytical model has been sought to further enhance the physical insights about the R_DGJLFET. Besides its complexity, analytical modeling of an electronic device has been a popular task among researchers to shorten the design time and avoid the need for TCAD tool-based design to understand the physical principle [166]. Various analytical or semi-analytical models for both long-channel and short-channel junctionless multigate FETs have been developed based on surface/center potential and drain current [44, 48, 105, 111, 167-179].

Sallese *et al.* [44] have developed an analytical model for the symmetric DG JLFET by using the charge density to calculate the drain current without consideration of SCEs and carrier quantization. Duarte *et al.* [45] have used the parabolic potential approximation for developing the analytical model for DG JLFET which captures the bulk conduction in all operating regions. Chen *et al.* [102] have approximated the surface potential in all three 0operating regions and developed the drain current model using the Pao-Sah integral. Jazaeri *et al.* [105] have approximated the 2-D potential distribution in ultrathin DG JLFET operating in the subthreshold regime using the parabolic method. Yesayan *et al.* [168] have estimated the channel charge in a long channel DG JLFET to propose an explicit model for the drain current. Cerdeira *et al.* [169] have done charge-based modeling for a potential profile in long channel DG JLFET.

Hu *et al.* [170] have proposed the analytical model for a short-channel GAA junctionless MOSFET in terms of potential, threshold voltage, and subthreshold swing. Lime *et al.* [171] have presented an explicit compact model for DC characteristics of long channel junctionless MOSFET. Hur *et al.* [47] have proposed a charge-based core compact model for the drain current in JLFETs with multigate architecture such as DG, cylindrical GAA, rectangular GAA, and tri-gate (TG). Baruah *et al.* [48] have presented the analytical model for potential and drain current for short channel DG JLFET using the variable separation technique without any fitting parameter. Paz *et al.* [172] have proposed an analytical charge-based model for

describing the drain current in both the accumulation and depletion regime of a TG junctionless transistor. For the first time, Xiao *et al.* [108] have proposed a new analytical model for potential and drain current while capturing the effect of dynamic channel boundary in short channel DG JLFET. Singh *et al.* [171] have analysed the 2-D channel potential and the threshold voltage of a DG JLFET with the effect of a vertical Gaussian-like doping profile. The authors have also presented a 2-D analytical model for the threshold voltage of a DGJLFET with dielectric pockets in the channel while considering the effect of source/drain depletion [174]. Shin *et al.* [175] have considered the limitations of heavy channel doping such as HCE and RDF in DG JLFET and proposed the subthreshold analytical model based on the Fourier series and Green's function.

Ajay *et al.* [176] have modeled the drain current in DG MOSFET considering the space over the underlap regions towards the source and drain as the cavities for biomolecules which modulates the dielectric constant and shifts the threshold voltage of the device. Shalchian *et al.* [142] have presented the charge-based model for ultrathin DG JLFET considering the quantum confinements. Duarte *et* al. [168] have presented a compact model for approximating the quantum electron density in DG JLFET operating in a subthreshold regime. Jaiswal *et al.* [111] have modeled the effect of variations in the length of underlap regions on the SCEs in an asymmetric DG JLFET. The authors have also presented the modeling of SCEs in a core-shell based DG JLFET [112].

Shafizade *et al.* [174] have presented the explicit model for ultrathin GAA junctionless FET while including the 2-D quantum confinement effects. Kaushal *et al.* [180] have presented analytical modeling of negative capacitance in junctionless FinFET with fringing field effects. Gola *et al*. [180] have introduced an analytical model for thermal noise in TG JLFET with substrate bias effects.

From the literature [7]][112][114][175], it has been noticed that to understand the OFF-state behaviour, it is imperative to analyse the JLFET operating in the subthreshold region. Hence, in the present work, the analytical model for the proposed R_DGJLFET operating in the subthreshold region has been formulated. The model derivation was started by defining the 2-D Poisson's equation in a recessed silicon channel and then in underlap regions towards source/drain ends. The explicit expressions for surface and center potential have been obtained in all three silicon regions. Using these expressions, the analytical expression for subthreshold drain current has been formulated. The effect of drain bias on the minimum center potential has been presented with an estimation of its location in the channel. Moreover, to obtain better physical insights about the device behaviour, the effect of work function, doping concentration, effective oxide thickness, and gate length on the subthreshold

drain current has also been incorporated. Furthermore, the effect of gate length reduction on the subthreshold slope has been presented. In the underlap regions the effect of fringe capacitance originating from the gate edges has been considered using conformal mapping [181]. The model results have been validated through a comparison with the simulation results obtained from the Silvaco Atlas device simulator [136]. It has been found that the model results are in close agreement with the simulation results.

5.2 Device structure

The 2-D schematic of the R_DGJLFET analysed to derive the analytical model has been shown in Figure 5.1. In this work symmetric R_DGJLFET has been considered with equal dielectric thickness, work function, and terminal voltage for both gate electrodes. Also, the lengths of underlap regions towards the source and drain ends have been considered identical and have been denoted with L_U instead of the previously used symbols L_{US} and L_{UD}, respectively.

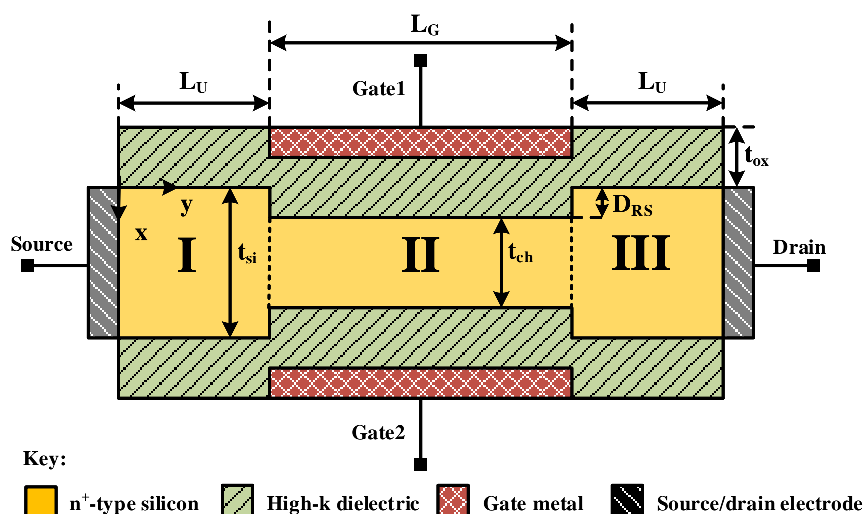


Figure 5.1 The analyzed 2-D schematic of R_DGJLFET with three regions.

In Figure 5.1, it can be seen that the whole silicon layer has been divided into three rectangular adjacent regions which have been labeled as I, II, and III in roman letters. The origin coordinates have been fixed at the top-left corner of region I in terms of x – and y – which represent the lengths across to and along the channel, respectively. Region II comprises the overlapped area between the gates in the y-direction i.e. $L_U \leq y \leq L_U+L_G$, where L_U is the length of underlap region towards the source/drain and L_G denotes the length of the Gate1/Gate2 electrode. Region I and III represent the underlap areas bounded as $0 \leq y \leq L_U$ and $L_U+L_G \leq y \leq L_G+2L_U$, respectively. In underlap region, the silicon thickness has been represented with t_{si}, while in region II, it is denoted with $t_{ch} = t_{si} - 2 \times D_{RS}$, where D_{RS} represents the depth up to which the silicon has been recessed.

5.3 Analytical model for the potential profile in R_DGJLFET

The present analytical work has been started while assuming the absence of (a) incomplete ionization i.e. all impurity atoms have been ionized, and (b) any crystal flaws in terms of traps and defects in the semiconductor device. Hence, for these physical phenomena, no term has been included in the right-hand side of Poisson's equation.

5.3.1 Surface potential model

The potential distribution $\psi(x, y)$ in the silicon layer is governed by the 2-D Poisson's equation [105] as given in Eq. 5.1.

$$\frac{\partial^2\psi(x,y)}{\partial x^2}+\frac{\partial^2\psi(x,y)}{\partial y^2}=\frac{qn_i}{\varepsilon_{si}}.e^{\left(\frac{\psi(x,y)-V_{qf}}{V_T}\right)}-\frac{qN_D}{\varepsilon_{si}} \tag{5.1}$$

where, $\psi(x, y)$ is the channel potential in the silicon layer, V_{qf} is the quasi-fermi potential of an electron in the silicon layer, n_i is the intrinsic charge density, N_D is the silicon doping concentration, and ε_{si} is the silicon permittivity. V_T is the thermal voltage as given in Eq. 5.2.

$$V_T=\frac{kT}{q} \tag{5.2}$$

Here, k is Boltzmann's constant, T is absolute temperature, and q is the electron charge.

5.3.1.1 Surface potential model for region II

Region II comprises the silicon area which is displaced in terms of both x- and y- distances w.r.t. from the origin coordinates fixed in the region I. Hence, new origin coordinates X_2 and Y_2 for region II has been defined in the following manner.

$$x=D_{RS}+X_2 \Rightarrow X_2=x-D_{RS} \text{ and} \tag{5.3}$$

$$y=L_U+Y_2 \Rightarrow Y_2=y-L_U \tag{5.4}$$

Also, it has been assumed that region II is fully depleted in the subthreshold region with negligible contribution from the mobile charge carriers. Hence, Eq. 5.1 can be re-written for region II in the following way:

$$\frac{\partial^2\psi_2(X_2,Y_2)}{\partial X_2^2}+\frac{\partial^2\psi_2(X_2,Y_2)}{\partial Y_2^2}=-\frac{qN_D}{\varepsilon_{si}} \tag{5.5}$$

where, $\psi_2(X_2,Y_2)$ is the channel potential in region II. As presented by Young [182], the 2-D potential distribution in this region can be approximated assuming parabolic in nature along the X-direction:

$$\psi_2(X_2,Y_2)=C_{21}(Y_2)+C_{22}(Y_2)X_2+C_{23}(Y_2)X_2^2 \tag{5.6}$$

To find the value of the unknown $C_{21}(Y_2)$, $C_{22}(Y_2)$, and $C_{23}(Y_2)$, the following boundary conditions [178] have been applied to Eq. 5.6.

- Since the proposed device has been considered symmetric, hence, the potential at the top and bottom surface of region II can be expressed as follows:

$$\psi_2(0,Y_2) = \psi_2(t_{ch},Y_2) = \psi_{s2}(Y_2) \tag{5.7}$$

- The electric field at the Gate1 electrode can be written as:

$$\left.\frac{\partial\psi_2(X_2,Y_2)}{\partial X_2}\right|_{X_2=0} = \frac{C_{ox}\left[\psi_{s2}(Y_2) - V_{GS} - V_{FB2}\right]}{\varepsilon_{si}} \tag{5.8}$$

- The electric field at the Gate2 electrode can be written as:

$$\left.\frac{\partial\psi_2(X_2,Y_2)}{\partial X_2}\right|_{X_2=t_{ch}} = -\frac{C_{ox}\left[\psi_{s2}(Y_2) - V_{GS} - V_{FB2}\right]}{\varepsilon_{si}} \tag{5.9}$$

Using these boundary conditions, the unknows $C_{21}(Y_2)$, $C_{22}(Y_2)$, and $C_{23}(Y_2)$ have been evaluated as:

$$C_{21}(Y_2) = \psi_{s2}(Y_2) \tag{5.10}$$

$$C_{22}(Y_2) = \frac{C_{ox}\left[\psi_{s2}(Y_2) - V_{GS} - V_{FB2}\right]}{\varepsilon_{si}} \tag{5.11}$$

$$C_{23}(Y_2) = \frac{C_{ox}}{\varepsilon_{si}}\frac{\left[V_{GS} - V_{FB2} - \psi_{s2}(Y_2)\right]}{t_{ch}} \tag{5.12}$$

where, $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate oxide capacitance, ε_{ox} is the permittivity of gate dielectric material. V_{GS} is the gate-to-source voltage and V_{FB2} is the flat band voltage of region II. Mathematically, it can be written as given in Eq. 5.13 [166].

$$V_{FB2} = \Phi_m - \Phi_{si} \tag{5.13}$$

where, Φ_m and Φ_{si} are the work function of gate metal and silicon, respectively. The work function of silicon can be written as given in Eq. 5.14 [166].

$$\Phi_{si} = \chi_{si} + \frac{E_{G2}}{2} - V_{bi} - \left(\frac{qN_f}{C_{ox}}\right) \tag{5.14}$$

$$V_{bi} = \frac{kT}{q}\ln\frac{N_D}{n_i} \tag{5.15}$$

which is known as built-in potential at the source end. The parameters χ_{si}, and E_{G2} are the electron affinity and increased value of the energy band gap of silicon in region II. The gate capacitance, $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ and, N_f represents the oxide charge density at the silicon-oxide interface. Substituting the value of $C_{21}(Y_2)$, $C_{22}(Y_2)$, and $C_{23}(Y_2)$, in Eq. 5.6 and rearranging

the solution, the complete expression of $\psi_2(X_2, Y_2)$ has been obtained which is written in Eq. 5.16.

$$\psi_2(X_2, Y_2) = \psi_{s2}(Y_2) + \psi_{s2}(Y_2)\left\{\frac{C_{ox}}{\varepsilon_{si}}\right\}X_2 - \psi_{s2}(Y_2)\left\{\frac{C_{ox}}{\varepsilon_{si}}\right\}\frac{X_2^2}{t_{ch}} + (V_{FB2} - V_{GS})\left\{\frac{C_{ox}}{\varepsilon_{si}}\right\}X_2 - (V_{FB2} - V_{GS})\left\{\frac{C_{ox}}{\varepsilon_{si}}\right\}\frac{X_2^2}{t_{ch}} \quad (5.16)$$

Now, from Eq. 5.16 calculating the value of $\frac{\partial^2\psi_2(X_2,Y_2)}{\partial X_2^2}$ and $\frac{\partial^2\psi_2(X_2,Y_2)}{\partial Y_2^2}$, and substituting back in Eq. 5.5, a 1-D second-order differential equation [110] has been obtained as given.

$$\frac{\partial^2\psi_{s2}(Y_2)}{\partial Y_2^2} - \lambda_2^2.\left[\psi_{s2}(Y_2) - \sigma_2\right] = 0 \quad (5.17)$$

Here, $\lambda_2 = \sqrt{\alpha_{s2}}$ (5.18)

$$\alpha_{s2} = \sqrt{\frac{2C_{ox}K_s}{\varepsilon_{si}t_{ch}}} \quad (5.19)$$

The parameter K_S is a fitting parameter whose value lies between 0 and 1 and needs to be adjusted according to variations in V_{GS}, V_{DS}, N_D, and Φ_G to match the model predictions with the TCAD simulation results. Furthermore,

$$\sigma_2 = (V_{GS} - V_{FB2}) + \frac{qN_Dt_{ch}}{2C_{ox}} \quad (5.20)$$

The solution of Eq. 5.17 gives the final equation of surface potential in region II, which can be written in terms of the initial (x, y) coordinates as given in Eq. 5.21.

$$\psi_{s2}(y) = A_2\,.e^{((y-L_U).\lambda_2)} + B_2\,.e^{-((y-L_U).\lambda_2)} + \sigma_2 \quad (5.21)$$

The values of the unknowns A_2 and B_2 have been given in Eq. 5.22 and Eq. 5.23, respectively, and determined using the boundary conditions defined in Eq. 5.24 and Eq. 5.25.

$$A_2 = \psi_{i1} - \sigma_2 - B_2 \quad (5.22)$$

$$B_2 = \frac{(\psi_{i1} - \sigma_2).e^{L_G\lambda_2} - (\psi_{i2} - \sigma_2)}{2\sinh(L_G\lambda_2)} \quad (5.23)$$

- $\psi_{s2}(L_U) = \psi_{i1}$ (5.24)
- $\psi_{s2}(L_U+L_G) = \psi_{i2}$ (5.25)

In Eq. 5.24 and Eq. 5.25, the ψ_{i1} and ψ_{i2} represents the potential at the interface of regions I-II and II-III i.e., at $y = L_U$ and, $y = L_U + L_G$ respectively. The interfacial potential ψ_{i1} has been

calculated using the boundary conditions for the electric field at $y = L_U$ which has been given in Eq. 5.26 [184].

$$\left.\frac{\partial \psi_{s1}(y)}{\partial y}\right|_{y=L_U} = \left.\frac{\partial \psi_{s2}(y)}{\partial y}\right|_{y=L_U} \tag{5.26}$$

Similarly, the interfacial potential ψ_{i2} has been calculated using the boundary conditions for the electric field at $y = L_U + L_G$ as given in Eq. 5.27 [176].

$$\left.\frac{\partial \psi_{s2}(y)}{\partial y}\right|_{y=L_U+L_G} = \left.\frac{\partial \psi_{s3}(y)}{\partial y}\right|_{y=L_U+L_G} \tag{5.27}$$

The calculated value of $\psi_{i1}$and ψ_{i2} has been shown in Eq. 5.28 and Eq. 5.29, respectively [176].

$$\psi_{i1} = \frac{\left[(V_{bi} - \sigma_1).P_1 + \sigma_1.Q_1 - \sigma_2.R_1 + (V_{bi} + V_{DS}).\lambda_2\right]}{S_1} \tag{5.28}$$

$$\psi_{i2} = \frac{\left[(V_{bi} - \sigma_2).P_2 + \sigma_2.Q_2 - \sigma_3 R_2 + (V_{bi} + V_{DS}).\frac{\lambda_3}{M}\right]}{S_2} \tag{5.29}$$

The parameters σ_2 and σ_3 will be defined later on in sub-sections 5.3.1.2 and 5.3.1.2, respectively. Moreover, M has been formulated while calculating the fringe capacitance, C_{fr}, hence will be defined in section 5.3.4. The value of P1, R1, Q1, S1, P2, R2, Q2, and S2 has been given in Eq. 5.30-5.36, respectively.

$$P_1 = \left(\frac{\lambda_1}{M}\right).e^{\left(\frac{\lambda_1 L_U}{M}\right)}.\sinh(\lambda_2 L_G).\left[\coth\left(\frac{\lambda_1 L_U}{M}\right) - 1\right] \tag{5.30}$$

$$Q_1 = \left(\frac{\lambda_1}{M}\right).\sinh(\lambda_2 L_G).\coth\left(\frac{\lambda_1 L_U}{M}\right) \tag{5.31}$$

$$R_1 = \lambda_2.\left[\sinh(\lambda_2 L_G) - e^{(\lambda_2 L_G)} + 1\right] \tag{5.32}$$

$$S_1 = Q_1 - \lambda_2.\left[\sinh(\lambda_2 L_G) + e^{(\lambda_2 L_G)}\right] \tag{5.33}$$

$$P_2 = \lambda_2.e^{(\lambda_2 L_G)}.\sinh\left(\frac{\lambda_3 L_U}{M}\right).[\coth(\lambda_2 L_G) - 1] \tag{5.34}$$

$$Q_2 = \lambda_2.\sinh\left(\frac{\lambda_3 L_U}{M}\right).\coth(\lambda_2 L_G) \tag{5.35}$$

$$R_2 = \left(\frac{\lambda_3 L_U}{M}\right).\left[\sinh\left(\frac{\lambda_3 L_U}{M}\right) - e^{\left(\frac{\lambda_3 L_U}{M}\right)} + 1\right] \tag{5.36}$$

$$S_2 = Q_2 - \left(\frac{\lambda_3 L_U}{M}\right).\left[\sinh\left(\frac{\lambda_3 L_U}{M}\right) + e^{\left(\frac{\lambda_3 L_U}{M}\right)}\right] \tag{5.37}$$

In these equations the value of λ_1 and λ_3 is related to the region I and III and will be given in sub-sections 5.3.1.2 and 5.3.1.2, respectively

5.3.1.2 Surface potential model for region I

In comparison to gate overlap region II, the length of gate underlaps regions I and III are halved. The gate also influences the electron concentration in these regions due to the strong fringing field. Hence, full depletion in the underlap regions has also been assumed for V_{GS} = 0.0 V. As a result, the first term in the R.H.S. of Eq. 5.1 can be neglected. Also, as the position of origin has been assumed fixed on the top-left corner of the region I, hence, the potential distribution can be approximated in terms of the original coordinates x with y. Using the parabolic potential approach, the potential distribution in the region I can be written as given in Eq. 5.38 [183].

$$\psi_1(x, y) = C_{11}(y) + C_{12}(y).x + C_{13}(y).x^2 \qquad (5.38)$$

To find the value of the unknown $C_{11}(y)$, $C_{12}(y)$, and $C_{13}(y)$, the following boundary conditions have been applied to Eq. 5.38 [176].

- Since the proposed structure has been considered symmetric, hence, the potential at the top and bottom surface of the region I can be expressed as follows:

$$\psi_1(0,y) = \psi_1(t_{si},y) = \psi_{s1}(y) \qquad (5.39)$$

- The electric field at the Gate1 electrode can be written as:

$$\left.\frac{\partial\psi_1(x,y)}{\partial x}\right|_{x=0} = \frac{C_{eff}\left[\psi_{s1}(y)-V_{GS}-V_{FB1}\right]}{\varepsilon_{si}} \qquad (5.40)$$

- The electric field at the Gate2 electrode can also be written as:

$$\left.\frac{\partial\psi_1(x,y)}{\partial x}\right|_{x=t_{si}} = -\frac{C_{eff}\left[\psi_{s1}(y)-V_{GS}-V_{FB1}\right]}{\varepsilon_{si}} \qquad (5.41)$$

where, $V_{FB1}$is the flat band voltage of region I and has been defined in Eq. 5.42 [166].

$$V_{FB1} = \Phi_m - \chi_{si} + \frac{E_G}{2} - V_{bi} \qquad (5.42)$$

Importantly, here the parameter E_G represents the typical value of the band gap for silicon. Here, C_{eff} represents the effective capacitance in the region I and III, which is defined in terms of fringing capacitance as given in Eq. 5.43.

$$C_{eff} = K_g.C_{fr} \qquad (5.43)$$

K_g is another fitting parameter with a constant value of 2.25. The value of C_{fr} will be given later on in this chapter. Using these boundary conditions, the value of the unknowns $C_{11}(y)$, $C_{12}(y)$, and $C_{13}(y)$ has found as:

$$C_{11}(y) = \psi_{s1}(y) \tag{5.44}$$

$$C_{12}(y) = \frac{C_{eff}[\psi_{s1}(y) - V_{GS} - V_{FB1}]}{\varepsilon_{si}} \tag{5.45}$$

$$C_{13}(y) = \frac{C_{eff}}{\varepsilon_{si}} . \frac{[V_{GS} - V_{FB1} - \psi_{s1}(y)]}{t_{si}} \tag{5.46}$$

Using the value of $C_{11}(y)$, $C_{12}(y)$, and $C_{13}(y)$ in Eq. 5.38, the expression of $\psi_1(x, y)$ has been obtained, which can be written as given in Eq. 5.47.

$$\psi_1(x,y) = \psi_{s1}(y) + \psi_{s1}(y).\left\{\frac{C_{eff}}{\varepsilon_{si}}\right\}x - \psi_{s1}(y).\left\{\frac{C_{eff}}{\varepsilon_{si}}\right\}.\frac{x^2}{t_{si}} + (V_{FB1} - V_{GS}).\left\{\frac{C_{eff}}{\varepsilon_{si}}\right\}.x$$
$$-(V_{FB1} - V_{GS}).\left\{\frac{C_{eff}}{\varepsilon_{si}}\right\}.\frac{x^2}{t_{si}} \tag{5.47}$$

Following the approach illustrated in sub-section 5.3.1.1, the surface potential in the region I can be represented as given by:

$$\psi_{s1}(y) = A_1 .\ e^{\left(y.\frac{\lambda_1}{M}\right)} + B_1 .e^{-\left(y.\frac{\lambda_1}{M}\right)} + \sigma_1 \tag{5.48}$$

Where, $\lambda_1 = \sqrt{-K_{s0}}$ (5.49)

$$K_{s0} = \alpha_{s1}.K_S.M^2 \tag{5.50}$$

$$\alpha_{s1} = -\frac{2C_{eff}}{\varepsilon_{si}t_{si}} \tag{5.51}$$

$$\sigma_1 = (V_{GS} - V_{FB1}) + \frac{qN_Dt_{si}}{2C_{eff}} \tag{5.52}$$

The expression of the unknowns A_1 and B_1 have been given in Eq. 5.53 and Eq. 5.54, respectively, and determined using the boundary conditions defined in Eq. 5.55 and Eq. 5.56 [176].

$$A_1 = V_{bi} - \sigma_1 - B_1 \tag{5.53}$$

$$B_1 = \frac{(V_{bi} - \sigma_1).e^{\left(L_U.\frac{\lambda_1}{M}\right)} - \left(\psi_{i1} - \sigma_1\right)}{2\sinh\left(L_U.\frac{\lambda_1}{M}\right)} \tag{5.54}$$

$$\psi_{s1}(0) = V_{bi} \tag{5.55}$$

and $\psi_{s1}(L_U) = \psi_{i1}$ (5.56)

5.3.1.3 Surface potential for region III

Region III comprises the silicon area which is displaced in y direction w.r.t. the origin coordinates in the region I. Hence, new origin coordinates X_3 and Y_3 for region III in the has been defined in the following way.

$$x=X_3 \Rightarrow X_3= x \text{ and} \tag{5.57}$$

$$y=Y_3+(L_U+L_G) \Rightarrow Y_3= y-(L_U+L_G) \tag{5.58}$$

As regions I and III are symmetric, hence, similar assumption of strong depletion in region III has also been considered. As a result, the 2-D Poisson's equation defining the channel potential in region III can be written as [105]:

$$\frac{\partial^2\psi_3(X_3,Y_3)}{\partial X_3^2}+\frac{\partial^2\psi_3(X_3,Y_3)}{\partial Y_3^2}=-\frac{qN_D}{\varepsilon_{si}} \tag{5.59}$$

where, $\psi_3(X_3,Y_3)$ is the channel potential in region III. A parabolic potential profile has been assumed to obtain the approximate solution of the 2-D distribution of $\psi_3(X_3,Y_3)$ [181].

$$\psi_3(X_3,Y_3)=C_{31}(Y_3)+C_{32}(Y_3)X_3+C_{33}(Y_3)X_3^2 \tag{5.60}$$

To find the value of the unknown $C_{31}(Y_3)$, $C_{32}(Y_3)$, and $C_{33}(Y_3)$, the following boundary conditions have been applied on Eq. 5.60 for the potential and electric field at the top and bottom surfaces [178]:

- Since the two gate electrodes in the proposed structure are symmetric, hence, the potential at the top and bottom surface of region III can be expressed as follows:

$$\psi_3(0,Y_3)=\psi_3(t_{si},Y_3)=\psi_{s3}(Y_3) \tag{5.61}$$

- The electric field at the Gate1 electrode can be written as given:

$$\left.\frac{\partial\psi_3(X_3,Y_3)}{\partial X_3}\right|_{X_3=0}=\frac{C_{eff}\left[\psi_{s3}(Y_3)-V_{GS}-V_{FB3}\right]}{\varepsilon_{si}} \tag{5.62}$$

- The electric field at the Gate2 electrode can be written as given:

$$\left.\frac{\partial\psi_3(X_3,Y_3)}{\partial X_3}\right|_{X_3=t_{si}}=-\frac{C_{eff}\left[\psi_{s3}(Y_3)-V_{GS}-V_{FB3}\right]}{\varepsilon_{si}} \tag{5.63}$$

where, $V_{FB3}$is the flat band voltage of region III and can be written as follow [166].

$$V_{FB3}=\Phi_m-\chi_{si}+\frac{E_G}{2}-V_{bi} \tag{5.64}$$

Using these boundary conditions, the value of the unknowns $C_{31}(Y_3)$, $C_{32}(Y_3)$, and $C_{33}(Y_3)$ is found as:

$$C_{31}(Y_3)=\psi_{s3}(Y_3) \tag{5.65}$$

$$C_{32}(Y_3)=\frac{C_{eff}\left[\psi_{s3}(Y_3)-V_{GS}-V_{FB3}\right]}{\varepsilon_{si}} \tag{5.66}$$

$$C_{33}(Y_3) = \frac{C_{eff}}{\varepsilon_{si}} \frac{[V_{GS} - V_{FB3} - \psi_{s3}(Y_3)]}{t_{si}} \quad (5.67)$$

Using the value of $C_{31}(Y_3)$, $C_{32}(Y_3)$, and $C_{33}(Y_3)$ in Eq. 5.60, the expression for $\psi_3(X_3, Y_3)$ has been obtained as given in Eq. 5.34.

$$\psi_3(X_3,Y_3) = \psi_{s3}(Y_3) + \psi_{s3}(Y_3)\left\{\frac{C_{eff}}{\varepsilon_{si}}\right\}X_3 - \psi_{s3}(Y_3)\left\{\frac{C_{eff}}{\varepsilon_{si}}\right\}\frac{X_3^2}{t_{si}} + (V_{FB3}-V_{GS})\left\{\frac{C_{eff}}{\varepsilon_{si}}\right\}X_3$$

$$- (V_{FB3} - V_{GS})\left\{\frac{C_{eff}}{\varepsilon_{si}}\right\}\frac{X_3^2}{t_{si}} \quad (5.68)$$

Following the approach illustrated in sub-section 5.3.1.1, the surface potential for region III has been represented in terms of initial coordinates x- and y- as given by:

$$\psi_{s3}(y) = A_3.\, e^{\left((y-L_U-L_G).\frac{\lambda_3}{M}\right)} + B_3.e^{-\left((y+L_U+L_G).\frac{\lambda_3}{M}\right)} + \sigma_3 \quad (5.69)$$

where, $\lambda_3 = \sqrt{-K_{d0}}$ (5.70)

$$K_{d0} = \alpha_d\, K_S M^2 \quad (5.71)$$

$$\alpha_d = -\frac{2C_{eff}}{\varepsilon_{si} t_{si}} \quad (5.72)$$

$$\sigma_3 = (V_{GS} - V_{FB3}) + \frac{qN_D t_{si}}{2C_{eff}} \quad (5.73)$$

The value of the unknowns A_3 and B_3 have been given in Eq. 5.74 and Eq. 5.75, respectively, and determined using the boundary conditions defined in Eq. 5.76 and Eq. 5.77 [176].

$$A_3 = \psi_{i2} - \sigma_3 - B_3 \quad (5.74)$$

$$B_3 = \frac{(\psi_{i2} - \sigma_3).e^{\left(L_U.\frac{\lambda_3}{M}\right)} - (V_{bi} + V_{DS} - \sigma_3)}{2\sinh\left(L_U.\frac{\lambda_3}{M}\right)} \quad (5.75)$$

$$\psi_{s3}(L_G+L_U) = \psi_{i2} \quad (5.76)$$

and $\psi_{s3}(L_G+2L_U) = V_{bi}+V_{DS}$ (5.77)

where, V_{DS} is the drain-to-source voltage.

5.3.2 Center potential model for regions I, II, and III

In a junctionless transistor, initially, the OFF-state leakage current starts flowing through the leakiest path available at the center of the silicon layer. Hence, the center potential becomes an important parameter of interest, unlike the conventional MOSFETs in which the current flows near the surface of the silicon layer. The center potential $\psi_{c1}(y)$ for the region I can be found by putting $x = \frac{t_{si}}{2}$ in Eq. 5.47 [105].

$$\psi_{c1}(y) = a_1.\psi_{s1}(y) + b_1 \quad (5.78)$$

$$a_1 = 1+\frac{1}{8}\left(\frac{\lambda_1}{M}\right)^2.t_{si}^2 \quad (5.79)$$

$$b_1 = (V_{FB1} - V_{GS}).\left\{\frac{1}{8}\left(\frac{\lambda_1}{M}\right)^2.t_{si}^2\right\} \quad (5.80)$$

In a similar manner, $\psi_{c2}(y)$ and $\psi_{c3}(y)$ can be obtained, by putting $x=\frac{t_{ch}}{2}$ and $x=\frac{t_{si}}{2}$ in Eq. 5.16, and Eq. 5.68, respectively. The final expressions for the center potential of regions II and III have been given as:

$$\psi_{c2}(y) = a_2.\psi_{s2}(y) + b_2 \quad (5.81)$$

$$a_2 = 1+\frac{1}{8}\lambda_2^2.t_{ch}^2 \quad (5.82)$$

$$b_2 = (V_{FB2} - V_{GS}).\left\{\frac{1}{8}\lambda_2^2.t_{ch}^2\right\} \quad (5.83)$$

Also, $\psi_{c3}(y) = a_3.\psi_{s3}(y) + b_3$ (5.84)

$$a_3 = 1+\frac{1}{8}\left(\frac{\lambda_3}{M}\right)^2.t_{si}^2 \quad (5.85)$$

$$b_3 = (V_{FB3} - V_{GS}).\left\{\frac{1}{8}\left(\frac{\lambda_3}{M}\right)^2.t_{si}^2\right\} \quad (5.86)$$

5.3.3 The minimum center potential, ψ_{c2min}

The minimum center potential defines the subthreshold current flowing in a junctionless device. Due to the parabolic profile, the minimum value of center potential has been found in region II of R_DGJLFET. To calculate the value of minimum center potential and estimate its location, it must follow the given relationship [105]:

$$\frac{\partial\psi_{c2}(y)}{\partial y} = 0 \quad (5.87)$$

Using Eq. 5.21 in Eq. 5.81 and then putting the value of $\psi_{c2}(y)$ in Eq. 5.87 gives the location of minimum center potential as given by:

$$y_{min} = L_U + \frac{1}{2\lambda_2}\ln\left(\frac{B_2}{A_2}\right) \quad (5.88)$$

Now putting the value of y_{min} in Eq. 5.42, the minimum center potential is given as:

$$\psi_{c2min} = a_2.\left[2.\sqrt{A_2B_2} + Y_2\right] + b_2 \quad (5.89)$$

5.3.4 The fringe capacitance (C_{fr}) in the underlap region I and III

The Gate1 and Gate2 electrodes have no overlap over the region I and III as depicted in Figure 5.1. Hence, the effective value of capacitance is different from the gate capacitance (C_{ox}), which is called fringe capacitance (C_{fr}). The C_{fr} arises due to the electric field lines

from both gate electrodes through the spacer dielectric. As the L_U is half of the L_G it means that the C_{fr} remains significant throughout the underlap regions and depletes the electrons considerably. Hence, the estimation of C_{fr} becomes important for defining the potential profile in underlaps regions I and III. The C_{fr} has been determined using the conformal mapping technique [176], [177].

$$C_{fr} = \frac{2\varepsilon_{ox}}{m\pi M} \tag{5.90}$$

where m=3 has been used to satisfy |sin(mπ/2)| =1 [176] and to match the model with simulation results.

$$M = -\frac{L_U}{\sinh\left(\cosh^{-1}\left(\frac{t_{ox}+(D_{RS}+t_g)}{t_{ox}}\right)\right)} \tag{5.91}$$

5.3.5 Analytical model for subthreshold drain current and subthreshold slope

The drain current in subthreshold current can be written as [110]:

$$I_{DS} = \frac{q\mu_n n_i V_T W_G.\left[1 - e^{\left(-\frac{V_{DS}}{V_T}\right)}\right]}{\left[\int_0^{L_U}\frac{dy}{\int_0^{t_{si}} e^{\left(\frac{\psi_{c1}(y)}{V_T}\right)}dx} + \int_{L_U}^{L_U+L_G}\frac{dy}{\int_0^{t_{ch}} e^{\left(\frac{\psi_{c2}(y)}{V_T}\right)}dx} + \int_{L_U+L_G}^{2L_U+L_G}\frac{dy}{\int_0^{t_{si}} e^{\left(\frac{\psi_{c3}(y)}{V_T}\right)}dx}\right]} \tag{5.92}$$

Here, μ_n is the electron mobility and W_G is the gate width. To solve Eq. 5.92, the analytical approximation has been used for the three terms in the denominator as given by [178]:

$$I_{DS} = \frac{q\mu_n n_i V_T W_G.\left[1 - e^{\left(-\frac{V_{DS}}{V_T}\right)}\right]}{[F_I + F_{II} + F_{III}]} \tag{5.93}$$

Where,

$$F_I = \int_0^{L_U}\frac{dy}{G_I(y)} \approx \frac{L_U}{4}\left[\frac{1}{2G_I(0)} + \frac{1}{\sum_1^3 G_I(k_1.\frac{L_U}{4})} + \frac{1}{2G_I(L_U)}\right] \tag{5.94}$$

$$F_{II} = \int_{L_U}^{L_U+L_G}\frac{dy}{G_{II}(y)} \approx \frac{L_G}{6}\left[\frac{1}{2G_{II}(L_U)} + \frac{1}{\sum_1^4 G_{II}(k_2.\frac{(L_U+L_G)}{6})} + \frac{1}{2G_{II}(L_U+L_G)}\right] \tag{5.95}$$

$$F_{III} = \int_{L_U+L_G}^{2L_U+L_G}\frac{dy}{G_{III}(y)} \approx \frac{L_U}{4}.\left[\frac{1}{2G_{III}(L_U+L_G)} + \frac{1}{\sum_1^3 G_{III}(k_3.\frac{(2L_U+L_G)}{4})} + \frac{1}{2G_{III}(2L_U+L_G)}\right] \tag{5.96}$$

Here, $G_I(y)$, $G_{II}(y)$, and $G_{III}(y)$ are defined using the trapezoidal rule as follows [109], [178]:

$$G_I(y) = \int_0^{t_{si}} e^{\left(\frac{\psi_{c1}(y)}{V_T}\right)}.dx = t_{si}.\left[e^{\left(\frac{\psi_{c1}(y)}{V_T}\right)}\right] \tag{5.97}$$

$$G_{II}(y) = \int_0^{t_{ch}} e^{\left(\frac{\psi_{c2}(y)}{V_T}\right)}.dx \approx \frac{t_{ch}}{4}.\left[e^{\left(\frac{\psi_{s2}(y)}{V_T}\right)} + e^{\left(\frac{\psi_{c2}(y)}{V_T}\right)} + 2.e^{\left(\frac{\psi_2(t_{ch}/4,\ y)}{V_T}\right)}\right] \tag{5.98}$$

$$G_{III}(y) = \int_0^{t_{si}} e^{\left(\frac{\psi_{c3}(y)}{V_T}\right)}.dx = t_{si}.\left[e^{\left(\frac{\psi_{c3}(y)}{V_T}\right)}\right] \tag{5.99}$$

Eq. 5.94-5.96 and Eq. 5.97-5.99 represents the approximation along y- and x-directions, respectively. The subthreshold slope with units of mV/dec represents the amount of V_{GS} needed to change the I_{DS} by one decade and is formulated as the inverse of the slope of $\log(I_{DS})$ vs. V_{GS} [166]. The formula shown in Eq. 5.100 has been used to calculate the subthreshold slope for $V_{DS} = 1.0$ V.

$$SS = \left[\frac{\partial \log(I_{DS})}{\partial V_{GS}}\right]^{-1} \tag{5.100}$$

5.4 Model validation and discussions

5.4.1 Simulation set-up

The results of potential profiles and subthreshold drain current evaluated from the analytical model have been validated by comparing them with the simulation results obtained from the Silvaco Atlas TCAD tool [137]. Various physical models have been used in TCAD simulations such as *fermi* to include the effect of heavy doping in silicon [135], the SRH model for carrier recombination [137][138], the non-local BTBT model [134], the density gradient model to account for the carrier confinement [136] and the Lombardy model to consider the dependence of carrier mobility on doping concentration, temperature, and transverse electric field [134]. It is to be noted that the symbols represent the TCAD simulation results while the lines depict the model results. With these considerations, the center potential distribution has been captured with the analytical model to a good extent. The effect of the gate and drain biases, doping concentration, and gate work function of R_DGJLFET on the center potential in the OFF-state has been presented.

For the R_DGJLFET, a uniform n-type doping of 1×10^{19} cm^{-3} has been used in the silicon layer [63]. The silicon thickness in underlap (region I and III) and recessed (region II) has been kept fixed at 10 nm and 6 nm, respectively. The HfO_2 with an effective oxide thickness of 1 nm has been used as the gate dielectric material [132]. The gate work function (Φ_G) of 5.1 eV has been chosen for achieving effective OFF-state depletion [133].

5.4.2 Effect of drain and gate biases on the center potential

A constant width of 1 µm for the gate electrode (W_G) has been used in all simulations. For R_DGJLFET with a gate length of 20 nm, the center potential profile along the channel for different values of drain bias has been presented in Figure 5.2(a). From Figure 5.2(a), it can be seen that for zero gate and drain voltages, the center potential profile is symmetric throughout the device. However, increasing the value of V_{DS} (= 50 mV) results in a small uplift of center potential especially in the right half (20 nm ≤ y ≤ 40 nm) portion of the device. As the value of drain voltage is increased, the energy barrier at the drain-channel interface lowers down, which eases the electrons to reach the drain end and represents the increase in center potential.

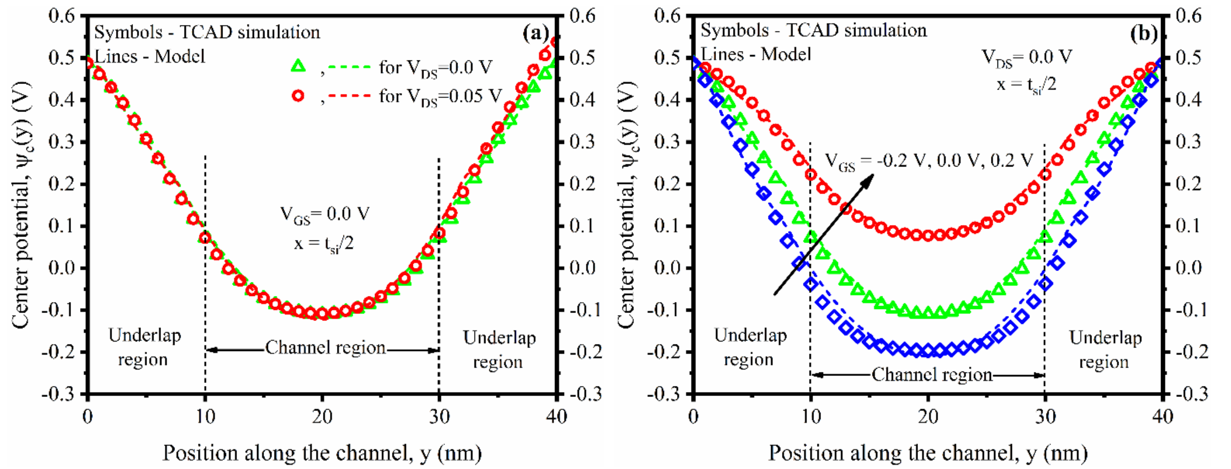


Figure 5.2 (a) Center potential along the channel in R_DGJLFET with variations in (a)V_{DS} and, (b) V_{GS}.

Figure 5.2(b) shows the effect of variations in V_{GS} on the center potential in the y-direction. From Figure 5.2(b), it has been observed that for the zero value of both V_{GS} and V_{DS}, the center potential in region II becomes negative which indicates the depletion of electrons from the channel. Tuning the V_{GS} with a negative value (-0.2 V) favours the restriction on mobile charge carriers in the channel more efficiently which leads to a more negative potential. However, increasing the value of V_{GS} towards the positive end (0.2 V) results in the weakening of the electric field $\left.\frac{\partial\psi_2(X_2,Y_2)}{\partial X_2}\right|_{X_2=0}$ and $\left.\frac{\partial\psi_2(X_2,Y_2)}{\partial X_2}\right|_{X_2=t_{ch}}$ in region II as given in Eq. 5.8 and Eq. 5.9, respectively. The reduced value of the electric field permits more electrons in the channel and higher center potential has been observed as shown in Figure 5.2(b).

5.4.3 Effect of variations in N_D and Φ_G on the center potential

The junctionless device needs to be heavily doped to get a high ON-current [17]. The effect of variations in N_D on center potential along the channel has been presented in Figure 5.3(a).

From Figure 5.3(a) it is observed that the variations in N_D with values of 1×10^{19} cm^{-3}, 5×10^{18} cm^{-3}, and 1×10^{18} cm^{-3} change the center potential proportionally.

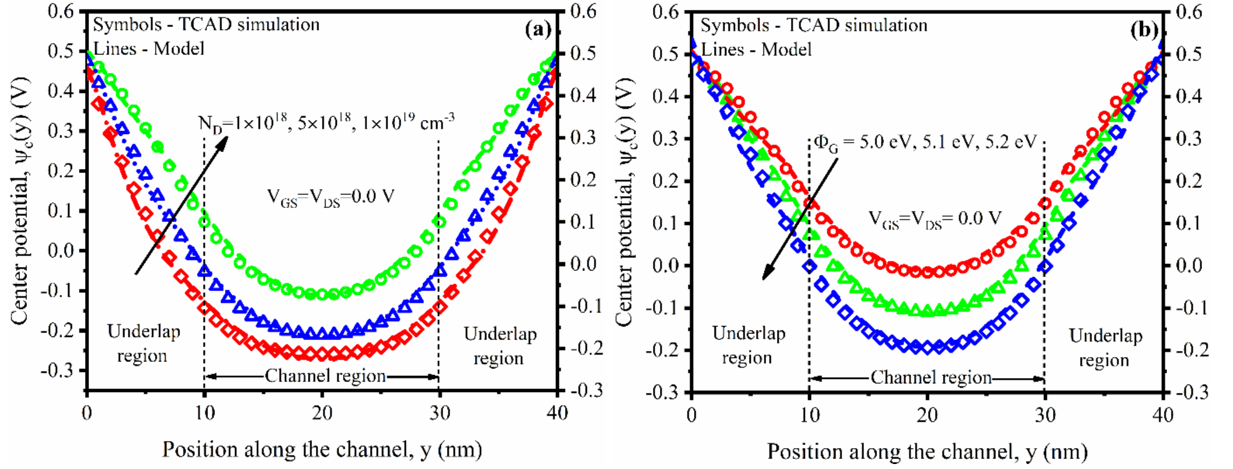


Figure 5.3 Center potential along the channel in R_DGJLFET with variations in (a) N_D and, (b) Φ_G.

Smaller doping concentration favours channel depletion more efficiently. Mathematically, the effect can be understood from Eq. 5.19. Decreasing the value of N_D reduces the parameters- σ_2 which in turn lowers down the $\psi_{s2}(y)$ in Eq. 5.21 and hence, $\psi_{c2}(y)$ in Eq. 5.81. A similar effect can be observed in the region I and II also, in terms of $\sigma_1$and σ_3, which ultimately affects $\psi_{c1}(y)$ in Eq. 5.78, and $\psi_{c3}(y)$ in Eq. 5.84 with similar means, respectively.

The effect of variation in Φ_G on the center potential along the channel has been shown in Figure 5.3(b). From Figure 5.3(b), it has been observed that the gate work function is the key to regulating the OFF-state behaviour of R_DGJLFET. Increasing the work function values from 5.0 eV to 5.2 eV establishes better gate control over the channel region which leads to lesser smaller potential. The higher the value of Φ_G, the greater the flat-band voltage of R_DGJLFET. The increased value of V_{FB} leads to a reduction in the value of σ_2 in Eq. 5.19, which eventually reduces both $\psi_{s2}(y)$ and hence, $\psi_{c2}(y)$ in Eq. 5.21, and Eq. 5.81, respectively.

5.4.4 Relation between center and surface potentials

Although the center potential governs the current flow in a junctionless device, still the dependence of center potential on surface potential in R_DGJLFET has been analysed. As depicted in Figure 5.4(a), it has been found that the $\psi_{s2}(y)$ varies linearly with variations in $\psi_{c2}(y)$. The curve follows the linear relationship between $\psi_{s2}(y)$ and $\psi_{c2}(y)$ as given in Eq. 5.74. In Figure 5.4(a), $\psi_{c2}(y)$ has been changed with variations in V_{GS} in the range of 0.0 V to 0.65 V. The linear relationship between $\psi_{s2}(y)$ and $\psi_{c2}(y)$ is also maintained in underlap regions I and III as given in Eq. 5.79, and Eq. 5.85, respectively. The location of the

minimum center potential ψ_{c2min} has been found on the leakiest path in the channel region for $V_{GS} = 0V$.

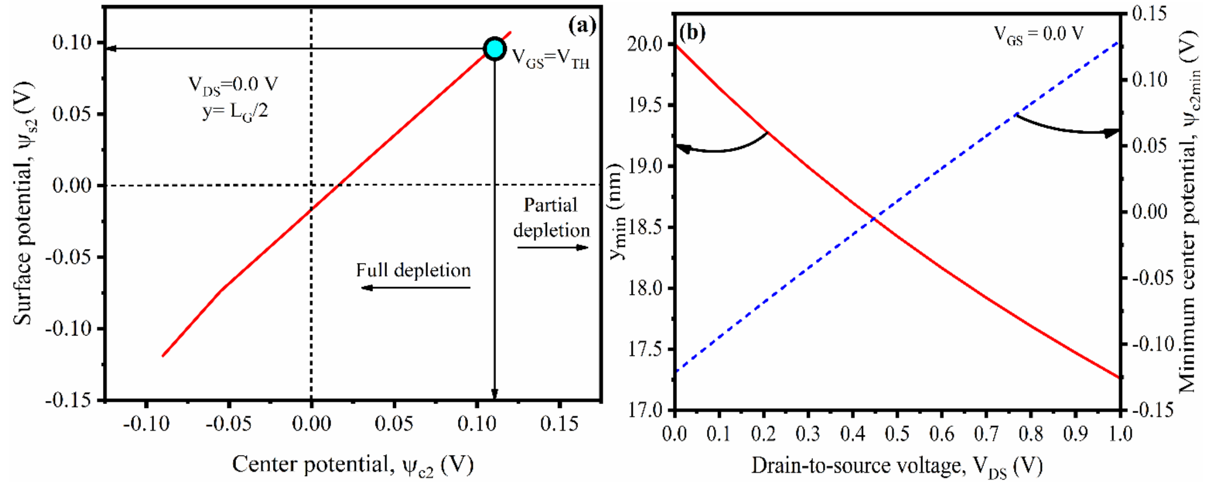


Figure 5.4(a) Relation between center and surface potential, (b) effect of V_{DS} on minimum center potential and its location in R_DGJLFET.

In R_DGJLFET, the maximum effect of the gate electric field occurs in region II, hence the location of ψ_{c2min} (i.e. y_{min}) has been observed in this region. However, the y_{min} depends on V_{DS} non-linearly, and with an increase in V_{DS}, its position shifts towards the source end as shown in Figure 5.4(b), deduced from Eq. 5.88. Moreover, as described earlier in the context of $\psi_{c2}(y)$, the ψ_{c2min} increases with V_{DS} and changes its value from negative domain to positive as shown in Figure 5.4(b).

5.4.5 Effect of variations in N_D and Φ_G on the subthreshold drain current

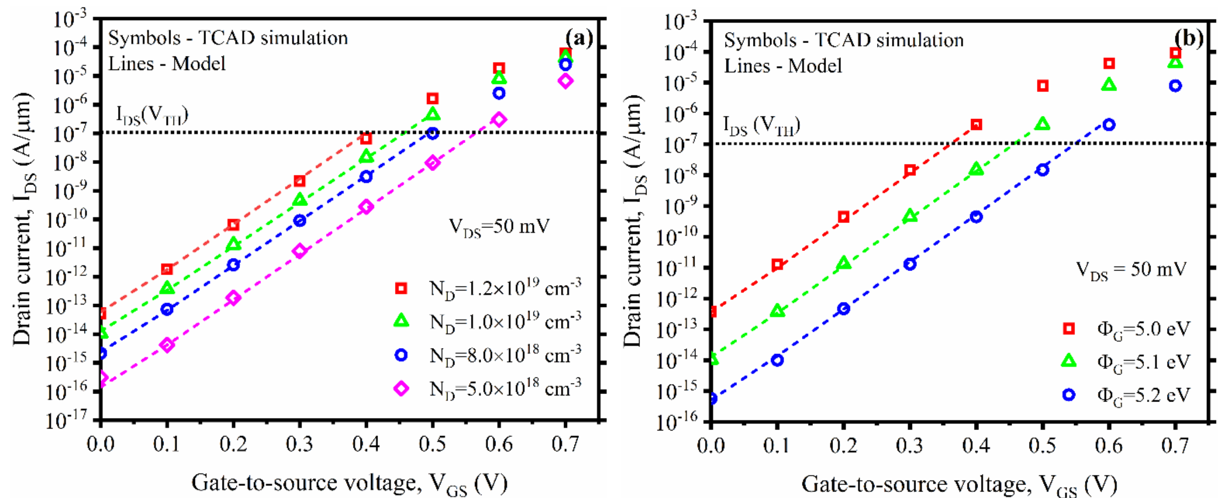


Figure 5.5 Subthreshold drain current characteristics for R_DGJLFET with variations in (a) N_D and, (b) Φ_G.

The foremost motive of this work is to analytically model the potential profile and subthreshold drain current (I_{DS}) in R_DGJLFET. The I_{DS} has been shown on a logarithmic scale in the subsequent figures as the current value varies significantly in the subthreshold

region. Figure 5.5(a) shows the subthreshold characteristics in terms of I_{DS} vs. V_{GS} for different values of N_D. In Figure 5.5(a), the $I_{DS}(V_{TH})$ denote the subthreshold current value at threshold voltage (V_{TH}) which has been obtained with the constant current method [109] in TCAD simulation results. It can be analysed that doping the silicon channel with a higher value of N_D results in more leakage current in OFF-state. However, reducing the doping concentration with $N_D < 10^{19}$ cm^{-3} improves the depletion with a penalty of increased V_{TH}.

In Figure 5.5(b), the effect of gate work function with different values of 5.0 eV, 5.1 eV, and 5.2 eV on the subthreshold characteristics has been presented. Here, it can be observed that increasing the value of Φ_G shifts the overall curve downwards due to the increased value of the electric field in the device which results in improved depletion with smaller electron concentration.

5.4.6 The effect of variations in EOT and L_G on subthreshold drain current

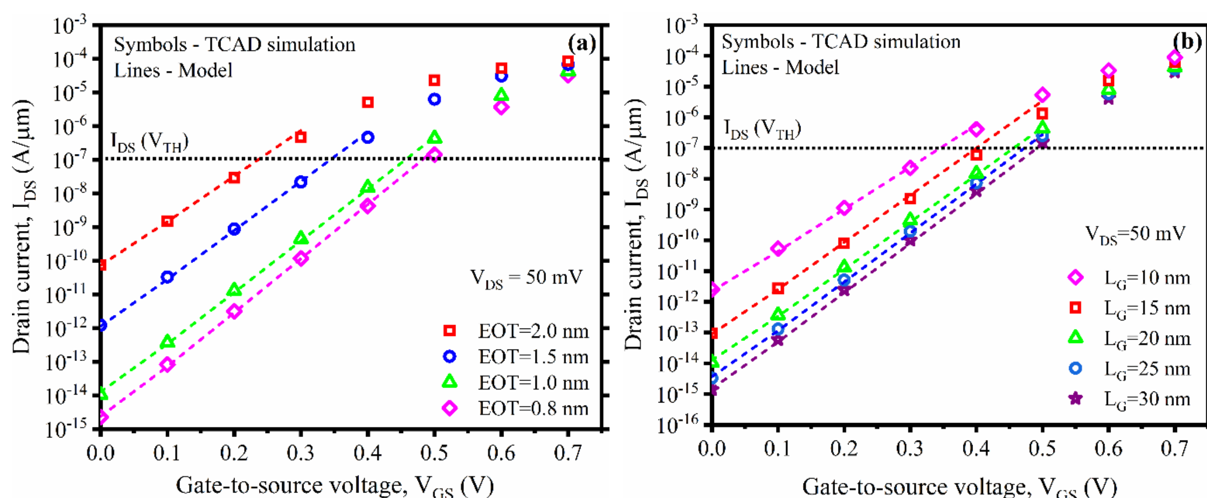


Figure 5.6 Subthreshold drain current characteristics for R_DGJLFET with variations in (a) EOT, and (b) L_G.

In R_DGJLFET, the HfO_2 has been used as high-k material, which offers similar charge-voltage profiles with a thicker dielectric layer. However, achieving the EOT precisely is still a process issue. Hence, to account for the importance of EOT, its effect on I_{DS}-V_{GS} characteristics has been reflected in Figure 5.6(a). From Figure 5.6(a), it can be observed that in the case of R_DGJFET with L_G=20 nm, patterning the thicker gate dielectric (EOT > 1 nm) deteriorates the I_{DS} significantly for V_{GS}=0.0 V which eventually lead to a reduction in I_{ON}/I_{OFF} ratio.

The performance degradation with thicker gate dielectric occurs due to smaller gate oxide capacitance which results in the weakening of the electric field across the channel as given in Eq. 5.8 and Eq. 5.9. The gate length, L_G is another important design parameter to analyse the performance of a transistor in the subthreshold region. Figure 5.6(b) shows the effect of

variations in L_G on I_{DS} for the proposed R_DGJLFET. From Figure 5.6(b), it has been observed that in the shown range of V_{GS} the reduction in L_G results in a higher value of current in the R_DGJLFET. With a smaller value of $L_{G,}$ the distance between the drain and the source end is reduced which increases the effect of drain bias in the channel. This helps to increase the number of electrons (i.e. higher I_{DS}) in the channel for the applied gate voltage.

5.4.7 The effect of gate length variations on the subthreshold slope

The SS is an important parameter of a MOSFET device which reflects its ability to turn off quickly. The SS for the developed model has been calculated using Eq. 5.100. For varying the L_G from 45 nm down to 10 nm, the SS for R_DGJLFET has been presented in Figure 5.7.

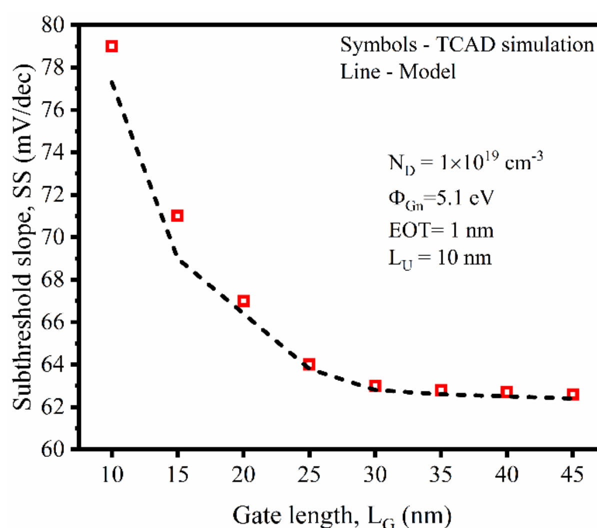


Figure 5.7 Subthreshold slope of R_DGJLFET with variations in L_G.

From Figure 5.7, it can be observed that the developed model of R_DGJLFET closely approximates the SS with the obtained value from the TCAD tool up to $L_G \geq 20$ nm. However, by reducing the L_G less than 20 nm the model slightly overestimates the value of SS, which may be due to the non-inclusion of SCEs and QCEs in the work.

5.5 Conclusions

In this chapter the analytical model for potential and drain current in the subthreshold region of R_DGJLFET has been formulated. The model has been developed comprehensively by solving a 2-D Poisson's equation in three continuous rectangular silicon regions, resulting in explicit expressions for the surface potential, center potential, and subthreshold drain current. The developed analytical model has been validated with the TCAD based simulation results and both have been found reasonably close. The model provides enhanced physical insights with the incorporation of the effect of various design parameters such as N_D, Φ_G, EOT, and L_G on the I_{DS}. Moreover, the effect of reduction in L_G on SS has also been modeled.

Chapter-6
Conclusions and future scope of the present work

6.1 Conclusions

Advancement in today's semiconductor industry has been motivated by the goals of low power dissipation and high performance in nanoscale devices. Lately, the JLFETs with the absence of abrupt p-n junctions and similar I-V characteristics as that of IM counterparts have been materialized to fulfill these requirements. The research work presented in the thesis has been divided into three major parts. Firstly, the JLFET with recessed silicon in the channel region i.e., R_DGJLFET has been proposed and its performance has been compared with C_DGJLFET. The channel and gate design guidelines for the proposed R_DGJLFET have been provided by investigating the variations in L_G, D_{RS}, L_{RS}, EOT, Φ_G, and misalignment. Secondly, the various logic gates based on the proposed R_DGJLFET namely NOT, 2-input NAND, and NOR have been implemented. In last, the analytical model for potential and drain current in the subthreshold region has been developed and validated in close agreement with the respective TCAD simulation results.

In the present work, it has been concluded that:

- The structural engineering with reduced silicon thickness between the two gate electrodes effectively helps to achieve improved channel depletion in the proposed R_DGJLFET by restricting the electron density in OFF-state. The proposed device reflects better performance with its smaller I_{OFF}, higher I_{ON}/I_{OFF}, steeper SS, and lower DIBL while maintaining its performance edge over the C_DGJLFET by scaling the L_G.
- In addition, the effect of variations in D_{RS} and L_{RS} has been studied and found that these parameters can be used for coarse and fine-tuning of the performance of R_DGJLFET, respectively. Aiming at the design of the gate electrode, it has been observed that the proposed R_DGJLFET continuously outperforms the C_DGJLFET for different values of EOT and Φ_G with its improved and robust performance. A range of Φ_G has been found for obtaining the optimum performance from the proposed R_DGJLFET.
- Furthermore, it has been observed that the R_DGJLFET reflects robustness against misalignment with smaller performance variations in terms of SS and DIBL in the digital domain and TGF, $f_{T,}$ and GBW in the analog domain, comparatively.
- At the circuit level, the R_DGJLFET based digital logic gates namely NOT, 2-input NAND, and NOR have been implemented with desired transient behaviour. The

R_DGJLFET based inverter reflects steeper VTC and wider low/high noise margins while it presents an attractive low-power solution with smaller P_{DC}, comparable P_{SW}, and lesser P_{SC}. The proposed R_DGJLFET also works reliably in an analog block namely a CS amplifier and amplifies a sinusoidal signal of milli volt amplitude within a wide frequency range.

- The parabolic potential approximation based 2-D analytical model has been developed for the subthreshold drain current of R_DGJLFET and explicit expressions for surface potential, center potential, and the drain current have been obtained. The developed analytical model reflects close agreement with the respective TCAD simulation results. The model enhances the physical insights about the operation of R_DGJLFET in the subthreshold regime considering the effect of N_D, L_G, Φ_G, and EOT and depicts the effect of gate length scaling on SS successfully.

6.2 Future scope

The work findings presented in section 6.1 helps to understand the operation of R_DGJLFET from the device to the circuit level in a qualitative manner. Moreover, the present work provides a technological platform to further stir the research efforts in the field of design, modeling, and circuit implementation of semiconductor devices.

- In the present work, most of the simulation work has been done considering the uniform doping profile in the silicon layer which does not represent a practical circumstance. Therefore, the investigation of the performance of the proposed R_DGJLFET with random dopant fluctuations can lead to more new intuitions.
- The simulation study can also be done by incorporating the effect of temperature, dual/triple gate material/dielectrics, and different spacer materials.
- The analytical modeling of the proposed R_DGJLFET has been done in a subthreshold regime using the parabolic potential approach, which agrees with the TCAD simulation results in a good manner. Moreover, a mathematical analysis valid in all operating regimes of R_DGJLFET can be done while considering 1) structural quantum confinement and, 2) non-equilibrium Green’s function approach.
- To confirm the utility, the experimental realization of the proposed R_DGJLFET can be done though contemplating its remarkable performance as an inducement.

Appendix-A

Suggested major fabrication steps for proposed R_DGJLFET

The top-view of the sequence of major fabrication steps to realize the R_DGJLFET has been presented in Figure A1.

Step 1: - Considering silicon-on-insulator (SOI) wafer of Unibond^{TM} as the starting material, a layer of intrinsic silicon with a thickness of 1 μm will be defined over the whole SOI wafer. Then using electron beam lithography (EBL) and inductively coupled plasma (ICP) dry etching technique the intrinsic silicon layer with length and width of 40 nm and 10 nm, respectively will be patterned over the buried oxide (BOX) of 200 nm thickness (not shown) as shown in Figure A1(a).

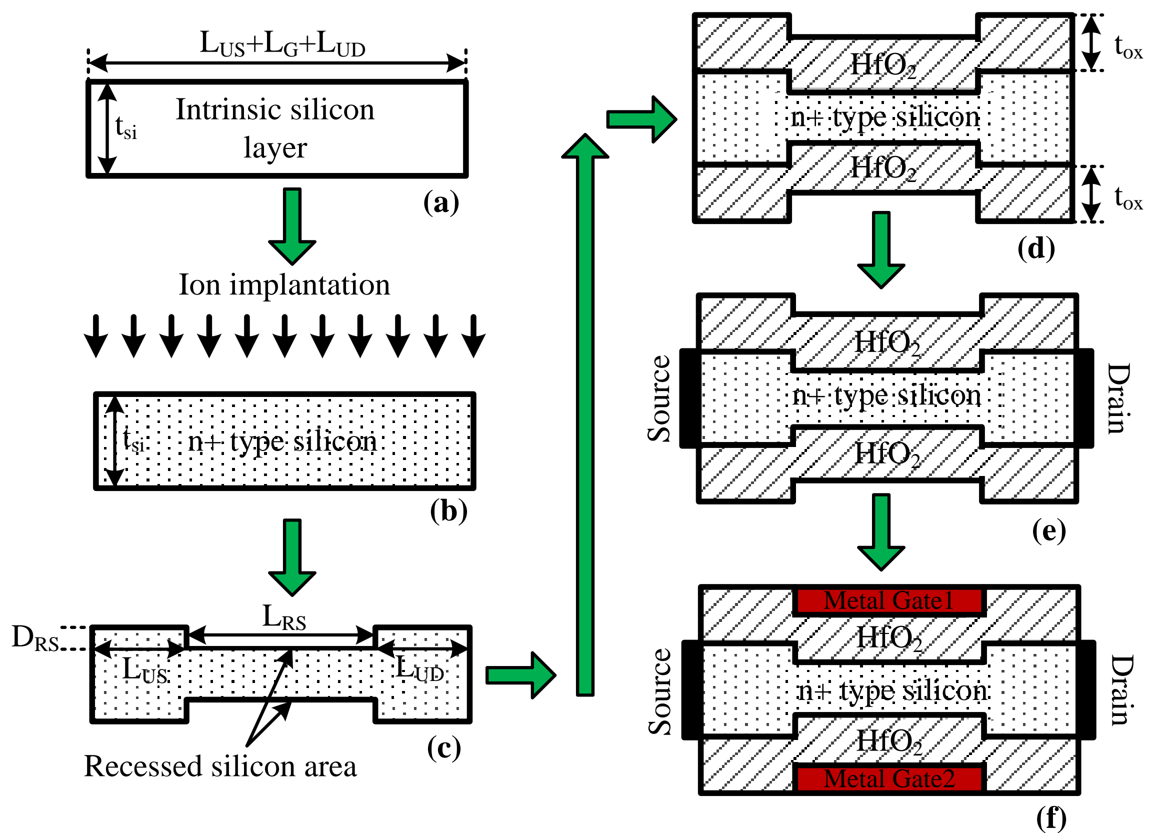


Figure A1 Top-view of suggested fabrication steps for n-channel R_DGJLFET.

In Figure A1(a), it is to be noted that the plane of paper has been considered as the top surface of BOX layer and the length and width of silicon film has been labelled with respective dimensions of R_DGJLFET.

Step 2: - In the second step, the intrinsic silicon layer will be uniformly doped with Arsenic atoms for with appropriate dose concentration and implant energy in order to realize a n+ type junctionless device as shown in Figure A1(b). Subsequently, the sample will be annealed in Nitrogen ambient at 1000°C for 5 minutes.

Step 3: - In third step the doped silicon layer will be recessed up to predefined length and depth in the channel area using EBL and ICP techniques. The top cross-sectional view of the resulting profile has been shown in Figure A1(c).

Step 4: - In the next step, using the atomic layer deposition system, a layer of HfO_2 will be deposited over the recessed and underlap areas of the doped silicon layer. The HfO_2 layer will be patterned for the thickness of 1 nm (EOT) using BCl_3 plasma etching over the channel region as shown in Figure A1(d).

Step 5: - Aluminium metallization will be done and the source/drain contacts will be defined as depicted in Figure A1(e).

Step 6: - In last step, the gate material with appropriate work function will be deposited over the HfO_2 to define the Gate1 and Gate2 electrodes over the channel region as reflected in Figure A1(f).

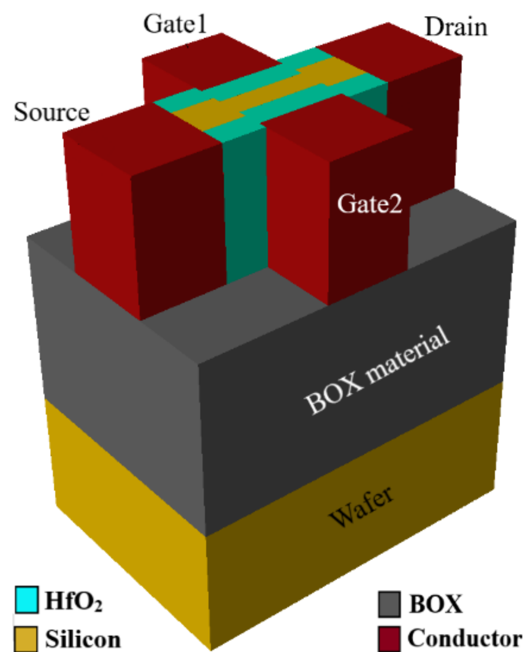


Figure A2 3-D schematic view of symmetric n-channel R_DGJLFET.

Moreover, we have followed the described sequence of steps in Silvaco TCAD also and the resulting 3-D cross-sectional view of symmetric R_DGJLFET is shown in Figure A2. In Figure A2, the gate and source/drain electrodes have been enlarged deliberately than their respective sizes in the device to have a clearer view of contacts.

List of publications

SCI Journal Papers:

Published

1. Sandeep Kumar, Arun Kumar Chatterjee and Rishikesh Pandey, "Performance analysis of gate electrode work function variations in double-gate junctionless FET," *Silicon*, vol. 13, pp. 3447-3459, Oct. 2020. (SCI Journal, **Impact Factor: 3.4, Publisher: Spinger). doi***: https://doi.org/10.1007/s12633-020-00774-x*

2. Sandeep Kumar, Arun Kumar Chatterjee and Rishikesh Pandey, "Performance enhancement of recessed silicon channel double gate junctionless field-effect-transistor using TCAD tool," *Journal of Computational Electronics*, vol. 20, pp. 2317-2330, Sept. 2021. (SCI Journal, **Impact Factor: 2.1, Publisher: Spinger). doi**: *https://doi.org/10.1007/s10825-021-01774-9*

3. Sandeep Kumar, Arun Kumar Chatterjee and Rishikesh Pandey, "Study of digital/analog performance parameters of misaligned gate recessed double gate junctionless field-effect-transistor for circuit level application," *Semiconductor Science and Technology*, vol. 37, no. 4, pp. 045017-1-045017-17, March, 2022. (SCI Journal, **Impact Factor: 1.9, Publisher: IOP). doi**: *https://doi.org/10.1088/1361-6641/ac579d*

4. Sandeep Kumar, Arun Kumar Chatterjee and Rishikesh Pandey, "Design and analysis of recessed double gate junctionless field-effect-transistor based digital standard cells," *Silicon*, vol. 14, pp. 11323-11335, April, 2022. (SCI Journal, **Impact Factor: 3.4 Publisher: Spinger). doi**: *https://doi.org/10.1007/s12633-022-01874-6*

Communicated

1. Sandeep Kumar, Arun Kumar Chatterjee and Rishikesh Pandey, "Analytical modeling of recessed double gate junctionless field-effect-transistor in subthreshold region," Submitted for possible publication in International Journal of Numerical Modelling Elecrtonic Networks, Devices and Fields **[Status: Under review]**.
2. Sandeep Kumar, Arun Kumar Chatterjee and Rishikesh Pandey, "Effect of variations in effective oxide thickness on the performance of nanoscale recessed double gate junctionless field-effect-transistor," Submitted for possible publication in ECS Journal of Solid State Science and Technology **[Status: Revision submitted]**.

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